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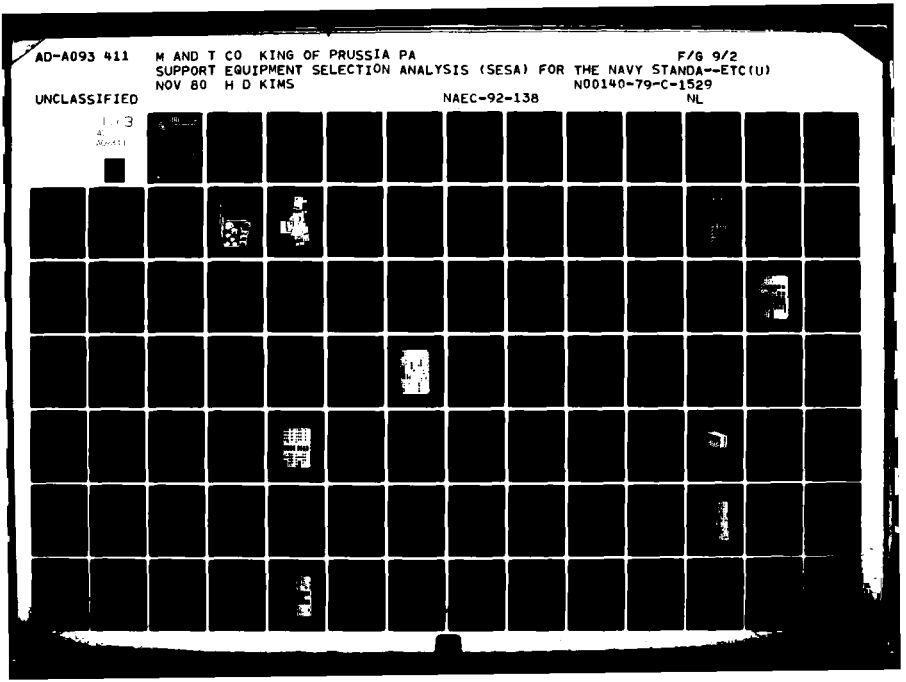

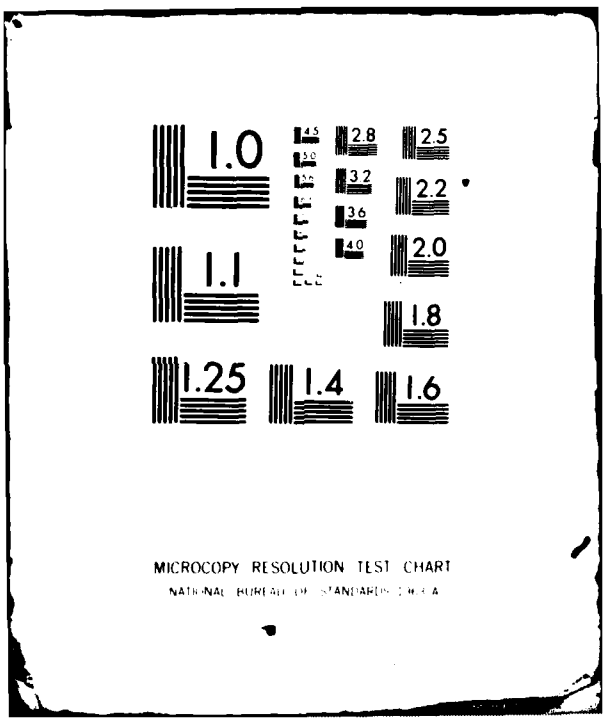
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NAVAL AIR ENGINEERING CENTER

REPORT NAEC-92-138

LAKEHURST, N.J.
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SUPPORT EQUIPMENT SELECTION ANALYSIS (SESA) FOR THE NAVY STANDARD AIRBORNE COMPUTER SET (AN/AYK-14(V))

Avionics Support Equipment Division
Ground Support Equipment Department
Naval Air Engineering Center
Lakehurst, New Jersey 08733

17 NOVEMBER 1980

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SUPPORT EQUIPMENT SELECTION ANALYSIS (SESA) FOR THE NAVY STANDARD AIRBORNE COMPUTER SET (AN/AYK-14(V))

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Automatic Test Equipment (ATE)

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The purpose of the AYK-14 Support Equipment Selection Analysis (SESA) is to determine from a tester-avionics compatibility and/or maintenance cost basis, the optimum support equipment for the intermediate (I) level and depot (D) level maintenance sites. This includes the selection of those avionics requiring Automatic Test Equipment (ATE) support, the actual ATE, and the development of ATE.

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SUMMARY

A. PURPOSE. The purpose of the AYK-14 Support Equipment Selection Analysis (SESA) is to determine, from a tester-avionics compatibility and/or maintenance cost basis, the optimum support equipment for the intermediate (I) level and depot (D) level maintenance sites. This includes the selection of those avionics requiring automatic test equipment (ATE) support, the actual ATE, and the development of ATE.

B. CONCLUSIONS

1. As a weapon replaceable assembly (WRA), the AYK-14 computer system can be configured with as few as 2 shop replaceable assemblies (SRAs) to as many as 16 SRAs. This SESA study involves five Navy programs that will use seven AYK-14 configurations that require I-level maintenance support. A total of 27 SRA types are available for the AYK-14. Six of the SRAs can be tested with standard test equipment while 21 SRAs are to be supported with automatic support equipment.

2. The 5 Navy programs planning to use the AYK-14 computer system will require maintenance support at 30 I-level and 2 D-level sites. However, while workloads at the D-level mandates the use of ATE, the workload at any one I-level site is insufficient to solidly justify ATE procurement to support the AYK-14.

3. Because of its built-in test equipment (BITE) and built-in test (BIT) capability, the AYK-14 as a WRA unit can execute a diagnostic test program which is loaded from a suitcase tester, and fault isolate itself to one SRA 90 percent of the time for over 80 percent of malfunctioning AYK-14s.

4. While all eight of the testers, which were considered for I-level maintenance support, could meet the test requirements of the AYK-14 as a WRA, only two of the seven testers considered for D-level support could meet the SRA test requirements of the AYK-14.

5. A mixed tester support approach was considered to provide the optimum trade-off between tester-avionics compatibility and maintenance cost. This mixed tester approach would include both the suitcase tester and the depot ATE for I-level support. One type ATE planned for the I-level sites in support of other avionic test requirements will also be used to support the AYK-14. No ATE is to be procured to support only the AYK-14 at the I-level because the site workload, the WRA test requirements, and the life cycle costs involved cannot justify ATE for the exclusive support of the AYK-14.

C. RECOMMENDATIONS

1. The optimum trade-off between AYK-14 test requirements and maintenance support costs for I-level maintenance indicates that a mixed tester support approach should be used:

a. At the 23 I-levels that will have the USM-429 (CAT III-D) tester (due to workloads other than the AYK-14), this same tester will be used to support the AYK-14 WRA maintenance workload.

b. At the remaining seven I-levels that will not have the USM-429 testers, the ASM-607 memory loader verifier will be used to support the AYK-14 WRA maintenance workload.

2. In order for the ASM-607 to be effective as a WRA tester, a diagnostic test program is required. It is recommended that the diagnostic test program designed by the Control Data Corporation (CDC) for the AN/ASM-18 loader-verifier be adapted to operate on the ASM-607 and that appropriate software and hardware interface between the ASM-607 and the AYK-14 be procured by the NAVAIRSYSCOM.

3. Because the AN/ASM-607 (suitcase automatic tester) is relatively new and because modification to the CDC diagnostic test program is required, it is recommended that this hardware and software be used by CDC during the Reliability Improvement Warranty (RIW) program of contractor maintenance support prior to the Navy support date (NSD).

4. In order to meet the stringent SRA test requirements and heavy workloads at the D-level, it is recommended that two USM-429, CAT III-D testers be procured for depot support of the AYK-14.

5. In order to gain the maximum utilization from the mixed tester approach, which is proposed for I-level AYK-14 support, it is recommended that the present AYK-14 maintenance philosophy be modified as follows:

> When the USM-429, CAT III-D tester is used at I-level, the maintenance approach should permit repair of the AYK-14 to the replaceable component or part level rather than to only the SRA level. This is especially true when the I-level is on a carrier, where repair is presently performed at the component or part level on similar avionics.

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I. INTRODUCTION

A. BACKGROUND

1. The Navy has designated the AN/AYK-14(V) as the standard airborne computer set. This computer set is presently being considered for use in 18 Navy programs. The design selected by the Naval Air Systems Command (NAVAIRSYSCOM) for the AYK-14 is intended for a wide range of airborne missions. The AYK-14 is a subset of a recently developed Control Data Corporation (CDC) 480 computer. CDC is in the final phase of developing the AYK-14 for the Navy.

2. This computer set uses advanced functional circuitry and modular hardware design with built-in test equipment (BITE) and built-in test (BIT) firmware. In addition, the AYK-14 design utilizes the latest techniques of large-scale integration (LSI). Ultimately, many of the AYK-14's design techniques will find their way into other avionics designs over the next ten years.

3. The computer set can be configured in one of two basic chassis, with a third chassis for memory expansion if required. Figure 1 shows the AYK-14 in the XN-2 chassis configuration. The computer set is flexible in its configuration arrangement of shop replaceable assemblies (SRAs) and can range from a minimum configuration containing only 2 SRAs to an expanded configuration that contains 16 SRAs and provides a full mini-computer capability.

4. While 18 Navy programs could utilize the AN/AYK-14(V), the following 5 are considered firm and are the only programs considered in this SESA:

F/A-18

LAMPS

AV-8B

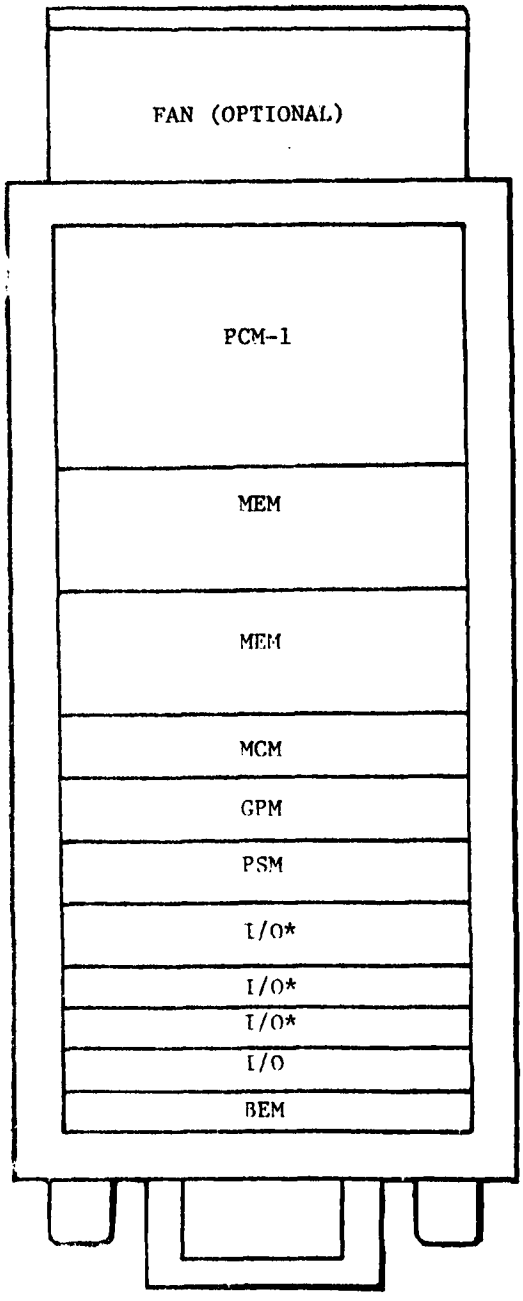
EA-6B

FIREBRAND

These five programs use seven separate computer configurations. All seven configurations were evaluated for support in the SESA.

5. The complete complement of available electronics for the AYK-14 includes 27 SRAs. Twenty-one SRAs are designated for automatic testing. The six remaining SRAs are relatively simple and can be tested with standard test equipment (STE) and would not require the expensive development of test program sets (TPSs). In addition, the two power supply SRAs each contain five sub-SRAs which are also designated for automatic testing.

6. The 5 Navy programs that were included in this SESA will require 30 intermediate (I) maintenance sites and 2 depot (D) level sites. While the five Navy programs included in this study represent firm programs using the AYK-14, the Navy anticipates extensive application of its standard airborne computer set in future Navy programs. It is anticipated that in the future most of the Navy's I-level maintenance sites will eventually require support of the AYK-14.



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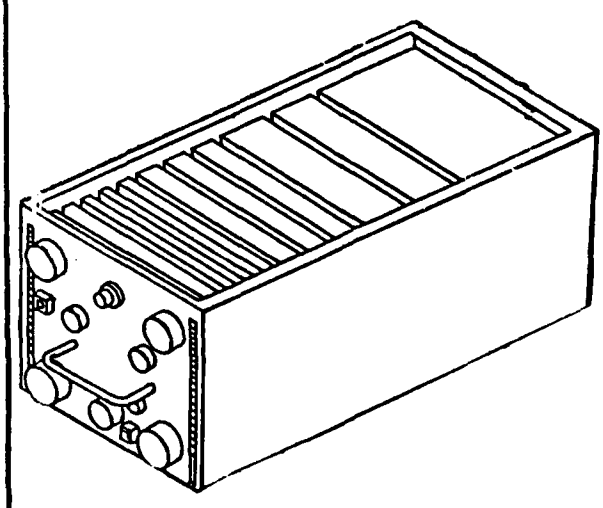


Figure 1 - AN/AYK-14(V) Computer Set (XN-2 Configuration)

B. SUPPORT EQUIPMENT SELECTION ANALYSIS (SESA) SUMMARY

1. AVIONICS TEST REQUIREMENTS ANALYSIS. The individual AN/AYK-14 SRAs were analyzed to determine their test requirements. Of a total of 27 SRAs, 6 were judged not candidates for automatic test equipment (ATE) because they were very simple units that could be tested easily with manual test equipment and because they were not cost effective for ATE testing. The 21 SRAs that were candidates for ATE were primarily digital SRAs. There are 19 digital SRAs and 2 analog SRAs with 6 unique sub-SRAs. Six of the 19 digital SRAs utilize LSI.

2. TESTER CAPABILITY STUDY. The tester capability study considered eight testers as viable candidates for the AYK-14 maintenance support. All testers except item h are in the ATE inventory, fully logistically supported. Item h should be in the ATE inventory prior to AYK-14 deployment.

a. AN/ASM-607, Memory Loader/Verifier

b. AN/USM-429, CAT III-D

c. AN/USM-403, HATS

d. AN/USM-449, AAI-5565

e. AN/USM-453, DIMOTE II

f. AN/ASM-608, NSTS

g. AN/USM-247, VAST

h. MINI-VAST Tester (F-18 Program)

3. TESTER AVIONICS COMPATIBILITY ANALYSIS. Each of the tester's capabilities was compared with the AYK-14's test requirements. Any tester deficiencies were related by a compatibility factor (B), which was reflected as an increase in TPS development costs. Testers with the lowest compatibility resulted in the highest TPS costs.

4. TESTER WORKLOAD ANALYSIS. The workload analysis included three areas:

a. Prior tester workload

b. Projected AN/AYK-14 workload

c. Determining tester utilization

5. LIFE CYCLE COST AND IMPACT ANALYSIS

a. The life cycle cost and impact (LCCI) analysis brings together all the predictable cost elements associated with the AN/AYK-14 support. These costs include nonrecurring or development costs, recurring or site start-up costs, and sustaining costs for a ten-year period.

b. The following testers, in order of cost ranking, were determined by the LCCI analysis for I- and D-level support of the AYK-14:

I-LEVEL SUPPORT LCC ($K)		D-LEVEL SUPPORT LCC ($K)	
AN/ASM-607	7,780	AN/USM-429 (CAT III-D)	7,334
AN/USM-429 (CAT III-D)	17,944	AN/USM-247 (VAST)	9,175
AN/USM-453 (DIMOTE II)	23,660	AN/USM-449 (AAI-5565)	9,788
AN/USM-403 (HATS)	40,588	AN/ASM-608 (NSTS)	9,857
AN/ASM-608 (NSTS)	49,586	AN/USM-403 (HATS)	10,017
AN/USM-449 (AAI-5565)	57,577	AN/USM-453 (DIMOTE II)	11,746
MINI-VAST	93,666	MINI-VAST	15,299
AN/USM-247 (VAST)	173,567		

c. On a life cycle cost basis for I- and D-level maintenance support, a combined or mixed tester support approach is recommended. The two lowest cost candidates for I-level (ASM-607 and USM-429 (CAT III-D)), and the lowest cost candidate for D-level (USM-429 (CAT III-D)) were combined as follows:

TYPE	QTY	COST ($K)
AN/ASM-607	7	1,747
AN/USM-429	23	7,303
TOTAL	30	9,050

The combined approach utilizes 23 previously planned USM-429 (CAT III-D) testers to maximize the I-level test capability and to minimize spares, and uses the ASM-607 at the remaining 7 I-level sites where ATE is not planned. For I-level comparison, the $9,050K combined cost could be justifiably decreased to $5,861K if the CAT III-D weapon replaceable assembly (WRA) TPS costs (nonrecurring and sustaining) are included in the depot costs (rather than being included in I-level costs). The WRA TPS costs at I-level then become:

TYPE	QTY	COST ($K)
AN/ASM-607	7	1,747
AN/USM-429	23	4,114
TOTAL	30	5,861

The WRA TPSs are required for depot support and will also be used at I-levels that have the CAT III-D tester.

6. TECHNICAL RISKS

a. When the required testers and support software are not actually in service within the fleet, then a technical risk exists. When a tester does exist, a technical risk exists which is proportionate to the degree of incompatibility between the avionics test requirements and the tester's capability.

b. For AYK-14 support at I-/D-level, the ASM-607/USM-429 in combination offer the lowest technical risk for the following reasons:

(1) Highest technical compatibility

(2) Both presently in Navy inventory

(3) WRA and SRA test program sets for the USM-429 have lowest technical complexity.

c. The USM-429 has commonality of utilization as a WRA tester at I-level as well as a WRA and SRA tester at the D-level.

II. AVIONICS TEST REQUIREMENTS ANALYSIS

A. GENERAL. The avionics test requirements analysis (TRA) addresses the test requirements of the AYK-14 as a WRA (Figure 2) and its individual SRA modules (Figure 3). The objective of the TRA is to define the WRA and SRAs test requirements envelope in relation to the maintenance philosophy. This section includes three parts:

- o System architecture of the AYK-14
- o Maintenance philosophy
- o Technical description of the SRAs and sub-SRAs

1. SYSTEM ARCHITECTURE

a. The system architectural philosophy for the AN/AYK-14(V) is based on the following key features:

- o The architecture and instruction set is upwardly compatible with that of the AN/UYK-20 computer system, permitting the adaption and use of existing AN/UYK-20 support software.
- o The AYK-14's hardware is functionally partitioned into pluggable modules or SRAs. These modules are the standard building blocks used in configuring functionally large or small computer systems.
- o Intermodule communications are standardized via uniform internal bus structures, thus permitting reconfiguration and addition of new SRAs without impacting the basic computer.

b. These combined system architecture features permit the configuring of specific AN/AYK-14 computers to meet the processing requirements of a wide variety of military systems.

c. A system block diagram of the AYK-14 is presented in Figure 4. The major individual subsystems of the computer system (within the dashed lines) are:

- o Processing Subsystem
- o Memory Subsystem
- o Input/Output (I/O) Subsystem
- o Power Subsystem

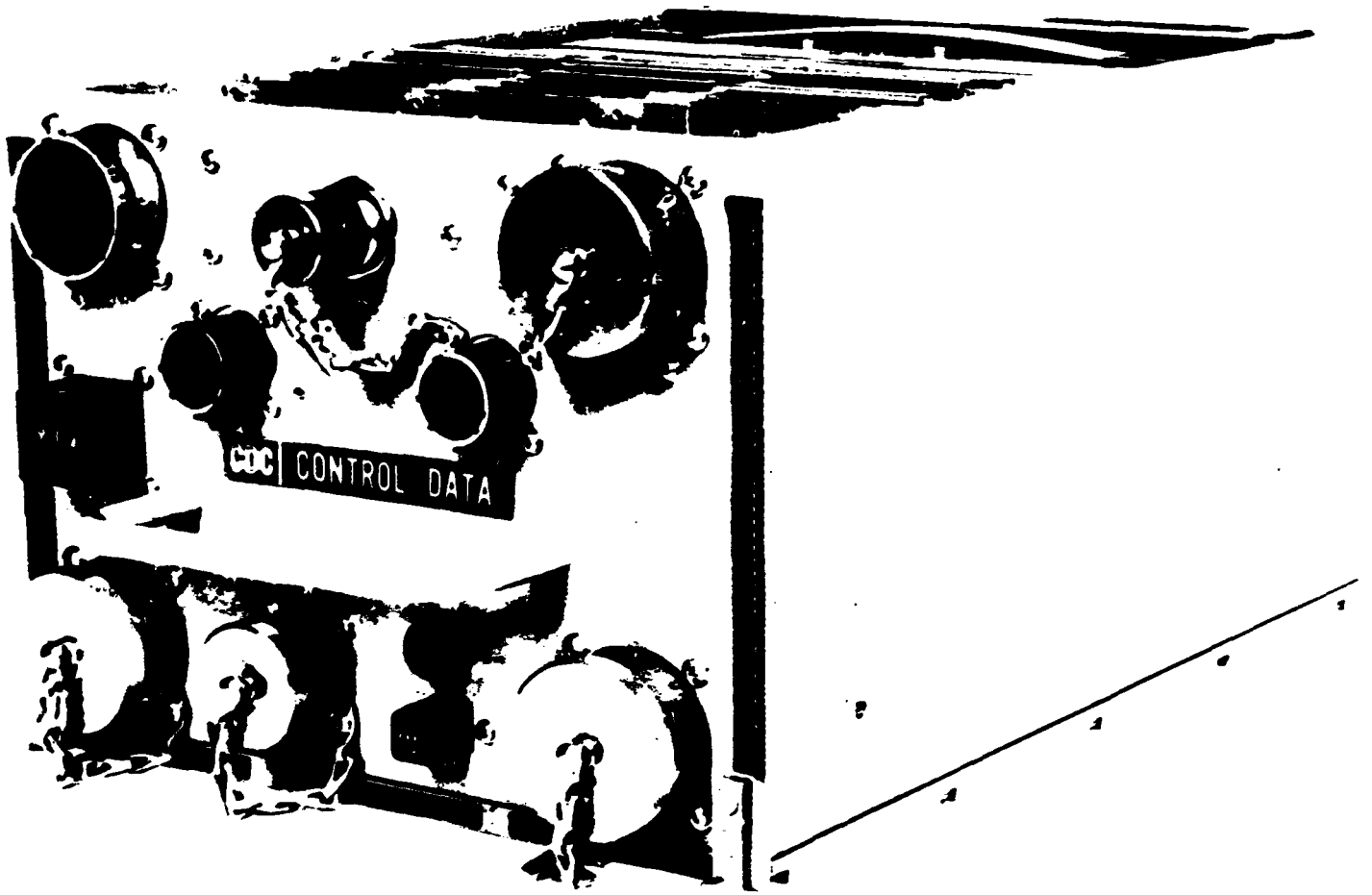


Figure 2 - Navy Standard Airborne Computer (AN/AYK-14(V))

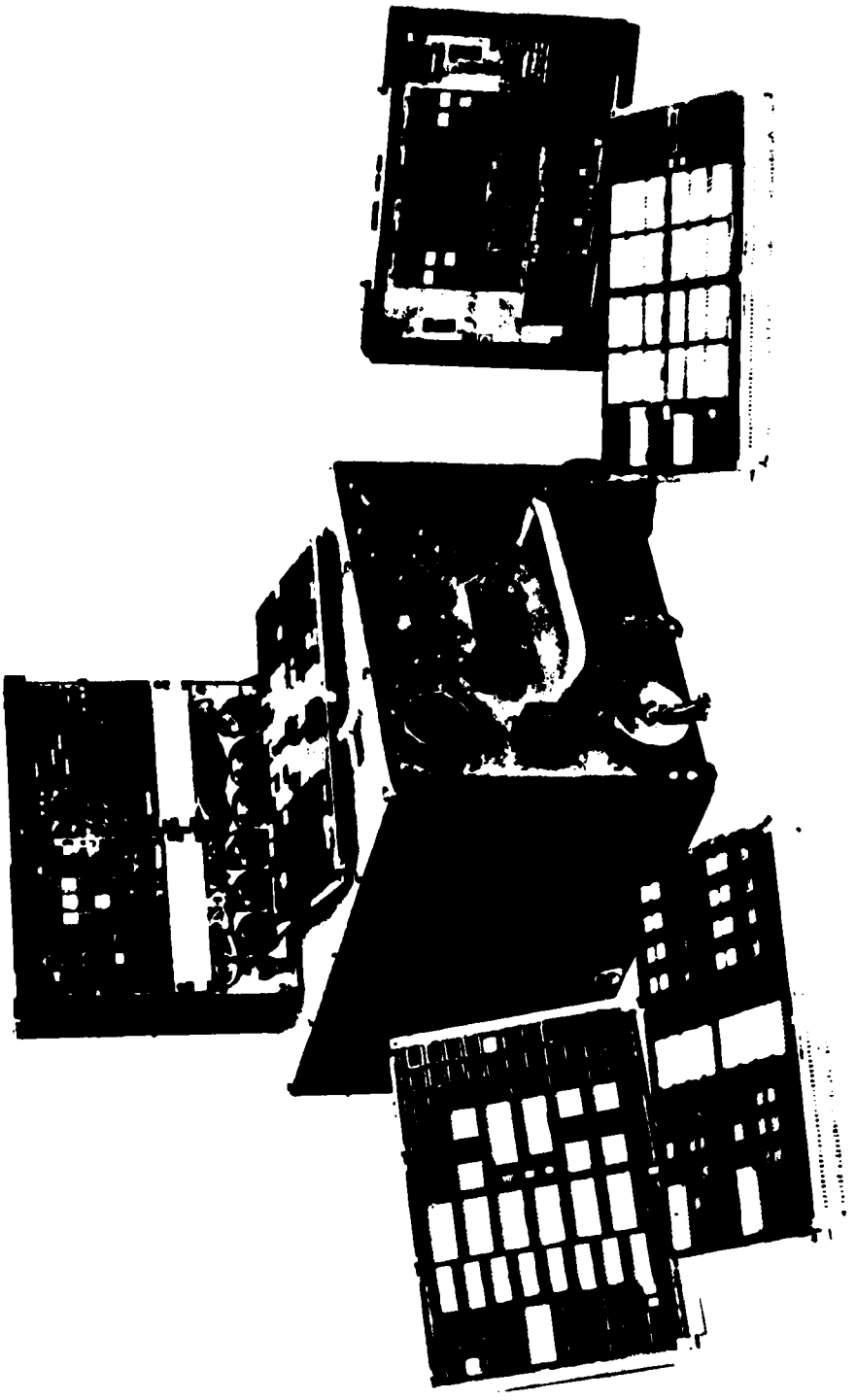


Figure 3 - AN/AYK-14(V) with Several Pluggable Modules

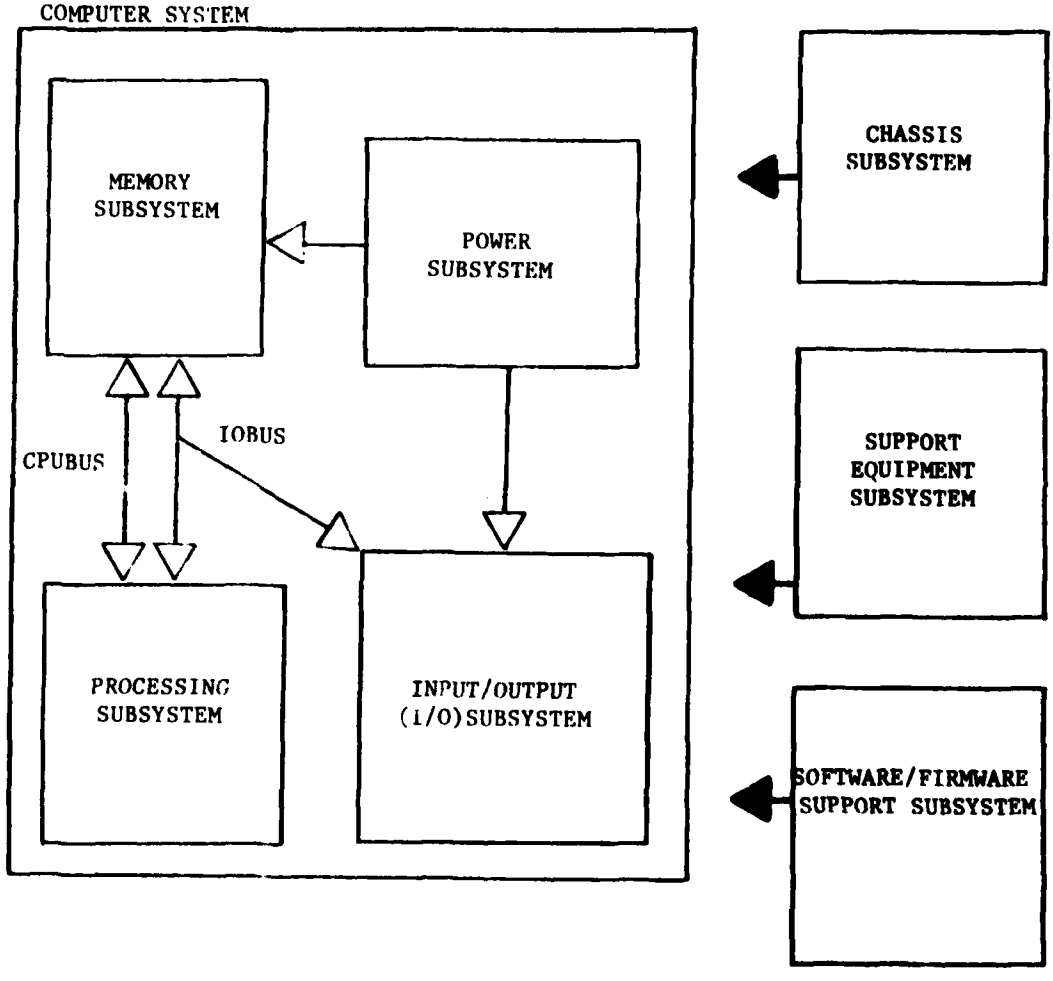


Figure 4 - AN/AYK-14(V) System Block Diagram

These four subsystems are interconnected via the intermodule bus communications (CPU bus, I/O bus), etc. The subsystem clock items noted within, are the SRA modules which can be configured for the subsystem. The three external subsystems noted in Figure 4 are:

- o Chassis Subsystem
- o Support Equipment Subsystem
- o Software/Firmware Support Subsystem

d. First we will discuss the computer system and its four subsystems. This will be followed by a discussion of the chassis subsystem and the software/firmware support system. The support equipment subsystem will be discussed in Section III.

2. MAINTENANCE PHILOSOPHY

a. The AN/AYK-14(V) standard airborne computer set maintenance baseline definition, as stated in the level of repair analysis (LORA) report G13672 dated June 1977, is as follows:

o "Organizational": Detect/isolate via built-in test equipment (BIT/BITE) to Weapon Replaceable Assembly (WRA); remove/replace WRA.

o "Intermediate": Fault isolate (via loader/verifier, selected ground support equipment (GSE), and/or automatic test equipment (ATE) where applicable) to failed shop replaceable assembly (SRA/sub-SRA). Assumed some repairs at intermediate level, with remaining returned to depot. Final maintenance concept will be determined upon completion of the final LORA.

o "Depot": Fault isolate SRA/sub-SRA to failed component(s), remove/replace component(s), and return item to supply for reissue to using organization. Depot verification and testing utilized ATE, and repair action utilized common support equipment, plus ATE interface device.

b. The above maintenance baseline can be further clarified as presented graphically in Figure 5. When a malfunction occurs in the AN/AYK-14(V) while still in an aircraft, the resident BIT program detects the fault and identifies it on a GO/NO-GO fault indicator on the front of the computer set chassis. When the hardware fault warning interrupt occurs, the in-flight performance monitoring (IFPM) program processes the interrupt by testing the CPU (general processing module (GPM) and processor support module (PSM) SRAs) and the memory interface (MCM SRA). After the malfunction is verified by the IFPM, the AN/AYK-14(V) computer set is removed from the aircraft as a WRA and replaced with a properly functioning WRA. This maintenance action takes place at the organizational maintenance level.

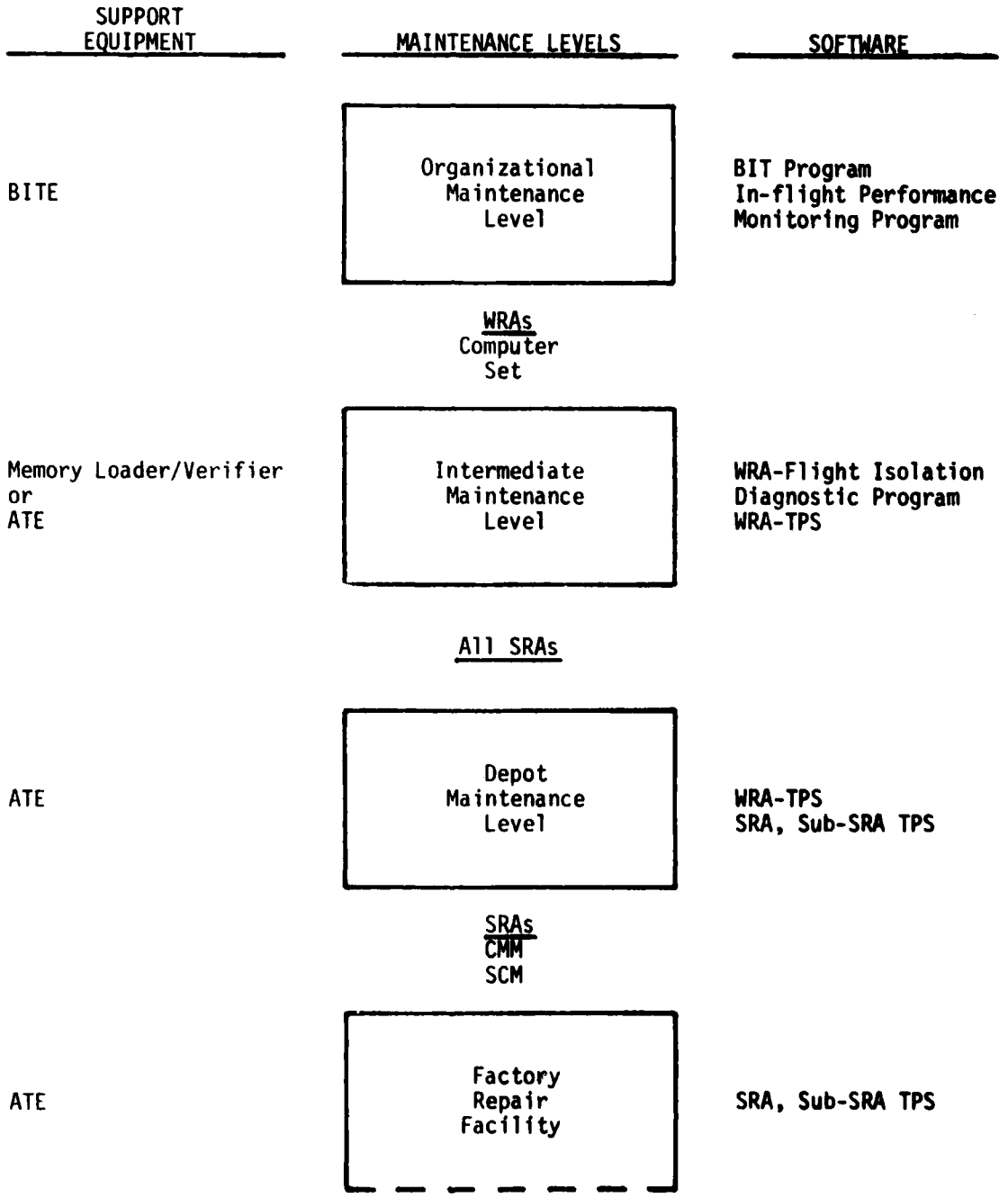


Figure 5 - AN/AYK-14(V) Maintenance Baseline

c. The faulty WRA is sent to the intermediate I-level maintenance facility where the malfunction in the WRA is isolated to the malfunctioning SRA or sub-SRA, depending on the I-level support equipment capability. This maintenance action can be accomplished in three steps. The AN/AYK-14(V) can be used to test itself in conjunction with a memory loader/verifier (MLV) unit, or with ATE to isolate faults to the SRA/sub-SRA level through the fault isolation diagnostic (FID) test program. Once the malfunctioning SRA/sub-SRA is isolated, the WRA cover is removed and the failed SRA/sub-SRA is removed by the release of the SRA wedge-lock fasteners. The SRA/sub-SRA is replaced with a spare, and the FID test program is again performed by the AN/AYK-14(V) to verify proper WRA operation. The computer set is now ready for return to the organizational level. Those I-level maintenance facilities that have ATE will be capable of SRA/sub-SRA repair to the component level for most of the SRA's depending on the ATE test capability. The present AYK-14 maintenance philosophy does incorporate the utilization of component repair at the I-level. Present I-level maintenance on board carriers does not utilize SRA component repair capability of ATE for similar electronics.

d. Possible exceptions to SRA I-level repair would be memory control module (MCM), core memory module (CMM), and semiconductor memory module (SMM) SRAs. Those I-level maintenance facilities without an ATE capability would forward the malfunctioning SRAs/sub-SRAs to the depot maintenance facility for repair. After repair at the depot, SRAs/sub-SRAs would be returned to the I-level facilities for reissue in WRAs to the organizational level as required. Due to the importance of operation and difficulty in testing memories, it may be necessary that memory SRAs (CMM and SMM) be repaired at the manufacturer's facility.

B. COMPUTER SYSTEM. The computer system is composed of four subsystems: processing, memory, input/output, and power. These subsystems contain 21 different types of SRAs or modules. The computer subsystems and their SRAs are discussed next.

1. PROCESSING SUBSYSTEM. This subsystem is contained in three SRAs. The general processing module (GPM) contains all the microprogrammed control arithmetic unit, registers, and bus interfaces. The processor support module (PSM) contains the supporting elements such as micromemory, real-time clocks, bootstrap memory, bus interface, and event (interrupt) logic required to complete the function of the GPM. Together the GPM and the PSM SRAs form a 16-bit central processing unit (CPU) of a general-purpose computer. The extended arithmetic unit (EAU) provides a high-speed, 32-bit floating-point hardware, and operates under the control of the GPM.

2. MEMORY SUBSYSTEM. The memory subsystem includes various combinations of three SRAs. The memory subsystem includes interchangeable 16K- and 32K-word core memory modules (CMM) and 16K-word semiconductor memory modules (SMM) with 18-bit word length. The CMM cycle time is 900 nanoseconds, and the SMM cycle time is 400 nanoseconds. The memory control module (MCM) interfaces between the GPM and the memory modules (CMM or SMM). The MCM has both CPU bus and I/O bus interfaces which permit the GPM to use one bus for instruction access and the other for operands to enhance effective access time. The MCM also provides two channels to memory modules, the OMEMBUS and EMEMBUS, which can increase effective access time through interleaved address between two memory banks.

3. INPUT/OUTPUT SUBSYSTEM

a. The AYK-14 system organization provides up to 16 input/output (I/O) channels, each on individual SRAs which communicate with the processing subsystem via the IOBUS. The standardization of interval interfaces permits any I/O channel module type to be interchanged in the chassis I/O slots by simple plug-in replacement. Available chassis provide from four to six I/O channels, including the discrete interface module (DIM). Expansion to more I/O channels is possible but requires the additional memory expansion unit (MEU) type enclosures. Ten types of input/output interface SRAs are available to match standard I/O channel characteristics. These are:

- o Discrete Interface Module (DIM)
- o Serial Interface Module (SIM)
- o NTDS Interface Module (NIM)

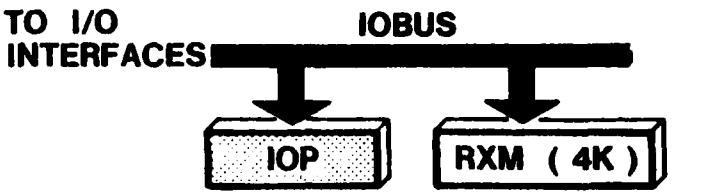
- o RS-232-C Interface Module (RIM)
- o PROTEUS Interface Module (PIM)
- o Input/Output Processor (IOP)
- o Bus Extender Module (BEM)
- o Read/Write Expandable Module (RXM)
- o PIC/POC/SDC Module (PPSM)
- o Discrete Input/Output Module (DIOM)

b. The input/output controller (IOC) functions can be executed by either the CPU (GPM and PSM) or the optional I/O processor (IOP). The IOP, operating in conjunction with the CPU, greatly enhances the processing throughput of the AYK-14. The IOP combines the basic function of a CPU in one module with a reduced instruction set and performance level. The IOP is microprogrammed to serve either as an IOC or as a single-module, 16-bit, general-purpose CPU without modification. Special I/O channel configurations may be added as required without modifications to backpanel wiring, internal interfaces, or microcode. This is an important feature of the AYK-14, since a principal problem area in military system applications involves accommodating special equipment and sensor interfaces.

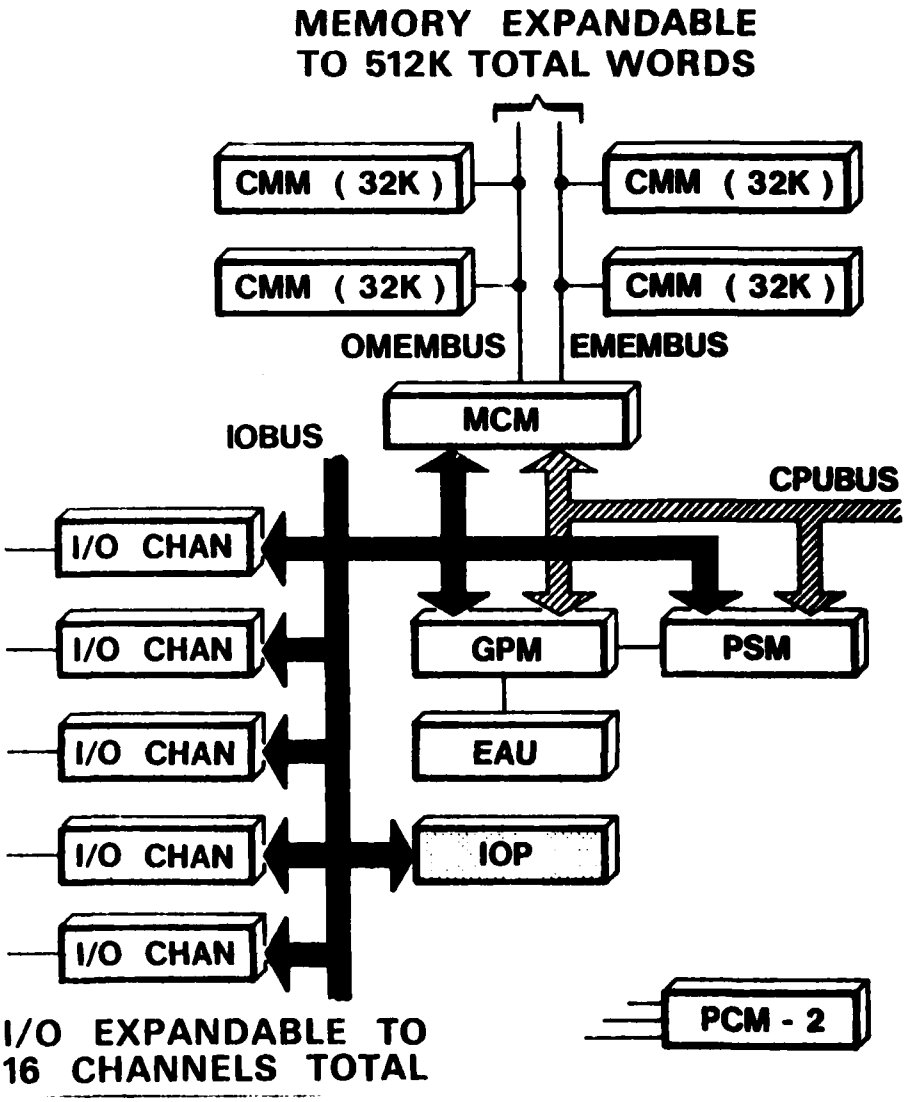
4. POWER SUBSYSTEM. Power for all SRAs in a chassis or enclosure is supplied by a Power Converter Module (PCM) with appropriate regulated voltage and current capabilities. At present there are two types of PCMs. Only one PCM is used in any one AYK-14 computer system. Each PCM includes five sub-SRAs. PCM-1 provides approximately 390 watts of output power; and power, 115-VAC, 400 cycle, three-phase, Wye-connected.

5. COMPUTER SYSTEMS CONFIGURATION

a. The functional partitioning of the 27 SRAs and the internal bus structures provide for a flexible configuration of a wide range of AYK-14 computer systems. The computer system configurations allow for the building up of a system by the addition of SRAs to meet each weapon system's computing bandwidth and capacity requirements. For example, Figure 6 shows the minimum AYK-14 computer configuration, which consists of a 16-bit input/output processor (IOP) and a read/write expandable module (RXM) of 4K by 18-bit random access semiconductor memory with the option of adding a 4K PROM. This minimum configuration computer system assumes that the SRA modules are incorporated as part of the user's equipment. The user's equipment would also supply the required regulated 5 Vdc power for the SRAs and also provide the input/output adapter to the IOBUS interface. This minimum configuration can also be used as a computing element in a distributed computer processing system.



Minimum Configuration



Expanded Configuration (XN-1)

Figure 6 - Two Configurations of
The AN/AYK-14

b. An expanded computer system configuration (Figure 6) also provides a complete 16-bit, general-purpose computer with high-speed floating point hardware, hardware I/O controller (IOC), 128K words of 18-bit core memory (CMM), and up to 16 I/O channels of various types.

C. CHASSIS SUBSYSTEM. All SRA modules plug into an ATR-type chassis equipped with slots to accommodate a combination of SRA types. Currently three standard chassis types designed for MIL-E-5400, class II environments are available for 16-bit computers. Figures 7, 8, and 9 show the three chassis types along with the module configurations available for each. Connector locations, basic dimensions, weight and power are shown. It should be noted that the MEU (Figure 9) is an extension unit to be used with the XN-1 (Figure 7) or XN-2 (Figure 8) chassis to provide additional memory, processing, and/or I/O capability. Mulitple MEU chassis can be used to further expand the system. In addition, chassis for specific weapon systems may require modifications to the three basis chassis. In this case a modified XN-1 chassis would be designated XN-1A, B, or C, etc.

D. SOFTWARE/FIRMWARE SUPPORT SUBSYSTEM. The basic approach to software support for the AYK-14 is to preserve existing operational and support software developed for the AN/UYK-20 computer system. The AYK-14 computer executes an instruction set which is a compatible extension of the AN/UYK-20 instruction set. The Navy supports both the AN/UYK-20 and the AN/AYK-14 support software. The general approach to AYK-14 software development is to use a commercial host computer (CDC 6000 series) to prepare and transfer the software to the AYK-14 via magnetic tape. Three types of AYK-14 software/firmware support will be discussed:

- o Organizational-level software
- o Intermediate-level software
- o Support software

1. ORGANIZATIONAL-LEVEL SOFTWARE

a. The in-flight performance monitoring (IFPM) programs work with the BITE to insure that the AYK-14 computer system is capable of successfully completing its tactical mission. These program modules are written in MACRO-20 assembly language and are executed in conjunction with the standard real-time executive (SDEX/14) program. The IFPM, which consists of the CPU/memory quick-look test (CMQT), processes the hardware fault warning interrupt generated by the Built-In-Test (BIT) timer. The CMQT performs a test of the CPU (CPM and PSM) as well as the 500 words of ROM memory, takes 8 milliseconds to execute, and runs in an operation mode defined by the user at assembly.

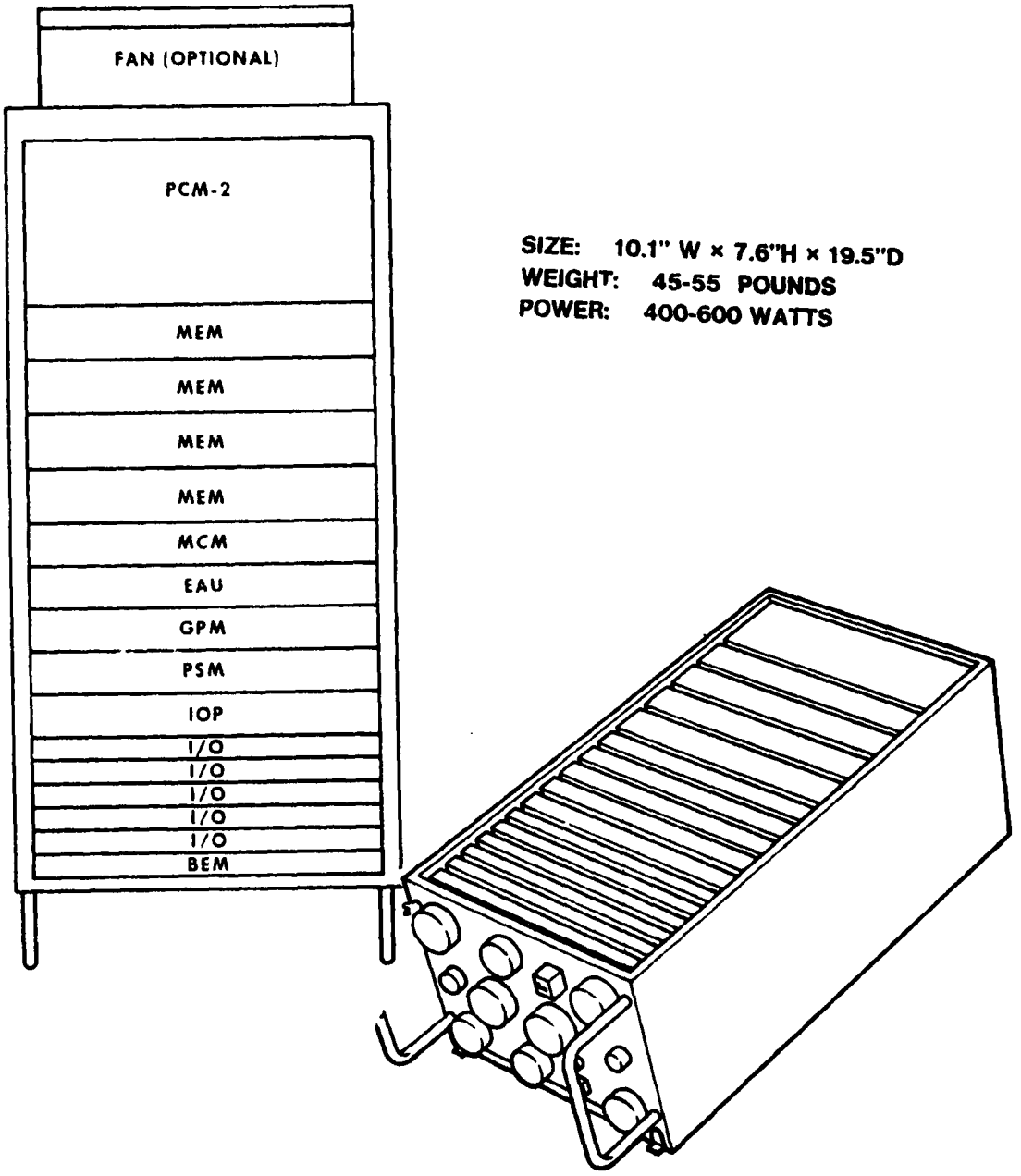
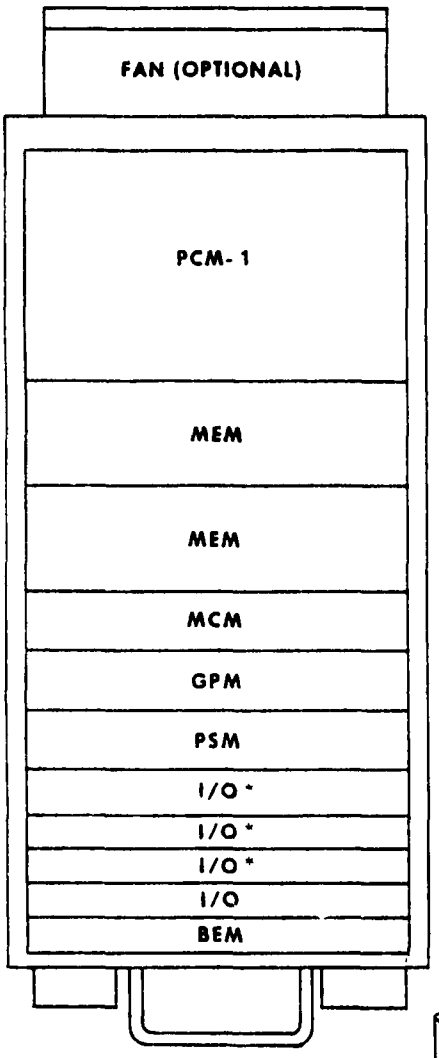


Figure 7 - AN/AYK-14(V) XN-1 Configuration



*serial-type I/O channel

SIZE: 10.1"W x 7.6"H x 14.0"D
WEIGHT: 30-38 POUNDS
POWER: 215-400 WATTS

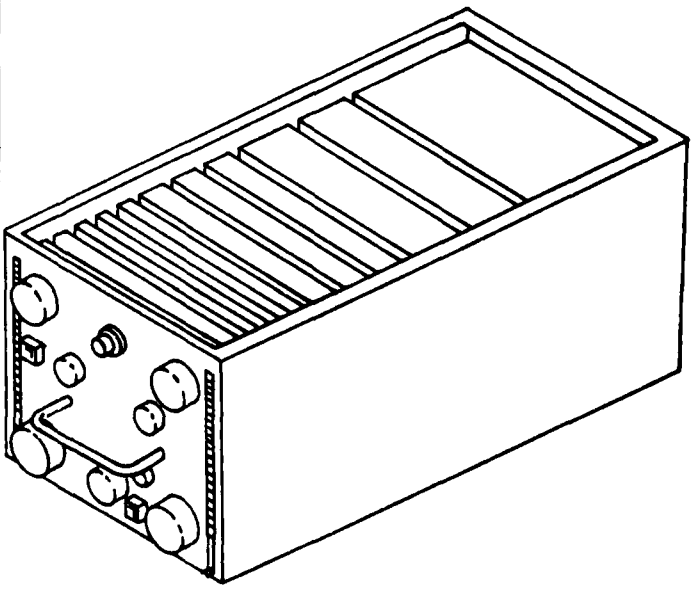
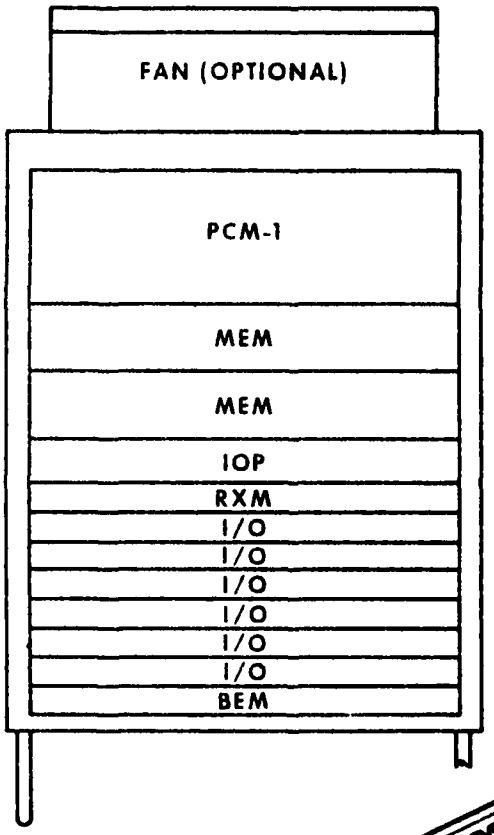


Figure 8 - AN/AYK-14(V) XN-2 Configuration



SIZE: 10.1"W x 7.6"H x 12.7"D
WEIGHT: 28-35 POUNDS
POWER: 150-350 WATTS

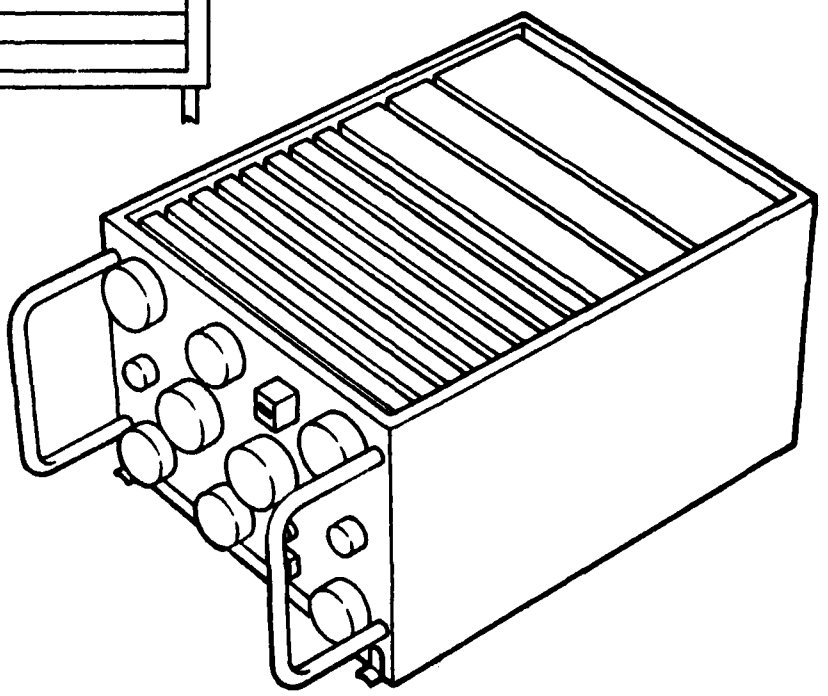


Figure 9 - AN/AYK-14(V) Memory Expansion Unit

b. The IFPM also interfaces to the hardware BITE automatically or as selected. The automatic interface is with the continuous hardware BITE. The functions checked by the BITE are:

(1) Continuous Hardware BITE

- o Memory Parity
- o Memory Protect
- o Memory Channel Time-out
- o Power Monitoring
- o Overtemperature Monitoring
- o Bus Time-outs
- o I/O Channel Parity
- o I/O Channel Time-out
- o SIM Manchester Code Format Verification
- o BIT Timer
- o BIT Indicator

(2) Programmable Hardware BITE

- o I/O Wraparound
- o BIT Firmware
- o Computer Support Interface

c. Additional program modules for the IFPM will contain an I/O test, additional memory tests, and a four-segment CPU test. These features are predicted by CDC to result in detection of 98 percent of the faults in the AYK-14 computer system.

2. INTERMEDIATE-LEVEL SOFTWARE

a. The SRA diagnostics are software programs to detect and isolate hardware failures in the AYK-14 computer set at the intermediate (I) maintenance level. The SRA diagnostic programs are modular and configurable to test all possible AYK-14 computer configurations and to thoroughly test the three major subsystems of the AYK-14 processing subsystem, memory subsystem, and input/output subsystem. At the present time the SRA diagnostic programs are designed to operate on CDC's AN/AYM-18 loader/verifier unit (LVU), and on CDC's computer control unit (CCU). However, the Navy has

designated the AN/ASM-607 memory loader/verifier unit as the O- and I-level support equipment for memory loading and program verification. The following discussion of the SRA diagnostic program assumes that the appropriate software modifications noted above have been completed.

b. The design objective of the SRA isolation diagnostics is to test the operation of the AYK-14 system and detect and isolate faults to one SRA for 95 percent of the detected faults and to two SRAs for 99 percent of the detected faults. The SRA diagnostics consist of a set of tests developed to examine the functions of the individual SRA modules as shown in Figure 10. The SRA Executive (SRA EX 1) interfaces with the ASM-607 and the SRA isolation diagnostics through a series of tests. The diagnostics are organized as follows:

- o SRA CPU Executive Test
- o CPU Test
- o IOP Test
- o Memory Test
- o I/O Tests

c. The diagnostics tests are loaded from magnetic tape on the ASM-607 into the AYK-14. The diagnostic routines are executed in an offline test environment at the intermediate Maintenance shop. During the test procedure, using the ASM-607, the AYK-14 is not connected to any peripheral equipment. However, the I/O functions may be tested by utilizing external wraparound cables. Without the wraparound cable approach, the tests of the I/O modules do not include the tests of the transmitter/receiver circuitry in the I/O SRAs. The full detection and isolation requirements for the SRA isolation diagnostics are achieved through testing in conjunction with the AYK-14's BIT firmware and its BITE hardware.

d. Figure 11 shows an AN/AYK-14 equipment configuration. The SRA diagnostics shall detect and isolate errors in the SRA modules described below:

(1) General Processing Module (GPM). The GPM contains a 48-bit microcommand control register; an arithmetic/logic unit; two register files, each with 256 16-bit words; two memory buses; and the interface to the LVU/CCU.

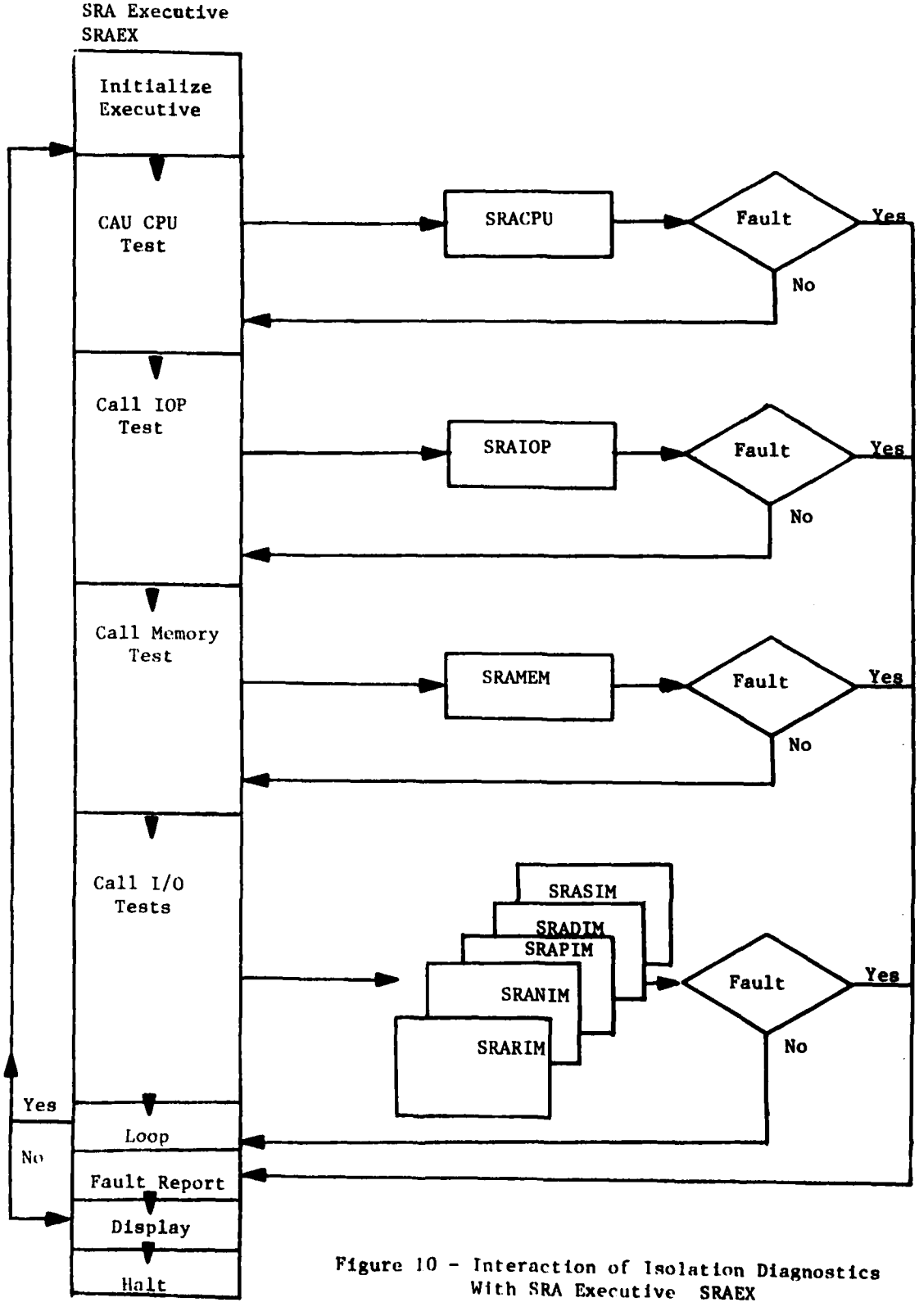


Figure 10 - Interaction of Isolation Diagnostics With SRA Executive SRAEX

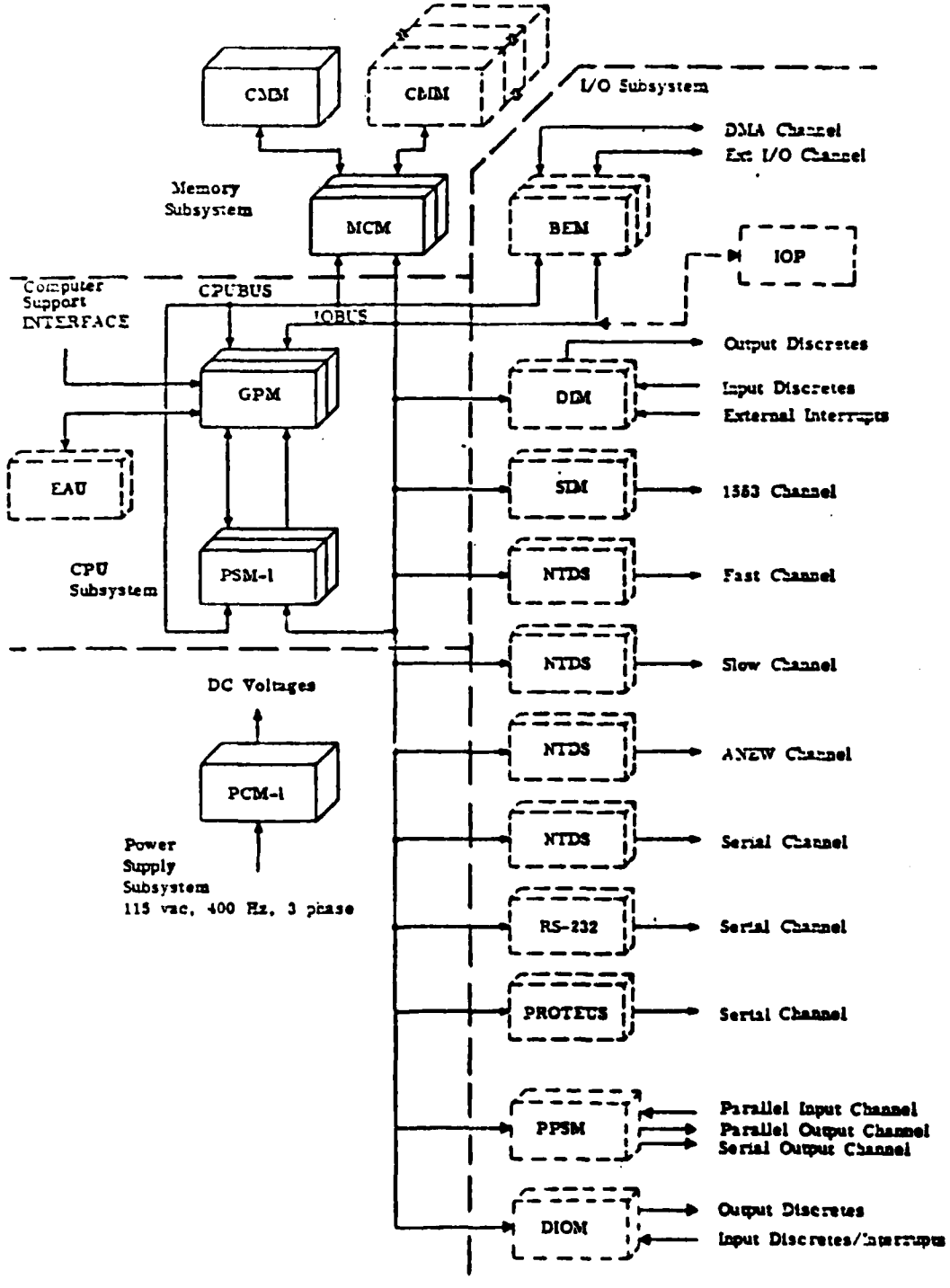


Figure 11 - An AN/AYK-14 System, Block Diagram

(2) Processor Support Module (PSM). The PSM supports the GPM by providing interrupt control, clocks, ROM bootstrap, and micromemory to hold the GPM firmware. The PSM also provides an external bootstrap load discrete and system reset discrete inputs.

(3) Memory Control Module (MCM). The MCM provides the logic needed to interface the GPM to the main memory. This logic transforms the 16-bit relative address received from the GPM into a 19-bit memory address. It also provides the logic for handling the memory protect and parity checking.

(4) Input/Output Processor (IOP). The IOP contains a 48-bit microcommand control register, an arithmetic logic unit, PROMs, a register file with 256 16-bit words, one memory bus, and the interface to the computer support equipment.

(5) Core Memory Module/Semiconductor Memory Module (CMM/SMM). These modules provide the main memory for the CPU system. They contain 18-bit words and are accessed via the MCM.

(6) Bus Extender Module (BEM). The BEM provides external interfaces to the internal buses of the AN/AYK-14.

(7) Discrete Interface Module (DIM). The DIM provides 32 input discretes, 32 output discretes, and 8 external interrupts. The eight external interrupt priorities are setable under software control.

(8) Serial Interface Module (SIM). The SIM provides dual bus interface to a MIL-STD-1553A channel. The SIM provides software selectable bus controller and remote terminal operating modes.

(9) NTDS Slow Channel. The NTDS slow channel provides a Type A parallel interface per MIL-STD-1397.

(10) NTDS Fast Channel. The NTDS fast channel provides a Type B parallel interface per MIL-STD-1397.

(11) NTDS ANEW Channel. This channel provides a Type C parallel interface per MIL-STD-1397.

(12) NTDS Serial Channel. The NTDS Serial Channel provides a serial interface per MIL-STD-1397.

(13) PROTEUS Channel. This channel provides a 10 MHz bit rate serial channel.

(14) RS-232 Channel. The RS-232 Channel provides serial RS-232 asynchronous, selectable baud capability.

(15) PIC/POC/SOC Module (PPSM). The PPSM provides the following three channels:

(a) One parallel input channel (PIC) capable of receiving a data word of 32 bits in length with a maximum word transfer rate of 260K words per second.

(b) One parallel output channel (POC) capable of transmitting a data word of 32 bits in length with a maximum word transfer rate of either 200K or 1M words per second.

(c) One serial output channel (SOC) capable of transmitting a serial NRZ data word of 16 bits in length at a word transfer rate of either 200K or 1M words per second.

(16) Discrete Input/Output Module (DIOM). The DIOM is capable of receiving a combination of 48 discrete inputs/interrupts and transmitting 144 discrete outputs.

(17) Extended Arithmetic Unit (EAU). The EAU consists of a programmable architecture designed to provide high-speed arithmetic algorithms for floating point arithmetic and trigonometric functions. In the AN/AYK-14 computer instruction set, the EAU provides increased CPU performance for floating point arithmetic instructions.

3. SUPPORT SOFTWARE

a. Microcode Cross-Assembler. The microcode cross-assembler is a FORTRAN-coded assembler capable of accepting microcode instruction from source cards and tapes, and of producing program listings and absolute object code onto magnetic tape and disk. This absolute object code is executable by the AN/AYK-14(V). The cross-assembler is capable of assembling a microcode program of at least 4K microcode words. It can be hosted on any computer hosting ANSI standard FORTRAN (version 3.9, 1966) with sufficient memory and two tape units.

b. Microcode Simulator. The microcode simulator provides an independent host capability to enable a user to test the microcode program assembled for dependent host capability to enable a user to test the microcode program assembled for the AN/AYK-14(V). The simulator fully simulates the microcode program assembled for the AN/AYK-14(V). The simulator fully simulates the microcode instruction repertoire, and interrupts, accepts, and executes assembled AN/AYK-14(V) microcode. The simulator requires less than 60K bytes of memory and is coded in FORTRAN. The microcode simulator software is operable on any computer hosting ANSI standard FORTRAN (version 3.9, 1966).

c. Cross-Assembler.

(1) The AN/AYK-14(V) cross-assembler accepts assembly source code in 80-column card images and produces relocated object code. The object code formats are accepted by the loader programs used to link the assembler-produced code for execution.

(2) The cross-assembler recognizes instruction mnemonics for entire AN/AYK-14(V) instruction repertoire, address labels, octal and decimal numeric notation, arithmetic operations (including add, substract, multiply, divide, and binary shift), multiple address counters, and full macro capability.

(3) Cross-assembler instruction mnemonics provide output disposition control, hard copy listing control, symbol definition capability, address counter control and conditional assembly capability.

(4) Input to the cross-assembler consists of:

- o Main program source statements in 80-column card images.
- o Library element source statements in 80-column card images, user-specified as in-line source code assembly.

(5) Output from the assembler consists of:

- o Relocatable object code on punched cards and magnetic tape.
- o Object output code listing with octal and hexadecimal.
- o Source program test listing.

- o Symbol cross-reference listings.
- o Error messages.
- o Symbol table information on the object code output device.
- o User-specified source statements in the object code output stream.
- o User-specified diagnostic source statements in the test listing.

d. CMS-2M Compiler. The CMS-2M complier uses the U.S Navy standard programming language for tactical applications. It produces an object code for the AN/AYK-14(V). The CMS-2M compiler is host computer independent and can operate on a variety of host computers. Typical host computers include the Univac 1108, CDC 6000, IBM 360/370, and PDP 11. Included in the CMS-2M compiler is the system tape generator. The minimum host computer facility must include 65K works of memory and four magnetic tape units.

e. Standard Real-Time Executive (SDEX/14). SDEX/14 is the nucleus of the AN/AYK-14(V) real-time system operating in the AN/AYK-14(V) computer. A computer system is formed and optimized by the addition of site-specific system functions and user modules. Functions of SDEX/14 are: initialization, scheduling, interrupt management, input/output management, and error management.

E. AN/AYK-14(V) SHOP REPLACEABLE ASSEMBLIES (SRAS) AND TEST PARAMETERS

1. GENERAL

a. The SRA modules (Figure 12) of the AN/AYK-14(V) computer are designed for use in MIL-E-5400 (airborne) environment when installed in suitable enclosures. The total range of conditions includes temperatures of -54°C to 71°C, at altitudes to 70,000 feet, and levels of shock, vibration humidity, and EMI appropriate to these environments.

b. All SRA modules are designed for conducting cooling via a heat sink backing the printed circuit boards. The modules have ramp clamps along both short edges to provide solid mechanical and thermal contact to the slots in the chassis. Heat is transferred from the chassis heat sink via an air plenum, which may be supplied by a vehicle cooling air system or optional bolt-on fan. No cooling air is required over SRA components. Figure 3 presents the two basic SRA module configurations: single printed circuit SRA and the double printed circuit SRA.

c. All computer SRA modules except the PCM are 6.48 by 9.00 inches. The GPM, PSM, BEM, MCM, and IOP SRAs are mountable on 0.85-inch centers and weigh approximately 2 pounds each. All I/O SRAs are mountable on 1.45-inch centers and weigh approximately 3.1 pounds each. SRA modules and chassis have a provision for keying to prevent improper SRA insertion into the chassis.

d. The AN/AYK-14(V) SRAs will be discussed in the order of subsystems as follows:

- o Processing Subsystem SRAs: GPM, PSM, EAU
- o Memory Subsystem SRAs: MCM, CMM, SMM
- o Input/Output Subsystem SRAs: DIM, SIM, NIM, RIM, PIM, IOP, BEM, RXM, PPSM, DIOM
- o Power Subsystem SRAs: PCM-1, PCM-2

2. PROCESSING SUBSYSTEM SRAs

a. General Processor Module (GPM)

(1) The GPM (Figure 13) is one double printed circuit board SRA, containing the 48-bit microcommand control, LSI bit-slice arithmetic unit, two register files, two busses, and the LV/CCU interface circuitry. The two circuit boards (A and B) of the GPM are presented in Figures 14 and 15. The GPM block diagram is presented in Figure 16. The GPM contains all the data manipulation hardware and microprogram control architecture for the central processing unit (CPU) and IOC processors. The 48-bit C register holds the current microcommand during execution. The current microcommand controls one machine cycle and also specifies the

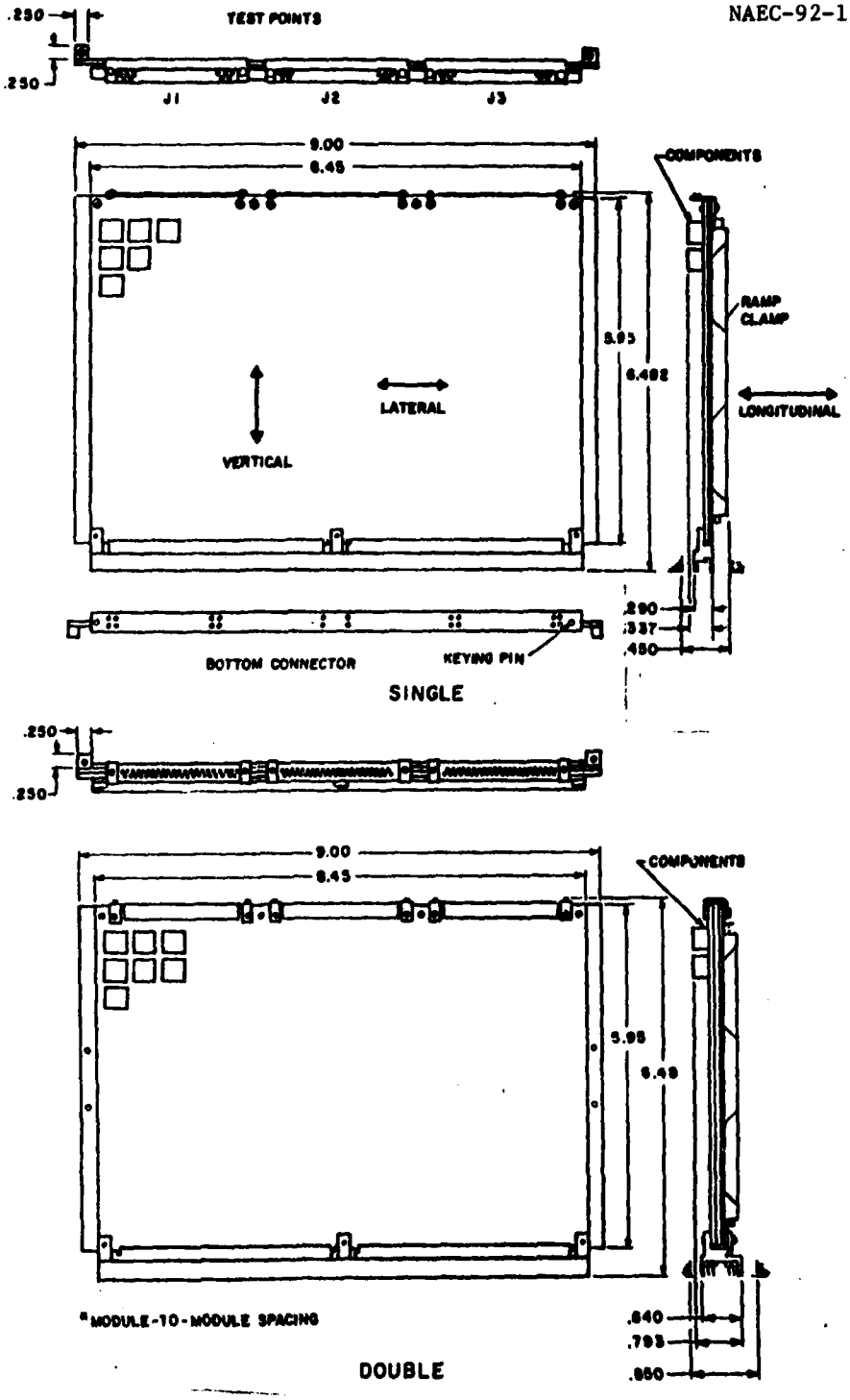


Figure 12 - SRA Module Configurations

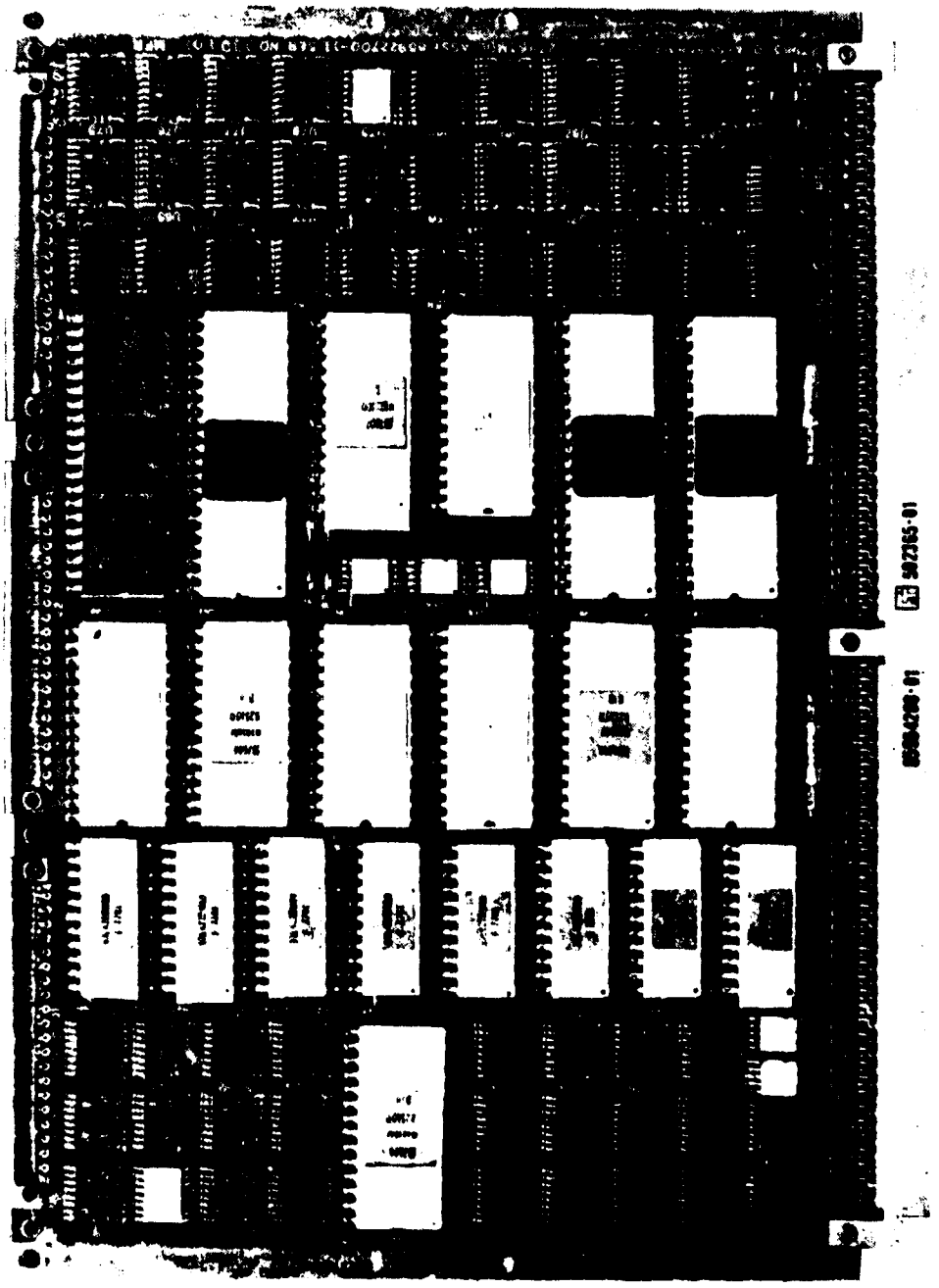


Figure 13 - General Processor Module, Board A

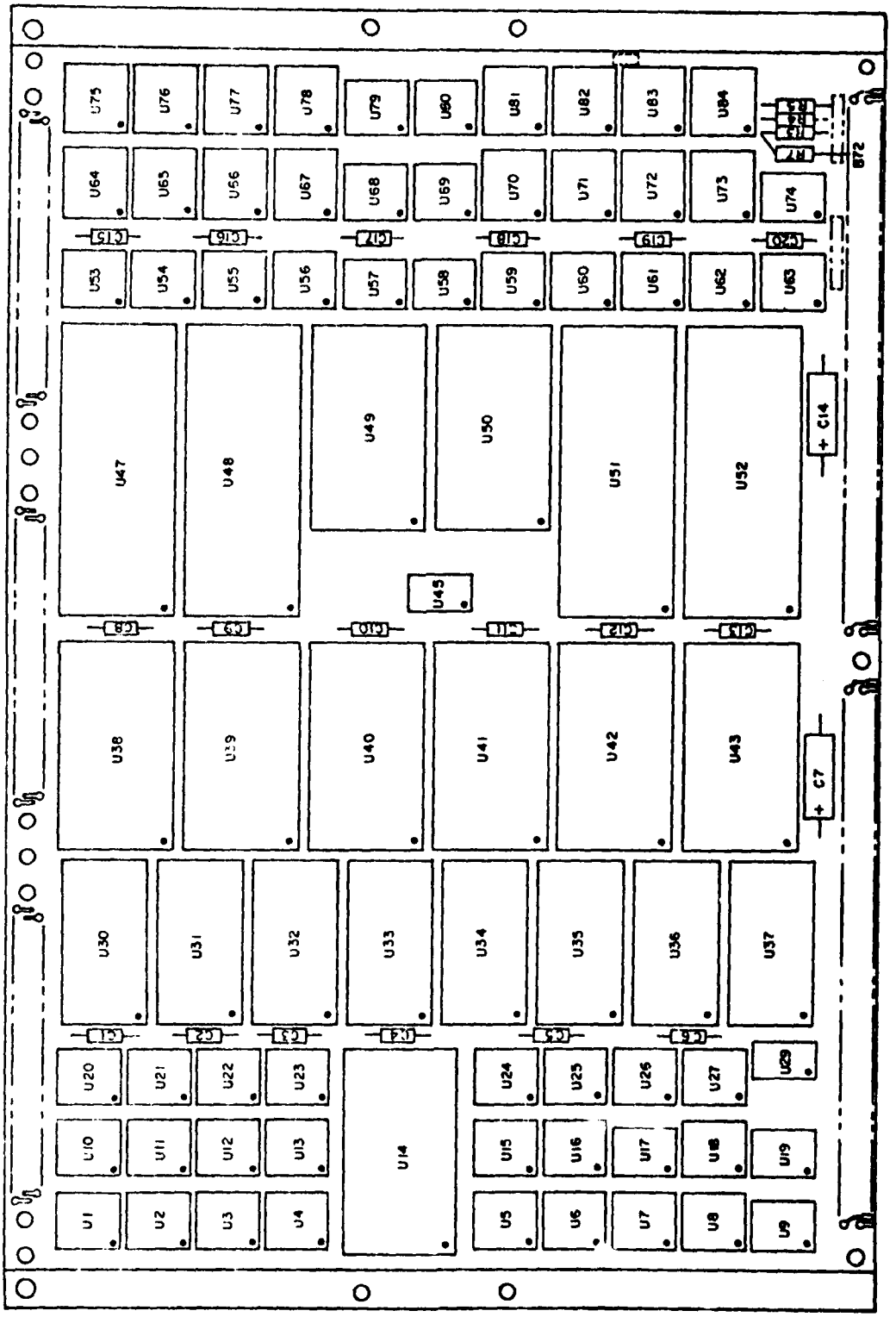


Figure 14 - General Processor Module, Circuit Card A

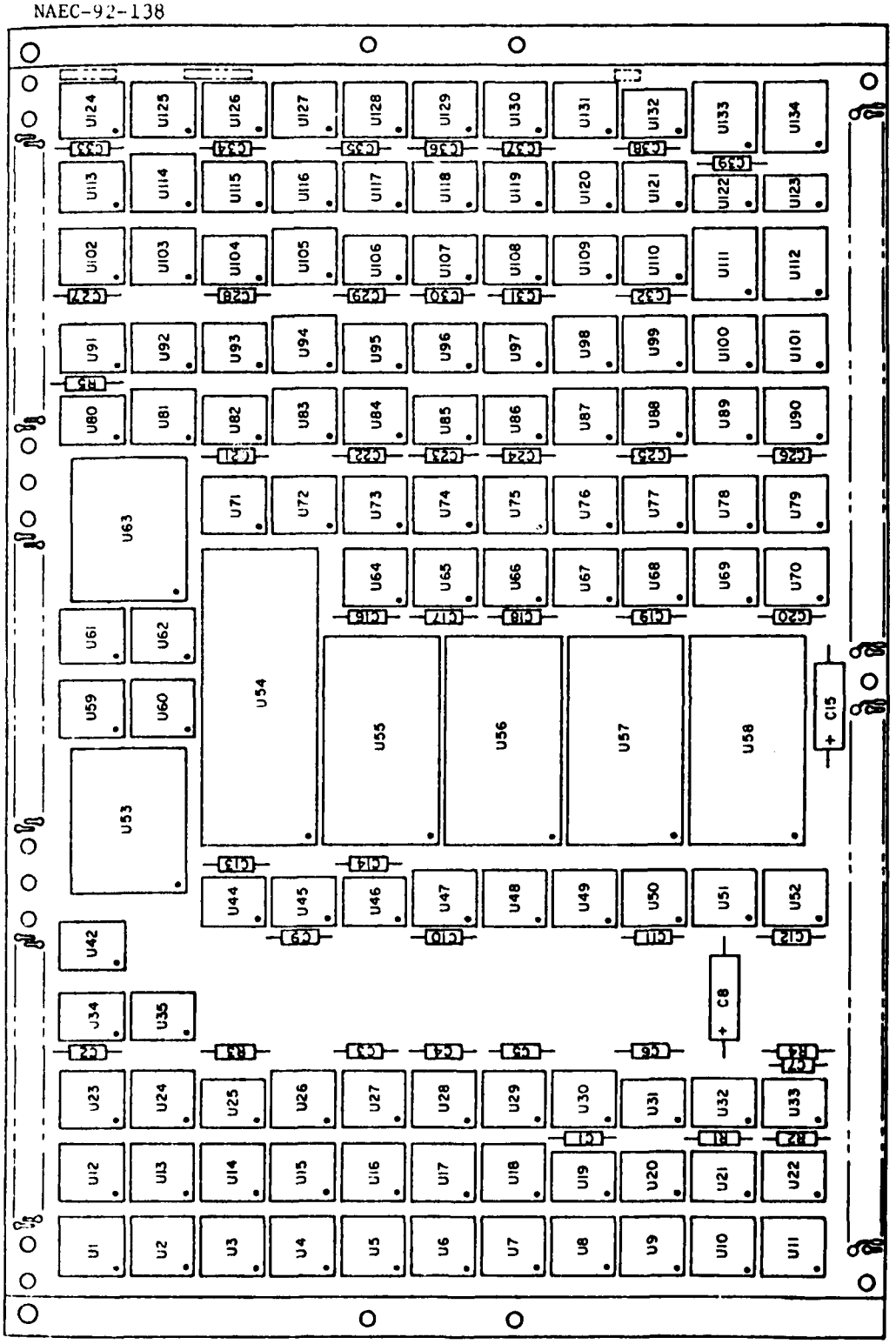


Figure 15 - General Processor Module, Circuit Card B

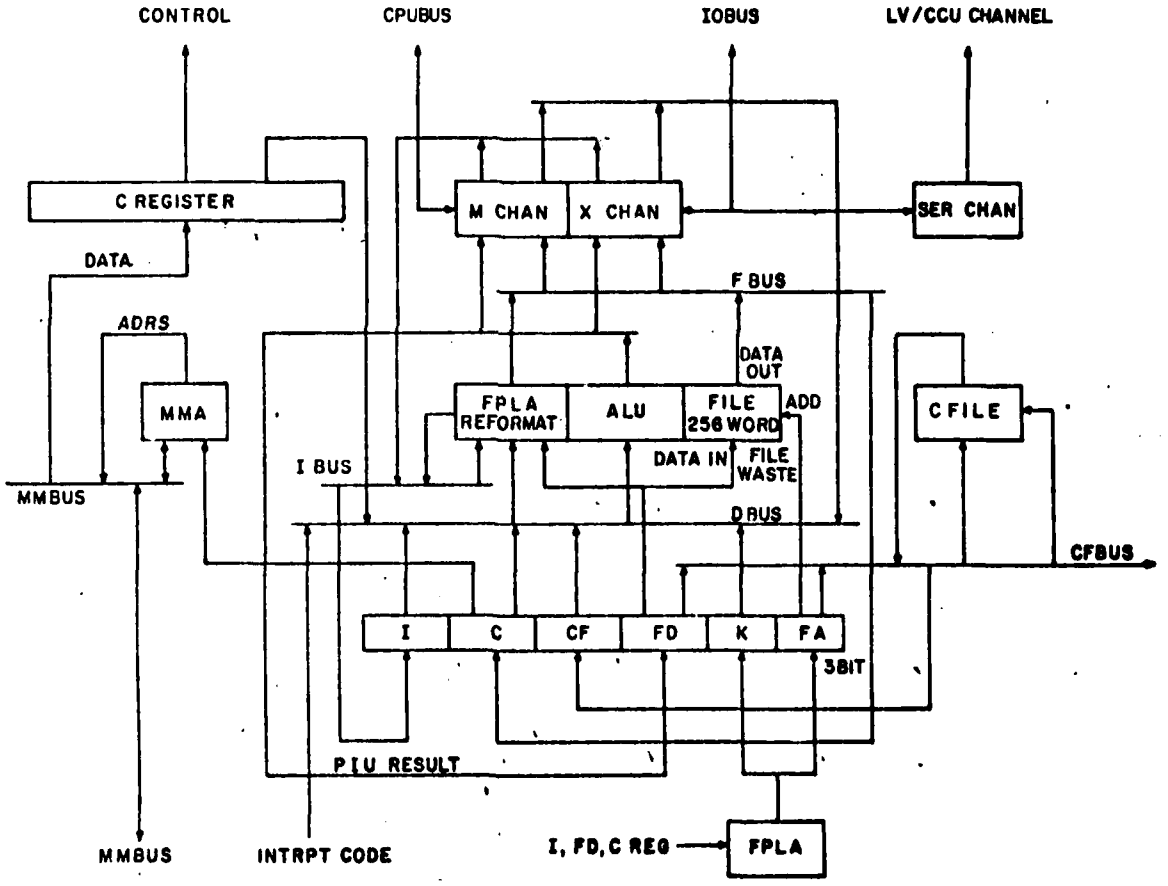


Figure 16 - General Processor Module (GPM), Block Diagram

address of the next microcommand. The current microcommand execution is overlapped with the next microcommand access. The micromemory address (MMA) control supplies the 12-bit address of the next microcommand-to-micromemory bus (MMBUS) based on current microcommand (C register) fields. The MMA is implemented using AMD 2909 LSI circuits and contains four address sources which may be specified directly, or conditionally, based on status conditions resulting from the last microcommand. These address sources are:

- o An increment register containing the current address plus one.
- o A four-register stack for subroutine return address.
- o A jump address register that is conditionally loaded from microcommand fields.
- o A direct data path connected to the lower 12(U) register bits. (This path allows micromemory jumps to address based on instruction decode values.)

The C register data inputs are also connected to the MMBUS, since the micromemory is located on the PSM-1 SRA rather than the GPM SRA.

(2) The GPM is a 16-bit microprogrammable processor based on the AMD 2900 series microprocessor slice LSI devices. The architecture is augmented for high-speed performance with additional registers, internal data, and control transfer paths. The GPM features which contribute to its performance include:

- o 48-bit microcommand control
- o Microprogram address sequencing to 4K words
- o 180-nanosecond microcommand cycle
- o 256 by 16-bit word register file
- o 256 by 16-bit word multiport C file
- o Dual identical parallel bus interfaces (CPUBUS and IOBUS)
- o Event interface
- o Interface to micromemory on PSM
- o Serial interface to support equipment
- o Interface to EAU

The GPM operates from microcommands stored on the PSM (up to 4K words of micromemory).

(3) The arithmetic logical unit (ALU) consists of the 16-bit arithmetic section of the CPU. This hardware is implemented using four AMD 2901 LSI circuits and includes the ALU, 16 random access memory (RAM) registers, the Q register, data multiplexers, and shifting capability. The ALU section is used to perform arithmetic an logical functions, including multiply and divide iterations. The AMD 2901 file addresses, instruction bits, and the carry-in signal are provided directly from appropriate C register bits. In addtion to internal AMD 2901 functions, the current microcommand may specify a data source onto the D bus as AMD 2901 input data and may specify either the I register or the M or X channel address register as a destination register at the end of every microcommand. The ALU can operate with two's complement, fixed point data.

(4) The GPM provides a 256-word file, which is addresed by the 8-bit FA register. Each microcommand specifies an FA register input source via the FA FPLA. The FA FPLA is programmed to transfer various register fields to the FA register as selected by the C register. The address register file is gated into the U register by the F bus; in addition, if a file write operation is specified, the address file location receives data from the FD register. The file access occurs in parallel with the specified ALU operation.

(5) The reformat FPLA output may be selected onto the F bus and into the U register instead of a file data word by the microcommand. The reformat FPLA is programmed to transform data (such as an instruction read from memory) into a micromemory jump address. This FPLA performs the instruction decode function during the emulation process. The micromemory address may be transferred to the MMA hardware directly from the U register.

(6) A 256-word control C file is also included in the GPM architecture. The 16-bit C file is addressed by the FA register and receives data from the FD register. The C file read data is transferred to the D bus by the 16-bit CF register. The C file is unique in that the address/data bus is available to ther SRA modules. C file control allows up to four users to access the C file. This C file bus is the means of communication with the optional FAIL.

(7) Several special registers are provided by the GPM architecture. The 16-bit I register, which may be conditionally gated from the I bus, normally holds the instruction being decoded. The 16-bit U register receives file and FPLA data for transfer to MMA or the D bus. The FD register holds ALU data to be written into the file or C file. The K register inlcudes an 8-bit iteration counter and an 8-bit status register. The 8-bit FA register provides the file and C file address.

(8) The M and X channels each include an output address (or control) register gated from the ALU output, an output data register gated from the F bus, and an input data register connected to the D bus. The M and X channels interface with the CPU and I/O buses.

(9) The LV/CCU channel provides a serial interface for computer control. The microprogram firmware communicates with the LV/CCU channel registers by means of the X bus. A combination of hardware and firmware allows control, display data, and memory data to be transferred to the CCU or LV and allows entry of data from the CCU or LV into computer registers or memory.

(10) Most GPM microinstructions are executed in 180 nanoseconds. This time includes reading the next microcommand. Other microinstructions, those specifying an ALU shift operation and certain ALU input transfers from the D bus, require a 210-nanosecond execution time.

(11) The testing parameters of the GPM are noted in Table 1.

TABLE 1

GENERAL PROCESSOR MODULE TESTING PARAMETERS

SRA configuration: Double digital circuit card SRA	
IC count: Board A, 84 IC's; board B, 127 IC's: total IC's, 208	
Connector pin count: 3 top 41-pin test point connectors	- 123 pins
2 bottom 152-pin I/O connectors	- 304 pins
Total	- 427 pins
Signal I/O pins: Board A, 138 pins; board B, 136 pins; total	274 pins
Test point pins: J-1, 37 pins; J-2, 27, J-3, 38; total	102 pins
Total I/O pins -	376 pins
Power pins: Board A, 14 pins; board B, 14, total power pins,	28 pins
Test point power pins (test point connectors):	10 pins
Total required pins (both boards):	414 pins
Power required: +5 vdc 9.4 amp max, 47 watts	
Oscillators: 19.2 MHz, 33.33 MHz	
Bidirectional lines: M bus, 24 bits; X bus, 24 bits	

b. Processor Support Module (PSM). The PSM augments GPM functions to form a complete 16-bit computer in two double modules. The partitioning of the functions between GPM and PSM was designed to allocate those functions to the PSM that might require modification as applications change. The PSM features include:

- o Up to 4K by 48 bits of PROM micromemory for the GPM.
- o 1K by 16 bits of PROM bootstrap memory for computer system initiation via the 1553A I/O channel or the CCU console.
- o Two parallel bus interfaces (CPUBUS and IOBUS).
- o Event interface.
- o Event monitor logic, which forms the basic hardware portion of the event (interrupt) processing.
- o Four loadable/readable clocks for monitoring and timing functions (1-microsecond resolution).
- o 32-bit high-speed multiply logic.
- o Bit timer with 2.097-second increment 4-bit count.

(1) The PSM provides the necessary features to complement the GPM and complete the basic CPU functions of the processing subsystem. The PSM is a double-card SRA. The PSM from the B circuit card side is shown in Figure 17. The A circuit card side is presented in Figure 18.

(2) The functional features of the PSM are noted in the PSM block diagram, Figure 19. The PSM provides space for mounting up to 4K words of programmable read only memory (PROM) for the microprogram memory. For the CPU, 3K words of micromemory, which are uniquely coded to perform the CPU functions, are provided. When the PSM contains this micromemory complement it is referred to as the PSM-1. The PROM micromemory receives 12-bit addresses from the GPM via the MMBUS and returns the 48-bit micromemory data on the MMBUS. Partitioning the micromemory on the PSM closely divides the power dissipation between the GPM and PSM and allows all unique ROM (including ROM bootstrap memory) to be located on the same module. Multiple subsystems are thus allowed to use identical GPMs.

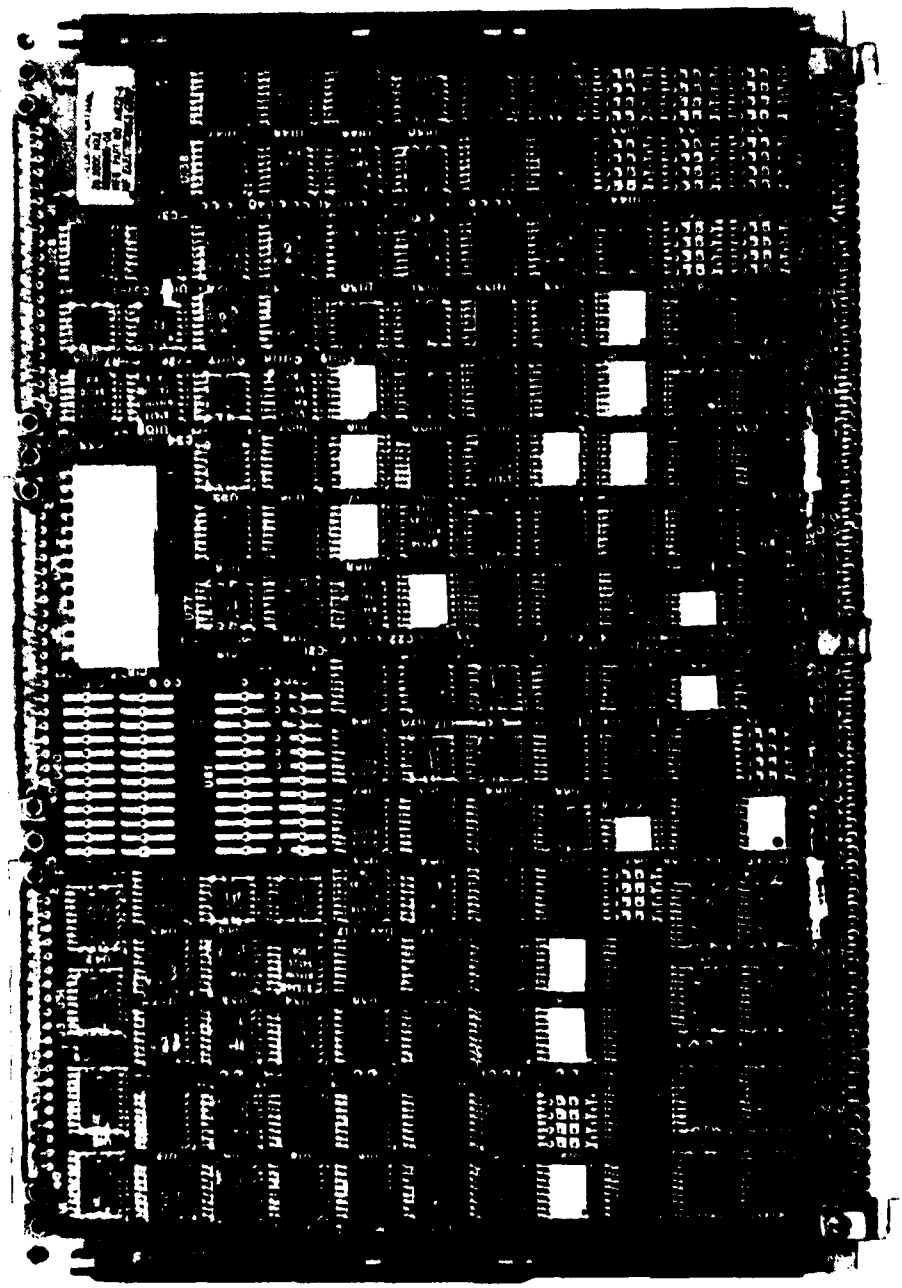


Figure 17 - Processor Support Module, Circuit Card B

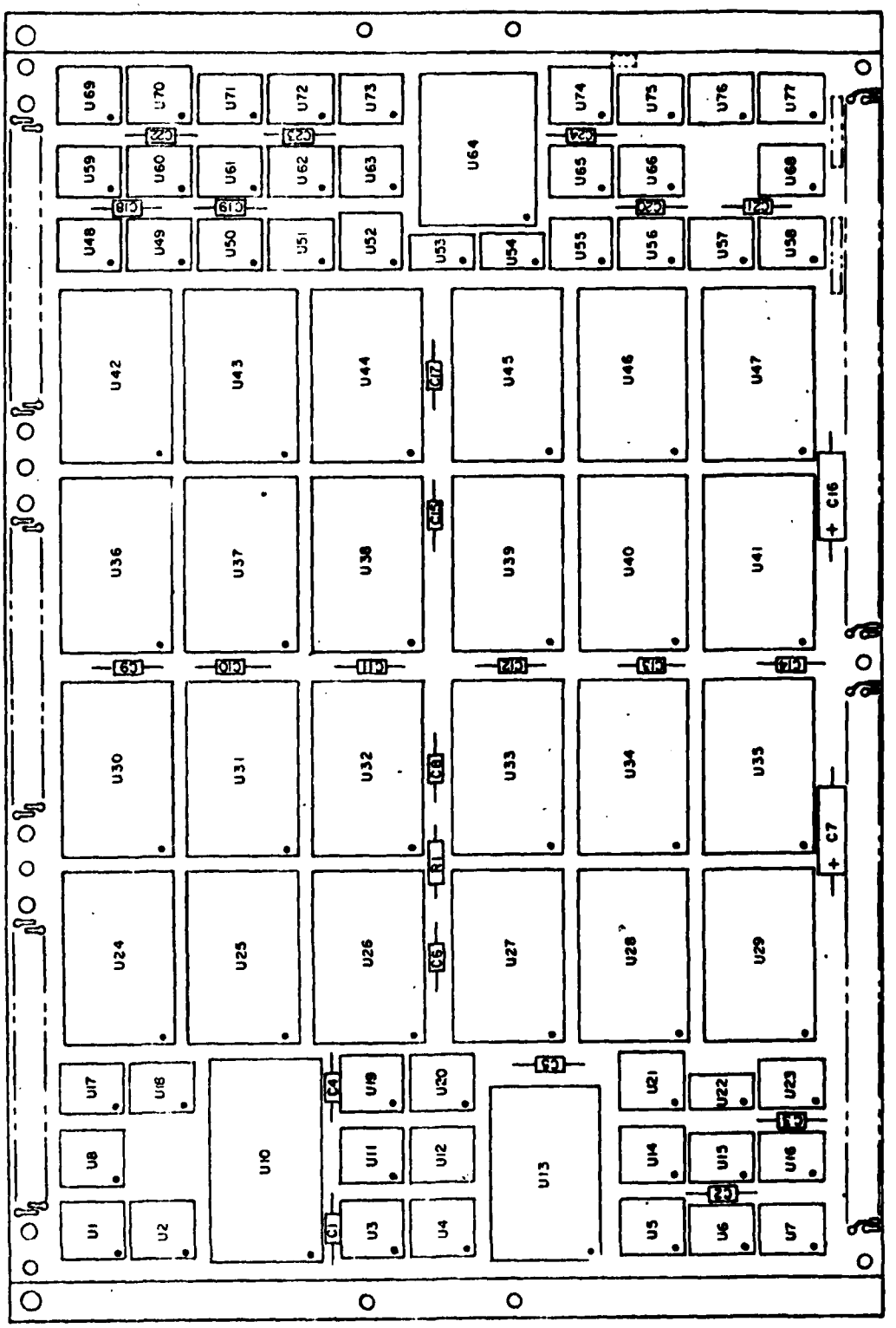


Figure 18 - Processor Support Module, Circuit Card A

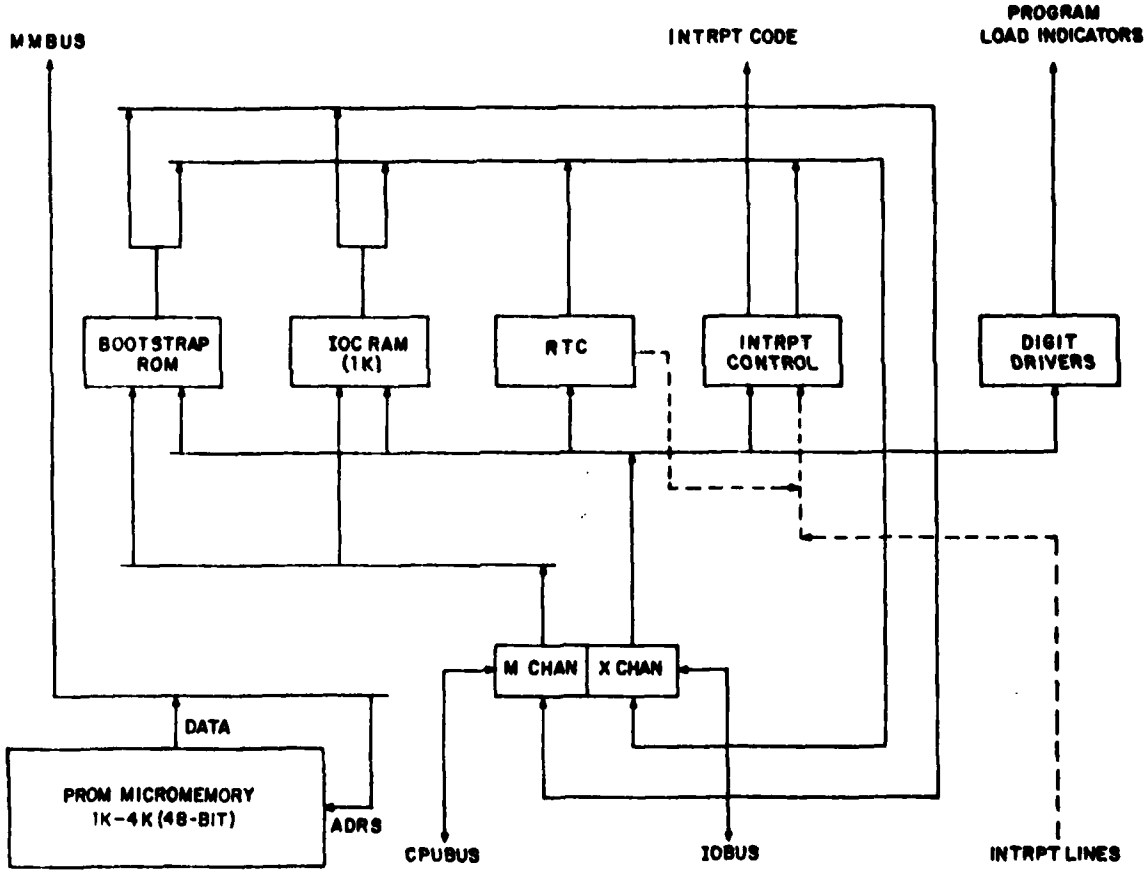


Figure 19 - Processor Support Module, Block Diagram

(3) The remaining PSM functions are connected to the GPM, the CPUBUS, and/or IOBUS. The bootstrap ROM feature contains 192 words of addressable read-only program memory. The ROM is addressable on either the IOBUS or the CPUBUS. The ROM is addressed as main memory locations 000_8 through 077_8 and 300_8 through 477_8 when specified by status register 1, bit 12. Special hardware is used to decide the ROM address ranges and allows the ROM to be selected rather than main memory. This relieves the emulator firmware of having special, time-consuming routines to determine ROM address ranges. The ROM is implemented using high-speed bipolar PROM integrated circuits. The software program to be stored in the ROM bootstrap memory is burned into the PROM integrated circuits during the manufacturing cycle.

(4) The PSM real-time clocks (RTCs) communicate with the GPM using the I/O bus, under control of firmware routines. The RTC is not addressable by software as an I/O channel, but by special firmware initiated by RTC interrupt routines and by software instructions that load, store, enable, and disable the RTC or monitor clock. The RTC logic on the PSM is part of the timing function. The remaining timing function, the basic system clock, is contained on the GPM. Thus, the timing function is completely integrated into the CPU on the SRAs. The timing features are completely duplicated in the IOC, since this subsystem also contains a GPM and a PSM (PSM-2). The RTC hardware consists of two files, each containing four 16-bit words. The first file contains four RTC value words, which are set from the firmware by the IOBUS. The other file is the current count file. Count file words are counted at a rate determined by the module wiring and firmware control. The count file registers are set to the value file word content when commanded by a firmware bus command and automatically each time the count terminates.

(5) Two value/count file register pairs implement the AN/AYK-14(V) monitor clock. The first pair is programmed to overflow at 100-microsecond rate. The output of this clock is used as the timing source for the second register pair. The second pair is programmed to provide the program-addressable monitor clock and generates an interrupt each time the count terminates. A third count/value file pair is used to implement the lower 16 bits of the 32-bit RTC. This count file register is counted at a 1-microsecond rate (when enabled) and generates an interrupt each time the count overflows. The upper 16 RTC bits are contained in one of the GPM register files and are updated under firmware control. This part of the RTC is updated even if the interrupt associated with the lower 16 bits of the RTC is disabled. The last value/count is available for special firmware usage. A crystal-controlled oscillator provides the RTC time base.

(6) The IOC random access memory (RAM) logic is optional, and associated hardware is not included on the PSM-1 module for the CPU. The PSM-2 module, for the IOC, does contain the IOC RAM, which consists of a 1K semiconductor, 400-nanosecond, 18-bit RAM. It is used as the basic 1K of IOC program memory. The IOC RAM is assigned a block of memory addresses and provides a non-paged memory for IOC programs.

(7) The interrupt system communicates with the GPM using the IOBUS, but it is assigned a channel number that is not accessible by software I/O instructions. This interface allows the firmware to transfer interrupt mask words and other control parameters to the interrupt system (such as allowing the firmware to generate internal interrupts resulting from instruction execution and to generate the two external interrupts). The interrupt system receives interrupt lines from external modules and contains appropriate interrupt priority, interrupt and mask registers, and interrupt code generating hardware. The interrupt system sends an interrupt code of the highest priority interrupt directly to the GPM. This allows the firmware to read the interrupt code onto the D bus, and through the reformat FPLA to generate a firmware jump address. The presence of an interrupt code may be tested by the firmware during software program execution. In addition to the three classes of external and internal software interrupts, special interrupts for firmware use are generated. These include I/O channel interrupts related to I/O chain programs and I/O channel service requests.

(8) The PSM also contains the interface and control logic to drive the program load indicators.

(9) The testing parameters of the PSM are noted in Table 2.

TABLE 2

PROCESSOR SUPPORT MODULE TESTING PARAMETERS

SRA configuration: Double digital circuit card SRA		
IC Count: Board A, 75 IC's; board B, 143 IC's; Total IC's 218		
Connector pin count: 3 top 41-pin connectors	-	123 pins
2 bottom 152-pin connectors	-	304 pins
Total	-	427 pins
Signal I/O pins: Board A, 131 pins; board B, 121 pins; total,		252 pins
Test point pins: J-1, 31 pins; J-2, 39 pins; J-3, 21 pins; total ,		91 pins
Total		343 pins
Power pins: Board A, 14 pins; board B, 15 pins; total,		29 pins
Test point power pins (test point grounds)		6 pins
Total required pins (both boards)		378 pins
Power required: +5vdc, 8.6 amp max, 43 watts		
Oscillators: board A, 32 MHz to 16 MHz; board B, 20 MHz		
Bidirectional/differential lines:		
Board A, none		
Board B, bidirectional lines - X Bus, M bus, 32 bits		
Board B, differential lines - 2 outputs, 4 pins; 5 inputs, 10 pins		

c. Extended Arithmetic Unit (EAU). The EAU SRA is a 32-bit, high-speed, floating-point processor which operates under the control of the GPM and interfaces directly to it. The EAU utilizes the AN/UYK-20 floating-point format which consists of an 8-bit exponent and a 24-bit mantissa as well as performs high-speed, 32-bit, fixed-point division. Typical execution times, including GPM control, are 4 microseconds for add and 5 microseconds for multiply. All AN/AYK-14(V) computers configured with a GPM and PSM execute all AYK-14(V) floating point arithmetic instructions. When configured without the EAU, the instructions are implemented via firmware. The incorporation of the EAU automatically increases floating point execution speed without firmware changes.

(1) The execution speeds for add, multiply, and divide are shown in Table 3. The EAU is double circuit card SRA. Figures 20 and 21 present the A board and B board of the EAU.

TABLE 3

EXTENDED ARITHMETIC UNIT PERFORMANCE

Instruction	Percent Mix	Execution Time (microseconds)	Weighted Time	Kops
Add	80	2.160	1.728	
Multiply	10	3.660	.366	
Divide	10	6.005	.601	
Total	100		2.695	371

(2) The EAU is more than just a hardwire, floating point arithmetic module. It consists of a programmable architecture designed to provide high-speed arithmetic algorithms for fixed or floating point arithmetic. In the AN/AYK-14(V) computer instruction set, the EAU provides increased CPU performance for all floating point instructions as well as 32-bit data length fixed point multiply and divide.

(3) In future applications and configurations of the AN/AYK-14(V) SRAs, this module could be utilized, by reprogramming of PROM circuits, to perform arithmetic algorithms such as polynomial expansions, trigonometric functions, fast Fourier transform (FFT) operations, cordic algorithms, and so forth. This designed-in capability of the EAU could broaden the applications and use of the AN/AYK-14(V) computer.

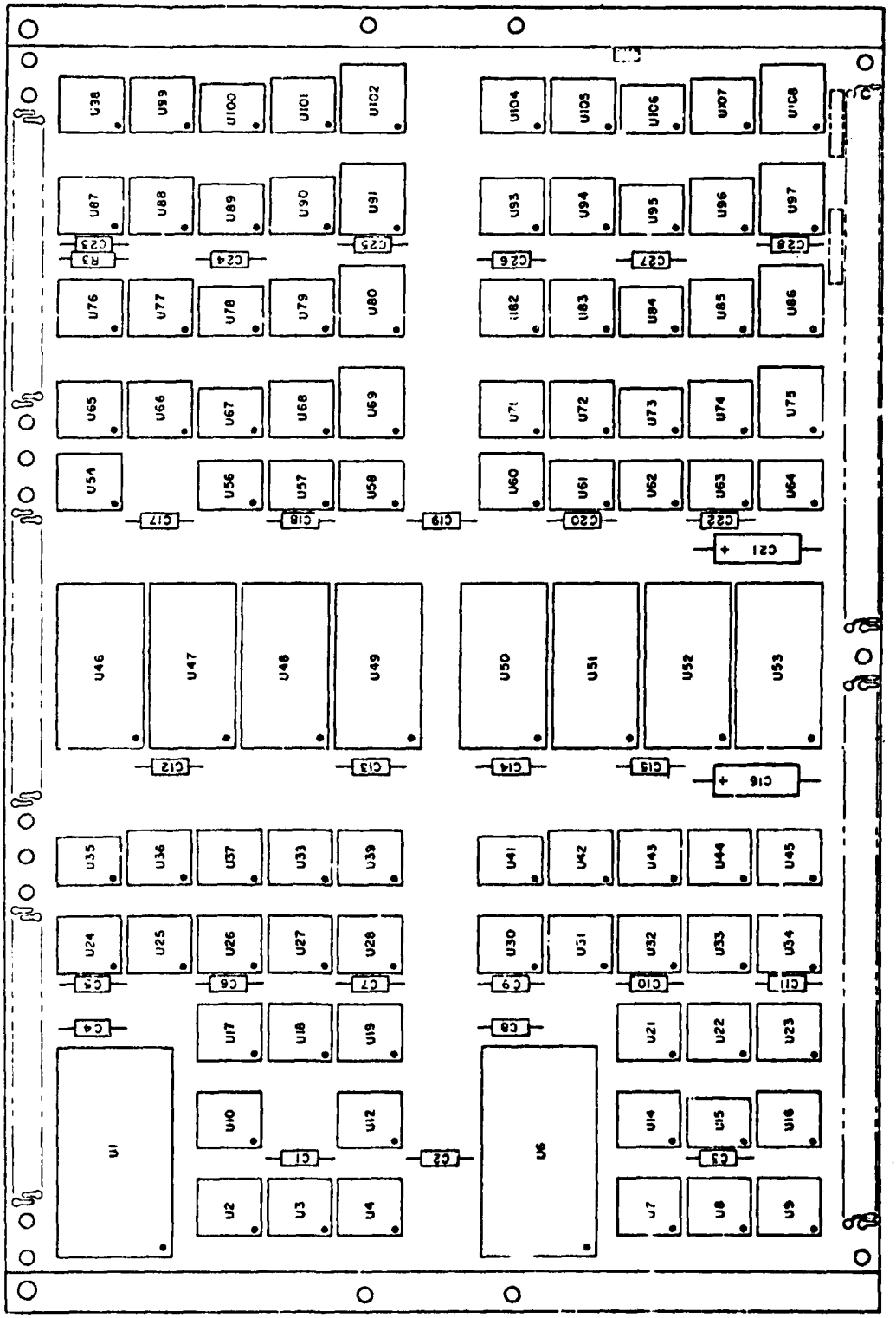


Figure 20 - Extended Arithmetic Unit, Circuit Card A

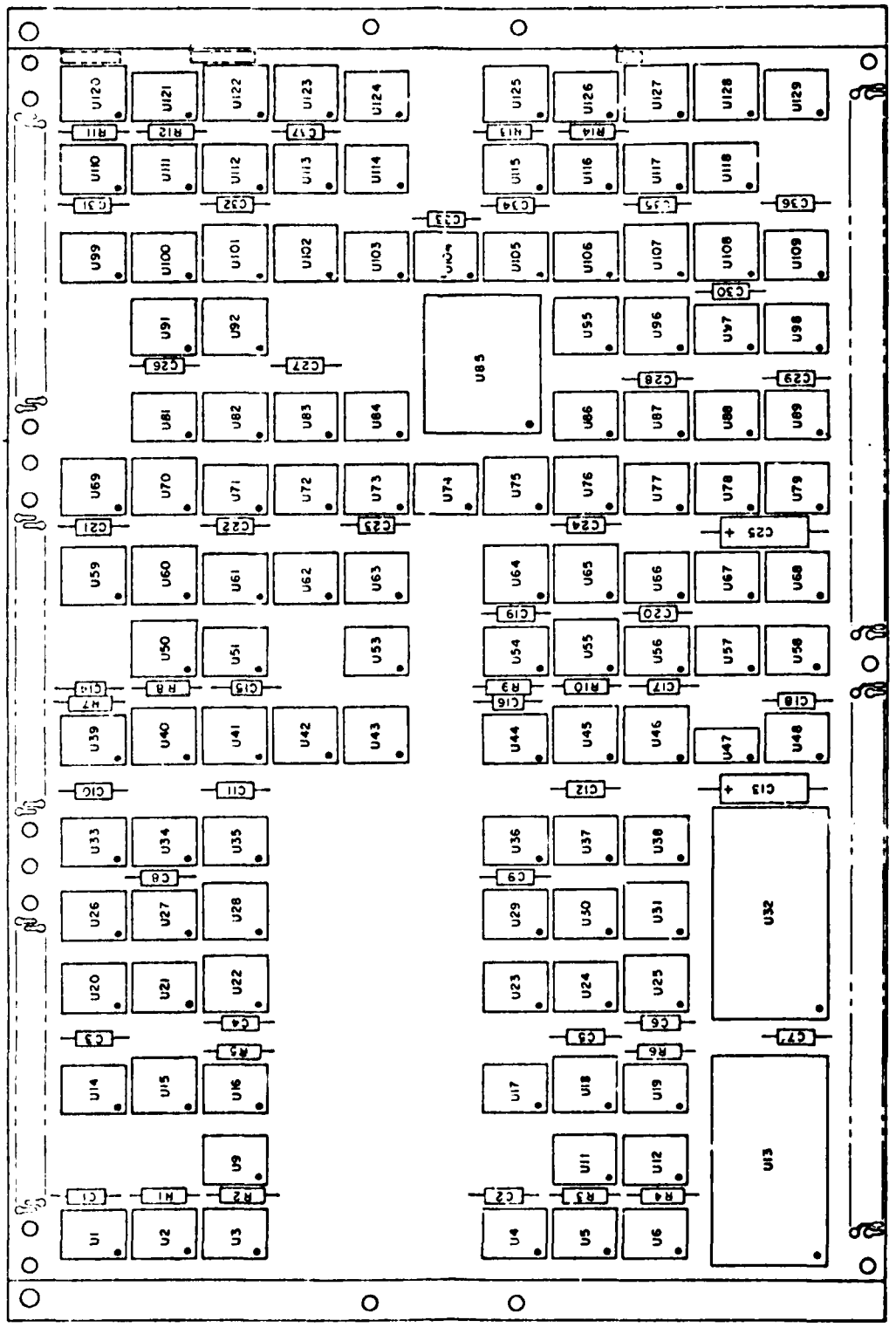


Figure 21 - Extended Arithmetic Unit, Circuit Card B

(4) Figure 22 depicts the various architectural elements of the EAU. The shift network, multiply hardware, and arithmetic sections are all 32 bits wide. The arithmetic section is constructed using AMD 2901 LSI circuits and also contains 16 storage registers. This arithmetic section performs exponent and fractional data arithmetic for floating point operations. The shift network provides for rapid numerical alignment, scaling, and normalization. The testing parameters of the extended arithmetic unit are described in Table 4.

TABLE 4

EXTENDED ARITHMETIC UNIT TESTING PARAMETERS

SRA configuration: Double digital circuit cards, each 6 inches x 9 inches
IC count: Board A, 96 IC's; board B, 119 IC's; total IC's, 215
Connector pin count: 3 top 41-pin connectors - 123 pins
2 bottom 151-pin connectors - 304 pins
Total - 427 pins
*Signal I/O pins: Board A, pins; board B, pins; total, pins
*Test point pins: J-1, pins; J-2, pins; J-3, pins total pins
Total I/O pins
*Power pins: Board A, pins; board B, pins; total, pins
*Test point power pins: pins
*Total required pins (both boards): pins
Power required: +5 vdc, 9.2. amps, 46 watts
*Oscillators:
*Bidirectional lines:
*Data not available; EAU in development.

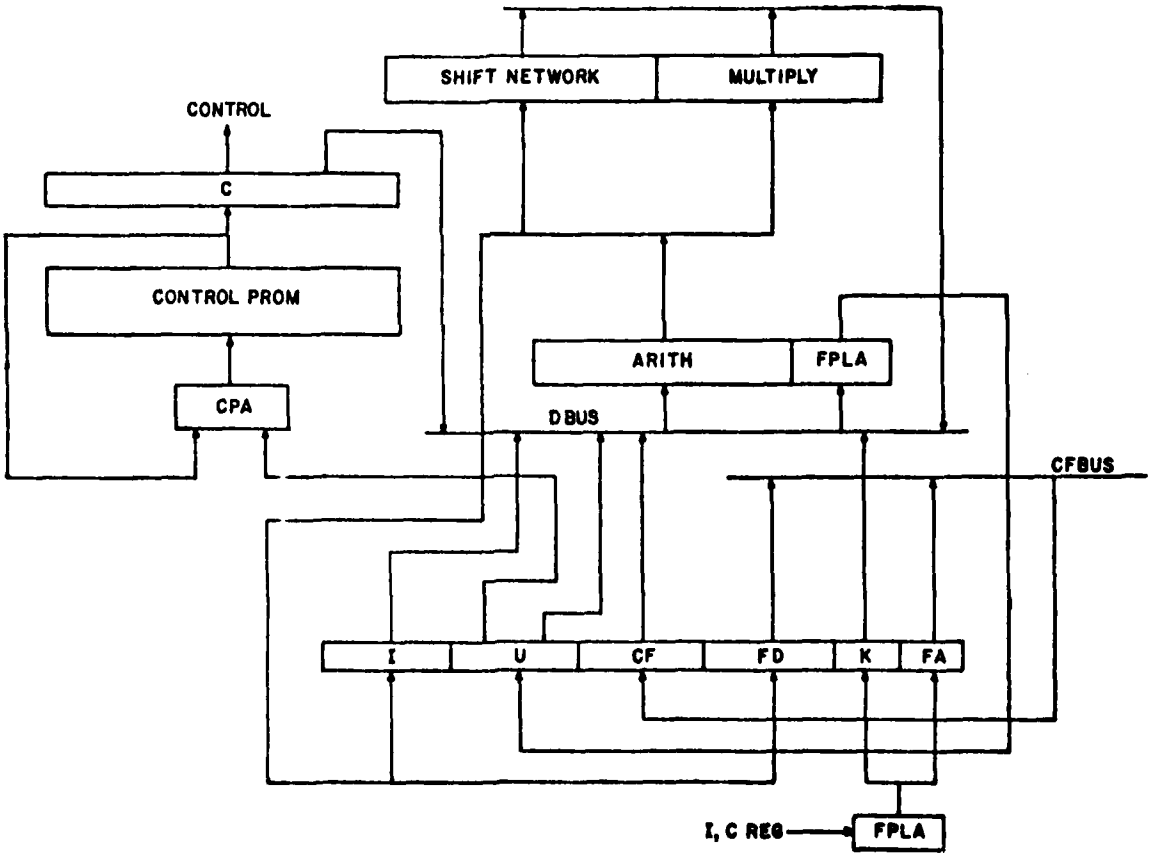


Figure 22 - Extended Arithmetic Unit, Block Diagram

3. MEMORY SUBSYSTEM SRAs

a. Memory Control Module (MCM). The MCM provides a two-port paged interface of two independent, interleaved memory channels, and thus allows simultaneous access by two users. The MCM contains the control, interface, and paging logic to operate core and semiconductor memories with the AN/AYK-14(V) computer system. The MCM features include:

- o Interfaces to CPUBUS and IOBUS
- o Dual memory bus interfaces to memory modules OMEMBUS and EMEMBUS
- o 16-bit address to 19-bit address paging system
- o Phasing of memory modules between memory buses
- o Parity bit logic, one parity bit per bite; block protect in paging system: Read protect, Write protect, Execute protect.

(1) The memory control module is contained on a double circuit card SRA. Figure 23 presents circuit card A of the MCM. The MCM provides the necessary logic to interface the CPU and I/O subsystems to main memory by providing an interface between the CPUBUS, the IOBUS, and the two memory buses as shown in Figure 24, MCM block diagram. The MCM consists of two completely independent ports interfaced to two completely independent memory channels, thus allowing two simultaneous memory references. MEMBUS selection (or interleave) is determined by the least significant bit of the memory address (thus, the terms even and odd memory buses).

(2) The MCM provides the mechanism within each port to transform a 16-bit relative address received on the port to a 19-bit physical address by passing it through the page and protect logic. This logic consists of a page file, which is a 256-word by 16-bit bipolar RAM that is addressed by the six most significant bits of the relative address and a 2-bit state register. This allows up to four sets of 64 page registers for possible multi-state processing. Each page register contains the required 9-bit page base address, which is appended to the least significant 10 bits of the relative address to form the final 19-bit physical address. With the least significant bit determining which MEMBUS to access, the remaining 18 bits form the address sent to the selected MEMBUS.

(3) The page file also contains three lockout bits, which are used to protect any 1K page of memory against an unwanted access. One bit protects against executing an instruction out of the addressed page, another protects against a readout of the addressed page, and the third protects against a write into the addressed page. The type of operation (read, write, and instruction fetch) is decoded from the 8-bit control code that is received along with the address on the IOBUS and CPUBUS. A comparison of this code against the appropriate lockout bit determines whether a protect fault has been generated. In the case of the two read operations, the MCM executes the read and returns the data to the IOBUS or

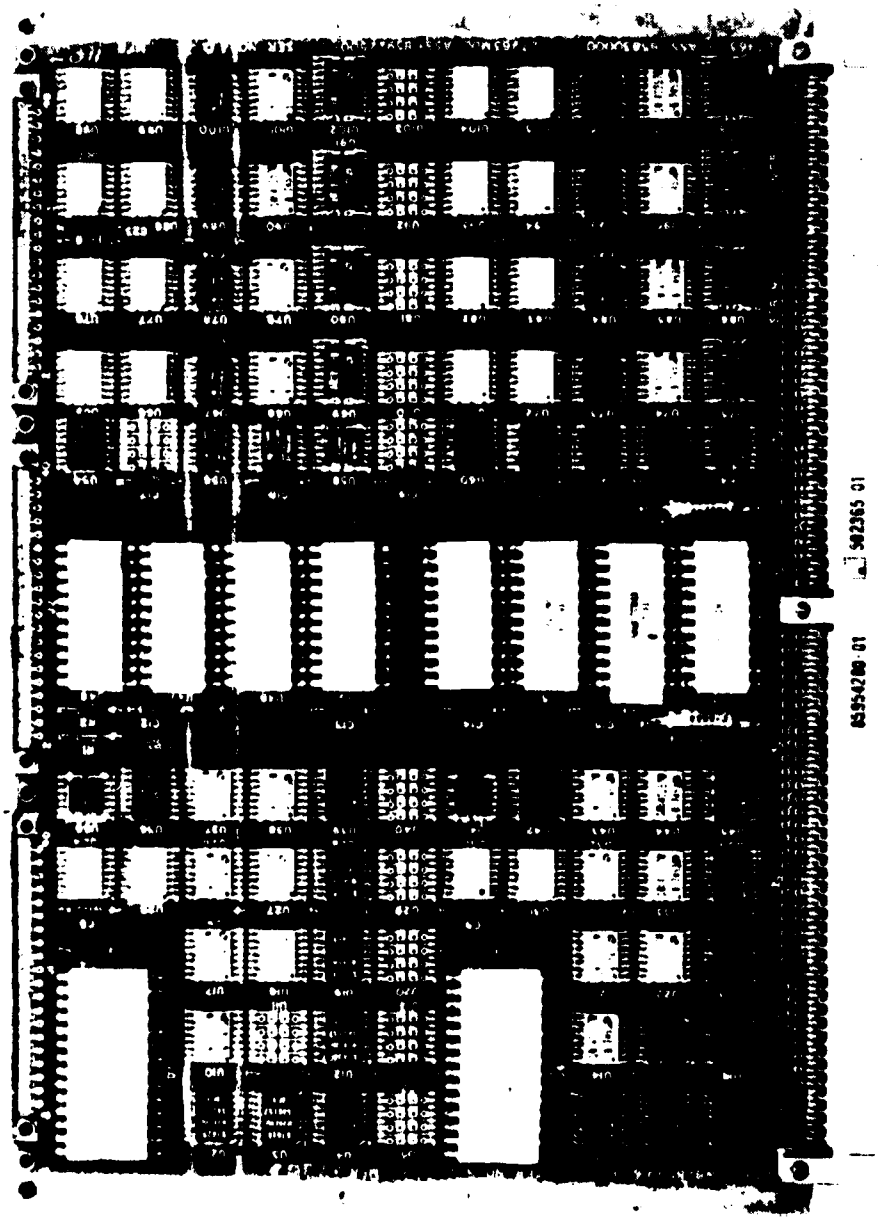


Figure 23 - Memory Control Module, Circuit Card A

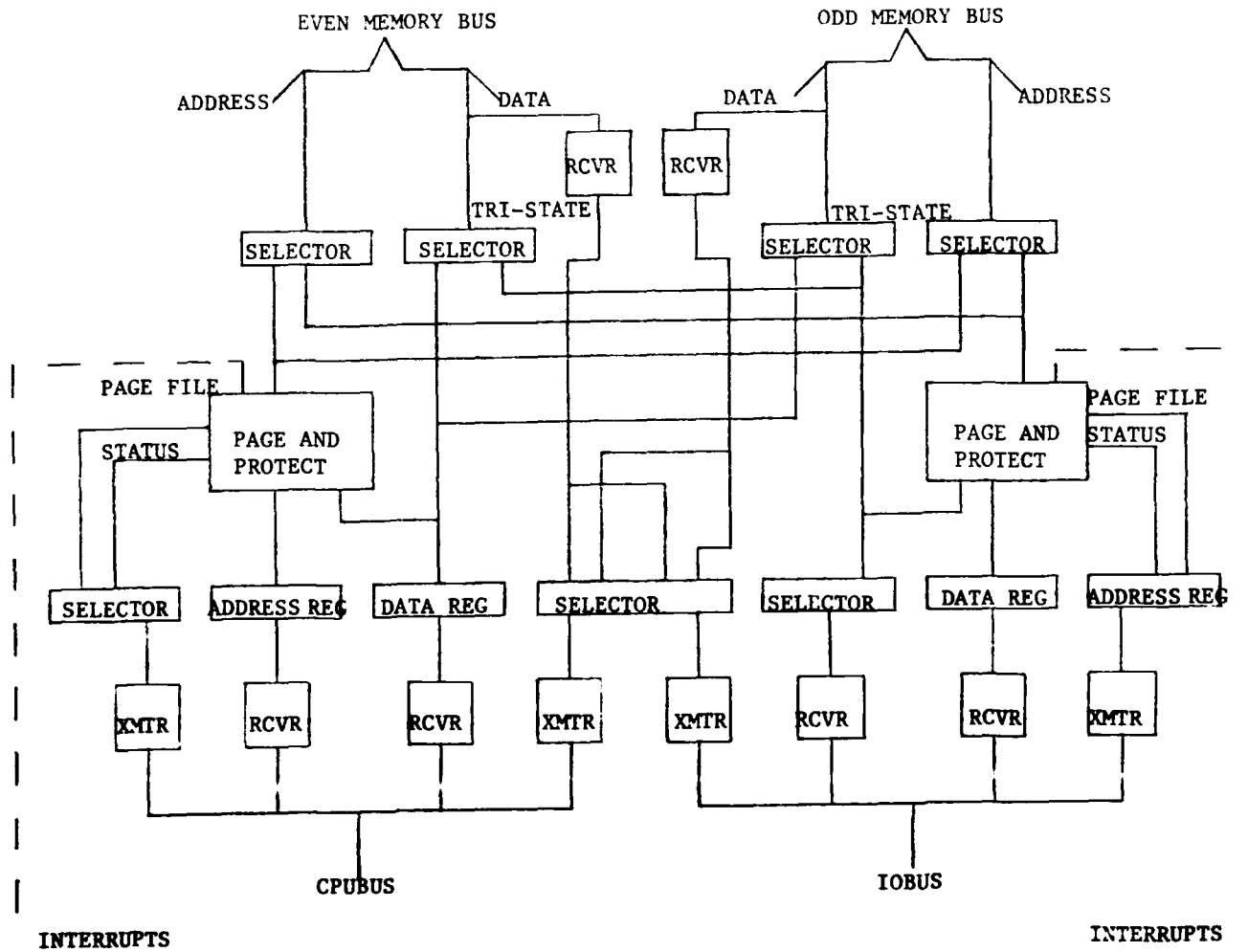


Figure 24 - Memory Control Module, Block Diagram

CPUBUS along with the bus error bit. This error bit flags out to the bus user at the firmware level that an error condition has occurred. At the same time, the appropriate protect fault status bit is set in the status register. In the case of the write protect fault, the MCM hardware aborts the write operation and performs a read instead, while sending a bus error bit to the user and setting the appropriate status bit. The most significant bit in each word of the page file is the page modification indicator, which is set to a logic 1 if at any time the page in memory is written into.

(4) There are two basic types of operations that the MCM will perform, a data transfer operation and a function/status operation. These are determined by the control code received with the address on every CPUBUS or IOBUS request. A data transfer operation is used, as the name implies, to transfer a single data word from memory (a read cycle) or to memory (a write cycle). A function/status transfer operation is used to define or change certain parameters and/or characteristics of the control logic within each port of the MCM or is used to permit reading the conditions that have occurred within the port or the condition to which the port has been set.

(a) A function operation is basically an output operation to the MCM and is used to write into the page file, to set up the 2-bit state register that is used as part of the page file address, and to set up the mode register, which determines the parity to be written and how the check bit is to be written. This allows the firmware to perform such functions as releasing or modifying memory protection, writing bad parity, or modifying the check bit at request of the CCU.

(b) A status operation is basically an input operation from the MCM and is used, as the name suggests, to find out what the status of the port is. There are two status operations. The first is a simple read of the page file. This operation transfers the 16-bit contents of the addressed page file to the CPUBUS or IOBUS. The second status operation is a transfer of the status register to the CPUBUS or IOBUS. The status register contains the following status conditions:

- o Parity error - even MEMBUS
- o Parity error - odd MEMBUS
- o Write protect fault
- o Read protect fault
- o Execute protect fault
- o No response on even MEMBUS
- o No response on odd MEMBUS
- o Check bit error

The status operation can also clear the status register after it has been transferred to the CPUBUS or IOBUS.

(5) On all data transfers, the MCM port performs the paging transformation on the relative address and checks the lockout status of the referenced page. It also determines which MEMBUS is to be referenced and then generates a request to the appropriate channel. Each memory channel of the MCM contains completely independent control logic to control the MEMBUS, to determine priority of the users, and to control the routing of the data between the port and the MEMBUS. On a write operation, the port logic generates the check bit and the parity bit (the parity of the 16 data bits and the check bit). The 16 data bits, along with the check bit and the parity bit, form the 18-bit data word to the MEMBUS.

(6) The 18-bit word is routed under control of the memory channel logic to the memory data bus. In the case of two simultaneous requests, the channel "ping-pongs" the priority. That is, the last MEMBUS user must wait until the next reference. In this way, no one user is allowed to lock out another user from the MEMBUS. During a read operation, the checklist and parity status are checked in the channel and sent to the connected port. Either condition causes an interrupt to be generated back to the user. There is also a response timer in each channel so that if a memory does not respond, a no-response interrupt is generated back to the user.

(7) The testing parameters of the memory control unit are presented in Table 5.

TABLE 5

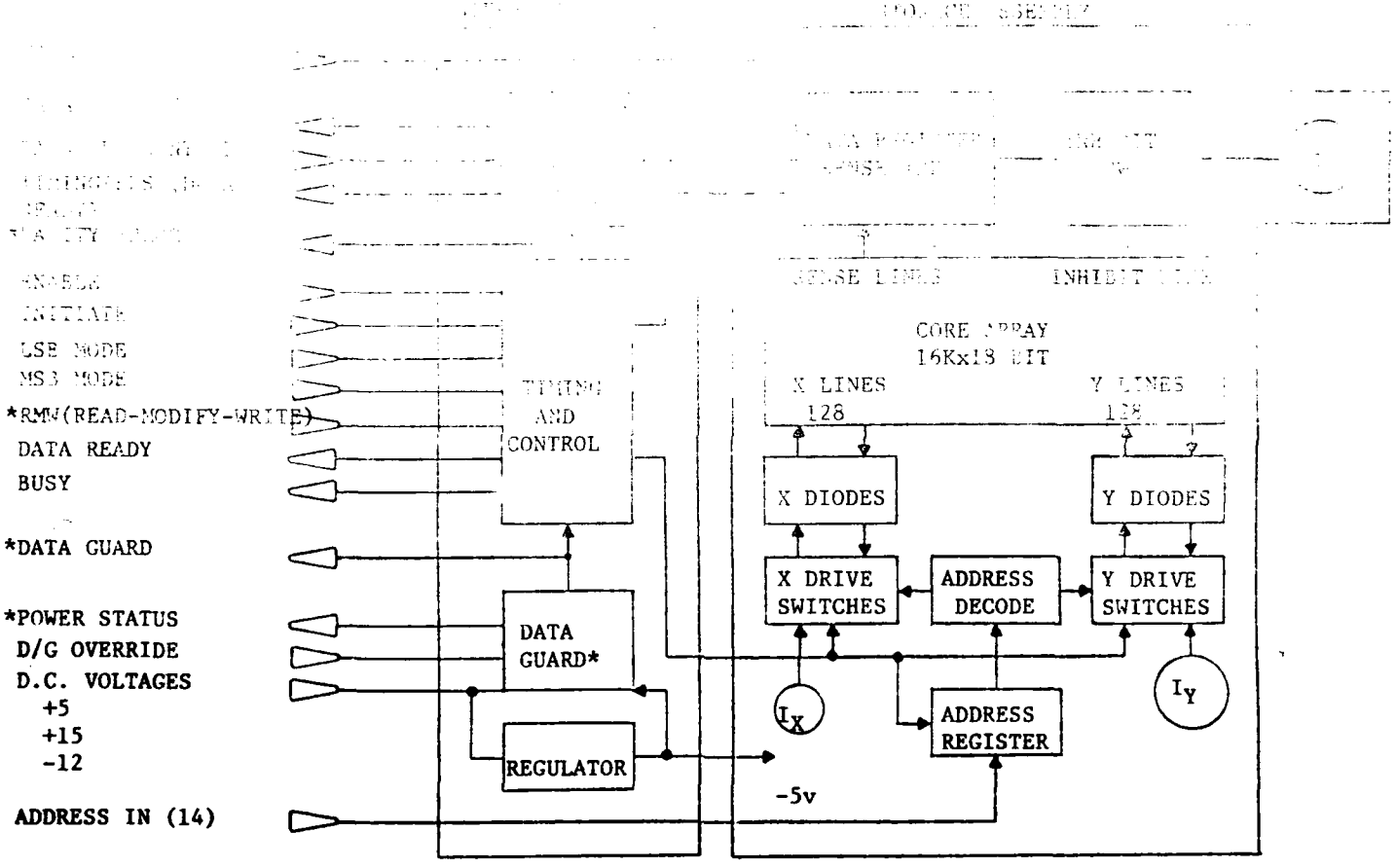
MEMORY CONTROL MODULE TESTING PARAMETERS

SRA configuration:	Double digital circuit cards, each 6 inches x 9 inches		
IC count:	Board A, 96 IC's; board B, 96 IC's; total, 192 IC's		
Connector pin count:	3 top 41-pin connectors	-	123 pins
	2 bottom 151-pin connectors	-	304 pins
	Total	-	427 pins
Signal I/O pins:	Board A, 94; board B, 88; total		182 pins
Test point pins:	J-1, 35; J-2, 34; J-3, 36; total		105 pins
			287 pins
Power pins:	Board A, 14; board B, 14; Total		28 pins
Test point power pins:			6 pins
Total required pins (both boards):			321 pins
Power required:	+5 vdc, 7.2 amp, 36 watts		
Oscillators:	33.3 MHz		

Bidirectional lines:	Board A	Board B
	X Bus 16 pins	X BUS 16 pins
	M Bus 20 pins	M Bus 20 pins
	Total 36 pins	Total 36 pins

b. Core Memory Module (CMM). The CMM is available as a 32K by 18-bit word module. The CMM is a plug-in unit containing all of the specified core storage, associated drive and sense electronics, timing and control logic, and interface circuitry. A block diagram of the CMM is shown in Figure 25. The form-factor and electrical interface of the 32K CMM is identical to the semiconductor memory module (SMM), discussed in paragraph C3, which provides for complete interchangeability of memory as noted in Figure 26. The CMM features are:

- o 900-nanosecond read/write cycle time
- o 350-nanosecond access time
- o Low power, average 31 watts for 32K words (based on half 1's 50-percent standby), maximum 64 watts
- o Bite operation
- o Interface to OMEMBUS or EMEMBUS
- o Read/modify/write capability
- o Data guard (optional), indicates power supply out of tolerance
- o Tri-state output and parity (optional)



*=OPTIONAL

Figure 25 - Core Memory Module, Block Diagram

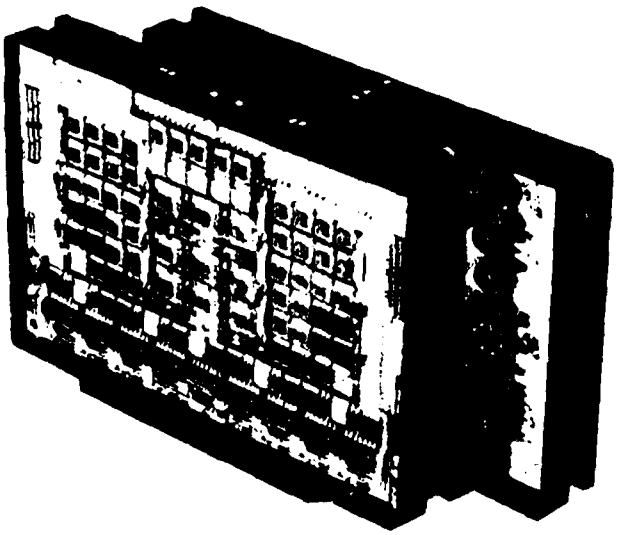


Figure 26 - Core Memory Module (front), Semiconductor Memory Module (rear)

(1) The CMM is available in a 32K by 18-bit and a 16K by 18-[illegible] for the AN/AYK-14(V) (the 32K core memory is standard). [illegible]-bit core memory is the CDC-9P, which is shown in exploded [illegible] This memory module is a nonvolatile, electrically al[illegible] core memory, which is electrically and mechanically [illegible] with a number of other available standard memory modules but [illegible] lower power dissipation. The module contains all the necessary [illegible] sense electronics required to read and write the memory. In [illegible], the CDC-9P provides all the electronics necessary to interface [illegible] the memory controller module (MCM) using the MEMBUS. This 3D, 3-[illegible] memory features a 350-nanosecond access time, a 900-nanosecond cycle [illegible], and a transistor-transistor logic (TTL) interface fully compatible [illegible] AN/AYK-14(V) requirements. This high performance, low-power memory [illegible] also available from a second source.

(2) The CDC-9P is comprised of two subassemblies, the storage [illegible]ly and the interface board (Figure 28). The storage assembly con[illegible] of two identical multilayer boards (Figure 29) which contain all of [illegible] electronics for drive and sense in addition to the 18-core arrays. [illegible] drive and sense components are surface-mounted on one side of each board, [illegible] 16K by 9 bits of core are contained on the reverse side. All core [illegible], between boards is continuous.

(3) The circuit design of the memory meets the component power [illegible] requirements of the AN/AYK-14(V) specification. In addition, [illegible] are derated to an extent that in a single failure mode condition, [illegible] of components is prevented. To provide a minimum weight, mini[illegible] component design, integrated circuits, thick film resistor networks, [illegible] multiple diode/transistor packages are used for all functions unless [illegible] limited by power dissipation limits. All semiconductors are available [illegible] at least two sources.

(4) The memory module utilizes a low-drive, temperature-inde[illegible] core. The low drive current requirement of this core allows the use [illegible] of driver components and provides for lower thermal stresses on all drive [illegible] circuit components. The module has a maximum power dissipation of less than [illegible] watts over the full temperature range. The low module power dissipation [illegible] low demand on both system power supplies and chassis cooling. The [illegible] core independence of the core eliminates the need for temperature-[illegible]sing current sources and relaxes the normally stringent requirements on [illegible] thermal gradients across the core arrays.

(5) The CDC-9P memory provides circuitry to prevent the loss [illegible] stored data during the power on/off sequences or during voltage tran[illegible]. These circuits prevent the start of a memory reference whenever [illegible] input voltages are outside ±4 percent of nominal. The module pro[illegible] adequate storage to complete reference in progress during a voltage [illegible] transient and will accept command as soon as the input voltages return to [illegible] the ±4 percent limits.

(6) The memory module was designed to meet, and is presently [illegible] being tested to, the AN/AYK-14(V) environmental requirements, including [illegible] high temperature operation (writing at one temperature extreme and read[illegible] at the other).

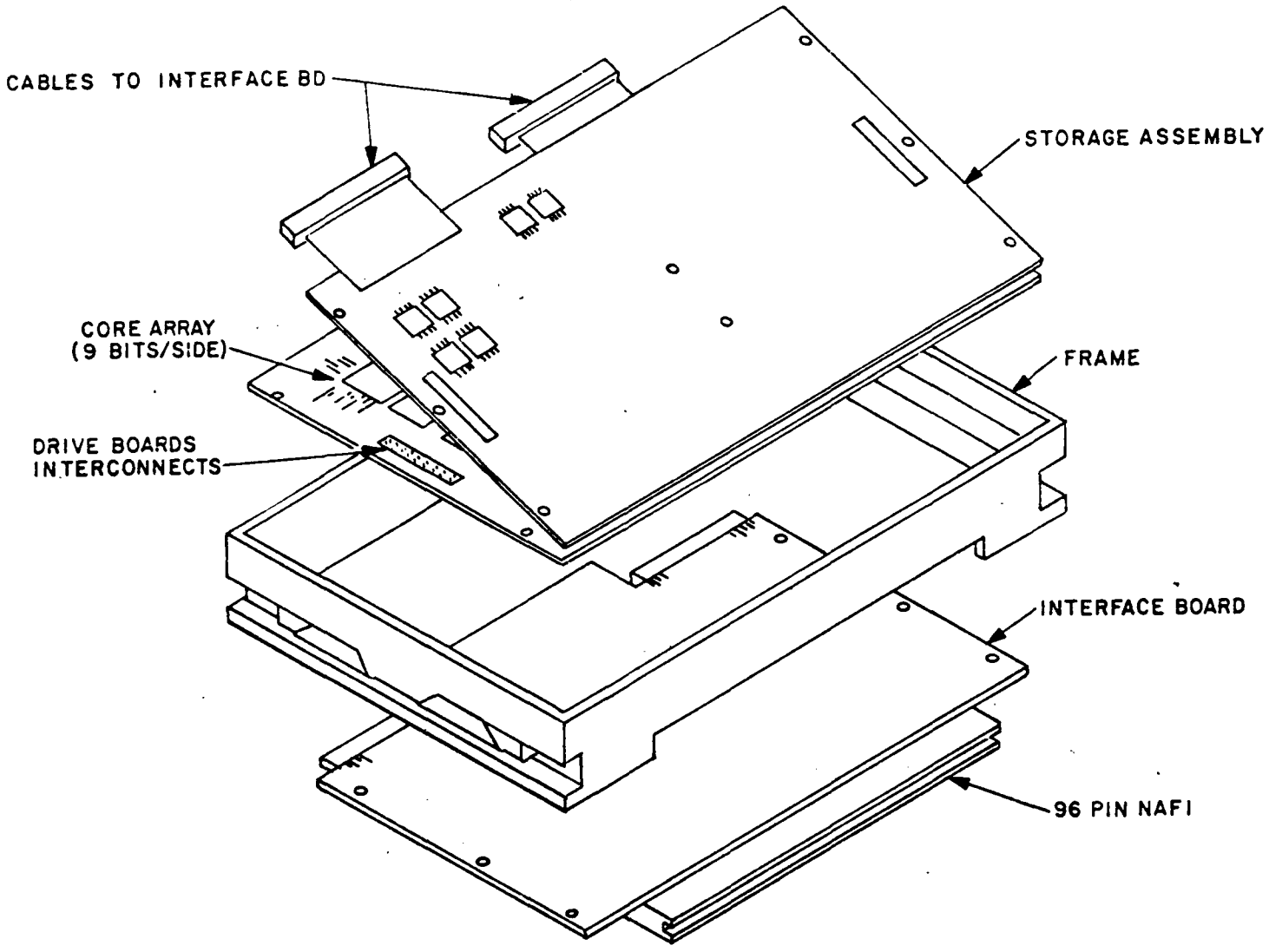


Figure 27 - CDC-9P Configuration (Exploded View)

NAVC-92-138

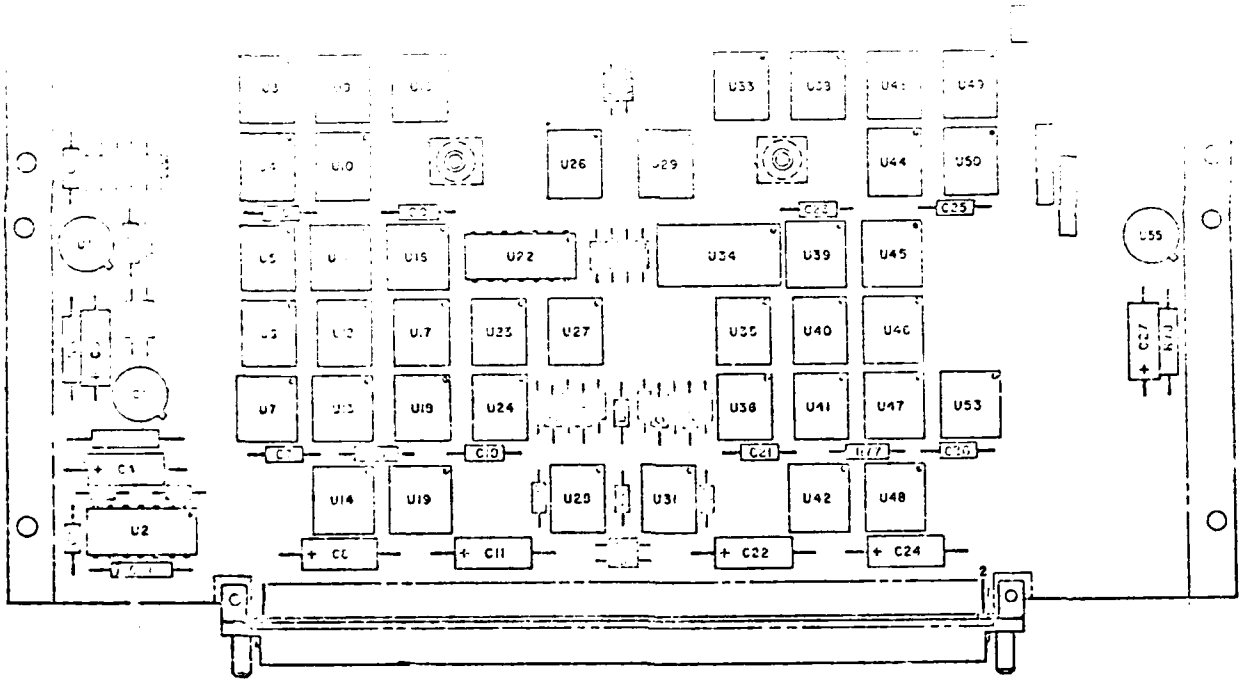


Figure 28 - **Core Memory Module,** Interface Board

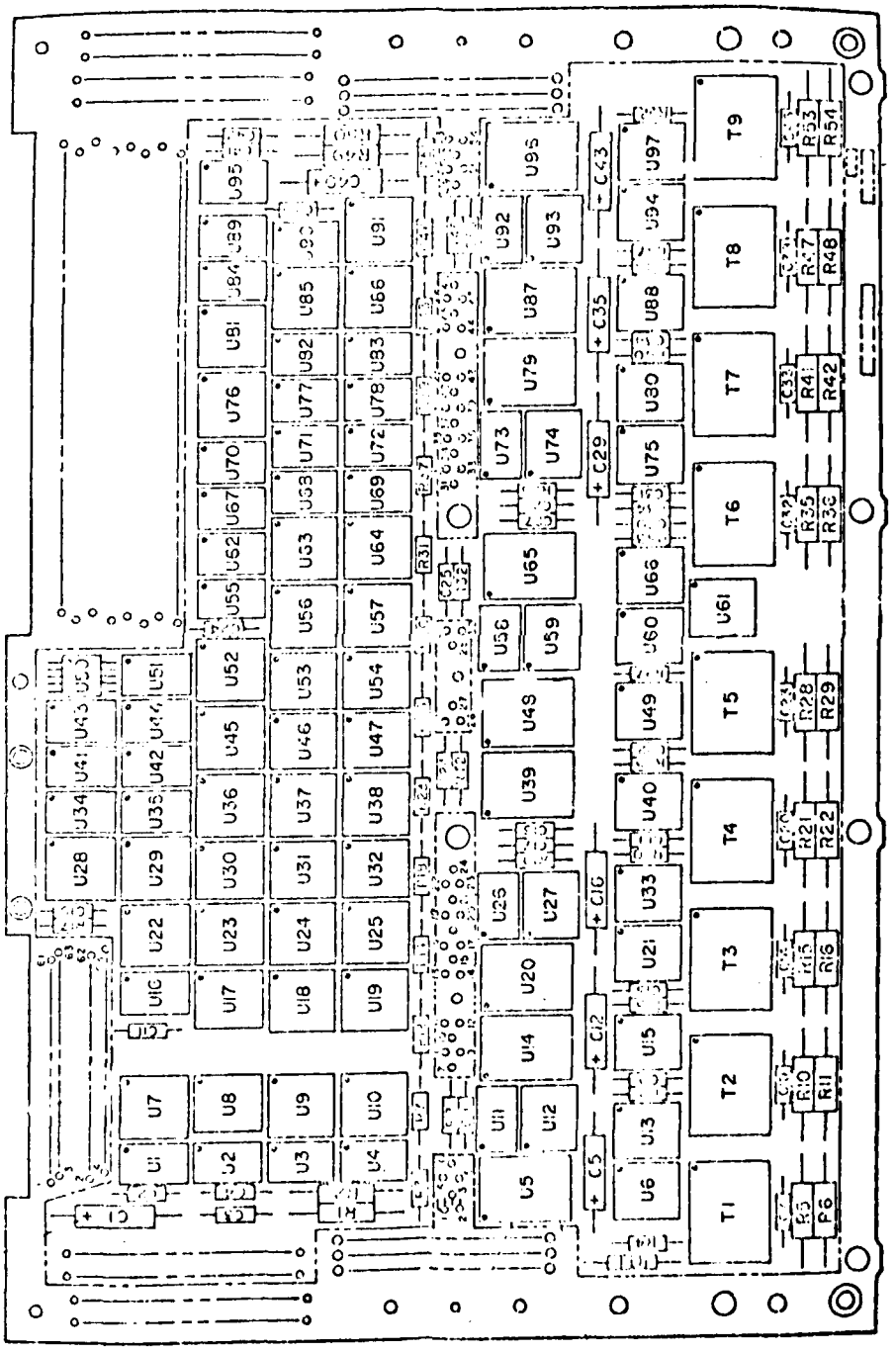


Figure 29 - CMM Storage Assembly or Core Board

[illegible] for the interface
[illegible] the interface timing diagram. The
[illegible] provide the timing and control circuits, the voltage
[illegible] and power protection circuits, and the 96-pin NAFI style inter-
[illegible] module, therefore, consists of only
[illegible] board, two of which are identical. The two as-
[illegible] in aluminum frame with ramp clamps on each side
[illegible] the module in the chassis and an effi-
[illegible] the heat exchanger. The complete module measures

[illegible] mechanical design of the CDC-9P was heavily influenced by serviceability and repairability concepts. While the entire module [illegible] is SRA, it is possible to readily replace either of [illegible] subassemblies. In addition, all components on both subassemblies [illegible] and repairable. Test points are available at the interface connector to monitor critical memory functions during trouble-[illegible] [illegible] points, in addition to all I/O signal pins, can be [illegible] open without causing damage to the module electronics. The 80 twisted-wire organization provides a design that utilizes a [illegible] and component types.

[illegible] Due to the complexity of testing the core memory module, [illegible] is included as Figure 32. In addition, the summary test [illegible] is listed in Table 6.

TABLE 6

[illegible] MODULE (CMM) TEST PARAMETERS

[illegible] subassemblies, double digital circuit card

[illegible] assembly, two multilayer boards

[illegible] board

[illegible] 106 IC's	212 IC's
[illegible] 41 IC's	41 IC's
Total	253 IC's

[illegible] 96-pin NAFI

[illegible]	80 pins
Power [illegible] pins	15 pins
[illegible] required:	95 pins

[illegible] vdc, -12 vdc; 60 watts

[illegible]

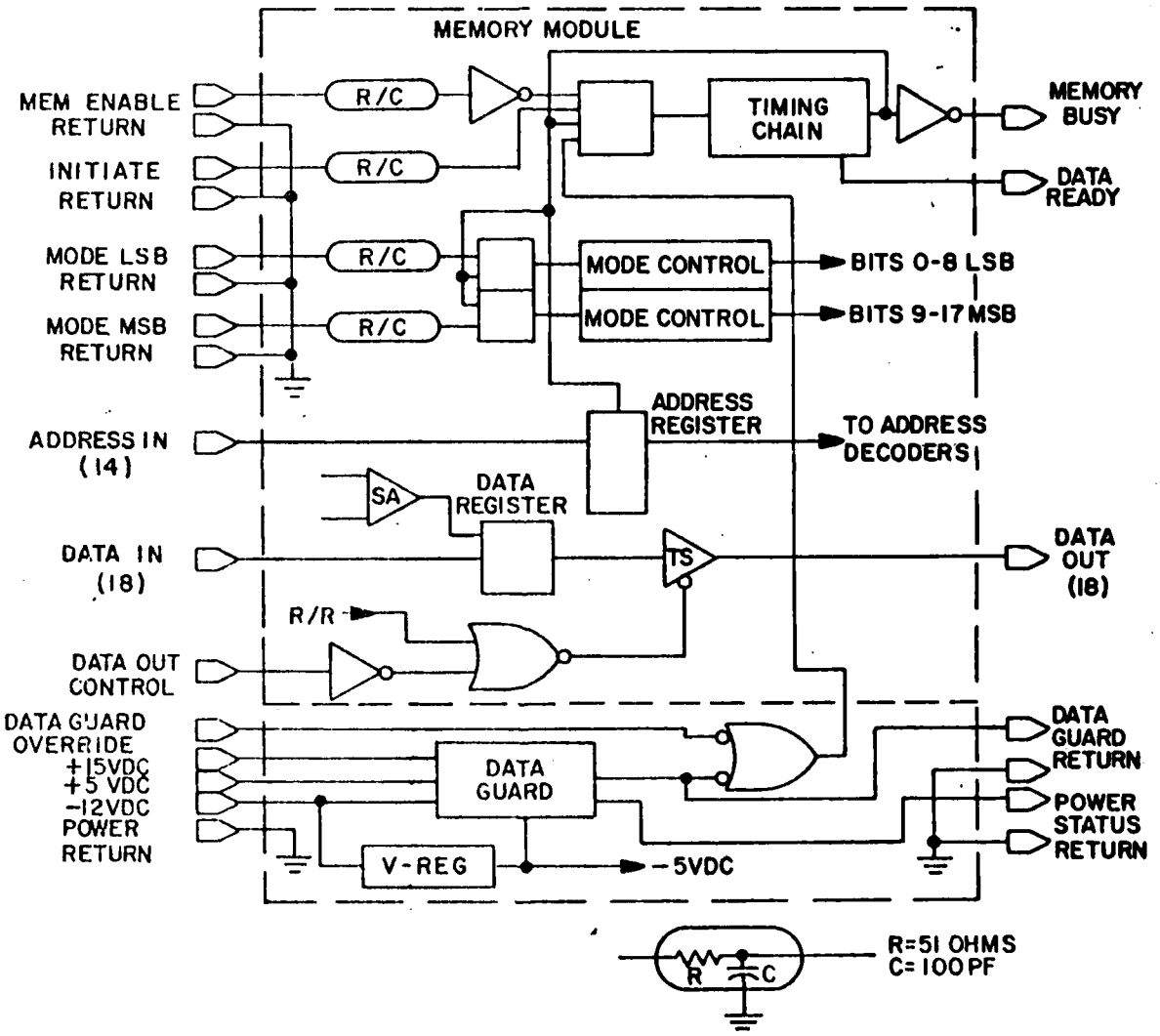
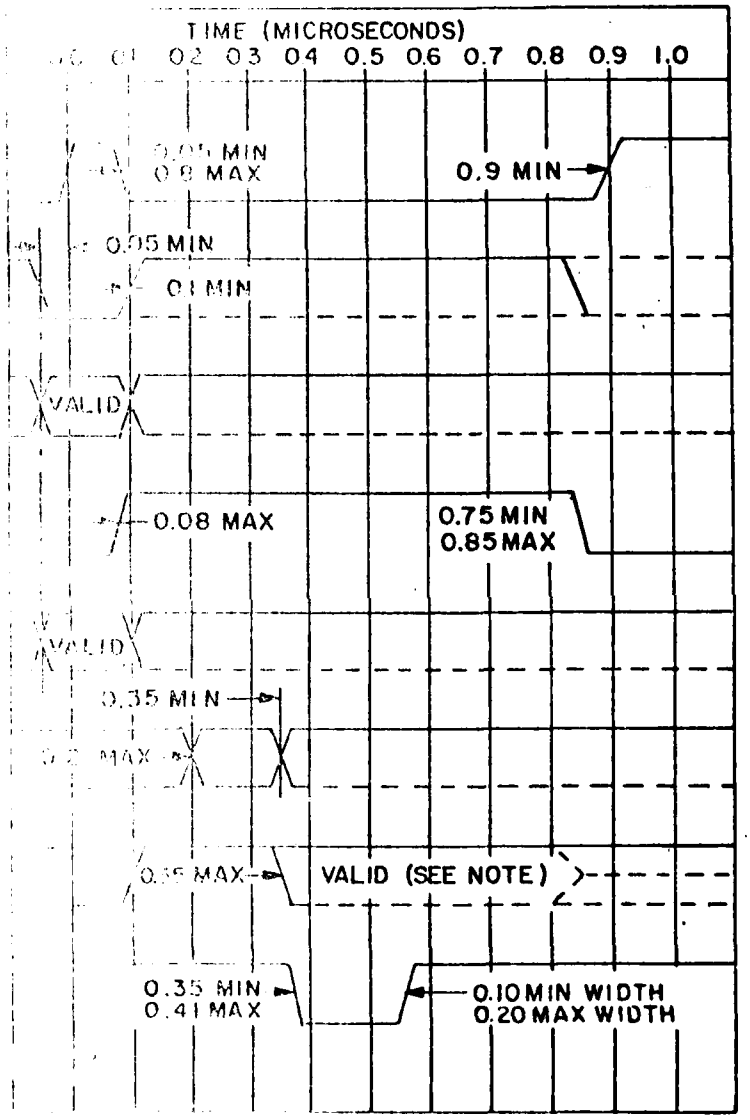


Figure 30 - CDC-9P Interface Diagram



LEVEL ONLY DURING READ/RESTORE CYCLE UNLESS HELD
LOW-LEVEL "DATA-OUT CONTROL" SIGNAL AT I/O

CDC 9P INTERFACE

CDC-9P Interface Timing Diagram

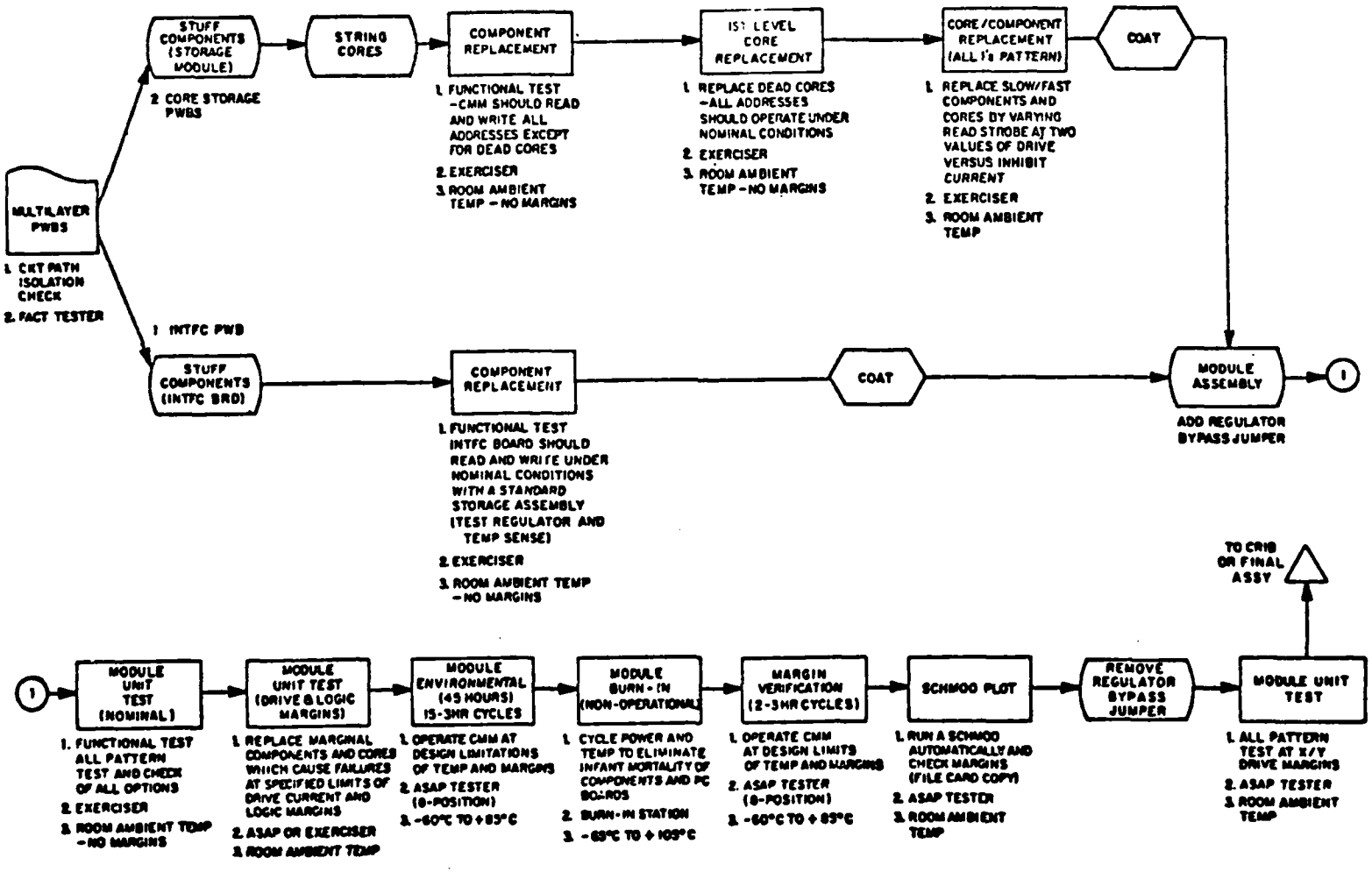
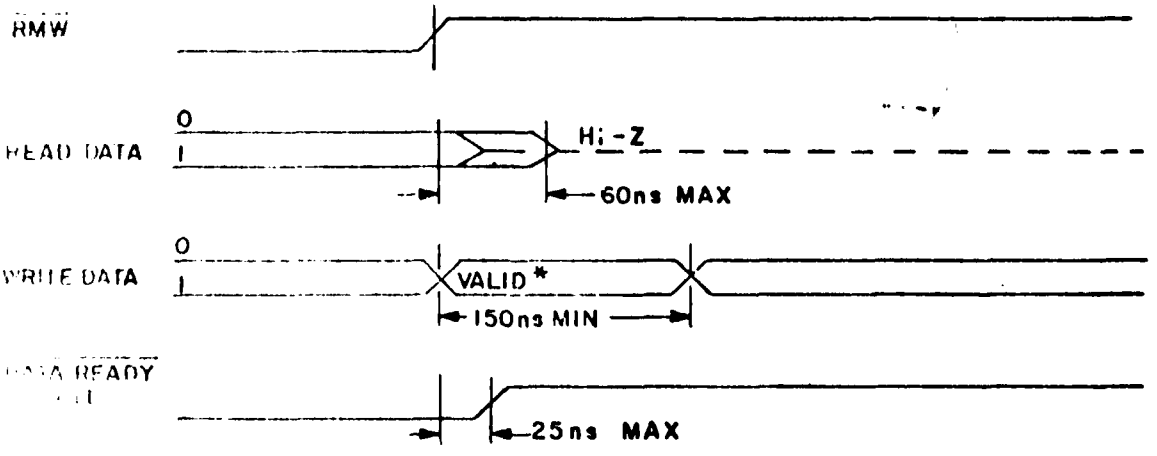


Figure 32 - **Core Memory Module, Test Flow Diagram**

(19) CDC-9P Read-Modify-Write Option. The CDC-9P provides as part of its standard timing and control the ability to perform read-modify-write operations. This feature is controlled via a single interface line designated $\overline{RMW}$. To perform a read-modify-write operation, the $\overline{RMW}$ line is driven to a logic "0" (low) at least 50 nanoseconds prior to the leading edge of the cycle-initiate signal, and the mode-control signals, R/W, must be in the high state (Read-Restore). The CDC-9P memory performs a normal read half cycle (retrieve core data in place on the memory interface bus) and halt with the "Data Ready" signal in its logical low state. When the $\overline{RMW}$ is released (goes to a logic "1"), the core data is dropped from the interface, the write data from the user is gated into an internal register, the "Data Ready" signal returns to its logical high state, and the memory performs the write half cycle. The interface timing diagram at the time of $\overline{RMW}$ release is shown in Figure 33.

(a) The $\overline{RMW}$ input load is as shown in Figure 34. The 1K pull up resistor guarantees a logic "1" level on the $\overline{RMW}$ input when the function is not used or if it is driven by an open-collector driver. The 1K resistor and 100pf capacitor form a filter which rejects low-level, high-frequency noise on the interface.

(b) The design of the read-modify-write function is such that no delay is introduced into normal read-restore or clear-write operations. There is a limit, however, to the length of time that the $\overline{RMW}$ may remain in the logic "0" state following cycle initiate. An internal memory time-out in the memory module will clear the memory timing if the busy flip-flop is set for longer than 10 ±5 microseconds. In the event that this occurs, the addressed data word will be left in all "0" state.



* If Parity Option is installed, write data must be valid an additional 100 ns minimum prior to release of the $\overline{RMW}$ signal.

Figure 33 - Read-Modify-Write, Timing Diagram

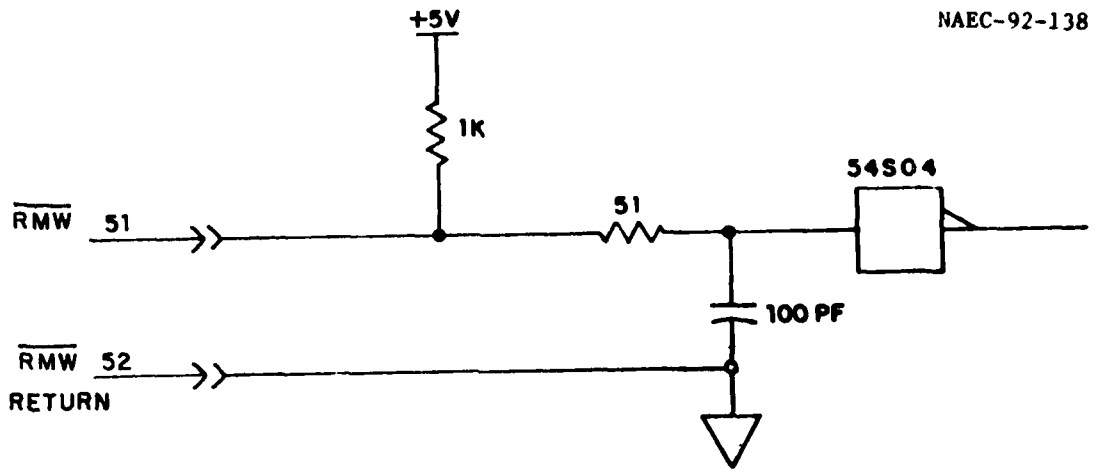


Figure 34 - Read-Modify-Write, Input Load

(11) CDC-9P Parity Option. The parity option for the CDC-9P provides a low-cost means of generating and checking memory parity in cases where only 16 interface data bits are required. The additional two data bits are utilized as parity bits internal to the memory module, one each for the upper and lower half words. The standard interface timing diagram remains valid. Write data must be stable at the memory interface connector no later than 200 nanoseconds after the leading edge of the cycle-initiate signal. Data input pins for data bits 8 and 17 must be open if the parity option is installed, for these are the two bits used as internal parity bits (interface connector pins 41 and 63). Interface connector pins 26 and 92, normally used as the tri-state output for data bits 8 and 17, are used as outputs for parity error lower (PEO) and parity error upper (PEI) respectively. The parity error output signals are active in the logic "0" state and are valid from 100 nanoseconds after the leading edge of "Data Ready" until 400 nanoseconds after the leading edge of "Data Ready," as shown in Figure 35.

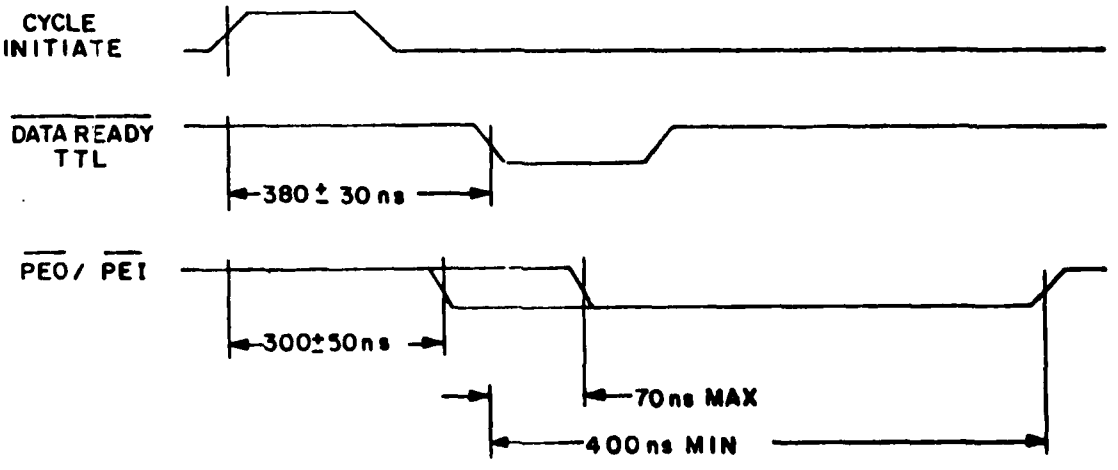


Figure 35 - Core Memory Module, Parity Option

[illegible] (SMM). The SMM provides 16K by 18-bit [illegible] in a single module which is compatible and interchangeable with the CMM [illegible] paragraph C2 above. The features of the SMM are:

[illegible] nanosecond read access time

[illegible] power, 10 watts average for 16K words and 30 watts maximum [illegible]

[illegible] MEMBUS or LMEMBUS

[illegible] Mountable on 1.45-inch centers

(1) A high-speed, electrically alterable SMM has been designed [illegible] for this application. The module provides volatile storage for 16K by 18-bit words, and requires significantly lower power than the [illegible] with the standby and operating modes.

(2) Three prototype SMMs have been assembled and evaluated. The [illegible] have been operating in the CDC 480 computer system since April [illegible]. Electrical and physical compatibility with the CMM has been verified, and mixed operation of CMM and SMM has also been proven.

(3) The SMM operates with read and write cycle times of less [illegible] nanoseconds and a read access time of less than 300 nanoseconds. [illegible] are generated by tapped delay lines and S/R flip-flops [illegible] a power-up master clear circuit. Separate mode control [illegible] permit independent operation of each 9-bit byte in either the read [illegible] modes. Input supply voltages are the same as the CMM (that is, +5, [illegible]).

(4) Voltage monitoring circuits provide a power status signal [illegible] connector to signify when all supply voltages are within [illegible] tolerance. A data guard signal locks out memory references [illegible] voltages drift more than 4 percent from their normal [illegible] memory references are locked out, the +15-volt input can drop [illegible] and the -12-volt input can drop to -8 volts before data in the [illegible] circuit will be destroyed. Typical power requirements at [illegible] watts standby or 21 watts when operating a 400-nanosecond [illegible].

(5) The SMM circuits are contained on two multilayer printed [illegible], which are attached to a common frame and interconnected by [illegible] connectors. One board includes 16K bytes of memory; [illegible], control, drive, input, and output circuits; and the interface [illegible] The second board includes the other 16K bytes of memory, addi[illegible] circuits, and a voltage regulator. The total module weight is [illegible] pounds.

(6) The module design is based on a fully static 4K by 1 metal oxide semiconductor (MOS) RAM integrated circuit, the SEMI 4200, manufactured by Electronic Memories and Magnetics Corporation, with second source available from General Instruments. The device is packaged in a 22-pin, side-brazed ceramic dual in line package. Dynamic memory devices were not considered acceptable for this application because of their susceptibility to "soft" or intermittent errors, their high refresh rates at elevated temperature, and the loss of memory access during refresh intervals. Reliability is affected by both the higher failure rates of the dynamic devices and the additional components of the refresh circuitry. Refresh-related problems also make fault isolation and maintainability much more difficult than for a design based on static devices.

(7) The test parameters for the SMM are presented in Table 7.

TABLE 7

SEMICONDUCTOR MEMORY MODULE TEST PARAMETERS

SRA Configuration: Double digital circuit card SRA
*IC count:
*Connector pin count:
*Power requirement:
*Cycle time:
*Access time:
*Data not available; SMM in development.

a. INPUT/OUTPUT SUBSYSTEM SRAs. The I/O channel structure of the AN/AYK-14(V) computer system provides for communications between the computer and peripheral equipment and/or other AN/AYK-14(V) computers. Each of up to 16 I/O channels in a given computer configuration may be assigned a unique 4-bit channel logical number which the software uses to address the given channel. A second unique 4-bit channel priority number is defined for each I/O channel in a given configuration by the physical I/O channel module location for use in resolving possible conflicts among the several I/O channels. Available I/O channel types include the following:

- Discrete
- Serial 1553A (1 MHz)
- Serial NYDS (10 MHz)
- Serial RS-232 C asynchronous (selectable baud rate)
- Serial Proteus (10 MHz)
- Parallel NTDS slow (-15 v)
- Parallel NTDS fast (-3 v)
- Parallel NTDS ANEW (+3.5 v)

a. Discrete Interface Module (DIM). The DIM (Figure 36) is used to provide a convenient interface for communications single-bit status, event, and control information between user devices and the computer. The DIM I/O channel module provides the following I/O interfaces:

- 8 external interrupts with individual mask bits and program-selectable priority. These appear to the software as class III, F 11 interrupts.
- 32 bidirectional discretes (DIO) program selectable in groups of four as input or output signals.
- 16 input discretes (DID).
- 16 "switch closure" input discretes (DIS)

(1) The DID and DIS inputs are accessible only through a jumper from the top of the DIM, and are available only when the DIM is installed in SRA location A02 in certain AN/AYK-14(V) chassis configurations.

(2) While the DIM communicates with external equipment via discrete lines, the software interface to the DIM is via 16-bit parallel words. If a given output bit is desired to be set, an "image word" in main memory

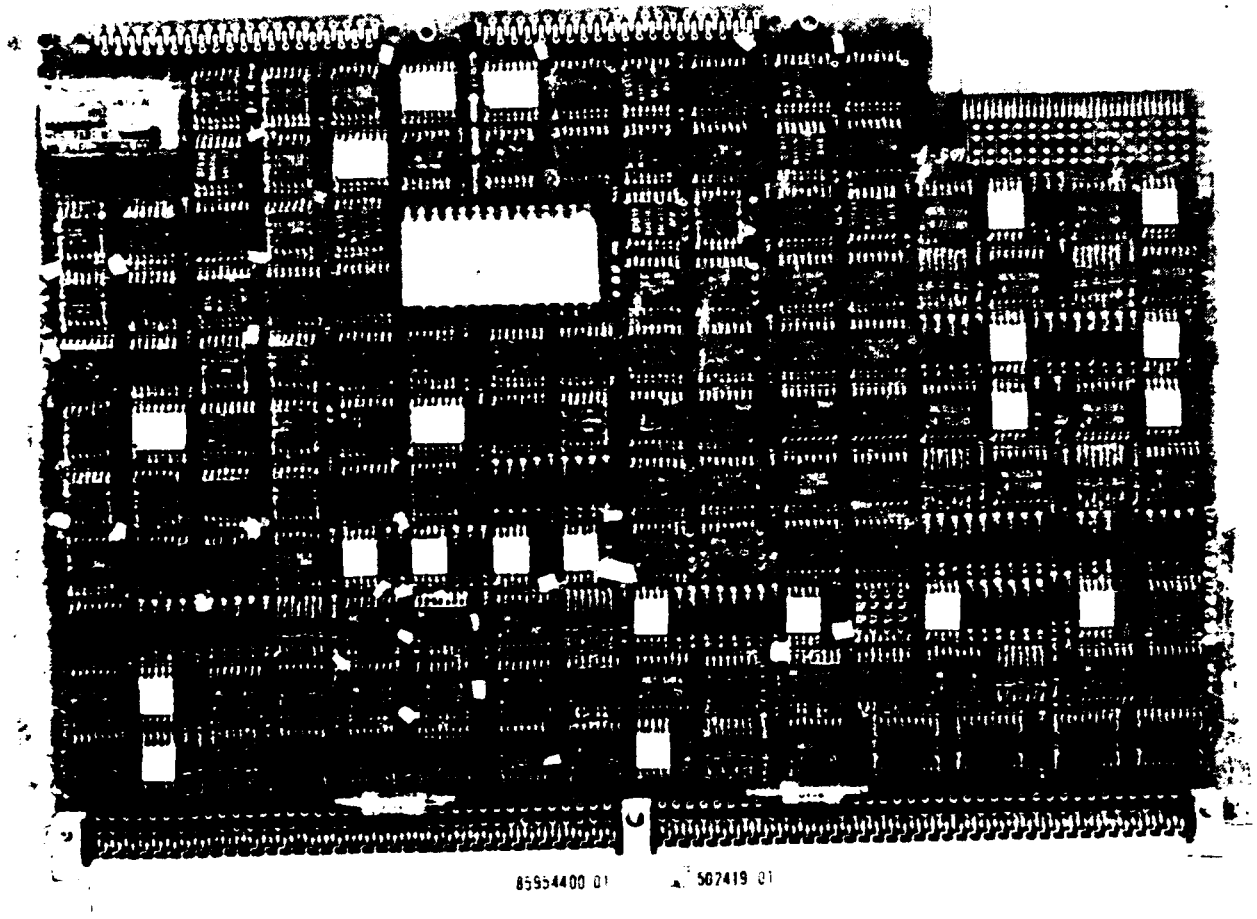


Figure 36 - Discrete Interface Module (DIM)

would be set and the entire word output to the DIM. For inputs, an entire 16-bit word is read into memory from the DIM and an individual bit then tested. This feature permits use of DIM discretes in a parallel channel mode.

(3) Input and output transfers between DIM and main memory are initiated via an Initiate Message (E2 hex) or Initiate Transfer (E3 hex) instruction executed in an I/O channel program. Either input or output (but not both) chaining can be active at any given time. The DIM circuit card assembly is shown in Figure 37.

(4) The DIM as shown in Figure 38 contains an IOBUS interface implemented in the same manner as all other I/O channel types. As with all channel types, this portion of logic includes IOBUS transceivers, IOBUS interface control signals, and sequencing logic necessary to interface between the module hardware and the IOC via the IOBUS. For discussion purposes, the remainder of the DIM logic is partitioned into the output discrete section, the input discretes section, and the event and interrupt inputs section. The DIM consumes about 11 watts on a 6-inch by 9-inch module.

(5) The output discrete section includes 32 transistor-transistor logic (TTL)-*compatible differential* transmitters and 32 output latches or flip-flops. These latches are implemented with addressable latch medium scale integrated (MSI) circuits using only four integrated circuit packages.

(6) The input discrete section contains 34 receivers, two of which are special for the reset and bootstrap load initiate signals. These two signals are routed into the event and interrupt section of the DIM. The remaining 32 inputs are grouped into two sets of 16 and multiplexed to the IOBUS interface for input to the IOC.

(7) The two special discretes plus eight external interrupt inputs are routed through the event and interrupt section to PSM-2 of the IOC (PSM-1 if the CPU subsystem is used). The interrupt control, however, provides mask register and priority, both definable by the software by means of firmware.

(8) The DIM provides differential TTL interfaces including 32 output discretes, 32 input discretes, 8 external interrupt inputs, and 2 special event inputs.

(9) The input/output main timing for the DIM, PROTEUS, and NTDS is shown in Figure 39. The testing parameters for the DIM are listed in Table 8.

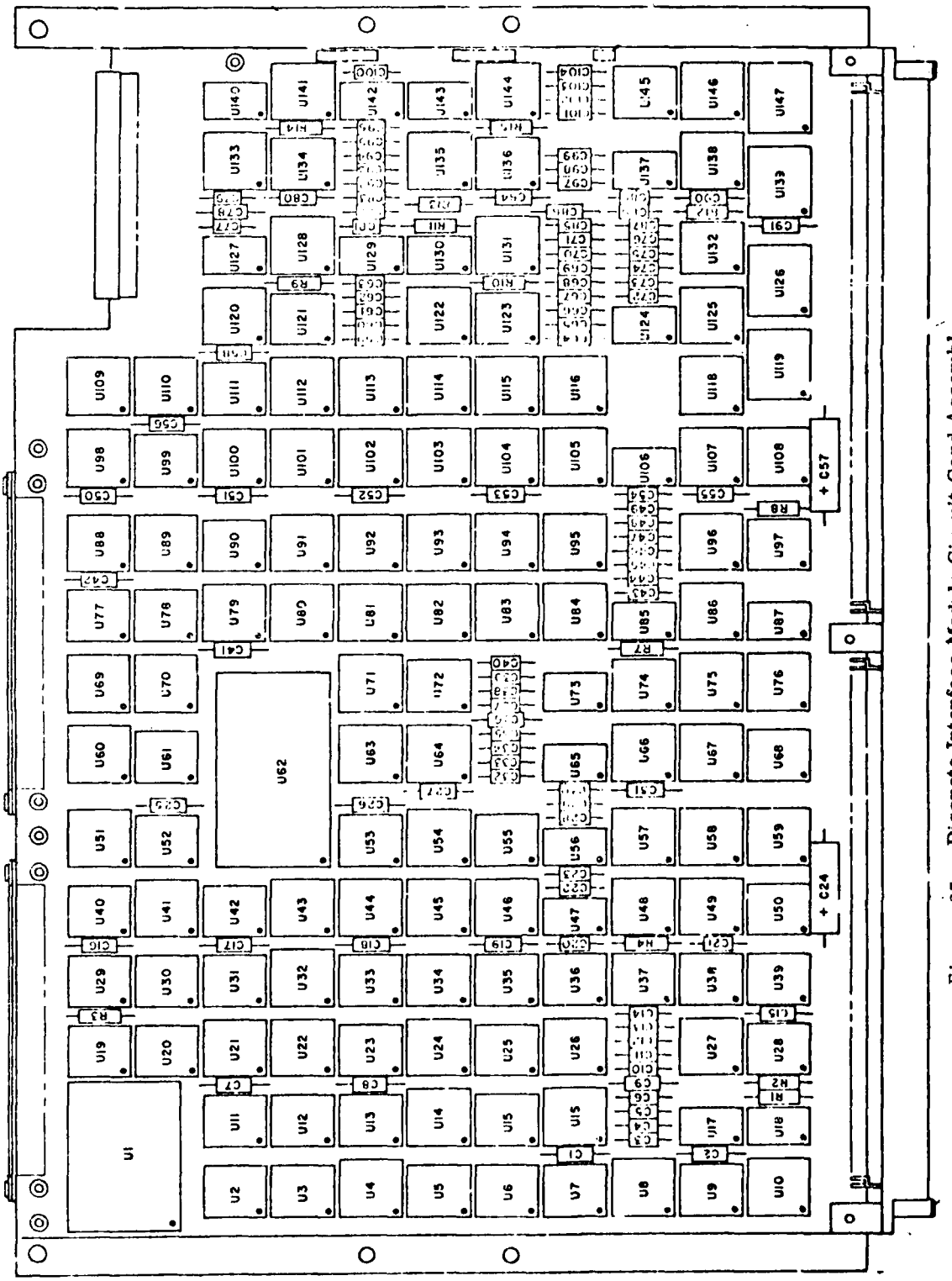


Figure 37 - Discrete Interface Module, Circuit Card Assembly

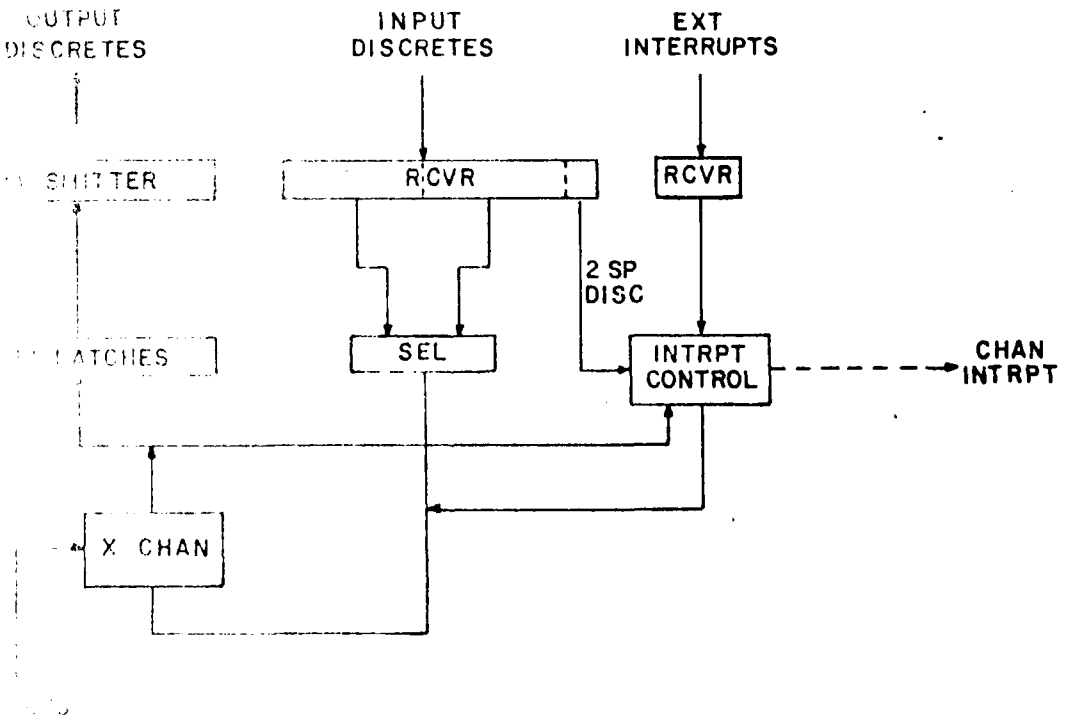


Figure 38 Discrete Interface Module, Block Diagram

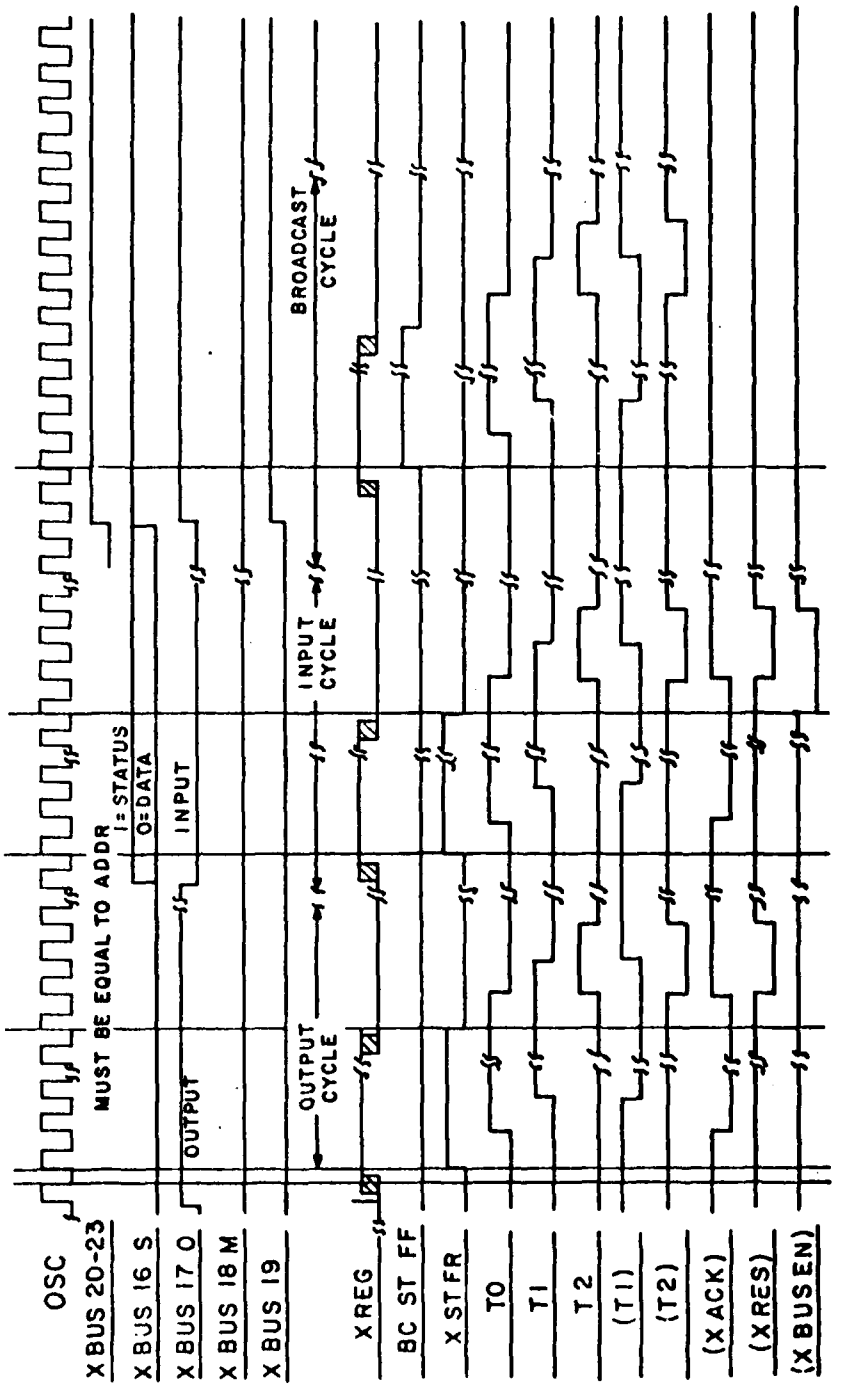


Figure 39 - Input/Output Main Timing (DIM, PROTEUS, and NTDS)

TABLE 8

[illegible] FUNCTIONAL MODULE (DFM) TEST PARAMETERS

[illegible] digital [illegible] SRA		
[illegible]		
[illegible] pin count: one [illegible] pin connector		= 152
[illegible] pin connectors		= 82
64-pin cable		= 64
Total		298
Signal I/O pins		133 pins
[illegible]		72 pins
Total I/O		205 pins
Cable (signals)		64 pins
[illegible]		20 pins
Total required		289 pins

[illegible] required = [illegible] vdc, 2.8 amp, 14 watts

[illegible]: U1, 32 MHz; U2, 16 MHz; U70, 4 MHz; U69, 8 MHz

[illegible]: X bus, 16 bits (bits 0-15)

[illegible]: Interrupts, 8 (16 pins)

"[illegible]" interrupts, 8 (16 pins)

"DI" interrupts, 0-32 I/O (64 pins)

[illegible]: Recognize interrupts and obtain status words

b. Serial Interface Module (SIM). The SIM implements a serial multiplex data channel meeting the channel control and format characteristics of MIL-STD-1553A. This channel type is the standard intersystem communication facility on board modern military aircraft. The SRA interfaces to two 1553 buses for redundant operation.

(1) The SRA can operate with any MIL-STD-1553A protocol and can function as either a bus controller or remote terminal unit. Information is transferred on a single, shielded, twisted pair line at a 1-MHz bit rate. Data is transferred in 20-microsecond frames, each divided into 17-bit times of 1 microsecond and one 3-microsecond sync interval. All messages are addressed and use three types of words:

- o Command word - sent by bus controller to address appropriate terminal, specify message type, and set data word count for subsequent transfer.
- o Status word - set by a terminal in response to command word. Identifies terminal and reports status.
- o Data word - contains 16 bits of message data, sync pattern, and a parity bit.

(2) The SIM I/O channel provides the following modes of operation:

- o Bus Controller (BC) - controls and initiates all data transfers on the 1553A bus.
- o Remote Terminal (RT) - responds to BC requests for transmission and reception.
- o Bus Monitor (BM) - monitors bus for activity and stores every word when received on the bus.
- o Off - no channel activity.
- o Self-Test (ST) - is a subset of "Off" in which an internal wraparound test is performed. No data is transmitted or received on the bus.

(3) The SIM channel operation meets the requirements of MIL-STD-1553A. The channel structure provides for up to 32 users per bus. Messages on the bus start with one or two command words from the BC, followed by status word from the RT and up to 32 data words.

(4) The SIM incorporates parallel-to-serial conversion, word formatting, sync detection, word decoding, and message control, with hardware programmability by means of FPLA circuits. The SIM SRA is shown in Figure 40, and the SIM circuit card assembly is shown in Figure 41.

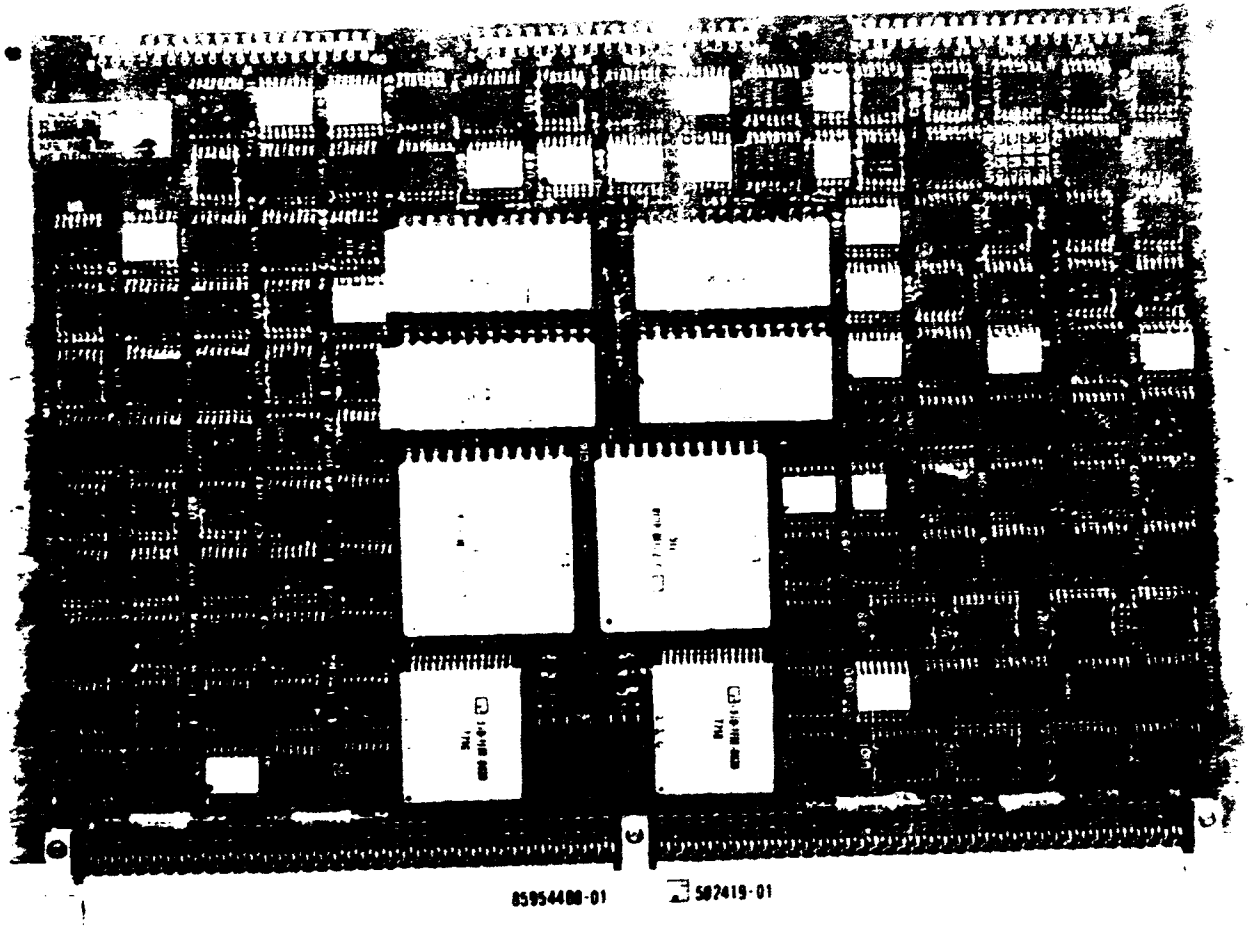


Figure 40 - Serial Interface Module (SIM)

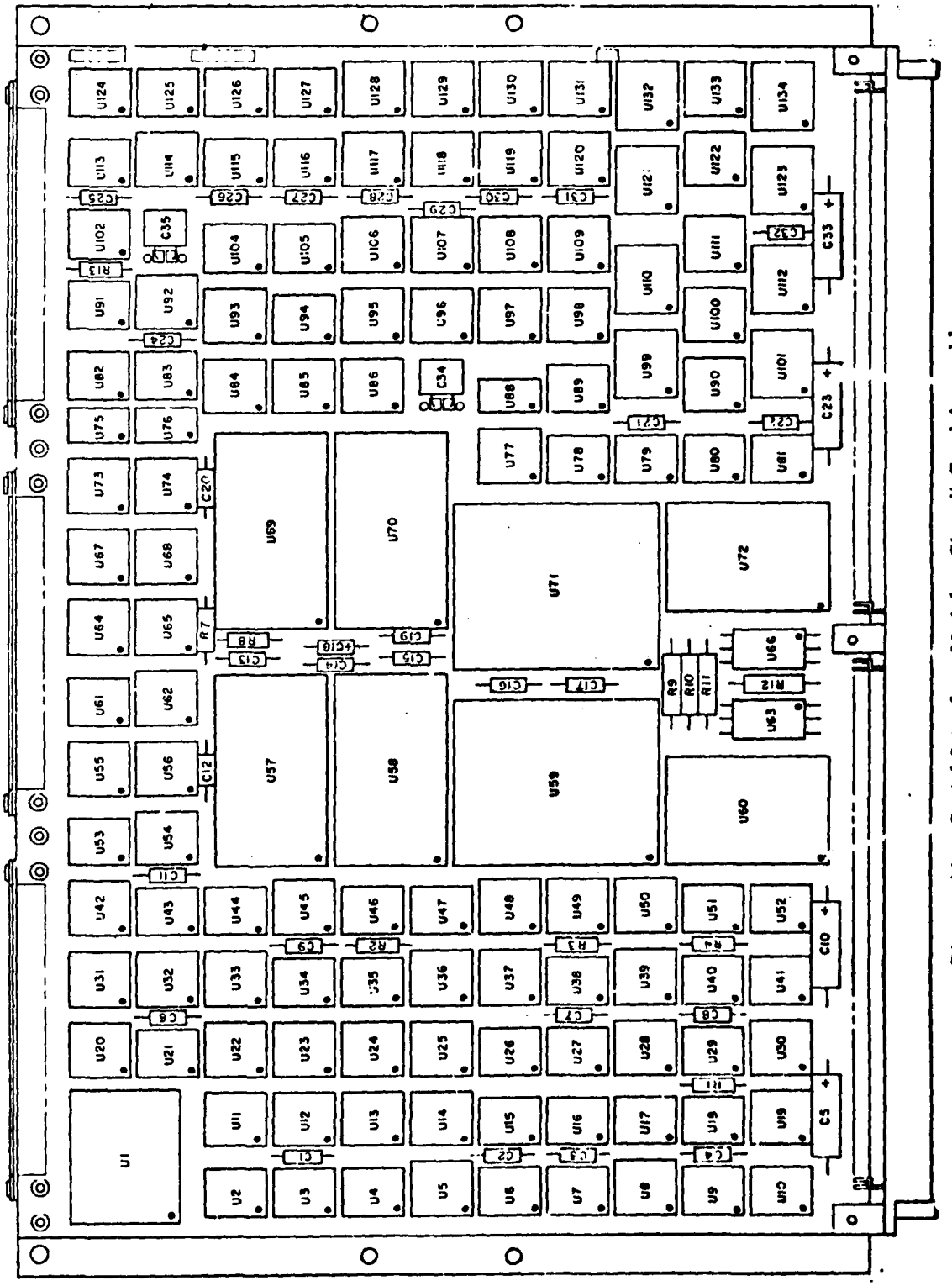


Figure 41 - Serial Interface Module, Circuit Card Assembly

... principal I/O channel type module in the AN/... computer. This module provides an interface to the state-of-the-art airborne multiplex bus data transmission schemes. The FPLA circuits discussed in this section are utilized in the SIM implementation to achieve extreme flexibility and allow future adaptation to varying message protocols.

(6) A basic block diagram of the SIM is shown in Figure 42. ... module contains an interface to the IOBUS with logical channel code defined by back panel wiring in the chassis. The portion of the diagram labeled XCHAN includes the IOBUS transceivers, the IOBUS interface control signals, and the sequencing logic necessary to interface between the rest of the SIM and the IOC by way of the IOBUS. The output section of the SIM includes a data buffer, a parallel-to-serial shift register, a word-encoding section of logic, and dual transmitters into the transformer interfaces with the dual 1553A buses. The receiver section of the SIM contains two receivers fed by the dual 1553A busses, word decode logic, a serial-to-parallel shift register, and a data buffer for receiver words. The section of the SIM block diagram labeled MESSAGE CONTROL sequences words within message block transfers and performs the required automatic status responses and error handling.

(7) Three portions of the SIM (the encode logic, the decode logic, and the message control) are implemented in a unique scheme with minimal hardware yet extremely flexible programmability. A single FPLA circuit is utilized in each of these three portions of logic.

(8) Several hardwired and microprogrammed schemes for implementing the SIM have been investigated by Control Data. None of these schemes has yielded a more minimal package count nor a more flexible and programmable architecture than the proposed design. The presently operational breadboard SIM has demonstrated that FPLA packages are more powerful and appropriate for this logic application than are PROM packages.

(9) The encode logic combines a single FPLA integrated circuit ... with a bit counter and a state register. A clock signal, initiate ... and a data bit stream from the parallel-to-serial shift register are fed to this logic. The encode logic, in turn, generates sync pattern, Manchester-coded serial bit waveforms to the transmitters, and provides load and shift enable control to the shift register. When initiated by the message control, the encode logic is given a message mode code which defines the desired format for the word encoding. Any one of eight different formats may be defined. These include sync polarity, sync error, data bit error, and even or odd parity definition. This enables transmission of ... only valid words onto the 1553A bus, but also words with sync errors, Manchester-code errors, or parity errors. Thus, a built-in diagnostic ... facility is provided for the SIM module.

(10) In the encode logic portion of the SIM, all of the characteristics of the transmitted bit stream are programmed into the FPLA in ... decode logic. Any change in these characteristics (that is, more or fewer bits per word or sync pattern redefinition) are easily accommodated

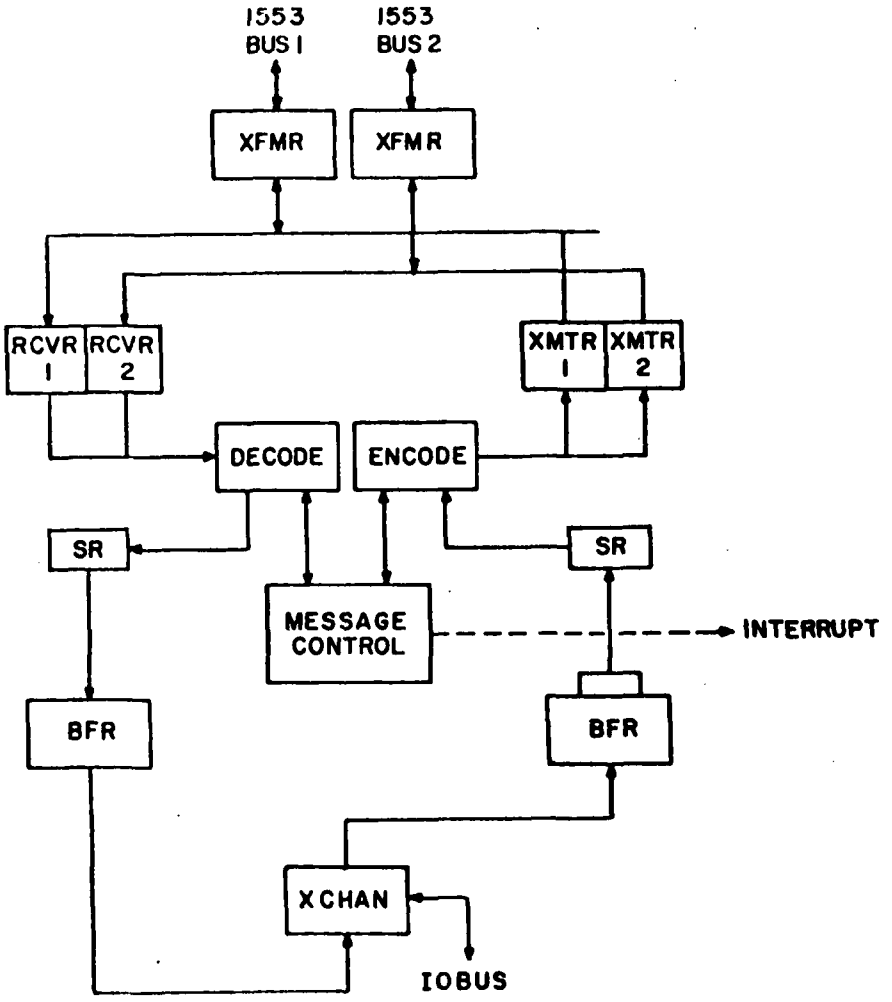


Figure 42 - Serial Interface Module, Block Diagram

changing the FPLA program. The presently operational SIM at Control Data utilizes 37 min-terms of the total 48 available in the FPLA within the encode logic. This entire function, including sync generation, bit counting, parity generation, and error insertions, is implemented in a total of only six integrated circuit packages.

(11) The decode logic performs sync detection and extraction, bit stream determination, parity checking and bit counting using a digital sampling scheme. This logic is again implemented with a FPLA plus a sampling register, a bit counter, and a state register. The bit samples, along with state and bit counter values, are fed into an FPLA. The program in the FPLA controls the sequencing of the state register and the advances of the bit counter based upon detected transition times of the sample signals. Decisions associated with error conditions and valid/invalid received words are programmed into the FPLA. The breadboard SIM utilizes only 9 integrated circuit packages and 37 terms of the total 48 in the FPLA for this entire function.

(12) The message control logic is the third portion of the SIM that utilizes an FPLA circuit. It accepts a message or channel mode register, the status of the decode logic, and field of input words in the serial input register. Its function is to monitor input command and status words, identify and compare unit number assignments, and perform status response initiation to the encode logic and interrupt initiation to the IOC when [illegible]. The message or channel mode is defined by means of the IOBUS [illegible] and enables the channel to perform as a command controller, remote terminal, or newly defined protocol scheme such as polling controller or polled terminal. The protocol characteristics are programmed into the FPLA and lend great flexibility to the SIM. Other mode information has also been used in FPLA programming to force the receiver to monitor its own transmitted messages and provide "looped around" self-test of the SIM.

(13) The test parameters for the SIM are shown in Table 9.

TABLE 9

SERIAL INTERFACE MODULE TEST PARAMETERS

SRA configuration: Single digital circuit board SRA		
IC count: 133 IC's		
Connector pin count:	Three top 41-pin connectors	- 123 pins
	One bottom 152-pin connector	- 152 pins
	Total	- 275 pins
Signal I/O pins		67 pins
Test point pins		94 pins
	Total I/O pins	- 161 pins
Power/ground pins		22 pins
	Total required	- 183 pins
Power required: +5 vdc, -12 vdc, +15 vdc; 3.2 amp, 1.3 amp, 1.1 amp; 16 watts		
Bidirectional lines: X bus (16 pins)		
Differential: 6 output (12 pins)		
Oscillator: 1 MHz		

(2) NTDS Interface Modules (NIM). There are four types of NIM's, each capable of operation according to MIL-STD-1397:

- NTDS Fast - 16-bit parallel transfer of up to 250,000 words per second. Binary voltage of 0 vdc (logical 1) and -3 vdc (logical 0).
- NTDS Anew - 16-bit parallel transfer of up to 250,000 words per second. Binary voltage levels of 0 vdc (logical 1) and 3.5 vdc (logical 0).
- NTDS Slow - 16-bit parallel transfer of up to 41,667 words per second. Binary voltage levels of 0 vdc (logical 1) and -15 vdc (logical 0).
- NTDS Serial - serial data transfer of up to 10 megabits per second on one cable. Bipolar ±3.25-volt signals.

(1) Channel interface lines for NTDS fast, slow, and ANEW are shown in Figure 43 and channel interface lines for Serial are shown in Figure 44. Two NIM parallel channels can be operated together to form a 32-bit-wide parallel channel. Transfer operation on the serial channel involves the use of 48-bit control frames and 34-bit data frames (32-bit message data, function, or interrupt code, and 1-bit word ID, 1-bit sync), according to procedures defined in MIL-STD-1397. The modules support operation in computer-to-computer, [illegible] externally specified addressing modes as described in [illegible].

(2) A parallel data channel is 16 bits wide and contains two associated bits to perform the handshake control required. The parallel I/O [illegible] an input data channel and an output data channel, each with its two control bits. One I/O channel requires 18 transmitters and 18 receivers to convert the TTL logic levels to the applicable NTDS channel levels. Two I/O channels [illegible] single 6- by 9-inch module.

(3) The NTDS Fast (Figure 45) and the Anew (Figure 46) data channels [illegible] same type of dual integrated circuit receiver. Discrete resistors are [illegible] line terminators to meet the required tolerance. A capacitor and bias [illegible] complete the circuit requirements. The NTDS Fast transmitter uses a [illegible] level translator and an inverter for each driver. A totem pole type of [illegible] is formed between -5 volts and ground using the two translators. One [illegible] is driven by the signal and the other by the inverted signal. A line [illegible] used as the Anew transmitter. It is a derivative of the MC205, a type [illegible] same Anew interfaces.

(4) The NTDS Slow interface (Figure 47) uses two hybrid circuits from [illegible] Technology, Inc. Their CT510 driver and CT511 dual receiver are designed [illegible] the Slow interface specification.

(5) The NTDS Serial I/O channel (Figure 48) has two bidirectional [illegible], an input line and an output line, which send both data and control [illegible] as a stream of phase-modulated pulses. The pulse stream format differentiates control information from data words. A comparator with feedback to add [illegible] 40.5-volt hysteresis is used as a receiver for the Serial channel.

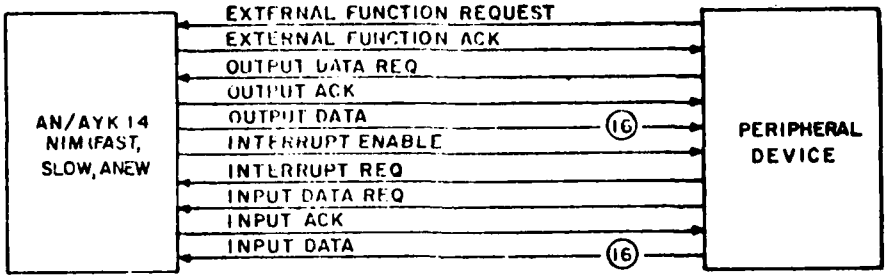


Figure 43 - NTDS Slow, Fast, and Anew Channel Interface

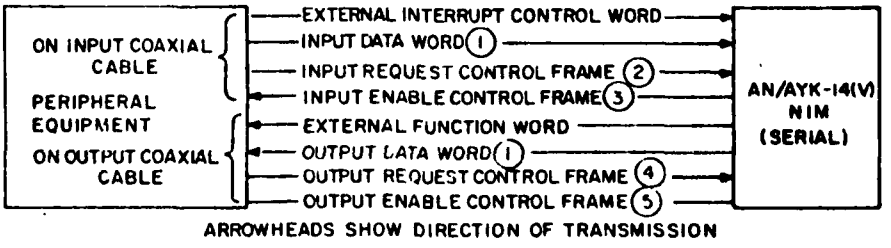


Figure 44 - NTDS Serial Channel Interface and Message Format

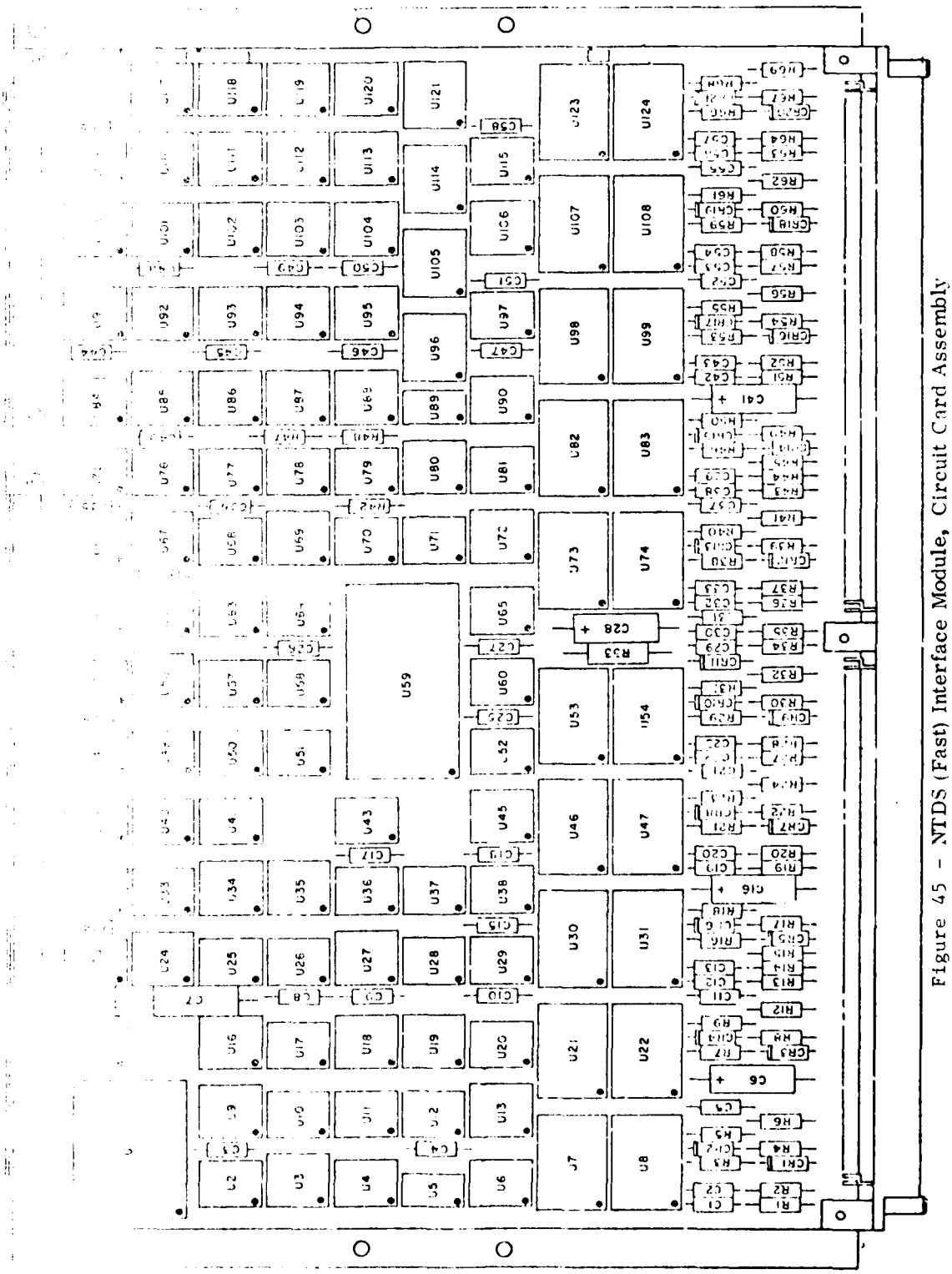


Figure 45 - NTDS (Fast) Interface Module, Circuit Card Assembly

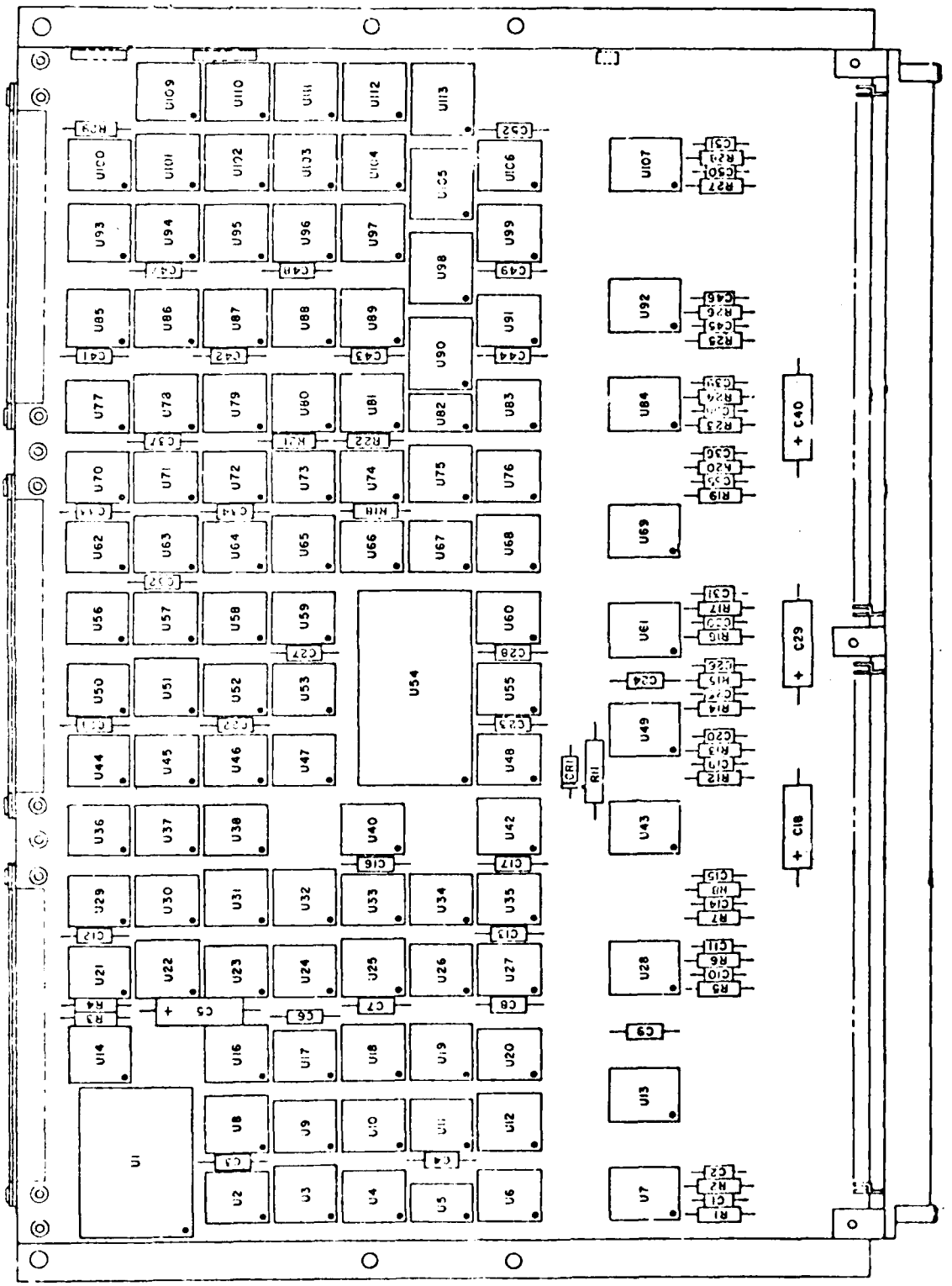


Figure 46 - NTDS (ANEW) Interface Module, Circuit Card Assembly

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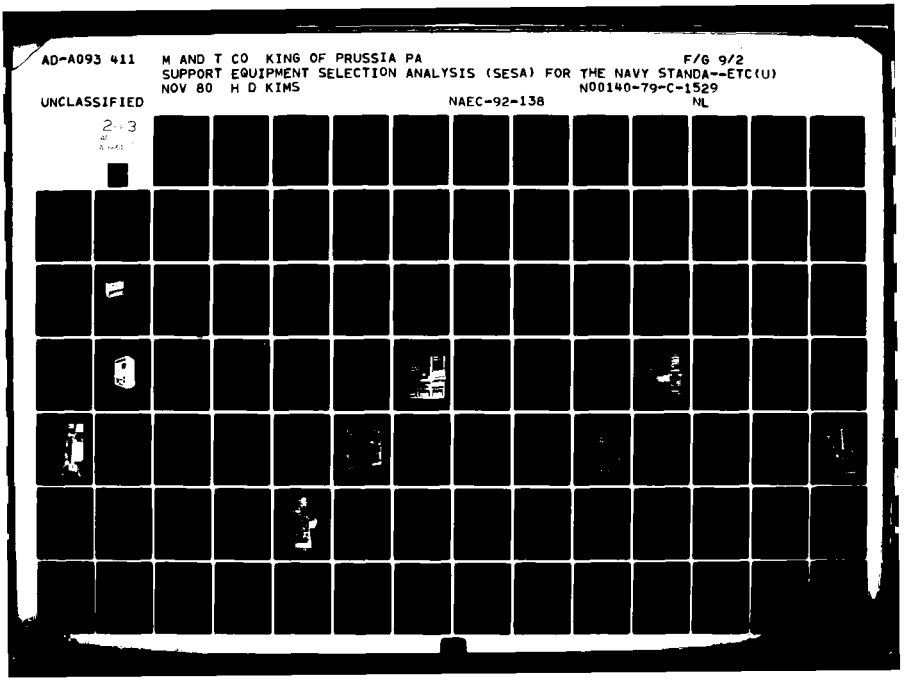
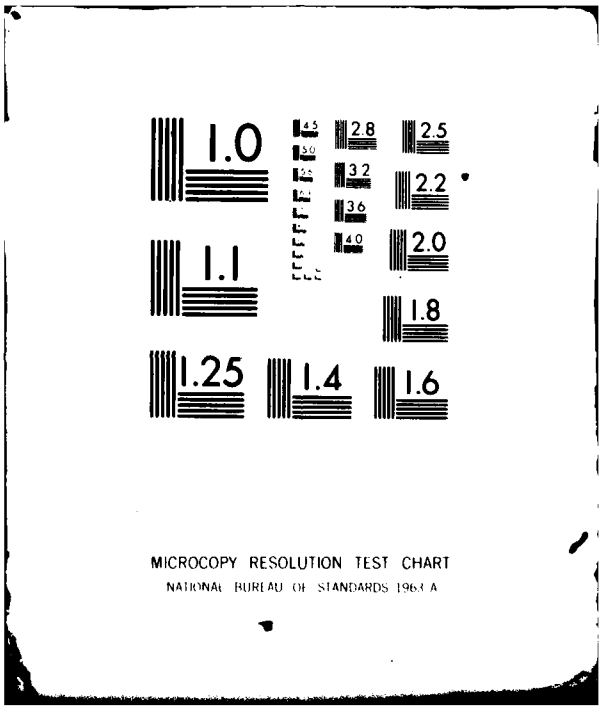
SUPPORT EQUIPMENT SELECTION ANALYSIS (SESA) FOR THE NAVY STANDA--ETC(U)
NOV 80 H D KIMS N00140-79-C-1529
UNCLASSIFIED NAEC-92-138 NL




1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963 A

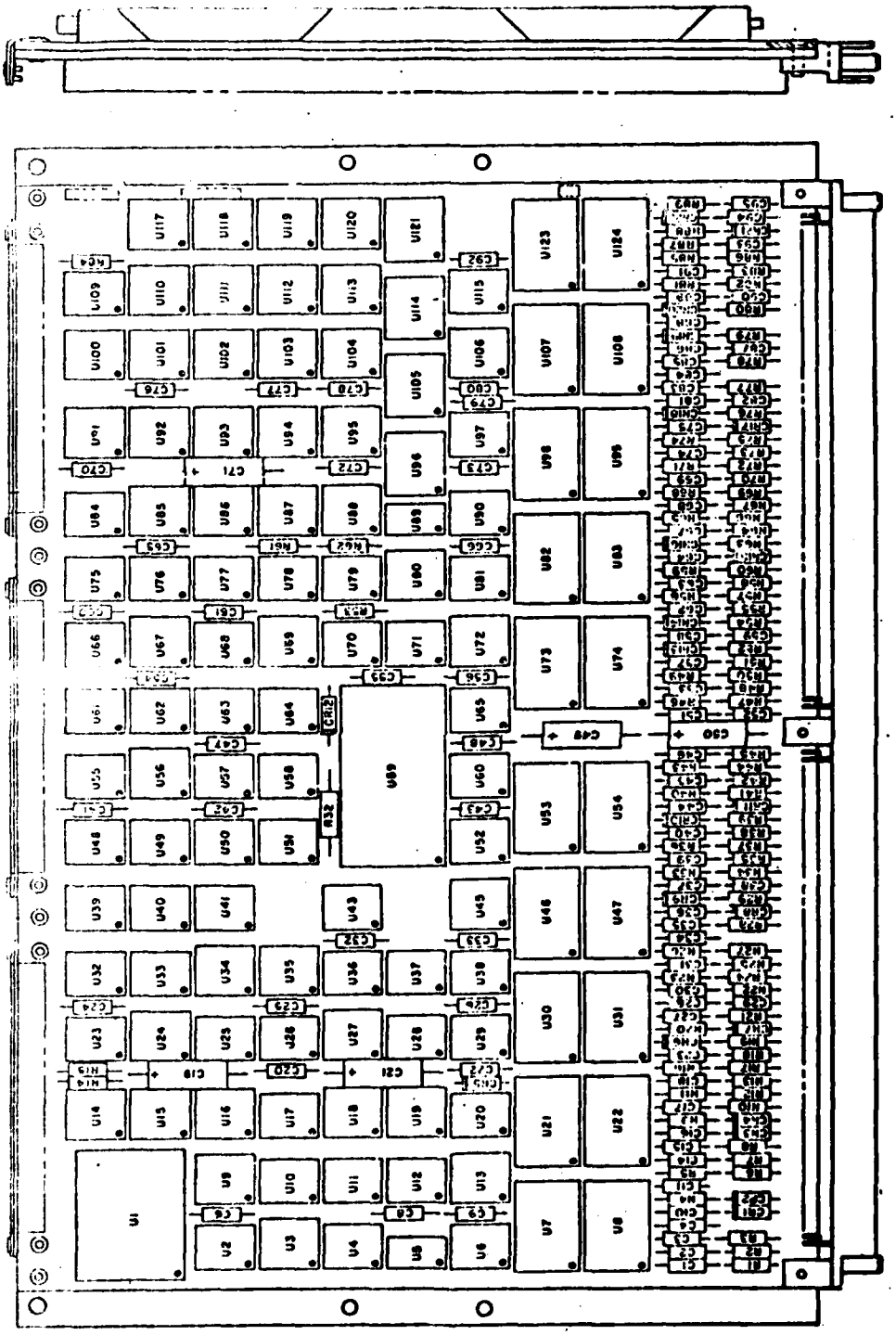


Figure 47 - NTDS (Slow) Interface Module, Circuit Card Assembly

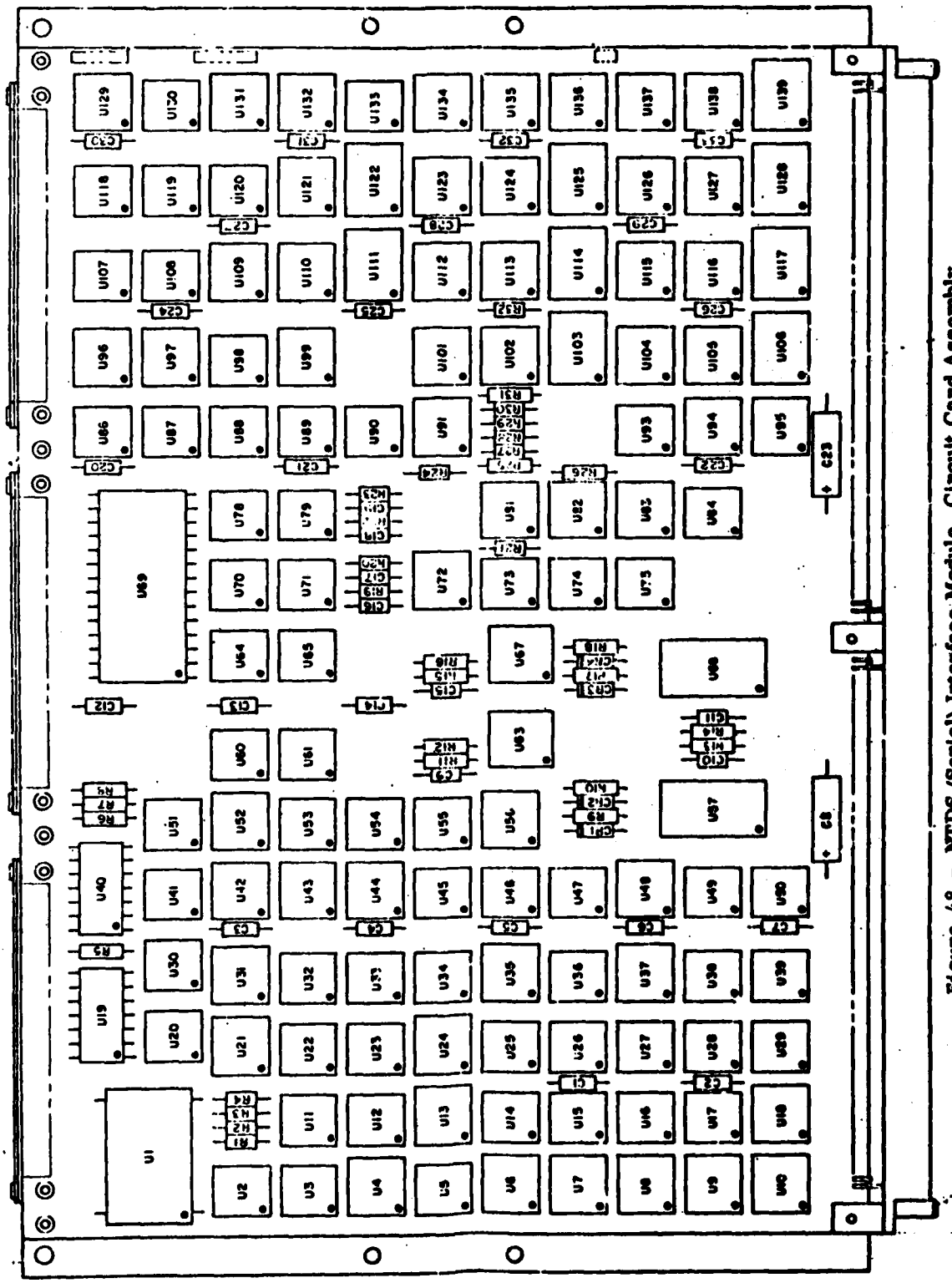


Figure 48 - NTDS (Serial) Interface Module, Circuit Card Assembly

requires two resistors external to the integrated circuit. A receiver and a transmitter are connected in parallel at the transmission line terminator. Thus, when data is being received, the transmitter impedance must be high compared to the 75-ohm coaxial cable impedance. A current switch type of transmitter is used in this circuit. Each I/O channel has two receivers and two transmitters. A number of these may connect to the logic, which generates and decodes the phase-modulated pulse stream.

(6) The AN/AYK-14(V) I/O subsystem will interface with all four types of NTDS data channels: Fast, Slow, Anew, and Serial. Each 6-by-9 module will contain one I/O channel. The four types are interchangeable at an SRA level in the WRA.

(7) Further commonality is obtained between the NTDS Fast and Slow interfaces by utilizing the same components and printed-circuit boards on these modules. The unique characteristics of the interfaces are obtained by changing the time constants and the voltages to the transmitter/receiver, simplifying training and testing requirements for these cards.

(8) The test parameters for NIM (Fast, Anew, Slow, and Serial) are shown in Tables 10, 11, 12, and 13.

TABLE 10 - NTDS (FAST) INTERFACE MODULE TEST PARAMETERS

SRA configuration:	Single digital circuit board SRA		
IC count:	120 ICs		
Connector pin count:	3 top 41-pin connectors		-123 pins
	1 bottom 152-pin connector		-152 pins
		TOTAL	275 pins
Signal I/O pins			132 pins
Test point pins			43 pins
		TOTAL I/O	175 pins
Power/ground pins			22 pins
		TOTAL REQUIRED	197 pins
Data rate:	250 words/second		
Power required:	+5 vdc, -5 vdc, -12 vdc; 3.56 amp, 3.56 amp, 1.48 amp; 17.8 watts		
Bidirectional lines:	16 lines or 32 lines X bus		
Differential lines:	Input, 20 lines (40 pins)		
	Output, 20 lines (40 pins)		
Oscillator:	32 MHz, 16 MHz, 2.28 MHz		

TABLE 11

NDTS (ANEW) INTERFACE MODULE TEST PARAMETERS

SRA configuration: Single digital circuit board SRA		
IC count: 109 IC's		
Connector pin count: 3 top 41-pin connectors		- 123 pins
One bottom 152-pin connector		- 152 pins
	Total	- 275 pins
Signal I/O pins		- 132 pins
Test point pins		- 42 pins
	Total I/O	174 pins
Power/ground pins		20 pins
	Total required	194 pins
Data rate: 250K words/second		
Power required: +5 vdc, -12 vdc; 1.8 amp, 0.1 amp; 10.2 watts		
Bidirectional lines: 16 lines or 32 lines X bus		
Differential lines: Input, 20 lines (40 pins)		
Output, 20 lines (40 pins)		
Oscillators: 32 MHz, 16 MHz		

TABLE 12

NTDS (SLOW) INTERFACE MODULE TEST PARAMETERS

SRA configuration:	Single digital circuit board SRA	
IC count:	120 IC's	
Connector pin count:	3 top 41-pin connectors	- 123 pins
	One bottom 152-pin connector	- 152 pins
	Total	- 275 pins
	Signal I/O pins	132 pins
	Test point pins	43 pins
	Total I/O	175 pins
	Power/ground pins	22 pins
	Total required	197 pins
Data rate:	40 K words/second	
Power required:	+5 vdc, -5 vdc, -12 vdc; 3.46 amp, (not used), 1.45 amp; 17.3 watts	
Bidirectional lines:	16 lines or 32 lines X bus	
Differential lines:	Inputs, 20 lines (40 pins)	
	Output, 20 lines (40 pins)	
Oscillators:	32 MHz, 16 MHz, 2 MHz, 222 kHz	

TABLE 13

NTDS (SERIAL) INTERFACE MODULE TEST PARAMETERS

SRA configuration: Single digital circuit board SRA		
IC count: 129 IC's		
Connector pin count: 3 top 41-pin connectors		- 123 pins
One bottom 152-pin connector		- 152 pins
Total		- 275 pins
Signal I/O pins		- 56 pins
Test point pins		- 43 pins
Total I/O		99 pins
Power/ground pins		17 pins
Total required		116 pins
Data rate: 10 M bits/second		
Power required: +5 vdc, -5 vdc; 1.7 amp, 0.2 amp; 9.5 watts		
Bidirectional lines: 16 lines X bus (est.)		
Differential lines: Inputs, 20 lines (40 pins) (est.)		
Output, 20 lines (40 pins) (est.)		
Oscillators: 32 MHz, 16 MHz, (est.)		

d. RS-232-C Interface Module (RIM). The RIM (Figure 49) provides a full-duplex RS-232-C serial channel operable at selectable baud rates from 150 to 9,600 baud for the asynchronous mode and in synchronous mode to 9,600 baud. The module can be converted to operate to MIL-STD-188C with some component changes, but without circuit board modifications.

(1) An EIA-STD-RS-232-C serial channel communicates over a serial interface which transfers data and control information in both directions, using the input and output cable configuration in Figure 50. Full-duplex operation at rates to 9,600 baud is possible. The control lines are turned "on" and "off" by I/O command and chaining instructions to communicate with peripheral equipment. The peripheral equipment can, in turn, set control lines to transfer interrupt, response to controls, and status information to the computer. While the RS-232-C channel module is capable of either synchronous or asynchronous operation, the chassis configuration (connector wiring) permits only a single type of operation on a given channel.

(2) A single RS-232-C compatible channel is contained on the RS-232-C channel SRA. This module is compatible with the other proposed AN/AYK-14(V) I/O channel types in terms of the I/O bus interface, interrupt interface, and control firmware interface. This module type may, as a result, be located in any I/O channel SRA slot. Like all other AN/AYK-14(V) computer modules, this module will be designed to meet the MIL-E-5400, Class II environment as required.

(3) The RS-232-C channel is implemented using a universal asynchronous receiver/transmitter (UART) integrated circuit as shown in the block diagram, Figure 51. This results in a cost-effective, low-power approach and provides selectable baud rates up to 9.6K baud for the asynchronous mode. The transmitter/receiver circuits provide for a voltage mode signal interface per RS-232-C. Provisions are also made for a current-loop mode of transmission.

(4) The timing/mode control logic generates the required baud rate clocks for the UART, with the baud rate selectable by software. This logic also generates the appropriate channel interrupts.

(5) The X channel logic provides the interface with the standard AN/AYK-14(V) I/O bus.

(6) The test parameters for the RIM are shown in Table 14.

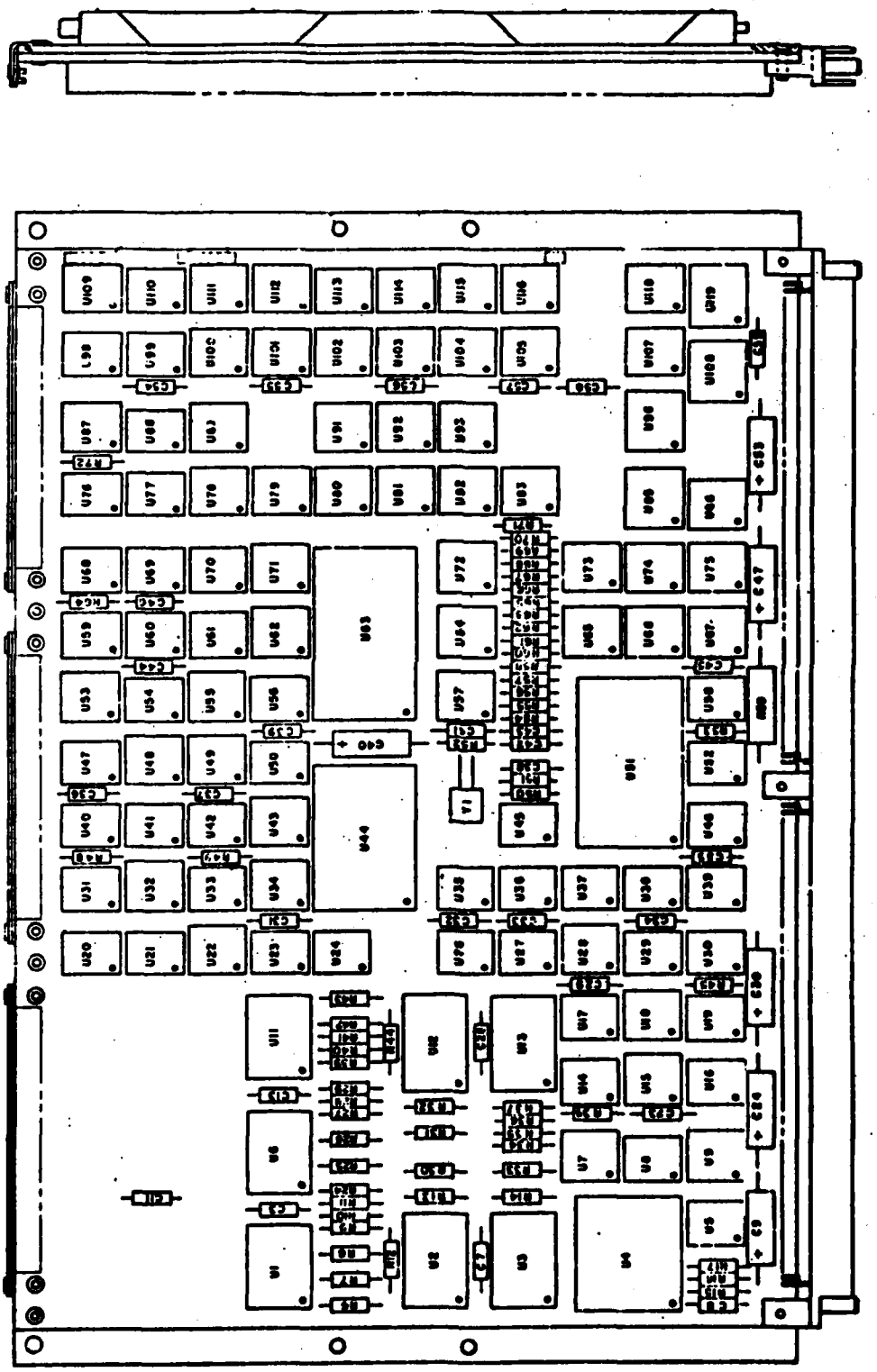


Figure 49 - RS-232-C Interface Module, Circuit Card Assembly

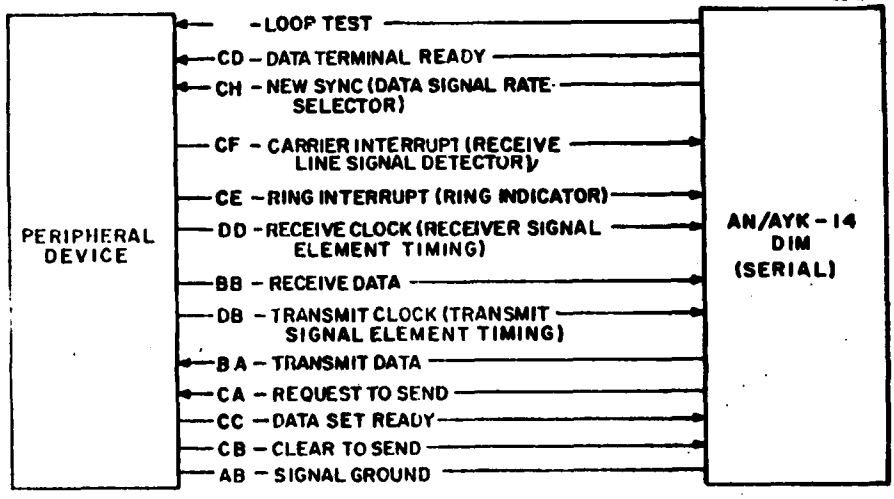


Figure 50 - RS-232-C Interface Module, Series Channel Interface

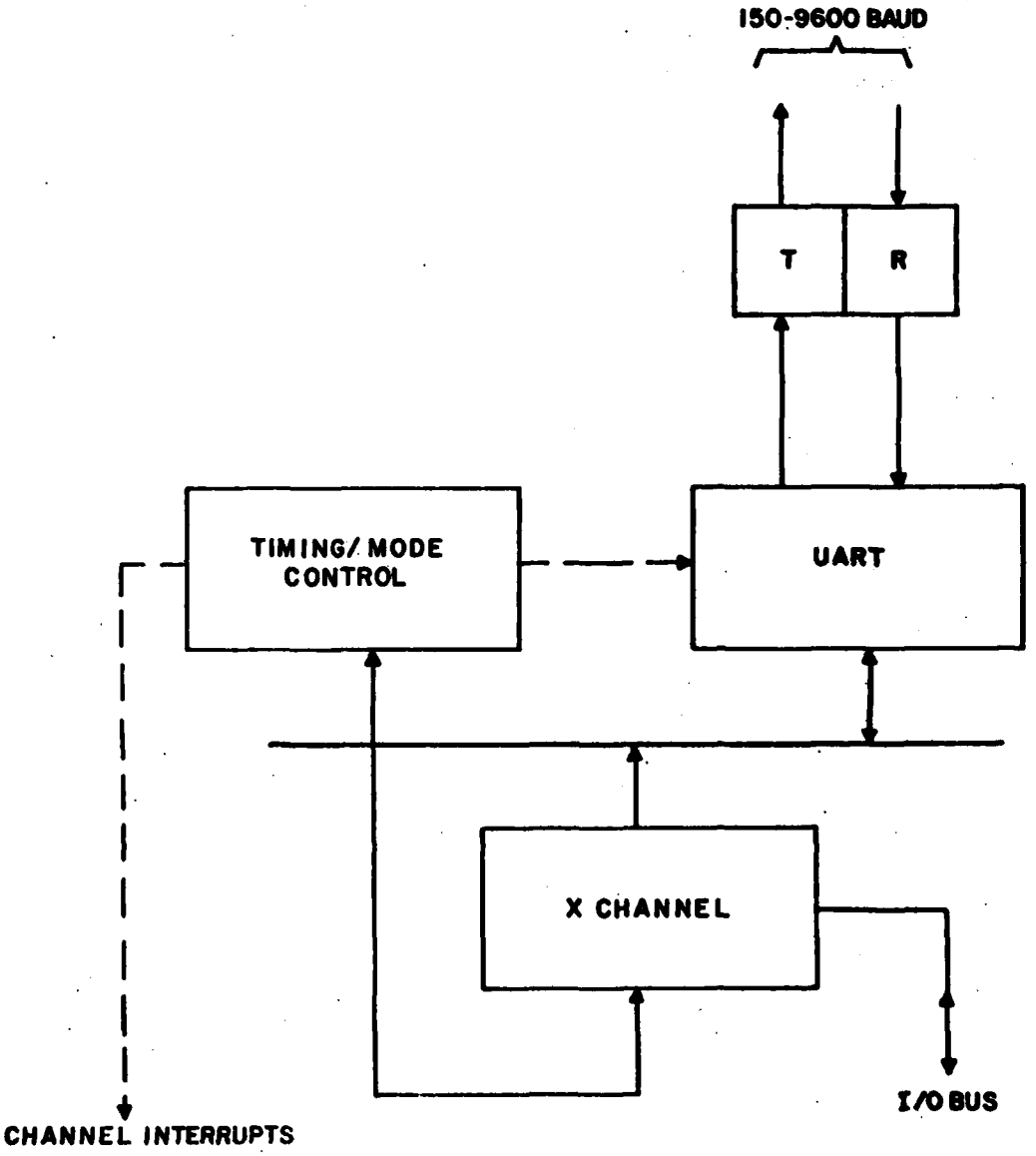


Figure 51 - RS-232-C Interface Module, Channel Block Diagram

TABLE 14

RS-232-C INTERFACE MODULE TEST PARAMETERS

SRA configuration: Single digital circuit board SRA		
IC count: 110 IC's		
Connector pin count:	3 top 41-pin connectors	- 123 pins
	one bottom 152-pin connector	- 152 pins
	TOTAL	- 275 pins
	Signal I/O pins	89 pins
	Test point pins	49 pins
	TOTAL I/O	138 pins
	Power/ground pins	55 pins
	Total required	193 pins
Data rate: 150 to 9,600 baud		
*Power required: 15 watts		
Bidirectional lines: 16 lines X bus		
*Voltage and current not available.		

e. PROTEUS Interface Module (PIM). The PIM (Figure 52) contains the logic to implement a PROTEUS digital channel pair capable of full-duplex data transmission at a nominal 10-MHz bit rate. The channel is designed to NAVAIR-DEVCEN specification No. A30-15590.

(1) Transmission on the PROTEUS channel (Figure 53) is between a source and a sync with initiation and control by the source. The channel pair uses a total of eight differential NRZ signals. A source transmits 6-bit control words and 34-bit data words (32 message bits, one parity bit, and one word-type bit). The sync responds to each source word with an appropriate 6-bit control word to accomplish a positive handshaking procedure on a word-by-word basis. Parity is provided on both control and data words for error detection, and retransmission is used for error correction.

(2) As shown in Figure 54 one sync channel and one source channel are included. The sync channel receives 34-bit data words and receives and transmits 6-bit control words. Each data and control word contains an identifier bit and parity bit plus 32 or 4 information bits respectively. The control frame interchanges on the sync channel are controlled by the sync control logic. The IN SR register is 32 bits in length and provides serial assembly and input to the memory via the I/O bus interface in two 16-bit words. The source channel transmits 34-bit data words and transmits and receives 6-bit control words. The OUT SR register is 32 bits in length and provides assembly of two 16-bit data words from the I/O bus interface logic into a 32-bit serial word for transmission. The source channel control frame exchanges are controlled by the source control logic of the source channel.

(3) All communications between the PDM and subsystems in the AN/AYK-14(V) computer are compatible with the "channel-type-independence" design of the various I/O channel modules, so that this channel type is completely interchangeable with others in the I/O subsystem.

(4) The PIM test parameters are shown in Table 15.

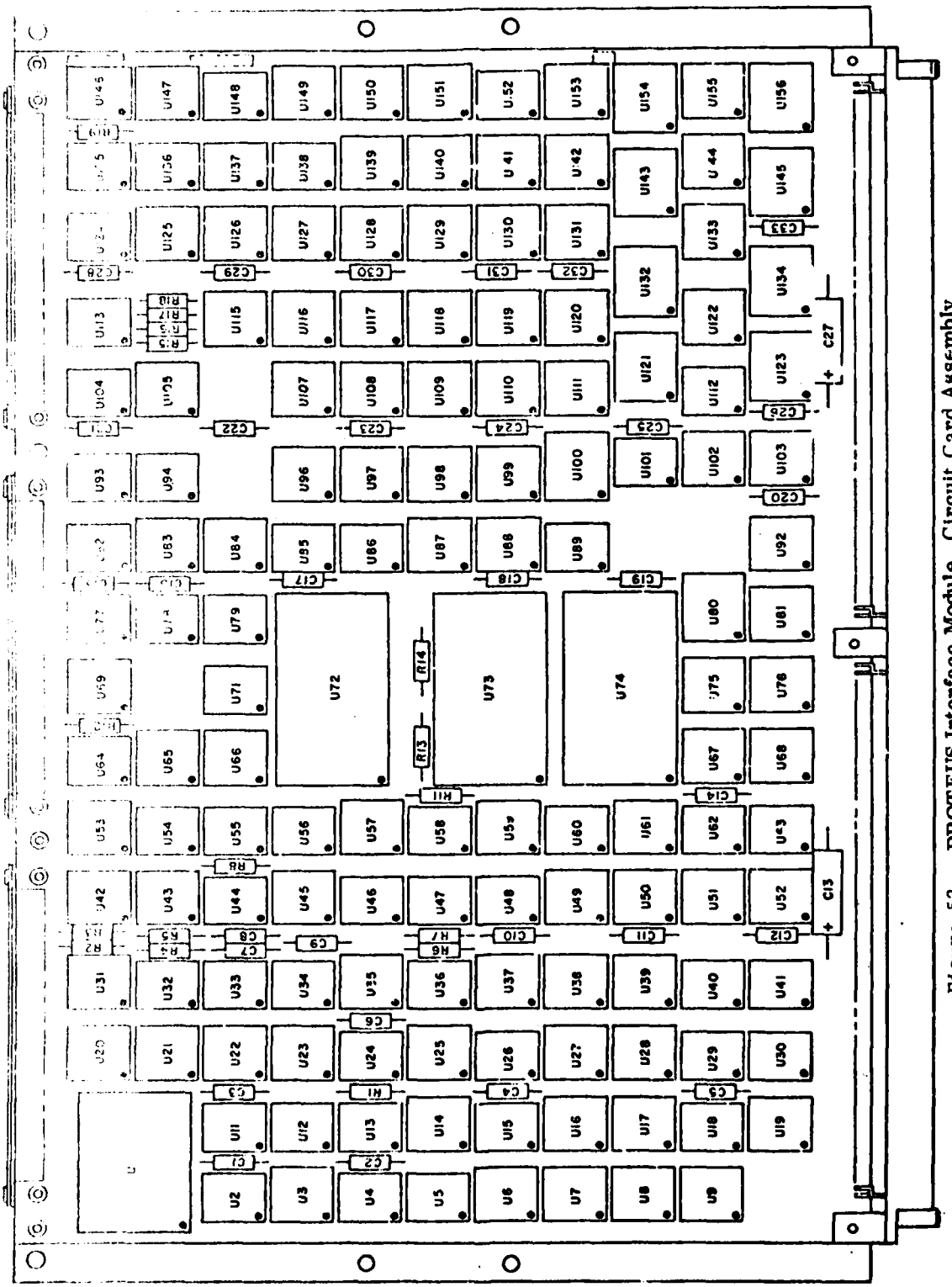


Figure 52 - PROTEUS Interface Module, Circuit Card Assembly

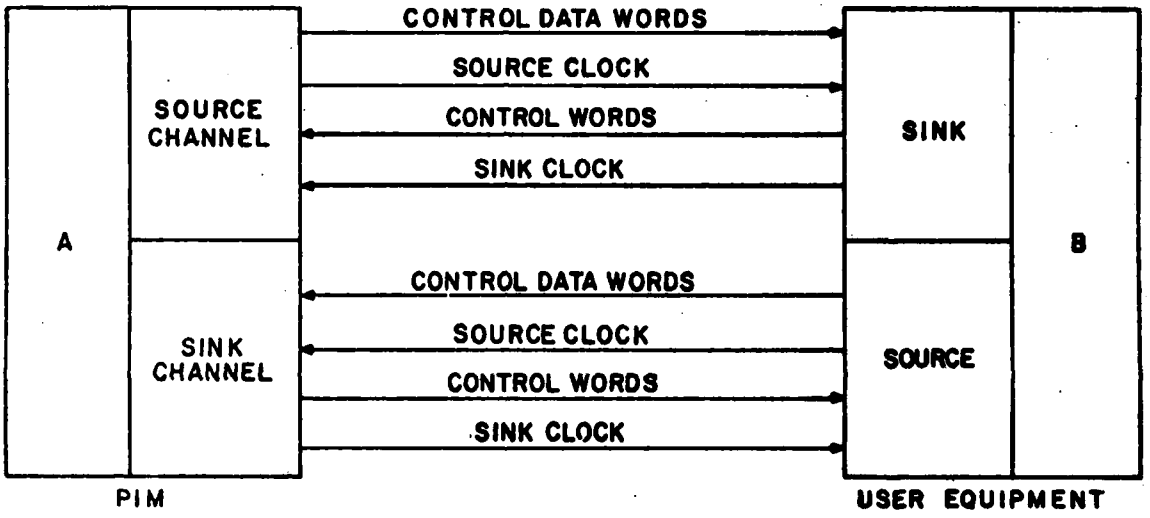


Figure 53 - PROTEUS Interface Module, Channel Pair

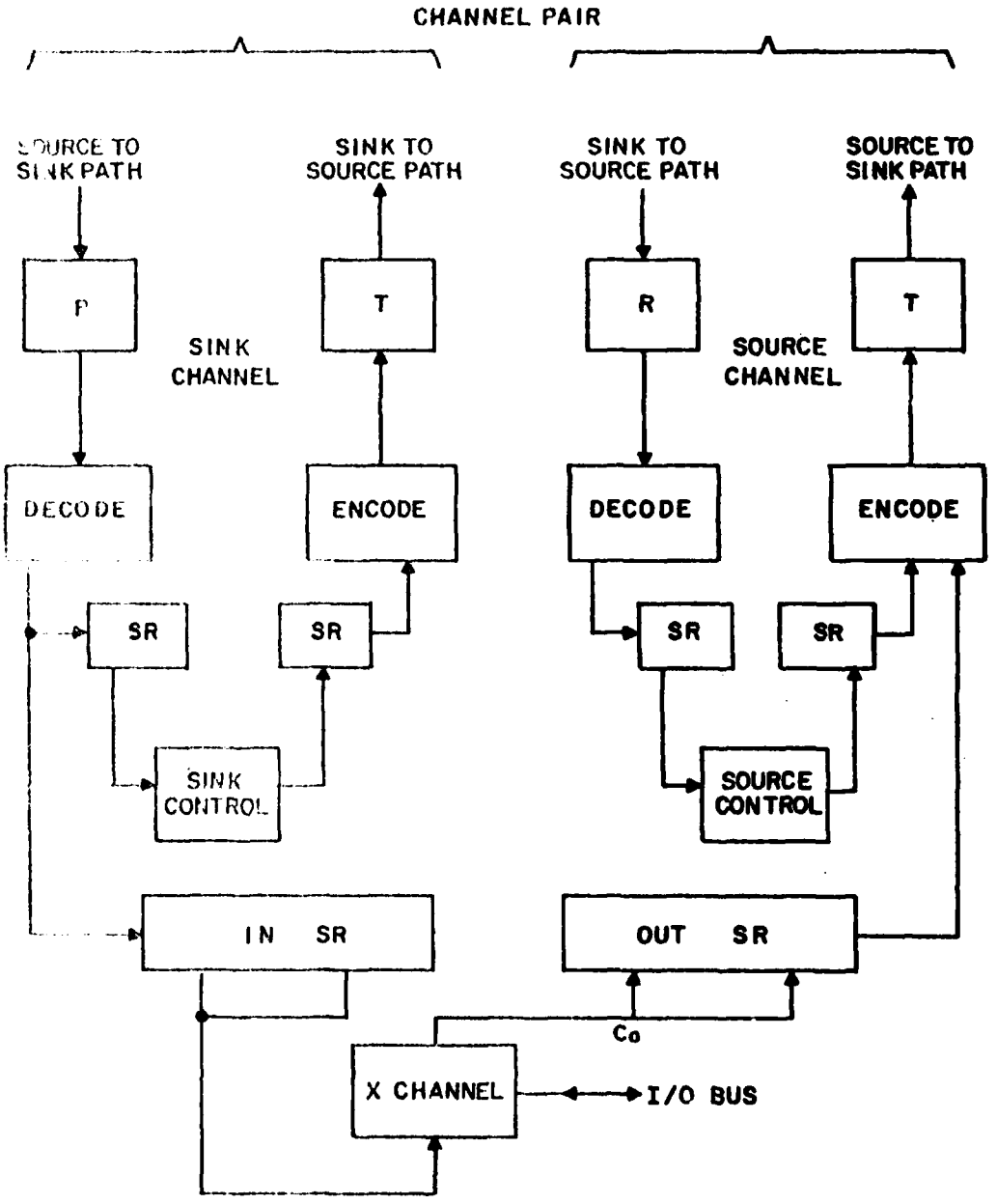


Figure 54 - PROTEUS Interface Module, Channel Block Diagram

TABLE 15

PROTEUS INTERFACE MODULE TEST PARAMETERS

SRA configuration: Single digital circuit card SRA		
IC count: 149 IC's		
Connector pin count: 3 top 41-pin connectors		- 123 pins
One bottom 152-pin connector		- 152 pins
Total		- 275 pins
Signal I/O pins		64 pins
Test point pins		83 pins
TOTAL I/O		147 pins
Power/ground pins		18 pins
Total required		165 pins
Data rate: 10 MHz bit rate		
Power required: +5 vdc, 2.6 amp, 13 watts		
Bidirectional lines: 16 bits X bus		
Differential lines: 8 total (4 input and 4 output), 16 pins		
Oscillator: 20 MHz, 10 MHz		

1. INPUT/OUTPUT PROCESSOR MODULE (IOP). The IOP is a complete 16-bit processor combining the basic functions of the GPM and the PSM on a double circuit card module. The instruction set is a subset of the AP/AYP-14(V) instruction set. To accomplish a one-module processor, [illegible] performance and features are reduced from the GPM/PSM capability. The IOP is intended for use in three general applications:

- As a small-scale, stand-alone, general-purpose processor with emulation capabilities.
- As an I/O controller (IOC) in conjunction with a GPM as instruction processor.
- As a combination IOC and instruction processor in conjunction with a GPM.

Features of the IOP include:

- 48-bit microcommand control
- Up to 2K micromemory on the module
- 250-nanosecond microcommand cycle
- 7 [illegible] 16-bit word register file
- Single parallel bus interface (*IOBUS*)
- Event interface
- Serial interface to support equipment
- Real-time clock with 1-microsecond resolution
- BIT-timer, 2.097-second increment, 3-bit count
- Event monitor logic
- Microcommand format identical to GPM

The IOP is a double circuit card module. Circuit card A is shown in Figure 55 and circuit card B is shown in Figure 56. The test parameters of the IOP [illegible] are shown in Table 16.

TABLE 16

INPUT/OUTPUT PROCESSOR TEST PARAMETERS

SRA configuration:	Double digital circuit card SRA		
IC count:	Circuit card A, 107 IC's; circuit card B, 100 IC's; total, 207 IC's		
Connector pin count:	3 top 41-pin connectors		- 123 pins
	2 bottom 152-pin connectors		- 304 pins
		Total	- 427 pins
	Signal I/O pins		229 pins
	Test point pins		116 pins
		TOTAL I/O	345 pins
	Power/ground pins		36 pins
		Total required	381 pins
Power required:	Card A, +5 vdc		
	Card B, +5 vdc, +15 vdc		
	8.8 amp, 44 watts		
Bidirectional lines:	Card A, X bus 24 lines, 2 sets (48 pins)		
	Card B, None		
Differential lines:	Card A, 4 lines (8 pins)		
	Card B, 6 lines (12 pins)		
Oscillator:	32 MHz, Card B		

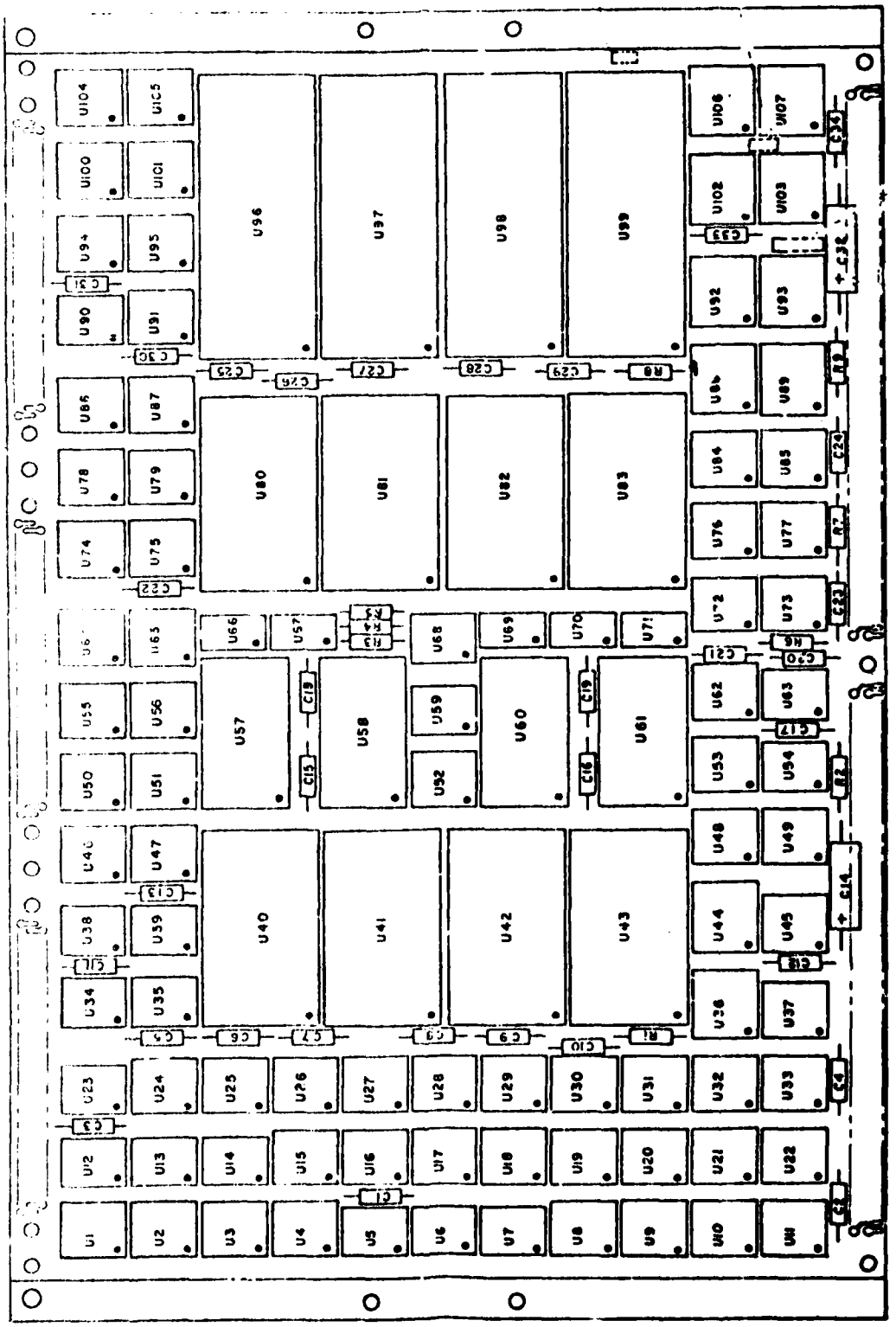


Figure 55 - Input/Output Processor, Circuit Card A

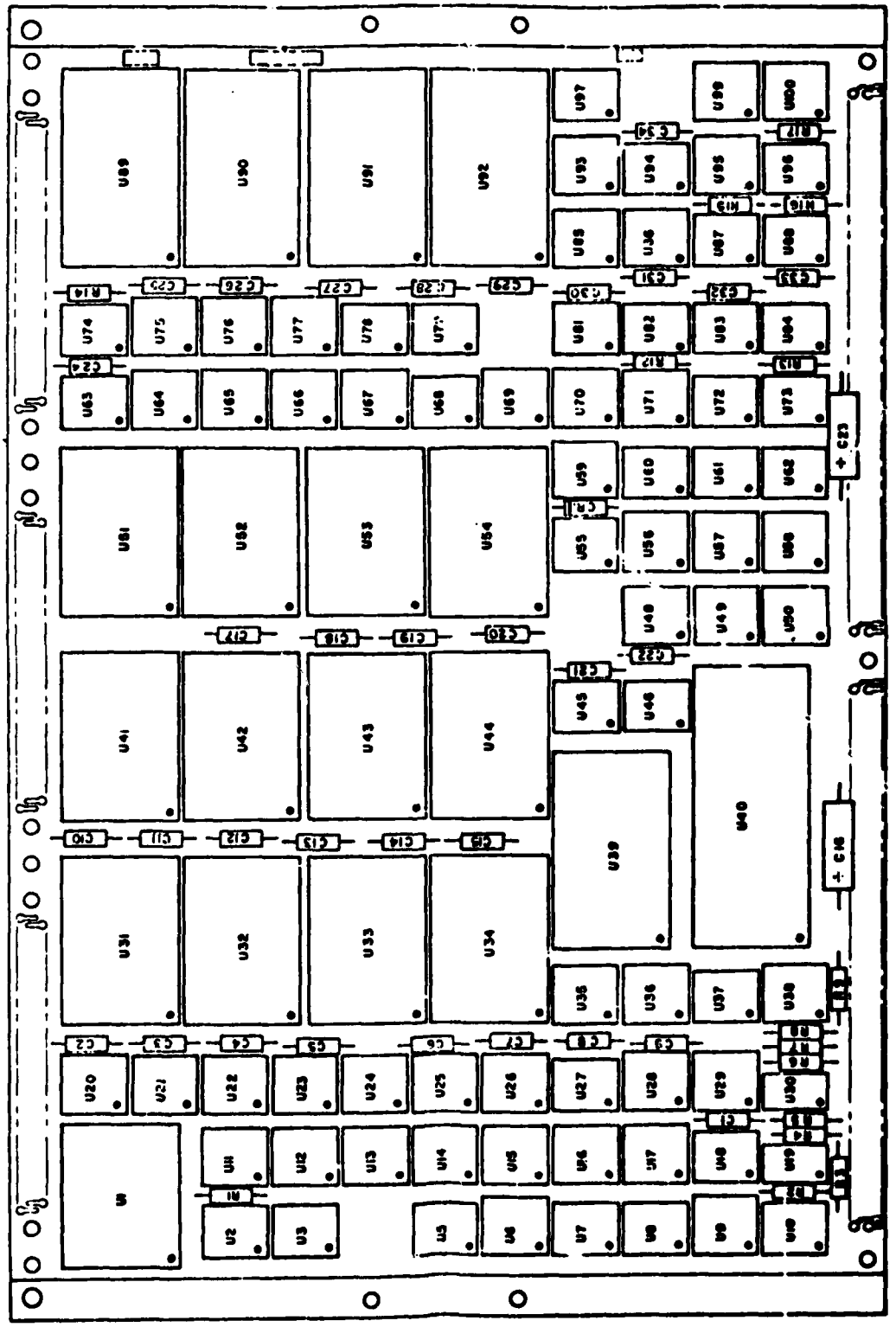


Figure 56 - Input/Output Processor, Circuit Card B

BUS EXTENDER MODULE (BEM). The BEM (Figure 57) provides an extension of the internal AN/AYK-14(V) buses and interfaces outside the enclosure to permit expansion of memory, processor, and/or I/O subsystems to additional enclosures up to 15 feet (total cable length) from the computer. All voltage levels are TTL compatible and employ differential line drivers/receivers for all interfaces. The electrical and logical design permits BEM-to-BEM communication. The BEM does not have a channel address as do other I/O modules, but operates transparent to bus operation. The BEM can be used to interface a direct memory access (DMA) channel.

(1) The BEM interfaces internal to the AN/AYK-14(V) computer are with the CPUBUS, IOBUS, and MEMBUS, as shown in Figure 58. The MEMBUS is actually a local control and data path interface that enables overlapped operation in two memory modules. The MEMBUS may, therefore, be envisioned as two separate buses: MEMBUS 1 for even address words and MEMBUS 2 for odd address words. All four buses are routed through TTL-compatible differential transmitter and receiver circuits to provide external extension to the computer unit. The required circuitry on the BEM is not very extensive, but the pin requirements dictate a double board SRA and total 228-pin connectors. Any communication performed on these buses which addresses hardware external to the unit and in other units experiences a slight speed degradation - approximately 75 nanoseconds in one direction with 10 feet of interconnect cable length. The BEM design ensures that data signal skewing and delays are greater than control signal delays so that worst case setup and hold times for information on the buses is not affected by using the BEM. Each input presents 110 ohms impedances.

(2) The BEM utilizes 143 integrated circuit packages and dissipates 20 watts total. Each bus interface section, however, is powered from separate power planes so that configurations that only require certain bus extensions may be tailored in the interconnector panel wiring to power only those sections.

(3) The BEM test parameters are shown in Table 17.

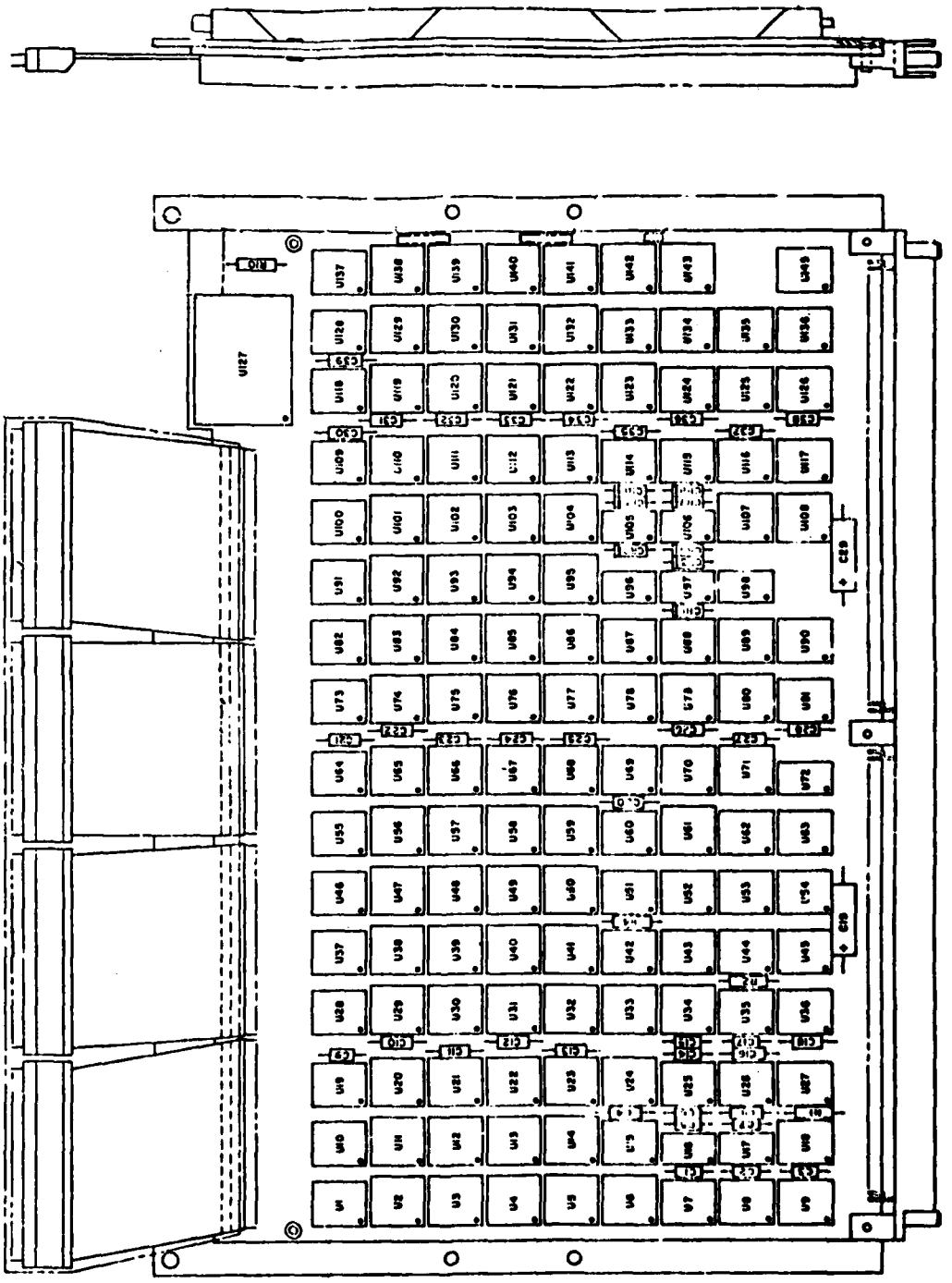


Figure 57 - Bus Extender Module Circuit Card Assembly

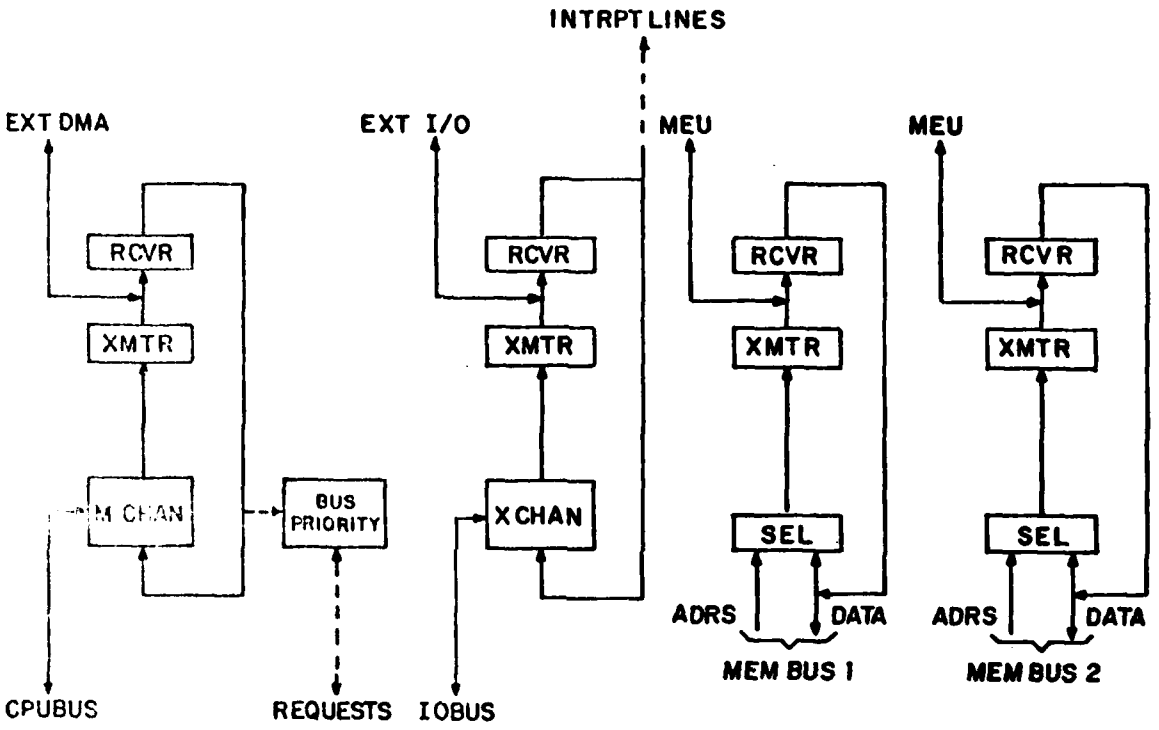


Figure 58 - Bus Extender Module Block Diagram

TABLE 17

BUS EXTENDER MODULE TEST PARAMETERS

SRA configuration:	Single digital circuit card SRA	
IC count:	143 IC's	
Connector pin count:	Four 64-pin connectors	- 256 pins
	One 152-pin connector	- 152 pins
	Total	- 408 pins
	Signal I/O pins	136 pins
	Test point pins	228 pins
	Power/ground pins	21 pins
	Total required	385 pins
Power required:	+5 vdc, 5.8 amp, 29 watts	
Bidirectional lines:	EMEMBUS, OMEMBUS, X bus, M bus; 16 bits, 16 bits, 24 bits, 24 bits = 80 bits	
Differential lines:	208 lines	
Oscillator:	33.3 MHz	

b. READ/WRITE EXPANDABLE MODULE (RXM). The RXM contains 4K words by 18 bits of read/write static semiconductor memory and an optional additional 4K words of read-only memory (ROM or PROM). Features include:

- 400-nanosecond cycle time
- 300-nanosecond access time
- Interface to IOBUS or CPUBUS
- Parity logic, one bit per byte

(1) This memory is unpaged and does not interface with the MCM. It is intended to operate directly with a processor via either the IOBUS or CPUBUS interface. Multiple RXM's can be used in a system up to a total of 65,536 words; however, the present AN/AYK-14(V) chassis (XN-1) and (MEU) provides space for only one RXM each. The primary application of RXM's is to provide memory functions for small AN/AYK-14(V) configurations using the IOP as a stand-alone processor. An RXM can also be used as a private program memory for the IOP when used in configurations employing both the IOP and CPU in combinations. In the latter case, the CPU will not have access to the RXM. When installed in the XN-1 or MEU chassis, the RXM is assigned address ranges F000 to FFFF (HEX) for the RAM portion and E000 to EFFF (HEX) for the optional PROM portion.

(2) The RXM is an optional module in any I/O subsystem containing an IOC. The RXM block diagram is shown in Figure 59. This single SRA contains both a CPUBUS interface and a IOBUS interface, 4K words by 18 bits of storage, parity and check bit logic, and timing and control circuitry necessary to sequence read/write operations and interface with the IOC via the CPUBUS and IOBUS. The address range which this module recognizes is defined by back panel wiring in the chassis of any configuration. This allows all RXM's in any configuration to be identical and completely interchangeable regardless of the logical addresses associated with physical card placements in the unit.

(3) The RXM read access time is typically 300 nanoseconds, and total cycle time is 400 nanoseconds. The storage media is provided by 18 4K-word by 1-bit RAM packages. Printed circuit board wiring and component mounting area actually exists on the RXM to populate the module with 36 total RAM packages for 8K words by 18 bits of storage. This option need not be used but is available for increased packaging density in systems that require a large amount of IOC program memory.

(4) The total power required by the RXM is 9 watts, with 4K words for 18 bits of storage mounted. There are a total of 51 IC packages on the module, with 18 for storage and the remainder for CPUBUS and IOBUS interface transceivers, timing chain and control circuits, and parity and check bit logic. All handshaking control with the IOC via the CPUBUS and IOBUS, as well as internal sequencing during a transfer cycle, is independent of any other SRAs. The RXM is packaged on a standard 6-by-9-inch module.

(5) The RXM test parameters are shown in Table 18.

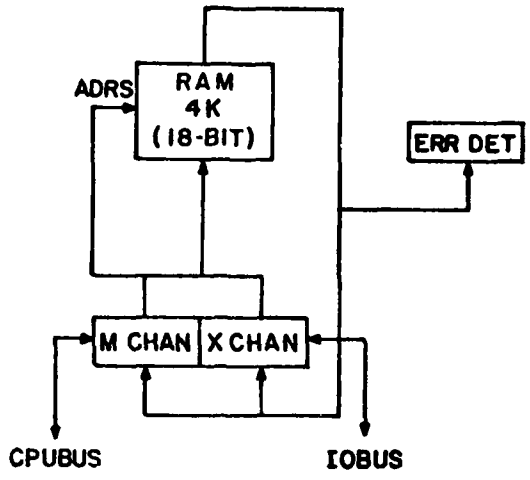


Figure 59 - Read/Write Expandable Module, Block Diagram

TABLE 18

READ/WRITE EXPANDABLE MODULE TEST PARAMETERS

SRA configuration: Single digital circuit card SRA		
IC count: 85 IC's		
Connector pin count:	3 top 41-pin connectors	- 123 pins
	One bottom 152-pin connector	- 152 pins
	Total	- 275 pins
Signal I/O pins		71 pins
Test Point Pins		27 pins
Power/ground pins		20 pins
	Total required	118 pins
Power required: 9 watts		

5. POWER SUBSYSTEM SRA's (PCM-1 AND PCM-2). Within the power subsystem [illegible] are two alternative power converter modules (PCM-1 and PCM-2). The PCM (Figure 60) provides regulated dc power required to operate AN/AYK-14(V) modules from military aircraft power source. Two sizes of PCM's are currently available to power various computer configurations. The PCM's are themselves modular designed, and new capacities can be developed to meet other power [illegible] or computer configuration requirements. The PCM's operate from 115-vac, [illegible]-phase, 400-Hz, wye-connected input power. The design is compatible with MIL-STD-704B and MIL-STD-461A, Notice 3.

a. PCM-1 has a full load capability of 390 watts and the PCM-2 has a full load capability of 390 watts plus 152 watts, or a total of 540 watts, as indicated in Table 19.

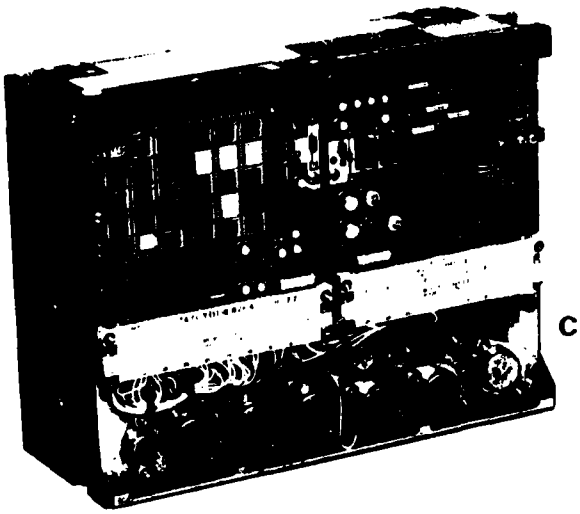
TABLE 19

POWER CONVERTER MODULE CHARACTERISTICS

MODULE	INPUT	CURRENT +15V	CURRENT +5V	CURRENT -12V	CURRENT -5V	OUTPUT AVAILABLE POWER	EFFICIENCY (PERCENT)	POWER FACTOR
[illegible]	3-Phase, 400 Hz, 115 vac	46A	3.5A	8.5A	1.0A	390W	68	0.87
[illegible]	3-Phase, 400 Hz, 115 vac	25A	1.0A	1.0A		152W (Added to PCM-1)	68	0.87

b. A block diagram of the PCM is shown in Figure 61. The PCM is current limiting with automatic recovery after removal of the load fault is provided on the +15-volt, -12-volt, and -5-volt outputs. Overcurrent on the [illegible] volt output will result in loss of all output voltages until the load fault is cleared and input power is recycled. This provides short-circuit protection on all outputs. The overvoltage circuit on each output is activated whether the overvoltage is due to a fault internal or external to the PCM.

c. The PCM will initiate a normal power-off sequence if the ac input [illegible] falls below approximately 80 volts for longer than 100 microseconds or if any input phase is interrupted. Regulated outputs are provided for a minimum of 400 microseconds after removal of input power to enable the computer state to be stored. The +15 volts is then crowbarred to prevent altering memory contents during power-off. The PCM initiates a power-on sequence when input voltage returns to normal limits.



PCM-1

COMMON FEATURES

- MIL-STD-704
- 115V; 3PH ; 400Hz ; Y-CONNECTED
- EFFICIENCY : 72 %
- PROTECTION/MONITOR :
  - OVERTEMP
  - OVERCURRENT
  - OVERVOLTAGE
  - ON/OFF SEQUENCING
  - INTERRUPTS TO PROCESSOR
- PLUGGABLE
- DUAL-SOURCED

UNIQUE FEATURES	PCM-1	PCM-2
● SIZE:	7.1"H x 9.0"W x 3.5"D	7.1"H x 9.0"W x 4.9"D
● WEIGHT:	9.1 POUNDS	11.5 POUNDS
● DELIVERABLE POWER:	390 WATTS	540 WATTS

Figure 60 - Power Converter Module

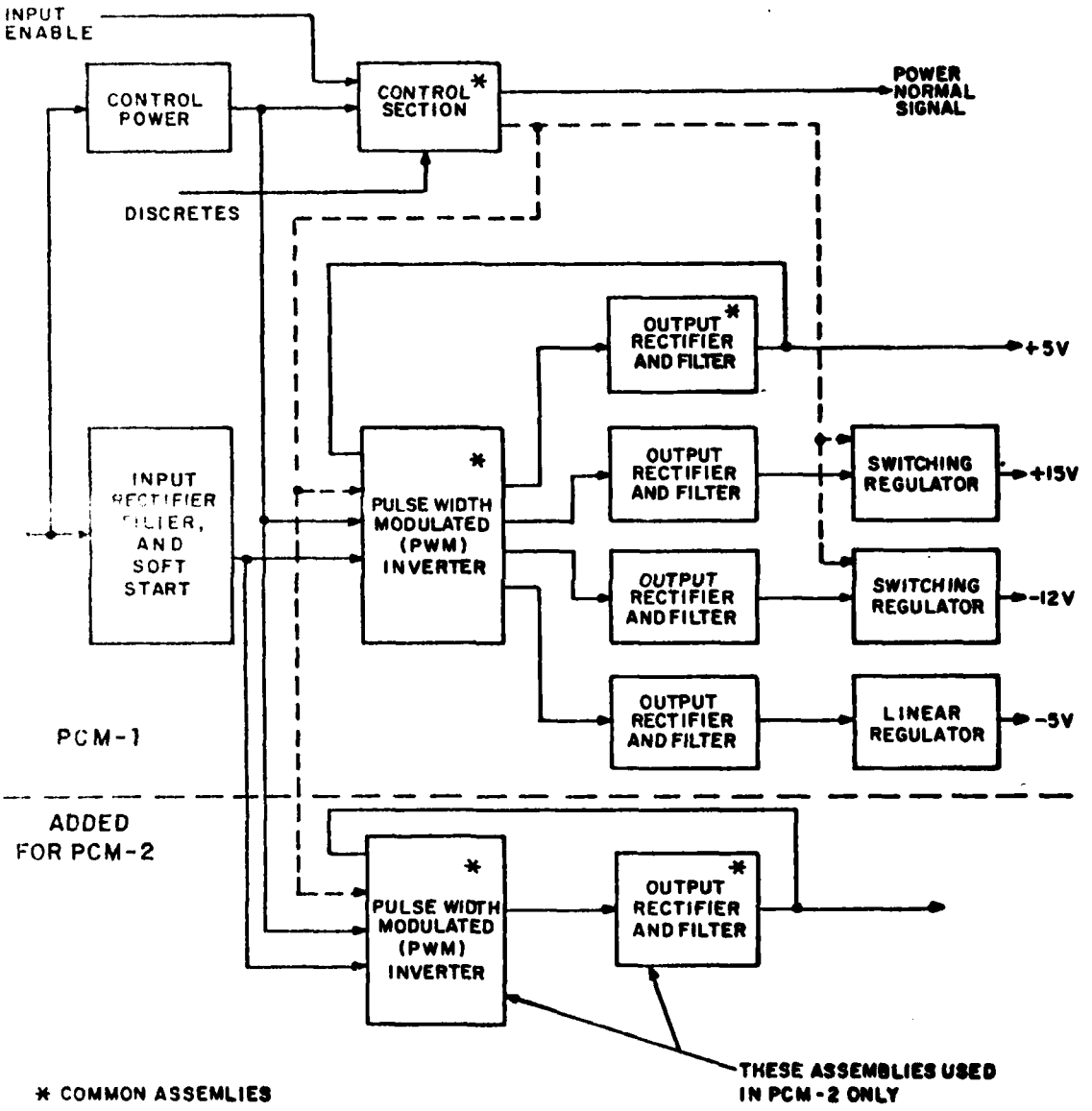


Figure 61 - Power Converter Module Block Diagram

d. Two thermostatic switches are included in each PCM, and a computer interrupt is generated when an abnormally high internal temperature is reached. A power-off sequence may be initiated by the CPU as a result of the interrupt. At a slightly higher temperature (but sufficiently low to prevent component damage), a normal power-off sequence is automatically initiated. A power-on sequence is automatically initiated when the PCM cools to normal operating temperature. In any event, sufficient time is allowed (after the power abnormal signal) to save the state of the computer in core memory before output voltages are reduced to zero. A thermal overload discrete will be available on an operational connector as well as on the maintenance connector.

e. A three-phase bridge rectifier and an inductive input filter provide unregulated dc voltage to the pulse width modulated inverter. The energy storage required to operate for 400 microseconds after interruption of input power is provided by multiple energy storage capacitors in a pluggable assembly. A softstart circuit limits the surge current during initial application of input power and provides a low impedance for normal operation.

f. A bridge inverter using four high-voltage, high-speed transistor switches converts the dc input to a constant, high-frequency ac output, which is capacitively coupled to the transformer primary (Figure 62). The high transistor voltage rating enables the inverter to meet the 180-volt rms surge requirements of MIL-STD-704. The transformer output is rectified and filtered to provide an efficiently regulated +5-volt output. The prototype inverter's efficiency (excluding drive losses and output rectifier/filter losses) was approximately 90 percent. Solid tantalum output capacitors per MIL-C-39003 (CSR13) in a pluggable assembly provide low ac output impedance over the operating temperature range. Comparison of the +5-volt output to a stable reference voltage results in a feedback signal which varies the inverter pulse width to obtain a constant average rectified output regardless of input voltage or load current variations. The pluggable printed wiring assembly used in the pulse-width modulated inverter is interchangeable between PCM-1 and PCM-2.

g. Additional rectifiers and LC filters provide a dc input voltage to the switching (or linear) regulators, which regulate against line voltage variations (Figure 63). A pluggable printed wiring assembly containing two regulator circuits controls the power elements of the +15-volt and -12-volt switching regulators in PCM-1. The operating frequency is chosen to minimize inductor size and weight without resulting in excessive switching losses. Three terminal linear regulators are used to supply the low current requirements of the -5 volts of PCM-1 and the +15 volts and -12 volts of PCM-2.

h. A line frequency transformer and linear regulators are used to provide power to the control section and the printed wiring assembly used in the pulse-width modulated inverter. The control section consists of a pluggable printedwiring assembly containing primarily digital integrated circuits. It monitors the input voltage conditions, the two thermostatic switches, and the input enable signal and initiates power-on and power-off sequences under appropriate conditions. It issues the interrupt at the lower of the two thermostatic switch temperatures and also interconnects the control sections of the PCM's if two or more PCM's are used to power a system.

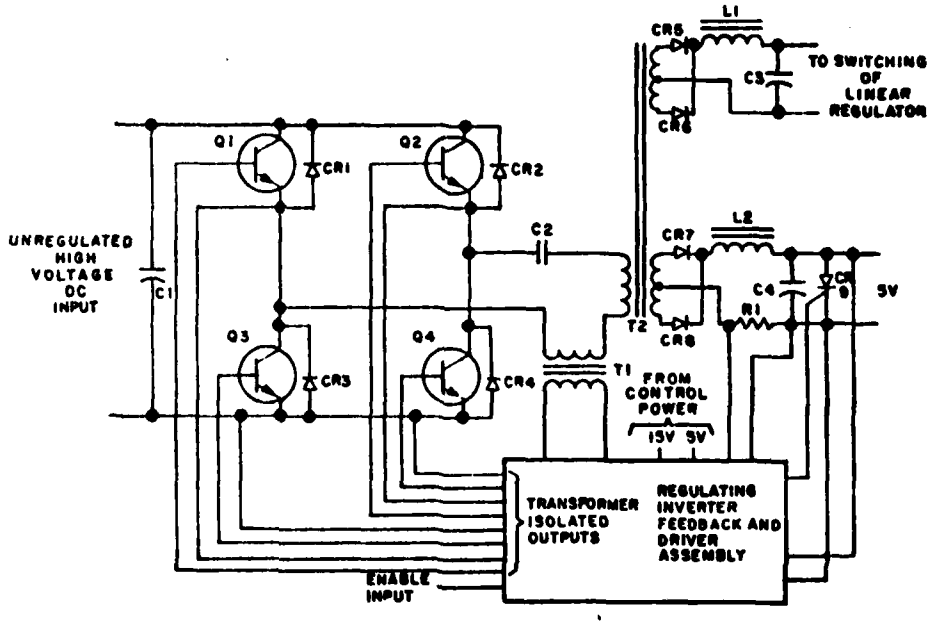


Figure 62 - Simplified Regulating Inverter Schematic

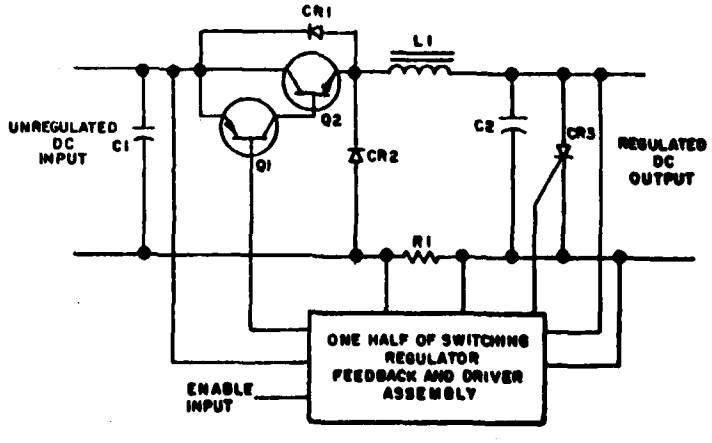


Figure 63 - Simplified Switching Regulator Schematic

i. Conditions required to initiate a power-on sequence include the following:

(1) Input voltage within tolerance.

(2) Temperature within normal limits.

(3) Input enable signal is low.

j. Conditions initiating a power-off sequence include the following:

(1) Low input voltage.

(2) Missing input phase.

(3) Temperature exceeding the higher thermostatic switch temperature.

(4) Input enable signal is high.

k. Protective circuit design techniques and component derating in compliance with RM-533D2-1 further ensure a reliable operating system.

l. In Table 20 are shown the significant test parameters of the PCM-1 and PCM-2. The sub-SRA's of the PCM are shown in Figures 64 through 68. The test parameters for these sub-SRA's are shown in Tables 21 through 23.

TABLE 20

POWER CONVERTER MODULE PCM-1 AND PCM-2 TEST PARAMETERS

SRA configuration: Chassis with 2 analog sub-SRAs and 3 hybrid sub-SRAs		
Active component count:		
	Diodes PCM-1	12
	PCM-2	14
	Bridge rectifiers PCM-1	4
	PCM-2	4
	Heat sink (sub-SRA-4)	
	Hybrid circuits	3
	Voltage regulators	2
	Transistors	4
	Diodes	22
Connector pin count:	68 plus	
Power required:	PCM-1 - 390 watts	
	PCM-2 - 540 watts	

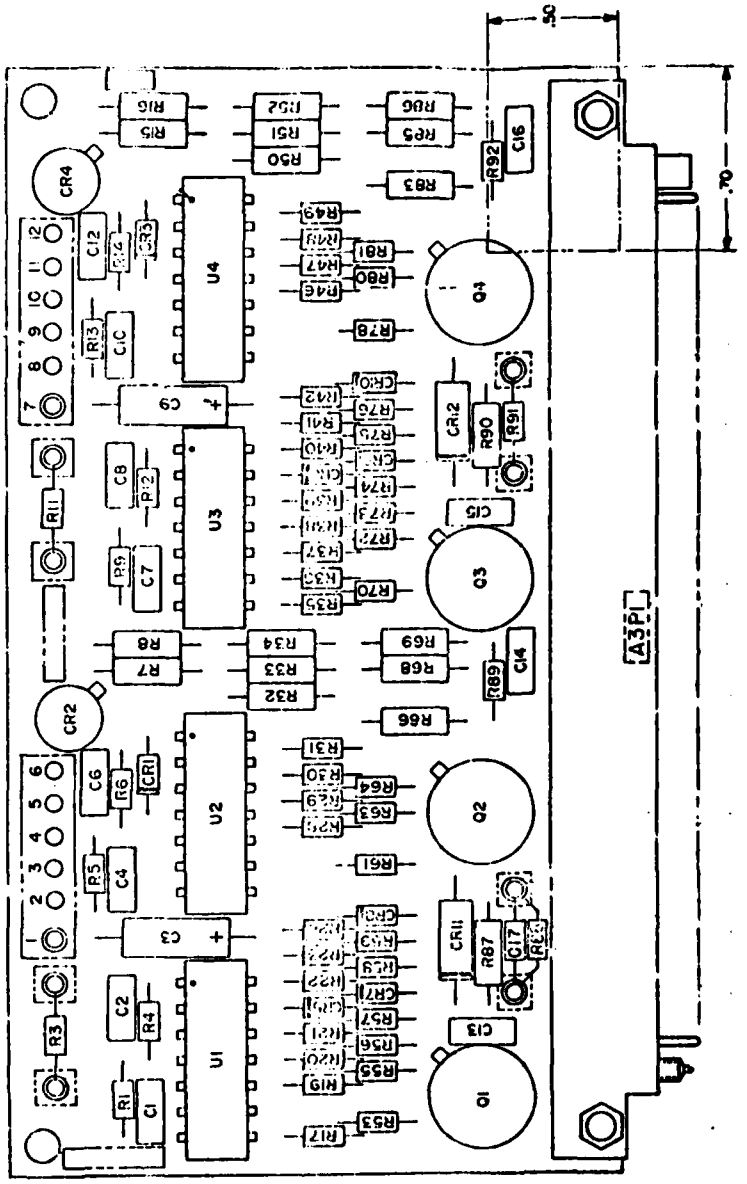


Figure 64 - Power Converter Module Regulator, Sub-SRA-1

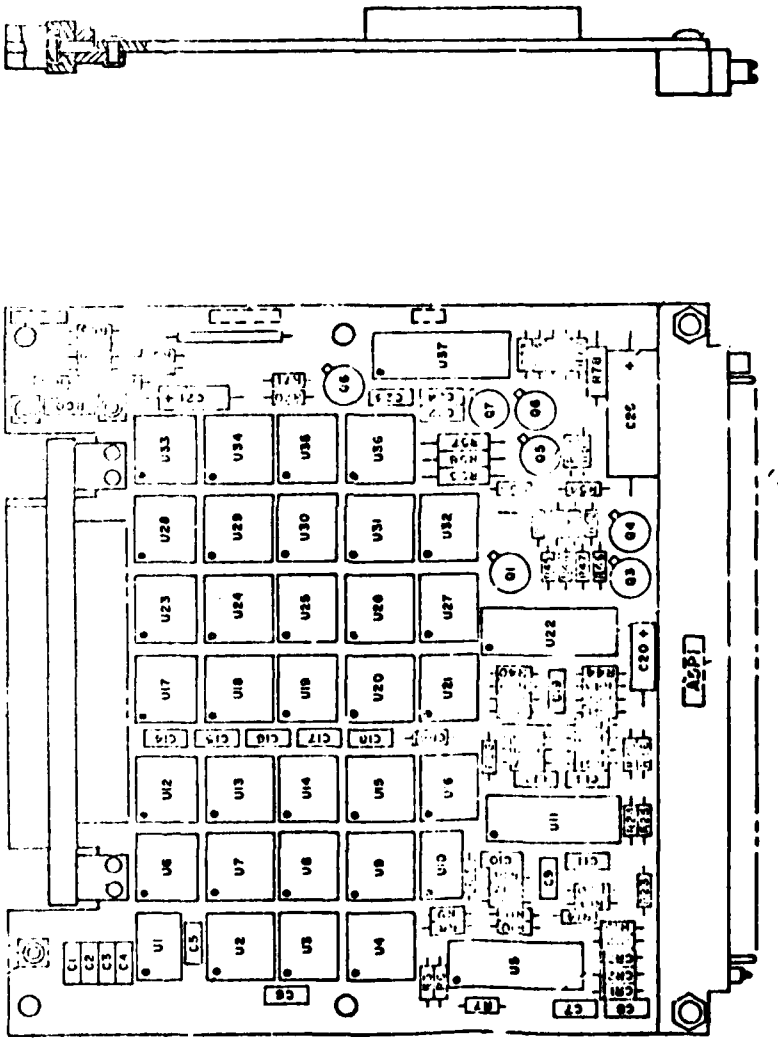


Figure 65 - Power Converter Module Control, Sub-SRA-2

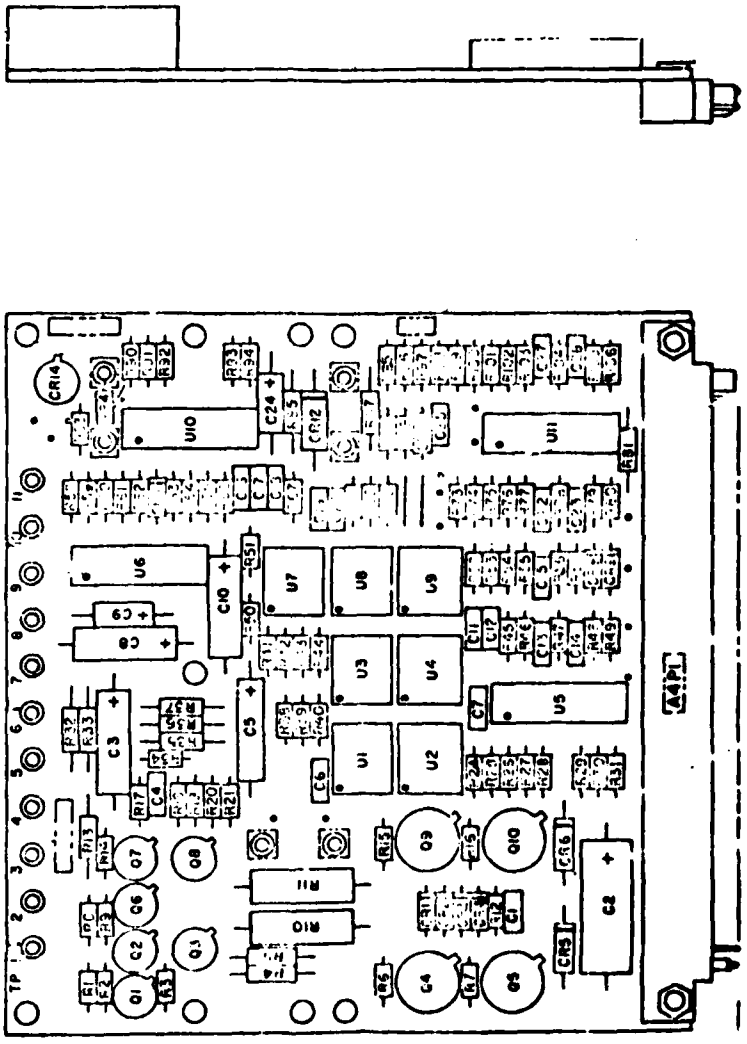


Figure 66 - Power Converter Module Regulator Inverter, Sub-SRA-3

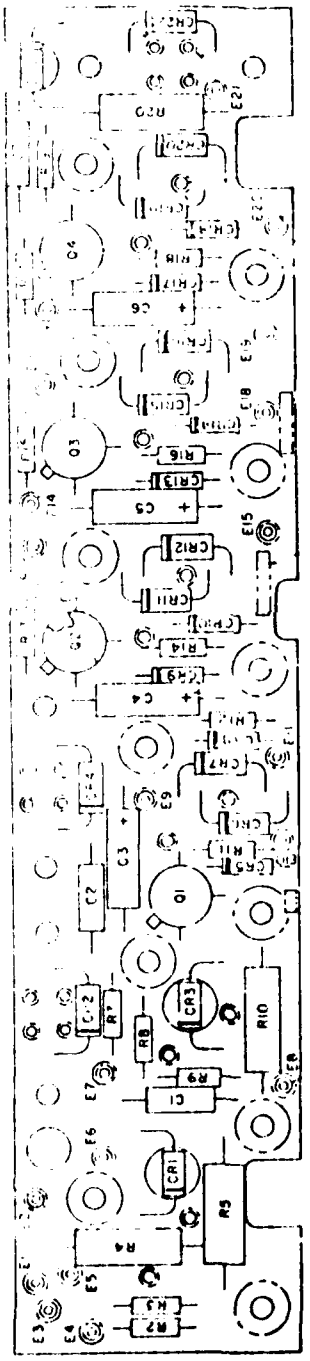


Figure 67 - Power Converter Module Heat Sink, Sub-SRA-1

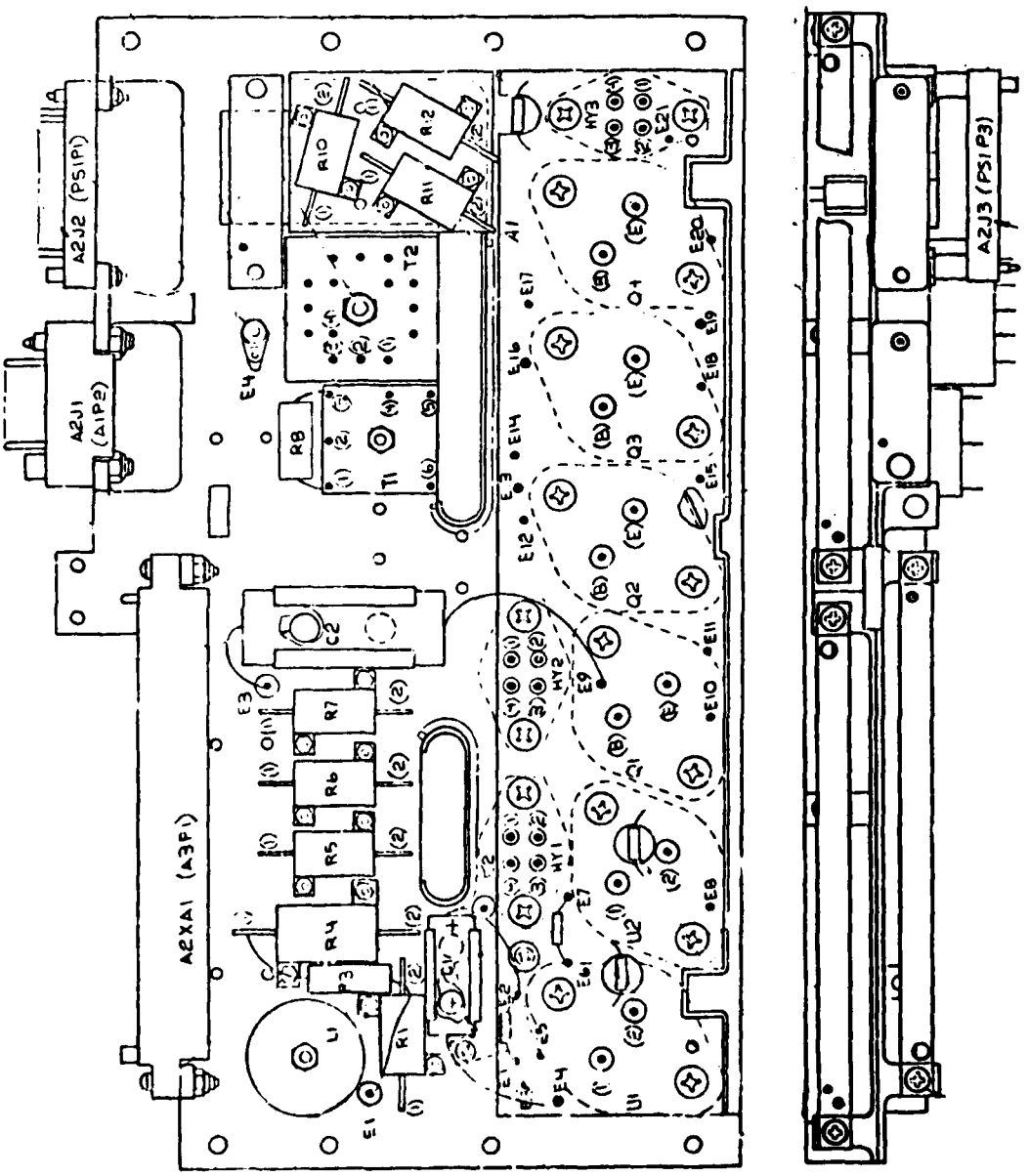


Figure 68 - Power Converter Module Heat Sink Assembly

TABLE 21

[illegible] REGULATOR, SUB-SRA-1 TEST PARAMETERS

Sub-SRA configuration:	Single analog sub-SRA circuit card
[illegible] component count:	
[illegible]	4
[illegible]	4
LED's	2
Diodes	8
Connector pin count:	
Circuit I/O pins	16 pins
Test points	12 pins
Total required	28 pins
Power required	[illegible] vdc, -12 vdc

TABLE 22

[illegible] MODULE CONTROL, SUB-SRA-2 TEST PARAMETERS

Sub-SRA configuration:	Single hybrid sub-SRA circuit card
[illegible] component count:	
Digital:	IC's - MSI (11), SSI (22)
Analog:	4 IC's
	7 transistors
	12 diodes
[illegible] pin count:	P1 - 70 pins
	J1 - 50 pins
	Total - 120 pins
	Input/output - 74 pins
	Test points - 1 pin
	Total required - 75 pins

TABLE 23

POWER CONVERTER MODULE REGULATOR INVERTER, SUB-SRA-3 TEST PARAMETERS

Sub-SRA configuration: Single hybrid sub-SRA circuit card

Active component count:

Digital	-	9 ICs
Analog	-	1 IC
		10 transistors
		1 LED

Connector pin count:

Digital I/O	-	5
Analog I/O	-	20
Test point	-	11
Total required	-	36 pins

[illegible] TEST EQUIPMENT CAPABILITY ANALYSIS

[illegible] test capabilities of eight testers will be re[illegible] maintenance support alternatives for WRA [illegible]

[illegible] Memory Loader/Verifier
[illegible], VAST [illegible]
[illegible], HATS
[illegible], AAI-5365
[illegible], OMOTE II
[illegible]
[illegible], MINI-VAST
[illegible]

[illegible] testers (with the exception of AN/ASM-607, Memory [illegible] evaluated as alternative SRA testers at the [illegible] level.

[illegible], AN/ASM-607 (FIGURE 69)

[illegible] Instrument Inc., Equipment Group, Dallas, TX

[illegible]

[illegible]

[illegible] F-14, A-6E, A-4M, A-7C/D/E, [illegible]

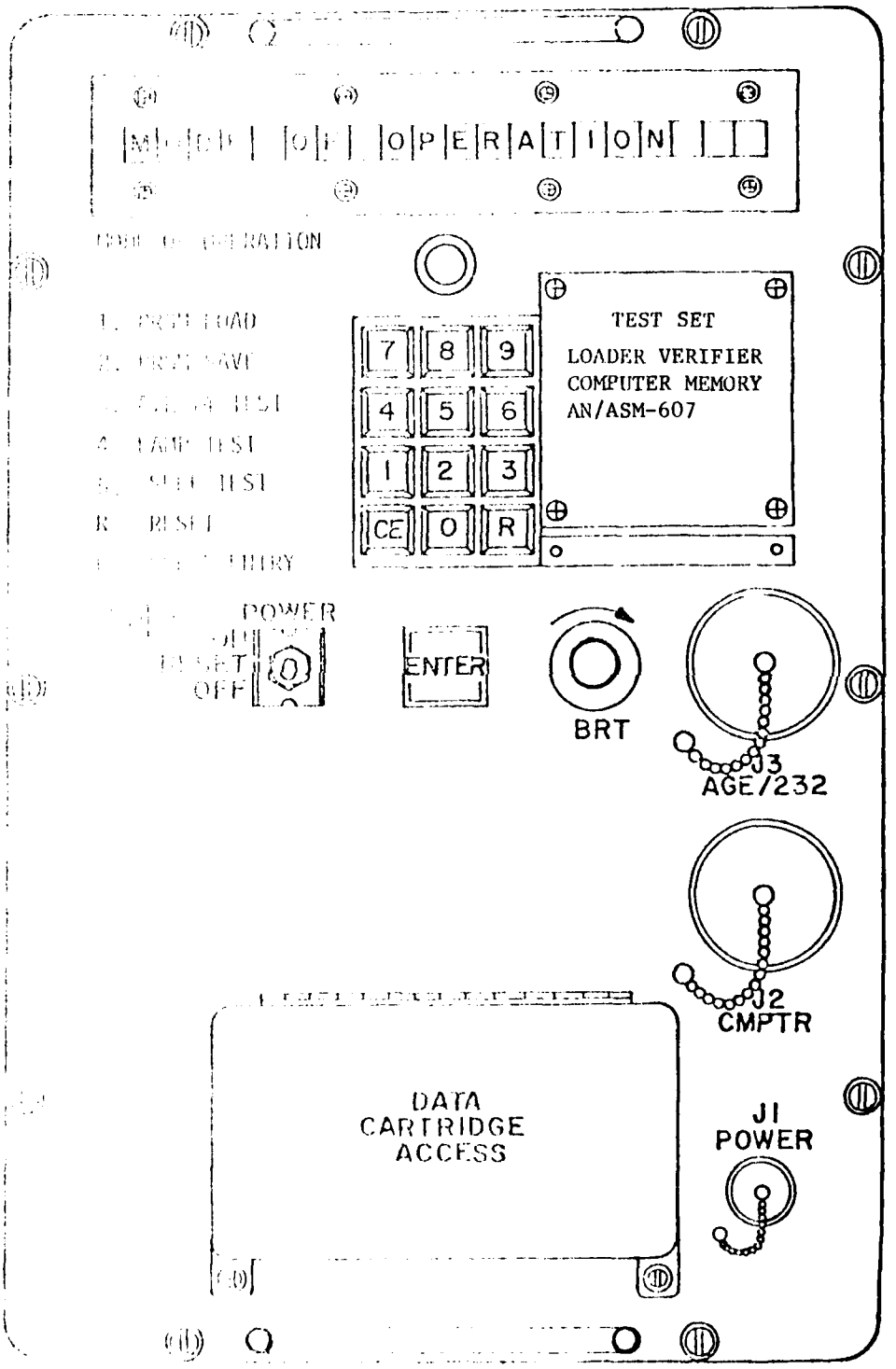
TBD

TBD

[illegible] MIL-T-21200 (Case)

[illegible] Loader/Verifier (MLV) (Figure 69) portable micro[illegible], with proper interfaces, for computer [illegible] loading/verifying of aircraft and ground [illegible] At the organizational level, the MLV can be [illegible] on-board computer via the 1553A MUX bus [illegible] maintenance use, the MLV can be interfaced [illegible] maintenance connecter (J-7) through the MLV's [illegible] of the 1553 MUX Bus computer 155-pin connec[illegible] (Figure 70.)

Figure 69 - Memory Loader/Verifier AN/ASM-607



Memory Loader/Verifier Operator Control Panel

b. In the case of testing an AYK-14 computer, a special computer interface adapter kit is required. This interface adapter kit includes:

- o Input/output interface card (common to all seven configurations of the AYK-14
- o Interface cables: MLV power cable, J-3/J-2 cable, AYK-14 wraparound cable set.
- o Control Program (stored on tape)*
- o SRA Fault Isolation Diagnostic (FID) Program*

* The MLV control program would interface with the SRA diagnostic program and be contained on the same cassette tape (magnetic tape).

TECHNICAL DETAILS

Electrical Design Parameters

Microprocessor (Intel 8080)
20-character Alphanumeric (visible in sunlight)
8192 x 8 bits PROM, 4096 x 8 bits RAM

14.7 mega bits (Raymond Model 6401-01A)
115V, 3Ø, 400 Hz, 1/2 amp
12-Key keyboard, 1 labeled switch

AGE connectors
Software controlled
8 SDC programs, 8 AYK-14 programs

Detects 95% of all possible malfunctions
Software controlled
MUX AGE connector

Mechanical Design Parameters

Combination case to MIL-T-21200
Operator interface/equipment mounting
Modular approach

Front panel heat sink
EMI/moisture sealed
[illegible] pounds

18" x 18" x 12"
Repairable, flexible
Easy door mounting
Accessible through front panel

C. CAT III-D (COMPUTERIZED AUTOMATIC TESTER), AN/USM-429, FIGURE 71

1. DATA SUMMARY

Manufacturer:	Grumman Aerospace Corp., Bethpage, NY
Unit Cost:	$500K
First Deployed:	1975
Aircraft Supported:	E-2C, EA-6B, F-14, A-6E, A-7E, TA-7C, A/F-18, AV-8B
Where Deployed:	Ships: CV-59(1), CV-60(1), CV-61(1), CV-62(1), CV-63(1), CV-64(1), CVN-65(1), CV-66(1) CV-67(1), CVN-68(1) CVN-69(1), CVN-70(1)
	AIMDs: MIR(1), Mugu(1), Oceana(1), NORVA(1)
	NAMTDs: MIR(1)
	NARFs: NORIS(1), NORVA(1)
	Vendors: GAC(7), PRD(1), LTV(1)
Planned Deployment:	AIMDs: Alameda(1), El Toro(1), Lemoore(1), JAX(1), Cecil(1), Yuma(1), Cherry Pt.(1), Beaufort(1), PAX(1), Whidbey Is.(1), Pensacola(1)
No. of TPSs:	Approximately 6 (for WRAs) and 906 (for SRAs)
Specifications:	Best commerical practices

2. DESCRIPTION. The CAT III-D (AN/USM-429) tests analog, digital, and hybrid SRAs from DC to 50 MHz. CAT III-D is of second generation technology with the following salient points:

a. Most powerful dynamic digital circuit card tester presently in inventory: 432 pins, 256 bits deep at 10 MHz.

b. On-line interpretive compiling in BASIC language.

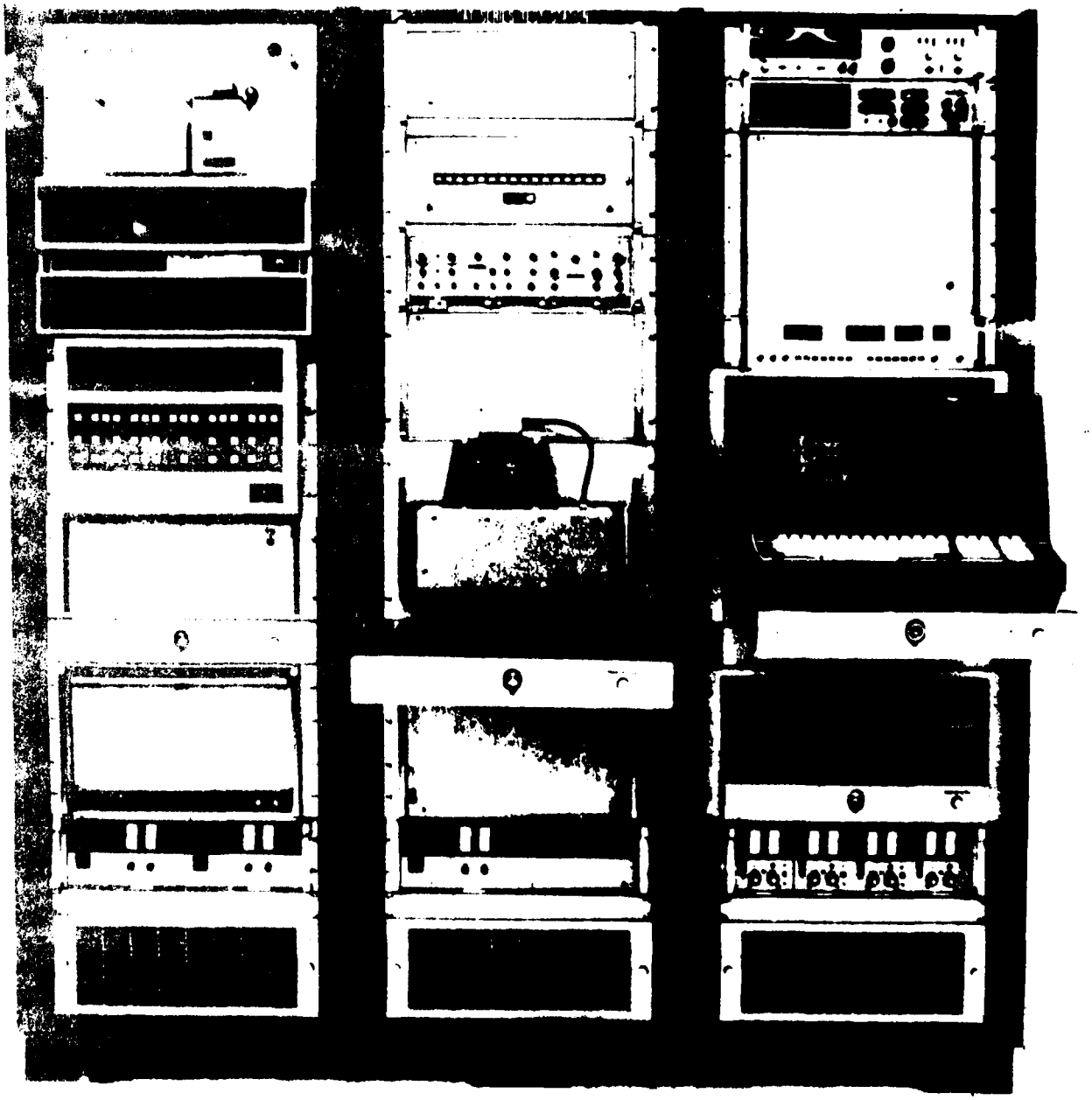


Figure 71 - CAT III-D, AN/USM-429

3. TECHNICAL DETAILS

STIMULUS

Sine:	(.01 - 12.9M)Hz	Pulse:	PRF: (25 - 25M)Hz
Square:	(.01 - 12.9M)Hz		PW: (15n - 40m)sec
Triangle:	(.01 - 12.9M)Hz		Delay: (15n - 10m)sec
			Rise/Fall: (7n - 50μ)sec

MEASUREMENT

AC Volts:	(0 - 500)V, (45 - 100M)Hz	Frequency:	(0 - 100M)Hz
DC Volts:	(1m - 500)V	Time:	(100n - 10^9)sec
Resistance:	(0 - 10M)ohms		

DIGITAL

I/O Pins:	437	Max Skew (DWG):	50 nsec
Programmable Pins:	432	Word Depth:	256, expandable to 1024
Data Rate:	DC - 10MHz	Logic Level	±20V, ±5

POWER SUPPLY

Total 8 Programmable Power Supplies

(1)±(0 - 6)VDC, 10a	(4)±(0 - 36)VDC, 3a
(1)±(0 - 15)VDC, 6a	(2)±(0 - 55)VDC, 2a

COMPUTER AND PERIPHERALS

Computer

Computer Manufacturer:	HP 21MX Series E (ECP Version); HP 2100S (prior version)
Word Length:	16 bits
Memory Size:	128K
DMA Channels:	1
I/O Channels	14
Speed:	350 nsec
Bus:	IEEE-488-1975
No. of Interface Pins:	528, (Programmable-480)

Peripherals

CRT with keyboard:	24 line, 80 char, ASCII keyboard (colorgraphic on ECP Version)
Printer:	250Lpm, 80 char/line
Disc Memory:	2 Discs, one fixed, one removable Storage: 2.45MBytes/disc Data Transmission Rate: 2.5Bits/sec
Paper Tape Reader:	300 char/sec
TTY:	No
Software Development Station:	Yes

Software Features

Language:	ATLAS and BASIC
OP System:	Disc
Self Test:	Self-test and diagnostic capability
Method of Translation:	2-pass ATS Basic compiler (on-line)
CASAR Compatible:	Yes
Other:	Full capability to edit source language programs. LOGOS compatible Model V(1) ECP . (Fault Isolation) has guided probe capability. . Manchester Bus Interface, compatible with MIL-STD-1553B.

D. HATS (HYBRID AUTOMATIC TEST SYSTEM), AN/USM-403(V), FIGURE 72

1. DATA SUMMARY

Manufacturer:	General Dynamics, San Diego, CA	
Unit Cost:	$800K	
First Deployed:	1975	
Aircraft Supported:	S-3A	
Where Deployed:	Ships:	CV-59(1), CV-60(1), CV-61(1), CV-62(1), CV-63(1), CV-64(1), CVN-65(1), CV-66(1), CV-67(1), CVN-68(1), CVN-69(1)
	AIMDs:	NORIS(2), Cecil(2), PAX(1)
	NAMTDs:	MIR(1)
	NARFs:	Alameda(1)
	Vendors:	GD(1), LAC(3)
No. of TPSs:	Approx:	750 (for SRAs)
Specifications:	Best commercial practices	

2. DESCRIPTION. The HATS (AN/USM-403) test analog, digital, and hybrid SRAs from DC to 300 MHz. HATS uses advanced third-generation stimulus and measurement, and provides the following features:

a. A programmable interface unit that minimizes the need for adapters other than for connector matching.

b. An on-line ATLAS Interpreter for on-station TPS generation.

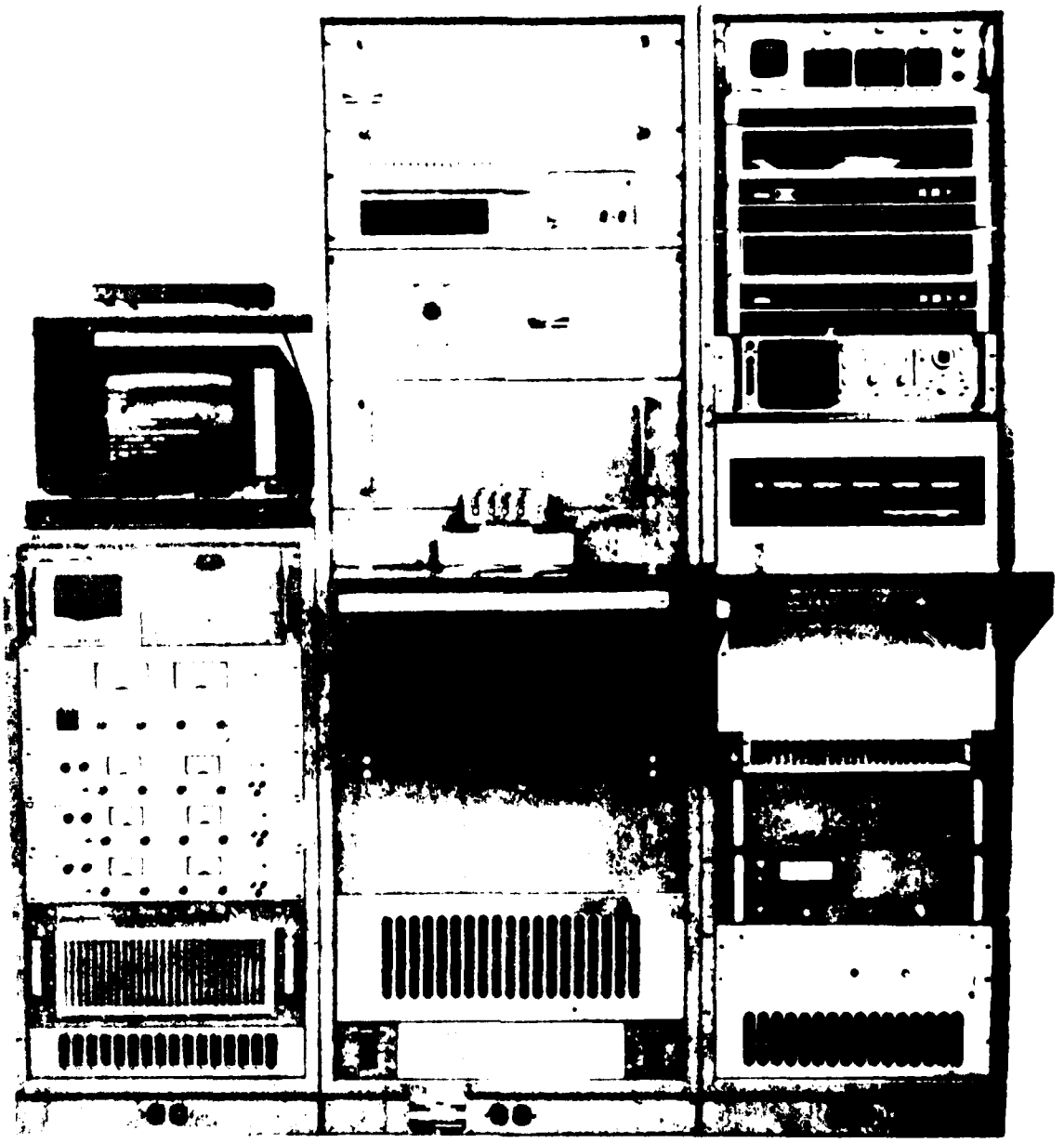


FIGURE 72 - BATS, AN/USM-403 (V)

3. TECHNICAL DETAILS

STIMULUS

Sine:	(.01 - 3M)Hz	Triangle:	(.01 - 50K)Hz
Square:	(.01 - 1M)Hz	Sawtooth:	(.01 - 100K)Hz
Pulse: PRF:	(100 - 4M)Hz	Resistive Loads:	(51 - 5302)ohms, prog.
PW:	(100n - 60)sec	Synchro/Res:	11.8V/0° - 360°/400Hz

MEASUREMENT

AC Volts:	(20m - 500)V, (2 - 200M)Hz	Angle Position:	0° - 360°
DC Volts	±(1m - 500)V	Waveform:	(1 - 300M)Hz
Resistance:	(.1 - 10M)ohms		(1m - 500)V
Frequency:	(0 - 300M)Hz	Distortion:	(2 - 10M)Hz
Time:	(100n - 60)sec	Spectrum:	(1 - 300M)Hz
Phase Angle:	(0° - 360°) / (2 - 40K)Hz		(1m - 500)V
Oscilloscope:	(manual), (0 - 50M)Hz (HP-181AR)	Network:	(2 - 300M)Hz, 0° - 360°
		Capacitance:	(10p - 10μ)farads

DIGITAL

Programmable Pins:	160	Logic Level:	±20
Data Rate:	DC - 1MHz	Max Skew:	30nsec, (60nsec/50 pins)
Word Depth:	256 bits		

POWER SUPPLY

(5) Programmable DC Power Supplies

(3) ±(0 - 40)VDC, 5a
±(0 - 40)VDC, 30a
±(0 - 200)VDC, .5a
(154 Voltage Sources)
(154 +(0 - 30)VDC, 100ma

(1) Programmable AC Power Supplies

(1) (.5 - 130)VRMS, 50va, (45 - 10K)Hz

COMPUTER AND PERIPHERALS

Computer

Computer Manufacturer:	Varian V-620-100
Word Length:	16 bits
Memory Size:	24K (expandable to 32K)
DMA Channels:	1
I/O Channels:	2
Speed:	2 μsec
Bus:	IEEE-488-1975
No. of Interface Pins:	385, (programmable - 160)

Peripherals

CRT with Keyboard:	24 line, 80 char, 9600 baud; 72-key keyboard
Printer:	30 char/sec, ASC II Code, 80 char/line
Disc Memory:	Storage: 2.3M words
Paper Tape Reader:	Remex Model RR305 or equiv.
Software Development Station:	No

Software Features

Language:	ATLAS(ARINC 416-8)
Operating System:	Disc
Self-Test:	Has self-test, diagnostics and calibration capability
Method of Translation:	On-line interpreter
CASAR Compatible:	Yes
Other:	On-line probing capability

E. AAI-5565 AUTOMATIC TEST SYSTEM (AN/USM-449), FIGURE 73

1. DATA SUMMARY

Manufacturer:	Aircraft Armaments, Cockeyesville, MD	
Unit Cost:	$600K	
First Deployed:	1978	
Aircraft Supported:	P-3	
Where Deployed:	Ships:	None
	AIMDs:	Barbers Pt(1), Brunswick(1), Agana(1), Cubi Pt(1), Keflavik(1), Moffett(1), Jacksonville(1), Kadena(1), Sigonella(1), Misawa(1).
	NAMTDs:	Moffett(1), Jax(1)
	NARFs:	None
	Foreign:	Australian Air Force (1)
(Planned)Deployment:	Ships:	None
	AIMDs:	Jax(1), Bermuda(1), Lages(1), Glen View(1), PAX(1), Rota(1), Willow Grove(1), Weymouth(1), New Orleans(1), Detroit(1), Whidbey(1), Van ATL(1), Van PAC(1)
	NAMTDs:	U.S. Air Force(1)
	NARFs:	NORVA(1), Alameda(2), JAX(1)
	Vendors:	AAI(2)
	Foreign:	Australian AF(1), Norway(1)
No. of TPSs:	Approx. 31 (For WRA's) and 1019 (For SRA's)	
Specifications:	Best commercial practices	

2. DESCRIPTION. The AAI-5565 Automatic Test System (AN/USM-449) tests analog, digital and hybrid WRA's and SRA's from DC to 3GHz. The AAI-5565 is of second generation technology, with the following principal features:

a. It is a combination of two testers: the AAI-5500, 1970 vintage analog/hybrid depot tester; and the AAI-6650, a 1975 vintage dynamic digital tester.

Figure 73 - AAI-5565 ATE System (AN/USM-449)

b. Has dual-port capability (static and hybrid).

c. On-line compiling in ATLAS.

d. Hundreds of existing TPSs developed on the AAI-5500, used at NAVAIREWORKFAC; are upward compatible on the AAI-5565.

3. TECHNICAL DETAILS

STIMULUS

Sine:	(.01 - 1M)Hz	Triangle:	(.01 - 1M)Hz
Square:	(.01 - 1M)Hz	Ramp:	(.01 - 1M)Hz
Pulse: PRF -	(9.9 - 9.9M)Hz	Resistive Loads:	(.1 -30K)ohms
PW -	(40u - 9.99m)sec	Synchro/Res:	(11.8, 26, 90V/ 0° - 360° /400Hz)
RF Gen:	(.1M - 1.3G)Hz		

MEASUREMENTS

AC Volts:	(0 - 1K)V, (20 - 1M)Hz to 7.5KV (w/probe)	Frequency:	(3 - 3G)Hz
		Time:	(10μ - 99.99)sec
DC Volts	(0 - 1K)V; to 10KV (w/probe)	Period:	(10n - 99m)sec
RF Volts:	(3m - 3)V, (25K - 500M)Hz	Capacitance:	(10p - 10m)farads
Resistance:	(0 - 10M)ohms	Oscilloscope:	(manual)w/probe
Synchro/Res:	(11.8, 26, 90) V/0° - 360°/400Hz	Phase Angle:	(0° - 360°)

DIGITAL

Programmable Pins:	128(expandable to 240)	Max Skew:	±15 nsec
Data Rate:	DC-10MHz	Logic Level:	±5V, ±20V
Word Depth:	256 bits*		

*Depths can be added in 256-bit increments, pin-to-pin as required.

POWER SUPPLY

Total 17 Programmable and 2 Fixed Power Supplies

(4)	+(0 - 32)VDC, 2a	(2)	±(0 - 199)VDC, 200ma
	+(0 - 32)VDC, 3a	(2)	±(0 - 50)VDC, 10a
(2)	+(0 - 50)VDC, 1a		±(0 - 20K)VDC, 2ma
	+(0 - 500)VDC, 200ma		
(2)	+(0 - 28)VDC, 3a		±28 VDC, 20a
(2)	+(0 - 300)VDC, 200ma		±5 VDC, 2.5a

Total 16 AC Power Supplies 13 Fixed, 2 Programmable, 1 Manual

120 VRMS, 10a, 60Hz, 1 phase	30 VRMS, .75a, 400Hz, 3 phase
120 VRMS, 3a, 400Hz, 1 phase	120 VRMS, 130ma, 400Hz, 3 phase
120 VRMS, 5a, 400Hz, 3 phase	30 VRMS, .75a, 400Hz, 1 phase
(2) 6.3 VRMS, 10a, 400Hz, 1 phase	120 VRMS, 130ma, 400Hz, 1 phase
11.8 VRMS, 2a, 400Hz, 3 phase	
26 VRMS, .75a, 400Hz, 3 phase	(2) (1m - 60)VRMS, 70ma, 400Hz 3 phase, prog.
69.3 VRMS, .25a, 400Hz, 3 phase	
6.8 VRMS, 3a, 400Hz, 3 phase	(0 - 130)VRMS, 5a, 400Hz, 3 phase (manual)

COMPUTER AND PERIPHERALS

Computer

Computer Manufacturer:	Interdata 8/16
Word Length:	16 bits
Memory Size:	64K bytes
DMA Channels:	DNA*
Speed:	DNA
No. of Interface Pins:	(Both Ports): 1712, (programmable 880)

Peripherals

CRT with Keyboard:	Yes
Printer:	(2), 300Lpm, 72 col wide
Disc Memory:	(1) Floppy, 250K Bytes, (1) Disc, 50M Bytes
Paper Tape Reader:	Optional
Software Development Station:	Yes

Software Features

Language:	ATLAS IEEE-416-13
OP System:	Disc
Self-Test:	Diagnostic & calibration (on-line)
Method of Translation:	On-Line Interpreter/Off-Line ATLAS Compiler
LASAR Compatible:	Yes
Other:	DETOL as secondary language

* DNA - Data not available in manufacturer's specification.

. DIMOTE II, TEST SET, ELECTRONIC SYSTEMS (AN/USM-453B), FIGURE 74

1. DATA SUMMARY

Manufacturer:	Sperry Microwave Electronics Div., Clearwater, FL	
Unit Cost:	200K (per 1979)	
First Deployed:	1978	
Aircraft Supported:	A-7, TARPS-Pod, ITCS, AN/AWM-67	
Where Deployed:	Ships:	CV-59(1), CV-60(1), CV-61(1), CV-62(1), CV-63(1), CV-64(1), CVN-65(1), CV-66(1), CV-67(1), CVN-68(1), CVN-69(1), CVN-70(1)
	AIMDs:	Lemoore(2), Cecil(1), Key West(1)
	NAMTDs:	Lemoore (1)
	NARFs:	JAX(1)
	Vendors:	Sperry(3), LTV(2), Motorola(3)
No. of TPSs:	Approx: 5 (For WRAs) and 112 (For SRAs)	
Specifications:	MIL-T-28800	

2. DESCRIPTION. The Test Set, Electronic Systems (AN/USM-453B), which is frequently referred to as DIMOTE II (Digital Module Tester), tests the less complex analog, digital, and hybrid SRAs from DC to 20MHz. DIMOTE II is of second-generation technology; it is IEEE/488 compatible, and significantly less expensive than the other testers in the inventory, but also limited in the following areas:

a. Cannot automatically isolate faults to the small ambiguity groups that the larger testers can.

b. Does not have an on-line compiling capability.

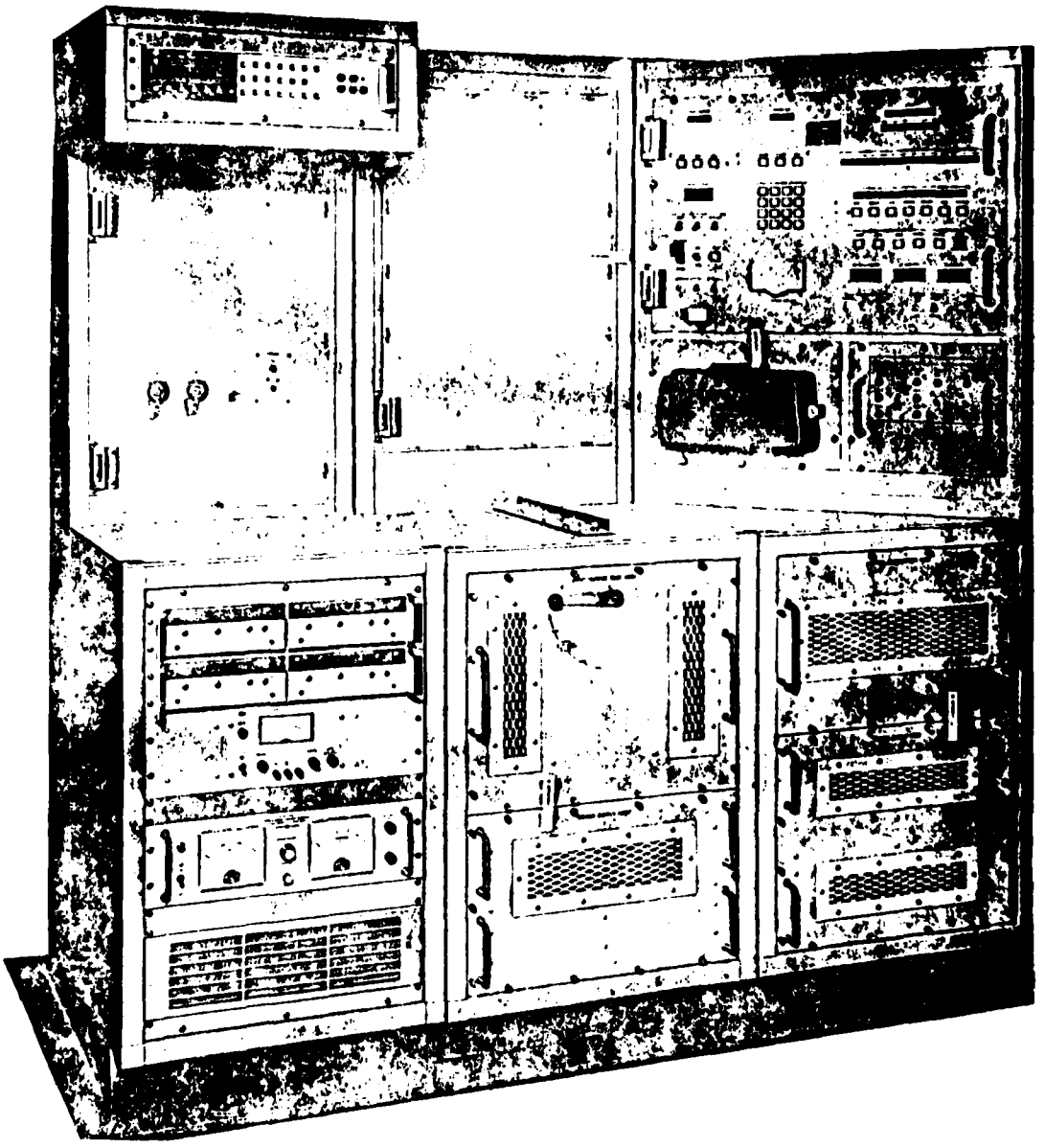


Figure 74 - Test Set, Electronic Systems (AN/USM-453B)
DIMOTE II

3. TECHNICAL DETAILS

STIMULUS

Sine:	(1 - 100K)Hz	Sawtooth:	(1 - 100K)Hz
Square:	(1 - 100K)Hz	Arbitrary:	(1 - 100K)Hz
Triangle:	(1 - 100K)Hz	AC Buffer Amplifier:	26V/150ma
Synchro/Res:	(11.8, 26)V/0°- 360°/400Hz		

MEASUREMENT

AC Volts:	(1m - 100)V, (10 - 1K)Hz	Time:	(100n-9.99)sec
DC Volts:	(1m - 100)V	Period:	(200n-9.99)sec
Resistance:	(10 - 1M)ohms	Events:	(1-99M)events
Frequency:	(100 - 20M)Hz	Oscilloscope:	(TEK 465M)
Synchro/Res:	(11.8, 26)V/0° - 360°/400Hz		

DIGITAL

I/O Pins:	96, expandable to 192	Word Depth:	256
Data Rate:	(1 - 10M)Hz	Logic Levels:	(-12 to +28)V

POWER SUPPLY

Total 4 Programmable and 2 Fixed Power Supplies

(2)±(2.5 - 28)VDC, 500ma, Prog.
(1)±(2.5 - 15)VDC, 500ma, Prog.
(1)±(3-15)VDC, 1a, Prog.
(1)+5VDC, 2.5a, Fixed
(1)+28VDC, 1a, Fixed

COMPUTER AND PERIPHERALS

Computer

Computer Manufacturer:	Sperry Microwave, FL
Word Length:	8 bits (microprocessor)
Memory Size:	32K words
DMA Channels:	DNA*
Speed:	DNA
No. of Interface Pins:	280, (programmable - 96 (expandable to 192))
Bus:	IEEE-488-1975

Peripherals

CRT with Keyboard:	No
Printer:	No
Disc Memory:	No
Magnetic Cartridge:	4 track
Software Development Station:	No

Software Features

Language:	Machine and Slang (Sperry Test Language)
OP System:	Microprocessor Controlled
Self-Test:	Yes, On-line
Method of Translation:	Sperry Test Language Compiler (Off-line)
LASAR Compatible:	Yes, LASAR/AFLASH
Other:	Has guided probe capability

* DNA - Data not available in manufacturer's specification.

G. NSTS (NAVIGATION SYSTEM TEST SET), AN/ASM-608(V), FIGURE 75

1. DATA SUMMARY

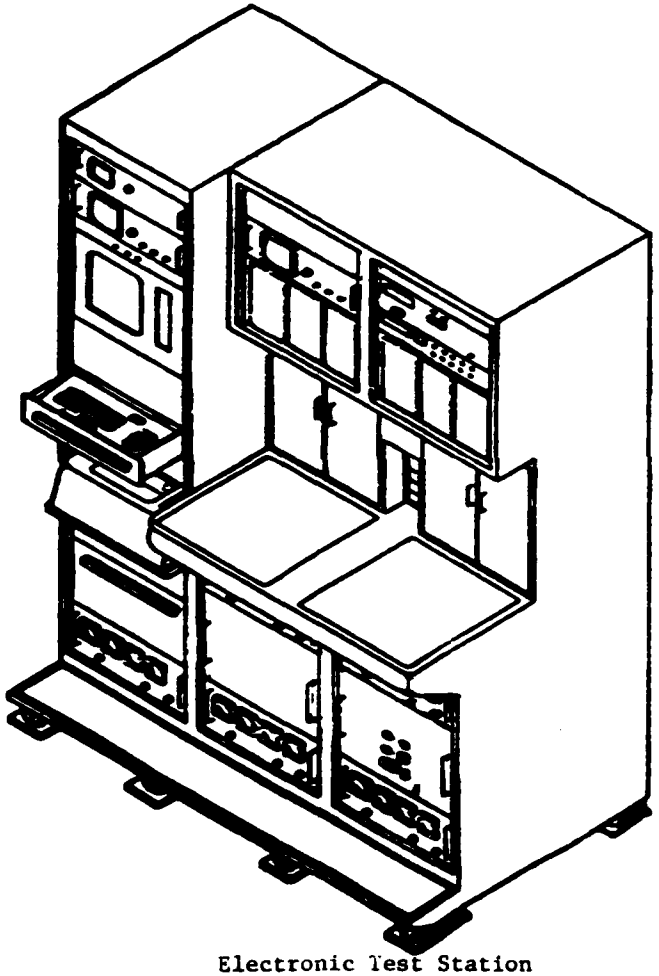
Manufacturer:	Litton/Guidance and Control Systems, Woodland Hills, CA
Unit Cost:	$450K (IMUTS)
First Deployed:	1978
Aircraft Supported:	F-14, E-2C, S-3A, A-6E, RF-4B
Where Deployed:	Ships: None
	AIMDs: El Toro (2), Iwakuni (1)
	NAMTDs: El Toro (1)
	NARFs: NORIS (1)
	Vendors: None
No. of TPS's:	5 (for WRAs) and 8 (for SRAs)
Specifications:	MIL-T-28800

2. DESCRIPTION. The NSTS (Navigation System Test Set), AN/ASM-608(V), tests analog, digital and hybrid WRAs and SRAs from DC to 100MHz. NSTS is of second-generation technology, with the following main features:

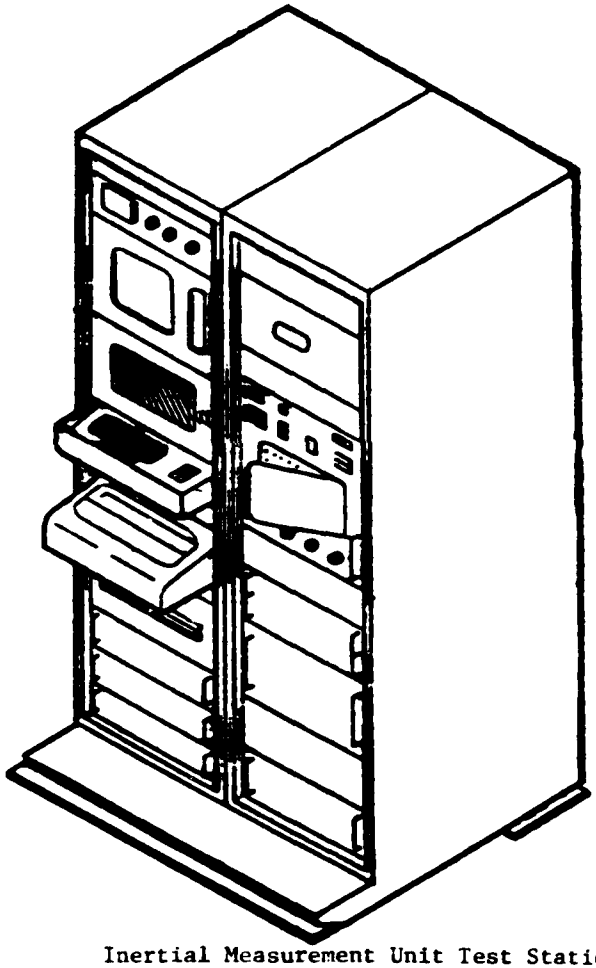
a. It is a combination of a two-bay, stand-alone tester called Inertial Measurement Unit Test Set (IMUTS), and a three-bay electronic stimulus and measurement section called the Electronic Test Station (ETS), which is IMUTS dependent.

b. On-line ATLAS interpretive compiling.

c. Compatible with IEEE/488 Instrumentation Data Bus.



Electronic Test Station
(ETS)



Inertial Measurement Unit Test Station
(IMUTS)

NAEC-92-138

Figure 75 - NSTS (Navigation System Test Set) AV/ASM-608(V)

3. TECHNICAL DETAILS

STIMULUS

Sine:	(10m - 13M)Hz	Triangle:	(10m - 13M)Hz
Square:	(10m - 13M)Hz	Sawtooth:	(1 - 1M)Hz

MEASUREMENT

AC Volts:	(20m -1K)V, (20 - 300K)Hz	Phase Angle:	(2 - 100K)Hz, 0^{o} - 360^{o}
DC Volts:	(2m - 1K)V	Wave Form:	(20m - 1K)V, (20 - 300K)Hz
Resistance:	(0 - 100M) ohms	Distortion:	to 4.8KHz
Time:	(100n - 10^{9})sec	Oscilloscope:	(0 - 60M)Hz, (TekR7603)
Synchro/Res:	26V/0^{o} - 360^{o}/400Hz		

DIGITAL

I/O Pins:	326	Logic Level:	±30V
Data Rate:	DC - 10MHz	Max Skew:	100 nsec
Word Depth	128 bits		

POWER SUPPLY

Total (6) Programmable and (1) Fixed DC Power Supplies

(1) ±(0 - 40)VDC, 20a
(2) ±(0 - 6) VDC, 8a
(1) ±15VDC, .5a, (Fixed)
(2) ±(0 - 42)VDC, 5a
(1) ±(0 - 85)VDC, 2.5a

Total (2) Fixed AC Power Supplies, (1) D/A Converter

26 VAC, 1a, 400Hz, 1 phase
115VAC, 9a, 400Hz, 3 phase
(0 - 115)VAC, 60a, 400Hz (D/A Converter)

COMPUTER AND PERIPHERALS

Computer

Computer Manufacturer:	Turpin 1000 - (Emulated PDP 11/35)
Word Length:	16 bits
Memory Size:	64K words
DMA Channels:	DNA
Speed:	8.5khz
Bus:	IEEE 488
No. of Interface Pins:	1,248

Peripherals

CRT with Keyboard:	Yes, with Colorgraphs
Printer:	Yes
Disc Memory:	Yes
Software Development Station:	No

Software Features

Language:	ATLAS
OP System:	Disc
Self-Test:	Yes
Method of Translation.	On-Line Interpreter
LASAR Compatible:	Yes
Other:	Fortran Z for self-test

NOTE: DNA - Data not available in manufacturer's specification.

H. MINI-VAST, AN/USM-470(V)1, FIGURE 76

1. DATA SUMMARY

Manufacturer:	PRD Electronics Co., Syosset, NY
Unit Cost:	$2.8 million
First Deployed (future):	1982
Aircraft Supported (future):	F-18
Where Deployed (Future):	6 AIMDs, 12 Carriers, 2 NAMTDs, 1 NARF
No. of TPSs (future):	Approx 40 (for WRAs)
Specifications:	MIL-T-28800

2. DESCRIPTION. The MINI-VAST test station tests digital, analog, and hybrid WRAs and SRAs from DC to 100 MHz. MINI-VAST is a combination of second-generation stimulus building blocks from VAST and commercial sources, and a third-generation sampling and measurement system with improved digital testing performance over the existing VAST stations. In addition, it has a full on-line ATLAS interpretive compiler and is compatibile with IEEE/488 Instrumentation Data Bus.

Figure 76 - MINI-VAST, AN/USM-470(V)1

3. TECHNICAL DETAILS

STIMULUS

Sine:		(0 - 20M)Hz	Triangle:	(0 - 10K)Hz
Square:		(0 - 10M)Hz	Ramp/Step:	(0 - 10M)Hz
Pulse:	PRF-	(1 - 5M)Hz	Delays:	(200n - 9.99)sec
	P.W.	(.3m - .999m)sec	Resistive Loads:	(1 - 99.9K)ohms, (1-5)W
Pressure:		(-1500 to 100K) ft		(1-5K)ohms, (1-500)W
	Static -	(.157 - 15.5)psi	Video:	(511 - 1023) lines
	Dynamic -	(.038 - 36.1)psi		30 frames/sec, (35MHz Bandwidth)
Syncro/Res:		(11.8, 26, 90)V; (100, 400, 800)Hz/0° - 360°		

MEASUREMENT

AC Volts:	(.01 - 999)V	Time:	(.1m - 10)sec
DC Volts:	(.01 - 999)V	Phase Angle:	(10 - 100K)Hz/0° - 180°
Resistance:	(.1 - 10M)ohm	Events:	50n sec(pw); $(1-10^9)$pulse
Frequency:	(.1 - 100M)Hz	Distortion:	0 - 25MHz
Video:	(511 - 1023)lines, 30 frames/sec sample aperture: 100n sec video bandwidth: 35MHz		

DIGITAL

I	O	I/O	Depth	Rate	Logic Level
-	-	8 RZ/NRZ	8192	4 MHz	±30v
-	-	144	1	200 kHz	±30v
32	32	-	1	200 kHz	±30v
-	-	32	1024	10 MHz	±30v
-	-	32	1024	10 MHz	±30v
-	-	64	4096	10 MHz	±30v
-	-	112	1024	10 MHz	±30v

POWER SUPPLY

DC Supplies:

6 Fixed PS (DC)

(2) +5VDC, 3a
(2) +12VDC, 2a
+28VDC, 5a
(1) +(28 or 12) VDC, 600ma

13 Programmable PS (DC)

(3) ±(.1-35)VDC, 2.5a
(3) ±(10-16)VDC, 5a
(3) ±(3-7)VDC, 12a
±(22-32)VDC, 20a
(3) ±(1-35)VDC, 2.5a

AC Power Supply:

4 Fixed PS (AC)

(2) 6.35 VRMS, 10a, 400Hz, single phase
115VRMS, 10a, 400Hz, single phase
115VRMS, 10a, 400Hz, three phase

3 Programmable PS (AC)

(5 - 135)VRMS, 1a, 400Hz, single phase

(2 - 80)VRMS, 10a, 400Hz, single phase

(89 - 135)VRMS, 10a, 400Hz, three phase

COMPUTER AND PERIPHERALS

Computer

Computer Manufacturer:	Harris/6
Word Length:	24 bits
Memory:	64K words
DMA Channels:	3
Speed.	660 nsec
Bus:	IEEE 488
No. of Interface Pins:	1,336 pins, 1,208 programmable

Peripherals

CRT with Keyboard:	Yes
Magnetic Tape:	No*
Card Reader:	No*
Paper Tape Reader:	No*
Printer:	Yes
Disc:	2 CDC Discs; 10MByte/Disc
TTY:	No*

Software

Language:	ATLAS
OP System:	Disc
Self-Test:	Calibration and diagnostic
Method of Translation:	Compiler (on-line and off-line)
LASAR Compatible:	Yes
Software Development Station:	Yes

* Built-in provision for direct plug-in capability.

I. VAST (VERSATILE AVIONICS SHOP TESTER), AN/USM-247, FIGURE 77

1. DATA SUMMARY

Manufacturer:	PRD Electronics Co., Syosset, NY	
Unit Cost:	$4 million	
First Deployed:	1972	
Aircraft Supported:	F-14, E-2C, S-3A, A-7	
Where Deployed:	Ships:	CV-59(3), CV-60(3), CV-61(3), CV-62(3), CV-63(4), CV-64(4), CVN-65(4), CV-66(4), CV-67(4), CVN-68(4), CVN-69(4)
	AIMDs:	Lemoore(2), MIR(6), Mugu(1), NORIS(5), Cecil(5), Key West(6), NORVA(2), Oceana(5), PAX(11)
	NARFs:	Alameda(2), NORIS(2), JAX(1), NORVA(4)
	NAMTDs:	MIR(2), Oceana(3)
	Vendors:	LCC(2), PRD(3), GAC(3), LTV(1), McAIR(1)
No. of TPSs:	Approx:	184 (for WRAs) and 518 (for SRAs)
Specifications:	MIL-T-21200	

2. DESCRIPTION. The AN/USM-247 Versatile Avionics Shop Tester (VAST) tests digital, analog, and hybrid WRAs and SRAs from DC to 18 GHz. VAST is of second-generation technology, with the following salient points:

a. Largest (14 racks), most powerful, comprehensive avionic automatic tester in DOD inventory.

b. No on-line compiling.

c. Test language is VITAL* (VAST Interface Test Application Language) not ATLAS.

d. Ability to add and subtract building blocks to accommodate changing testing requirements.

* VITAL is a computer language especially developed for use with the VAST system.

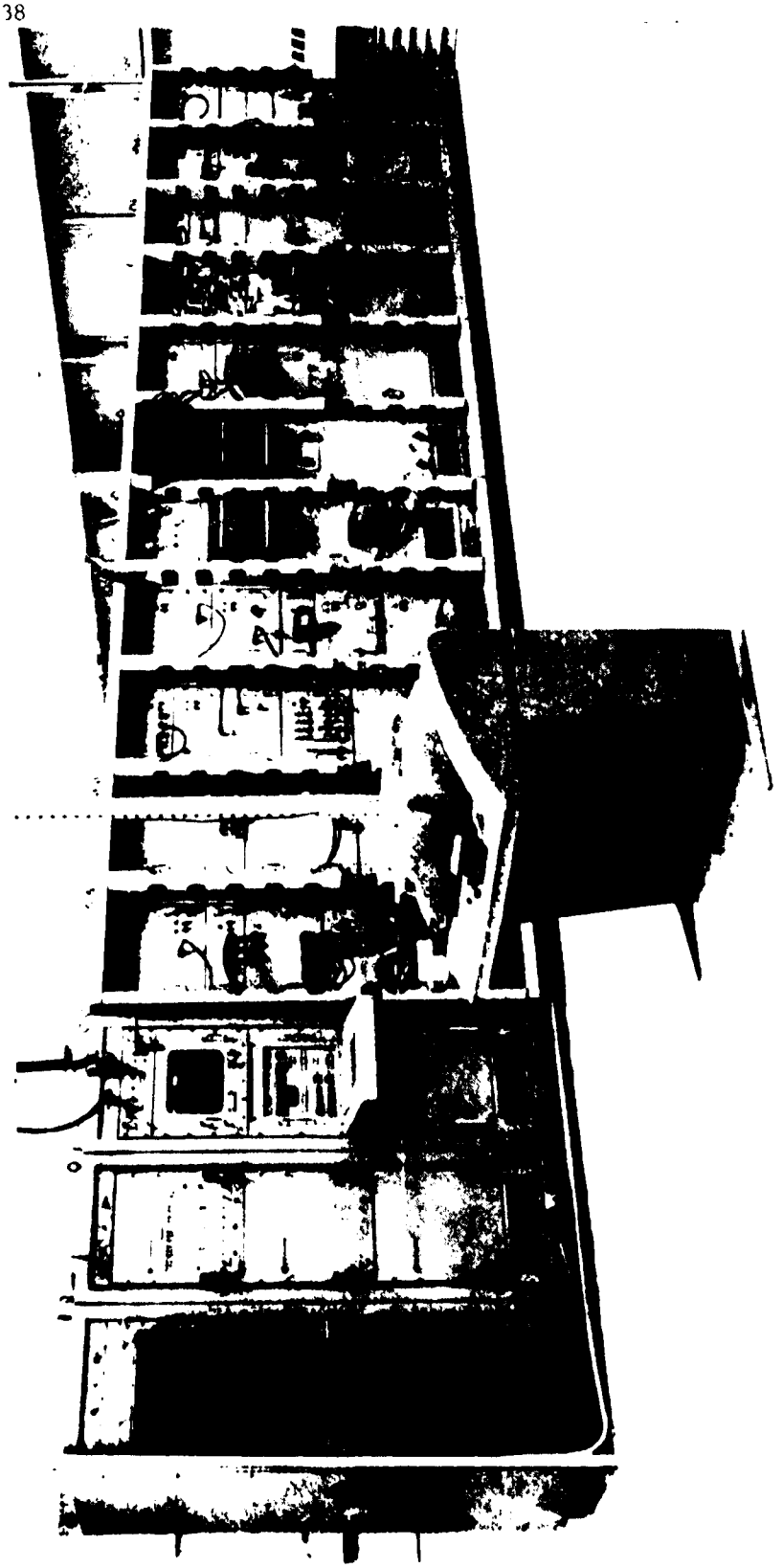


Figure 77 - VAST, AN/USM-247

3. TECHNICAL DETAILS

STIMULUS

Sine:	(.1 - 500M)Hz	Ramps/Steps:	(20 - 10M)Hz
RF:	(.4 - 18)GHz	Synchro/Resolver:	(5 - 125)V/0° - 360°
Pulse: PRF-	(1 - 1.65M)Hz		(400 - 10K)Hz
P.W.	(.3 - .99m)sec	Resistive Loads:	(1 - 100K)ohms
Video Generator:	(511 - 1023)lines bandwith - 35MHz		

MEASUREMENT

AC Volts:	(.01 - 1K)V (10 - 16K)Hz	Events:	50nsec
		Noise Meter:	(30M-18G)Hz
DC Volts:	(.01 - 1K)V	Waveform:	(10 - 10M)Hz
Resistance:	(.1 - 9.99M)ohms	Power:	(1m - 10m)W, (500M-18G)Hz
Frequency:	(.1 - 100M)Hz	Servo:	0° - 360° (5-3K)Hz
Time:	(1u - 10) sec	Synchro/Res:	(5-125)V/0° - 360° (400 - 10K)Hz

DIGITAL

I/O	Input Pins	Output Pins	Word Depth	Data Rate	Logic Level
-	32	-	2048	10 MHz	±5 v
-	-	32	1024	10 MHz	±5 v
-	16	-	1024	25 MHz	±.76 v
224	-	-	256	500 kHz	±5 v (TTL)
-	32	32	256	250 kHz	±28 v
-	32	32	286	250 kHz	±30 v
64	-	-	-	-	TTL

POWER SUPPLY

8 Fixed DC Power Supplies

+1.5VDC, 20a
+ 5VDC, 3a,.3a
+ 12VDC, 2a
+ 28VDC, 5a, (2) 10a, 30a

18 Programmable DC Power Supplies

	MAX
(3)±(.1 -35)VDC:	2.5a
(3)±(1 - 35)VDC;	2.5a
(3)±(10 - 16)VDC;	5a
(3)±(3 -7)VDC;	12a
±(22 - 32)VDC;	20a
(2)+(30 - 500)VDC;	3a
(2)+(30 - 500)VDC;	1a
±(.5 - 1)KVDC;	.5a

4 Fixed AC Power Supplies

(2) 6.35 VRMS, 10a, single phase
115 VRMS, 10a, single phase
115 VRMS, 10a, three phase

5 Programmable AC Power Supplies

(0 - 115)VRMS, 10a, single phase, 400Hz)
(5 - 135)VRMS, 1a, single phase, 400Hz)
(2 - 80)VRMS, 10a, single phase, 400Hz)
(89 - 135)VRMS, 5a, three phase, 400Hz)
(0 - 500)VRMS, (NAS), single phase, 400Hz)

COMPUTER AND PERIPHERALS

Computer

Computer Manufacturer:	Varian R6221/L
Word Length:	18 bits
Memory Size:	24K words (R6221), 32K words (R622L)
DMA Channels:	4
Speed:	1.8 sec.

Peripherals

CRT with Keyboard - CRT:	16 lines and 32 char/line
Keyboard:	ASC II Code
Printer:	Yes
Mag Tape:	2 Reel-to-reel units (Ampex ATM13-II)
Disc Memory:	One Fixed, one removable (HP 7906) Data Transfer Rate: 975.5 K Bytes/sec storage: 9.8 M Bytes/Disc
Paper Tape Punch/Reader:	Yes
TTY:	Available as roll up (ASR-35)
Software Development Station:	Yes, off-line

Software Features

Language:	VITAL
OP System	Tape or Disc
Self-Test	Yes
Method of Translation:	Compiler, off-line
LASAR Compatible:	Yes (linkage through VITAL compiler)
OTHER:	Several Digital and Analog Test Languages; FLOVIT, prints TPS diagnostic paths; Supplemental data generator.

IV. AVIONICS-ATE COMPATIBILITY ANALYSIS

A. GENERAL. In Section II the test requirements for the AN/AYK-14 as a WRA and its 21 SRAs were analyzed. In Section III, the ATE test capabilities were analyzed. This section compares the avionics test requirements with the ATE test capabilities to determine the avionics-ATE compatibility.

B. WRA-ATE COMPATIBILITY.

1. In the case of the AYK-14 WRA, there are five WRA configurations included in the SESA, as follows:

- o F/A-18 XN-2A/XN-2
- o LAMPS XN-1A/XN-1
- o AV-8B XN-2D
- o EA-6B XN-4A
- o Firebrand XN-3

Within the five WRA configurations noted above, there are four different chassis configurations of the AYK-14: XN-1, XN-2, XN-3, and XN-4. The letter differences within a chassis configuration indicates an SRA type of quantity difference within the configuration. For example: the F/A-18 and the AV-8B both use the XN-2 chassis configuration (both have a total of ten SRAs). However, the F/A-18 has eight SRA types, while the AV-8B has only seven SRA types.

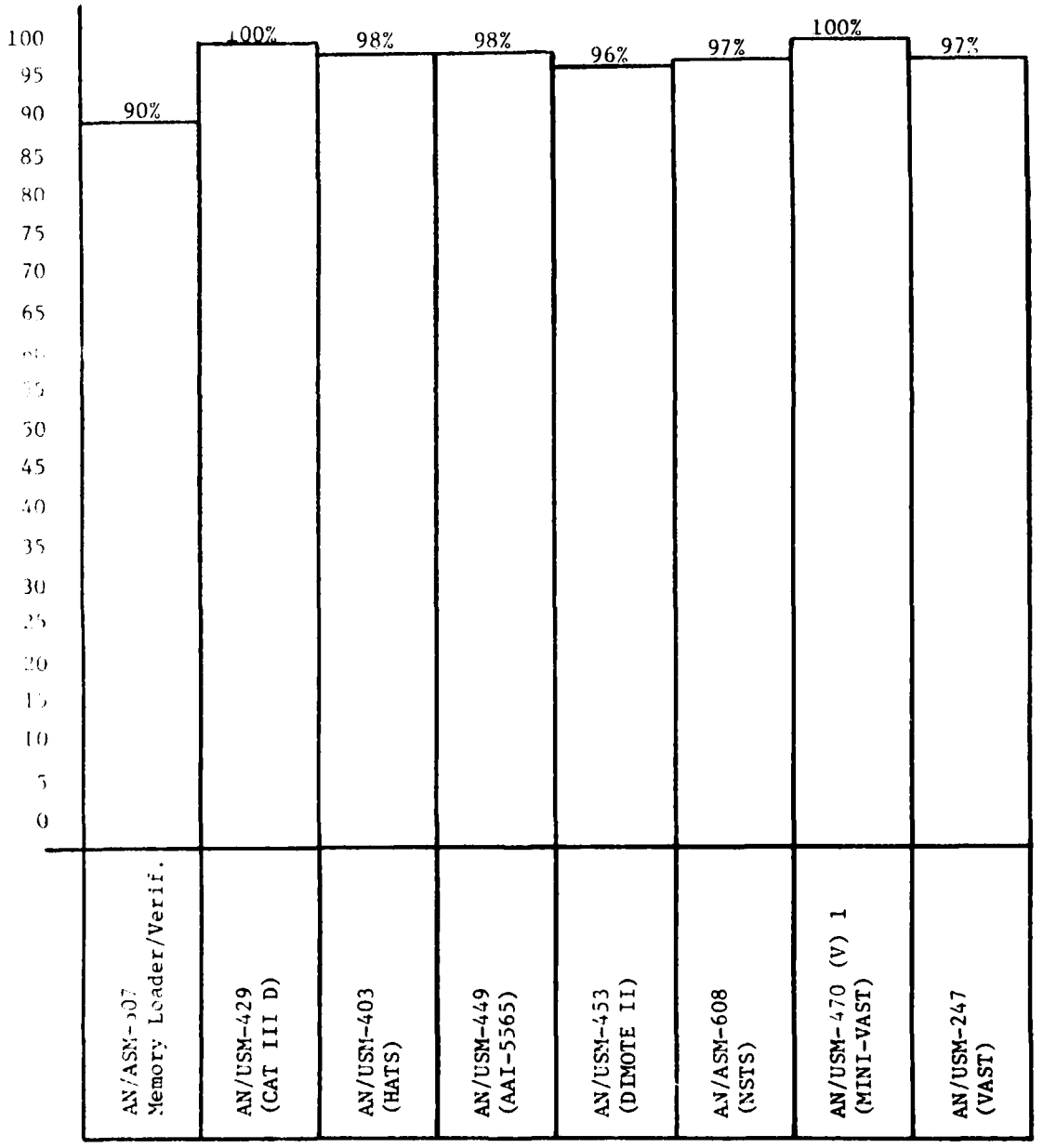
2. The avionics tester compatibility to each tester is determined by comparing the WRA test requirements for the five WRA configurations, with the test capabilities of the eight alternative testers. The AYK-14 WRA tester compatibility percentage (WTC) is presented in Table 24. By virtue of the AYK-14 Internal Fault Diagnostic program, any tester that can load the program into the computer will provide a 90% testing capability. Therefore, the WTC% is computed with a base value of 90%. Both the WRA compatibility factor (B_2) and the WRA tester compatibility percentage (WTC) for the eight testers is indicated below.

Tester	WRA Tester Compatibility % (WTC)	WRA Compatibility Factor (B_2)
AN/ASM-607	90	-
AN/USM-429 (CAT III-D)	100	1.00
AN/USM-403 (HATS)	98	0.81
AN/USM-449 (AAI 5565)	98	0.78
AN/USM-453B (DIMOTE II)	96	0.56
AN/ASM-608 (NSTS)	97	0.68
AN/USM-470(V)1 (MINI-VAST)	100	1.00
AN/USM-247 (VAST)	97	0.71

TABLE 24

AN/AYK-14

WRA TESTER COMPATIBILITY % (WTC)
(Intermediate Level)



The values for the tester SRA and WRA compatibility factors (B_1 and B_2) were derived from the following algorithms, using the summary data from Table 25.

$$B_1 = \frac{\text{No. of SRAs a tester has full capability of testing}}{\text{Total No. of ATE testable SRAs}}$$

$$B_2 = \frac{\left(\frac{\text{No. of SRAs not fully testable}}{3}\right) + \text{No. of SRAs a tester can fully test}}{\text{Total No. of ATE testable SRAs}}$$

$$WTC\% = .9 + 0.1\ (B_2)$$ where: B_2 = WRA tester compatibility factor
WTC% = WRA tester compatibility percentage

3. This avionic-tester compatibility information indicates that all nine testers provide an acceptable capability for testing the AYK-14 as a WRA at the intermediate maintenance level.

C. SRA-ATE COMPATIBILITY.

1. There are a total of 27 SRAs and 6 sub-SRAs available for the various configurations of the AYK-14. The 27 SRAs test requirements are compared with the tester capabilities in Table 25. There are 6 SRAs that will be testable using standard test equipment. This leaves 21 SRAs that are candidates for testing on ATE. Within the 21 there are 6 SRAs that are utilizing large-scale integration (LSI) techniques; the remainder utilize medium-scale integration (MSI) and small-scale integration (SSI) techniques. The SRA testing and repair will be performed at the depot maintenance level and/or factory repair facility. At the bottom of Table 25 are noted the tester compatibility factors (B_1) and the SRA tester capability (STC) percentages of the seven candidate testers. The SRA tester capability (STC) percentage is calculated as follows:

$$\%\ STC = \frac{\text{Total number of SRAs a tester can test}}{\text{Total number of ATE testable SRAs}}$$

Graphically the % STC is presented in Table 26 as follows:

Tester	% STC
AN/USM-429 (CAT III-D)	100
AN/USM-403 (HATS)	91
AN/USM-449 (AAI 5565)	71
AN/USM-453B (DIMOTE II)	48
AN/ASM-608 (NSTS)	81
AN/USM-470(V)1 (MINI-VAST)	100
AN/USM-247 (VAST)	90

2. The AN/ASM-607 is totally unsuitable as a depot-level SRA diagnostic tool, and therefore, was not considered. Only two testers, the AN/USM-429 and the AN/USM-470(V)1, were compatible with the testing requirements of the SRA.

TABLE 25

AYK-14 AVIONIC TESTER

COMPATIBILITY

SRAs	DEPOT-LEVEL MAINTENANCE						
	CAT III D	DAIS	SAI [illegible]	DEPOT II	ASM 608	MINI VAST	VAST
1*General Processor Mod	x	PI, DR	PI, DR	PI, DR	DR, SS	x	DR, SS
2*Processor Support Mod	x	X DR	PI, DR	PI, DR	DR, SS	x	X DR
3 Memory Control Mod	x	x	PI	PI	SS, WD	x	x
4 Discrete Inter Mod	x	x	x	PI, SS	x	x	x
5 Core Memory Mod	x	x	x	XDR	X DR	x	X DR
6 Serial Interf Mod	x	x	x	x	x	x	x
7 Power Conv. Mod-1	x	x	x	x	x	x	x
8 Power Conv. Mod-2	x	x	x	x	x	x	x
9*Protocol Interf Mod	x	X	X DR	DR, SS	X DR	x	X DR
10*Extended Arith. Mod	x	X DR	X DR	DR, SS	X DR	x	X DR
11*Input/Output Pro Mod	x	PI, DR	PI, DR	PI, DR	PI,DR,WD	x	DR, SS
12 NTDS - FAST	x	x	x	x	x	x	x
13 Input Output Mem Mod	x	x	x	XDR	X DR	x	X DR
14 Bus Extended Mod	x	x	x	PI, SS	x	x	x
15 NTDS - SLOW	x	x	x	x	x	x	x
16 NTDS - ASEW	x	x	x	x	x	x	x
17 ENCL/MISC Comp(XX-1)	STE	STE	STE	STE	STE	STE	STE
18 ENCL/MISC Comp(XX-2)	STE	STE	STE	STE	STE	STE	STE
19 ENCL/MISC Comp(XX-3)	STE	STE	STE	STE	STE	STE	STE
20 Fan Assembly	STE	STE	STE	STE	STE	STE	STE
21 RS 232 I/O Mod	x	x	x	PI, SS	x	x	x
22 Semi Cond Mem Mod	x	x	x	XDR	X DR	x	X DR
23 NTDS - Serial	x	x	x	x	x	x	x
24 PIC Proc/SOC Mod	x	X DR	PI, DR	PI, DR	PI,DR,WD	x	X DR
25 Discrete I/O Mod	x	x	x	PI, DR	x	x	x
26 ENCL/MISC Comp(XX-4)	STE	STE	STE	STE	STE	STE	STE
27 ENCL/MISC Comp(XX-5)	STE	STE	STE	STE	STE	STE	STE
SRA Tester Compatibility Factor (B_I)	1.0	0.71	0.67	0.33	0.52	1.0	0.57
SRA Tester Capability % STC	100%	91%	71%	48%	81%	100%	90%

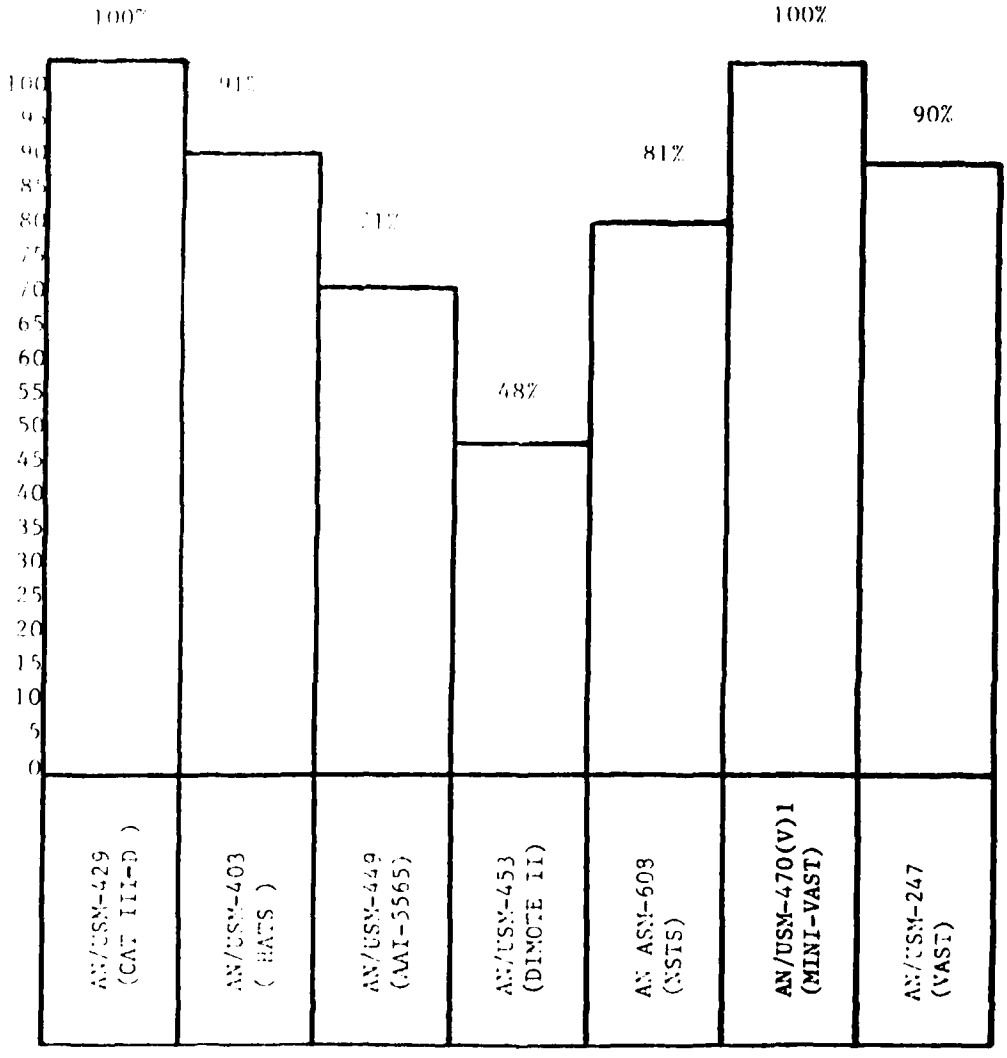
x = Full ATE Capability
X = Partial ATE Capability
STE = Standard Test Equipment
* = LSI SRA

TESTER INCOMPATIBILITY
PI = Pin Input/Output
DR = Data Rate
SS = Station Skew
WD = Word Depth

TABLE 26

AN/AYK-14

SRA TESTER COMPATIBILITY % (STC)
(DEPOT LEVEL)



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V. WORKLOAD ANALYSIS

A. GENERAL

1. The fourth phase of the ground support equipment (GSE) selection process is the GSE workload analysis. The sequences of the GSE loading analysis are presented in Figure 78. The major parts of the analysis are included in the three blocks as follows:

a. Prior workload

b. Projected workload

c. Determining GSE utilization

2. The objective of the analysis is to determine the number of additional GSE required at each intermediate and depot maintenance site to support the AN/AYK-14 computer system. The GSE utilization is defined as the avionic workload normalized to the GSE work capacity and is the summation of: all prior GSE workloads, projected workloads, and the workload due to self-test of the GSE itself.

3. The first phase (A) in the GSE workload analysis is to determine all existing and planned GSE installations and the workloads resulting from prior and planned avionic support other than for the AYK-14. The purpose of this phase is to determine site GSE availability or potential unused GSE capacity that would be utilized in support of the AYK-14. This phase normally would include site surveys (1A) and the determination of site GSE availability (2A). Due to the large number of intermediate (I) level sites (30), the time period of the analysis (1986-1995), and the limited time available for conducting the analysis, it was determined that an analysis based on the Navy's Rails Views Model would provide an adequate basis for determining prior workloads.

4. The second phase (B) of the analysis was to determine the projected GSE workload due to the AYK-14. This phase of the analysis included the following four steps:

1B - Avionic Mission Evaluation

2B - Avionic Reliability and Maintainability Evaluation

3B - Avionic Test Design Evaluation

4B - Development of Avionic Workload per site

a. The mission evaluation step (1B) determines the avionic utilization that directly contributes to the AYK-14 workload due to each of the five weapon systems that will use the AYK-14:

- o F/A-18
- o LAMPS
- o AV-8B
- o EA-6B
- o Firebrand Target

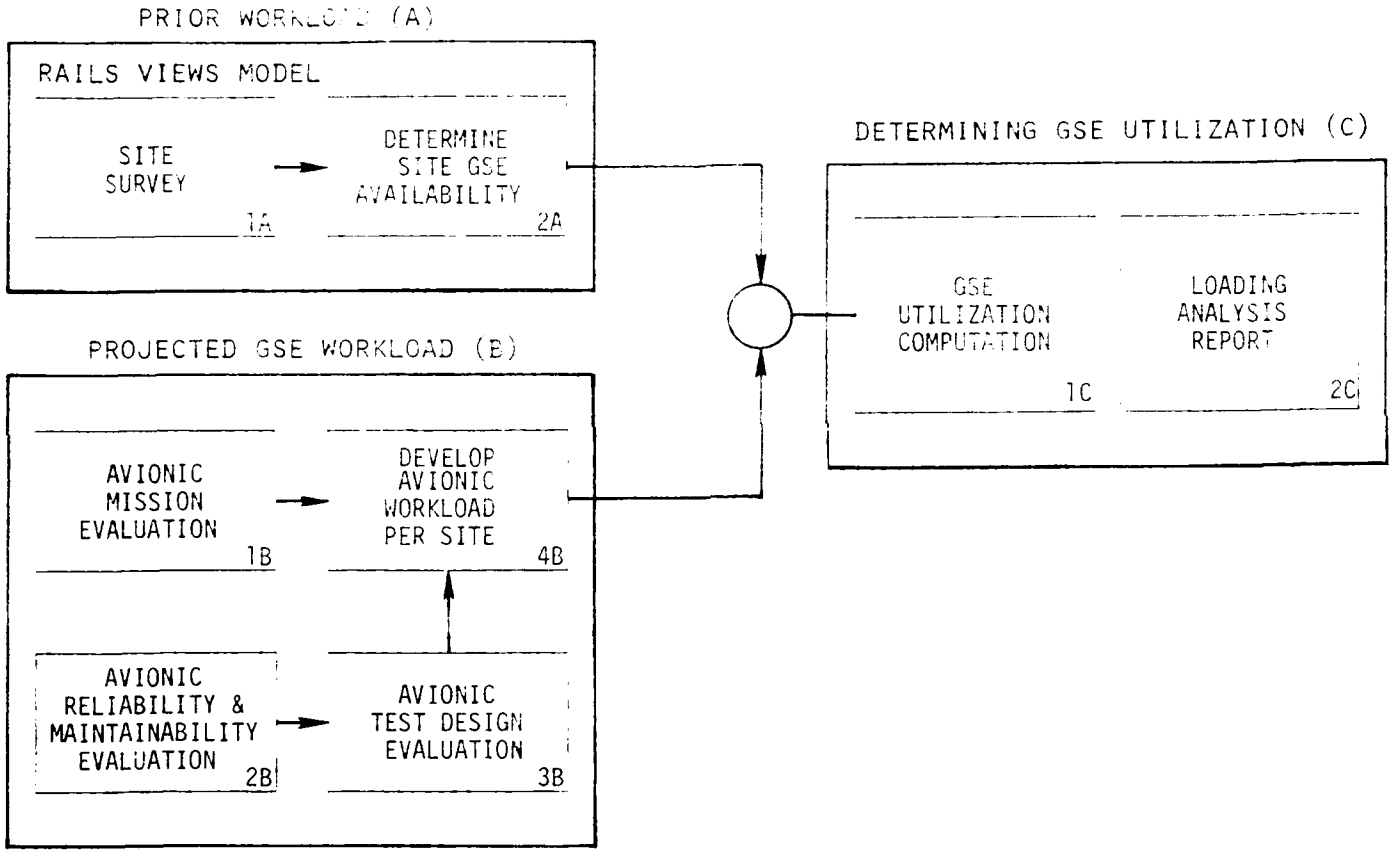

FIGURE 78 - Ground Support Equipment Loading Analysis

b. In step 1B, the following is determined: number of aircraft per site, cumulative flight hours, and the avionic equipment operating hours. Step 2B involves the reliability and maintainability factors of mean-time-between failures (MTBF). In step 3B the mean time to repair (MTTR) is determined for each type of avionics WRA and each SRA. The fourth step (4B) involves the evaluation of avionic test design data obtained from avionic test requirements analysis (TRA), and discussions with the equipment manufacturers (Control Data Corp., Grumman Aircraft Corp., and Texas Instruments Corp.) to determine average test times for WRAs and SRAs.

5. The third phase (C) of the analysis is the computation of GSE utilization (1C), the determination of the required number of additional GSE required per site, and the preparation of the Loading Analysis Report (2C).

6. Each of the three phases of the loading analysis as they apply to the AYK-14 is discussed next.

B. PHASE A, PRIOR WORKLOAD

1. Figure 79 notes the planned automatic test equipment (ATE) to be located at the AYK-14 intermediate- and depot-level sites. Eight GSE systems were included in this analysis:

- o AN/ASM-607 (Memory loader/verifier)
- o AN/USM-429 (CAT III-D)
- o AN/USM-403 (HATS)
- o AN/USM-449 (AA1-5565)
- o AN/USM-453B (DIMOTE II)
- o AN/ASM-608 (NSTS)
- o AN/USM-470(V)1 (MINI-VAST)
- o AN/USM-247 (VAST)

The 30 I-level sites included:

- o NAS North Island
- o NAS Mayport
- o NAS Cubi Point
- o NAS Sigonella
- o NAS Barbers Point
- o NAS Atsugi
- o NAS Guantanamo
- o NAS Diego Garcia
- o NAS Lemoore
- o NAS Cecil Field
- o MCAS Beaufort
- o MCAS El Toro
- o MCAS Iwakuni
- o NAS Patuxent River
- o NAVMISCEN Point Mugu
- o MCAS Yuma
- o NAS Whidbey Island
- o MCAS Cherry Point
- o CV59 through CV70

NOTE: NAS = Naval Air Station. MCAS = Marine Corps Air Station
NAVMISCEN = Naval Missile Center

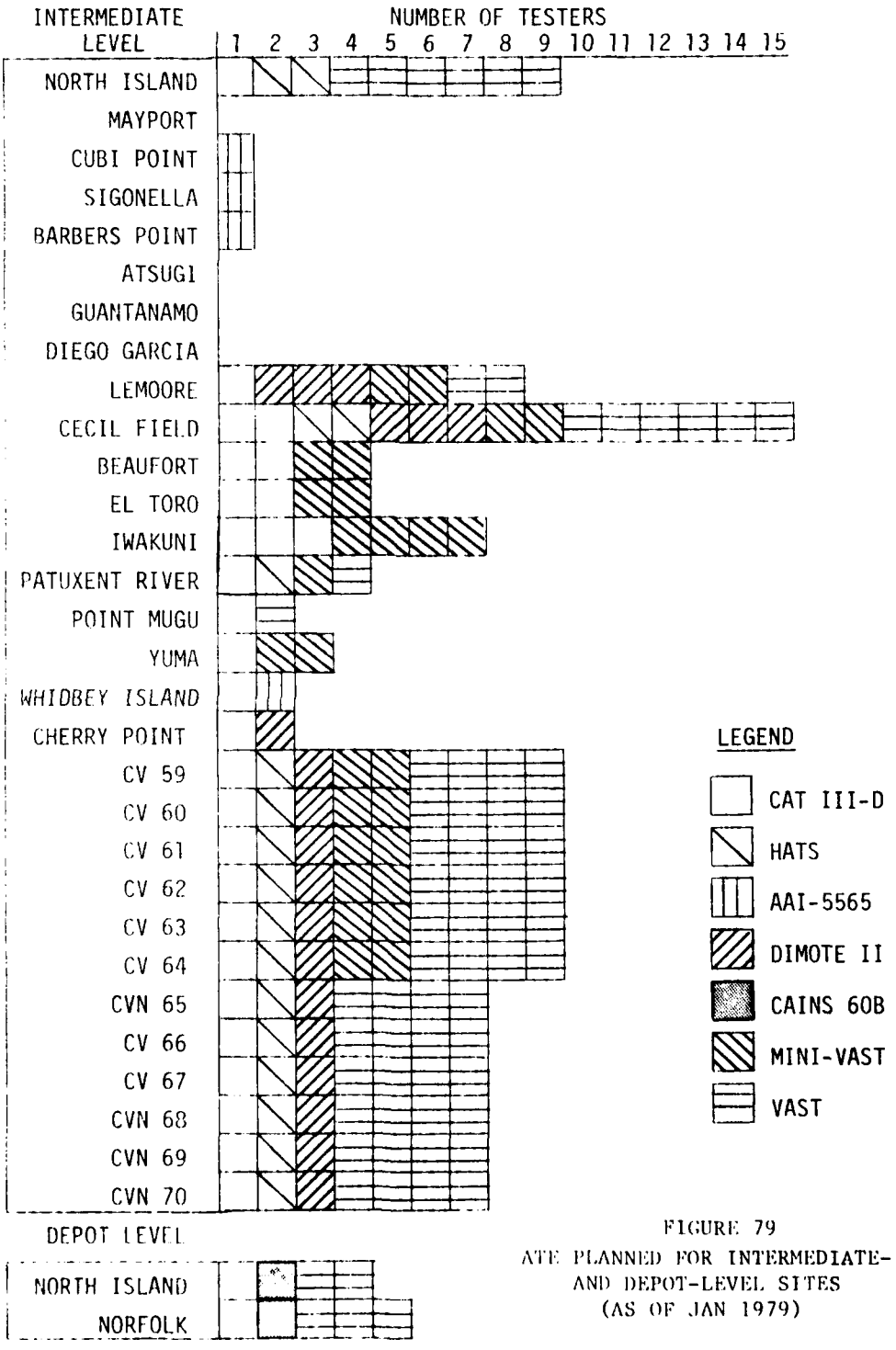

FIGURE 79
ATE PLANNED FOR INTERMEDIATE- AND DEPOT-LEVEL SITES (AS OF JAN 1979)

2. The two depots in support of the AYK-14 are: NAS North Island (NORIS) and NAS Norfolk (NORVA). The Naval Air Rework Facilities (NARF) at NORIS and NORVA perform the depot-level maintenance for the Naval Aviation Maintenance Program. Phase A of the workload analysis would normally have required I-level and D-level site surveys based on the AYK-14's use in the 5 firm programs noted earlier in the report. As can be seen in these figures, the extent of such a site survey would be neither time nor cost effective. To gain an appreciation for the significance of prior GSE loading, the Navy's Rails Views Model data was used instead of directly gathering the data based on individual site surveys. The Rails Views Model is based on prior loadings on the Navy's standard VAST (Versatile Avionics Shop Tester) ATE. This GSE model projects the following prior workload:

- o Shorebased I-Level sites, 72% loaded
- o Carrier I-Levels, 46% loaded
- o Depots, 43% loaded.

a. These prior loading percentages are based on the following maximum GSE availability:

- o Shorebased I- and D-Levels: 8 hours/shift
  2 shifts/day
  21 days/month
- o Carrier I-Level: 8 hours/shift
  2 shifts/day
  30 days/month

Thus, the shorebased shops have a maximum GSE availability of 336 hours/month/GSE. The carriers have an availability of 480 hours/month/GSE.

b. The projected GSE workloads based on the Rails Views Model are:

- o Shorebased I-Levels: 242 hours/month/GSE
- o Carrier I-Levels: 221 hours/month/GSE
- o Depot (D) Levels: 145 hours/month/GSE

C. PHASE B, PROJECTED GSE WORKLOAD. In order to determine the projected workload due to the AYK-14 at each I- and D-level site, four steps are involved:

1B - Avionic Mission Evaluation

2B - Avionic Reliability and Maintainability Evaluation

3B - Avionic Test Design Evaluation

4B - Develop Avionic Workload per site

1. Avionic Mission Evaluation. In Table 27 the average number of aircraft per site for all weapon systems is noted, as well as the estimated cumulative flight hours/month. The average number of aircraft per site for the five firm programs (F-18, LAMPS, EA-6B, AV-8B, and Firebrand) was based on data contained in the individual Weapon Systems Planning Documents (WSPDs). The cumulative flight hours are based on a wartime schedule of 60 hours per month per aircraft. The avionic equipment operating hours per month is based on 1.5 avionic hours per flight hour.

2. Avionic Reliability and Maintainability Evaluation. The second step in Phase B (projected GSE workload) of the workload analysis identifies the mean-time-between-failures (MTBF) for each AYK-14 configuration (WRAs). The specified MTBF and derated MTBF for each of the five configurations of AYK-14's are:

Weapon System	AYK-14 Configuration	Number Per Aircraft	Specified MTBF (Hr)	Derated MTBF (Hr)
F/A-18	XN-2A/XN-2	2	1,615	538
LAMPS	XN-1A/XN-1	2	1,617	539
AV-8B	XN-2D	1	1,200	400
EA-6B	XN-4A	1	1,725	575
Firebrand	XN-3	1	2,500	833

The derated MTBFs are estimated at $(\frac{MTBF}{3})$ because of the excellent BIT/BITE in the AYK-14 configurations. The "normal" derating is $\frac{MTBF}{X}$ where X varies from 5 to 10 depending on the particular equipment.

3. Avionic Test Design Evaluation. Based on discussions with CDC and Navy I-level personnel, the average good (G) AYK-14 (WRA) test time (TT), including hook-up, end-to-end (ETE), and disassembly, averaged 40 minutes.

TABLE 27 - AVIONIC MISSION EVALUATION

SHOREBASED INTERMEDIATE (I) LEVEL MAINTENANCE SITES	AVERAGE NUMBER OF AIRCRAFT WITH 2 AYK-14	AVERAGE NUMBER OF AIRCRAFT WITH 1 AYK-14	AVERAGE NUMBER OF AIRCRAFT TOTAL	FLIGHT HOURS PER MONTH	AVIONIC EQUIPMENT OPERATING HOURS PER MONTH WITH 2 AYK-14	AVIONIC EQUIPMENT OPERATING HOURS PER MONTH WITH 1 AYK-14	AVIONIC EQUIPMENT OPERATING HOURS PER MONTH TOTAL
NORTH ISLAND	52	-	52	3,120	9,360	-	9,360
MAYPORT	65	-	65	3,900	11,700	-	11,700
CUBI POINT	22	-	22	1,320	3,960	-	3,960
SIGONELLA	22	-	22	1,380	3,960	90	4,050
BARBERS POINT	13	-	13	780	2,340	-	2,340
ATSUGI	5	-	5	240	720	-	720
GUANTANAMO	2	-	2	120	360	-	360
DIEGO GARCIA	2	-	2	120	360	-	360
LEMOORE	137	-	137	8,220	24,660	-	24,660
CECIL FIELD	69	-	69	4,140	12,420	-	12,420
BEAUFORT	60	-	60	3,600	10,800	-	10,800
EL TORO	24	64	88	5,280	10,080	-	10,080
IWAKUNI	24	4	28	1,680	4,680	-	4,680
PATUXENT RIVER	18	6	24	1,440	3,780	-	3,780
POINT MUGU	6	83	89	5,340	8,550	-	8,550
YUMA	6	48	54	3,240	5,400	-	5,400
WHIDBEY ISLAND	57	-	57	3,420	5,130	-	5,130
CHERRY POINT	11	84	95	5,700	8,550	-	8,550
CARRIER (I) LEVEL							
CV-59-70: 1-6	12	4	16	5,760	15,120	-	15,120
7-12	4	-	4	1,440	2,160	-	2,160
DEPOT (D) LEVEL							
NORTH ISLAND	0	-	0	0	0	-	0
NORFOLK	0	-	0	0	0	-	0

This was arrived at as follows:

$$TT_{WRA_G} = \text{Hook-up} + \text{E-T-E} + \text{Disassembly}$$

$$10 \text{ Min.} + 20 \text{ Min.} + 10 \text{ Min.}$$

$$= 40 \text{ Min.}$$

The average bad (B) WRA test time is calculated as follows:

$$TT_{WRA_B} = \text{Hook-up} + \frac{\text{E-T-E}}{2} + \text{SRA}_{REP} + \text{E-T-E} + \text{Disassembly}$$

$$10 \text{ Min.} + \frac{20 \text{ Min.}}{2} + 10 \text{ Min.} + 20 \text{ Min.} + 10 \text{ Min.}$$

$$= 60 \text{ Min.}$$

The average test time on ATE for a WRA mix of 20% good WRAs and 80% bad WRAs, as received at the I-level maintenance shop, was calculated as follows:

$$TT_{WRA} = 0.8\ (WRA_{TT_B}) + 0.2\ (WRA_{TT_G})$$

$$= 0.8\ (60 \text{ Min.}) + 0.2\ (40 \text{ Min.})$$

$$= 48 \text{ Min.} + 8 \text{ Min.} = 56 \text{ Min. or rounded to 1 Hr/WRA.}$$

The WRA repairable quantities going to the depot is estimated at 20% of the I-level WRA workload. The SRA repairable quantities going to the depot is calculated based on 1.25 SRAs per WRA failure.

4. Develop Avionic Workloads Per Site. Using the data developed in steps 1B through 3B above, the final step (4B) determines the AYK-14 workloads per site. Starting with the avionic equipment operating hours per month (developed in step 1B), the derated MTBFs (step 2B), and the MTTR and number of SRAs per WRA failure (in step 3B), the WRA site workload WRAs per month is calculated as follows:

$$WL_{WRA} = \frac{\text{Avionic Equipment Hours}}{MTBF_D}$$

The SRA site workload is calculated as follows:

$$WL_{SRA} = WL_{WRA} \times 1.25 \text{ SRAs/WRA failure}$$

The test time (TT) for site loading is calculated for WRAs and SRAs as follows:

$$TT_{WRA} = WL_{WRA} \times MTTR$$

$$TT_{SRA} = WL_{SRA} \times MTTR$$

The results of the workload calculations for each site is presented in Table 28. The sum of the individual I-level WRA workloads is: 288 AYK-14s fail per month at the 30 I-level sites. Based on field experience it is estimated that 20% of the I-level AYK-14s which failed (55 AYK-14s), will require depot (D) level repair. The depot WRA workload is 27 WRAs per month for each site (North Island and Norfolk). Under the AYK-14 maintenance philosophy, no SRAs are to be repaired at the I-level sites, they must be repaired at the D-level. The SRA workload will then be 170 SRAs for each depot. Based upon past experience with similar avionics, the average MTTR for WRAs and SRAs is estimated at 1 hour each, the I-level GSE test time requirement varies from 1 hour per month at Atsugi, to 46 hours per month at Lemoore. Each depot's workload is 197 hours per month.

D. PHASE C, DETERMINING GSE UTILIZATION. The final phase in the loading analysis is to determine the number of additional GSE required at each site. In Table 28 the site test time requirements were developed. The maximum test capacity per test for a 2-shift operation, 8 hours per shift and 21 days per month (shorebased) and 30 days per month (carriers) provides: 336 hours per month per GSE at shorebased sites and 480 hours per month per GSE on carriers. The maximum allowable operating time for GSE is 75% of maximum capacity. The GSE self-testing time is based on 5% of avionic testing time (TT). Thus, the available GSE testing time per site is calculated as follows:

For shorebased I-Level sites:

TT_{GSE_L} = #GSE/site (Maximum GSE Loading - Rails Views prior loading)

= #GSE/site (336 hours/month/GSE X 75% - 336 hours/month/GSE X 72%)

For carrier I-Level sites:

TT_{GSE_C} = #GSE/site (480 hours/month/GSE X 75% - 480 hours/month/GSE X 46%)

For Depot (D) Level sites:

TT_{GSE_D} = #GSE/site (336 hours/month/GSE X 75% - 336 hours/month/GSE X 43%)

The GSE utilization (GSEU) per site is calculated as follows:

U_{GSE} = Test Time available at site - Avionic Test Time required (TT_R) - GSE self-test (TT_{ST})

$= TT_{GSE} - TT_R - TT_{ST}$

TABLE 28 - WRA AND SRA SITE LOADING

SHOREBASED INTERMEDIAT (I) LEVEL MAINTENANCE SITES	AVIONIC EQUIPMENT OPERATING HOURS PER MONTH AIRCRAFT WITH 2 AYK-14	1 AYK-14	SITE WORKLOAD WRAs PER MONTH (WLWRA) AIRCRAFT WITH 2 AYK-14	1 AYK-14	TOTAL	SRAs PER MONTH TO DEPOT (WLSRA)	SITE WORKLOAD TEST TIME PER MONTH WRA	SRA	TOTAL AVIONIC TEST TIME REQUIRED PER MONTH
NORTH ISLAND	9,360	-	17	-	17	22	17	0	17
MAYPORT	11,700	-	22	-	22	27	22	0	22
CUBI POINT	3,960	-	7	-	7	9	7	0	7
SIGONELLA	3,960	90	7	-	7	9	7	0	7
BARBERS POINT	2,340	-	4	-	4	5	4	0	4
ATSUGI	720	-	1	-	1	1	1	0	1
GUANTANAMO	360	-	1	-	1	1	1	0	1
DIEGO GARCIA	360	-	1	-	1	1	1	0	1
LEMOORE	24,660	-	46	-	46	56	46	0	46
CECIL FIELD	12,420	-	23	-	23	29	23	0	23
BEAUFORT	10,800	-	20	-	20	25	20	0	20
EL TORO	4,320	5,760	8	14	22	28	22	0	22
IWAKUNI	4,320	360	8	1	9	11	9	0	9
PATUXENT RIVER	2,520	1,260	5	2	7	9	7	0	7
POINT MUGU	1,080	7,470	2	9	11	14	11	0	11
YUMA	1,080	4,320	2	11	13	16	13	0	13
WHIDBEY ISLAND	5,130	-	9	-	9	11	9	0	9
CHERRY POINT	990	7,560	2	19	21	26	21	0	21
CARRIER (I) LEVEL									
CV 59-70: 1 - 6	12,960	2,160	24	4	28	35	28	0	28
7 - 12	2,160	-	4	-	4	5	4	0	4
DEPOT (D) LEVEL									
NORTH ISLAND	0	-	27	-	27	0	27	170	197
NORFOLK	0	-	27	-	27	0	27	170	197

The number of GSE required for each of the 7 different GSEs planned for the 30 AYK-14 I-level sites and 2 depots are included in Tables 29 through 35. Based on the planned GSE, the required GSE for AYK-14 support at I- and D-level sites are:

GSE Type	I-Level	D-Level
o AN/ASM-607	30	*
o AN/USM-429 (CAT III-D)	7	2
o AN/USM-403 (HATS)	15	2
o AN/USM-449 (AAI 5565)	26	2
o AN/USM-453 (DIMOTE II)	16	2
o AN/ASM-608 (NSTS)	30	2
o AN/USM-470(V)1 (MINI-VAST)	17	2
o AN/USM-247 (VAST)	13	0

* Not suitable for D-level SRA diagnostics.

The details of the GSE utilization is contained in Tables 29 through 35; this data presents the current and projected testers as of January 1979.

TABLE 29 - AN/USM-429 (CAT III-D) GSE UTILIZATION

SHOREBASED INTERMEDIATE (I) LEVEL MAINTENANCE SITES	ANALYSIS ITEM: AYK-14 WORKLOAD PER MONTH (TT_A) Hr/Mo	GSE SELF-TEST TIME REQUIRED (TT_{ST}) Hr/Mo	NO. OF GSE ATE AT SITE	GSE TEST TIME AVAILABLE AT SITE (TT_{GSE}) Hr/Mo	GSE UTILIZATION PER SITE: EXCESS OR REQUIRED TEST TIME (U_{GSE}) Hr/Mo	NO. OF ADDITIONAL GSE REQUIRED AT SITE
NORTH ISLAND	17	1	1	10	(8)	0
MAYPORT	22	1	0	0	(23)	1
CUBI POINT	7	0	0	0	(7)	1
SIGONELLA	7	0	0	0	(7)	1
BARBERS POINT	4	0	0	0	(4)	1
ATSUGI	1	0	0	0	(1)	1
GUANTANAMO	1	0	0	0	(1)	1
DIEGO GARCIA	1	0	0	0	(1)	1
LEMOORE	46	2	1	10	(38)	0
CECIL FIELD	23	1	2	20	(4)	0
BEAUFORT	20	1	2	20	(1)	0
EL TORO	22	1	2	20	(3)	0
IWAKUNI	9	1	3	30	20	0
PATUXENT RIVER	7	0	1	10	3	0
POINT MUGU	11	1	1	0	(12)	0
YUMA	13	1	1	0	(14)	0
WHIDBEY ISLAND	9	1	1	10	0	0
CHERRY POINT	21	1	1	10	(12)	0
CARRIER (I) LEVEL (CV 59-70)						
1 - 6	28	1	6	834	805	0
7 - 12	4	0	6	834	830	0
DEPOT (D) LEVEL						
NORTH ISLAND	209	11	1	107	113	1
NORFOLK	209	11	1	107	(113)	1

TOTAL GSE REQUIRED AT: I-LEVEL 7 ; D-LEVEL 2 .

TABLE 30 - AN/USM-403 (HATS) GSE UTILIZATION

SHOREBASED INTERMEDIATE (I) LEVEL MAINTENANCE SITES	ANALYSIS ITEM: AYK-14 WORKLOAD PER MONTH (TT_A) Hr/Mo	GSE SELF-TEST TIME REQUIRED (TT_{ST}) Hr/Mo	NO. OF GSE ATE AT SITE	GSE TEST TIME AVAILABLE AT SITE (TT_{GSE}) Hr/Mo	GSE UTILIZATION PER SITE: EXCESS OR REQUIRED TEST TIME (U_{GSE}) Hr/Mo	NO. OF ADDITIONAL GSE REQUIRED AT SITE
NORTH ISLAND	17	1	2	20	(2)	0
MAYPORT	22	1	0	0	(23)	1
CUBI POINT	7	0	0	0	(7)	1
SIGONELLA	7	0	0	0	(7)	1
BARBERS POINT	4	0	0	0	(4)	1
ATSUGI	1	0	0	0	(1)	1
GUANTANAMO	1	0	0	0	(1)	1
DIEGO GARCIA	1	0	0	0	(1)	1
LEMOORE	46	2	0	0	(48)	1
CECIL FIELD	23	1	2	20	(4)	0
BEAUFORT	20	1	0	0	(21)	1
EL TORO	22	1	0	0	(23)	1
IWAKUNI	9	1	0	0	(10)	1
PATUXENT RIVER	7	0	1	10	(3)	0
POINT MUGU	11	1	0	0	(12)	1
YUMA	13	1	0	0	(14)	1
WHIDBEY ISLAND	9	1	0	0	(10)	1
CHERRY POINT	21	1	0	0	(22)	1
CARRIER (I) LEVEL (CV 59-70)						
1 - 6	28	1	6	834	805	0
7 - 12	4	0	6	834	830	0
DEPOT (D) LEVEL						
NORTH ISLAND	197	10	0	0	(207)	1
NORFOLK	197	10	0	0	(207)	1

TOTAL GSE REQUIRED AT: I-LEVEL 15 ; D-LEVEL 2 .

TABLE 31 - AN/USM-449 (AAI-5565) GSE UTILIZATION

SHOREBASED INTERMEDIATE (I) LEVEL MAINTENANCE SITES	ANALYSIS ITEM: AYK-14 WORKLOAD PER MONTH (TT_A) Hr/Mo	GSE SELF-TEST TIME REQUIRED (TT_{ST}) Hr/Mo	NO. OF GSE ATE AT SITE	GSE TEST TIME AVAILABLE AT SITE (TT_{GSE}) Hr/Mo	GSE UTILIZATION PER SITE: EXCESS OR REQUIRED TEST TIME (U_{GSE}) Hr/Mo	NO. OF ADDITIONAL GSE REQUIRED AT SITE
NORTH ISLAND	17	1	0	0	(18)	1
MAYPORT						
CUBI POINT	7	0	1	10	3	0
SIGONELLA	7	0	1	10	3	0
BARBERS POINT	4	0	1	10	6	0
ATSUGI	1	0	0	0	(1)	1
GUANTANAMO	1	0	0	0	(1)	1
DIEGO GARCIA	1	0	0	0	(1)	1
LEMOORE	46	2	0	0	(48)	1
CECIL FIELD	23	1	0	0	(24)	1
BEAUFORT	20	1	0	0	(21)	1
EL TORO	22	1	0	0	(23)	1
IWAKUNI	9	1	0	0	(10)	1
PATUXENT RIVER	7	0	0	0	(7)	1
POINT MUGU	11	1	0	0	(12)	1
YUMA	13	1	0	0	(14)	1
WHIDBEY ISLAND	9	1	1	10	0	0
CHERRY POINT	21	1	0	0	(22)	1
CARRIER (I) LEVEL (CV 59-70)						
1 - 6	28	1	0	0	(29)	6
7 - 12	4	0	0	0	(4)	6
DEPOT (D) LEVEL						
NORTH ISLAND	197	10	0	0	(207)	1
NORFOLK	197	10	0	0	(207)	1

TOTAL GSE REQUIRED AT: I-LEVEL 25 ; D-LEVEL 2

TABLE 32 - AN/USM-453B(DIMOTE II) GSE UTILIZATION

SHOREBASED INTERMEDIATE (I) LEVEL MAINTENANCE SITES	ANALYSIS ITEM: AYK-14 WORKLOAD PER MONTH (TT_A) Hr/Mo	GSE SELF-TEST TIME REQUIRED (TT_{ST}) Hr/Mo	NO. OF GSE ATE AT SITE	GSE TEST TIME AVAILABLE AT SITE (TT_{GSE}) Hr/Mo	GSE UTILIZATION PER SITE: EXCESS OR REQUIRED TEST TIME (U_{GSE}) Hr/Mo	NO. OF ADDITIONAL GSE REQUIRED AT SITE
NORTH ISLAND	17	1	0	0	(18)	1
MAYPORT	22	1	0	0	(23)	1
CUBI POINT	7	0	0	0	(7)	1
SIGONELLA	7	0	0	0	(7)	1
BARBERS POINT	4	0	0	0	(4)	1
ATSUGI	1	0	0	0	(1)	1
GUANTANAMO	1	0	0	0	(1)	1
DIEGO GARCIA	1	0	0	0	(1)	1
LEMOORE	46	2	3	30	(18)	0
CECIL FIELD	23	1	3	30	6	0
BEAUFORT	20	1	0	0	(21)	1
EL TORO	22	1	0	0	(23)	1
IWAKUNI	9	1	0	0	(10)	1
PATUXENT RIVER	7	0	0	0	(7)	1
POINT MUGU	11	1	0	0	(12)	1
YUMA	13	1	0	0	(14)	1
WHIDBEY ISLAND	9	1	0	0	(10)	1
CHERRY POINT	21	1	0	0	(12)	1
CARRIER (I) LEVEL (CV 59-70)						
1 - 6	28	1	6	834	805	0
7 - 12	4	0	6	834	830	0
DEPOT (D) LEVEL						
NORTH ISLAND	197	10	0	0	207	1
NORFOLK	197	10	0	0	207	1

TOTAL GSE REQUIRED AT: I-LEVEL 16 ; D-LEVEL 2 .

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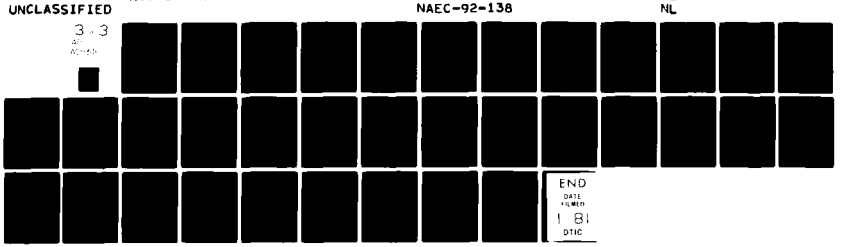
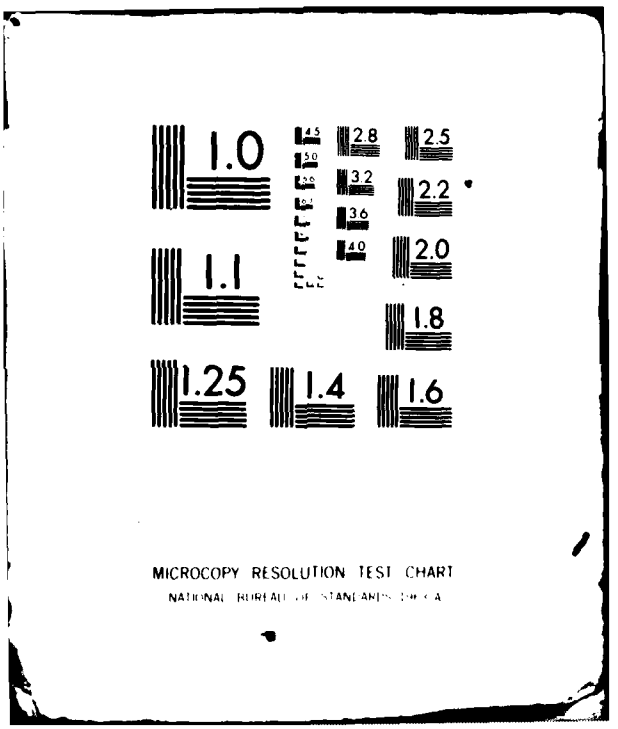
UNCLASSIFIED NAEC-92-138 NL

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1.1
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4.5
5.0
5.6
6.3
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

TABLE 33 - AN/ASM-608 (NSTS) GSE UTILIZATION

SHOREBASED INTERMEDIATE (I) LEVEL MAINTENANCE SITES	ANALYSIS ITEM					
	AYK-14 WORKLOAD PER MONTH (TT_A) Hr/Mo	GSE SELF-TEST TIME REQUIRED (TT_{ST}) Hr/Mo	NO. OF GSE ATE AT SITE	GSE TEST TIME AVAILABLE AT SITE (TT_{GSE}) Hr/Mo	GSE UTILIZATION PER SITE: EXCESS OR REQUIRED TEST TIME (U_{GSE}) Hr/Mo	NO. OF ADDITIONAL GSE REQUIRED AT SITE
NORTH ISLAND	17	1	1	10	(18)	1
MAYPORT	22	1	0	0	(23)	1
CUBI POINT	7	0	0	0	(7)	1
SIGONELLA	7	0	0	0	(7)	1
BARBERS POINT	4	0	0	0	(4)	1
ATSUGI	1	0	0	0	(1)	1
GUANTANAMO	1	0	0	0	(1)	1
DIEGO GARCIA	1	0	0	0	(1)	1
LEMOORE	46	2	0	0	48	1
CECIL FIELD	23	1	0	0	24	1
BEAUFORT	20	1	0	0	21	1
EL TORO	22	1	0	0	23	1
IWAKUNI	9	1	0	0	10	1
PATUXENT RIVER	7	0	0	0	7	1
POINT MUGU	11	0	0	0	12	1
YUMA	13	1	0	0	14	1
WHIDBEY ISLAND	9	1	0	0	10	1
CHERRY POINT	21	1	0	0	22	1
CARRIER (I) LEVEL (CV 59-70)						
1 - 6	28	1	0	0	29	6
7 - 12	4	0	0	0	29	6
DEPOT (D) LEVEL						
NORTH ISLAND	197	10	1	107	100	1
NORFOLK	197	10	1	107	100	1

TOTAL GSE REQUIRED AT: I-LEVEL 30 ; D-LEVEL 2 .

TABLE 34 - AN/USM -470(V)1 (MINI-VAST) GSE UTILIZATION

SHOREBASED INTERMEDIATE (I) LEVEL MAINTENANCE SITES	ANALYSIS ITEM: AYK-14 WORKLOAD PER MONTH (TT_A) Hr/Mo	GSE SELF-TEST TIME REQUIRED (TT_{ST}) Hr/Mo	NO. OF GSE ATE AT SITE	GSE TEST TIME AVAILABLE AT SITE (TT_{GSE}) Hr/Mo	GSE UTILIZATION PER SITE: EXCESS OR REQUIRED TEST TIME (U_{GSE}) Hr/Mo	NO. OF ADDITIONAL GSE REQUIRED AT SITE
NORTH ISLAND	17	1	0	0	(18)	1
MAYPORT	22	1	0	0	(23)	1
CUBI POINT	7	0	0	0	(7)	1
SIGONELLA	7	0	0	0	(7)	1
BARBERS POINT	4	0	0	0	(4)	1
ATSUGI	1	0	0	0	(1)	1
GUANTANAMO	1	0	0	0	(1)	1
DIEGO GARCIA	1	0	0	0	(1)	1
LEMOORE	46	2	2	20	(28)	0
CECIL FIELD	23	1	2	20	(4)	0
BEAUFORT	20	1	2	20	(1)	0
EL TORO	22	1	2	20	(3)	0
IWAKUNI	9	1	4	40	(30)	0
PATUXENT RIVER	7	0	1	10	3	0
POINT MUGU	11	1	0	0	(12)	1
YUMA	13	1	2	20	6	0
WHIDBEY ISLAND	9	1	0	0	(10)	1
CHERRY POINT	21	1	0	0	(22)	1
CARRIER (I) LEVEL (CV 59-70)						
1 - 6	28	1	12	1,668	1,639	0
7 - 12	4	0	0	0	(4)	6
DEPOT (D) LEVEL						
NORTH ISLAND	197	11	1	107	100	1
NORFOLK	197	11	0	0	100	1

TOTAL GSE REQUIRED AT: I-LEVEL 17 ; D-LEVEL 2 .

TABLE 35 - AN/USM-247 (VAST) GSE UTILIZATION

SHOREBASED INTERMEDIATE (I) LEVEL MAINTENANCE SITES	ANALYSIS ITEM					
	AYK-14 WORKLOAD PER MONTH (TT_A) Hr/Mo	GSE SELF-TEST TIME REQUIRED (TT_{ST}) Hr/Mo	NO. OF GSE ATE AT SITE	GSE TEST TIME AVAILABLE AT SITE (TT_{GSE}) Hr/Mo	GSE UTILIZATION PER SITE: EXCESS OR REQUIRED TEST TIME (U_{GSE}) Hr/Mo	NO. OF ADDITIONAL GSE REQUIRED AT SITE
NORTH ISLAND	17	1	6	60	42	0
MAYPORT	22	1	0	0	(23)	1
CUBI POINT	7	0	0	0	(7)	1
SIGONELLA	7	0	0	0	(7)	1
BARBERS POINT	4	0	0	0	(4)	1
ATSUGI	1	0	0	0	(1)	1
GUANTANAMO	1	0	0	0	(1)	1
DIEGO GARCIA	1	0	0	0	(1)	1
LEMOORE		2	2	20	(28)	0
CECIL FIELD	23	1	6	60	36	0
BEAUFORT	20	1	0	0	(22)	1
EL TORO	22	1	0	0	(23)	1
IWAKUNI	9	1	0	0	(10)	1
PATUXENT RIVER	7	0	1	10	3	0
POINT MUGU	11	1	1	10	(2)	0
YUMA	13	1	0	0	(14)/6	1
WHIDBEY ISLAND	9	1	0	0	(10)	1
CHERRY POINT	21	1	0	0	(22)	1
CARRIER (I) LEVEL (CV 59-70)						
1 - 6	28	1	12	1,668	1,639	0
7 - 12	4	0	0	1,668	1,664	0
DEPOT (D) LEVEL						
NORTH ISLAND	197	10	2	214	7	0
NORFOLK	197	10	3	321	114	0

TOTAL GSE REQUIRED AT: I-LEVEL 13 ; D-LEVEL 0 .

VI. LIFE CYCLE COST AND IMPACT ANALYSIS

A. GENERAL. The GSE Life Cycle Cost and Impact Analysis provides the methodology for calculating the elemental costs associated with using each of the eight alternative testers in support of the AYK-14. The resulting cost elements are then used as inputs to the GSE selection process and provide a data base of information for future GSE decisions in AYK-14 logistic support. The cost element structure includes three major cost categories:

- o Nonrecurring costs
- o Recurring costs
- o Sustaining costs

1. NONRECURRING COSTS. The nonrecurring life cycle costs include four cost subdivisions:

- o Modifications to support equipment costs
- o Integrated logistics support costs
- o Test program set costs
- o Government-furnished factors costs

2. RECURRING COSTS. Within the recurring costs are those initial costs required to set up the intermediate and depot sites in the following cost element areas:

- o Support Equipment (SE) Hardware Costs
- o Support Equipment (SE) Installation Costs
- o Support Equipment (SE) Technical Publications Costs
- o Support Equipment (SE) Modification Costs
- o Special Support Equipment Costs
- o Initial Support Equipment Spares Costs
- o Incremental Prime Equipment Site Spares Costs
- o Test Program Set (TPS) Costs
- o Maintenance Assist Modules Costs
- o Interconnecting Device (ID) Initial Spares Costs

3. SUSTAINING COSTS. The sustaining cost time period for their calculations was 10 years. The individual cost elements under sustaining costs are calculated using the baseline test equipment (VAST) for which historical data is available. This baseline data is then derated to the appropriate value for a given tester through the use of a relative complexity factor (alpha). The following cost elements are included in sustaining costs:

- o Depot Rework Costs
- o Depot Component Repair Costs
- o Packaging, Handling, Storage, and Transportation Costs
- o Depot Calibration Costs
- o Intermediate/Depot Repair Costs
- o Intermediate-Level Calibration Costs
- o Training Costs
- o Replenishment Spares and Repair Parts Costs
- o Technical Publications Revision Costs
- o In-Service Engineering Costs

B. COST MODEL ELEMENT ALGORITHMS

1. The following cost model algorithms were used in determining the anticipated life cycle costs of choosing a particular tester to accomplish repair of the AYK-14 avionics (WRA) at the intermediate maintenance level and SRAs at the depot maintenance level.

2. Many of the individual cost model calculations make use of a tester relative complexity factor (alpha) as a multiplier. The complexity factor is computed as a percentage of the bascline tester, which is VAST. In the area of TPS nonrecurring costs, calculations involved the use of a relative compatibility factor (Beta) as a multiplier. The compatibility factor for each tester was developed in Section IV.

a. Ground Support Equipment Complexity Factor

Tester	No. Racks of Equipment	Complexity Factor α
VAST	14	1.00
MINI-VAST	6	0.43
AAI-5565	6	0.43
ASM-608 (NSTS)	3*	0.21
CAT III-D	3	0.21
HATS	2-1/2	0.18
DIMOTE II	1-1/2	0.11
ASM-607 (MLV)	1/4	0.02

*Electronic

b. Test Program Set Compatibility Factor (B)

Tester	SRA/WRA Compatibility Factor SRA (B1)	WRA (B2)
CAT III-D	1.00	1.00
MINI-VAST	1.00	1.00
HATS	0.71	0.81
AAI-5565	0.67	0.78
VAST	0.57	0.71
ASM-608 (NSTS)	0.52	0.68
DIMOTE II	0.33	0.56

$$B_1 = \frac{\text{\# of SRAs a tester has full capability of testing}}{\text{Total \# of ATE testable SRAs}}$$

$$B_2 = \frac{\left(\frac{\text{\# SRAs not fully testable}}{3}\right) + (\text{\# SRAs testable})}{\text{Total \# of ATE testable SRAs}}$$

3. NONRECURRING COST ALGORITHMS

a. Modification To Support Equipment Costs. These are development costs of modifications to the tester to increase tester-avionics compatibility. In the case of the AYK-14 all additional required testing compatibility would be included in the interconnecting devices for both WRA and SRA testing. Therefore, no tester modification costs are required.

b. Integrated Logistic Support Costs. Under this cost element are two ILS costs: New inventory testers and TPS.

(1) Tester ILS Costs: All testers considered as candidates for AYK-14 support are NAVAIR inventory testers. Accordingly, no test equipment ILS costs have been charged.

(2) Software ILS Costs: This element of cost includes four cost items. The algorithms are as follows:

- Test Program Set ILS = $0.40 \times ID_{NR\text{-}AYK\text{-}14}$
- Provisioning Data (PD) Costs = \$10K Constant
- Training (T) Costs = $0.40 \times ID_{NR\text{-}AYK\text{-}14} \times (A)$
- Technical Manuals (TM) Costs = $0.22 \times ID_{NR\text{-}AYK\text{-}14}$

Software ILS Costs =
TPS-ILS Costs + PD Costs + T Costs + TM Costs

c. Test Program Set Costs. This cost element includes the following:

- Test Program/Test Program Instruction (TP/TPI)
- Interconnecting Devices (ID) Costs
- Program Development Data (PDD) Costs

(1) The combination of TP/TPI and ID costs make up the TPS. The TPS costs are based on estimated costs for the S-3A Weapon System. Each of the SRAs for the AYK-14 was calculated individually as to circuit type and complexity to determine SRA TPS costs. The digital SRA cost algorithms are based on the use of computer simulation (D-LASAR) and follows a straight line relationship between circuit complexity and TPS costs, and follows the equation:

$Y=MX$

Y = TPS Nonrecurring Cost ($K)

M = Slope (Depends on IC complexity)

X = number of SRA active components

Therefore:

$TPS_{NR-COST\ MSI-SSI\ (\$K)} = 0.365 \times \#Active\ Components$

$TPS_{NR-COST\ LSI-MSI\ (\$K)} = 0.402 \times \#Active\ Components$

For the analog TPS_{NR} the algorithm is:

$$TPS_{NR(\$K)} = 1.5 \times (\#Active\ Components)^{1.338}$$

Once the TPS costs for SRAs have been determined, then the ATE TPS cost for WRAs can be determined as follows:

$$TPS_{NR-WRA} = \frac{0.75}{B_2} \sum_{i=1}^{N} TPS_{NR-SRA}$$

Where:

B_2 = Tester - WRA compatibility factor (See Section IV)

$$TPS_{NR-WRA} = \frac{0.75\ (\$1,280K)}{B_2}$$

$$= \frac{\$960K(\text{one WRA})}{B_2}$$

And,

$$TPS_{NR-WRA} = TP_{NR-WRA} + TPI_{NR-WRA} + ID_{NR-WRA}$$

On the Average:

$$TP_{NR-WRA} = 60\%\ TPS_{NR-WRA}$$

$$TPI_{NR-WRA} = 20\%\ TPS_{NR-WRA}$$

$$ID_{NR-WRA} = 20\%\ TPS_{NR-WRA}$$

For the CAT III-D TPS_{NR-WRA} costs:

$$TPS_{NR-7\ WRA} = TPS_{NR-1\ WRA} + 6\ (10\%\ TPS_{NR-WRA})$$

$$= \$960K + 6\ (0.1 \times \$960K)$$

$$= \$960K + \$576K$$

$$= \$1536K\ (7\ WRA\ Configuration)$$

$$TP_{NR-7\ WRA's} = 60\%\ TPS_{NR-7\ WRA} = 0.6 \times \$1,536K = \$922K$$

$$TPI_{NR-7\ WRA's} = 20\%\ TPS_{NR-7\ WRA's} = 0.2 \times \$1,536K = \$307K$$

$$ID_{NR-7\ WRA's} = 20\%\ TPS_{NR-7\ WRA's} = 0.2 \times \$1,536K = \$307K$$

(2) ID Reliability and Maintainability Costs:

$$ID_{R\&M}\ Costs = 0.05 \times ID_{NR-AYK-14}$$

(3) Program Development Data (PDD): This cost element includes that effort required to develop all TPS data needed to facilitate development of the TPSs during a phase-controlled program by the contractors under direction of the Navy. Analysis indicates that PDD costs are a function of TPS nonrecurring costs:

$$PDD_{NR-COSTS} = \frac{TPS_{NR-COSTS}}{5}$$

Therefore, the total WRA TPS development costs are:

$$TPS_{NR} = TPS_{NR-WRA} + PDD + ID_{R\&M}$$

d. Government-Furnished Factors (GFF) - This cost element includes four items:

- o Support Equipment Costs
- o Test Requirement Documents Costs
- o Unit-Under-Test Set Costs
- o UUT Set Contractor Maintenance/Repair Costs

(1) Support Equipment Costs: This cost element includes the costs of SE hardware required for TPS development, SE installation, technical publications, and any hardware modifications required. The algorithms developed to calculate their costs are based on a ratio comparison to existing support equipment program costs as follows:

- SE Hardware = $10\%(SE_{UC} \times \#SE)$ + Installation Cost (IC)

  $= .1 \times SE_{UC} + IC$

- Support Equipment Spares (SES) = $10\%(10\%/yr \times SE_{UC} \times \#SE) \times \#TPS_{yr}$

  $= .02 \times SE_{UC}$

- $SES_{CMS} = 10\% \times \#TPS_{yr} \times SES_{UC}$

  $= .2 \times SES_{UC}$

- $SSE = 10\% \ (125K \times (\alpha) \times \#SE) \times \#TPS_{yr}$

  $= \$25K \times (\alpha)$

- $SE_{CMS} = 10\%/yr \times \#TPS_{yr} \times SE \times SE_{UC}$

  $= 0.2 \times SE_{UC}$ *$\#TPS_{yr} = 2_{yr}$

  $\#SE = 1$

$$SE\ Costs = SE_H + SES + SES_{CMS} + SE_{CMS} + SSE$$

$$= (0.10 + 0.02 + 0.20 + 0.20)\ SE_{UC} + (\$25K \times (\alpha)) + IC$$

$$= (0.52 \times SE_{UC}) + (\$25K \times (\alpha)) + IC$$

(2) Test Requirements Documents (TRDs): This element includes the effort required to perform a Test Requirement Analysis (TRA) for each WRA/SRA to be supported by the testers under evaluation, and the preparation of the TRD. The algorithm for TRD/TRA costs is:

$$TRD_{NR} = \frac{TPS_{NR\text{-}COSTS}}{4}$$

TRD costs for WRA at the intermediate level and SRA TRDs for the depot level were not included in the LCC based on NAVAIRSYSCOM direction.

(3) Unit-Under-Test (UUT) Costs: This element includes the costs of avionic WRAs/SRAs required during the TPS development process. This cost is a function of the prime equipment WRA cost and SRA costs.

$$UUT_{NR} = 50\% \sum_{L=1}^{N\ Systems} WRA_{UC} \text{ or } SRA_{UC} \quad \text{Where UC = Unit Cost}$$

$WRA_{UC} = \$36.6K\ each_{(AVG)}$ $SRA_{UC} = \$2.7K\ each_{(AVG)}$

(4) UUT Contractor Maintenance/Repair (CM/R): This element includes the maintenance support costs associated with the support of UUTs during the 2-year TPS development period. It is calculated as a fixed percentage of UUT costs/year.

$$UUT_{CMS} = 10\%/yr \times \#TPS_{yrs} \times UUT_{UC}$$

(5) GFF Cost Summary:

$$GFF_{Cost-WRA} = SE_{Costs} + TRD_{NR} + UUT_{Costs} + UUT_{CMS}$$

$$= (0.52 \times SE_{UC}) + (\$25K \times (\propto)) + IC + 0 + \frac{\$36.6K \times 7}{2} + (0.2 \times \$256K)$$

$$GFF_{Cost-SRA} = (0.52 \times SE_{UC}) + (\$25K \times (\propto)) + IC + 0 + \frac{\$2.7K \times (21)}{2} + (0.2 \times \$256K)$$

Example ASM-607

$$GFF_{Cost-WRA} = (0.52 \times \$65K) + (\$25K \times (0.02)) + 0 + 0 + \frac{(\$36.6K \times 7)}{2} + (0.2 \times \$256K)$$

$$= \$33.80K + \$0.50K + 0 + 0 + \$128.1K + \$51.2K$$

$$= \$214K$$

CAT III-D

$$GFF_{Cost-WRA} = (0.52 \times \$500K) + (\$25K \times (0.21)) + \$60K + 0 + \frac{(\$256.2K)}{2} + (\$51.2K)$$

$$= \$260K + \$5.25K + \$60K + 0 + \$128.1K + \$51.2K$$

$$= \$504.55K$$

$$GFF_{Cost-SRA} = SE_{Cost} + TRD_{NR} + UUT_{Cost} + UUT_{CMS}$$

$$(0.52 \times \$500K) + (\$25K \times (0.21)) + \$60K + 0 + \frac{\$56.7K}{2} + \$11.34K$$

$$= \$364.94K$$

4. RECURRING COST ALGORITHMS

a. Support Equipment Hardware Costs:

$$SE_{HC} = SE_{UC} \times \#SE$$

b. Support Equipment Installation Costs:

$$SE_{IC_{ATE}} = \#SE \times \$100K \text{ (Shipboard)} \times \$60K \text{ (Shore site)}$$

$$SE_{IC_{607}} = 0$$

c. Technical Publications Cost:

$$TP_{R\text{-}Cost} = 0.03 \times SE_{UC} \times \#SE$$

d. Modification Costs:

$$M_{R\text{-}Cost} = M_{UC} \times \#SE$$

e. Special Support Equipment

$$SSE_{R\text{-}Cost} = \$125K \times (\alpha) \times \#SE$$

f. Initial Support Equipment Spares Costs:

$$SE_{S\text{-}Cost} = 0.23 \times SE_{UC} \times \#SE$$

g. Incremental Prime Equipment Site Spares:

Zero cost, by NAVAIRSYSCOM direction

h. Test Program Sets:

$$TP_{R\text{-}Cost} = \frac{ID_{NR} \times \#Sites}{5}$$

i. Maintenance Assist Modules (MAMs). This cost element includes the cost associated with obtaining any required MAMs necessary to resolve ambiguity groups which are otherwise not directly resolvable through use of the tester and TPS. The required costs are a function of the level of MAMs required and the cost of the prime equipment SRAs.

Therefore: MAMs% = 2X + 1.8

Where: X = Existing ambiguity ratio without MAMs
MAMs% = The required MAMs% of the total avionics suite modules.

$$\text{Then: MAMs Costs} = \text{MAMs\%} \times \sum_{i=1}^{\#UUT} SRA_{UC} \times \#\ \text{Sites}$$

Where: SRA_{UC} = SRA Unit Cost

X_{607} = 1.14 ambiguity ratio for ASM-607

X_{ATE} = 1.02 ambiguity ratio for ATE

$MAMs_{ATE}\% = 2 \times (1.02) + 1.8 = 3.84\%$

$MAMs_{607\%} = 2 \times (1.14) + 1.8 - 4.08\%$

$$MAMs_{ATE}\text{Costs} = \text{MAMs\%} \times \sum_{i=1}^{\#UUT} SRA_{UC} \times \#\ \text{Sites}$$

$$= 0.0384 \times \$2.7K \times 21\ \text{SRAs} \times 30 = \$65.32K$$

j. Interconnecting Devices Initial Spares

$$ID_{R\text{-}Cost} = 0.23 \times \frac{ID_{NR}}{5} \times \#\ \text{Sites}$$

5. SUSTAINING COST ALGORITHMS. All sustaining costs are calculated for a period of 10 years. The individual cost elements are calculated for the VAST system as the baseline and then derated to the appropriate value for each alternate tester through the relative complexity factor ($\propto$).

a. Depot Rework. This element includes the costs associated with annual depot overhaul of testers. The algorithm is based on a known $40,000 per year per station cost for VAST depot rework.

$$\text{Depot Rework Costs} = \$40K \times 10\ \text{yr} \times (\propto) \times \#GSE$$

$$(\$40K) \times (10) \times (0.21) \times (7)$$

$$= \$588K\ \text{(for CAT-III-D)}$$

b. Depot Component Repair. This element includes the estimated costs to provide necessary repair to tester building blocks. The calculation is based on the VAST station costs.

$$\text{Depot Component Repair} = \$10.24K/\text{yr} \times 10\ \text{yr} \times (\propto) \times \#GSEs$$

$$= \$10.24K \times 10 \times 0.21 \times 7$$

$$= \$102.4K \times (\propto) \times \#\text{New GSE}$$

c. Packaging, Handling, Storage, Transportation (PHST). These are the costs incurred in sending tester SRAs back to the depot for repair and subsequent return to the supply system. This cost element is based on a percentage of component repair costs as follows:

PHST Costs = 20% x $102.4K x 10 yr x ($\alpha$) x #GSEs

= (0.2) x (102.4) x (10) x (0.21) x (7)

= $301K (For CAT III-D)

= ($204.8K) x ($\alpha$) x (#New GSE)

d. Depot Calibration. This cost element includes the normal yearly recalibration costs required of a tester other than those performed during end item rework. It is based solely on the estimated required amounts of labor needed to accomplish the tasks each year. Therefore:

- VAST single station calibration costs/year =

  2 men x 4 days x 8 hours/day x $32/hour = $2.048K

- Depot Calibration Costs = $2.048K x 10 yr x ($\alpha$) x #GSE

  = $2.048K x 10 x 0.21 x 7

  = $30K (CAT III-D)

  = 20.48K x (α) x # New GSE

e. Intermediate-/Depot-Level Repair. This cost element accumulates the I- and D-level labor hours cost associated with an individual tester. Costs are based on estimated VAST station workloads and then derated by the appropriate complexity factor (α). It is also assumed that 80% of the total repair activity occurs at the IMA level performed by workers earning $18,000/year, and that approximately 1,430 hours of depot activity were accrued in a given year on VAST. Therefore:

- IMA Hours = 0.8/0.2 x 1430

- IMA Hourly Labor Rate = $18,000/2080 hr/yr

- VAST I-Level Repair Costs = $8.65/hr x 5720 hr = $50,000

Therefore:

I-Level Repair Costs = Test Time/Mo. x 12 mo/yr x 10 yr x $8.65/hr at (I-Level)

= 273 hr/mo x 12 mo/yr x 10 yr x $8.65/hr at (I-Level)

= $283K (For testers at I-Level)

D-Level Repair Costs = Test Time/mo x 12 mo/yr x 10 yr x $24/hr D-Level

= 418 hr/mo x 12 mo/yr x 10 yr x $24/hr

= $1,204K (For testers at D-Level)

f. Intermediate-Level Calibration. The cost element includes the normal yearly calibration of I-level testers. An assumption has been made that approximately 60% of the total calibration man-hours are expended at the IMA, and that I-Level calibration costs are $8.65/hour as defined earlier.

Assuming:

o VAST Depot Level Annual Calibration Costs = 2 men x 32 hr

o IMA Level Calibration Hours = $64 \times \frac{0.6}{0.4} = 96$ hr

o I-Level VAST Station Calibration Costs =

96 hr/yr. x $8.65/hr. = $830/yr

IMA Calibration Costs ≈ $830/yr x 10 yr x (∝) x # stations

= $830 x 10 x 0.21 x 7

= $12K (For CAT III-D)

= ($8.3K x (∝) x (# New GSE)

g. Training Costs = (Operator Training Costs + Maintenance Training Costs) x (∝) x (# GSE) x (ARATE) x (# yr-1)

= $18.2K x (∝) x (# GSE) x (ARATE) x (# yr-1)

= $81.9K (∝) x (# GSE)

h. Replenishment Spares and Repair Parts. This element includes all costs associated with obtaining additional GSE modules and parts to replace those lost to attrition over the 10-year life cycle. Analysis of available budget work sheets and existing program data pointed to a relationship between replenishment costs and recurring GSE acquisition costs for avionics GSE.

Therefore:

o RSRP = 10% x 10 yr (ATE costs + ID costs) x # GSEs

Where:

Hardware Costs = Recurring GSE Costs

ID Costs = Recurring ID Costs = $\frac{ID_{NR}}{5}$

RSRP = $0.1 \times 10 \left(\$500K \times \# GSE\right) + \left(\frac{ID_{NR}}{5} \times \# IDs\right)$

= $0.1 \times 10 \left(\$500K \times 7\right) + \left(\frac{\$307K}{5} \times 30\right)$

= \$5,342K (For CAT III-D)

i. Technical Publications and Revisions (TPR). All engineering, printing, and publishing costs associated with technical documentation updates over the 10-year AYK-14 GSE sustaining period are included. Replenishment of Calibration Standards for all support sites is also included. Revision costs are a function of the number of pages required and the relative complexity of the particular tester.

TPR Costs = N pages x D cost/page x 10 yr x (α)

= \$21.4K x (α)

N = 10.7 pages/yr

D = \$200/page

j. In-Service Engineering

TPS Maintenance = 7%/yr x 10 yr x TPS_{NR}

= .07 x 10 x \$1,536K

= \$1,075K

= 0.7 x TPS_{NR}

C. LIFE CYCLE COST SUMMARY

1. The LCC summary for intermediate WRA support of the AYK-14 is presented in Table 36. The ranking by cost of the nine candidate testers for I-level support is as follows:

Tester	LCC ($K)
AN/ASM-607 (MLV)	7,788
AN/USM-429 (CAT III-D)	17,944
AN/USM-453 (DIMOTE II)	23,660
AN/USM-403 (HATS)	40,588
AN/ASM-608 (NSTS)	49,586
AN/USM-449 (AAI-5565)	57,557
AN/USM-470(V)1 (MINI-VAST)	93,665
AN/USM-247 (VAST)	173,567

2. For the depot support of the AYK-14 SRAs, the LCC Summary is presented in Table 37. The ranking by cost of the seven candidate testers for depot level support is as follows:

Tester	LCC ($K)
AN/USM-429 (CAT III-D)	7,334
AN/USM-247 (VAST)	9,175
AN/USM-449 (AAI-5565)	9,788
AN/ASM-608 (NSTS)	9,857
AN/USM-403 (HATS)	10,017
AN/USM-453 (DIMOTE II)	11,746
AN/USM-470(V)1 (MINI-VAST)	15,299

3. Since the AN/USM-429 (CAT III-D) tester is the most cost effective depot-level tester in support of the AYK-14 and was the second most cost effective intermediate level tester in support of AYK-14 (WRA) testing, we will now review the cost effectiveness of utilizing a combinational tester approach to the I-level support of WRA testing. The LCC summary of this combinational approach (AN/ASM-607 and AN/USM-429 (CAT III-D)) is presented in Table 38. The combinational WRA support approach LCC is as follows:

			LCC ($K)
o	7	- AN/ASM-607 (MLV)	1,747
o	23	- AN/USM-429 (CAT III-D)	7,303
	30	Total	9,050

NOTE:
Included in the CAT III-D I-Level costs are WRA-TPS nonrecurring cost of $1,076K or a decrease of $3,189K. These costs could be justifiably charged to the Depot where the WRA TPSs are required. This would lower the I-level costs to $5,861K.

TABLE 36 - LIFE CYCLE COST SUMMARY
(WRA SUPPORT)
I-LEVEL

TESTER ALTERNATIVE	LIFE CYCLE COST SUMMARY ($K)			GRAND TOTAL ($K)
	NONRECURRING	RECURRING	SUSTAINING	
AN/ASM-607 MLV	866	3,375	3,547	7,788
AN/USM-429 CAT III-D	2,773	7,219	7,952	17,944
AN/USM-403 HATS	3,470	18,945	18,173	40,588
AN/USM-449 AAI-5565	3,482	25,077	28,997	57,556
AN/USM-453 DIMOTE II	4,445	9,024	10,191	23,660
AN/ASM-608 NSTS	3,841	22,396	23,349	49,586
AN/USM-470(V)1 MINI-VAST	3,542	46,776	43,337	93,655
AN/USM-247 VAST	6,023	87,278	80,266	173,567

TABLE 37 - LIFE CYCLE COST SUMMARY
D-LEVEL
(SRA SUPPORT)

TESTER ALTERNATIVE	LIFE CYCLE COST SUMMARY ($K)			GRAND TOTAL ($K)
	NONRECURRING	RECURRING	SUSTAINING	
AN/USM-429 CAT III-D	2,247	1,522	3,565	7,334
AN/USM-403 HATS	3,192	2,318	4,507	10,017
AN/USM-449 AAI-5565	3,268	1,889	4,631	9,788
AN/USM-453 DIMOTE II	5,966	992	4,789	11,747
AN/ASM-608 NSTS	3,982	1,508	4,367	9,857
AN/USM-470(V)1 MINI-VAST	3,014	5,354	6,931	15,299
AN/USM-247 VAST	5,982	221	2,972	9,175

TABLE 38 - LIFE CYCLE COST SUMMARY
(WRA SUPPORT)
COMBINATIONAL

TESTER ALTERNATIVE	LIFE CYCLE COST SUMMARY ($K)			GRAND TOTAL ($K)
	NONRECURRING	RECURRING	SUSTAINING	
AN/ASM-607 (7) MLV	321	672	754	1,747
AN/USM-429 (23) CAT III-D	2,773	1,801	2,729	7,303
COMBINATION (7) AN/ASM-607 (23) AN/USM-429	3,094	2,473	3,483	9,050

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VII. RISK ASSESSMENT

A. In this SESA, three risk categories were analyzed:

Technical Risks

Schedule Risks

Cost Risks

The testers and test program sets were evaluated in all three categories at both the I- and D-levels of maintenance. The following risk characteristics were considered for each risk element to determine whether a particular risk was evaluated as low (L), medium (M), or high (H) risk:

Is tester in the Navy's inventory.

Availability of tester from manufacturer.

Avionic test requirements complexity.

Tester-avionics compatibility.

Test program set complexity.

Tester procurement data availability.

Quality of tester unit cost estimate.

Quality of tester delivery schedule.

Time period of tester and TPS procurement.

B. A risk assessment summary is presented in Table 39. Each of the eight tester candidates is noted and the three risk categories (technical, schedule, and cost) are subdivided into intermediate level for WRA support and depot level for SRA and WRA support. Risk value judgments based on the risk characteristics noted above were determined for each tester and TPS risk elements for both the I- and D-level; the combined risk assessment rankings are noted in the right column of Table 39. The lowest combined risk category was assigned to the ASM-607, USM-429 (CAT III-D), and the USM-449 for the I-level, and to the USM-429 (CAT III-D) for the D-level.

TABLE 39 - RISK ASSESSMENT SUMMARY

TESTER CANDIDATES	TECHNICAL RISK				SCHEDULE RISK				COST RISK				COMBINED RISK ASSESSMENT RANKING	
	INTERMEDIATE LEVEL (WRA)		DEPOT LEVEL (SRA & WRA)		INTERMEDIATE LEVEL (WRA)		DEPOT LEVEL (SRA & WRA)		INTERMEDIATE LEVEL (WRA)		DEPOT LEVEL (SRA & WRA)			
	TESTER	TEST PROGRAM SETS	TESTER	TEST PROGRAM SETS	TESTER	TEST PROGRAM SETS	TESTER	TEST PROGRAM SETS	TESTER	TEST PROGRAM SETS	TESTER	TEST PROGRAM SETS	I LEVEL	D LEVEL
AN/ASM-607 MEMORY LOADER VERIFIER	L	L	NA	NA	L	L	NA	NA	L	L	NA	NA	12	NA
AN/USM-429 CAT III-D	L	L	L	L	L	L	L	L	L	L	L	L	12	12
AN/USM-449 AAI-5565	L	L	L	M-	M	L	L	L	L	L	L	M	14	15
AN/USM-403 HATS	L	L	M	L-	M	L	M	M	L	L	L	L-	14	16
AN/ASM-608 NSIS	L	L	M-	M-	M-	M	M-	M	L	L	L	M	15	19
AN/USM-453 DIMOTE II	L	L	M	H	M-	L	M-	H	L	L	L	H	13	27
AN/USM-470(V)1 MINI-VAST	L	L	M-	M-	M	M	M	M	M	M	M	M	20	22
AN/USM-247 VAST	L	L	M	M	L	L	L	M	L	L	L	M	12	20

NA = Not Applicable
L = Low Risk Value Judgment
M = Medium Risk Value Judgment
H = High Risk Value Judgment

H = 6
H- = 5
M = 4
M- = 3
L = 2
L- = 1

APPENDIX A

COST ANALYSIS

Life cycle cost summaries are presented as follows:

TABLE A1 - AN/ASM-607 (MEMORY LOADER/VERIFIER) WRA SUPPORT COMBINATION AND WRA SUPPORT

NONRECURRING COSTS	WRA SUPPORT COMBINATION COST ($K)	WRA SUPPORT COMBINATION TOTAL($K)	WRA SUPPORT COST ($K)	WRA SUPPORT TOTAL ($K)
MODIFICATION TO SUPPORT EQUIPMENT.....	0.000		0.000	
INTEGRATED LOGISTIC SUPPORT.....	68.905		68.905	
TEST PROGRAM SETS.....	166.953		584.334	
GOVERNMENT-FURNISHED FACTORS.....	84.705	320.563	212.805	866.004
RECURRING COSTS				
HARDWARE.....	455.000		1,950.000	
INSTALLATION.....	35.000		150.000	
TECHNICAL PUBLICATIONS.....	13.650		58.500	
MODIFICATION.....	0.000		0.000	
SPECIAL SUPPORT EQUIPMENT.....	17.500		75.000	
INITIAL SUPPORT EQUIPMENT SPARES.....	104.650		448.500	
INCREMENTAL PRIME EQUIPMENT SITE SPARES....	0.000		0.000	
TEST PROGRAM SETS.....	34.286		514.290	
MAINTENANCE ASSIST MODULES.....	4.099		61.488	
ID INITIAL SPARES.....	7.825	672.010	117.369	3,375.147
SUSTAINING COSTS				
DEPOT REWORK.....	56.000		240.000	
DEPOT COMPONENT REPAIR.....	14.336		61.440	
PACKAGING, HANDLING, STORAGE, TRANSPORTATION	28.672		122.880	
DEPOT CALIBRATION.....	2.867		12.288	
INTERMEDIATE-LEVEL REPAIR.....	62.286		283.392	
INTERMEDIATE-LEVEL CALIBRATION.....	1.162		4.980	
TRAINING.....	14.014		60.060	
REPLENISHMENT SPARES AND REPAIR PARTS.....	489.286		2,464.290	
TECHNICAL PUBLICATIONS REVISION.....	.428		.428	
IN-SERVICE ENGINEERING.....	84.994	754.045	297.479	3,547.237
TOTAL LIFE CYCLE COST ($K)		1,746.618		7,788.428

TABLE A2 - AN/USM-429 (CAT III-D) WRA SUPPORT COMBINATION, WRA SUPPORT, AND SRA SUPPORT

NONRECURRING COSTS	WRA SUPPORT COMBINATION COST($K)	WRA SUPPORT COMBINATION TOTAL($K)	WRA SUPPORT COST($K)	WRA SUPPORT TOTAL($K)	SRA SUPPORT COST($K)	SRA SUPPORT TOTAL($K)
MODIFICATION TO SUPPORT EQUIPMENT.....	0.000		0.000		0.000	
INTEGRATED LOGISTIC SUPPORT.....	222.751		222.751		187.408	
TEST PROGRAM SETS.....	2,112.688		2,112.303		1,761.691	
GOVERNMENT-FURNISHED FACTORS.....	437.465	2,772.904	437.465	2,772.519	296.113	2,247.212
RECURRING COSTS						
HARDWARE.....	0.000		3,500.000		1,002.000	
INSTALLATION.....	0.000		280.000		80.000	
TECHNICAL PUBLICATIONS.....	0.000		105.000		30.060	
MODIFICATION.....	0.000		0.000		0.000	
SPECIAL SUPPORT EQUIPMENT.....	0.000		183.750		52.605	
INITIAL SUPPORT EQUIPMENT SPARES.....	0.000		805.000		230.460	
INCREMENTAL PRIME EQUIPMENT SITE SPARES....	0.000		0.000		0.000	
TEST PROGRAM SETS.....	1,428.070		1,859.760		103.293	
MAINTENANCE ASSIST MODULES.....	47.141		61.488		0.000	
ID INITIAL SPARES.....	325.864	1,801.075	424.074	7,219.072	23.641	1,522.059
SUSTAINING COSTS						
DEPOT REWORK.....	0.000		588.000		168.336	
DEPOT COMPONENT REPAIR.....	0.000		150.528		43.094	
PACKAGING, HANDLING, STORAGE, TRANSPORTATION	0.000		301.056		86.188	
DEPOT CALIBRATION.....	0.000		30.106		8.619	
INTERMEDIATE-LEVEL REPAIR.....	221.076		283.392		1,206.374	
INTERMEDIATE-LEVEL CALIBRATION.....	0.000		12.201		3.493	
TRAINING.....	0.000		147.147		42.126	
REPLENISHMENT SPARES AND REPAIR PARTS.....	1,428.070		5,359.760		1,105.293	
TECHNICAL PUBLICATIONS REVISION.....	4.494		4.494		4.494	
IN-SERVICE ENGINEERING.....	1,075.550	2,729.190	1,075.354	7,952.038	896.861	3,564.878
TOTAL LIFE CYCLE COST ($K)		7,303.169		17,943.629		7,334.149

TABLE A3 - AN/USM-403 (HATS) WRA AND SRA SUPPORT

NONRECURRING COSTS	WRA SUPPORT COST ($K)	WRA SUPPORT TOTAL ($K)	SRA SUPPORT COST ($K)	SRA SUPPORT TOTAL ($K)
MODIFICATION TO SUPPORT EQUIPMENT	0.000		0.000	
INTEGRATED LOGISTIC SUPPORT	272.647		276.805	
TEST PROGRAM SETS	2,607.220		2,464.193	
GOVERNMENT-FURNISHED FACTORS	590.390	3,470.257	450.740	3,191.738
RECURRING COSTS				
HARDWARE	12,000.000		1,600.000	
INSTALLATION	600.000		80.000	
TECHNICAL PUBLICATIONS	360.000		48.000	
MODIFICATION	0.000		0.000	
SPECIAL SUPPORT EQUIPMENT	337.500		45.000	
INITIAL SUPPORT EQUIPMENT SPARES	2,760.000		368.000	
INCREMENTAL PRIME EQUIPMENT SITE SPARES	0.000		0.000	
TEST PROGRAM SETS	2,300.760		143.934	
MAINTENANCE ASSIST MODULES	61.488		0.000	
ID INITIAL SPARES	525.504	18,945.252	32.941	2,317.875
SUSTAINING COSTS				
DEPOT REWORK	1,080.000		144.000	
DEPOT COMPONENT REPAIR	276.480		36.864	
PACKAGING, HANDLING, STORAGE, TRANSPORTATION	552.960		73.728	
DEPOT CALIBRATION	55.296		7.373	
INTERMEDIATE-LEVEL REPAIR	283.392		1,203.840	
INTERMEDIATE-LEVEL CALIBRATION	22.410		2.988	
TRAINING	270.270		36.036	
REPLENISHMENT SPARES AND REPAIR PARTS	14,300.760		1,743.934	
TECHNICAL PUBLICATIONS REVISION	3.852		3.852	
IN-SERVICE ENGINEERING	1,327.312	18,172.732	1,254.498	4,507.113
TOTAL LIFE CYCLE COST ($K)		40,588.241		10,016.726

TABLE A4 - AN/USM-449 (AAI-5565) WRA AND SRA SUPPORT

NONRECURRING COSTS	WRA SUPPORT COST ($K)	WRA SUPPORT TOTAL ($K)	SRA SUPPORT COST ($K)	SRA SUPPORT TOTAL ($K)
MODIFICATION TO SUPPORT EQUIPMENT	0.000		0.000	
INTEGRATED LOGISTIC SUPPORT	283.042		276.112	
TEST PROGRAM SETS	2,707.128		2,640.041	
GOVERNMENT-FURNISHED FACTORS	491.315	3,481.485	351.665	3,267.818
RECURRING COSTS				
HARDWARE	15,600.000		1,200.000	
INSTALLATION	1,040.000		80.000	
TECHNICAL PUBLICATIONS	468.000		36.000	
MODIFICATION	0.000		0.000	
SPECIAL SUPPORT EQUIPMENT	1,397.500		107.500	
INITIAL SUPPORT EQUIPMENT SPARES	3,588.000		276.000	
INCREMENTAL PRIME EQUIPMENT SITE SPARES	0.000		0.000	
TEST PROGRAM SETS	2,379.090		154.434	
MAINTENANCE ASSIST MODULES	61.488		0.000	
ID INITIAL SPARES	543.375	25,077.453	35.356	1,889.290
SUSTAINING COSTS				
DEPOT REWORK	4,472.000		344.000	
DEPOT COMPONENT REPAIR	1,144.832		88.064	
PACKAGING, HANDLING, STORAGE, TRANSPORTATION	2,289.664		176.128	
DEPOT CALIBRATION	228.966		17.613	
INTERMEDIATE-LEVEL REPAIR	283.392		1,203.840	
INTERMEDIATE-LEVEL CALIBRATION	92.794		7.138	
TRAINING	1,119.118		86.086	
REPLENISHMENT SPARES AND REPAIR PARTS	17,979.090		1,354.434	
TECHNICAL PUBLICATIONS REVISION	9.202		9.202	
IN-SERVICE ENGINEERING	1,378.174	28,997.232	1,344.021	4,630.526
TOTAL LIFE CYCLE COST ($K)		57,556.170		9,787.634

TABLE A5 - AN/USM-453B (DIMOTE II) WRA AND SRA SUPPORT

NONRECURRING COSTS	WRA SUPPORT COST ($K)	WRA SUPPORT TOTAL ($K)	SRA SUPPORT COST ($K)	SRA SUPPORT TOTAL ($K)
MODIFICATION TO SUPPORT EQUIPMENT	0.000		0.000	
INTEGRATED LOGISTIC SUPPORT	390.457		542.224	
TEST PROGRAM SETS	3,771.075		5,280.949	
GOVERNMENT-FURNISHED FACTORS	282.915	4,444.447	143.265	5,966.438
RECURRING COSTS				
HARDWARE	3,200.000		400.000	
INSTALLATION	640.000		80.000	
TECHNICAL PUBLICATIONS	96.000		12.000	
MODIFICATION	0.000		0.000	
SPECIAL SUPPORT EQUIPMENT	220.000		27.500	
INITIAL SUPPORT EQUIPMENT SPARES	736.000		92.000	
INCREMENTAL PRIME EQUIPMENT SITE SPARES	0.000		0.000	
TEST PROGRAM SETS	3,313.800		309.918	
MAINTENANCE ASSIST MODULES	61.488		0.000	
ID INITIAL SPARES	756.861	9,024.149	70.711	992.129
SUSTAINING COSTS				
DEPOT REWORK	704.000		88.000	
DEPOT COMPONENT REPAIR	180.224		22.528	
PACKAGING, HANDLING, STORAGE, TRANSPORTATION	360.448		45.056	
DEPOT CALIBRATION	36.045		4.506	
INTERMEDIATE-LEVEL REPAIR	283.392		1,203.840	
INTERMEDIATE-LEVEL CALIBRATION	14.608		1.826	
TRAINING	176.176		22.022	
REPLENISHMENT SPARES AND REPAIR PARTS	6,513.800		709.918	
TECHNICAL PUBLICATIONS REVISION	2.354		2.354	
IN-SERVICE ENGINEERING	1,919.820	10,190.867	2,688.483	4,788.533
TOTAL LIFE CYCLE COST ($K)		23,659.463		11,747.100

TABLE A6 - AN/ASM-608 (NSTS) WRA AND SRA SUPPORT

	WRA SUPPORT		SRA SUPPORT	
NONRECURRING COSTS	COST ($K)	TOTAL ($K)	COST ($K)	TOTAL ($K)
MODIFICATION TO SUPPORT EQUIPMENT.....	0.000		0.000	
INTEGRATED LOGISTIC SUPPORT.....	323.236		348.877	
TEST PROGRAM SETS.....	3,105.795		3,360.761	
GOVERNMENT-FURNISHED FACTORS.....	411.915	3,840.946	272.265	3,981.903
RECURRING COSTS				
HARDWARE.....	13,500.000		900.000	
INSTALLATION.....	1,200.000		80.000	
TECHNICAL PUBLICATIONS.....	405.000		27.000	
MODIFICATION.....	0.000		0.000	
SPECIAL SUPPORT EQUIPMENT.....	787.500		52.500	
INITIAL SUPPORT EQUIPMENT SPARES.....	3,105.000		207.000	
INCREMENTAL PRIME EQUIPMENT SITE SPARES.....	0.000		0.000	
TEST PROGRAM SETS.....	2,712.990		196.224	
MAINTENANCE ASSIST MODULES.....	61.488		0.000	
ID INITIAL SPARES.....	623.553	22,395.531	45.016	1,507.740
SUSTAINING COSTS				
DEPOT REWORK.....	2,520.000		168.000	
DEPOT COMPONENT REPAIR.....	645.120		43.008	
PACKAGING, HANDLING, STORAGE, TRANSPORTATION	1,290.240		86.016	
DEPOT CALIBRATION.....	129.024		8.602	
INTERMEDIATE-LEVEL REPAIR.....	283.392		1,203.840	
INTERMEDIATE-LEVEL CALIBRATION.....	52.290		3.486	
TRAINING.....	630.630		42.042	
REPLENISHMENT SPARES AND REPAIR PARTS.....	16,212.990		1,096.224	
TECHNICAL PUBLICATIONS REVISION.....	4.494		4.494	
IN-SERVICE ENGINEERING.....	1,581.132	23,349.312	1,710.933	4,366.645
TOTAL LIFE CYCLE COST ($K)		49,585.789		9,856.288

TABLE A7 - AN/USM-470(V)1 (MINI-VAST) WRA AND SRA SUPPORT

	WRA SUPPORT		SRA SUPPORT	
NONRECURRING COSTS	COST ($K)	TOTAL ($K)	COST ($K)	TOTAL ($K)
MODIFICATION TO SUPPORT EQUIPMENT	0.000		0.000	
INTEGRATED LOGISTIC SUPPORT	222.751		187.408	
TEST PROGRAM SETS	2,112.303		1,759.931	
GOVERNMENT-FURNISHED FACTORS	1,206.715	3,541.769	1,067.065	3,014.404
RECURRING COSTS				
HARDWARE	34,000.000		4,000.000	
INSTALLATION	680.000		80.000	
TECHNICAL PUBLICATIONS	1,020.000		120.000	
MODIFICATION	0.000		0.000	
SPECIAL SUPPORT EQUIPMENT	913.750		107.500	
INITIAL SUPPORT EQUIPMENT SPARES	7,820.000		920.000	
INCREMENTAL PRIME EQUIPMENT SITE SPARES	0.000		0.000	
TEST PROGRAM SETS	1,856.820		102.984	
MAINTENANCE ASSIST MODULES	61.488		0.000	
ID INITIAL SPARES	424.074	46,776.132	23.570	5,354.054
SUSTAINING COSTS				
DEPOT REWORK	2,924.000		344.000	
DEPOT COMPONENT REPAIR	748.544		88.064	
PACKAGING, HANDLING, STORAGE, TRANSPORTATION	1,497.088		176.128	
DEPOT CALIBRATION	149.709		17.613	
INTERMEDIATE-LEVEL REPAIR	283.392		1,203.840	
INTERMEDIATE-LEVEL CALIBRATION	60.673		7.138	
TRAINING	731.731		86.086	
REPLENISHMENT SPARES AND REPAIR PARTS	35,856.820		4,102.984	
TECHNICAL PUBLICATIONS REVISION	9.202		9.202	
IN-SERVICE ENGINEERING	1,075.354	43,336.513	895.965	6,931.020
TOTAL LIFE CYCLE COST ($K)		93,654.414		15,299.478

TABLE A8 - AN/USM-247 (VAST) WRA AND SRA SUPPORT

	WRA SUPPORT		SRA SUPPORT	
NONRECURRING COSTS	COST ($K)	TOTAL ($K)	COST ($K)	TOTAL ($K)
MODIFICATION TO SUPPORT EQUIPMENT	0.000		0.000	
INTEGRATED LOGISTIC SUPPORT	310.069		296.272	
TEST PROGRAM SETS	2,966.136		3,078.075	
GOVERNMENT-FURNISHED FACTORS	2,746.840	6,023.045	2,607.190	5,981.537
RECURRING COSTS				
HARDWARE	65 000.000		0.000	
INSTALLATION	520.000		0.000	
TECHNICAL PUBLICATIONS	1,950.000		0.000	
MODIFICATION	0.000		0.000	
SPECIAL SUPPORT EQUIPMENT	1,625.000		0.000	
INITIAL SUPPORT EQUIPMENT SPARES	14,950.000		0.000	
INCREMENTAL PRIME EQUIPMENT SITE SPARES	0.000		0.000	
TEST PROGRAM SETS	2,582.160		179.802	
MAINTENANCE ASSIST MODULES	61 188		0.000	
ID INITIAL SPARES	589.743	87,278.391	41.152	220.954
SUSTAINING COSTS				
DEPOT REWORK	5,200.000		0.000	
DEPOT COMPONENT REPAIR	1,331.200		0.000	
PACKAGING, HANDLING, STORAGE, TRANSPORTATION	2,662.400		0.000	
DEPOT CALIBRATION	266.240		0.000	
INTERMEDIATE-LEVEL REPAIR	283.392		1,203.840	
INTERMEDIATE-LEVEL CALIBRATION	107.900		0.000	
TRAINING	1,301.300		0.000	
REPLENISHMENT SPARES AND REPAIR PARTS	67,582.160		179.802	
TECHNICAL PUBLICATIONS REVISION	21.400		21.400	
IN-SERVICE ENGINEERING	1,510.033	80,266.025	1,567.020	2,972.062
TOTAL LIFE CYCLE COST ($K)		173,567.461		9,174.553

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GLOSSARY

ALU.....Arithmetic logical unit
ATE.....Automatic test equipment

BC.....Bus controller
BEM.....Bus extender module
BIT.....Built-in test
BITE.....Built-in test equipment
BM.....Bus monitor

CCU.....Computer control unit
CDC.....Control Data Corporation
CMM.....Core memory module
CMQT.....CPU/memory quick-look test
CPU.....Central processing unit

DID.....Input Discretes
DIM.....Discrete interface module
DIO.....Bidirectional discretes
DIOM.....Discrete input/output module
DIS.....Switch closure input discretes
DMA.....Direct memory access
DNA.....Data not available

EAU.....Extended arithmetic unit

FFT.....Fast Fourier transform
FID.....Fault isolation diagnostic

GFF.....Government-furnished factors
GPM.....General processing module
GSE.....Ground support equipment

HEX.....Hexadecimal notation

ID.....Interconnect devices
IFPM.....In-flight performance monitoring
ILS.....Integrated logistic support
IOC.....Input/output controller
IOP.....Input/output processor

LCC/I.....Life cycle costs and impact analysis
LORA.....Level of repair analysis
LSI.....Large-scale integration
LVU.....Loader/verifier unit

MAM.....Maintenance assist modules
MCM.....Memory control module
MEU.....Memory expansion unit
MLV.....Memory loader verifier
MMA.....Micromemory address
MMBUS.....Microcommand to micromemory bus

MOS.....Metal oxide semiconductor
MSI.....Medium-scale integration
MTBF.....Mean-time-between-failures
MTTR.....Mean-time-to-repair

NARF.....Naval Air Rework Facilities
NIM.....NTDS-interface module
NRZ.....No return to zero
NSD.....Navy support date

PCM.....Power converter module
PDD.....Program development data
PIM.....Proteus interface module
PPSM.....PIC/POC/SDC Module
PROM.....Programmable read only memory
PSM.....Processor support module

RAM.....Random access memory
RIM.....RS-232-C interface module
RIW.....Reliability improvement warranty
RMW.....Read-modify-write
RT.....Remote terminal
RTC.....Real time clock
RXM.....*Read/write expandable module*

SDEX.....Standard real time executive
SESA.....Support equipment selection analysis
SIM.....Serial interface module
SMM.....Semiconductor memory module
SRA.....Shop-replaceable assembly
SSI.....Small-scale integration
ST.....Self-test
STE.....Standard test equipment

TPS.....Test program set
TRA.....Test requirement analysis
TRD.....Test requirement documents
TT.....Test time
TTL.....Transistor-transistor logic

UART.....Universal asynchronous receiver/transmitter
UUT.....Unit under test

VAST.....Versatile avionics shop tester
WL.....Workload
WRA.....Weapon replaceable assembly

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