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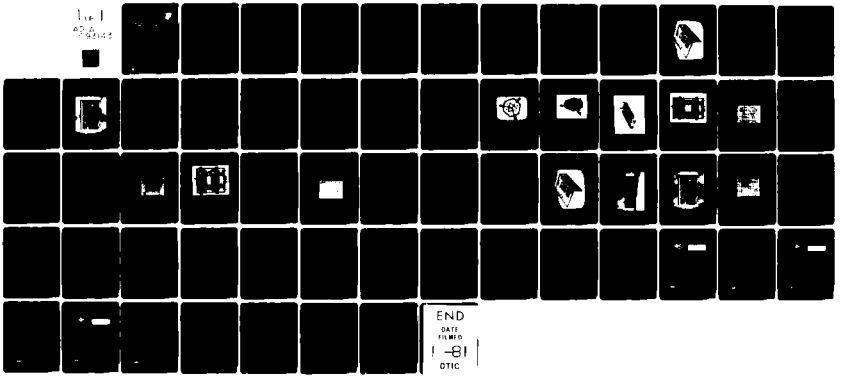

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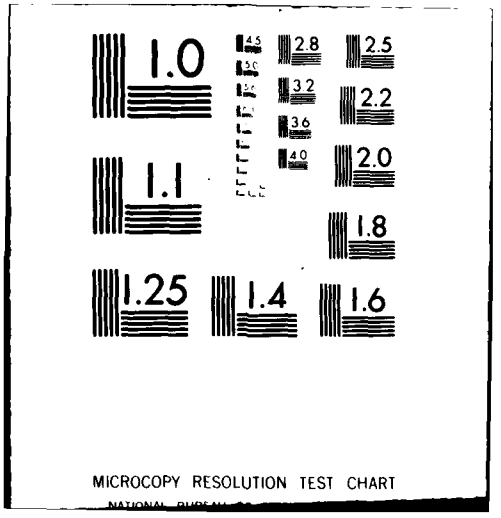
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RADC-TR-80-330
Interim Report
October 1980

LEVEL II

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BROADBAND LINEAR COMMUNICATIONS AMPLIFIER

Ford Aerospace and Communications Corporation

Dr. Pang T. Ho

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER: RADC-TR-80-330	2. GOVT ACCESSION NO.: AD-A093 143
3. RECIPIENT'S CATALOG NUMBER:	
4. TITLE (and Subtitle): BROADBAND LINEAR COMMUNICATIONS AMPLIFIER	5. TYPE OF REPORT & PERIOD COVERED: Interim Report. Sep 77 — Sep 80
	6. PERFORMING ORG. REPORT NUMBER: N/A
7. AUTHOR(s): Dr. Pang T. Ho	8. CONTRACT OR GRANT NUMBER(s): F30602-77-C-0189 new
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Ford Aerospace and Communications Corporation, WDL Division, 3939 Fabian Way, Palo Alto CA 94303	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62702F 45192114 21
11. CONTROLLING OFFICE NAME AND ADDRESS: Rome Air Development Center (DCCT), Griffiss AFB NY 13441	12. REPORT DATE: Oct 1980
	13. NUMBER OF PAGES: 62 61
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Same	15. SECURITY CLASS. (of this report): UNCLASSIFIED
	15a. DECLASSIFICATION DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer: Frederick D. Schmandt (DCCT)

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Amplifiers
Microwave
High Speed Digital

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Under this program a X-band, 5-watt linear solid state amplifier was designed, fabricated, and tested. The amplifier delivers saturated output power of 10 watt with power gain of 32 dB at 8GHz. For linear amplification, the third order intermodulation distortion of the amplifier is - 32 dBc at 5 watt (two-tone) output power level. The overall DC to RF conversion efficiency is 11% at saturation with total power consumption of 92.5 watt.

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SUMMARY

The objective of this program is to develop an X-Band, 5-Watt, linear solid state communication amplifier for line of sight radio communication with high data transmission efficiency. The amplifier should operate between 7.125 GHz and 8.4 GHz with better than 30 dB gain at rated output power.

During this program, GaAs power FET transistors manufactured by both Fujitsu and MSC (Microwave Semiconductor Corporation) were evaluated. MSC CHIP-PAC GaAs power FETs were chosen for the amplifier design. A 6-stage GaAs FET power amplifier was designed, manufactured, and tested. The amplifier consists of a total number of 17 FET amplifiers with 6 amplifiers parallelly power combined at the final output stage to achieve the required output power. For linear amplification, the amplifier shows 33.6 dB gain with third order intermodulation products better than 32 dB down from the carrier. The amplifier has a noise figure of 12.9 dB at 8 GHz. At saturation, the amplifier delivers 10 watts of output power with DC to RF conversion efficiency equal to 11%.

The X-Band, 5-watt, linear solid state communication amplifier developed under this contract has proven that GaAs Field Effect Transistor amplifiers are definitely a feasible replacement for Traveling Wave Tube Amplifiers in many applications. The linear FET amplifier exceeds TWTA in the area of linearity, AM to PM conversion, and noise figure. The linear FET amplifier's power output and power-added efficiency are competitive with that of a TWTA.

Future effort in the areas of mechanical packaging, temperature compensation, and power supply are required. A complete engineering model should be built and tested to realize an X-Band solid state amplifier for TWTA replacement.

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ILLUSTRATIONS
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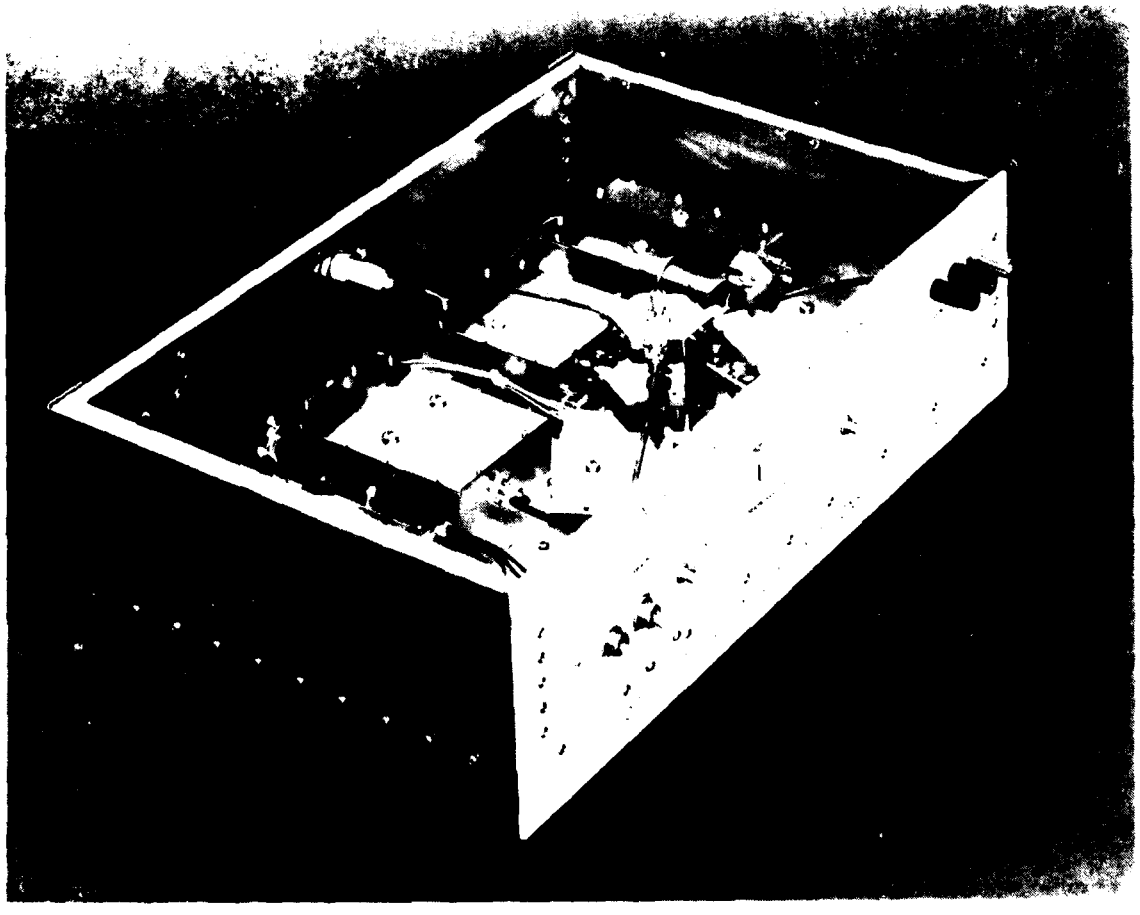
I. INTRODUCTION

The objective of this program is to develop a X-Band, 5-watt, linear solid state amplifier for line of sight radios with high data transmission efficiency. The frequency of operation locates between 7.125 GHz to 8.4 GHz.

During this program, a 6-stage FET amplifier was designed, manufactured, and tested. The amplifier delivers saturated output power of 10 watt with power gain of 32 dB at 8 GHz. For linear amplification, the third order intermodulation distortion of the amplifier is -32 dBc at 5 watt (two-tone) output power level. The overall DC to RF conversion efficiency is 11% at saturation with total power consumption of 92.5 Watt.

Figure 1-1 is a photograph of the complete amplifier. Table 1-1 summarizes the performance of the X-Band, 5-watt linear solid state power amplifier.

RF operating life test is being performed on the completed amplifier. As of 9/12/80, 8903 hours have been accumulated on the amplifier. Out of 17 power FETs, 3 FETs failed during the life test. The failure FETs were replaced and the RF life test program is being continued.



Photograph of the X-Band, 5 watt Linear Solid State Amplifier

Figure 1-1

PARAMETER	LINEAR MODE	SATURATED MODE
RF Power Output	5 Watt	10 Watt
Frequency Band	8 GHz	8 GHz
Gain	33.7 dB	32 dB
Noise Figure	12.8 dB	--
C/IMD (3)	32 dB	12 dB
Spurious Signal	≤ -80 dB	≤ -80 dB
Differential Delay	< 1 ns/14 MHz	< 1 ns/14 MHz
Input and Output VSWR	≤ 1.3:1	1.3:1
AM to PM Conversion	1°/dB	< 3°/dB

PERFORMANCE OF X-BAND, 5-WATT LINEAR SOLID STATE AMPLIFIER

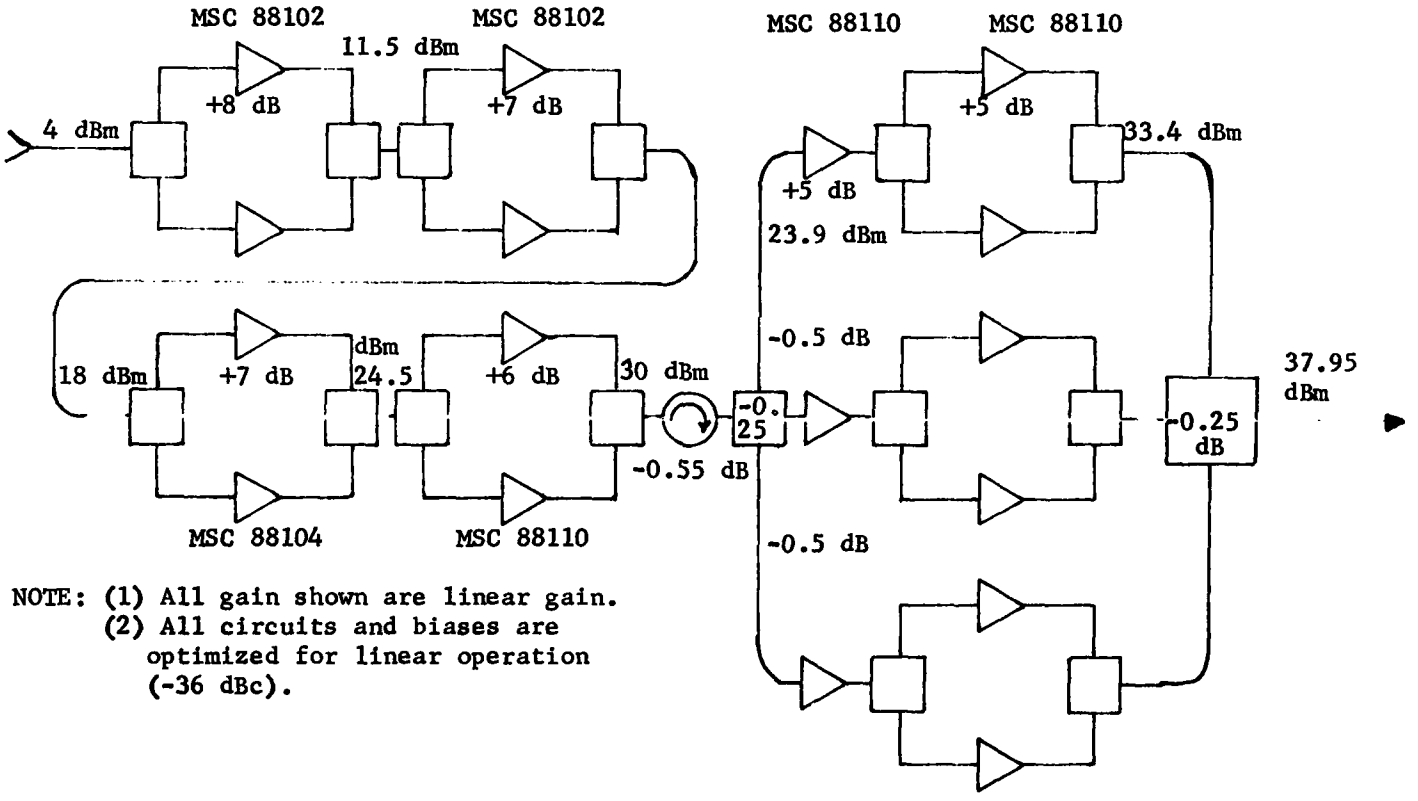
Table 1-1

II. AMPLIFIER DESIGN AND PERFORMANCE

A circuit block diagram of the X-Band, 6-Stage FET Amplifier with input and output power level indicated is shown in Figure 2-1. The 5-watt linear amplifier consists of two cascaded balanced low level drivers, two cascaded balanced high level drivers, and a three-way power combined power amplifier module. Isolator was used in between the high level driver and power amplifier to provide the required interstage isolation. The complete amplifier was packaged in a 19" x 12" x 5" chassis for shelf mounting. The amplifier consists of five individual amplifier modules, power divider, and combiner modules. Figure 2-2 shows the planar modular configuration of the linear solid state amplifier. Individual amplifier stages were built on carriers, and were manufactured and tested separately before final integration.

The active device used in this amplifier is commercially available and is Microwave Semiconductor Corporation's high power field effect transistors MSC 88110, MSC 88104, and MSC 88102. The CHIP-PAC Series GaAs FETs are chosen to minimize the package parasitic effect and optimize the amplifier performance. The manufacturer's data sheet of these power FETs is attached in Appendix 5.1 for reference. Their electrical characteristics are summarized in Table 2.1.

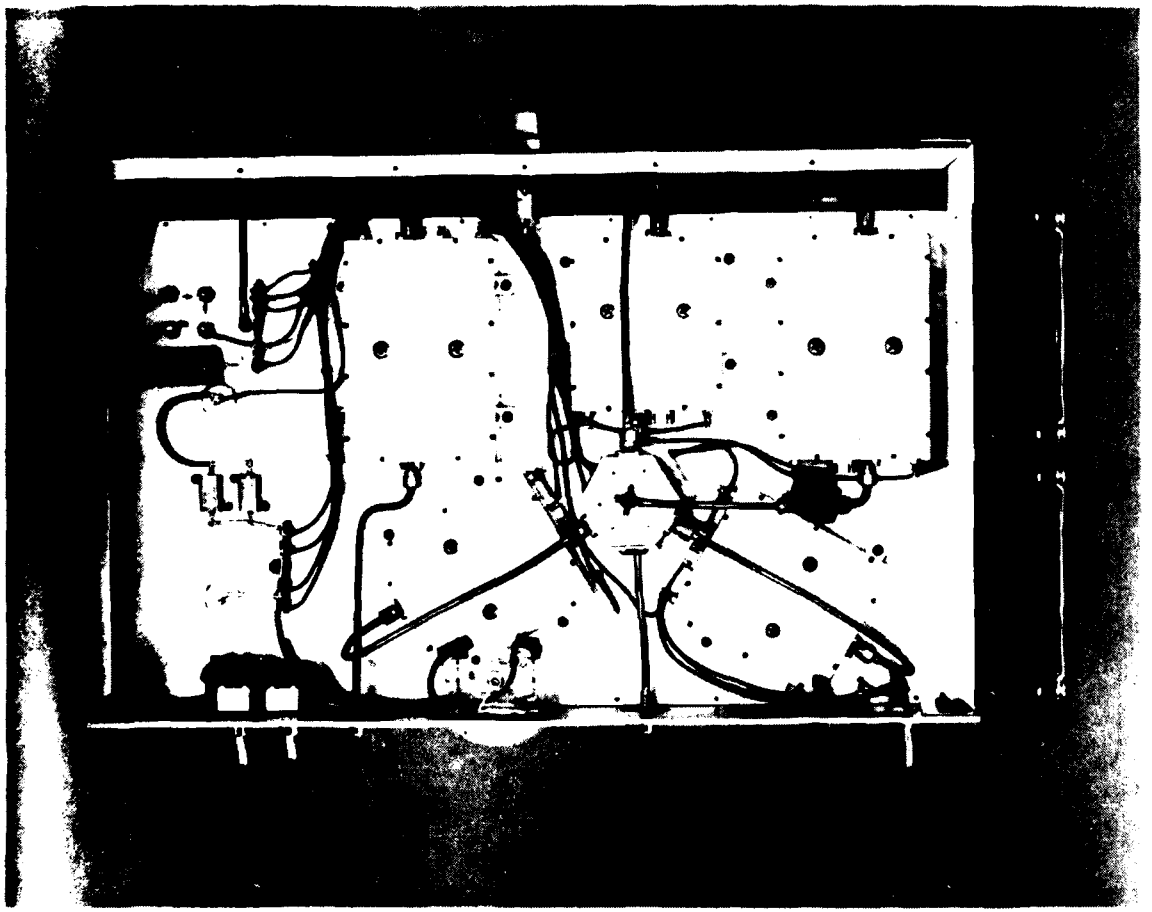
In the design of the single stage, high power, solid state amplifier, the small signal S-parameter of the devices were measured first. The optimum impedance contours for the high power or high linearity operation were then obtained by the method of substitution. Based upon the measurement result, the linear solid state amplifiers were then designed and realized in MIC form on alumina substrate.



NOTE: (1) All gain shown are linear gain.
(2) All circuits and biases are optimized for linear operation (-36 dBc).

Circuit Block Diagram of the X-Band, 5-Watt Linear Solid State Amplifier

Figure 2-1



PLANAR MODULAR CONFIGURATION OF THE LINEAR SOLID STATE AMPLIFIER

Figure 2-2

Model Number	Test Freq. (MHz)	Pout TYP (W)	Pout MIN (W)	PIN (W)	Vds NOM (V)	I_{DSS} NOM (mA)	θ_{CC} TYP (^{o}C/W)	Case Style (Carrier)
MSC 88100	12000	0.060	0.050	0.016	8	90	45	100
MSC 88101	12000	0.200	0.175	0.056	8	150	35	100
MSC 88102	12000	0.400	0.350	0.125	9	300	25	100
MSC 88104	12000	1.000	0.800	0.280	9	700	20	100
MSC 88110	12000	2.000	1.800	0.630	9	1500	10	101

ELECTRICAL CHARACTERISTICS OF MSC MICROWAVE POWER GaAs FETs

Table 2-1

In the following sections, the circuit designs and test results of the individual amplifier stage are discussed in detail.

2.1 Power Combining and Dividing Circuits

Due to the electrical and thermal limitation of the single solid state device, power combination techniques are needed to increase the output power of the solid state amplifier and to meet the specific system requirement. In the X-Band, 5-watt linear solid state amplifier, two different types of power combining and dividing circuits were designed and used: 3 dB interdigitated quadrature coupler and 3-way in-phase power combiner and divider.

2.1.1 3 dB Interdigitated Quadrature Coupler

In the power combining scheme, one of the most important building blocks is the 3 dB quadrature coupler, which can take a variety of forms dependent on the particular application. The quadrature coupler has the unique property that its input impedance remains matched even when its two split power arms are not properly terminated, provided the reflection coefficients in both arms are equal in amplitude and phase. This feature is particularly advantageous when combining wide band amplifiers whose input VSWR general is rather poor at band edge. Besides, by parallel combining two nonlinear amplifiers, their phase distortion will compensate each other, and improve the overall intermodulation product of the amplifier.

Based upon the design equations for the interdigitated couplers, the even and odd mode characteristic impedance for a 3 dB, 4 fingers coupler were calculated to be 176.2 ohm and 52.6 ohm. The design equations are repeated here for completeness.

$$Y_o^2 = \frac{\left[(K-1)\,Y_{oo}^2 + Y_{oo}Y_{oe}\right]\left[(K-1)Y_{oe}^2 + Y_{oo}\,Y_{oe}\right]}{(Y_{oo} + Y_{oe})^2} \qquad (1)$$

$$C = \left[\frac{(K-1)\, Y_{oo}^{\,2} - (K-1)\, Y_{oe}^{\,2}}{(K-1) Y_{oo}^{\,2} + 2\, Y_{oo}\, Y_{oe} + (K-1)\, Y_{oe}^{\,2}} \right]^2 \qquad (2)$$

Where Y_o is the characteristic admittance of the system

K is the number of the interdigitated fingers

C is the desired power coupling coefficient

Y_{oe} is the even mode admittance of the coupled line

Y_{oo} is the odd mode admittance of the coupled line

To minimize the conductor loss, the 3 dB interdigitated quadrature couplers were fabricated on a 1" x 0.5" x 0.025" fused silica substrate with Mo (100 A^{o}) - Au (150 microinch) metalization. The coupler finger spacing is 0.015" $\pm$ 0.00015" after etching. The 3 dB coupler shows 0.33 dB insertion loss with better than 18 dB isolation at 8 GHz. The frequency response of the couplers is shown in Figure 2-3.

2.1.2 3-Way In-Phase Combiner and Splitter

The final combiner used for the X-Band, 5 watt solid state power amplifier is a 3-way balanced Wilkinson type combiner in a highly flexible configuration.

It is constructed in microstrip form on Teflon fiberglass of dielectric constant of 2.3. The total loss, including connectors is 0.25 dB across a 1 GHz bandwidth. Isolation is in excess of 28 dB between all input ports, and VSWR is 1.15:1 maximum.

The test results of the 3-way in-phase combiner is shown in Figure 2-4. Across a 500 MHz band of interest, isolation is 30 dB and VSWR is 1.1:1. High isolation is maintained by using half-wave transmission lines to the isolation resistors. Pict-

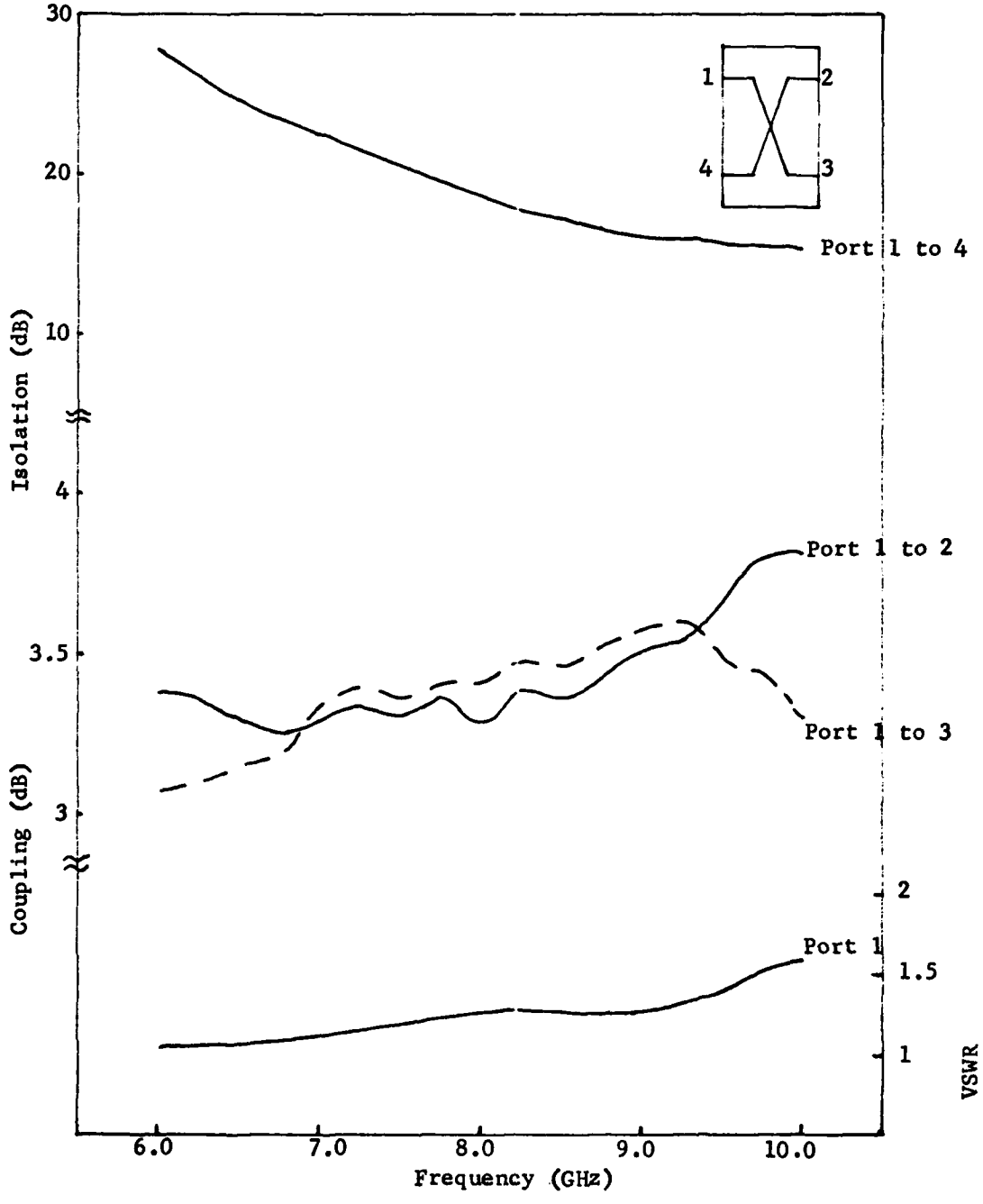


Figure 2-3 Performance of the 3-dB Interdigitated Coupler

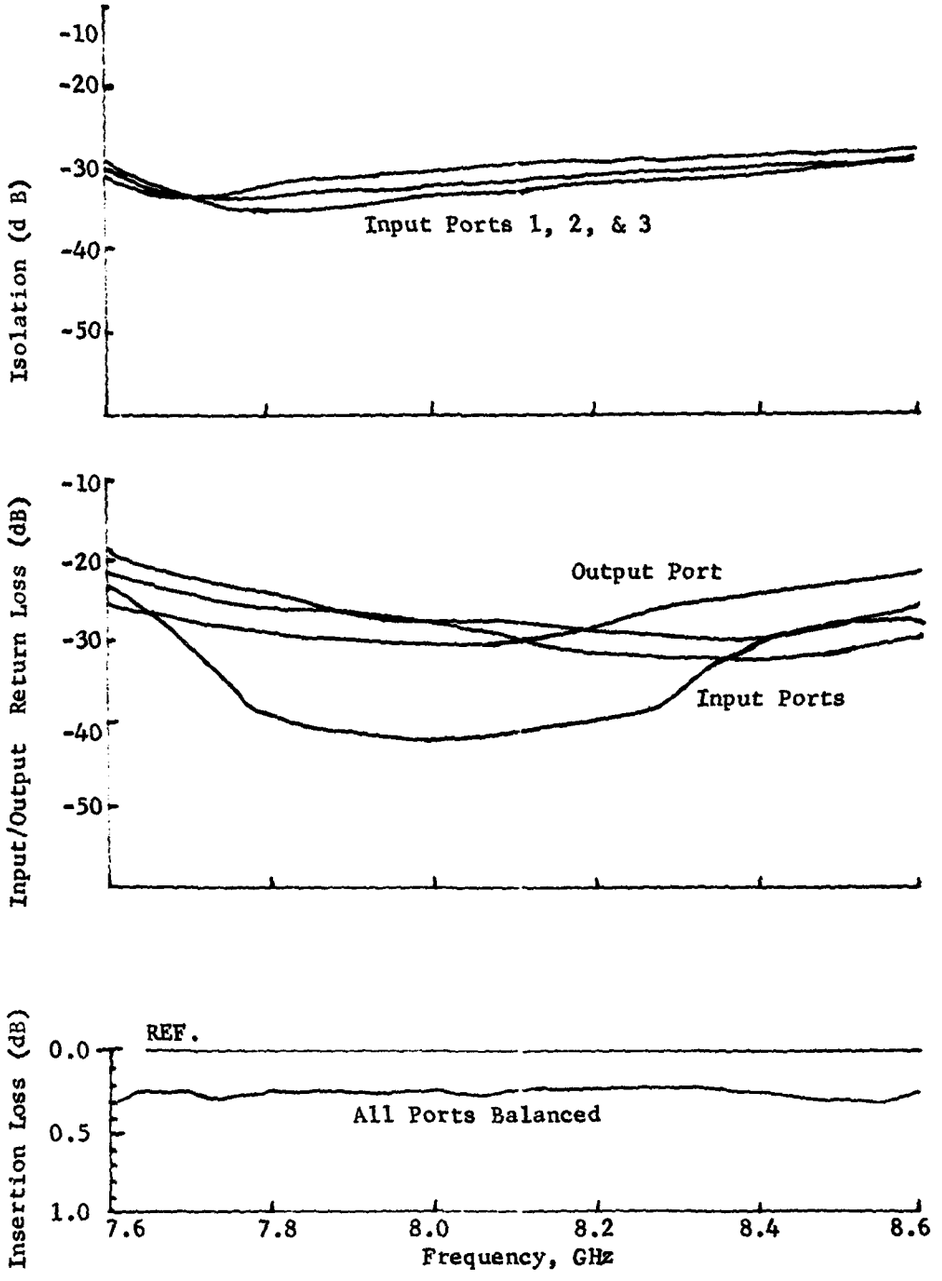


Figure 2-4 Performance of the X-Band, 3-Way In-Phase Power Combiner

ures of this combiner is shown in Figures 2-5(a) and 2-5(b).

2.2 Low Level Driver Amplifier

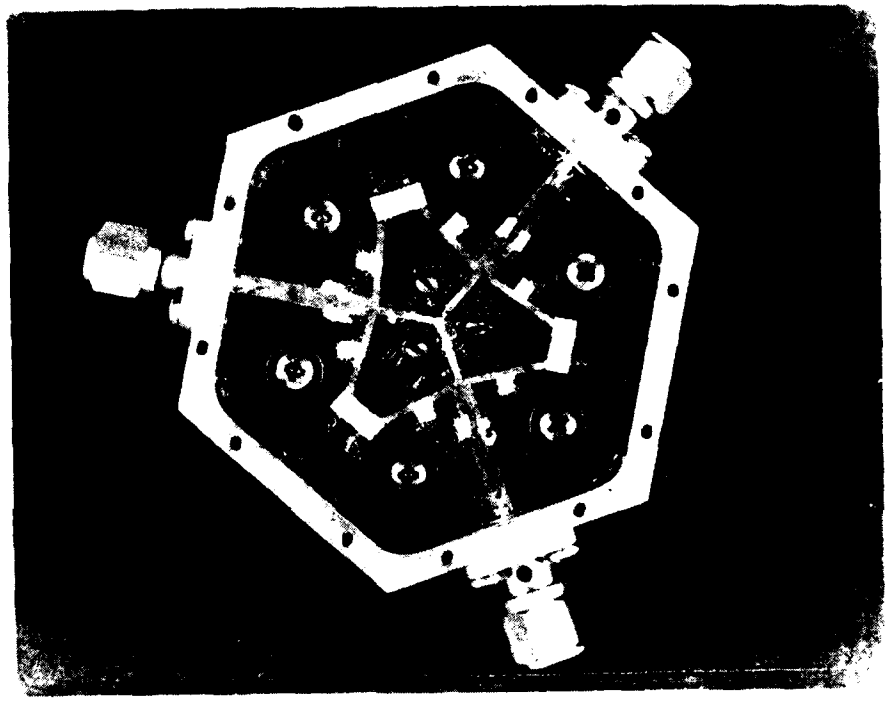
The low level driver amplifier consists of two parallel MSC 88102 FET amplifiers and four 3 dB interdigitated couplers. Each FET amplifier was individually tested for optimum DC biasing and RF circuit matching. Figure 2-6 shows the basic amplifier carrier. The input and output matching circuits were constructed on 1" x 2" x 0.025" alumina substrate with Cr-Cu-Au metalization. After individual testing, the amplifiers and couplers are then mounted into the chassis for integration test. Figure 2-7 is a photograph of the low level driver amplifier.

With drain bias voltage at -10 volt and gate power supply at -5 volt, the low level driver amplifier shows 14 dB gain. Figure 2-8 is an oscilloscope photograph of the frequency response of the amplifier. Under two-tone intermodulation test, the amplifier shows C/IMD (3) better than 44 dB at 4 dBm of input power (sum of both tone signals).

2.3 High Level Driver Amplifier

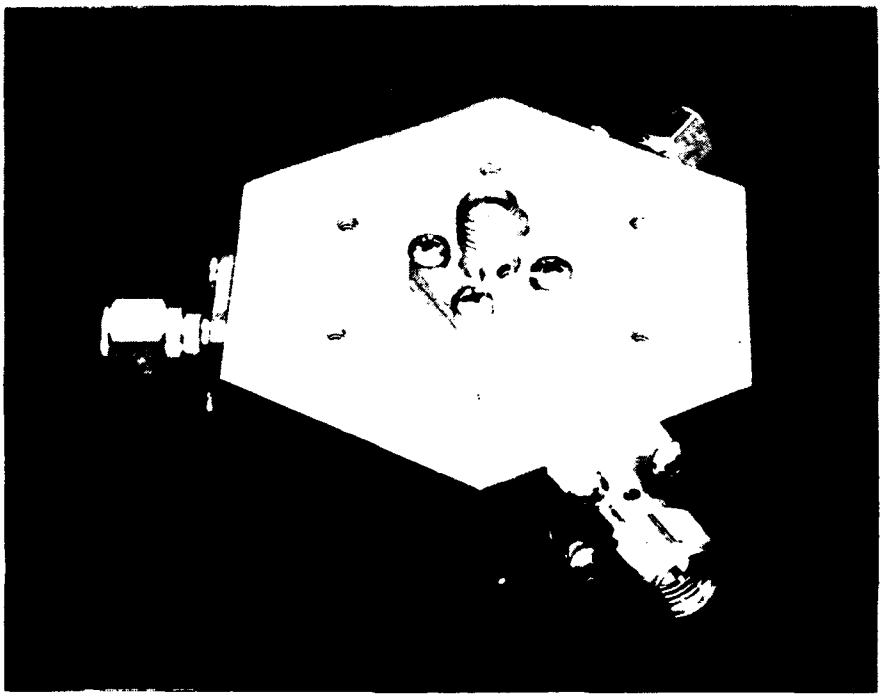
The mechanical construction of the high level driver amplifier is similar to the low level driver amplifier. The high level driver amplifier consists of a parallel combined MSC 88104 and a parallel combined MSC 88110. Parallel combining of GaAs FET with quadrature hybrid improves device to device isolation, minimizes device to device variation problems, and makes the module integration task easier. Figure 2-9 is the circuit block diagram of the high level driver amplifier.

Figure 2-10 shows the two-tone intermodulation test data of high level driver amplifier. With 18 dBm input power, the amplifier delivers 30 dBm of output power with C/IMD (3) better than 30



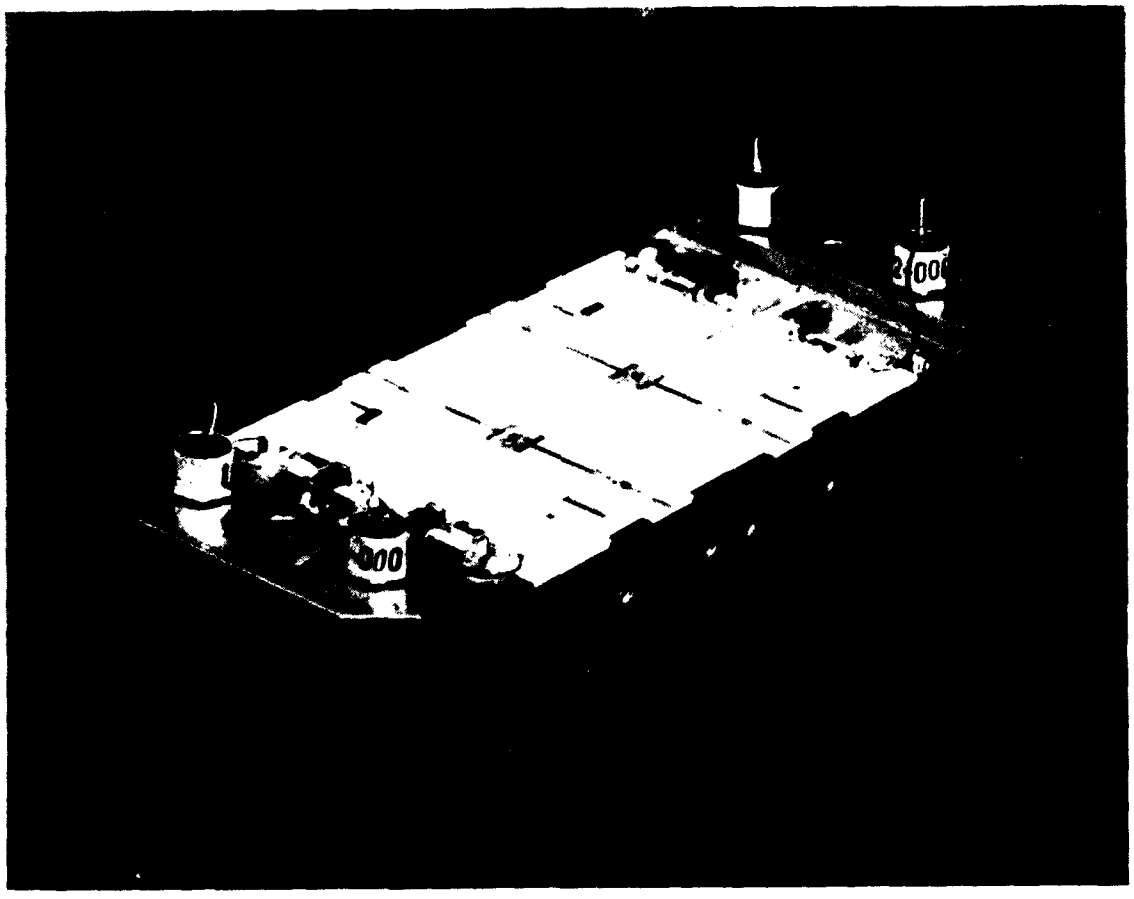
3-Way In-Phase Power Combinder Circuit

Figure 2-5(a)



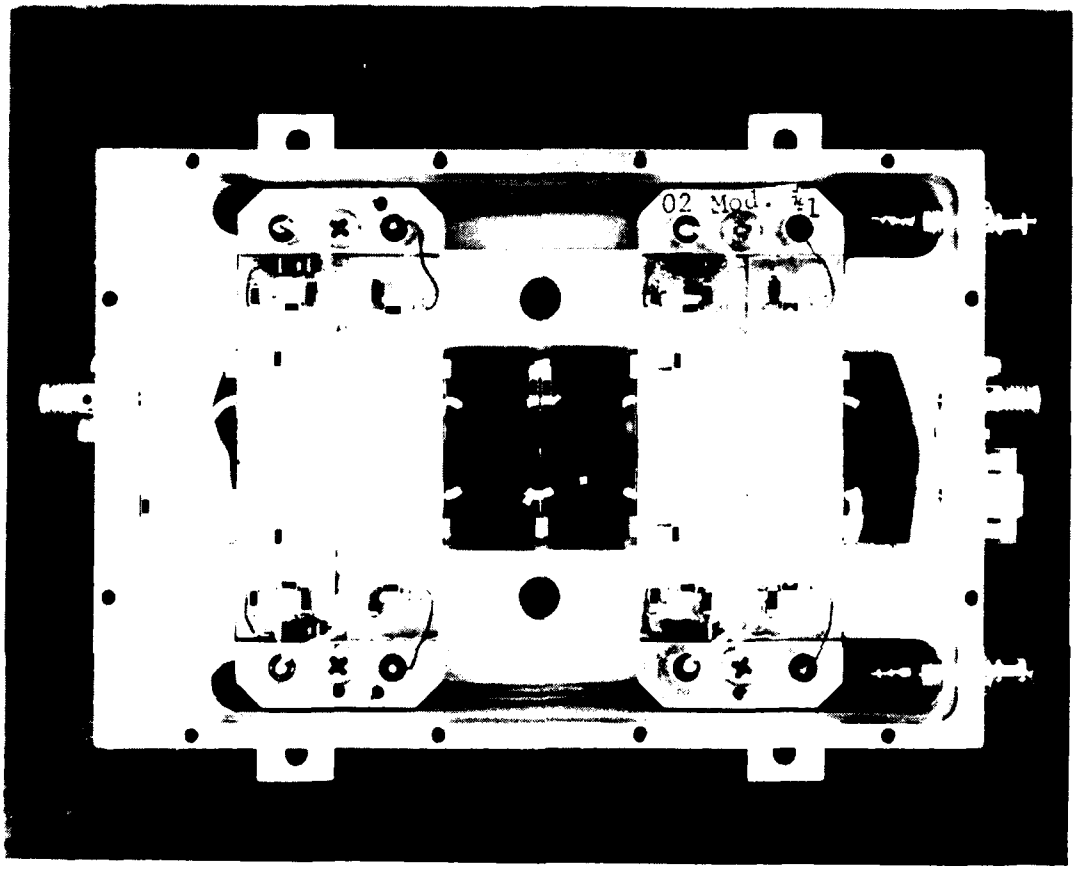
3-Way In-Phase Power Combiner Chassis

Figure 2-5(b)



PHOTOGRAPH OF THE BASIC FET AMPLIFIER CARRIER

Figure 2-6



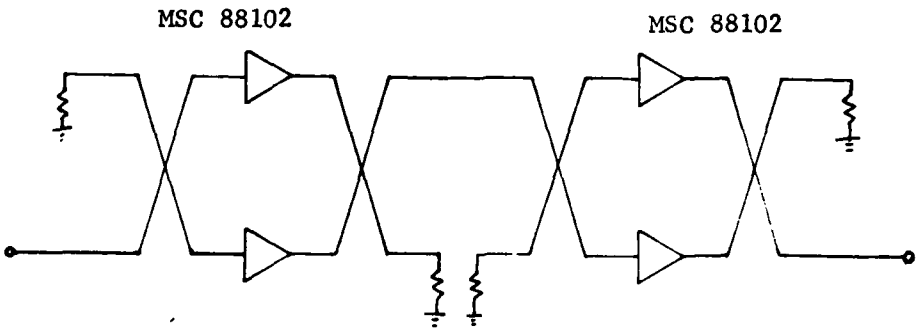
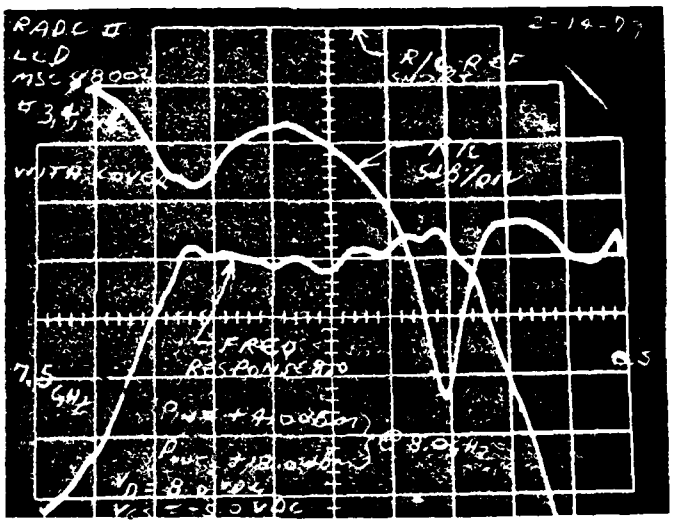


Figure 2-7 Photograph of the Low Level Driver Amplifier



FREQUENCY RESPONSE OF THE LOW LEVEL DRIVER AMPLIFIER

Figure 2-8

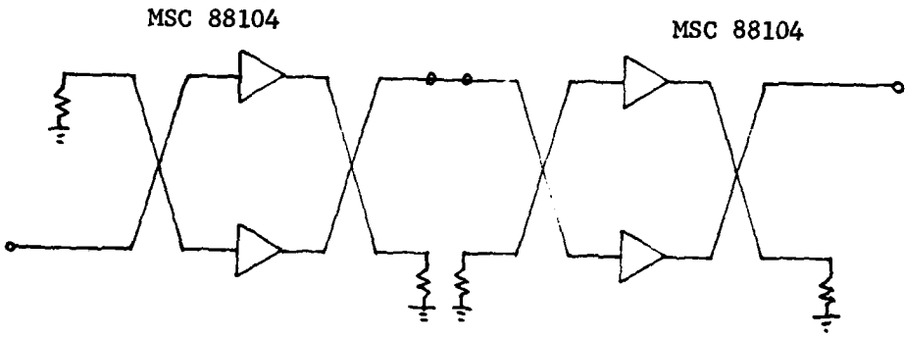
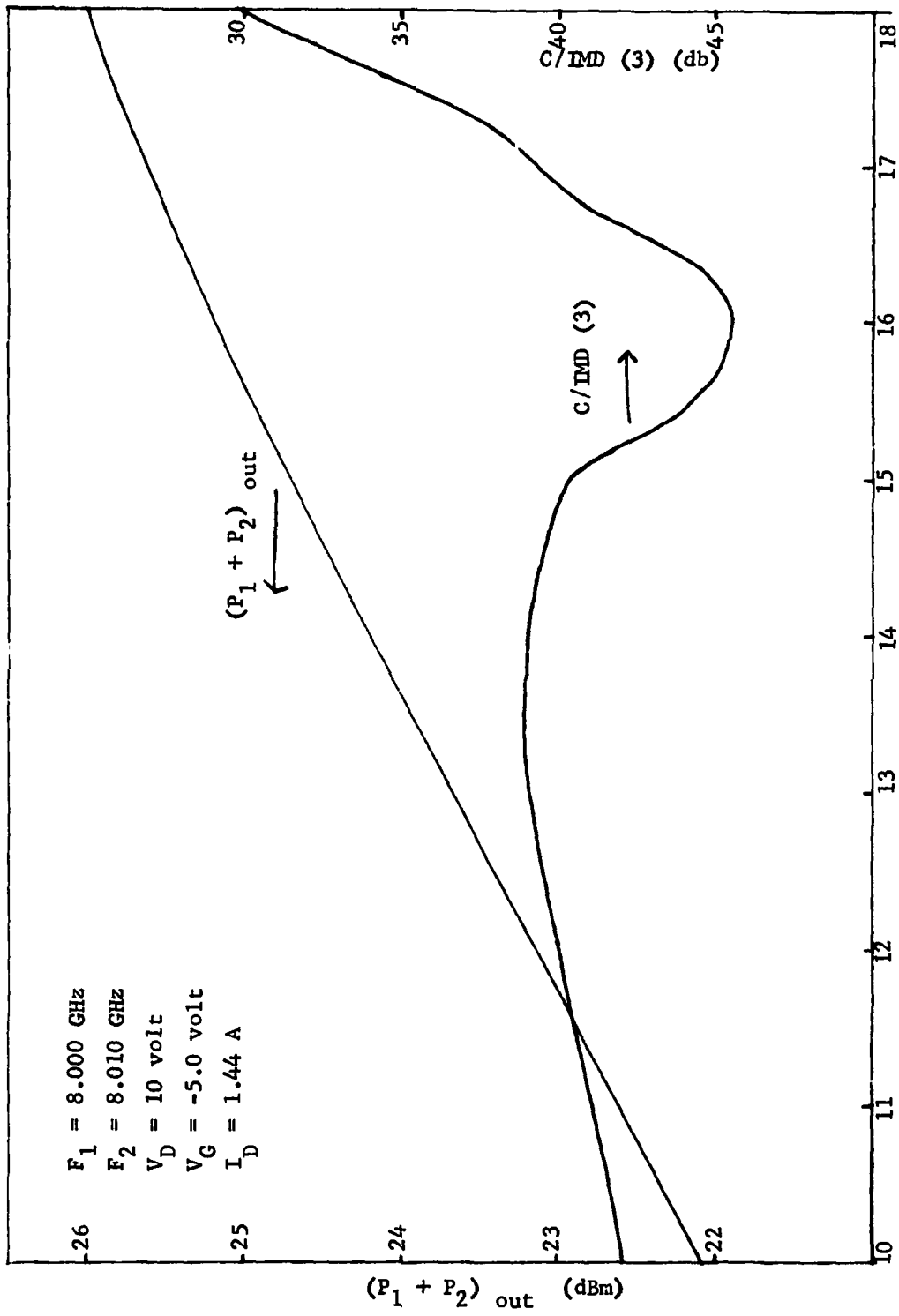


Figure 2-9. Circuit Block Diagram of the High Level Driver Amplifier



Two-Tone Intermodulation Measurement of High Level Driver Amplifier.

Figure 2-10

dB. Figure 2-11 is the frequency response of the high level driver amplifier.

2.4 Power Amplifier Module

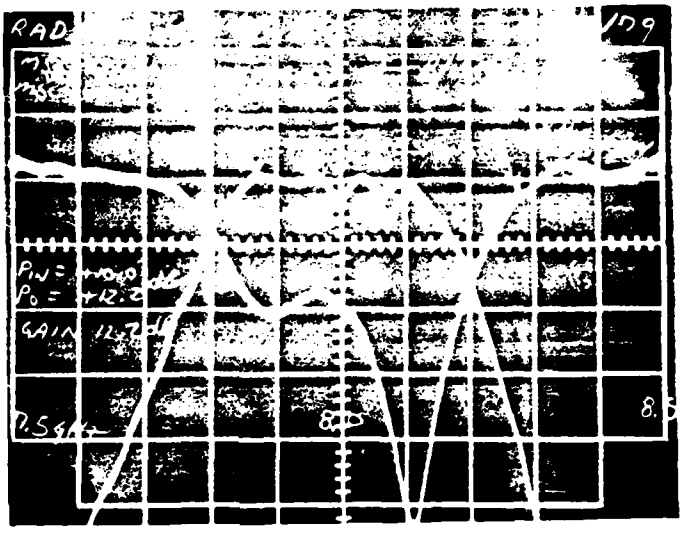
The power amplifier module uses two MSC 88110 FETs parallel combined at output, and driven by a single stage MSC 88110. Figure 2-12 shows the circuit block diagram and the photograph of the power amplifier module. All the impedance matching networks are designed on 1" x 2" x 0.025" alumina substrates using computer optimization. Tuning is done with tabs added to the traces as required. The pairs of amplifiers are tuned as pairs on "drop-in" carriers to integrate with the 3 dB interdigitated couplers. Three different solder melt temperature solders along with wire bonding and inter-connect stress relief loops between substrates are utilized in the module fabrication to prevent thermal stress failures.

Extreme care was taken in the DC bias techniques to prevent oscillation and circuit losses. Gate and drain bias circuits are shown in Figure 2-12a. All components are on MIC in chip form with the exception of the feed-through RFI filter. All 3 power amplifier modules are of the same mechanical construction to minimize manufacturing costs.

Figure 2-13 shows the typical frequency response of the power amplifier module #3. With 23.25 dBm of input power, the #3 power amplifier module delivers 32.95 dBm of output power, with C/IMD (3) equal to 40 dB. Table 2-2 summarizes the performance of the three power amplifier modules at various power levels.

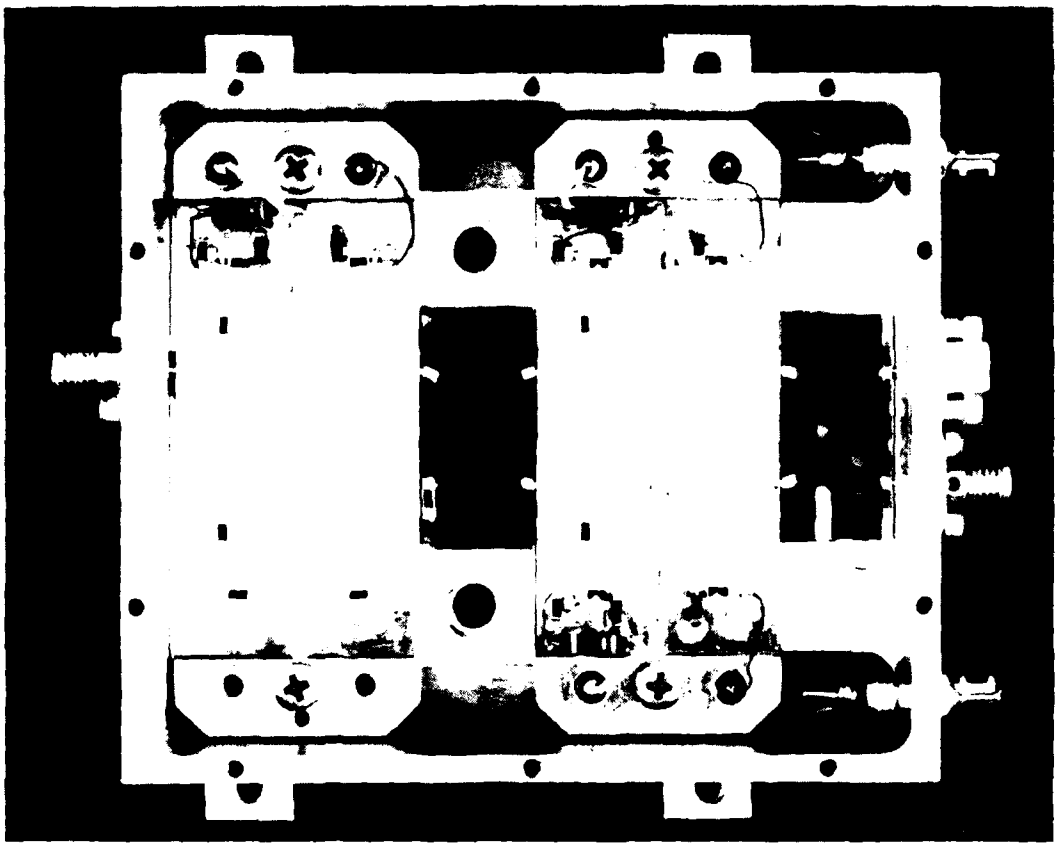
2.5 Mechanical Design

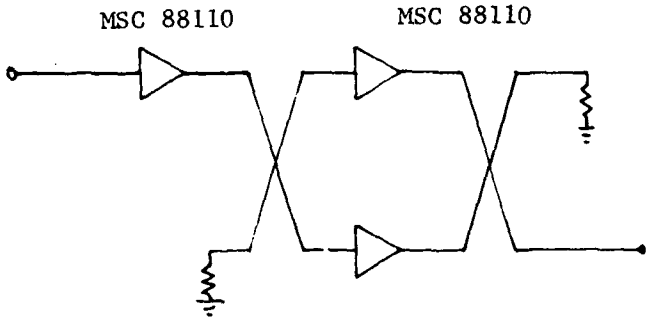
The individual single stage modules were mounted on flat aluminum sub-chassis base plates to form multistage modules. The sub-



FREQUENCY RESPONSE OF THE HIGH LEVEL DRIVER AMPLIFIER

Figure 2-11





PHOTOGRAPH OF THE POWER AMPLIFIER MODULE

Figure 2-12

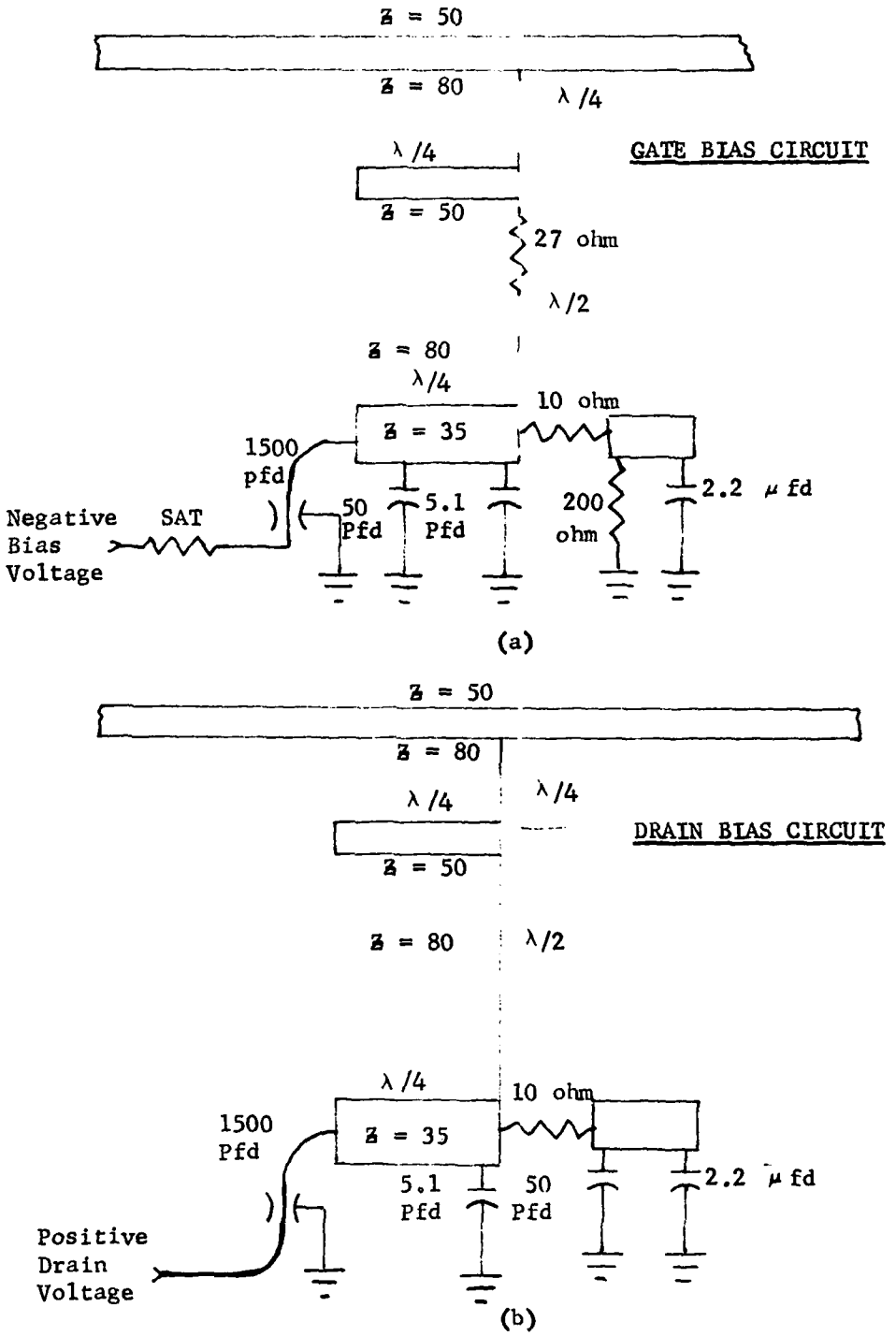
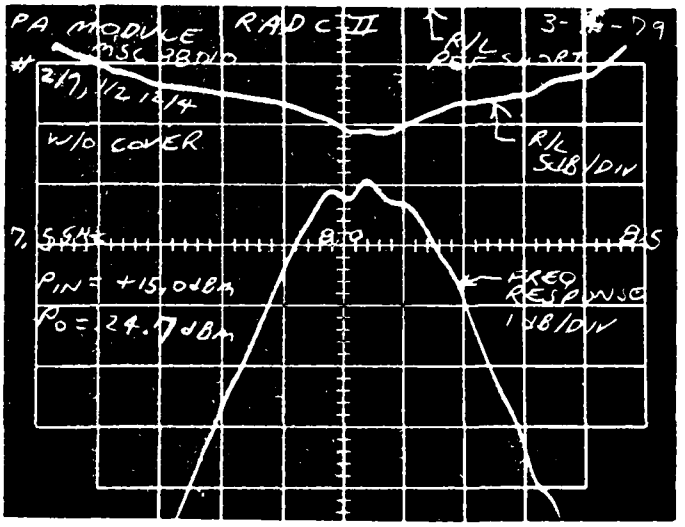


Figure 2-12a. Bias Circuitry of the FET Amplifiers



FREQUENCY RESPONSE OF THE POWER AMPLIFIER MODULE #3

Figure 2-13

Parameters Pin (dBm)	Module #1		Module #2		Module #3	
	Pout (dBm)	C/IMD (3) (dB)	Pout (dBm)	C/IMD (3) (dB)	Pout (dBm)	C/IMD (3) (dB)
15	24.1	44.5	24.6	48	24.7	52
20	29.1	37	29.6	38	29.76	44
23.25	32.15	30	32.65	34	32.95	40

TWO-TONE INTERMODULATION TEST DATA OF POWER AMPLIFIER MODULES

Table 2-2

chassis base plates were in turn bolted down to a heavy aluminum heat-sink. The overall size of the complete amplifier measures 19 inches wide, 12 inches deep, and 5 inches high. Long lengths of .141 semi-rigid cable were used between modules to minimize the power combining losses. Cooling fans were installed on the side of the chassis to remove the heat generated by the power FETs.

The power conditioning circuit was incorporated in the amplifier. Zener diodes were used to prevent accidental overvoltage applied to the FET terminal. Figure 2-14 is the schematic diagram of the power conditioning circuit.

The picture in Figure 2-15 shows an isometric view of the entire amplifier with its top cover removed. The picture in Figure 2-16 shows the front panel view of the amplifier. The picture in Figure 2-17 is top view of the completed amplifier.

2.6 Amplifier Integration

The amplifier integration starts with three power amplifier modules. Due to the symmetrical design of the 3-way power dividing and combining circuits, the phase shift introduced by the cables and power amplifier modules is extremely critical. Different combinations of cables and power amplifier modules were measured and matched on the HP 8542B automatic network analyzer to achieve phase balance between three power amplifier modules to within 10 degrees.

The low level driver and high level driver were integrated next. Figure 2-18 shows the frequency response of the cascaded low level driver and high level driver. Figure 18a is the two-tone intermodulation test result.

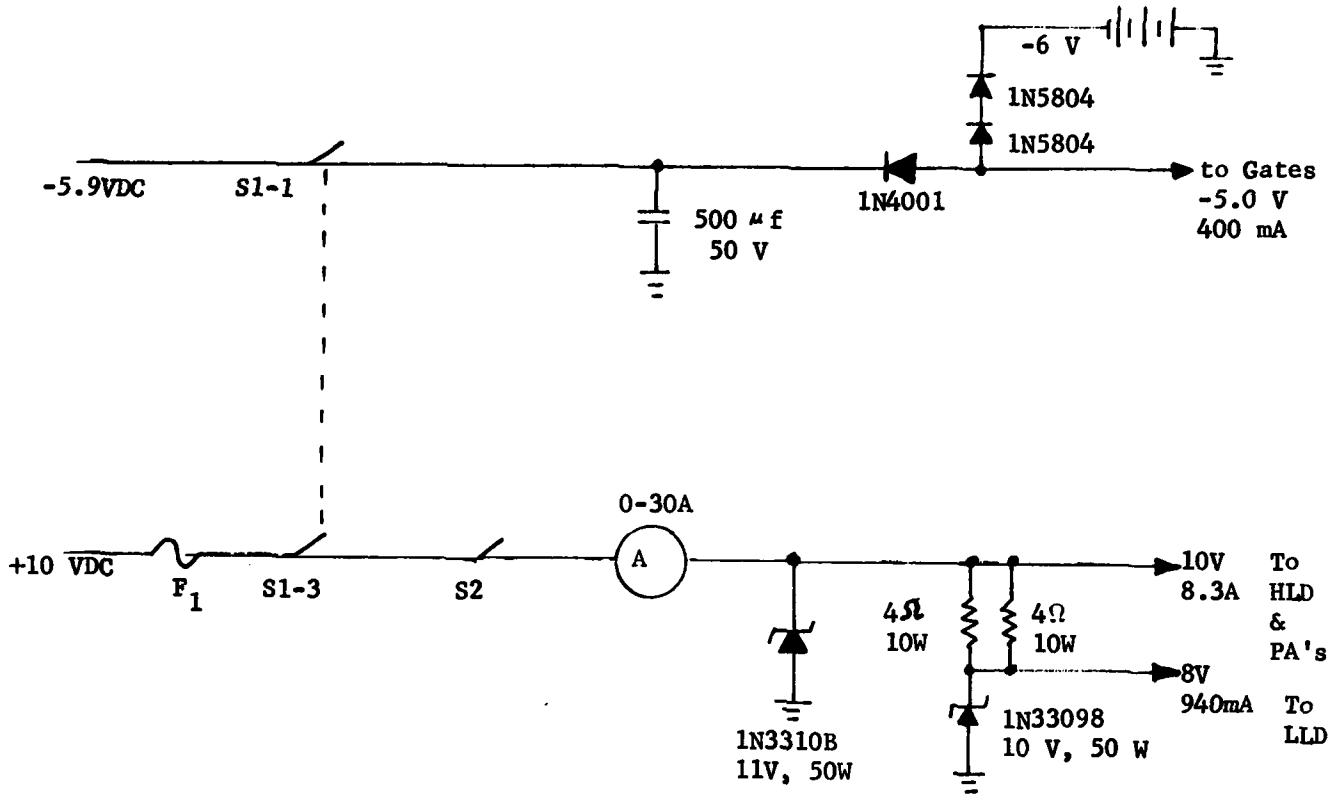
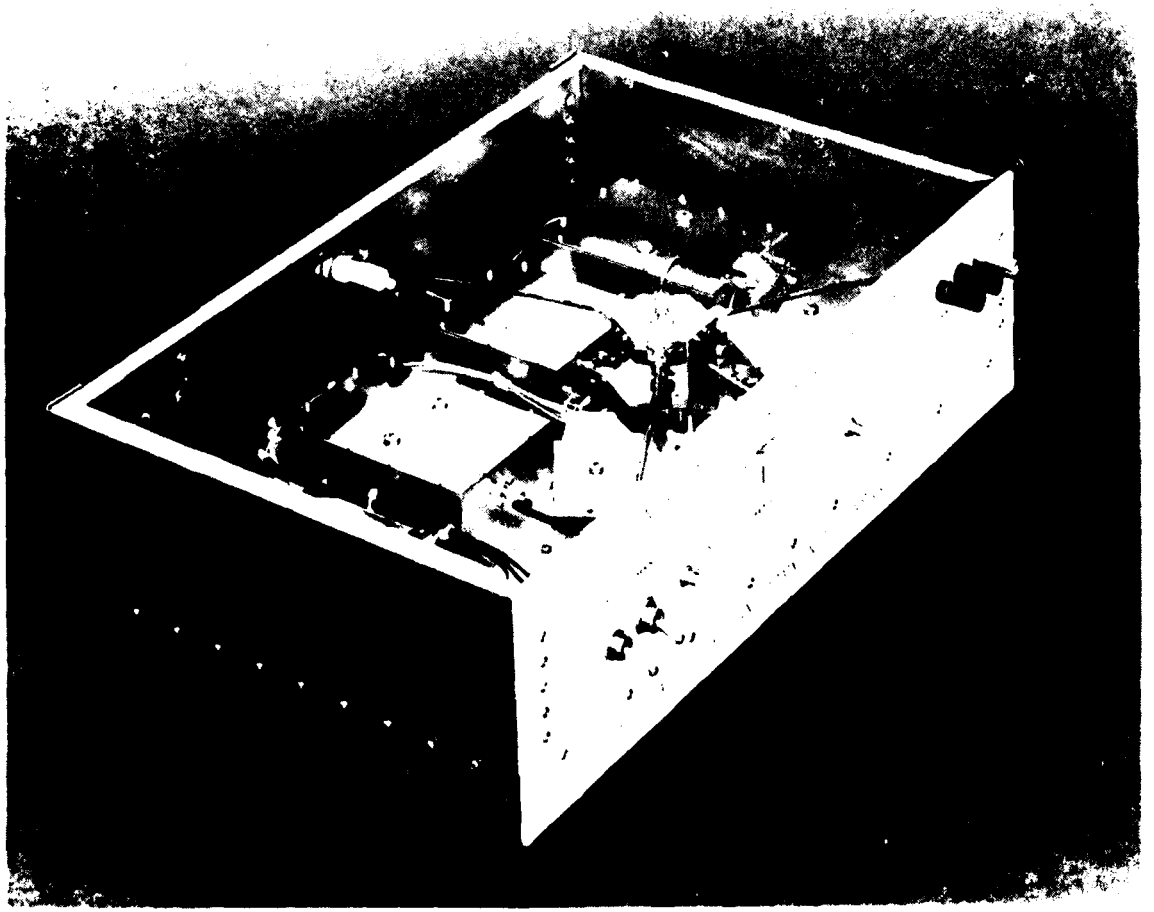
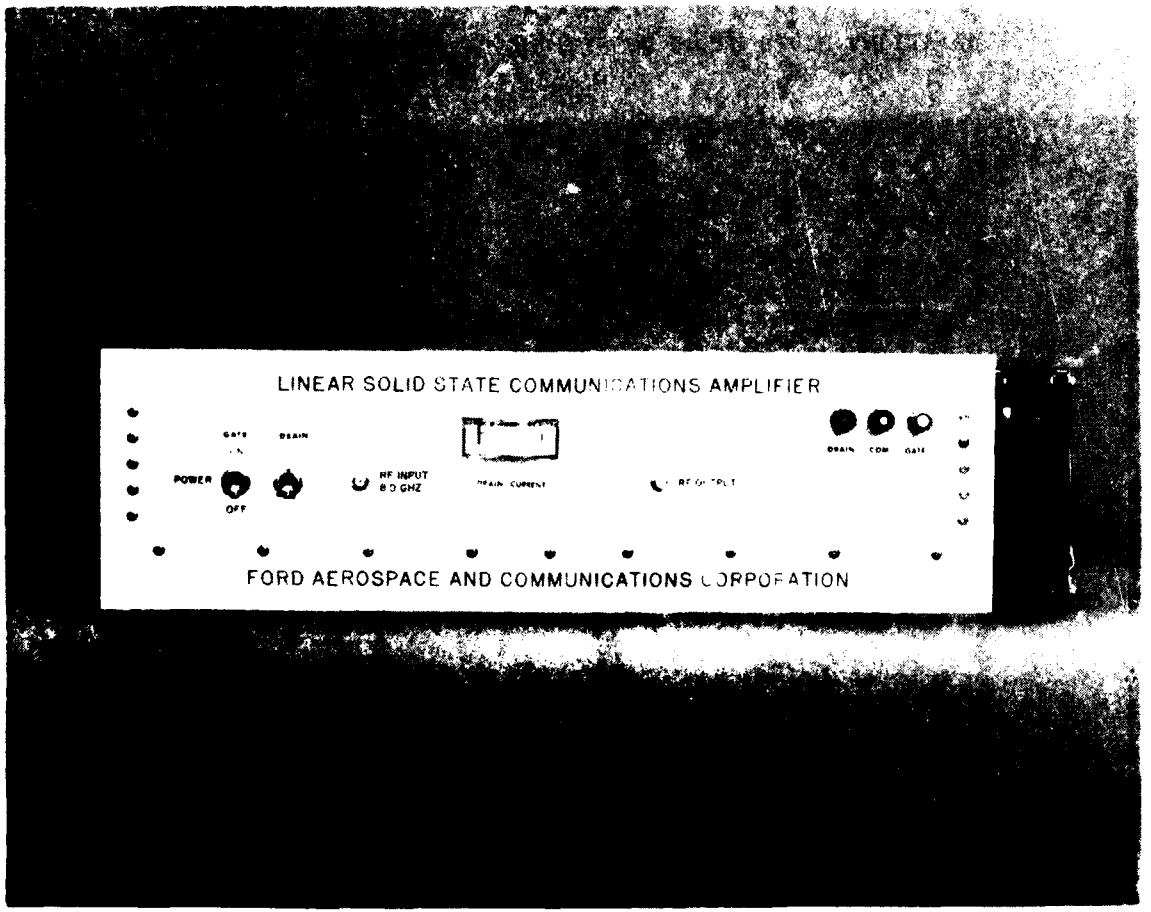


Figure 2-14. Schematic Diagram of the Power Conditioning Circuit



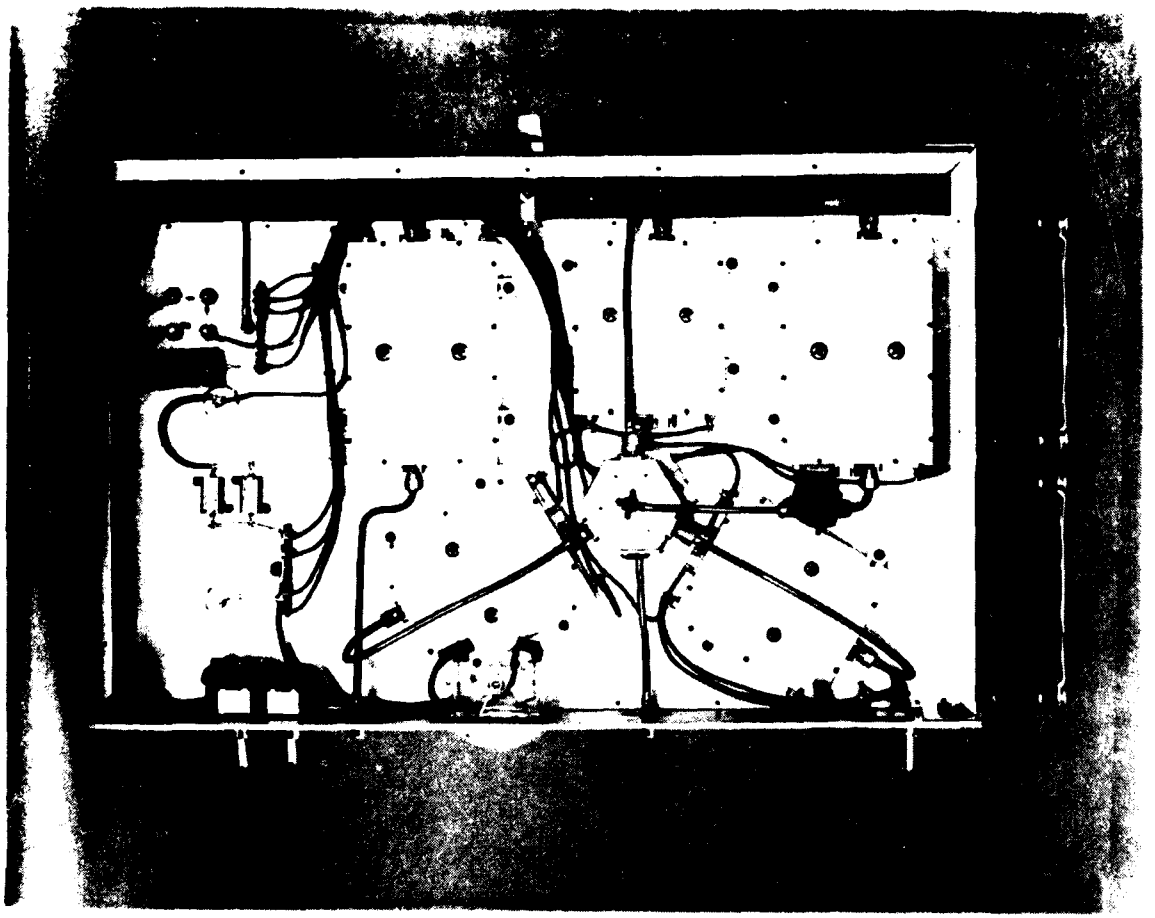
ISOMETRIC VIEW OF THE X-BAND, LINEAR SOLID STATE AMPLIFIER

Figure 2-15



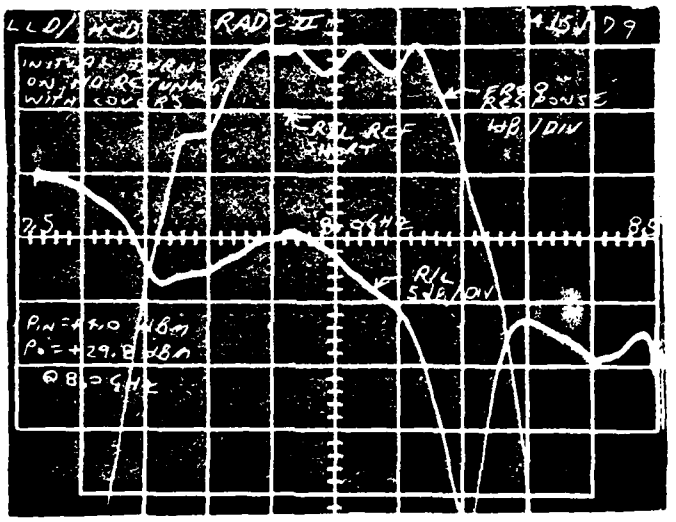
FRONT PANEL VIEW OF THE X-BAND LINEAR SOLID STATE AMPLIFIER

Figure 2-16



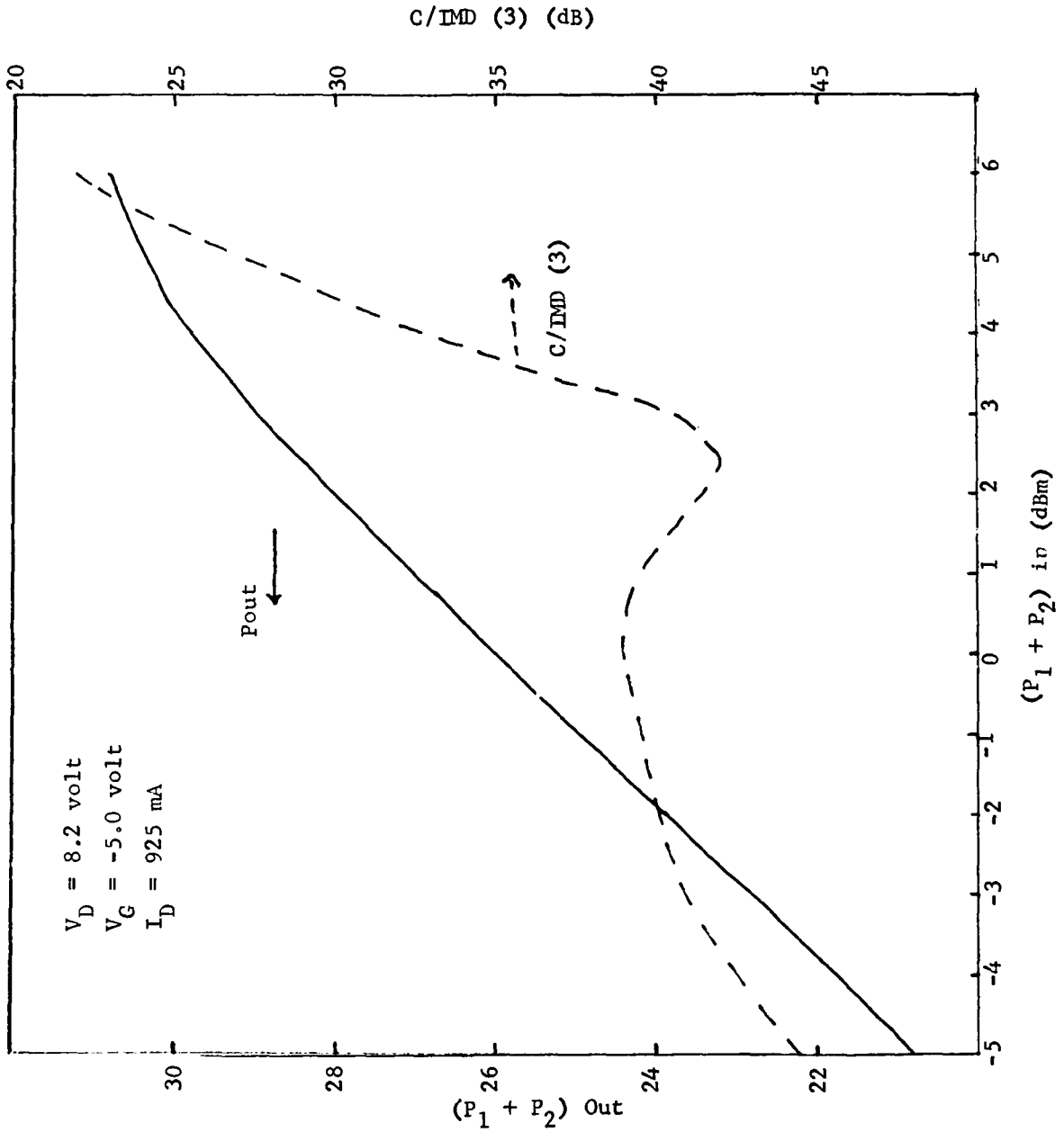
TOP VIEW OF THE X-BAND, LINEAR SOLID STATE AMPLIFIER

Figure 2-17



FREQUENCY RESPONSE OF THE CASCADED LOW LEVEL DRIVER AND HIGH LEVEL DRIVER

Figure 2-18



Two-Tone Intermodulation Test of the Cascaded Low Level Driver and High Level Driver

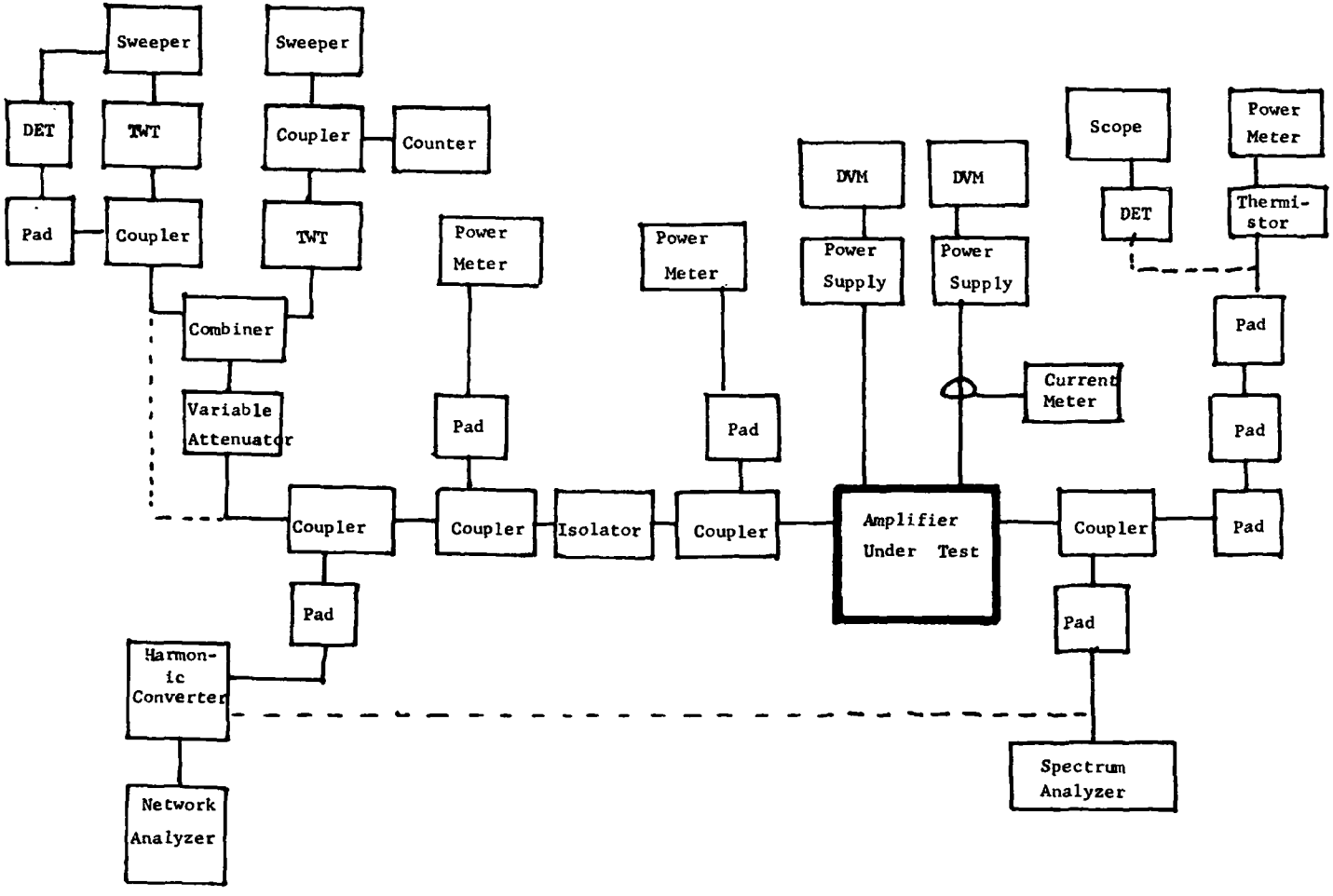
Figure 2-18a

2.7 Final Test Results

All the test data present in this section is for the entire power amplifier after final integration. The general test set-up is shown in Figure 2-19. The first curve is the RF power input vs RF power output. The transfer characteristics of the amplifier is shown in Figure 2-20. At 1 dB compression point, the amplifier delivers 39.95 dBm of output power with 32.7 dB gain. The second harmonic contents of the amplifier is shown on the same graph. At saturation, the maximum 2nd harmonic content is -25.5 dBc. With the amplifier turn off, the cold insertion loss of the amplifier is 83 dB at 8 GHz. The overall phase shift of the amplifier is depicted in Figure 2-21. The amplifier shows less than 10 degree of phase shift with AM/PM conversion coefficient better than 3 degree/dB. The maximum power consumption of the amplifier is 92.5 watt.

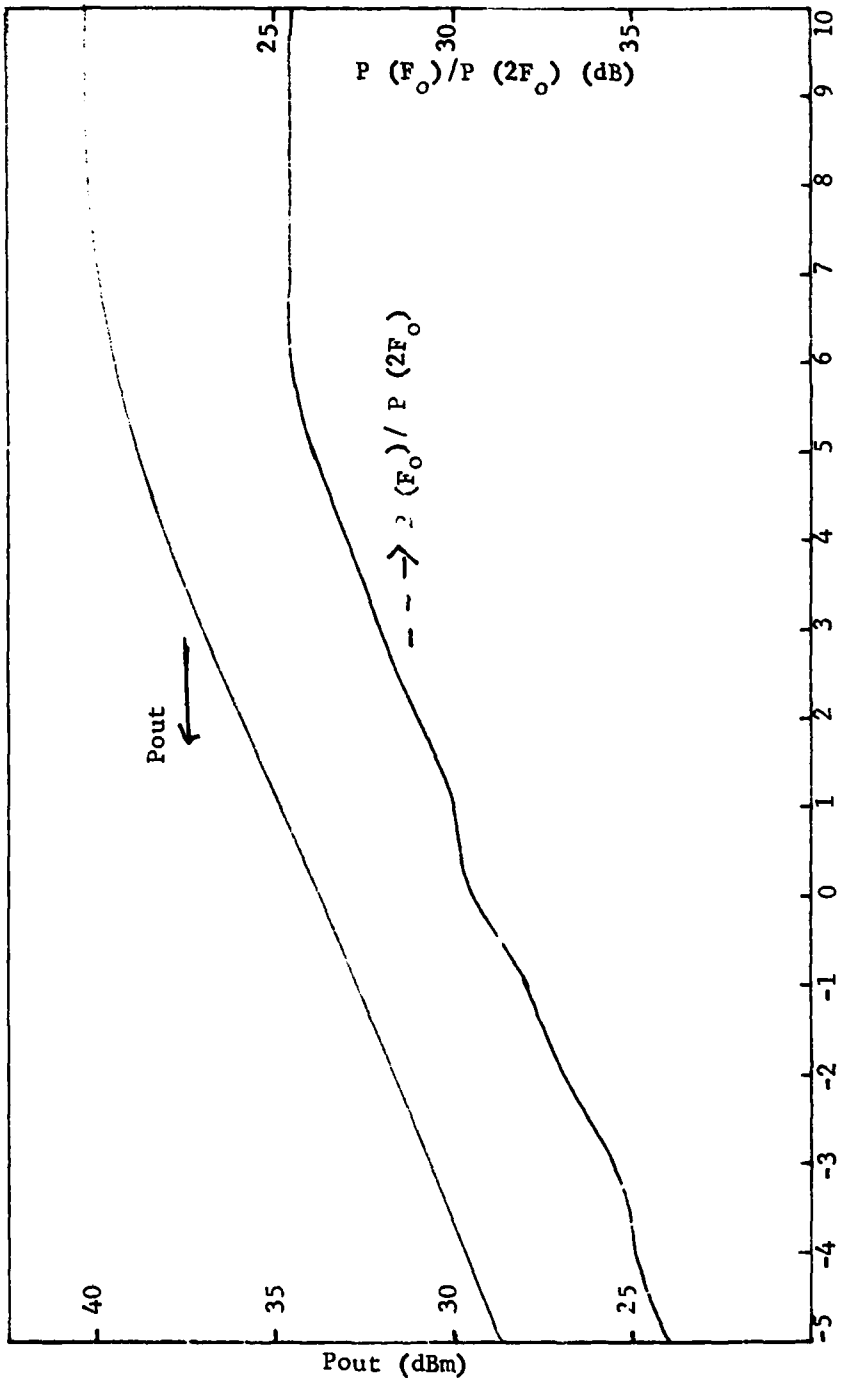
Figure 2-22 shows the frequency response of amplifier and group delay of the amplifier under small signal condition. The amplifier bandwidth is 350 MHz with maximum group delay of 11 nanoseconds.

The next curve, Figure 2-23, displays the intermodulation distorsion versus RF input power under two signal test condition. The plotted C/IMD (3) is each of the third order product to each of the signal. The intermodulation distorsion at 8 GHz is -32 dBc at required 5 watt power output level. The plateau that occurs at -32 dBc C/IMD (3) is a result of circuit tuning and optimizing of the FET biasing for linear operation at given power level. Spurious outputs of amplifier were searched from DC to 18 GHz. No spurious was found within 80 dB of the carrier output power.



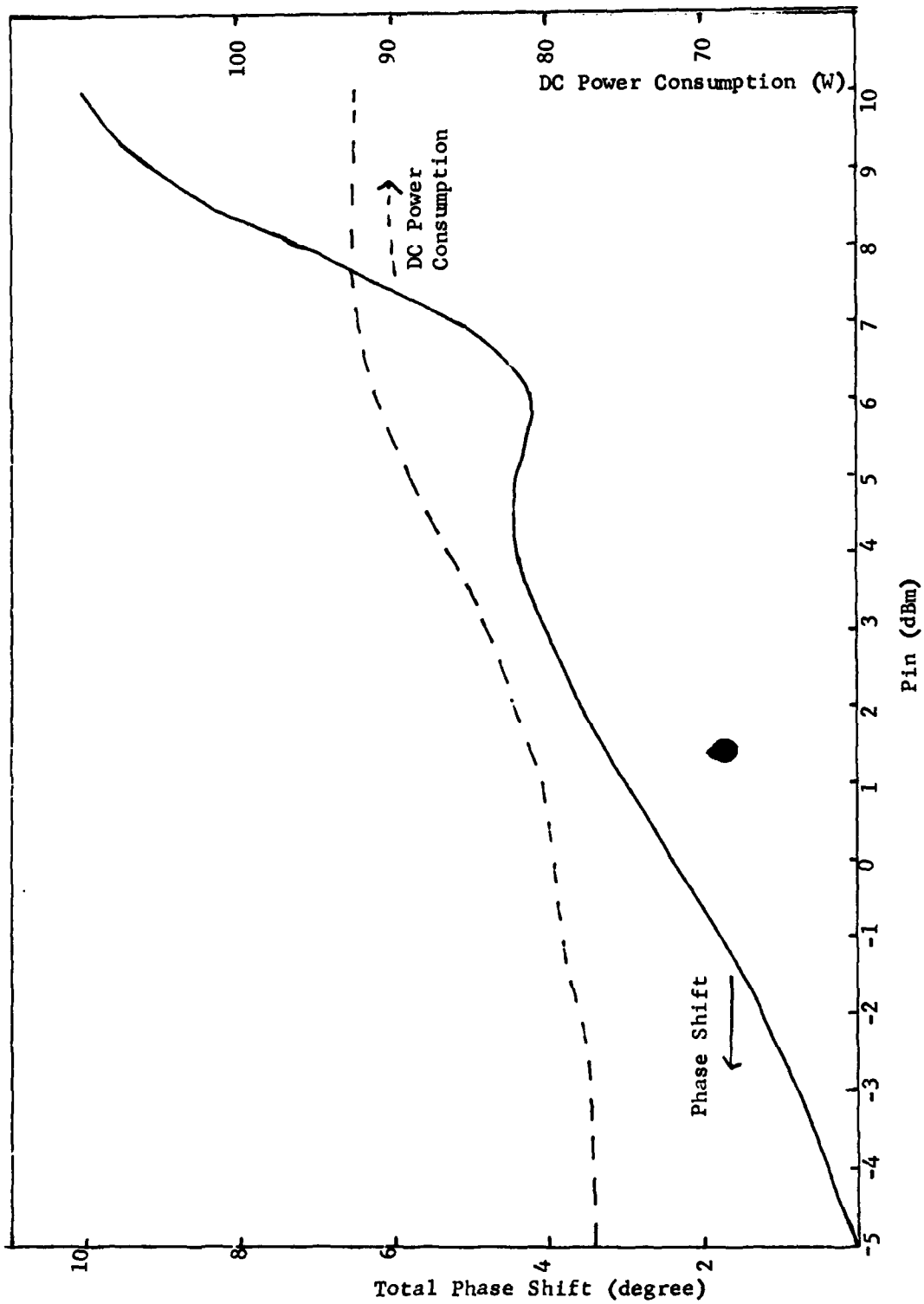
GENERAL TEST SET-UP FOR THE RADC AMPLIFIER

Figure 2-19



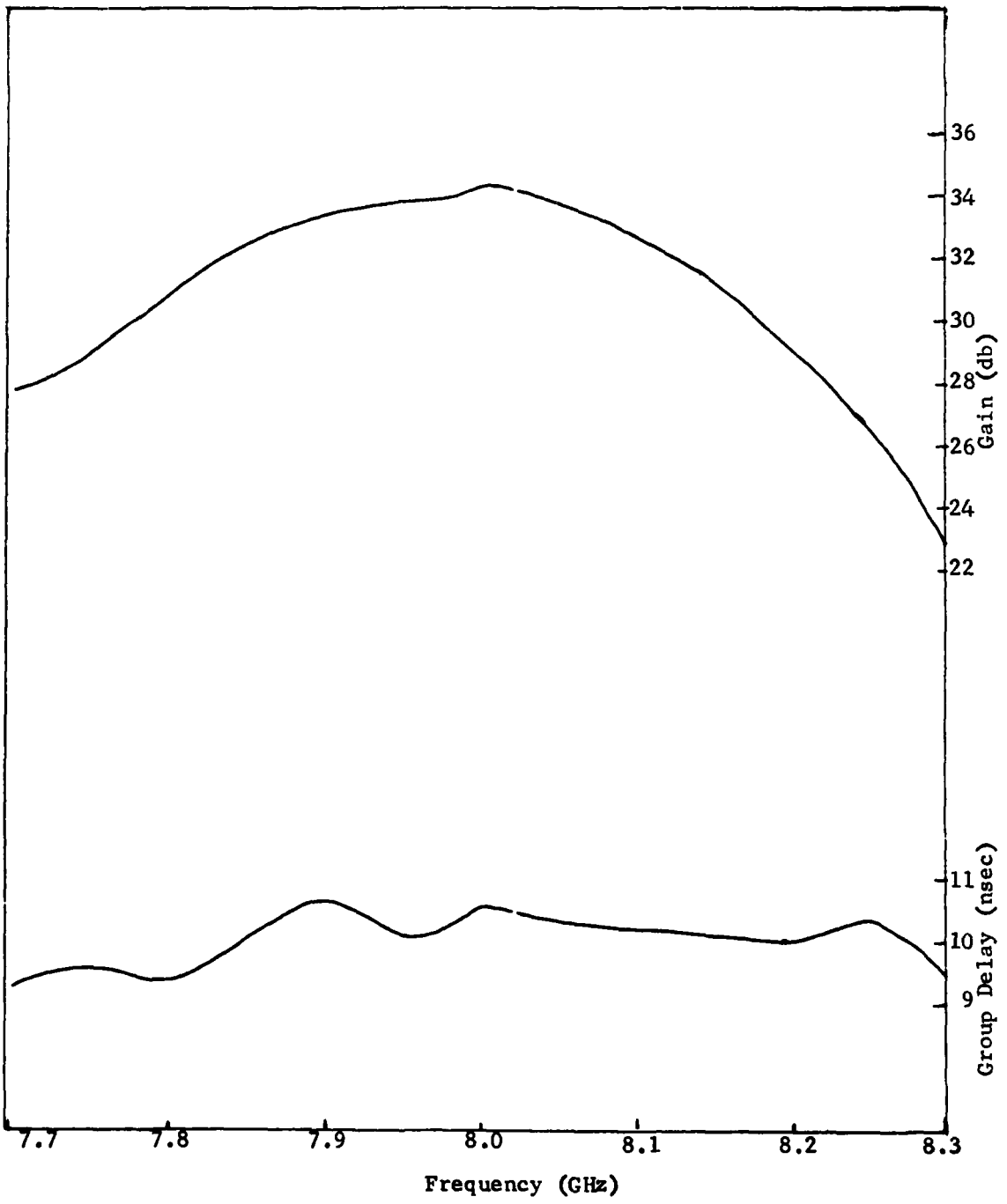
Power Transfer Function of the X-Band Linear Solid State Power Amplifier and its Output Second Harmonic Content

Figure 2-20



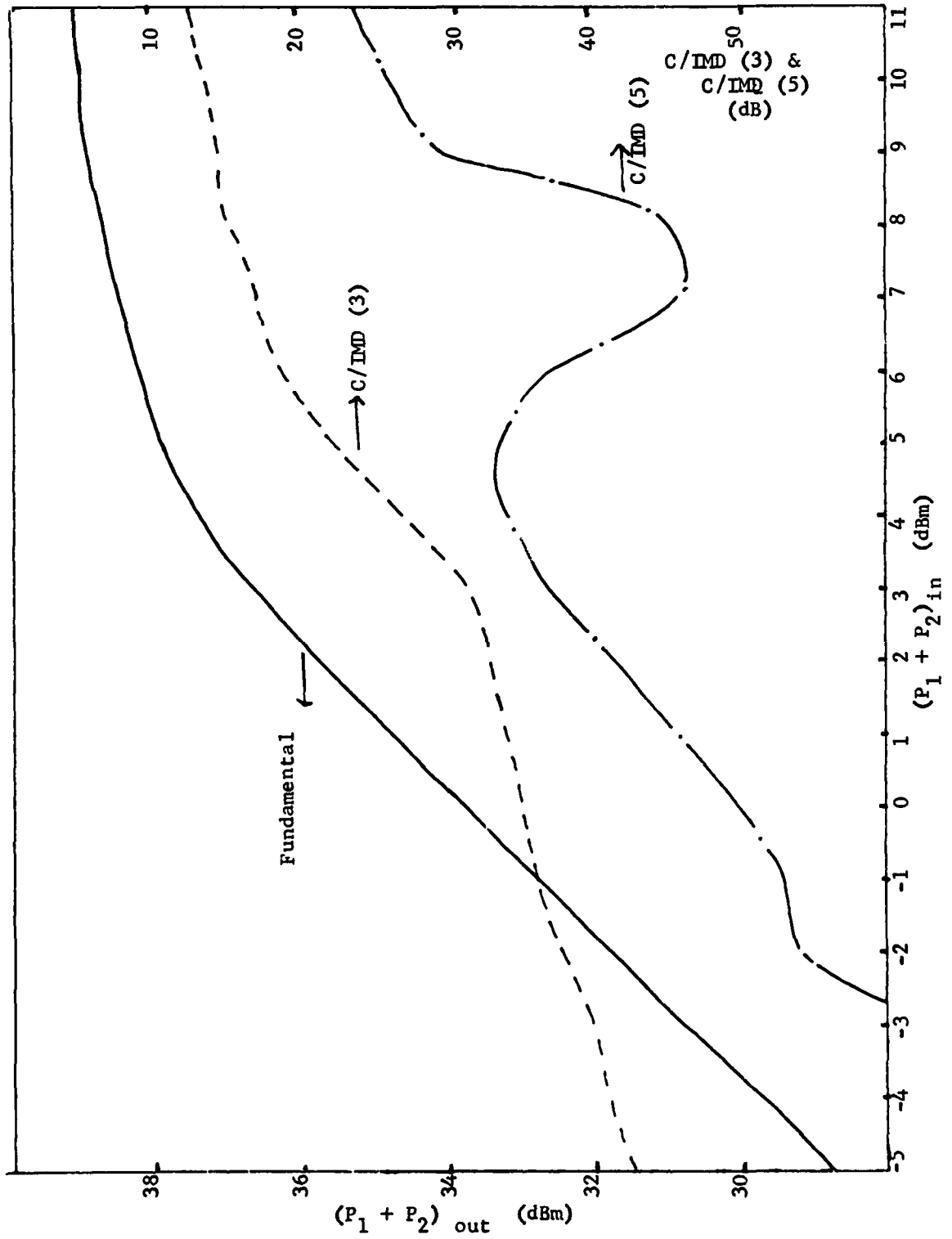
Total Phase Shift and DC Power Consumption of the X-Band Linear Solid State Power Amplifier

Figure 2-21



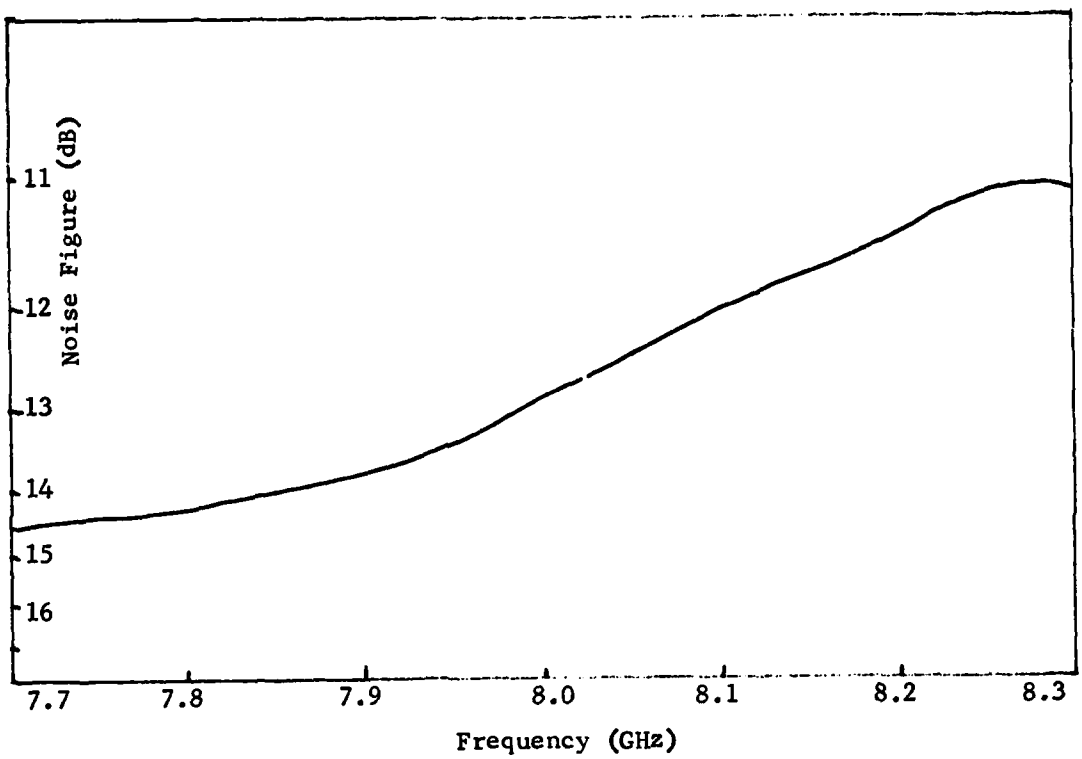
Frequency Response and Group Delay of the X-Band, Linear Solid State Power Amplifier

Figure 2-22



Two-Tone Intermodulation Test of the X-Band, Linear Solid State Power Amplifier
Figure 2-23

The input and output VSWR of the amplifier is 2.1 and 1.24 respectively. The noise figure of the complete amplifier was measured and plotted in Figure 2-24. At 8 GHz, the amplifier shows a noise figure of 12.9 dB.



Noise Figure of the X-Band, Linear Solid State Power Amplifier

Figure 2-24

III. RF LIFE TEST OF THE X-BAND, LINEAR SOLID STATE AMPLIFIER

The original amplifier development contract was amended to include a two-year RF life test program after completion of the amplifier. The life test program started on July 19, 1979. The chassis temperature was set equal to 32°C. After 143 hours of continuous operation, the power amplifier module #2 failed. Within power amplifier module #2, the driver FET MSC 88110 and one of the FET MSC 88110 at the output stage failed. Power Amplifier Module #2 was removed from the amplifier chain and RF life test was continued. On January 25, 1980, after another 4700 hours of operation, power amplifier module #1 failed. This time, one of the output FET MSC88110 burned out. Both module #1 and Module #2 were replaced with new GaAs FETs. The complete amplifier was placed back on life test April 10, 1980. As of September 12, 1980 there have been no further failures.

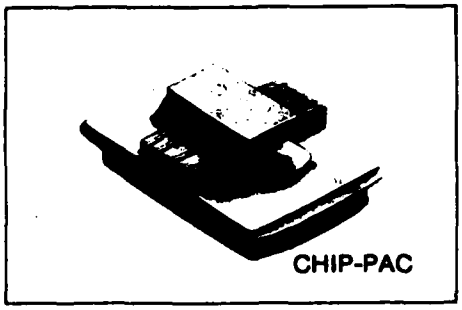
IV. CONCLUSIONS AND RECOMMENDATIONS

Excellent electrical performance of the X-Band, solid state linear amplifier has been demonstrated. The experimental model linear solid state amplifier developed by Ford Aerospace and Communications Corporation for RADC has proven that GaAs Field Effect Transistors are definitely a feasible replacement for Traveling Wave Tube Amplifiers for many applications. The FET linear amplifier meets or exceeds TWTA performance in the areas of Linearity, Intermodulation Distortion Products, Group Delay, AM to PM conversion, and Noise Figure. Further effort in the mechanical packaging, the temperature compensation circuit, and the power supply are required. A complete engineering model of the X-Band, linear solid state amplifier with associated power supply circuitry should be built and tested in the near future to realize an X-Band solid state amplifier for TWTA replacement.

The RF life test program indicates some infant mortality problems with the MSC power FETs. Proper screening test procedures should be established to weed out these weak devices before assembly. A full scale reliability test program is also needed to evaluate the reliability of GaAs power FETs under various operating conditions to guarantee the long term operation of X-Band, linear solid state amplifiers.

V. APPENDIX

5.1 MSC GaAs Power FET Data Sheet



X-BAND LOW-POWER 0.05 WATT GaAs FET MSC 88100

PRELIMINARY DATA SHEET TE-813A

MICROWAVE SEMICONDUCTOR CORP

Issue October 1978

Product Description

The MSC "88100 series" of devices are high power GaAs Field Effect Transistors in Chip-carriers employing the latest state-of-the-art technology and fabrication techniques. The devices are designed for linear power amplifiers and for oscillator applications up to at least 15 GHz. The transistors are supplied in a low-loss, minimum parasitic, ultra miniature CHIP-PAC chip carrier. The GaAs FET chip is flip-chip mounted for minimum thermal resistance as measured by Infra-Red Scanning Microscope.

Features

- **High Linear Gain**
- **High Power-Added Efficiency**
- **Wide Dynamic Range**
- **Low Distortion**
- **Metal-Ceramic Chip-Carrier**
- **Gold-Based Refractory Metallization**

Absolute Maximum Ratings (T_A = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNITS
Drain to Source Voltage	V_{DS}	10	V
Gate to Source Voltage	V_{GS}	-8	V
Total Dissipation	P_T	1.5	W
Storage Temperature	T_{stg}	-65 to +200	°C
Operating Temperature (Channel)	$T_{channel}$	-65 to +150	°C

Electrical Characteristics (T_A = 25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain Current	I_{DSS}	V_{DS} = 5V, V_{GS} = 0	50	90	140	mA
Transconductance	G_m	V_{DS} = 5V	-	20	-	m℧
Pinch-off Voltage	V_p	V_{DS} = 5V	-	6	-	V
Thermal Resistance	θ_{jc}	(IR Scanning)		[illegible]		°C/W
Output Power @ f = 12GHz	P_{OUT} (TEST)	V_{DS} = 8.0V, $V_{GS} \approx$ -1V, P_{IN} = + 12 dBm	50	65	-	mW

Typical RF Performance (T_A = 25°C)

PARAMETER	SYMBOL	@ f = 8GHz	@ 10GHz	@ 12GHz	UNITS
Power at 1 dB Compression Point	P_{out}	65	65	65	mW
Gain at 1 dB Compression Point	G_p	9.5	8.0	6.5	dB
Third Order Intercept Point	IMD_3	28	28	28	dBm

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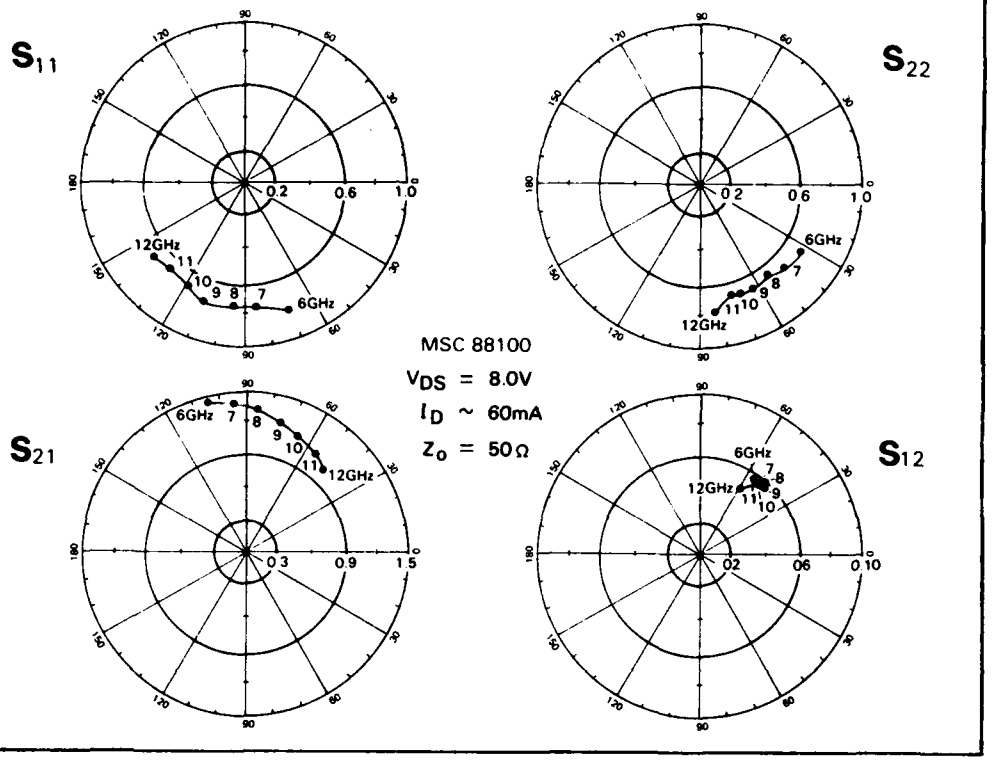
Printed in U S A

Typical S-Parameters — —(Also available on COMPACT ™ databank)



HANDLING AND MOUNTING RECOMMENDATIONS FOR THE MSC 88100 SERIES (CHIP—PAC)

The CHIP-PAC series GaAs FETs are intended for power generation and amplification at frequencies above 8 GHz. For frequencies below 8 GHz, the standard hermetic FLIPAC series are recommended.

When using the CHIP-PAC, one must always be mindful that the chip is exposed and gross mis-handling will permanently damage the device.

(1) The CHIP-PAC consists of a gold plated copper ground plane, and two alumina standoffs. The source is connected to the ground via a flip-chip mount, while wire bonds are used to attach the drain and gate of the FET to the metallized standoffs. The drain is identified by an ink dot.

(2) When soldering the CHIP-PAC into a circuit a minimum of flux should be used. Excess flux can condense on the chip and cause degraded performance.

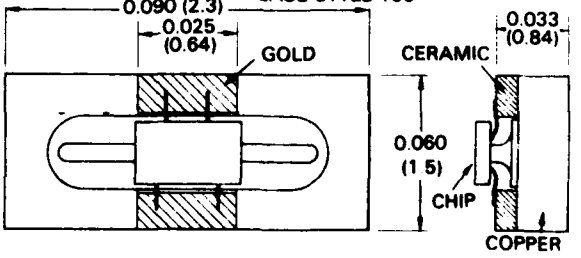
(3) To solder the CHIP-PAC into a circuit, a temperature of less than 300°C should be used. The device should not be held at temperature longer than needed, but in no case longer than 3 minutes.

(4) Wire bonds from the standoffs to the circuit can be made with any technique. Ultrasonic, thermo-compression or wedge bonds are all acceptable, the temperature limits are the same as those above for soldering.

(5) A curve tracer can be used to test the FET without fear of burnout. The only precautions are a reasonably good thermal path for the FET and short leads to prevent low frequency oscillations (Ferrite beads may also help). Other than these, common sense need be your only guide.

(6) MSC GaAs FETs are not sensitive to static discharges generated during normal handling of devices. Therefore, no special grounding of equipment and personnel is recommended.

Outline Drawing : CHIP-PAC (Preliminary)
CASE STYLE 100



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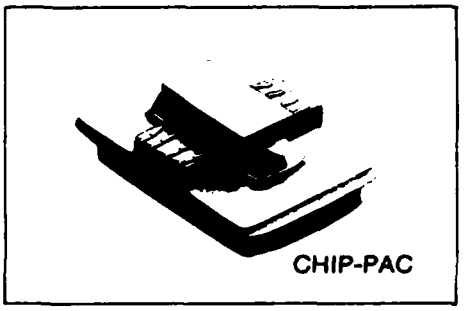


X-BAND MEDIUM-POWER 0.5 WATT GaAs FET MSC 88102

PRELIMINARY DATA SHEET TE-812 A

MICROWAVE SEMICONDUCTOR CORP.

Issue October 1978

Product Description

The MSC "88100 series" of devices are high power GaAs Field Effect Transistors in Chip-carriers employing the latest state-of-the-art technology and fabrication techniques. The devices are designed for linear power amplifiers and for oscillator applications up to at least 15 GHz. The transistors are supplied in a low-loss, minimum parasitic, ultra miniature CHIP-PAC chip carrier. The GaAs FET chip is flip-chip mounted for minimum thermal resistance as measured by Infra-Red Scanning Microscope.

Features

- **High Linear Power Output**
- **High Power-Added Efficiency**
- **Wide Dynamic Range**
- **Low Distortion**
- **Metal-Ceramic Chip-Carrier**
- **Gold-Based Refractory Metallization**

(T_A = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNITS
Drain to Source Voltage	V_{DS}	10	V
Gate to Source Voltage	V_{GS}	-8	V
Total Dissipation	P_T	3.2	W
Storage Temperature	T_{stg}	-65 to +200	°C
Operating Temperature (Channel)	$T_{channel}$	-65 to +150	°C

(T_A = 25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain Current	I_{DSS}	V_{DS} = 5V, V_{GS} = 0	200	300	450	mA
Transconductance	G_m	V_{DS} = 5V	-	75	-	m℧
Pinch-off Voltage	V_p	V_{DS} = 5V	-	6	-	V
Output Power @ f = 12GHz	P_{OUT} (TEST)	V_{DS} = 9.0V, $V_{GS} \approx$ -2V, P_{IN} = +21.0 dBm	350	400	-	mW

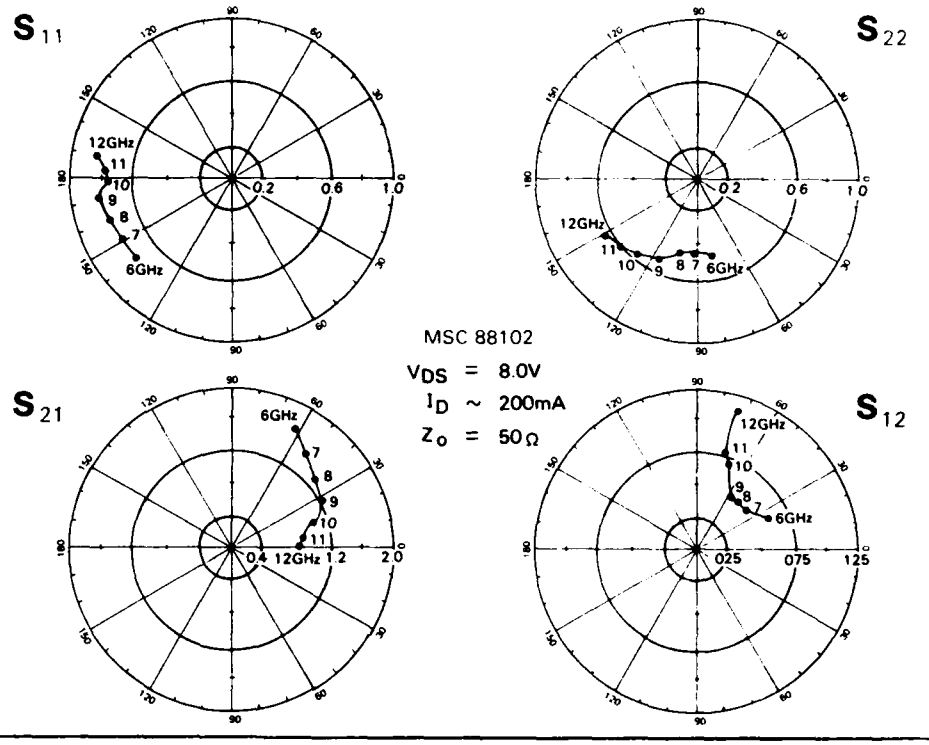
(T_A = 25°C)

PARAMETER	SYMBOL	@ f = 8GHz	@ 10GHz	@ 12GHz	UNITS
Power at 1 dB Compression Point	P_{out}	500	500	500	mW
Gain at 1 dB Compression Point	G_p	8.0	6.5	5.5	dB
Third Order Intercept Point	IMD_3	37	37	37	dBm

MSC MICROWAVE SEMICONDUCTOR CORP.
100 SCHOOL HOUSE ROAD SOMERSET N J 08873 PHONE (201) 469 3311 TWX (710) 480-4730 TELEX 833473

Printed in U S A

Typical S-Parameters — (Also available on COMPACT™ databank)



HANDLING AND MOUNTING RECOMMENDATIONS FOR THE MSC 88100 SERIES (CHIP—PAC)

The CHIP-PAC series GaAs FETs are intended for power generation and amplification at frequencies above 8 GHz. For frequencies below 8 GHz, the standard hermetic FLIPAC series are recommended.

When using the CHIP-PAC, one must always be mindful that the chip is exposed and gross mis-handling will permanently damage the device.

(1) The CHIP-PAC consists of a gold plated copper ground plane, and two alumina standoffs. The source is connected to the ground via a flip-chip mount, while wire bonds are used to attach the drain and gate of the FET to the metallized standoffs. The drain is identified by an ink dot.

(2) When soldering the CHIP-PAC into a circuit a minimum of flux should be used. Excess flux can condense on the chip and cause degraded performance.

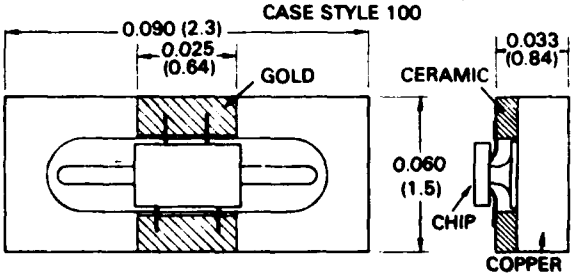
(3) To solder the CHIP-PAC into a circuit, a temperature of less than 300°C should be used. The device should not be held at temperature longer than needed, but in no case longer than 3 minutes.

(4) Wire bonds from the standoffs to the circuit can be made with any technique. Ultrasonic, thermo-compression or wedge bonds are all acceptable; the temperature limits are the same as those above for soldering.

(5) A curve tracer can be used to test the FET without fear of burnout. The only precautions are a reasonably good thermal path for the FET and short leads to prevent low frequency oscillations (Ferrite beads may also help). Other than these, common sense need be your only guide.

(6) MSC GaAs FETs are not sensitive to static discharges generated during normal handling of devices. Therefore, no special grounding of equipment and personnel is recommended.

Outline Drawing : CHIP-PAC (Preliminary)
CASE STYLE 100



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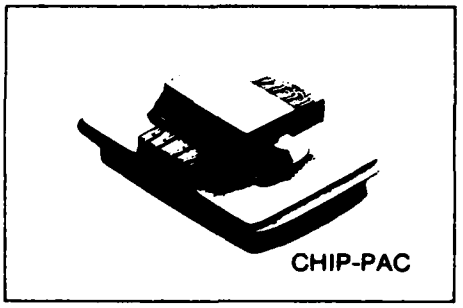

X-BAND HIGH-POWER 1.0 WATT GaAs FET MSC 88104

PRELIMINARY DATA SHEET TE-814A

MICROWAVE SEMICONDUCTOR CORP

Issue October 1978

Product Description

The MSC "88100 series" of devices are high power GaAs Field Effect Transistors in Chip-carriers employing the latest state-of-the-art technology and fabrication techniques. The devices are designed for linear power amplifiers and for oscillator applications up to at least 15 GHz. The transistors are supplied in a low-loss, minimum parasitic, ultra miniature CHIP-PAC chip carrier. The GaAs FET chip is flip-chip mounted for minimum thermal resistance as measured by Infra-Red Scanning Microscope

Features

- **High Linear Power Output**
- **High Power-Added Efficiency**
- **Wide Dynamic Range**
- **Low Distortion**
- **Metal-Ceramic Chip-Carrier**
- **Gold-Based Refractory Metallization**

Absolute Maximum Ratings (T_A = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNITS
Drain to Source Voltage	V_{DS}	10	V
Gate to Source Voltage	V_{GS}	-8	V
Total Dissipation	P_T	6.4	W
Storage Temperature	T_{stg}	-65 to +200	°C
Operating Temperature (Channel)	$T_{channel}$	-65 to +150	°C

Electrical Characteristics (T_A = 25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain Current	I_{DSS}	V_{DS} = 5V, V_{GS} = 0	500	700	900	mA
Transconductance	G_m	V_{DS} = 5V	-	140	-	m℧
Pinch-off Voltage	V_p	V_{DS} = 5V	-	6	-	V
Output Power @ f = 12GHz	P_{OUT} (TEST)	V_{DS} = 9.0 V, $V_{GS} \approx$ -2V, P_{IN} = +24.5 dBm	800	1000	-	mW

Typical RF Performance (T_A = 25°C)

PARAMETER	SYMBOL	@ f = 8GHz	@ 10GHz	@ 12GHz	UNITS
Power at 1 dB Compression Point	P_{out}	1.0	1.0	1.0	W
Gain at 1 dB Compression Point	G_p	7.0	6.5	5.0	dB
Third Order Intercept Point	IMD_3	39	39	39	dBm

MICROWAVE SEMICONDUCTOR CORP.
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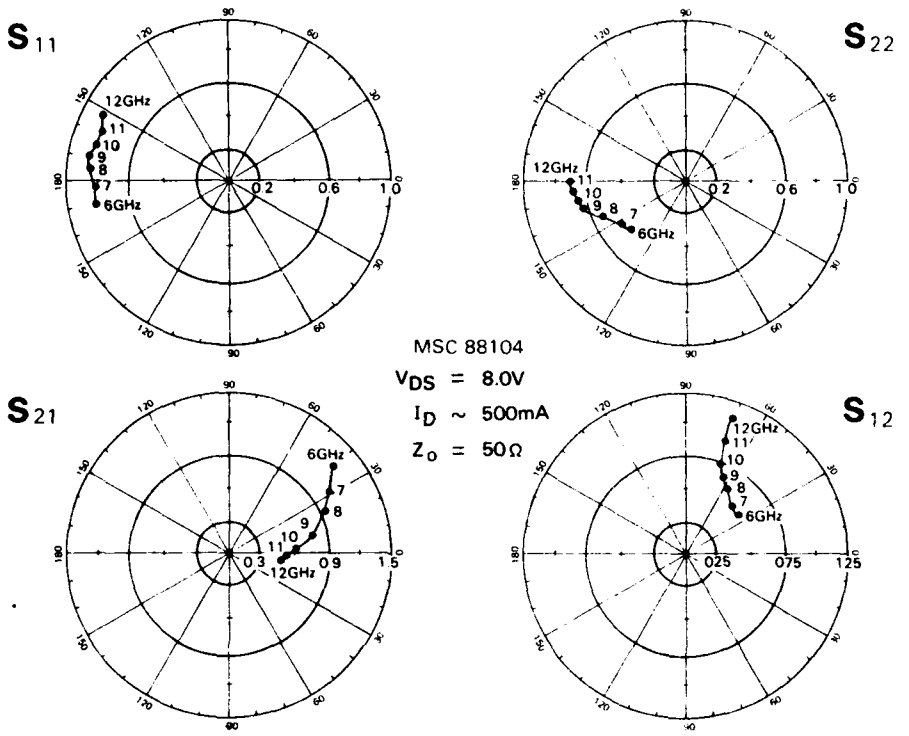
Printed in U.S.A.

Typical S-Parameters —

— (Also available on COMPACT ™ databank)



HANDLING AND MOUNTING RECOMMENDATIONS FOR THE MSC 88100 SERIES (CHIP—PAC)

The CHIP-PAC series GaAs FETs are intended for power generation and amplification at frequencies above 8 GHz. For frequencies below 8 GHz, the standard hermetic FLIPAC series are recommended.

When using the CHIP-PAC, one must always be mindful that the chip is exposed and gross mis-handling will permanently damage the device.

(1) The CHIP-PAC consists of a gold plated copper ground plane, and two alumina standoffs. The source is connected to the ground via a flip-chip mount, while wire bonds are used to attach the drain and gate of the FET to the metallized standoffs. The drain is identified by an ink dot.

(2) When soldering the CHIP-PAC into a circuit a minimum of flux should be used. Excess flux can condense on the chip and cause degraded performance.

(3) To solder the CHIP-PAC into a circuit, a temperature of less than 300°C should be used. The device should not be held at temperature longer than needed, but in no case longer than 3 minutes.

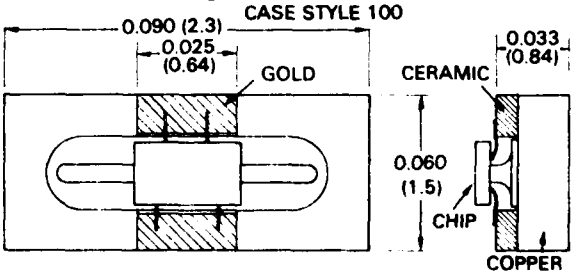
(4) Wire bonds from the standoffs to the circuit can be made with any technique. Ultrasonic, thermo-compression or wedge bonds are all acceptable, the temperature limits are the same as those above for soldering.

(5) A curve tracer can be used to test the FET without fear of burnout. The only precautions are a reasonably good thermal path for the FET and short leads to prevent low frequency oscillations (Ferrite beads may also help). Other than these, common sense need be your only guide.

(6) MSC GaAs FETs are not sensitive to static discharges generated during normal handling of devices. Therefore, no special grounding of equipment and personnel is recommended.

Outline Drawing : CHIP-PAC (Preliminary)

CASE STYLE 100



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5.2 Operating Instructions for the Linear Solid State Amplifier

The following operating instructions and precautions are presented here in order to prevent operational damage to the Linear Solid State Amplifier. Although Solid State FET amplifiers offer increased life time and reliability over TWTA's, they are unforgiving to associated equipment failure and to human errors. A power supply conditioning circuit is built into the amplifier to prevent failures due to untimely power line outages. The instructions listed below are necessary good engineering practices to prevent damage due to human or associated equipment failures.

1. Two DC power supplies are required. One for +10 volts (nom.) at 10 amps (min.) and the other for -6 volts (nom.) at 1/2 amp (min.).

2. Always turn on the negative (-6 volts) power supplies BEFORE the positive (+10 volts) power "ON" supply.

3. Check out both power supplies for any oscillations from no load up to full rated loads. This should include their turn-on and turn-off oscillations in case of AC line intermittant failure. No oscillations should be present.

4. Upon initial turn-on of amplifier, reset power supplies for correct voltages. Reset voltage of -6 volt supply first.

5. Never turn-on amplifier with RF input signal applied. (This is only a safety measure and is not necessarily

mandatory.)

6. Maximum power input for linear operation is +2 dBm. Absolute maximum RF power input is +10 dBm. (Due to the linear optimization techniques designed into the amplifier, no input limiter is provided). The above mentioned linear power level limits are for RMS RF power as measured by a power meter of continuous multi-tone and single tone signals.

7. Nominal RF output levels are 5 watts linear (-32 dB IMD, 2-tone) and 10 Watts saturated single signal or narrow band FM.

8. Design center frequency is 8 GHz.

9. A fan is supplied to blow air across the heat sink fins located on the bottom. Use this or an equivalent fan at all times that the amplifier is "ON".

10. A plexiglass top is provided to allow viewing of the MIC circuitry without endangering the tuned circuitry to curious probing.

11. Power supply leads of #18 Ga wire or larger should be used. Space lugs should be used at the rear power input terminal of the amplifier. Separate common return wires MUST be used for each of the two power supplies.

12. Always load the output with a reasonably good RF load at the operating frequencies.

5.3 LIST OF ABBREVIATIONS AND SYMBOLS

FET	Field Effect Transistor
GaAs	Gallium Arsenide
IMD	Intermodulation Distortion
VSWR	Voltage Standing Wave Ratio
D.C.	Direct Current
TWTA	Traveling Wave Tube Amplifier
MHz	Megahertz
GHz	Gigahertz
RF	Radio Frequency
Pin	Input pout
Pout	Output power
η	Efficiency
SAT	Saturated
Δ	Delta, Change
ω	Omega, 2 times frequency
t	time
Idc	Direct current
dB	Decibel

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of
Rome Air Development Center

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