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WALSH PREPROCESSOR

American Electronic Laboratories, Inc.

James Van Cleave

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time of arrival) are not known. The purpose of this program was to develop an improved exploratory development model of a system to detect the presence of low SNR signals, on a single pulse-by-pulse basis.

The technique chosen for this program was the use of the Walsh Transform as the basis for a two transform digital filter. This technique had been demonstrated by AEL as a result of in-house IR/D programs and implemented to USAF preliminary requirements under a previous contract for a Walsh Adaptive Filter (RADC Report TR-78-82 for Contract F30602-76-C-0299). The current program was to further develop the technique and to fabricate a programmable unit suitable for test and evaluation purposes against a variety of potential applications. The system name, Walsh Preprocessor (WP), was derived from the use of a Walsh transform to adaptively filter signals of varying pulse widths and repetition rates.

An exploratory development model was fabricated, tested and delivered to the USAF Foreign Technology Division (FTD). The testing conducted prior to delivery indicated improvement over conventional threshold detection of 2.9 dB to 12.8 dB in pulse detection sensitivity dependent upon pulse width, probability of detection and false alarm rate. The overall performance of the system will be further verified by the tests to be performed by FTD although the preliminary tests were successful.

The system operates upon a post detection video signal and generates a filtered version of the input signal in real time using a pipeline processor. The WP System operates as a filter to be installed typically between a receiver and signal processing equipment. The filtering algorithm using Walsh Transforms is described in detail in Appendix A of this report.

The unit developed under this contract has proven the technique and provided a versatile equipment for application on several critical USAF needs. The next development step would be to produce models incorporating features specifically tailored toward signals examined during the test and evaluation phase.

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EVALUATION

The Walsh Preprocessor is a follow-on effort of the Walsh Adaptive Filter. This effort was implemented to provide an expanded capability for the Air Force in detecting pulse-type signals in a high noise environment. Namely, an improvement in pulse detection sensitivity and a programming capability to assist an analyst in tailoring the unit to the noise environment and detection probability.

The principal mode of operation is to analyze the post detected video output of any microwave ELINT or ESM receiver.

This exploratory development model will be used to determine the applicability of Walsh Technology in various Air Force disciplines. This device was developed under TPO 1 C 4B for operational suitability testing and evaluation. The device is currently undergoing such testing at FTD.

This effort completes plans for development of WAF technology under this TPO.

Edward C. Buzas
EDWARD C. BUZAS
Project Engineer

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SUMMARY

A common problem in the area of signal processing is that of the detection of pulse signals having very low signal-to-noise ratios (SNR). This problem is worsened when major signal parameters (pulse width and time of arrival) are not known. The purpose of this program was to develop an improved exploratory development model of a system to detect the presence of low SNR signals, on a single pulse-by-pulse basis.

The technique chosen for this program was the use of the Walsh Transform as the basis for a two transform digital filter. This technique had been demonstrated by AEL as a result of in-house IR&D programs and implemented to USAF preliminary requirements under a previous contract for a Walsh Adaptive Filter (RADC Report TR-78-82 for Contract F30602-76-C-0299). The current program was to further develop the technique and to fabricate a programmable unit suitable for test and evaluation purposes against a variety of potential applications. The system name, Walsh Preprocessor (WP), was derived from the use of a Walsh transform to adaptively filter signals of varying pulse widths and repetition rates.

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Section I

INTRODUCTION

This final technical report documents the design and development of an exploratory development model of the Walsh Preprocessor under contract F30602-79-C-0048 for the U.S. Air Force Rome Air Development Center (RADC).

The contract called for the development of an adaptive filter, based on the Walsh-Hadamard transform, which would enhance the signal-to-noise ratios of pulse type signals. The filter is required to operate with no a-priori knowledge of pulse width, amplitude, or time of arrival. System outputs are available as both a reconstructed video signal and a delayed and gated video input. The unit was designed for use in feasibility studies in both laboratory and controlled field environments.

One exploratory development model was delivered to FTD in March 1980. This model met or exceeded all contract specifications.

The Walsh Preprocessor (WP) uses a filtering algorithm which was developed by American Electronic Laboratories, Inc. (AEL) during two company sponsored IR&D programs, each of one year duration. The first IR&D program was the theoretical and empirical development of the algorithms using computer simulations. The second IR&D program sponsored the design and fabrication of a breadboard filter unit which was used to prove feasibility and for demonstration purposes. A previous RADC contract to AEL provided for the development of a Walsh Adaptive Filter, (WAF), based on the AEL IR&D breadboard. The design of the Walsh Preprocessor incorporated several improvements to the WAF.

This technical report constitutes portions of the previous report RADC TR-78-82 for the WAF, as appropriate to the improved and expanded Walsh Preprocessor.

Section II of this final report discusses the theory of operation of the WP system. A detailed description of the unit is given in Section III while Section IV discusses operating procedures and applications. The test results are documented in Section V, the reliability failure record of the integrated circuits is discussed in Section VI, and AEL's conclusions and recommendations are given in Section VII. Appendix A is an extensive discussion of the filtering algorithm.

Section II

THEORY OF OPERATION

The purpose of the Walsh Preprocessor (WP) is to enhance the detection of low SNR pulse signals of unknown width and time of arrival. The conventional technique for this has been a voltage threshold detector which requires a high input SNR to prevent false alarms. The WP operation is based on the principle that the recognition and filtering of low SNR pulsed signals of unknown width and time of arrival can best be performed after transformation of the input signal into other than the time domain. The WP uses the Walsh-Hadamard orthogonal transform of which the transform domain is called sequency. The term sequency is defined as one-half the number of zero crossings of the orthogonal function, over the period of analysis. The following sections present a general discussion of the filtering theory. AEL has been assigned a patent (4,038,539, awarded to J. VanCleave) on the detection and filtering means and method. A detailed description of the algorithm of implementation is given in Appendix A.

ORTHOGONAL TRANSFORMS

The Fourier Transformation is perhaps the most well known of all orthogonal transformations due to the fact that electrical engineering is based on a fundamental understanding of the relationships between time and frequency domain. However, there exists a great many orthogonal functions such as the transforms of Laplace, Walsh, Haar, Karhunen-Loeve, plus the Z-Transform as well as the polynomials of Legendre, Hermite, Laguerre, the functions of Bessel and Lebesgue, and the Sturm-Liouville series. All may be represented as a sequence of functions:

$$X_1(t) \dots\dots\dots X_n(t)$$

which are orthogonal in the interval $(-T/2, T/2)$

such that:

$$\int_{-T/2}^{T/2} X_n(t) X_m^*(t) dt = \begin{cases} 1 & \text{if } m = n \\ 0 & \text{if } m \neq n \end{cases}$$

Now that we have defined a set of orthogonal functions, we may expand any reasonably behaved function (such as a signal) into a series:

$$f(t) = \sum_{n=1}^N a_n X_n(t)$$

that converges to the function $f(t)$. In other words, we can break the signal $f(t)$ down into a series of orthogonal functions. Figure 1 shows the first 16 orthogonal functions of the Fourier, Hadamard (Walsh), Karhunen-Loeve, and Haar transforms. Again, the Fourier is most common, and the transform simply

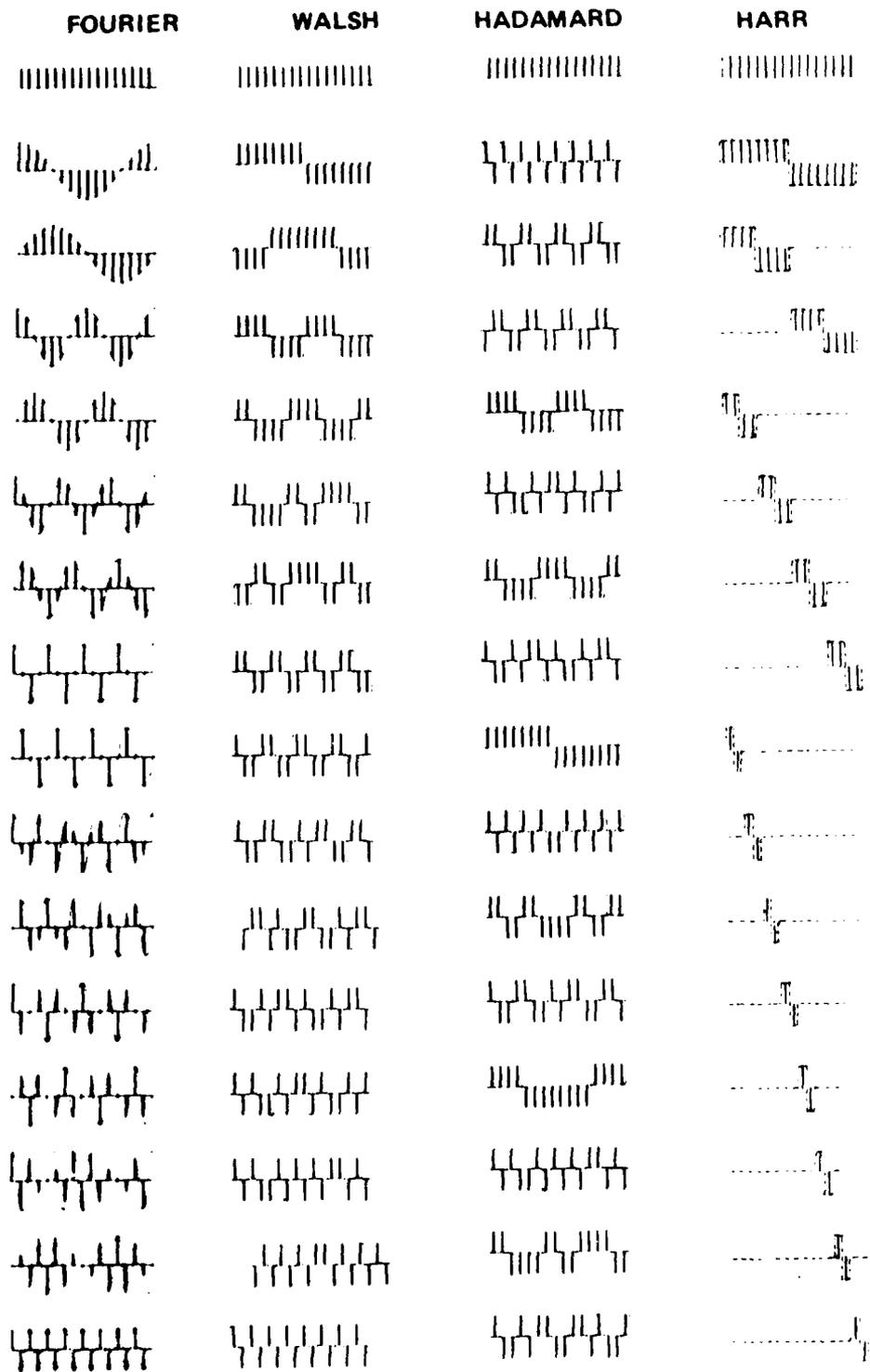


Figure 1. Discrete Orthogonal Functions N=16

represents a time domain function as a series of phased sine waves, which is also called harmonic analysis. If the signal were a pure sine wave, then only one of the Fourier functions would correlate, and a single frequency spectrum line would result.

The Hadamard (Walsh) functions are similar to square waves and if the input signal were a properly phased square wave, a single sequency spectrum line could result from the Walsh Transform. The Walsh transform analyzes signals by examination of the rate-of-zero-crossings of an axis, which is not always exactly equal to the signal frequency, hence is termed sequency. These transforms represent a waveform as a combination of phased squarewave-line functions, rather than sine waves as per the Fourier Transform. It is far easier to generate and process squarewave binary functions in a digital processor (either software controlled or hardwired) than it is to process sinewaves.

The Walsh-Hadamard transformation is a true orthonormal transformation which, in addition to having other well behaved properties, is orthogonal, unique and complete. These properties assure us that 1) for any set of input data, there exists one and only one set of transformed output data and 2) an inverse transform exists to guarantee that all input data can be totally reconstructed, if desired, by first performing the forward transform (time-to-sequency domain) followed by the inverse transform (sequency-to-time domain). Furthermore, the forward and inverse transform algorithms are identical, provided that the data is properly ordered.

FAST WALSH TRANSFORM ALGORITHM

The Forward Fast Walsh Transform (FFWT) and Inverse Fast Walsh Transform (IFWT) Processors are functionally identical digital circuits which calculate the transformation between the time domain and the sequency domain. The algorithm used by both circuits is the same, with the only difference between the two being the digital word lengths and a scale factor. The circuits use the Cooley-Tukey algorithm which is shown in flow diagram form in Figure 2 for an 8 point transform. This transform can be calculated using three levels of arithmetic operations as shown. Level 1 operates on pairs of data separated by $N/2$ samples where N is the number of points in the transform. Level 2 uses pairs separated by $N/4$ and in Level 3 the spacing is $N/8$ for adjacent samples. This sequence is valid for any value of N which, of course, must be a binary number. Each level adds and subtracts the samples with the weighting functions (W^n) all being equal to one. The Walsh Preprocessor has an N equal to 256 and requires 8 levels to calculate the transform. Figure 3 is a block diagram of the circuit and indicates the pipeline manner in which the forward and inverse transforms are performed. Each level contains two delay circuits which serve to align the data into the proper time sequence. The delay interval decreases by one-half for each advancement of level order. The switches shown between the levels are only representations of the switching function performed and are actually implemented using logic circuits. A block diagram of a typical level is shown in Figure 4. This figure is the same for all levels of the FFWT and IFWT with the circuitry differences being those necessary to accommodate the different word lengths. The memories are either shift registers or random access memories (RAM) depending upon the delay required. The adder and subtractor are Arithmetic Logic Units (ALU) MSI circuits.

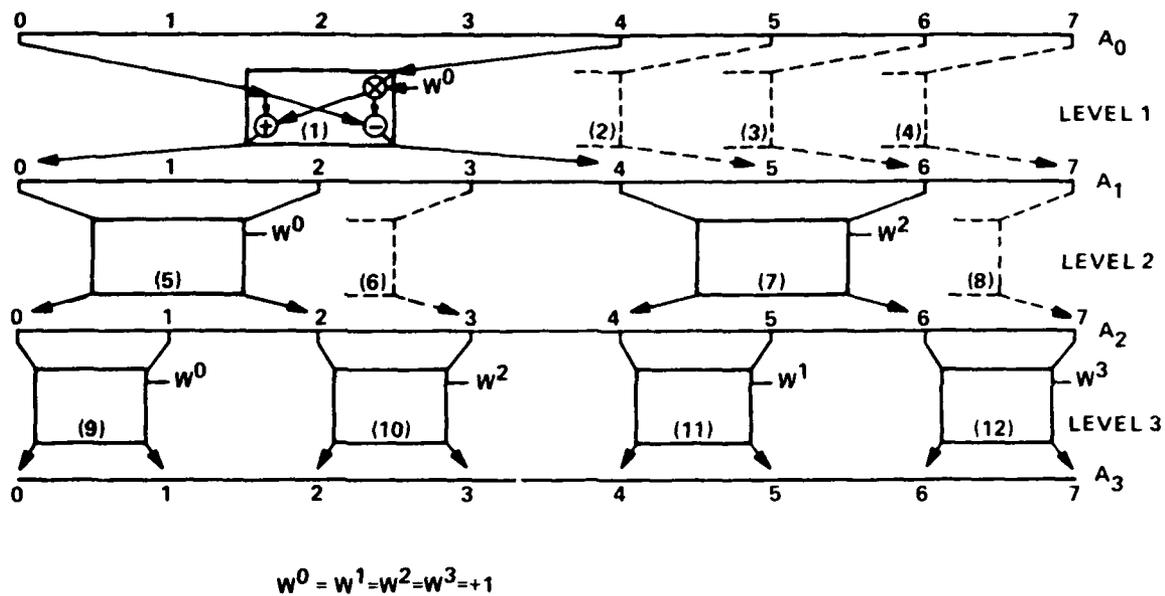


Figure 2. Cooley-Tukey Algorithm Flow Diagram for N=8

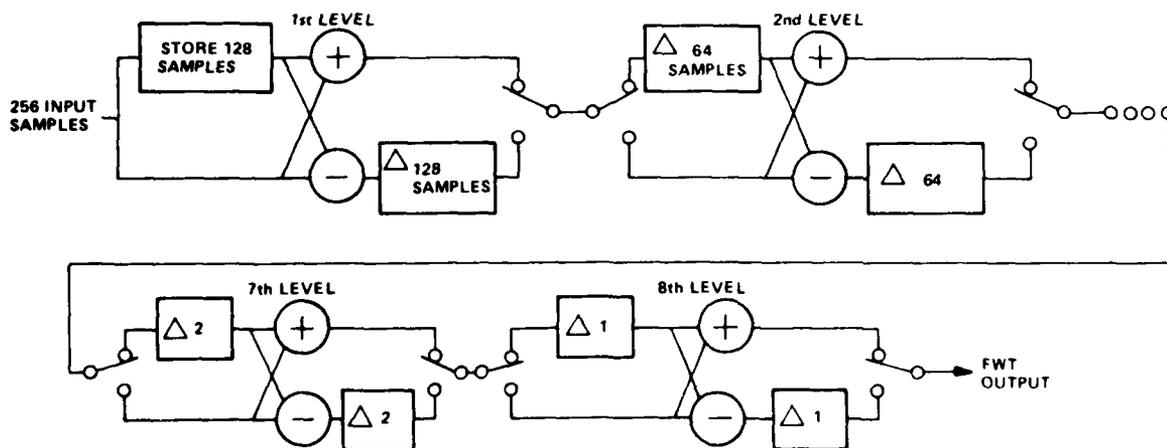


Figure 3. 8 Level Pipeline Fast Walsh Transform Processor Block Diagram

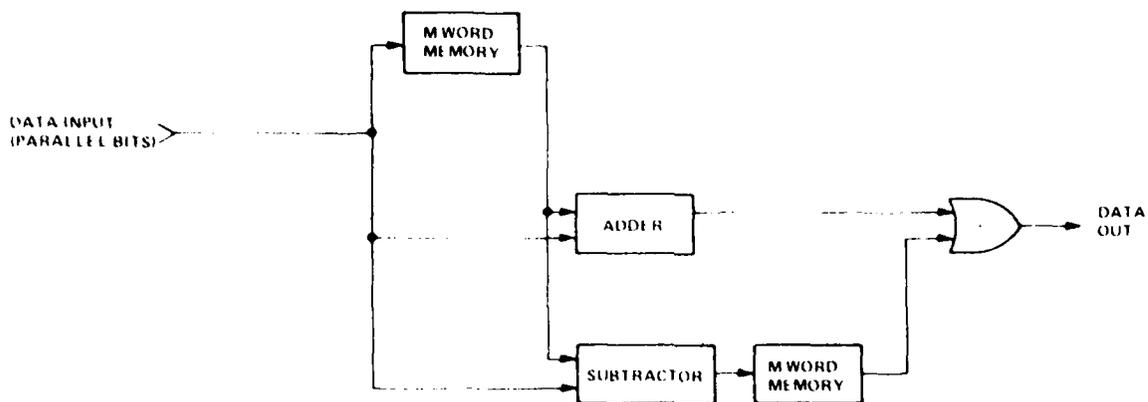


Figure 4. Typical Fast Walsh Transform Level Block Diagram

The FFWT and IFWT use fixed point implementation and the levels are designed to prevent overflow of the words. The circuit delay between the first input sample and the first output word is equal to one block aperture time or 256 sample periods. The circuit delay is fixed at this number of samples, hence the actual time delay is inversely proportional to the system sampling rate.

FILTERING ALGORITHM

Two processing algorithms are used in the WP system: the sequency analysis algorithm and the sequency sorting algorithm. Both implemented algorithms operate on the sequency output of the Forward Fast Walsh Transform circuitry as shown in Figure 5.

The sequency analysis processor completes its function only after the full spectrum block (of 256 elements) is available. However, the sequency analysis processor controls the sorting parameters needed by the sequency sorting processor. The sequency sorting processor operates on the delayed serial output of the FFWT. The delay is necessary to allow the sequency analysis processor to provide the control output prior to the arrival of the first serial sequency word of the block at the sequency sorting processor.

The sequency analysis processor provides two major functions: 1) the determination as to whether or not any non noiselike signal is present in the

(FILTER CHANNEL PORTION OF WALSH PREPROCESSOR)

PROGRAMMABLE THRESHOLD CONSTANTS

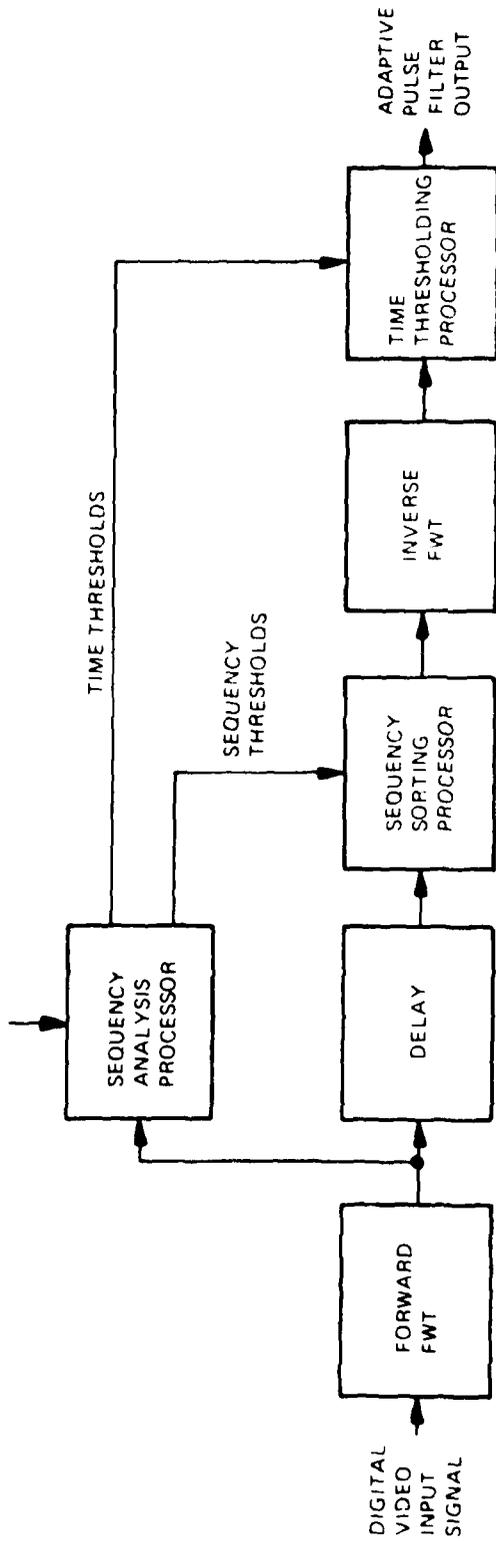


Figure 5. Sequence Spectrum Processor Block Diagram

block, and 2) if a signal is present, what the estimated width and SNR parameters are. The technique used involves multiple sequency spectrum amplitude comparisons, based on the following theorem:

Given a group of N regularly spaced time domain samples consisting of a rectangular or nearly rectangular single polarity pulse signal of M samples width and unknown position plus additive noise such as Gaussian, Rayleigh or Ricean noise, then:

- A. If this group of N (where N is most conveniently a binary multiple; i.e., $N=2^x$ where x is any integer) samples are transformed into the Walsh sequency domain, then the pulse position can be approximately represented by the lowest N/M sequency terms. If these N/M terms are retained and all others discarded, then an inverse Walsh transformation will result in a time domain signal of significantly enhanced signal to noise ratio.
- B. Furthermore, if both pulse width and position are unknown, yet, the desired signal is corrupted by Gaussian, etc., noise of approximately uniform sequency distribution, then both width and position may be enhanced by passing all sequency terms above a given threshold, starting with the lowest sequency term and proceeding until the terms consistently are at or below the (noise) threshold.

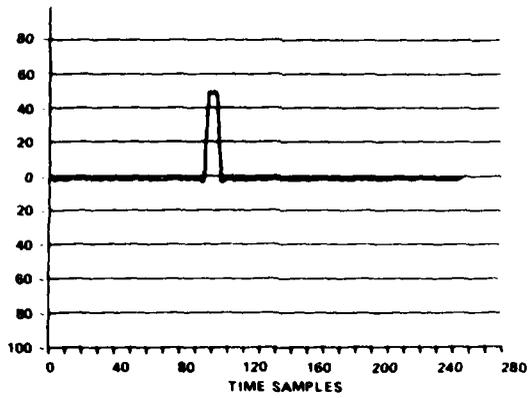
Paragraph A is the general theorem and Paragraph B is an application of Paragraph A. Both paragraphs are utilized in the Walsh Preprocessor.

Figures 6 and 7 illustrate the above principal for high and low SNR pulses. The sequency elements associated with a pulse have a definite tendency toward low sequencies (left hand side of sequency domain plots). Also, wideband noise has a definite tendency to be distributed evenly over all sequencies. Both of these tendencies are independent of pulse position. Thus, the adaptive sequency sorting algorithm consists of the following parts:

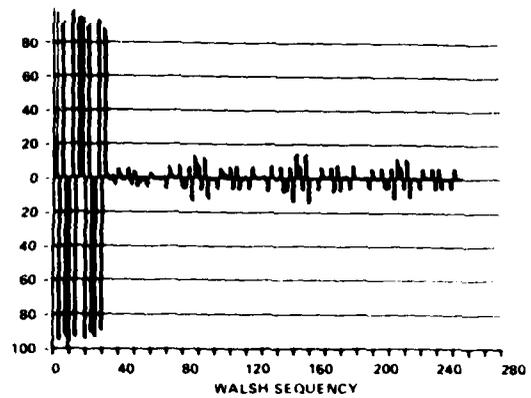
- a) An adaptive low pass corner cutoff whereby all sequencies above some sequency value are rejected.
- b) An adaptive amplitude threshold whereby large amplitude sequency elements are passed and small elements are rejected.
- c) Various additional subalgorithms that handle special cases, such as inputs with multiple overlapping pulses, etc.

These sequency elements retained are applied to the inverse FWT without amplitude distortion or other modification. Only those sequency elements associated with a signal or signal like input are passed, all others being rejected.

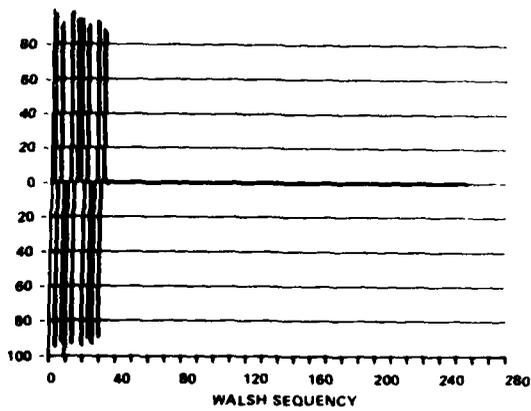
Since the input signal is decomposed into Walsh eigenfunctions, filtered, and recomposed, the filtered output signal can appear as a "squared up" or quantized pulse as shown in Figure 7. Thus, the WP tends to form a rectangular or staircase approximation pulse at the output, regardless of input pulse shape.



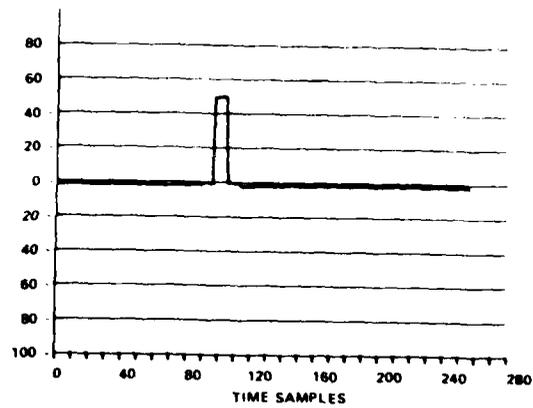
HIGH SNR PULSE IN TIME DOMAIN



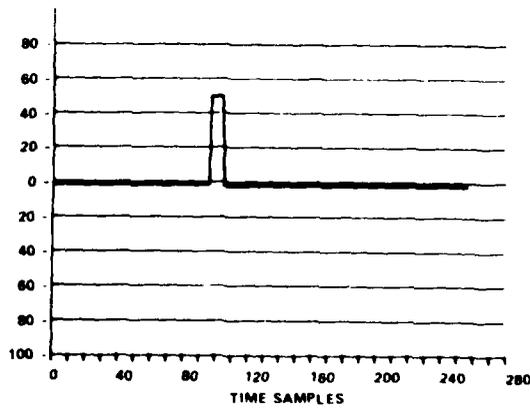
HIGH SNR PULSE IN SEQUENCY DOMAIN



FILTERED HIGH SNR PULSE IN SEQUENCY DOMAIN



FILTERED HIGH SNR PULSE IN TIME DOMAIN



FILTERED AND THRESHOLED HIGH SNR PULSE IN TIME DOMAIN

Figure 6. Walsh Filtering of High SNR Pulse

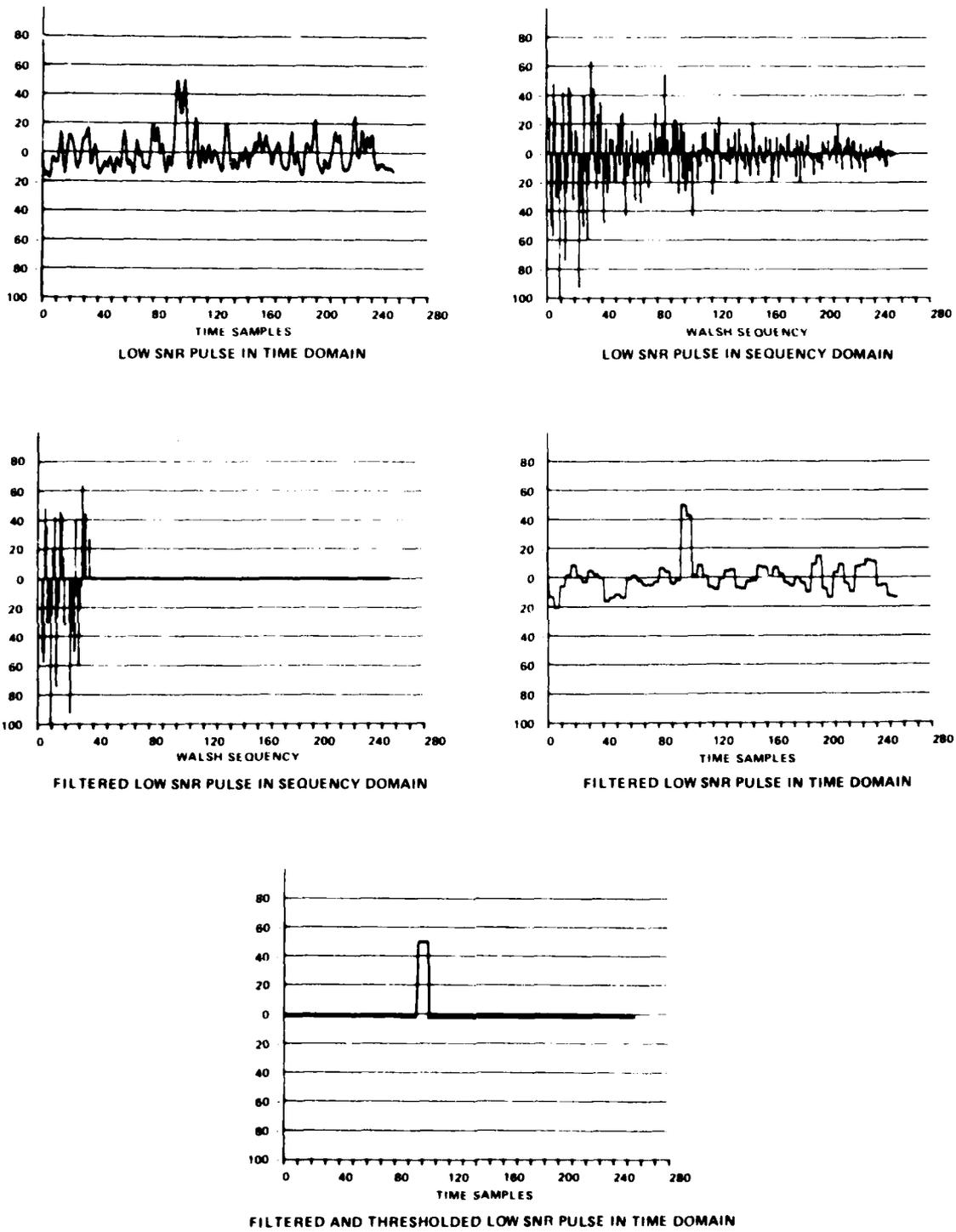


Figure 7. Walsh Filtering of Noisy Pulse

Section III

SYSTEM DESCRIPTION

The Walsh Preprocessor System consists of a Filter Channel, a Delay Channel, an I/O panel, and a Power Supply all of which are mounted in a movable rack as shown in Figure 8. The Filter Channel contains the pulse detection and filtering circuitry while the Delay Channel generates a delayed and gated video output. An Input/Output (I/O) panel provides front panel access to the I/O connections present on the rear of the Filter Channel and Delay Channel, and the entire system is powered by the Power Supply. Each of these units is described in detail in the following sections using the block diagram of Figure 9.

FILTER CHANNEL.

The Filter Channel shown in Figure 10, is the core of the WP System for it is the pulse detector and filter. The video input to this unit is matched in voltage range and impedance using the front panel controls. The impedance matching is accomplished using a 75 to 50 ohm pad which is selected using relays controlled by the front panel switches. The voltage range is adjusted using a 63 db range variable attenuator which is adjustable in 1 db steps. This attenuator also compensates for the loss through the impedance matching pad for the 75 ohms input. The vernier gain control changes the attenuator value in 1 db steps from the nominal position for each voltage range. The purpose of this circuitry is to adjust all input voltages to between 0 and +2v at 50 ohms. The input bandwidth of the channel is adjusted to less than one-half of the digitizing rate to prevent aliasing. The input signal anti-aliasing filtering is performed by a fixed 9.3 MHz low pass filter in series with a variable low pass filter for the four lowest digitizing rates. The variable low pass filter is an analog circuit which is controlled by the pulse width range. The input to the Analog to Digital Converter can be monitored at the Test A/D point and should be adjusted for signal amplitudes of +2.0 volts.

Input voltage range indicators have been provided in the WP. An UNDER-RANGE light indicates that insufficient input noise is being applied to the WP A to D converter; hence the VOLTAGE RANGE attenuator should be rotated counter-clockwise. An OVERANGE light indicates that the ADC is being saturated; hence the VOLTAGE RANGE attenuator should be rotated counter-clockwise. When both the UNDERANGE and OVERANGE lights are on, a noiseless, strong signal is being applied to the WP. It must be remembered that the WP is principally used for weak, noisy pulses.

The WP Filter Channel contains two (2) built-in default values of detection thresholds (false alarm rates) for each pulse width range, plus it can be externally programmed for other threshold values. Either filtered and unfiltered sequency spectrum outputs, in either normal (bipolar) or power (unipolar) formats, are available by front panel switch selection.

The A/D converter is a five bit unit capable of a 50 MHz sample rate. The unit is clocked from the system clock circuit and provides the five bit word in two's complement form with +1.0 volts as the center of the A/D range. The

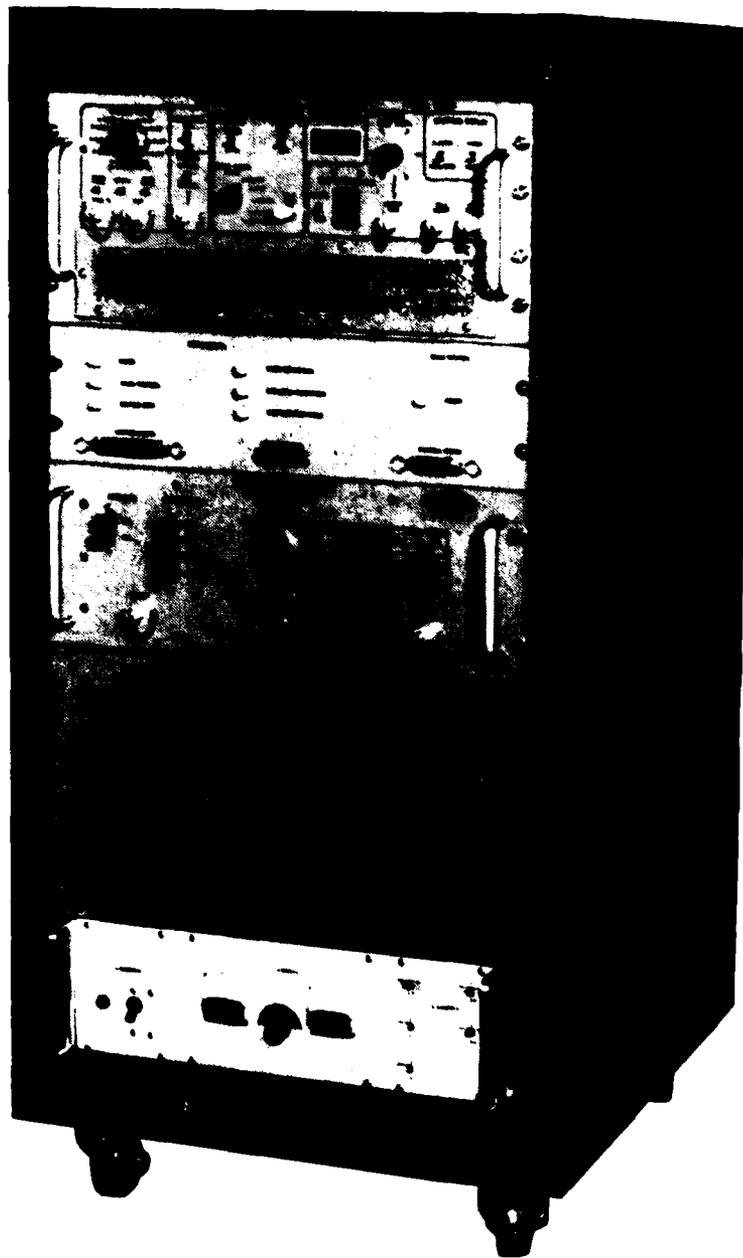


Figure 8. Walsh Preprocessor System

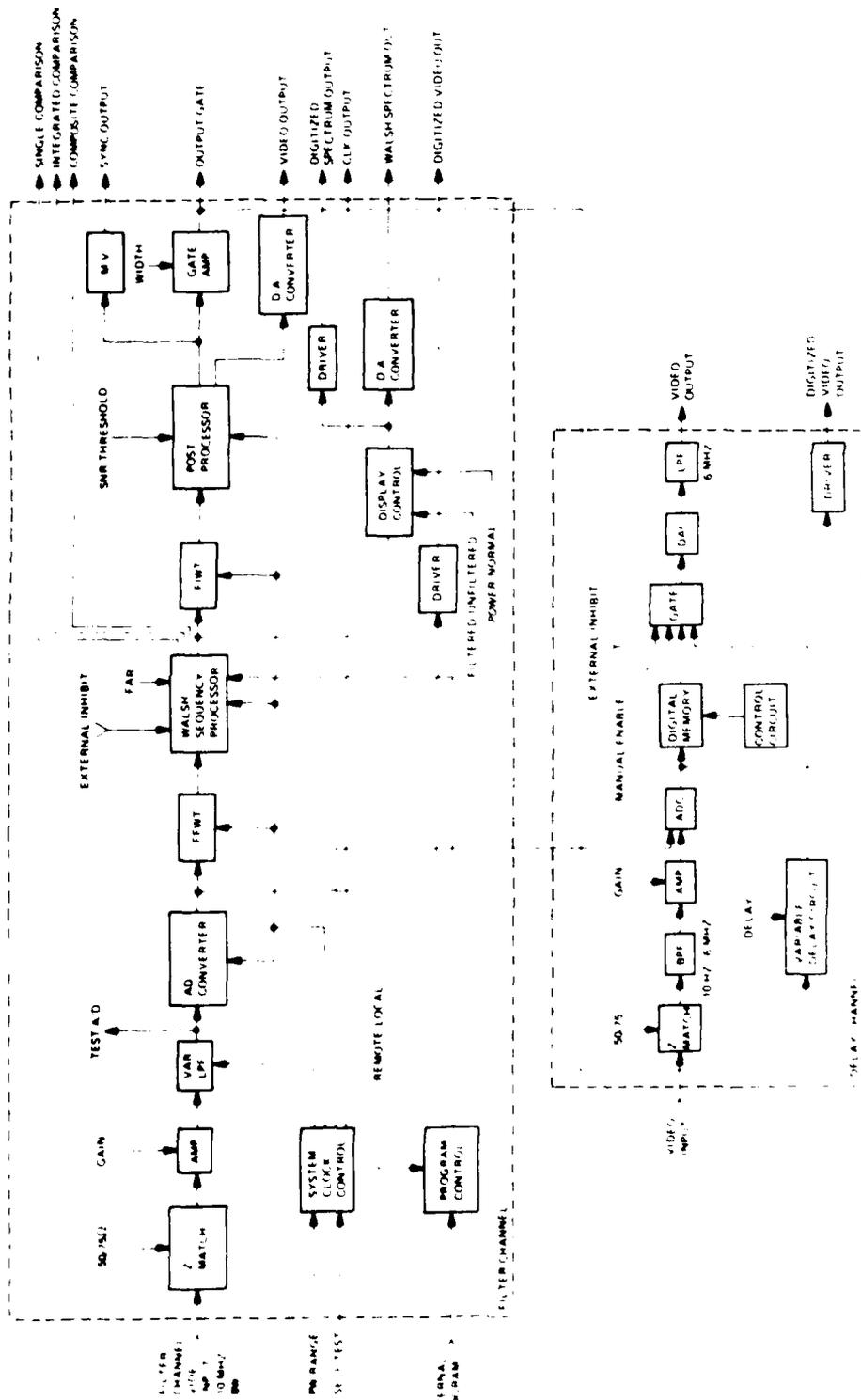


Figure 9. Walsh Preprocessor Block Diagram

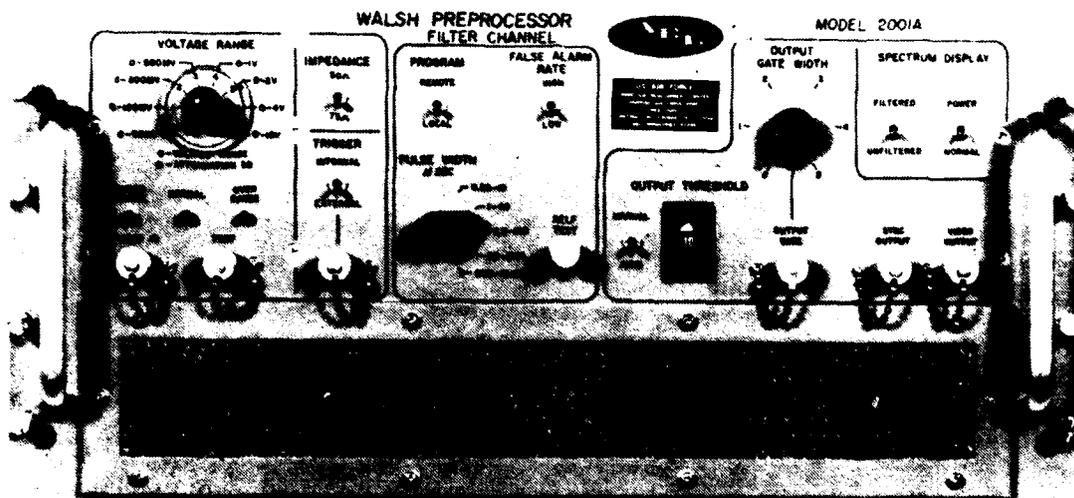


Figure 10. Filter Channel Front Panel

circuit uses a standard parallel conversion technique to achieve the required operating speed.

The Forward Fast Walsh Transform (FFWT) is performed using two's complement arithmetic in a fixed point implementation. Each level of the FFWT increases the word size by one bit so that the output of the eighth level provides thirteen bit data words. Each of the eight levels is very similar and contains an input and output memory plus an adder and subtractor. The memories are Emitter-Coupled-Logic (ECL) random access memories (RAM), which are used as shift registers. The length of the shift register is 128 words in level one and decreases by one-half for each higher level. The adders and subtractors are ECL 4 bit arithmetic logic units (ALU) cascaded to accept the longer word lengths. The thirteen bit word is reduced to a ten bit word by truncation of the lower three bits since the shorter word contains adequate signal information for the filtering process.

The Walsh Sequency Processor or Sequency Spectrum Processor performs both the analysis and filtering as described in Section 2. Three ratios of sequency averages are computed for each transform. The sums of the first 4, 16, 64 and 256 Walsh coefficients are calculated in real time using four separate accumulators and two adders. The four averages (Ave 4, 16, 64 and 256) are computed simply by shifting the binary point to the left 2, 4, 6 and 8 places, respectively. The ratios $\frac{\text{Ave 256}}{\text{Ave 4}}$, $\frac{256}{16}$, and $\frac{256}{64}$ are then calculated by

division in the Central Processing Unit (CPU) section of the circuit. The analysis is completed by comparisons of the ratios against the set of processing

values. The arithmetic and comparison operations are performed in the CPU portion of the spectrum processor. This circuit is configured similar to a computer and has multiple registers, an arithmetic unit, a data bus and an instruction bus. The CPU operates at the system digitizing rate which is a maximum of 20 MHz. Comparisons are performed by subtraction and looking for a sign change. The result of this analysis is to provide a decision to select a set of filtering values to be used on the sequency domain which has meanwhile been reordered into ascending sequency and stored. The sequency is filtered one line at a time starting with the Walsh 1 term (two zero crossings). The lines are compared both individually and in groups against thresholds and any line below threshold is set to zero. The comparison and filtering of each line takes one clock period such that the filtered output occurs at the same word rate as the digitized output. The output of the filter is the input to the Inverse FWT. A maximum of 128 Walsh lines are required for the IFWT; thus, the filter operates at a 50% duty cycle.

The Inverse FWT is identical to the FFWT except that it has only seven levels, instead of eight, and the word sizes are larger. The input word is nine bits and the output has been truncated to twelve bits by dropping the four most significant bits at the output of the last level.

The post processor reorders the IFWT output into time sequence and stores the data. The peak value of each transform is detected during this time and is used to calculate the time domain threshold. This threshold, which is used to filter the time domain, is determined by the peak value, average value and a constant previously selected at the analysis of this transform. The threshold is calculated using the equation:

$$\text{Threshold} = (\text{Peak} - \text{Ave}) \times K + \text{Ave}$$

$$\text{where } K < 1.0$$

The output time domain is generated by filtering the stored time values, one sample at a time, using the threshold value. This filtering is done at one-half of the system clock rate such that the output time scale is equal to that of the input. A manual threshold can be used in place of the calculated value through the front panel controls.

The video output is provided both as a logic level gate and as an analog video signal. The analog video signal is generated by passing the post processor output through a D/A converter with a 50 ohm output driver. The analog video output is a linear reproduction of the relative input amplitude.

The gate output is a logic level gate which corresponds to the time threshold decision. This output can be stretched in pulse width at the trailing edge using the front panel control. A narrow sync pulse is also generated using the logic level gate as a trigger. The gate output is used by the Delay Channel to gate the delayed video signal.

A second D/A converter and 50 ohm output driver is used to generate a Walsh Spectrum display. This output indicates the filtered spectrum as it enters the IFWT. An internal switch allows the sequency filter to be bypassed whereby the output then displays the complete Walsh spectrum.

The complete system clocking is developed from a single clock circuit. This circuit uses a crystal controlled 20 MHz oscillator as the basic reference source from which all clocks are derived. The clock signals are distributed to all the boards using differential twisted pair lines. An external clock source can be used and is selected using an internal switch.

DELAY CHANNEL

The Delay Channel, shown in Figure 11, provides the delay and gating functions for the video input. The gating signal is generated by the Filter Channel and applied internally to the Delay Channel. The Delay Channel presently has five fixed delays which permit operation with all pulse width ranges. Each fixed delay is adjustable by up to 7 advance or 8 retard clock samples.

The video input can be matched to peak voltage ranges of 0-1, 0-2, 0-4 and 0-10 volts with input impedance of 50 or 75 ohms. All of these controls are mounted on the front panel of the Delay Channel. The input impedance is adjusted to 50 ohms using a 75 to 50 ohm matching pad as required. This pad is selected by relays operated by the front panel controls. The voltage ranges

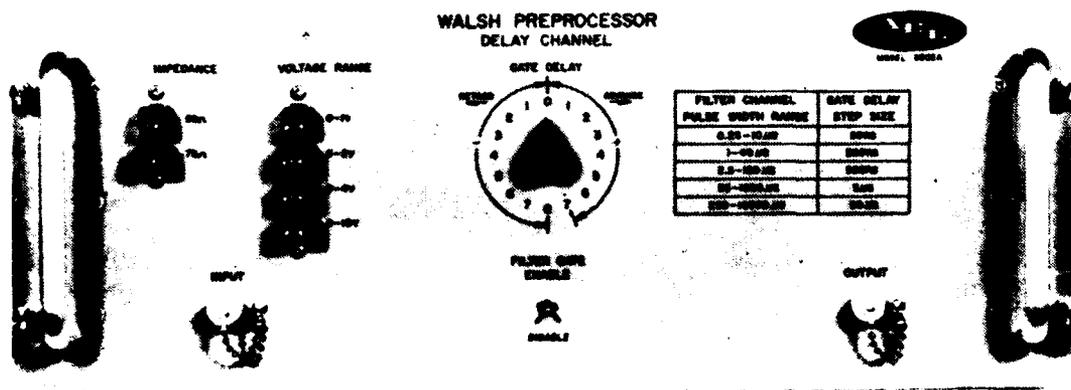


Figure 11. Delay Channel Front Panel

are set using fixed attenuators and relays. A 10 Hz to 6 MHz bandpass filter is used to condition the signal. The signal is converted to an eight bit digital word and stored in a digital delay memory. The memory cycle time is derived from the Filter Channel clock to provide the digital memory with a delay time that tracks the processing time in the Filter Channel. The memory data is recalled eight clock times before the corresponding OUTPUT GATE is available from the Filter Channel. The gate is delayed from zero to 15 clock times as selected by a front panel rotary switch. This allows relative movement between the gate and the delayed signal. The gate may precede the signal by up to eight clock times or follow the signal by up to seven clock times. A front panel switch enables the delayed gate from the Filter Channel to gate the delayed signal. The gated memory data is converted back to bipolar video form. The video output stage incorporates a 6 MHz low pass filter designed to drive a 50 ohm load.

POWER SUPPLY

The system power supply was specified by AEL and manufactured by Lambda Electronics. The unit contains the WP ON-OFF switch, which is integral with a circuit breaker, an indicator light and a switchable ammeter and voltmeter for all the supplies. The power supply generates voltage of ± 20 , +5, -2, and -5.2 volts and Section IV of this report describes the controls and operation. The unit consists of five commercial supplies which were mounted into a single rack. The +5, -2, and -5.2 volt supplies are of the switching regulator design while the ± 20 volt supplies are linear type units due to the requirements for low ripple on these voltages. Although the power supply does not require forced air cooling, the unit should never be mounted such that the natural convection cooling air flow is restricted in any way. The power supply also has a switched AC output which is used to power the Filter Channel and Delay Channel cooling fans. All the supplies have individual over-voltage protection circuits and the switching supplies also have thermal overload protection.

The input power requirements for the WP system are:

Voltage:	105 to 130 VAC, single phase
Frequency:	47 to 63 Hz
Power:	800 watts

I/O PANEL

The I/O panel provides connections to the rear mounted controls for the Filter Channel and Delay Channel from the front of the system. The panel contains only cabling and no circuitry. The controls and signals that are present on this panel are:

- 1) Delay Unit External Enable
- 2) Filter Channel External Enable
- 3) Walsh Spectrum Output

- 4) Digitized Spectrum Output
- 5) Filter Channel Digitized Video Output
- 6) Delay Channel Digitized Video Output
- 7) System Clocks

This panel is not required for WP system operation and is provided only as a convenience to the operator. If the system were to be installed where space is at a premium the panel could be eliminated.

MECHANICAL CONSTRUCTION

The WP System is mounted in a moderately sized movable rack. The Filter Channel and Delay Channels are both mounted on slides for ease of maintenance. Both units can be extended fully on their slides without removing any cables or connections.

Caution must be exercised when both the Filter and Delay Channels are fully extended on their slides, since the rack can be inadvertently tipped over if additional weight is placed on the Filter Channel.

Size and Weight

<u>Unit</u>	<u>H</u>	<u>W</u>	<u>D</u>	<u>Weight</u>
Filter Channel (Model 2001A)	8.75"	19"	22.5"	58 lbs.
Delay Channel (Model 2002A)	7"	19"	22.5"	22 lbs.
Power Supply (Assy. 13119-1)	5.25"	19"	22.5"	150 lbs.
<u>Total WP System</u>	47"	22"	24"	280 lbs.

Section IV

SYSTEM OPERATION

This section provides a description of controls and indicators, useful operation procedures based on typical applications, plus theory of operation. Procedures in this section are written to guide an operator who is familiar with both the nature of the signals to be detected and the desired output response.

CONTROLS AND INDICATORS - FILTER CHANNEL

The controls located on the front panel of the Filter Channel are grouped by function. The Input controls are on the left side of the panel, the Processing controls are in the center, and the Output controls are located on the right side of the front panel. Each control and indicator is listed and its function described in Table 1.

OPERATING PROCEDURE - FILTER CHANNEL

The Filter Channel video signal is connected to the VIDEO IN BNC and the controls set for the proper impedance, voltage range and pulse width range. The best performance is obtained when the lowest valid pulse width range is used. Table 2 shows the Filter Channel characteristics that vary with pulse width range. If the INPUT VOLTAGE range does not closely match one of the PRESET VALUES, the FINE ATTENUATION control can be used. The VOLTAGE RANGE switch would be set to the range just below the maximum signal amplitude and the attenuation control used to reduce the maximum input signal to +2.0 volts as measured at the TEST A/D BNC. The green NORMAL light should be illuminated. The voltage range and attenuation controls should be such that the maximum input voltage does not exceed +2.0 volts at the Test A/D point.

The standard setting for the FALSE ALARM RATE switch would be in the HIGH position which gives a system false alarm rate of nominally 100 per second at the 0.1 to 20 μ sec pulse width range. This setting gives the highest system sensitivity. The LOW position will give a rate of approximately 10 per second at the 0.1 to 20 μ sec pulse width range and is used when a lower probability of false alarm is desired. The false alarm rates drop non-linearity as the wider pulse width ranges are selected.

The normal setting for the output threshold is in the AUTO position where the Filter Channel continuously computes the correct time threshold. The operator can control the output level threshold manually using the thumbwheel switch.

The video output signal is available both as a TTL logic level signal, OUTPUT GATE, and as a reconstructed video signal, VIDEO OUTPUT, capable of driving a 50 ohm load. The pulse width of the TTL output can be increased

TABLE 1. FILTER CHANNEL CONTROLS AND INDICATORS

Control or Indicator	Function
1) VOLTAGE RANGE	Selection of the operating voltage range of the VIDEO INPUT signal. The ATTENUATION control must be set for zero dB.
2) ATTENUATION	This control increases the attenuation in the video input circuit in 1 dB steps to allow fine adjustment of the input voltage level.
3) IMPEDANCE	Selection of the input impedance to be either 50 or 75 ohms.
4) UNDERRANGE	This red indicator lights when the input noise level falls below the recommended minimum.
5) OVERRANGE	This red indicator lights when the input signal exceeds the range of the A/D converter.
6) NORMAL	This green indicator lights when the input signal is within the recommended range.
7) TEST A/D	510 ohm output line for monitoring the signal into the A/D converter.
8) TRIGGER Switch	Selection of either internal or external triggering.
9) TRIGGER BNC	Rising edge of a TTL compatible pulse causes the start of a Walsh Transform.
10) PROGRAM	Selection either enables or disables remote programming.
11) PULSE WIDTH	Selection of the optimum pulse width range to match the video input pulse widths.
12) FALSE ALARM RATE	Selection of either the HIGH or LOW False Alarm Rate.
13) SELF TEST	Selection causes an overrange pulse to be injected into both channels.
14) OUTPUT GATE WIDTH	This control increases the width of the OUTPUT GATE from zero to greater than 10%.
15) OUTPUT THRESHOLD Toggle Switch	Selection of the time domain threshold calculated by either the WP or the manual thumbwheel switch.
16) OUTPUT THRESHOLD Thumbwheel Switch	Control of the manual time domain threshold from a minimum value of 0 to a maximum value of 15.
17) SPECTRUM DISPLAY Switches	Selection of either FILTERED or UNFILTERED spectrum display presented in either NORMAL (bipolar) or POWER (rectified) format.
18) OUTPUT GATE BNC	Signals the presence of a pulse at the Video Output BNC with a TTL logic 1.
19) SYNC OUTPUT BNC	A 100 ns wide TTL pulse which is synchronized with the rising edge of the OUTPUT GATE.

TABLE 2. FILTER CHANNEL CHARACTERISTICS VS. PULSE WIDTH RANGE

Pulse Width Range	Digitizing Rate	Bandwidth	Delay
0.25 - 10 μ sec	20 MHz	10 MHz	58.9 μ sec
1 - 40 μ sec	5 MHz	2.5 MHz	235.6 μ sec
2.5 - 100 μ sec	2 MHz	1 MHz	589 μ sec
25 - 1000 μ sec	0.2 MHz	0.1 MHz	5.89 msec
250 - 10,000 μ sec	0.02 MHz	0.01 MHz	58.9 msec

in five steps using the OUTPUT GATE WIDTH control. The pulse width increase for each position and pulse width range is as follows:

Position	0.25-10	1-40	2.5-100	25-1000	250-10,000
0	0	0	0	0	0
1	100 nsec	0.4 μ sec	1 μ sec	10 μ sec	100 μ sec
2	200 nsec	0.8 μ sec	2 μ sec	20 μ sec	200 μ sec
3	400 nsec	1.6 μ sec	4 μ sec	40 μ sec	400 μ sec
4	800 nsec	3.2 μ sec	8 μ sec	80 μ sec	800 μ sec
5	1600 nsec	6.4 μ sec	16 μ sec	160 μ sec	1600 μ sec

The increase in pulse width always occurs at the trailing edge of the pulse. A TTL logic level synchronization pulse is available at the SYNC OUTPUT BNC. This pulse is synchronized with the leading edge of the video output signal and has a nominal width of 0.1 μ sec.

Proper Choice of Pulse Width Range

The proper WP performance will occur when the input video noise bandwidth is at least one-half the sampling rate. The sampling rate vs. pulse width range was listed in Table 2; however, a rule of thumb is that the input video noise bandwidth, as viewed on a conventional spectrum analyzer, should ideally be within 3 dB of perfectly flat from DC to a frequency equal to twice the reciprocal of the shortest pulse width of the range selected; i.e., 8 MHz for the 0.25-10 microsecond pulse width range.

Noise is shaped by any low pass filter in such a way that it begins to appear as random pulses having a width less than but approximately equal to the reciprocal of the bandwidth; as a result, the WP cannot always distinguish these improperly filtered noise pulses from real pulses, and, therefore, could produce a significantly increased false alarm rate if not compensated for by specific programming. The WP can be programmed to operate optimally from any noise bandwidth.

The input noise bandwidth of the equipment driving the Filter Channel should be determined using a conventional spectrum analyzer. The 3 dB point should be noted, and a digitizing rate (per Table 2) that is less than or equal to twice the required 3 dB noise bandwidth should be selected in order to attain maximum performance. Choosing of a sample rate less than twice the noise bandwidth cannot produce aliasing of the analog-to-digital converter since the WP has built-in anti-aliasing low pass filters.

Internal Controls

There are two internally mounted switches in the Filter Channel which are the OSC INT/EXT control and the FIL/BYP control. The normal system operation uses the internal (INT) crystal oscillator with the digitizing rates as listed in Table 2 for all of the pulse width ranges. An external clock can be used with the WP system. This signal is connected to the EXTERNAL CLOCK BNC on the rear of the Filter Channel and must have the following characteristics:

Frequency:	up to 20 MHz
Waveform:	Square Wave
Voltage:	ECL 10,000 series levels

The pulse width range used will select one of the five discrete video bandwidths shown in Table 2. The operator must recognize that the digitizing rate, at the 0.25-10 μ sec PW range, will be the external clock frequency and the rate will decrease with PW range as shown.

The second internal control is the FIL/BYP switch which selects the operational mode of the Walsh sequency filter between normal filter operation (FIL) and no sequency filtering or bypass (BYP). This mode is optimally used when the input video signal can be synchronized to the Filter Channel using the SYNC OUTPUT signal on the rear of the unit. The effect of filtering vs. bypass operation on various input signals can be demonstrated using this technique.

Remote Programming Procedure

This section describes "cause and effect" relationships of remotely programming the Walsh Preprocessor. During this discussion the reader should become familiar with the Pulse Classification Flowchart shown in Figure 12. As seen in the flowchart, the decisions determining the path of flow are based on four averages. These averages are of the first 4, 16, 64, and all 256 sequency coefficients in the Walsh Spectrum. The signature of the input data is contained in the first three averages. The average of all 256 determines a bias level for each transform. It is necessary to normalize the first three averages using the Ave 256 value before characteristics of different transforms can be compared.

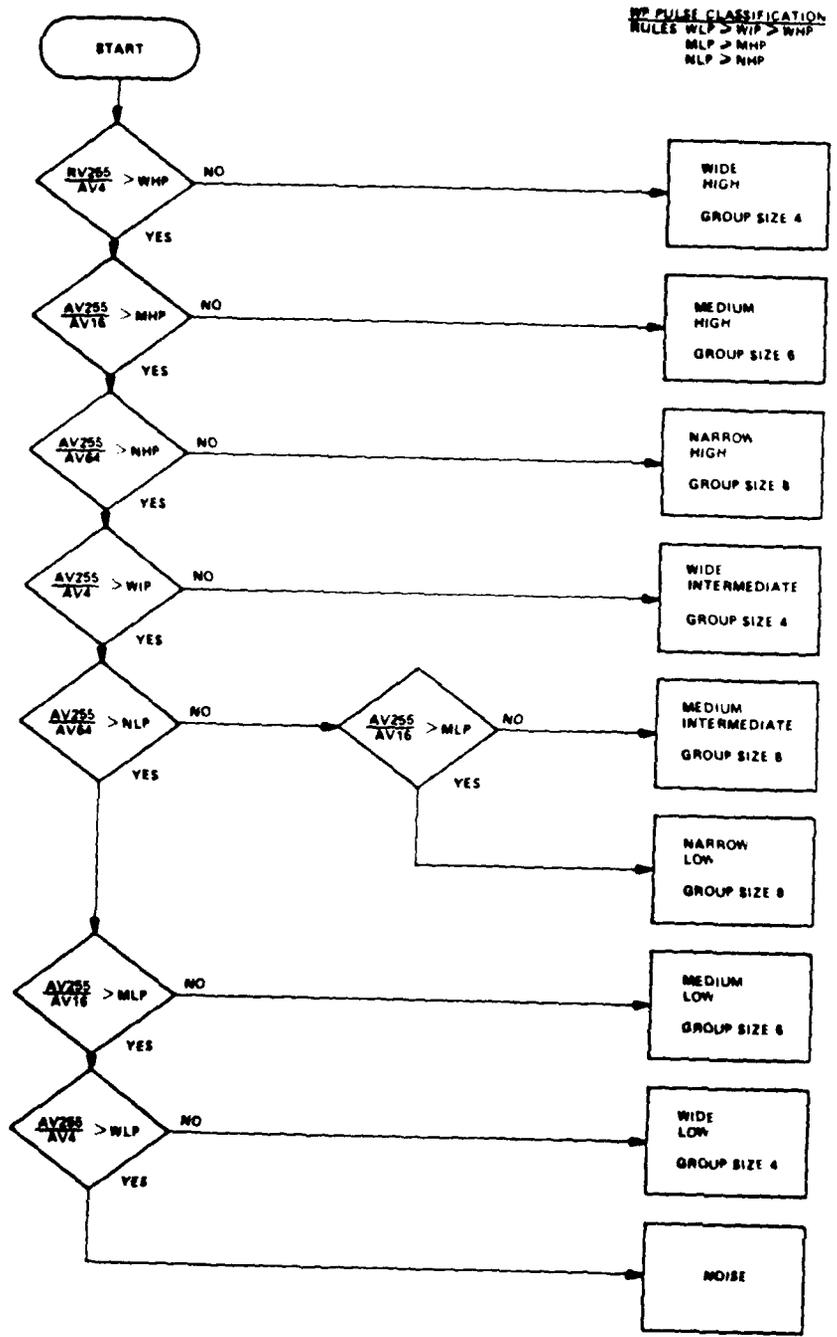


Figure 12. Pulse Classification Flowchart

The noise level of the input signal directly affects the magnitude of the Ave 256 value. When there is insufficient input noise, the value of Ave 256 drops, and not enough significant binary digits are retained to allow proper normalization. When the Ave 256 value falls below the recommended minimum value, the red UNDERRANGE light on the front panel is turned on.

The first eight of the boxes in the flowchart are for the input transforms which contain a pulse. The last box is for those transforms where no input signal was detected. The False Alarm Rate (FAR) is determined by which paths are taken when the WP receives an input of pure noise. The WP will reconstruct a pulse out of the noise received when any path other than the noise path is selected. The FAR can be adjusted using the variables in the decision blocks to change the trade-off between selecting the path of a particular pulse characteristic and the noise path.

The HIGH/LOW FAR switch on the Filter Channel selects one of two sets of path variables. However, only the three variables of low amplitude pulses (NLP, MLP, and WLP) determine the false alarm rate. The path variables should not be changed until the operator is confident that the three threshold coefficients for each pulse characteristic are adjusted properly. Any of the nine paths shown on the flowchart may be forced by the operator (providing that the UNDERRANGE indicator is not on).

CONTROLS AND INDICATORS - DELAY CHANNEL

The operating controls for the Delay Channel are listed in Table 3. The GATE DELAY rotary switch step size is dependent on the Filter Channel pulse width range. A table relating the pulse width range to the gate delay step size is indicated on the front panel.

OPERATING PROCEDURE - DELAY CHANNEL

The Delay Channel can be operated with either the same video signal as the Filter Channel, or a second video source which is synchronized with the Filter Channel input. The video INPUT and OUTPUT BNC connections are clearly marked on the Delay Channel front panel. The input IMPEDANCE should be matched to the source, and the VOLTAGE RANGE set to the proper value.

The FILTER GATE toggle switch is set to ENABLE in the normal mode of operation. The Delay Channel provides a delay which is eight clock times longer than the processing delay through the Filter Channel. This delayed signal is gated with the Filter Channel OUTPUT GATE. The GATE DELAY rotary switch allows the operator to adjust the gate about both sides of the delayed signal. When the FILTER GATE toggle switch is in the DISABLE position, the input signal is passed with delay but without gating.

THEORY OF OPERATION - DELAY CHANNEL

The video signal enters the INPUT BNC first and goes through a 50/75 ohm impedance matching network. After matching, the signal has a 50 ohm impedance and is attenuated 6 dB from the input signal. Next, the signal

TABLE 3. DELAY CHANNEL CONTROLS AND INDICATORS

Control or Indicator	Function
IMPEDANCE	Selection of either 50 or 75 ohm input impedance.
VOLTAGE RANGE	Selection of peak input voltage swing in steps of 1, 2, 4 or 10 volts.
GATE DELAY	Adjustment of the Filter Channel Gate with respect to the delayed signal.
FILTER GATE	Selection of either gating the delayed video signal with the Filter Channel Gate (ENABLE) or passing all input signals with a constant time delay (DISABLE).

is passed through a series of attenuators selected by the voltage range switches on the front panel. The signal at this point has a maximum swing of 0.5 volts peak to peak. The normalized signal passes through a 10 Hz to 6 MHz band pass filter and then is amplified by a factor of four. (At this point, the video signal is multiplexed with a self test pulse which is generated and selected by the Filter Channel when the SELF TEST push button is activated.) This signal goes to the A/D converter where it is digitized with eight bit resolution. The Digital Delay Circuit receives the A/D data, buffers it, sends it to the I/O Panel, and stores the data in a first in first out (FIFO) memory. The FIFO is set for a fixed delay which is eight clock times longer than the delay through the Filter Channel.

The gate from the Filter Channel is internally connected to a variable delay (0 to 15 clock times) circuit on the Digital Delay Board. The variable delay is controlled by the front panel rotary switch. The delayed filter gate can be used as a window which enables the FIFO output. This function is controlled by the FILTER GATE ENABLE/DISABLE toggle switch on the front panel. When in the DISABLE position, all of the FIFO data is passed; in the ENABLE position, only the FIFO output which is concurrent with the delayed filter gate is passed to the D/A converter.

TYPICAL APPLICATION OF WP SYSTEM

The WP System requires a post-detection video signal used as the Filter Channel input in all modes of operation. This input can typically be the output of a receiver, wideband tape recorder, spectrum analyzer, etc. The input impedance, voltage range and sample rate (pulse width range) of the Filter Channel must be matched to the input signal parameters. The Filter Channel output is available both as a reconstructed analog video signal and a digital logic level gate, both of which can be used directly. In this mode of operation the WP is operating as a standard filter with a low SNR input and a high SNR output.

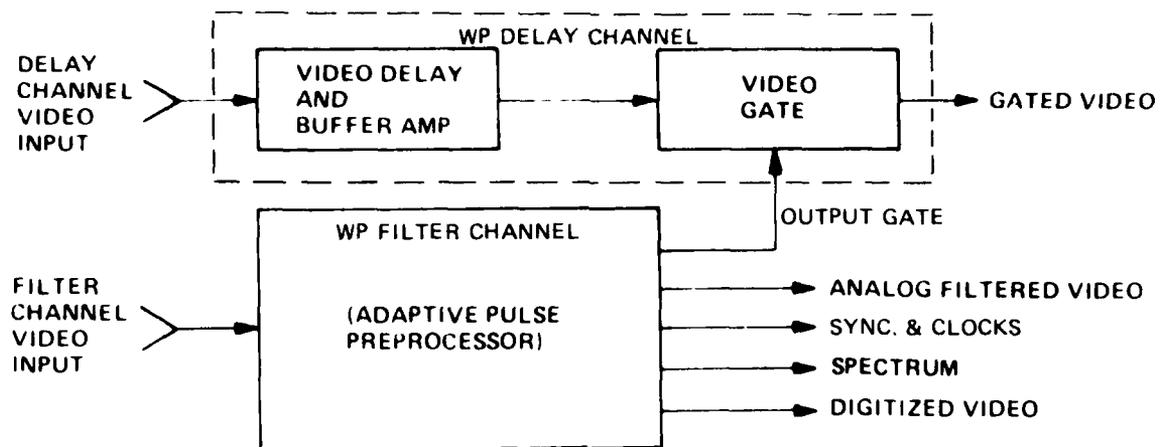


Figure 13. Postdetection Video Processing

The WP System is also capable of delaying and gating a video signal. Figure 13 shows the I/O connections for the video application. The Filter Channel and Delay Channel can be the same or different video signals. If they are not the same signal, the time skew between the two should be a maximum of 1.5 microseconds to permit proper adjustment of the system. The gated video input has dedicated and separate controls for impedance and voltage level.

Section V

TEST RESULTS

INTRODUCTION

This section describes the results of Walsh Preprocessor (WP) testing for the three interrelated parameters of: probability of detection (P_D), probability of false alarm (P_{FA}), and input signal-to-noise ratio (SNR). There are several other untested parameters of importance; however, a thorough testing program to completely evaluate the performance of the WP system requires an extended period of time using a variety of signal types and parameters. This testing program will be performed by the USAF in later efforts at FTD.

This section describes the tests performed during the WP system checkout phase. The test results are presented in a graphical format which illustrate the WP performance for several values of pulse width and signal to noise ratio. The tests were concentrated on P_D , P_{FA} , and SNR. No quantitative evaluation was made of the parameter estimation (pulse width and time of arrival) properties of the WP system which may be of equal or greater importance.

DESCRIPTION OF TESTS

The delivered WP was preset at two selectable false alarm probabilities: 4×10^{-4} (high) and 10^{-6} (low) measured at all sample rates (pulse width ranges). The pulse width ranges that were extensively tested were the 0.25 - 10 μ sec and the 1 - 40 μ sec ranges. For each range and P_{FA} , four (4) values of pulse width were used with four (4) values of P_D at each pulse width. The pulse width was measured visually on an oscilloscope and the input SNR was calculated as the ratio of peak signal to RMS noise. A detailed block diagram of the test set-up is shown in Figure 14. The P_{FA} is calculated as the counted False Alarm Rate (FAR), per second, divided by the sample rate in Hz. The false alarm probabilities were measured for both the 0.25 - 10 μ sec and the 1 - 40 μ sec pulse width ranges. The P_D was calculated as the ratio of the number of output to input pulses. The number of output pulses was measured by a counter whose input was gated to ensure that the output pulse occurred during the correct time interval and with a maximum count of one.

PROBABILITY OF DETECTION VS SNR

Figures 15 through 18 are plots of SNR versus P_D for the four pulse widths. The test results, as expected, indicate that as pulse width is increased the input SNR required for a given P_D is reduced. The high and low FAR settings give curves which are similar in shape, but the sensitivity at the higher FAR is better by approximately 1 dB at the 0.25 - 10 μ sec range and 3 dB at the 1 - 40 μ sec range. For a given pulse width, the P_D increases as the input SNR is raised.

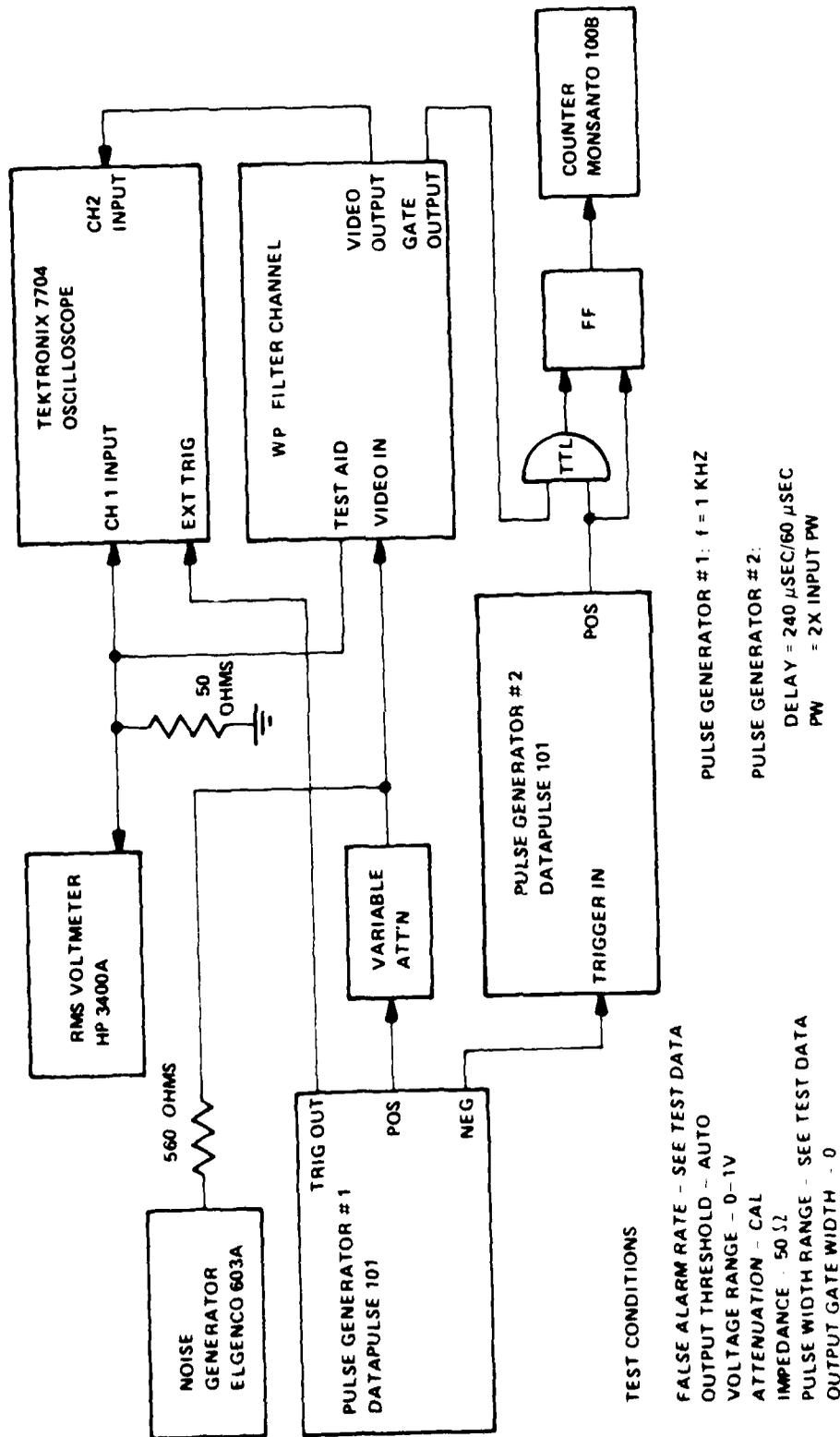


Figure 14. WP Performance Test Setup

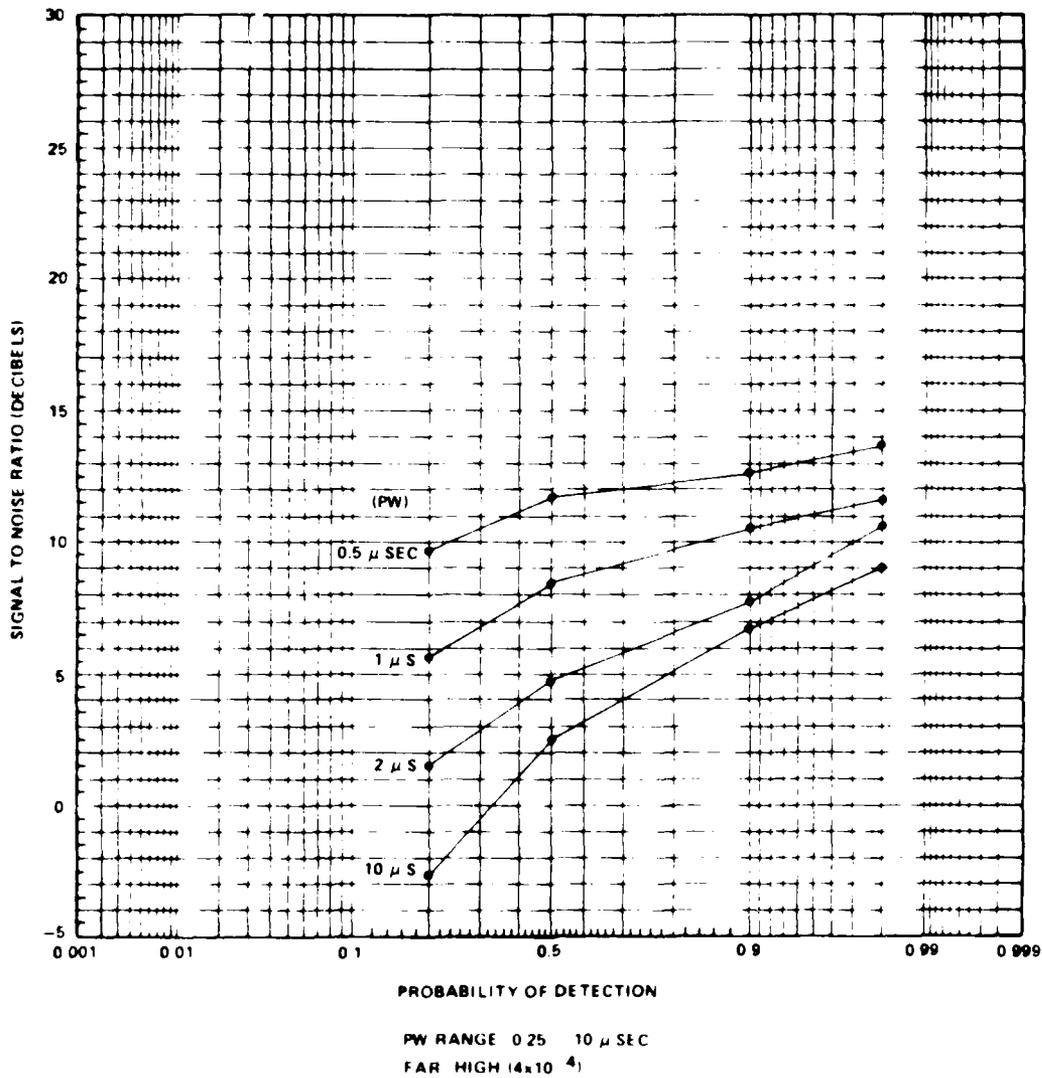


Figure 15. SNR vs. P_D , High FAR, 0.25 - 10 μ sec

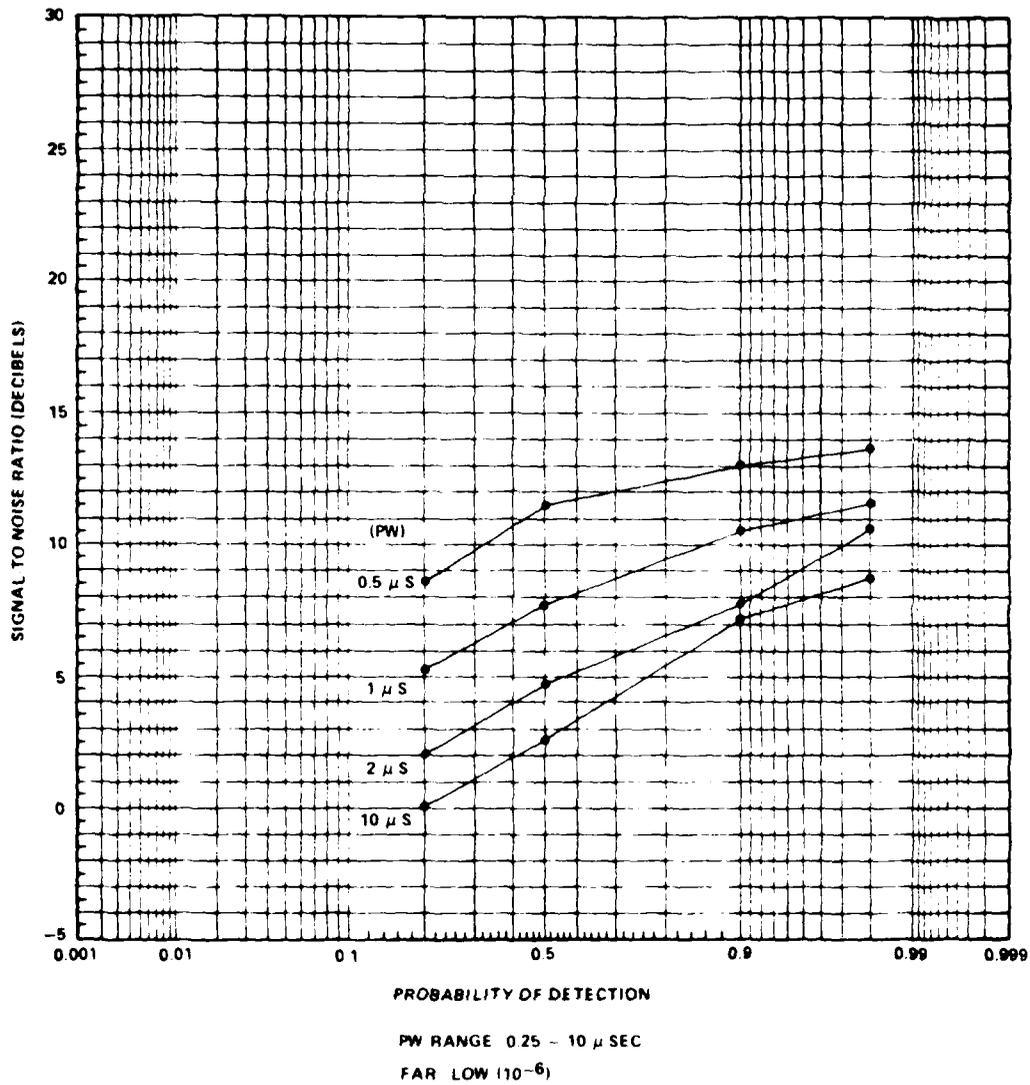


Figure 16. SNR vs. P_D , Low FAR, 0.25 - 10 μ sec

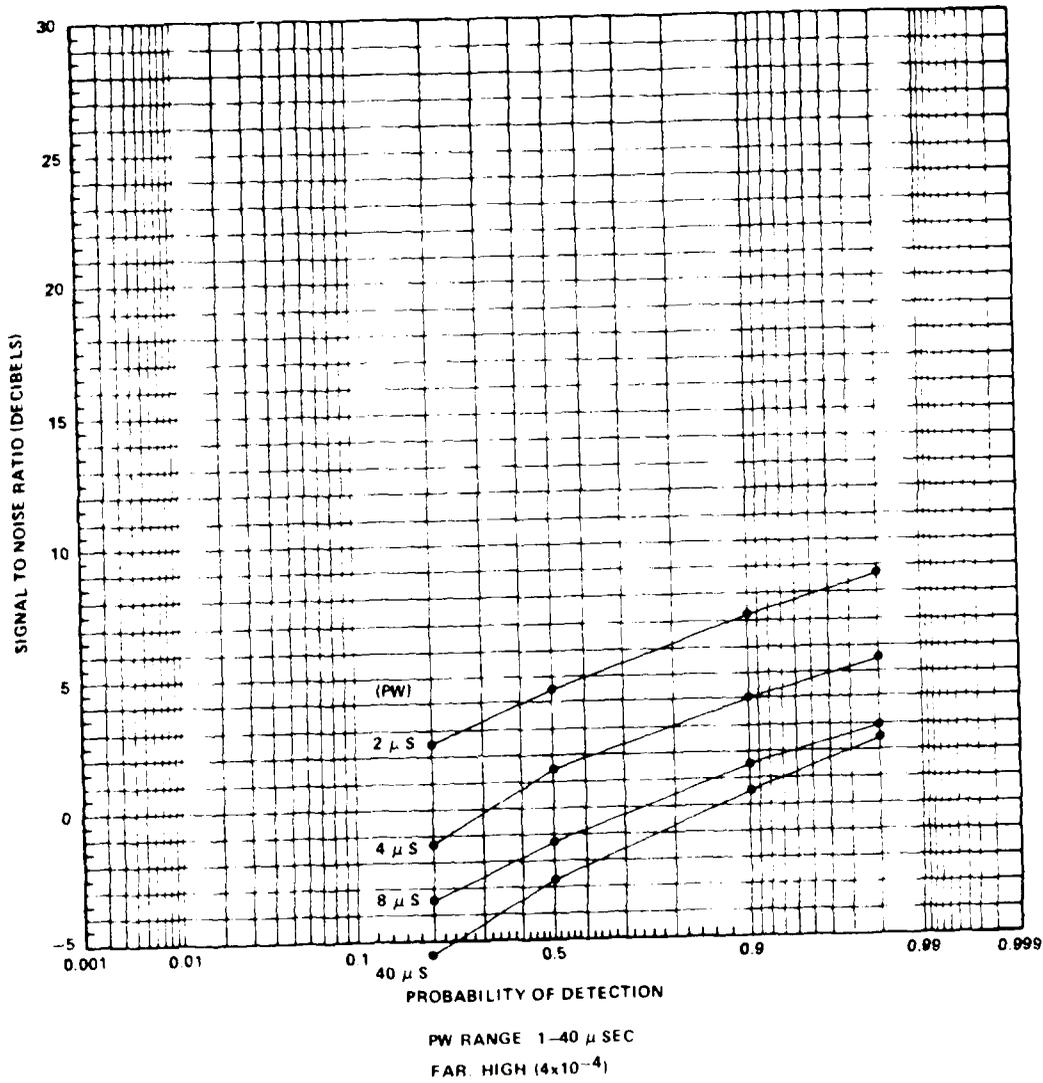


Figure 17. SNR vs. P_d , High FAR, 1 - 40 μ sec

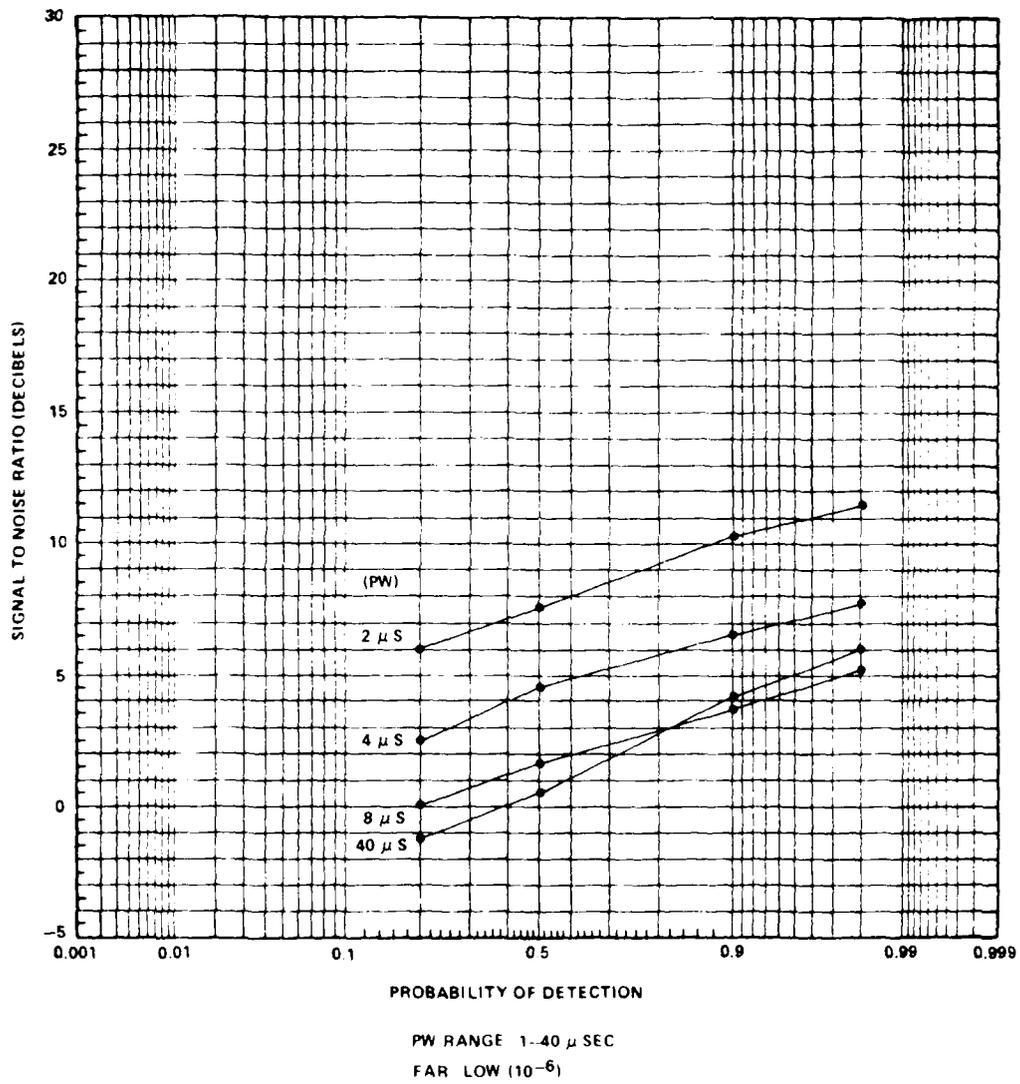


Figure 18. SNR vs. P_D , Low F/R, 1-40 μ sec

A comparison between the two pulse width ranges for the same FAR setting shows curves which are very similar when the product of input pulse width and sampling rate is considered. For example, a 40 μ sec pulse at 5 MHz (1 - 40 μ sec range) should theoretically be equivalent to a 10 μ sec pulse at 20 MHz (0.25 - 10 μ sec), in terms of the time bandwidth product and these two sets of curves should be highly similar. The differences noted are significant and attributed to the lack of a flat 10 MHz noise source for the 0.25 - 10 μ sec range; the excellent performance of the 1 - 40 μ sec range is considered to be typical.

The comparison of the above test results against a conventional pulse detection system currently in use is not an easy task. Almost all of the published data concerns probability of detection without any regard for pulse parameter estimation such as pulse width or time of arrival. If a comparison is made solely on the basis of P_D , the curves shown in Figure 19* can be used with modifications. The SNR shown is at IF and should be corrected to a video SNR using the following approximate equation for video detector SNR degradation:

$$\text{SNR video} = \frac{(\text{SNR IF})^2}{1 + (\text{SNR IF})}$$

This equation shows that at high SNR the two ratios are essentially equal and at low SNR there can be several dB differences between them with the IF SNR always being higher. The false alarm rates at the 20 MHz sample rate were 4.0×10^{-4} and 1.0×10^{-6} calculated as the ratio of the average number of false alarms per second to the video bandwidth with noise but no signal present. A comparison between the test data and Figure 19 shows the following differences in sensitivity or processing gain.

PW = 0.25 - 10 μ sec Range						
High FAR ($P_{FA} = 4 \times 10^{-4}$)						
Mode	$P_D = 0.2$		$P_D = 0.5$		$P_D = 0.9$	
	Actual (dB)	Improvement (dB)	Actual (dB)	Improvement (dB)	Actual (dB)	Improvement (dB)
Normal SNR (IF)	17.0	--	20.0	--	22.5	--
Normal SNR (Video)	16.9	--	19.96	--	22.5	--
WP, 10 μ sec PW	7.5	9.5	12.5	7.5	16.8	5.7
WP, 2 μ sec PW	11.5	5.5	14.7	5.3	17.8	4.7
WP, 1 μ sec PW	15.7	1.3	18.4	1.6	20.6	1.9

Low FAR ($P_{FA} = 10^{-6}$)						
Mode	$P_D = 0.2$		$P_D = 0.5$		$P_D = 0.9$	
	Actual (dB)	Improvement (dB)	Actual (dB)	Improvement (dB)	Actual (dB)	Improvement (dB)
Normal SNR (IF)	20.0	--	21.5	--	23.5	--
Normal SNR (Video)	19.96	--	21.47	--	23.5	--
WP, 10 μ sec PW	10.0	10.0	12.7	8.8	17.2	6.3
WP, 2 μ sec PW	12.0	8.0	14.8	6.7	17.9	5.6
WP, 1 μ sec PW	15.3	4.7	17.8	3.7	20.6	2.9

* Reference: M.I. Skolnik, Radar Handbook, McGraw-Hill 1970, p. 2-19.

PW = 1.0 - 40 μ sec Range

High FAR ($P_{FA} = 4 \times 10^{-4}$)

Mode	$P_D = 0.2$		$P_D = 0.5$		$P_D = 0.9$	
	Actual (dB)	Improvement (dB)	Actual (dB)	Improvement (dB)	Actual (dB)	Improvement (dB)
Normal SNR (IF)	17.0	-	20	-	22.5	-
Normal SNR (Video)	16.9	-	19.96	-	22.5	-
WP, 40 μ sec PW	4.5	12.5	7.2	12.8	10.6	11.9
WP, 8 μ sec PW	6.6	10.4	8.8	11.2	11.6	10.9
WP, 2 μ sec PW	12.5	4.5	14.5	5.5	17.2	5.3

Low FAR ($P_{FA} = 10^{-6}$)

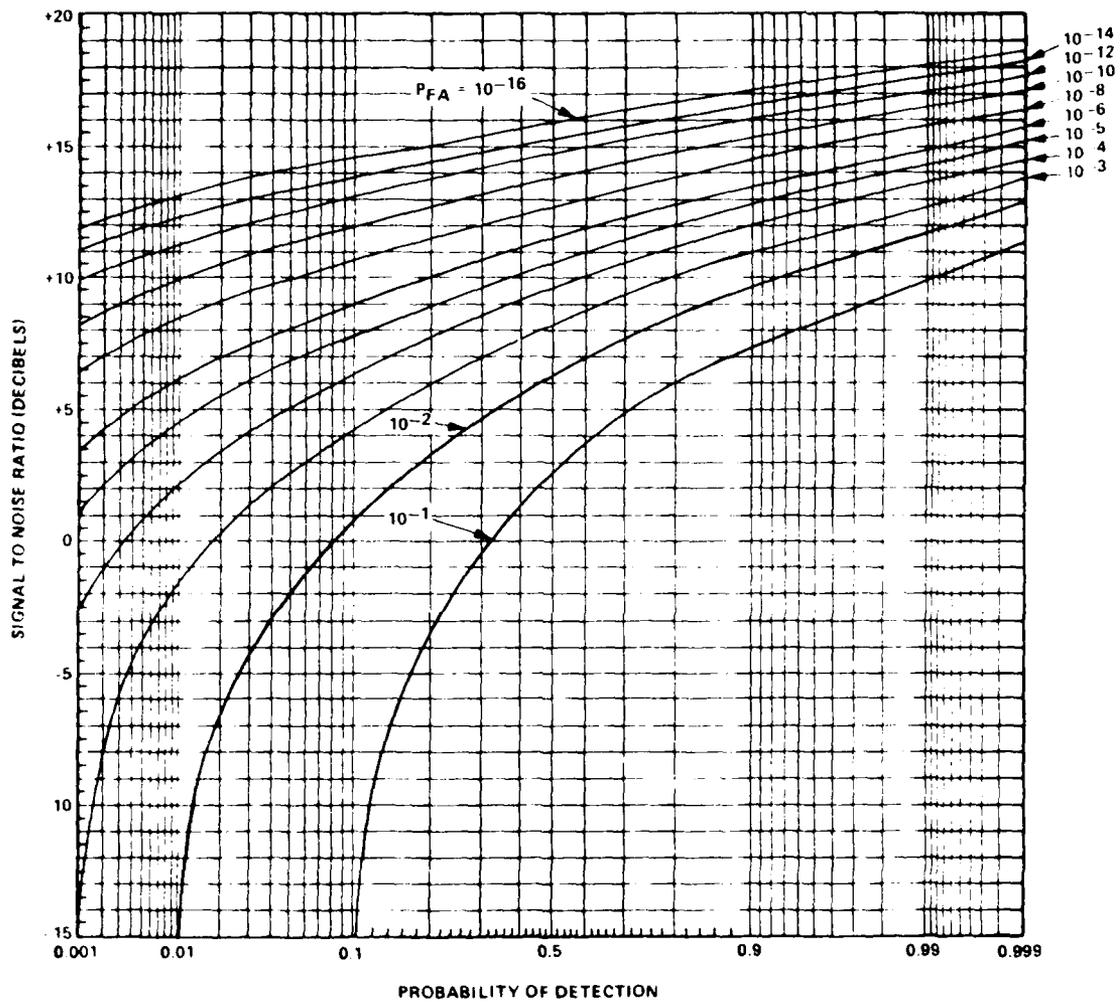
Mode	$P_D = 0.2$		$P_D = 0.5$		$P_D = 0.9$	
	Actual (dB)	Improvement (dB)	Actual (dB)	Improvement (dB)	Actual (dB)	Improvement (dB)
Normal SNR (IF)	20	-	21.5	-	23.5	-
Normal SNR (Video)	19.96	-	21.47	-	23.5	-
WP, 40 μ sec PW	8.9	11.1	10.6	10.9	14.1	9.4
WP, 8 μ sec PW	10.0	10.0	11.8	9.7	13.8	9.7
WP, 2 μ sec PW	16.0	4.0	17.7	3.8	20.3	3.2

As the test data shows, the difference between the theoretical SNR and the actual WP data varies between 12.8 dB at the high FAR in the 1 - 40 μ sec PW range down to 2.9 dB at the low FAR in the 0.25 - 10 μ sec PW range. That is, the WP improvement is between 2.9 dB and 12.8 dB, dependent upon the detection parameters chosen.

These tests show the very significant detection capability improvement of the WP system, even though they must be treated as approximate values due to the visual measurement potential inaccuracies involved. Furthermore, the performance is expected to improve as the hardware becomes refined.

VISUAL SIGNAL DATA

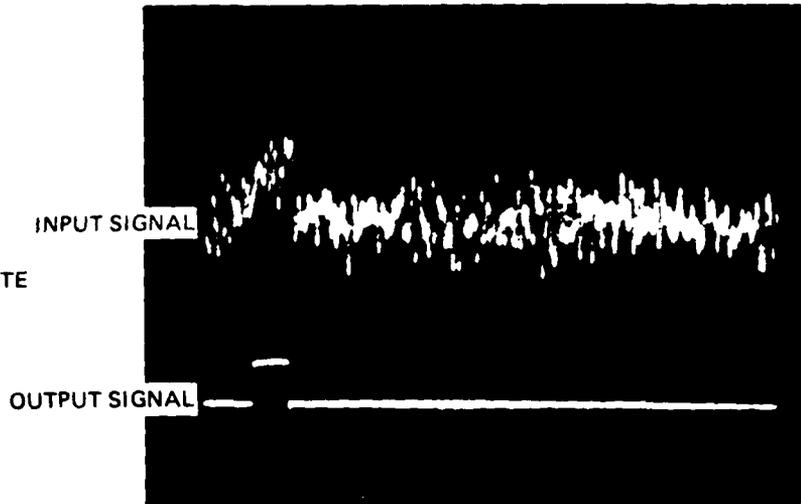
Figures 20 through 27 show WP performance widths under various input pulses and random noise levels, at a 2.5 MHz video bandwidth (1 - 40 μ sec PW range) and 10 MHz video bandwidth (0.25 - 10 μ sec PW range), using the default threshold values. These figures illustrate the ability of the WP to correctly detect a pulse embedded in noise.



Required signal to-noise ratio at the input terminals of a linear-rectifier detector as a function of probability of detection for a single pulse, with the false alarm probability as a parameter. A nonfluctuating signal is assumed.

Figure 19. Theoretical SNR vs. P_D

2.5 MHz BAND WIDTH
4 X 10⁻⁴ FALSE ALARM RATE
4 μ s PULSE WIDTH



2.5 MHz BAND WIDTH
4 X 10⁻⁴ FALSE ALARM RATE
13 μ s PULSE WIDTH

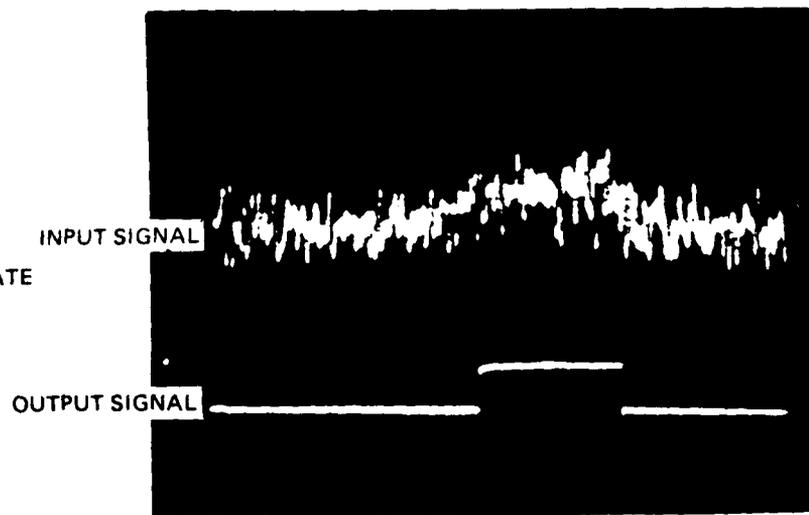
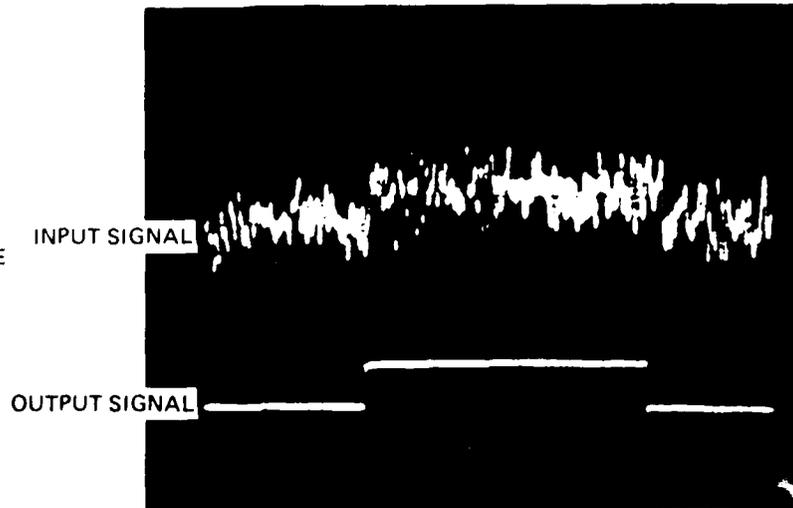


Figure 20. Walsh Preprocessor Performance at 4 μ sec and 13 μ sec Input Pulse Widths for 2.5 MHz Band Width

2.5 MHz BAND WIDTH
4 X 10⁻⁴ FALSE ALARM RATE
28 μ s PULSE WIDTH



2.5 MHz BAND WIDTH
4 X 10⁻⁴ FALSE ALARM RATE
1.5 μ s PULSE WIDTH

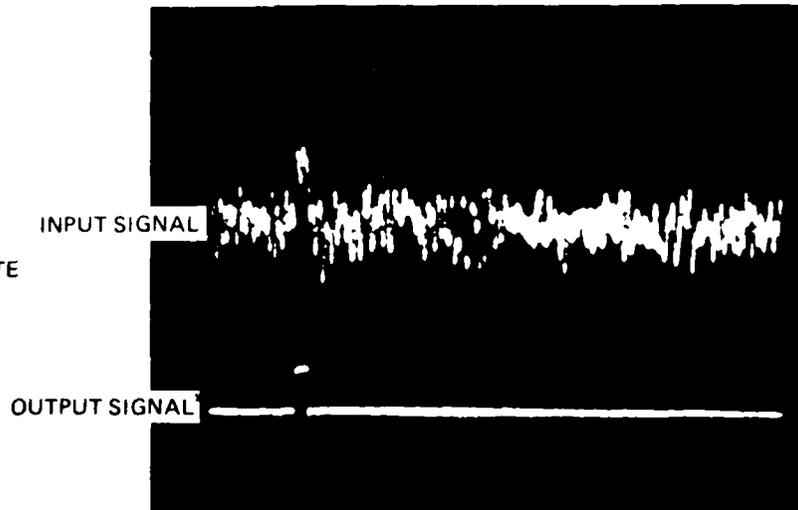
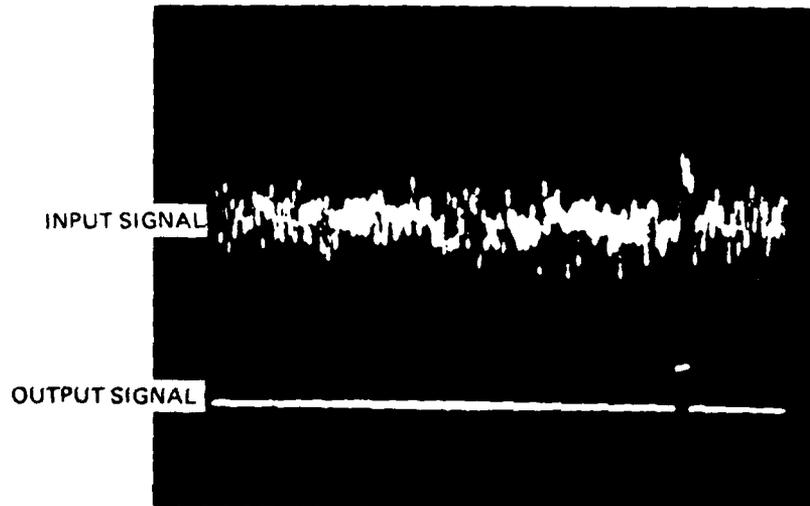


Figure 21. Walsh Preprocessor Performance at 28 μ sec and 1.5 μ sec Input Pulse Widths for 2.5 MHz Band Width

2.5 MHz BAND WIDTH
4 X 10⁻⁴ FALSE ALARM RATE
1.5 μ s PULSE WIDTH



2.5 MHz BAND WIDTH
4 X 10⁻⁴ FALSE ALARM RATE
1.5 μ s PULSE WIDTH

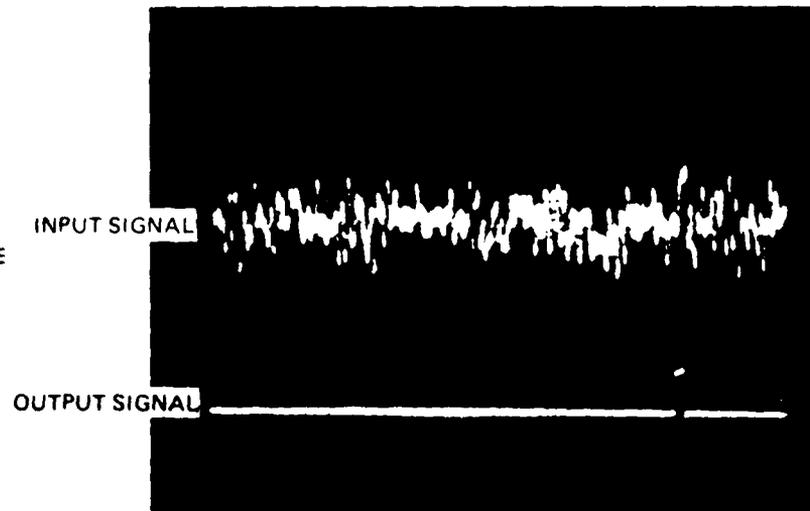
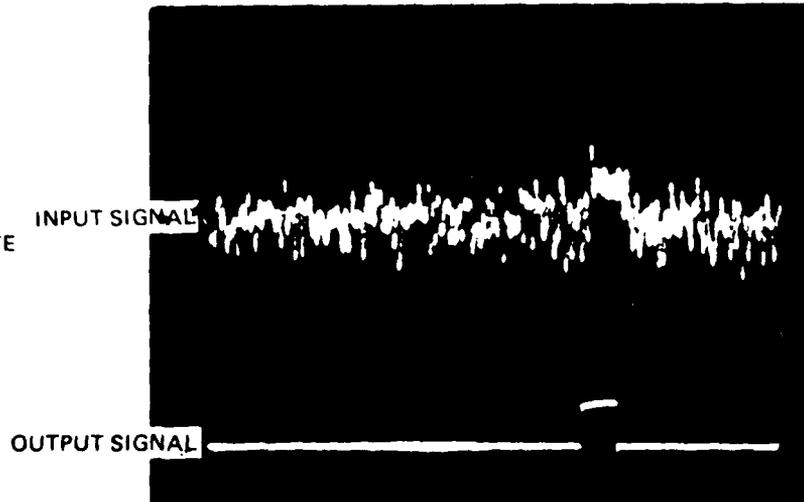


Figure 22. Walsh Preprocessor Performance at 1.5 μ sec Input Pulse Width for 2.5 MHz Band Width

2.5 MHz BAND WIDTH
 4×10^{-4} FALSE ALARM RATE
4 μ s PULSE WIDTH



2.5 MHz BAND WIDTH
 4×10^{-4} FALSE ALARM RATE
4 μ s PULSE WIDTH

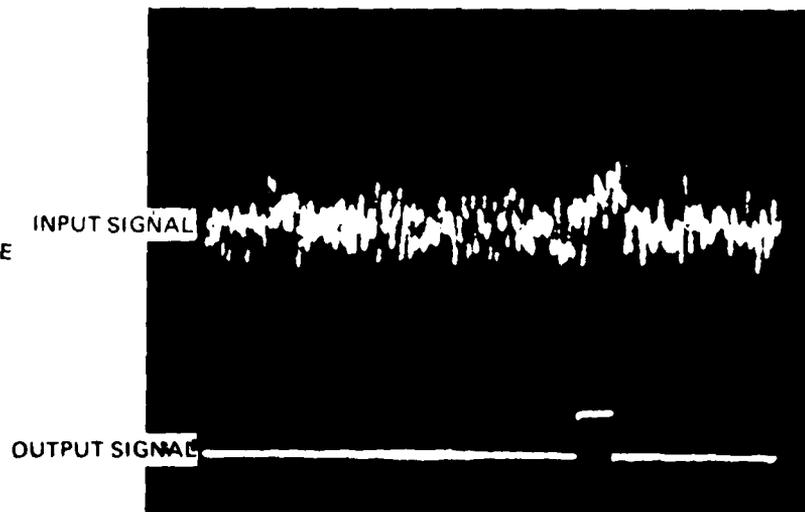
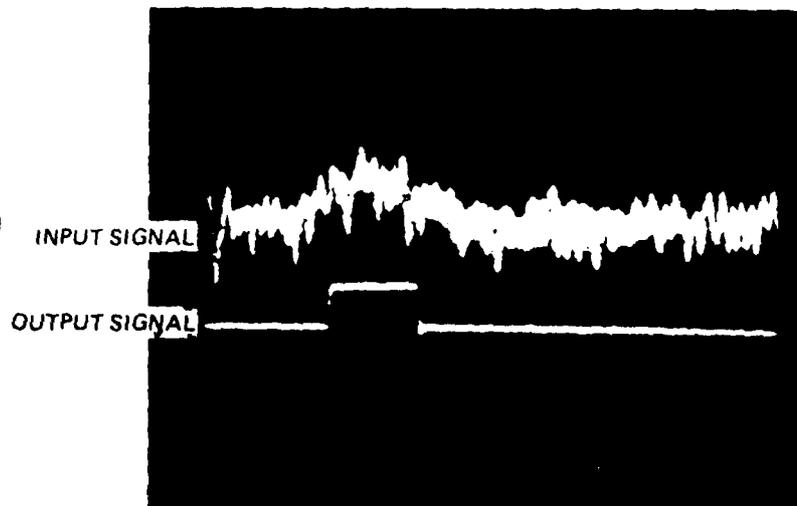


Figure 23. Walsh Preprocessor Performance at 4 μ sec Input Pulse Width for 2.5 MHz Band Width

10 MHz VIDEO BAND WIDTH
5 MHz NOISE BAND WIDTH
 10^{-4} FALSE ALARM RATE
1.5 μ s PULSE WIDTH



10 MHz VIDEO BAND WIDTH
5 MHz NOISE BAND WIDTH
 10^{-4} FALSE ALARM RATE
1.5 μ s PULSE WIDTH

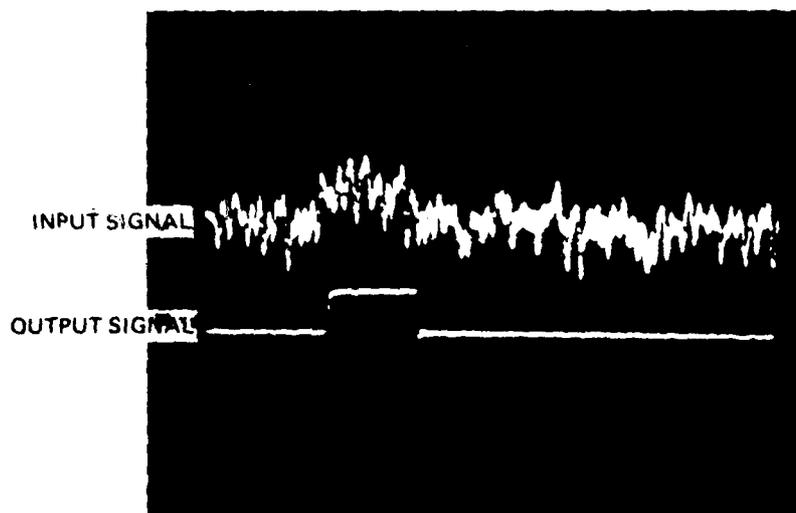
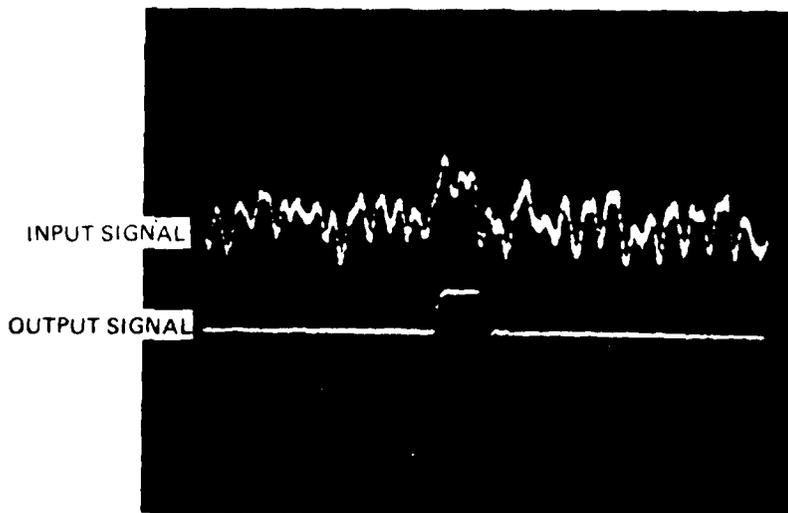


Figure 24. Walsh Preprocessor Performance at 1.5 μ sec Input Pulse Width for 10 MHz Video and 5 MHz Noise Band Widths

10 MHz VIDEO BAND WIDTH
5 MHz NOISE BAND WIDTH
 10^{-4} FALSE ALARM RATE
0.5 μ s PULSE WIDTH



10 MHz VIDEO BAND WIDTH
5 MHz NOISE BAND WIDTH
 10^{-4} FALSE ALARM RATE
0.4 μ s PULSE WIDTH

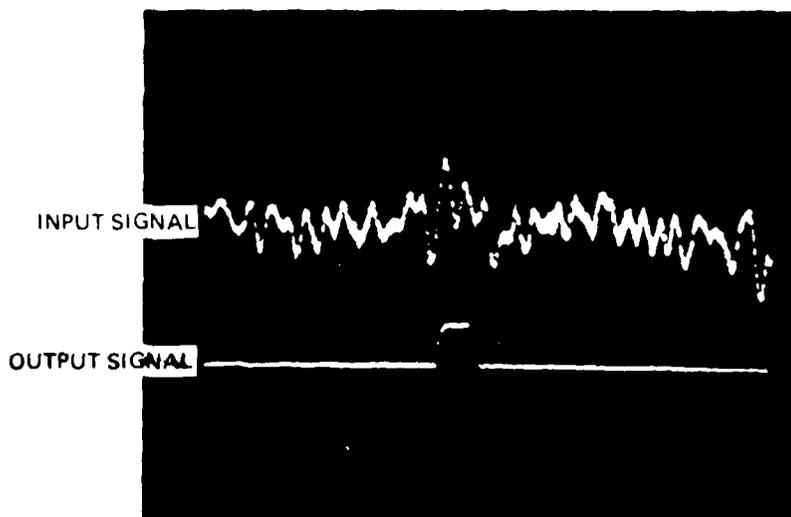
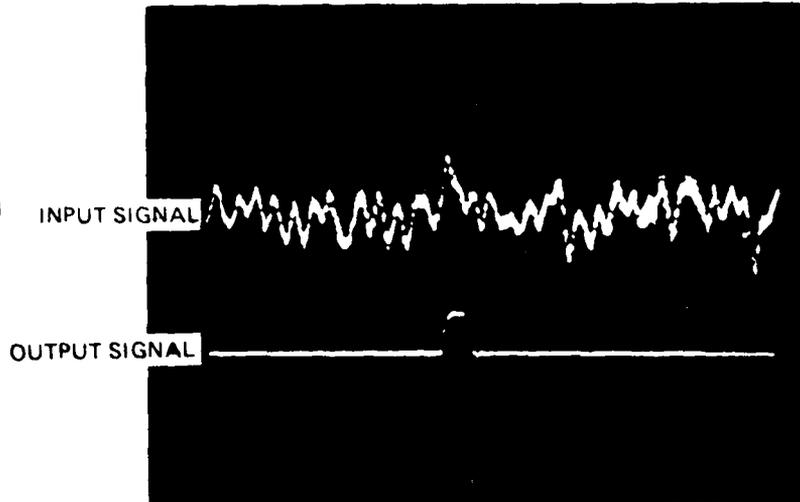


Figure 25. Walsh Preprocessor Performance at 0.5 μ sec and 0.4 μ sec Input Pulse Widths for 10 MHz Video and 5 MHz Noise Band Widths

10 MHz VIDEO BAND WIDTH
5 MHz NOISE BAND WIDTH
 10^{-4} FALSE ALARM RATE
0.4 μ s PULSE WIDTH



10 MHz VIDEO BAND WIDTH
5 MHz NOISE BAND WIDTH
 10^{-4} FALSE ALARM RATE
0.4 μ s PULSE WIDTH

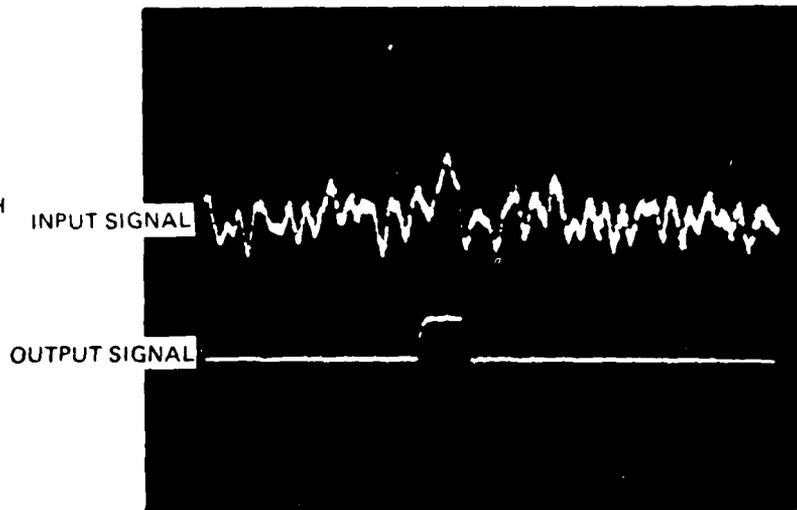
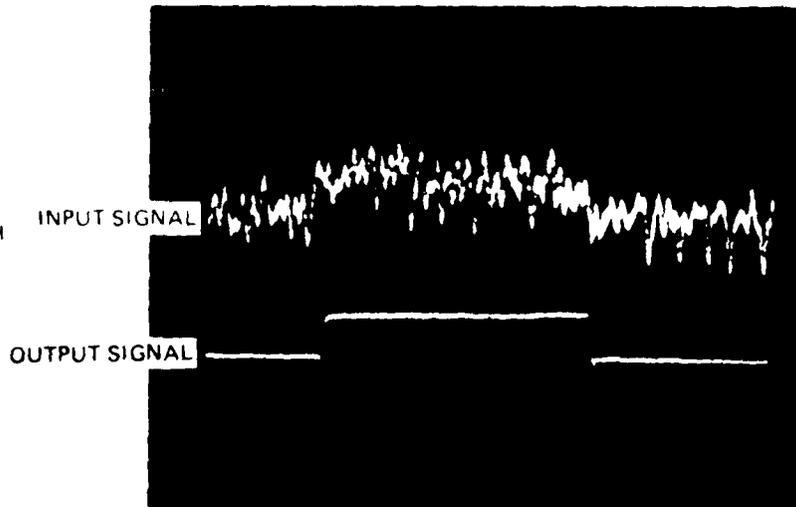


Figure 26. Walsh Preprocessor Performance at 0.4 μ sec Input Pulse Width for 10 MHz Video and 5 MHz Noise Band Widths

10 MHz VIDEO BAND WIDTH
5 MHz NOISE BAND WIDTH
 10^{-4} FALSE ALARM RATE
5 μ s PULSE WIDTH



10 MHz VIDEO BAND WIDTH
5 MHz NOISE BAND WIDTH
 10^{-4} FALSE ALARM RATE
0.5 μ s PULSE WIDTH

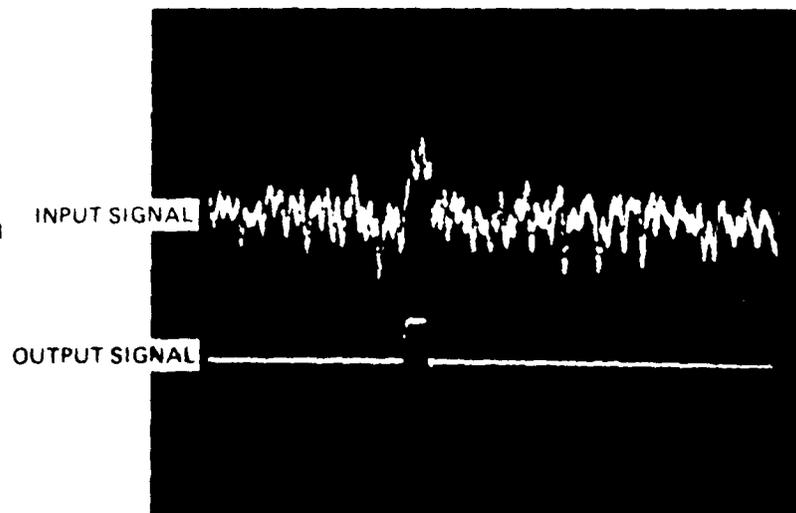


Figure 27. Walsh Preprocessor Performance at 5 μ sec and 0.5 μ sec Input Pulse Widths for 10 MHz Video and 5 MHz Noise Band Widths

Section VI

RELIABILITY FAILURE RECORD

The faulty integrated circuits found during the term of this contract were isolated by using the self-test setup. For this test, the WP is allowed to free run; the sync out of the rear of the Filter Channel is used to trigger a pulse generator. The output of the pulse generator drives the filter channel video input. The internal FIL/BYP is set for BYP (bypass) to allow all of the input data to pass through the Filter Channel without being filtered. The video output is connected to an oscilloscope for visual comparison with the filter channel input. The pulse width, pulse amplitude, and pulse delay controls on the pulse generator are adjusted, while observing the effect on the oscilloscope. Any unexplained large spikes in the video output indicate an IC failure.

Most IC failures are extremely dependent on all three pulse generator parameters. When an error is detected, an ECL word generator is substituted for the pulse generator and the Filter Channel A/D converter. If the failure is intermittent, the trouble can be isolated using an oscilloscope to prove the test connections on each wire wrap board. If a hard error exists, the signal at the test connections are compared with a computer emulation of the Filter Channel for the given input transform.

There were five I.C. failures found during the length of this contract (see Table 4). Testing was not conducted by AEL when the GFE was received, which makes it difficult to measure the failure period.

TABLE 4. SUMMARY OF WP FAILURES

Date	I.C. Type	Corrective Action	Time to Restore
7/30/79	10115	Replace	0.25 hr.
7/30/79	10115	Replace	0.17 hr.
9/11/79	10181	Replace	1.00 hr.
9/11/79	10181	Replace	0.33 hr.
12/3/79	10176	Replace	2 hr.

Section VII

CONCLUSIONS AND RECOMMENDATIONS

The Walsh Preprocessor system has demonstrated its ability to detect low SNR pulse signals and has met or exceeded all the required specifications set forth in the Statement of Work. It is felt that the WP will assist the U.S. Air Force in applications requiring the detection and processing of low level signals. However, the ultimate value of the system can best be determined by the results of the subsequent test and evaluation phase to be performed by the sponsor.

A thorough and detailed testing program is recommended for the evaluation of the WP system. This program should include both simulated and real signals using a variety of signal characteristics. The most important of the system parameters that should be tested are the probability of detection and parameter estimation (pulse width and position). The performance of the unit in a variety of applications such as radar warning, communications, telemetry, TEMPEST, ELINT and ESM should also be evaluated.

The testing performed to date has shown that the system false alarm rate (FAR) is a non-linear function of the sample rate. The two default value PFAs have been adjusted at each sampling rate to give values 4×10^{-4} . The WP is programmable such as to achieve any desired PFA from 0.5 to about 10^{-12} .

As described in Section III of the report, the WP system performance is determined by a set of forty (40) constants which have been pre-programmed into the system. These constants, which determine the FAR, probability of detection, and parameter estimation have default values that were adjusted at each sample rate.

There are currently eight (8) different decision paths available within the WP; three wide pulse, two medium pulse, two narrow pulse and one noise path. It is not obvious to the WP programmer just which path is dominant, for a given signal, without attachment of external counters, etc. This path choice information would provide a valuable aid to the programmer who is dealing with an unknown noisy signal, attempting to optimize detection under a high-pressure, short-fuse, application. Several design change choices for visual and/or print out means are available to provide this path choice information.

Appendix A

ADAPTIVE PULSE FILTERING PROCESS

The Adaptive Pulse Filtering Process (APFP) is utilized to remove noise from single or multiple signals such as to:

- 1) Improve signal-to-noise ratio by typically 10 dB and as much as 15 dB.
- 2) Improve pulse width measurement accuracy at low SNR.
- 3) Improve pulse position (time-of-arrival) measurement accuracy at low SNR.
- 4) Improve pulse amplitude measurement accuracy at low SNR.
- 5) Discriminate against nonpulse signals, such as DC input signals, independent of DC input.
- 6) Remove distortion from pulse signals.

The APFP consists of five (5) elements: (a) Analog to Digital Converter; (b) Forward (Fast) Walsh Transformer; (c) Sequency Spectrum Processor; (d) Inverse (Fast) Walsh Transformer; and (e) Threshold Detector.

The APFP operation is based on the principle that a pulse signal can be readily identified and separated from noise by electronic analysis of the Walsh Transform of that signal. It is the function of the sequency spectrum processor to perform this identification/separation task. Once the separation is complete, the enhanced signal is transformed back into the original time domain by the Inverse (Fast) Walsh Transformer.

As an illustrative example of the APFP operation, consider a short interval of time in which 256 time domain samples of noise and signal are produced by the Analog to Digital Converter operating on the output of a conventional pulse receiver. Assume that a pulse of 8 samples duration is present, and hidden somewhere within the 256 sample batch. By examination of the Forward Walsh Transformer output, all pulse information is approximately contained within the lowest 32 sequency (Walsh domain) elements; therefore, the lowest 32 Walsh domain elements are retained, and the pulse is essentially recovered, but 224/256 of the noise is discarded.

NOTE

An explanation of all the notations used in this appendix is given at the conclusion.

GENERAL OPERATION OF APF PROCESSOR

The generalized block diagram of the Adaptive Pulse Filter (APF) is shown in Figure A 1. Analog video input signals, such as those from the output of

either the linear AM or log AM (log IF) detector of a pulse receiver, are applied to the Analog to Digital Converter (ADC) portion of the Adaptive Pulse Filter (APF) Processor, where they are sampled and converted to a serial stream of digital words. The signal input at point A is assumed to be band limited to BW Hz by a low pass filter function. The ADC sampling rate is programmable and is equal to RBW ($R \geq 2$) and is typically 4 BW ($R = 4$). The serial stream of digital time domain words is converted to a serial stream of frequency domain digital words by a pipeline Forward Walsh Transformer, although any time multiplexed parallel Walsh transformer will also suffice.

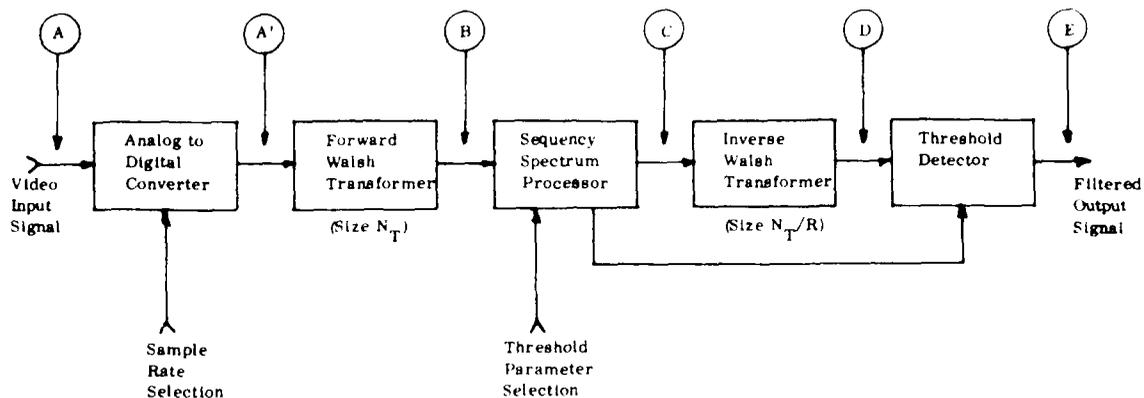


Figure A-1. Adaptive Pulse Filter Block Diagram

The Forward Walsh Transformer describes an input time domain function $f(t)$ as a finite series of ($N = \frac{N_T}{2}$) orthogonal functions known as Walsh functions, as follows:

$$f(t) = a_0 \text{WAL}(0,t) + a_1 \text{SAL}(1,t) + b_1 \text{CAL}(1,t) + a_2 \text{SAL}(2,t) + b_2 \text{CAL}(2,t) + \dots + a_{n=N} \text{SAL}(n=N,t) + b_{n+N} \text{CAL}(n=N,t)$$

where $a_0 = \int_0^1 f(t)dt = \text{DC average}$

and $a_n = \int_0^1 \text{SAL}(n,t)f(t)dt$

$$b_n = \int_0^1 \text{CAL}(n,t)f(t)dt$$

where $n = 0, 1, 2, \dots, N$

For all above cases, the integral is replaced by a discrete summation over N_T samples in this process. For a description of the Walsh functions SAL and CAL, the reader is referred to pages 3-5, H.F. Harmuth "Transmission of Information by Orthogonal Functions," New York, Springer 1969. Sequence order

may be defined as one-half of the average number of zero crossings per second of the corresponding Walsh function.

The serial data stream of sequency domain elements, in order of advancing sequency (i.e., lowest sequency ($n = 0, 1, 2 \dots N_T/2$) first appear at point B of Figure A-1. The Sequency Spectrum Processor acts on the sequency domain elements such as to pass certain signal associated elements while discarding others. The passed elements appear at point C of Figure A-1 and are then applied to the Inverse Walsh Transformer. Since the Walsh transformation is orthogonal (hence, unique and complete) a sampled time domain signal may be forward transformed to sequency domain, then inverse transformed back to time domain without loss of information but with a fixed delay.

The retained sequency domain elements are thus inverse transformed to time domain and appear at point D of Figure A-1. If the Sequency Spectrum Processor were to pass all N_T sequency domain elements, the data at point D would be identical except for a fixed delay to that at point A. The Sequency Spectrum Processor does not pass all sequency elements however (N_T/R maximum), hence the filtering action. This filtering performance is dependent upon certain threshold selection parameters applied to the Sequency Spectrum Processor.

A time domain threshold detector, acting to clip noise products, is used after inverse transformation, resulting in the filtered output signal at point E of Figure A-1. This time domain threshold setting is also determined by the Sequency Spectrum Processor.

The entire APF Processor can be implemented either in digital hardware form or computer software programmed hardware form, with a fixed "pipeline" delay between raw input data and filtered output data. The APF process can also be implemented in analog form, but would be highly inefficient in terms of cost and performance.

Figures A-2 to A-11 show the APF process at all critical stages. Figure A-2 is a block of 256 samples of a high signal-to-noise ratio (SNR) pulse with width of 8 samples, such as is seen at point A of Figure A-1. Figure A-3 is the 256 ($N_T = 256$) element sequency domain of this pulse, such as would appear at point B of Figure A-1, in sequency order. The first 32 samples are associated with the pulse; the remainder are primarily associated with noise. The Sequency Spectrum Processor will pass only the first 32 elements, resulting in the signal of Figure A-4 which corresponds to what would appear at point C of Figure A-1. After inverse transformation, the filtered time domain signal of Figure A-5 results, such as would appear at point D of Figure A-1. This signal is then thresholded, resulting in the signal of Figure A-6, such as would appear at point E of Figure A-1. Figure A-6 depicts the reconstructed, filtered version of the signal of Figure A-2. Figure A-7 shows the same input signal (point A) but at a lower SNR. Its transform is shown in Figure A-9. The inverse transform (point D) is shown in Figure A-10 and the thresholded output (point E) is shown in Figure A-11. Figures A-7 to A-11 show the powerful nature of sequency domain processing to sort signals (especially pulses) from noise.

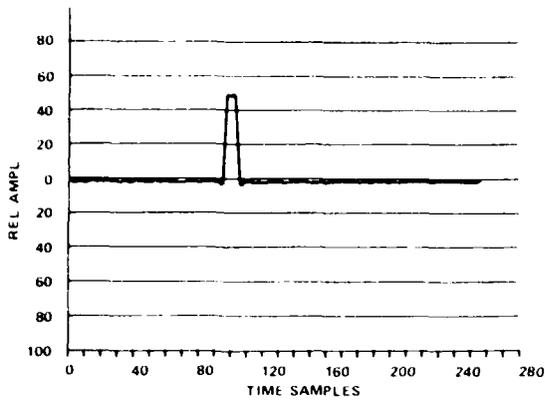


Figure A-2. High SNR Pulse in Time Domain

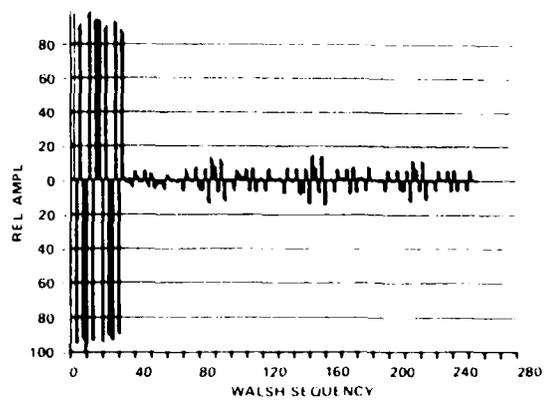


Figure A-3. High SNR Pulse in Sequency Domain

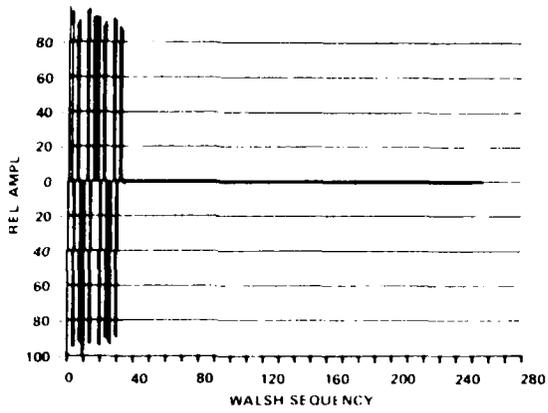


Figure A-4. Filtered High SNR Pulse in Sequency Domain

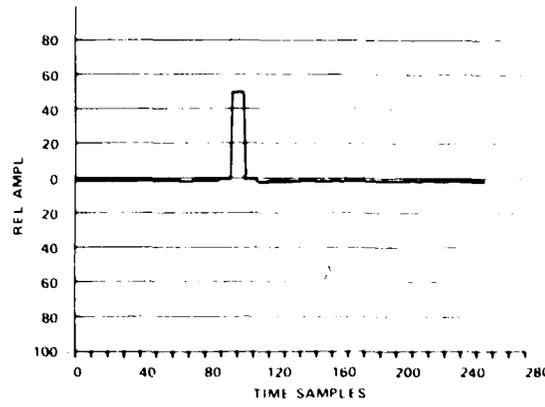


Figure A-5. Filtered High SNR Pulse in Time Domain

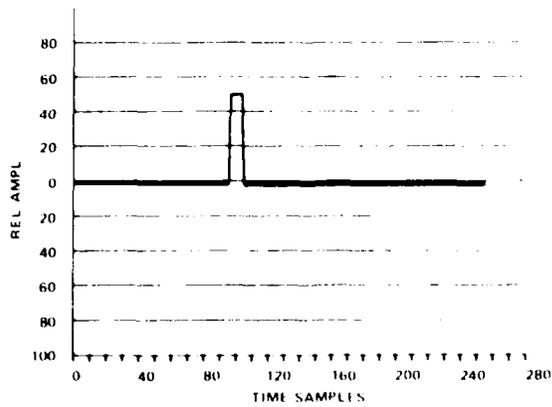


Figure A-6. Filtered and Thresholded High SNR Pulse in Time Domain

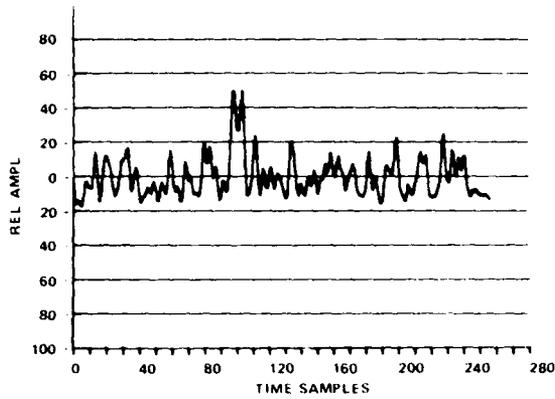


Figure A-7. Low SNR Pulse in Time Domain

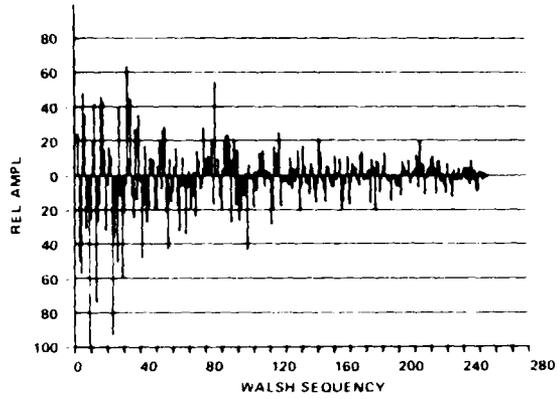


Figure A-8. Low SNR Pulse in Sequency Domain

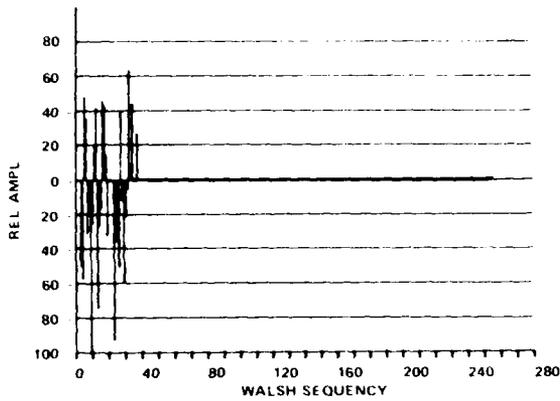


Figure A-9. Filtered Low SNR Pulse in Sequency Domain

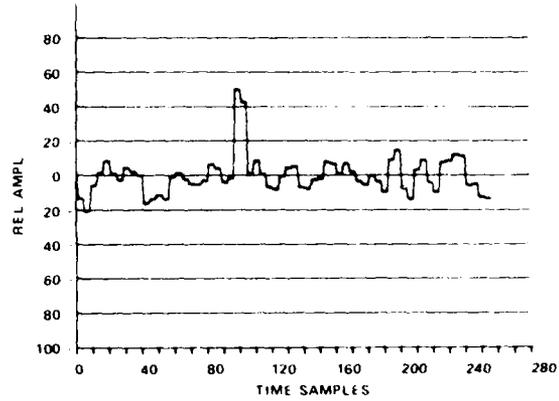


Figure A-10. Filtered Low SNR Pulse in Time Domain

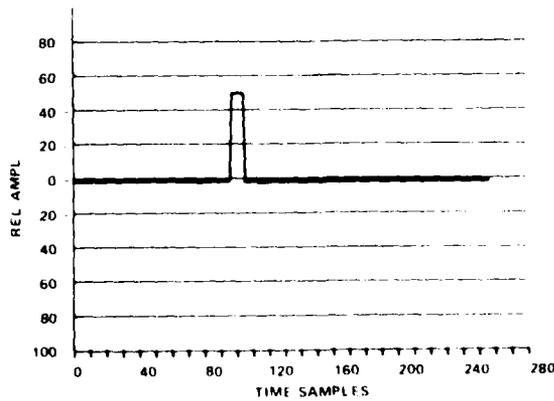


Figure A-11. Filtered and Thresholded Low SNR Pulse in Time Domain

The process is independent of the DC level at point A; the sequency threshold does not utilize the DC level information and the time thresholding adaptively adjusts for DC level. This characteristic eliminates critical calibration adjustment of the DC output of a receiver, and prevents threshold degradation due to DC shift from presence of a CW signal at the receiver input.

The process is optimized for but not restricted to rectangular pulses. If other shaped pulses are received, the processor will pass additional sequency elements such as to adaptively detect both position and width.

PRINCIPLE OF OPERATION OF SEQUENCY SPECTRUM PROCESSOR

The previous Figures A-2 to A-11 showed the results of sequency domain filtering of noisy pulse signals. The key principle of operation centers around the techniques and circuits that set the decision thresholds for the sequency processing, i.e., the apparatus that automatically and adaptively dictates just which sequency lines are retained for inverse transformation with all others being blanked. The sequency spectrum processor operates as follows:

- 1) Examines all N_T samples of the Forward Walsh Transformer output and calculates X average rectified (signal-plus-noise) level ratios.
- 2) Compares all sequency samples (a_j) to thresholds (T_{AX}) which are preprogrammed multiples of the above average ratios, starting with sequency sample ($j-1$) and increasing monotonically to the highest sequency sample ($j-N_T$).
- 3) Samples sufficiently above the threshold value are kept while all others are discarded.
- 4) Whenever several (K_X) successive sequency samples are discarded, all following samples are automatically discarded regardless of amplitude.
- 5) In addition to sequency spectrum processing, it provides a time domain threshold (T_H') for processing all time domain samples (b_i) after the inverse Walsh Transform has taken place.

Item 1) is key to the process because it provides the signal analysis information which sets up the processing thresholds. This analysis is based on a known difference in sequency spectrum between noise only conditions and noise plus pulse conditions.

NOISE ANALYSIS

In the noise only case, the sequency spectrum has a Gaussian amplitude probability distribution for Gaussian time domain input noise. Figure A 12 shows a typical random noise time domain input, approximately Gaussian, and of wide bandwidth due to $N_T/2$ independent samples (for example a 20 MHz noise bandwidth sampled at 40 MHz). As illustrated in Figure A 12, there are 128 independent samples in the $N_T = 256$ sample block. The sequency domain of this noisy signal is shown in Figure A 13, and illustrates the following general conditions.

- a) The wideband noise sequency domain amplitude has relatively constant statistics (average, variance) over the first $N_T/2$ samples (128 in Figure A-13) and slightly lower amplitude statistics in the last $N_T/2$ samples. The point at which the noise level drops in the sequency domain is highly dependent upon the input noise bandwidth as will be later illustrated.
- b) Very little "clumping" of sequency lines occur, that is, several lines having a high approximately equal value. Thus, there exists no concentration of energy around any particular sequency value.

Although the Adaptive Pulse Filter will operate over a very wide variety of input bandwidths, the processor decision parameters must be programmed for each input bandwidth. That is, the processor is normally calibrated and aligned with the receiver(s) with which it is to operate.

Figure A-14 shows a somewhat less broadband noise input of $N_T/4$ independent samples (64). This noise has no relationship with that of Figure A-12. Figure A-15 shows the sequency domain of the noise of Figure A-14. The sequency spectrum statistics are constant out to about the 64th sample, whereupon they drop and drop again after the 128th sample.

Figure A-17 shows even narrower "broadband" noise of $N_T/8$ independent samples (32). This relates to a 5 MHz low pass filtered video input to a 40 MHz sampling rate APF, which is unusually low but illustrates the dependence of the noise analysis mode thresholds on the input bandwidth. Figure A-17 shows the sequency domain of the signal of Figure A-16. The sequency spectrum statistics are now constant to about the 32nd sample, a point at which they drop and drop again after the 64th and 128th samples.

The above noise analysis discussion and illustrations are only intended to provide a background and insight into the sequency domain analysis (Item 1). Of course, in dealing with random variables, it is possible that extremely rare sequency spectrums of any amplitude and position can occur. A collection of noise samples can rarely resemble a pulse, but when this occurs the APF processor will treat it as such, as would any conventional pulse detector. Any detector performance can be described in terms of a receiver operating characteristic (ROC, H.L. VanTrees, "Detection, Estimation, and Modulation Theory, Part 1," Wiley, New York, p. 36-40) which describes true detection vs. false alarm performance. The powerful aspect of the APF processor is that for a fixed false alarm probability, for example, the true detection probability is much higher than that of more conventional detectors such as the fixed threshold detector.

NOISY PULSE ANALYSIS

The recognition of pulse presence in the sequency domain is based on the following observation:

"Given a sequency block of N_T samples, which contains a pulse of width W , then the information describing the pulse width and position is approximately contained in the lowest (N_T/W) Walsh sequency domain elements." For the examples in Figures A-2 to A-11, the pulse width W was 8 samples, N_T was

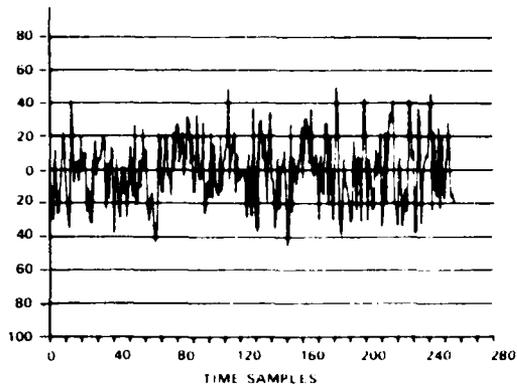


Figure A 12. Wideband
($N_T/2$ Independent Samples) Noise,
Time Domain

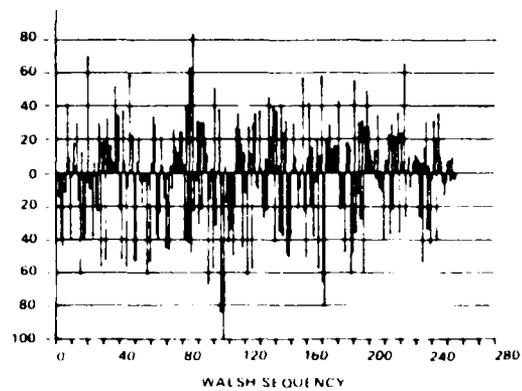


Figure A 13. Wideband
($N_T/2$ Independent Samples) Noise,
Sequency Domain

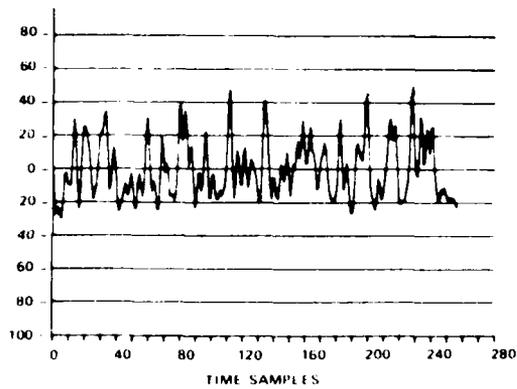


Figure A 14. Band Limited
($N_T/4$ Independent Samples),
Time Domain

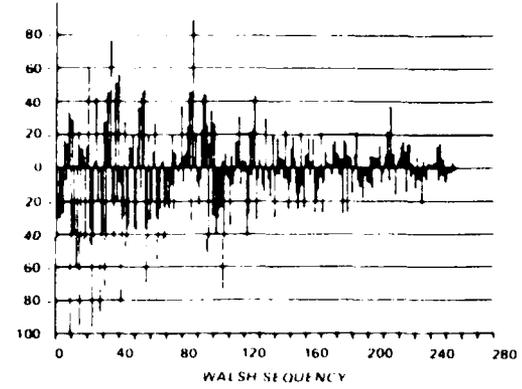


Figure A 15. Band Limited
($N_T/4$ Independent Samples),
Sequency Domain

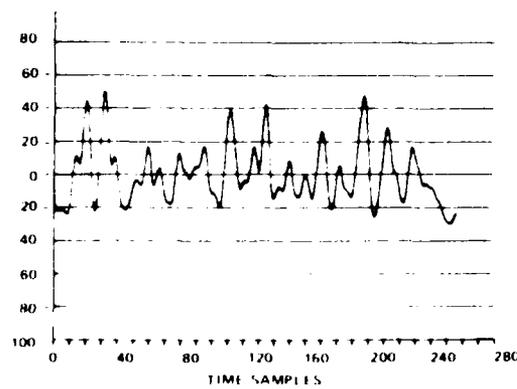


Figure A 16. Band Limited
($N_T/8$ Independent Samples),
Time Domain

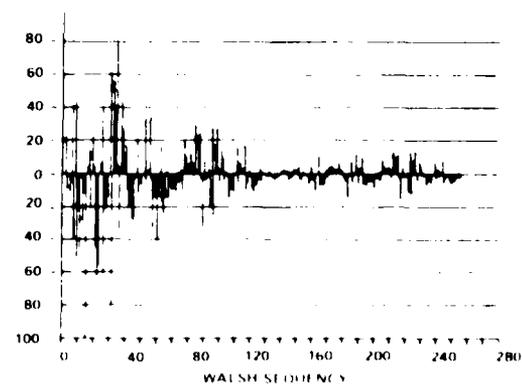


Figure A 17. Band Limited
($N_T/8$ Independent Samples),
Sequency Domain

256; hence, most of the necessary pulse position and width information was contained in the lowest $256/8 = 32$ elements.

The above observation can be mathematically proven to also relate the fact that the lowest (N_T/W) elements can, at worst case, provide a pulse position and width error of $W/2$ samples. This is due to the fact that the Walsh transform is not shift-invariant; that is, a pulse of width 8 samples centered at the 100th sample has a different frequency spectrum than one of width 8 samples centered at the 101st sample, etc. The information necessary to position the pulse to within $W/4$ samples requires the lowest ($2N_T/W$) elements at worst case. Thus, a fixed low pass frequency filter function will not suffice to detect a pulse. The APF functions adaptively such as to allow more frequency elements, hence higher position and width accuracy at high signal-to-noise levels yet provide reliable detection with low false alarm rates (but somewhat lower width and position accuracies) for weak pulses that ordinarily would be totally undetectable.

When a pulse of width W is present, the frequency domain statistics drastically change from that of broadband noise; in particular, the lowest (N_T/W) frequency elements. It is the function of the APF processor (Item 1) to detect this statistical change, and now armed with the above background information, we are ready to describe this process.

SEQUENCY ANALYSIS PROCESS

Referring to the block diagram of Figure A-18, the Frequency Analysis portion of the APF processor is that portion between points B (Walsh Transform output) and B' (Threshold outputs). This portion calculates all frequency processing thresholds plus the time domain (post inverse Walsh Transform) threshold (Item 5). It is to be recognized that the Forward and Inverse Walsh Transformers are of the serial in-serial out "pipeline" type. Both the Forward transformer output and Inverse transformer input frequency elements are in terms of advancing frequency; i.e., of frequency (DC), the next of frequency 1 (SAL(1,t)), the next of frequency 2 (CAL(2,t)), then frequency 2 (SAL(2,t)), etc. A memory of D_{1X} words delays the data until all thresholds are calculated. The number D_{1X} is the number of word clock cycles required for the analysis time.

The Frequency Analysis portion of the APF processor calculates a number relating to the total energy in the data block. It can be shown by Parseval's theorem that the RMS value (power) of all N_T time domain values is equal to the RMS value of all frequency domain values with a constant scale factor. Although the RMS measurement operation can be utilized in the processor, it has been found that the average of all N_T rectified frequency domain values is simpler to calculate with negligible loss in decision accuracy.

Either the rectified average or RMS of all N_T elements is calculated, as well as the rectified average or RMS of the first N_1 elements, the first N_2 elements, etc., up to the first N_X elements. The ratio of the sums of the first N_1 and all N_T is calculated resulting in the single number \bar{N}_1/\bar{N}_T . Similarly the values of \bar{N}_2/\bar{N}_T up to \bar{N}_X/\bar{N}_T are calculated. If there were only noise present, and if the noise were broadband as per Figures A-12 and A-13, then all values of \bar{N}_1/\bar{N}_T ,

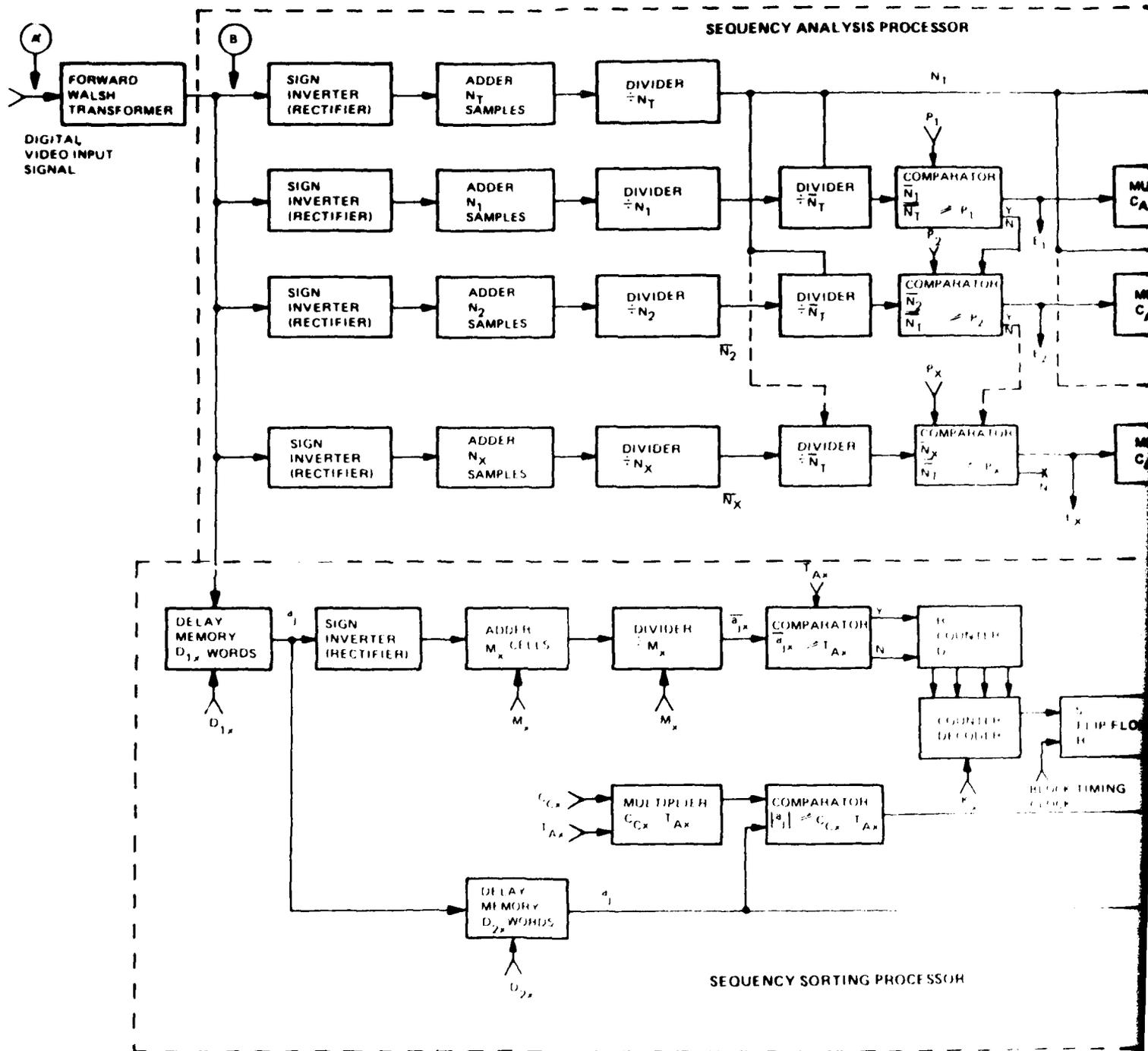
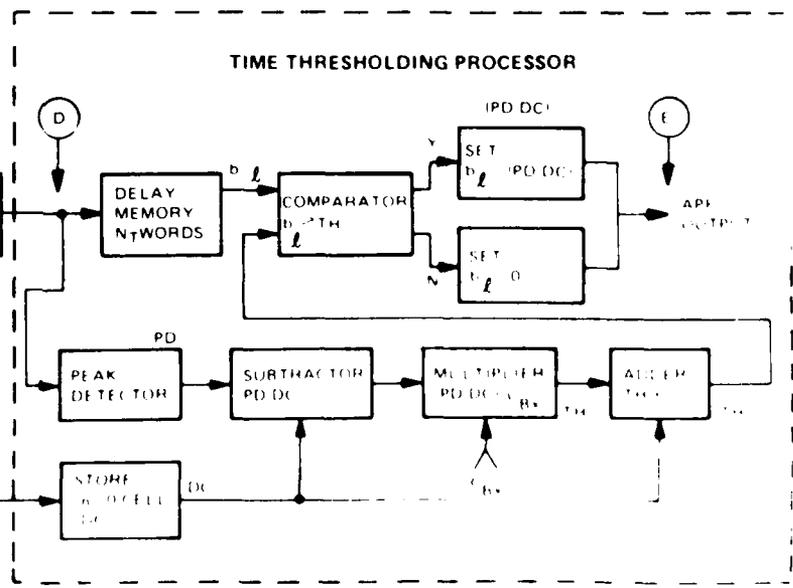
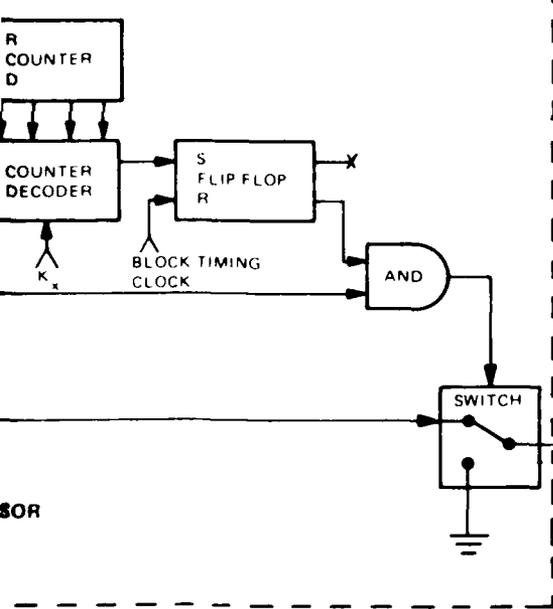
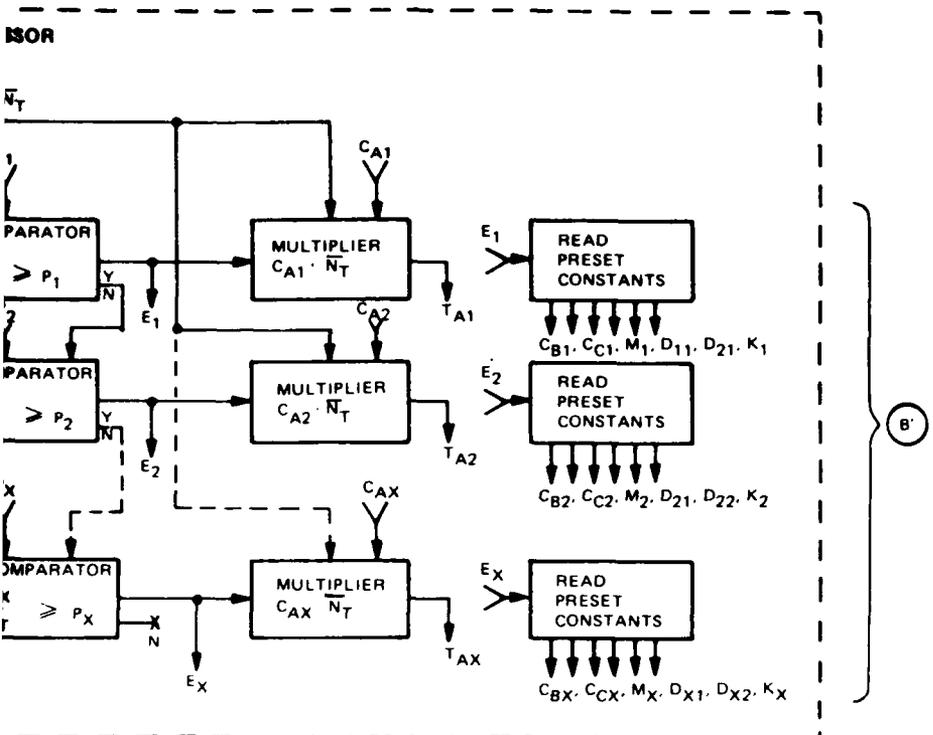


Figure A-18. Adaptive Pulse Filtering Detailed Block Diagram



$\bar{N}_2/\bar{N}_T \dots \bar{N}_X/\bar{N}_T$ would tend to unity, representing flatness of frequency domain statistics. If for example, the value of \bar{N}_1/\bar{N}_T were equal to 2.0, however, with \bar{N}_2/\bar{N}_T being perhaps 1.2 and all others near unity, then it is most probable that a noisy pulse is present having a width of approximately N_T/N_1 samples.

Typically at least two averages are calculated, with three being the most common. Each average is chosen to optimize the expected pulse width. For example, using an $N_T = 256$ point block with sample rate at 40 MHz (one sample every 25 ns), and an expected signal environment of pulse widths of between 100 ns and 5000 ns, then a value of $N_1 = 6$ and $N_2 = 30$ works well but values of $N_1 = 4$, $N_2 = 12$, and $N_3 = 48$ is more consistent. The approximate matched value is $N_x = N_T/W_x$, thus for our example if 0.4 microsecond (16 sample) pulses were expected a value of $N_x = 256/16 = 16$ would be optimum. The peaks of each averager output vs. pulse width are reasonably broad over about three octaves 8:1; thus a minimum configuration would require Q number of averages with

$$Q = 1/3 \log_2 \left(\frac{W_{\max}}{W_{\min}} \right)$$

with W_{\max} the maximum pulse width and W_{\min} the minimum.

The values of \bar{N}_x/\bar{N}_T ($x = 1, 2, 3, \dots, X$) are then compared to a preset threshold P_x . The values of P_x in general decrease as x increases because 1) the variance of the average decreases as more independent noise samples are used and 2) the presence of a pulse (for a fixed signal-to-noise ratio) becomes more difficult to detect at narrower widths (higher N_x) because the pulse energy is dispersed over more frequency elements. Also, as the value of N_x approaches a noise corner (such as shown in Figures A-15 and A-17), then the value of P_x must be modified to compensate for a nonflat frequency spectrum.

The values of P_x can be set up in field operation in conjunction with a receiver for a given false alarm rate by monitoring the comparator output with a digital frequency counter and accordingly adjusting P_x . Ordinarily, each P_x is set for equal contribution to the required false alarm rate; but priorities may establish other than equal weightings.

The comparators thus examine each value of \bar{N}_x/\bar{N}_T in relation to P_x and decide as to the presence or absence of a signal. The longer pulses (lowest x) is examined first; if more is found then x increments to look for shorter pulses; if none is found for $x = X$ then all frequency spectrum elements are blanked with the exception of the DC value (frequency 0) which is always retained to prevent DC discontinuity (flicker) for display purposes.

If a particular \bar{N}_x/\bar{N}_T exceeds P_x , then i is not advanced, and two thresholds are generated 1) a value T_{Ax} , the frequency domain threshold and 2) a value C_{Bx} , the post transformation time domain threshold. These thresholds appear at B' in Figure A-18. The value of Γ_{Ax} is equal to a multiple (C_{Ax}) of \bar{N}_T , with C_{Ax} typically between 1.1 and 4.0. For example, if $N_T = 256$ with broadband noise, $N_T/256$ represents the average value of a frequency element.

The elements containing "detectable" signals are usually at least 1.1 times the average; thus a value of $C_{AX} = 1.5/256$ would be typical. Again, the values of C_{AX} are dependent upon the noise bandwidth. If C_{AX} is too low, too many sequency elements will be passed and a noisy output and/or multiple false pulses can occur. If C_{AX} is too high, too few sequency elements will be passed and pulse position and width inaccuracy may result.

Whichever mode (value of x) is chosen, the appropriate enabling line E_x is energized; if none is chosen then no line is enabled and all sequency elements other than DC are blanked.

SEQUENCY SORTING PROCESS

The Sequency Sorting Process operates on the sequency domain (delayed) data (a_j) from the Forward Walsh Transformer based on the thresholds calculated previously during the sequency analysis process.

The sorting process operates on rectified integrated sequency data; that is each sequency element is rectified and added to the sum of the next ($M_x - 1$) sequency elements, and this total sum compared to ($M_x T_{AX}$) the threshold. This integration is necessary in order to circumvent gaps in the sequency spectrum for pulses of narrow width at certain positions. A pulse does not always provide a low pass block of sequency lines as in Figure A-3; under certain pulse conditions there exist gaps.

The integration length M_x is preset for each of the x number of modes available as controlled by the sequency analysis process. Typical values of M_x for the previous example $N_T = 256$, $N_1 = 6$, $N_2 = 30$ is $M_1 = 6$, $M_2 = 10$.

Per Figure A-18, M_x cells are integrated, resulting in a delayed data stream $\overline{a_{jx}} = 1, 2, 3, \dots, (N_T - M_x)$. The integrated $\overline{a_{jx}}$ data is normalized by dividing M_x and compared to (T_{AX}); if $\overline{a_{jx}} > T_{AX}$ then the counter is not advanced, but is reset.

The counter counts K_x integrated data words $\overline{a_{jx}}$ below the T_{AX} threshold, and is reset by an above threshold condition. This action simply looks for K_x successive integrations below threshold (typically 3); when it occurs, all higher sequency elements are blanked. That is, the processor has determined that the sequency block associated with a data pulse has ended.

Each of the a_j sequency elements, after being properly delayed by Delay Memory D_{2x} , is compared to a threshold equal to $C_{CX} T_{AX}$. The value of C_{CX} is typically between 1.1 and 1.8. If a sufficiently high amplitude sequency element is present, it will be passed provided that the K_x counter has not been filled. Per the gate logic of Figure A-18, if a_j th element is below the $C_{CX} T_{AX}$ threshold, the following AND gate is inhibited, and the a_j th element is blanked. If a_j is above threshold, the a_j element is passed, provided that the K_x counter is not filled.

When the counter decoder indicates that K_X successive drop-outs are present, the flip-flop is set such as to inhibit data for the remainder of the sequency block, which is then reset.

Figure A-8 showed the effect of thresholding on the noisy data of Figure A-8. The processor has blanked the 2nd, 21st, 22nd, 23rd, and 37th line and the pulse block has ended. From Figure A-3, we know that the data block really ended at the 33rd line; however, noise statistics prevented the processor from determining this until the 39th line, and by examination of Figure A-8 it is apparent that significant noise energy exists between the 33rd and 39th lines. (This is due to the integrate M_X cells in conjunction with K_X "NO" counter.)

The switch function in the sequency sorting portion of Figure A-18 operates on the data after an appropriate delay of $(D_{1X} + D_{2X})$ words, which assures that the total delay through the Sequency Sorting Processor will be constant, independent as to which mode of integration and threshold parameters are selected by the sequency analysis processor.

The data at point C is that of Figures A-4 and A-9, and is ready for Inverse Walsh Transformation, after which the time domain signal appears as in Figures A-5 and A-10. Since the sampling rate is sufficiently high such that the shortest pulse is sampled R times ($R \geq 2$ and typically 4), the sequency signal spectrum is approximately contained below N_T/R sequency; thus only the lowest N_T/R sequency elements are retained at maximum. This can greatly simplify the Inverse Walsh Transformation due to essentially elimination of the first $\log_2 R$ tiers of the $\log_2 N_T$ process (i.e., for $N_T = 256$ and $R = 4$, the first two of the eight FWT tiers are grossly simplified). R is a binary integer, 1, 2, 4, etc. (Ordinarily, $\log_2 N_T$ tiers are necessary in an FWT.)

TIME THRESHOLDING PROCESS

The time domain signals of Figures A-5 and A-10 represent sequency domain filtered pulse signals. Figure A-10 is particularly instructional because it shows the prominence of the filtered pulse and the attenuated baseline clutter. Thresholding of the signal of Figure A-10 will produce a clean reconstruction of the pulse as shown in Figure A-11. The proper setting of the threshold TH is at some ratio of the peak to average difference of the filtered signal, such as 50% (a typical value). In the example of Figure A-10, the positive peak (PD) is at +50, the average (DC) is 0; thus, the peak to average difference is 50, the 50% threshold TH would be at 25 since $DC = 0$, $TH = 25$, allowing excellent reconstruction.

Instead of using the zero baseline, the negative peak, which is known, could be used and the threshold TH set at 65% of the positive peak to negative peak ratio, which is also at 25.

The peak of the filtered time domain must be determined in either case. A memory of N_T words must be provided to appropriately delay the data until the peak is found by the peak detector of Figure A-18. The DC value is the value of the lowest sequency ($n=0$) term, which is picked off before the Inverse Walsh Transformer (stored during peak scanning), and applied to the subtractor and

adder such as to result in the DC level compensating threshold $TH' = (PD-DC) C_{BX} + DC$. If any time domain sample in the block is above this threshold, it is set to the value of PD; otherwise it is set to zero.

GENERALITIES OF THE PROCESS

The previously described process for recognition of a pulse signal of unknown amplitude, width, and position is achieved by transformation into an orthogonal domain so as to: (1) eliminate the position variable (all pulses in time domain produce low frequency "clumping"); and (2) easily isolate the width variable (by integration from frequency 0 up to M_X) such that the detection problem is reduced to amplitude detection only (thresholding). The frequency domain (Walsh Transformation) is shown to be very well suited for pulse processing for two major reasons: (1) the square-wave-like Walsh functions are similar in format to the rectangular-like pulses found in radar and telemetry; and (2) the (Fast) Walsh Transform hardware results in the simplest orthogonal transform circuit implementation. Nevertheless, the basic technology of Adaptive Pulse Filtering can be accomplished in other orthogonal domains, such as Fourier, Haar, Rademacher, etc.

EXPLANATION OF NOTATIONS, ADAPTIVE PULSE FILTERING PROCESS

- R Number of samples for the shortest pulse of interest. Also, since the video bandwidth in Hz is assumed to be at least equal to the reciprocal of the shortest pulse in seconds, R is the ratio of sampling rate to video bandwidth. As R is typically equal to 4, a 40 MHz sample rate (one sample every 25 ns), pulses as short as 0.1 μ sec (100 ns) can be accommodated, provided that the video input bandwidth is a minimum of 10 MHz.
- N_T Number of time domain samples per block, also equal to the number of frequency domain elements per block.
- n A variable, indicating frequency number of each Walsh function, in zero crossings per block. Each frequency number has two functions (elements): SAL (n,t) which is an even function and CAL (n,t) which is an odd function. An exception is frequency number 0 which has only CAL (o,t), also called WAL (o,t).
- t A variable, representing time.
- N Highest frequency number present that is also equal to $N_T/2$. For an $N_T = 256$ element transform, the highest frequency number present is SAL (128,t).
- a_n The SAL function of frequency number n.
- b_n The CAL function of frequency number n.
- X The total number of modes of operation of the frequency spectrum processor. Each mode consists of: (1) an analysis integration over N_X frequency elements resulting in the word \bar{N}_X ; (2) an analysis threshold

comparison of \bar{N}_x/\bar{N}_T to a programmed threshold P_x ; (3) a mode processing enable decision E_x , based on the sequency domain analysis; (4) a calculation of a sequency domain threshold T_{Ax} ; (5) a selection of a preprogrammed time domain threshold multiplication factor T_{Bx} ; (6) a sorting integration over M_x sequency elements resulting in the word $\overline{a_{jx}}$ which is compared to the factor T_{Ax} ; and (7) a below threshold word counter of length K_x .

$x =$ A variable, indicating the particular mode chosen for discussion
 $1 \leq x \leq X$.

NOTATIONS PARTICULAR TO THE SEQUENCY ANALYSIS PROCESSOR

$N_x =$ The number of sequency elements integrated in the x th mode in the sequency analysis processor. This integration always starts with the $n = 1$ th element and ends at the N_x th sequency element.

$\bar{N}_x =$ A number equal to the sum of the N_x sequency elements (except for DC, WAL (o,t)) integrated in the sequency analysis processor.

$\bar{N}_T =$ A number equal to the sum of all N_T sequency elements (except DC (WAL (o,t)) in the block.

$P_x =$ The preprogrammed threshold level applied to \bar{N}_x the sum of the first N_x sequency elements integrated in the sequency analysis processor.

$E_x =$ The enable line for the x th mode which is a direct result of the fact that $\bar{N}_x/\bar{N}_T \geq P_x$

$C_{Ax} =$ A preprogrammed constant which is used to calculate the sequency domain threshold of the x th mode.

$T_{Ax} =$ The sequency domain threshold of the x th mode which is precisely equal to the product of C_{Ax} and \bar{N}_T .

$C_{Bx} =$ A preprogrammed constant which is used to calculate the time domain threshold occurring after the inverse Walsh Transformer. The value of C_{Bx} is dependent upon x , the mode chosen by the sequency analysis processor.

NOTATIONS PARTICULAR TO THE SEQUENCY SORTING PROCESSOR

$M_x =$ The number of elements integrated in the Sequency Sorting integrator. The integrator is a sliding type, adding the previous ($M_x - 1$) elements to each new element.

$j =$ A variable, indicating the j th element of the sequency data stream within the Sequency Sorting Processor, after the appropriate delay, ($1 \leq j \leq N_T$)

- a_j The sequency element data stream, consisting of a_1 , followed by b_1 , followed by a_2 , followed by b_2 up to a_N ($j = N_T$).
- $\overline{a_{jX}}$ The rectified, integrated and normalized sequency element data, after being rectified, integrated over M_X cells, and divided by M_X .
- D_{X1} A number representing the delay expressed by the number of clock samples, for mode x . This function acts to delay the sequency domain data stream during the sequency analyses process prior to sorting.
- D_{X2} A number representing the delay, expressed by the number of clock samples, for mode x , that serves to match up the delays for all x modes, such that the total delay through the Sequency Spectrum Processor is the same for all x modes.
- C_{CX} A preprogrammed constant, used in setting the sequency element threshold at a value equal to $C_{CX} T_{AX}$, for each mode x .
- K_X A preprogrammed constant, setting the maximum number of consecutive times that the rectified, integrated normalized sequency element data ($\overline{a_{jX}}$) is below the T_{AX} threshold, prior to setting all remaining sequency elements to zero.

NOTATIONS PARTICULAR TO THE TIME THRESHOLDING PROCESSOR

- b_j The reconstructed time sample data stream, after exiting from the inverse Walsh Processor and after a delay of N_T samples.
- PD The peak (largest value) of the (N_T size) block of time domain samples (b_j).
- DC The average value of the (N_T size) block of time domain samples (b_j), which is equal to $WAL(o,t)$.
- TH The time domain relative threshold value, prior to the addition of the DC baseline $TH = (PD - DC)C_{BX}$.
- TH' The time domain absolute threshold, equal to $TH + DC$.



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