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DATA CONTROLLER SYSTEM FOR FATIGUE CRACK MONITORING USING A POT--ETC(U)
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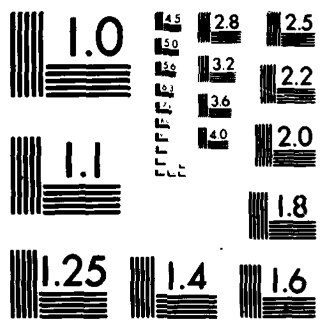

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DATA CONTROLLER SYSTEM FOR FATIGUE CRACK MONITORING USING A POTENTIAL DROP TECHNIQUE

Barry J. Baxter

Approved for Public Release

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ABSTRACT

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C O N T E N T S

* * *

DATA CONTROLLER SYSTEM FOR FATIGUE CRACK MONITORING USING A POTENTIAL DROP TECHNIQUE

1. INTRODUCTION

In order to predict the remaining life of a component containing a fatigue crack growing under the influence of fluctuating loads, it is necessary to determine the relationship between fatigue crack growth rate and the stress intensity at the crack tip. This relationship is usually determined by applying a constant range of cyclic loading to a pre-cracked test specimen, and monitoring the rate of crack growth while the crack tip stress intensity range increases with increasing crack length. It is clearly important that accurate measurements of crack length are made throughout the test, and the crack length monitoring system in use at MRL is based on the most sensitive technique available; potential drop (PD) crack monitoring [1] which utilises the change in electrical resistance of a specimen as a crack extends. The technique usually relies on passing a constant current through the specimen, and monitoring changes in potential across the cracked region. This technique produces a continuous record of potential which may be related, by means of a suitable calibration equation, to the instantaneous crack length.

Recent improvements to the MRL crack-monitoring system have made it possible for the testing machine to be operated whilst unattended and with automatic print-out of crack length, number of fatigue cycles, and crack tip stress intensity during the test. The major components of the new system are :

(i) Servo-hydraulic testing machine (MTS Systems Corporation)

(ii) PD system

(iii) Desk calculator (Hewlett Packard 97S)

(iv) Data control unit

The calculator and data controller also make it possible to end the test when specific crack lengths (a) crack growth rates (da/dn) or crack tip stress intensity (ΔK) conditions are achieved.

The crack length monitoring system is described in detail elsewhere (ref. 1) and is summarised in Appendix 1. The data control system is described in detail in this report.

2. SYSTEM OPERATION

A schematic diagram of the equipment is shown in Fig. 1(a). In operation the output from the MTS function generator is taken to a four decade counter in the data controller. After a selected count interval the digital voltmeter (DVM) is interrogated and, when its reading is completed, a signal is produced which enables the DVM output to be passed to the calculator, together with the count interval.

The calculator program, the flow diagram for which is shown in Appendix 2, converts the DVM reading into crack length and calculates ΔK and crack growth rate. From these parameters the calculator is programmed either to allow a further block of fatigue load cycles to be made or alternatively switches off the fatigue cycling to enable a new set of conditions to be applied for the next part of the fatigue program. For each operation of the program the following information is printed by the calculator :

1. Voltage from crack monitor.
2. Accumulated total number of fatigue cycles.
3. $\frac{a}{W} = \frac{\text{crack length}}{\text{specimen width}}$
4. $\frac{da}{dN}$ = crack growth per cycle
5. ΔK = crack tip stress intensity factor

3. DATA CONTROL UNIT

The function of this unit may be divided into the following sections :

1. Fatigue interval counter and display.
2. Control logic.
3. DVM Interface.
4. Power supplies.

Apart from front panel controls, shown in Fig. 1(b), and the mains transformer, these sections are contained on two printed circuit boards. The lower board contains item 3 while all the others are contained on the upper board. With the exception of the display all the digital integrated circuits are of the TTL 74 series.

The connections between the data control unit and the DVM, HP97S and MTS are given in Tables 1, 2, 3(a) and 3(b) respectively.

4. INTERVAL COUNTER AND DISPLAY

The square wave signal from the MTS function generator on pin 8/9 is fed to the first of four decade counters, C_1 - C_4 (Fig. 2). The count interval switch (SWIa-d) is wired to the counters to give intervals of 10, 10^2, 10^3 in a 1, 2, 5 sequence ending with 10^4. After the selected count interval, the 555 timer is triggered by the counter to produce an 11 ms pulse which sends a signal to the DVM "Trip" terminal via 2 gates. A "Read" switch is also connected to trigger the 555 to enable manual initiation of the read cycle.

The output from the first counter C_1, is also used to drive the count display D_1 - D_3, which provides an indication of one tenth of the fatigue cycles. This is formed from three TIL 306 numeric display counters, which are connected to provide synchronous counting with leading zeros blanked. At the initiation of a "Read" cycle they are automatically cleared to zero, together with the main decade counters by gate 26a. The display intensity is modulated by the supply 50 Hz to ensure long display life.

5. CONTROL LOGIC

The control logic used for synchronising the data and the calculator is shown in Fig. 3(a); the circuit for the count interval switch SW1 is given in Fig. 3(b). The logic timing used to ensure the correct sequence of events during the "Read" cycle is shown in Fig. 4.

The 11 ms pulse from the 555 timer which initiates the "Read" cycle is applied to the Trip terminal of the DVM via gates 00a and 26b. This causes the DVM to read and convert into digital form the voltage at its input terminals. During this operation the DVM 'conversion complete' signal is in its busy state, i.e. '0'. On completion, the '1' state is delayed by 1½ ms through gates 13a and 13b to ensure stable data from the DVM. This delayed signal is used as a LOAD signal to load the awaiting data into the calculator. Since the 'conversion complete' signal has a 30 microsecond rise-time, Schmitt-trigger gates are used to ensure the 2 microsecond rise time required by the calculator. This loading function immediately produces a busy signal in the form of $\overline{LE}$ ('1') from the calculator and this is used, through gates 00b and 00c, to operate a panel indicator which shows green when ready to accept data and red when loading data or running a program.

As a result of the program calculations any one of the three "Flag" indicators may be set. Each Flag has its own function as follows :

Flag 0 - Relay RL3 (Fig. 3(a)) operates. The contacts (4A 250V) are for future use and are shown in Table 3(b).

Flag 1 - Relay RL1 de-energised, which switches off the hydraulic supply. Two safety precautions are included in this circuit.

(i) The relay must be energised to enable the hydraulic power to be switched on.

(ii) The calculator must be connected to the data controller before the relay can be energised.

Flag 2 - Relay RL2 operates for 60 ms and switches off the machine program. The MTS machine was modified to allow external control of the 'Program' switch.

If it is required to operate the MTS machine independently from the calculator the 'Interlock' switch (Figs. 3(a) and b) may be set in the 'MTS' position. This bypasses the relay interlock and also switches off the 5V power supply to the logic units. A dummy Data Controller plug may also be used for the same purpose.

6. DVM INTERFACE

The data channels of the calculator require TTL level inputs in binary coded decimal (BCD) form. Since the digital output from the DVM DM 2022 is in the form "0" = - 1V and "1" = - 11V it is necessary to provide an invert and scale function on each line. The LM 3900 quad. operational amplifier unit was selected to achieve this function and six were used for the task. Figure 5 shows one set of amplifiers. Each set is the same, except for the 'conversion complete' amplifier, the differences being shown in the figure.

Since the decimal point is indicated by a '1' on one of five lines from the DVM it is necessary to encode this into BCD on 3 lines, and this is achieved by means of diodes on the output of the 5 decimal point amplifiers, shown in Fig. 5.

The second block of data to the calculator is the count interval selection. This is achieved by two wafers (Fig. 3(b) SWI e & f) on the switch and two diode encoders. The first digit signifies the 1, 2, 5 integers and the second the decade multiplier, both in BCD format. Thus 23 represents a count interval of 2000.

7. POWER SUPPLIES

Details of the power supply are given in Fig. 6. The various levels of d.c. supply required throughout the unit are derived from a transformer and rectifiers with smoothing capacitors and integrated circuit regulators. Each of the 5 supplies is regulated to within approximately 20 mV for line and load variations. Table 4 shows the voltages derived and their uses. The a.c. to the 5 volt rectifier is separately switched as described in the paragraph on Control Logic.

8. SUMMARY

A control unit has been designed and constructed to handle the data from a digital voltmeter monitoring crack growth during fatigue cycling. These data, together with information on the number of cycles from the MTS machine, are fed to a desk calculator (HP97S) which calculates crack length, crack growth rate and stress intensity factor. If any of these factors exceeds pre-set levels in the calculator program the fatigue cycle is stopped. Power supplies for the various units were also designed and incorporated.

9. REFERENCE

1. Clark, G. (1979). A high sensitivity potential-drop technique for fatigue crack growth measurement. *Report MRL-R-755.*

TABLE 1

DATA CONTROL UNIT - DVM (DM 2022) INTERCONNECTION

DVM (DM 2002)	PLUG (DCU/36)	CONNECTION
	1-5	Spare
SK1/F	6	Common Ground
SK2/S	7	DP 4
SK2/M	8	DP 3
SK2/H	9	DP 2
SK2/C	10	DP 1
SK1/Y	11	10^2 8
SK1/t	12	10^2 4
SK1/BB	13	10^2 2
SK1/FF	14	10^2 1
SK1/B	15	Conversion complete
SK2/W	16	DP 5
SK1/K	17	10^4 2
SK1/H	18	10^4 1
	19-22	Spare
SK1/L	23	Trip
	24	Spare
SK1/X	25	10^1 8
SK1/s	26	10^1 4
SK1/AA	27	10^1 2
SK1/EE	28	10^1 1
SK1/Z	29	10^0 8
SK1/u	30	10^0 4
SK1/CC	31	10^0 2
SK1/HH	32	10^0 1
SK1/W	33	10^3 8
SK1/r	34	10^3 4
SK1/z	35	10^3 2
SK1/DD	36	10^3 1
SK2/DD } SK2/CC }		Connected

T A B L E   2

DATA CONTROL UNIT TO HP 97S

PLUG DCU/50

PIN	CONNECTION		PIN	CONNECTION	
1	Common grnd		26	$\overline{\text{LE}}$ Interlock Board	
2			27	grnd	
3	FL 2 Interlock Bd		28	grnd	
4	FL 1 " "		29	LOAD Interlock Board	
5	FL 0 " "		30	o.c	
6	1	Count	31	o.c	GO TO A
7	2	Interval	32	grnd	
8	4	Selection	33	o.c	
9	grnd	Zeros	34	o.c	
10	grnd	Enter	35	1	Count
11	grnd		36	2	Interval
12	o.c		37	4	Selection
13	o.c		38	grnd	Digit
14	1	10^0 output	39	1	Decimal Output
15	2		40	2	
16	4		41	4	
17	8		42	grnd	
18	1	10^2 output	43	1	10^1 output
19	2		44	2	
20	4		45	4	
21	8		46	8	
22	1	10^4 output	47	1	10^3 output
23	2		48	2	
24	grnd		49	4	
25	grnd		50	8	

TABLE 3(a)

CONTROL UNIT TO MTS

PLUG DCU/9

PIN	CONDITION	PIN	CONDITION
1	N.O. contact Hyd. Relay	6	
2	Com. " " "	7	
3		8	Trig. Out. to Counter IN
4	N.O. contact Prog. Relay	9	MTS Com.
5	Com. " " "		

TABLE 3(b)

FLAG O CONNECTOR

PLUG DCU/5

PIN	CONDITION
A	Normally open contact
C	Common contact
E	Normally closed contact
B D F	Spare

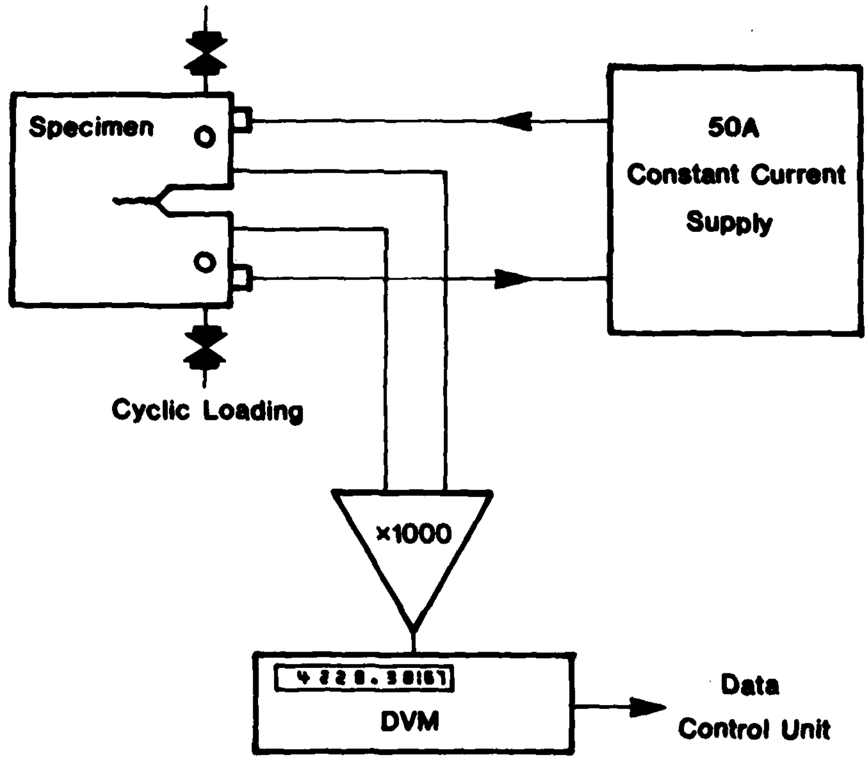
T A B L E 4

Voltage	Regulator	Use	Current Available
± 15 V	LM 7815	D.V.M. Interface op. amps.	350 mA
+ 5 V B	LM 7805	logic and counter	1 A
+ 5 V D	LM 7805	count interval display	1 A
+ 12 V	µA 78 MG	relays	350 mA

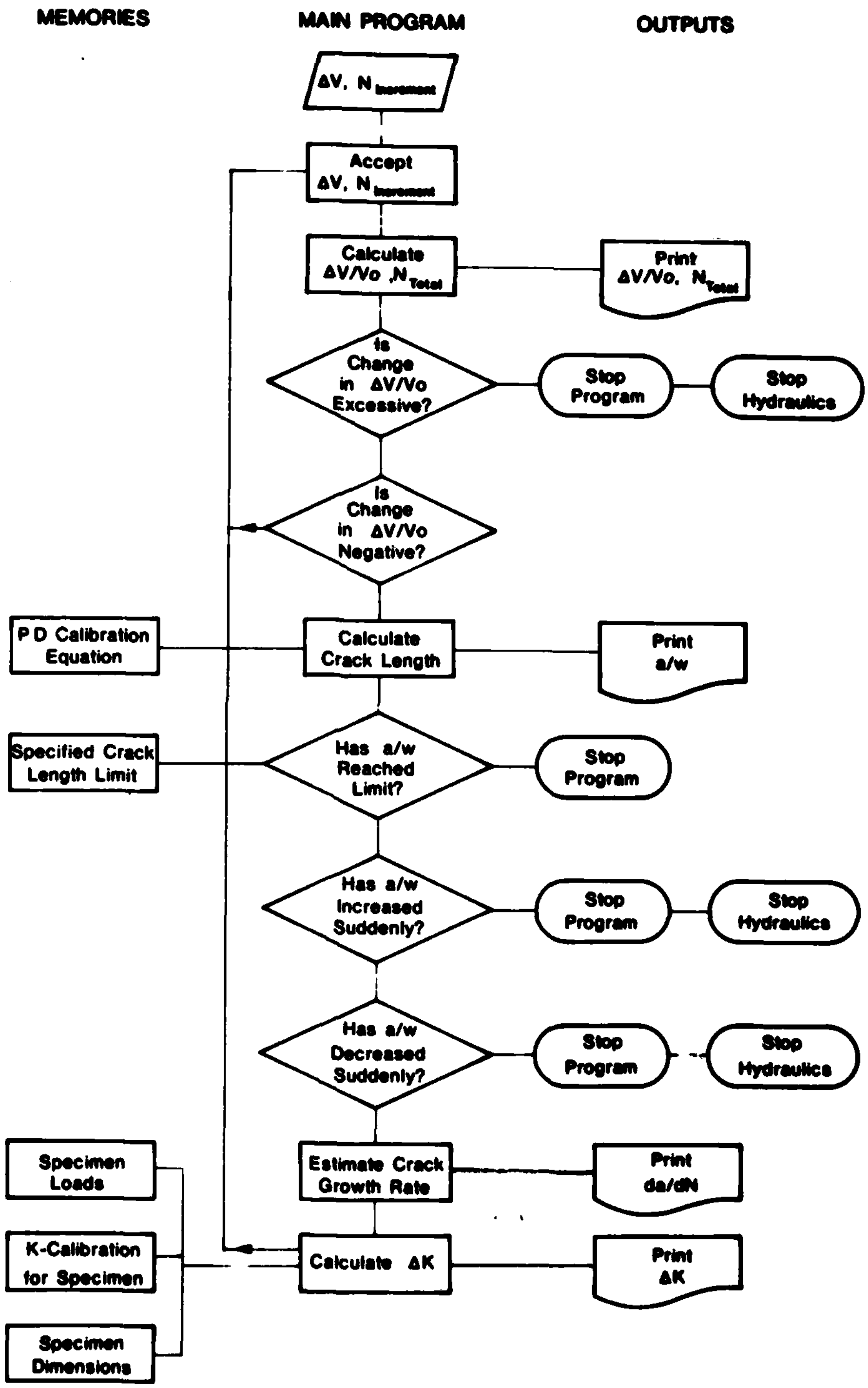
APPENDIX 1

The potential drop crack length monitor (Ref. 1) is shown in the diagram.

A stabilised and constant current flows through the cracked specimen; as the crack grows the resistance increases and produces a higher output voltage. With currents of 50 A the potential drop is in the microvolt region; a x1000 gain low drift amplifier is therefore required to bring the signal to a level for reliable DVM measurement. The relationship between crack length and voltage is represented by a polynomial equation in the calculator program.



APPENDIX 2



CRACK LENGTH MONITORING PROGRAM

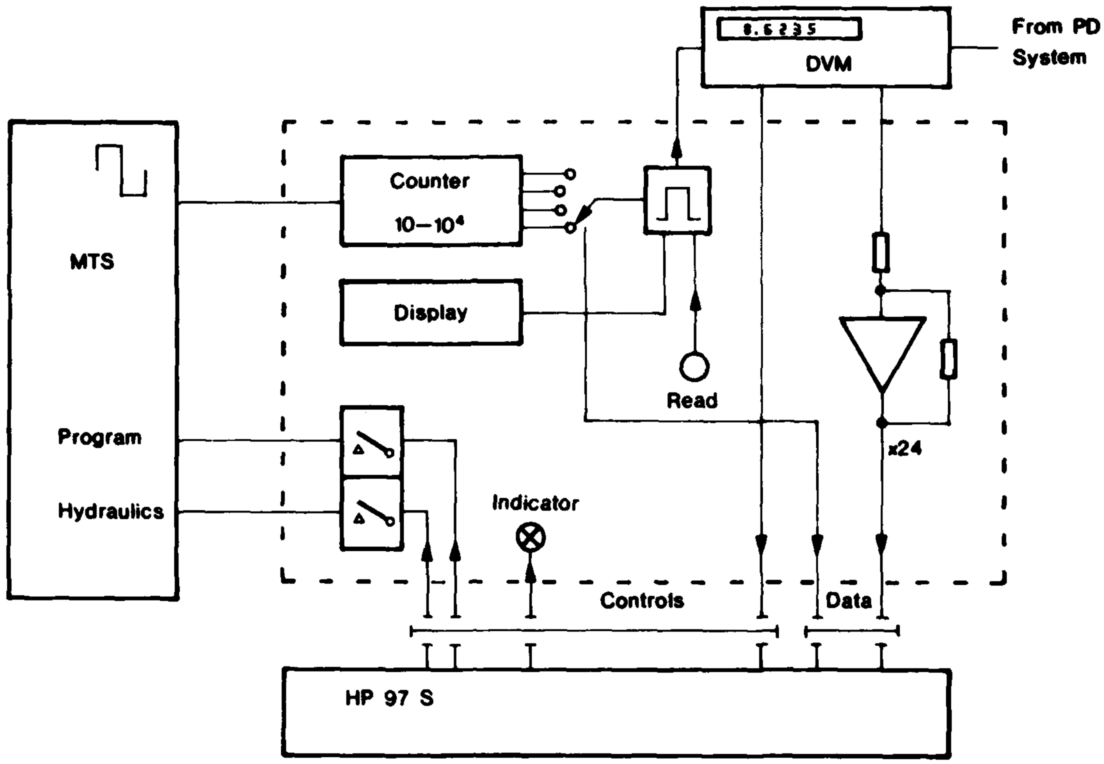


FIG. 1a - SYSTEM SCHEMATIC

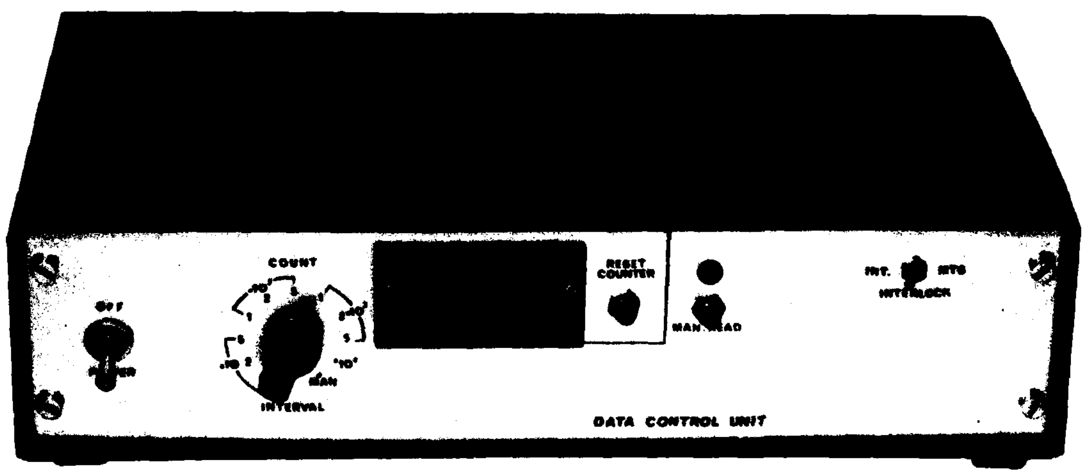


FIG. 1b

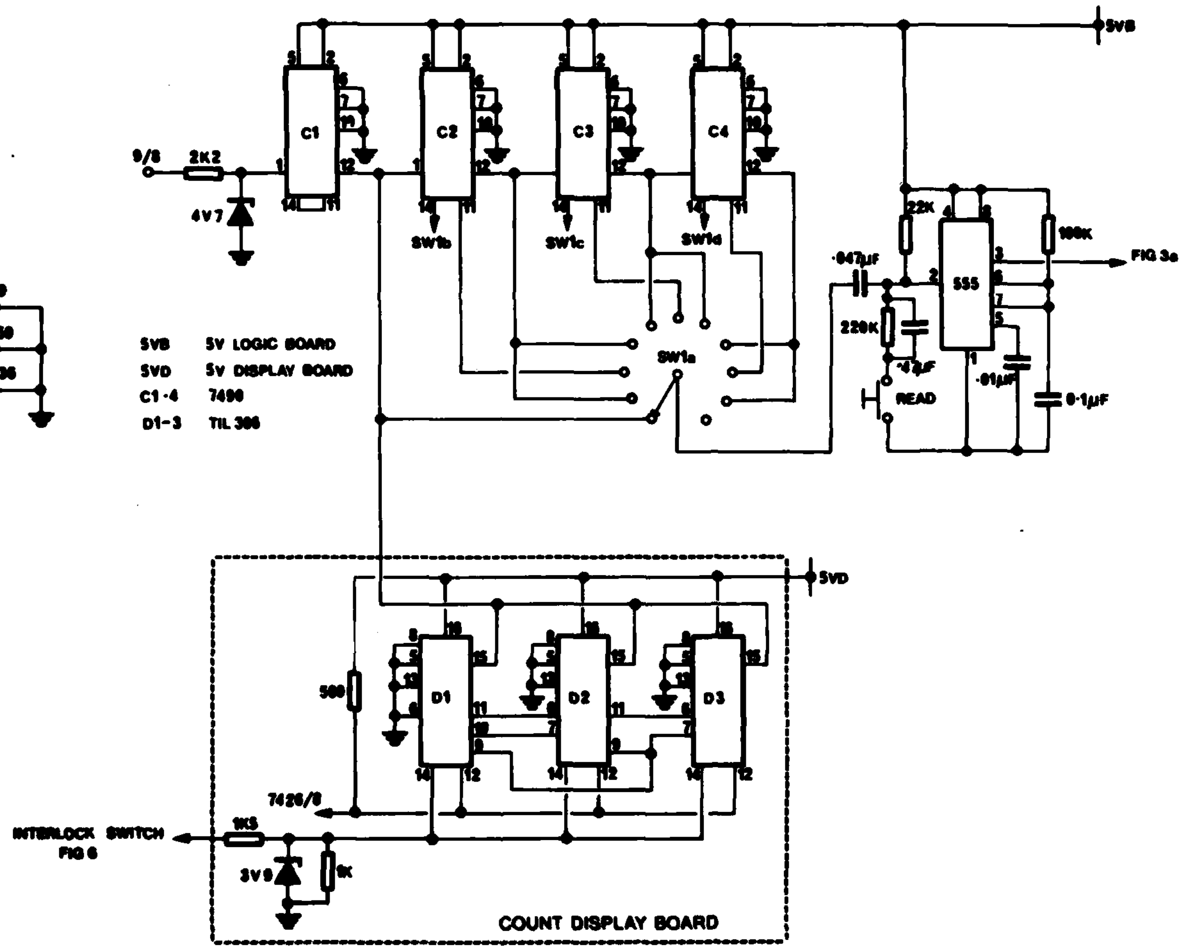


FIG. 2 - INTERVAL COUNTER AND DISPLAY

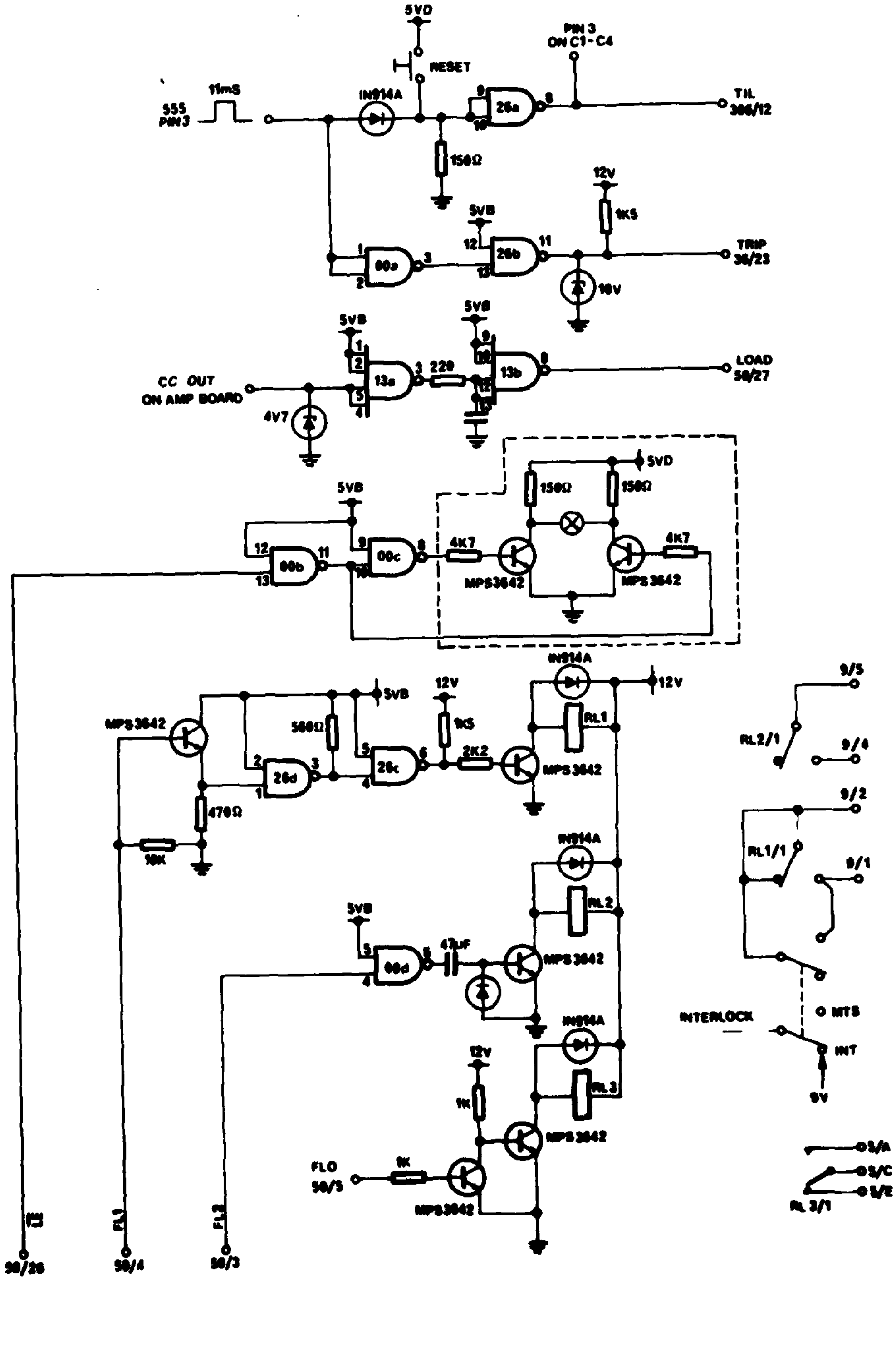


FIG. 3a - CONTROL LOGIC

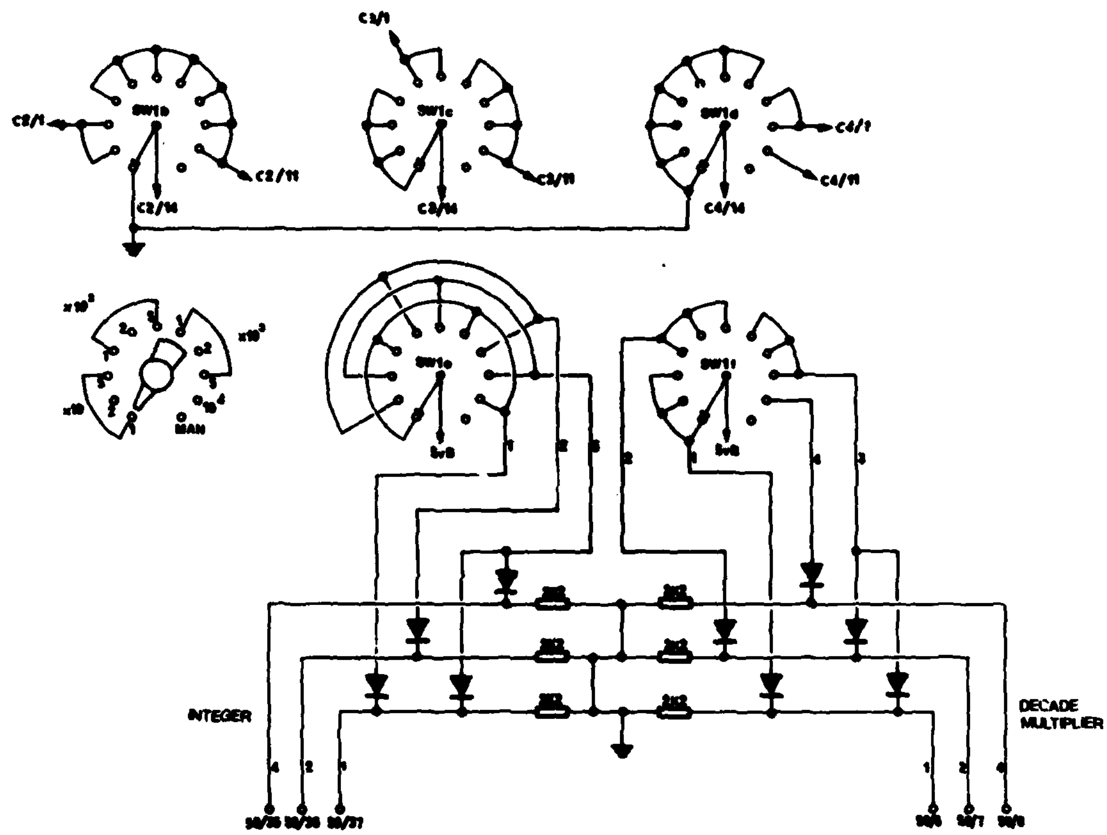


FIG. 3b - COUNT INTERVAL SWITCH

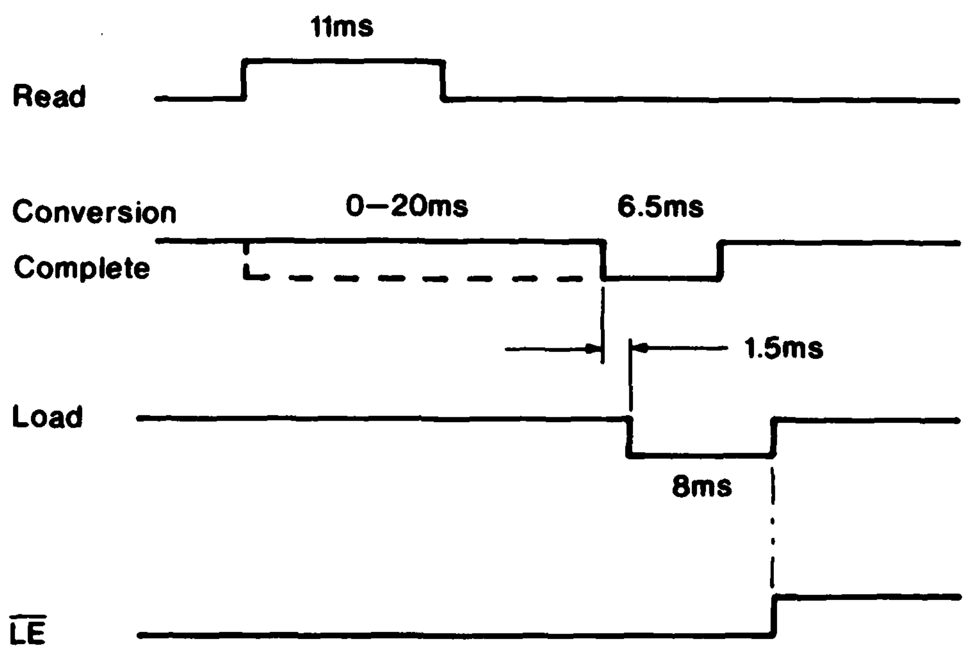
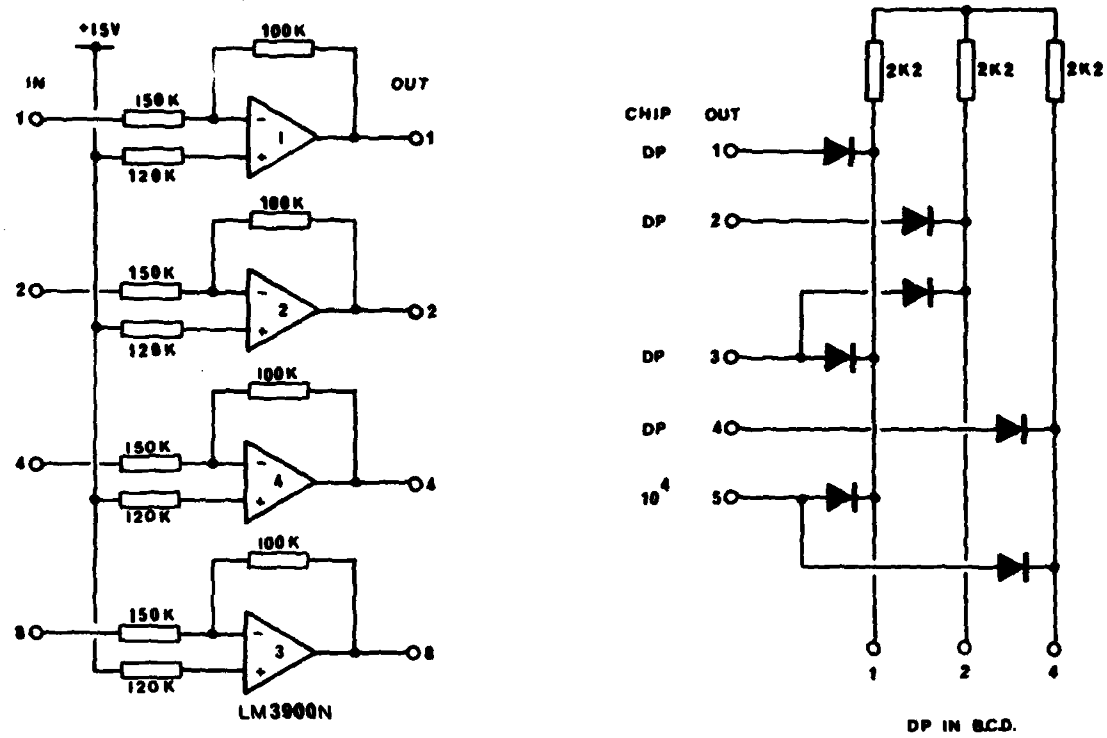


FIG. 4 - CONTROL SEQUENCE TIMING



CHIP DESIGNATION	INPUT OUTPUT No	AMP No
10^0 10^1 10^2 10^3	1	1
	2	2
	4	4
	8	3
10^4	1	1
	2	2
	5 (DP)	4
	CC	3
DP	1	1
	2	2
	3	4
	4	3

CC AMPLIFIER COMPONENTS

INPUT 390K

"+" 160K

FEEDBACK 100K

FIG. 5 - D.V.M. INTERFACE BOARD

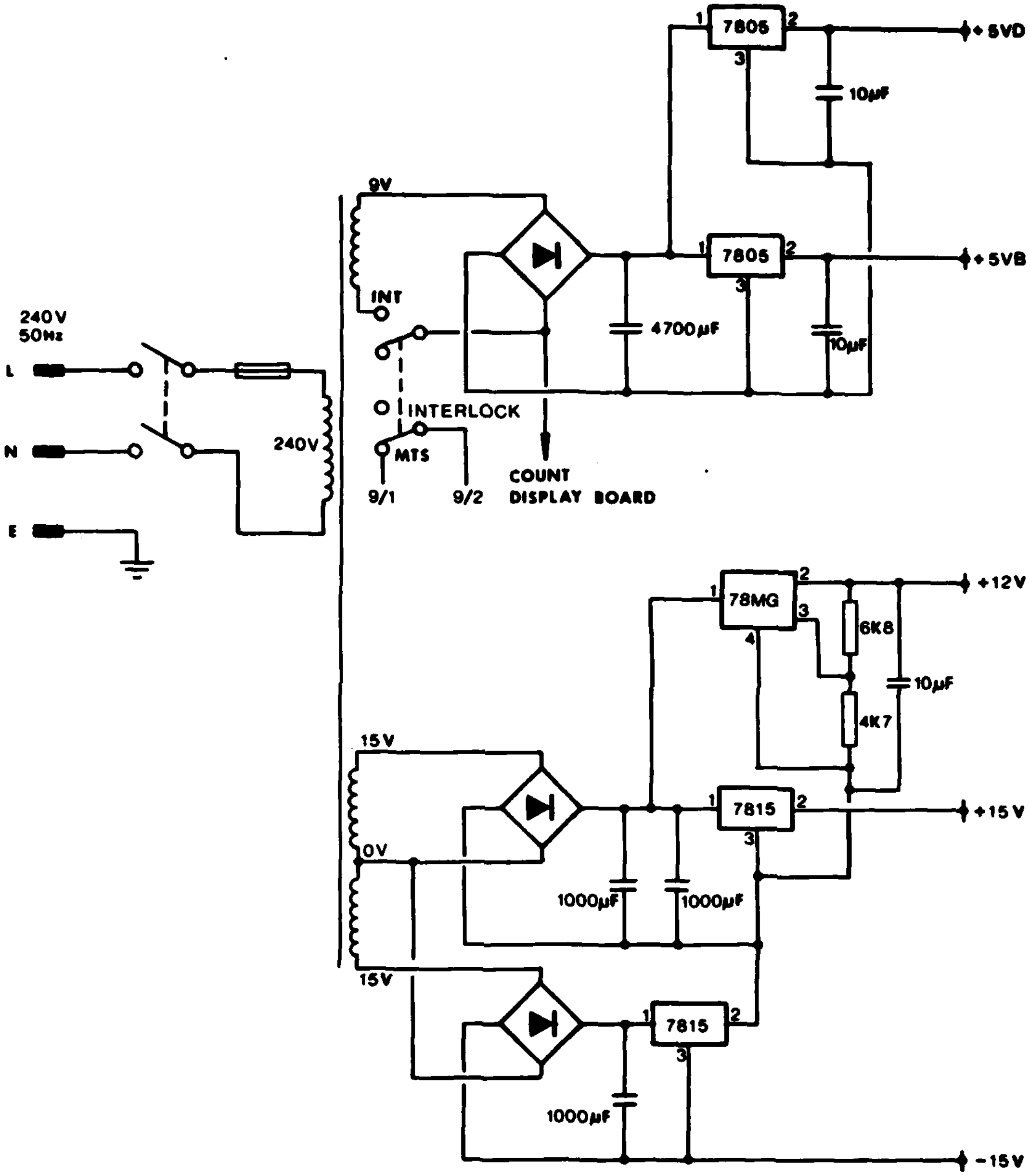


FIG. 6 - POWER SUPPLIES ON COUNTER AND INTERLOCK BOARD

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