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DYNAMIC PROPERTIES OF ELECTRONIC TRAPPING CENTERS AT THE Si-SiO_2 INTERFACE

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FINAL REPORT

N. M. JOHNSON

LEVEL II

September 1980

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U.S. Army Research Office

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The Si-SiO_2 interface possesses defects which may be considered characteristic of the thermal oxidation process. Electronic defects introduce a broad peak in the interface-state distribution which is centered ~0.3eV above the silicon valence-band maximum. Furnace anneals remove these levels yielding the generally observed U-shaped distribution. The ESR interface defect was evaluated over a range of annealing temperatures ($\leq$600 C). The spin signal rapidly decays in MOS structures annealed above 250 C. An anneal in atomic

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20. ABSTRACT (continued)

deuterium at 230 C completely annihilated the spin center, which could not be recovered with vacuum anneals up to 600 C. The surface-potential dependence of the interface spin center was investigated in order to further establish the correlation between the paramagnetic defect and interface states. It was found that the ESR amplitude changes reversibly by approximately 25% as the surface potential is adjusted between inversion and accumulation conditions.

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The metal-oxide-semiconductor (MOS) structure is the basis of many important silicon planar devices including the insulated-gate field effect transistor, nonvolatile semiconductor memories (e.g., metal-nitride-oxide-semiconductor and floating-gate MOS devices), and charge transfer devices. The operation of MOS devices is based on the ability to modulate the electrical conductivity of the silicon surface by an applied electric field; consequently the electronic properties of the Si-SiO_2 interface strongly influence device operation.[1,2] This interface possesses electronic defects that generally degrade device performance. Electrical measurements reveal the following two manifestations of interface defects: (1) a continuous distribution of interface trapping levels that extends throughout the silicon forbidden energy band and (2) a random spatial distribution of fixed positive charge situated in the oxide near the interface. The fixed space charge acts as a static sheet charge which contributes, for example, to non-zero turn-on voltages in MOS field-effect transistors. Interface states primarily influence device performance through their dynamic interaction with mobile charge carriers in the silicon. The microscopic identities of the interface defects which are responsible for the above electrical characteristics have not been established.

The electronic properties of the interface strongly depend on materials processing. On state-of-the-art MOS devices it is generally found that the Si-SiO_2 interface possesses a U-shaped continuum of interface states in the silicon bandgap with the minimum density located near midgap.[3,4] This distribution, with midgap densities of $\leq 1 \times 10^{10}$ eV^{-1} cm^{-2}, is obtained by the combination of a high-temperature, post-oxidation anneal[5] and a low-temperature, post-metallization anneal.[6] For interfaces obtained by thermal oxidation without a subsequent anneal, the interface-state distribution is dominated by a broad peak centered approximately 0.3 eV above the silicon valence-band maximum.[7,8] This peak may be considered the signature of an inherent interface defect. Theoretical studies have shown that such a

peak can arise from silicon dangling bonds at the interface.[9] Trivalent silicon defects at the $Si\text{-}SiO_2$ interface have been identified by electron spin resonance (ESR).[10] The spin density correlates with the density of (midgap) interface states but not with the annealing behavior of the fixed positive space charge. In the present study, the nature of this correlation was further examined with specific attention given to the annealing behavior of the characteristic interface-state distribution and low-temperature ($\leq$600 C) annealing of the spin center. This study, with experimental results and discussion, is presented in Appendix A.[11] The results provide the most direct evidence to date that subjecting aluminum-gate MOS devices to a conventional low-temperature anneal (i.e., sinter) leads to hydrogenation of silicon dangling bonds at the $Si\text{-}SiO_2$ interface. Also, the results suggest that, while both the electronic interface defect and the interface spin center are removed at low temperatures, the annealing processes are not identical. Further study is required to establish the nature of the correlation between these characteristic interface defects.

Based on the report[10] that the interface paramagnetic defect density is correlated with the interface-state density (at midgap), a study was initiated of the surface-potential dependence of the interface spin center. The research was conducted in collaboration with Dr. E. H. Poindexter and co-workers at the U.S. Army Electronics Technology and Devices Laboratory (Fort Monmouth, New Jersey). Initial results from this study are presented in Appendix B.[11] It is shown that the amplitude of the interface ESR signal changes reversibly by approximately 25% as the surface potential in the MOS test device is adjusted between inversion and accumulation conditions. The results confirm that the spin defect is located within 10A of the interface and suggest that the trivalent silicon defect is part of a host site for interface charge trapping, although it may not itself act as a trap. It is anticipated that the ESR-compatible MOS test structure will be a useful probe in future interface defect studies.

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APPENDIX A

CHARACTERISTIC DEFECTS AT THE Si-SiO_2 INTERFACE

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ABSTRACT

The Si-SiO_2 interface possesses defects which may be considered characteristic of the thermal oxidation process. Electronic defects introduce a broad peak in the interface-state distribution which is centered ~0.3 eV above the silicon valence-band maximum. Furnace anneals remove these levels yielding the generally observed U-shaped distribution. The ESR interface defect was evaluated over a range of annealing temperatures ($\leq$600 C). The spin signal rapidly decays in MOS structures annealed above 250 C. An anneal in atomic deuterium at 230 C completely annihilated the spin center, which could not be recovered with vacuum anneals up to 600 C.

INTRODUCTION

It has been established that the Si-SiO_2 interface possesses electronic defects which may be considered characteristic of the thermal oxidation process. Electrical measurements on MOS devices reveal a continuous distribution of interface states that extends throughout the silicon forbidden energy band and a random spatial distribution of fixed positive charge situated in the oxide near the interface. For interfaces obtained by thermal oxidation without a subsequent anneal, the interface-state distribution is dominated by a broad peak centered approximately 0.3 eV above the silicon valence-band maximum[1,2] This peak may be considered the signature of an inherent interface defect. Theoretical studies have shown that such a peak can arise from silicon dangling bonds at the interface.[3] Electron spin resonance (ESR)

reveals the presence of a paramagnetic center, designated as the P_b center, at the Si-SiO_2 interface which has been identified as a trivalent silicon defect bonded to three silicon atoms, with the dangling bond oriented normal to the interface on (111) silicon.[4] The spin density correlates with the density of (midgap) interface states but not with the annealing behavior of the fixed positive space charge. In this paper the nature of this correlation is examined moie closely with specific attention given to the annealing behavior of the characteristic interface-state distribution and low-temperature ($\leq$600 C) annealing of the spin center.

SAMPLE PREPARATION AND MEASUREMENT TECHNIQUES

Specimens for both electrical and ESR measurements were prepared from single-crystal silicon wafers. The wafers were oxidized in dry O_2 at 1000 C. Specimens which received no further thermal processing are designated "as oxidized." Other specimens received a 1000-C anneal in either argon or nitrogen in order to evaluate the effect of high-temperature anneals. All specimens were rapidly cooled to room temperature in the furnace ambient. MOS structures were formed by vacuum evaporating aluminum films with an RF-induction heated source; this avoided the generation of radiation damage in the SiO_2 layer.

Electrical measurements were performed on MOS capacitors fabricated on (100)-oriented p-type silicon. Deep-level transient spectroscopy (DLTS) and the quasistatic capacitance-voltage (QSCV) technique were used to measure electronic defect levels at the Si-SiO_2 interface. The DLTS measurement was performed in the constant-capacitance mode, which has distinct advantages for data analysis.[1] The experimental and analytical techniques for obtaining the interface-state distribution from CC-DLTS measurements are discussed elsewhere.[1,5] The QSCV technique provides the interface-state distribution over the central portion of the semiconductor bandgap.[6]

ESR measurements were performed on (111)-oriented p-type silicon wafers, with both surfaces polished. Specimens for ESR did not receive a high-temperature anneal. Room temperature ESR absorption spectra (X band) were measured at a nonsaturating power level and digitally recorded. Spin densities and g values were calculated by comparison with a weak pitch standard and DPPH.

EXPERIMENTAL RESULTS

In this section, results are presented from electrical and ESR measurements of characteristic defects at the thermally oxidized silicon surface. The interface-state distribution in as-oxidized and annealed MOS capacitors was measured by DLTS and QSCV techniques. ESR was used to investigate low-temperature ($\leq$600 C) annealing of the interface spin center.

Interface-state distributions are shown in Fig. 1 for as-oxidized and annealed MOS capacitors. The distributions were obtained from the QSCV technique. For the as-oxidized sample the interface-state distribution displays a prominent peak located approximately 0.3 eV above the silicon valence-band maximum. On (100)-oriented silicon, the peak density is $\sim 1 \times 10^{12}$ eV^{-1} cm^{-2}. A furnace anneal in argon at the temperature of oxidation results in an overall reduction of the interface-state density across the silicon bandgap, with the characteristic peak remaining the dominant feature. The addition of a standard forming-gas (15% H_2, 85% N_2) anneal, performed after aluminum deposition, results in a substantial reduction of the interface-state density and essentially complete removal of the characteristic peak. Remaining is the U-shaped interface-state distribution which is generally observed in fully processed MOS test devices.

The effect of the annealing ambient on the interface-state distribution is shown in Fig. 2. The distributions were measured by CC-DLTS. In a previous study it was

shown that the cross section for hole capture, σ_p, is essentially constant and equal to 1×10^{-14} cm^2 for the characteristic interface-state distribution on oxidized (100)-oriented silicon.[2] The results in Fig. 2 show that a high-temperature post-oxidation anneal in either argon or nitrogen reduces the interface-state density over the measured energy interval, with nitrogen more effective as an annealing ambient. The characteristic peak clearly dominates the interface-state distribution in the CC-DLTS measurement, with the peak located approximately 0.25 eV above the silicon valence-band maximum. Near the silicon midgap the DLTS measurement is influenced by minority-carrier surface generation and bias-dependent trap occupation statistics and therefore does not yield the interface-state distribution; this is signified by the dashed-line segments in the distributions.

The ESR absorption spectrum for the interface defect center is shown in Fig. 3. The specimen consisted of (111)-oriented silicon, with both surfaces polished, which was oxidized in dry O_2 at 1000 C to yield an SiO_2 thickness of 2000 A. The spectrum was obtained with the magnetic field H_o normal to the Si-SiO_2 interface and was averaged over five scans to improve the signal-to-noise ratio. The dominant spin signal has a g-value of 2.0015 ± 0.0001 (for $H_o \perp$ interface). This is in agreement with results from previous studies of the Si-SiO_2 interface.[4] The interface ESR signal in Fig. 3 corresponds to a spin density of $6 (\pm 1) \times 10^{11}$ spins/cm^2. Also identifiable in the absorption spectrum is a weak signal with an isotropic g-value of 2.0057. By systematically varying the ratio of edge-to-surface area, it was demonstrated that this signal originates from the edges of the specimen and can be ascribed to dangling bonds on the rough-cut and exposed edges of the silicon wafer.

The effect of isochronal anneals on the interface spin density is shown in Fig. 4. For this study the thermally oxidized (111)-oriented silicon wafers were coated with 1000 A of aluminum. The MOS specimens were annealed in vacuum ($\sim 10^{-6}$ Torr)

for 15 min. at the specified temperatures. After annealing, the aluminum films were chemically etched for ESR measurements, in order to prevent loading of the microwave cavity. In specimens annealed with aluminum, the spin density decreases rapidly to zero for anneal temperatures above 250 C. As a means of assessing the role of the aluminum film, a single specimen which had been annealed with aluminum at 250 C was further annealed without aluminum. As shown in Fig. 4, temperatures above 400 C were required to significantly affect the spin density, and temperatures above 500 C were required to completely annihilate the spin signal. In a third experiment a specimen, with the aluminum removed, was annealed in atomic deuterium at 230 C for a time sufficient to completely remove the spin signal. The specimen was then vacuum annealed at successively higher temperatures from 230 C to 600 C. As shown in Fig. 4, the P_b spin signal was not regained for anneal temperatures up to 600 C.

The effect of low-temperature isochronal anneals on the interface-state distribution is shown in Fig. 5. The distributions were measured by the QSCV technique on (100)-oriented silicon specimens. On MOS capacitors the vacuum anneals reduce the interface-state density nearly uniformly over the silicon bandgap. After a 400-C anneal, the density of the characteristic peak has decreased by approximately 60%.

DISCUSSION AND CONCLUSIONS

With integrated-circuit quality MOS devices, it is generally found that the Si-SiO_2 interface possesses a U-shaped continuum of interface states as illustrated by the bottom curve in Fig. 1. Such distributions are obtained by the combination of a high-temperature post-oxidation anneal and a low-temperature post-metallization anneal. As shown in Fig. 1, the as-oxidized interface does not possess a U-shaped distribution. Rather, the defect-level continuum is dominated by a broad peak

centered approximately 0.3 eV above the silicon valence-band maximum. A high-temperature anneal results in a reduction of the interface-state density over the entire measured energy interval (see Figs. 1 and 2). However, the low-temperature post-metallization anneal completely removes the characteristic peak, yielding the U-shaped distribution in Fig. 1. For aluminum films on SiO_2 it has been proposed that the low-temperature anneal releases residual hydrogen at the metal-oxide interface which subsequently diffuses to the Si-SiO_2 interface where it reacts with silicon dangling bonds.[7,8] However, this mechanism has been considered speculative because the exact chemical nature of the interface defect has not been identified.

The results presented in Fig. 2 were obtained by CC-DLTS and provide an independent absolute measurement of the interface-state distribution for comparison with the results from the QSCV technique shown in Fig. 1. Both methods clearly establish the existence of the characteristic peak in the interface-state distribution. The CC-DLTS measurement further provides the cross section for majority carrier capture at the interface defects.[1,5]

The P_b interface spin center has been identified with trivalent silicon, and the spin density varies with silicon crystal orientation and oxidation/annealing conditions in a manner similar to interface states.[4] In this study, low-temperature isochronal anneals were used to obtain detailed information on the spin center for comparison with electrical measurements. The ESR measurements were conducted on (111)- rather than (100)-oriented silicon because of the higher spin density.[4] Figure 4 presents the first detailed information on the low-temperature annealing behavior of the interface spin center. For aluminum coated oxides, the P_b spin density decreases rapidly for anneal temperatures above 250 C. This behavior is attributable to the composite MOS structure, as evidenced by the significantly different response for samples annealed without aluminum. With the identity of the interface defect, the

above low-temperature annealing mechanism may be applied as follows: spin-center annihilation during anneals with aluminum is caused by the release of atomic hydrogen at the aluminum-SiO_2 interface which subsequently diffuses through the oxide layer and reacts with trivalent silicon defects to form stable non-paramagnetic silicon-hydrogen bonds. The role of atomic hydrogen in removing the P_b spin signal is further established with the results from the atomic deuterium anneal. Exposure of the oxidized silicon to atomic deuterium at 230 C completely annihilated the P_b center, and the signal was not recovered with subsequent isochronal anneals up to 600 C. This is the most direct evidence to date that subjecting MOS devices to a low-temperature anneal results in the hydrogenation of silicon dangling bonds at the Si-SiO_2 interface.

The results in Fig. 5 provide information on low-temperature annealing of interface states for comparison with the ESR results. Specifically, isochronal vacuum anneals of MOS capacitors reveal that even after a 400-C anneal (for 15 min.) a significant interface-state density remains, with the characteristic peak reduced in density by only ~60%. Figure 1 illustrates that a conventional 450-C furnace anneal (for 60 min.) produces the U-shaped distribution. However, the electrical measurements were performed on (100)-oriented silicon and therefore do not permit a direct comparison with the ESR data; the requisite electrical measurements on (111)-oriented silicon are in progress. The above results suggest that, while both the electronic interface defect and the P_b spin center are removed at low temperatures, the annealing processes are not identical. Further study is required to establish the nature of the correlation between these characteristic interface defects.

ACKNOWLEDGEMENT

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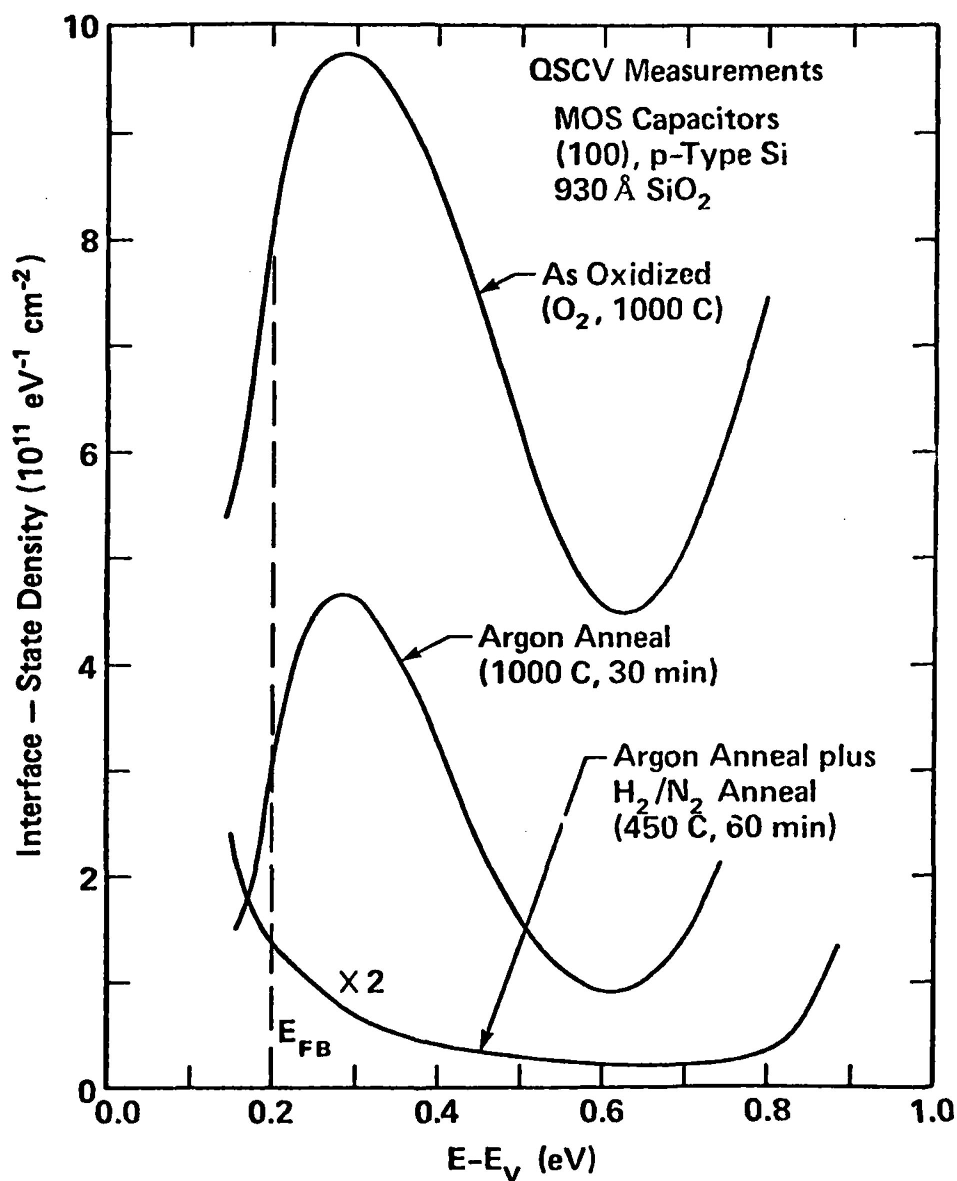

Fig. 1. Interface-state distributions in as-oxidized and annealed MOS capacitors.

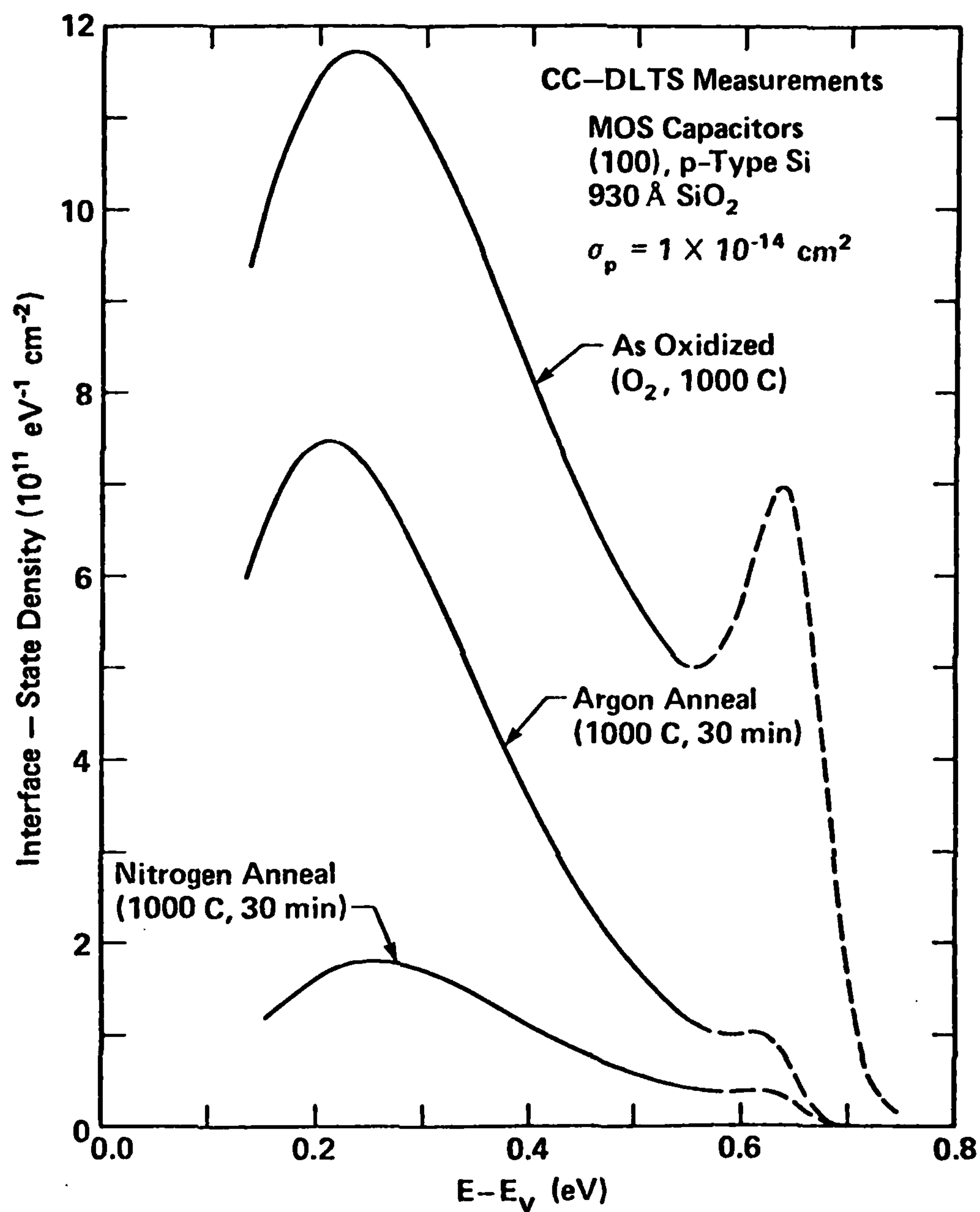

Fig. 2. Effect of high-temperature anneals on the characteristic interface-state distributio

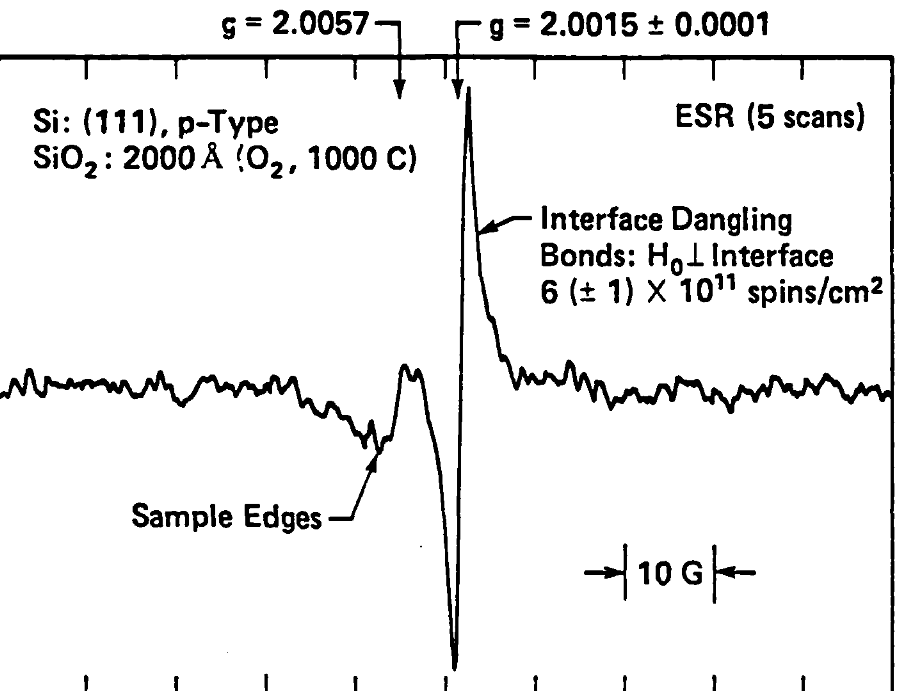

Fig. 3. ESR absorption spectrum for the P_b defect center at the Si-SiO_2 interface.

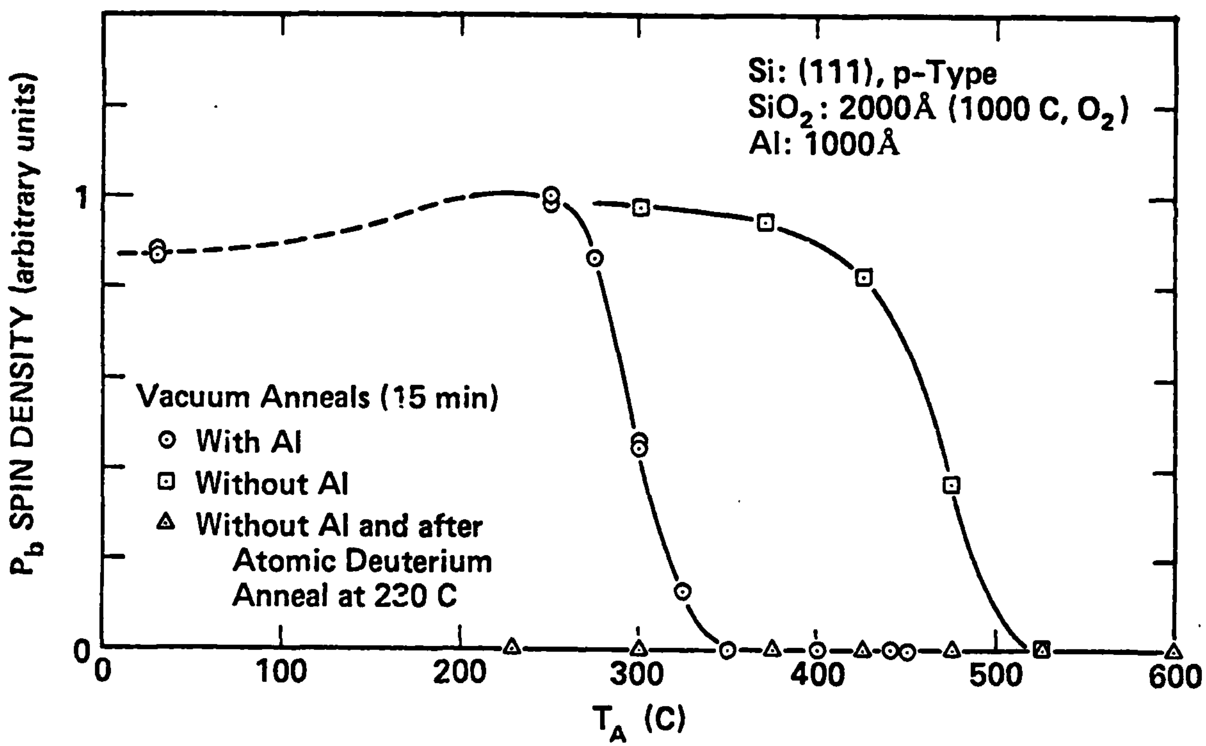

Fig. 4. Isochronal annealing of the P_b spin center in as-oxidized and deuterium-annealed specimens.

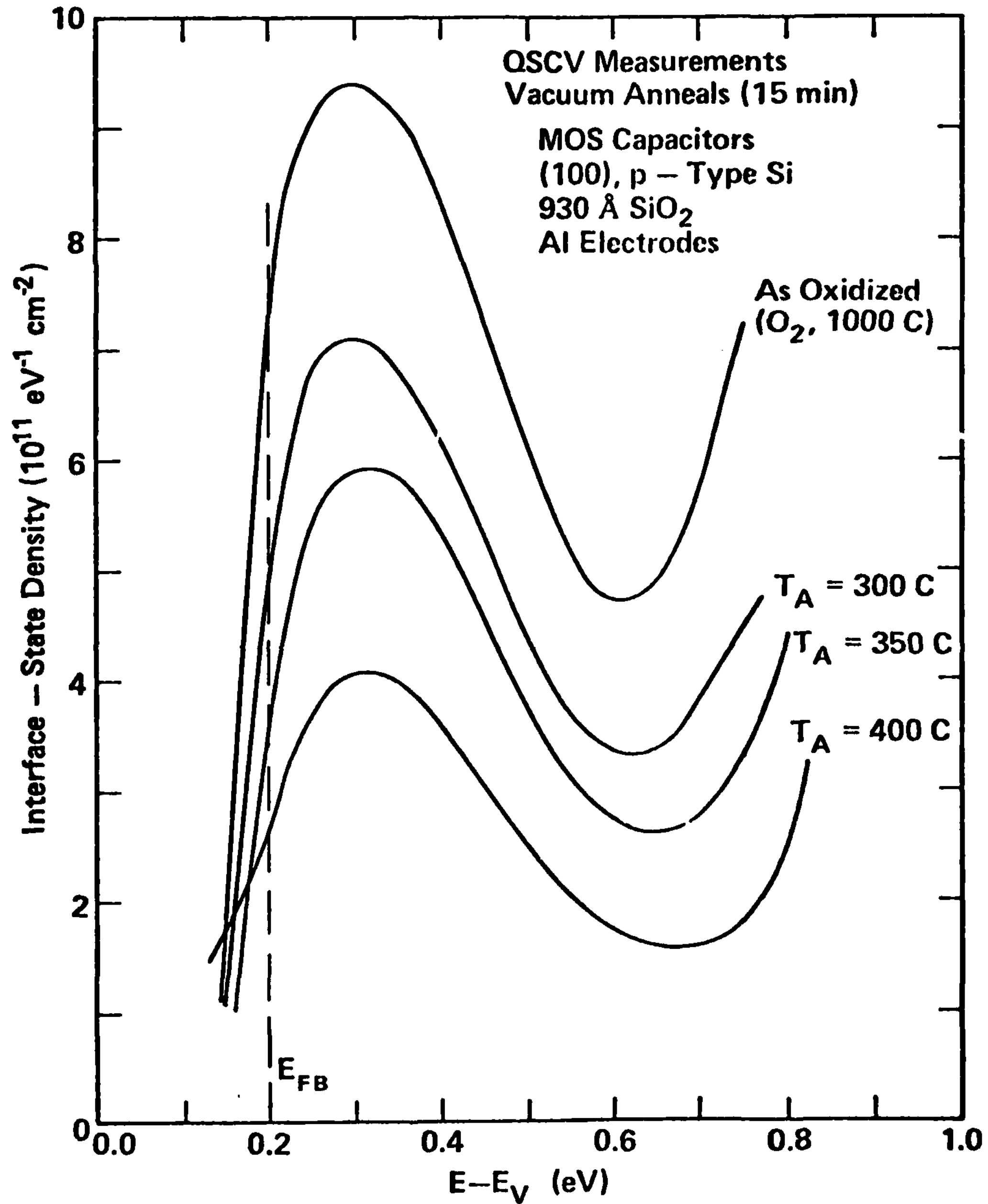

Fig. 5. Isochronal annealing of the characteristic interface-state distribution in as-oxidized MOS capacitors. The QSCV results are unreliable for energies that are nearer to the valence bandedge than the bulk Fermi energy E_{FB}.

APPENDIX B

SURFACE-POTENTIAL DEPENDENCE OF EPR CENTERS AT THE Si/SiO_2 INTERFACE

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ABSTRACT

Quantitative correlation of midgap D_{it} with the EPR P_b center $\cdot Si \equiv Si_3$ on oxidized (111) silicon suggests a possible contribution to D_{it} by this Si^{III} defect. An external voltage might thus affect the population of the spin center. We have now observed a variation in EPR amplitude of this center with an electric field normal to the interface during the measurement. A bias variable between +15 and -10 volts was applied to a 1000 A, 1 cm^2 aluminum electrode deposited on the oxide of a (111) silicon wafer. The EPR amplitude declined reversibly about 25% between 0 and -4 volts. In situ C-V measurements of surface potential indicate that the responsive component of the P_b center is just below the Fermi level in 50Ωcm p-type silicon. Details of further tests and suggested structural and electrical models will be discussed.

INTRODUCTION

The paramagnetic P_b defect center at the Si/SiO_2 interface of oxidized silicon wafers has been observed to be correlated with interface trap density D_{it} over a variety of material and processing variations.[1-3] The P_b spin concentration is quantitatively about equal to midgap D_{it}. The P_b center itself has been tentatively identified as a trivalent silicon defect, mainly $\cdot Si \equiv Si_3$, oriented to fit the respective crystallographic directions of non-bonded Si orbitals at the Si/SiO_2 interface of (111) or (100) wafers.[2] Because of the time-honored supposition that Si^{III} is a major source of interface states, it is of immediate interest to determine the exact nature of the connection (if any) between P_b and D_{it}.

Several possible situations can be imagined: (a) Si^{III} itself is a chargeable electrical trap, and a direct source of D_{it}; (b) Si^{III} is an intrinsic feature of the P_b center, but D_{it} arises from ancillary charges in the center; or (c) the P_b-D_{it} relation is indirect, or even coincidental. Important evidence on this question should be obtained from the behavior of the EPR signal with a DC potential applied normal to the Si/SiO_2 interface. In case (a) above, it might be expected that the shift of the P_b level(s) with respect to the Fermi level at the interface would cause a change in the occupancy of the center, varying between 0, 1, or 2 electrons as the interface goes from accumulation to depletion under different surface potentials. Thus a decisive effect on P_b amplitude would strongly support case (a). A weak effect would support (b), and no effect, (c).

EXPERIMENTAL DETAILS

Sample preparation for voltage-controlled EPR is a delicate compromise between serious difficulties. Leakage-prone large capacitors (1 cm^2) were required for useful EPR signal-to-noise ratio; these were fabricated on single-crystal (111) silicon wafers, p-type (boron doped), 20-50Ωcm. For electrical contact to the silicon substrate with minimal cavity loading, one edge was ion implanted with a high dose of boron prior to oxidation. Wafers were oxidized in dry O_2 at 1000 C for oxide thickness of 1980 A, then rapidly cooled in the O_2 ambient. This procedure maximizes P_b. Silicon dioxide was selectively removed from the wafer back and from the boron-implanted substrate-contact region prior to vacuum deposition of an aluminum thin film. The aluminum thickness was kept to less than 1000 A, to minimize cavity loading. Evaporation was performed with an rf induction-heated source to avoid radiation damage in the SiO_2. The Al layer was selectively etched to define the gate electrode and substrate contact. These oxidation and processing procedures have been shown to produce and retain electronic defects which may be considered characteristic of the thermally oxidized silicon surfaces.[3] The sample structure is shown in Fig. 1.

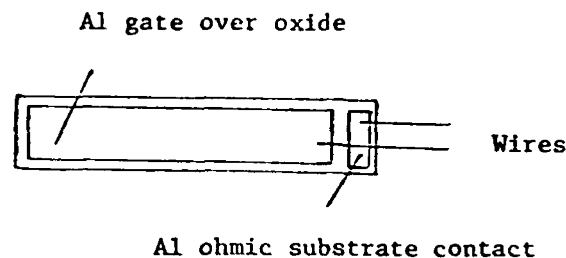

Fig. 1. Wafer sample for study of EPR P_b centers with applied DC bias.

The capacitors were electrically evaluated with conventional current and C-V techniques. Current measurements identified large-area low-leakage devices suitable for EPR. The high-frequency C-V curve is shown in Fig. 2. The C-V results were used to compute the silicon surface potential and intersection of the Fermi energy with the Si/SiO_2 interface.[4]

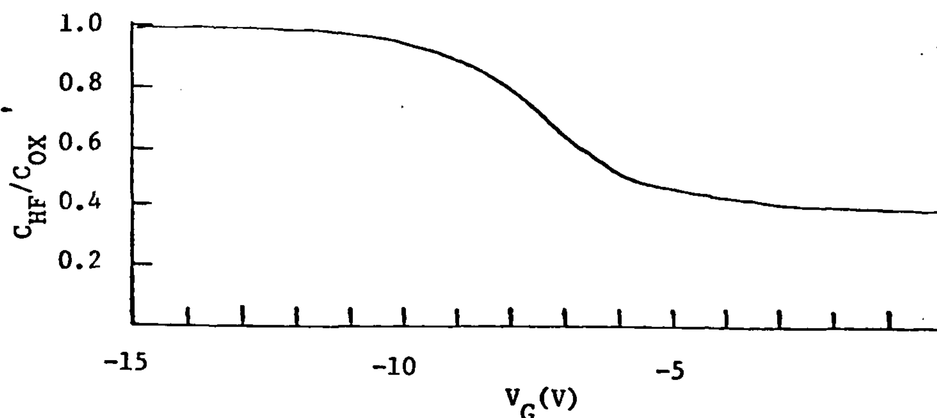

Fig. 2. High frequency C-V plot from MOS structure for EPR.

EPR at 295°K was observed on a Varian x-band spectrometer. The EPR signal was much weaker than our previous studies, which were typically made with a group of 5 samples oxidized on both sides. So it was necessary to use signal averaging, and to minimize spurious resonances. A freshly etched (resonance-free) silicon strip served as a neutral support for the test sample, and as a mount for the biasing wires. Pressure contacts were formed between the wire ends and the aluminum oxide plate and ohmic-contact plate, respectively. The fine wires did not load the cavity.

The sample assembly was suspended in the EPR cavity from the bottom of a quartz tube without an enclosing container. Applied DC potential was varied between -10V and +15 volts on the oxide plate. The leakage current with -10V was typically 1.5 ma, and the voltages indicated were not exceeded to avoid breakdown. The wafer was oriented with H_0 perpendicular to the crystal face, but the anisotropy of the P_b signal on a (111) face was confirmed.

RESULTS AND DISCUSSION

EPR signal amplitudes were measured at three microwave power levels: 2, 10, and 30 mw. The observed amplitude (in arbitrary units) for 10 mw power is plotted in Fig. 3. A large, reproducible change was observed between 0 and -4 volts. This suggests a broad spin level just beneath the zero-bias Fermi level in our 50Ωcm p-silicon.

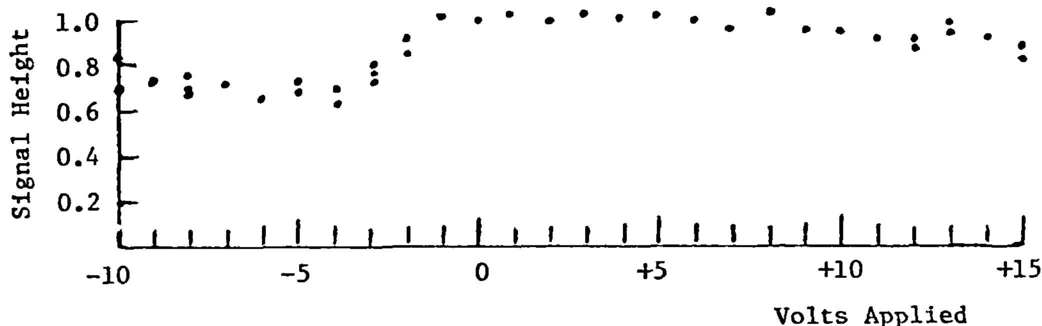

Fig. 3. EPR signal amplitude of P_b centers in MOS structure under applied DC bias.

This result, however, is misleading. When the microwave power was varied, the behavior of P_b was quite different. This indicated EPR saturation. A simple relation for signal height as a function of power P is $S=AP^{1/2}(1+KP)^{-1}$. The saturation parameter is K, and is proportional to the EPR relaxation time T_1. The spin concentration is A. The common procedure for quantitative comparison of spin concentrations is operation at low powers, $KP<<1$, so $S\sim P^{1/2}$. In our case, however, in the region of useful signal-to-noise, this is not true; amplitude data must be corrected for saturation to yield the true spin concentration. The saturation parameter K as a function of applied voltage was derived from the data at three power levels, and is shown in Fig. 4. The relaxation parameter K varies by a factor of 3 between 0 and -4 volts bias.

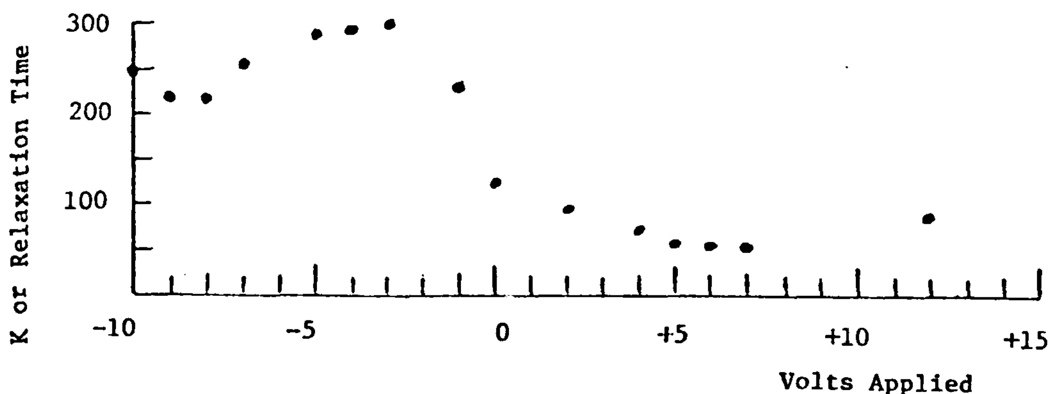

Fig. 4. Relative EPR relaxation time of P_b centers under applied DC bias.

The variation of K with applied voltage is a very significant finding. A readily reversible effect, stronger with positive bias, suggests coupling of P_b spins with mobile electrons attracted to the interface in the inversion regime. Simple spin-spin relaxation requires interacting spins to be within ∿10 A of each other, i.e., much closer than the tunneling limit. The P_b electrons are thus in close communication with the silicon. It cannot be stated whether the relaxation effect arises from mobile conduction electrons, or from electrons trapped near the $\cdot Si{\equiv}Si_3$ defect. The latter situation is case (b), defined in the introduction: Si^{III} as an intrinsic component of a host site for band-gap charge traps. The apparent close coupling of P_b with silicon electrons has another important meaning. It reinforces other lines of reasoning which place P_b at or very near the interface (i.e., etching experiments; the orientation dependence of P_b, uniquely acceptable at the interface, but very implausible in either the bulk Si or SiO_2).

The occupancy and energy level structure of P_b spin centers are of great interest. Saturation-corrected spin concentration is related to surface potential (E_F-E_V) in Fig. 5. It is emphasized that this is an uncertain result and is presented mainly to illustrate the theory of case (a), above. If Fig. 5 were indeed correct, it can be interpreted with two species of spin centers: (1) a donor level D just above the valence band, normally doubly occupied at zero bias: (2) an amphoteric center with donor level A_1 a little below midgap, and conjugate acceptor level A_2 near the conduction band. These levels are sketched in Fig. 6. At high negative bias A_1 and A_2 are empty; but a tail of D is above the Fermi level and thus singly occupied, yielding an EPR signal. With electron accretion at -4v bias, A_1 crosses the Fermi level, becomes singly occupied, and has an EPR signal. Finally, at high positive bias, A_2 gains an electron, which pairs with the A_1 electron, reducing the EPR signal. It is noteworthy that a similar amphoteric model has been invoked for optically-stimulated EPR in hydrogenated amorphous Si.[5]

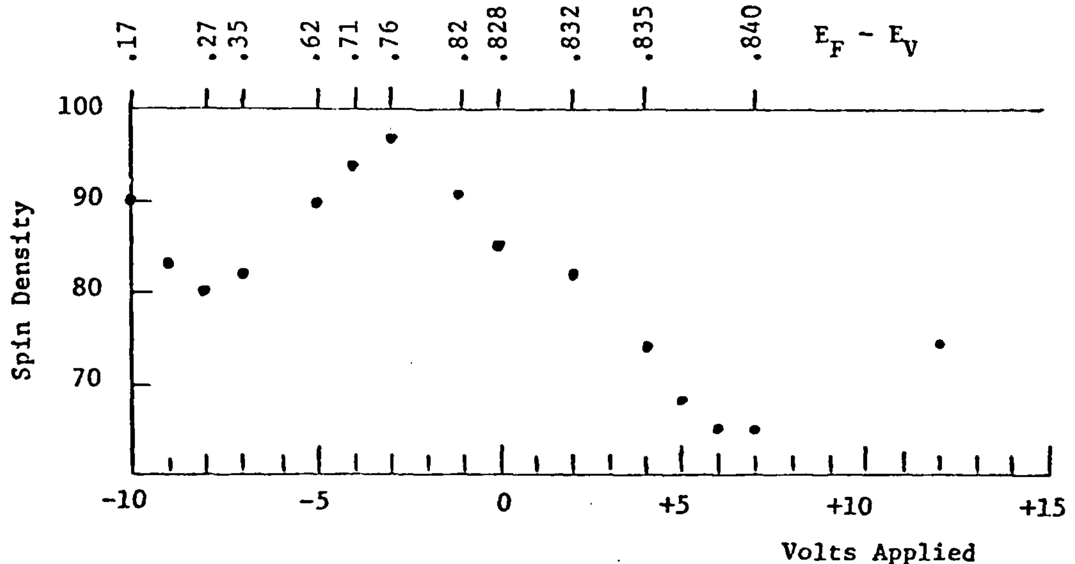

Fig. 5. Apparent P_b spin concentration under applied DC bias.

CONCLUDING REMARKS

Electrical control of a spectroscopic signal from the Si/SiO_2 interface is of considerable interest and reduces the likelihood of case (c), mentioned earlier, for the role of Si^{III} at the interface. The amplitude of the P_b ($\cdot Si{\equiv}Si_3$) EPR signal in p-doped silicon wafers has been observed to vary as a function of applied voltage.

Most or all of the effect is due to a change in electron relaxation time. The shorter time occurs with positive applied bias, and may reflect interaction of P_b electrons with interface electrons in the inversion regime of p-type silicon. The relaxation effect shows that P_b centers are in close proximity (10 A) to interface electrons. Not only does this substantiate the interface location of P_b, but it also suggests that Si^{III} may be part of a host site for interface charge traps (case (b), above), even if it does not itself act as a trap.

A number of experimental problems prevent confident deduction of net voltage-dependent spin concentration at this time. Sample burn-out precluded application of high potentials in the interesting regions near band-gap edges. The large relaxation effect over-shadows any spin population change. Nonetheless, this sharp change in electron T_1 indicates that the interface is usably uniform despite leakage currents. Improved technique may allow better measurement of spin concentration and possible discrimination between cases (a) and (b) for the role of $\cdot Si \equiv Si_3$ in regard to interface states.

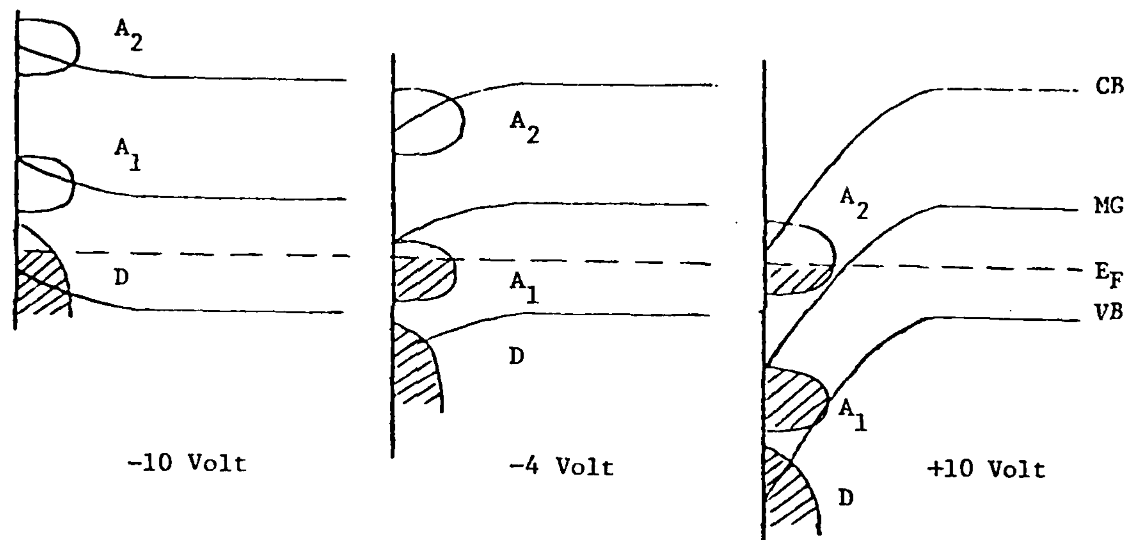

Fig. 6. Hypothetical spin-level structure and occupancy of P_b centers.

ACKNOWLEDGMENT

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