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TACTICAL VIDEO DISPLAY.(U)
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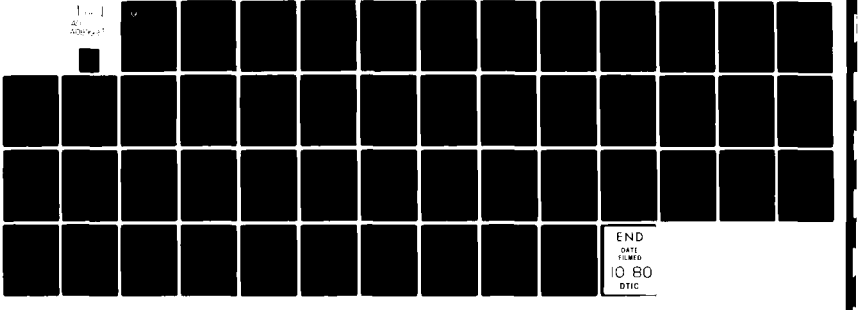

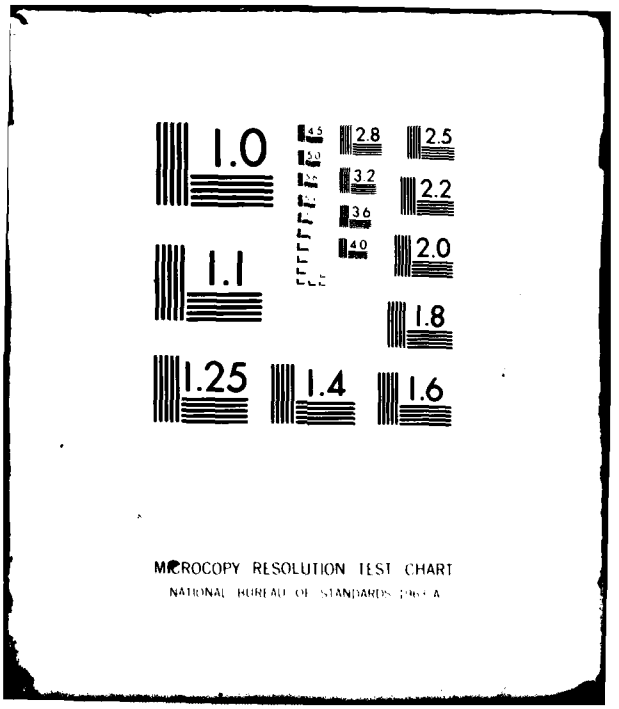
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MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963-A

Research and Development Technical Report

DELET-TR-79-0251-1

TACTICAL VIDEO DISPLAY

T. A. Gielow
R. H. Holly
HYCOM INCORPORATED
16841 Armstrong Avenue
Irvine, CA 92714

September 1980

First Interim Report for Period 10 Jun - 10 Dec 1979

Prepared for:
ELECTRONICS TECHNOLOGY & DEVICES LABORATORY

ERADCOM

US ARMY ELECTRONICS RESEARCH AND DEVELOPMENT COMMAND
FORT MONMOUTH, NEW JERSEY 07703

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Drive circuitry

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Hycom has completed the first phase of a development program to design and fabricate a 512 x 640 line electroluminescent display. The program entails two major areas of efforts: the first is to improve the display panel and the second is to improve the drive electronics. The display panel in this program is larger and is of higher resolution than any previous TFEL panel. The panel also incorporates a black layer to absorb refracted light and to enhance the contrast. The drive circuitry effort is to develop circuitry which will provide video

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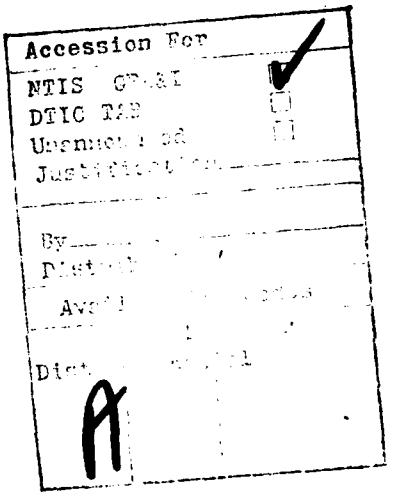
modulation with low power dissipation. The objective is to design a driver that can overcome the capacitive and resistive parameters of the panel while still being implementable in a compact and inexpensive form.

Preface

The fabrication of the TVD panels is supported in part by the Sharp Corporation of Japan. The initial black layer development effort, prior to this contract, and continuing support has been funded by the Sharp Corporation.



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FIGURES

ATTACHMENTS

Introduction

The Tactical Video Display Program is a two-year development effort designed to extend the state-of-the-art in the area of thin film electroluminescent display systems. The program entails two major areas of efforts: the first is to improve the display panel and the second is to improve the drive electronics. The display panel in this program is larger and is of higher resolution than any previous TFEL panel. The panel also incorporates a black layer to absorb refracted light and to enhance the contrast. The drive circuitry development effort is to develop circuitry which will provide video modulation with low power dissipation. The objective is to design a driver that can overcome the capacitive and resistive parameters of the panel while still being implementable in a compact and inexpensive form.

During the first six months of this program there have been several significant changes in the technical approach. Some changes have originated with ERADCOM personnel and some have originated with Hycom personnel. All of these changes have been to enhance the level of development that is to be achieved under the original goals of the program. Some of the more important design approach changes will be described in the section entitled "Technical Approach Changes".

Technical Approach Changes

The first technology tradeoff was in the size of the panel itself. A size limitation of the equipment available to us made the total glass size smaller than requested but we increased the line density to maintain the exact number of row and column elements. One of the main goals of the TVD program is to show that the TFEL technology is capable of producing bright, clear, multi-shaded images while being multiplexed on the basis of 512 line times. The tradeoff of total size for line density does not reduce the significance of this demonstration.

Another tradeoff made early in the program was to incorporate a full frame bit map to serve as a scan converter between standard interlaced television and the higher frame rates that enhance the performance of TFEL display systems. The bit map, dynamic MOS RAM, will be incorporated with the panel drivers to enhance their performance and to add flexibility to the modes of operation.

The greatest area of technology change is the panel driver circuitry. In our proposal we described a system that used monolithic MOS drivers and hybridized diodes to perform the drive function utilizing a minimum of driver circuitry mounting area. This approach was replaced by bipolar hybrid drivers uing a drive technique similar to most of our previous efforts when

we discovered the power loss due to electrode line heating that would accompany the use of these MOS drivers with a panel the size of the TVD panel. Bipolar transistors seemed to be the only drive elements that would handle the required voltage and surge currents. A study of the manufacturers of bipolar IC's led us to conclude that we had to use hybrids. During the hybrid development effort, a great amount of data about drivers, transistors, hybrids and TFEL panels were developed. Out of this study several new driver architectures were explored and a new promise of performance was realized. It was then discovered that a new breakthrough in the MOS technology area had occurred which meant the MOS transistors had on-state current surge characteristics which made them as good as bipolar for our purpose. It was also learned that these high current MOS transistors could be fabricated as C-MOS integrated circuits. After a few slight adjustments to the driver structure we found that we could again have a nearly monolithic drive scheme. At the present time the design work on the two new MOS IC's is underway and the promise of a more efficient flat panel display system is becoming a reality.

Accomplishments

I. Black Layer

The black layer we are now concentrating our efforts upon is what we believe to be unique to Hycom. We have found it to be more stable and less contaminating than the black layer processes which we have patterned our earlier efforts after as reported by other researchers. Our black layer obtains its black properties chiefly from the fact that it is a semiconductor with the proper band gap energy to absorb visible light photons, and in addition, we have been able to create a rounded surface dendrite type grain structure that greatly enhances the probability of absorption.

The procedure used to produce our black layer is to sputter ZnS in an atmosphere containing a small amount of sulfur hexafluoride in argon. The film properties are very sensitive to the substrate temperature and input power density, but the reproducibility of the film seems very good. Our present efforts are to zero in on the film properties which are to be optimized. This optimization will resolve the relationship between film absorption and film conductivity. The films have been produced as either poor dielectrics or good conductors. The dielectric film, which is our best film and our first choice, is produced using a very low power input.

The resistivity of the dielectric film is high enough to avoid the electric field spreading effect that would destroy the apparent panel resolution.

The stability and the passivity of the black layer film in the total structure appears to be very good but longer term testing is still required. There are still several obstacles to delivering the TVD panels with this black layer; the problems are all related to the fact that panels are being fabricated by a different process and in a different facility from where the black layer is added. The most obvious problem involves the adhesion and the etching of the aluminum electrodes. The adhesion problem may be related to the elapsed time between the deposition of the black layer and the aluminum layer and/or selection of the etchant. During the etching, the etchant appears to either cause the aluminum to lift up at the edges or to etch some of the black material under the aluminum. In our own laboratory we have selected a lift-off technique and we have not experienced either of these problems. To find solutions to these processing problems several smaller test panels are being exchanged, with Sharp, as part of our in-house research.

Typical electro-optical values obtained are:

$\rho \simeq 25K\Omega/\square$

Diffuse reflectance ≃ 1-2.5% (with TFEL structure, glass surface does not have AR coating)

This is presently a rather slow process; higher power input levels accelerate the deposition but the films tend to be more electrically conductive. The substrate temperature is also somewhat critical. Low temperatures cause low adhesion and high temperatures cause crystal dislocation faults in the phosphor layer. In spite of these problems we do have a good quality film with good reproducibility.

Figures 1 through 6 show curves of panels with various process parameters used to achieve a high light absorbant background. Each of these sample panels was made by depositing the black material over half of the panel thereby allowing a direct comparison of black background to aluminum background. Figures 1 and 2 are the same panel; Figure 1 is aluminum background and Figure 2 is black background. Likewise Figures 3 and 4 are paired, and Figures 5 and 6 are the same panel.

Figures 7, 8 and 9 are composites of 1 and 2, 3 and 4, and 5 and 6, respectively. From these it can be seen directly the amount of emitted light lost due to the absorption. By arbitrarily defining (but consistently using) the knee of the curve to be a doubling of the light in 10 volts, we see from Figure 7 that the knee of the aluminum is at 224 volts and 20 foot-Lamberts, whereas the knee of the black layer is at 227.5 volts and 12 foot-Lamberts. Choosing this voltage we can see that the light of the aluminum is 23 foot-Lamberts, i.e., a loss of one-half of the light. (The reflectivity is 1.67%.) Table 1 compares these properties for the three panels.

TABLE 1

Panel No.	Al Knee (volts)	BBG Knee (volts)	Al Knee (ft-L)	BBG Knee (ft-L)	Al at BBG Knee (ft-L)	Reflectivity (%)	Loss (%)
2-8	224	227.5	20	12	23	1.67	48
3-2	205	218	20	13	28	1.12	54
3-10	228	235	15	6	20	1.4	70

II. *Drivers*

We have commenced an agreement with Supertex, Inc. of Sunnyvale, California, for the design of two MOS IC's which are called the column driver and the row driver. We expect delivery of these two devices about September, 1980. A description of these devices and the expected system performance follows.

A. Column Driver IC

The column driver IC is basically a digital-to-analog converter whose conversion characteristics are controllable from an external conversion control source. This external control is necessary to fulfill different conversion requirements presented by different panels and/or display systems. Additionally, as in the case of large panels with high resolution, it is necessary to change the conversion characteristics as the particular pixel being driven changes from a location near the driven end of a column to a location at the remote end of the column. The IC contains two levels of buffering, one digital and one analog, in order to optimize the timing of the three functions (data transfer, conversion and drive) so as to maximize system performance. Documents detailing the exact implementation are being circulated between Hycom and Supertex. Copies of these documents are attached.

Some of the new features of this driver are a "push-pull" output structure that sources or sinks only the minimum required current to achieve the desired voltage on the driven column. This results in a considerable power savings and it will minimize the heating of the column conductors. The driver output circuit, the digital storage, and the converter circuit are to be implemented 16 times on each IC. As an extra feature a binary operation mode for systems without a need for shading is also being included.

B. Row Driver IC

The row driver IC performs the scanning function for the display. The outputs can pull the rows down to -200 VDC one at a time or up to +200 in unison. There is also an "up" to ground and a "down" to ground capability for removing the drive voltages from the panel. The use of this IC will also eliminate the diode buses that have a prominent part of all previous systems. This IC implements a drive system that applies high voltage bipolar signals to the rows in a similar way to our previous designs except we now have the possibility of doing this with a single 200 volt power supply. The row driver IC is presently defined as driving 16 rows. A detailed description of this device is being jointly written by Hycom and Supertex, and the current document is attached.

C. System Performance

1. Power Estimates

The greatest amount of power, in all systems known to us, is consumed in the driving of the columns. It is this fact that has produced systems where the modulation voltage is much less than the drive voltage. The column driver IC tries to solve this problem by sourcing or sinking current to drive the column to the desired voltage. The current flow from the column driver to the selected row is inconsequential compared to the current needed to drive the column to the desired voltage against the coupling effects of the other columns. The greatest current experienced by a given column is when it is driven the opposite of all the other columns; for example, it is the only column bright on a dark panel or it is the only column dark on a bright panel. When all of the columns are driven to the same brightness level the minimum current is consumed. When half the columns are at one extreme of brightness and the other half is at the other extreme, the greatest power is consumed and the greatest amount of panel heat is generated. The coupling media between the columns are the non-selected rows. In the case of the TVD panel there are 511 such rows. The non-selected rows must be allowed to float if power is to be conserved. The rows float at a voltage level between the highest column voltage and the lowest column voltage. Any column that is to be at a voltage different from the set of floating rows must be pulled up or down to achieve its proper level.

The panel's resistance and capacitance can be determined using the process parameters of 15 ohms per square for the ITO and 52 picofarads per square millimeter for the actual pixel area. The line width for the TVD panel is 0.15 mm so a column has a resistance of 13,000 ohms and a capacitance of 600 picofarads. Multiplying these two together gives a value that may be viewed as similar to a time constant. For this panel it is 7.7 microseconds. This value figures into estimates of minimum drive time and calculations of line heating. The total capacitance of the panel is 0.4 microfarads. Using the worst case data pattern (vertical stripes, half-on/half-off), and empirical ratios we have from other projects, we can estimate the heat produced due to the resistance of the columns to be about 10.5 watts. For a solid data pattern at any shade, the heat in the glass drops to about 1.5 watts.

2. Brightness Estimates

The light output of the TVD panel is directly proportional to its frame rate for any given contrast ratio (measured in dark ambient). The predicted point brightness for the TVD panel running at 90 frames per second is about 25 foot-Lamberts. At this maximum level we are not certain how dark the "off" pixels will be but we believe that it will be less than one-tenth of this value. The integrated field brightness will be only 9 foot-Lamberts because of the low percentage of active area (36%). The panel brightness suffers because of the absorbent background and the large number of lines to be multiplexed. The panel will be multiplexed on the basis of one-out-of-525. The dwell time on a row is 21 microseconds.

3. Efficiency

The efficiency in lumens per watt will be calculated based on lit area in square feet times foot-Lamberts divided by the resistive heat produced in the glass. With the full active area of 0.08 feet^2 lit to 25 foot-Lamberts, we get 2.0 lumens. Dividing by the power estimate of 1.5 watts, we get 1.33 L/w. Using the worst case power consumption and data pattern, this figure drops to 0.1 L/w. Even an all "off" pattern will be heated by about 1 watt of resistive heat so the efficiency drops to less than 0.01 L/w. Any attempt to modulate the "off" pixels further "off" will actually increase the power consumption from the modulation supply.

III. Exerciser and Test Equipment

The exerciser, which will allow us to test and demonstrate all of the system attributes as specified in the design goals, has been conceived and will be incorporated into the control logic design which will start as soon as a few critical design decisions are made on the driver IC's. The basic timing and control routines have not changed but there has been a change in the utilization and placement of the bit map. Other forms of test equipment for the "selloff" and interim demonstrations have been built or purchased. The basic operational mode is NTSC television, commonly called RS170, so a source of live video and a TV camera can be used for testing.

Conclusion

Progress to date has exceeded intial expectations in both the panel fabrication and drive circuit electronics. Due to the delay in determining the type of drivers (hybrid versus monolithic) a change in the deliverable unit is necessary. The full panel drive will be delivered upon receipt of the monolithic drive packages.

The deliverable items planned are:

EDM_{32} (May 31, 1980)

This drive system enables a complete demonstration of the TFEL panel's resolution, brightness and uniformity. This system differs from the later two systems in that only a 32x32 dot pattern is generated and this pattern is repeated 320 times over the entire active area of the panel. Some of the patterns to be implemented are "all on," "all off," "diagonal line," "checkerboards," etc. Two intermediate shading levels between on and off will be provided. Since there are only 32 lines to scan each frame time, this system will be capable of very high frame rates. To enable measurements at frame rates more closely approximating the other display systems of this contract, various numbers of dummy line times may be inserted into each frame to simulate multiplexing over the full size of the panel. Because each column driver will be driving 20 columns it may not be possible to drive the panel quite as fast as the later system due to increased capacity loading.

Physically, this system consists of two parts. One part is the panel with connectors and the other is the driver circuitry. The cable will consist of 32 column wires and 32 row wires attached to connectors that mate the 1152 contacts of the panel. The driver circuitry will be self-contained, including power supplies and pattern generators.

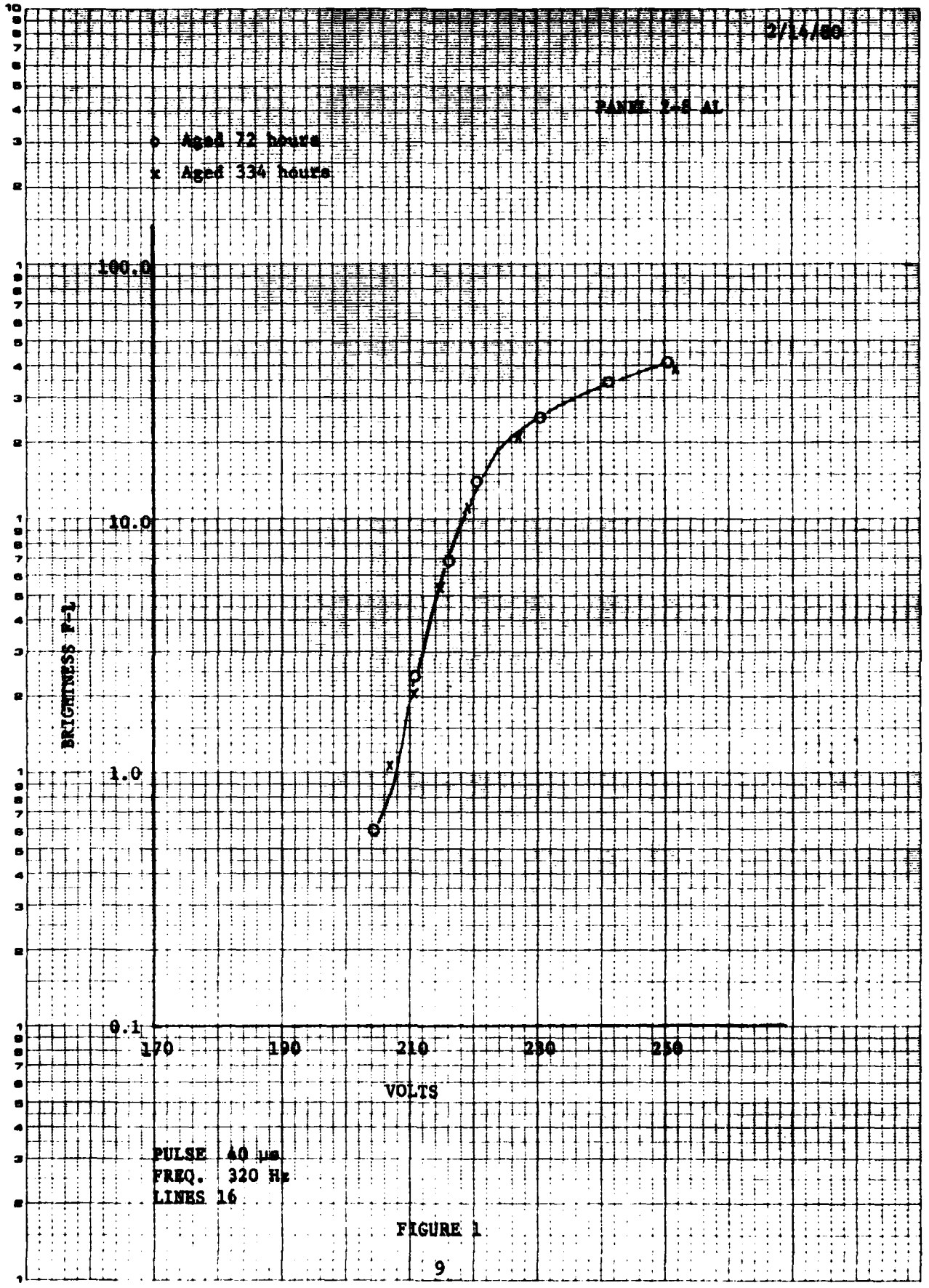
EDM I (Sept. 30, 1980)

This system is a breadboard version of the final system. The monolithic drivers are in standard dip packages and in sockets on wire-wrapped boards. There are eighteen 64-conductor wide, ribbon cables leading to the connector field at the panel. This system does not have the frame rate accelerating memory so that video is displayed in a reduced performance mode. The circuitry part of this system contains power supplies, drivers, pattern-generating exerciser and a video interface.

EDM II (May 31, 1981)

This device is the final version of the TVD display system. The monolithic drivers will have been repackaged into a more space-conserving package and, along with the memories, they will have been integrated onto a printed circuit card located behind the TFEL panel.

The circuitry, such as power supplies, exerciser and video interface not integrated with the panel, is in a second assembly connected by a less than 25 conductor cable. This system will display the video input data at a full performance level. An external computer interface will also be provided in the form of a word parallel digital version of the video interface.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x Aged 334 hours
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0.1
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190
210
230
250
VOLTS
PULSE 40 µs
FREQ. 320 Hz
LINES 16
DIETZGEN CORPORATION
MADE IN U.S.A.
NO. 340 -LS10 DIETZGEN GRAPH PAPER
SEMI-LOGARITHMIC
5 CYCLES X 10 DIVISIONS PER INCH

FIGURE 1

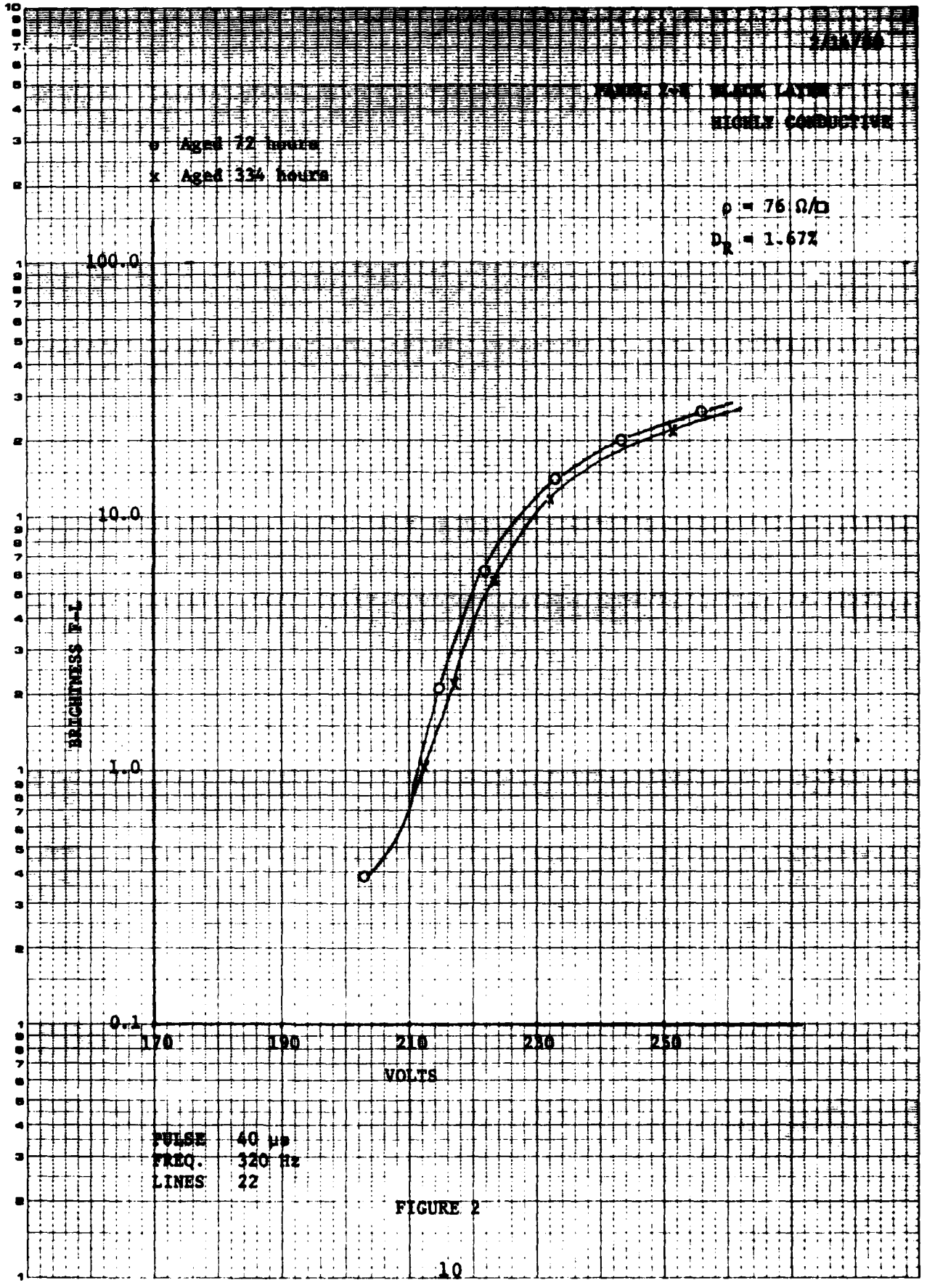


FIGURE 2

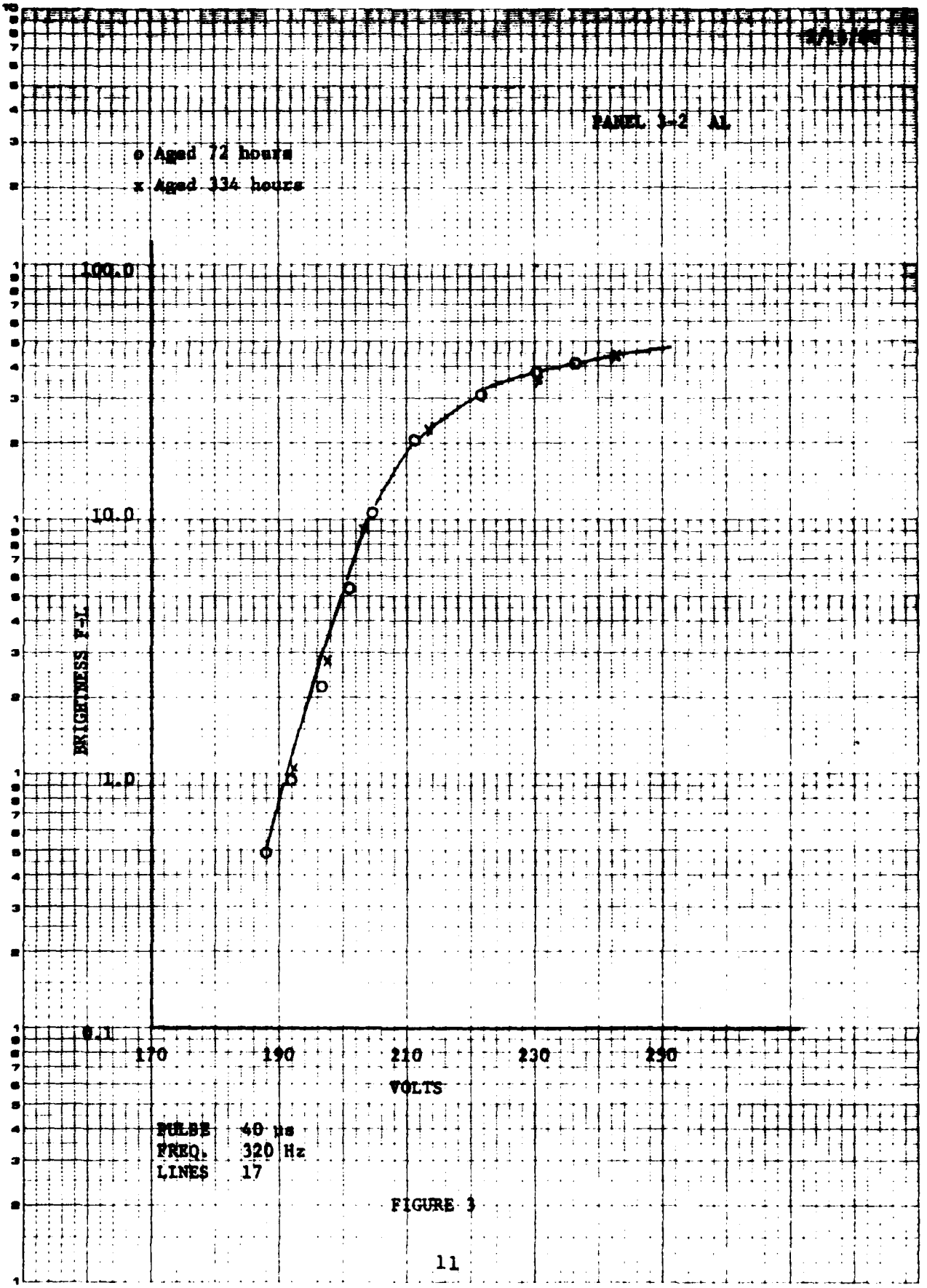
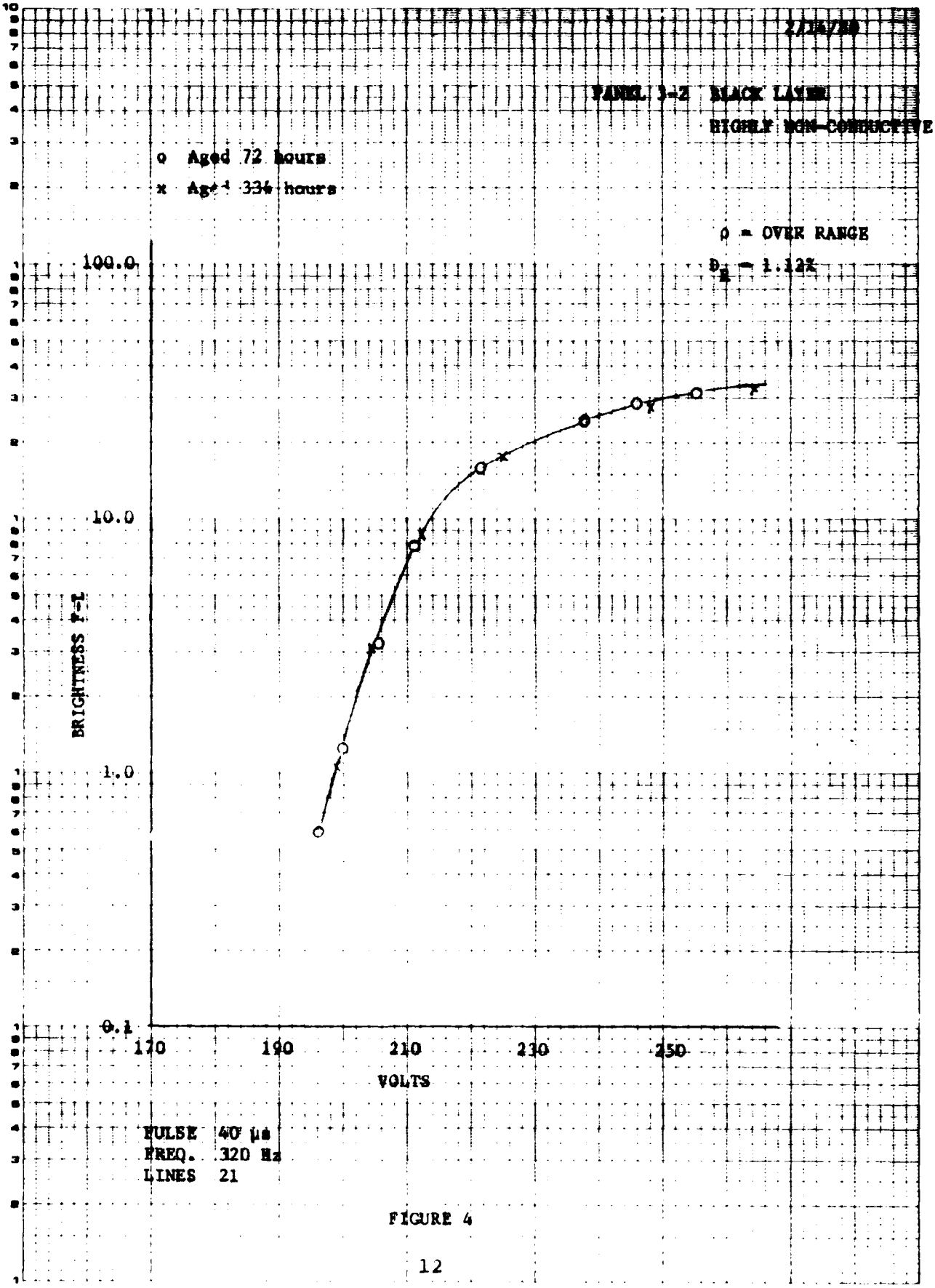


FIGURE 3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x Aged 336 hours
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D_E = 1.12%
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10.0
1.0
0.1
BRIGHTNESS F-L
170
190
210
230
250
VOLTS
PULSE 40 µs
FREQ. 320 Hz
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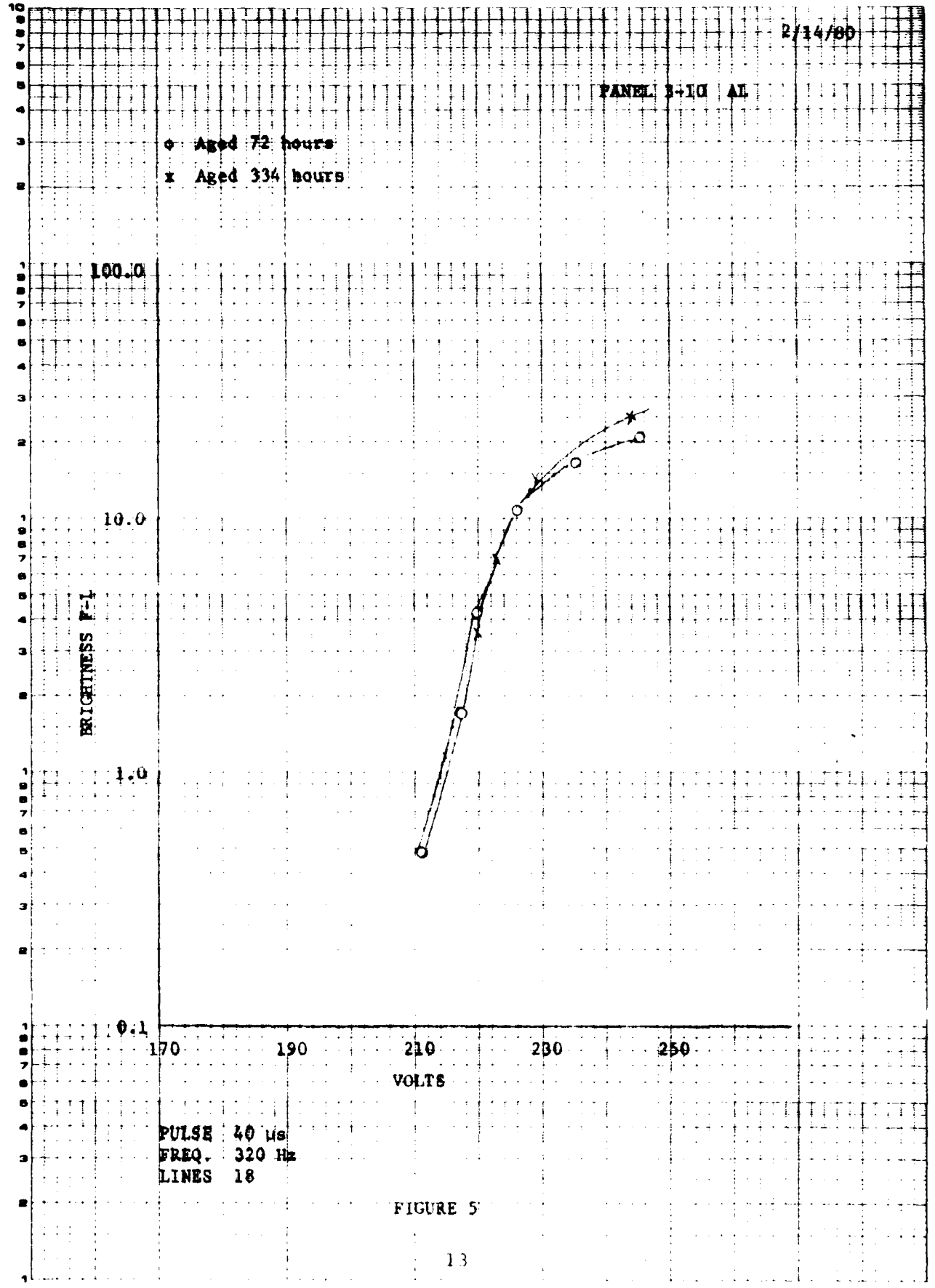
DIETZGEN CORPORATION
NO. 340R-LS10 DIETZGEN GRAPH PAPER
SEMI-LOGARITHMIC
5 CYCLES X 10 DIVISIONS PER INCH

FIGURE 4


2/14/80
PANEL 3-10 AL
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x Aged 334 hours
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0.1
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230
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VOLTS
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FREQ. 320 Hz
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DIETZGEN CORPORATION
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SEMI-LOGARITHMIC
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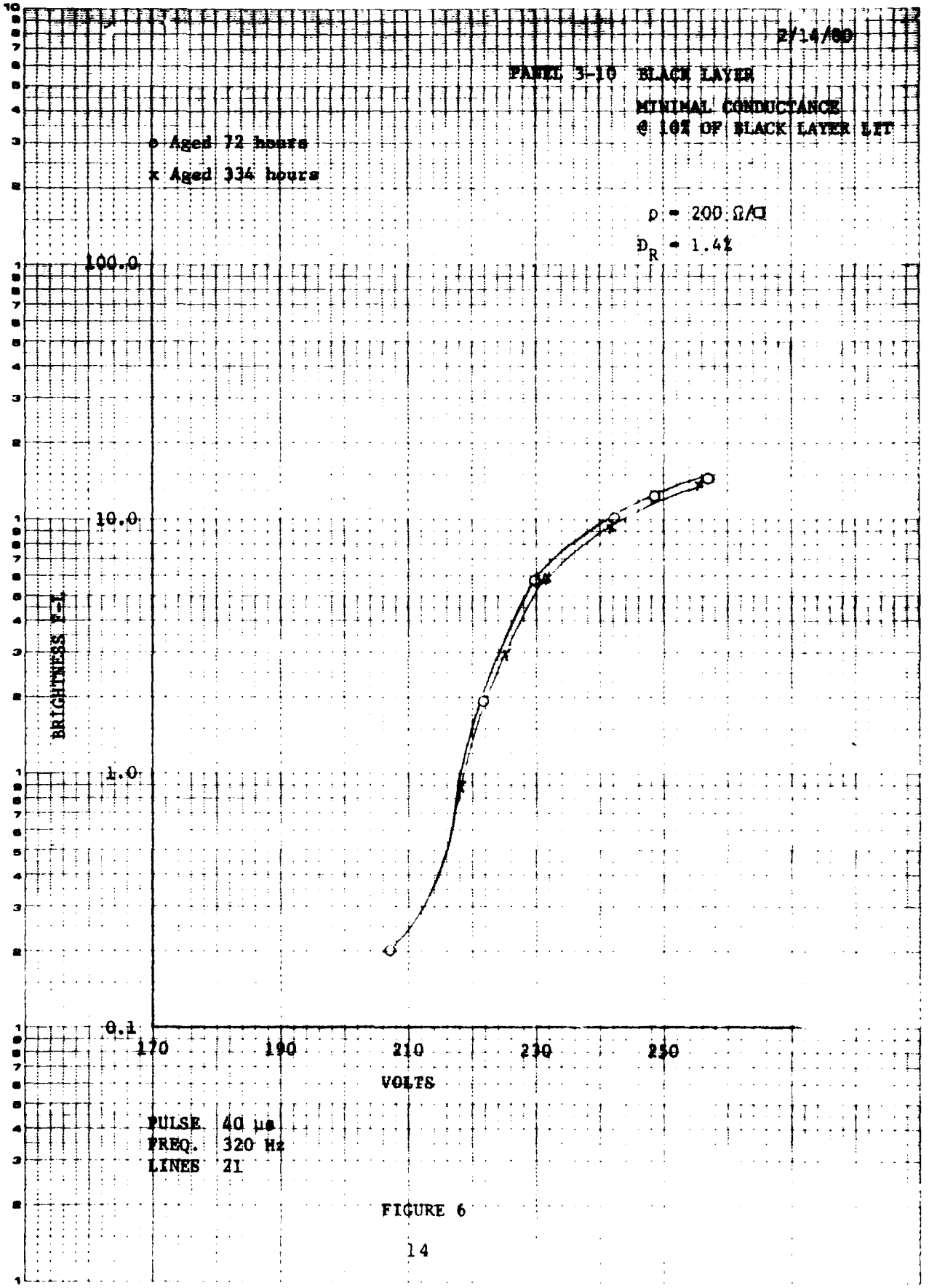
FIGURE 5



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NO. 340R-L510 DIETZGEN GRAPH PAPER
SEMI-LOGARITHMIC
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FIGURE 6

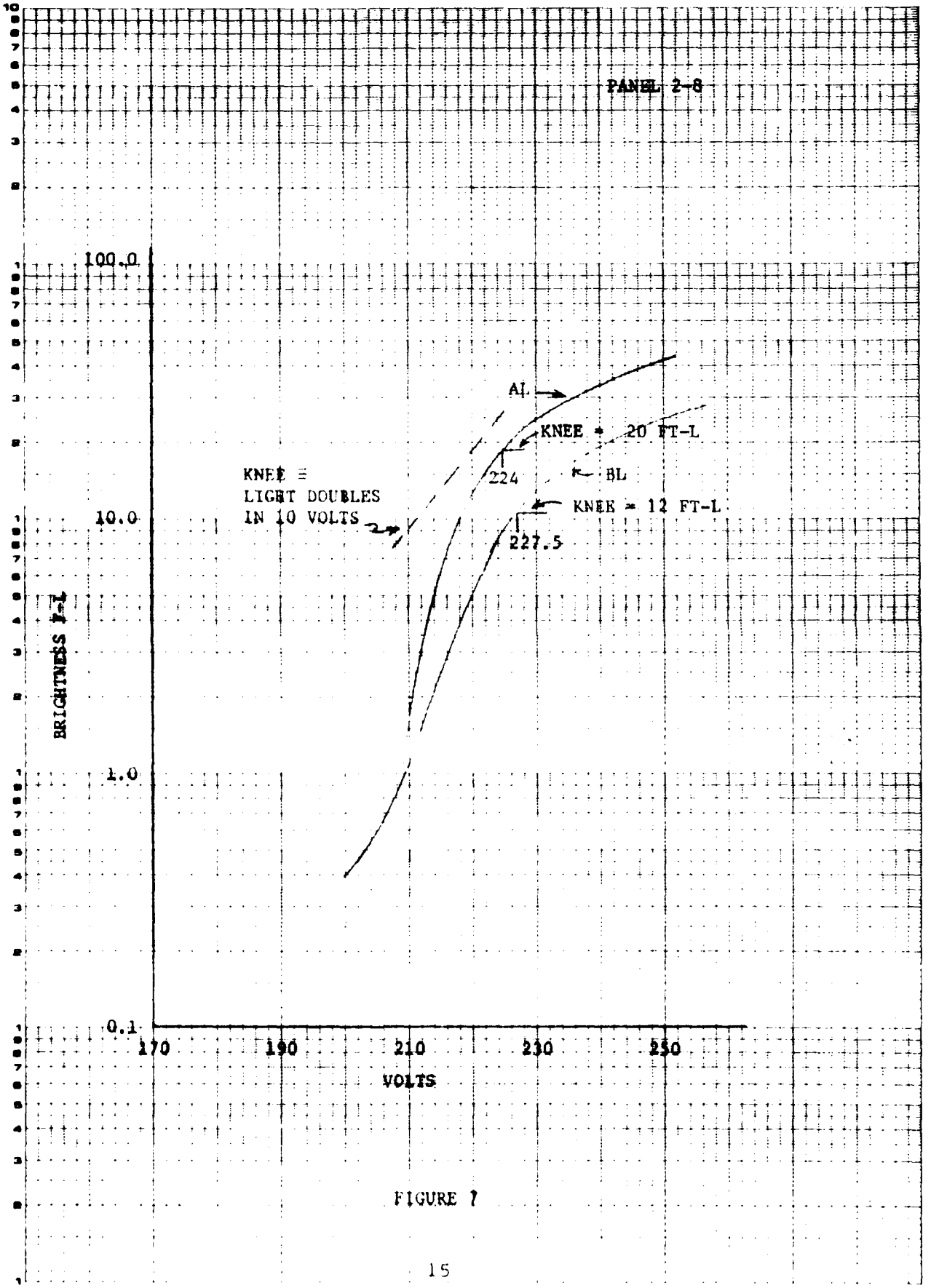
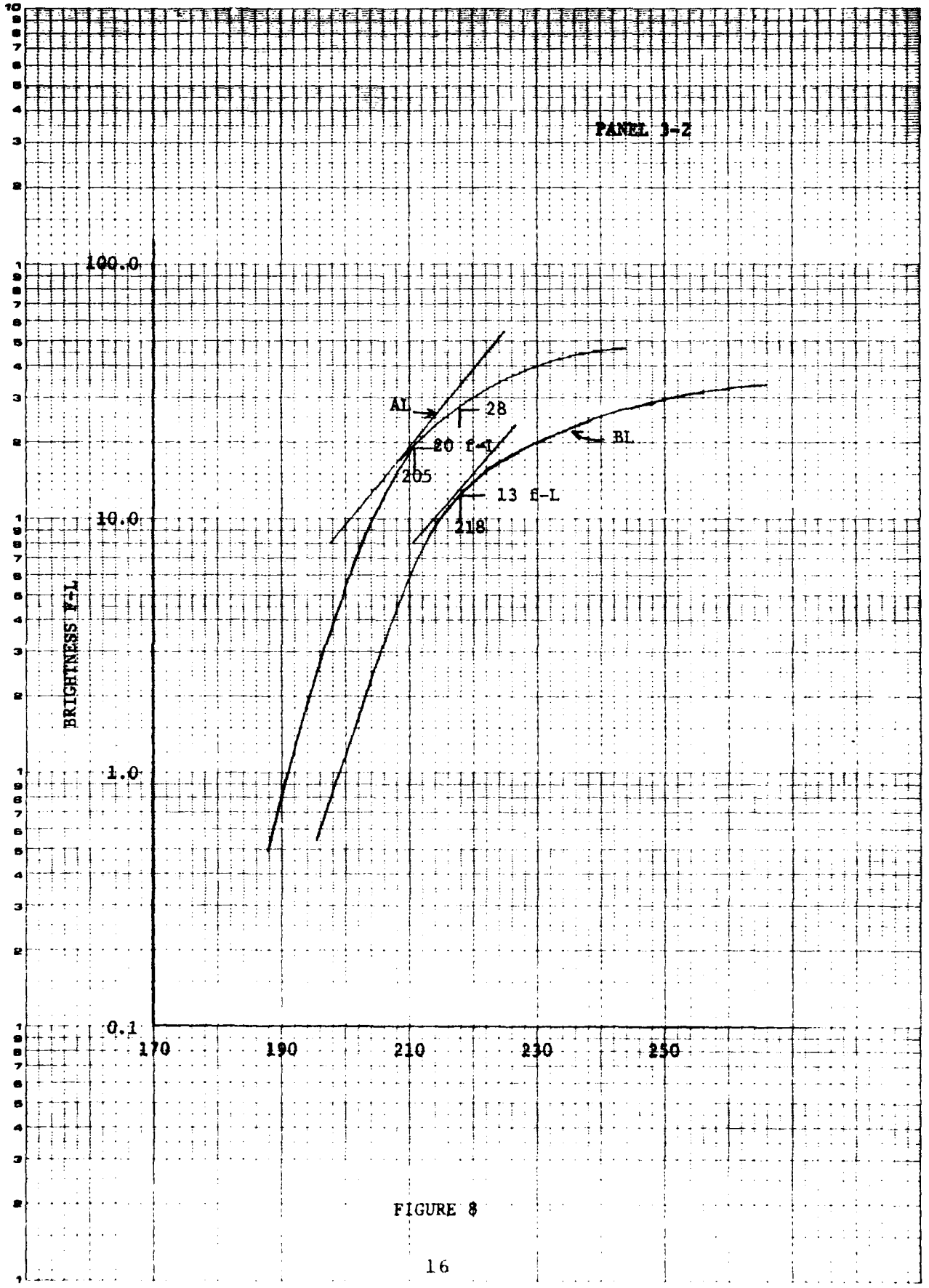


FIGURE 7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BRIGHTNESS f-L
AL
BL
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20 f-L
205
13 f-L
218
170
190
210
230
250
DIETZGEN CORPORATION
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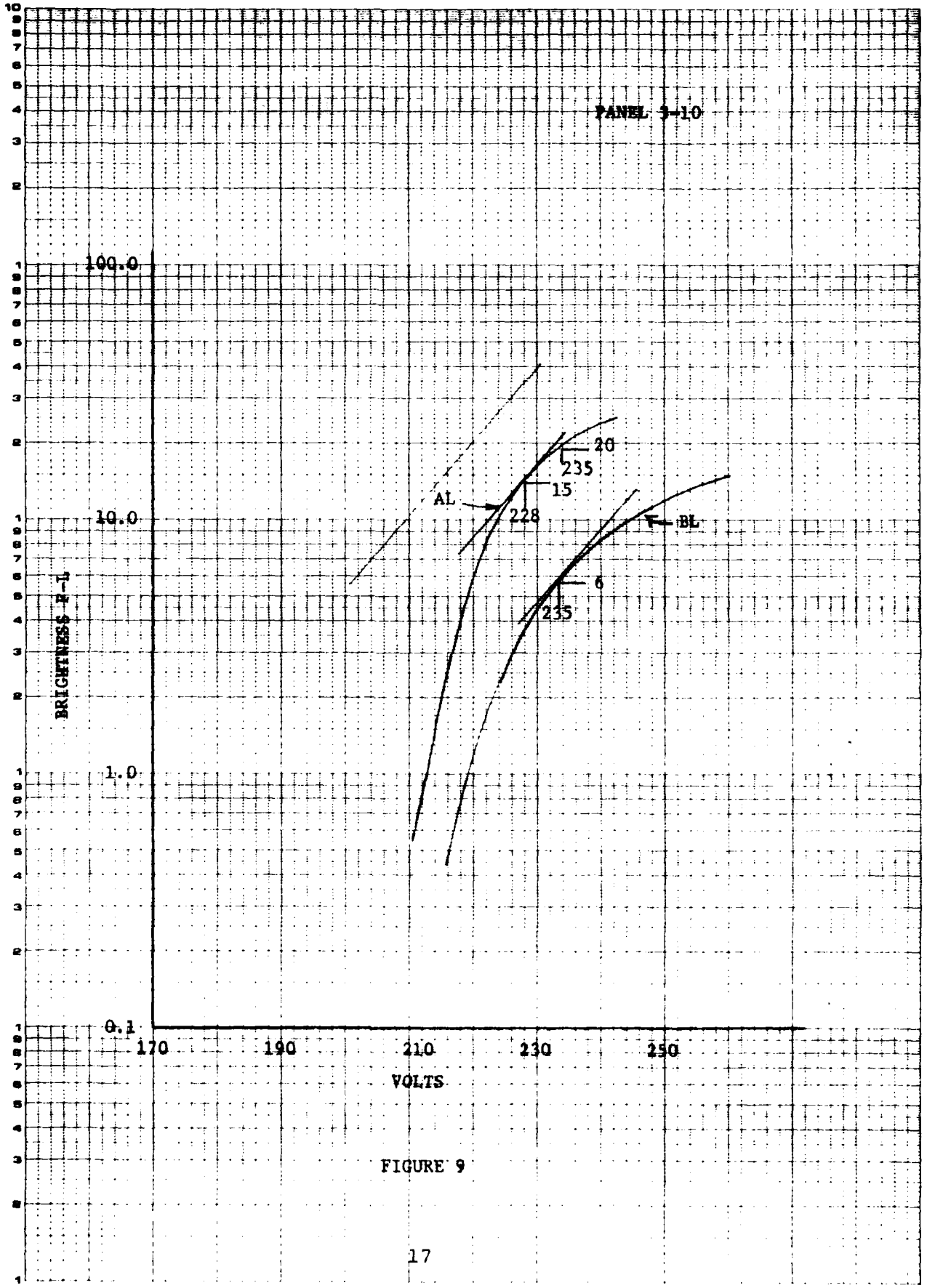
FIGURE 8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100.0
10.0
1.0
0.1
BRIGHTNESS FT-L
AL
BL
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15
228
6
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170
190
210
230
250
VOLTS
DIETZGEN CORPORATION
MADE IN U.S.A.
NO. 340R-L51D DIETZGEN GRAPH PAPER
SEMI-LOGARITHMIC
5 CYCLES X 10 DIVISIONS PER INCH

FIGURE 9

ATTACHMENT "A"

TFEL - COLUMN DRIVER

LTR	DESCRIPTION	DATE	APP.
		2/13/80	
Ø	COMPLETELY REVISED	2/22/80	
A	DELETE RIGHT/LEFT MODE	3/25/80	
B	REDUCE CLOCK FREQUENCY AND DRIVE CURRENT	4/29/80	
C	REPLACE PINOUT DIAGRAM AND NUMBERS ON OUTPUTS	7/9/80	

REV.																							
SHEETS	19	20																					
REV. STATUS OF SHEETS	REV.	A	A	B	A	B	0	A	0	A	C	0	C										
	SHEETS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18				

ORIGINATOR T. A. GIELOW

CHECK

APP.

APP.

APP.

APP.

HYCOM
16841 Armstrong Avenue
Irvine, CA 92705

SPECIFICATION

TFEL - COLUMN DRIVER

	SIZE	DWG.NO.
	A	
		SHEET OF

THE COLUMN DRIVER

The column driver has both a logic section and a high voltage output section. These sections will be described separately in conjunction with the drawings in Figures 1 and 2. The joint functioning of these sections will be explained in conjunction with the timing diagram in Figure 3.

The Logic Section

The column driver logic section contains 128 static D-type flip-flops. These flip-flops are partitioned into two blocks of 64. The first block is a 4-wide 16-long shift register and the second block is 16 independent 16-state counters. The counters are of a polynomial type using 4 flip-flops each. The shift register block and the counter block have separate clocks. Each of the 64 flip-flops in the counter section has a 2-input multiplexer in front of it to enable it to load or count data. The mode control line can be changed when the clock is low without disturbing the stored data. The diagram in Figure 1 shows the gates and flip-flops to perform these functions. In the shift register section, data on the 4 inputs is shifted in parallel along the 16 ranks of flip-flops and out the 4 outputs.

In the counter section the exclusive OR will cause the data to count in a polynomial fashion until the end count is reached. See Table 1. The lower shade numbers will reach the end count sooner. During the time the counter is not in the end condition,

a high level is provided to the output section. The counter counts down through the shade numbers so that after one clock a shade "15" has turned into a shade "14," etc. When shade "0" is reached, the counting stops and the output goes low.

Driver Section

The column driver also contains 16 column driver output circuits, each of which is made from 4 transistors plus a capacitor. The details of the circuit are shown in Figure 2. Each output circuit has an input from a counter in the logic section. The output circuits have a control input shown on the diagram as V_R. This input to the driver circuit is common to all 16 outputs and originates outside the column driver IC. This signal is analog in nature and appears as a slowly increasing voltage from zero to 60 volts. During the time this voltage is increasing the counters are also counting and their outputs are high. Until a given counter reaches its end state the capacitor charges to the full applied ramp input voltage. During the time that the counters are counting and the ramp is ramping the output voltage follows the charge on the capacitor. After the counting sequence has ended the ramp supply holds at its highest level until the drive sequence is finished and then it returns to zero volts. All of the charge in the storage capacitors is conducted away by the substrate diode of the transistor in the charging path.

Power Supplies

The column driver IC uses 2 power supplies. The first is for the shift register/counters and is fixed by the process at a voltage to be determined between +5 and +10 volts. The second supply is the output driver supply called V_M; this voltage will be adjustable from +20 to +60 as needed to control the overall system performance. The ramp voltage input is not primarily viewed as a power supply but it will have a voltage range of zero to the value of V_M. This voltage will rise from zero to V_M for each output cycle. The rate of rise will be between 5 and 15 volts per microsecond. When the ramp voltage is returning to zero the rate would be about 20 volts per microsecond.

Clock Rates

The column driver IC has 2 clock inputs which clock the static "D" flip-flops. These clocks operate the shift register and counter sections. There is no minimum frequency and the maximum shall be greater than 2 MHz. Edge triggering for the shift register section on the return to low is preferred with minimal set-up and post time but a DC clock with stable data requirement is acceptable.

If a DC clock is used it is preferable to have a pulse width of less than 50 ns to avoid having to provide data storage registers between these inputs and the data source (dynamic RAM). The clock requirement to the counter should be similar

to the clock of the shift registers but, in this case, there are no off-chip data requirements to meet. The 4 data outputs of the shift registers are expected to be static buffered versions of the 4 flip-flops in the last rank.

Input Levels and Loading

The load/count control and the data inputs should be compatible with TTL and represent less than one standard load. If this is not possible then open collector TTL and pull-up resistors to logic power supply will be used.

The clock inputs may require fast edges and the full power supply swing; if so, TTL to MOS clock drivers will be used.

Output Levels and Loading

The data outputs will only be required to drive the data inputs of the next column driver IC. The column driver outputs will need to source and sink the surge currents created by their output voltage, the TFEL panel's capacitance and the cross coupling effects of all the other column drivers in the display system.

The "N" and "P" channel output transistors should have their respective thresholds set so that their absolute sum is less than 3 volts. The function of the output circuit is to source or sink current as necessary to bring the voltage on the output line within the threshold limits as quickly as possible.

All transistors in the output circuitry will be exposed to up to 60 volts and the 2 output transistors will be exposed to heavy surge currents. The substrate diode of the charging transistor will need to conduct the discharge current in the storage capacitor when the ramp voltage input returns to zero ($2x10^7$ volts/sec).

The surge current that a column driver output may experience is dependent on many system parameters. Each panel, depending on its geometries, presents a different load to its drivers. Most of the foreseeable future panels will be of a high resolution type where the panels own resistance will limit the surge currents. For the purpose of this paper the load will be defined as a 600 ohm resistor in series with a 1000 picofarad capacitor. If this load were driven from a source impedance of 600 ohm, then the maximum current for a 60 volt swing would be 20 milliamps. Working backwards, we find that this 20 ma is only needed for the 60 volt swing which is accompanied by a 60 volt gate to source voltage, so a transconductance of 0.001 would appear to be adequate.

New Specification Data

Current limit not less than 12 ma;

On state resistance not greater than 600Ω;

Transconductance greater than 0.001 MHO.

Timing

This generation of the column driver has a wide range of applications and leaves the display system designer with great freedom to define his own timing. Therefore, the timing described here is for ease of understanding and may not represent any particular application. Figure 3 shows an example of the circuits operation in an overlapping mode. The time base of this example is 3 MHz and a "line time" is defined as 60 clocks. The "line time" (20μs) is the basis of both the input and output cycling. The smallest grouping of column drivers presently foreseen is two, so the example is based on 32 shift register clocks. In a test situation only 16 clocks would really be needed and they could be continuous rather than in bursts as imposed by our external refresh memory. As can be seen in the timing diagram, the output follows the ramp input for the interval between the time the new data is clocked in (load mode) and the time the counter reached the limit state. If the new data is the limit state, then no charging pulse is produced.

The charging transistor driven by the logic translation transistor must come on hard enough to conduct currents higher than those defined by the maximum speed of the rising ramp and the capacitor on the output structure gate node. The maximum rate of rise would be 1.5×10^7 volts/sec. (15 volts/microsecond). The capacitance at the gates of the output transistors should be large enough to hold the voltage defined by the charging circuit for 25 microseconds minimum independent of the surge currents or voltage on the output. The allowable rate of leakage can be expressed in terms of

the stored voltage since we are less sensitive at higher voltages. Five percent loss in 25μs seems to be conservative from the display point of view. The reverse transfer capacitance of the output transistors could represent a significant problem. The worst case is where a given output is trying to hold near zero volts and a high rate of voltage rise is coupled on to the drivers output. The voltage rise on the output could be as fast as the ramp supply. The P-CH current sinking transistor will turn on and remove the voltage from the output. The requirement is that the charge on the storage capacitor not rise by more than 0.75 volts. Fixed voltage offsets created by transistor thresholds are not as significant as error voltage offsets caused by cross coupling between columns.

The fact that this new design allows the output to track the ramp voltage (additive modulation mode without transfer gate) enables us to reduce the maximum surge current requirements to 20 milliamps from the previously required 50 and 100 ma level.

The preferred packaging is shown in Figure 4. These drawings are based on a package such as Kyocera type CA03601. This package is a 36-lead 400 mil square package. This package was tentatively chosen from a very limited selection presently known to us. The main selection criterion was overall outside size. The mapping of the functions onto the pins has been chosen to minimize circuit board area.

TABLE 1

SHADE NUMBER, DATA AND OUTPUT

Shade No.	Data Loaded	Pulse Width	Output Voltage	Light Output
15	1 0 0 1	Long	Near +60	Maximum
14	1 1 0 1			
13	1 1 1 1			
12	1 1 1 0			
11	0 1 1 1			
10	1 0 1 0			
9	0 1 0 1			
8	1 0 1 1			
7	1 1 0 0			
6	0 1 1 0			
5	0 0 1 1			
4	1 0 0 0			
3	0 1 0 0			
2	0 0 1 0			
1	0 0 0 1	Short		
0	0 0 0 0	No pulse	Near zero	Minimum

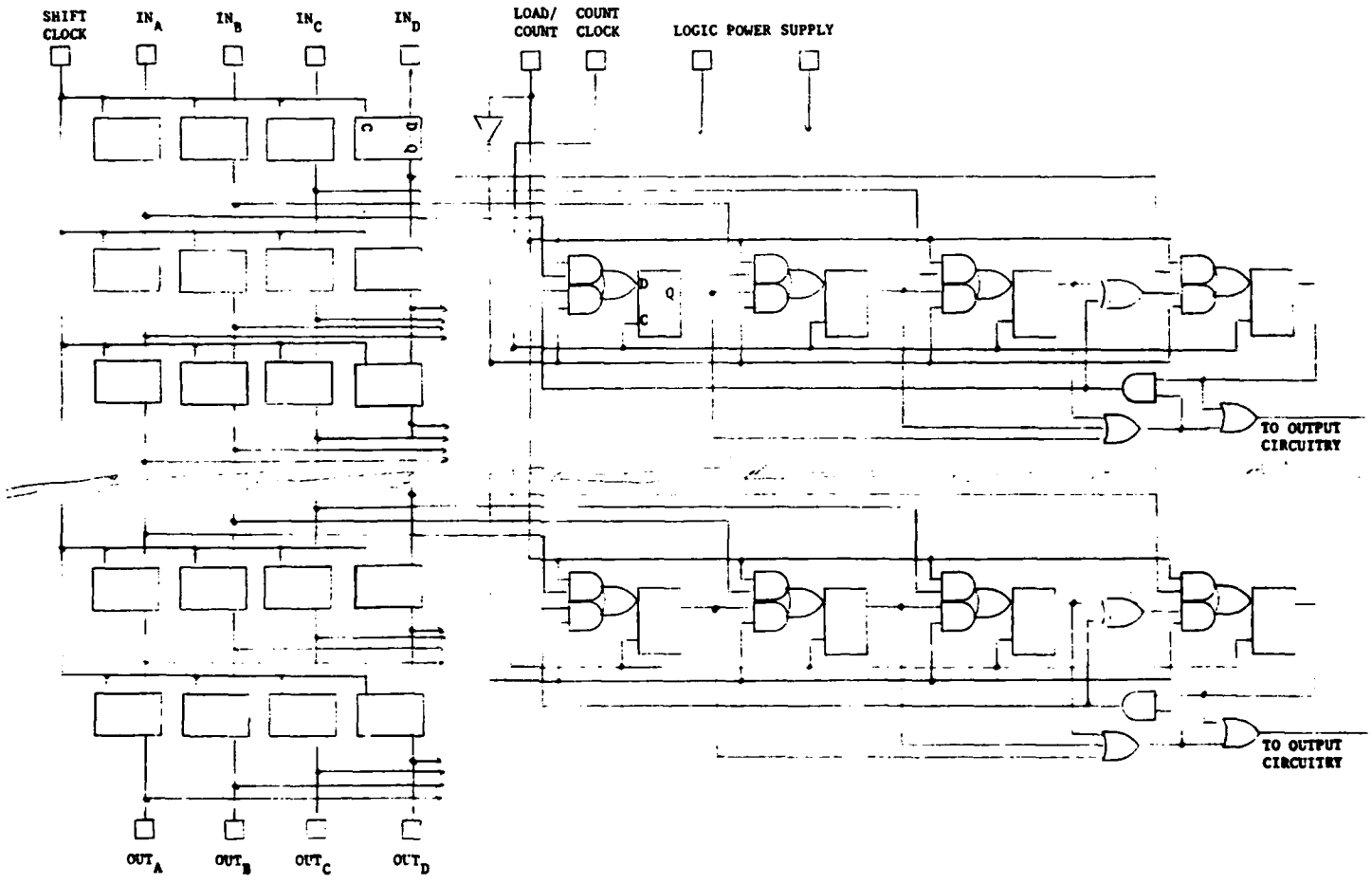

FIGURE 1. DETAILS OF LOGIC ELEMENTS

(Shown are 5 of 16 ranks of shift register and 2 of the 16 counters)

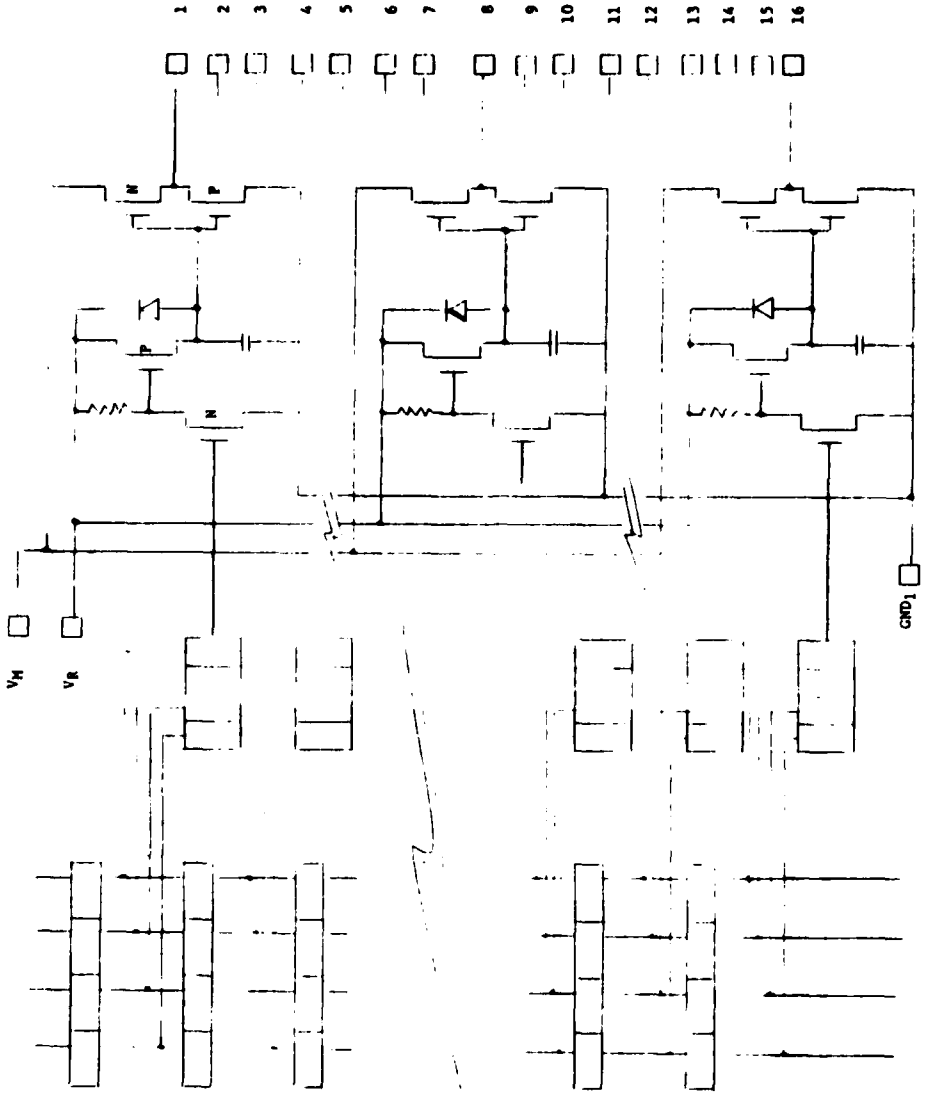

FIGURE 2. DETAILS OF OUTPUT CIRCUITS
(Shown are 3 of the 16 outputs)

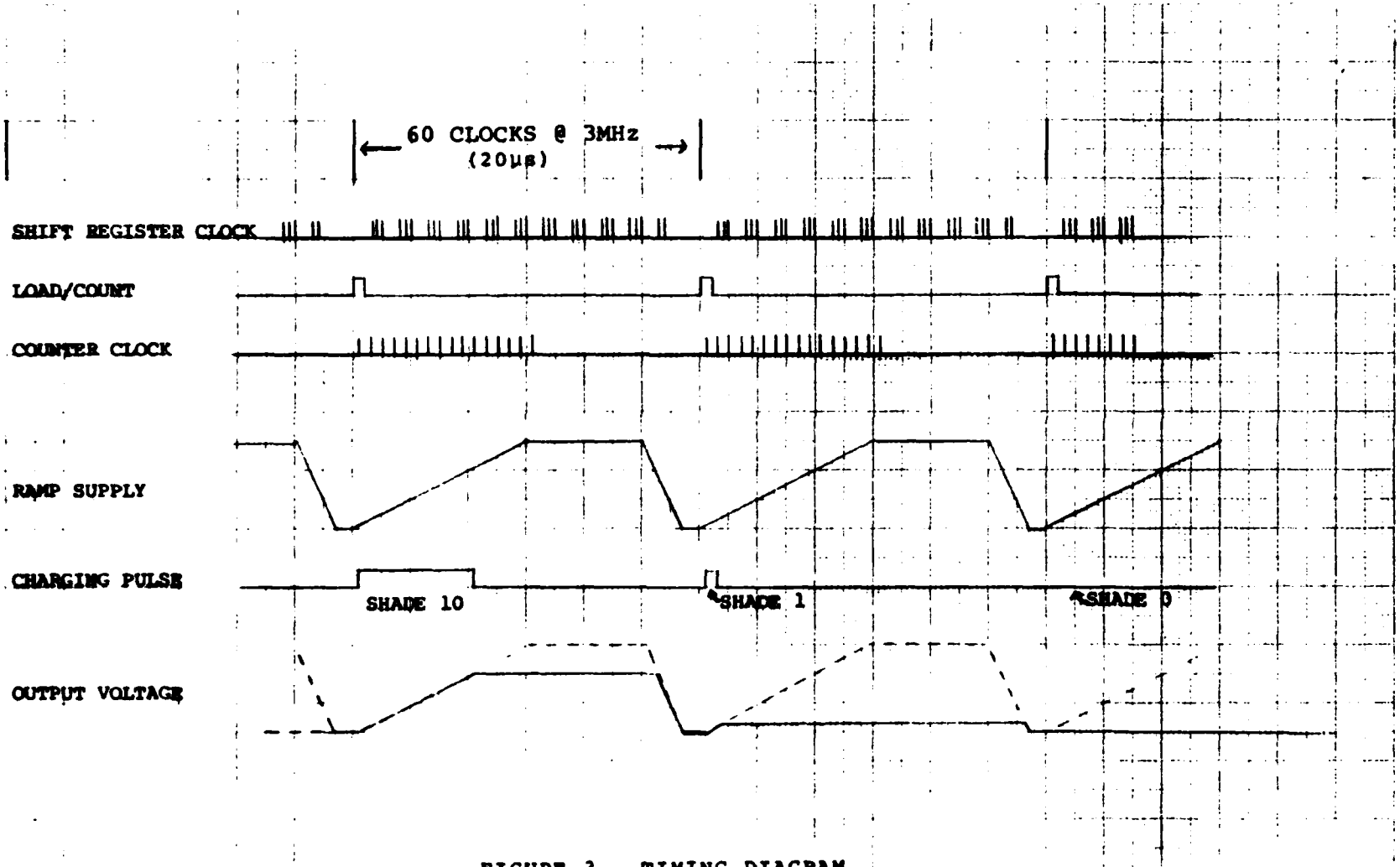

FIGURE 3. TIMING DIAGRAM

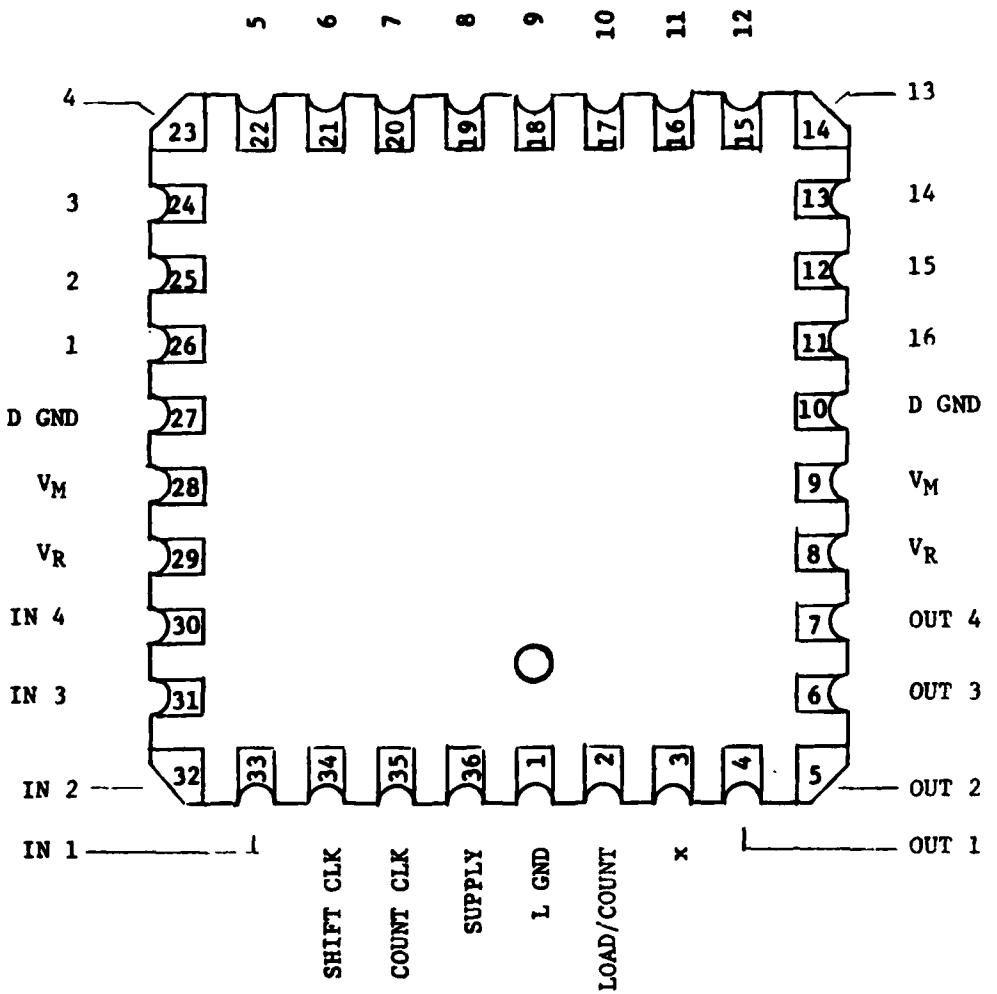

FIGURE 4. TOP VIEW OF COLUMN DRIVER (ABOUT 10X)

ATTACHMENT "B"

TFEL - ROW DRIVER

REVISIONS

LTR	DESCRIPTION	DATE	APP.
		2/13/80	
A	REVISED	3/5/80	
B	DELETE RIGHT/LEFT MODE, ADD SET/RESET MODE	3/25/80	
C	INCREASE ON STATE RESISTANCE	3/28/80	
D	REPLACE PINOUT DIAGRAM; ADD NUMBERS ON OUTPUTS	7/9/80	
E	INCREASE MINIMAL PULSE WIDTH	7/28/80	

REV.																								
SHEETS	19	20																						

REV. STATUS OF SHEETS																				
REV.	B	E	C	B	D	A	A	D												
SHEETS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		

ORIGINATOR T. GIELOW

CHECK

APP.

APP.

APP.

APP.

HYCOM
16841 Armstrong Avenue
Irvine, CA 92705

SPECIFICATION

TFEL - ROW DRIVER

SIZE A | DWG.NO.

SHEET OF

THE ROW DRIVER

The row driver contains 16 static "D-type" flip-flops. These flip-flops form a single 16-stage shift register which normally contains a maximum of one logic high state. This single logic high is clocked along the register to control which of the row driver outputs is to be driven during the scan pulse. All of the logic runs off a logic level power supply which is held fixed relative to the substrate. The output transistors are exposed to high voltages relative to the substrate and experience high surge currents on several occasions during each frame time. The substrate diodes associated with the drains of the output transistors are also used to deliver current to the display panel. Figure 1 shows the diagram of this device.

OPERATION AND SYSTEM UTILIZATION

The row driver IC is used to apply the scan and refresh voltages to a TFEL panel to enable it to display images when used in conjunction with the column driver IC described separately. The voltages to be supplied are both +200 and -200 volts, and after their application they must be removed by a voltage sinking step. The diagram in Figure 2 shows the IC in a system environment. The six power MOS FETS shown in the drawing control the application of voltages to the IC's substrate. Figure 3 shows the control signals and the output wave shape produced.

The drawings of Figures 1 and 2 show a change from previous drawings and discussions of this circuit in that the substrate diodes associated with the outputs will be utilized rather than including an additional diode wired to an up-bus.

LOGIC CIRCUIT DETAILS

The logic on this IC consists of 16 stages of "D-type" flip-flops plus the output control gates as shown in Figure 1. This logic is implemented in N-channel and uses a single +10 volt supply. A master clear has been provided to initialize the shift register each frame time. The normal operation calls for a single logic "high" to be clocked along the register with the enable being pulsed each time to create the SCAN function. This device may also be used in a selected scan mode by omitting the enable pulse and clocking the register faster to skip past non-selected rows. The ALL ON input turns on all the outputs and is used for the REFRESH SYNC function. See Figure 3 for control and output wave shape. The three functions, SCAN SYNC, REFRESH and REFRESH SYNC, are done in unison to all row driver outputs; all logic inputs and the one logic output are TTL compatible. The clocking function shall operate from zero to 200 KHz; clock pulse width is to be 0.25 microseconds minimum. The normal pulse width on the ENABLE is 8 to 20 microseconds and the ALL ON pulse width is 15 to 60 microseconds.

The first flip-flop in the serial shift register has the added feature of a mode control input which allows this stage to interpret the "RESET" command as a "SET" command if the input is "HIGH." This feature is useful in the normal scanning function to place a single "ONE" in the shift register. When a group of these row drivers is interconnected to form a long shift register only the first one in the string would have this mode control line set "HIGH." In the case just mentioned, the data input of the "first" device would be grounded and the placement of the "one" would be automatic.

OUTPUT CIRCUITRY DETAILS

The output transistors must sync currents of up to 250 ma and have a minimum breakdown voltage of 250 volts. The substrate diodes on the outputs should handle surge currents of up to 250 ma when only output capacitance is to be charged and 50 ma each when all 16 outputs are conducting in unison. The ON state resistance of the transistor should be less than 40 ohm.

The gnd/substrate pin must handle up to 1.6 amps.

SYSTEM OPERATION

Figure 2 shows the system environment of the row driver device. The six power MOS FETS are labeled A, B, C, D, E and F. These labels will be used in conjunction with the ALL ON and ENABLE to explain the wave shapes shown in Figure 3. To scan, one row of the panel is pulled to -200 volts. This is accomplished

by using the ENABLE and transistors "A" and "D". To SCAN SYNC, transistor "E" is turned on. The SCAN and SCAN SYNC is repeated for each row of the panel as determined by the position of the logic "high" in the shift register. To REFRESH, transistors B and C are turned on. To REFRESH SYNC, transistor F and the ALL ON input are used.

PACKAGING

The present preferred package, chosen from a limited known selection, is Kyocera type CA-03601 and the preferred pin-out is given in Figure 4.

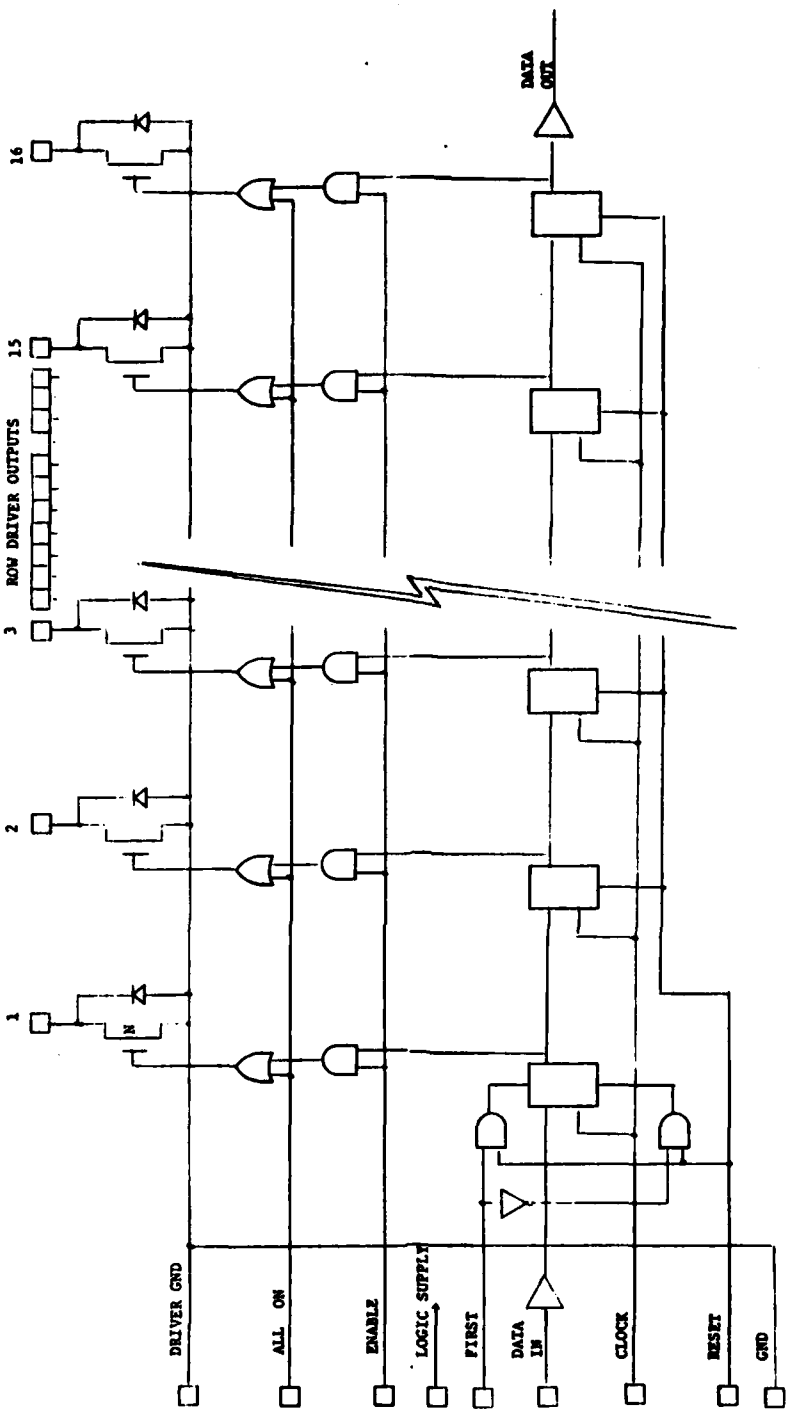

FIGURE 1. ROW DRIVER CIRCUITRY

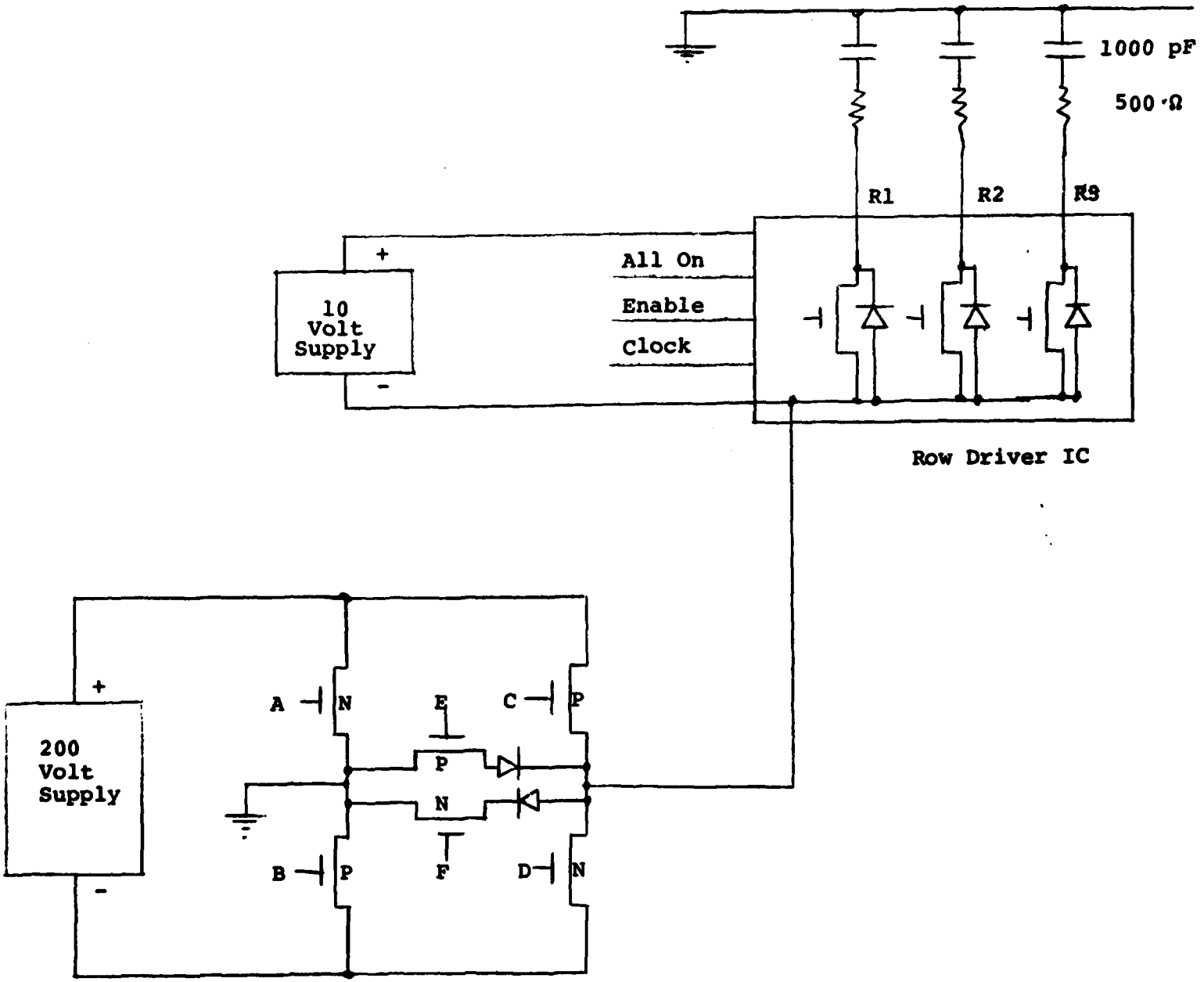

Figure 2 System Environment

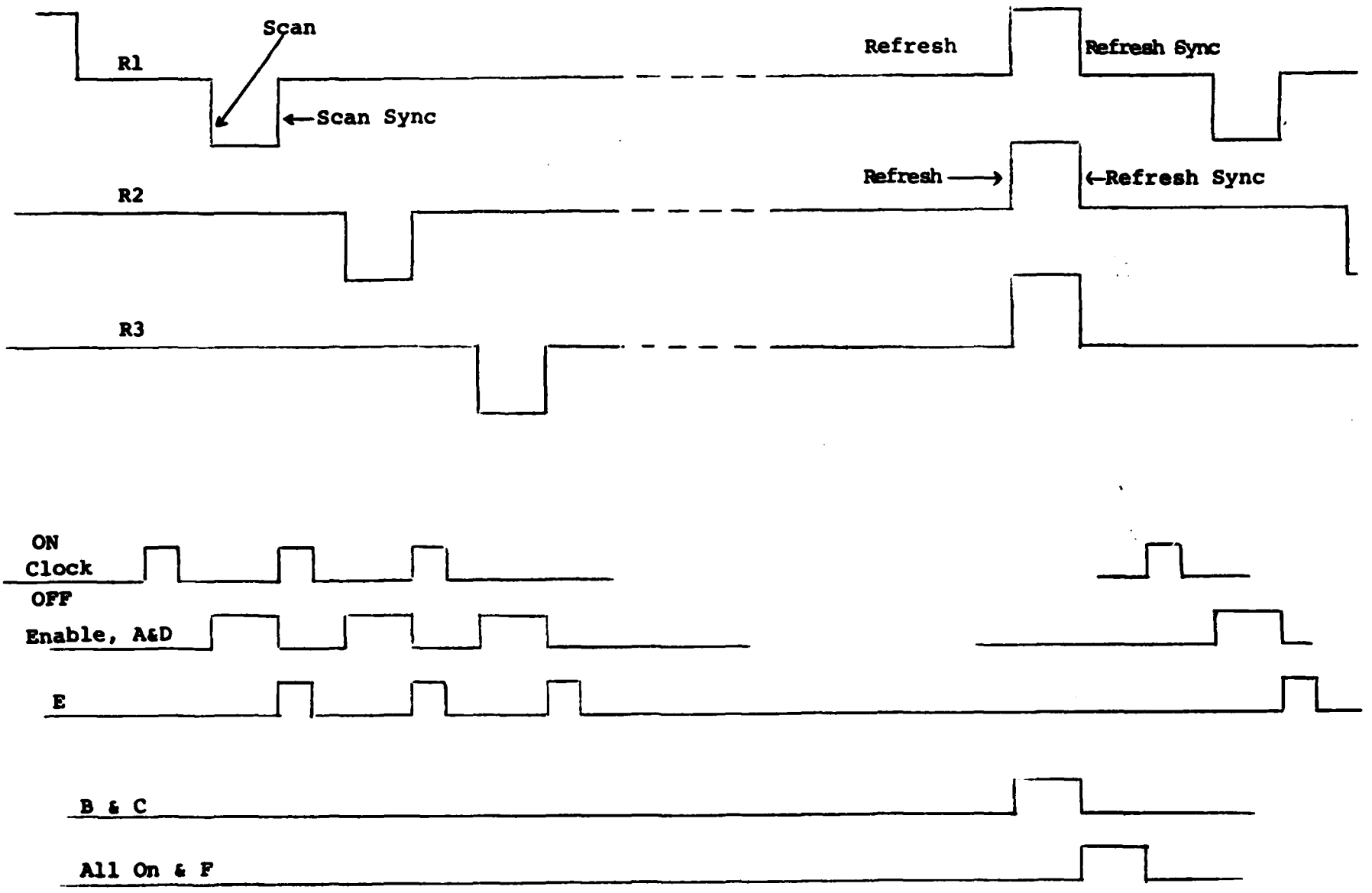

Figure 3 Output Waveform and Control Signal States

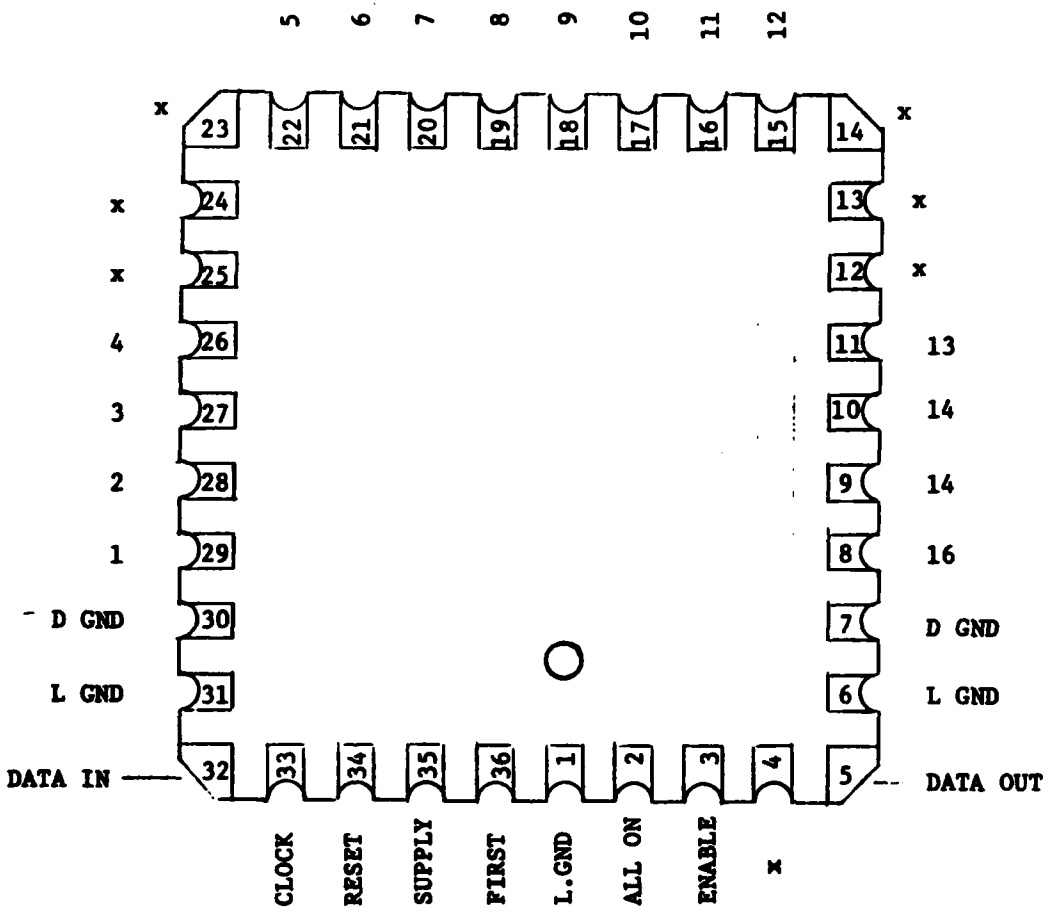

FIGURE 4. TOP VIEW OF ROW DRIVER (ABOUT 10X)

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