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DHRS TECHNICAL REPORT.(U)
JUL 80 G WYCOFF, W BAKER, J SEKIGUCHI, G HAAS F30602-79-C-0269
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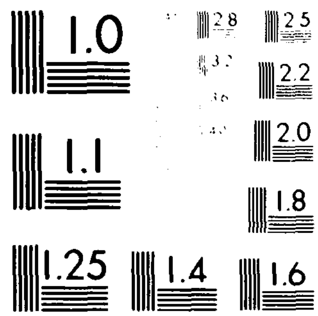

MICROCOPY RESOLUTION TEST CHART

LEVEL II

(12)

RADC-TR-80-200
Final Technical Report
July 1980

DHRS TECHNICAL REPORT

Northrop Corporation

Gary Wycoff
William Baker

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ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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APPROVED:

ANDREW R. PIRICH
Project Engineer

APPROVED:

OWEN R. LAWTER, Colonel, USAF
Chief, Intelligence & Reconnaissance Division

FOR THE COMMANDER:

JOHN P. HUSS
Acting Chief, Plans Office

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REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER	RADC-TR-80-200
2. GOVT ACCESSION NO.	AD-A089953
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle)	DHRS TECHNICAL REPORT
5. TYPE OF REPORT & PERIOD COVERED	Final Technical Report, 1 Oct 79 — 31 Mar 80
6. PERFORMING ORG. REPORT NUMBER	N/A
7. AUTHOR(s)	Gary Wycoff William Baker
8. CONTRACT OR GRANT NUMBER(s)	F30602-79-C-0269
9. PERFORMING ORGANIZATION NAME AND ADDRESS	Northrop Corporation/Image Systems Branch Electronic Division, 2301 West 120th Street Hawthorne CA 90250
10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS	63208F 665A0004
11. CONTROLLING OFFICE NAME AND ADDRESS	Rome Air Development Center (IRRE) Griffiss AFB NY 13441
12. REPORT DATE	Jul[redacted]80
13. NUMBER OF PAGES	41
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	Same
15. SECURITY CLASS. (of this report)	UNCLASSIFIED
15a. DECLASSIFICATION/DOWNGRADING SCHEDULE	N/A
16. DISTRIBUTION STATEMENT (of this Report)	Approved for public release; distribution unlimited.
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)	Same
18. SUPPLEMENTARY NOTES	RADC Project Engineer: Andrew R. Pirich (IRRE)
19. KEY WORDS (Continue on reverse side if necessary and identify by block number)	Real Time Processing Detection Identification Reporting Digital Imagery Enhancement

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The Final Technical Report submitted by Northrop Corporation contains a brief synopsis of the problems encountered during the design phase of the Data Handling Recording System (DHRS) program. An analysis is presented of the hardware design to handle 10^{11} bits of digital imagery data. One of the important results of the Northrop study was that a fundamental delay caused by the assumed target input rate (exceeding the exploitation output rate) cannot be improved upon except by employing additional

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exploitation stations or by assuring a longer exploitation time.

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EVALUATION

Northrop Corporation, addressed six technical topics that received special analysis during the Phase I study to establish the DHRS baseline configuration. These topics are:

1. Overall - System Design
2. Cache Storage
3. Mass Storage
4. Displays
5. Target Screeners
6. Compression/Expansion Techniques

The parameters which drove the preliminary architectural design of the DHRS were that (for the DHRS to operate without delays), the Image Interpreter must finish his exploitation/reporting tasks in less than 4.8 to 120 seconds. For worst case, as many as 6 exploitation stations would be required to process target data in real-time if each processing task took (on the average) only 30 seconds. Due to the high cost of multiple exploitation stations, Northrop decided on only one exploitation station, and thus the baseline architecture was designed.

ANDREW R. PIRICH
Project Engineer

ABSTRACT

The following document constitutes the final technical report on Contract F30602-79-C-0269, Data Handling/Recording System - Phase I. The work was performed in the Image Systems Branch of Northrop Corp., by Messrs Gary Wycoff, William Baker, J. Sekiguchi, and Dr. Gerry Haas.

CDRL A002

DHRS TECHNICAL REPORT

1.0 INTRODUCTION

The Data Handling and Recording System is a system of personnel, equipment, computer software and procedures capable of receiving and exploiting tactical reconnaissance information in near real time. The reconnaissance information is infrared imagery and location data from the AN/AAQ-9 forward-looking infrared (FLIR) and AN/AAD-5 downward-looking infrared (DLIR) multiplexed with AN/ARN-101 computer inertial navigation information. After demultiplexing, data is routed to the data processing and video and display consoles. Exploitation equipment is housed in a 20-by-8 by 8-foot shelter. The shelter contains computer and peripherals (magnetic tape units and disks) and conversion, and target/intelligence report writing. The shelter is modular, mobile, air transportable and capable of global deployment.

The DHRS technical report addresses six topics that received special analysis during the DHRS Phase I study to establish the baseline configuration submitted as CDRL A003, Technical Proposal/ Program Plan. These topics are discussed under the following subsections: Overall System, Cache Storage, Mass Storage, Displays, Target Screeners and Compression-Expansion.

2.0 OVERALL SYSTEM

2.1 Technical Problem

A significant difference exists between an operational future DHRS and the Advanced Development Model used to evaluate target screeners and to evaluate system response timeliness. Specifically, target input rates dramatically impact the size of the DHRS exploitation station, since Image Interpreter (II) exploitation time limits the DHRS throughput. It also affects the size of the cache memory (which functions as a buffer between the target input rate and the II exploitation rate). And finally, it determines a fundamental system parameter, throughput timeliness, and thus the requirements for real time and near real time target processing.

2.2 General Methodology

To bound the target input rates, two mission scenarios were developed (see Figure 1). The minimum is the surveillance mission. It is a low-altitude, wide-field-of-view updating of already located targets and consists of a 2 hour flight with 6 imaging segments each yielding one formation target and new targets in

MISSION SCENARIOS

- **SURVEILLANCE — UPDATE LOCATED TARGETS (DA)** — **MINI-MISSION**
  - LOW ALTITUDE
  - WIDE FOV
  - 2 HOUR YIELDING 6 IMAGE SEGMENTS EACH CONTAINING
    - 1 FORMATION TARGET
    - 3/4 NEW TARGETS

- **RECONNAISSANCE — FIND NEW TARGETS** — **MAXI-MISSION**
  - HIGH ALTITUDE
  - NARROW FOV
  - 30-MINUTE CONTINUOUS STRIP CONTAINING:
    - 3 FORMATION TARGETS
    - 30 INDIVIDUAL TARGETS
    - 60 NON-TARGETS

FIGURE 1

three out of four such segments. This mission is depicted in Figure 2. The maximum mission, called reconnaissance, is used to find new targets in an unsurveyed region. It consists of a high altitude flight with continuous sensor imaging and will collect images of 3 formation targets, thirty individual targets and 60 man made objects that are not targets. These figures are based on battlefield target densities described by General Stubblebein for the BETA program.

Within these bounds on target thougput rates, table 1 was constructed for both the AN/AAD-5 and the AN/AAQ-9 sensor in three scenarios; the present ADVISOR-62 data, during tests of the DHRS, and operationally as in a Reforger Exercise.

2.3 Technical Results

The critical parameters that impact the DHRS timelines and cache size are the average target frame rate and the average targets per target frame. For the DHRS to operate without delays, the II must finish his exploitation/reporting tasks in less than 4.8 to 120 seconds. Therefore, for worst case, as many as 6 exploitation stations would be required to process target data in real-time if each processing task took on the average of only 30 seconds. These parameters drove the preliminary architectural design of DHRS (see figure 3). It was obvious that the cost of multiple exploitation stations was prohibitive and unnecessary to the purpose of an Advanced Development Model (ADM). The project managers made a decision that only one exploitation station would be procured for the ADM and thus the baseline as shown in figure 4 was defined.

Before leaving this section, a time compression in the collected versus inputted target data must be mentioned as illustrated in figure 2. Although the sensor collects the image data over six-four minute segments in two hours, the Advisor-62 tape input to the DHRS plays back this data as if a continuous twenty-four minute image was collected, thus speeding up the target data rate by, at most, a factor of 5. The program managers made a decision that the Advisory-62 could be played back in segments that would simulate the actual target image collection rate.

3.0 CACHE STORAGE

3.1 Technical Problem

As mentioned in paragraph 2.1, the cache memory is simply a buffer that stores target input images when the input rate exceeds the exploitation output rate. The questions are then; How Large must the cache memory be? How does the difference in input versus output rate affect the system timelines? , and How should the cache be implemented?

RECONNAISSANCE MISSION (MINI-MISSIONS)

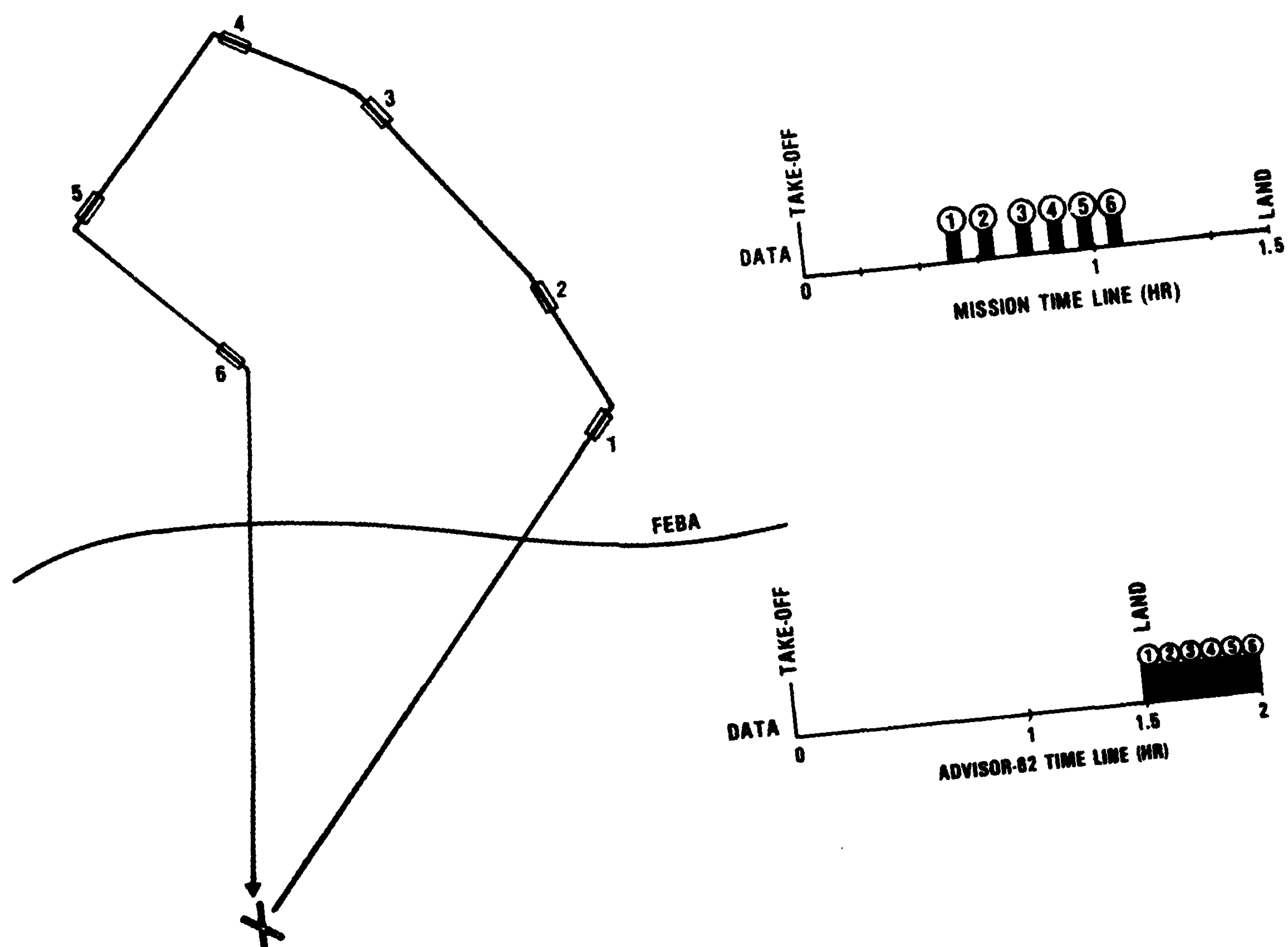


FIGURE 2

AVERAGE THROUGHPUT RATES

SENSOR	AAD-5			AAQ-9		
SCENARIO	AD-62	TEST	OP	AD-62	TEST	OP
MISSION DURATION (MIN)	--	--	120	--	--	120
TOTAL IMAGING TIME (MIN)	24	24	24	24	24	24
IMAGING SEGMENTS	6	4	6	60	30	18
SEGMENT DURATION (MIN)	4	6	4	0.4	0.8	1.3
TARGETS PER SEGMENT	20+10	20+10	8+2	4+1	3+1	3+1
TARGETS PER MISSION	180	120	60	300	120	72
AVERAGE TARGET RATE (PER MIN)	7.5	5	0.5	12.5	5	0.6
TOTAL FRAMES PER MISSION	17,280*	17,280*	17,280*	43,200	43,200	43,200
FRAME RATE (PER MIN)	720*	720*	720*	1,800	1,800	1,800
AVERAGE TARGETS PER TARGET FRAME	2.5	2.5	2.5	5	4	4
AVERAGE TARGET FRAME RATE (PER MIN)	3	2	0.2	2.5	1.25	0.15
TARGET FRAMES PER TOTAL FRAMES	1/240	1/360	1/720	1/720	1/1440	1/2400

*|FRAMES

TABLE 1

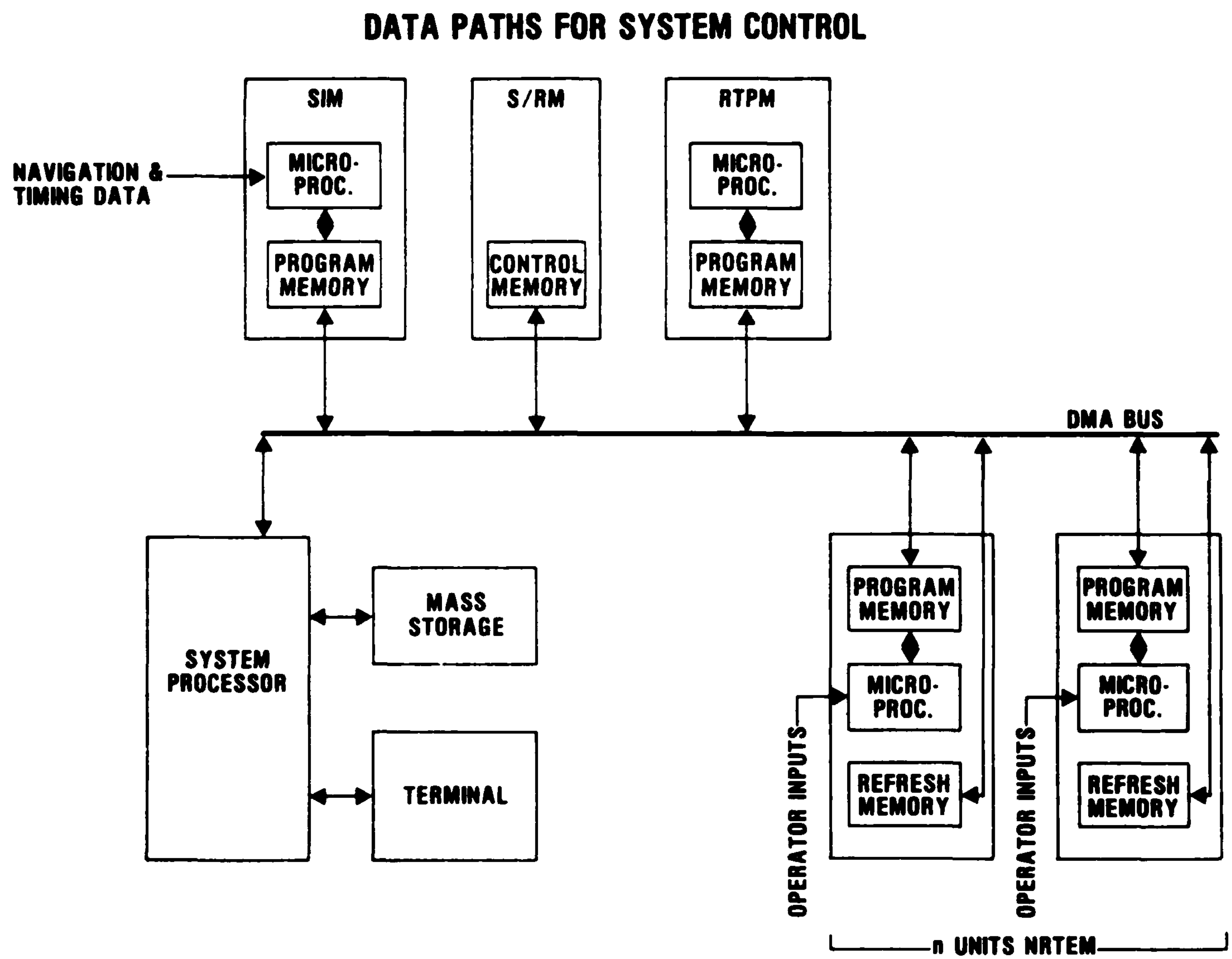


FIGURE 3, PRELIMINARY DHRS SCHEMATIC

DATA HANDLING RECORDING SYSTEM

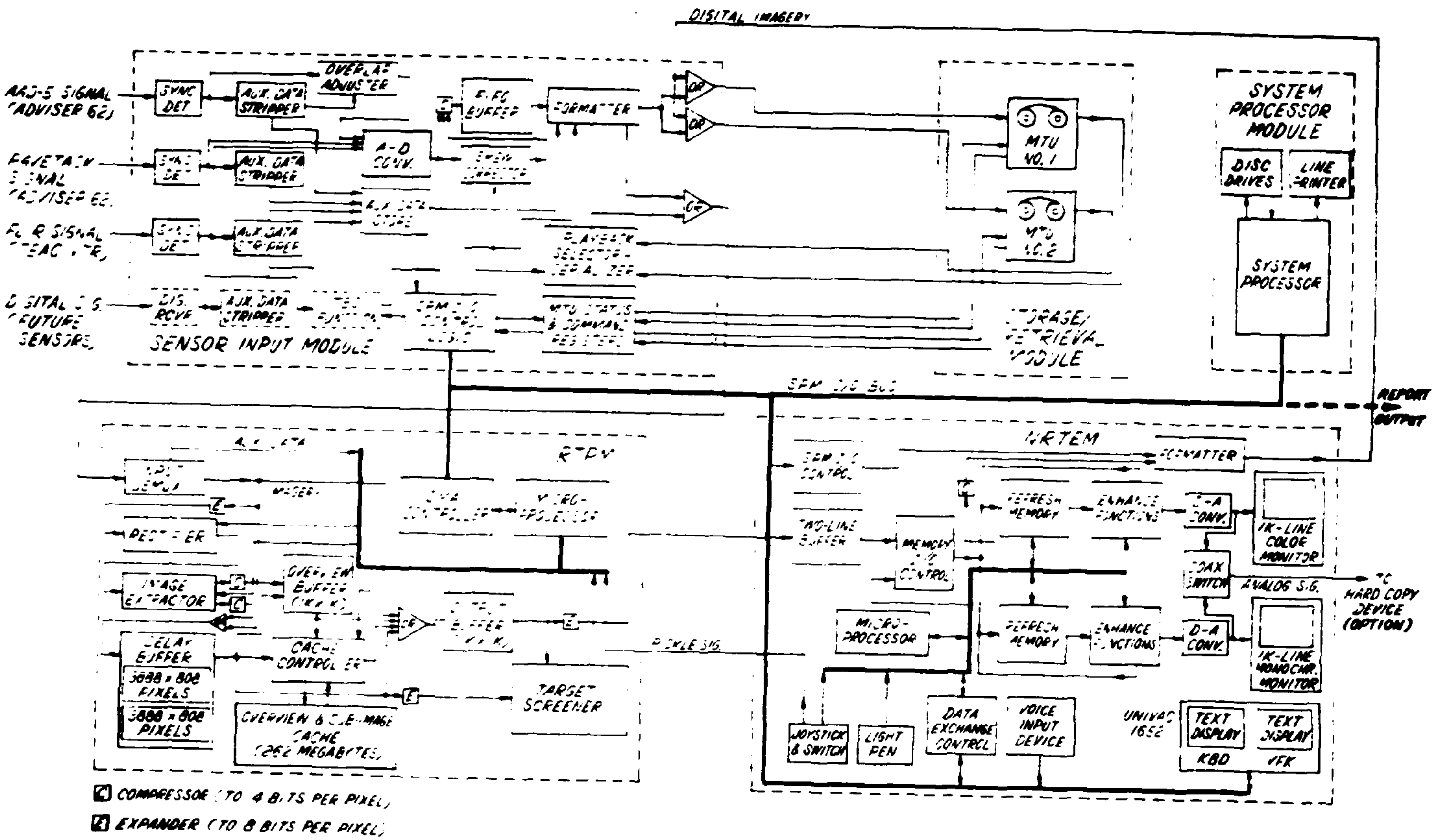


FIGURE 4

3.2 General Methodology

The assumed DHRS inputs are defined in figure 5. Figure 6 examines each of three ways that this data rate affects the system throughput based on an exploitation output rate of one target frame per minute. In case one, an unlimited cache is available and the twenty-four minutes of Advisor-62 is input continuously. In case 2 either a 20 or 30 frame cache is available and when either is filled (10 minutes for 20 frame cache and 15 minutes for 30 frame cache), the input from the Advisor-62 is interrupted until the cache is emptied (30 minutes and 45 minutes respectively). It is then restarted and in case of the 20 frame cache stopped again at 40 minutes and restarted at 60 minutes. The third case has no cache and the Advisor-62 input is stopped after each target image is received. In all cases, all processing of 72 target images is completed in 72 minutes. Figure 7 shows the number of images stored in the cache at any time. These data were developed without simulating the timeline of the data collection. Figure 8 shows the input when a realistic mission timeline is simulated and Figure 9 shows the cache loading for both 1 and 2 minute exploitation times. Table 2 shows how frame storage is performed by the cache. Finally, regardless of the cache size, delays in the system will occur because of exploitation/reporting time. Figure 10 examines these delays.

A final concern is the cost of the cache and the cost associated with exceeding the cache capacity. The cost of implementing the cache in RAM memory is two orders of magnitude more expensive per target frame than that of a disk memory. Second, the cost of storing the retrieving target frames that exceed the cache capacity in another memory device has associated with it a considerable cost in software and computer overhead.

3.3 Technical Results

The fundamental delay cause by the assumed target input rate exceeding the exploitation output rate cannot be improved upon except by employing additional exploitation stations or by assuming a faster exploitation time. A disk cache with virtually unlimited capacity costs about the same as a RAM cache of 7.5 target frame capacity. In addition, it will save all the software and computer costs associated with storing excess target images in another storage device. Finally, as shown in the Technical Proposal, the delays cause by implementing the cache in disk versus RAM will not exceed 2 seconds worst case, and thereby will not be objectional to the II. The disk cache was included in the baseline DHRS configuration.

4.0 MASS STORAGE

DHRS INPUT ASSUMPTIONS

AN/AAD-5

- 180 TARGETS PER MISSION
- 2.5 TARGETS PER TARGET FRAME
- 72 TARGET FRAMES PER MISSION
- 6 4-MINUTE IMAGING SEGMENTS PER MISSION
- 6 MINUTES BETWEEN IMAGING SEGMENTS

AN/AAQ-9

- 180 TARGETS PER MISSION
- 3 TARGETS PER TARGET FRAME
- 60 TARGET FRAMES PER MISSION
- 6 4-MINUTE IMAGING SEGMENTS PER MISSION
- 6 MINUTES BETWEEN IMAGING SEGMENTS

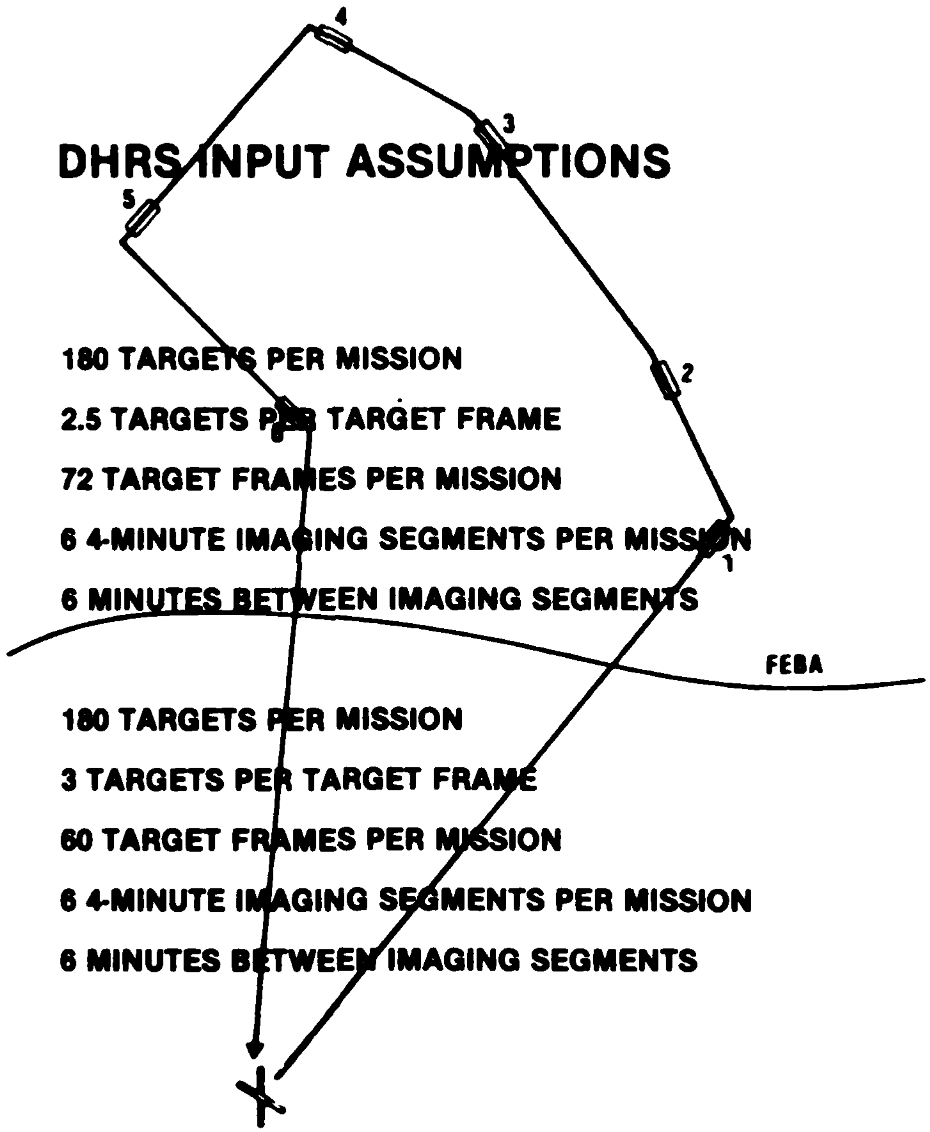
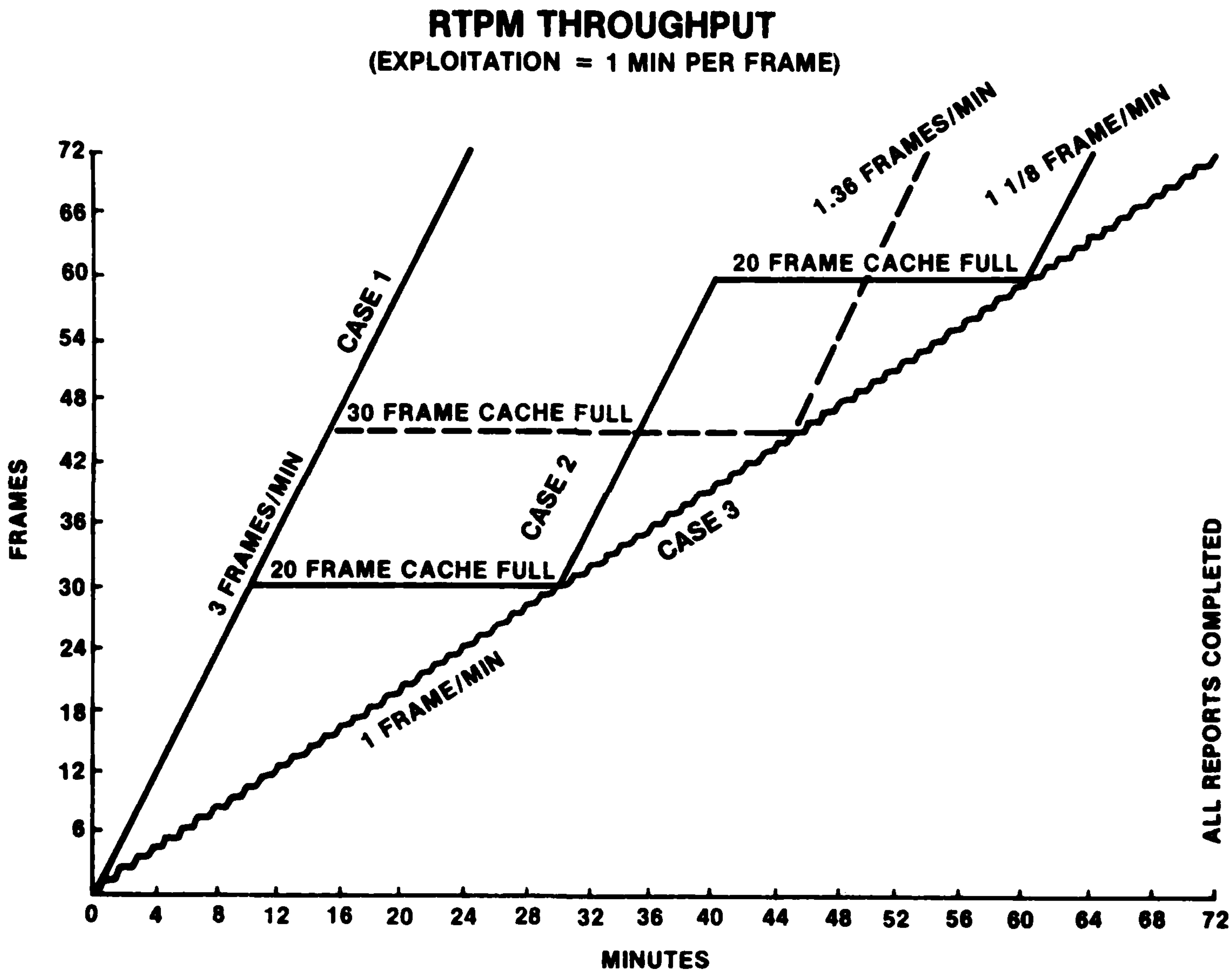


FIGURE 5



RTPM THROUGHPUT
(EXPLOITATION = 1 MIN PER FRAME)
FRAMES
72
66
60
54
48
42
36
30
24
18
12
6
0
4
8
12
16
20
24
28
32
36
40
44
48
52
56
60
64
68
72
MINUTES
CASE 1
3 FRAMES/MIN
30 FRAME CACHE FULL
20 FRAME CACHE FULL
CASE 2
CASE 3
1 FRAME/MIN
20 FRAME CACHE FULL
1.36 FRAMES/MIN
1 1/8 FRAME/MIN
ALL REPORTS COMPLETED

FIGURE 6

CACHE CONTENT

(EXPLOITATION = 1 MIN PER FRAME)

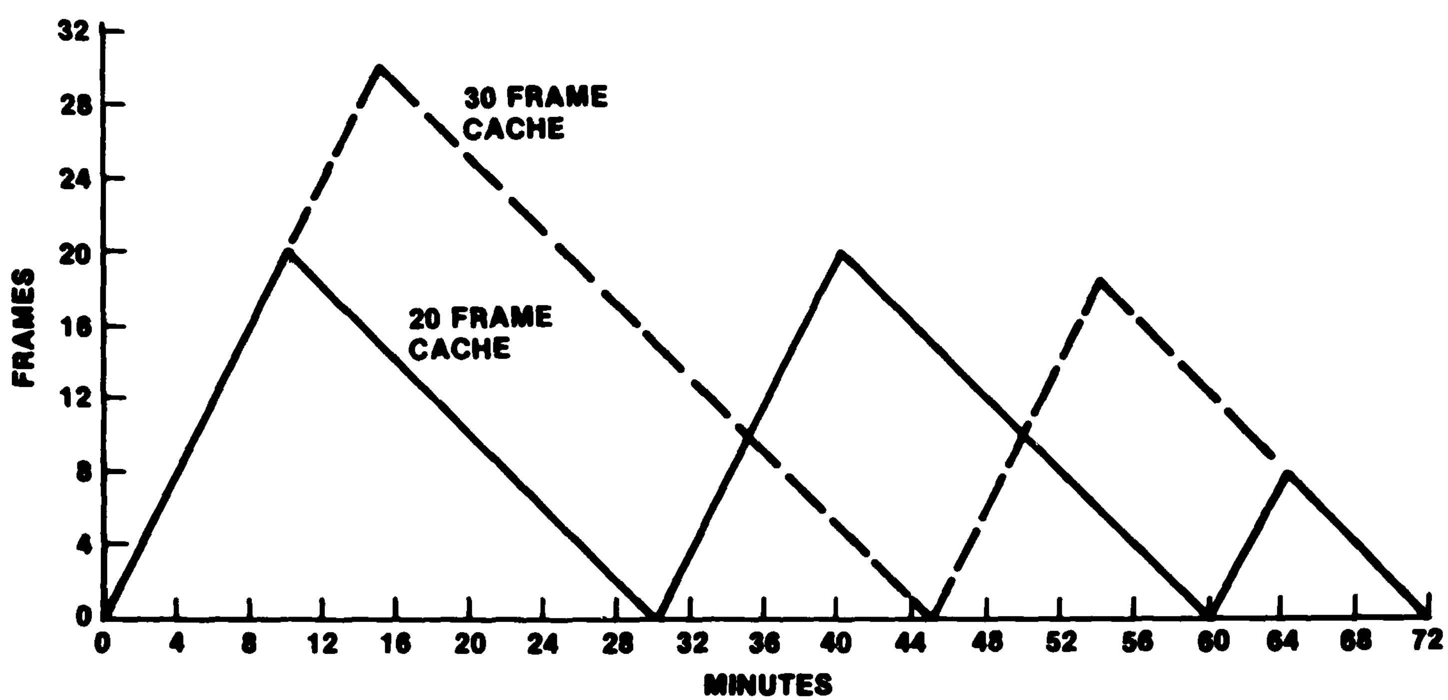


FIGURE 7

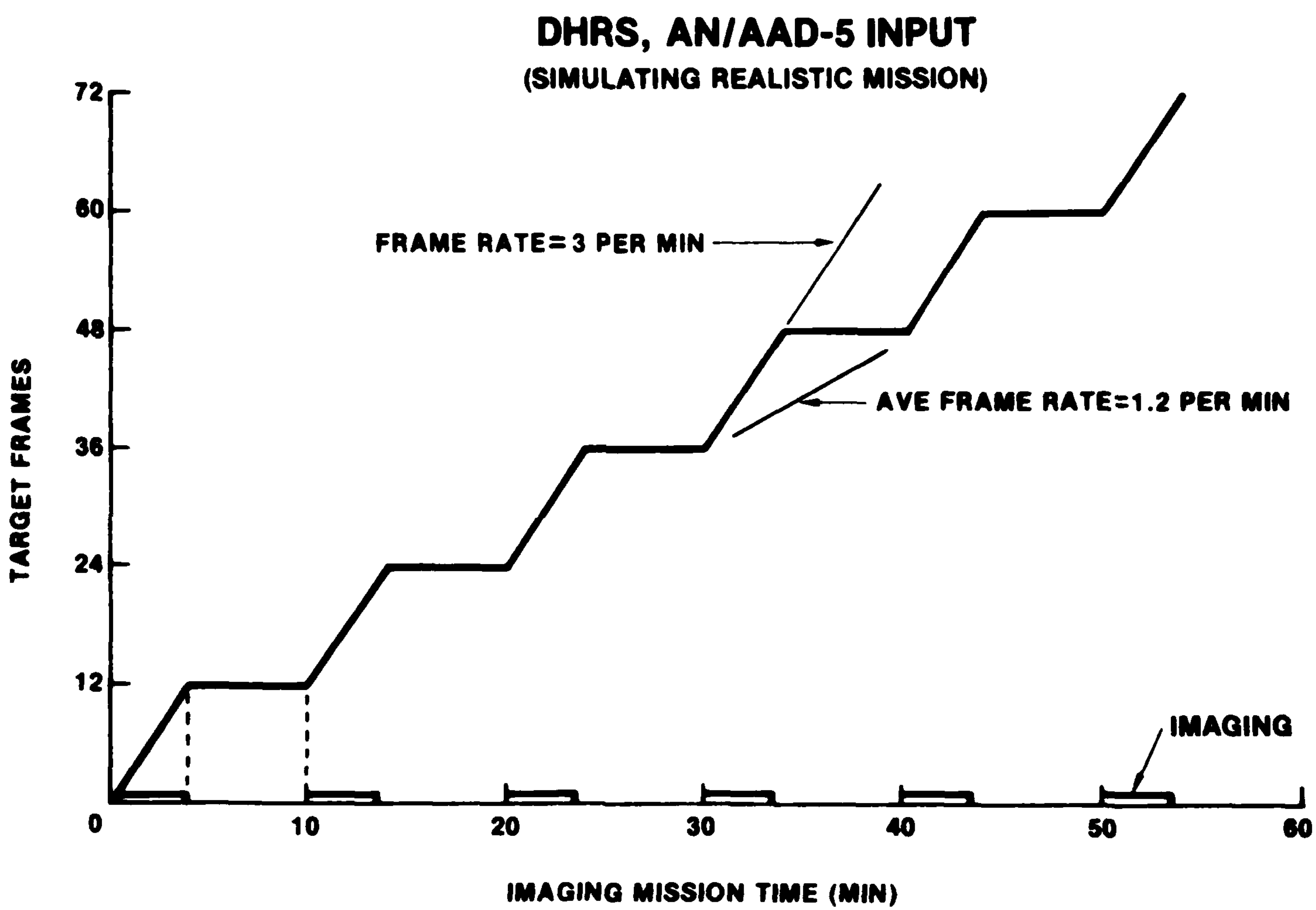

DHRS, AN/AAD-5 INPUT
(SIMULATING REALISTIC MISSION)
TARGET FRAMES
72
60
48
36
24
12
0
10
20
30
40
50
60
IMAGING MISSION TIME (MIN)
FRAME RATE=3 PER MIN
AVE FRAME RATE=1.2 PER MIN
IMAGING

FIGURE 8

AN/AAD-5 CACHE LOADING
(SIMULATING REALISTIC MISSION)

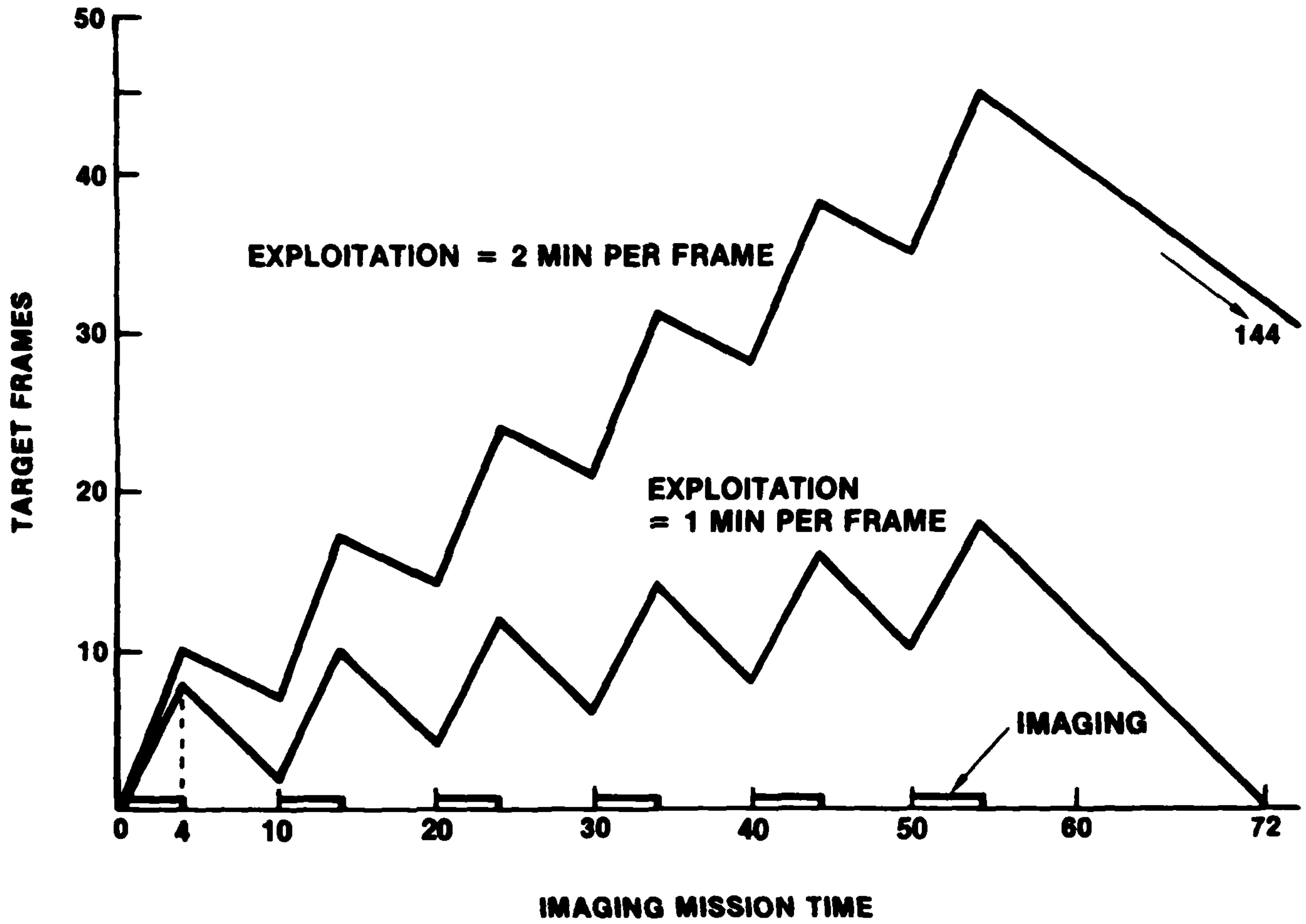


FIGURE 9

TABLE 2 CACHE OPERATION

IMAGING TIME (MIN)	TARGET FRAME NO.	IN NRTEM	IN CACHE (1 2 3 4 5 6 7 8)	REPORTED	DELAY (MIN)
1	1 2 3	1	2 2 3		
2	4 5 6	2	3 4 3 — 5 3 — 6	1	1
3	7 8 9	3	4 — 7 4 — 8 4 — 9	2	1.6
4	10 11 12	4	5 — 10 5 — 11 5 — 12	3	2.3
5		5	6 — 12 6 — 12 6 — 12	4	3
6		6	7 — 12 7 — 12 7 — 12	5	3.6
7		7	8 — 12 8 — 12 8 — 12	6	4.3
8		8	9 — 12 9 — 12 9 — 12	7	5
9		9	10 — 12 10 — 12 10 — 12	8	5.6
10		10	11 12 11 12 11 12	9	6.3
11	13 14 15	11	12 13 12 — 14 12 — 15	10	7
12	16 17 18	12	13 — 16 13 — 17 13 — 18	11	7.6
13	19 20 21	13	14 — 19 14 — 20 14 — 21	12	8.3
14	22	14	15 — 22	13	3

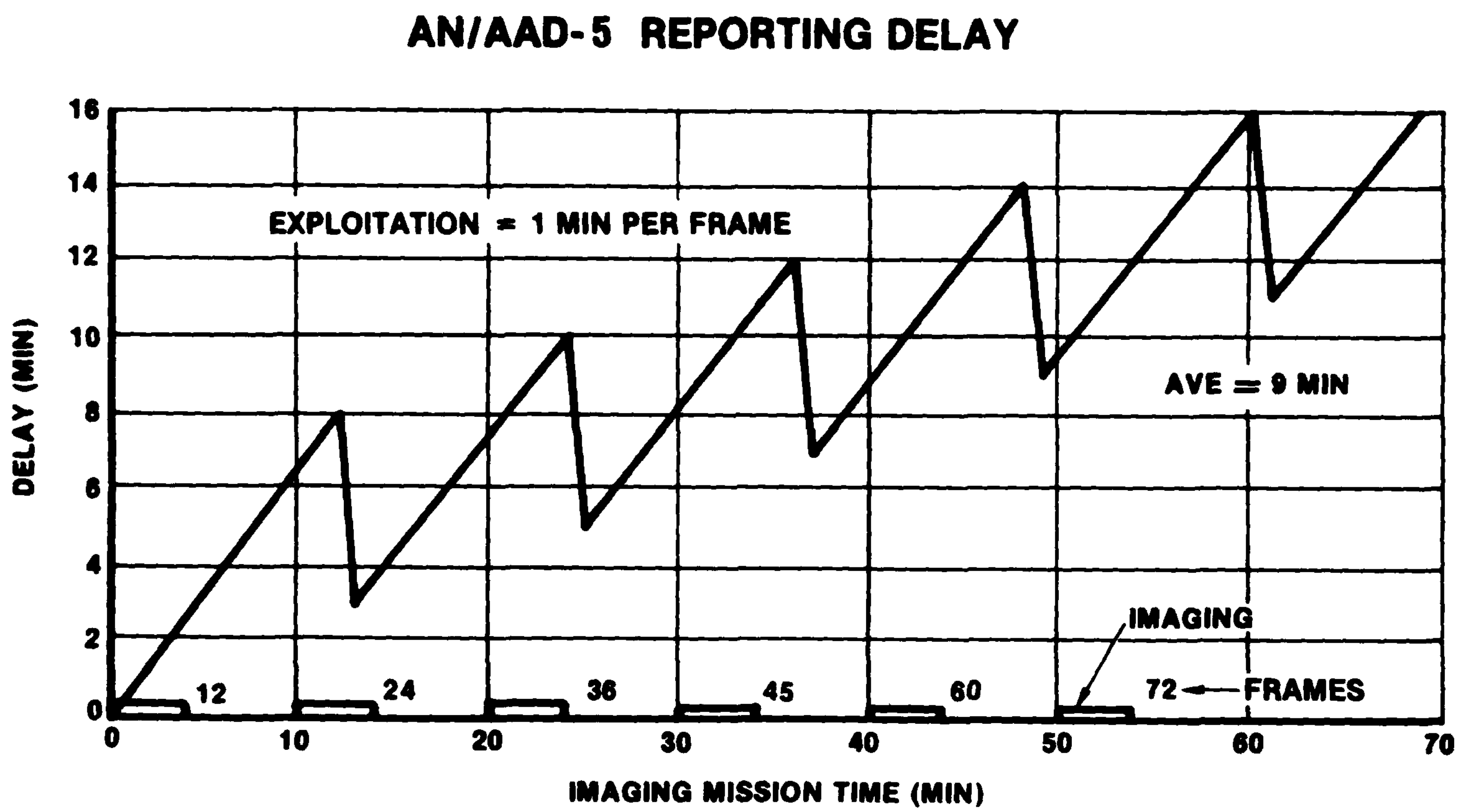

AN/AAD-5 REPORTING DELAY
EXPLOITATION = 1 MIN PER FRAME
AVE = 9 MIN
IMAGING
72 ← FRAMES
12
24
36
45
60
DELAY (MIN)
IMAGING MISSION TIME (MIN)
0
2
4
6
8
10
12
14
16
0
10
20
30
40
50
60
70

FIGURE 10

4.1 Technical Problem

Figure 11 summarizes the mass storage requirement of the DHRS. The characteristics of candidate technologies that might satisfy these requirements are shown in Figure 12. Included in the optical disk technology survey were those under development by RCA, MCA and the GE Advanced Archival Storage System (BEAMOS extension). Although these devices have been demonstrated in laboratory environments, no prospective manufacturer would commit to a production model delivery to support the DHRS schedule. Figure 13 tabulates the characteristics of instrumentation tape unit technology selected for the baseline DHRS configuration. The minimum cost for 10^{12} bits on line of 500 thousand dollars is considered excessive.

4.2 General Methodology

Figure 14 summarizes the conclusions of the technology trade off in selecting a mass storage device. With the characteristic defined for the mass storage, a request for proposal was prepared and sent to the following vendors:

Honeywell
Ampex
Bell and Howell
Sangamo
RCA (no bid)

4.3 Technical Results

With the mass storage device relieved of storing any cache overload (see paragraph 3.3) and with data compression, (see paragraph 7.3) a single reel of 28 track tape can store an entire 24 minutes of digitized Advisor-62 tape. It was selected as the most cost effective method of providing the required mass storage. Of the tape units, the Ampex HBR-3000 was selected for its match to the mass storage requirements and its cost, and is included in the DHRS baseline configuration.

5.0 DISPLAYS

5.1 Technical Problem

The AN/AAD-5 produces imagery of very large extent. How can this imagery be presented on a limited extent CRT, cost effectively?

5.2 General Methodology

A simply linear relationship exist between number of displayed pixels and cost, i.e. a 2048 line by 2048 pixel display costs approximately 4 times a 1024 line by 1024 pixel display and 16

STORAGE AND RETRIEVAL MODULE (S/RM) RFP REQUIREMENTS

CAPACITY: 10^{12} BITS EQUIVALENT (4.1.1.2.1)

OPERATING MODES: SIMULTANEOUS RECORD AND/OR PLAYBACK (4.1.1.3.3.1)

DATA TRANSFER RATES: 4.1.1.1.6: "... PRESENT BANDWIDTHS OF 6 TO 7 MHz..."

4.1.1.1.3: "... 100 MEGABITS/SEC."

4.1.1.2.5: "... SHALL STORE BOTH THE ... RTPM OUTPUT AND THE INPUT IMAGE."

FIGURE 11

S/RM CANDIDATE TECHNOLOGIES

- MAGNETIC DISC: A DISC SYSTEM FOR 10^{12} BITS IS NOT WITHIN REASON IN TERMS OF COST AND SIZE

- OPTICAL DISC: A MATURE PRODUCT IS NOT EXPECTED TO BE AVAILABLE AS REQUIRED BY DHRS. DEVELOPMENTS IN THIS AREA WILL BE MONITORED

- COMPUTER PERIPHERAL TAPE UNITS: DATA RATES AND STORAGE CAPACITIES AVAILABLE DO NOT SATISFY DHRS REQUIREMENTS

- INSTRUMENTATION TAPE UNITS: THIS IS THE TECHNOLOGY SUITED TO THE DHRS REQUIREMENTS

FIGURE 12

MTU CHARACTERISTICS

NUMBER OF TRACKS	14	28	42	84
TAPE WIDTH, INCHES	1	1	1	2
RECORD SPEED FOR 100 Mb/s (ips)	240	120	80	40
TAPE CAPACITY, BITS (APPROX.)	½ x 10^{11}	10^{11}	1½ x 10^{11}	3 x 10^{11}
NUMBER OF REELS FOR 10^{12} BITS	20	10	7	4
TAPE CHANGE INTERVAL FOR CONTINOUS RECORDING OF 100 Mb/s DATA, MINUTES	7.7	15.3	23.1	46.2
APPROXIMATE MTU COST, QUANTITY ONE	$56K	$96K	$160K	$500K
FOR 10^{12} BITS ON LINE	$1120K	$960K	$1120K	$1052K
W/SHARED ELECTRONICS	$685K	$500K	$474K	
FLOOR SPACE (SQUARE FEET)	120	60	84	48

FIGURE 13

S/RM VIEW

- SYSTEM PERFORMANCE/COST TRADE-OFF WILL ULTIMATELY PROVIDE A BASIS FOR S/RM CONFIGURATION CHOICE
- THE 28 TRACK SYSTEMS OFFER ADEQUATE DATA RATE CAPABILITY AND THE OPPORTUNITY TO MINIMIZE COST
- THE 84 TRACK SYSTEMS OFFER SUPERIOR PERFORMANCE
- OPTICAL DISC SYSTEMS OFFER PROMISE FOR THE FUTURE
- SYSTEM USAGE OF DATA COMPRESSION COULD SAVE COST

FIGURE 14

times more than a conventional 512 line by 512 pixel display. However, from a utility point of view, the 2K x 2K display is more effective than 4 and 16 times, respectively. This results from requiring overlap to avoid cutting targets in half when segmenting an image into smaller subdivisions. If 20% overlap is provided then a 2K x 2K display will require 5.8-1K x 1K and 33.2-5K x 5K displays. Therefore the cost benefit of a 2K x 2K display is 44% better than a 1K x 1K display and 101% better than .5K x .5K. These calculations imply that the largest display that supports the DHRS schedule, and is within DHRS budget limitation, should be utilized.

5.3 Technical Results

The cost and developmental risk associated with a 2K by 2K display eliminated it from further consideration at this time. A survey of ten companies that produce lower resolution image displays was conducted. The results of this survey is shown in tables 3-5. The Comtal Vision one/20 was selected for inclusion in the DHRS baseline since it provides 1K by 1K display with versatility and reasonable cost and delivery.

6.0 TARGET SCREENER

6.1 Technical Problem

Figure 15 is the objective of the effort assigned to MC^2 under a subcontract agreement. Specific evaluation criteria are shown in Figure 16.

6.2 General Methodology

A preliminary survey was made of 13 potential target screeners for which data was available. These target screeners were subsequently categorized as shown in Figure 18. All screeners used a basic algorithm generalized in Figure 19. The specific details used in the NEMD "ATC" are diagrammed in Figure 20.

6.3 Technical Results

The three previous mentioned screeners as well as the Rockwell International "ISA" target screener were considered equivalent, in that they all performed similarly and all equally failed to meet the evaluation criteria. Therefore, to evaluate availability in meeting the DHRS schedule and cost, request for proposal was sent to Westinghouse, Honeywell, Rockwell International and Northrop Electro-Mechanical Division. The responses received from the last two companies are included as Appendix B and C to CDRL A003 Technical Proposal/Program plan.

DISPLAY SYSTEM COMPARISON

		REFRESH MEMORY			DISPLAY PRESENTATION			
	MODEL	NUMBER	SIZE	ZOOM	TRUE COLOR	TEST PATTERNS	SPLIT SCREEN	REFRESH RATE
AYDIN	5216	8	512x512x8	2, 4, 8, 16	YES	ALL	4-WAY	60 Hz
COMTAL	ONE/20	64	512x512x8	2, 4	YES	ALL	4-WAY	30 Hz 60 Hz
DE ANZA	5000	4	512x512x8	2, 4, 8	YES	ALL	4-WAY	30 HZ
GENISCO	3000	3	512x512x8	2, 4, 8	YES	NONE	NONE	30 Hz 40 Hz
GRINNELL	270	4	512x512x8	2, 4, 8	YES	ALL	LEFT/RIGHT TOP/BOTTOM	30 HZ
HAZELTINE	17	10	512x512x8	NONE	YES	NONE	4-WAY	30 Hz
ISI	VIEWS	PROG.	PROG. (1 MBYTE)	1, 2,...,16	YES	ALL	NONE	30 Hz
I^2S/STC	70	12	512x512x8	1, 2,...,16	YES	ALL	4-WAY	30 Hz
LEXIDATA	3400	2	640x582x8	1, 2,...,16	YES	ALL	LEFT/RIGHT	30 Hz 60 Hz
RAMTEK	9400	4	512x512x8	1, 2,...,16	YES	ALL	4-WAY	30 Hz

TABLE 3

DISPLAY SYSTEM COMPARISON (Cont'd)

	PROCESSING CAPABILITIES				DISPLAY PRESENTATION			
	MICROPROCESSOR	VIDEO PROCESSOR	FEEDBACK LOOP	HISTOGRAM HARDWARE	TRUE COLOR	TEST PATTERNS	SPLIT SCREEN	REFRESH RATE
AYDIN	8086	NO	NO	NO	YES	ALL	4-WAY	60Hz
COMTAL	LSI-11	YES	8 BIT	YES	YES	ALL	4-WAY	30 Hz 60 Hz
DE ANZA	LSI-11	DUAL 16 BIT	DUAL 16 BIT	YES	YES	ALL	4-WAY	30 Hz
GENISCO	IN-HOUSE DESIGN	NO	NO	NO	YES	NONE	NONE	30 Hz 40 Hz
GRINNELL	NONE	YES	16 BIT	YES	YES	ALL	LEFT/RIGHT TOP/BOTTOM	30 Hz
HAZELTINE	NONE	NO	8 BIT	YES	YES	NONE	4-WAY	30 Hz
ISI	LSI-11	NO	NO	YES	YES	ALL	NONE	30 Hz
I^2S/STC	11/03	13 BIT	16 BIT	YES	YES	ALL	4-WAY	30 Hz
LEXIDATA	IN-HOUSE DESIGN	NO	NO	NO	YES	ALL	LEFT/RIGHT	30 Hz 60 Hz
RAMTEK	Z80 & 2901	NO	NO	NO	YES	ALL	4-WAY	30 Hz

TABLE 4

DISPLAY SYSTEM COMPARISON (Cont'd)

	GRAPHICS OVERLAYS AND CURSORS					LUTs		
	NUMBER GRAPHICS	NUMBER CURSORS	CURSOR SHAPE	METHOD OF COMBINATION	VECTOR/ CHARACTER	B&W SIZE	PSEUDO SIZE	LOAD DURING RETRACE
AYDIN	6	6	16x16 PROG.	REPLACE SUMMATION	FIRMWARE HARDWARE	4096x12	256x24	YES
COMTAL	512	1	16x16 PROG	REPLACE SUMMATION	FIRMWARE	256x8	256x24	YES
DE ANZA	8	3	16x16 PROG. 8 STD. SHAPES	LUT	FIRMWARE HARDWARE	256x8	256x24	YES
GENISCO	3	2	4 STD. SHAPES	REPLACE	FIRMWARE HARDWARE	256x8	4096x24	NO
GRINNELL	4	4	PROM	REPLACE	HARDWARE	4096x8	1024x24 4096x12	YES
HAZELTINE	8	2	FIXED	REPLACE CONTRAST	NONE	256x8	256x24	YES
ISI	PROG.	2	FIXED/ WINDOW	LUT	FIRMWARE	256x16	512x14	YES
I^2S/STC	8	2	64x64 PROG.	REPLACE SUMMATION	FIRMWARE	256x10 8192x10	256x30	YES
LEXIDATA	6	1	64x64 PROG.	LUT or HARD-WIRED	FIRMWARE	4096x32	4096x24	YES
RAMTEK	16	8	GRAPHICS OVERLAY	REPLACE LUT	FIRMWARE	4096x8	256x24	YES

TABLE 5

OBJECTIVE

DEFINE THE OPTIMUM TARGET SCREENER FOR DHRS

-- OVERRIDING CONSTRAINT --

NO MAJOR DEVELOPMENT. THE TARGET SCREENER WILL BE BASED UPON ONE OF THOSE ALREADY DEVELOPED AND FIELDABLE DURING OR BEFORE DHRS PHASE II. ENHANCEMENTS REQUIRING MINIMAL DEVELOPMENT COST WILL BE CONSIDERED.

FIGURE 15

EVALUATION CRITERIA

FLEXIBILITY AND EXPANDABILITY TO PROVIDE FOR:

- ACCOMMODATION TO NEW SENSORS
- INTRODUCTION OF NEW ALGORITHMS
- INTRODUCTION OF NEW TARGET CLASSES
- INTEGRATION INTO DHRS

AVAILABILITY/MATURITY

FUNCTIONAL AND OPERATIONAL REQUIREMENTS

- 100 Mbps INPUT RATES
- EIGHT CLASSES OF TARGETS
- EFFECTIVENESS:
  - 90% DETECTION
  - 80% CORRECT CLASSIFICATION
  - 10% OR LESS MISCLASSIFICATION
- VAN ENVIRONMENT

COMPATIBILITY WITH OVERALL DHRS

RELIABILITY/MAINTAINABILITY

COST

FIGURE 16

PRELIMINARY SURVEY

		LEVEL OF IMPLEMENTATION		CAPABILITIES						
				RECTIFICATION						
NAME/ DESCR	ORGN	EXPERIMENTAL LABORATORY	DESTINED FOR FIELD USE	RADIOMETRIC	GEOMETRIC	ENHANCE.	FEATURE EXTRACT.	DETECT	CLASSIF.	OTHER
PATS	HONEYWELL		✓	?	?	✓	✓	✓	✓	
AIS	NEMO		✓	✓	?	✓	✓	✓	✓	
IPS/ OLPARS	PAR	✓		?	?	✓	✓	✓	✓	
	ERIM	✓				✓	✓	✓	✓	
AUTOTHRESHOLD/ AUTOSCREENER/ATSS	HONEYWELL	✓		?	?	?	✓	✓	SORT OF	
AFES	PAR	✓		?	?	✓	✓	✓	✓	● STEREO ● VOICE
2-D FILTER CHIP	HUGHES	✓				✓	✓			
SARF	GM	✓					✓	✓	?	
DX-1	AFCRL	✓					✓	✓	?	
INTERSPACE	PURDUE	✓					✓	✓	?	
MERLIN	MSC	✓					✓	✓	?	
IBM INTERACTIVE SYSTEM	IBM	✓					✓	✓	?	
BICIPER	PAR	✓				✓	✓	✓		

FIGURE 17

INVESTIGATION HIGHLIGHTS

- CATEGORY 1 - SYSTEMS
  - HONEYWELL - "PATS"/"ISA"
  - WESTINGHOUSE - "SMART SENSOR"
  - NEMD - "ATC"
- CATEGORY 2 - COMPONENTS
  - ROCKWELL - "ALO"/"ISA" (PROBABLE CATEGORY 1)
  - HUGHES - PROGRAMMABLE ANALOG CHIP
- CATEGORY 3 - IDEAS/LABORATORIES
  - PAR - "IPS"
  - U. of MD. - RELAXATION, ANTI-PARALLEL PAIRS
  - SUNY (BING.) - TEXTURE CLASSIFICATION (80% ACCURACY)
  - USC - TEXTURE CLASSIFICATION (89% ACCURACY)

FIGURE 18

BASIC ALGORITHM

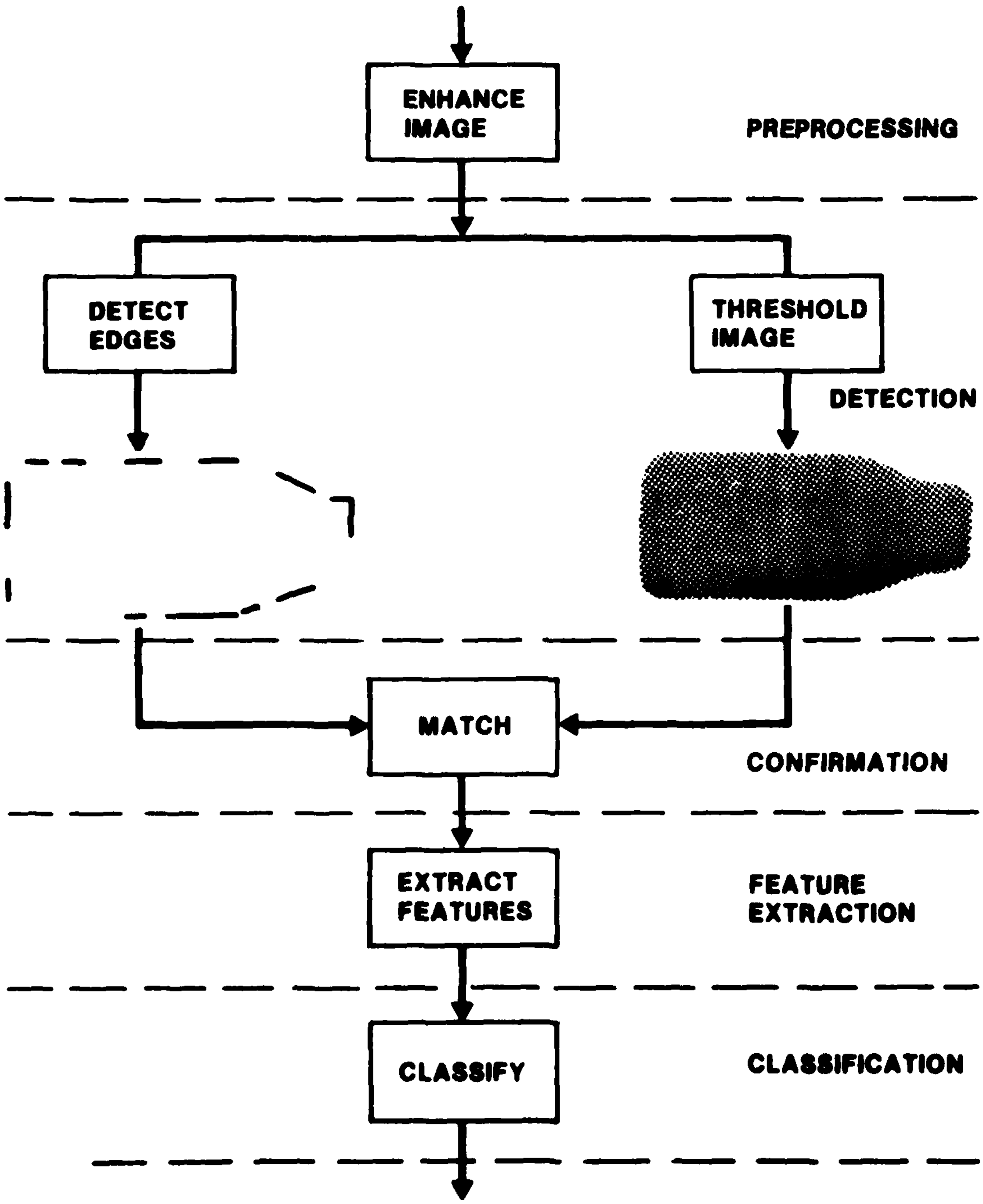


FIGURE 19

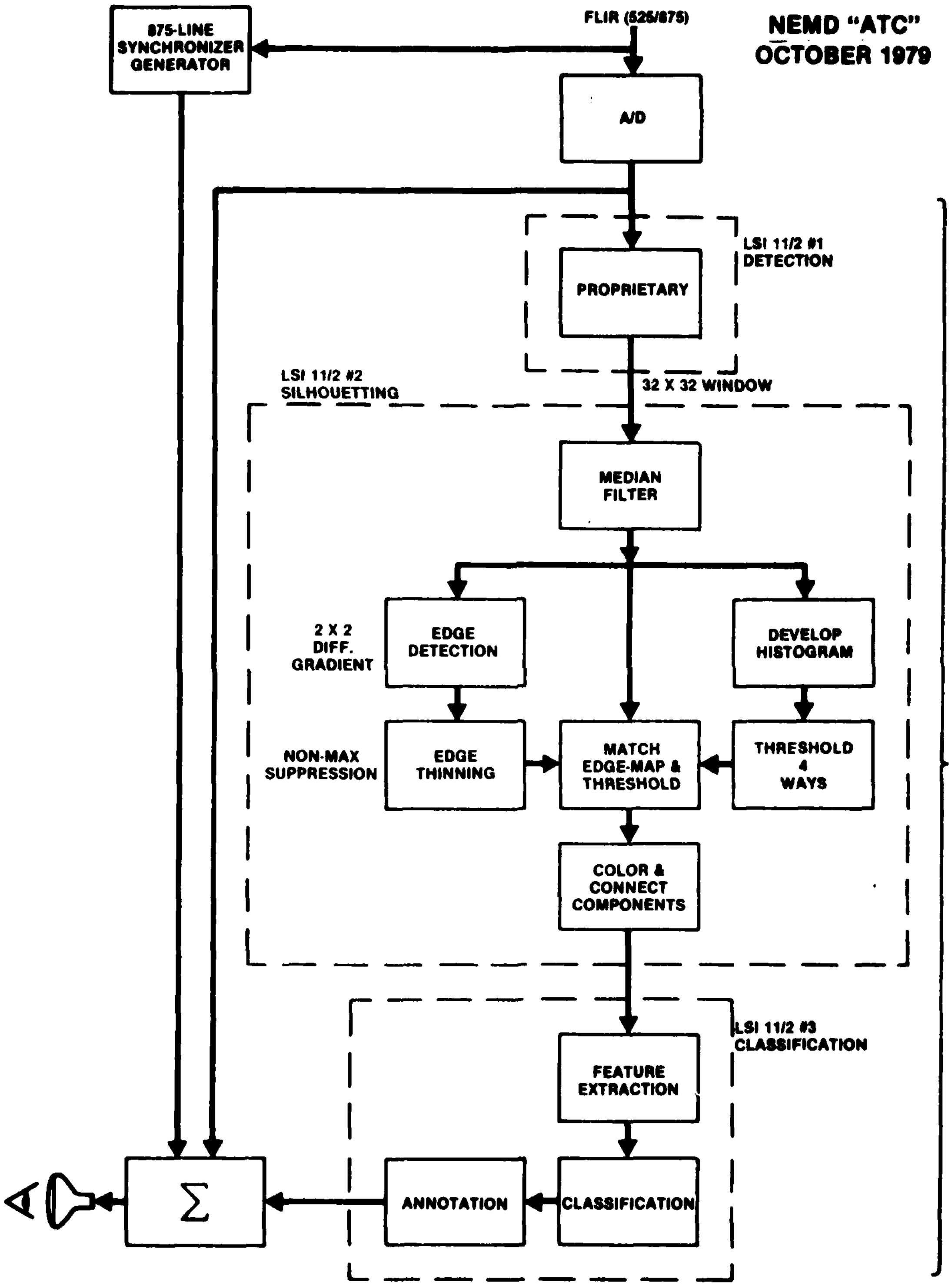

NEMD "ATC"
OCTOBER 1979
875-LINE SYNCHRONIZER GENERATOR
FLIR (525/875)
A/D
LSI 11/2 #1 DETECTION
PROPRIETARY
32 X 32 WINDOW
LSI 11/2 #2 SILHOUETTING
MEDIAN FILTER
2 X 2 DIFF. GRADIENT
EDGE DETECTION
DEVELOP HISTOGRAM
NON-MAX SUPPRESSION
EDGE THINNING
MATCH EDGE-MAP & THRESHOLD
THRESHOLD 4 WAYS
COLOR & CONNECT COMPONENTS
LSI 11/2 #3 CLASSIFICATION
FEATURE EXTRACTION
ANNOTATION
CLASSIFICATION
Σ
GENERAL PURPOSE PROCESSORS

FIGURE 20

7.0 COMPRESSION-EXPANSION

7.1 Technical Problem

The DHRS requires considerable amounts of expensive memory in the FIFO Buffer and Formatter of the SIM, the MTU's of the SRM, and Delay Buffer, Overview Buffer, Cache and Output Buffer of the RPTM. See Figure 4.

7.2 General Methodology

The literature on image data compression was surveyed to find a method of reducing the dynamic range of the image data while retaining its fidelity.

7.3 Technical Results

Differential Pulse Code Modulation (DPCM) was selected for inclusion in the DHRS baseline. DPCM was employed because: it exploits the signal statistics of digital imagery and the visual properties of the observer, it is simple to implement and it halves required memory and its attendent costs.(1)

(1) Netravali, Arun N., and Limb, John O., Picture Coding: A Review, IEEE 1980

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