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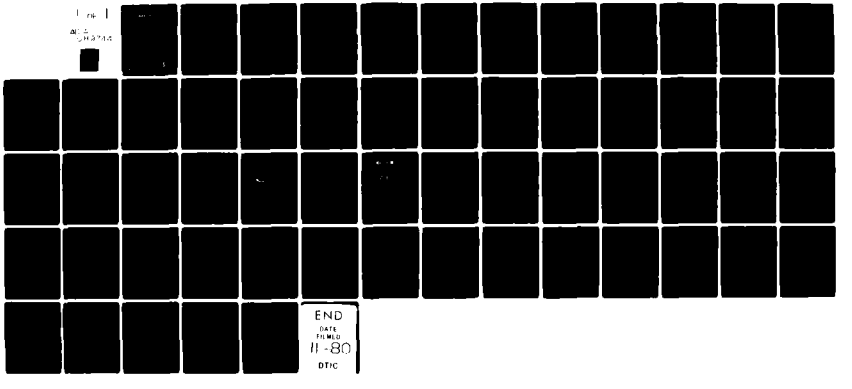

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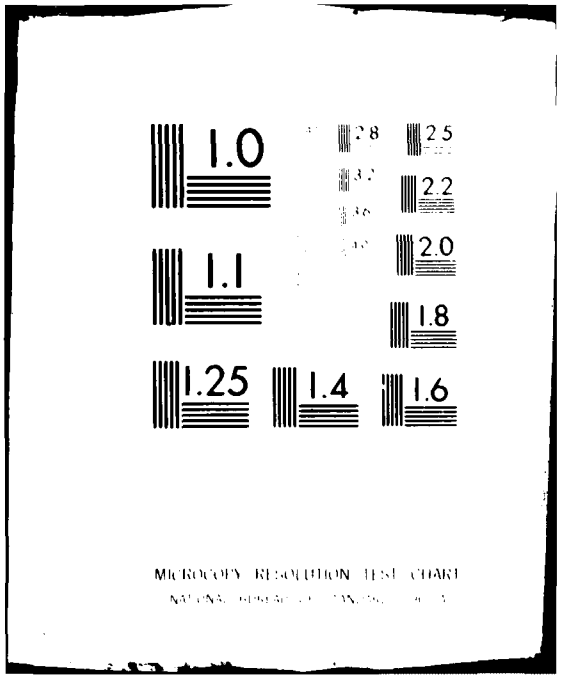
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THE BOEING COMPANY

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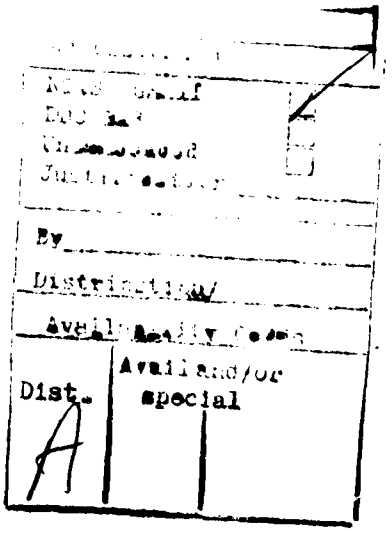
ABSTRACT

The results of a preliminary study on thermal modeling and analysis of microcircuits are presented. Studies covering typical components mounting methods, bonding agent materials component spacing, and cooling concepts are described. Temperature profiles of substrates, component temperatures and thermal resistances are presented. It is shown that the use of moly tabs, sputtered beryllia and thermo-electric coolers can significantly reduce component temperature levels. Additionally, it is illustrated that thermal modeling can aid the circuit designer in the layout and preliminary design phases.



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USE FOR TYPEWRITTEN MATERIAL ONLY

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NOMENCLATURE

A = Cross-sectional area of thermal conductance path
k = Temperature dependant thermal conductivity
K = Thermal conductance
L = Length of conductance path
F = Radiation interchange factor
T = Temperature
S = Thermal source strength
σ = Stefan - Boltzman constant

Subscripts
i = node index
j = node index

1.0 INTRODUCTION

Microcircuits consist of integrated circuit devices, semi-conductor components, and other non-semiconductor elements mounted in a patterned array. The various devices are electrically interconnected by thick film conductors, metalized connecting strips or wire bonds. The array is attached to a suitable substrate such as alumina, beryllia, or porcelain. Typically a substrate is then bonded to a base material and placed in a hermetically sealed container, as shown in Figure (1).

Primary sources of heat generation are considered to occur at emitter junction regions of the semiconductor devices. Secondary sources for thermal dissipation occur in the discrete elements such as thick and thin film resistors. Since both large temperature excursions and thermal cycling can significantly decrease the life of the circuit, consideration of thermal effects must be included during the design phase.

The importance of thermal cycles and increased circuit temperatures may be illustrated by considering life testing techniques for semiconductors (1)*. Accelerated life testing can be achieved by thermal cycling. That is, through thermal cycling the life time span of normal equipment can be compressed by a factor of 200 to 400. Similarly, elevated temperatures can result in increased aging. Silicon devices operated at 300°C will age 10,000 times faster than the same device at 125°C. The effect of a 200°C environment compared to one at 125°C results in increased aging at a rate of 170 times faster. Thus, the minimization of both temperature gradients and thermal cycling should be a constraint of the circuit designer.

The circuits considered herein are usually mounted on a substrate by either a metal filled epoxy or by a eutectic bond. Transfer of the thermal energy dissipated by the components is primarily by conduction through the bond material into the substrate. The thermal energy then diffuses through the remaining bond material

*Numbers in parenthesis denote references.

into the base where the heat can be removed from the package. The removal of the thermal energy from the package base can be acheived by a variety of standard techniques constrained only by the overall packaging method. That is, a conductive path through a circuit card to the mounting structure can be employed or forced convection exchange with the ambient environment may be utilized.

Circuit components are extremely small in physical dimensions but their power dissipation can be relatively large in terms of heat flux. It is not uncommon for a "power chip" to have dimensions of 20 mils by 15 mils while dissipating nearly one watt of energy. This gives a heat flux of 1.64×10^6 BTU/hr ft^2 over an area of 0.0003 square inches. The combination of the large localized heat fluxes, state of the art mounting techniques, and proposed large scale integrated circuit (high density packaging) are not compatible with current cooling techniques. Thus some technique is needed by the designer to determine the best spatial locations of the components in the array and for investigating new mounting and cooling methods. Thermal modeling offers such as design tool permitting parametric design changes, temperature predictions and comparative temperature control studies to be accomplished prior to circuit fabrication (2), (3), (4), and (5).

2.0 ANALYSIS

A physical description of a typical hybrid microcircuit and packaging container is illustrated by the sketch given in Figure 1. Each circuit contains multiple semiconductor devices and resistor elements mounted on a common base which may be cooled by a variety of techniques. The thermal energy dissipated by the multiple components and the presence of various material and interfaces presents a heat transfer problem which can be solved realistically only by computer methods, (6) and (7).

A generalized lumped parameter nodal thermal model was formulated to represent the various materials, interfaces and multiple heat dissipating components of a hybrid microcircuit, (6). The physical system was sectioned into an array of discrete nodal volumes, and the mass of each volume was then "lumped" at a point within the volume which it represented. The paths for heat transfer from one node to another were represented by conductors joining the appropriate nodes. The thermal model contained 2000 nodes to represent the circuit and substrate layers. The nodes were divided into 8 layers of material (volume containing) nodes and 2 layers of surface (boundary) nodes. All the layers were arranged in a 20 X 10 grid pattern with the size of the divisions in the grid, the thermal conductivity, and the thickness of the layers of material nodes being determined by the program user. The lowest layer of nodes, which represented the bottom surface of the base, were boundary nodes. Above the layer of boundary nodes were four layers of material nodes, thus allowing the use of four layers of material in the substrate. Another layer of boundary nodes was provided on the top surface of the substrate. While the geometry of the lower six layers, or substrate, could only be that of a square or rectangle, it was possible, through the use of special control cards, to represent various shapes and sizes of components in the upper four layers of nodes. These components consisted of epoxy layers, powered electrical devices, resistors, moly tab mounts, or connecting strips. In Figure 2 an example circuit is shown in which only two of the upper four

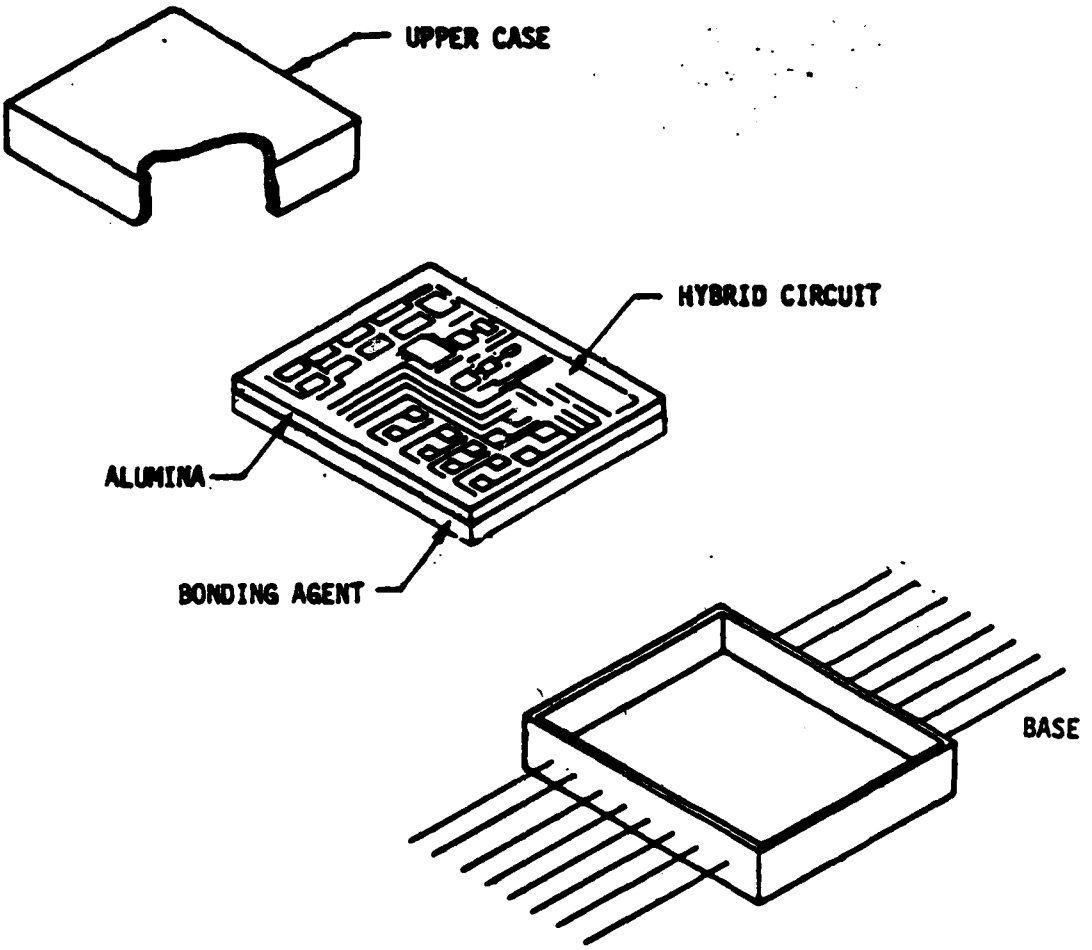


FIGURE 1: HYBRID MICROCIRCUIT

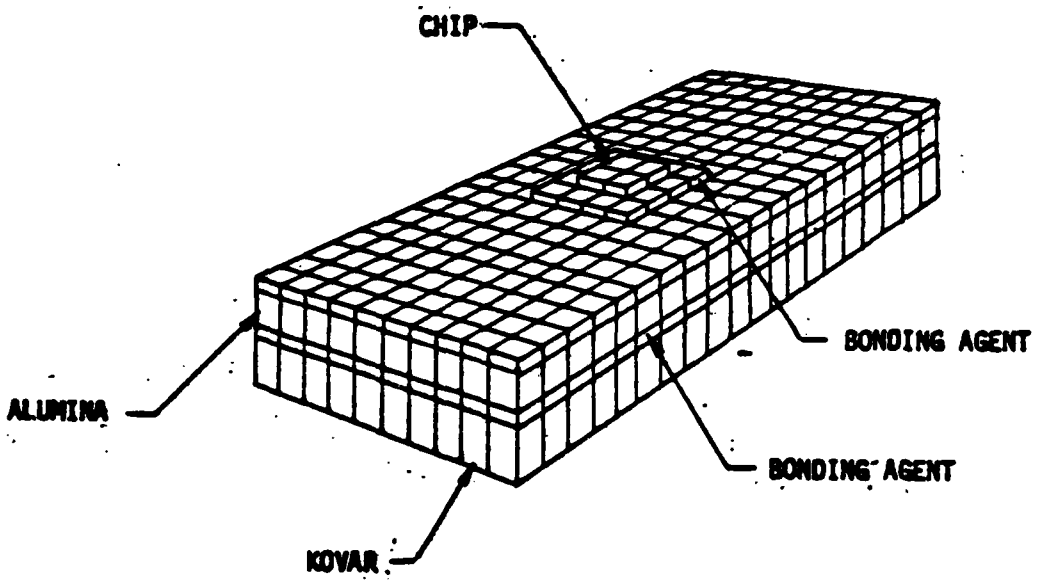


FIGURE 2: THERMAL MODEL OF A SINGLE CHIP AND SUBSTRATE

3.0 DISCUSSION OF RESULTS

A parameter which is often specified for circuit design purposes is the thermal resistance of a mounted powered component. The overall thermal resistance is defined by dividing the temperature difference between the device and the case by the thermal power dissipated in the device. In the case of a one watt thermal dissipation the value of temperature is equivalent to the thermal resistance. Table 1 lists typical material thermal conductivities.

3.1 Alumina Substrates

Using the analysis methods described in the previous section component temperatures, substrate temperature profiles and overall thermal resistances were calculated and studied for a variety of cases. The first case investigated concerned typical bonding methods for single chips to alumina substrates with an epoxy bonding agent, as shown in Figure 2. This particular chip, 20 X 30 X 5 mils in size, was considered to have 100 milliwatts of thermal energy to be dissipated through the laminate sublayers. As may be noted in Figure 3, the overall thermal resistance between the chip and kovar base is greatly influenced by the size of the epoxy bond. Initially, as the epoxy layer extends beyond the edge of the chip, the thermal resistance decreases until the fin effectiveness of the epoxy becomes insignificant. This indicates that epoxy "squeeze out" is beneficial until the area of the bond layer is approximately 4 times greater than the chip size for the configuration studied. When the epoxy area equals the chip area the thermal resistance was 120°C / watt while at an area ratio of 4 the thermal resistance was found to be 85°C/watt. In each specific case the change in thermal resistance depends upon the ability of the bonding agent to diffuse the thermal energy over a greater area prior to conduction into the substrate. It is this sensitivity of the thermal resistance to squeeze out which sometimes causes quality and temperature reliability problems. That is, circuits which are thought to be identical will have components operating at different temperatures.

MATERIAL	THERMAL CONDUCTIVITY* WATT/MIL-°C**
SILICON	0.0025
GOLD-SILICON EUTECTIC	0.0072
ABELFILM 517 (Al EPOXY)	0.00008
OHMEX SILVER EPOXY	0.0011
GOLD FILLED EPOXY (Au EPOXY)	0.0001
ALUMINA	0.00047
ECCOBOND 99 EPOXY	0.000043
KOVAR	0.00044
MOLYBDENUM	0.00348

* VALUES GIVEN ARE FOR 100°C

** 1 WATT/MIL °C = 2.275×10^{4} BTU/HRFT °F

TABLE 1: MATERIAL THERMAL CONDUCTIVITIES

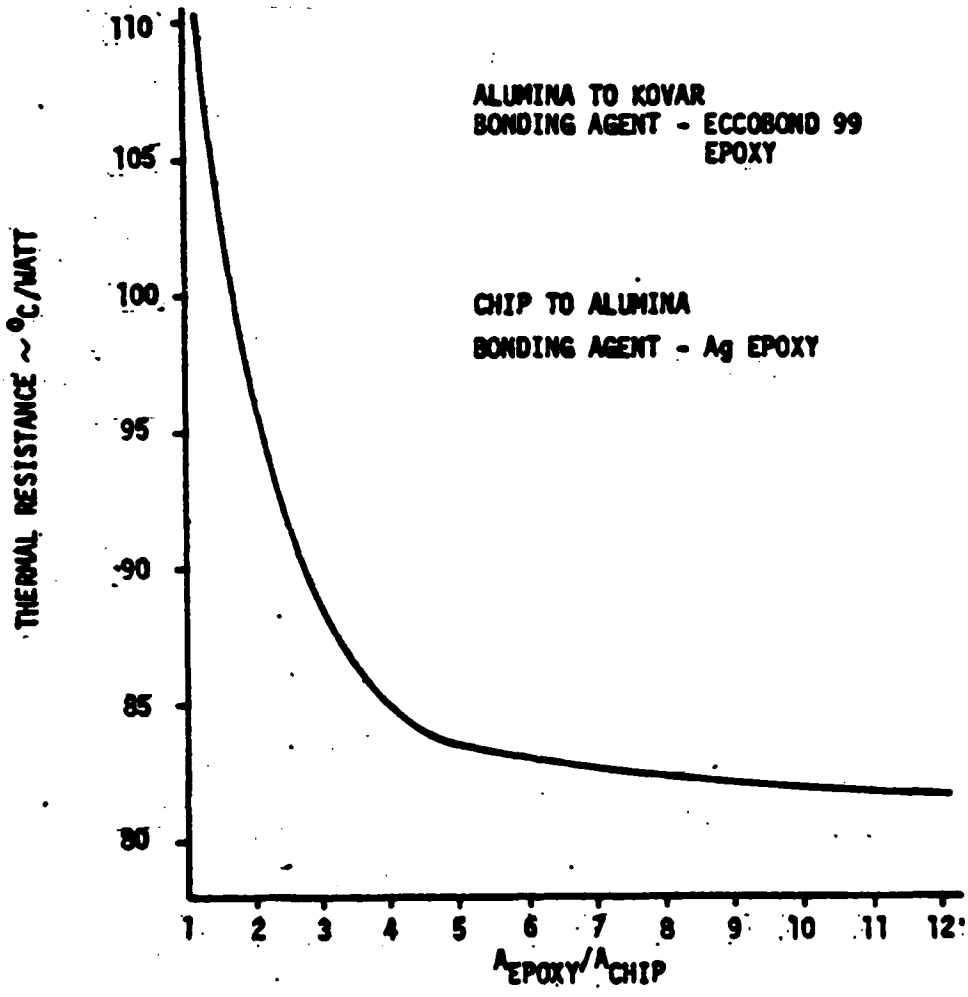


FIGURE 3: THERMAL RESISTANCE FOR 10 X 15 MIL. CHIP WITH EPOXY BONDING AGENT

layers of nodes were utilized. The upper of the two layers contained a single silicon chip, while the lower layer contained an Ohmex-Ag epoxy pad.

The two layers of surface nodes mentioned in the previous paragraph were used to simulate various boundary conditions. That is, by placing nodes on the outer surface convection and radiation boundary conditions could be included. Additionally, the model allowed any number of nodes to be designated as constant temperature nodes, thus fixing their temperature.

Several assumptions, other than those usually required for nodal thermal modeling, were made during the studies. It was assumed that the thermal energy of the various components was dissipated uniformly. Also, thermal energy dissipated by or conducted through the connecting strips was of secondary importance. Additionally, natural convection between the case and the upper substrate surface was negligible. The first assumption could not be validated, however, temperature errors introduced by this assumption would be small due to the relatively high thermal conductivity of the silicon chips in comparison to the substrate ceramic. A comparison of the thermal conductance of metalized strips to that of the adjacent substrate was made and the metalized strips were several orders of magnitude less than through the alumina. Natural convection of dry nitrogen in the small cavity (1 square inch by 0.1 inch) was also found to be negligible. For this case the Grashof number was 31.1 and is too low to be significant for internal convection effects.

Preliminary studies investigating the utility of thermoelectric cooling concepts required modification in the thermal model. That is, a subroutine which incorporated thermoelectric fundamentals was written and applied in terms of sources and sinks at node levels which normally represented the bonding agent between the substrate and Kovar base, Figure (2). Appendix A contains a description of thermoelectric fundamentals and a listing of the subroutine.

Typical temperature profiles for a chip bonded to a laminate are illustrated in Figure 4 and 5. Figure 4 shows the importance of minimizing the thermal resistance of the bonding agent between the alumina and kovar layers. It may be noted that the aluminum filled epoxy in this case tends to act as an insulating layer. Figure 5 shows how the thermal energy diffuses over the top surface of the alumina. In both figures isotherms are shown to depict the effective thermal paths.

Figure 6 shows the effect on base to chip temperature difference for two identical chips mounted on the same substrate. For the case under consideration the chip temperature or thermal resistance decreased as the chips were separated by increasingly greater distances. When the separation was approximately equal to the bonding pad dimension the temperature decreased to nearly the value of a singularly mounted component. This result is greatly influenced by the bonding pad size. Larger bonding pads produce a smaller increase in temperature when mounted close together because of their ability to diffuse the thermal energy. In the case illustrated here, a pad of Ohmex-Ag bonding agent 50 mils X 50 mils would cause only a 3°C increase in temperature for the same spacing criteria in comparison to the 7°C found for the 30 x 30 mil bonding pads.

3.2 Alumina Substrates with Heat Conducting Fluids

The above results indicated that a potentially attractive method for heat removal might be to replace the inert gas which covers the circuit face with a heat conducting fluid. Results for this study are given in Figure (7). As may be noted for typical silicone oil conductivities of 0.5 BTU/hr ft °F the difference between the chip temperature and the base was reduced by approximately 10%. This was not considered to be a significant reduction to warrant the added complexity introduced by such a solution.

3.3 Moly Tabs

A further study was conducted to determine the temperature control aspects of mounting semiconductor devices on moly tabs.* This

*Moly tabs denote Molybdenum mounting pads.

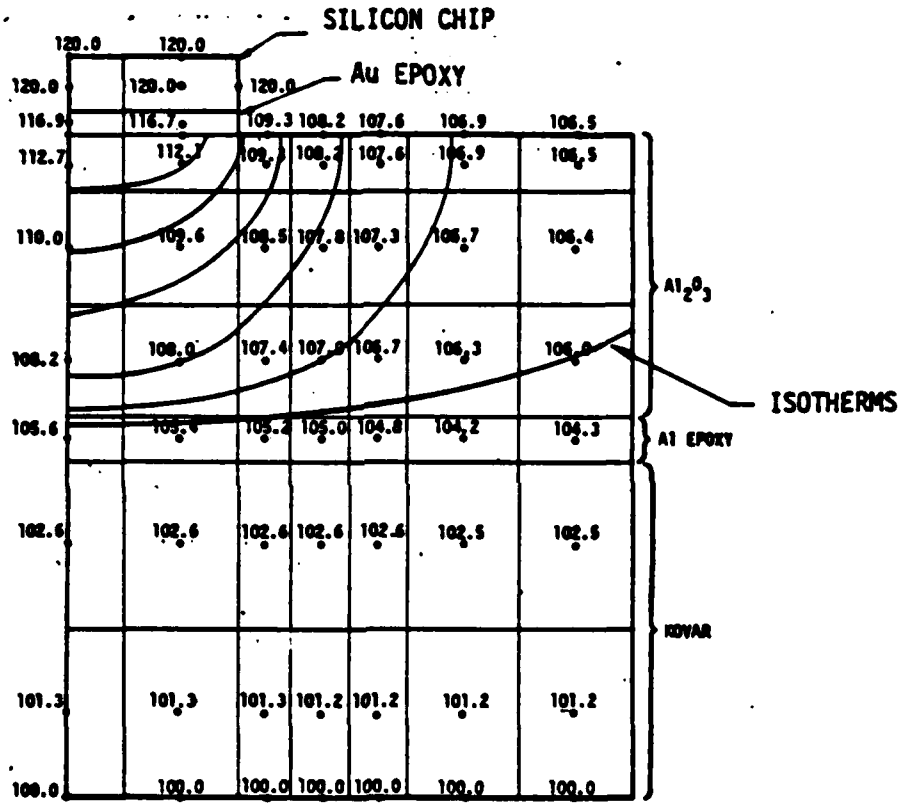


FIGURE 4: TEMPERATURE DISTRIBUTION AT CHIP MID SECTION

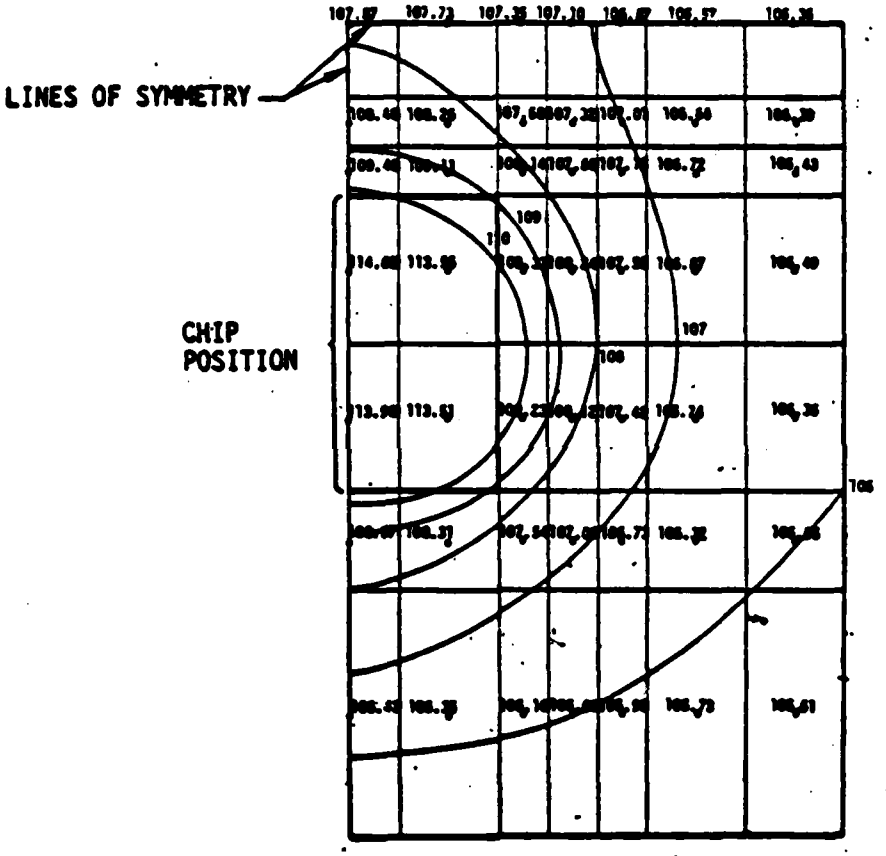


FIGURE 5: TEMPERATURE DISTRIBUTION ALONG SUBSTRATE UPPER SURFACE

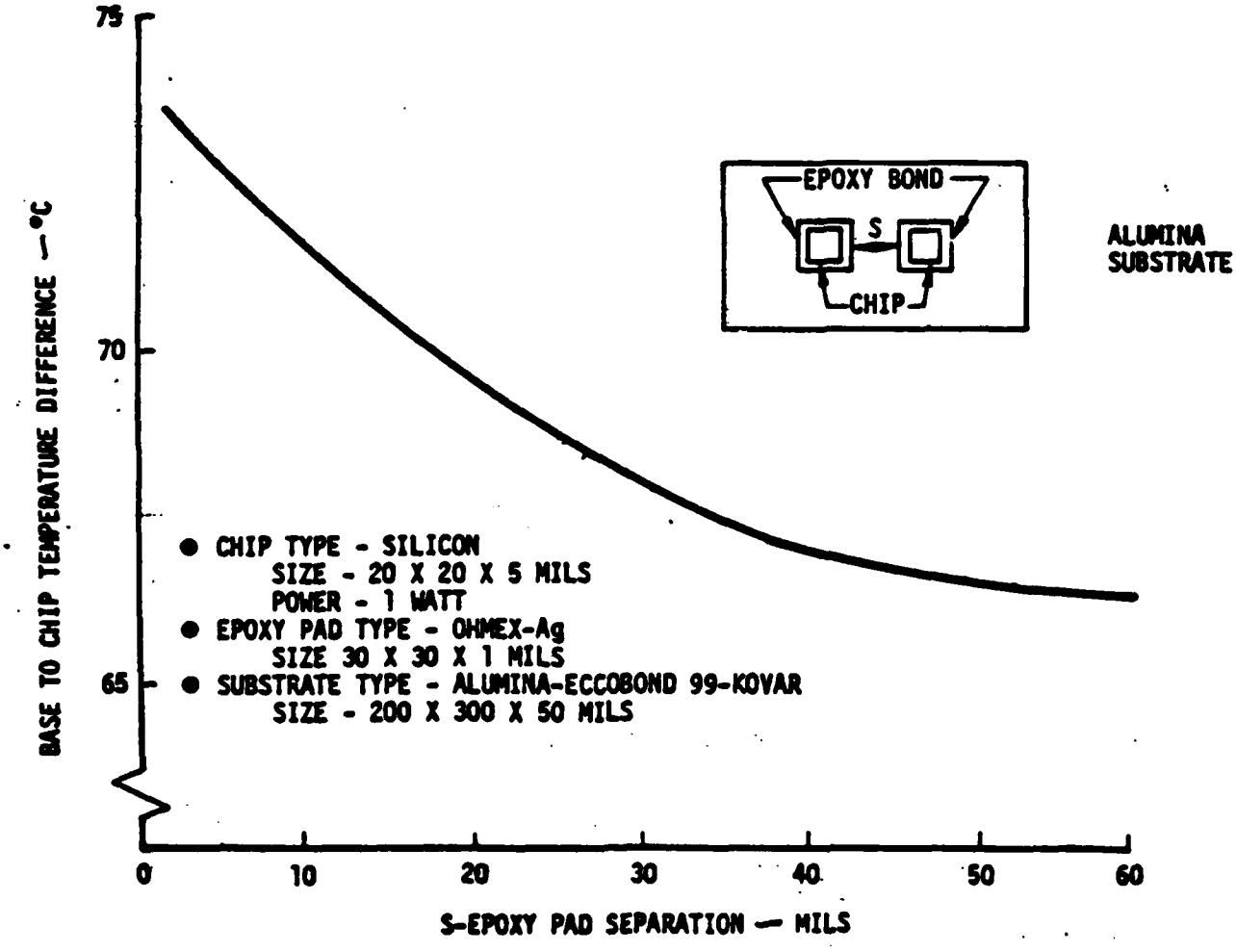


FIGURE 6: EFFECT ON CHIP TO BASE TEMPERATURE DIFFERENCE DUE TO SPACING BETWEEN CHIPS

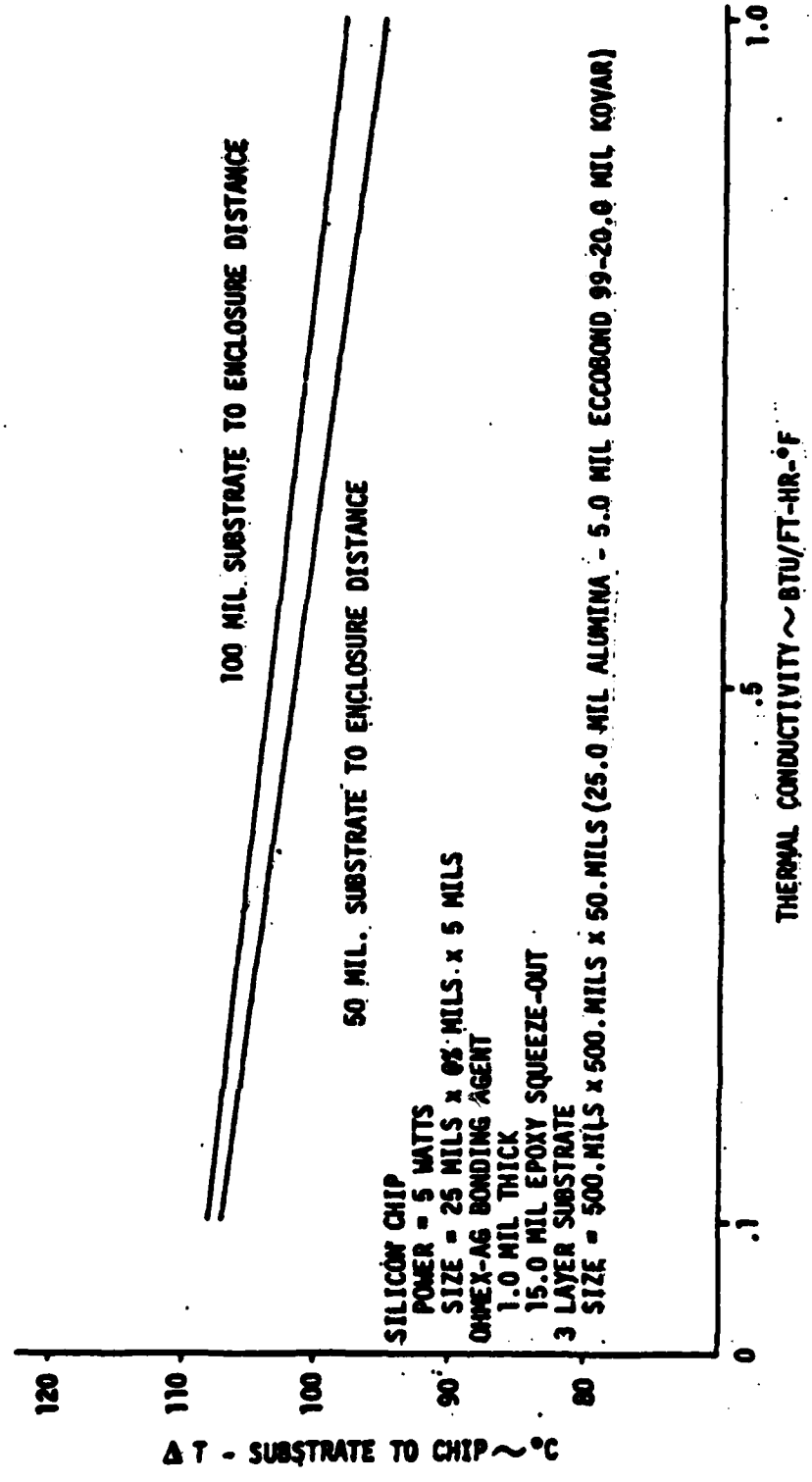


FIGURE 7: SILICON CHIP WITH COOLING OIL

mounting technique which is illustrated in Figure 8 provides an effective reduction in the localized heat flux similar to that achieved by the epoxy squeeze out, only in this case a higher thermal conductivity material which can be pre-sized is utilized. The results for the thermal resistance of the various size chips are given in Figure 9. As may be noted the moly tab tends to diffuse the thermal energy in a manner similar to that of a fin. Initially there is a large effect, but this decreases with an increase in the ratio of the moly tab area to chip area. The computer results were compared with a measured value which was experimentally obtained with a Bendix Thermal Analyzer. The Bendix Thermal Analyzer indicated a thermal resistance of approximately 56°C/watt while the numerical results gave a value of 51°C/watt. The difference between the two values may be due to errors in physical measurements, inaccuracies in thermal conductivities, or due to an unknown thermal resistance at a bond interface.

A multiple component design study of a specific circuit was undertaken to investigate various component mounting methods. The circuit which was analyzed is shown in Figure 10, and a description of the variations considered is listed in Table 2. The component to case temperature differences for the four cases are given in Table 3. As may be noted, the use of the moly tab results in a significant reduction in chip Q_{2B} temperature. The moly tab however increases the temperature of chip Q_{5B} because of the increased thermal conductance between Q_{2B} and Q_{5B}. Table 4 contains the component to case thermal resistance. The significant item shown by this table is the variation in the thermal resistance of chip Q_{5B}. The thermal resistance of this chip is directly influenced by the power dissipated by chip Q_{2B}. Conduction of the thermal energy from Q_{2B} to Q_{5B} determines the resultant temperature of Q_{5B} and thus the thermal resistance. As such, it may be surmized that the use of thermal resistance is not always an indication of a component's thermal performance. That is, low powered chips can appear to have a high thermal resistance

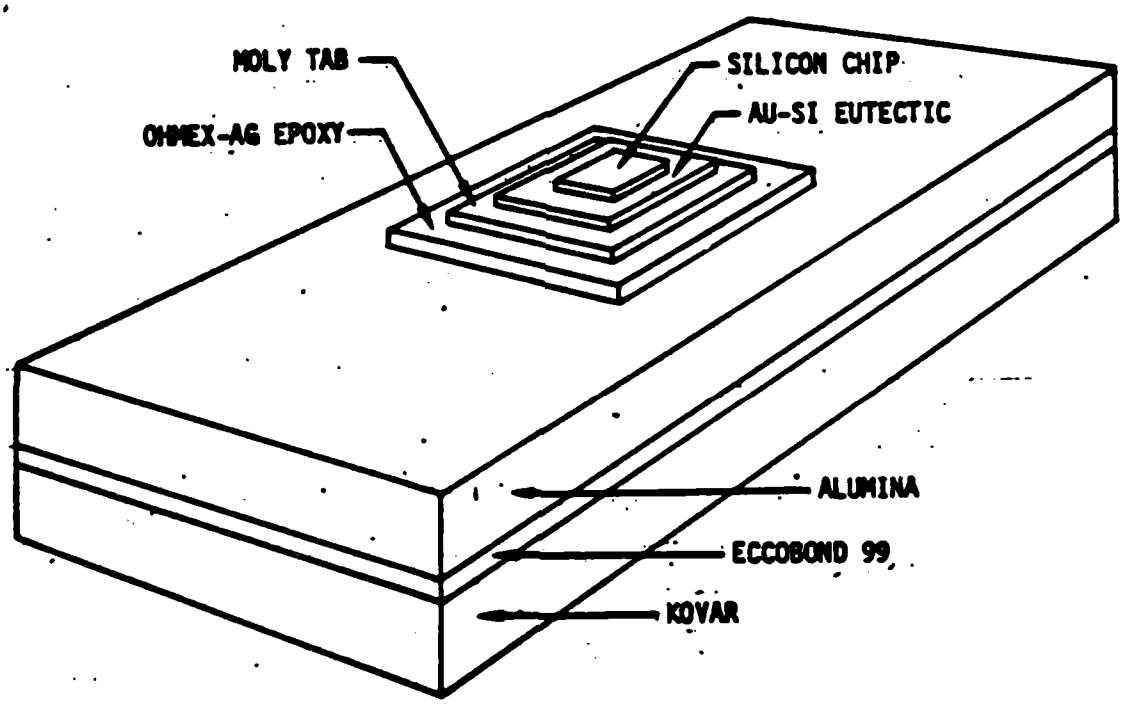


FIGURE 8: SINGLE CHIP WITH MOLY TAB MOUNTING

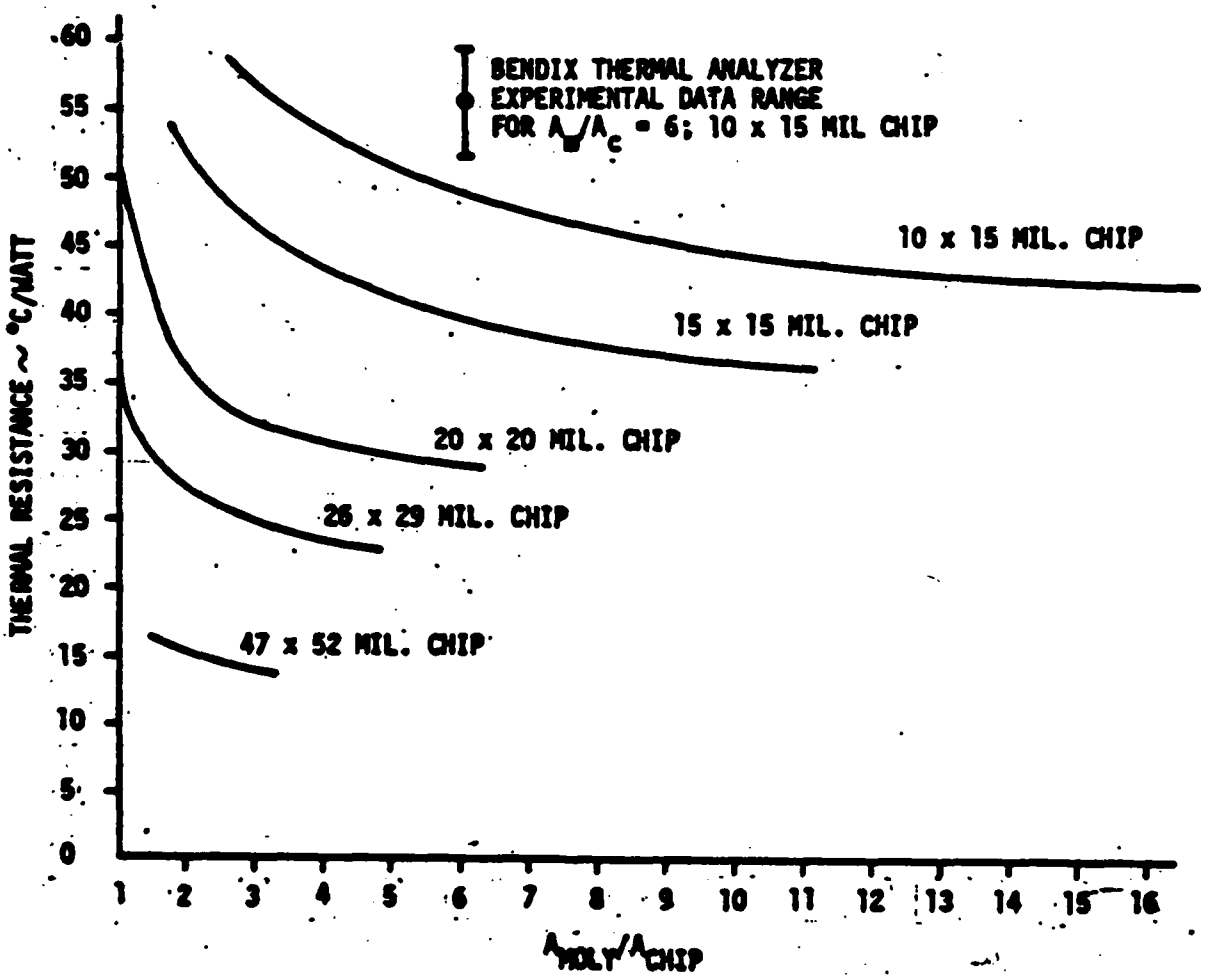


FIGURE 9: THERMAL RESISTANCE OF SILICON CHIPS MOUNTED ON MOLY TABS

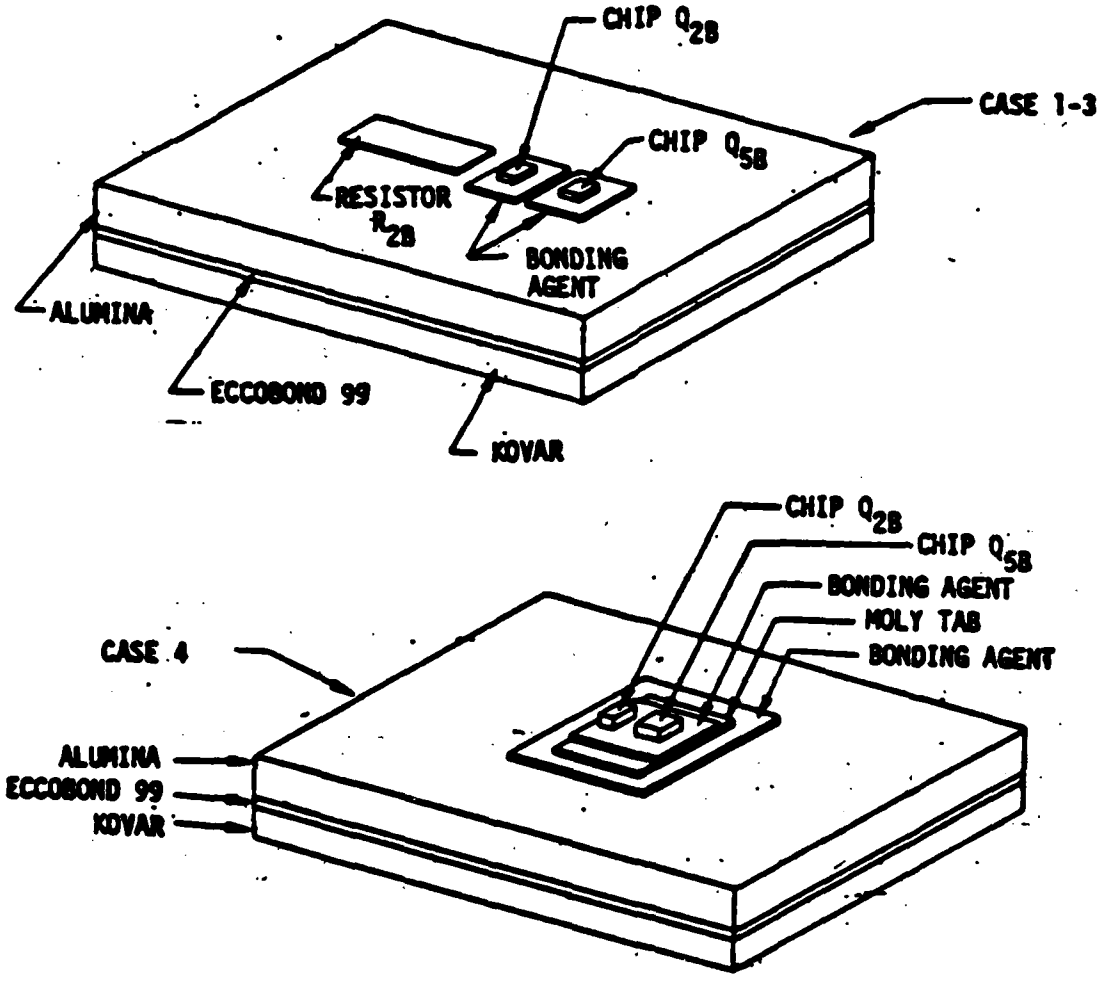


FIGURE 10: MULTIPLE COMPONENT MOUNTING STUDY

PARAMETERS FOR DESIGN STUDY OF MULTIPLE COMPONENT MOUNTINGS

CASE	Q_{2B} POWER MW	Q_{5B} POWER MW	R_{2B} POWER MW	BONDING AGENT
1	635	1	.85	0.0001 IN. AU-SI EUTECTIC
2	635	1	85	0.001 IN. OHMEX-AG EPOXY
3	635	20	85	0.0001 IN. AU-SI EUTECTIC
4	635	1	0	0.0001 IN. AU-SI EUTECTIC FOR CHIP TO MOLY TAB* 0.001 IN. OHMEX-AG EPOXY FOR MOLY TAB TO SUBSTRATE

* MOLY TAB DIMENSIONS .055 X .065 X .005 INCH

TABLE 2

	CASE 1	CASE 2	CASE 3	CASE 4
CHIP Q_{2B}	55.3°C	55.7°C	55.5°C	26.0°C
CHIP Q_{5B}	4.7	6.0	6.1	9.2
RESISTOR R_{2B}	4.5	4.7	4.6	—

TABLE 3: DESIGN STUDY COMPONENT TO CASE TEMPERATURE DIFFERENCE

	CASE 1	CASE 2	CASE 3	CASE 4
CHIP Q_{2B}	87.1	87.7	87.4	40.9
CHIP Q_{5B}	4700	6000	305	9200
RESISTOR R_{2B}	53.3	53.3	53.7	—

TABLE 4: DESIGN STUDY COMPONENT TO CASE THERMAL RESISTANCE $^{o}C/WATT$

when positioned near a high powered chip, while still operating at acceptable temperature levels.

3.4 Beryllia Substrates

A current state of the art technique used to reduce the thermal resistance for high powered solid state elements is to replace the alumina substrate with a beryllia substrate. Beryllia exhibits a thermal conductivity nearly equivalent to aluminum, thus the energy dissipated by the chip is diffused through out the substrate. The results for a beryllia substrate are shown in Figure 11. The chip temperature is then reduced to 113.5°C in comparison to 193°C, for an alumina substrate with the same boundary conditions, Figure 12. Beryllia however is extremely brittle and toxic when being worked. Hence it would be desirable to find another means of reducing the thermal resistance.

3.5 Alumina Substrates with Integrated Heat Pipe Cooling

The utility of using heat conducting fluids over microcircuits was found to be ineffective (Section 3.2). It was then suggested that an integrated heat pipe cooling concept might be able to reduce the chip operating temperature and decrease thermal cycling effects. To investigate this cooling technique various concepts were studied. Figures 13 to 15 contain illustrations of the concepts, thermo physical properties and results. Figure 13 depicts a single chip covered by a 5 mil wick saturated with a fluorocarbon fluid. The chip acts as the evaporator and the surrounding area and cover form the condenser. This scheme reduces the chip temperature from 193°C to 177.5°C. Thus, this method is not as effective as the moly tab mountings. If the wick thermal conductance could be increased by an order of magnitude then the chip would be cooled to 132.5°C. A combined moly tab heat pipe concept, Figure 15, reduced the chip temperature to 152.7°C. Comparisons between this concept and moly tab mounts indicates that the integrated heat pipe technique does not offer any significant advantage.

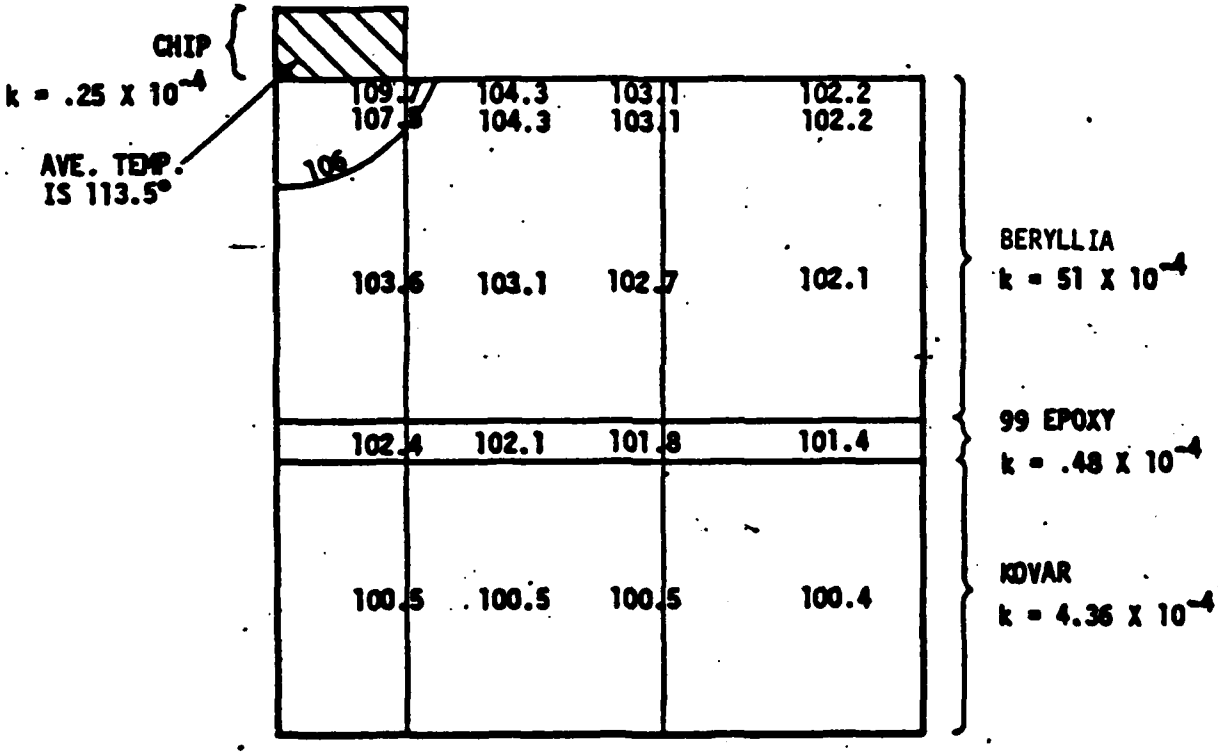


FIGURE 11: MICROCIRCUIT WITH BERYLLIA SUBSTRATE

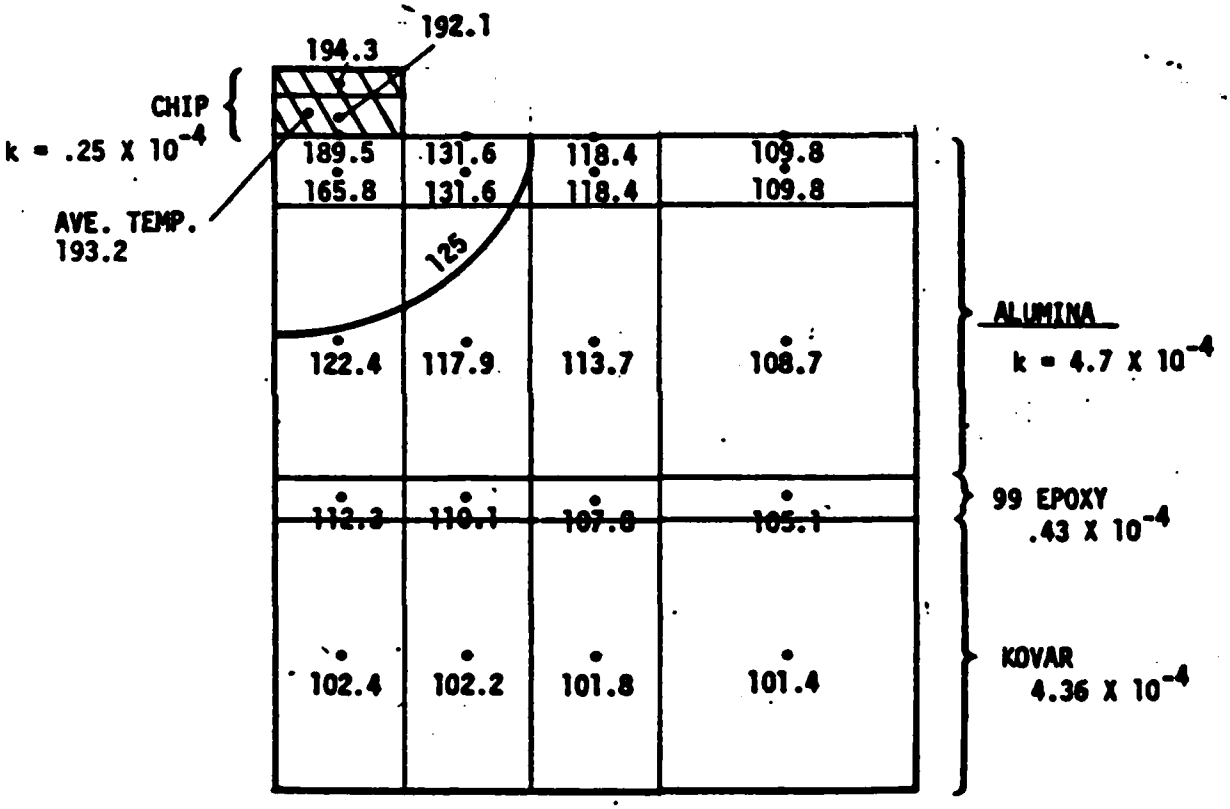


FIGURE 12: ISOTHERMS FOR MICROCIRCUIT ALUMINA SUBSTRATE

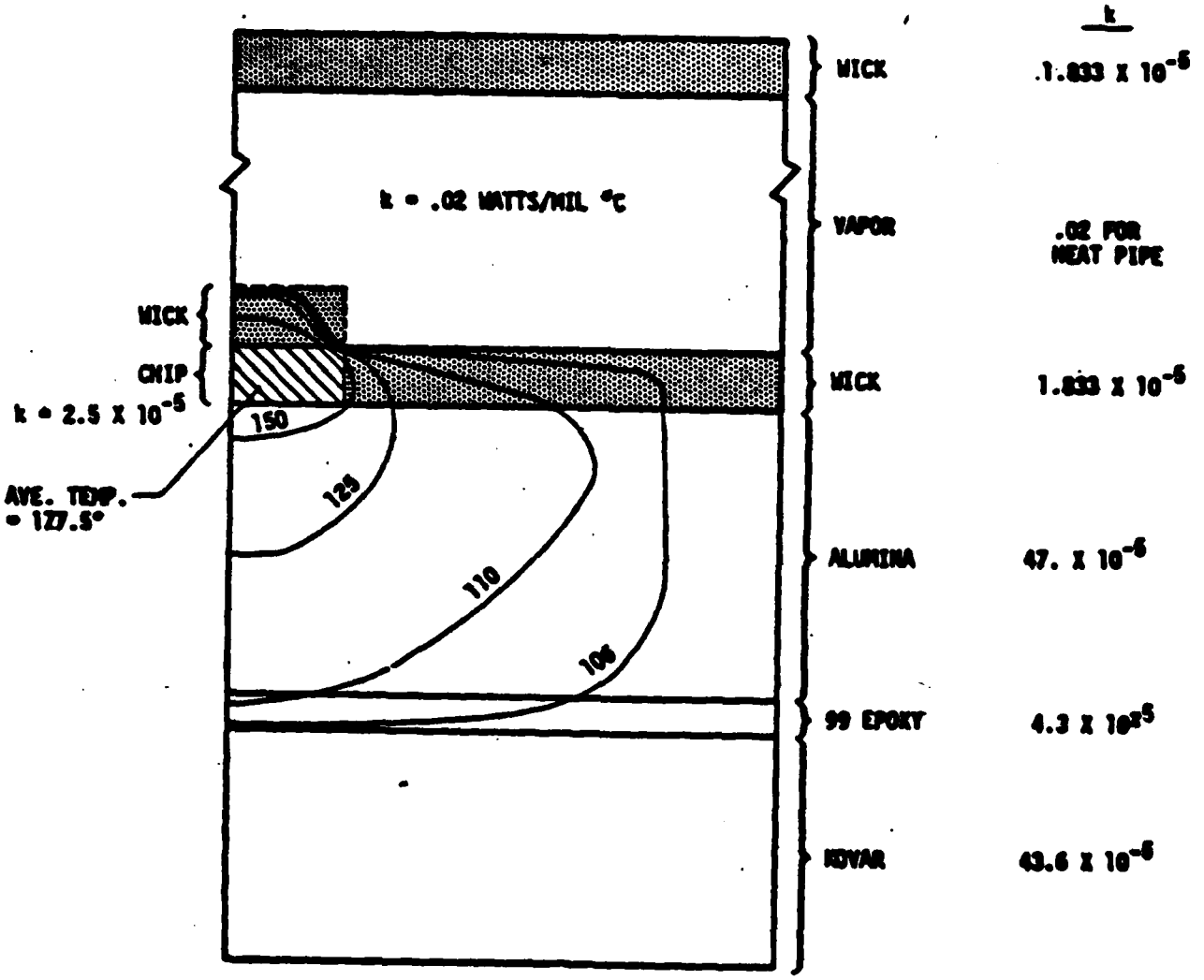


FIGURE 13: ISOTHERMS FOR MICROCIRCUIT WITH HEAT PIPE

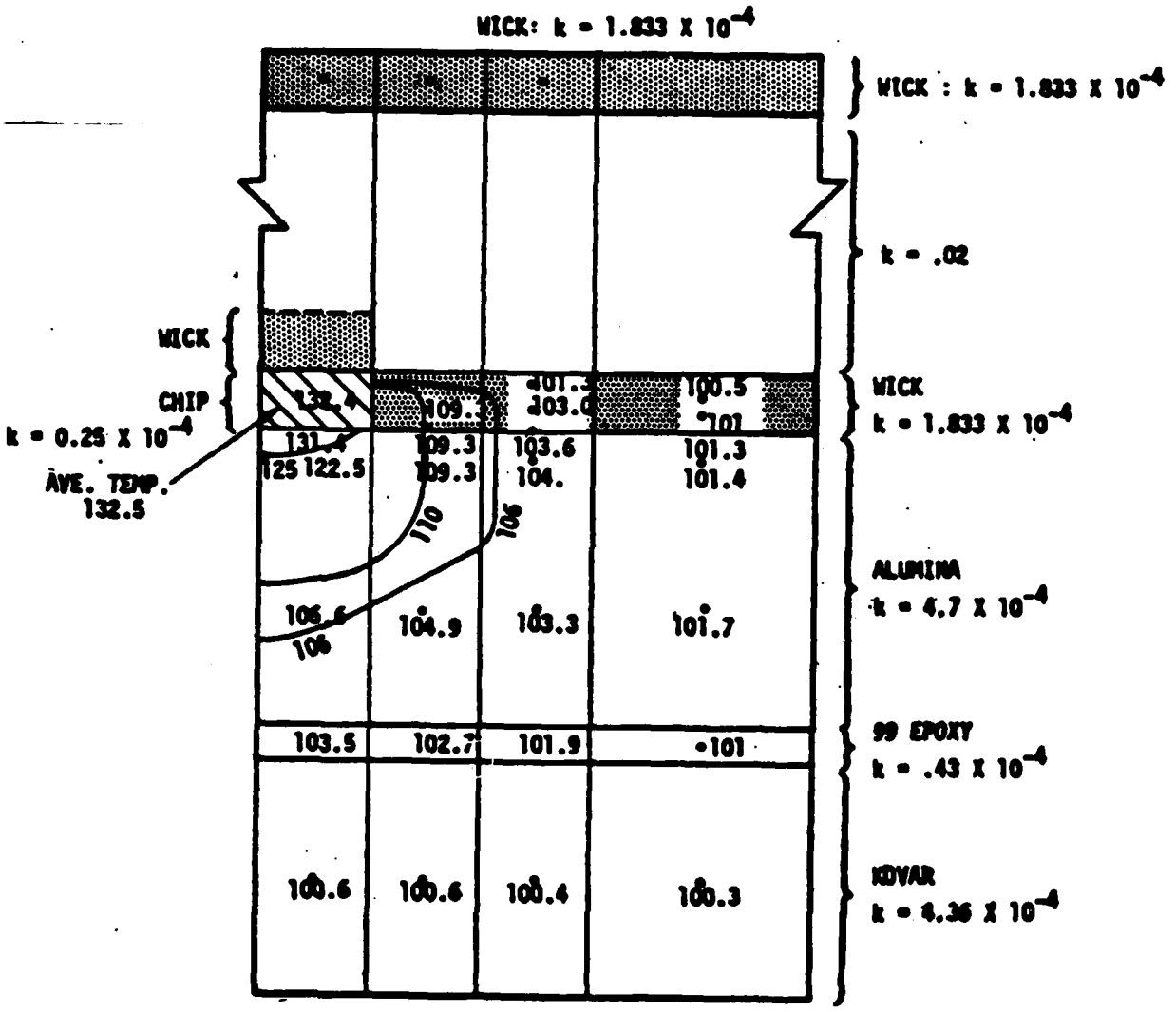


FIGURE 14: ISOTHERMS FOR MICROCIRCUIT WITH HEAT PIPE

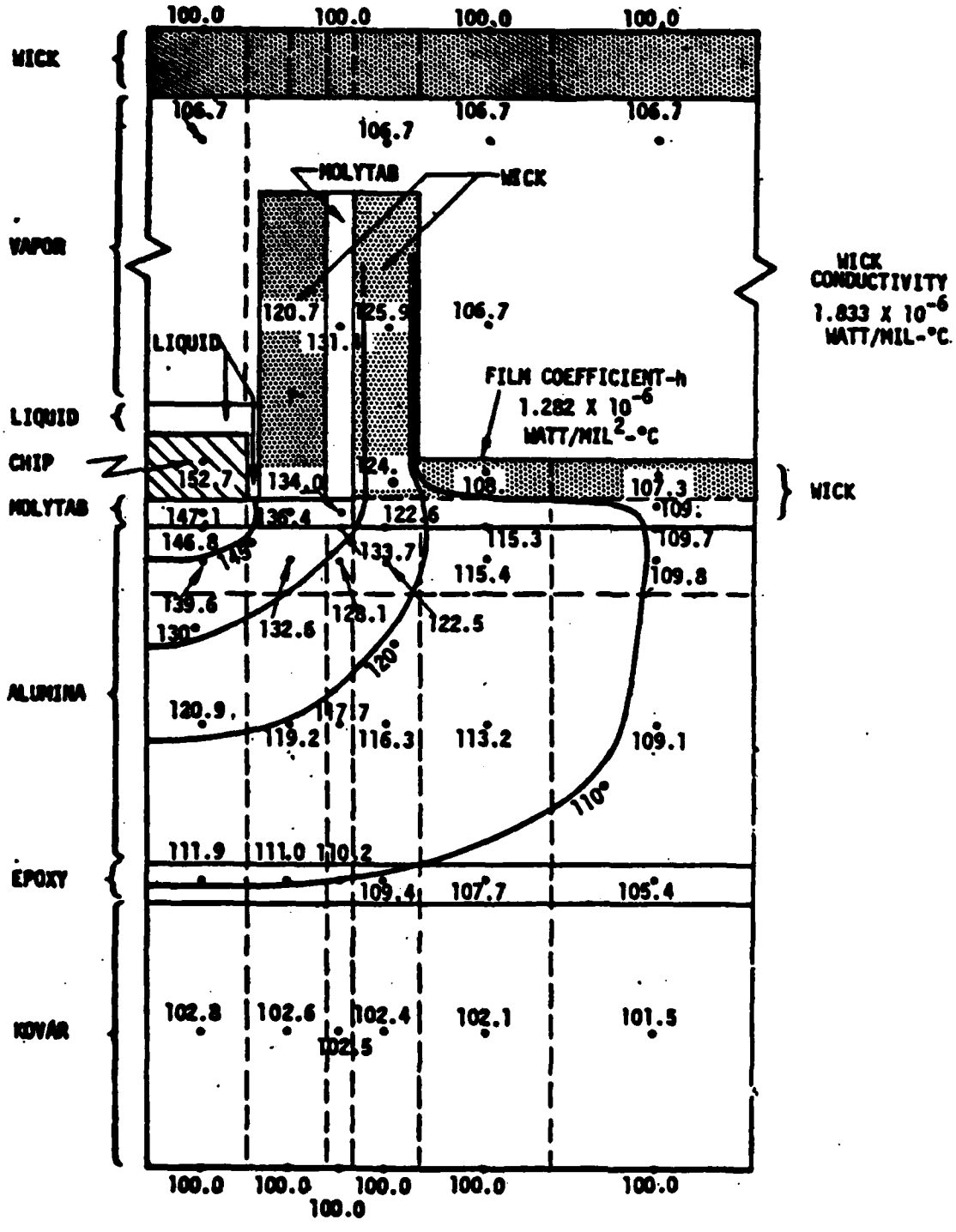


FIGURE 15: MICROCIRCUIT WITH HEAT PIPE

3.6 Alumina Substrate with Sputtered Beryllia

Another technique for diffusing the large localized heat flux dissipated within a solid state element is shown in Figure 16. This concept is similar to moly tab mounts wherein the beryllia acts as a thermal fin to reduce the heat flux incident to the alumina substrate. The results for two variations of sputtered beryllia are given in Figures 17 and 18. The chip temperature has been reduced significantly and this concept compares favorably with moly tab mounts and beryllia substrates techniques.

3.7 Thermoelectric Cooling

It has been proposed that for Large Scale Integration (LSI) electronic modules that thermoelectric coolers be applied to reduce solid state element temperatures, Figure 19. Two concepts were analyzed to examine this cooling technique, a single chip mounted on an alumina substrate and one using a beryllia substrate. The thermoelectric geometric configuration and materials are shown in Figure 20. Results for the computation are given in Figures 21 and 22. The chip temperature was reduced to 102.7 and 74.5°C respectively. This technique offers significant advantages in temperature control, however the COP for the coolers is approximately (.37). That is, for each watt of cooling (2.69) watts of electrical energy are required to operate the coolers.

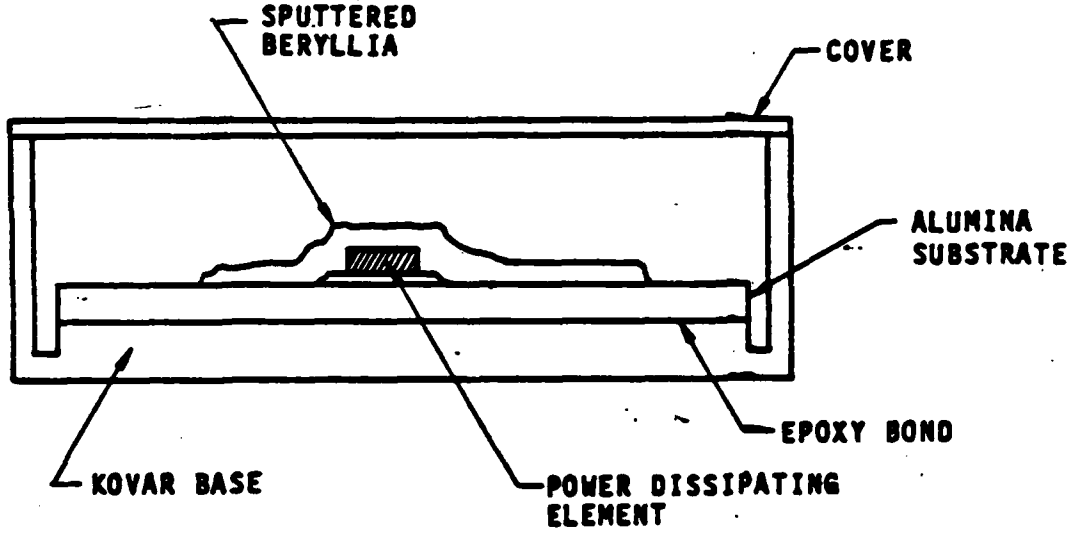
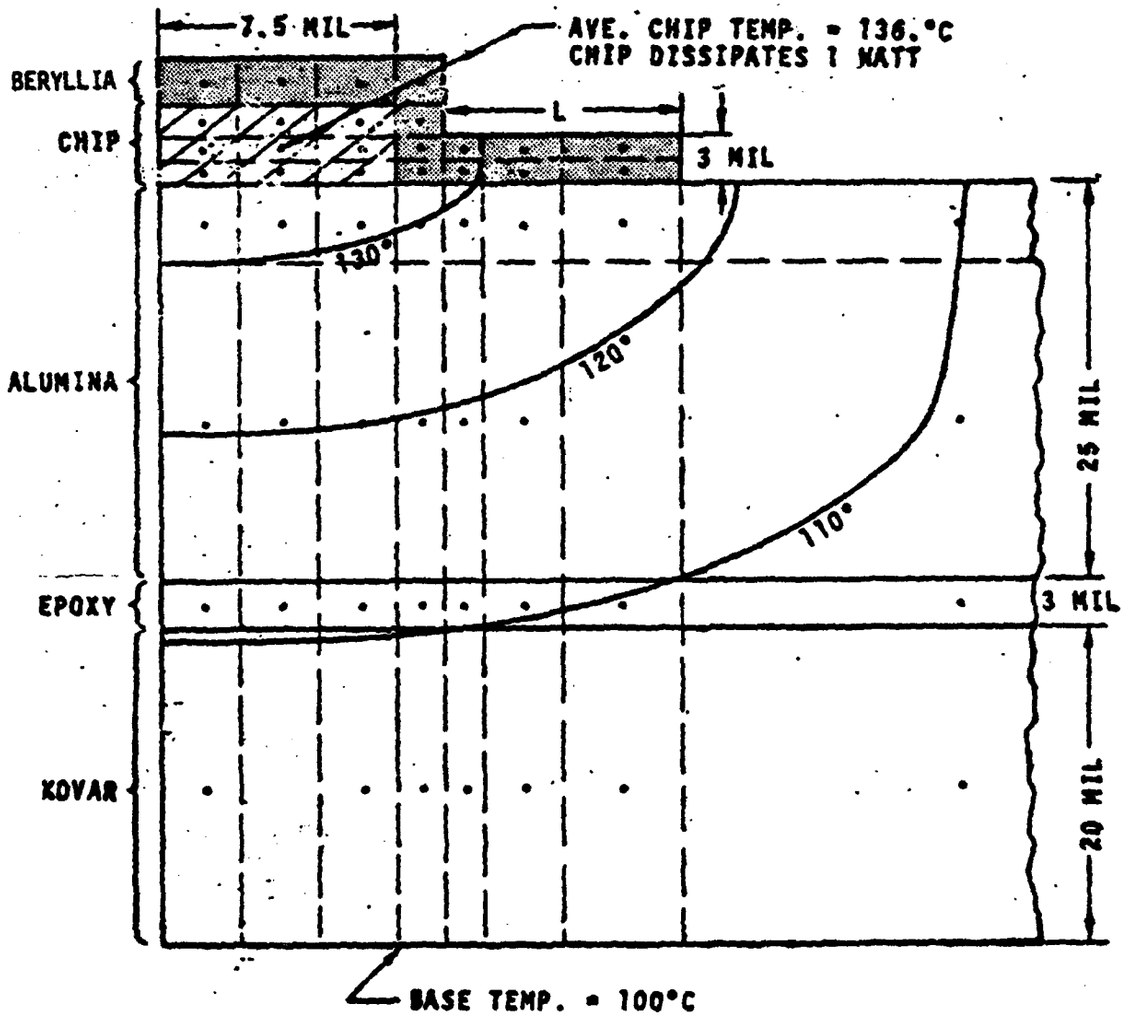


FIGURE 16: BERYLLIA SPUTTERED/THERMOELECTRIC COOLED ELEMENT



SCALE: 1 CM = 4 MIL

FIGURE 17: ISOTHERM PLOT FOR MICROCIRCUIT WITH BERYLLIA SPUTTERED OVER TOP SURFACE AND WITH L = 15 MIL

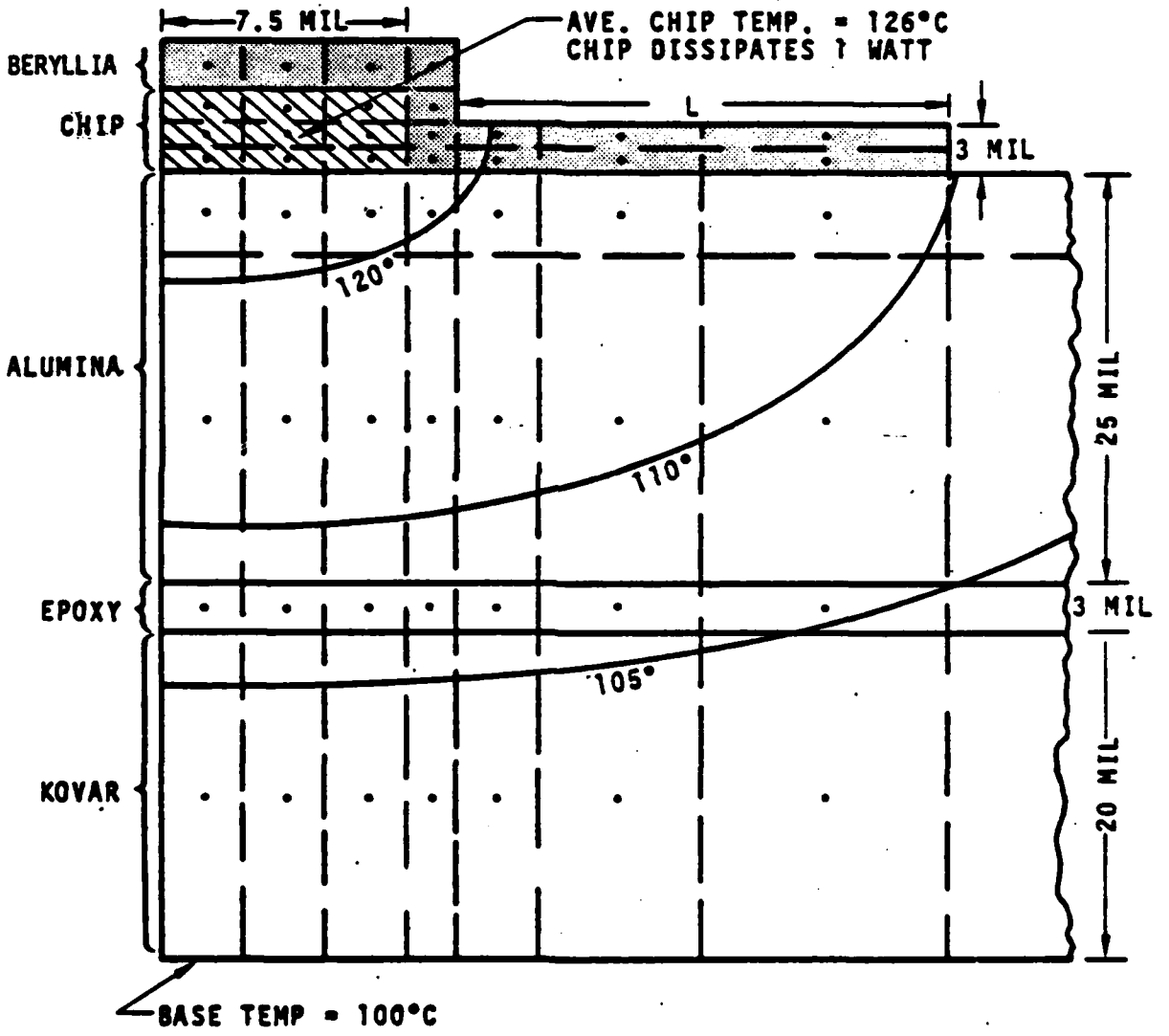


FIGURE 18: ISOTHERM PLOT FOR MICROCIRCUIT WITH BERYLLIA SPUTTERED OVER TOP SURFACE AND WITH L = 30 MIL

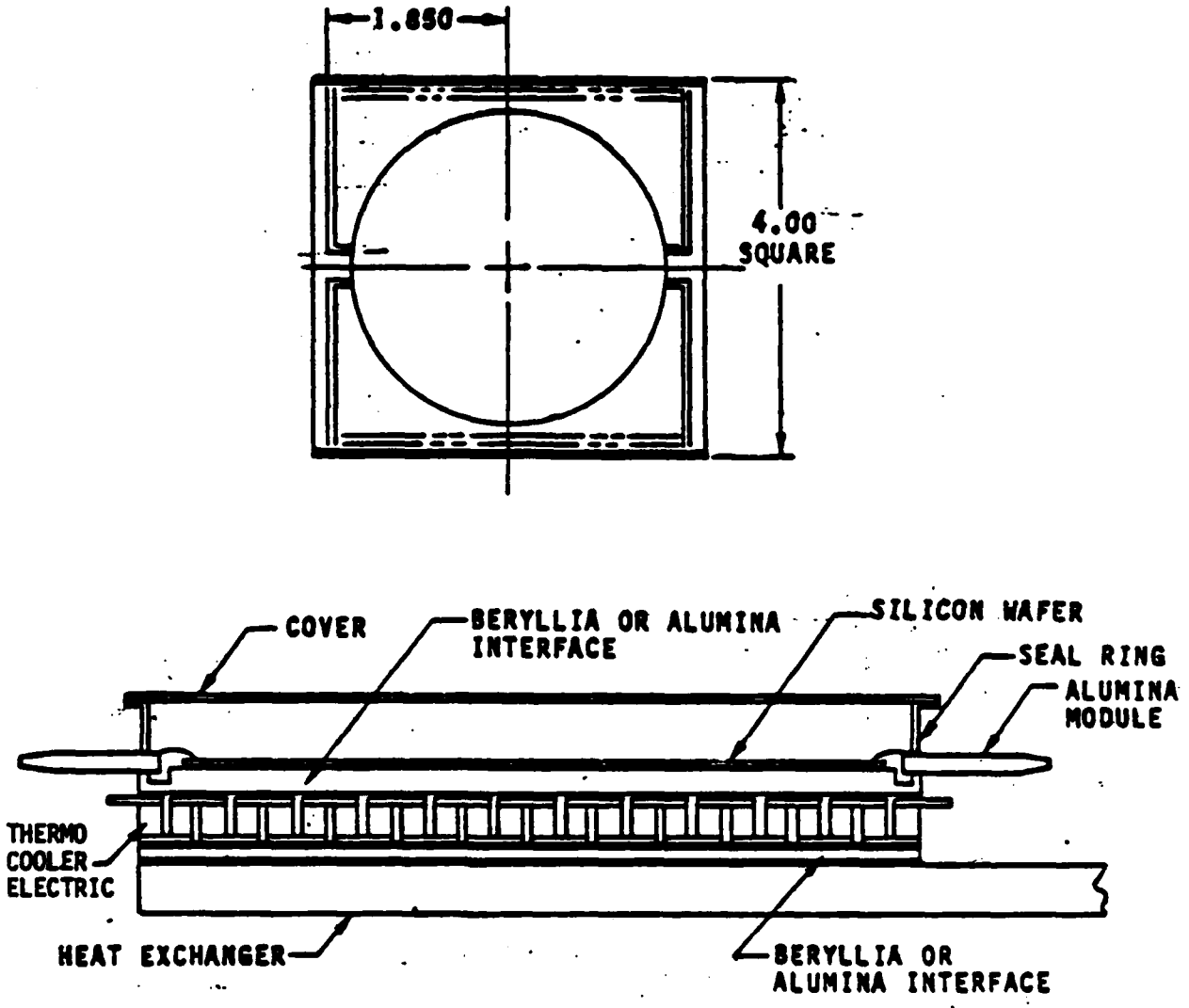


FIGURE 19: THERMOELECTRIC COOLED LSI MODULE

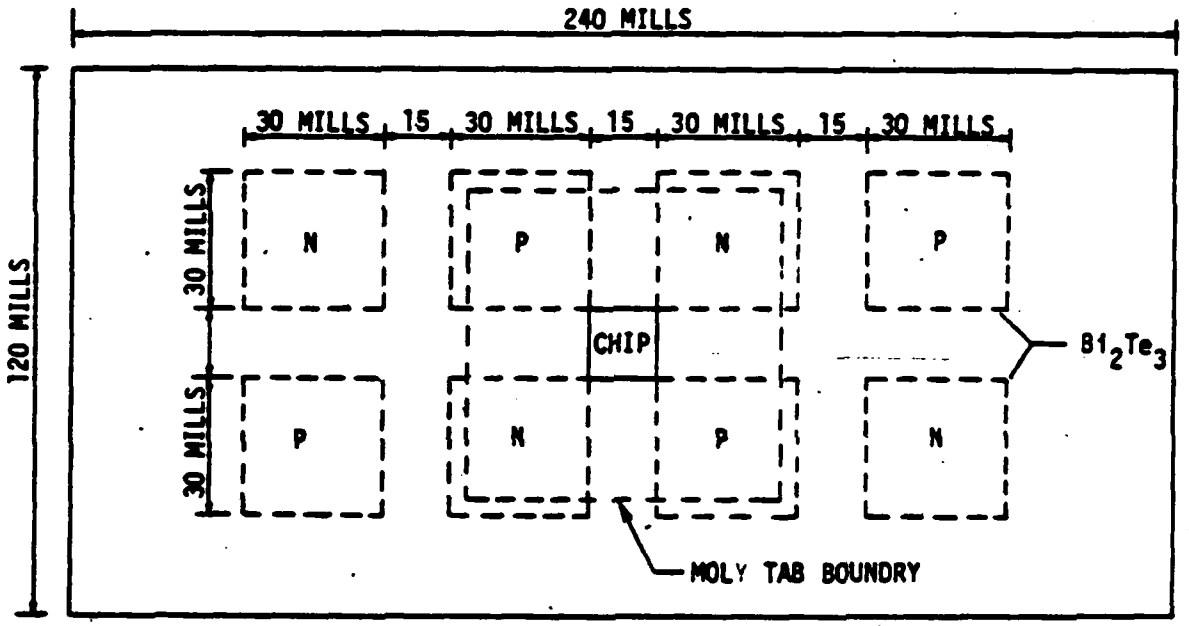


FIGURE 20: THERMOELECTRIC COOLED MICROCIRCUIT

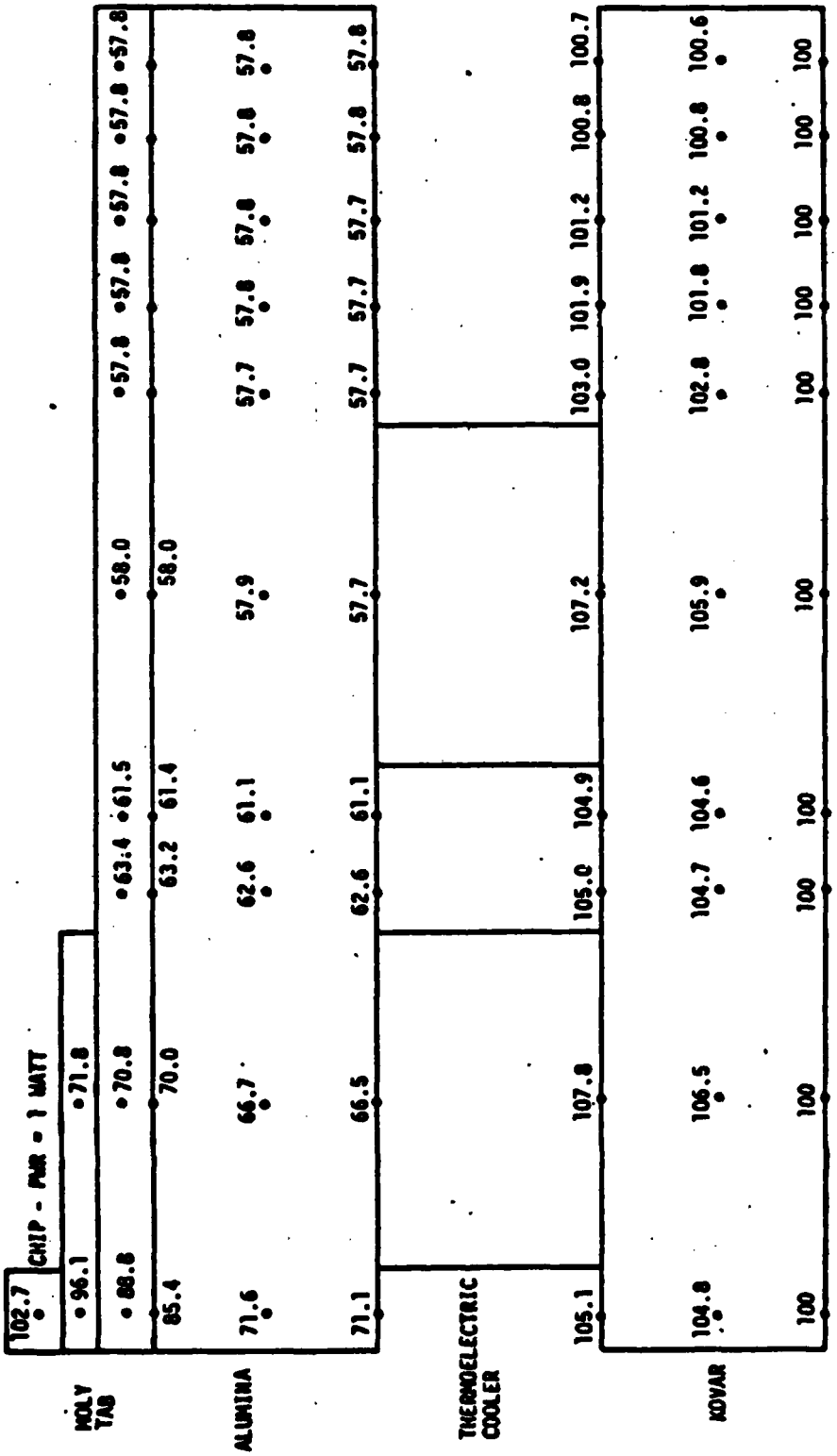


FIGURE 21: MICROCIRCUIT WITH THERMOELECTRIC COOLER - ALUMINA SUBSTRATE

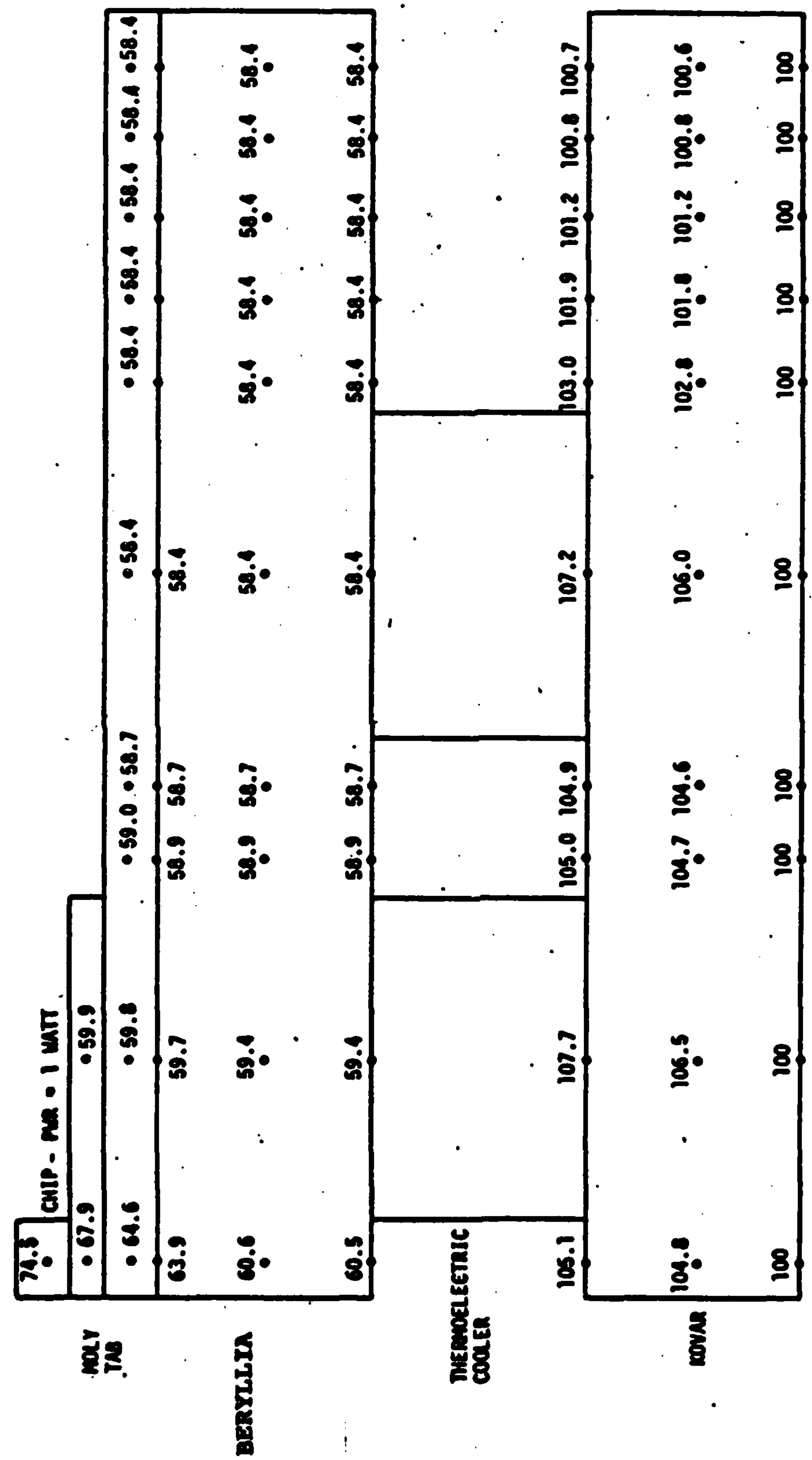


FIGURE 22: MICROCIRCUIT WITH THERMOELECTRIC COOLER - BERYLLIA SUBSTRATE

4.0 CONCLUDING REMARKS

The numerical results described in the previous section illustrates the utility of thermal models in predicting component temperatures and in aiding the engineer during initial design phases. Various trade studies can be completed rapidly allowing the placement of high powered components in regions where they will have minimal effect on surrounding devices. Additionally, different mounting and thermal control techniques can be compared in an effort to chosse those offering the best temperature control.

It was found that epoxy "squeeze out" can be beneficial in reducing the component temperatures. However epoxy squeeze out is difficult to control and thus when relied upon for temperature control can cause circuits to vary widely in maximum component temperatures. The use of moly tabs and sputtered beryllia resulted in significant reductions in component temperature levels. Additionally, it was shown that the integrated heat pipe cooling concept does not provide effective temperature control.

Thermoelectric coolers appear to offer a promising technique for controlling LSI module temperatures. This method however, requires the expenditures of significant electrical energy for the coolers to operate.

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APPENDIX

Fundamentals of Thermoelectric Cooling

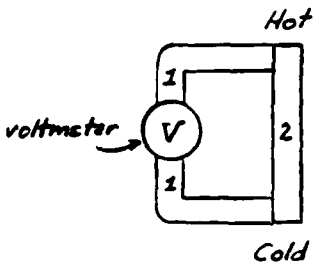
These effects are associated with the thermoelectric effect:

Seebeck

Thomsen

Peltier

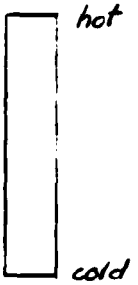
Sometimes Joulean heating (i^2R) is included as a thermoelectric effect, but due to its widespread occurence it is not customary to include it as a special and unique phenomenon.



The Seebeck effect occurs when 2 conductors are connected in a circuit with their junctions at different temperatures. Higher temperatures cause more electrons to populate states above the Fermi energy level. Their mobility is increased, and a diffusion to the cold end occurs. With more electrons at the cold end than at the hot end, an electrical potential is set up. If material 1 is the same as material 2, the same condition is set up in each, and there is no net effect. If the materials are dissimilar, the excitation to higher energy levels is different in each, and a net voltage results. This effect gives rise to the "thermocouple effect". The Seebeck effect is described by the Seebeck coefficient, α, such that

$$\alpha_{12} = \frac{dE_{12}}{dT} = \frac{dE_1}{dT} - \frac{dE_2}{dT} = \alpha_1 - \alpha_2$$

E_{12} is called the Seebeck potential or voltage.



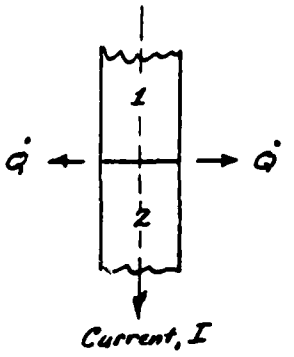
The Thomson effect occurs when a conductor is subjected to a thermal gradient. In such a conductor electrons would migrate to the cold end. If a voltage is imposed, the electrons are forced to move in the direction of the potential. In the case where electrons move from hot to cold, electrons give up energy as heat. If the electrons are forced to move in the opposite direction, i.e., from cold to hot, they add to their thermal energy state by absorption of heat. The Thomson effect is described by the

Thomson coefficient, τ, by

$$\dot{Q}_{(Thomson)} = \tau I \frac{dT}{dx}$$

where Q is the rate of thermal energy absorption or emission, I is the current, and dT/dX is the temperature gradient. In this case Q is positive when added for +I in the +X direction.

The Peltier effect is the reverse of the Seebeck effect in the sense that the transformations of energy are basically caused by the same phenomenon. Electrons convert kinetic to potential energy and vice versa, and their stored potential energy depends on these environments, i.e., the material containing them. Therefore as electrons move from material 1 to 2 they take up or release energy according to the capacity of the combined state to store potential energy. The Peltier effect is described by the Peltier coefficient, π_{12} (or ϕ_{12})



$$\dot{Q} = \pi_{12} I \quad \text{or} \quad \dot{Q} = \phi_{12} I$$

Classical thermodynamics has established relations among the 3 coefficients

$$\pi_{12} \text{ or } \phi_{12} = \alpha_{12} T$$

$$\& \quad \tau_{12} = T \frac{d(\alpha_{12})}{dT}$$

The analysis of thermoelectric cooling systems must include the irreversible effects of heat conduction and Joulean heating. These 2 can be described by the relations

$$\text{conduction}, \quad \dot{Q}_c = U(T_1 - T_0)$$

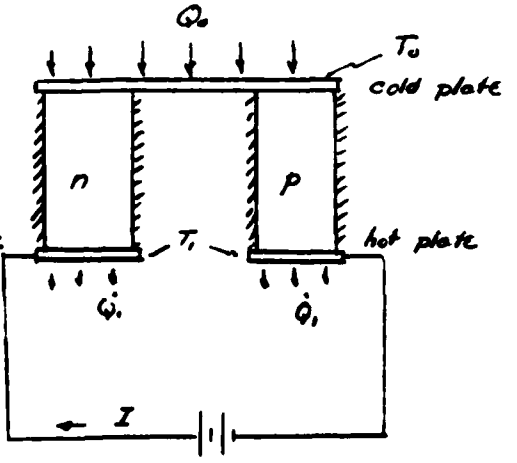
where U is an overall conduction coefficient, T_1 refers to the hot temperature, and T_0 refers to the cold or source temperature.

$$\text{joulean heating}, \quad \dot{Q}_j = I^2 R$$

where R is the electrical resistance.

Consider a thermoelectric system consisting of a material which has a positive Seebeck coefficient (p) and a material which has a negative coefficient (n). All 5 effects occur in this system:

- Peltier cooling
- Thompson heating
- heat conduction
- Seebeck voltage
- Joulean heating



The relation $\tau_{12} = T \, d\alpha_{12}/dT$ shows that if the Seebeck coefficient is constant, the Thomson coefficient is zero. It has been shown that taking an average value of α does account for moderate Thomson heating effects.

Also, it is customary to assume that 1/2 the Joulean heating goes to each plate. Therefore

$$Q_0 = \alpha_{pn} T_0 I - U(T_1 - T_0) - \tfrac{1}{2} I^2 R$$

$$\text{&} \qquad Q_1 = \alpha_{pn} T_1 I - U(T_1 - T_0) - \tfrac{1}{2} I^2 R$$

where the equivalence $\pi_{pn} = \alpha_{pn} T$ has been used.

or rearranging Q_0

$$T_1 - T_0 = \frac{\alpha_{pn} T_0 I - \frac{1}{2} I^2 R - Q_0}{U}$$

The power required to obtain this refrigerating effect is due to the Seebeck voltage and Joulean heating

$$W = \left[\alpha_{pn} (T_1 - T_0)\right] I + I^2 R$$

The coefficient of performance, C.O.P. is defined as Q_0/W

$$\therefore \quad C.O.P. = \frac{\alpha_{pn} T_0 I - U(T_1 - T_0) - \frac{1}{2} I^2 R}{\alpha_{pn} (T_1 - T_0) I + I^2 R}$$

This is compared to a Carnot cycle where the irreversible effects are absent i.e. $U = 0$ & $R = 0$

$$(C.O.P.)_{Carnot} = \frac{T_0}{T_1 - T_0}$$

Optimizing the system for Q_0 or $T_1 - T_0$ with respect to current results in

$$I_{opt} = \frac{\alpha_{pn} T_0}{R}$$

Also if we set $Q_0 = 0$ for the maximum $(T_1 - T_0)$ and use the optimum current

$$T_1 - T_0 = \frac{1}{U}\left(\alpha_{pn} T_0 I - \tfrac{1}{2} I^2 R\right) = \frac{1}{U}\left(\alpha_{pn} T_0 \frac{\alpha_{pn} T_0}{R} - \frac{1}{2} \frac{\alpha_{pn}^2 T_0^2}{R^2} R\right)$$

$$\text{or} \quad (T_1 - T_0)_{max.} = \frac{\alpha_{pn}^2 T_0^2}{2UR}$$

The "figure of merit" is defined as $Z \equiv \frac{\alpha_{pn}^2}{UR}$ such that

$$(T_1 - T_0)_{max} = \frac{Z}{2} T_0^2$$

Z is a function of material properties and typical values are given in the table below

Material	Z 1/°K
Chromel-constantan	0.0001
Sb-Bi	.00018
Sb-(91% Bi, 9% Sb)	.00023
ZnSb - Constantan	.0005
PbTe (p type) - PbTe(ntype)	.0013
Bi_2Te_3(p)-Bi_2 Te_3 (n)	.002
p-n Alloy Thermocouple	
(50% Bi_2Te_3, 50% Sb_2Te_3)	.0025
(75% Bi_2Te_3, 25% Bi_2Se_3 + minor $CuBr_2$ added)	.0025

For the above values of Z, U = k, thermal conductivity, and R = , electrical resistivity.

To optimize C.O.P. with respect to current, $\frac{\partial(C.O.P)}{\partial I} = 0$

$$\frac{\partial(C.O.P)}{\partial I} = \frac{(\alpha T_0 - IR)(\alpha \Delta T I + I^2 R) - (\alpha T_0 I - U\Delta T - \frac{1}{2} I^2 R)(\alpha \Delta T + 2IR)}{(\alpha_{pn}(T_1 - T_0) I + I^2 R)^2} = 0$$

multiplying out and collecting terms

$$I^2 (R\alpha T_0 + \frac{\alpha}{2} \Delta T R) - (2 U R \Delta T) I - U \alpha \Delta T^2 = 0$$

After some arithmetic, solving the quandrtic, and using the definition of Z

$$I = \frac{\alpha \Delta T (1 \pm \sqrt{1 + Z T_m})}{R Z T_m} \quad \text{where} \quad T_m = \frac{T_1 + T_0}{2}$$

The + sign applies and multiply by $(1 - \sqrt{1+ZT_m})$

$$I = \frac{\alpha \Delta T}{R Z T_m} \frac{(1 + \sqrt{1+ZT_m})(1 - \sqrt{1+ZT_m})}{(1 - \sqrt{1+ZT_m})}$$

$$I_{opt} = \frac{\alpha \Delta T}{R} \frac{1}{(\sqrt{1+ZT_m} - 1)} \quad \text{where} \quad T_m = \frac{T_1 + T_0}{2}$$

Straightforward substitution of I_{opt} into the above equation for C.O.P. yields the maximum C.O.P. *i.e. c.o.p. for I_{opt}*

$$(c.o.p)_{max} = \frac{\frac{T_0}{T_1 - T_0}\left(\sqrt{1+Z\bar{T}_m} - \frac{T_1}{T_0}\right)}{\sqrt{1+Z\bar{T}_m} + 1}$$

$(C.O.P.)_{max}$ and $(T_1 - T_0)_{max}$ are plotted on the next page for $T_1 = 300°K$ and various values of Z.

Summary:

$$I_{opt} = \frac{\alpha_{pn}\,\Delta T}{R\left(\sqrt{1+Z\bar{T}_m} - 1\right)} = \frac{V_{opt}}{R}$$

$$(C.O.P.)_{max} = \frac{\frac{T_0}{\Delta T}\left(\sqrt{1+Z\bar{T}_m} - \frac{T_1}{T_0}\right)}{\sqrt{1+Z\bar{T}_m} + 1}$$

} for max. c.o.p.

$$I_{opt.} = \frac{\alpha_{pn} T_0}{R}$$

$$(T - T_0)_{max} = \frac{1}{2} Z T_0^2 \quad \text{(no load)}$$

$$(Q_0)_{max} = U\left[\frac{Z T_0^2}{2} - (T_1 - T_0)\right]$$

} for max. ΔT or max. Q

Note that an estimate of Z can be made by running at "no load" and measuring T & T_0. The above expressions are for a specific value of $Z = \alpha_{pn}^2/RU$, but R and U involve geometry which may be optimized for performance. Consider U, the overall conduction path

$$U = k_n \frac{A_n}{L_n} + k_p \frac{A_p}{L_p} = k_n \gamma_n + k_p \gamma_p$$

where A = area, L = length, & $\gamma = A/L$

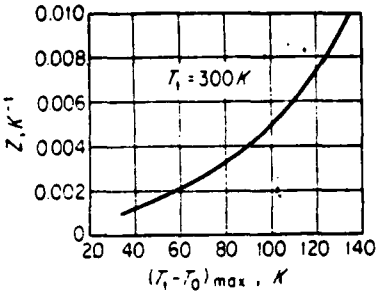
Also

$$R = \rho_n/\gamma_n + \rho_p/\gamma_p$$

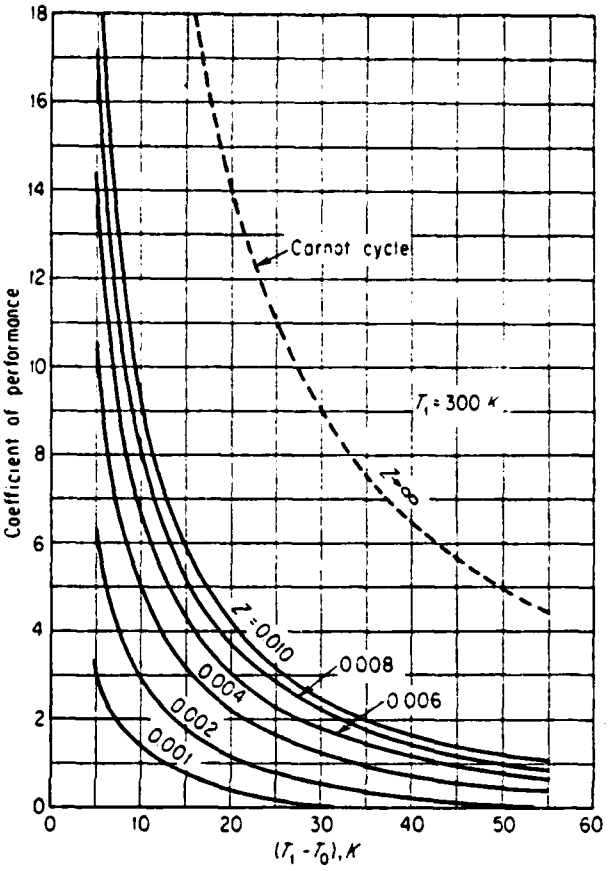
Such that $RU = k_n \rho_n + k_n \rho_p (\gamma_n/\gamma_p) + k_p \rho_n (\gamma_p/\gamma_n) + k_p \rho_p$

To minimize RU take $d(RU)/d(\gamma_n/\gamma_p) = 0$, and find that $\gamma_n/\gamma_p = (\rho_n k_p / \rho_p k_n)^{1/2}$ for this condition. For this value of γ_n/γ_p RU has the value

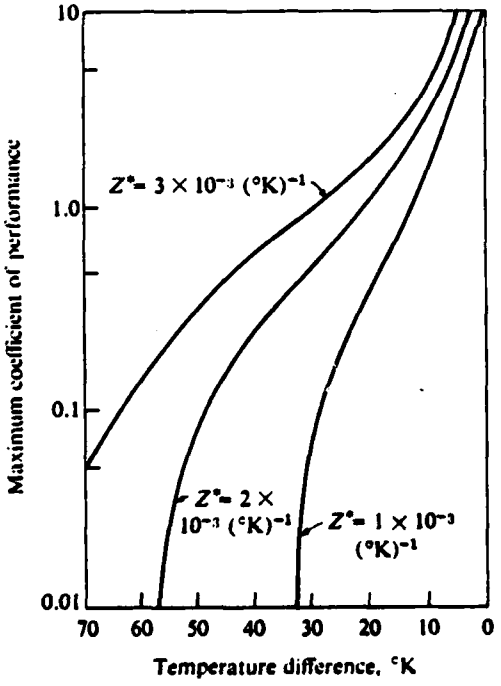
$$(RU)_{min} = \left[(\rho_n k_n)^{1/2} + (\rho_p k_p)^{\frac{1}{2}}\right]^2$$



Maximum theoretical temperature difference for a thermoelectric element.



Maximum theoretical coefficient of performance for a thermoelectric element.



The maximum coefficient of performance that can be achieved with a given temperature difference and a specified figure of merit for the couple. The hot shoe temperature is assumed to be 300°K.

If an electrical contact resistance of r is assumed at each junction (r at each end of each element]

$$R = \rho_n/\gamma_n + 2r/\gamma_n L + \rho_n/\gamma_n + 2r/\gamma_p L$$

where L is the length of the element (common to both)

The result is

$$\frac{\gamma_n}{\gamma_p} = \sqrt{\frac{k_p \rho_n \left(1 + \frac{2r}{\rho_n L}\right)}{k_n \rho_p \left(1 + \frac{2r}{\rho_p L}\right)}}$$

and the optimum value of Z is Z*

$$Z^* = \left[\frac{\alpha_{pn}}{\sqrt{k_p \rho_p \left(1 + \frac{2r}{\rho_p L}\right)} + \sqrt{k_n \rho_n \left(1 + \frac{2r}{L}\right)}}\right]^2$$

$$\text{If } k_p = k_n \text{ \& } \rho_p = \rho_n \qquad Z^* = \frac{\alpha^2}{k\rho \left(1 + \frac{2r}{\rho L}\right)}$$

The figure of merit, Z

Z is defined in terms of α, U, & R where in general

$$R = \frac{L_n}{A_n}\rho_n + \frac{L_p}{A_p}\rho_p \quad \& \quad U = \frac{A_n}{L_n}k_n + \frac{A_p}{L_p}k_p$$

For RU to be a minimum

$$\frac{A_n}{L_n} = \frac{L_p}{A_p} = \left(\frac{\rho_n}{\rho_p}\frac{k_p}{k_n}\right)^{\frac{1}{2}}$$

or in terms of $\gamma = A/L$

$$\frac{\gamma_n}{\gamma_p} = \left(\frac{\rho_n}{\rho_p}\frac{k_p}{k_n}\right)^{\frac{1}{2}}$$

which fixes the relative geometry.

Also for RU to be a minimum,

$$RU = \left[(\rho_n k_n)^{\frac{1}{2}} + (\rho_p k_p)^{\frac{1}{2}} \right]^2$$

If we had 2 materials with the same α, k, and ρ, we could write

$$Z = \frac{\alpha^2}{k\rho}$$

Some of the above properties are governed by the Wiedermann-Franz Law $k\rho$ = (Lorentz number) T. For metals, the Lorentz number has a value of 2.5×10^{-8} watt-ohm/°K^2. Also for metals, the Seebeck coefficient, α, has values on the order of 10^{-5} volt/°C. Therefore $Z = \alpha^2/\rho k \approx (10^{-5})^2/(2.5\times10^{-8})\,T \simeq 4\times10^{-3}/T$. For temperatures on the order of 300°K, $Z \approx 10^{-5}$. It is apparent that thermoelectric cooling with metal conductors is of minimal value.

Values of properties are shown below for some metals and semiconductors where $\sigma = \rho^{-1}$, the electrical conductance.

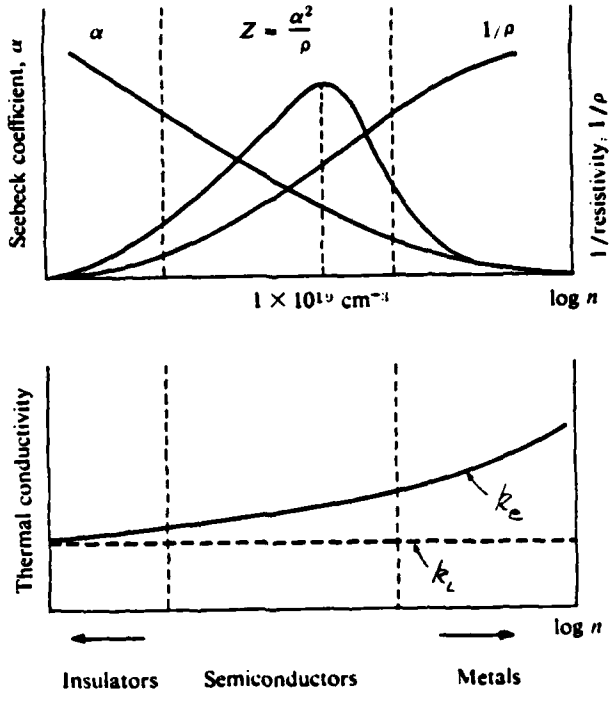
TABLE 2
Thermoelectric properites of metal

	Electrical Conductivity σ $(\Omega\text{-cm})^{-1}$	Seebeck Coefficient α $(\mu V/°C)$	Thermal Conductivity k (watt/cm °C)	$\alpha^2\sigma$	Figure of Merit $\frac{\alpha^2\sigma}{k}$
Copper	5.9×10^5	+2.5	3.96	3.7×10^{-6}	$9\ 3 \times 10^{-7}$
Nickel	1.5×10^5	-18	0.87	4.9×10^{-5}	$5\ 6 \times 10^{-5}$
Bismuth	8.6×10^3	-75	0.08	4.8×10^{-5}	6×10^{-4}

TABLE 3
Thermoelectric properties of semiconductors

	σ $(\Omega\text{-cm})^{-1}$	α $\frac{\mu V}{°C}$	k_L $\frac{watt}{cm\,°C}$	k_e $\frac{watt}{cm\,°C}$	$\alpha^2\sigma$	$Z = \frac{\alpha^2\sigma}{k}$
Germanium	1000	200	0 63	0 006	4×10^{-5}	$6\ 3 \times 10^{-7}$
Silicon	500	200	1 13	0 003	2×10^{-5}	$1\ 8 \times 10^{-5}$
Indium antimonide	2000	200	0 16	0 01	8×10^{-5}	$4\ 7 \times 10^{-4}$
Indium arsenide	3000	200	0 3	0 015	$1\ 2 \times 10^{-4}$	$3\ 8 \times 10^{-4}$
Bismuth telluride	1000	220	0 016	0 004	$4\ 7 \times 10^{-5}$	$2\ 3 \times 10^{-3}$

In TABLE 3, k_L is the lattice conductivity & k_e is the electronic conductivity such that $k = k_e + k_L$



A schematic representation of how the Seebeck coefficient, resistivity, and thermal conductivity depend on the concentration of extrinsic charge carriers.

The variation of α, ρ, k, and Z as a function of extrinsic charge carrier is sketched above. k_e is the electronic portion of the thermal conductivity, and k_L is that part associated with the lattice or phonon transfer.

The table below is from Spring, but note that α can not be separated out as an independent quantity.

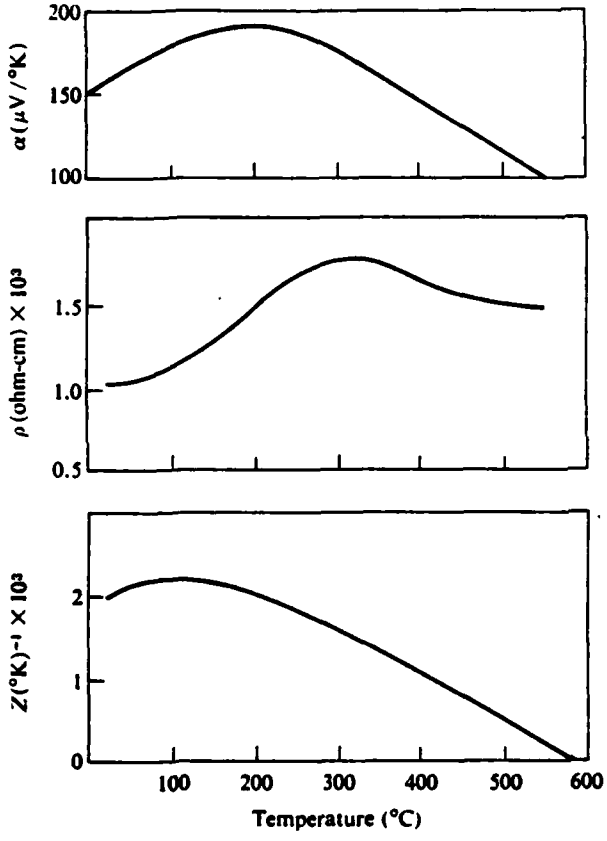
Thermoelectric materials

Spring:Direct Generation of Electricity

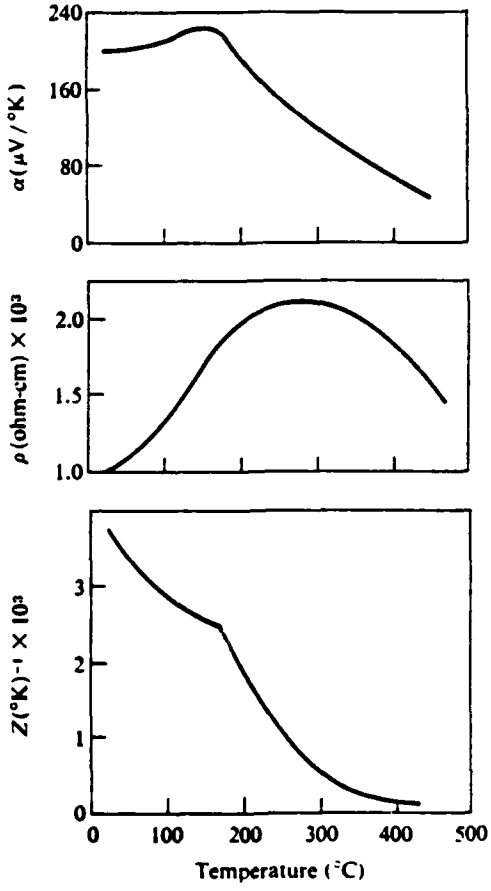
1	2	3	4	5	6	7	8	9	10
	E_g (eV)	Melting point (°C)	Type of semi-conductor	$\alpha^2\sigma^*$	K_e^* (W/cm deg C)	K_L (W/cm deg C)	Z_{max}	Temperature (°K)	Maximum operating temperature (°K)
Bi_2Te_3	0·15	575	n or p	4×10^{-3}	0·004	0·016	2×10^{-3}	300	450
$BiSb_4Te_{7\cdot5}$	—	—	p	$4{\cdot}6 \times 10^{-3}$	0·004	0·010	$3{\cdot}3 \times 10^{-3}$	300	450
Bi_2Te_2Se	0·3	—	n	$3{\cdot}6 \times 10^{-3}$	0·003	0·013	$2{\cdot}3 \times 10^{-3}$	300	600
PbTe	0·3	904	n or p	$2{\cdot}6 \times 10^{-3}$	0·003	0·02	$1{\cdot}2 \times 10^{-3}$	300	900
GeTe(+ Bi)	—	725	p	$3{\cdot}2 \times 10^{-3}$	—	0·02	$1{\cdot}6 \times 10^{-3}$	800	900
ZnSb	0·6	546	p	2×10^{-3}	—	0·17	$1{\cdot}2 \times 10^{-3}$	500	600
$AgSbTe_2$	0·6	576	p	$1{\cdot}4 \times 10^{-3}$	0·002	0·006	$1{\cdot}8 \times 10^{-3}$	700	900
InAs(+ P)	0·45	940	n	4×10^{-3}	—	0·07	6×10^{-4}	900	1100
CeS(+ Ba)	—	—	n	8×10^{-4}	—	0·01	8×10^{-4}	1200	1300
Cu_6Te_2S	—	930	—	18×10^{-4}	—	0·012	$1{\cdot}5 \times 10^{-3}$	1100	—
Ge–Si	0·8	—	n	3×10^{-3}	—	0·033	9×10^{-4}	900	1200
			p	2×10^{-3}			6×10^{-4}	900	

The figures given in columns 5, 6, 7 and 8 refer to the temperature quoted in column 9.

The data on this and the following page can be used in the design of thermoelectric coolers by calculating $k = \alpha^2/\rho z$. The figures are taken from Angrist "Direct Conversion of Energy".



The Seebeck coefficient, electrical resistivity, and figure of merit of an *n*-type alloy: 75% Bi_2Te_3, 25% Bi_2Se_3.



The Seebeck coefficient, electrical resistivity, and figure of merit of a *p*-type alloy: 25% Bi_2Te_3, 75% Sb_2Te_3(1.75% Se).

95% Bi_2Te_3 & 5% Bi_2Se_3

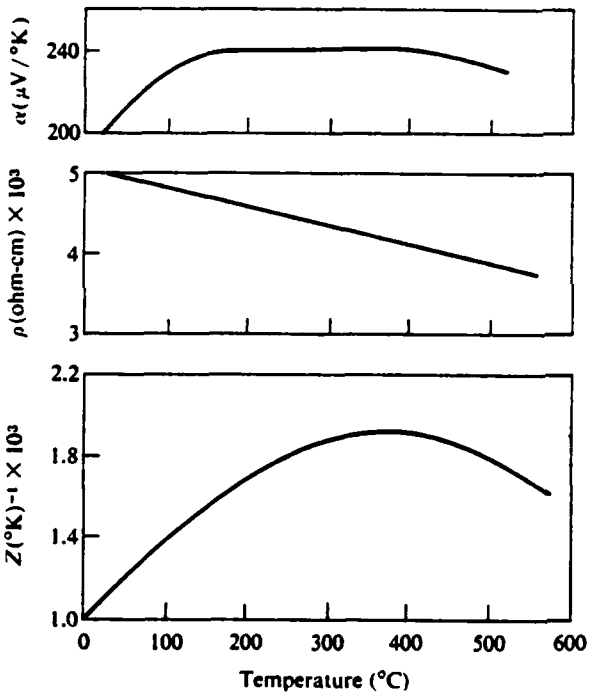
$\alpha_p = 195\ \mu V/K$

$\rho_p = 0.9 \times 10^{-3}\ \Omega\ cm$

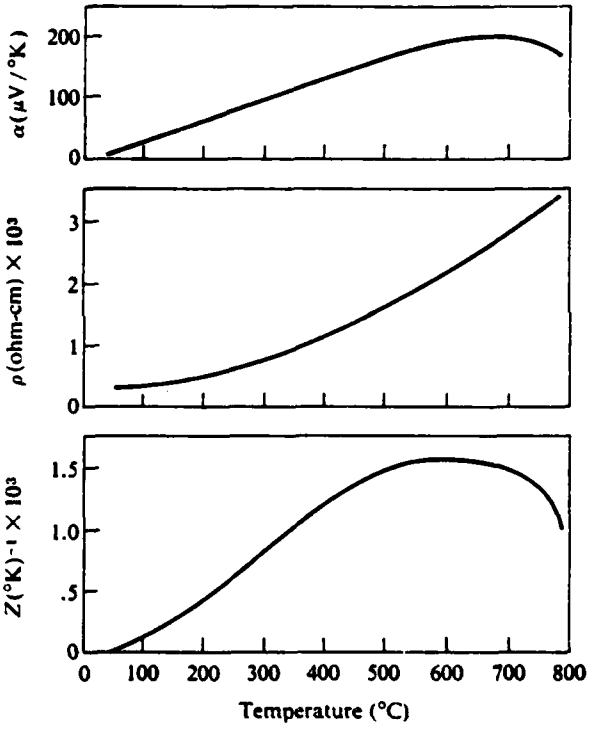
$Z_p = 2.5 \times 10^{-3}/°K$

p stands for positive

data from IECEC 1973 p. 229

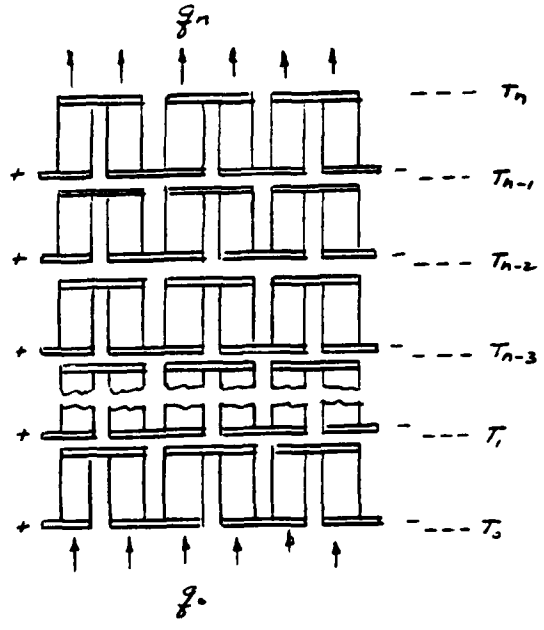


The Seebeck coefficient, electrical resistivity, and figure of merit of a *p*-type alloy: $AgSbTe_2$.



The Seebeck coefficient, electrical resistivity, and figure of merit of an *n*-type alloy: 75% PbTe, 25% SnTe.

Cascade Cooling



$$\text{C.O.P.} = \frac{q_o}{q_n - q_o}$$

define $\mu \equiv \frac{q_n}{q_o}$

such that $\mu = 1 + \frac{1}{\text{C.O.P.}}$

also for each stage $\mu_i = \frac{q_i}{q_{i-1}}$

such that $\mu_i = \prod_{i=1}^{n} \mu_i$

The optimum figure of merit comes into the calculation of optimum performance as previously defined:

$$Z^* = \left(\frac{\alpha_{pn}}{\sqrt{k_n \rho_n}\ \sqrt{k_p \rho_p}} \right)^2 (T_m)$$

In the optimization we use the Wiedermann-Franz Law $\frac{k\rho}{T} = L$
where L = Lorenz constant (2.5×10^{-8} volt^2/°K^2 for metals)
Therefore $k_n \rho_n = L_n T_m$ & $k_p \rho_p = L_p T_m$ &

$$Z^* = \left(\frac{\alpha_{pn}}{\sqrt{L_n}\ \sqrt{L_p}} \right)^2 = \text{constant} \qquad (\text{valid for } (T_n - T_c) \leq 60°)$$

It is convenient to use $\gamma^{-1} \equiv \sigma = \ell/A$ and to optimize μ with respect to d. If this is done,

$$\left(\frac{\sigma_n}{\sigma_p} \right)_i = \left[\left(\frac{k_n}{\rho_n} \right)_i \left(\frac{k_p}{\rho_p} \right)_i \right]^{\frac{1}{2}} = \left(\frac{A_p}{A_n} \right)_i \quad \text{for equal } \ell_i$$

Also it can be determined that for max. c.o.p.

$$(I_i)_{opt} \qquad \frac{(\alpha_{pn})_i (T_i - T_{i-1})}{R_i \left(\sqrt{1 + Z^* T_m} - 1 \right)}$$

With respect to temperature distribution, μ is a minimum when

$$T_i = \sqrt{T_{i-1} \times T_{i+1}}$$

$$\text{or} \quad T_i = T_0 \left(\frac{T_n}{T_0}\right)^{\frac{i}{n}} \quad \therefore \quad \frac{T_{i+1}}{T_i} = \left(\frac{T_n}{T_0}\right)^{\frac{1}{n}}$$

The above optimization procedures make the c.o.p.'s for all the stages equal. For these conditions

$$\mu = \left[\frac{\left(\frac{T_n}{T_0}\right)^{\frac{1}{n}}\sqrt{1+Z^2} - 1}{\sqrt{1+Z^2} - \left(\frac{T_n}{T_0}\right)^{\frac{1}{n}}}\right]^n$$

The preceeding theory was coded and used as a subroutine to MICTA. A listing is given below.

```
 LEVEL 21.6 ( MAY 72 )                    OS/360  FORTRAN H

            COMPILER OPTIONS - NAME=  MAIN,OPT=02,LINECNT=54,SIZE=0000K,
                               SOURCE,EBCDIC,NOLIST,NODECK,LOAD,MAP,NOEDIT,ID,NOXREF
 ISN 0002                   SUBROUTINE COOLER (CN,T)
 ISN 0003                   DIMENSION CN(1),T(1)
 ISN 0004                   REAL IOPT
                      C     A IS THE SEEBECK COEF. IN VOLTS PER DEG KELVIN
 ISN 0005                   A = .00038
                      C     B IS THE RESISTIVITY OF BI2-TE3 IN OHM-MILL
 ISN 0006                   B=.3937
 ISN 0007                   APN = CN(9)*CN(24)
 ISN 0008                   R = 2.*B*(CN(75)+CN(76))/APN
 ISN 0009                   IOPT = 8.0
 ISN 0010                   QC03 = A*IOPT*(T(1269)+273.)-.5*IOPT**2*R
 ISN 0011                   QC04 = A*IOPT*(T(1272)+273.)-.5*IOPT**2*R
 ISN 0012                   QC09 = A*IOPT*(T(1329)+273.)-.5*IOPT**2*R
 ISN 0013                   QC10 = A*IOPT*(T(1332)+273.)-.5*IOPT**2*R
 ISN 0014                   QH03 = A*IOPT*(T(1469)+273.)+.5*IOPT**2*R
 ISN 0015                   QH04 = A*IOPT*(T(1472)+273.)+.5*IOPT**2*R
 ISN 0016                   QH09 = A*IOPT*(T(1529)+273.)+.5*IOPT**2*R
 ISN 0017                   QH10 = A*IOPT*(T(1532)+273.)+.5*IOPT**2*R
 ISN 0018                   CN(4701)=QC03
 ISN 0019                   CN(4702)=QC04
 ISN 0020                   CN(4703)=QC09
 ISN 0021                   CN(4706)=QC10
 ISN 0022                   CN(4705)=QH03
 ISN 0023                   CN(4706)=QH04
 ISN 0024                   CN(4707)=QH09
 ISN 0025                   CN(4708)=QH10
 ISN 0026                   CN(4751)=R
 ISN 0027                   CN(4752)=APN
 ISN 0028                   CN(4753)=IOPT
 ISN 0029                   RETURN
 ISN 0030                   END
```

ACTIVE SHEET RECORD

SHEET NUMBER	REV LTR	ADDED SHEETS				SHEET NUMBER	REV LTR	ADDED SHEETS			
		SHEET NUMBER	REV LTR	SHEET NUMBER	REV LTR			SHEET NUMBER	REV LTR	SHEET NUMBER	REV LTR
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3						48					
4						49					
5						50					
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7						52					
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REVISIONS			
LTR	DESCRIPTION	DATE	APPROVAL