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STUDY OF THE PHYSICS OF INSULATING FILMS AS RELATED TO THE RELIABILITY OF METAL-OXIDE SEMICONDUCTOR DEVICES

IBM T.J. Watson Research Center

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This work includes a study of the morphology associated with the oxidation of polycrystalline silicon, a description of moderate field charge injectors using silicon rich SiO_2, a technique for studying trapping characteristics using these charge injectors and a review paper on radiation damage in SiO_2.

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STUDY OF THE PHYSICS OF INSULATING FILMS AS RELATED TO THE RELIABILITY OF METAL-OXIDE SEMICONDUCTOR DEVICES

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INTRODUCTION

Contemporary Si device technology utilizes polycrystalline silicon for conductors but also requires the use of thin insulating layers between these lines. Charge storage devices (Floating Gate Devices) depend on maintaining charge stored on the polycrystalline silicon conductors for long periods of time up to the lifetime of the product utilizing these structures. As a result, electrical leakage from these "critical" conductors cannot be tolerated to even in a minute extent. Previous work has shown that the leakage current characteristics of the oxide formed above poly silicon are largely determined by the morphology for the poly silicon surface. This requirement has stimulated the work by Irene, Tierney and Dong reported by the two papers included in this report which show the importance of intergranular oxidation in determining the morphology of the poly Si-SiO_2 interface. A paper by Irene, Dong and Zeto describes measurements made on the characteristics of high pressure SiO_2 films made by Zeto at the U.S. Army Electronics Technology and Devices Laboratory (ERADCOM), Fort Monmouth, New Jersey. These measurements indicate a higher density, higher refractive index and slower chemical etch rate for these films made at 800°C as compared with the films grown at 1 atmosphere of O_2 at 1000°C. Subsequent work has shown that this results from the lower temperature used for the growth (800°C vs 1000°C) rather than the higher pressure used.

The low field injection properties of the Si rich charge injectors can be used to study the trapping properties of intervening layers in a novel technique developed by DiMaria, Ghez and Dong as described in a paper that is also included. This technique provides a rapid evaluation of the trapping characteristics. These injectors are being evaluated for use with "Floating Gate Structures".

A review paper on Radiation Damage in SiO_2 is included that is based on a talk given by Young at the Tbilisi Conference on Radiation Physics of Semiconductors and Related Materials.

Papers Published:

1. D.J. DiMaria, "Graded or Stepped Band-Gap-Insulator MIS Structures (GI-MIS or SI-MIS)", *J. Appl. Phys.* 50, 5826 (1979).

2. Z.A. Weinberg, D.R. Young, D.J. DiMaria, and G.W. Rubloff, "Exciton or Hydrogen Diffusion in SiO_2?", *J. Appl. Phys.* 50, 5757 (1979).

3. D.J. DiMaria, L.M. Ephrath and D.R. Young, "Radiation Damage in Silicon Dioxide Films Exposed to Reactive Ion Etching", *J. Appl. Phys.* 50, 4015 (1979).

4. D.J. DiMaria, "Charge Trapping in Thermal Silicon Dioxide", *Japan J. Appl. Phys.* 18, Supplement 18-1, 3 (1979).

Presentations Made:

1. E.A. Irene, "Si Oxidation Studies at Yorktown", at Yale University, March 9, 1979.

2. D.J. DiMaria, *(Invited)* "MOSFET Charge Storage Devices", at the American Physical Society Meeting, Chicago, Illinois, March 19-23, 1979.

3. D.J. DiMaria, "Radiation Damage in Silicon Dioxide", at the IEEE E.D.S. (Local Station), Rochester, NY, April 25, 1979.

4. D.J. DiMaria and D.W. Dong, "Graded or Stepped Insulator SI-MIS Structures (GI-MIS or SI-MIS)", at the Device Research Conference, University of Colorado, Boulder, CO, June 25-27, 1979.

5. R.F. DeKeersmaecker and D.J. DiMaria, "Hole Trapping in Ion-Implanted SiO_2", at the Conference on Insulating Films on Semiconductors, Durham, England, July 2-4, 1979.

6. D.R. Young, "Electron Trapping in SiO_2", at the Conference on Insulating Films on Semiconductors, University of Durham, Durham, England, July 2-4, 1979.

7. E.A. Irene, "Some Relationships Between the Oxidation Mechanism and Electrical Reliability of Polycrystalline Silicon Films", at the International Metallographic Society Meeting, July 1979.

8. D.R. Young, "Radiation Damage in SiO_2", at the International Conference on Radiation Physics of Semiconductors and Related Materials, Tbilisi, G.S.S.R, U.S.S.R., September 13-19, 1979.

9. R.F. DeKeersmaecker and D.J. DiMaria, "Hole Trapping in Ion-Implanted SiO_2", at the 9th European Solid State Device Research Conference, Munich, Germany, September 10-14, 1979.

SILICON OXIDATION STUDIES: MORPHOLOGICAL ASPECTS OF THE OXIDATION OF POLY CRYSTALLINE SILICON

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ABSTRACT Previous studies have shown that the oxide grown from polycrystalline silicon displays degraded reliability in terms of higher leakage current and premature dielectric breakdown as compared with the oxide grown from single crystal silicon. Present transmission electron microscope studies of the morphology of polycrystalline silicon films and the oxide grown therefrom show several novel features. The polycrystalline silicon becomes rougher after oxidation, the oxide displays thickness undulations which replicate the previous grain boundaries with thinner oxide over grain boundaries, and the oxide forms intergranularly as well as on the free silicon surface. Despite the intergranular oxide formation, the film skin of oxidized polycrystalline silicon does not become significantly more compressive. The surface roughness features of the polycrystalline silicon and oxide and the film stress values are explained by a Si creep mechanism. From these studies some aspects of the reliability of polycrystalline silicon and oxide are understood.

Introduction

The thermal oxidation of polycrystalline silicon (poly-Si) is technologically important because the Si0&d2. film produced from this oxidation, (from here on referred to as poly-OX), is needed to provide electrical isolation for conducting poly-Si lines and therefore the poly-OX must be a reliable, low conductivity, dielectric.

Kamins and MacKenna (1) have reported that at lower oxidation temperatures where the oxidation mechanism is predominantly surface reaction controlled, the rate of oxidation of poly-Si is characteristic of the random orientations of the poly-Si grains. The different oxidation rates across the surface would cause roughening. At higher oxidation temperatures where the oxidation is predominantly diffusion controlled a smoother poly-Si surface is produced. Andersen and Kerr (2) have reported that the higher than expected elecrical conductivity found for poly-OX films (3,4) is due to Si asperities which they observed on the poly-Si surface and which can cause local electric field enhancement. It was also reported (2,4) that higher temperature oxidation produces a lower conductivity poly-OX.

Based on these apparently concordant studies (1,2,3,4), it appears that the morphological and electrical characteristics of poly-OX are reasonably well understood. However, our recent transmission electron microscope (TEM) observations on poly-OX (5,6) to be detailed in this paper, strongly suggest that the morphology of the poly-OX itself (rather than, or in addition to, the poly-Si morphology) can cause the observed high conductivities of poly-OX. Furthermore the origin of poly-Si surface irregularities is elucidated from the TEM observations. A better understanding of poly-Si and poly-OX evolves which is based on the growth of a morphologically complex oxide film, poly-OX.

The present study is essentially a morphological characterization of the oxide films grown as a result of thermal oxidation of poly-Si. As a first step, the poly-Si itself is characterized by TEM and our results are compared with some of the relevant literature. Doped and undoped poly-Si films are oxidized from 800°C to 1200°C for short and long times and the morpholog-

ical results compared. In addition film stress measurements were performed on the poly-Si and poly-OX films, since these measurements were needed to confirm the mechanisms deduced from the morphological observations.

Experimental Procedures

Sample Preparation. Poly-Si films were deposited on thermally oxidized Si wafers by chemical vapor deposition, CVD, using gaseous SiH&d4. diluted in N&d2.. The CVD reactor temperature was either at 650°C to prepare initially amorphous silicon films or at 800°C to prepare initially polycrystalline films. In this study TEM observations were made on undoped and POCl&d3. doped films, prior to and after oxidation.

TEM. For TEM observations on poly-Si and poly-OX films, the Si substrates and oxide on Si were removed by chemical etching using HF-HNO&d3. mixtures by a previously outlined procedure (7) or by first pre-thinning using HF-HNO&d3. then using pyrocetichol-ethylenediamine - H&d2.0 mixtures at elevated temperature to remove single crystal and polycrystalline silicon but leaving oxide for observations and thirdly ion milling was occasionally used as an additional method to insure that the TEM observations were independent of the sample preparation procedures.

In some cases the poly-Si samples were oxidized and then thinned for TEM observation, however we found it useful to first thin a poly-Si specimen for TEM observation and then to oxidize the specimen and re-observe the same specimen for oxidation effects. In this case oxidation occurred from both sides of the poly-Si samples. We found no essential differences between these procedures except for the extent of oxidation.

Film Stress. The film stress of poly-Si films on oxidized Si substrate wafers was measured before and after oxidation of the poly-Si so as to observe any sintering and oxidation effects on the residual film stress. The method was to observe substrate bending by means of counting the Newton rings which are produced by optical interference between an optical flat and the curved substrates. The exact method used was previously discussed (9).

Experimental Results

Morphology of Poly-Si. For chemically vapor deposited silicon films, the temperature for the deposition is important in determining whether the silicon film is amorphous or crystalline. Fig. 1 shows as deposited silicon films prepared at 650°C on an oxidized silicon surface in a resistance heated CVD system in 1a and in a radiant heated system in 1b. In both cases the material is composed of small Si crystals imbedded in an amorphous Si matrix. The silicon deposited below 600°C appears to be totally amorphous by TEM while at CVD temperatures above about 700°C the films are entirely polycrystalline. These results are similar to published TEM studies on Si films (see for example ref. (10)). The specific polycrystalline morphology is dependent upon the temperature and time of annealing and on doping (10,11).

The changes which occur in poly-Si films as a result of oxidation heat treatments are of particular importance in the present study. Figure 2 compares the poly-Si morphology for films prepared at 650°C in 2(a)(b) and (c) to films prepared identically but doped by POCl&d3. deposition and drive in at 900°C in 2(d)(e) and (f). All the samples were oxidized in dry 0&d2. to produce about 30 nm Si0&d2. at 800°C for (a) and (d), 100°C for (b) and (e) and 1100°C for (c) and (f). From this comparison it is seen that the undoped samples all possess a more dendritic morphology which is characteristic of rapid crystallization but little grain growth. As the temperature exposure increases the number and size of equiaxed grains increases. Grain growth to equiaxed grain morphologies occurs readily for the doped samples and this is probably due to the increased mobility of Si atoms in the presence of P in Si (12).

Replicas of the surfaces of as-deposited and doped samples are shown in Fig. 3. It is seen that for the samples which received either an 800°C or 1100°C heat treatment, the surfaces are rougher for the undoped samples, i.e. there are more and sharper protuberances. Fig 2 has shown that the lateral dimensions of the grains is larger for the doped material. Therefore, it appears that due to the increased mobility of Si in presence of P(12) lateral grain

growth is possible for the doped samples but more difficult for the undoped poly-Si grains which extend upward rather than laterally.

As apparent from Fig. 3d, ridges on the replica outline the poly-Si grain boundaries. Since the replica is a negative impression of the poly-Si surface, the ridges represent depressions at the grain boundaries. Rather than being grain boundary grooves associated with the attainment of minimum radius of curvature, we believe that these features are due to intergranular oxidation. Evidence that these grooves widen and deepen with oxidation will be shown later.

The TEM observations show that doping and temperature determine the grain structure. P doping yields larger grains with smoother surfaces. Nearly dendritic morphologies are observed for undoped samples.

Morphology of Poly-Ox. As was shown in Fig. 2 there are basically two poly-Si grain morphologies: one is primarily dendritic and the other equiaxed. The tendency toward the equiaxed morphology increases as the mobility of Si atoms increases as a result of a higher processing temperature and/or phosphorous dopant concentration. The heavily doped poly-Si is more representative of an industrially useful case while the oxidation of the undoped material is of scientific interest. Fig. 4 shows a comparison of the oxide grown on single crystal Si in 4(a), undoped poly-Si in 4(b), doped poly-Si in 4(c), and in 4(d) doped poly-Si but thinned for TEM by ion milling rather than chemical etching so as to obviate any possible chemical etching artifacts. It is seen that the Si0&d2. grown on single crystal Si is comparatively featureless. The poly-OX, however, clearly shows thickness undulations. The thin regions of the poly-OX outline the previous grain boundaries as is especially apparent in Fig. 4c and d where the grain boundaries of the poly-Si are well defined. For the more complex poly-Si grain morphology i.e. smaller grains and mixed dendritic and equiaxed morphologies, the thickness undulations patterns are also more complex as seen in 4b. The use of chemical

etching and ion milling yielded essentially the same morphologies. Chemical etching being more rapid and equally reliable will be used throughout this study.

In order to clarify the magnitude of the intergranular oxidation effect and to further confirm the above thickness undulation observations in the absence of possible etching effects, the following experiment was performed. A poly-Si film on Si0&d2. on Si was prepared for TEM examination in the usual way (7) leaving an area of poly-Si thin enough for examination as shown in Fig. 5a. This sample was then oxidized repeatedly and examined after each oxidation to determine the effects of further oxidation treatments; the results are shown in Fig. 5. In 5b the sharply outlined relatively darker areas which have broad slip bands; bending contours and thickness fringes are the remnants of partially oxidized poly-Si grains. Surrounding these grains is poly-OX which has a graded thickness. The thinnest regions are nearest the previous grain boundaries. In some areas actual separation of the poly-OX occurs at the thinnest poly-OX regions. For illustration purposes Fig. 5(b) shows an area with a higher incidence of separation than is usual. Fig 5(c) is a more representative one with further advanced oxidation. We believe that the separation phenomena in 5(b) is due to the contraction of the silicon grain remnants upon cooling from the oxidation temperature. The silicon grain remnants contract more than the oxide causing tensile forces to be exerted at the already thinned oxide regions. Fig 5c shows the smaller crystalline remnants of the grains at the darkest hence thickest regions of the films. After the initial thinning to produce 5a the sample was not chemically or otherwise treated in any way after oxidation except to make the TEM observations and therefore the sample is coated with an oxide film parallel to the plane of the micrographs. This oxide film forms as a result of the oxidation of the free surface of the poly-Si grains as with the oxidation of single crystal Si. As oxidation progresses the oxide on the free surface grows thicker and thereby reduces the total electron transmission through the sample. This effect plus the fact that diffuse scattering occurs because the oxide is amorphous causes the micrograph images to become less sharp for samples with thick oxides. Fig. 5d shows the sample oxidized completely for ~ 18 hours. The very thick regions repre-

sent the grain centers which are consumed last but because of the greater oxide thickness the features of these regions are not discernable.

During oxidation the poly-Si surface becomes roughened more than the oxide although even the poly-OX surface is rough relative to the oxide grown on single crystal silicon. This is seen in Figure 6(a) and (c) which show oxidized poly-Si and 6 (b) and (d) which show the same samples with the oxide removed.

From these TEM observations several conclusions can be made. Firstly, the poly-OX is not uniformly thick, i.e. it has thickness undulations which replicate the previous grain boundaries with the thinnest poly-OX being near previous grain boundaries. Secondly, oxidation occurs intergranularly as well as on the free surface. The poly-Si surface, although initially rough, becomes further roughened as a result of oxidation. These characteristic features of the oxidation of poly-Si will enable a mechanism to be proposed.

Stress in poly-Si films. When Si is converted to Si0&d2. there is more than a twofold (2.2) increase in volume. For the oxidation of single crystal Si this volume is obtained by the outward expansion of the oxide film from the single crystal surface that is being oxidized. However, for the case of poly-Si oxidation in which oxidation occurs not only on the free surface but also intergranularly, the volume required for oxidation is not as readily available. The intergranular mode of oxidation could lead to the buildup of a large compressive stress in the plane of the poly-Si film. Experience has shown that even for total oxidation of poly-Si, the films do not show any mechanical failure due to stress buildup. Thick poly-Si films (10&u3.nm) have been reported (13) to impart a substantial tensile stress to silicon substrates. It was also reported (13) that this tensile stress could be reduced by adding oxygen to the CVD ambient. In a recent detailed study of the wafer deformation caused by poly-Si films (14), a tensile poly-Si film stress was also reported. This tensile stress increased during inert ambient (N&d2. or Ar) anneals due to sintering but decreased if 0&d2. was added to the

annealing ambient. These studies (13,14) strongly support the contention that intergranular oxidation can lead to a compressive stress.

In order to determine the change in film stress before and after oxidation of poly-Si, several poly-Si samples both undoped and POCl&d3.. doped were measured before and after oxidation. It is seen in Table 1 that for all samples the total change in stress after oxidation is small. The doped samples all became more compressive (−) while the undoped became more tensile (+) after oxidation. We believe that the scatter in the data is primarily due to the smallness of measured changes. These stress results can be understood by considering that the grain morphology of the undoped poly-Si samples is immature with respect to further high temperature heat treatments. As shown in Fig. 2 the undoped samples undergo grain growth during oxidation. Grain growth causes a reduction in volume by eliminating grain boundaries and with the volume decrease of the film, a more tensile stress is expected. Therefore, for the undoped material there are two opposing processes occurring during oxidation: intergranular oxidation causing a more compressive film stress and grain growth causing a more tensile stress. Apparently grain growth is more dominant. For the doped material, the grain morphology is more mature hence the dominant effect during oxidation is due to intergranular oxidation which results in a compressive stress.

Intuitively a large compressive stress is anticipated due to intergranular oxidation. The magnitude of this stress can be estimated by considering ~ 50 nm diameter grains with 1 nm intergranular oxide formed (from Figs. 4 and 5, only 1 nm intergranular is a very conservative value). From these values a film stress of more than 10"dynes/cm&u2. is calculated which yields more than 10&u2. more Newtons rings than is observed. It is clear that such a large stress would be easy to measure. The large discrepancy between the anticipated stress attributed to intergranular and measured stress strongly suggests that matter flows to create the necessary volume to accommodate intergranular oxidation and preclude the buildup of a large compressive stress.

Table 1

The Change in Residual Stress in Polycrystalline Silicon Films After Oxidation

Sample ID	Change in Number of Newton Rings	Change in Stress ($\Delta\tau \cdot 10^{8}$ dynes/cm^2)
Doped:		
30	−1.5	−7
33	−2	−9
34	−2	−9
38	−2.5	−11
Undoped:		
39	+6	+27
40	+7	+31
41	+5	+22
42	+5	+22
43	+5	+22
44	+5	+22

Model for the Oxidation of Poly-Si. The low stress values for poly-Si oxidation means that either Si and/or Si0&d2. plastically deforms or creeps to relieve the stress and preclude film failure. If Si0&d2. flows under oxidation conditions, then each oxidizing grain boundary acts as a source of Si0&d2. and from each boundary Si0&d2. would flow. The net result would be a thicker poly-OX at previous grain boundaries. Since negative thickness undulations are observed, it is concluded that Si creeps from the grain boundaries in order to relieve the strain.

A Nabarro-Herring type creep mechanism (19,20) closely describes the situation at hand. In this mechanism a compressive stress is exerted in the grain boundaries by the growing oxide in a direction parallel to the plane of the poly-Si film. To relieve the strain vacancies flow toward the oxidizing boundary thereby supplying the volume necessary to relieve the compression. Si atoms flow in the opposite direction thereby causing the grains to elongate in a direction normal to the stress. This type of mechanism has been observed to occur at high temperatures and under low stress which are the conditions where intergranular silicon oxidation commences.

The operation of this mechanism is clarified by consideration of Fig. 7. Fig. 7a shows the idealized grain morphology for poly-Si showing the free and grain boundary surfaces. As oxidation ensues a stress, τ, builds up in the grain boundaries as a result of the volume increase resulting from intergranular oxide formation. The small arrows show the direction of motion of Si atoms away from the source of the strain and towards the mid-grain regions so as to relieve the strain. This motion of Si depletes the ammount of Si at the grain boundaries and enhances the amount at the midgrain regions thereby elongating the grains normal to the stress. Simultaneous with the Si motion, oxidation also occurs and hence there is consumption of Si both in the grain boundaries and at midgrain regions. Therefore, the net result is a thinner oxide formed at previous grain boundaries due to Si depletion and a thicker oxide of mid grain regions that receive the excess Si. This flow of Si and the growth of the oxide is

seen in 7(c) and (d) where d_e is the extra growth of oxide due to the Si which flowed to the mid-grain regions.

At higher oxidation temperatures it may be expected that Si0&d2. as well as Si flows. This would result in less severe poly-OX thickness undulations for higher temperature oxidations and more severe for lower temperature oxidation. Fig. 8 shows a comparison of the same sample as used in Fig. 5 oxidized nearly completely and to the same extent at 800°C 8(a) and 1150°C 8(b). Less severe thickness undulations are seen for the higher temperature case.

In summary, a consistent explanation is realized by considering a Si creep mechanism as the predominant factor in determining the overall poly-Si and poly-OX morphology after oxidation.

Implications of the Model. From a comparison of dark and photo currents in poly-OX (4), a uniform barrier lowering effect was ruled out as the cause of higher than expected currents in poly-OX. Localized field enhancement effects due to protuberances on the poly-Si surface were deemed causitive of the observed high conductivity of poly-OX (2,3,4). The present study has shown that surface roughness of poly-Si is a direct result of intergranular oxidation of poly-Si. Also the original poly-Si grain morphology while being a function of preparation temperature and doping does not greatly affect the surface roughness of poly-Si after oxidation. This explains why higher than normal poly-OX currents are seen for poly-OX grown on doped and undoped poly-Si even though the original grain sizes and morphologies are vastly different.

In addition to poly-Si surface roughness effects, the present study also showed that the poly-OX has thickness undulations. The TEM micrographs show that the thin regions of poly-OX over previous grain boundaries represent a smaller area than the thick poly-OX over mid-grain regions. As estimated from the micrographs, the poly-OX is more than 25% thinner near previous grain boundaries. The usual film thickness measuring techniques used to

measure poly-OX thicknesses such as interference, ellipsometry or mechanical step height techniques will yield poly-OX thicknesses representative of the larger areas i.e. the thicker regions. However, the electronic currents in poly-OX are determined by the thinnest regions which yield the maximum field for an applied voltage. Therefore, the reported electric fields for poly-OX based on the conventionally measured poly-OX thicknesses could be erroneously low. It is interesting to note that a 30-35% decrease in film thickness will yield ~1.5 increase in field which is sufficient to explain some of the reported field enhancement effects in poly-OX (4).

We have found initial electrical shorts in some devices which utilize poly-Si lines. The shorts extend through the poly-Si lines and through an underlying oxide to the substrate or another line. The shorts occur as a result of removing the poly-OX on a line using an HF based chemical etchant so that metal can be evaporated for the contact to the poly-Si line. This shorting problem is understood by considering that due to intergranular oxidation of poly-Si, poly-OX forms in the grain boundaries of the poly-Si lines. When the surface poly-Ox is removed by chemical etching, the etchant penetrates into the intergranular poly-OX and in some places where intergranular oxidation is extensive, through the underlying oxide. Evaporated Al will fill these holes thereby causing the electrical shorts. These reliability implications are treated in more depth in a separate publication (15).

Conclusions

TEM studies of the oxidation mechanism of Poly-si has revealed the following:

1) There is intergranular oxidation as well as oxide forming on the free silicon surface.
2) The intergranular oxidation of poly-Si leads to poly-Si roughness and thickness undulations in poly-OX.

A Si creep mechanism describes the oxidation behavaior and the morphological features that develop as a result of oxidation help to explain some electrical reliability aspects of poly-ox.

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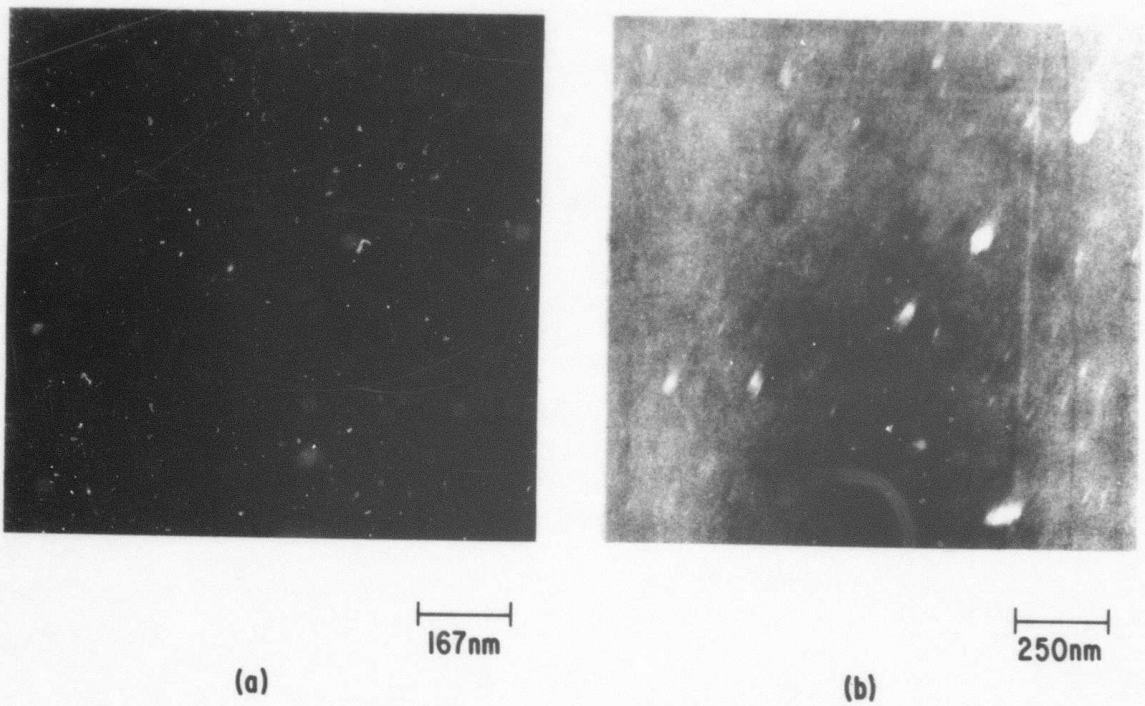

Fig. 1 Deflected aperature dark field TEM micrographs of poly-Si deposited onto an oxidized silicon substrate at 650°C by the decomposition of SiH_4 in (a) a resistance heated furnace and (b) a radiant heated system.

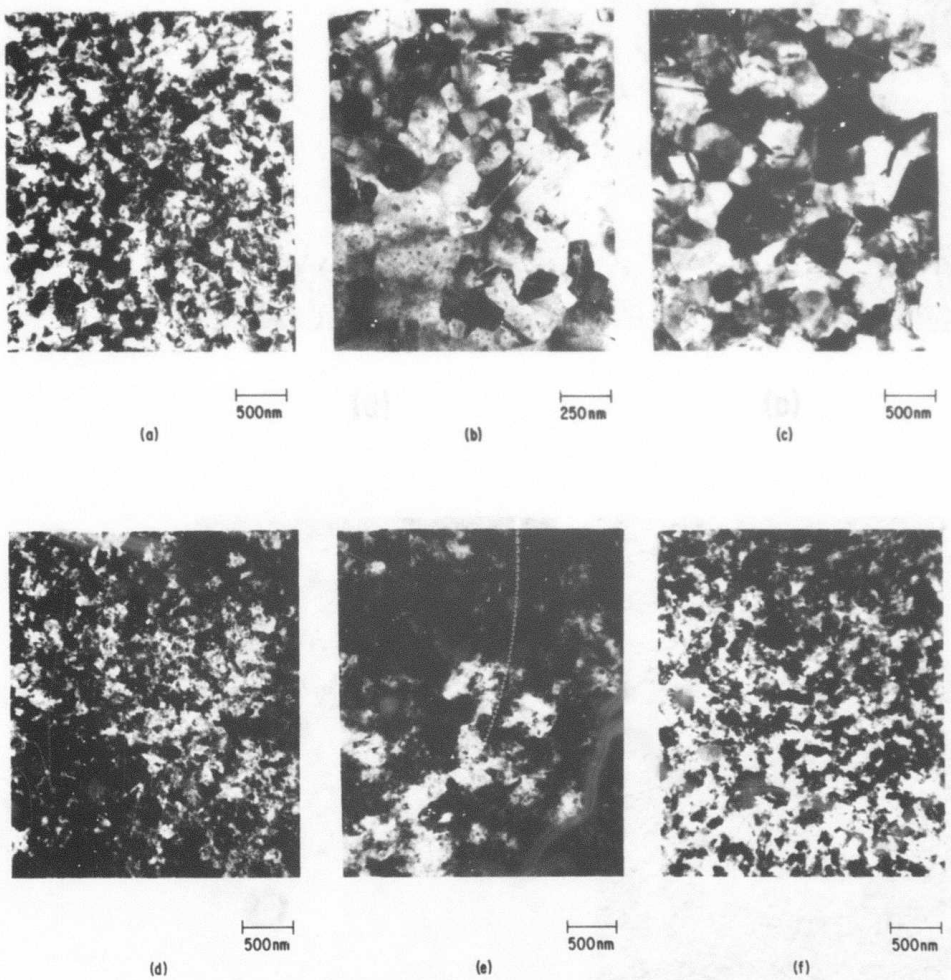

Fig. 2 Comparison of poly-Si deposited at 650°C oxidized (a) at 800°C, (b) 1000°C and (c) 1100°C to produce 30 nm SiO_2. For (d), (e) and (f) the samples are the same as (a) (b) and (c) respectively with the exception that (d), (e) and (f) have received $POCl_3$. doping. The SiO_2 was removed in HF prior to TEM.

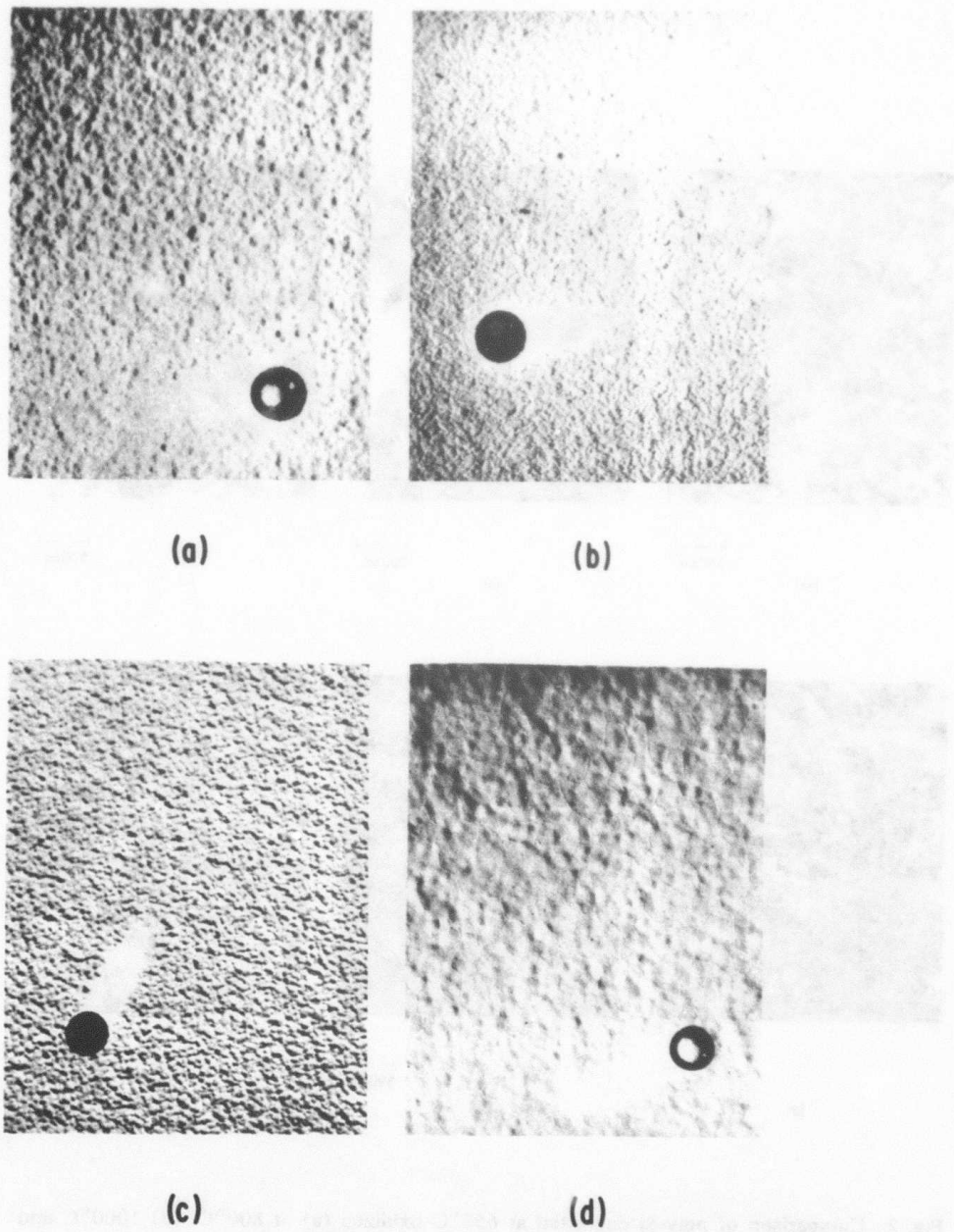

Fig. 3 Replicas (negative) of CVD silicon films (a) deposited at 650°C, undoped, 800°C oxidation, (b) deposited 650°C, $POCl_3$. doped, 800°C oxidation, (c) deposited at 800°C, undoped, 1100°C oxidation (d) deposited at 800°C, $POCl_3$. doped, 1100°C oxidation. The oxide was ~30 nm and removed prior to replication.

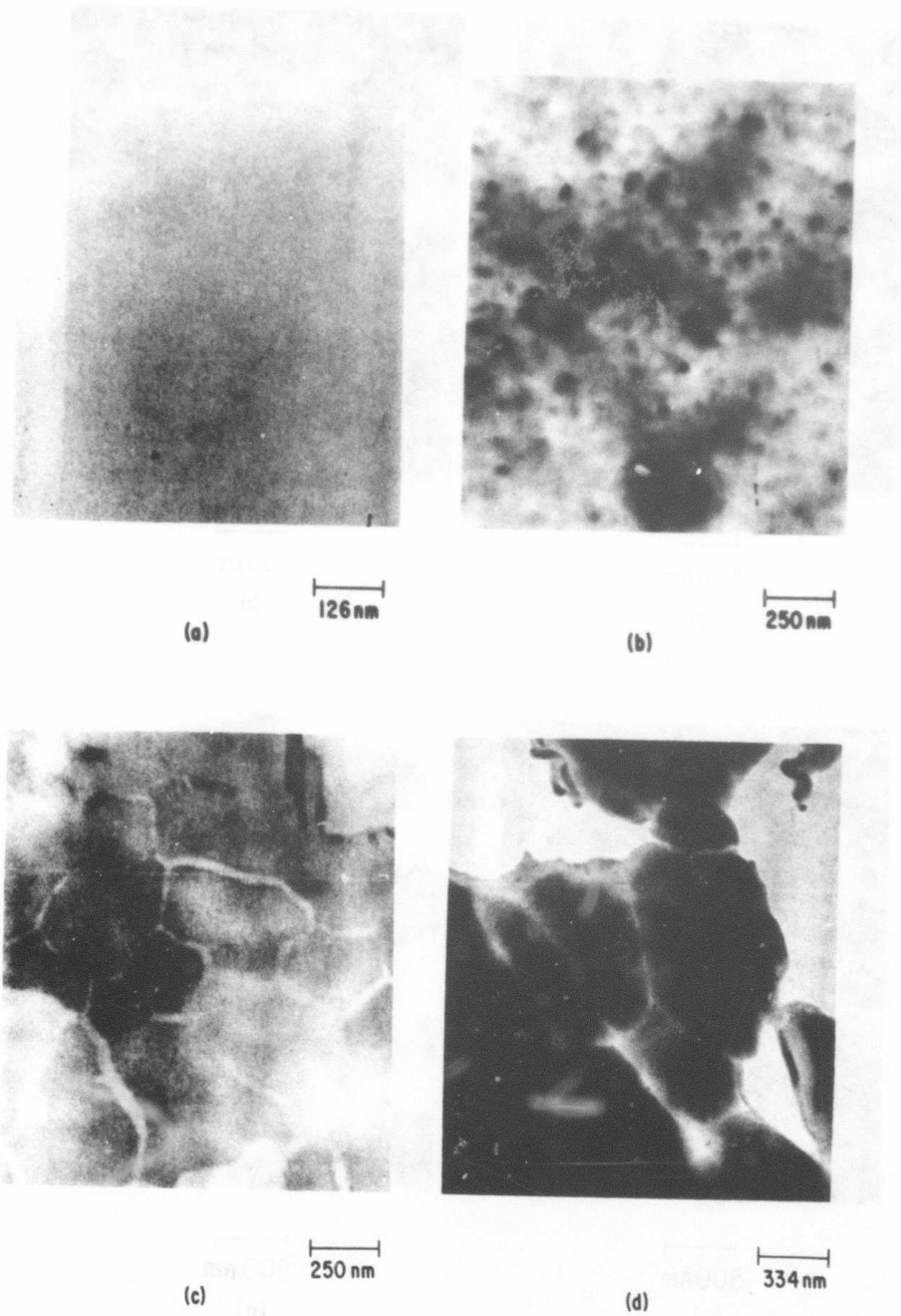

Fig. 4 Comparison of oxide grown at 1000°C in dry 0_2 on (a) single crystal Si (b) undoped poly-Si, (c) doped poly Si and (d) doped poly Si but prepared for TEM by ion milling

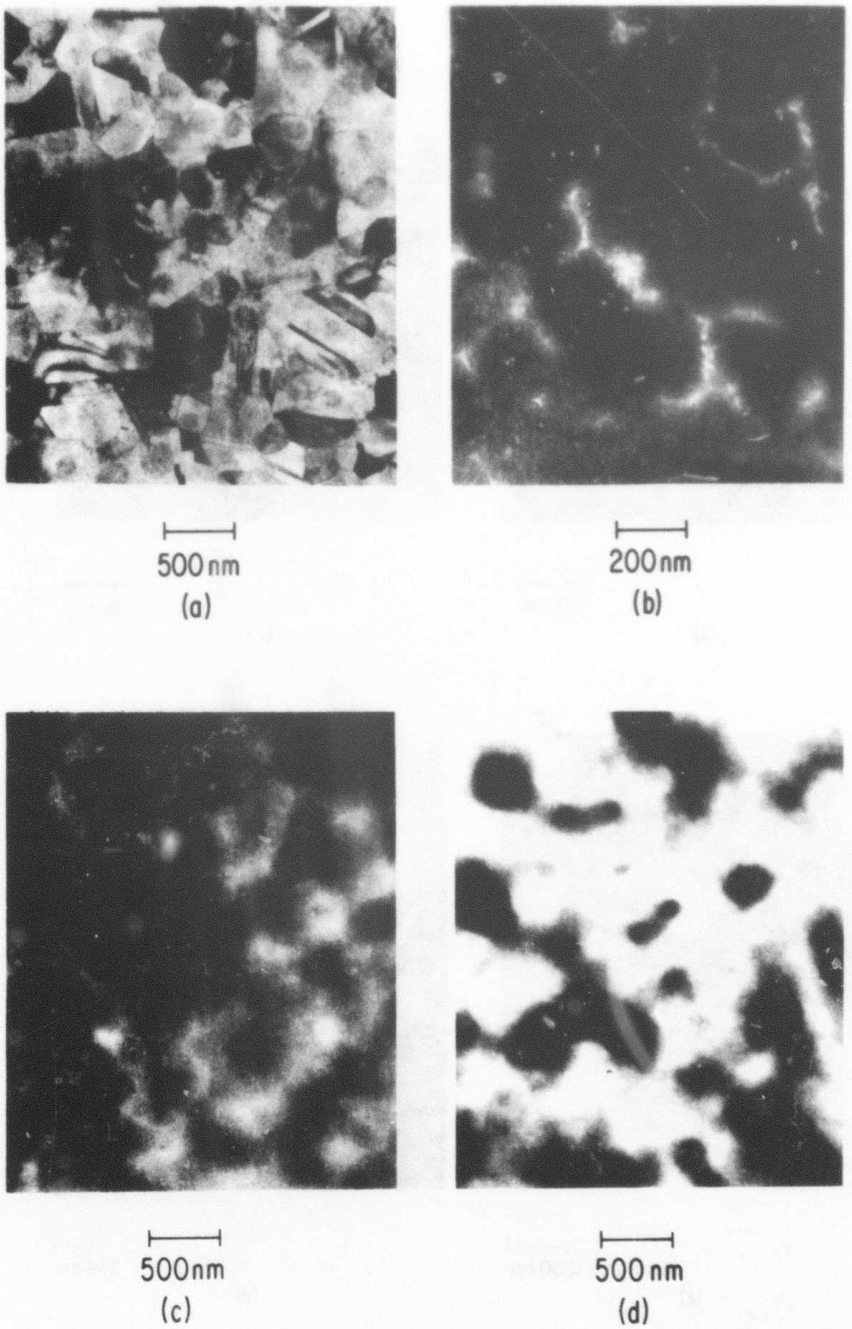

Fig. 5 Progressive stages of oxidation of poly-Si, (a) unoxidized, (b) oxidized to produce ~50 nm SiO_2, (c) oxidized to produce ~ 150 nm SiO_2 (d) completely oxidized ~ 300 nm SiO_2.

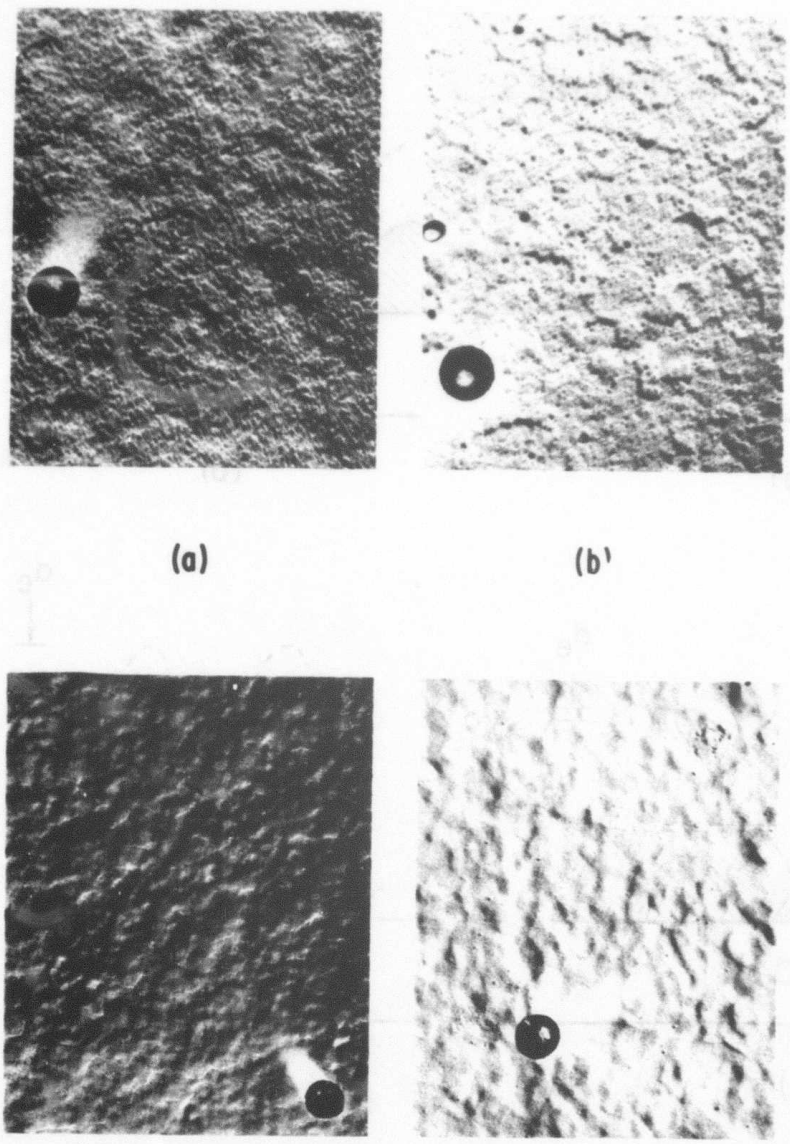

Fig. 6 Replicas of the surface of oxidized poly-Si and poly-Si with the poly-OX removed, (a) 650°C prepared, doped, oxidized to ~50 nm at 1000°C (b) same as (a) but oxide removed, (c) 800°C prepared, doped, oxidized to ~500 nm at 1000°C (d) same as (c) but oxide removed.

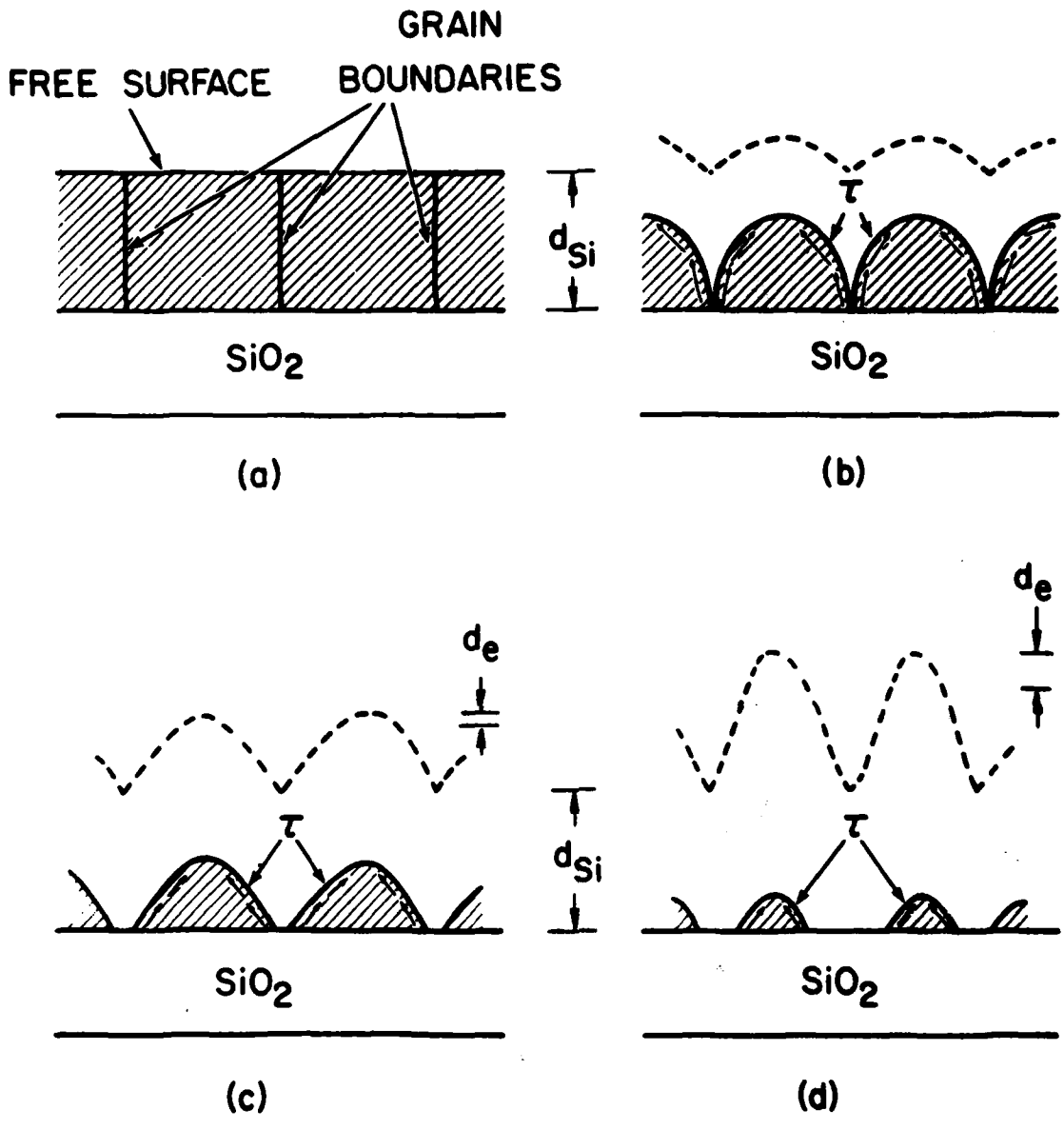

Fig. 7 Model for the intergranular oxidation of poly-Si (a) unoxidized, idealized grain structure (b), (c), (d) progressive stages of oxidation.

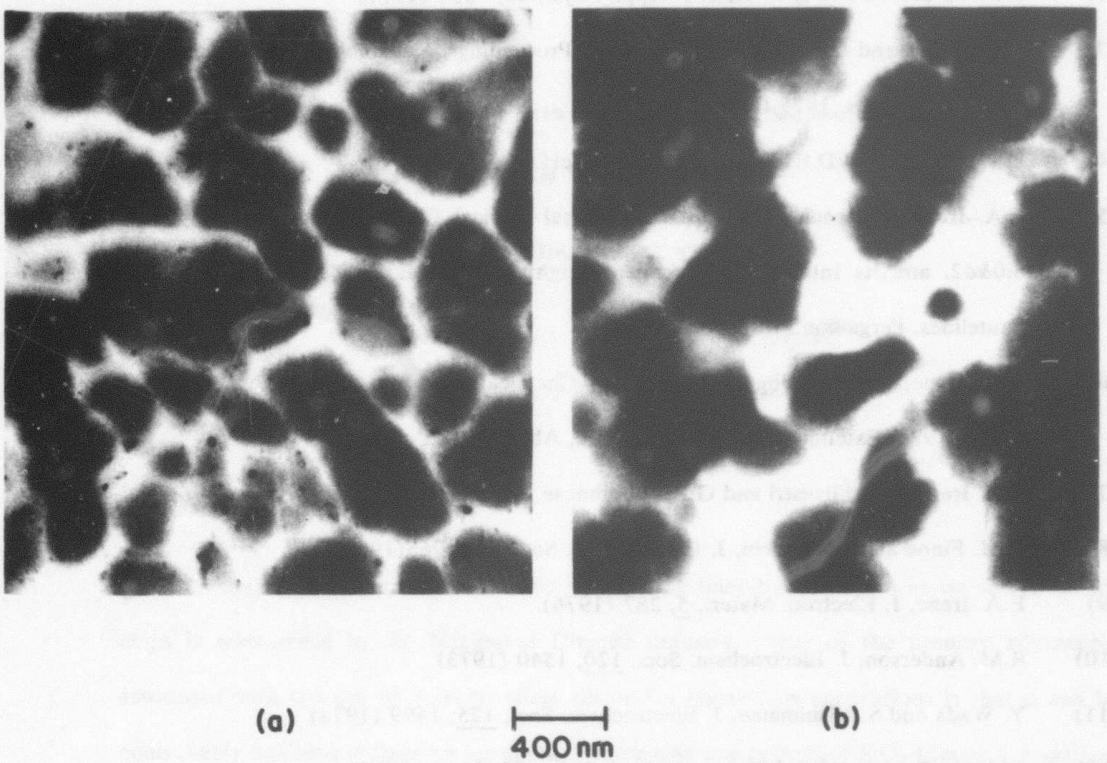

Fig. 8 Poly-Si samples as in Fig. 5, oxidized to the same extent in dry 0_2 (a) 800°C and (b) 1150°C.

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Some Relationships Between The Oxidation Mechanism and Electrical Reliability of Polycrystalline Silicon Films

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ABSTRACT

The use of polycrystalline silicon for conducting lines between devices on silicon device chips is widespread in the Integrated Circuits industry. One of the primary advantages associated with the use of polycrystalline silicon for electronics applications is that it can be controllably oxidized to form an insulating, passivating and protective SiO_2 film on the surface. However, several reliability problems with the oxide have arisen. The oxide grown on polycrystalline silicon has been found to have higher conductivity, increased numbers of premature dielectric breakdowns and initial shorts as compared with the oxide grown on single crystal silicon. A TEM study of the morphology of polycrystalline silicon films and the oxide grown therefrom has revealed that the polycrystalline silicon films become rough during oxidation, the oxide has thickness undulations and there is extensive intergranular oxidation. It is shown in the present study how these observations lead to an understanding of the major reliability problems associated with polycrystalline silicon.

Introduction

Polycrystalline silicon, poly-Si, is presently widely used in the electronics industry to fabricate highly conducting line interconnections between devices on integrated circuit chips. Films of poly-Si are usually doped with B, P, or As to achieve high conductivity and are grown to less than 10^3 nm thick by chemical vapor deposition, CVD, using gaseous SiH_4 as the source of Si. Blanket Si films are delineated using masking and etching techniques. CVD Si films prepared at a temperature of 650°C or lower are usually amorphous but further necessary high temperature processing such as doping, annealing and oxidation cause the films to crystallize to poly-Si.

The primary advantages associated with the use of poly-Si are twofold. First, the material, being Si, is compatible with other high temperature processing steps that are necessary for complete silicon device fabrication. Most metal films would delaminate or react during typical device processing. Secondly, the oxidation of poly-Si yields a self-passivating, protective and insulating SiO_2 film. This oxide called poly-ox, enables the preparation of multi-level devices using poly-Si lines with poly-ox insulation. Multi-level devices increase the device density on a chip.

The present study is primarily concerned with the second advantage, i.e. the oxidation of polycrystalline silicon. Notwithstanding the decided advantages associated with poly-Si, it was reported (1,2,3) that the oxide grown via the oxidation of poly-Si, poly-ox, displays significantly higher conductivity than the oxide grown from single crystal silicon. The higher conductivity of poly-ox leads to premature dielectric breakdown of the poly-ox films. In addition to this problem, a high indicence of initial electrical shorts was found with these shorts extending from the poly-Si conducting lines through an underlying oxide to either another poly-Si line or to a single crystal silicon substrate. This problem has occurred when metal contact holes were opened through the poly-ox to the poly-Si by masking and chemical etching procedures. The metal contact was evaporated Al. Apparently, the chemical etchant

($HF+H_20$) penetrated through the poly-ox, poly-Si, and underlying oxide leaving a hole into which the Al migrated and caused an electrical short.

Based on measurements of both dark and photocurrents, DiMaria and Kerr (2) have shown that the high currents in poly-ox are due to localized field enhancement effects. Since the poly-Si is composed of grains, these authors attribute the field enhancement to asperities on the poly-Si surface as a result of grains protruding from the surface. A field enhancement factor of 1.5-2 would explain their results. Anderson and Kerr (3) reported SEM observations of a rough poly-Si surface with asperities having a height to width ratio of 1.8. According to Lewis' calculations for an isolated protuberance of this dimension, a field enhancement of nearly 10 can be expected. Anderson and Kerr (3) require a factor of more than 3 to explain their data. However, since they show that the poly-Si surface asperities have an areal density of more than 5×10^9 cm^{-2}, Lewis' (4) calculations show that there is a reduction in field enhancement from 10 for the isolated case to less than 2 for the case of Anderson and Kerr. Therefore, localized field enhancement effects due only to poly-Si surface asperities do not explain all the poly-ox conductivity data. Furthermore, TEM surface replica studies to be shown later do not show the same high degree of surface roughness as reported by Anderson and Kerr (3).

A detailed study of the oxidation of poly-Si (5) has led to an identification of the characteristic features of this type of oxidation. The results of this previous study (5), to be reviewed in the present paper, yield explanations for the origin of poly-Si surface asperities and identifies another way in which the actual poly-ox electric field is locally higher than anticipated. In addition, the previously mentioned initial shorting problem with poly-Si can be understood from the oxidation results. Therefore, the present study deals firstly with describing the morphologial aspects of the oxidation of poly-Si, then use is made of these results to understand the electrical properties of poly-ox. Hence, the structure - property relationships will be demonstrated.

Experimental Procedures

All the polycrystalline silicon films were deposited onto oxidized single crystal silicon slices. The silicon slices were commercially available 2Ω-cm p-type silicon chem-mechanically polished on one side, 3.2 cm in diameter and .02 cm thick with (100) orientation. Prior to any film preparation, the silicon slices were thoroughly cleaned according to a previously published procedure (6). Oxidations of single crystal and polycrystalline silica were carried out in fused silica tubes inside resistance heated tube furnaces with pure dry O_2 flowing. The O_2 is fed into the oxidation furnaces from a liquid oxygen source. The polycrystalline silicon films were chemically vapor deposited from a mixture of SiH_4 and N_2 onto the oxidized silicon substrates. For phosphorous doped polycrystalline silicon samples, $POC\ell_3$ was deposited upon the polycrystalline silicon films and driven in for 10 min. at 870°C to homogenize and electrically activate the P atoms.

TEM examination consisted of direct transmission through thinned foils and surface replication to produce a negative representation of the surface. The thinning was done by first dicing the samples into sizes to fit the electron microscope sample holder, secondly coating the entire sample with wax, thirdly, scratching a hole in the wax on the silicon substrate side of the sample. The sample is then exposed to an etchant which readily attacks silicon. We found that mixtures of HF and HNO_3 were very useful, since Si is attacked very vigorously by this solution but the oxide film somewhat more slowly. Therefore, etching from the substrate side slows down naturally when the silicon substrate is penetrated. Mixtures of ethylenediamene, - pyrocatechol and H_2O (7) were also found to be useful since this solution also attacks silicon vigorously but hardly etches oxide at all. For this etchant mixture it is necessary to maintain the solution temperature above 80°C and therefore the wax mask is destroyed. This etchant is particularly useful for making TEM observations of SiO_2 films. In addition to these two

chemical etchants, we also used ion milling to thin samples. The results and conclusions in this study are the result of concordant TEM observations using all three of the preparation procedures so as to avoid etching related artifacts.

The surface replicas involve several steps. First is the negative replication of the surface using a collodion solution then the evaporation of a thin electron transmitting layer of platinum - carbon alloy. Finally, the thick collodion is removed leaving a thin electron transmitting negative replica of the surface under investigation.

Experimental Results

The progressive stages of oxidation of a poly-Si sample are shown in Fig. 1. Prior to oxidation (1a) the sample displays large equiaxed silicon grains of nearly random orientation. Upon oxidation several morphological features develop. Firstly, oxide forms in the grain boundaries, i.e. intergranularly, as well as on the free polycrystalline silicon surface. Fig. 1(b) and (c) show that the grains (which are the darker outlined objects) are shrinking laterally as oxidation proceeds. In fact there is as much oxide formed on the edge of the grains as on the free surface. Secondly, the oxide formed from the oxidation of poly-Si does not have a uniform thickness. The poly-ox is thinner at the previous grain boundaries and thicker near the mid-grain regions. Furthermore, it is seen that as the oxidation proceeds the thickness undulations become more severe. Thirdly, on some areas of partially oxidized samples there was actual cracking of the oxide at previous grain boundaries.

Figures 2 and 3 show that as deposited poly-Si samples are rather smooth. The sample shown in Fig. 2 was deposited at 800°C, then a $POC\ell_3$ layer was deposited and the P driven in at 870°C for 10 minutes. After doping, the samples were given a short 10 min. oxidation at 1100°C. The oxide was then stripped and the surface was as shown in Fig. 2a. It can be seen that the grains have smooth surfaces except that there are ridges which outline the grain boundaries. The ridges are in fact grooves on the poly-Si surface, since the replicas are

negatives of the real surface. These grooves arise as a result of integranular oxidation and subsequent removal of the oxide from the grain boundaries. Upon further oxidation the surface of the oxide is rough as shown in Fig. 2b. When the oxide is removed Fig. 2c shows that the poly-Si surface displays even larger and sharper surface features as compared with Fig. 2b. Fig. 3 shows a sample which was prepared at a lower temperature of 650°C, $POCl_3$ doped identically to the sample in Fig. 2 but then mildly oxidized at 800°C and the oxide was stripped prior to Fig. 3a. Again this series of micrographs shows that the poly-Si surface stripped of oxide is rougher than the poly-ox surface.

In order to determine if the oxidation temperature is important in altering the poly-ox surface morphology, the same poly-Si sample as shown in Fig. 1 and 2 was oxidized to about the same extent at both 800°C in Fig. 4a and 1150°C in Fig. 4b. These micrographs show that the thickness undulations in the poly-ox are more severe for the lower oxidation temperatures.

Model for Poly-Si Oxidation

The combined experimental results above provide the basis for a descriptive model for the oxidation of poly-Si. This model will now be presented and following the model the various reliability aspects of poly-ox will be discussed.

The conversion of Si to SiO_2 involves an increase in volume by a factor of ~2.2. For the case of intergranular oxidation, as is observed for poly-Si, this increase of volume within the grain boundaries means that a large compressive stress is anticipated to develop during oxidation unless the required volume is obtained. For the oxidation of a free Si surface, the oxide expands outward as it forms. However, deep within a grain boundary this free expansion is not possible. It is also observed that poly-Si films can be totally oxidized and the films do not peel or delaminate or otherwise fail. Stress measurements on poly-Si films before and after oxidation showed only a slightly increased (<10%) compressive stress (5). Therefore

either Si and/or SiO_2must flow during oxidation of poly-Si to create the required volume. If it is assumed that SiO_2 flows, then the oxidizing grain boundaries would serve as sources of SiO_2 and the oxide would flow out of the grain boundaries as it is produced. This would result in thicker oxide near underlying grain boundaries than over mid-grain regions. If Si flows, then the Si would migrate from the boundaries to the mid-grain regions leaving less Si near boundaries and more near the mid-grain regions to fuel the oxidation. This would result in thinner poly-ox over grain boundaries as is in fact observed in Figs. 1 and 4. Therefore, it is likely that Si is the predominant migrating species under oxidation conditions. This mechanism can be understood with the aid of Fig. 5. This Figure shows that as an idealized grain morphology (Fig. 5a) is oxidized (5b, c, d) a compressive stress develops due to the molar volume increase from Si to SiO_2. When the stress, τ, exceeds a critical value under specific oxidation conditions, Si flows in the direction of the arrows away from the oxidizing grain boundaries. In this way the necessary volume is produced to keep τ at the critical value. This type of plastic deformation is referred to as Nabarro-Herring creep (8,9).

Structure-Reliability Relationships

As mentioned previously there are three poly-ox reliability implications to be discussed: high leakage currents in poly-ox, premature failure related to the high leakage currents and initial electrical shorts between poly-Si lines and the substrate.

From the oxidation results shown in Figs. 1, 2 and 3 it is clear that the oxidation of poly-Si causes roughness to develop both in the poly-ox as thickness undulations in the oxide itself and on the poly-Si surface via the intergranular oxidation.

It is seen in Fig. 1 b, c and d for incompletely oxidized poly-Si that the area of the thinnest poly-ox regions is small compared to the thicker regions of oxide. With the use of conventional optical (interference, ellipsometry) or mechanical (step height) film thickness measurement techniques,the measured oxide film thickness will be weighted toward the larger

area and therefore thicker poly-ox regions. The electric field values reported in the literature (1,2,3) are calculated from the applied voltage divided by the measured poly-ox film thickness. Therefore, these electric field values will be erroneously low since they are based primarily on the maximum film thickness while the observed oxide currents are primarily related to the minimum thickness or maximum field conditions. As estimated from the TEM micrographs there is about 30% thickness fluctuation in the oxide on poly-Si. An overestimate of the film thickness of 30% would yield a calculated electric field 1.4 times lower than the maximum field which determines the conductivity. From DiMaria and Kerr's data (2) a factor of 1.5-2 is required to bring the poly-ox conductivity data in agreement with oxide grown on single crystal silicon. Therefore the observed poly-ox thickness fluctuations can also be responsible for the high poly-ox currents in addition to the poly-Si asperities (3).

It was shown that the poly-Si surface became roughened during oxidation. The intergranular mode of oxidation causes the grains to shrink laterally hence the height to width of the Si protrusions increases. Lewis (4) has reported that cathode surface protuberances can cause local field enhancement effects and that the height to width ratio and proximity of the protuberances are important factors that determine the actual amount of the field enhancement. According to Anderson and Kerr (3) poly-Si surface asperities with a height to width ratio of ~2 are found and with an areal density of $\sim 5 \times 10^9$ cm^{-2}. These numbers yield a mean field enhancement factor of less than 2 according to the calculations of Lewis (4). Anderson and Kerr (3) report a field enhancement of 10 from Lewis' calculations but it appears that they only considered isolated surface asperities while their SEM micrographs show closely spaced surface irregularities. Therefore, poly-Si surface asperities and thickness undulations in the poly-ox probably contribute nearly equally to the higher than expected currents in the oxide. Anderson and Kerr (3) also report that poly-ox grown at higher temperatures yield relatively lower conductivities but never as low as the thermal oxide grown from single crystal silicon. This high temperature effect may be due to the fact that the thickness undulations are minimized because of viscous flow of SiO_2 in addition to Si creep at

the higher temperatures. Fig. 4 substantiates this idea by showing a smoother poly-ox grown at the hgher temperature.

The shorting problem is easily understood by reference to Fig. 6. Fig. 6a shows aligned or nearly aligned grain boundaries which when exposed to oxidizing conditions can cause oxide penetration deep within the poly-Si layer and even through the poly-Si. When the poly-ox is removed in HF based etchants to expose the poly-Si for Al contact metallization, a hole is also etched through the integranular oxide and through the underlying oxide. The Al metallization will cause metal to short from the top contact to the substrate through the etched hole as shown in 6c.

Conclusions

The electrical reliability problems associated with poly-ox have been shown to be related to the morphology of the poly-Si as surface roughness, to the morphology of poly-ox through oxide thickness undulations and to intergranular oxidation. Therefore, certain electrical properties of poly-Si and poly-ox have been explained as a result of understanding the mode of oxidation of poly-Si, specifically the resulting poly-Si and poly-ox structures.

Acknowledgements

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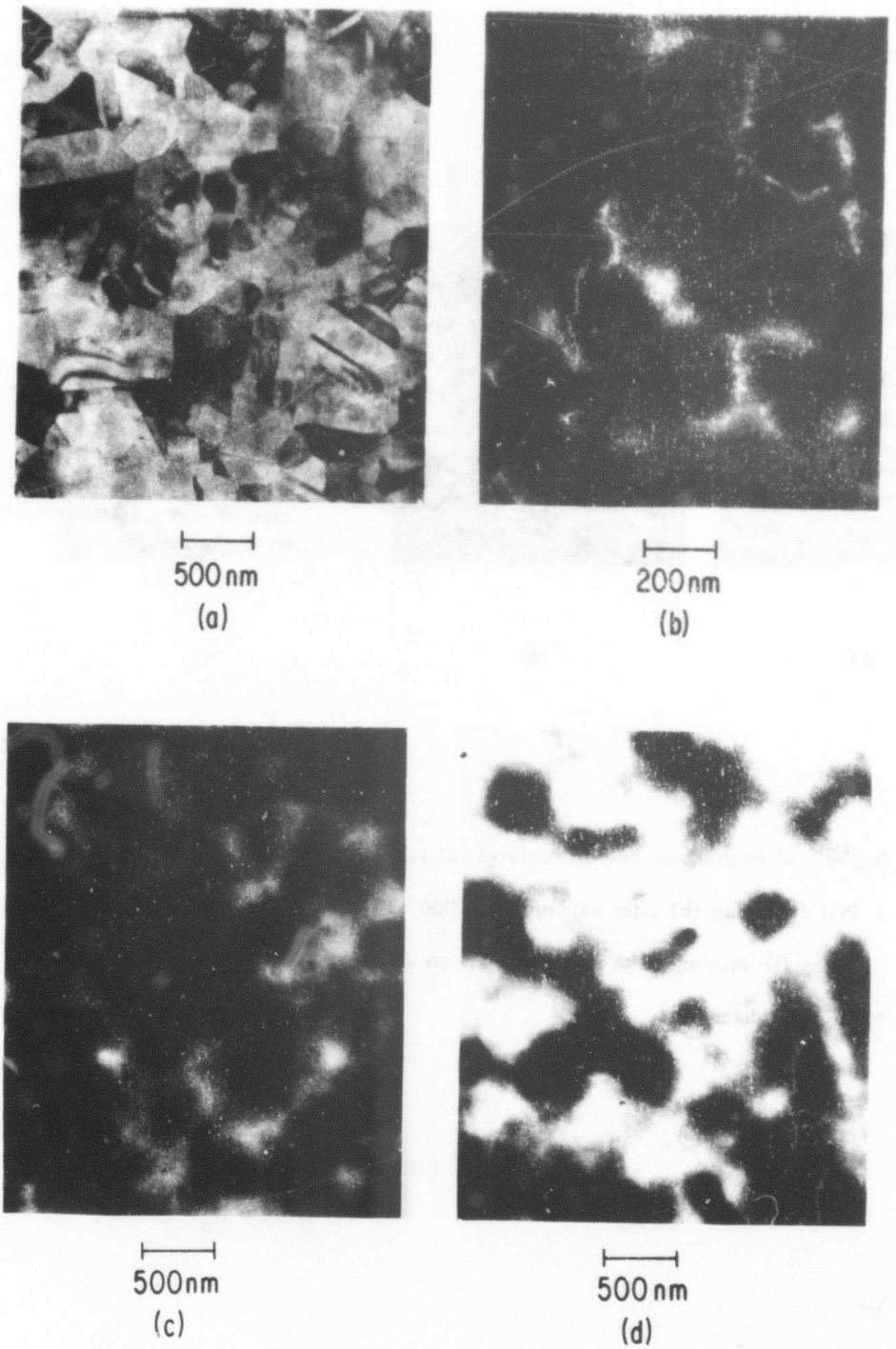
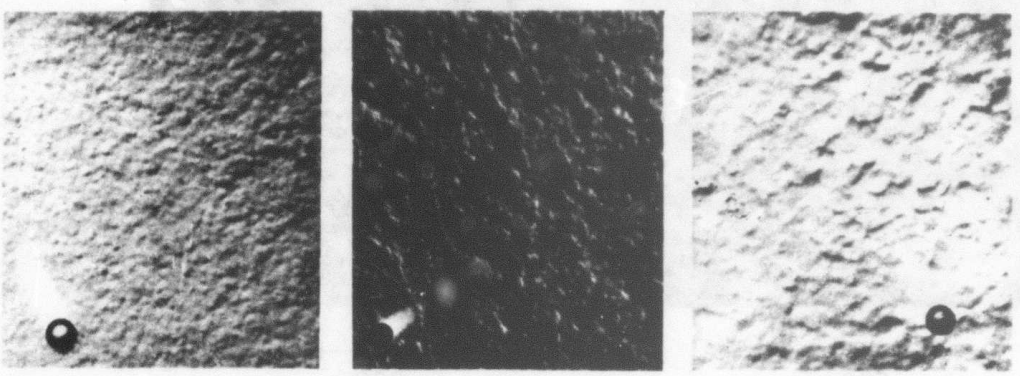


Figure 1 CVD polycrystalline Si films at various stages of oxidation (a) unoxidized, (b) 50 nm surface oxide, (c) 150 nm surface oxide, (d) completely oxidized.



(a) (b) (c)

Figure 2 Replicas of poly-Si and poly-ox surfaces (a) poly-Si, CVD preparation at 800°C + $POC\ell_3$ doping (b) after oxidation at 1000°C for 1 hr., (c) after removal of oxide by HF etching. The magnifications are identical and the latex spheres are ~500 nm in diameter.

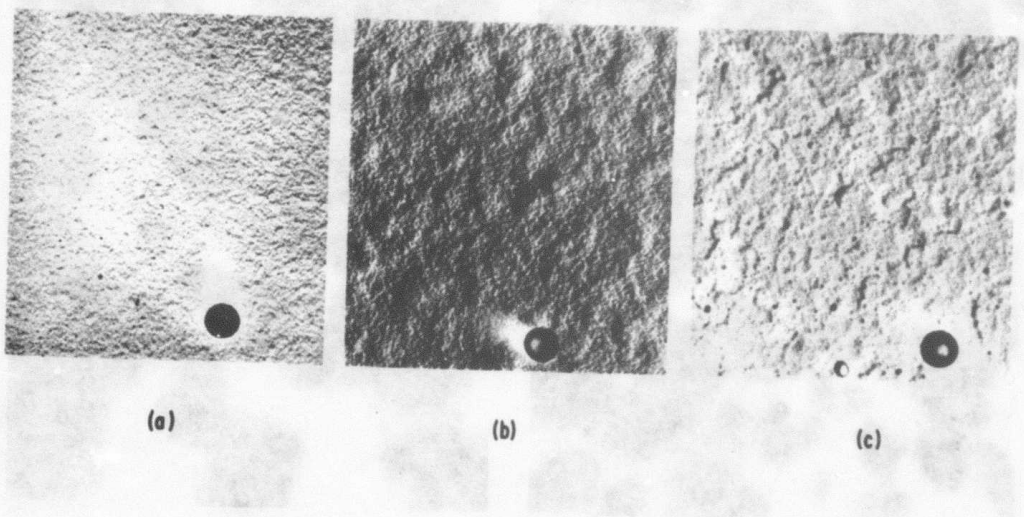


Figure 3 Replicas of poly-Si and poly-ox surfaces (a) poly-Si, CVD preparation at 650°C + $POC\ell_3$ doping, (b) after oxidation of 1000°C for 1 hr., (c) after removal of oxide by HF etching. The magnifications are identical and the latex spheres are ~500 nm in diameter.

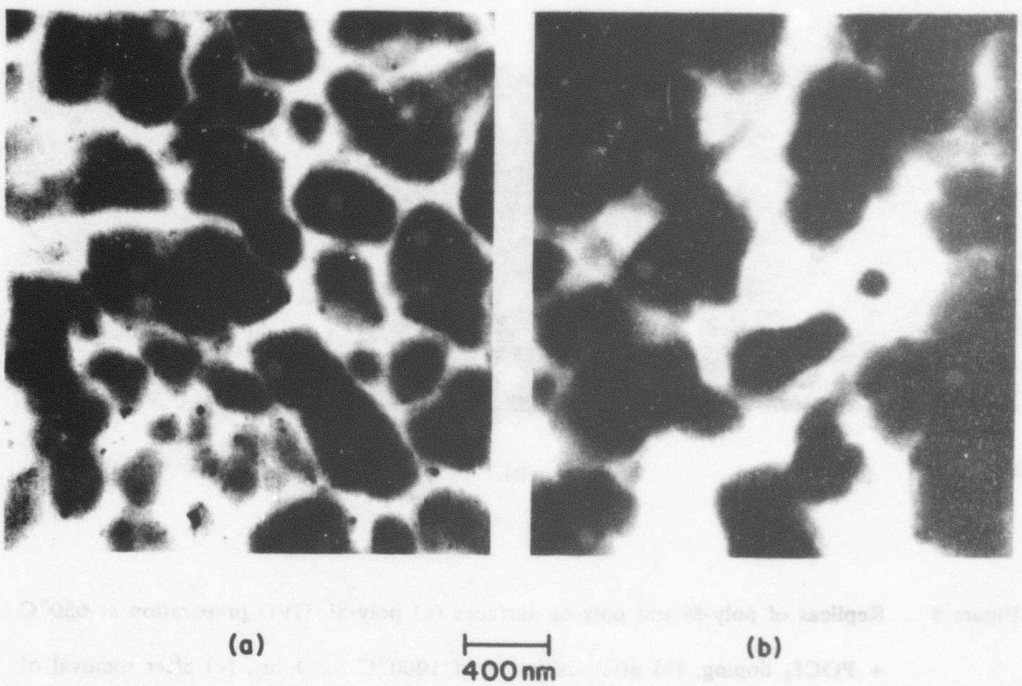


Figure 4 Poly-Si sample as in Fig. 2, oxidized to the same extent in dry O_2 at (a) 800°C and (b) 1150°C.

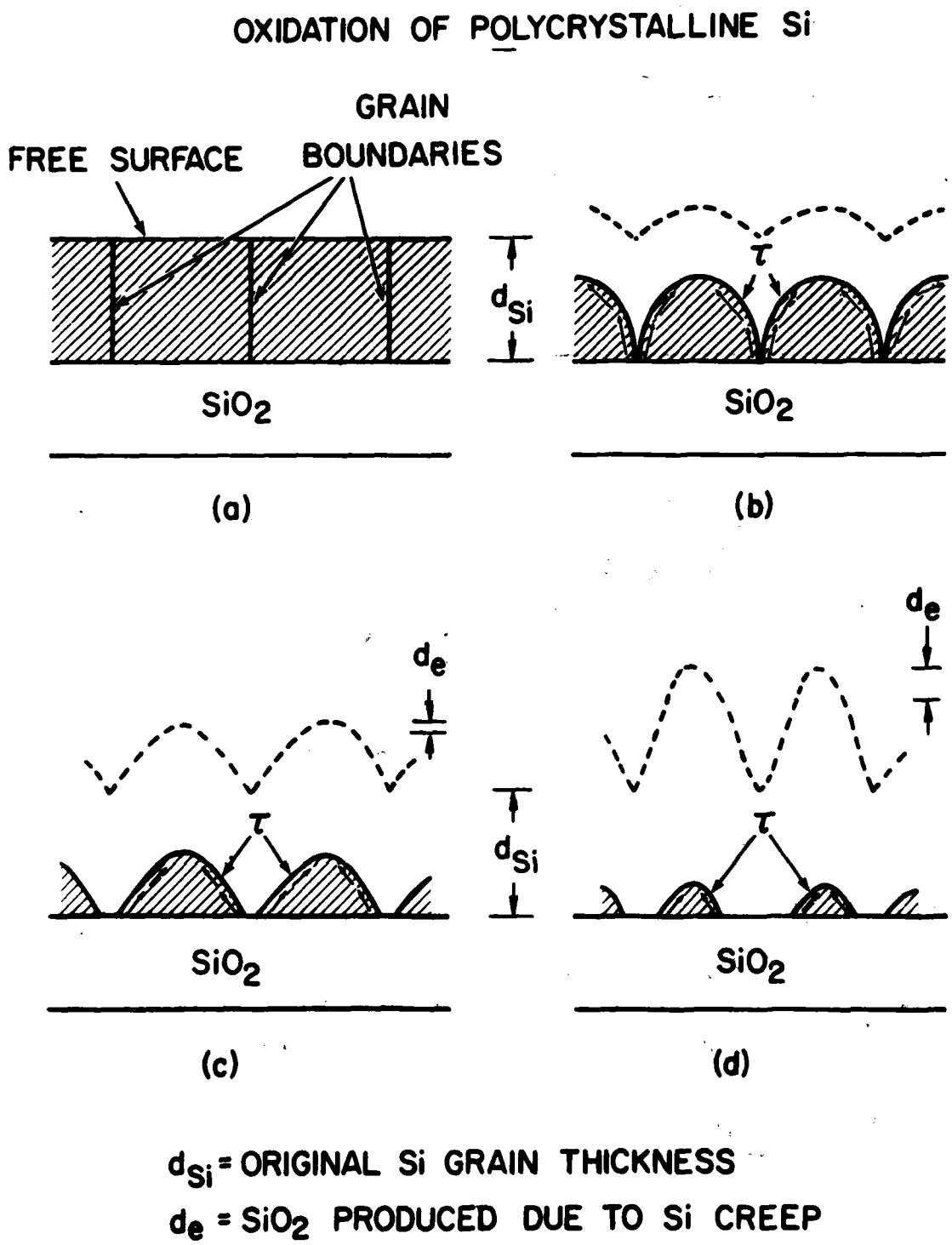


Figure 5 Model for the intergranular oxidation of poly-Si, (a) unoxidized ideal grain structure, (b) (c) (d) show progressive stages of oxidation.

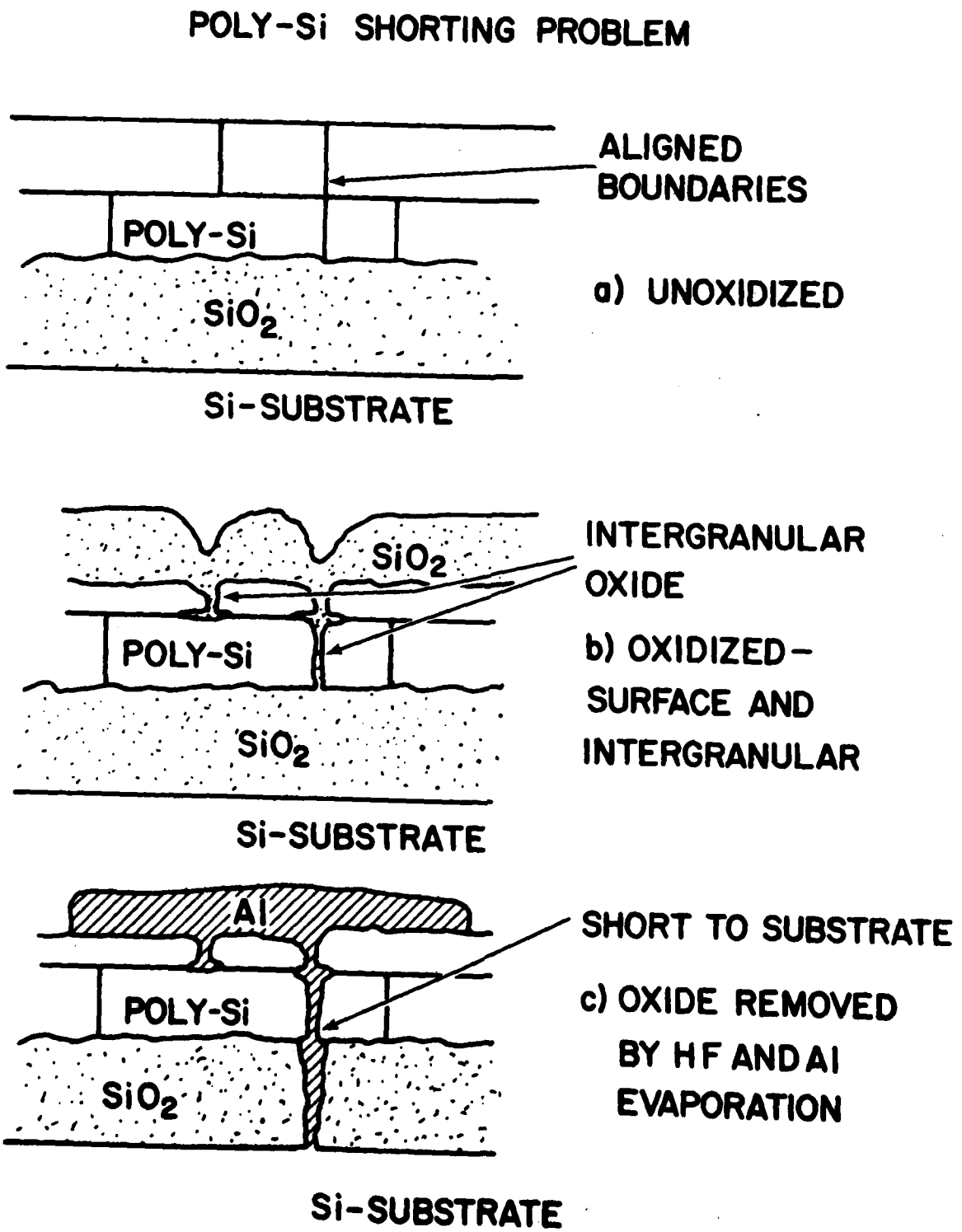


Figure 6 Poly-Si shorting problem (a) idealized unoxidized aligned poly-Si grains (b) after intergranular oxidation (c) after HF removal of the intergranular oxide and Al metallization.

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THREE DIMENSIONAL DEFECTS IN AMORPHOUS DIELECTRIC FILMS

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Abstract

This study shows TEM observations of defects in amorphous dielectric films. The defects are of the types that cause degraded electrical properties of the films. Defects related to the film processing parameters, the substrates upon which the films are grown and impurities in both the film growth ambient and substrate are shown. In many cases the nature of the defects are elucidated. This study demonstrates that defects are observable in thin films and that the defect structure of these materials provides an explanation for some of the electrical behavior observed for these films.

Several studies (1-4) have shown that dielectric breakdown statistics on amorphous dielectric films can be interpreted in terms of defects in the films. Film defects defined in this way were shown to vary with film processing parameters and certain film growth ambient additives (1-4). These studies have provided an important method that enables the observable statistics of dielectric breakdown to be related to film defects. However only little direct information on the nature of the film defects is obtained from electrical measurements. There have been numerous successful attempts to directly observe defects in dielectric films and Kern (5) has surveyed and compared the reported techniques. The emphasis of Kerns' review (5) is on techniques that enable the defects to be counted. Kern also points out that transmission electron microscopy, TEM, is capable of resolution sufficient to directly image film defects, yet specific TEM studies which show defects are absent from his review.

Therefore, the primary purpose of the present study is to show numerous TEM observations of actual defects in amorphous dielectric films and thereby demonstrate that defects are directly observable. Another purpose of this study is to attempt to correlate the TEM observations of defects with electrical measurements of defects. In several cases the correlations were found to be strong. Lastly, an attempt will be made to explain the origin of the observed defects. In many cases the origins of the defects can be related to processing parameters, the substrates upon which the films are grown or impurities in the film growth ambient. The experimental results to follow will be divided into these three categories.

Most of the experimental results to be reported are concerned with amorphous SiO_2 films, therefore, it is useful to consider the types of defects in SiO_2 that are likely to be present and that can be observed by TEM. The atomic arrangement in amorphous SiO_2 has been extensively studied (see for example refs (6) and (7)). Of particular relevance is the observation that despite the use of such diverse preparation techniques as glow discharge, thermal oxidation and preparation from the melt, the SiO_2 atomic arrangements were essentially unchanged (7). Yet the MOS field is replete with investigations which demonstrate that the final

electrical behavior expected from an SiO_2 film is intimately dependent on the exact method of preparation. It has also been established that for many amorphous materials some of the physical properties are altered by the materials preparation procedures (8). These observables are similarly encountered for crystalline materials wherein the defect type and quantity has been established as causitive. For amorphous materials it seems reasonable to expect the occurence of point defects (vacancies, interstitials and atomic impurities) and three dimensional defects (voids, cracks and particulates) since these latter types of defects do not require an extended regular array of atoms. Some of the three dimensional defects are anticipated to be larger than 2nm and therefore easily detectable by TEM and the observation of these types of defects is the subject of the present study.

Specifically, the results to follow embody TEM observations of defects in SiO_2 and Si_3N_4 films. The SiO_2 and Si_3N_4 films are prepared by a variety of techniques: thermal oxidation of single crystal Si, polycrystalline Si, porous Si, and heavily B doped Si; thermal oxidation using O_2 at 500 atm; thermal oxidation using H_2O and dry O_2, very thin SiO_2 films and HCl in O_2; chemically vapor deposited (CVD) SiO_2 and Si_3N_4 prepared both stoichiometric and Si rich; SiO_2 doped with Au, Al, As and NaCl; SiO_2 annealed at high temperatures. For convenience the observations are categorized according to processing variables (temperature, pressure, CVD versus thermal), the substrates (single crystal, polycrystal and porous Si) and impurities introduced in the gaseous ambient or solid phase. The observations of three dimensional defects in these materials, many of which are correlated to other physical properties of the material, affirms the authors belief that it is useful to describe much of the behavior of amorphous films in terms of the defect structure of the films.

Experimental Procedures

All of the films used in the present study were prepared by established techniques about which there exists considerable numbers of publications (see for example Ref. 9 for a description of chemical vapor deposition CVD, and oxidation processes for preparing thin films, Ref. 10 for porous Si films, and Ref. 11 for high pressure oxidized SiO_2 films.) All of the films were deposited either directly onto chem-mechanically polished and thoroughly cleaned single crystal Si substrates or onto thermally oxidized Si substrates.

For the purpose of TEM observations the samples were thinned from the Si substrate side by several chemical techniques (HF + HNO_3 mixtures, ethylenediamine + pyrocatechol + H_2O mixtures) and ion milling. Several techniques were used to avoid confusion arising from etch related microstructure.

Experimental Results

Processing Related Defects. Fig. 1 summarizes our results on the exposure of SiO_2 to high processing temperatures. Fig. 1a shows a typical area of an SiO_2 film grown in dry O_2 at 1100°C which has no observable defects. Fig. 1b shows a similarly grown sample which shows crystalline Si inclusions. Fig. 1c displays an oxide grown at 1100° as above but then annealed in N_2 at 1150°C for extended periods. The observations show that free Si inclusions are sometimes found in as-grown SiO_2 when the oxidation temperatures are above 1000°C and many more and usually larger Si inclusions are observed when the oxides are annealed at temperatures above 1000°C in Ar or N_2. Additionally, as will be shown later under the heading of impurity related defects, HCl additions to the oxidation ambient also increase the number and size of the Si inclusions. It is interesting that these TEM observations correlate with the findings of Osburn and Ormond (2, 3, 4) who report that dielectric breakdown related SiO_2 defect densities are increased for higher temperature oxidations, further increased with

high temperature inert gas anneals and more than 5% HCl in the ambient also increases the number of defects.

Previously we thought that these Si occlusions were produced as a result of the solid-solid reaction of Si with SiO_2 at the Si-SiO_2 interface (12). A disproportionation reaction yields gaseous SiO which can diffuse away from the interface where equilibration would again yield Si. The transport is summarized as:

$$Si(s) + SiO_2(s) = 2SiO(g)$$

which proceeds to the right at the interface and to the left producing Si away from the interface. The thermochemical calculations shown in Fig. 2 show that a considerable amount of Si is carried into the gas phase as SiO and therefore under non-oxidizing conditions the above chemical transport reaction may be operative to produce the free Si in the films i.e. under inert gas annealing. Extensive thermochemical calculations of Gulbransen and Jansson (13) demonstrate that for a practical but low oxygen pressure, $Po_2 = 10^{-12}$ atm, the value for P_{SiO} is some four orders of magnitude lower than for inert annealing as shown in Fig. 2. For more realistic oxidizing conditions where Po_2 will be greater than 10^{-7} atm, P_{SiO} is less than 10^{-16} atm. Therefore, it is not likely that the above disproportunation reaction is operative under oxidation conditions.

Typically, CVD dielectric films as compared to thermal SiO_2 exhibit higher dielectric breakdown densities, increased trapping and larger conductivities. This degradation of electrical quality may be due to the occurence of occluded particles in the films. Fig. 3 shows occluded SiO_2 and Si_3N_4 particles in CVD SiO_2 and Si_3N_4 films. We have observed this type of particulate to some degree in all the CVD films studied. The origin of this particulate seems to be well understood and we are able to alter the size and number of the particulates by altering the specific CVD conditions (14). An analysis of the important parameters is made with reference to Fig. 4. The "reaction volume" of the system depicted in Fig. 4 is that

volume in the CVD reactor in which a substantial amount of reaction occurs. For most CVD reactions this volume can be defined using temperatures. At a fixed power input to a furnace, lower and higher relative flow rates yield respectively V_1 and V_2 as relative reaction volumes. From our definition it is seen that the initial reactant concentration, C_i, drops sharply at the boundary of the reaction volume. In terms of temperature this point is shown as T_m, the minimum temperature of the reaction volume. For reaction volume V_1, the concentration of reactant at the substrates, C_{R1}, is less than the initial concentration, C_i while for V_2, C_{R2} is about equal to C_i. This description demonstrates how the substrate region of the reaction can become more dilute in reactants for the larger reaction volume V_1 than for V_2. Due to the decreased gas phase reactant concentrations in V_1 there is less gas phase reaction, nucleation and particle growth near the substrates. Therefore, V_1 will result in less occluded particulate in the films. In Fig. 4 it is shown pictorially how flow rates alter the reaction volume; but other parameters such as temperature profile, reactor geometry and reactant injection method will also effect the reaction volume. Generally, any method that dilutes the reactant in the substrate region of the reactor will not only reduce the occluded particulate but will also reduce the film growth rate and typically a trade off between rate and reliability is made.

In addition to the effect of particulates in CVD films, it is possible to vary the overall-composition of the films and thereby alter the electrical properties of the film. The composition of the solid phase is determined by altering the gas phase concentration of reactants which are potentially condensable. For example in the reaction to produce CVD SiO_2 we have used N_2O and SiH_4. SiH_4 alone has the potential to produce solid Si upon pyrolysis but N_2O alone will produce only gaseous materials. Therefore, increasing the amount of N_2O beyond the value necessary to produce stoichiometric SiO_2 has no effect on the overall film composition. This situation is also true for the reaction of NH_3 and SiH_4 to produce Si_3N_4. In both cases an excess of N_2O or NH_3 is used in order to be certain that a stoichiometric product is obtained. Increasing the amount of SiH_4 in either of the above reaction schemes will produce a Si enriched film of SiO_2 and Si_3N_4 (15). Specifically, we have found that by decreasing the

ratio N_2O/SiH_4 for CVD SiO_2 and NH_3/SiH_4 for Si_3N_4 the overall Si content of the film increased. The electrical conduction behavior of these films was observed to be non-ohmic but for specified values of applied fields, the conductivity of the films increased with increasing Si content. TEM examination summarized in Fig. 5 of the "as prepared" films of Si rich SiO_2 and Si_3N_4 showed that the films have connected channels. The films were prepared for TEM by chemically etching away the underlying Si wafer with an etchant which vigorously attacks Si but hardly attacks SiO_2 at all. Therefore, the channel like etch features in the films were attributed to regions where free silicon existed prior to etching. It is reasonable to expect free silicon in these films because the phase diagrams show no Si - SiO_2 or Si - Si_3N_4 solid-solid solubility. Recently, we have re-examined these films and have substantial proof using TEM and ESCA (16a) that free silicon exists in these films as phase separated particles. These particles will cause severe electric field distortions and thereby increase the local injection of carriers into the film and hence will measurably increase the conduction currents (16b). Therefore, through the use of CVD the overall film composition can be varied and in many cases the electrical properties of the material will also be altered.

High pressure oxidation of silicon offers considerable processing advantages in terms of significantly reducing the oxidation temperature necessary to achieve a desired oxidation rate (11). As with any novel technique there are usually processing problems which may lead to film defects. Fig. 6 shows a particularly defective area of a high pressure dry oxygen grown SiO_2 film. The occlusions are amorphous material with about the same image contrast as the oxide. We believe that these occlusions are particles of fused silica dust which originates from the fused silica pressure vessel liner. It is likely that this type of particulate has contributed to the degraded electrical properties seen on some pressure oxidation runs. Future pressure vessel designs and operation procedures will reduce this problem.

CVD Si_3N_4 is widely used as an oxidation mask for certain device processing steps. Fig. 7 shows that at 1000°C in steam the Si_3N_4 film is beginning to crystallize and oxidize. Above

this temperature oxidation is rapid and the film is destroyed while below 1000°C the Si_3N_4 film is functional as an oxidation mask.

Substrate Related Defects. The oxidation of silicon requires the transport of oxidant from the ambient-oxide surface through the oxide to the oxide-silicon interface. Because of this oxidant transport, the oxide will form on all the surfaces of the substrate exposed to oxidant. For single crystal silicon substrates, oxidation is restricted to well defined and polished crystallographic planes and oxide forms on these planes. For polycrystalline and porous Si substrates the situation is more complex.

Fig. 8 shows a comparison of the oxide grown on single crystal and polycrystalline silicon. It is seen in 8b and c that on polycrystalline silicon the oxide forms intergranularly as well as on the free surface and in addition there exists thickness undulations in the oxide which replicate the previously existing polycrystalline Si grain boundaries (12). The end result of this oxidation mode is both a non planar oxide and roughened silicon surface. In a MOS configuration the applied fields will become distorted and resulting local electric field enhancement effects will cause unusually large currents and possibly premature dielectric failure (17, 18).

Fig. 9 shows the result of partial oxidation of porous silicon. The porous silicon was prepared by electrolysis in HF solutions (10). The openness of the pores permits oxidation to extend into the pores. This effect is similar to the oxidation into grain boundaries as mentioned above but occurs to a greater extent because the pores are more open and widely spaced. The TEM results show unoxidized silicon protrusions as well as an undulating oxide morphology. Therefore degraded electrical properties are expected for this MOS system.

It is seen that defective oxides result from the fact that oxidation of silicon provides an oxide which conforms both to the Si surface topology, (as a CVD film would), and to the reactivity of the surface. The surface reactivity is not uniform for polycrystalline and porous silicon as it is for single crystal silicon. This is due to the fact that many different crystalli-

graphic planes and irregularly shaped surface features exposed to oxidation alter the activity of the surface atoms.

Impurity Related Defects. In this section the impurities considered are either in the oxidation ambient (H_2O, HCl), or in the SiO_2 (B, As) or deposited on the SiO_2 and driven in (Au, Al, NaCl).

In a previous study (21) it was shown that very thin thermally grown SiO_2 films (less than 15nm), grown with H_2O in the oxidation ambient displayed fewer dielectric breakdown defects than films grown in dry O_2. · The film growth thickness versus oxidation time data for the H_2O grown oxide films was found to be more parabolic than dry O_2 grown films. The tendency of the silicon oxidation kinetics toward parabolic kinetics is evidence for the rate limiting step being the diffusion of oxidant (20) while linear kinetics is attributed to surface reaction rate limitations. In the context of very thin SiO_2 films, the relatively more parabolic behavior for H_2O grown films indicates that these films are more protective since the films provide a more efficient barrier toward penetration of oxidant. The TEM micrographs of the thin films summarized by Fig. 10, show that these films have inhomogeneities which lead to uneven attack by the etchants ($HF\text{-}HNO_3$) used to remove the substrates. Since it is known that HF based etchants etch less dense SiO_2 faster than more dense SiO_2 (21), it is likely that the faster etching inhomogeneities are less dense regions. The combined dielectric breakdown, oxidation kinetics and TEM results have led to the proposition that these films have micropores, and that there is a difference in the micropore structure between wet and dry grown thin SiO_2 films which explains the defect densities and kinetics data obtained on the films (19).

The addition of chlorine containing compounds, in particular HCl, to the silicon oxidation ambient has received considerable attention in recent years due to reported cleaning effects on the oxide. However, it was discovered that when large amounts of HCl are added at high oxidation temperatures, an increased number of dielectric breakdown defects are observed (3).

In addition it was shown that at temperatures above 1150°C and with 6% HCl in O_2, a vigorous reaction occurs at the Si surface which can cause blistering of the oxide (22, 23). It is clear from these latter studies that volatile silicon compounds are produced and the silicon surface is etched during oxidation with chlorine additives. Our TEM observations summarized by Fig. 11 show a similar kind but greater number of Si inclusions than observed for high temperature oxidation and annealing. In this case, Si transports from the Si - SiO_2 interface into the oxide via gaseous halides. The fact that silicon chlorides are produced in the presence of O_2 means that there also exists the possibility of production of CVD SiO_2 by reaction between the silicon chlorides and oxidant. Therefore a mixture of two types of SiO_2 (CVD and thermal) and possibly other intermediate phases of Si oxychlorides would exist as a result of HCl additions to the oxidation ambient.

In the studies of the oxidation kinetics of heavily B doped silicon (24), an amorphous phase was found to be present in the oxide as shown in Fig. 12. Based on the fact that B_2O_3 is usually found in the amorphous state and that B_2O_3 is expected to phase separate from SiO_2 (25-27), the minor phase is deduced to be B_2O_3.

It is known that ion implantation into SiO_2 produces damage in the oxide. In Fig. 13 we show that free Si can be produced from As ion implantation. Presumably oxygen is knocked out by the bombarding As ions. This leaves free Si which can crystallize during high temperature anneal. In the region where selected area diffraction showed the free Si, there appears to be damage in the oxide which did not anneal away. These damaged regions may be where the free Si can readily precipitate during anneal.

The use of Au and Al contacts for MOS devices is commonplace. There are reports (28, 29) that these metals are not as passive with SiO_2 as once believed and reactions have been identified which may cause serious device damage. In agreement with the literature (28) Fig. 14 shows a reaction to have occured between Au and SiO_2 after 800°C heat treatment in N_2. Reacted regions are clearly visible after removal of the unreacted Au. No new phases were

detected but the amounts of any new phases may be below TEM detection limits or the phases may be amorphous.

For the Al - SiO_2 situation we also confirm the literature results (29, 30) which show the production. of an aluminum oxide phase. Fig. 15 summarizes the result of annealing an Al on SiO_2 film structure at 700°C for 5 min. in N_2. Partially molten and reacted Al grains are seen in 15a as the darker features with the underlying SiO_2 as the lighter areas. Fig. 15b and c show the electron diffraction patterns for the Al grains in 15a and a new phase, respectively. This new phase appears to be γ Al_2O_3. In order to determine if the γ Al_2O_3 phase was the result of outer surface oxidation of Al rather than reaction at the Al - SiO_2 interface, the Al - SiO_2 TEM samples which did not initially show the new aluminum oxide phase were heated at 500°C for 30 min. in O_2 and re-examined in TEM. Fig. 16 shows the result of this O_2 anneal. The Al grains appear with some surface roughness due to oxidation of the Al surface. Spaces are seen around some grains (the lighter areas). Only Al diffraction lines were seen as shown in the insert. Since it is known that the outer Al surface is oxidized by the O_2 ambient, it is clear that the oxide produced from that reaction is amorphous therefore yielding no diffraction while the oxide produced by the reaction of Al with SiO_2 during the higher temperature inert ambient annealing is crystalline giving rise to the γ Al_2O_3 diffraction lines. This new phase is also observed for lower temperature but longer time inert ambient anneals. It is reported that this inert gas annealing and reaction provides a beneficial effect on MOS characteristics (31) in terms of reduced fixed oxide charge. This effect may be related to a change in the metal-oxide work function.

The degradation effects of Na in MOS devices is well known and the relationship of Na to dielectric reliability degradation has also been reported (32). Fig. 17 shows that NaCl has reacted with SiO_2 films and after removal of the Si substrate for TEM study, large holes appear in the oxide. We believe that these large holes were regions which were reacted with the NaCl producing a product which is dissolved by the ethylenediamine, pyrocatechol - H_2O

etchant which hardly attacks normal SiO_2. Surrounding the etched holes are unreacted and partially reacted NaCl. The reaction identified here between the NaCl and the SiO_2 may be the cause of the dielectric degradation of SiO_2 by Na.

Conclusions

A variety of differently prepared SiO_2 and Si_3N_4 films were observed by TEM. In all cases a distinctive microstructure was observed in each of the different films which could be related to process, substrate or impurity differences. In most cases the appearances of the unique microstructures or defects could be correlated with a degraded dielectric integrity of the film; and in several instances the origin of the defects was understood to a degree sufficient to eliminate the defects by changes of certain film preparation parameters.

It is demonstrated in this study that the directly observed defects in amorphous films provide an additional dimension to the description of the films properties. It is also clear that further work is required to fully substantiate the defect structure in amorphous films.

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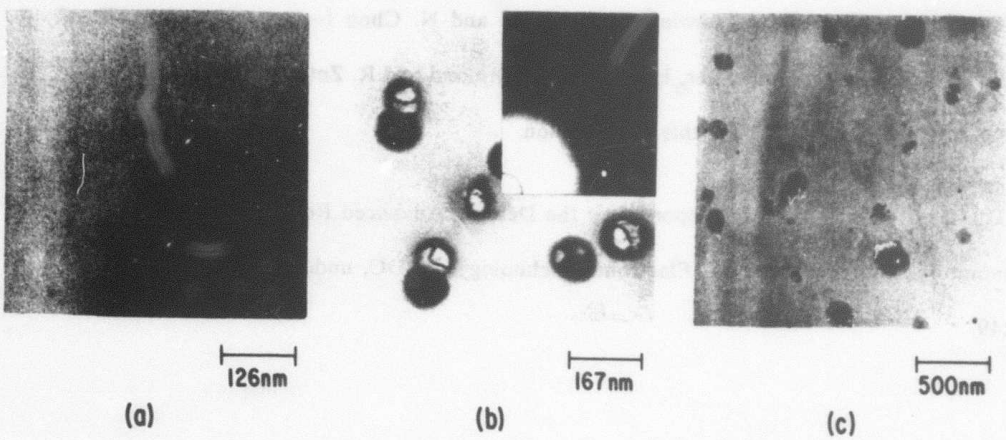

Figure 1. SiO_2 films grown in dry O_2 at 1100°C, (a) with no observable defects, (b) with Si inclusions and (c) annealed at 1150°C in N_2 for 24 hrs.

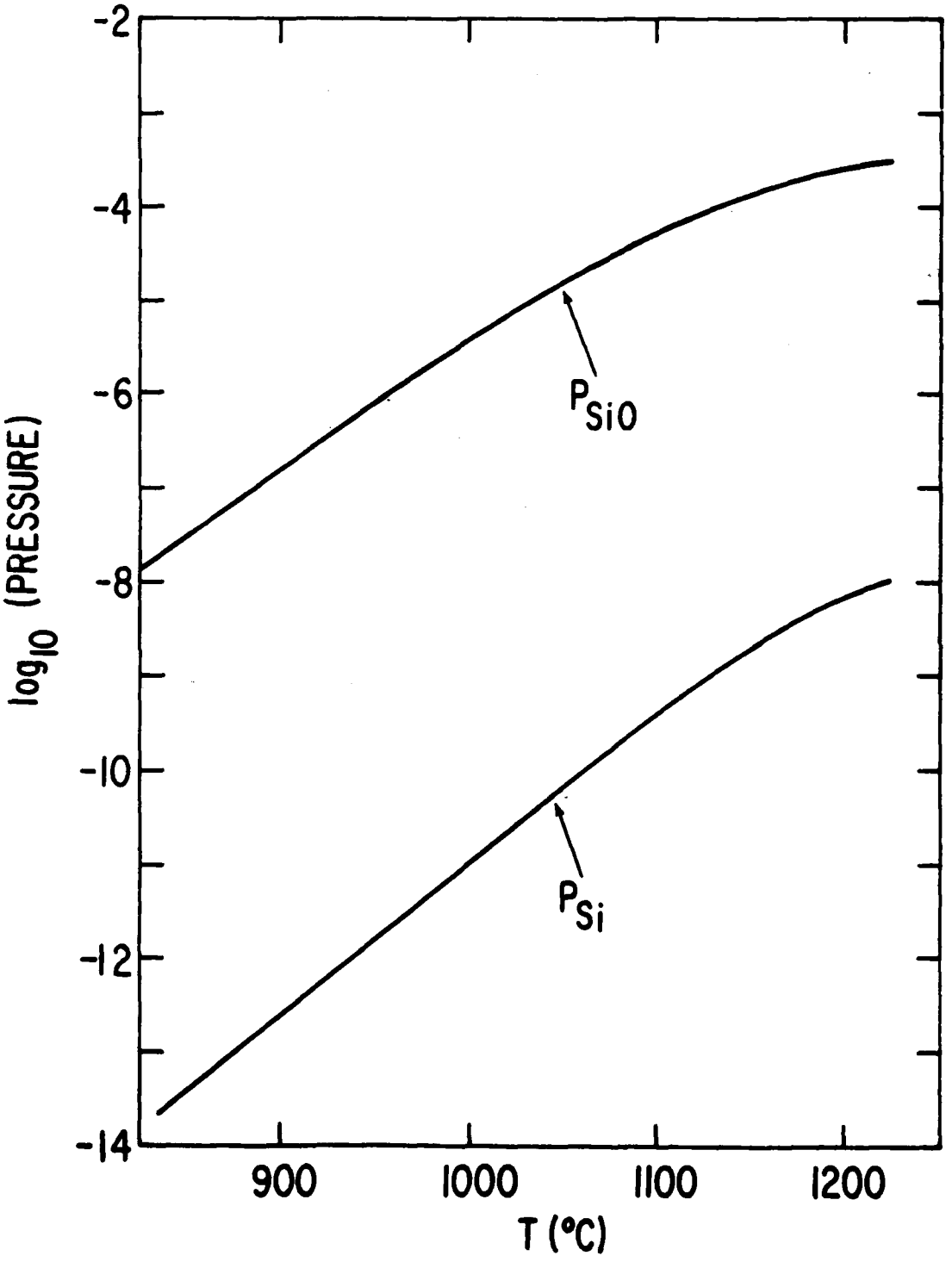

Figure 2. **Plot of vapor pressures of Si(g) over Si(s) and SiO(g) from Si(s) + SiO_2(s) = 2 SiO(g).**

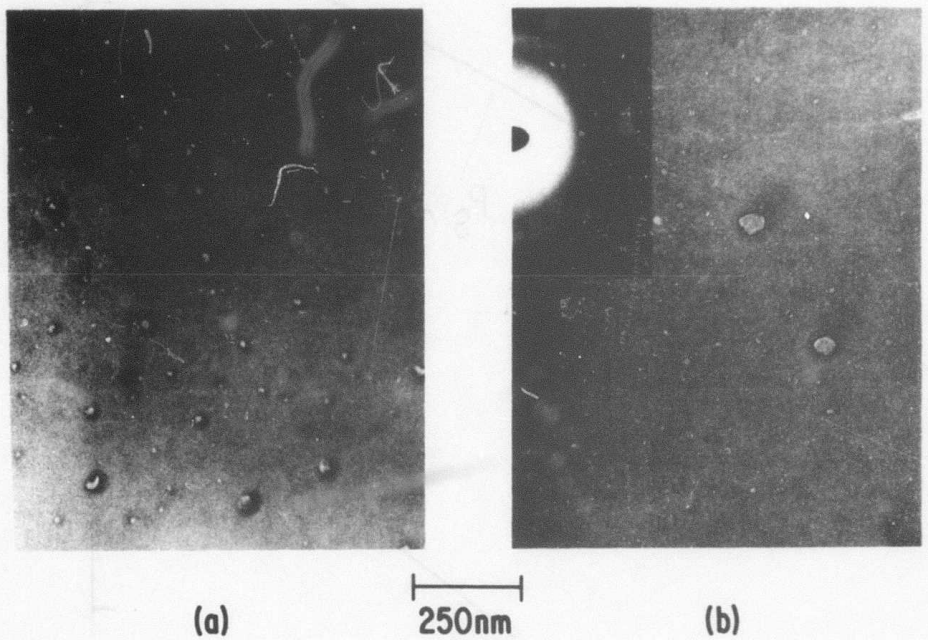

Figure 3. CVD SiO_2(a) and Si_3N_4(b) films showing occluded particles.

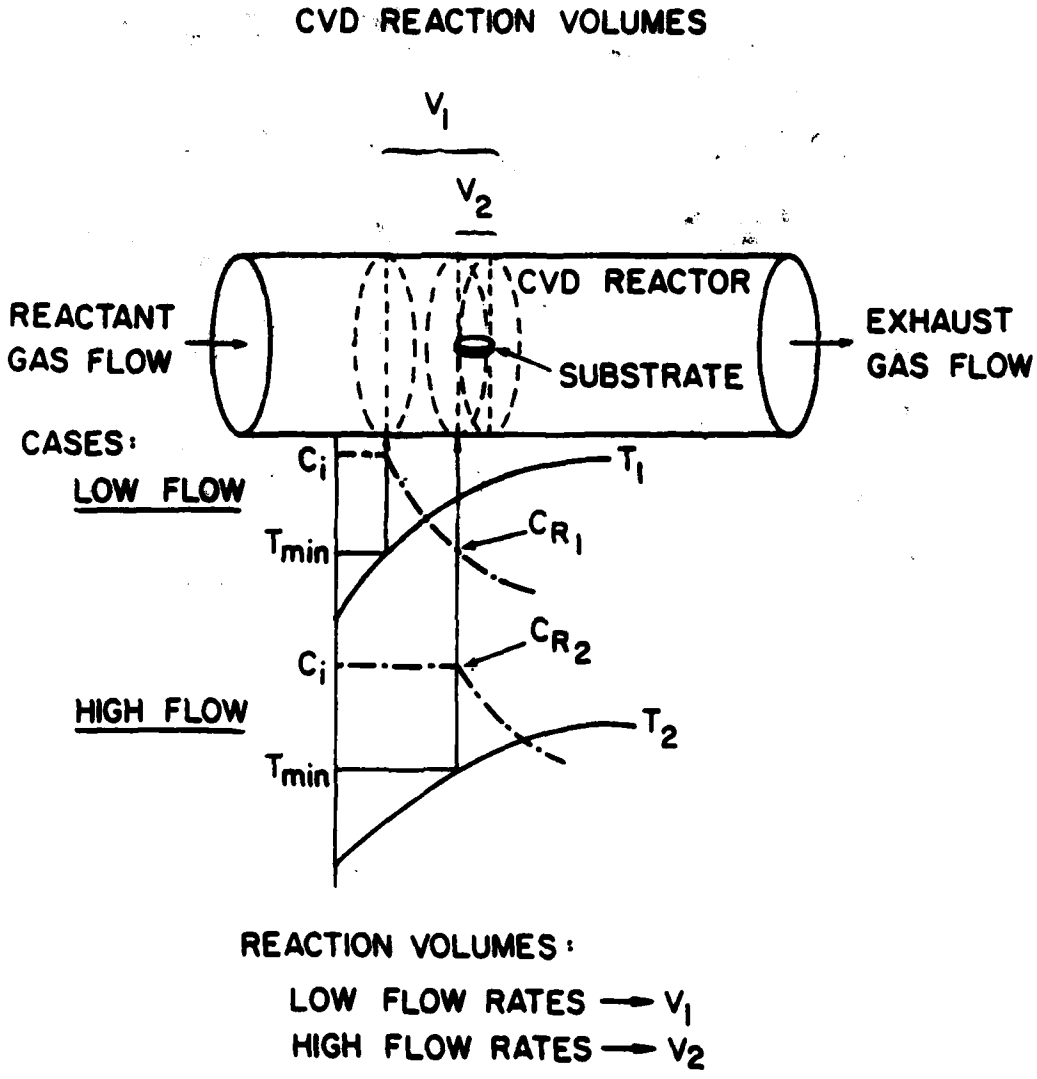

Figure 4. **Reaction volume variations with flow rates.**

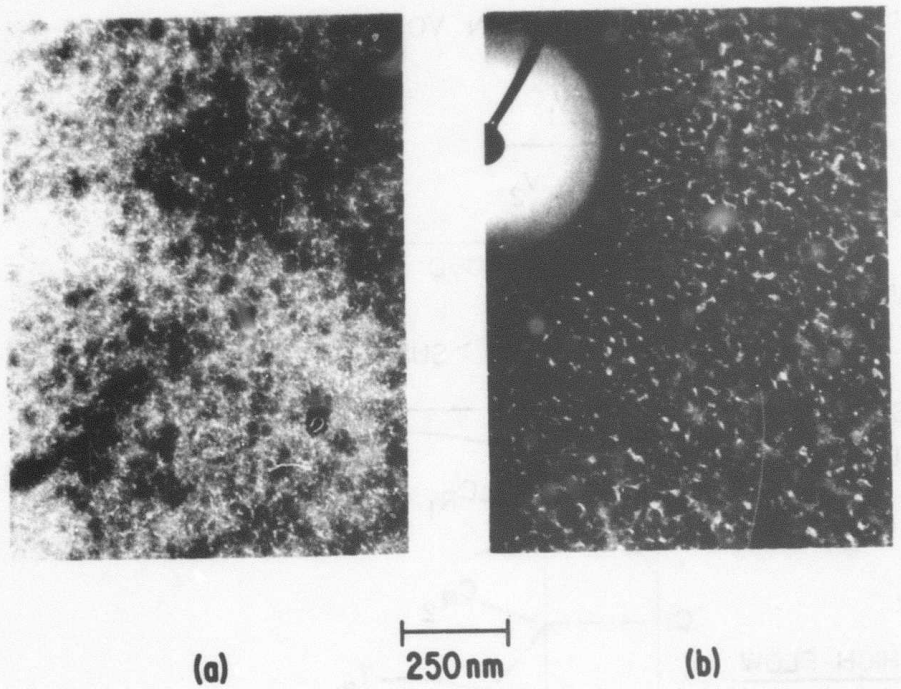

Figure 5. Si rich SiO_2(a) and Si_3N_4(b) films which have been etched to remove the free Si.

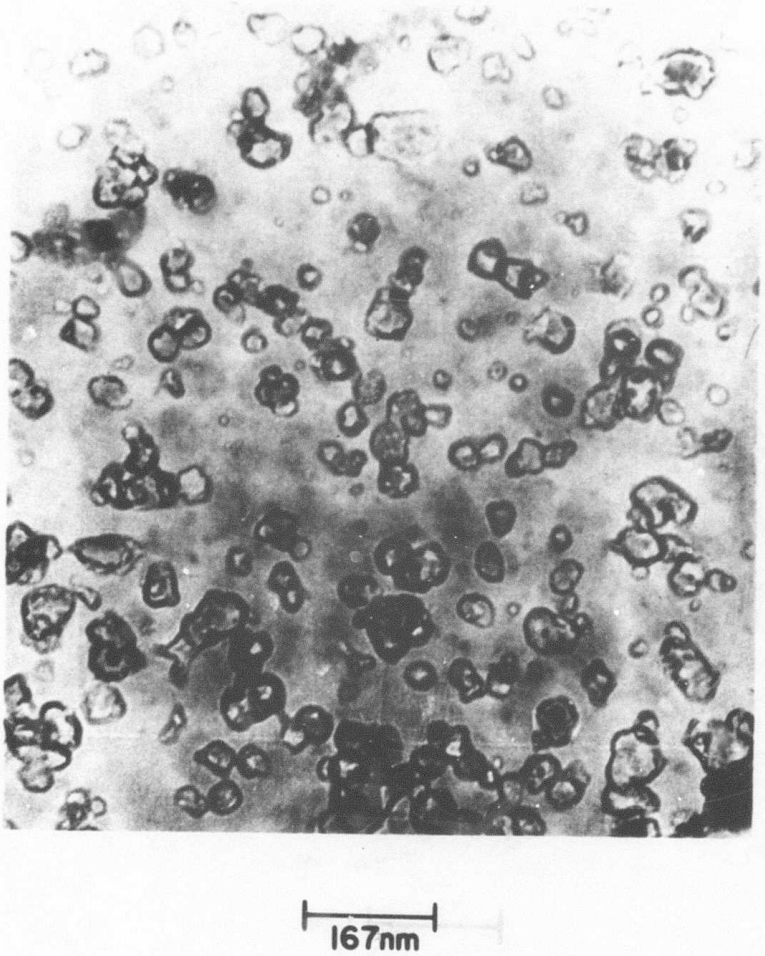

Figure 6. High Pressure (500 atm dry O_2 - 800°C) grown SiO_2 film showing a defective area with SiO_2 occlusions.

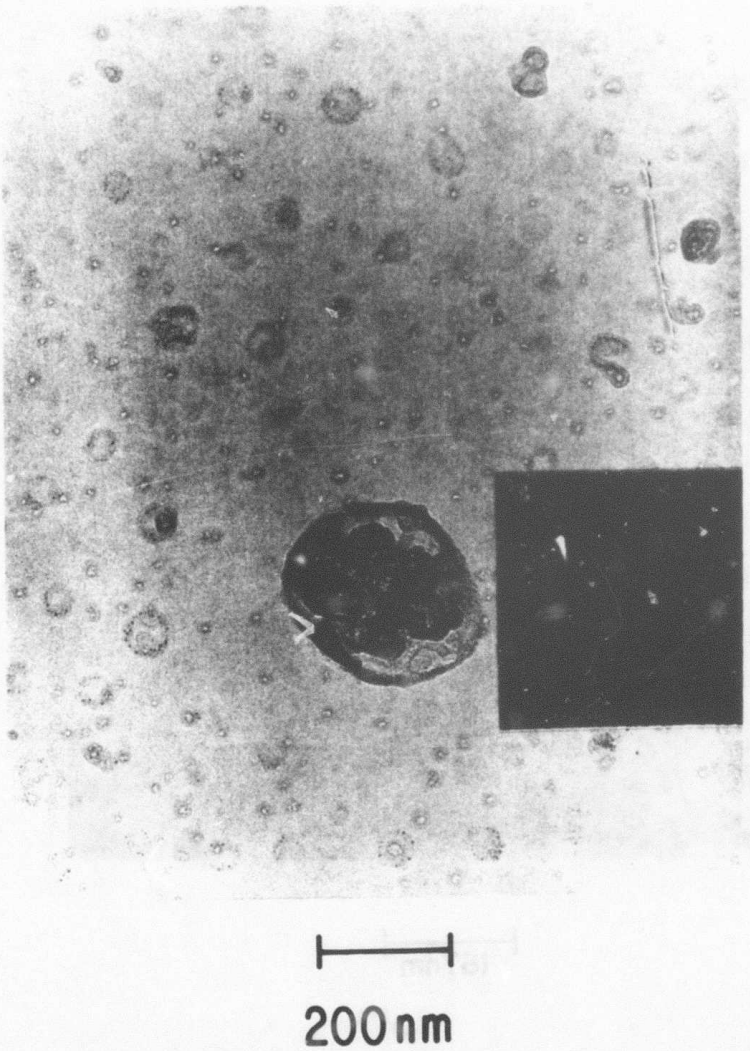

Figure 7. CVD Si_3N_4 film exposed to 1000°C steam showing surface crystallization. The insert shows a dark field micrograph of the large crystallite.

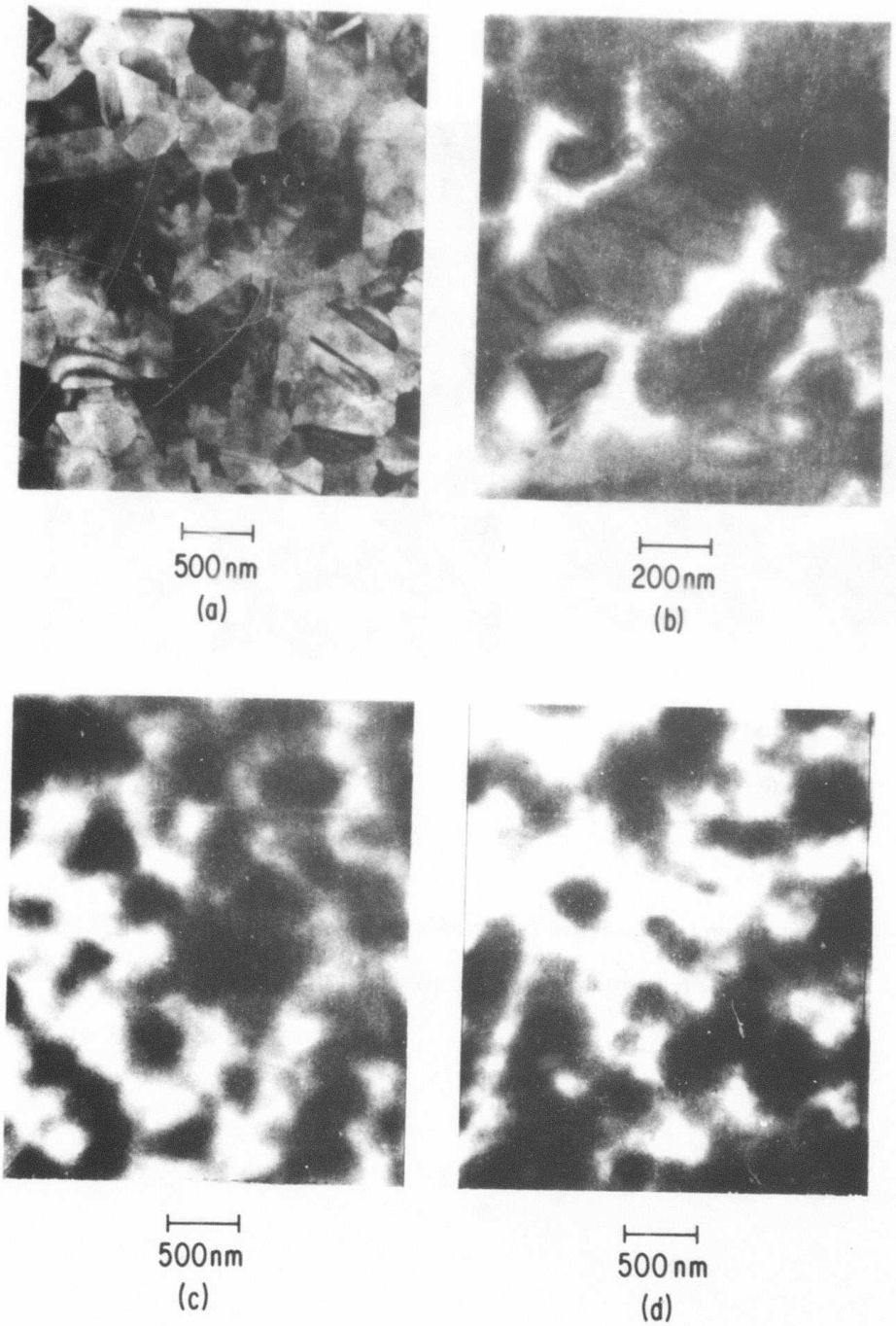

Figure 8. (a) Polycrystalline film grown by CVD and $POCl_3$ doped, (b) same as (a) but oxidized at 1000°C to yield 50 nm SiO_2 (c) oxidized to yield 150 nm SiO_2 (d) completely oxidized.

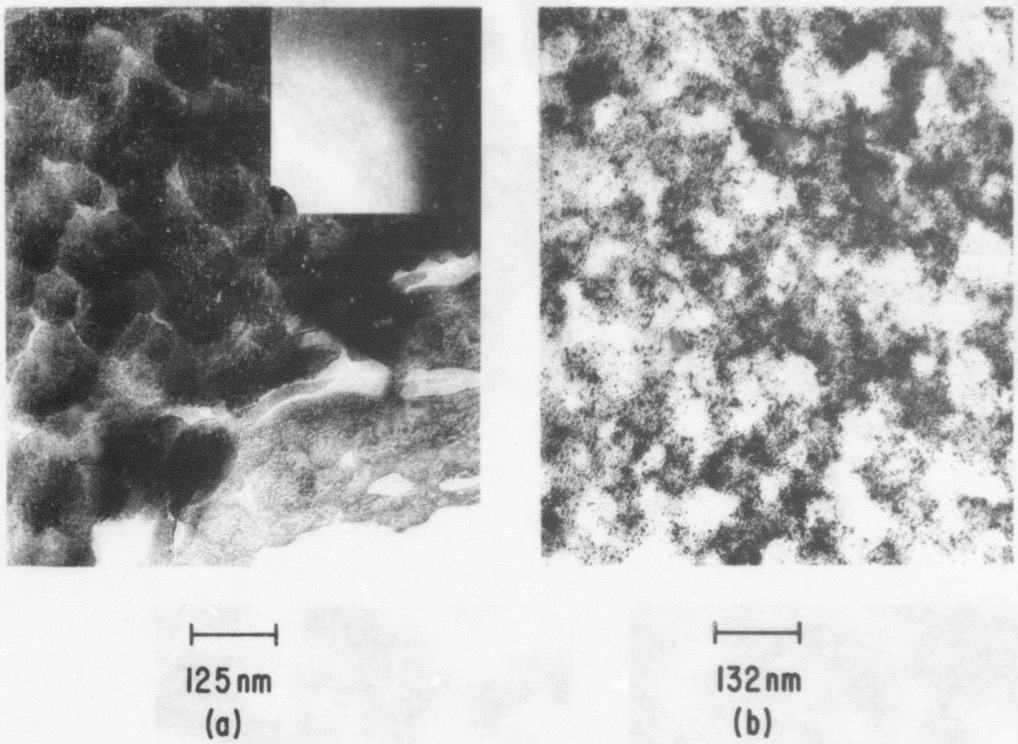

Figure 9. **Porous silicon (a) unoxidized (upper left) and fully oxidized (lower right) with diffraction for fully oxidized area, (b) partially oxidized showing Si islands as dark specks.**

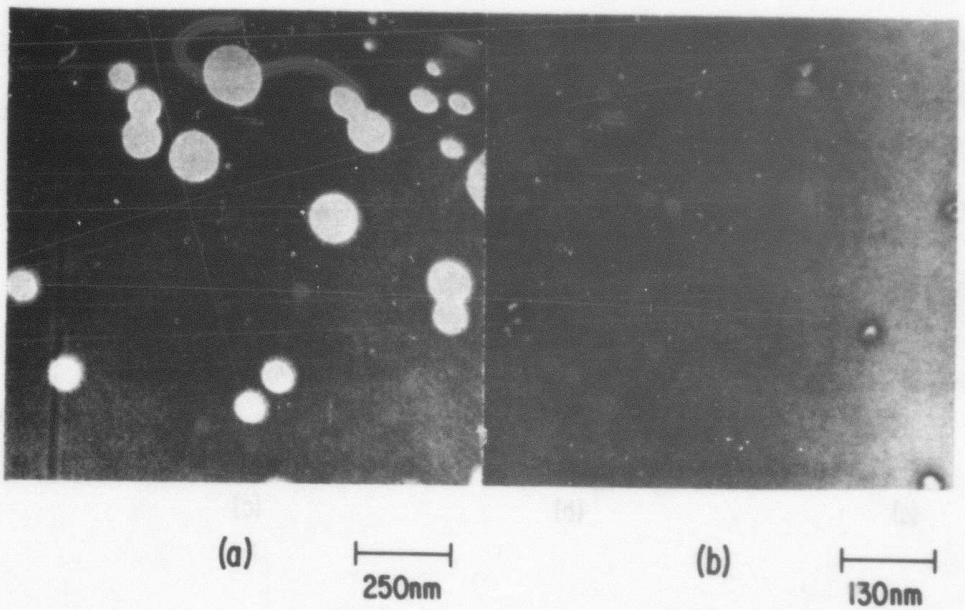

Figure 10. Imhomogenous etch patterns in thin SiO_2 films (a) etched with $HF\text{-}HNO_3$ (b) etched with ethylenedramine - pyrocatechol - H_2O mixture.

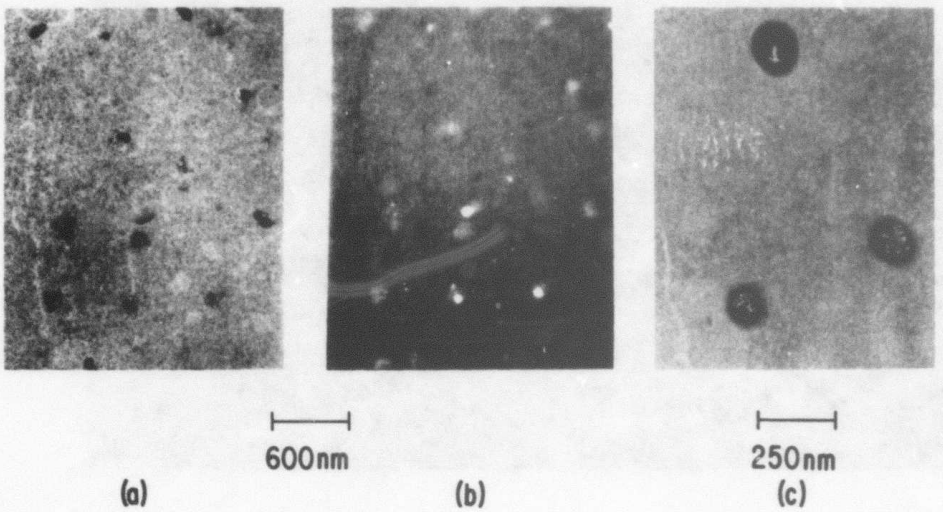

Figure 11. SiO_2 film prepared at 1100°C with 6% HCl in O_2. Si inclusions are observed in (a) and (c) and (b) is a dark field of (a).

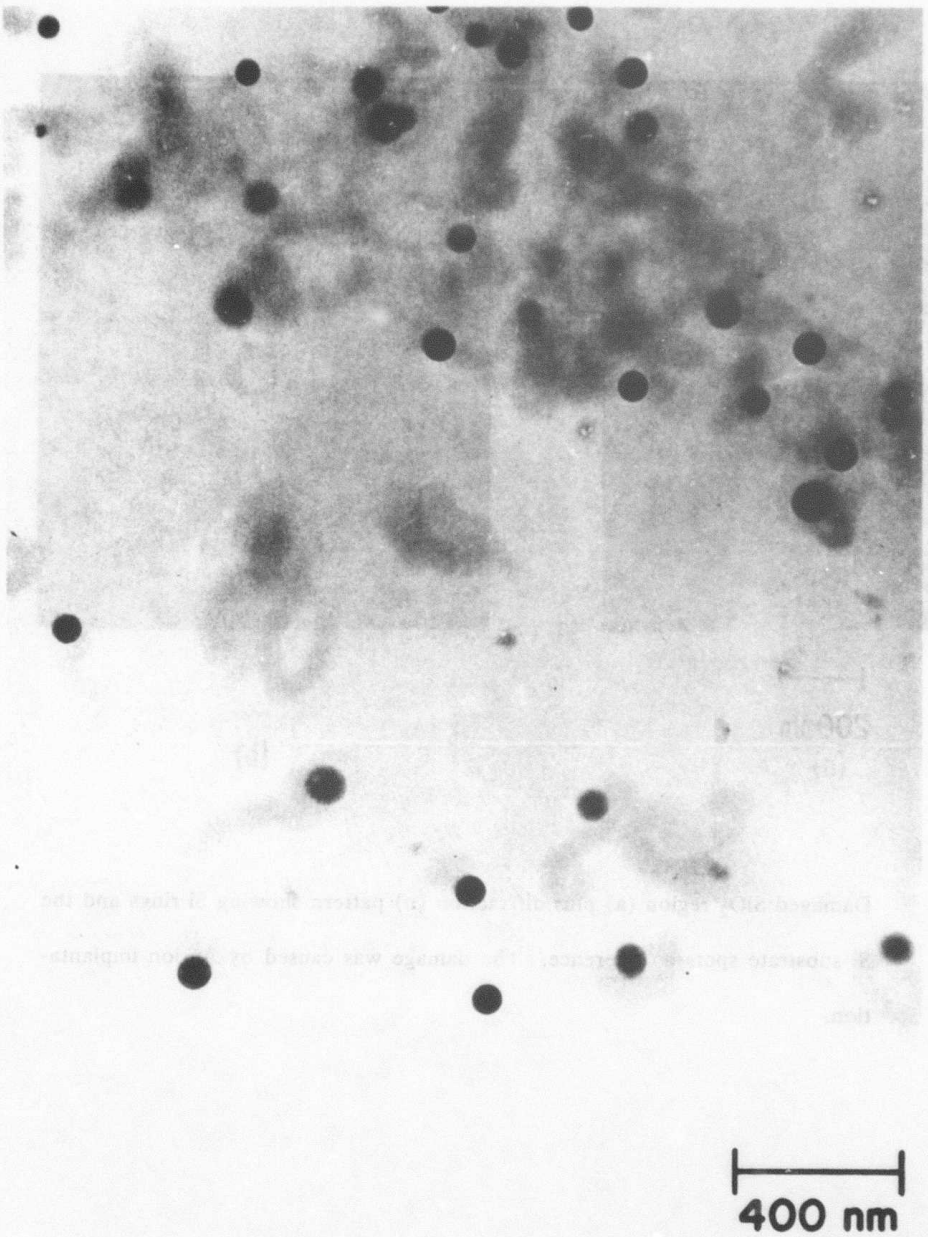

Figure 12. SiO_2 film prepared by oxidizing Si doped with B at ~10^{20} atoms/cm^2. B_2O_3 phase separated particles are observed.

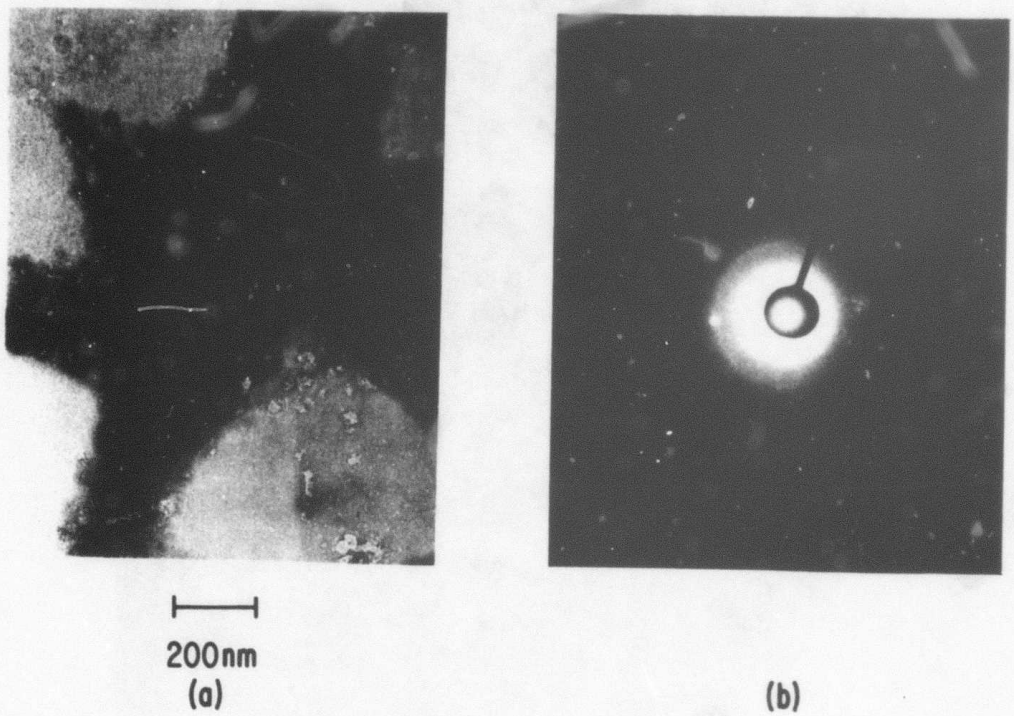

Figure 13. Damaged SiO_2 region (a) plus diffraction (b) pattern showing Si rings and the Si substrate spots as reference. The damage was caused by As ion implantation.

Figure 14. Au on SiO_2 annealed at 800°C and Au partially removed by aqua regia. Regions where Au was removed show evidence of reaction.

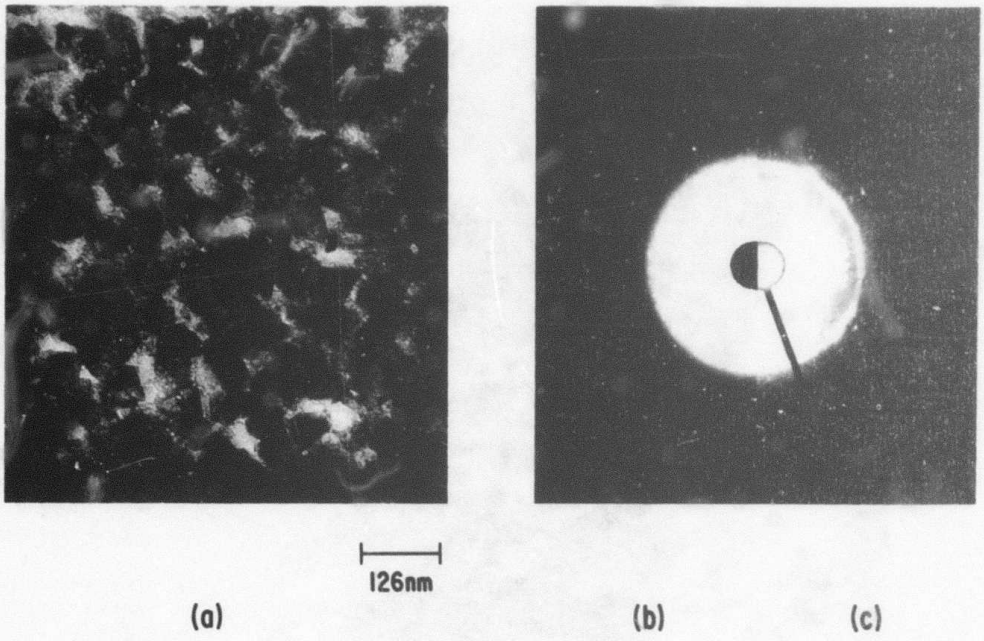

Figure 15. (a) Al grains on SiO_2, annealed for 5 min. at 700°C in N_2, (b) diffraction due to Al, (c) diffraction due to new aluminum oxide phase.

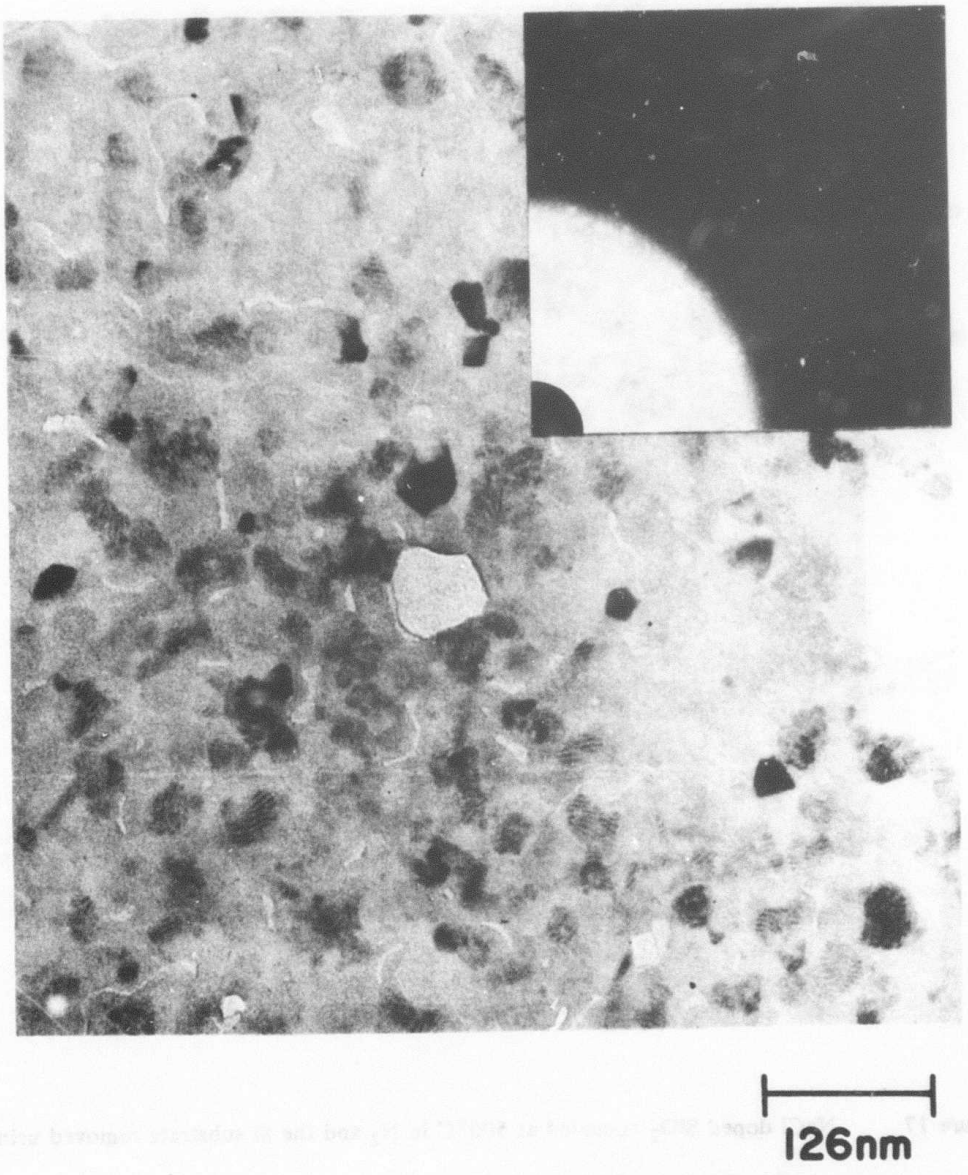

Figure 16. Al grains on SiO_2 annealed in O_2, at 500°C for 30 min. Only Al lines seen in diffraction.

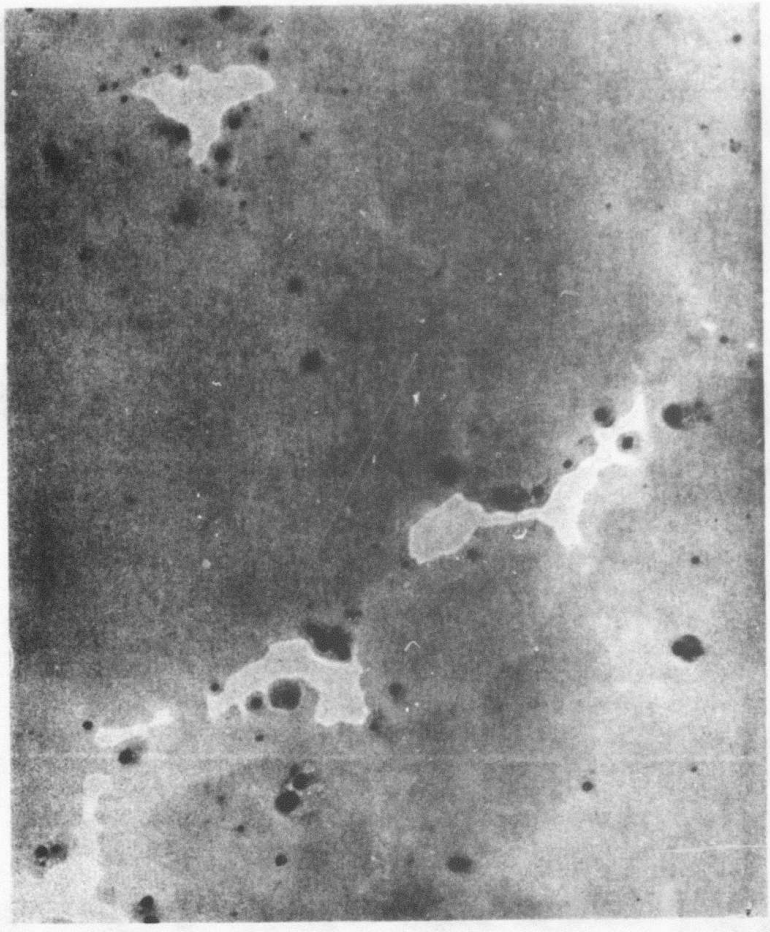

Figure 17 NaCl doped SiO_2 annealed at 500°C in N_2 and the Si substrate removed using ethylenediamine - pyrocatechol - H_2O mixtures. Dark regions are NaCl islands.

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Residual Stress, Chemical Etch Rate, Refractive Index and Density Measurements on SiO_2 Films Prepared Using High Pressure Oxygen

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ABSTRACT

Dry oxygen pressure at 500 atm is used to grow SiO_2 films 10^3 nm thick on silicon at 800°C. The residual film stress, chemical etch rate, refractive index, and density of the pressure-oxide films is measured and compared with measurements of thermal oxide films prepared at 1 atm dry oxygen pressure. The high-pressure/low-temperature films exhibited higher refractive indices, slower chemical etch rates, and higher measured densities compared to 1 atm thermal oxides prepared at 1000°C. These results are attributed to the lower oxidation temperature rather than the higher oxidation pressure of the pressure-oxide films. It is concluded that the formation of higher density SiO_2 films is a specific result of low temperature processing. The use of high pressureh oxidation provides a convenient technique to prepare the low temperature high density SiO_2 films of sufficient thickness for further study

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Key Words: high pressure oxidation, silicon, silicon dioxide, density, film stress

INTRODUCTION

Recently, Zeto et al (1,2) reported enhanced oxidation rates for single crystal silicon thermally oxidized in dry oxygen at elevated oxygen pressures up to 500 atm. It was shown (1) that the silicon oxidation rate obtained by using oxygen at 140 atm (ie the pressure of oxygen in commercially available oxygen tanks) and 800°C was comparable to the rate obtained by using 1 atm oxygen at 1200°C. Therefore, the use of elevated oxygen pressures enables a reduction of the oxidation temperature and/or time for an oxidation step. This temperature/time reduction has great technological importance because of the need to maintain sharp dopant profiles and minimize the creation of thermally induced defects in modern small devices. The use of steam (3) and high pressure steam (4) for the thermal oxidation of silicon also offers considerable kinetic enhancement, however, the quality of the SiO_2 and Si may be degraded based on reports of increased electron trapping in SiO_2 due to H_2O (5) and increased Si defects resulting from exposure of the Si to steam oxidation (6).

Whether the MOS industry will accept a new process, such as the use of increased oxidant pressures, will depend both on the need for the lower temperature processing and the demonstration that the SiO_2 quality is not degraded by the new process. It is clear from the industry trend towards smaller devices that lower processing temperatures are required and therefore this study is aimed toward demonstrating that important aspects of the SiO_2 quality resulting from high pressure dry oxidation of silicon can be equivalent to the SiO_2 grown in the conventional 1 atm processes.

As with any new process, the dry high pressure oxidation process has problems associated with reproducibility and optimization. Notwithstanding these anticipated difficulties, Zeto et al (2) reported that mobile and fixed charge levels were acceptably low (in the low $10^{10} charges/cm^2$ range) on many samples. These promising results have provided the impetus to improve the process through equipment evolution and to obtain more physical properties data on the resulting SiO_2 films.

The present study reports the results of several physical properties measurements on SiO_2 grown by the high pressure dry oxidation of silicon: residual film stress, chemical etch rates, density, refractive index and film morphology as obtained by transmission electron microscopy (TEM). Collectively, these measurements show that the films have increased density as compared with 1 atm films prepared at conventional oxidation temperatures of 1000°C. The higher refractive indices, slower etch rates and higher measured densities of the high-pressure low-temperature films are attributable to the lower processing temperatures rather than the higher oxygen pressures. Thus a specific advantage of high pressure oxidation methods is that these higher density low temperature SiO_2 films can be prepared in practical oxidation times.

EXPERIMENTAL PROCEDURES

Sample Preparation

Four high pressure dry oxygen oxidation runs were performed as described below to grow oxides about $10^3 nm$ thick on six Si substrates. The Si slices were nominally 2 Ω -cm P type, 2.54 cm diameter and 0.02 cm thick. Three each of <111> and <100> orientations were used and designated 111, 112 and 113 for the <111> samples and 012, 013 and 014 for the <100> samples. Control oxides were grown at 1 atm, 1000°C or 800°C in pure dry O_2 on <100> silicon to similar thicknesses and were used in the film stress, etch measurements and refractive index measurements to obtain meaningful comparisons with the high pressure grown samples. Prior to any oxidation all Si slices were thoroughly cleaned by a previously described procedure (7). The six samples for high pressure oxidation were initially oxidized at 1000°C in 1 atm ultra dry O_2 to obtain 100 nm SiO_2. This was done to obtain a reproducible initial curvature in the Si substrates for the stress measurements.

Pressure Oxidation

The apparatus used for the high pressure dry oxidation was described previously (1) with the exception that a larger pressure vessel was used to accommodate the 2.54 cm. diameter Si slices noted above. For each of the experimental oxidations, the Si slices were heated to about 800°C while a vacuum was drawn on the vessel. Then, 500 atm dry oxygen pressure was applied within several minutes. After the desired oxidation time the pressurized vessel was withdrawn from the furnace and cooled by radiation. All samples were oxidized at 800°C to yield about $10^3 nm$ SiO_2. The oxidation rates for the <100> samples were about 87 nm/hr and 132 nm/hr for the <111> Si. The H_2O content of the pressurized gas was measured as less than 1 ppm.

Film Stress

The residual room temperature stress was calculated from a measurement of the curvature of a Si wafer before and after the SiO_2 film growth by dry pressure-oxidation. The change in Si curvature was measured by an optical interference technique. The apparatus, appropriate equations, elastic constants used for the calculations as well as the procedures were previously described (8) for a study of Si_3N_4 film stress. Only a small difference (less than 10%) is anticipated in the residual stress for <100> and <111> orientations due to the difference of elastic constants for the different Si orientations and we ignored this difference in the present study. The pressure-oxide samples had about 5% thickness non-uniformity across the sample as compared with about 1% for the 1 atm SiO_2 oxides. The direct implication of this on the measured film stress has not been determined but it may contribute to the overall scatter of the pressure-oxide stress data.

Chemical Etch Rates

Chemical etch rates have been shown to be a very sensitive measure of SiO_2 film density (12). The temperature, composition and extent of agitation of the etchant solution can all alter chemical etch rates. In order to preclude obscuring comparisons between high pressure oxides, controls and low temperature oxides due to experimental diffculties, samples and controls for a given comparison were etched simultaneously in the same solution. For the comparison of high pressures oxides with 1 atm 1000°C standards, two samples of each were etched together in a commercially available 9/1: NH_4F/HF mixture at ~22°C. For this comparison (Figure 1) more scatter was seen for the pressure oxides. The scatter was due to the larger non-uniformity of the SiO_2 thickness for these samples and the problem of returning to the same spot on the sample for ellipsometric thickness measurement after each exposure to etchant. However, the results to be reported are outside this scatter. Similarly, the comparison of etch rates for the 1 atm 800°C and 1000°C grown SiO_2 was made on samples etched in a 9/1: NF_4/HF simultaneously and together at ~22°C. The differences in the 1000°C 1

atm controls are presumably due to the above mentioned temperature, agitation and etchant batch differences.

Density

The SiO_2 film density, ρ_1 was calculated from measured values for the mass change of the samples before and after removal of the film by etching and the volume of the film as obtained from the area of the Si wafer and the film thickness. Only the film on the polished side of the Si was used and a correction was made for the area lost as the Si wafer flat. The weighing accuracy was better than $3 \times 10^{-6} g$ while the oxide mass was about $10^{-3} g$. The average film thickness accuracy was estimated to be better than about 3% based on multiple ellipsometric measurements taken across the wafers and the surface area was known to better than 3%. Based on these values, the error in ρ, $\Delta \rho$, is calculated to be about 10^{-2}. Therefore, the higher density measured for the high pressure grown and the 800°C, 1 atm oxides as compared with 1000°C, 1 atm is a real difference but the absolute values are somewhat uncertain to better than several percent.

Film Thickness and Refractive Indexes

The SiO_2 thickness and refractive indexes were measured by ellipsometry. A description of the instrument with the various constants used was previously published (9). The reported measurements of refractive index were made near one-half of an ellipsometric period i.e. at odd multiples of ~140 nm for the 632.8 nm light and ~120 nm for 546.1 nm light. Near these thicknesses the ellipsometric measurement is most sensitive to different refractive indexes. The index measurements were made during the course of the etching experiments and the index values corresponding to half-period thicknesses were tabulated.

TEM

Samples were prepared for microscopy by removal of the Si with an $HF - HNO_3$ etchant. Since the SiO_2 was too thick (~ 1 μm) for penetration by the 100 KeV electrons, the etchant was also used to etch away most of the SiO_2 leaving about 100 nm for examination by TEM.

EXPERIMENTAL RESULTS

Residual Stress Measurements

A comparison of the SiO_2 film stress for the high pressure oxides, controls (1 atm O_2, 1000°C) and literature values are shown in Table 1. All of the stresses shown in Table 1 both measured in this study and from the literature are compressive stresses. The high pressure oxides show more scatter in the stress values than the controls and this may be due to the greater thickness non-uniformity found for these films (about 5% across the wafers). Considering the scatter in the stress values, the film stress for the high pressure oxides is the same as for the controls. Optical microscopic examination revealed no evidence for Si slip due to stress on any of the substrates.

Chemical Etch Rates

Figure 1 shows the combined etching results from two pressure-oxide and two control samples 1 atm 0_2, 1000°C. Individually the etch rates were 50.0 nm/min and 48.2 nm/min for the pressure samples and 58.6 nm/min and 58.7 nm/min for the controls. The spread in the pressure-oxide samples was due to thickness non-uniformity which required returning to the exact same spot on the SiO_2 film for the repeated thickness measurements. However, the difference in etch rate between pressure-oxides and controls was well outside the scatter and is therefore considered significant. Pliskin and Lehman (12) reported that a more dense SiO_2 can give rise to a slower etch rate in an HF based etchant.

Index of Refraction

Table 2 shows that the high pressure grown samples have a significantly higher refractive index than the controls. This may be caused by pressure oxides having a higher density since it was reported that a higher SiO_2 film density will yield a measurably higher refractive index (12). The measurements associated with sample 013 are particularly interesting, since this

sample has an initial oxide thickness near one-half an ellipsometric period. The initial oxide thickness is about 1000 nm, of which 100 nm is a 1 atm 1000°C SiO_2 and the remaining SiO_2 has been grown at 800°C with 500 atm oxygen. Since oxidation takes place at the Si - SiO_2 interface, the 1 atm SiO_2 is always on top of the high pressure SiO_2 hence it would be removed after the first etching. However, before etching the composite index is larger than for 1 atm 1000°C SiO_2 but smaller than the high pressure SiO_2 while after the removal of this outer SiO_2 that has a lower index, the index returns to the pressure oxide value. This is a predictable result based on the fact that 1 atm, 1000°C SiO_2 has a lower index than the 500 atm 800°C films and this result demonstrates the sensitivity of the ellipsometric measurement.

Film Density

Since both the etch rate and index of refraction measurements showed the possibility that pressure-oxide SiO_2 samples have higher density, the direct measurement of density was performed. Table 3 shows that indeed the pressure-oxide films have a higher density than the 1 atm oxides.

TEM

Figure 3 shows an area of a pressure-oxide film which had an unusually large amount of particulate. Diffraction showed the particulate to be amorphous and the electron contrast appeared to be about the same as for the 1 atm SiO_2. The pressure vessel used to prepare these samples contained a fused silica test tube liner to hold the silicon slices. We believe that the particulate is SiO_2 dust from the fused silica insert since procedures required that it be thermally cycled, physically handled, and mechanically vibrated in every experiment. Undoubtedly this particulate would contribute to various dielectric failure modes, therefore a second generation high pressure oxidation system has been designed to eliminate this problem.

Up to this point the properties measurements on the high pressure oxides taken collectively indicate that these films have a higher density that the 1 atm 1000°C controls. However, in

view of a recent study by Taft (13) which shows that a higher refractive index results from lower oxide growth temperatures, the higher density found for the high pressure oxides in this study may be due to the 800°C oxidation temperature and therefore independent of the higher oxidation pressure. To check this possibility measurements of the refractive index, etch rates and density using the same techniques described above were done on 800°C, 1 atm oxygen grown SiO_2 films. The results shown in Table 4, while not extensive, clearly show that the lower temperatures produce a more dense oxide film. When an 800°C 1 atm SiO_2 film was heated in flowing N_2 at 1000°C for 2 hrs, the refractive index returned to the 1000°C value. This suggests that higher defect concentrations produced at higher temperatures are responsible for the lower densities. Further work to clarify this situation is in progress.

SUMMARY AND CONCLUSIONS

It was previously demonstrated that a significant oxidation rate enhancement is obtained by using high dry O_2 pressures and that acceptable oxide charge and interface state levels could also be obtained. The present study extends the property measurements to include film stress, chemical etch rate, refractive index, density and TEM morphology. These measurements show that: (1) there is no significant difference in the residual Si/SiO_2 film stress for high pressure and 1 atm thermal oxides, (2) high-pressure/low-temperature thermal oxide SiO_2 films have a significantly higher density than films prepared at conventional oxidation temperatures such as 1000°C, and (3) 1 atm thermal oxides prepared at 800°C have a higher density than films prepared at 1000°C.

The formation of high density SiO_2 films on silicon is therefore a specific merit of reduced oxide growth temperatures. The preparation of these higher density SiO_2 films is an advantage afforded by high pressure oxidation methods since higher pressures allow the oxides required in IC devices to be prepared at reduced temperatures in practical oxidation times. It remains to be determined whether or not the higher density material has other interesting properties, such as improved dielectric strength.

ACKNOWLEDGEMENT

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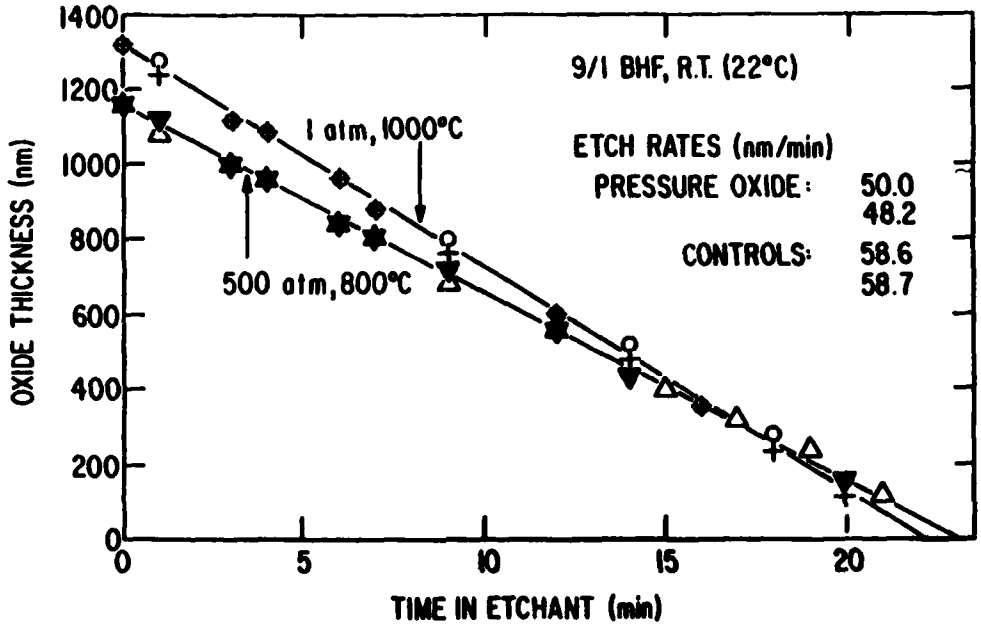

Figure 1. Plot of SiO_2 thickness versus time in etchant for two pressure-oxide and two control samples.

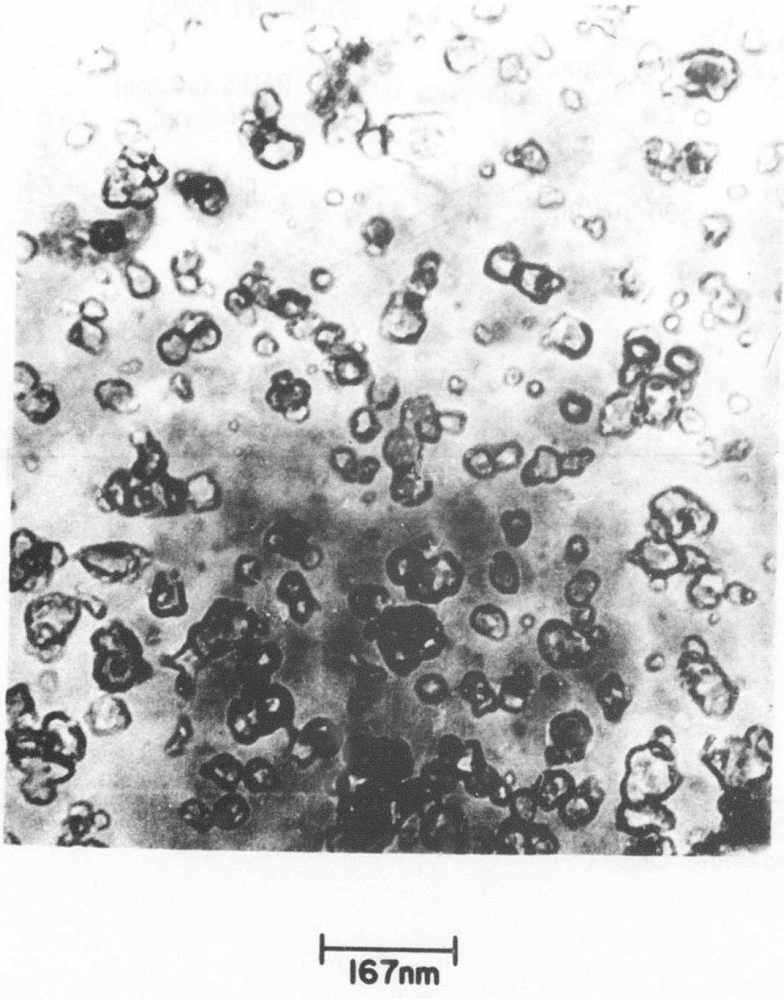

Figure 2. TEM micrograph of pressure-oxide area which has a large number of amphorous SiO_2 inclusions.

Table 1

SAMPLE ID	STRESS ($dynes/cm^2/\cdot 10^{-9}$)
PRESSURE OXIDES (500 atm, 800°C)	
012	1.5
013	4.0
014	4.0
111	2.3
112	4.0
113	2.8
Average:	3.1
CONTROLS (1 atm, 1000°C)	
005	4.1
006	4.2
LITERATURE	
Jaccodine and Schlegal (10)	2.0 for 875°C SiO_2 2.7 for 1000°C SiO_2
Whelan et al (11)	3.7 for 1200°C SiO_2

Table 1. Residual Film Stress Results for Pressure-Oxide SiO_2, Normal 1 atm SiO_2 and Literature Values. All stresses shown are compressive.

Table 2

SAMPLE ID	SiO_2 THICKNESS (nm)	REFRACTIVE INDEX (at λ = 632.8 nm)
PRESSURE OXIDES (500 atm, 800°C)		
112	947.6	1.476
	153.3	1.475
014	983.0	1.473
	941.4	1.473
	685.7	1.475
	129.8	1.478
113	960.0	1.475
013	967.2 (No etch)	1.467
	684.6	1.477
	Average Pressure-Oxide = 1.475	
CONTROLS (1 atm, 1000°C)		
001	959.0	1.461
002	931.4	1.461
	1293.0	1.462
	Average Control = 1.461	

Table 2. Refractive Index Results for Pressure-Oxide SiO_2 and Control Samples for 632.8 Light.

Table 3

SAMPLE ID	DENSITY (g/cm^3)
PRESSURE-OXIDES (500 atm, 800°C)	
113	2.41
013	2.35
CONTROL (1 atm, 1000°C)	
005	2.26

Table 3. Density Results for Pressure-Oxide and Control Samples.

Table 4

Refractive Index:	1.468 @ 632.8 nm light 1.476 @ 546.41 nm light
Etch Rate:	800°C - 1 atm - 72 nm/min 1000°C - 1 atm - 81 nm/min Control
Film Density:	two samples 2.47 g/cm^3 2.42 g/cm^3

Table 4. Refractive Index, Etch Rate and Film Density Results for 1 atm 800°C SiO_2

HIGH CURRENT INJECTION INTO SiO_2 FROM Si RICH SiO_2 FILMS AND EXPERIMENTAL APPLICATIONS

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Abstract: Chemically vapor deposited (CVD) Si rich SiO_2 layers on thermal or CVD SiO_2 layers incorporated into metal-insulator-semiconductor (MIS) capacitor structures are shown to give very large injected electron currents at low to moderate negative gate voltage biases. The dependence of this injection mechanism on the Si rich SiO_2 composition and thickness, temperature, capacitor area, annealing conditions, gate metal (Al or Au), and underlying SiO_2 thickness is described. Photocurrent measurements are discussed and are shown to give similar barrier energies as seen for "uniform" internal photoemission into SiO_2. From the experimental electrical and photo-electrical measurements described here and TEM and Auger studies of others, a possible model to explain this phenomenon based on electric field distortion caused by a two phase mixture of amorphous Si and SiO_2 is presented.

Two experimental applications of these structures are described. In one application, an electrically-alterable read-only memory (EAROM) structure is fabricated, and it is shown to operate at lower voltage ($\leq$ 13 V) and power than popular commercially available devices. The other application involves a "multilayer" structure with alternating layers of polycrystalline Si islands (20 Å or 40 Å in diameter) and CVD SiO_2 deposited on thermal SiO_2 incorporated into an MIS capacitor which also gives large injected electron currents at moderate negative gate voltages similar to the currents observed with Si rich SiO_2. This latter experimental application lends credibility to the proposed two phase model.

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I. INTRODUCTION

Chemically vapor deposited (CVD) Si rich SiO_2 films are currently being used in the electronics industry for passivation in integrated circuits. The Japanese, who were the first proponents of these films which they called semi-insulating polycrystalline-silicon (SIPOS) doped with oxygen atoms[1-5], have used them for surface passivation in bipolar[1,2] and complementary metal-oxide-semiconductor (C/MOS)[3] integrated circuits (IC's). Recent work by the Japanese[5] and members of our laboratory[6] have shown that these films are composed mostly of amorphous Si and SiO_2 in a two phase network, although other forms of oxide (like SiO), might be present [5]. High temperature (1000° C) annealing of the CVD Si rich SiO_2 films causes small crystalline regions ($\lesssim$ 100 Å in diameter) of Si to form. The conductivity of CVD Si rich SiO_2 is much greater than that of SiO_2 at any electric field strength, and it has been shown to be a strong function of the percentage of excess atomic Si[3,4,7]. The conductivity of these films is highly non-ohmic and increases strongly with increasing average electric field[7].

In one section of the study presented here, it will be shown that these Si rich SiO_2 films, when deposited on top of thermal or CVD SiO_2 films and incorporated into metal-insulator-silicon (MIS) structures, give very high electron current injection at moderate average electric fields. Experiments describing the dependence of these injected dark currents on temperature, Si rich SiO_2 composition, thickness variation of the layers of the composite structure, annealing conditions, metal electrode material, and electrode area are described. From these data, photocurrent, and capacitance measurements, a possible model involving the two phase nature of the Si rich SiO_2 films for this enhanced current injection is presented.

In the second section of this study, experimental applications of the composite Si rich SiO_2 – SiO_2 structures will be discussed in detail. These composites will be referred to as stepped or graded insulator MIS (SI-MIS or GI-MIS) structures. One of the experimental applications presented is the use of the composite in electrically-alterable read-only memory

(EAROM) where structures have been fabricated which can be "written" with voltages as low as −13 V on the Al gate electrode in a few milliseconds with excellent charge retention. "Erasure" of these structures is, however, more difficult and requires minutes at similar voltages. Under positive gate voltage bias, some holes are believed to be injected into the SI-MIS or GI-MIS and annihilate some of the captured electrons in the charge trapping layer of this EAROM ("erase" operation).

The other experimental application involves duplicating the high current injection of SI-MIS or GI-MIS structures by using a "multilayer" instead of the Si rich SiO_2 layer deposited on top of SiO_2. This "multilayer" structure is formed from alternating films of CVD SiO_2 and poly-crystalline Si islands (20 Å or 40 Å in diameter). The electrical similarity of the "multilayer" and SI-MIS or GI-MIS structures adds some support to the two phase model.

II. EXPERIMENTAL

A. Sample Preparation

The Si rich SiO_2 layers were chemically vapor deposited on top of thermal SiO_2 layers grown on <100> 2 Ωcm p-type or n-type single crystal Si substrates. All thermal SiO_2 layers were given a 5 min. - 1000°C - N_2 anneal prior to being removed from the furnace. In some cases, chemically vapor deposited (CVD) SiO_2 layers were stacked on top of the thermal SiO_2 layers prior to CVD Si rich SiO_2 deposition. A top gate electrode of Al or Au with an area of .005 to .006 cm^2 (except where stated differently) was then deposited. These electrodes were 4,000 Å or 135 Å thick for Al and 4,000 Å or 175-300 Å thick for Au with the thin, semitransparent electrodes being used for photocurrent measurements. Except where indicated, all metal electrodes were deposited in a vacuum less than 10^{-6} Torr from resistance heated W boats. All Al electrode samples had a 400°C forming gas (90% N_2 - 10% H_2) anneal performed after metallization except where stated as otherwise. Figure 1 summarizes typical groups of samples used in this study. Their controls were identical except for the absence of

the Si rich SiO_2 layer in groups #1-#3 and/or the W layer in groups #2 and #3. A W layer less than a monolayer thick was deposited[12,13] in some cases, to study an EAROM use of charge trapping with these structures. The CVD Si rich SiO_2 layers or CVD SiO_2 were deposited at a moderate temperature (700°C) using conditions described in previous publications[8–10]. R_o, which is defined as the ratio of the concentration of N_2O to SiH_4 in the gas phase, was varied between 3 and 10 for the CVD Si rich SiO_2 films, and was 100 for the CVD SiO_2 layers used in this study. The range from R_o = 10 to R_o = 3 gives 7% and 13% excess atomic Si over stoichiometric SiO_2, respectively. Na^+ levels were shown to be $\lesssim 3 \times 10^{11}$ cm^{-2} as measured by the use of temperature-bias stressing (+10 V at 200°C for 30 min, then cooled back to room temperature under +10 V bias). All samples were stored in a nitrogen dry box when not it use.

The resistivities of 1000 Å thick Si rich SiO_2 films deposited on 2 Ωcm p-Si substrates with Al gate electrodes as a function of the average electric field are shown in Fig. 2 for the range of compositions used here. SiO_2 has a resistivity $> 10^{12}$ Ωcm over this same range of fields. The resistivities in Fig. 3 were not very sensitive to the polarity (although negative gate voltage bias was used in obtaining these data) or to post-metallization annealing. However, the detailed conductivity of the Si rich SiO_2 films is a function of their thickness and the voltage polarity used due to trapped space charge build-up in the films and its effect on injection from the contacts. Thinner Si rich SiO_2 layers have a conductivity that is more contact-limited than bulk-limited, with correspondingly lower resistivities due to the smaller amount of bulk space charge build-up.

The Si rich SiO_2 is believed to be a two phase mixture of amorphous Si and SiO_2[5,6]. Si crystallities ($\lesssim$ 100 Å in diameter) have been observed to form with high temperature annealing at 1000°C in thick films $\geq$ 1000 Å[5,6]. Crystallities, if present at all, must be less than 10-20 Å in diameter on the low temperature processed films ($\lesssim$ 700°C) and on unannealed films[5,6]. This is shown schematically in Fig. 3. These Si rich SiO_2 films were some-

what rough[9] as determined by scanning electron microscopy (SEM)[11]. Densely packed hillocks with average heights of $\lesssim$ 300 Å and average base widths of 600 Å were seen on 1000 Å thick R_o = 3 CVD Si rich SiO_2 films deposited on <100> 2 Ωcm p-Si. Control samples with 1000 Å of CVD SiO_2 deposited at the same temperature (700°C) showed no roughness. Si rich SiO_2 films deposited on Si with thicknesses of 500 Å and 200 Å were also studied using SEM, and they showed progressively smaller hillocks. The 200 Å films (R_o = 3) had hillocks with average base widths of 200 Å and average heights $\lesssim$ 100 Å. The Si rich SiO_2 layers are very thin ($\leq$ 250 Å) in all GI-MIS or SI-MIS structures studied here.

B. Apparatus

The experimental apparatus to do photocurrent as a function of gate voltage (photo I-V) or light energy and capacitance as a function of gate voltage (C-V) has been described in previous publications[12,13,14]. The point-by-point dark current as a function of gate voltage measurements (dark I-V) were also performed using the same voltage stepping unit as used in the photo I-V measurements[13]. Dark I-V measurements, done at a constant gate voltage ramp rate dV_g/dt, used a Keithley #26000 logarithmic picoammeter to measure current and a voltage source with adjustable ramp rates.

III. CURRENT INJECTION AND CAPACITANCE

In the first part of this section (III-A), the experimental results of the enhanced electron injection from Si rich SiO_2 into thermal or CVD SiO_2 layers will be discussed in detail. The current dependence on composition of the Si rich SiO_2 injector, SiO_2 or injector thickness, annealing temperature, electrode material (Al or Au), and area will be presented. Photocurrent measurements will be described in the second part of this section (III-B) along with their dependence on Si rich SiO_2 composition and electrode material. In section III-C, both a.c. and quasi-static capacitance measurements on SI-MIS or GI-MIS structures will be

discussed. Finally, in section III-D various plausible models for this high current injection phenomena at moderate average electric fields will be presented.

A. Dark Currents

Figure 4 shows typical data for dark current as a function of gate voltage (I-V) taken point-by-point starting at 0 V for various SI-MIS and GI-MIS structures from group #1 summarized in Fig. 1 and discussed in Section II. These are compared against a control structure with the Si rich SiO_2 layer absent but otherwise with identical processing. From these data, an electron current enhancement of $\approx 10^5$ times that of the thermal SiO_2 control (MLO-1-P6) for the same negative gate voltage bias is seen. This enhancement is not very sensitive to the thickness or composition of the Si rich SiO_2 injector shown in Fig. 4 provided that next to the Al gate electrode there is a layer of the most heavily doped Si rich SiO_2 that was used (that is, $R_o = 3$). However, the electron injection was degraded when only an $R_o = 10$ layer ($\approx$ 7% excess atomic Si over stoichiometric SiO_2[7]) was deposited on top of the thermal SiO_2 layer as compared to the structures in Fig. 4. The current injection under negative gate voltage bias in the control structure is due to Fowler-Nordheim tunneling of electrons through an $\approx$ 3 eV energy barrier at the Al–SiO_2 interface [15].

The current ledge observed at low voltages in Fig. 4 is due to space charge build-up in the injector layer which tends to hold off further current injection until a certain voltage is reached. Fig. 5 shows a point-by-point I-V cycling experiment designed to explore the nature of the charge trapping in the injector. Between each current cycle from 0 V to a certain negative gate voltage and then back to 0 V, a C-V characteristic was also recorded as shown in Fig. 6. The current trace in the upper half of Fig. 6 shows that most of the trapped electrons are returned to the Al electrode during the return portion of the cycle due to a local reversal of the field caused by the presence of the trapped negative charge. There is, however, some walk-out of the I-V curves (particularly between the first and second cycles) due to part

of the charge carriers remaining trapped in the injector. This walk-out is dependent on the composition of the injector; that is, more conductive Si rich SiO_2 layers show less walk-out. The C-V voltage shifts which are sensitive to the field near the substrate Si–SiO_2 interface are much smaller than the voltage shifts between the I-V curves (which are sensitive to the field in the injector region) in the low voltage region before the ledge. This is consistent with this residual charge trapping being located in the injector which is closest to the Al electrode[8,10,14]. Decreasing the injector thickness and therefore the bulk charge trapping, decreases the width of the ledge and tends to wash it out. The effect on the C-V characteristics for thinner injectors also becomes unnoticeable.

Hole injection for the samples from group #1 from the Al gate into the SiO_2 layer by means of the Si rich SiO_2 injector was also tested by observing I-V and C-V characteristics. C-V characteristics definitely showed positive trapped charge build-up at low to moderate positive gate voltages probably in the Si rich SiO_2 injector region. However, the I-V characteristics, when compared again to a control structure with no injector, were similar but not conclusive in ruling out the possibility of small amounts of hole injection into the SiO_2 layer due to the lack of an exact determination of local electric fields. The current injection under positive gate voltage bias in the control structure is due to Fowler-Nordheim tunneling of electrons through an $\approx$ 3 eV energy barrier at the substrate Si–SiO_2 interface[15]. In a later section (IV-A), some possible evidence from EAROM measurements supporting hole injection will be presented. However, a distinction between holes injected directly from the gate electrode or holes left behind by electrons in the Si rich SiO_2 layer which move back to this electrode, possibly by tunneling, can not be made at the present time.

Figure 7 shows the temperature dependence of the electron injection current of a SI-MIS structure. Each of these I-V characteristics were taken from 0 V at a constant voltage ramp rate of $-.47$ V/sec on a virgin unstressed location from the same region on wafer MLO-1-P3. The low voltage current ledge here is due to a displacement current equal to C_I

dV_g^-/dt where C_I is the total capacitance of the insulator stack (SiO_2 and Si rich SiO_2 layers) and V_g^- is the negative applied gate voltage. The trapping ledge seen in the point-by-point data of Figs. 4 and 5 due to space charge build up in the injector is concealed by this larger displacement current. As can be seen from this figure, the current is weakly varying with temperature, by about an order of magnitude from 77°K to 200°C (473°K). This sort of variation is consistent with Fowler-Nordheim tunneling[15].

Figures 8 and 9 show the dependence of the current on injector thickness and SiO_2 thickness on samples from all three groups in Fig. 1. Only samples without a W trapping layer from groups #2 and #3 were used. The current ledges observed on some samples at high current levels is due to bulk electron trapping in CVD SiO_2 layers, and this will be discussed in a future publication.[16] From Fig. 8, it is observed that injector thicknesses down to 50 Å can be used. Below 50 Å, electron injection degrades. Fig. 9 shows that the slope and turn-on voltage of these SI-MIS structures can be controlled by varying the composite SiO_2 thickness. This is important for device applications as will be discussed in Section IV-A.

The electron injection dependence for SI-MIS structures on gate electrode material was also studied. Au injects less than Al for comparable gate voltages probably because of the difference in work functions[17,18]. However, the difference in the dark currents was somewhat smaller than expected from interfacial energy barrier differences[15]. This difference in currents varied depending on the thickness of the Si rich SiO_2 layer used (in samples with thinner injectors the difference was larger) probably due to trapped space charge build-up changes with thickness (less space charge in thinner injectors).

One series of SI-MIS structures was subjected to various annealing conditions to observe the effect on electron injection. These data are shown in Fig. 10. As seen, high temperature annealing (1000°C) does not have much effect on the injection characteristic even though it is known from transmission electron microscopy (TEM) and Auger electron spectroscopy (AES) that Si crystallites form at these temperatures[5,6]. After annealing at

1000°C for 30 min in forming gas (90% N_2 and 10% H_2), an anomalous result was seen due to high lateral surface conductivity (dashed curve in Fig. 10). This anomalous result was shown by TEM and AES to be due to the reduction by H_2 of some of the surface oxide to Si. To remove this lateral surface conductivity, reactive ion etching (RIE) with CF_4 was used on half of wafer C as shown by the dot-dashed curve in Fig. 10. Using the Al gate electrodes of these capacitor structures as a mask, the Si rich material was vertically etched away to the underlying thermal SiO_2 layer between the Al electrodes.

On certain SI-MIS samples with Al gate electrodes similar to those in Fig. 10, the effect of no annealing was investigated. Here the standard post-metallization anneal at 400°C for 20 min in forming gas was not performed. The dark current-voltage characteristics of these structures were essentially the same as those on identical samples that had been post-metal annealed.

The SI-MIS structures showed a current dependence which was approximately proportional to the electrode area from 2.2×10^{-3} cm^2 to 1.3×10^{-2} cm^2. This implies that the injection is uniform on this macroscopic scale.

Lateral conductivity effects were ruled out as possible explanations for any of the dark current data presented here by RIE with CF_4 on half of the wafer for the various samples in Fig. 1. Using the Al gate electrode of these capacitor structures as a mask, the Si rich SiO_2 material was etched vertically away between the Al electrodes. Dark current measurements on etched and unetched portions of the wafers yielded identical results.

B. Photocurrents

Using thin, semitransparent Al electrodes (≈ 135 Å thick) or Au electrodes (175-300 Å thick) various samples with different SiO_2 thicknesses (160-500 Å) and Si rich SiO_2 compositions and thicknesses (the full range in Fig. 1) were tested for photocurrent

response. Fig. 11 shows typical data for the photoresponse (defined in this figure as Y) as a function of photon energy using chopped light techniques with ac detection[12] which was used to separate the smaller photocurrents from the larger dark currents at voltages (particularly at −16 V on MLO-5F) where the enhanced dark current injection mechanism due to the Si rich SiO_2 injector is operative. The flat portion below ≈ 3 eV is due to a 90° out of phase Si substrate signal, while that above 3 eV is due to internal photoemission from the negatively biased gate electrode. As seen in this figure, the photoresponse of the SI-MIS for negative gate voltage bias is somewhat similar to the control MIS structure. Except for the current enhancement expected for Schottky barrier lowering[17], the photoresponse was not particularly a strong function of the applied gate voltage. These characteristics were also similar for various SiO_2 thicknesses and Si rich SiO_2 compositions such as those in Fig. 1. The normalization to transmitted light intensity through the metal electrode[12,19] or to that absorbed in the metal electrode taking account of optical interference effects in the multilayer film[12,19] also was not critical. Square root photoresponse plots[20,21] yielded a similar comparison to that shown in Fig. 11. Static dc photoresponse measurements at gate voltages below the strong dark current response due to electron injection also yielded similar results to Fig. 11 as shown in Fig. 12. The photoresponse also was not particularly sensitive to Si rich SiO_2 injector composition (graded or one step with R_o = 3) as shown in Fig. 12. Photoresponse under positive gate bias yielded results typical of internal photoemission from the Si substrate into SiO_2[17, 20-22] as expected. All photocurrents were stable and indicative of a steady state condition.

Data similar to that in Fig. 11 were also observed for electron emission from Au electrodes into SI-MIS structures as shown in Fig. 13. However, for Au injection the magnitude of the photoresponse was less than that for Al, as was seen for the dark currents. The control sample (Au-SiO_2-Si) in this case is different, showing approximately the 1 eV interfacial energy barrier increase expected with an Au electrode as compared to Al[17] (see

Fig. 13). The method of Au deposition (e-beam or resistance heated W boat) had little effect on the photocurrent data displayed in Fig. 13 or the dark current.

From the data of Figs. 11-13, the cube root of the photoresponse on the SI-MIS structures tends to show two thresholds near 3 eV and 4 eV. This is reminiscent of internal photoemission of electrons from the single-crystal Si conduction band and valence band into the SiO_2 conduction band where the interfacial energy barrier heights are $\approx$ 3 eV and $\approx$ 4 eV, respectively[21,22]. The details of the tail from 3 eV to 4 eV on the SI-MIS sample with the Au gate electrode in Fig. 13 was sensitive to the Si rich SiO_2 thickness. Samples with thinner injectors did not show the tail as clearly. Again these differences are probably due to trapped space charges as suggested for the dark currents in section III-A.

C. Capacitance

Small signal a.c. capacitance measurements with SI-MIS or GI-MIS structures on 2 Ωcm p-Si substrates biased in accumulation were performed to deduce an effective dielectric constant for the Si rich SiO_2 layer. The insulator stack capacitance C_I determined in this way was independent of measuring frequency from 1 MHz to 100 Hz for a small a.c. signal of 15 mV. C_I for structures from group #1 shown in Fig. 1 were also independent of negative gate voltage bias out to -45 V where high current injection from the Si rich SiO_2 layer is occurring (see Fig. 4). The substrate Si-SiO_2 interface was unaffected by the presence of the Si rich SiO_2 layer in SI-MIS or GI-MIS structures of Fig. 1 where low frequency distortion of C-V curves was used as an indicator for the presence of substrate Si – SiO_2 interface states[23,24]. The dielectric constant deduced for the R_o = 3 Si rich SiO_2 material was 7.5 ± 1.0 which is coincidentally very close to the average value of the sum of Si (11.7) and SiO_2 (3.9).

Quasi-static capacitance as a function of gate voltage measurements[23] were also performed. Here the insulator stack capacitance was deduced from the d.c. current measured

while ramping the voltage on p-Si substrate samples from 0 V at a constant ramp rate (−.47 V/sec in most cases) into accumulation; that is, $C_I = I/(dV_g^-/dt)$. In these measurements, C_I was observed to switch from a low value equal to the small signal a.c. results discussed in the preceeding paragraph to a value equivalent to that which would be expected if the Si rich layer were absent or totally metallic. The voltage at which C_I switched (which was not a strong function of ramp rate or cycling) was about the same as that at which electron injection from the gate electrode into the Si rich SiO_2 layer and trapping in this layer started to occur; for example, ≈ -10 V on the structures in Fig. 4 as discussed in Section III-A. This result is consistent with the low resistivity of the Si rich SiO_2 layer with respect to the underlying oxide layer and with the strongly decreasing resistivity of the Si rich SiO_2 with increasing gate voltage.

D. Discussion and Models

The dark current injection phenomena for the SI-MIS and GI-MIS structures (for example, see Figs. 4 and 5) can be divided into two regimes. The low voltage regime (for example, less than ≈ -22 V in Fig. 4) is believed to be controlled by the injection (possibly local) from the metal gate contact and the charge trapping and conduction properties of the Si rich SiO_2 layer (see section III-A). The moderate voltage regime (for example, $\gtrsim -22$ V in Fig. 4) is believed to be controlled by the Si rich SiO_2 interface with the underlying SiO_2 layer although the contacts and bulk of the Si rich SiO_2 layer must supply the carriers to this interface. In this section, several possible models for the moderate voltage regime will be discussed. Some models, such as uniform grading of the energy bandgap, will be ruled out from experimental evidence. Of these models, electric field distortion due to the two phase nature of the Si rich SiO_2 layer seems very plausible, and it will be discussed in detail.

The photocurrent results which are very sensitive to the contacts and the Si rich SiO_2 layer are discussed in terms of a model which depends on internal photoemission from the gate electrodes and bulk photoexcitation from the amorphous Si regions in the Si rich SiO_2 layer.

The data of Sections III-A, III-B and III-C in the moderate voltage regime could be explained by several possible mechanisms which include:

1) energy bandgap grading

2) trap assisted tunneling

3) electric field distortion associated with two phase materials.

These mechanisms could be operating uniformly and/or locally over the electrode area. They are shown schematically in Figs. 14-16. Another possibility which is electric field enhancement due to surface roughness[25,26] at the top gate metal electrode – Si rich SiO_2 interface seems doubtful because electron injection due to this enhancement should be terminated by trapped electronic space charge build-up in the Si rich SiO_2 layer [27]. This might be the explanation for the initial current rise at low voltages in Figs. 4 and 5 before the onset of the Si rich SiO_2 charge trapping ledge.

Grading of the energy bandgap which is uniform over the electrode area also seems a doubtful explanation from the photocurrent measurements (see Section III-B). These measurements indicated an energy barrier of $\gtrsim$ 3 eV, whereas the dark current measurements would require approximately a $<$ 2 eV barrier at the Al-Si rich SiO_2 interface (taking the differences in dielectric constants of the different layers into account) as the limiting energy barrier controlling the electron injection process. However, uniform bandgap grading or stepping is thought to be the explanation for high current injection in CVD Si_3N_4 ($\approx$ 5 eV bandgap) – CVD SiO_2 ($\approx$ 9 eV bandgap) systems[28] and CVD Si_3N_4 – thermal SiO_2 systems with a heavy As implant modifying the energy barrier at the Si_3N_4 – SiO_2 interface[29].

Since it is believed by the Japanese group[5] and our group[6], that the Si rich SiO_2 layers are formed from at least two phases (namely amorphous Si and SiO_2), a localized injection scheme on a microscopic scale seems very reasonable. However, these localized injecting regions must be small (tens of Å s) and densely packed in order to give the appearance of a uniform injection as dictated by discrete charge trapping studies which indicate that the injected current is uniform.[16] It can be shown that the rate at which purposely introduced "W" traps embedded between the SiO_2 layers charge-up can be satisfactorily predicted by assuming a uniform dark current injection.[16] A similar result is deduced for the CVD and thermal SiO_2 traps.[16]

At fields where electrons start to be injected readily into the SiO_2, the Si rich SiO_2 layers will have a very low resistivity (see Fig. 2 and section III-C) as compared with that of SiO_2 ($> 10^{12}$ Ωcm). Conduction through the Si rich SiO_2 layer probably proceeds by electronic hopping (direct tunnelling) from one amorphous Si region to the next (as shown schematically in a very ideal fashion in Fig. 17). However, Poole-Frenkel conduction (field-assisted thermal ionization) might also be operative under certain conditions, particularly if the potential wells of the Si regions interact with one another (due to their closeness) and lower the energy barriers. The Si rich SiO_2 interface with the underlying SiO_2 layer probably limits and controls the current flow into the SiO_2, and therefore the current observed in the external circuit. This limiting interfacial current should be Fowler-Nordheim-like which is consistent with the weak temperature dependence (see Fig 7) and the strong voltage dependence (see Fig. 4) observed for the dark currents. If the surface of the Si regions at the interface have any curvature, localized electric field distortions and current enhancements will result[25]. Only a local field enhancement of $\gtrsim 1.5$ is necessary to explain the dark current data. This is shown schematicallly in Fig. 17 and probably is the most reasonable explanation. The weak dependence of the measured dark currents of the SI-MIS or GI-MIS structures on the thickness of the more heavily doped Si rich SiO_2 layers (see Figs. 4 and 8) is also consistent with the low resistivity of these films compared to SiO_2 at the electric fields of interest

(most of the voltage is dropped across the SiO_2 layer) and with the current limiting nature of the SiO_2 – Si rich SiO_2 interface. Electron heating and scattering effects in the Si potential wells (see Fig. 17) could also influence the measured currents where hot electrons arriving at the Si rich SiO_2 – SiO_2 interface would "see" a smaller energy barrier. However, there is no strong experimental evidence for such effects since the dependencies on Si rich SiO_2 thickness and on temperature are observed to be weak for the GI-MIS and SI-MIS structures studied here.

Another possibility is trap assisted tunneling in the region between the last layer of the Si regions in the two phase Si rich SiO_2 network and the underlying SiO_2 layer. It is reasonable that many localized states across the SiO_2 bandgap can be introduced in this transition region. "Local" grading of the energy bandgap could also result in this transition region.

The dependence under negative gate voltage bias of the dark currents (see section III-A) on gate metal (Al or Au) suggests that the supply of electronic carriers at the SiO_2 – Si rich SiO_2 interface is controlled by the efficiency of getting these electrons into the Si rich SiO_2 layer from the contacting metal gate. Au has an electronic work function which is $\approx$ 1 eV greater than Al. This probably accounts for the differences observed for almost any type of injection mechanism operative at the metal – Si rich SiO_2 interface (that is, Fowler-Nordheim tunneling, direct tunneling, trap-assisted tunneling, and Schottky emission). Direct Al or Au contact to Si regions would not be expected to show much dependence on the metal work function due to Fermi level pinning.[30] Clearly, the nature of the metal contact is sensed in the measured currents which implies that space charge in the "thin" Si rich SiO_2 layer is never large enough to limit the injection of carriers in such a way as to significantly reduce the effects of the contacts. However, on SI-MIS structures with Au electrodes some bulk trapped space charge effects were seen as described in section III-A, where structures with thicker Si rich SiO_2 layers showed smaller differences in dark currents in comparing injection from Au and Al contacts. This implies that the larger number of bulk trapped

charges in the thicker injectors were more effectively screening the effect of the work function of the metal gate electrode (conductivity was more bulk-limited as compared to contact-limited).

The insensitivity of the electron current injection of the Si rich SiO_2 layer to annealing at 1000°C (see Fig. 10) which forms Si crystallites possibly out of the amorphous regions, suggests that the microscopic state of the SiO_2 – Si rich SiO_2 interface and the proposed electric field distortion associated with it does not change significantly. Of course, the conductivity of the Si rich SiO_2 layer itself and its interface with the metal gate electrode must not be affected drastically by the pre-metallization 1000°C annealing.

The photocurrent tail down to 3 eV on SI-MIS structures with Au electrodes as compared to control structures with no tail (see Fig. 13) suggests that some of the electrons are being photo-excited from the conduction band or from states across the bandgap of the amorphous Si regions in the Si rich SiO_2 layers. Electrons in the Si regions would be expected to have a $\simeq$ 3 eV barrier height (Si conduction band to SiO_2 conduction band) with the SiO_2 regions. The pronounced second threshold near 4 eV seen on all SI-MIS structures (see Figs. 11-13) could be due to photoemission from the Si valence band of the Si regions into the SiO_2 regions (barrier height of $\approx$ 4 eV). In addition, photoemission of electrons from the Au or Al Fermi levels into the SiO_2 regions with barrier energies $\approx$ 3 eV and $\approx$ 4 eV, respectively, will also be operative. Since the number of electrons in the Si conduction band and/or in states across the bandgap available for photoexcitation is small compared to the number in the Si valence band, it would be expected that the photocurrent tail down to 3 eV on the SI-MIS sample with the Au gate electrode would be sensitive to the Si rich SiO_2 thickness. This was seen experimentally as discussed in section III-B.

IV. EXPERIMENTAL APPLICATIONS

In this section, experimental applications using Si rich SiO_2 deposited on thermal or CVD SiO_2 and incorporated into SI-MIS structures will be discussed. In section IV-A, simple EAROM structures using the high current injection properties at moderate average electric fields are shown to operate at voltages as low as −13 V in a few milliseconds for a "write" operation. In Section IV-B, a novel "multilayer" structure fabricated using alternate layers of poly-Si islands and CVD SiO_2 on top of a thermal SiO_2 layer will be discussed and shown to operate similarly to SI-MIS structures with the CVD Si rich SiO_2 layer.

A. EAROM Structures

Electrically-alterable read-only memory (EAROM) and electrically-programmable read-only memory (EPROM) structures are solid state devices that can store information in a non-volatile fashion (information is not lost in case of a power failure) for long periods of time and also have the capability of occasionally being "erased" and rewritten with new information. Most commercially available EAROMs and EPROMs are based on floating-gate avalanche-injection MOS (FAMOS) like structures[31-35] as shown schematically in Fig. 18b. To "write" or store information on the floating polycrystalline-Si (poly-Si) layer embedded in SiO_2, a Si junction is avalanched and hot electrons are injected locally into the thermal SiO_2. These electrons subsequently move under the influence of an electric field to the floating poly-Si layer where they are trapped and spread out uniformly over its entire area. Write voltages applied to the top gate electrode usually vary between 20-30 V, although one structure using high temperature thermal nitridation of the Si substrate[35] instead of thermal SiO_2 between the Si substrate and floating poly-Si layer has been reported to operate at ≈ 10 V. All these structures are high power because of the very high currents in the Si needed for the charging process. The localized nature of the high current injection process is very sensitive to processing conditions. Surface states and positive charges are also observed to

build-up near the injection point at the substrate Si-SiO_2 interface which is also usually the interface used to sense the stored charge on the floating poly-Si layer. Although very stable, FAMOS-like EPROM structures are usually difficult to "erase" requiring ultraviolet light for periods of time as long as hours to photodetrap electrons on the floating poly-Si layer[31-34]. Some FAMOS-like EAROM structures are erased by "hot" hole injection from a junction in the Si substrate[35,36] which also has surface state and positive charge build-up problems[14]. Other FAMOS-like EAROM structures are erased by electron tunneling from the floating poly-Si gate to the top gate electrode[37,38] using the rough poly-Si – thermal SiO_2[39] interface for enhanced local electric field emission[26,37-39].

Some commercially available EAROM structures are based on the metal-thick silicon nitride-thin tunnel silicon dioxide-silicon (MNOS) structure[40]. These devices are written (erased) in a uniform fashion over the entire device area by tunneling electrons (holes) from the Si substrate through the thin tunnel-SiO_2 layer into the Si_3N_4 layer where the carriers are trapped. These structures can operate at speeds of less than 1 msec at gate voltages between 20-30 V and can be cycled (written and erased) about 10^5 times. However, MNOS structures are not as stable as FAMOS structures and charge stored in the Si_3N_4 layer will rearrange itself and leak-off in time due to the conductivity and bulk trapping properties of the Si_3N_4[12]. Trapped carriers can also back-tunnel from near the Si_3N_4-SiO_2 interface to the Si substrate through the thin ($\simeq$ 25-30 Å) SiO_2 layer[41]. In addition, the thin tunnel SiO_2 layer must be uniformly, reproducibly, and accurately grown so that the device operating voltages remain within certain limits on a given wafer or from wafer to wafer.

The EAROM structures described here using the injection properties of Si rich SiO_2 deposited on thermal or CVD SiO_2 are very stable, similar to FAMOS type structures, and can operate at low power and voltage. Fig. 18a schematically shows a SI-MIS or GI-MIS EAROM. The charge storage layer can be optimized separately from the injector, and it can be formed by using a continuous poly-Si layer or by discrete traps such as W or WO_3[9,10,42-44].

The SI-MIS EAROMs described here used deposited W atoms for electron trapping. These structures are summarized in Fig. 1. C-V characteristics were used as an indication of the charge state of the SI-MIS capacitors[45,46]. These are shown in Figs. 19 and 20 for structures from groups #2 and #3 described in Fig. 1. In these figures, the SI-MIS EAROM is written from its uncharged virgin state by injecting electrons by means of the thin Si rich SiO_2 layer. These electrons flow through the CVD SiO_2 layer under the applied electric field to the W trapping layer where some of them (25% to 40%[9]) are trapped producing a negative space charge which causes a parallel shift of the C-V characteristic to more positive voltages[45,46]. The structure from group #2 shown in Fig. 19 can be written in 3 msec at −25 V. An equivalent structure with a continuous poly-Si trapping layer which captures *all* injected electrons should be 2–4 times as fast for the same gate voltage. Fig. 20 shows a structure from group #3 which is essecntially a scaled down version of that in Fig. 19 where all the oxide thicknesses have been halved. This device can be written in the same time (3 msec) to approximately the same charge state (3–4 × 10^{12} e/cm^2) with half the gate voltage (−13 V). Only one other EAROM device can be written in ≤ 1 msec at this gate voltage[35], however since this device is FAMOS-like it still requires higher power than the SI-MIS EAROM.

The SI-MIS structures shown in Fig. 19 and Fig. 20 were much more difficult to erase, requiring times on the order of minutes at voltages similar to those used for writing. Some of these structures could not be erased all the way back to the virgin uncharged C-V characteristic (for example, see Fig. 20). After the first write-erase cycle, the structures cycled fairly reproducibly. Control structures without the Si rich SiO_2 layer showed no charging or discharging under similar write-erase conditions. This was also true for structures without the "W" trapping layer or without both layers.

Erasure of the SI-MIS EAROMs seems to be due, at least partially, to hole injection from the Si rich SiO_2 layer (see section III-A) and subsequent annihilation of the electrons

trapped in the W layer. This was tested experimentally by electronic charging of the W layer of a structure similar to that in Fig. 19 except that the Si rich SiO_2 injecting layer was absent. The charging was performed using avalanche injection from the Si[47] or high field Fowler-Nordheim tunneling from the Al gate electrode[15]. Then this structure was stressed under a positive gate voltage of 25 V for 10 min (erase operation in Fig. 19). About 1/2 of the trapped negative charge (for the same amount of electron trapping as in Fig. 19) was lost probably by field ionization[8], but complete erasure was never seen.

Various experiments were performed on the SI-MIS EAROMs to show that the charge retention was excellent and characteristic of the W trapping layer and not the Si rich SiO_2 injector. The flat-band voltage shift, defined as the voltage shift between C-V characteristics at the capacitance value when the electric field at the substrate Si-SiO_2 interface is zero, was used as an indicator for loss (or gain) of electrons trapped on the W sites. After electronic charging of the structure in Fig. 19 to approximately the same charge state as shown, flat-band voltage shifts in the direction of charge loss of $\leq$ 25 mV were seen with either gate stressing voltages of 0 V or +4 V for 3×10^5sec. A 50 mV loss of charge was seen in taking the first C-V characteristic immediately after charging. Also negative bias stressing tests were performed to test for typical "perturbs" one would expect with this structure in an array. On a virgin sample like that in Fig. 19 a flat-band shift of 150 mV was seen in 2.1×10^5sec at $V_g = -6$ V. Fig. 21 shows charge build-up in the W layer with a stressing voltage of $V_g = -8$ V. Clearly, the charge build-up is saturating after the first few 1000 sec even though the W traps are essentially empty. Space charge build-up in the thin Si rich SiO_2 injector itself is limiting this current injection at -8 V (as discussed in section III-A) and is responsible for this phenomena which is desirable in actual device arrays. $V_g = -8$ V, which is about 1/3 of the write voltage, is a typical voltage some unwritten cells in an array might "see" while other cells are being written. Some bias stressing was done at elevated temperatures (up to 200°C). A slight acceleration in charge loss was seen at 200°C for 0 V or at +4 V stressing. However, this enhancement is what would be expected from the thermal

detrapping characteristics of captured electrons on W trapping sites[9]. As was shown in Section III-A, the weak temperature dependence of the electron injection from the Si rich SiO_2 layer only caused a slight increase in electron injection and trapping at elevated temperatures which is also desirable for potential EAROM device applications.

Using techniques involving the SI-MIS or GI-MIS ramp I-V and C-V characteristics which will be discussed in a future publication[16], it was clearly shown that the trapped charge (whose internal electric field is sensed by the substrate Si surface) is building up only in the W layer for the write conditions used here. At high negative gate voltages, trapping in the CVD and thermal SiO_2 layers will also occur.[16]

B. Multilayer Structures

In this section, a "multilayer" structure will be discussed which has high electronic current injection properties similar to those observed for Si rich SiO_2 layers on SiO_2. This multilayer was constructed by depositing on top of 400 Å of thermal SiO_2 four alternating layers of CVD polycrystalline Si islands approximately 20 Å or 40 Å in diameter (as determined from TEM[6]) which were separated by five alternating layers of CVD SiO_2, each layer 50 Å in thickness. Finally, an Al gate metallization with a 400°C forming gas anneal for 20 min was done. This structure was an attempt to intentionally duplicate the two-phase CVD Si rich SiO_2 layers. As seen in Fig. 22, a current enhancement for negative gate voltages was observed as compared to the control structure (Si – 400 Å thermal SiO_2 – Al). No pronounced dependence of this high current on the two sizes of poly-Si islands used (20 Å or 40 Å) was seen. More than likely some of the poly-Si was consumed during CVD SiO_2 deposition at 700°C. For positive gate bias, no current enhancement over the control was seen. In fact, the injected current was less than the control suggesting for this polarity that the multilayer structure appears to have a thicker insulating layer as would be expected. All samples were checked by RIE for lateral leakage currents influencing the ramp I-V characteris-

tics. Identical dark current results were obtained on the RIE-ed and non-RIE-ed sides of the wafers.

The first layer of poly-Si islands deposited on the thermal SiO_2 probably form planar interfaces with this smooth underlying oxide if not much of the poly-Si near the edges of the islands or grain boundaries is consumed during the CVD SiO_2 depositions. However, each successive layer of poly-Si islands will not be planar because of replication of the surface of the underlying poly-Si islands which are coated with thin CVD oxides. Poly-Si islands with curved surfaces facing the thermal SiO_2 layer will give field distortion and current enhancement.

V. CONCLUSIONS

Clearly, this paper has presented a totally controllable means for achieving high current injection into SiO_2 from any interface. The applications to non-volatile memory have been demonstrated and could lead to several new types of devices.

With further optimization of the injector, the possibility of switching times $\leq \mu$sec might be achieved, and then a non-volatile random-access-memory (NVRAM) could be realized. Optimization would entail even higher current injection at lower voltages using materials which would "effectively" give even lower barriers at the injecting interface. For example, stacked materials with decreasing energy bandgap in the direction of the metal or poly-silicon gate contact could be used. Silicon rich Si_3N_4 layers on top of silicon dioxide (CVD or thermal) layers are another interesting possibility which are also compatible with silicon technology. With "insulator engineering", the desired dark current-voltage characteristic could be attained for a given device application by stacking the appropriate insulators together.

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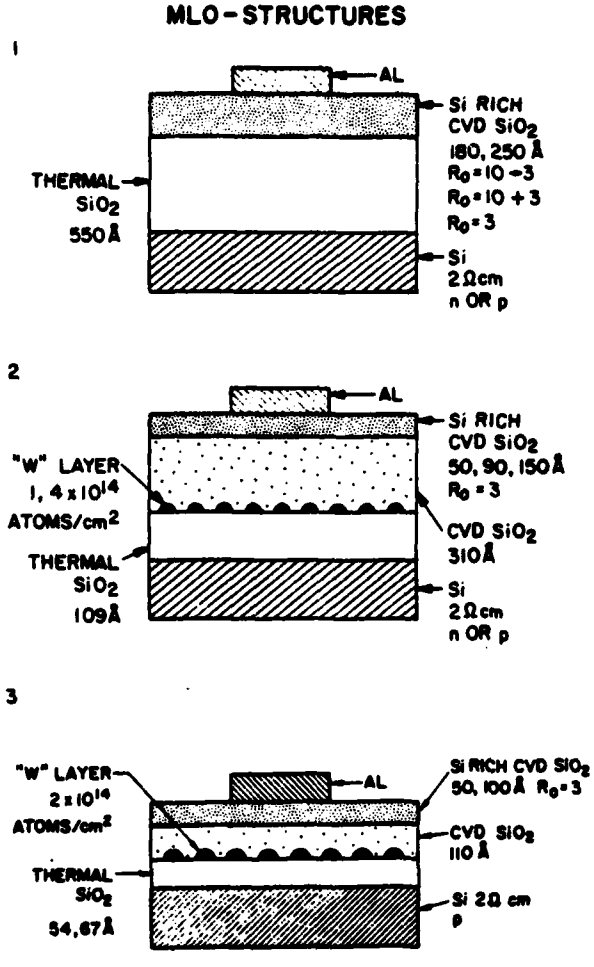


Fig. 1. **Schematic illustration chart of various types of samples used in this study. The Si rich SiO_2 layer was either stepped or graded with $R_o = [N_2O] / [SiH_4]$ shown in Fig. 2 as an indicator of the Si content of this layer. R_o from 10 (40% atomic Si) to 3 (46% atomic Si) was used with Si content increasing towards the top metal gate electrode when several layers were stacked on top of the underlying SiO_2 ($R_o = 10 + 3$) or when a graded layer was used ($R_o = 10 \rightarrow 3$).**

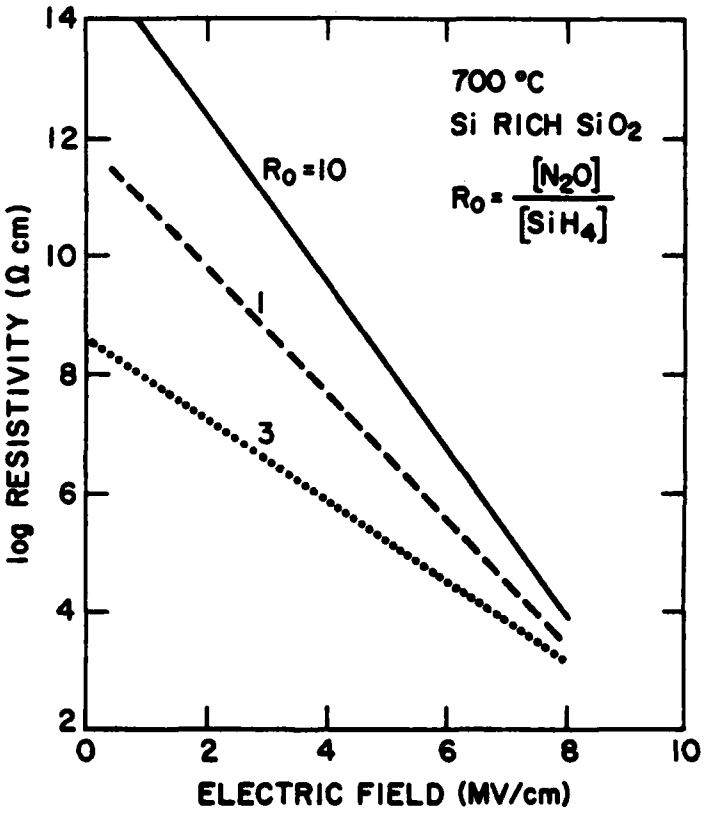


Fig. 2. Logarithm of the resistivity of various types of Si rich SiO_2 layers used in this study as a function of the average electric field. Taken from Reference 7.

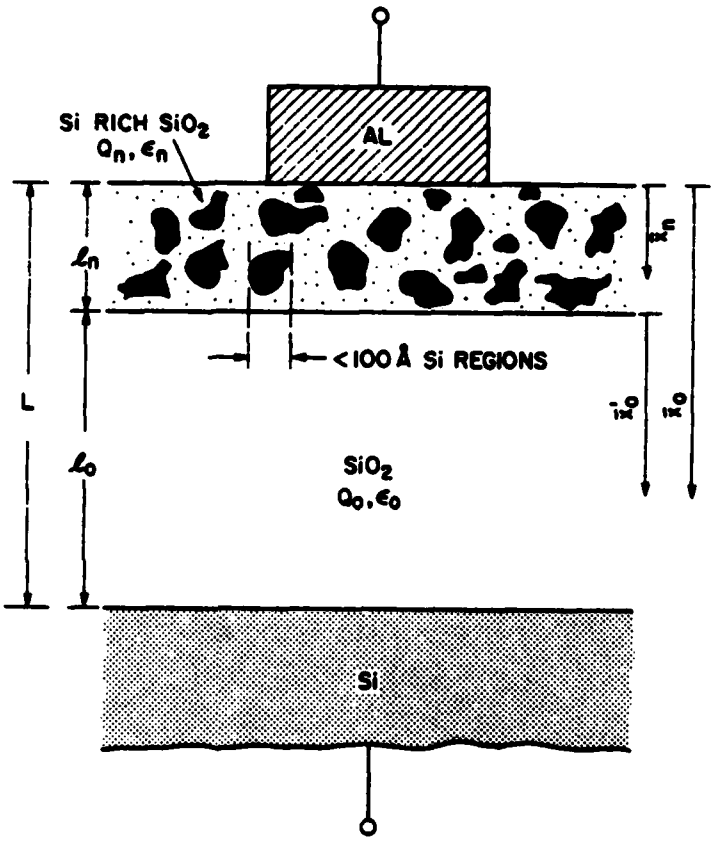


Fig. 3. **Schematic illustration of proposed two phase model of the Si rich SiO_2 injector incorporated into a SI-MIS capacitor.**

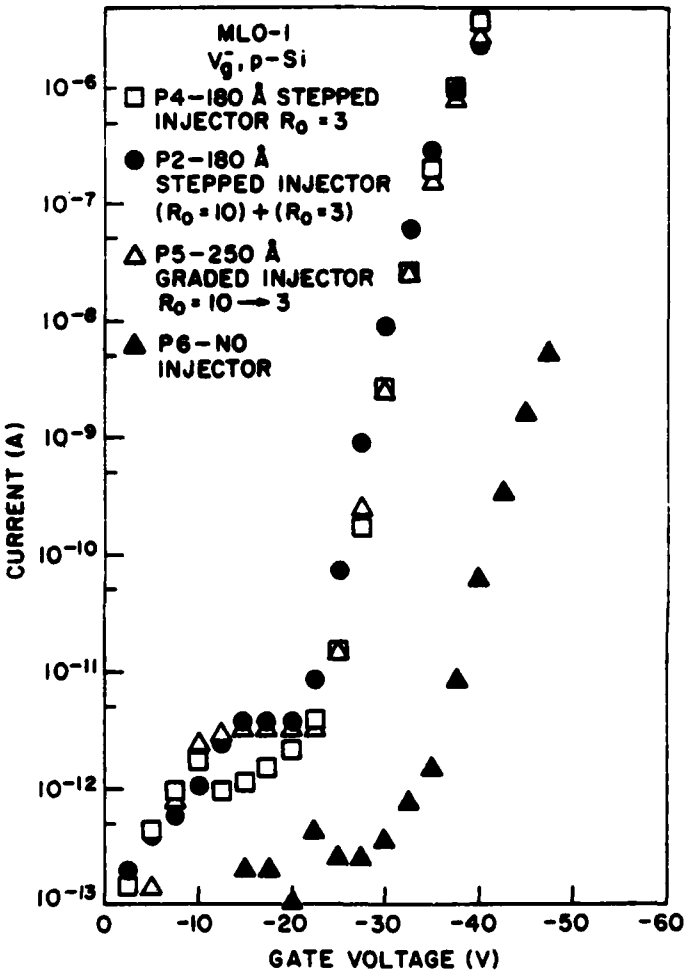


Fig. 4. **Point by point magnitude of the dark current as a function of negative gate voltage on various GI-MIS and SI-MIS structures from group #1 of Fig. 1. In this measurement, the gate voltage was stepped by −2.5 V starting from 0 V every 20 sec with the dark current being measured 18 sec after each voltage step increase.**

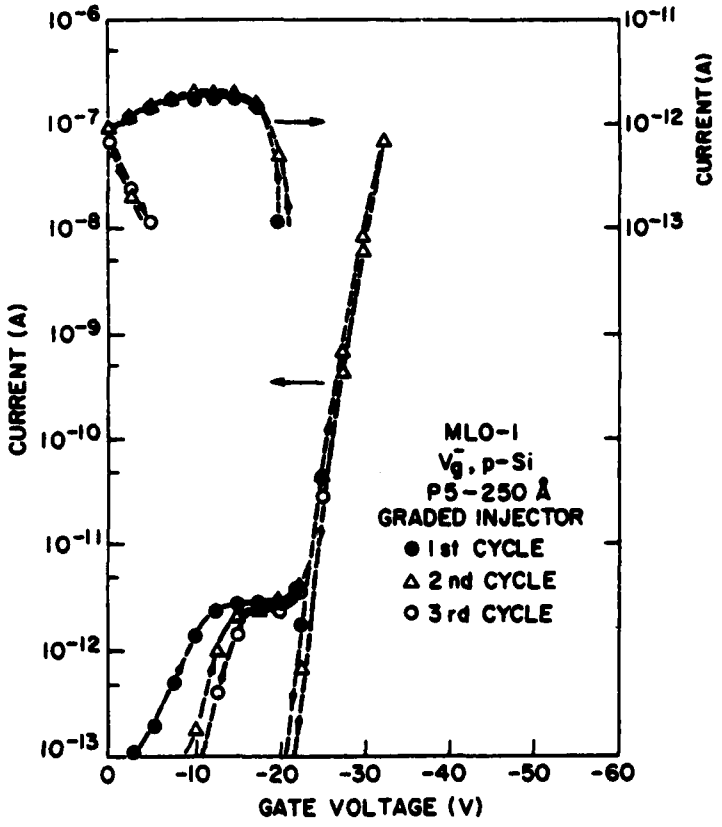


Fig. 5. Point by point magnitude of the dark current as a function of negative gate voltage on a GI-MIS structure from group #1 of Fig. 1 which was cycled three times. Same measurement conditions as in Fig. 4 with return trace also being recorded. Data in the upper left-hand corner of this figure and the corresponding current scale indicate current reversal during the return portion of the cycle stepping back to 0 V with 2.5 V per step increments.

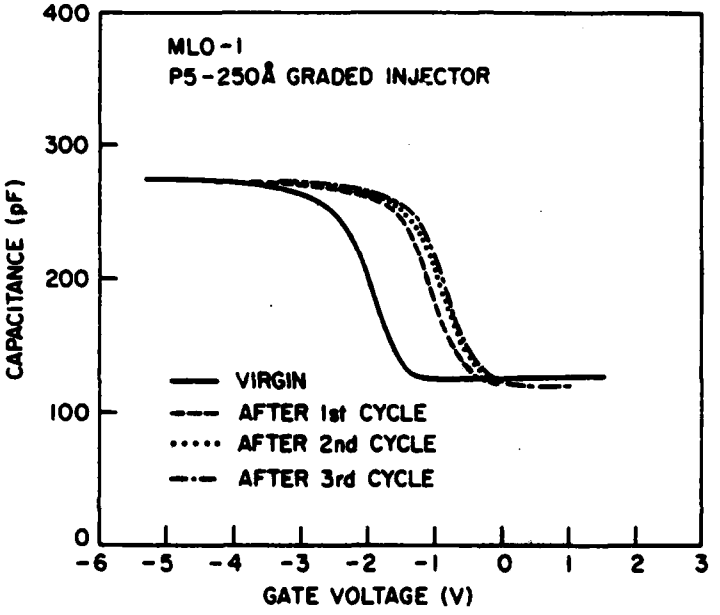


Fig. 6. High frequency (1 MHz) capacitance as a function of gate voltage on the same sample as in Fig. 5 before cycling (virgin) and after each cycle shown in Fig. 5.

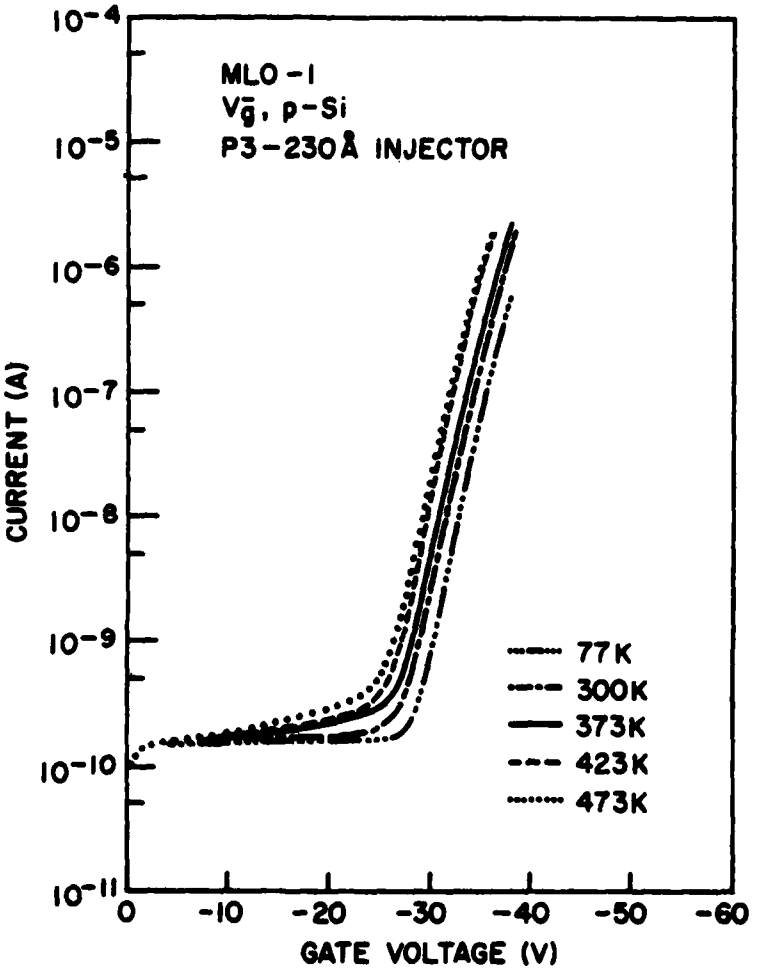


Fig. 7. **Ramped (−.47 V/sec) magnitude of the dark current as a function of negative gate voltage on a SI-MIS structure from group #1 of Fig. 1 for various temperatures from 77°K to 200°C.**

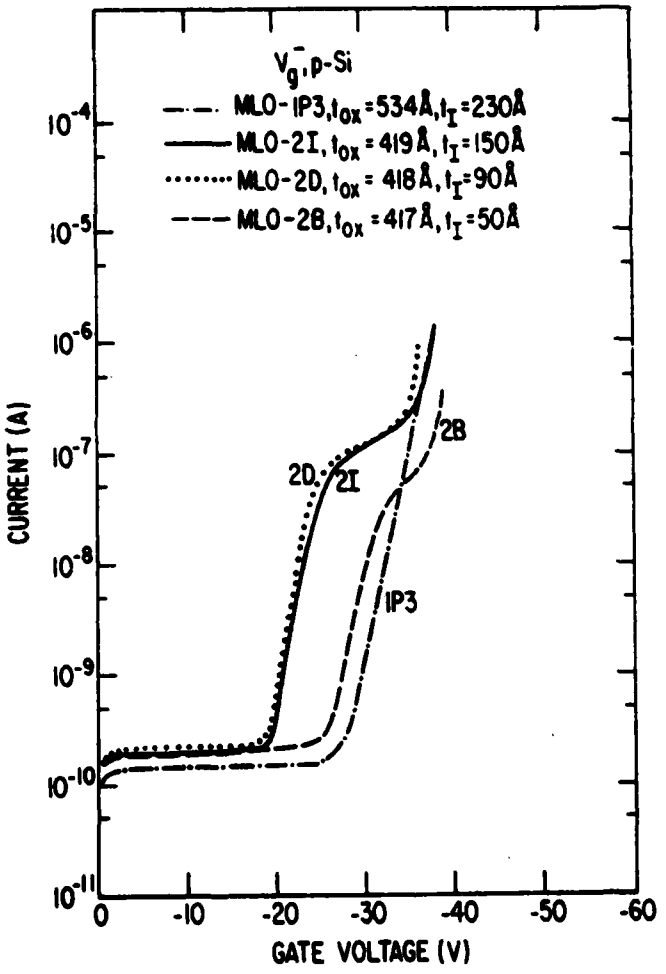


Fig. 8. **Ramped (−.47 V/sec) magnitude of the dark current as a function of negative gate voltage on various SI-MIS structures without a W trapping layer described in Fig. 1 for various Si rich SiO_2 injector thicknesses.**

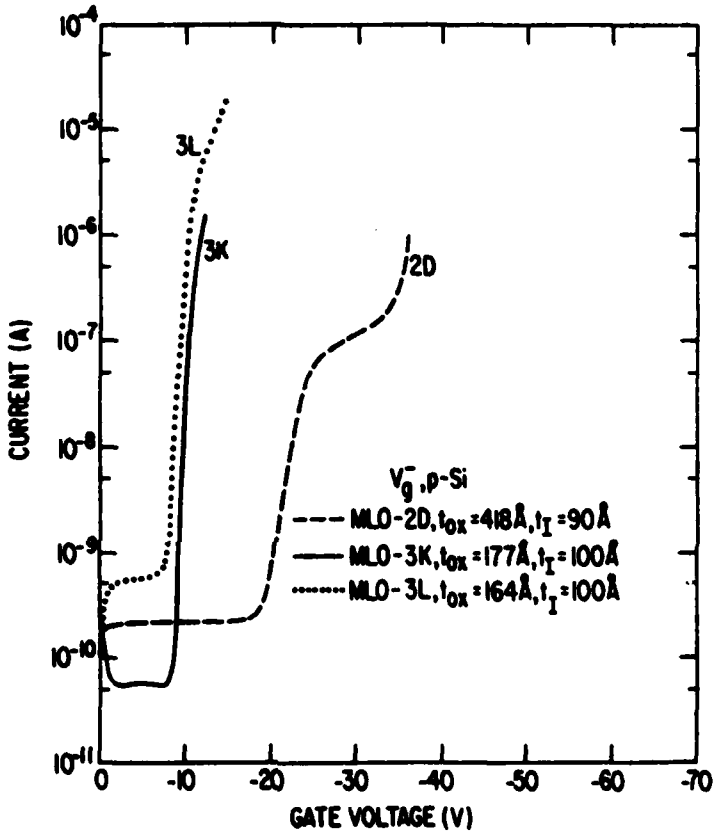


Fig. 9. Ramped (−.47 V/sec) magnitude of the dark current as a function of negative gate voltage on various SI-MIS structures without a W trapping layer described in Fig. 1 for various total SiO_2 (thermal and CVD) thicknesses.

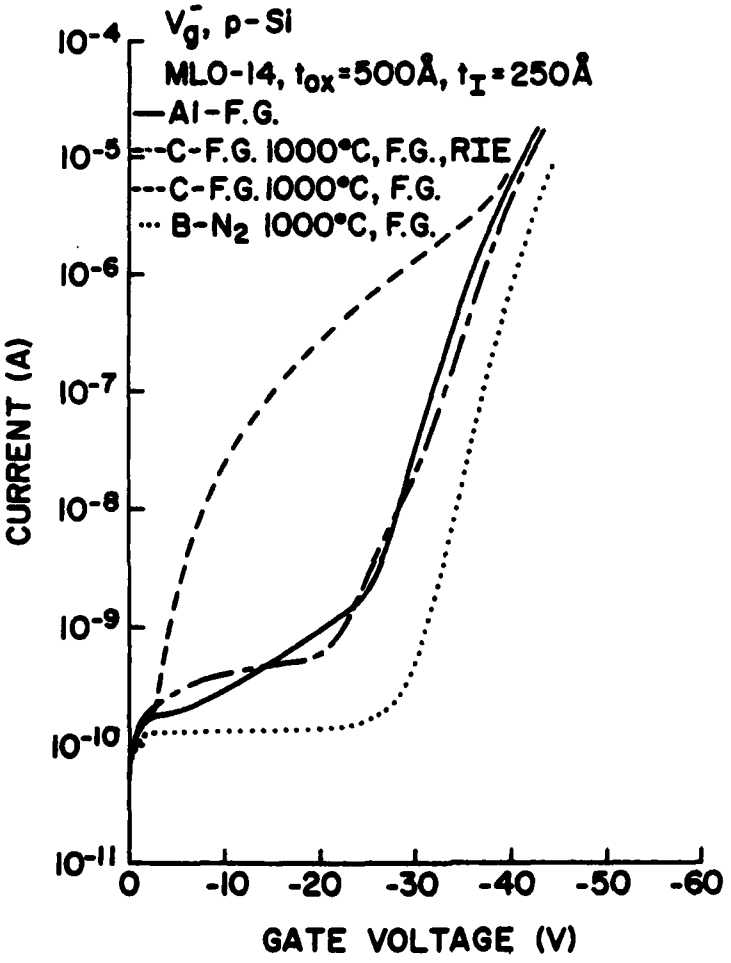


Fig. 10. Ramped (−.47 V/sec) magnitude of the dark current as a function of negative gate voltage on SI-MIS structures annealed under various conditions. The high temperature anneals (1000°C, 30 min) were done prior to metallization. The 400°C forming gas (90% N_2 and 10% H_2) anneal was performed after Al gate metallization. The thermal SiO_2 layer was 500 Å thick and the R_o = 3 Si rich SiO_2 injector was 250 Å thick. Reactive ion etching (RIE) of MLO-14C down to the underlying SiO_2 layer was done in CF_4 using the Al gate electrode as a mask to reduce surface leakage currents.

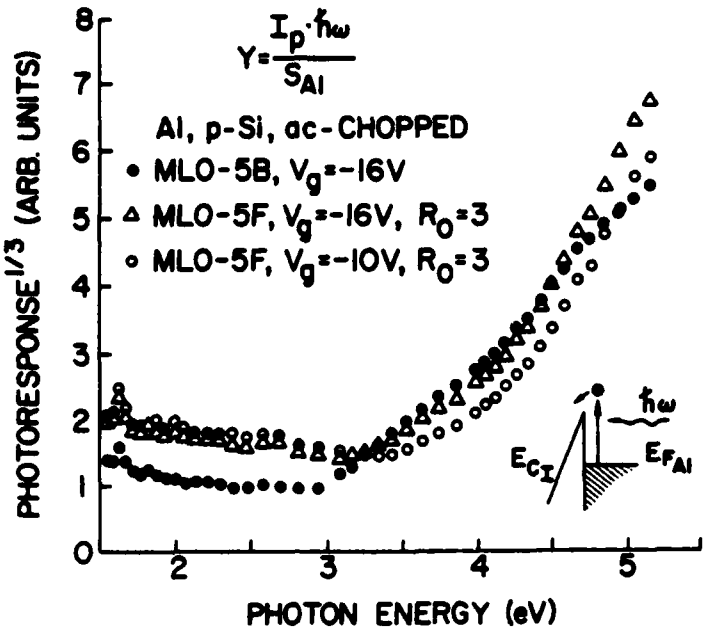


Fig. 11. Cube root of the a.c. photoresponse as a function of photon energy on various SI-MIS structures under negative gate voltage bias. R_o = 3 Si rich SiO_2 material with a thickness of 120 Å was used for the injector on MLO-5F, the gate electrode was Al (135 Å), and the thermal SiO_2 thickness was 290 Å. MLO-5B is the control structure with no injector.

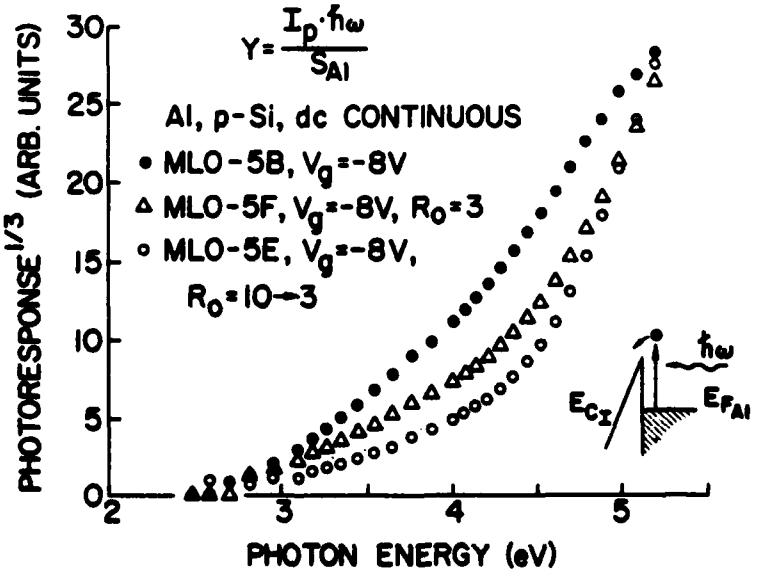


Fig. 12. Cube root of the d.c. photoresponse as a function of photon energy on various SI-MIS and GI-MIS structures under negative gate voltage bias. R_o = 3 or R_o = 10→3 Si rich SiO_2 material with a thickness of 120 Å was used for the injector on MLO-5F and MLO-5E, respectively; the gate electrode was Al (135 Å); and the thermal SiO_2 thickness was 290 Å. MLO-5B is the control structure with no injector.

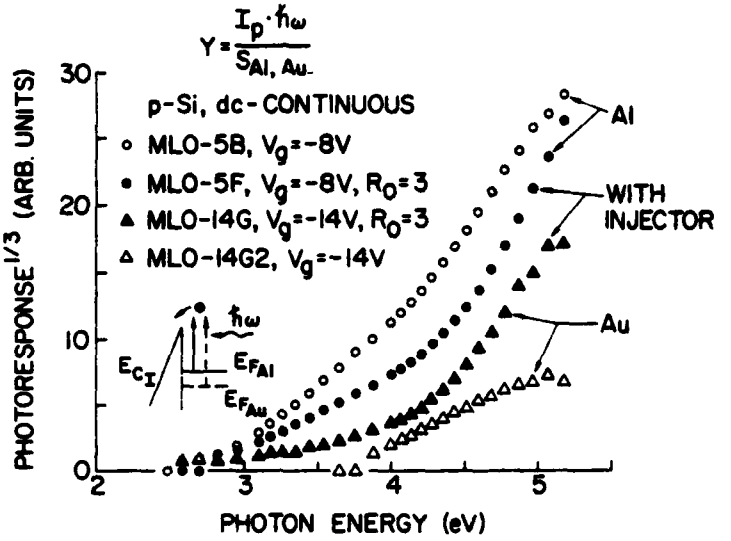


Fig. 13. Cube root of the d.c. photoresponse as a function of photon energy on various SI-MIS structures under negative gate voltage bias. R_0 = 3 Si rich SiO_2 material with thicknesses of 120 Å on MLO-5F and 250 Å on MLO-14G was used for the injector, the gate electrode was Au (200 Å) or Al (135 Å) where indicated, and the thermal SiO_2 thicknesses were 290 Å on MLO-5B and MLO-5F and 500 Å on MLO-14G and MLO-14G2. MLO-5B and MLO-14G2 are control structures with no injectors.

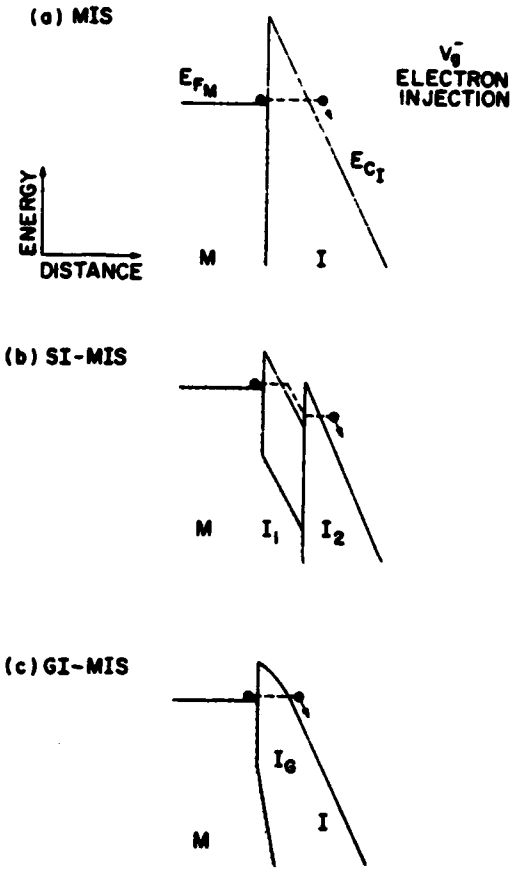


Fig. 14. Schematic energy band representation of (a) normal electron Fowler-Nordheim tunneling into SiO_2 from a metal gate electrode under negative voltage bias as compared to enhanced current injection due to energy bandgap stepping or grading with (b) SI-MIS and (c) GI-MIS structures for the same average electric field in the SiO_2 layer. Taken from Reference 29.

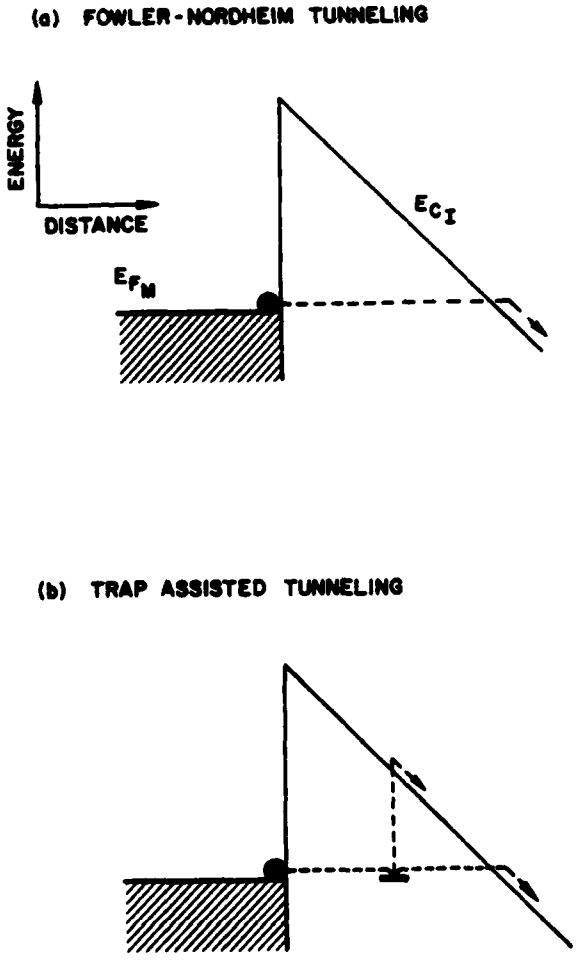


Fig. 15. Schematic energy band representation of (a) electronic Fowler-Nordheim tunneling into SiO_2 as compared to enhanced current injection due to (b) trap assisted tunneling for the same average electric field in the SiO_2 layer. Once an electron has tunneled directly from the metal electrode to the trap, it can either thermalize (vertical ---) or tunnel again (horizontal ---) to the SiO_2 conduction band.

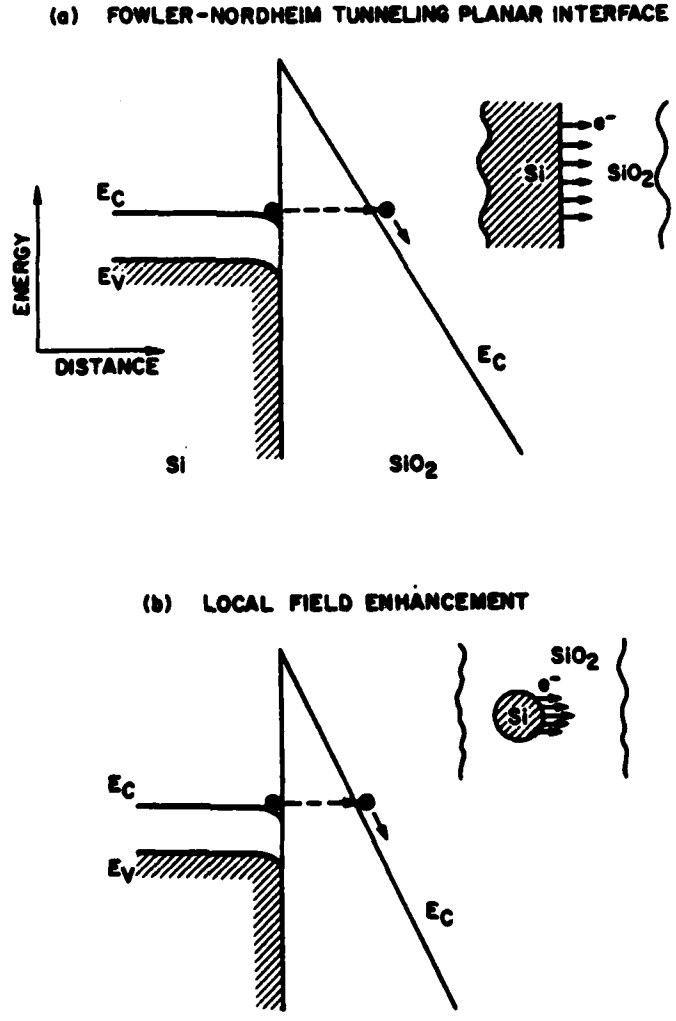


Fig. 16. Schematic energy band representation of (a) electronic Fowler-Nordheim tunneling into SiO_2 from a planar Si surface as compared to (b) enhanced current injection from a Si sphere whose curvature causes an increase in the local electric field near its interface with SiO_2.

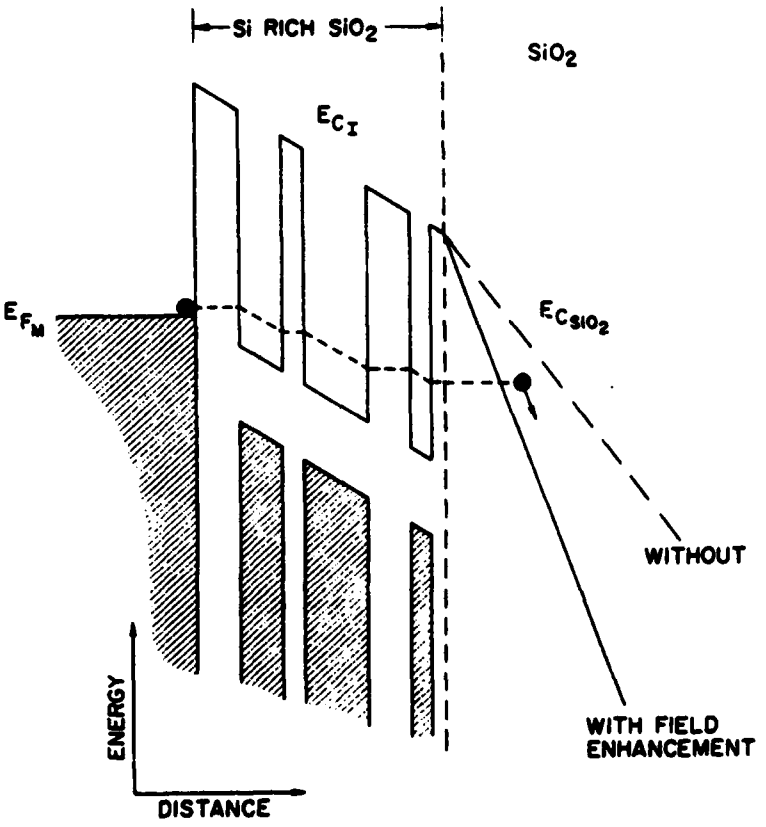
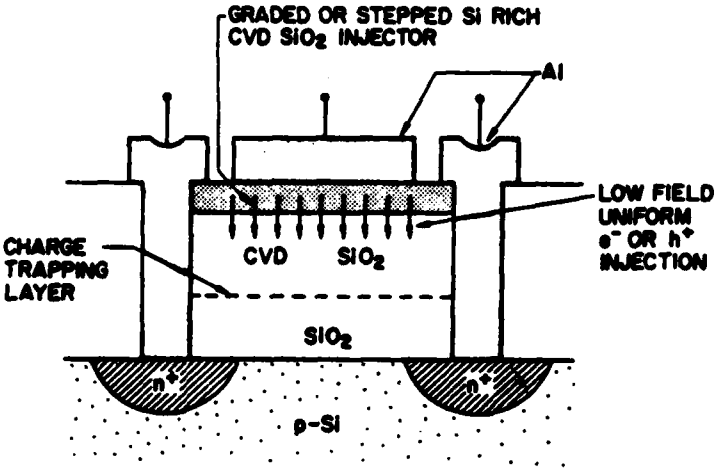


Fig. 17. Schematic energy band representation of conduction in the Si rich SiO_2 layer via hopping (direct tunneling between isolated amorphous Si regions in the SiO_2 matrix of this two phase system) and subsequent high field injection into the underlying SiO_2 region due to local electric field distortions such as shown in Fig. 16b.

(a) GI-MOS



(b) FAMOS

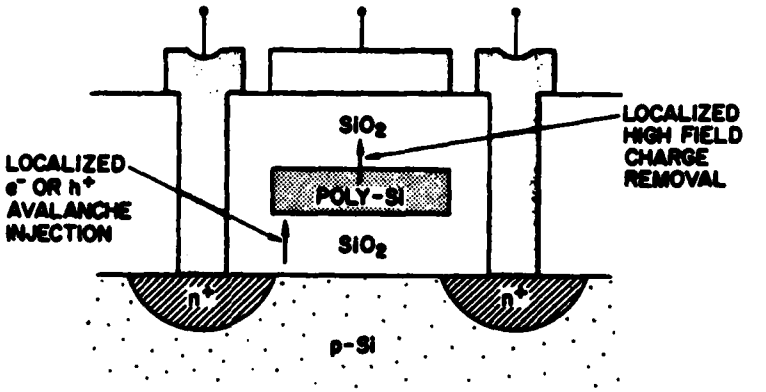


Fig. 18. Schematic representation of EAROMs in an n-channel field effect transistor (FET) configuration where (a) is an example of a GI-MIS or SI-MIS FET with a charge trapping layer and (b) is a stacked-gate FAMOS FET with a poly-Si charge storage layer. Charge injection for "writing" or "erasing" these structures is indicated by the arrows. Structures are not drawn to scale.

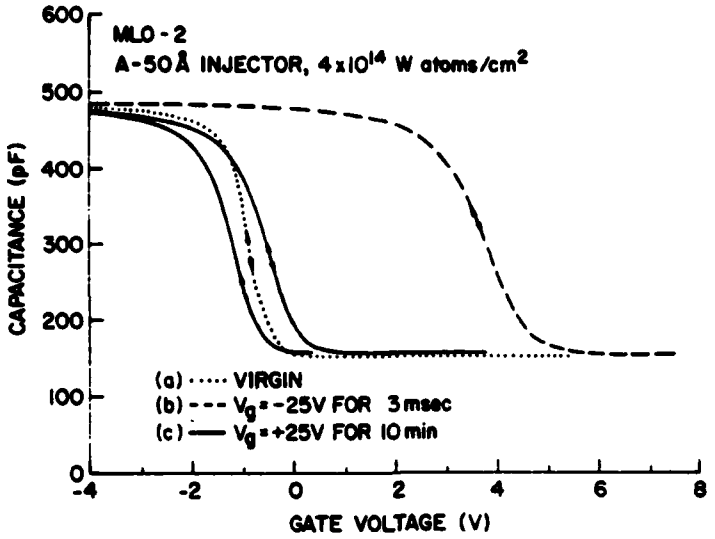


Fig. 19. Capacitance as a function of gate voltage on a SI-MIS structure with a W trapping layer from group #2 of Fig. 1 for various charge states: (a) virgin as-fabricated structure, (b) after "writing" (electron injection and trapping on W layer) with −25 V for 3 msec, and (c) after "erasing" (trapped electron removal or annihilation) with +25 V for 10 min. Hystersis in curve c was seen in taking first C-V trace as indicated.

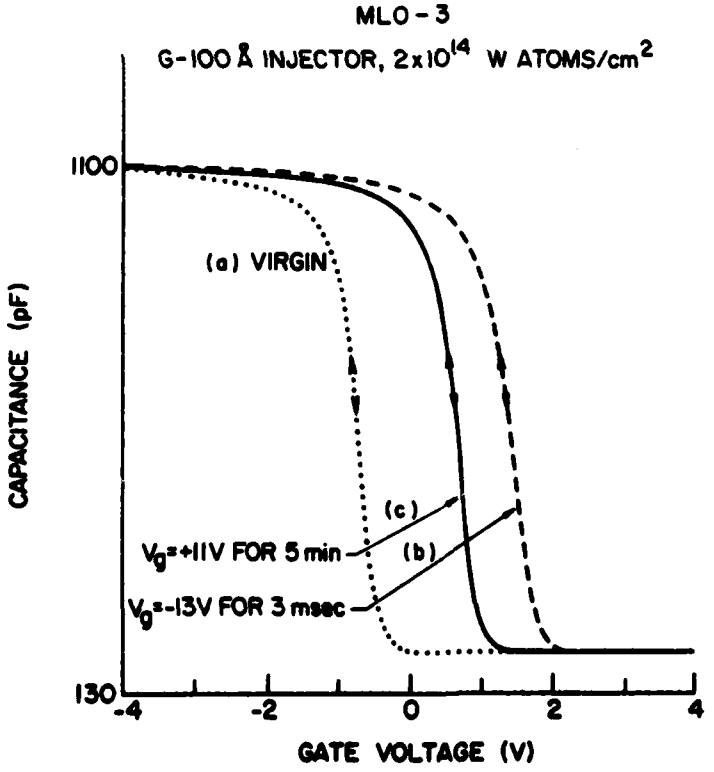


Fig. 20. Capacitance as a function of gate voltage on a SI-MIS structure with a W trapping layer and a thermal oxide thickness of 54 Å from group #3 of Fig. 1 for various charge states approximately equivalent to those in Fig. 19 except that this structure could not be erased back to its virgin charge state.

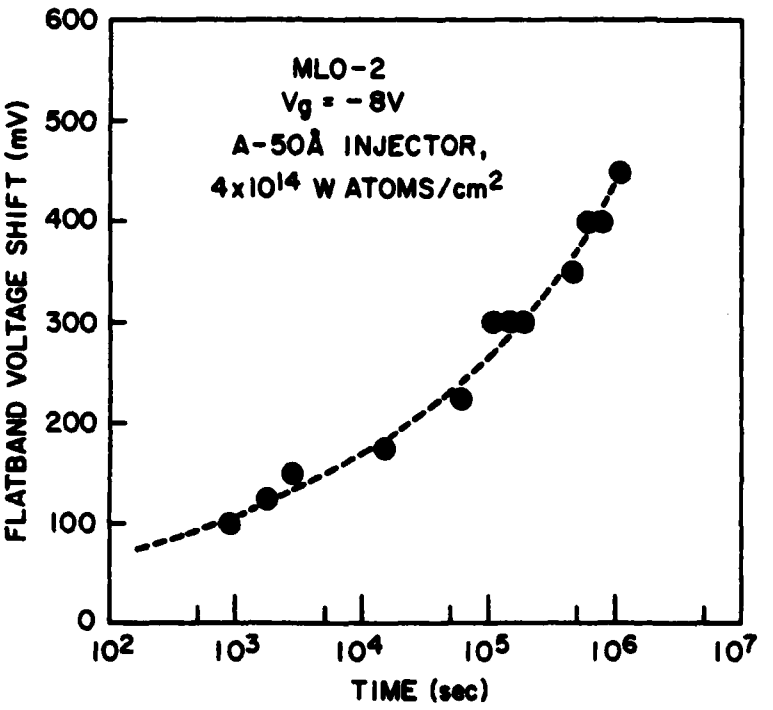


Fig. 21. **Flatband voltage shift as a function of time on a SI-MIS structure equivalent to that in Fig. 19 which was stressed with V_g = −8 V from an initial uncharged virgin state. Voltage shifts indicate "perturbs" due to unintentional writing of W trapping layer.**

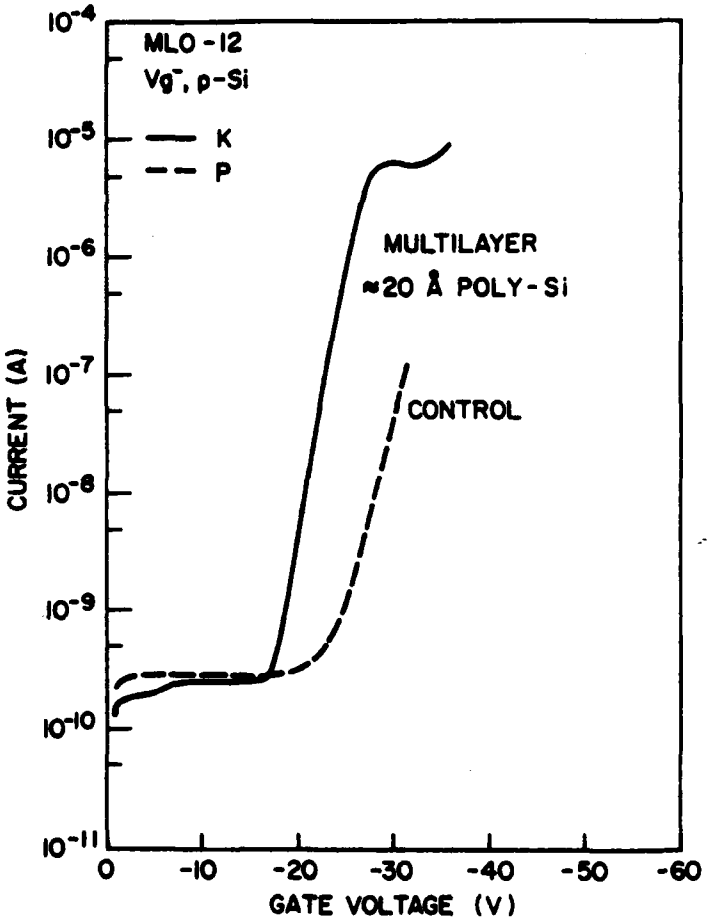


Fig. 22. Ramped (−.47 V/sec) magnitude of the dark current as a function of negative gate voltage on a "multilayer" structure made up of alternating layers of poly-Si islands and CVD SiO_2 stacked on top of thermal oxide as described in the text and on a control structure which had an identical thermal oxide but no "multilayer".

CHARGE TRAPPING STUDIES IN SiO_2 USING HIGH CURRENT INJECTION FROM Si RICH SiO_2 FILMS

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Abstract: The high electron injection phenomenon of Si rich SiO_2 films deposited on top of SiO_2 can be used for novel charge trapping studies of sites normally present or purposely introduced in the SiO_2. From the position and extent of current ledges observed in dark current as a function of ramped gate voltage (I-V), the capture cross section and total number of traps can be determined. Using these measurements with capacitance as a function of gate voltage (C-V), the trap distribution centroid and number of trapped charges can also be found. Several experimental examples are given including trapping in thermal SiO_2, in chemically vapor deposited (CVD) SiO_2, and on W less than a monolayer thick sandwiched between thermal and CVD SiO_2. These SI-MIS ramp I-V results for the trapping parameters are shown to be in good agreement with those determined using the conventional photo I-V and avalanche injection with flat-band voltage tracking techniques. A numerical simulation of the ramp I-V measurements assuming electric field-enhanced Fowler-Nordheim tunneling at the Si rich SiO_2-SiO_2 interface is described and is shown to give good agreement with the experimental data. These techniques for SI-MIS structures are faster and easier, although less accurate, than the conventional techniques.

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I. INTRODUCTION

Thin Si rich SiO_2 layers deposited on SiO_2 and incorporated into stepped or graded insulator metal-insulator-silicon (SI-MIS or GI-MIS) structures, as shown in Fig. 1, give high electron injection into the SiO_2 layer at moderate negative gate voltages [1,2]. Fig. 2 illustrates this phenomenon and compares various SI-MIS and GI-MIS structures to a control sample with no Si rich SiO_2 injector layer present, but otherwise processed in an identical fashion. This high current injection at moderate gate voltages will be shown to allow dark current as a function of gate voltage (dark I-V) characteristics to be used for easy, rapid, trap characterization on sites normally present or purposely introduced in SiO_2 layers. Fig. 3 shows charge trapping ledges caused by traps in a chemically vapor deposited (CVD) SiO_2 layer on top of thermal SiO_2 [3] and on W (less than a monolayer thick) related sites sandwiched between these two oxide layers [3-8]. The ledges only appear on samples fabricated with the thin Si rich SiO_2 injector. No ledges are seen on samples without the injector present, although in principle they should appear [9]. This absence of trapping ledges is due to the high applied electric fields necessary to get significant current injection in normal MIS structures. The high electric fields probably pull charge carriers out of the traps as soon as they are captured possibly by field ionization, and/or the high fields decrease the trapping rate of the carriers [3]. As will be shown here, the position and extent of the charge trapping ledges in dark I-V characteristics will give the trapping parameters of interest: initial trapping probability, capture cross-section, and total number of traps [3]. When these dark I-V characteristics are used together with capacitance as a function of gate voltage (C-V) measurements [10,11], the centroid and total amount of trapped charge can also be determined.

The details of the high current injection phenomena produced by the CVD Si rich SiO_2 layers has been discussed in a previous publication [2]. The high current is believed to be caused by a localized electric field distortion at the Si rich SiO_2 – SiO_2 interface due to the two phase (amorphous Si and SiO_2) nature of this material [12-14], by the size (tens of Angstroms) and large density of the amorphous Si regions [12,13], and by the low resistivity of the Si rich SiO_2 layer itself compared to SiO_2 [14]. However, the trapping parameters of sites in the SiO_2 region (not the Si rich SiO_2 injector) are independent of the details of the injection process; they depend only on the magnitude of the current injected at moderate gate voltages.

Three different trapping sites will be investigated using the SI-MIS ramp I-V technique described here. These sites include traps normally present in thermal SiO_2 layers grown on Si substrates [15,16], traps normally present in CVD SiO_2 layers deposited on thermal SiO_2 [3], and W related trapping sites produced by depositing W, less than a monolayer thick, between

thermal and CVD SiO_2 layers [3-8]. In each case, the results of trap characterization from the SI-MIS ramp I-V measurements will be compared to results obtained using conventional avalanche-injection with flat-band voltage tracking [16-18] and photocurrent as a function of gate voltage (photo I-V) techniques [5,19,20]. This comparison shows good agreement in all cases. The main advantages of SI-MIS ramp I-V measurements will be shown to be its speed and simplicity, particularly when large numbers of samples must be tested.

In section II, the sample preparation and experimental apparatus will be described. In section III, the SI-MIS ramp I-V technique will be presented together with the experimental results for the three trapping sites under consideration here. Comparison with conventional techniques to show the accuracy of the technique will also be performed. Finally in section IV, a numerical simulation will be compared to the experimental ramp I-V results.

II. EXPERIMENTAL

A. Sample Preparation

The Si rich SiO_2 layers were chemically vapor deposited (CVD) on top of thermal SiO_2 layers grown on <100> 2 Ωcm p-type single crystal Si substrates or on top of CVD SiO_2 layers. All thermal SiO_2 layers were given a 5 min. - 1000°C - N_2 anneal prior to being removed from the furnace. In some cases, CVD SiO_2 layers were stacked on top of the thermal SiO_2 layers prior to CVD Si rich SiO_2 deposition. A top gate electrode of Al with an area of .006 cm^2 and a thickness of 4,000 Å was then deposited from resistance heated W boats under a vacuum of less than 10^{-6} Torr. All Al electrode samples had a 400°C forming gas (90% N_2 - 10% H_2) anneal for 20 min performed after metallization. In some samples, a W layer less than a monolayer in thickness was deposited between the thermal and CVD SiO_2. The samples used in this study are summarized below:

MLO - 2D	Si - thermal SiO_2 (109 Å) - CVD SiO_2 (310 Å) - Si rich SiO_2 (90 Å) - Al
MLO - 2F	Si - thermal SiO_2 (109 Å) - W (1×10^{14} atoms/cm^2) - CVD SiO_2 (310 Å) - Si rich SiO_2 (90 Å) - Al
MLO - 1P4	Si - thermal SiO_2 (535 Å) - Si rich SiO_2 (180 Å) - Al

Control samples without the Si rich SiO_2 layer present, but otherwise identically processed (MLO-2K, MLO-2J and MLO-1P6, respectively) were also fabricated.

The CVD SiO_2 and Si rich SiO_2 were deposited at 700°C using a concentration ratio, R_o, of N_2O to SiH_4 in the gas phase of 100 and 3, respectively [14]. For $R_o = 3$, the Si rich SiO_2 has an excess of 13% atomic Si over stoichiometric SiO_2 [14]. The resistivity of this Si rich SiO_2 film is much less than that of SiO_2 at any electric field strength [14]. Na^+ levels were shown to be $\lesssim 3 \times 10^{11}$ cm^{-2} as measured by the use of temperature bias stressing (+10 V at 200°C for 30 min, then cooled back down to room temperature under +10 V bias). All samples were stored in a nitrogen dry box when not in use.

B. Apparatus

Dark I-V measurements, done at a constant but adjustable voltage ramp rate dV_g/dt where V_g is the voltage on the gate electrode, used a Keithley #26000 logarithmic picoammeter to measure current. Point-by-point dark current as a function of gate voltage measurements were performed using the same voltage stepping unit used in photo I-V measurements, previously described [20]. The experimental apparatus to do photocurrent as a function of gate voltage (photo I-V) [5,19,20], capacitance as a function of gate voltage (C-V) [10,11], and avalanche-injection with flat-band voltage tracking [16-18] have also been described in previous publications. Photo I-V and avalanche-injection with flat-band tracking measurements were used to determine independently the trapping parameters.

III. CHARGE TRAPPING STUDIES

In this section, the SI-MIS or GI-MIS ramp I-V technique is described in detail and applied to trapping in thermal SiO_2, CVD SiO_2, and on W-related sites. In section III-A, the physics describing the occurrence of the charge trapping ledges for any site is discussed.

A. CVD SiO_2 and W Traps

Examples of charge trapping ledges in I-V characteristics obtained at a constant voltage ramp rate are shown in Figs. 3-5 for the CVD SiO_2 traps and "W" traps. Similar characteristics are seen in these figures for voltage ramp rates from −.047 V/sec to −47 V/sec. The constant displacement currents observed at gate voltages before current injection starts are equivalent to $C_I(dV_g^-/dt)$ where C_I is the total dielectric stack capacitance.

The ledge occurs when the electric field near the injecting interface is being held approximately constant since the increase in the internal field of the trapped electron space

charge build-up nearly cancels the increase due to the voltage ramp. The electric field near the injecting interface at any time t can be shown from simple electrostatics (using Poisson's equation) [5,20] to be given by

$$E(t) = \frac{(V_g^- - \Phi_{ms} - \Psi_s) - Q_o\frac{(L-\bar{x}_o)}{\varepsilon_o} - Q_n[\frac{(\ell_n-\bar{x}_n)}{\varepsilon_n} + \frac{\ell_o}{\varepsilon_o}]}{\ell_n + \frac{\varepsilon_n}{\varepsilon_o}\ell_o} \quad (1)$$

for the case of a dual dielectric structure where the "o" and "n" subscripts refer to the layers closest to the Si substrate and Al gate electrode, respectively. In the case considered here "o" refers to the total SiO_2 layer (thermal and CVD oxides) while "n" refers to the thinner Si rich SiO_2 layer. Fig. 1 schematically shows the dual dielectric structure and the notation used in this section with the origin of coordinates at the Al–Si rich SiO_2 interface. In Equation 1, L is the total thickness of the composite structure ($L = \ell_o + \ell_n$), ℓ_o (ℓ_n) is the thickness of the SiO_2 layers of the composite structure (Si rich SiO_2 layer), Φ_{ms} is the work function difference between the metal and semiconductor electrodes, Ψ_s is the silicon surface potential, $\bar{x}_o$ ($\bar{x}_n$) is the centroid of the trapped charge distribution in the SiO_2 layer (Si rich SiO_2 layer) as measured from the Al interface with the Si rich SiO_2 layer, Q_o (Q_n) is the "bulk" trapped charge per unit area of this distribution in oxide layer (Si rich SiO_2 layer), and ε_o (ε_n) is the low frequency permittivity of SiO_2 (Si rich SiO_2 layer).

The thin Si rich SiO_2 layers are neglected in the calculations that follow because of their low resistivity as compared to SiO_2. This is shown in Fig. 6 where the quasi-static capacitance, $C = I_{ext}/(dV_g^-/dt)$ where I_{ext} is the current measured in the external circuit, as a function of gate voltage characteristic [21] is plotted. This characteristic is observed to switch at low voltages from a value indicative of a two layer dielectric stack with dielectric constants of 3.9 and 7.5 for the SiO_2 and Si rich SiO_2 layers, respectively, to a value close to that of the SiO_2 layer alone. This figure indicates that the conductivity of the Si rich SiO_2 is much greater than that of SiO_2 as expected [14], and little voltage is dropped across this layer at the gate voltages of interest in the ramp I-V studies which will be described. However, small signal a.c. (15 mV rms) measurements from 1 MHz to 100 Hz at any negative voltage bias where the p-Si substrate is accumulated also indicate a dual dielectric stack of SiO_2 and Si rich SiO_2 with dielectric constants of 3.9 and 7.5, respectively. The dip observed in the quasi-static measurements between 0 and −1 V is due to the capacitive response of the p-Si in series with the insulator stack [21]. Therefore, in these calculations, the injection current per unit area J^- ($J^- = I^-/A$ where A is the electrode area) is limited by the SiO_2–Si rich SiO_2

interface. I^- is the particle current which is equivalent to the current measured in the external circuit minus the displacement current due to the voltage ramp; that is, $I_{ext} - C_I (dV_g^-/dt)$. The dependence of this current density on Si rich SiO_2 composition and thickness has been previously described [2]. It will be shown in this section that for the well known case of electron trapping on "W" atoms sandwiched between thermal and CVD SiO_2 layers [3-8], the centroid of the captured carriers is in excellent agreement with the actual location when the thin Si rich SiO_2 layer is ignored. As J^- becomes large enough, a particular trapping center starts to fill and

$$\frac{dQ_o(t)}{dt} = J_I^- \sigma_{c_o} N_{\infty_o}. \tag{2}$$

Here J_I^- is the current level per unit area ($J_I^- = I_I^-/A$) near the start of the ledge (see Figs. 4 and 5), σ_{c_o} is the capture cross section, and N_{∞_o} is the total number of traps per unit area. Under the approximate condition that $\frac{dE(t)}{dt} \approx 0$ when the traps start to fill, using Equation 1 and neglecting the Si rich SiO_2 layer,

$$\frac{dV_g^-}{dt} = \frac{1}{\varepsilon_o}(\ell_o - \bar{x}'_o)\frac{dQ_o(t)}{dt} \tag{3}$$

Here $\bar{x}'_o$ is the centroid distance measured from the SiO_2-Si rich SiO_2 interface where $\bar{x}'_o = \bar{x}_o - \ell_n$. Also, this equation would also hold for any double dielectric system where $\frac{dQ_n}{dt} = 0$ since $L - \bar{x}_o = \ell_o - \bar{x}'_o$. Equation 3 assumes that the silicon surface potential and charge centroid in the oxide layer do not change with time. The former assumption is true for the p-Si substrates used here, because they are strongly accumulated for the negative gate bias conditions of these measurements. The latter condition will be shown to be true from the data for the cases considered here. In general, this latter condition is satisfied if the initial trapping probability ($N_{\infty_o}\sigma_{c_o}$) is $\lesssim .3$ [3-5,19]. Substituting Equation 2 into Equation 3 and solving for $N_{\infty_o}\sigma_{c_o}$ yields

$$N_{\infty_o}\sigma_{c_o} = \frac{\varepsilon_o}{(\ell_o - \bar{x}'_o)}\frac{\frac{dV_g^-}{dt}}{J_I^-}. \tag{4}$$

As seen in Figs. 4 and 5, $N_{\infty_o}\sigma_{c_o}$ is independent of the voltage ramp rate $\frac{dV_g^-}{dt}$ divided by J_I^-. Therefore, the onset of the charge trapping ledge should move to larger negative gate voltages with increasing rate ramp due to the finite slope of the dark current-voltage characteristic. This is seen experimentally in Figs. 4 and 5. Integration of Equation 3 over the extent of the

current ledge (from traps unfilled to traps filled) yields

$$N_{\infty_o} = \varepsilon_o \frac{\Delta V_{g_L}^-}{q(\ell_o - \bar{x}_o')} \tag{5}$$

where q is the charge on an electron (-1.6×10^{-19} coul) and $\Delta V_{g_L}^-$ is the voltage width of the ledge (see Figs. 4 and 5). Substituting Equation 5 into Equation 4 yields,

$$\sigma_{c_o} = \frac{\dfrac{q\, dV_g^-}{dt}}{\Delta V_{g_L}^- J_I^-} \tag{6}$$

Table I lists values for σ_{c_o}, N_{∞_o}, and $N_{\infty_o}\sigma_{c_o}$ determined using the technique described here and compares them to values determined using avalanche injection with flat-band voltage tracking [18] on similar MIS structures without the Si rich SiO_2 layer. As seen from this table, the agreement is very good. The values for the charge distribution centroids $\bar{x}_o'$ which are needed to find N_{∞_o} and $N_{\infty_o}\sigma_{c_o}$ were determined using a technique which will be described next.

Figures 7–10 show sequential C-V and ramp I-V measurements on the same SI-MIS structures as in Figs. 4 and 5. Before and after each ramp I-V cycle, a C-V trace is recorded starting with the as fabricated virgin sample. From the flat-band voltage shifts ΔV_{FB} obtained from the C-V characteristics and the voltage shifts ΔV_g^- obtained from the ramp I-V measurements, the trapped charge per unit area in traps located in one of the SiO_2 (thermal or CVD) layers and the centroid of this distribution can be obtained in much the same way as with the photo I-V technique [5,19,20]. The voltage shifts ΔV_{FB} and ΔV_g^- indicate the extent of trap filling at any time as reflected by the electric field in the Si substrate near the Si–SiO_2 interface and in the SiO_2 layer near the SiO_2–Si rich SiO_2 interface, respectively. ΔV_g^- is equivalent to that portion of the charge trapping ledge traversed during a ramp I-V cycle (or between cycles) and, in this case, it is always a negative number.

The C-V flat-band voltage shift, ΔV_{FB} [10,11], and the ramp I-V voltage shift, ΔV_g^- [15,19,20], can be shown from electrostatics to be

$$\Delta V_{FB} = -Q_o \left[\frac{(\bar{x}_o - \ell_n)}{\varepsilon_o} + \frac{\ell_n}{\varepsilon_n} \right] - \frac{\bar{x}_n Q_n}{\varepsilon_n} \tag{7}$$

and

$$\Delta V_g^- = \frac{Q_o}{\varepsilon_o}(L - \bar{x}_o) + Q_n \left[\frac{(\ell_n - \bar{x}_n)}{\varepsilon_n} + \frac{\ell_o}{\varepsilon_o} \right] \tag{8}$$

for a dual dielectric system with trapped charges Q_o and Q_n in the SiO_2 layer and Si rich SiO_2 layer, respectively, as discussed previously. Equation 8 is derived from Equation 1. ΔV_g^- is the change in gate voltage necessary to keep the electric field near the injecting interface, E(0), approximately constant as traps fill during a dark current, ramp I-V measurement. Assuming that the trapped charge state of the Si rich SiO_2 layer is not changing significantly during the ramp I-V cycle which can be verified experimentally (see Reference 2 and compare Figures 7, 9 and 11), equations 7 and 8 reduce to

$$\Delta V_{FB} = -Q_o \left(\frac{\bar{x}_o'}{\varepsilon_o} + \frac{\ell_n}{\varepsilon_n} \right) \tag{9}$$

$$\Delta V_g^- = \frac{Q_o}{\varepsilon_o}(\ell_o - \bar{x}_o') \tag{10}$$

where the relation $\bar{x}_o = \bar{x}_o' + \ell_n$ has been used. If the low resistivity of the Si rich SiO_2 layer during current injection into SiO_2 is taken account of as was done in an earlier portion of this section by neglecting this layer, Equation 10 would still be valid. However, the Si rich SiO_2 layer can <u>not</u> be neglected during high frequency, small signal, a.c. C-V measurements as stated earlier. As seen, Equation 9 must contain a term indicating this layer's contribution to the total a.c. capacitance. From Equations 9 and 10, the total number of trapped charges per unit area N_o and centroid $\bar{x}_o'$ as measured from the SiO_2-Si rich SiO_2 interface is given by

$$\frac{\bar{x}_o'}{\ell_o} = \left(1 - \frac{\Delta V_g^-}{\Delta V_{FB}}\right)^{-1} x \left(1 + \frac{\Delta V_g^-}{\Delta V_{FB}} \frac{\varepsilon_o \ell_n}{\varepsilon_n \ell_o}\right) \tag{11}$$

and

$$N_o = \frac{\varepsilon_o}{q\ell_o}(\Delta V_g^- - \Delta V_{FB}) \times \left(1 + \frac{\varepsilon_o}{\varepsilon_n}\frac{\ell_n}{\ell_o}\right)^{-1} . \quad (12)$$

Clearly, Equations 11 and 12 reduce to the well known single dielectric results for bulk trapped charge [5,19,20], if $\ell_n \to 0$ and $\bar{x}_o' \to \bar{x}_o$. Tables II and III summarize the values of $\bar{x}_o'/\ell_o$ and N_o deduced from Equations 11 and 12 using the experimental quantities ΔV_g^- and ΔV_{FB} obtained from the data of Figs. 7 and 8 for "W" trapping and Figs. 9 and 10 for CVD oxide trapping. Values of $\bar{x}_o'/\ell_o$ determined in this manner are in good agreement with the predicted position of $\bar{x}_o'/\ell_o$ and with the value of $\bar{x}_o/\ell_o$ determined using the photo I-V technique on similar MIS samples without the Si rich SiO_2 layer present. This agreement is also summarized in Tables II and III. As seen from the tables, the centroid is not a very strong function of the amount of trapped charge. This is expected for the two cases considered here where the initial trapping probability is $\approx .3$ for a delta-function-like "W" trapping distribution and $\approx 4 \times 10^{-3}$ for approximately uniformly distributed trapping in the CVD oxide.

Trapping in the CVD oxide which is believed to be related to H_2O incorporated into the film during deposition shows another interesting phenomena. When these traps are nearly filled with electrons, a compensating positive charge appears in the film near the Si-SiO_2 interface and causes the C-V characteristic to shift to lower gate voltages. The values for N_{o_e} and N_{o_p} in the last entry in Table III showing this phenomena were calculated from ΔV_{FB} and ΔV_g^- using relationships like Equations 9 and 10 containing terms for the positive and negative charges with the centroids of each distribution assumed to be $\bar{x}'_{o_e}/\ell_o = .25$ for the electrons and $\bar{x}'_{o_p}/\ell_o = 1$ for the positive charges. The appearance of this positive charge was not dependent on the voltage ramp rate and therefore the current level (see Fig. 4). It tended to appear at electric fields of 8-9 MV/cm in the oxide films. This type of positive charge phenomena is also seen in thermal SiO_2 layers at higher currents and will be discussed later. Native thermal SiO_2 trapping sites have capture probabilities $\leq 10^{-5}$, and these traps also are thought by some researchers to be related to H_2O [3,15,16]. High temperature annealing (1000°C in N_2 for 30 min) on the CVD SiO_2 layers, lowers the trapping probability and hence moves the current ledge to higher current levels. This annealing is believed to drive off H_2O. The appearance of the positive charge at the Si–SiO_2 interface under negative gate bias voltage conditions is believed by some to be related to the diffusion of a neutral species to the Si–SiO_2 interface where it is subsequently ionized or dissociated. Weinberg has argued that excitons may cause this phenomena [22], but agrees that atomic hydrogen could produce

a similar result [23]. Atomic hydrogen released during electron capture by some of the water related sites [15], its diffusion to the Si–SiO_2 interface, and its ionization to H^+ still remains a possible explanation.

B. Thermal SiO_2 traps

Charge trapping in thermal SiO_2 layers was also investigated using the ramp I-V technique described in preceding paragraphs. Figure 11 shows sequential ramp I-V cycling through a charge trapping ledge caused by electron traps in a thermal SiO_2 layer, and Figure 12 shows the corresponding C-V characteristics. These figures also show that the formation of the positive charge at the SiO_2 interface [3,16,23,24] occurs at lower negative bulk trapped charge densities but at about the same electric field magnitudes (8-9 MV/cm). The formation of the positive space charge did not depend on the injection current level as was similarly seen for the CVD oxide case.

From Figure 11 and Equations 4, 5, and 6, the initial trapping probability, the effective capture cross sections, and total number of traps per unit area can be determined for the sites which capture electrons. For $J_I^- = -3 \times 10^{-5}$ A/cm^2 and $\Delta V_{g_L}^- = -17$ V, $N_{\infty_o} \sigma_{c_o} = 1.2 \times 10^{-5}$; $\sigma_{c_o} = 8.9 \times 10^{-19}$ cm^2; and $N_{\infty_o} = 1.4 \times 10^{13}$ cm^{-2}. These results were not very sensitive to current level as was similarly seen for the CVD oxide and W trapping results. In these calculations, $\bar{x}'_{o_e}$ was set equal to $\ell_o/2$ (charge centroid is half the SiO_2 thickness) which has been shown using the photo I-V technique on MOS structures without the Si rich SiO_2 injector [3,16,23]. The results for $N_{\infty_o} \sigma_{c_o}$, σ_{c_o}, and N_{∞_o} are consistent with results reported in the literature for electron trapping sites believed to be related to H_2O [3,15,16,23]. Initial trapping probabilities are $\lesssim 10^{-5}$ with trap densities and capture cross sections dependent on processing [3,16]. In a recent paper by Young et al. using avalanche injection-flatband voltage tracking and photo I-V techniques, capture cross-sections for sites in SiO_2 films of the same thickness without the injector were determined to be $\approx 3 \times 10^{-18}$ cm^2 and 3×10^{-19} cm^2 for two traps with about the same densities [16]. This is in good agreement with the result here which would more heavily weigh the larger cross section trap. The total number of thermal SiO_2 traps per unit area determined (1.4×10^{13} cm^{-2}) on the SI-MIS structure used here was larger than the total determined by Young et al. (2.8×10^{12} cm^{-2} [16]). However, Young's structures saw a 1000°C anneal in N_2 for 30 min prior to metallization which reduces the H_2O content of the films and therefore the number of these traps.

One conclusion concerning the electric field dependence of the appearance of positive charges in CVD and thermal oxides comes from comparing the previous results. This positive charge appears at electric field magnitudes between 8-9 MV/cm in these films. The magnitude of the average field ($|V_g - \Phi_{ms} - \Psi_s|/L$) is $\approx$ 8.5 MV/cm, while the magnitude of the field near the Si-thermal SiO_2 interface is $\geq$ 9 MV/cm (which is equal to the magnitude of the average field plus ΔV_{FB}). Approximately the same magnitudes of the electric fields ($\geq$ 9 MV/cm) were observed on control samples without the Si rich SiO_2 injector when positive charge started to form. However, for these controls, very little negative charging in the bulk of the CVD oxide or thermal oxide layers was observed because of the normally low injection currents from the Al-SiO_2 interface under negative voltage bias. The extent of this positive charge formation was low (much less than observed in Figs. 10 and 12), and these structures suffered destructive voltage breakdown when the formation of the positive charge began. If similar structures with CVD SiO_2 on top of thermal SiO_2 (see Table III) but no Si rich SiO_2 injector were charged using internal photoemission or avalanche injection to similar trapped electron densities, no large positive charge formation was observed. However, some small amounts of positive charge were observed particularly under internal photoemission from the Al. Here the electric field magnitudes at the Si-SiO_2 interface were $\lesssim$ 5.8 MV/cm and the average field magnitudes were $\lesssim$ 7 MV/cm because of the electron injection techniques used with the Al internal photoemission experiments having higher field magnitudes at the Si-SiO_2 interface. The overall conclusion from comparing all results is the possibility that positive charge which forms at the Si-SiO_2 interface could also be influenced, at least in part, by the high electric fields at this interface. The dependence of this positive charge on bulk CVD SiO_2 or thermal SiO_2 electron trapping, as far as the negative gate voltage ramp I-V measurements are concerned, could be due to the added contribution to the field at the Si-SiO_2 interface from the trapped negative space charge. However, under avalanche injection from the substrate Si where the *electric field* at this interface is held *constant* [16,18] for a constant injection current density, positive charges were observed to build up in both CVD SiO_2 and thermal SiO_2 MOS structures which were not annealed to drive out H_2O [16], but not in the annealed structures, after negative bulk oxide charge trapping started. Thus, it appears that this positive charge formation depends on both the amount of H_2O in the oxide layers and the local electric field at the Si-SiO_2 interface.

Weinberg et al. also saw positive charge build-up near the Si-SiO_2 interface at high electric fields using negative corona charging of the exposed SiO_2 surface [25]. They observed an electric field magnitude threshold of $\approx$ 11 MV/cm at an electron current density of 5×10^{-7} A/cm^2 for this charge build-up. They attempted to use a model dependent on hole

tunneling from the Si substrate into the SiO_2 layer, but the results were not consistent with simple Fowler-Nordheim tunneling. Weinberg subsequently saw a dependence on the crystallographic Si substrate orientation [26].

The positive oxide charges near the Si-SiO_2 interfaces behaved on all samples somewhat like "slow" donor states which could be filled or discharged by tunneling electrons from or to the Si conduction band at positive and negative voltages, respectively. This behavior was also observed by Young et al. [16] on thermal SiO_2 MOS structures in which the interfacial positive charge was formed after avalanche injecting $\lesssim .1$ coul/cm^2 of electrons under positive voltage bias conditions independent of the current level [16] (similar to the SI-MIS structures). Somewhat less than this amount of injected negative charge ($\gtrsim .01$ coul/cm^2) was necessary in the negative gate bias ramp I-V measurements on the SI-MIS structures to start the positive charge formation (see Figs. 11 and 12). However, the SI-MIS structures have a larger number of thermal SiO_2 traps than Young's oxides [16] as was described previously. Thus, it appears that the same phenomena are occurring in both Young's experiments [16] and the ones described here on the SI-MIS structures.

IV. NUMERICAL SIMULATION

In this section, a computer simulation of the ramp I-V measurements is described and is shown to give good agreement with the experimental data for the three cases considered in section III which scan the range of trapping probabilities from 3×10^{-1} to 1.2×10^{-5}. The ramp I-V current measured in the external circuit, I_{ext}, is composed of two terms

$$I_{ext} = C_o \frac{dV_g^-}{dt} + J^-(t) \times A \qquad (13)$$

where the first term refers to the displacement current due to the ramp rate dV_g^-/dt and the capacitance of the thermal oxide layer and/or CVD SiO_2 layer, C_o, and the second term is the injected particle current per unit area. The Si rich SiO_2 layer is neglected because of its high conductivity as described in section III-A.

Previous experimental evidence suggests that the injected particle current is controlled by the Si rich SiO_2 interface with the SiO_2 layer, and that it is Fowler-Nordheim-like in nature [27,28]. Furthermore, due to the two phase (amorphous Si and SiO_2) composition of the Si rich SiO_2 layer, densely packed amorphous Si regions embedded in an SiO_2 matrix have been proposed to give electric field distortions which locally increase the field on a microscopic scale near the Si rich SiO_2 – Si interface. However, due to the microscopic nature of the

distortions and their density, the trapping sites in the SiO_2 layer away from this interface "see" an approximately uniform injection in a macroscopic sense [2]. Therefore, in the simulation, the particle current per unit area, J^-, has been modeled as Fowler-Nordheim emission from a Si conduction band from the amorphous Si regions into an SiO_2 conduction band at the Si rich SiO_2 – SiO_2 interface with a field enhancement factor χ due to the field distortions caused by the two phases. J^- is given by [27]

$$J^-(t) = \frac{q^3[\chi E(t)]^2}{16\pi^2\hbar\Phi_B} \exp\left[\frac{-4(2m_e^{*})^{1/2}\Phi_B^{3/2}}{3\hbar\chi\,|qE(t)|}\right] \tag{14}$$

where $\hbar$ is Planck's constant divided by 2π, Φ_B is the barrier height from the Si conduction band to the SiO_2 conduction band (3.1 eV was used [3], with no corrections for image-force barrier lowering which would be small), and m_e^* is the effective mass of a tunneling electron (.5 of the free electron mass was used [27,28]). Corrections for temperature dependence which would be small [27] were also not included in Equation 14. The electric field, E(t), near the Si rich SiO_2 – SiO_2 interface can be derived from Equation 1 by again neglecting the Si rich SiO_2 layer because of its high conductivity assuming $Q_n \to 0$, $\ell_n \to 0$, and $\varepsilon_n \to \varepsilon_o$. With these assumptions, Equation 1 reduces to

$$E(t) = \frac{(V_g^-(t)-\Phi_{ms}-\Psi_s)}{\ell_o} - \frac{Q_o(t)}{\varepsilon_o}\frac{(\ell_o-\bar{x}_o)}{\ell_o} \tag{15}$$

Finally, the build-up of trapped charge on any sites either normally present or purposely introduced in an SiO_2 layer can be described from first order kinetics for trapping probabilities less than unity by [3]

$$\frac{dQ_o(t)}{dt} = \frac{J^-(t)}{q}\,\sigma_{c_o}\,[qN_{\infty_o}-Q_o(t)]. \tag{16}$$

This equation reduces to Equation 2 for the case where the traps are nearly empty ($N_{\infty_o} >> Q_o(t)/q$) near the start of the charge trapping ledge as discussed in section III-A.

Equations 13–16 uniquely define the current measured in the external circuit as a function of ramped gate voltage. They form a non-linear system that must be solved numerically. It was found that the well known Runge-Kutta method of interpretation gave excellent results if the initial condition $Q_o(0) = 0$ was replaced by the analytic behavior (A.12), as described in the Appendix. In addition, a mesh size of the order of one-tenth of the voltage range during which the current first rises steeply gave accurate results. This voltage difference

is directly proportional to $\tau_2 - \tau_1$ of the Appendix [cf. Eqs. (A.11), (A.13), and (A.15)]. Equations 4 and 5 for the current at the ledge and the extent of the ledge are dimensional equivalents of Eqs. (A.14) and (A.17). All these considerations are embodied in a simple interactive APL program the first calls for experimental conditions, and then automatically calculates the turning points, the mesh size and useful voltage range, and finally computes the current, field, and trapped charge as a function of gate voltage.

Figures 13 and 14 show the solutions of the equations and plots $N_o - V_g$, $|E| - V_g$, and $|I_{ext}| - V_g$ characteristics for the case of electron trapping on W related sites embedded in an oxide layer. Figures 15 and 16 show the numerical simulation of $|I_{ext}| - V_g$ for the case of electron trapping in CVD SiO_2 and thermal SiO_2 sites. The open circles in Figs. 13, 15 and 16 are the experimental data from the ramp I-V measurements on SI-MIS structures MLO-2F, MLO-2D, and MLO-1P4, respectively. The values of N_{o_o},σ_{c_o}, $\bar{x}_o$ used in the computer simulations were taken from Tables I, II and III and section III-B. The voltage ramp rate used was $-.47$ V/sec, and $\Phi_{ms} + \Psi_s$ was set equal to -1 V. The value of χ used was determined from the ratio of the voltages at constant current after the onset of particle current injection of the sample with no injector to the sample with the Si rich SiO_2 injector using the data of Figs 2 and 3. As can be seen in the simulation (Fig. 14), the traps start to fill near the start of the current ledge and the electric field remains approximately constant over the extent of the ledge until the traps are filled. These general results were also seen for simulations of CVD SiO_2 and thermal SiO_2 trapping. This verifies the assumptions concerning the onset of trapping and $dE/dt \approx 0$ used in section III-A to obtain Equations 4-6 from which charge trapping parameters were determined. As can be seen from Figs. 13, 15, and 16, the simulation is in good agreement with the experimental data for all the cases considered here, particularly in the first current rise and ledge regions.

V. CONCLUSIONS

The techniques discussed are clearly made possible by the property of the thin Si rich SiO_2 layer: high current injection at moderate average electric fields into the SiO_2 layers. Similar techniques to study charge trapping could be used with an MOS capacitor [9]. However, to get similar magnitudes of current in these MOS structures without a Si rich SiO_2 injecting layer requires very high average electric fields (see Fig. 4) which could field-ionize trapped charges as soon as they are captured and/or reduce significantly charge carrier capture rate [3]. Also voltage breakdown of the MOS structures due, for example, to weak spots is much more probable at the higher average fields.

These techniques using the SI-MIS structures are very advantageous in terms of speed as compared to conventional avalanche injection with flat-band voltage tracking to determine σ_{c_o} and N_{t_o} and photo I-V to determine Σ_o and N_o. However, the conventional techniques, although more tedious, are probably more accurate particularly in separating trapping sites with comparable capture probabilities as shown for thermal SiO_2. Ramp I-V and C-V measurements on SI-MIS structures are very practical when large amounts of data on many samples are required for trapping centers in SiO_2 either normally present, purposely introduced, or introduced inadvertently during processing.

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APPENDIX: Analytic approximations

For a constant ramp rate r, the gate voltage is $V_g^- = -rt$, and Eqs. (13-16) read

$$-I_{ext}/A = c - J^-, \tag{A.1}$$

$$-J^- = aE^2 \exp(-b/|E|), \tag{A.2}$$

$$E = -dt' + eN_o, \tag{A.3}$$

$$\frac{dN_o}{dt'} = f(-J^-)(N_{\infty_o} - N_o). \tag{A.4}$$

Here, t' stands for the shifted time variable $t - t_o$, where $t_o = -(\Phi_{ms} + \Psi_s)/r$, and N_o is the trapped charge at time t ($N_o = Q_o/q$). It is assumed that initial current injection due to the Si surface potential and work function differences between the Si and Al contacts is negligible, so that N_o, E, and therefore J^- are effectively zero for $t \leq t_o$. The constants a.....f (all positive) are obtained by comparing Eqs. (13-16) and (A.1-4). Thus

$$\left.\begin{aligned} &a = |q|^3\chi^2/16\pi^2\hbar\Phi_B, \quad b = 4(2m_e^*)^{1/2}\Phi_B^{3/2}/3\hbar|q|\chi, \\ &c = \varepsilon_o r/\ell_o, \quad d = r/\ell_o, \quad e = (|q|/\varepsilon_o)(1-\bar{x}_o/\ell_o), \\ &f = \sigma_{c_o}/|q|. \end{aligned}\right\} \tag{A.5}$$

The discussion is simpler if one transforms these equations to a dimensionless form. Introducing reduced field, charge, current, and time

$$\left.\begin{aligned} &\mathcal{E} = E/b, \quad u = -\ln[(N_{\infty_o} - N_o)/N_{\infty_o}], \\ &j = -J^-/c, \quad \tau = t'd/b, \end{aligned}\right\} \tag{A.6}$$

one gets the convenient form

$$-I_{ext}/Ac = 1 + j, \tag{A.7}$$

$$j = \alpha\mathcal{E}^2 \exp(-|\mathcal{E}|^{-1}), \tag{A.8}$$

$$\delta = -\tau + \beta(1 - \exp(-u)), \tag{A.9}$$

$$\frac{du}{d\tau} = \gamma j, \quad u(0) = 0. \tag{A.10}$$

In these equations, $\alpha = ab^2/c$ depends only on fundamental constants and the ramp rate, $\beta = eN_{s_o}/b$, and $\gamma = be_o f$. Note that the Fowler-Nordheim current has been normalized to the capacitive current c, that the product $\beta\gamma = N_{s_o}\sigma_{c_o}(1 - \bar{x}_o/\ell_o)$ gives the value of $N_{s_o}\sigma_{c_o}$, and that the time-like variable τ is proportional to V_g^-; thus,

$$V_g^- = -b\ell_o\tau + (\Phi_{ms} + \Psi_s). \tag{A.11}$$

The essential singularity of the Fowler-Nordheim current (A.8) precludes straightforward numerical integration. Therefore one must first find the initial behavior around $\tau = 0$ by Picard iteration. This will also yield useful analytic results. The initial condition suggests the first iterate $u_1 = 0$, and Eqs. (A.9) and (A.8) then give $\delta_1 = -\tau$ and

$$j_1 = \alpha\tau^2 \exp(-\tau^{-1}). \tag{A.12}$$

Insertion of expression (A.12) into (A.10) allows the computation of the second iterate u_2 in terms of exponential integrals, and the process can then be repeated. However, the above results are sufficient. For example, the first turning point τ_1, at which the current first rises rapidly is given by $j(\tau_1) \cong j_1(\tau_1) \cong 1$. This states nothing more than the equality of the capacitive and Fowler-Nordheim currents. Using Eq. (A.12) and taking logarithms, one easily sees that

$$\tau_1 \cong (\ln \alpha - 2 \ln \ln \alpha)^{-1}, \tag{A.13}$$

for large values of α, as is the case here.

The behavior for intermediate values of time is also readily available. As the space charge builds up, it creates a field opposed to that generated by the driving gate voltage. One expects the $\delta(\tau)$ and therefore the $j(\tau)$ curves to flatten. The time (voltage) τ_2 for this occurrence is given approximately by the condition $d\delta/d\tau \cong 0$ (see also the discussion of section III). Differentiating Eq. (A.9), using (A.10), and remembering that $N_o << N_{s_o}$ in that range, one gets

$$j(\tau_2) \cong (\beta\gamma)^{-1}. \tag{A.14}$$

If one approximates j by the first Fowler-Nordheim current j_1 [cf. Eq. (A.12)], then the current ledge begins when

$$\tau = \tau_2 \cong \left(\ln (\alpha\beta\gamma) - 2 \ln \ln (\alpha\beta\gamma) \right)^{-1}. \tag{A.15}$$

Note that $N_o/N_{\infty_o} \cong \tau/\beta +$ const. in the neighborhood of τ_2 as Eqs. (A.10) and (A.14) easily show.

Finally, the extent of the ledge is readily estimated, because this ledge terminates when all traps are filled. The condition $N_o \cong N_{\infty_o}$ implies $u \to \infty$ and $\varepsilon \to -\tau + \beta$. Therefore the current (A.8) becomes

$$j \sim \alpha (-\tau + \beta)^2 \exp (-|-\tau + \beta|^{-1}). \tag{A.16}$$

This is nothing more than another Fowler-Nordheim current, parallel to j_1 and displaced by an amount β on the $\tau-$ scale. Thus the current (A.16) increases rapidly for

$$\tau > \tau_3 = \tau_2 + \beta. \tag{A.17}$$

The estimates for τ_1, τ_2, and τ_3 are essential for the successful implementation of any integration scheme. Furthermore, the above results allow immediate computation of the physical quantities σ_{c_o} and $N_{\infty_o}(1 - \bar{x}_o/\ell_o)$. This is illustrated in section IV of the text.

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Table I

"W" – Trapping Parameters

Technique	$N_{\infty_0}\ \sigma_{c_0}$	$N_{\infty_0}(cm^{-2})$	$\sigma_{c_0}(cm^2)$
SI-MIS Ramp I-V	3.0×10^{-1}	1.1×10^{13}	2.7×10^{-14}
MIS†‡	3.1×10^{-1}	1.1×10^{13}	2.7×10^{-14}

CVD Oxide – Trapping Parameters

Technique	$N_{\infty_0}\ \sigma_{c_0}$	$N_{\infty_0}(cm^{-2})$	$\sigma_{c_0}(cm^2)$
SI-MIS Ramp I-V	4.1×10^{-3}	1.1×10^{13}	3.6×10^{-16}
MIS‡	3.4×10^{-3}	1.2×10^{13}	2.9×10^{-16}

† Taken from Table I of Reference 12 with correction for charge centroid position.

‡ MIS structures were used with avalanche injection and flatband voltage tracking techniques. Centroids were determined using the photo I-V technique.

Table II

"W" – Number of Trapped Charges
and Centroid Location

Ramp I-V Cycle	ΔV_g^-(V)	ΔV_{FB}(V)	$\mathbb{x}_o'/\ell_o$	$N_o(cm^{-2})$
3rd – 2nd	−2.5	7	.71	4.4×10^{12}
4th – 2nd	−4	11.2	.71	7.1×10^{12}
4th – 3rd	−1.5	4.3	.71	2.7×10^{12}

a) $\mathbb{x}_o'/\ell_o$ calculated $= \frac{310\ \text{Å}}{419\ \text{Å}} = .74$

b) $\mathbb{x}_o/\ell_o$ using photo I-V = calculated values knowing thickness of layers (see References 18 and 19).

Table III

CVD Oxide – Number of Trapped Charges and Centroid Location

Ramp I-V Cycle	ΔV_g^-(V)	ΔV_{FB}(V)	$\mathfrak{T}_{o_e}'/\ell_o$	$N_{o_e}(cm^{-2})$	$N_{o_p}(cm^{-2})$
2nd – 1st	−3.5	+1.4	.21	2.3×10^{12}	0
3rd – 1st	−9.5	+4.25	.23	6.4×10^{12}	0
3rd – 2nd	−6	+2.85	.25	4.1×10^{12}	0
4th – 1st	−14	−.75	.25 (Assumed)	9.5×10^{12}	3.3×10^{12}

$\mathfrak{T}_{o_e}'$ = centroid of trapped electron distribution; $\mathfrak{T}_{o_e}'/\ell_{o_{CVD}}$ range

$$= \frac{(.21 \rightarrow .25) \times 419\ \text{Å}}{310\ \text{Å}} = .28 \rightarrow .34$$

N_{o_e} = number of trapped electrons per unit area

$\mathfrak{T}_{o_p}'$ = ℓ_o = centroid of trapped positive charge distribution (assumed)

N_{o_p} = number of trapped positive charges per unit area

a) $\mathfrak{T}_{o_e}'/\ell_o$ calculated assuming uniform distribution in CVD oxide $= \frac{\frac{310\text{Å}}{2}}{419\text{Å}} = .37$

b) $\mathfrak{T}_{o_e}/\ell_{o_{CVD}}$ range using photo I-V = .16 → .31.

$\mathfrak{T}_{o_p}$ using photo I-V = ℓ_o

$\mathfrak{T}_{o_e}$ and $\mathfrak{T}_{o_p}$ determined using photo I-V sensing and internal photoemission charging from Al with 4.5 eV light and with V_g^- ranging from −7 to−35 V on a set of samples (.1 Ωcm p Si – 300 Å thermal SiO_2 – 350 Å CVD SiO_2 – 135 Å Al) equivalent to SI-MIS structures in Table III except for injector. $\mathfrak{T}_{o_e}/\ell_{o_{CVD}}$ shows a range of values for different amounts of trapped electrons similar to the densities in Table III. However, charging by avalanche injection from the Si substrate did move the centroid of the negative charge distribution closer to the center of the CVD oxide film. Trapped electron distribution increases near CVD oxide interfaces with other materials. No large accumulation of positive charge was observed at the Si-SiO_2 interface under avalanche-injection charging out to $\Delta V_{FB} \approx 16$ V; however, some was observed particularly under internal photoemission charging at −28 to −35 V.

FIGURE CAPTIONS

Fig. 1. Schematic illustration of proposed two phase model of the Si rich SiO_2 injector incorporated into a SI-MIS capacitor. Notation is defined in the text.

Fig. 2. Point by point magnitude of the dark current as a function of negative gate voltage on various GI-MIS and SI-MIS structures. In this measurement, the gate voltage was stepped by −2.5 V starting from 0 V every 20 sec with the dark current being measured 18 sec after each voltage step increase. The Si rich SiO_2 layer was either stepped or graded with R_o defined as $[N_2O]/[SiH_4]$ as an indicator of the Si content of this layer. R_o from 10 (40% atomic Si) to 3 (46% atomic Si) was used with Si content increasing towards the top metal gate electrode when several layers were stacked on top of the underlying 550 Å thick thermal SiO_2 layer (R_o = 10 + 3) or when a graded layer was used (R_o = 10 → 3). The current ledge observed at low voltages is due to trapped space charge build-up in the Si rich SiO_2 injector layer which tends to hold off further current injection until a certain voltage is reached [2].

Fig. 3. Magnitude of the dark current as a function of negative ramped (−.47 V/sec) gate voltage on several SI-MIS structures and their control MIS structures which do not have the Si rich SiO_2 injecting layer present.

Fig. 4. Magnitude of the dark current as a function of negative ramped gate voltage on a SI-MIS structure with a CVD SiO_2 layer deposited on thermal SiO_2 (MLO-2D) for various voltage ramp rates. A virgin as-fabricated location was used for each ramp rate.

Fig. 5. Magnitude of the dark current as a function of negative ramped gate voltage on a SI-MIS structure equivalent to that in Fig. 4 except for the presence of a W trapping layer (MLO-2F) for various voltage ramp rates. A virgin as-fabricated location was used for each ramp rate.

Fig. 6. Quasi-static capacitance ($C = I_{ext}/(dV_g^-/dt)$) as a function of gate voltage on a SI-MIS structure with 230 Å of Si rich SiO_2 (R_o = 3) deposited on 534 Å of thermal SiO_2 (MLO-1P3) compared to a control MIS sample with no Si rich SiO_2 layer present (MLO-1P6).

Fig. 7. Magnitude of the dark current as a function of negative ramped (−.47 V/sec) gate voltage on one SI-MIS structure equivalent to those in Fig. 5 which was cycled four times to consecutively higher voltages through the W trapping ledge. On the return portion of the trace (.47 V/sec), the displacement current $C_I dV_g^-/dt$ changes sign.

Fig. 8. High frequency (1 MHz) capacitance as a function of gate voltage on the same sample as in Fig. 7 before cycling (virgin) and after each cycle shown in Fig. 7.

Fig. 9. Magnitude of the dark current as a function of negative ramped (−.47 V/sec) gate voltage on one SI-MIS structure equivalent to those in Fig. 4 which was cycled four times to consecutively higher voltages through the CVD oxide trapping ledge. On the return portion of the trace (.47 V/sec), the displacement current $C_I dV_g^-/dt$ changes sign.

Fig. 10. High frequency (1MHz) capacitance as a function of gate voltage on the same sample as in Fig. 9 before cycling (virgin) and after each cycle shown in Fig. 9.

Fig. 11. Magnitude of the dark current as a function of negative ramped (−.47 V/sec) gate voltage on one SI-MIS structure with only a thermal SiO_2 layer (MLO-1P4) which was cycled five times to consecutively higher voltages through the thermal oxide trapping ledge. On the return portion of the trace (.47 V/sec), the displacement current $C_I dV_g^-/dt$ changes sign.

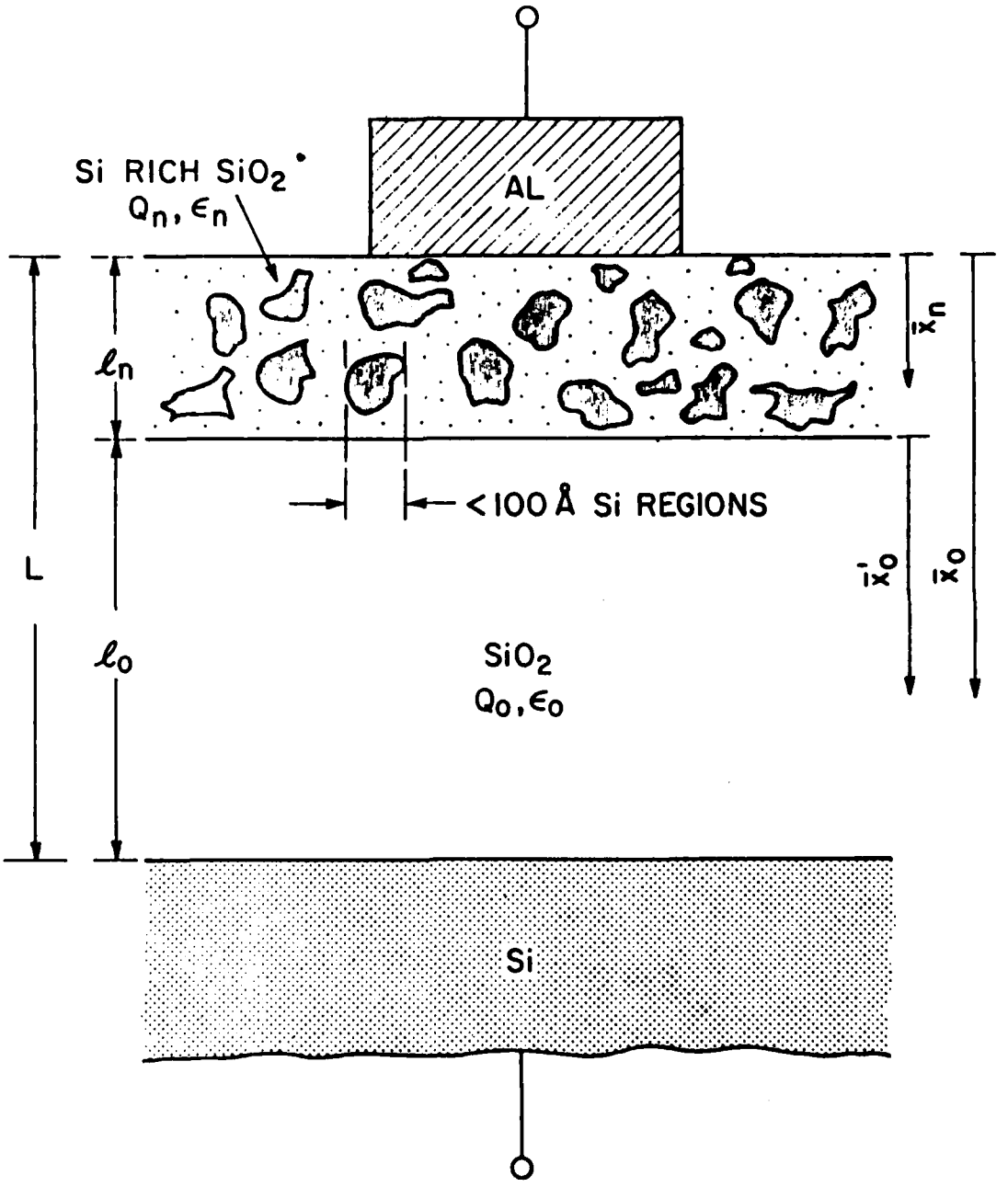
Fig. 12. High frequency (1 MHz) capacitance as a function of gate voltage on the same sample as in Fig. 11 before cycling (virgin) and after each cycle shown in Fig. 11.

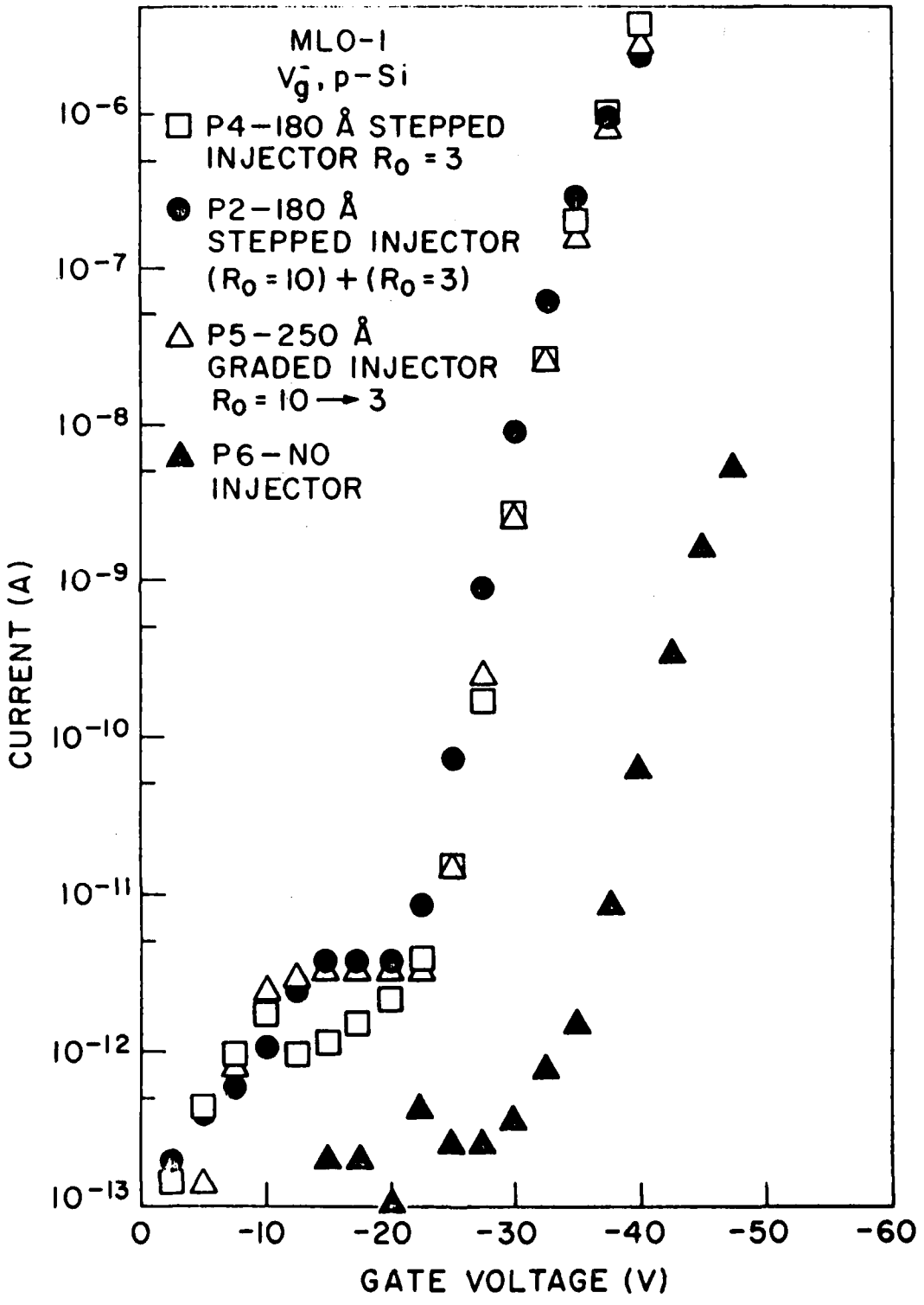
Fig. 13. Numerical simulation as described in the text for the magnitude of the current measured in the external circuit as a function of negative gate voltage for W trapping sites in the SI-MIS structures considered here. The open circles are experimental data for MLO-2F.

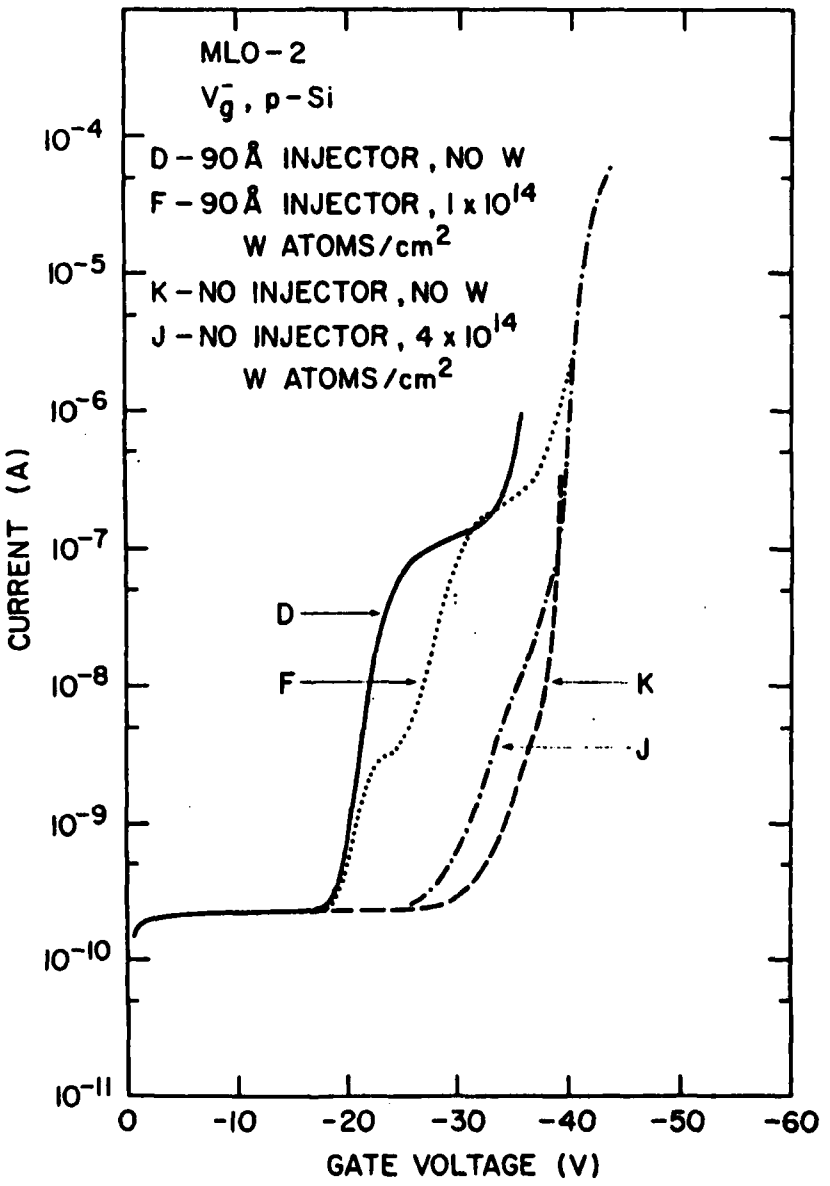
Fig. 14. Numerical simulation as described in text for trapped charge build-up, and the magnitude of the electric field at the Si rich SiO_2–SiO_2 interface as a function of negative gate voltage for W trapping sites in the SI-MIS structures considered here.

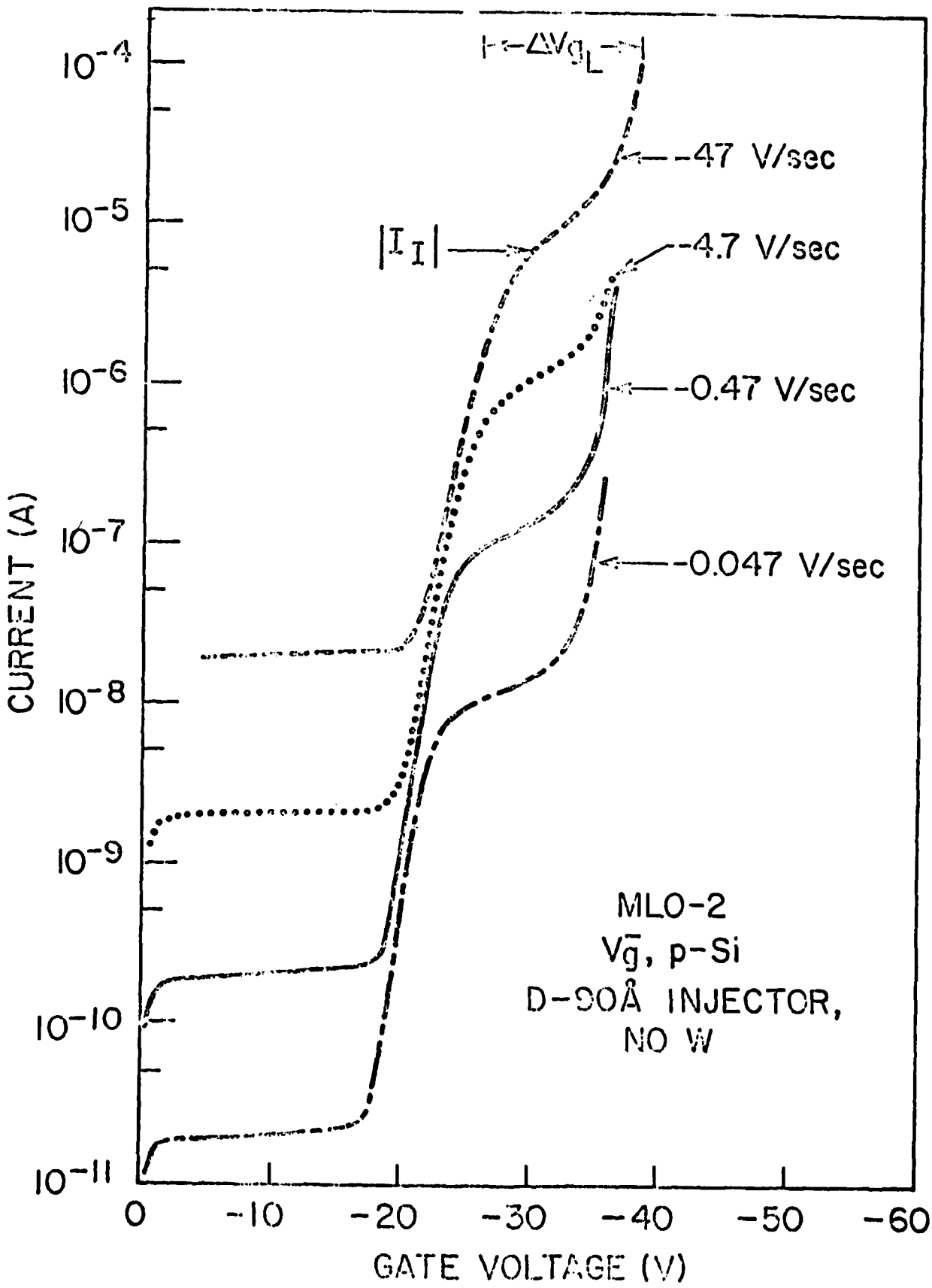
Fig. 15 Numerical simulation as described in the text for the magnitude of the current measured in the external circuit as a function of negative gate voltage for CVD SiO_2 trapping sites in the SI-MIS structures considered here. The open circles are experimental data for MLO-2D.

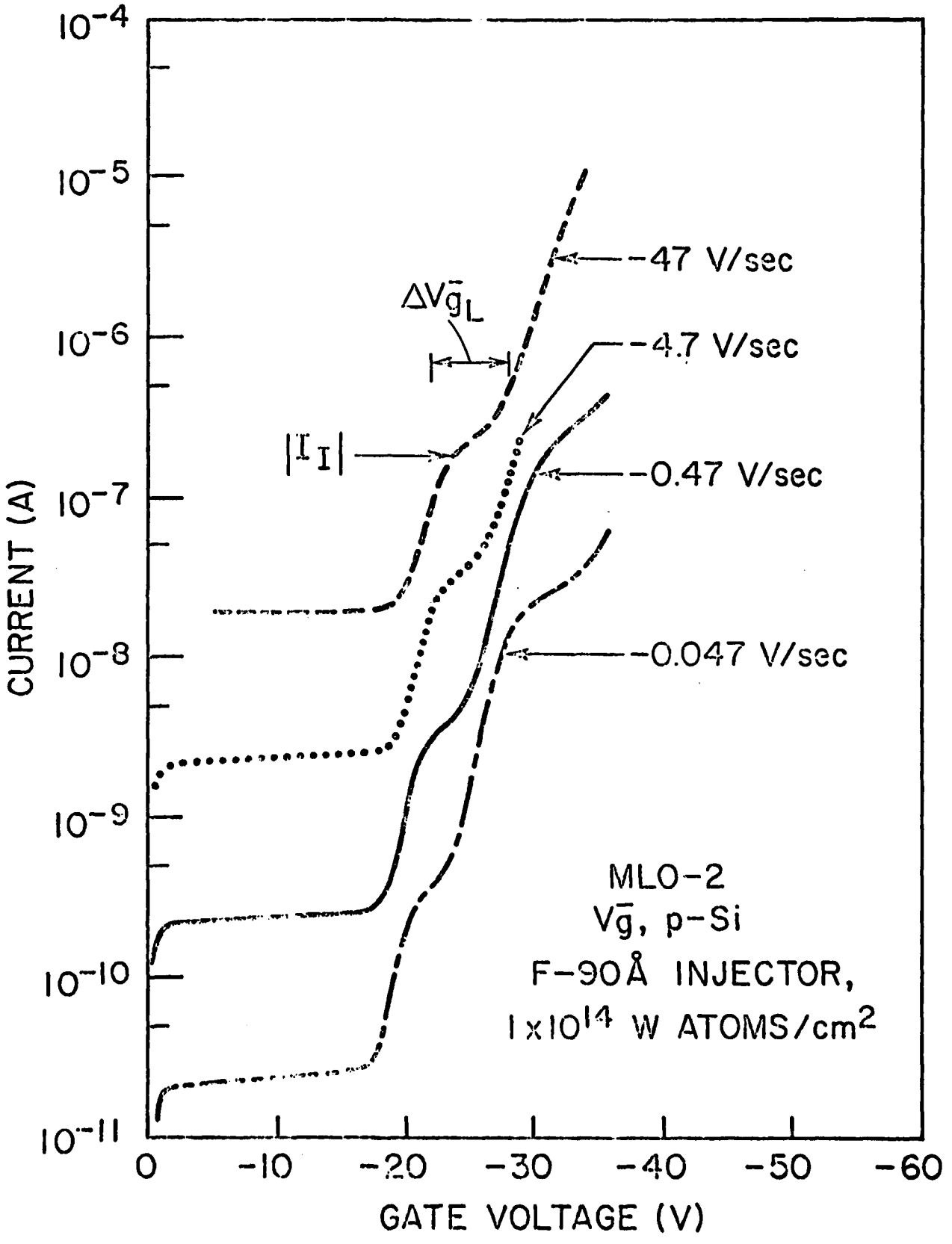
Fig. 16 Numerical simulation as described in the text for the magnitude of the current measured in the external circuit as a function of negative gate voltage for thermal SiO_2 trapping sites in the SI-MIS structures considered here. The open circles are experimental data for MLO-1P4.

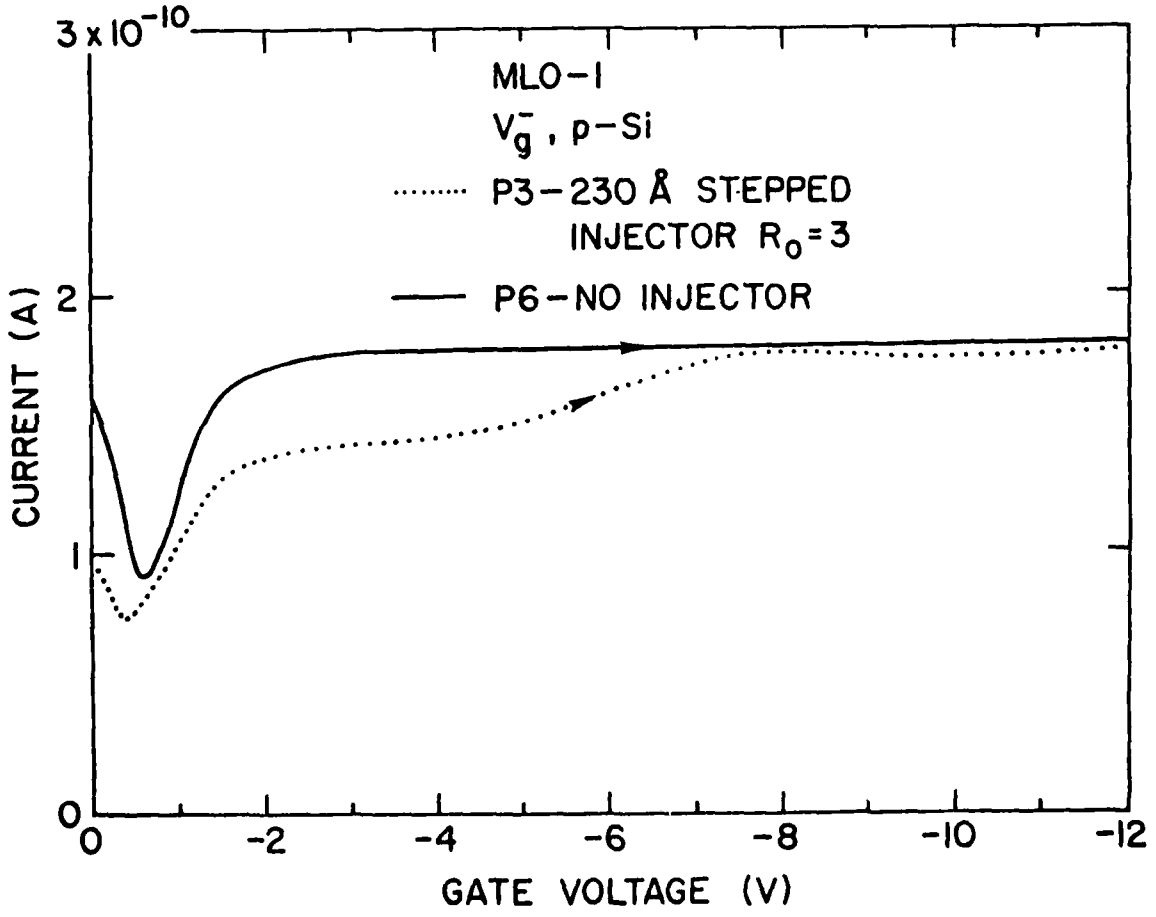

Si RICH SiO_2
Q_n, ϵ_n
AL
ℓ_n
$\bar{x}_n$
< 100 Å Si REGIONS
L
$\bar{x}_0$
$\bar{x}_0$
ℓ_0
SiO_2
Q_0, ϵ_0
Si

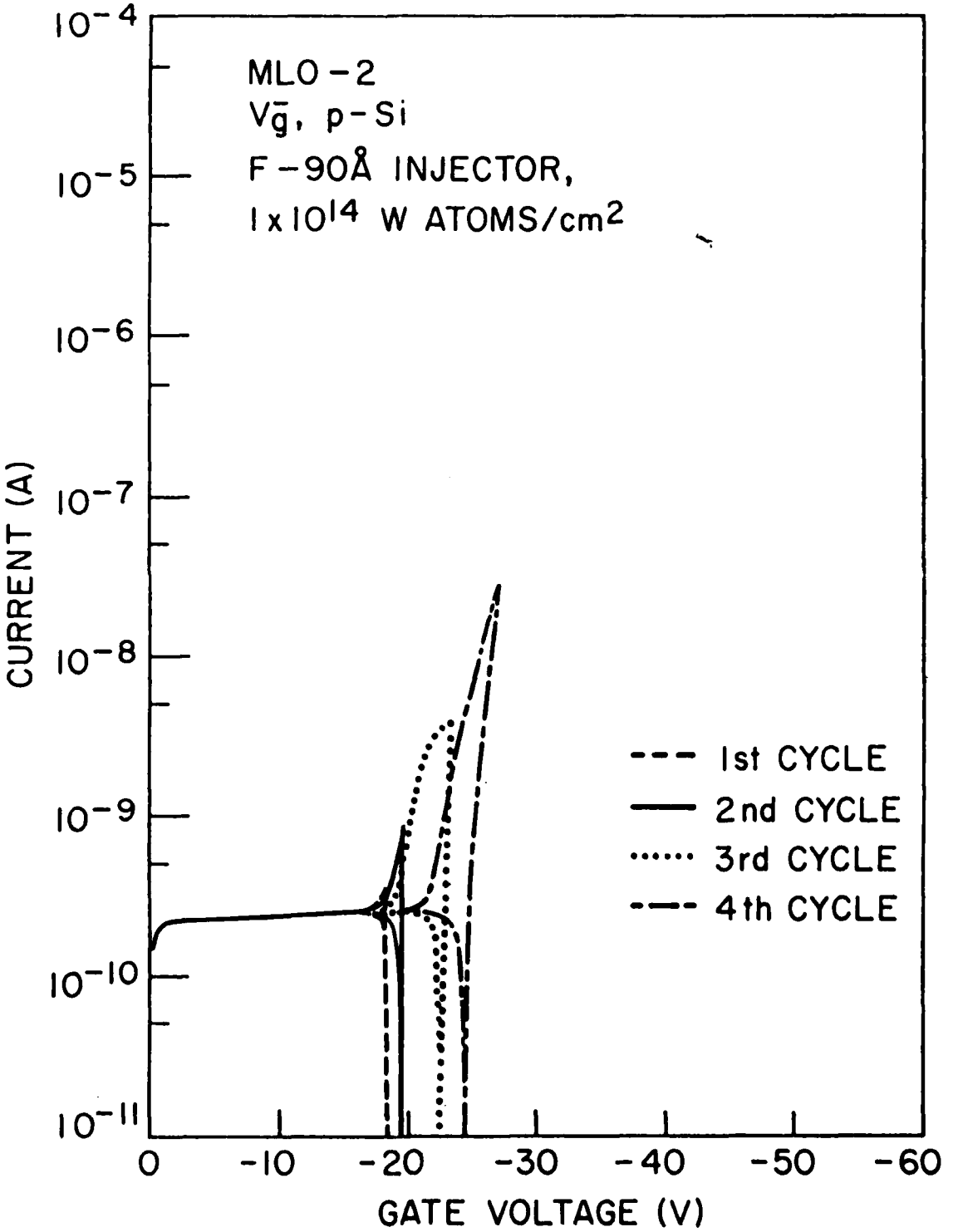

MLO-1
V_g^-, p-Si
P4-180 Å STEPPED INJECTOR $R_0 = 3$
P2-180 Å STEPPED INJECTOR $(R_0 = 10) + (R_0 = 3)$
P5-250 Å GRADED INJECTOR $R_0 = 10 \rightarrow 3$
P6-NO INJECTOR
CURRENT (A)
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
0
-10
-20
-30
-40
-50
-60
GATE VOLTAGE (V)

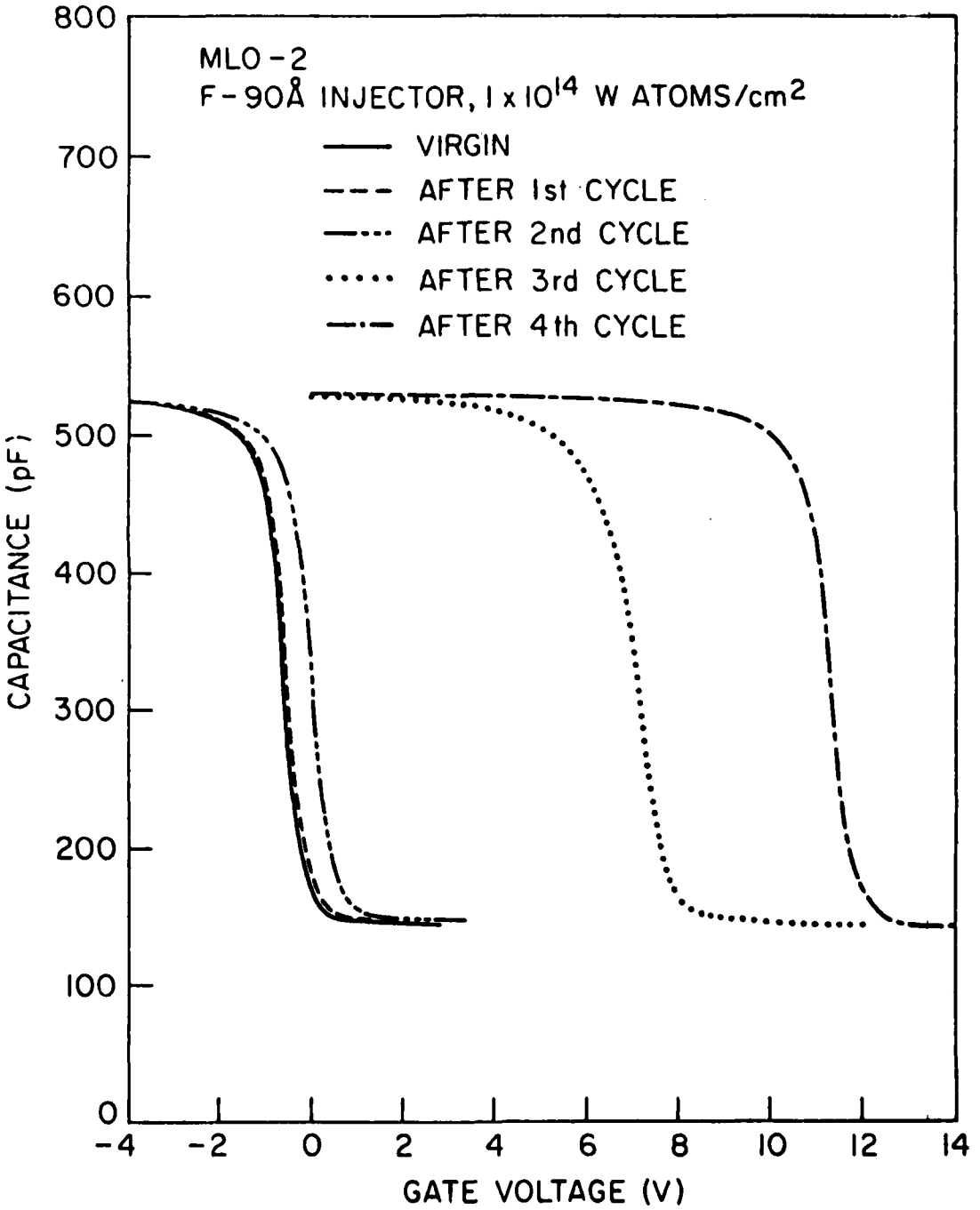

MLO-2
V_g^-, p-Si
D - 90 Å INJECTOR, NO W
F - 90 Å INJECTOR, 1 x 10^{14} W ATOMS/cm^2
K - NO INJECTOR, NO W
J - NO INJECTOR, 4 x 10^{14} W ATOMS/cm^2
CURRENT (A)
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
D
F
K
J
0
-10
-20
-30
-40
-50
-60
GATE VOLTAGE (V)

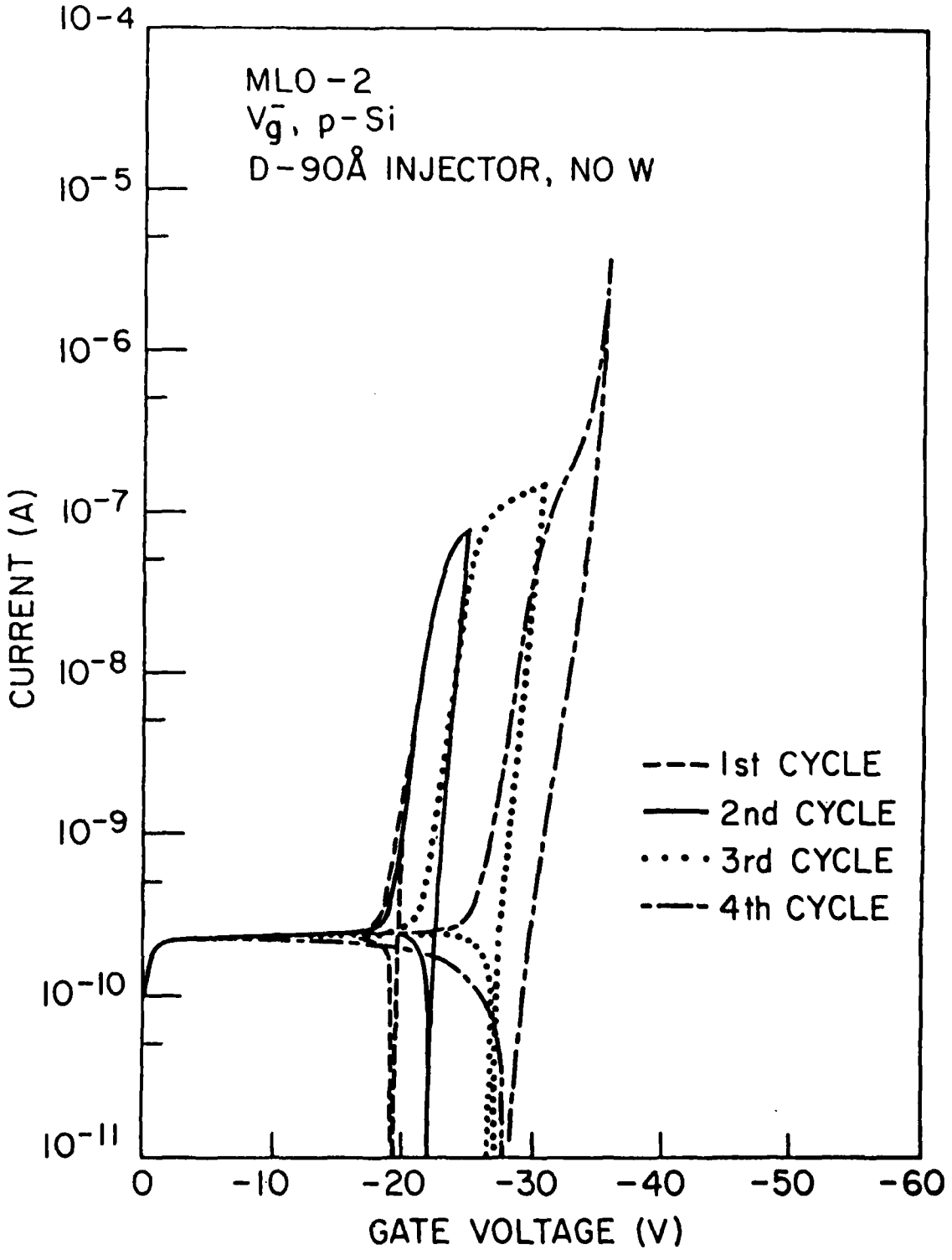

10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
CURRENT (A)
$\leftarrow\Delta V_{g_L}\rightarrow$
-47 V/sec
$|I_I|$
-4.7 V/sec
-0.47 V/sec
-0.047 V/sec
MLO-2
$V_{\bar{g}}$, p-Si
D-90Å INJECTOR,
NO W
0
-10
-20
-30
-40
-50
-60
GATE VOLTAGE (V)

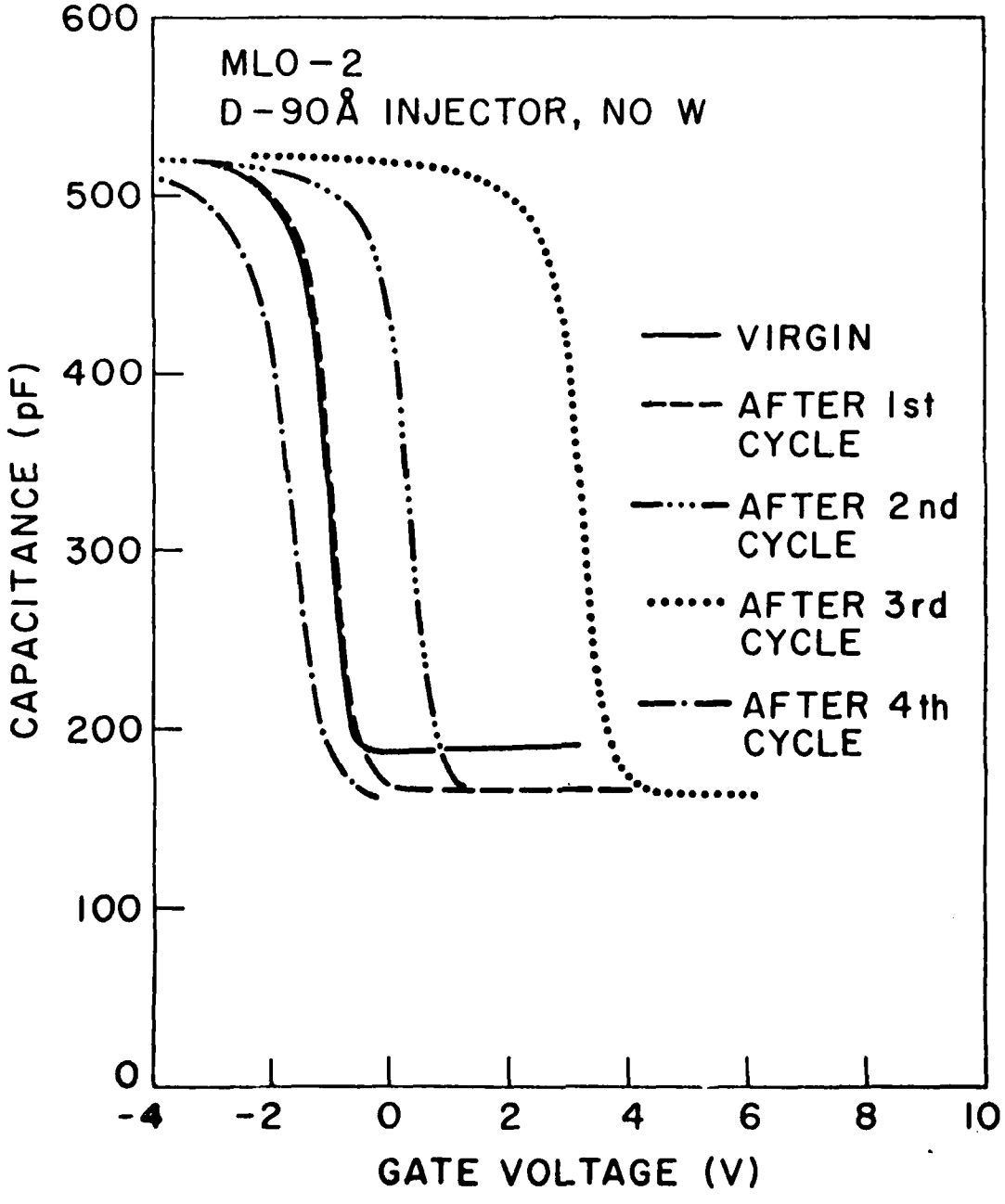

10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
CURRENT (A)
$\Delta V\bar{g}_L$
$|I_I|$
-47 V/sec
-4.7 V/sec
-0.47 V/sec
-0.047 V/sec
MLO-2
$V\bar{g}$, p-Si
F-90Å INJECTOR,
1×10^{14} W ATOMS/cm^2
0
-10
-20
-30
-40
-50
-60
GATE VOLTAGE (V)

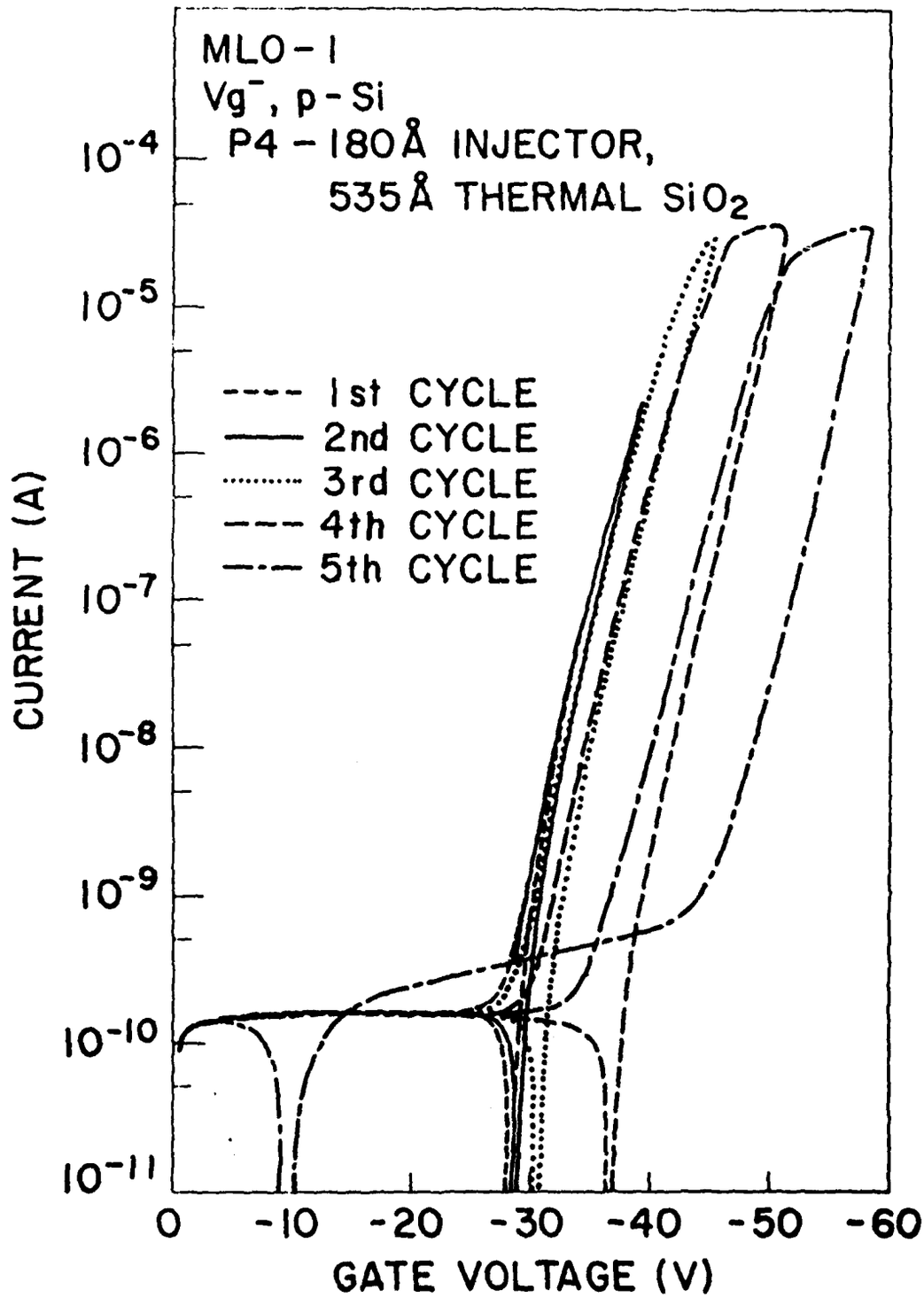

3 x 10^-10
2
1
0
CURRENT (A)
MLO-1
V_g^-, p-Si
P3-230 Å STEPPED INJECTOR R_0=3
P6-NO INJECTOR
0
-2
-4
-6
-8
-10
-12
GATE VOLTAGE (V)

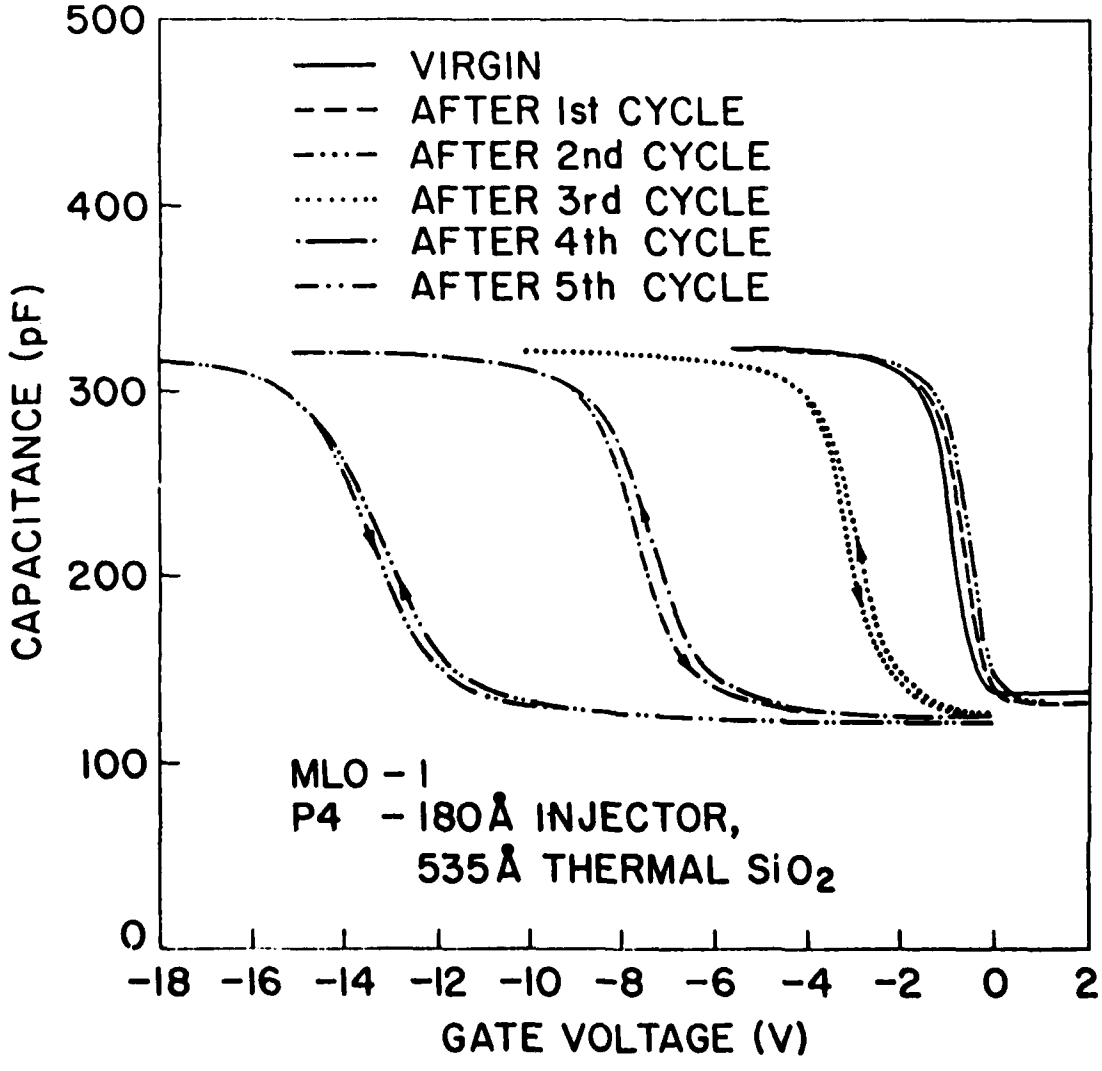

MLO-2
Vg, p-Si
F-90Å INJECTOR,
1x10^14 W ATOMS/cm^2
CURRENT (A)
10^-4
10^-5
10^-6
10^-7
10^-8
10^-9
10^-10
10^-11
0
-10
-20
-30
-40
-50
-60
GATE VOLTAGE (V)
1st CYCLE
2nd CYCLE
3rd CYCLE
4th CYCLE

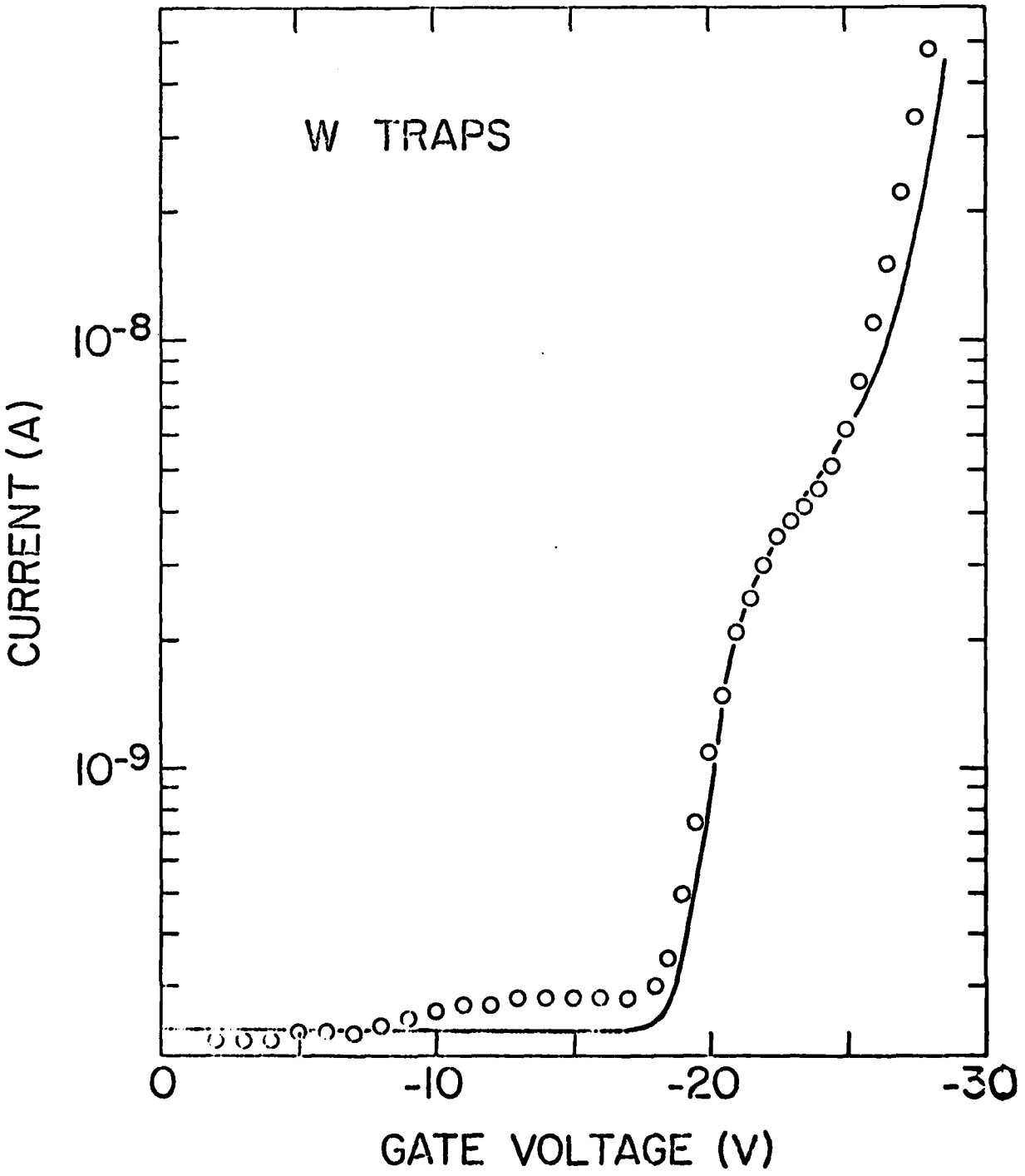

MLO-2
F-90Å INJECTOR, 1 x 10^14 W ATOMS/cm^2
VIRGIN
AFTER 1st CYCLE
AFTER 2nd CYCLE
AFTER 3rd CYCLE
AFTER 4th CYCLE
CAPACITANCE (pF)
800
700
600
500
400
300
200
100
0
-4
-2
0
2
4
6
8
10
12
14
GATE VOLTAGE (V)

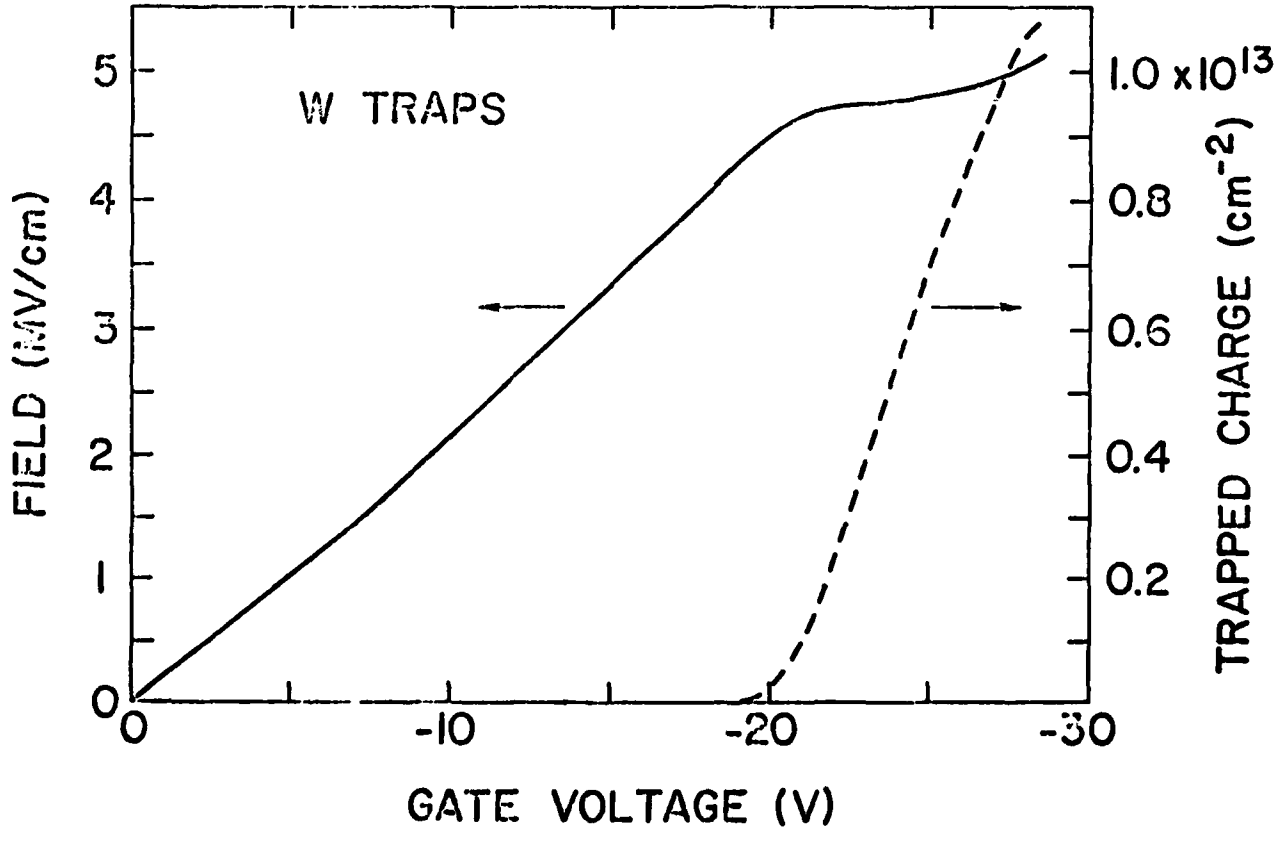

MLO-2
V_g^-, p-Si
D-90Å INJECTOR, NO W
CURRENT (A)
10-4
10-5
10-6
10-7
10-8
10-9
10-10
10-11
0
-10
-20
-30
-40
-50
-60
GATE VOLTAGE (V)
1st CYCLE
2nd CYCLE
3rd CYCLE
4th CYCLE

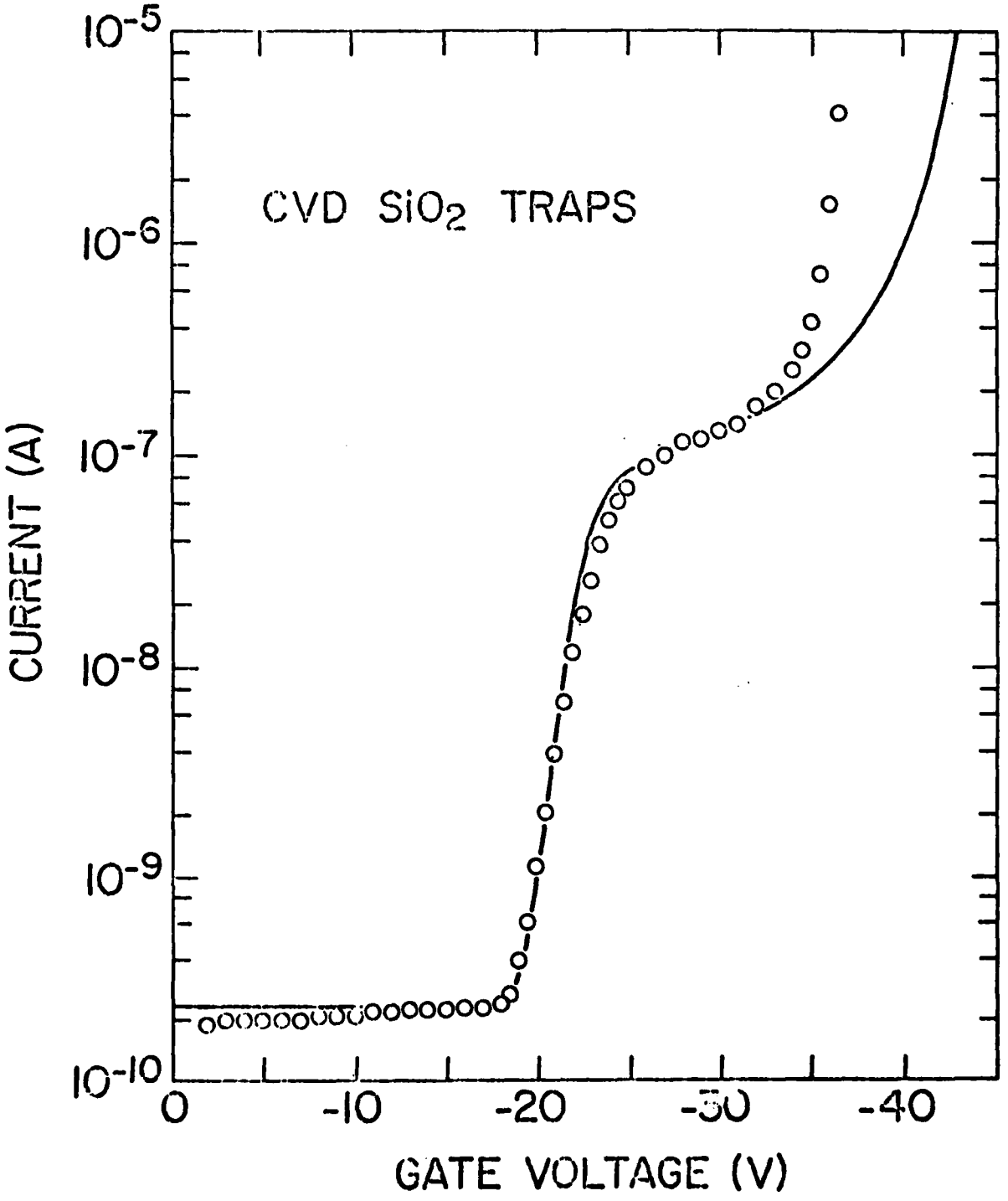

MLO-2
D-90Å INJECTOR, NO W
VIRGIN
AFTER 1st CYCLE
AFTER 2nd CYCLE
AFTER 3rd CYCLE
AFTER 4th CYCLE
CAPACITANCE (pF)
600
500
400
300
200
100
0
-4
-2
0
2
4
6
8
10
GATE VOLTAGE (V)

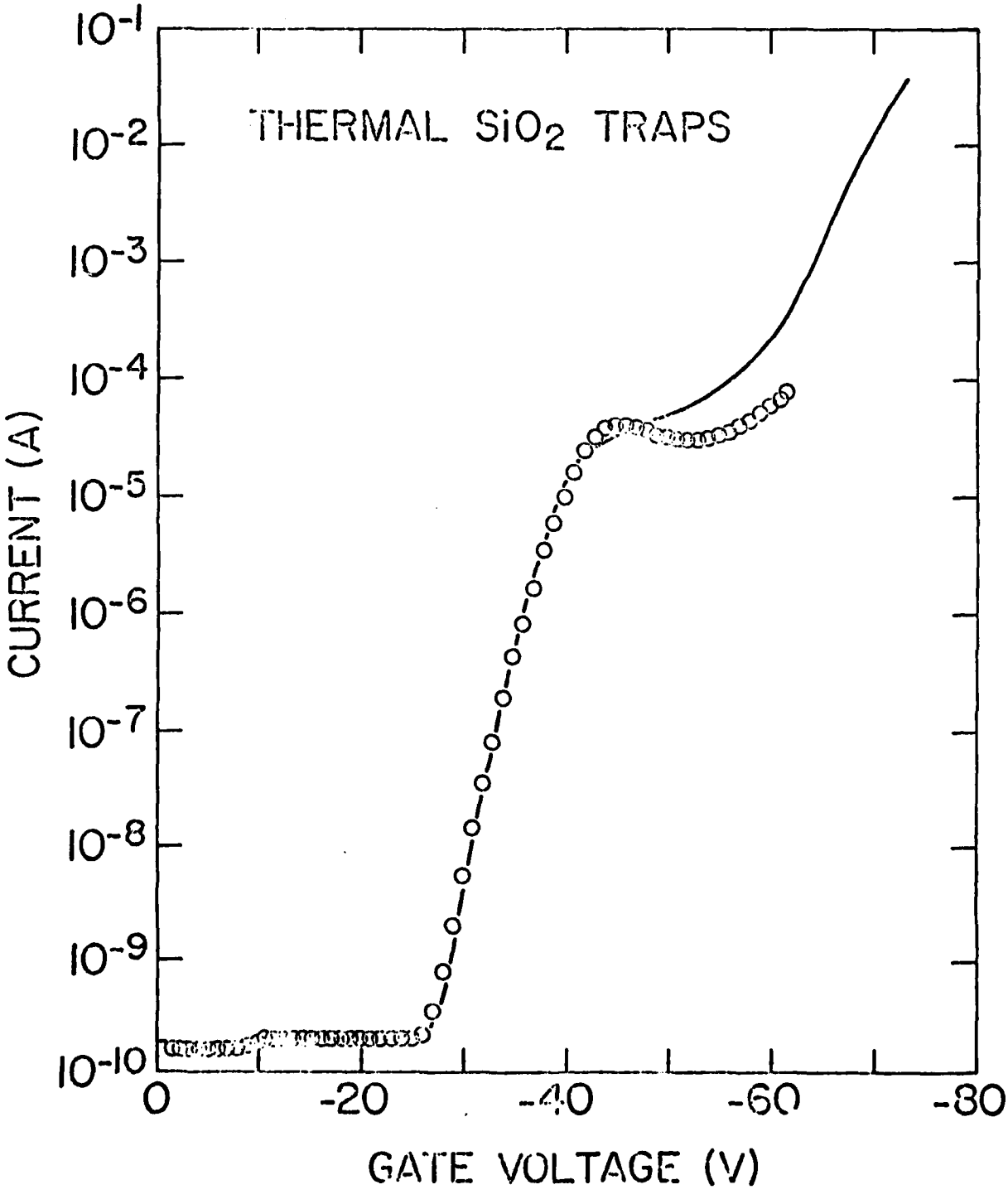

MLO-1
Vg⁻, p-Si
P4 – 180Å INJECTOR,
535Å THERMAL SiO2
1st CYCLE
2nd CYCLE
3rd CYCLE
4th CYCLE
5th CYCLE
CURRENT (A)
10-4
10-5
10-6
10-7
10-8
10-9
10-10
10-11
0
-10
-20
-30
-40
-50
-60
GATE VOLTAGE (V)


VIRGIN
AFTER 1st CYCLE
AFTER 2nd CYCLE
AFTER 3rd CYCLE
AFTER 4th CYCLE
AFTER 5th CYCLE
MLO - 1
P4 - 180Å INJECTOR,
535Å THERMAL SiO2
CAPACITANCE (pF)
500
400
300
200
100
0
-18 -16 -14 -12 -10 -8 -6 -4 -2 0 2
GATE VOLTAGE (V)


W TRAPS
CURRENT (A)
10-8
10-9
0
-10
-20
-30
GATE VOLTAGE (V)


W TRAPS
FIELD (MV/cm)
TRAPPED CHARGE (cm^{-2})
GATE VOLTAGE (V)
0
1
2
3
4
5
0.2
0.4
0.6
0.8
1.0 x10^{13}
-10
-20
-30


CVD SiO2 TRAPS
CURRENT (A)
10-5
10-6
10-7
10-8
10-9
10-10
0
-10
-20
-30
-40
GATE VOLTAGE (V)


THERMAL SiO_2 TRAPS
CURRENT (A)
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
0
-20
-40
-60
-80
GATE VOLTAGE (V)

RADIATION DAMAGE IN SiO_2

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ABSTRACT

This paper describes the electrical effects in SiO_2 layers exposed to ionizing radiation. These SiO_2 layers are formed on Si substrates at high temperatures (1000°C) to a thickness of 500 to 1500 Å. Radiation is shown to cause a build up of positive charge at the Si – SiO_2 interface and in addition, the formation of electron and hole traps in the bulk of the SiO_2. The effect of annealing treatments is described. The spatial location of the positive charge and the bulk traps is determined using the photo I-V technique. There is also a brief discussion of the effects on devices resulting from exposure to radiation.

I. INTRODUCTION

This paper will discuss radiation effects in SiO_2 formed by the thermal oxidation of silicon at a relatively high temperature (1000°C). These SiO_2 layers are typically 500 to 1000 Å thick and can be made with high purity and accurately controllable thicknesses. This technology has been developed by the semiconductor industry which uses them as the insulator above silicon in the active gate region of MOS transistors. As a result of radiation applied to MOS transistors, charge can build up in the SiO_2 which changes the device characteristics.

There are two concerns with respect to radiation:

A. Devices that are used in a radiation environment.

B. The effect of radiation applied during the construction of the device.

In the latter case, annealing treatments can be used which eliminate some but not all of the damage that has occurred.

The major effect of radiation applied to MOS devices is to form a positive charge at the Si – SiO_2 interface [1,2]. This radiation can be X-rays, electrons, or vacuum ultra-violet photons, whose energy exceeds the band gap in SiO_2. The positive charge results from holes transported to the interface where they are trapped. The trapping probability (ratio of the number of trapped carriers to the number of injected carriers) for holes is 10–40% depending on the processing conditions for the SiO_2. Electrons have a very low trapping probability in SiO_2 (10^{-5} to 10^{-6}) and therefore migrate to either the Si substrate or the metal gate. Many of the holes recombine with the electrons in the SiO_2 unless a large electric field is applied during the radiation.

During the operation of N channel MOSFETs there is a small but important electron current through the SiO_2. One source of this is due to the electrons flowing in the channel between the source and drain. A small percentage of these electrons acquire sufficient energy from the field to overcome the barrier of 3.1 eV at the Si – SiO_2 interface and flow into the oxide. This is shown schematically in Fig. 1. Contemporary MOSFET technology uses a reduced source to drain distance and therefore the channel electrons lose less energy in the silicon which results in more of them being injected into the SiO_2. As a result electron trapping in SiO_2 becomes more important as the source to drain spacing is decreased. The low trapping probability of a normal oxide makes the devices tolerant to this effect; however, it has been observed that neutral traps are formed in the SiO_2 by radiation [3] as well as positive

charges. This reduces the number of electrons that can flow before trapped oxide charge develops that would change the device characteristics. The effect of the traps induced by radiation is to degrade the useful lifetime of the device. Since practical limits exist for annealing this damage in MOSFETs, residual traps will be present in devices fabricated by techniques involving ionizing radiation during the latter stages of processing. This paper will discuss both the positive charge effect and the neutral trap effect. D.J. DiMaria [4] has written a comprehensive review of electron and hole trapping in SiO_2 in a recent paper that can be referred to by the reader.

II. MEASUREMENT TECHNIQUES

A. Charge Measurement

Three methods are used for measuring the charge in the SiO_2 film:

(*i*) Device measurements such as the threshold voltage of MOSFET's.

(*ii*) C-V measurements.

(*iii*) Photo I-V measurements.

Techniques (*ii*) and (*iii*) use simple MOS capacitors as compared to the relatively complex device structures required for (*i*) and as a result, (*ii*) and (*iii*) are frequently used for basic studies. The C-V technique is illustrated in Fig. 2. The important consideration is that the flat band voltage shift (ΔV_{FB}) is determined by the total trapped charge (Q) and χ. Unless χ is known, Q can not be determined. The photo I-V technique developed by DiMaria [5], consists of the application of light with an energy greater than the Si – SiO_2 or the Gate Metal – SiO_2 barrier energy, and requires a measurement of I *vs.* V as shown in Fig. 3. This technique requires the use of a semitransparent gate electrode. The current for positive gate voltages is controlled by the emission of electrons from the silicon and for negative gate voltages by emission of electrons from the gate. The electric field in the oxide near the relevant interface controls the emission from that interface. The presence of negative charge in the oxide induces a repulsive field which must be overcome by the applied field before emission from that interface can occur. This results in a displacement of the I-V curve along the voltage axis with the displacement being a measure of the field due to the oxide charge. This displacement can be measured for positive and negative gate voltages. Since there are only two unknowns, Q and χ can be calculated. Both methods (*ii*) and (*iii*) are used extensively in our work. The C-V method depends on the field in the silicon and the photo I-V

method on the field in the SiO_2. The results of these methods will be different if charge is at or very close to the Si – SiO_2 interface. This difference can be used as a measure of charge at that interface.

B. Charge Injection

The study of traps requires the injection of charge into the SiO_2. This can be done by various means and three methods have been used extensively in our laboratory:

(*i*) Optical generation of minority carriers in Si that are accelerated by the field in the depletion region under the channel of a MOSFET. This technique was developed by Ning and Yu [6].

(*ii*) Injection of carriers using internal photoemission. This technique is illustrated in Fig 3 and was first suggested by Williams [7].

(*iii*) The use of avalanche injection was first described in a paper by Nicollian, Goetzberger, and Berglund [8] and is illustrated in Fig. 4. Sufficient electric field is applied to the silicon (in depletion) to create an avalanche breakdown. This technique requires the application of an r.f. voltage waveform to the MOS capacitor. The shape of the waveform is critical if the apparatus is used for hole injection as well as electron injection. The type of waveform required for hole injection is a saw tooth.

The first technique (*i*) requires the use of a MOSFET structure. The other techniques can be used with MOS capacitors. Internal photoemission is useful for studying traps with a relatively large cross section which require a small electron current flow through the SiO_2. Small cross section traps require a larger current which can be obtained using avalanche injection.

C. System Design

Electronic systems have been designed to enable us to make the measurements, store the data in a computer and analyze the results. The analysis of the results is described in the references included [3,5,6].

III. POSITIVE CHARGE EFFECTS

The first order result of the application of radiation, with an energy greater than the band gap of SiO_2, is to produce a positive charge at the Si – SiO_2 interface as observed by Snow, Grove and Fitzgerald [1] and by Mitchell and Wilson [2]. The positive charge is due to holes migrating through the SiO_2 and being trapped at the Si – SiO_2 interface. Fig. 5 shows schematic drawings of the positive charge build up due to radiation. In the absence of an applied electric field, many of these holes recombine with the electrons before they reach the interface; however, if a field is applied they can migrate to the interface where 10-50% of them are trapped.

Extensive studies have been carried out by Aubuchon [9] on the dependence of the threshold voltage shift of MOS transistors, in response to radiation, on the processing conditions. His work was concerned with p-channel transistors which use a negative gate bias. This bias would be expected to attract most of the holes to the gate – SiO_2 interface and not to the Si – SiO_2 interface. Therefore, the effects he studied can be expected to be smaller than what we would expect for n-channel transistors. He observed a significant improvement in the radiation hardness of his devices if the SiO_2 is annealed at 800°C after the SiO_2 is grown, but the radiation hardness degrades if higher annealing temperatures are used. It is reasonable to assume that these results were due to a variation in the hole trapping probability as a result of the processing conditions he used. Other studies of the effect of processing conditions have been carried out by Aitken and Young [10], by Eer Nisse and Derbenwick [11], and by Derbenwick and Gregory [12].

The location of the positive charge has been studied by DiMaria, Weinberg and Aitken [13] with the conclusion that it is within 50 Å of the Si – SiO_2 interface. After holes are trapped at the interface, electron flow can be induced (using avalanche injection) and the annihilation of the holes observed. The electron trapping cross sections for these positively charged traps (holes) has been measured to be 3×10^{-13} cm^2 at low fields ($\approx$ 1 MV/cm) by Aitken and Young [14] and has been shown to be strongly field dependent [4,13].

The positive charge can be eliminated (in the case of Al gate devices) by thermal treatments at temperatures less than 400°C as described in the work of Harari and Royce [15] and by the work of Zaininger [16]. Temperatures required to anneal the positive charge are higher if Si gates are used instead of Al gates as shown in Fig. 6, based on the work of Aitken [17]. Annealing temperatures are limited to ~ 400°C with Al gates due to Al – SiO_2 reaction; however, with Si gates higher temperatures can be used but are eventually limited by

Al – Si relations in MOSFETs. It is interesting to note that Al plays a beneficial role even though the Al is not in direct contact with the SiO_2. Annealing treatments can be used if the radiation exposure occurs during device processing but can not be used if the device is operating in a radiation environment. Hole trapping at the Si – SiO_2 interface can also be studied using avalanche injection from the Si [18-20].

Powell [21] has used VUV to generate holes in the SiO_2 and a positive gate bias to transport them to the Si – SiO_2 interface. The field enhancement due to the holes was sufficient to induce electron emission from the Si into the SiO_2.

Another type of positive charge can be generated in the vicinity of the Si – SiO_2 interface by the application of VUV with negative bias shown by the work of Weinberg and Rubloff [22]. Similar effects have been observed by the passage of electron currents, using avalanche injection, through the SiO_2 for prolonged periods of time [23,24]. This charge results from the generation of donor states in the SiO_2 that can be charged and discharged by the application of electric fields [24]. Recent work by Weinberg, Young, DiMaria, and Rubloff [25] has shown that exposure of the sample to H_2O enhances this effect and it has been suggested that these states are due to either excitons or atomic hydrogen diffusing to the Si – SiO_2 interface [25].

IV. NEUTRAL TRAPS

In addition to the positive interfacial charge, neutral electron traps are generated in the SiO_2 as observed by Aitken and Young [26]. The electron trapping cross sections have been measured to cover the range of 10^{-15} to 10^{-18} cm^2. The spatial location of these traps has been discussed in the paper by DiMaria, Ephrath, and Young [27] for radiation that penetrates through the SiO_2 (25 keV electrons and SiO_2 thicknesses of 525 Å and 1095 Å). The samples were exposed to the 25 keV electrons and subsequently the traps were charged using avalanche injection. The voltage shifts were measured in Fig. 7(a) by the C-V method, and in Figs. 7(b) and 7(c) the voltage shifts were measured by photo I-V for negative and positive gate voltages, respectively. These shifts are essentially equal, with the centroid of the trapped charge in the middle of the SiO_2, indicative of a uniform trap density in the SiO_2. If the radiation does not penetrate the SiO_2, we would expect the spatial distribution of the traps would correspond to that of the radiation. These neutral traps have also been generated by X-ray exposure and by the radiation coming from a gas plasma [27].

Aitken [17] used MOSFET structures to study the effect of annealing treatments after radiation exposure. Results of threshold voltage measurements are given in Fig. 8. These structures had poly-Si gates. The initial rise is due to the annihilation of the trapped holes by the electrons and the subsequent rise is due to the neutral traps. The trapped holes are not removed by the 400°C anneal since these devices use poly-Si gates. A temperature of 550°C is not sufficient to remove all the damage.

Recent work by DeKeersmaecker and Aitken has shown an enhanced trapping of holes in SiO_2 that has been exposed to radiation. These hole traps are in the bulk of the SiO_2. Aitken [3] has suggested that the neutral traps are due to broken bonds in the SiO_2 tetrahedra similar to a model proposed by Eer Nisse and Norris [30] to explain their stress measurements on SiO_2 samples exposed to radiation. Aitken has also described these neutral traps as dipole-like radiation defects. It is reasonable to assume that these dipole-like defects can act as both electron and hole traps.

V. ATOMIC DISPLACEMENT DAMAGE

The types of radiation discussed up to this point can not cause atomic displacements. Ion implantation can induce atomic displacements which increase the trapping rate [31,32]. In Fig. 9 the effect of heat treatment on the trapping rate is shown for a sample that had been implanted with Al. It is seen that temperatures of ~ 1000°C are required to eliminate the damage.

VI. CONCLUSIONS

Positive charge at the Si – SiO_2 interface and neutral electron – hole traps in the bulk of the SiO_2 are generated by ionizing radiation. The positive charge effect is the most important consideration for MOSFET devices that must operate in a radiation environment, and this charge results in a shift of the device characteristics along the gate voltage axis. The positive charges and neutral traps can lead to an enhanced drift in device characteristics with time if the device is operated under conditions that provide an injected current into the SiO_2. The radiation providing these effects can also arise from processes encountered in the construction of the device. In this case, annealing treatments can be used. The annealing of the trapped holes can be accomplished at a lower temperature if the devices use Al gates (400°C) than if the devices use Si gates (600°C). The annealing of the neutral traps also requires temperatures of ~ 600°C which can not be done with Al electrodes in place. Reference is

made to a model proposed by Aitken of a dipole-like defect that explains the electron and hole trapping properties of the neutral traps. Atomic displacement damage created by ion implantation requires a temperature of 1000°C for annealing.

ACKNOWLEDGEMENTS

The author is indebted to D.J. DiMaria, J.M. Aitken, Z. Weinberg and R.F. DeKeersmaecker for many discussions and who have done much of the work reported here. This paper has been carefully reviewed by D.J. DiMaria, M.I. Nathan, and J.M. Aitken. Technical assistance has been rendered by J.A. Calise and F.L. Pesavento. Samples have been prepared by the I.B.M. Yorktown Si Process Facility and the work has been supported in part by the Defense Advanced Research Agency (RADC) and monitored by the Deputy for Electronic Technology, under Contract No. F-19628-78-C-0225.

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FIGURE CAPTIONS

Figure 1. Cross section of n-channel MOSFET showing "hot electron injection".

Figure 2. C-V charge measurement technique. The flat band voltage shift is ΔV_{FB}, $\bar{x}$ is the charge centroid measured with respect to the gate electrode, ε is the dielectric permitivity of SiO_2 and Q is the total trapped charge in the SiO_2 per unit area.

Figure 3. Photo I-V technique for measurement of charge (Q) and charge centroid $\bar{x}$.

Figure 4. Avalanche injection.

Figure 5. Schematic drawing showing positive charge build up as a result of positive gate bias (Fig. 5a) and negative gate bias (Fig. 5b).

Figure 6. Annealing of positive charge as a function of temperature as a function of time with Al Gates, Si Gates and gates with Al on top of the Si. The radiation used to generate the holes was electrons with a charge of 10^{-4} coul/cm^2 at 25 keV.

Figure 7. Neutral traps charged by avalanche injection. The C-V voltage shift resulting from this charging is shown in Fig. 7(a) and the photo I-V voltage shifts shown in Figs. 7(b) and (c) for negative and positive gate voltages, respectively.

Figure 8. Shift in threshold voltage in optically defined, irradiated poly-silicon MOSFET's as a function of the number of electrons injected per square centimeter of gate area with anneal history as a parameter. The MOSFET's were annealed for 30 min at each of the temperatures shown on the figure. Trapping in an unirradiated control device is shown for comparison.

Figure 9. Flat band voltage vs. time with avalanche injection. This sample had been implanted with Al and the effect of subsequent heat treatments is shown.

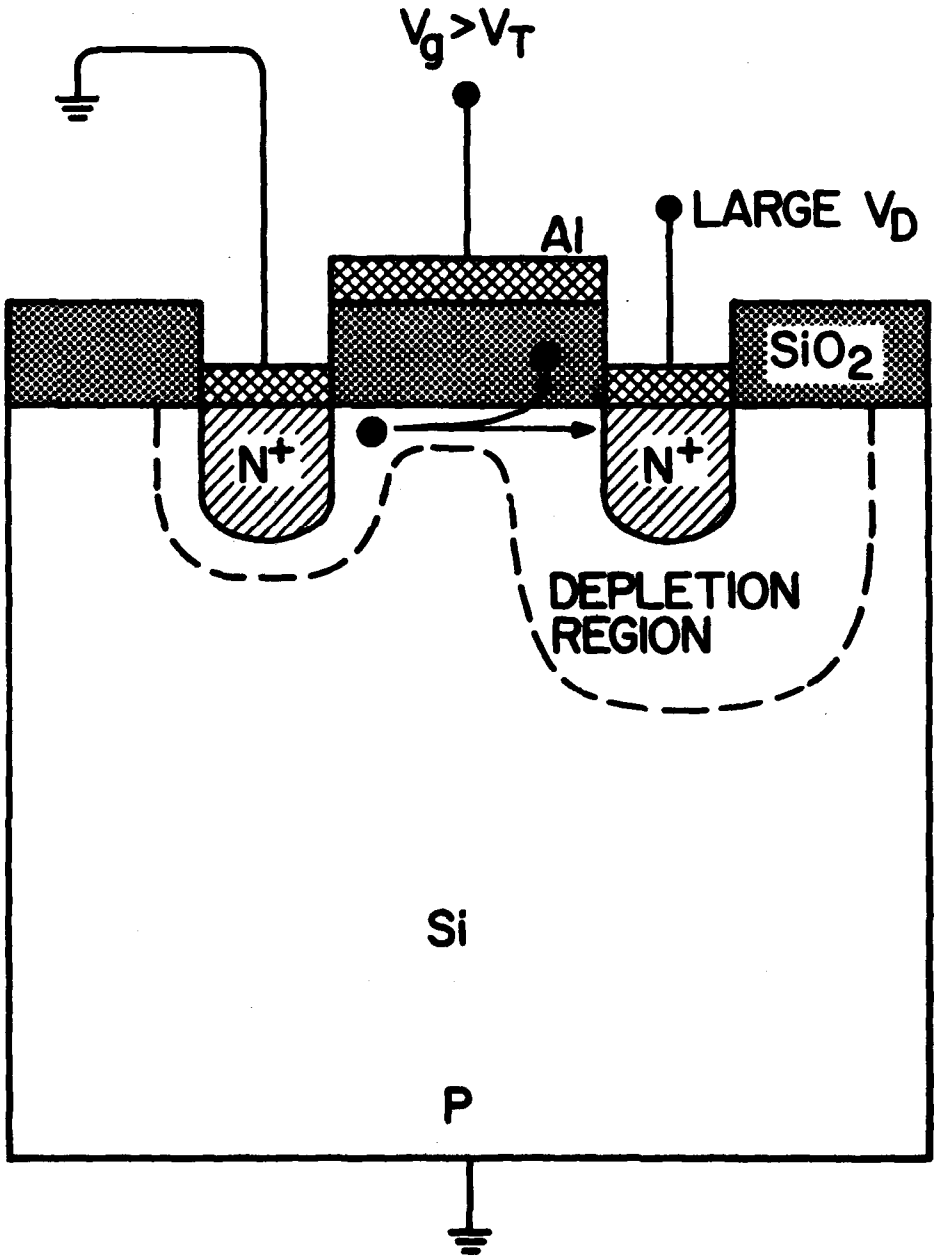
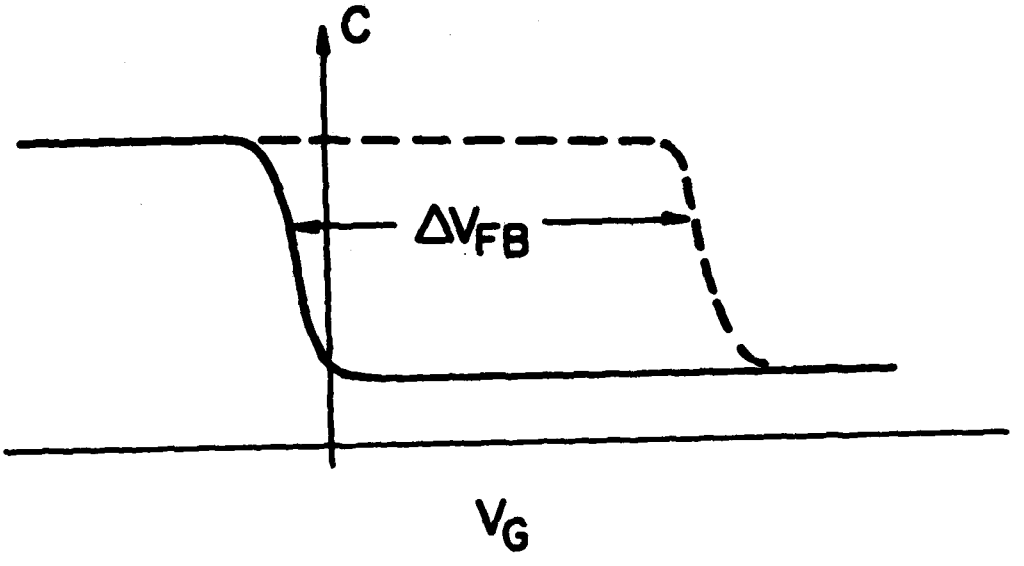


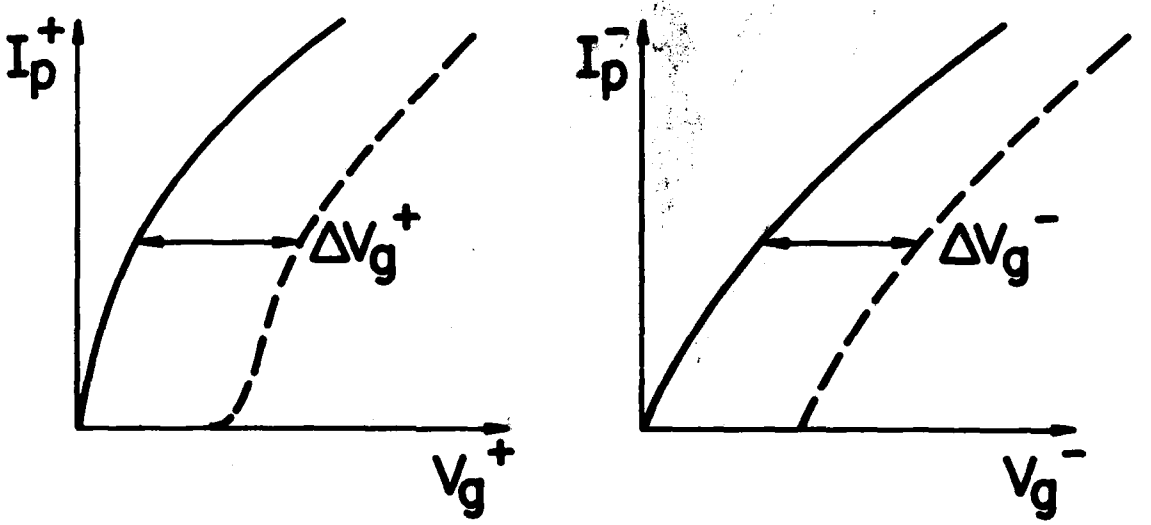
FIGURE 1



$$\text{FLAT-BAND VOLTAGE SHIFT} = \Delta V_{FB} = -\frac{\bar{x}}{\epsilon} Q$$

FIGURE 2

PHOTOCURRENT-VOLTAGE (PHOTO I-V)

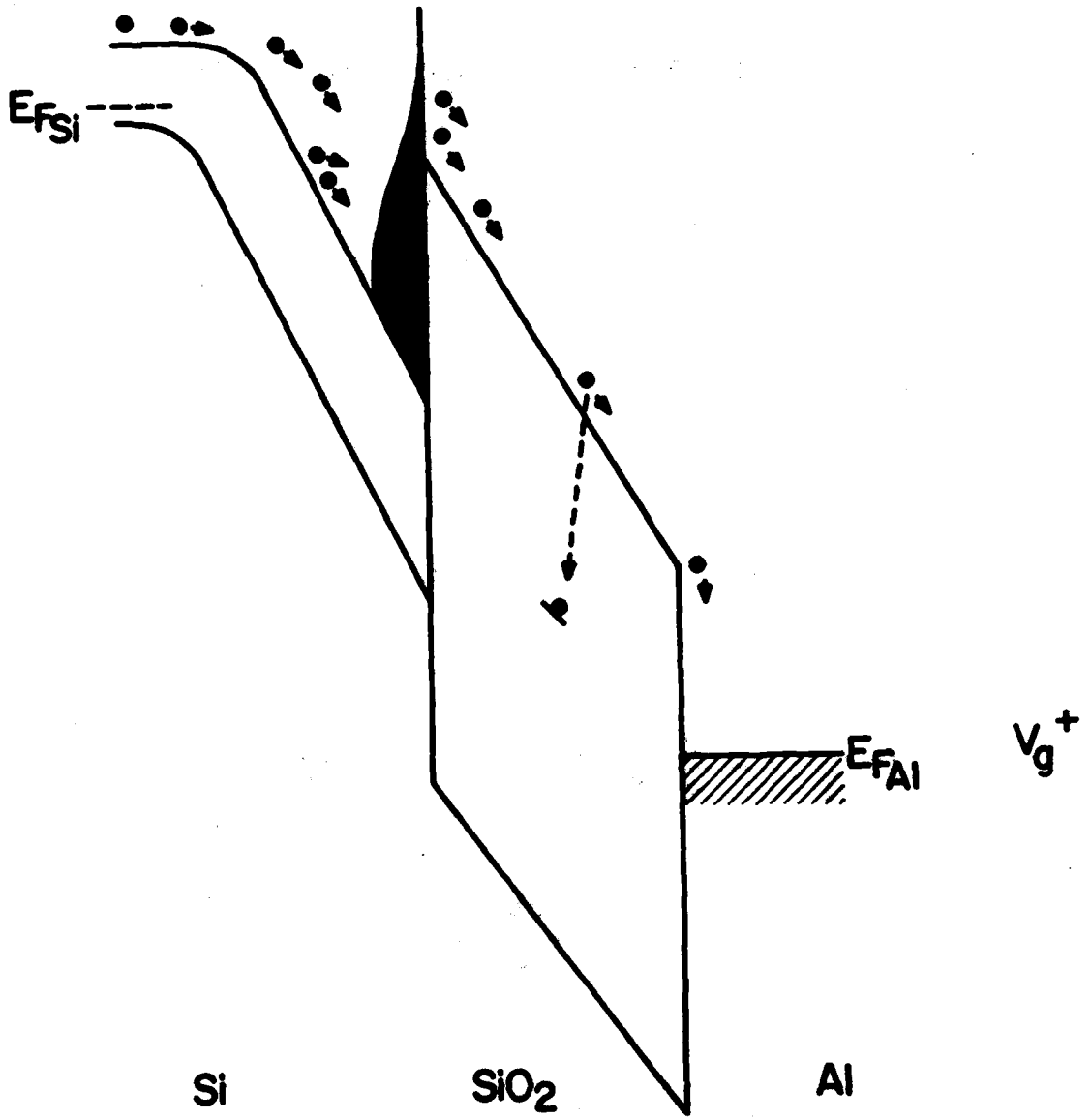


$$\Delta V_g^+ = -\frac{\bar{X}}{\epsilon} Q \qquad \Delta V_g^- = \frac{(L-\bar{X})}{\epsilon} Q$$

$$\bar{X} = L\left(1 - \frac{\Delta V_g^-}{\Delta V_g^+}\right)^{-1}$$

$$Q = \frac{\epsilon}{L}\left(\Delta V_g^- - \Delta V_g^+\right)$$

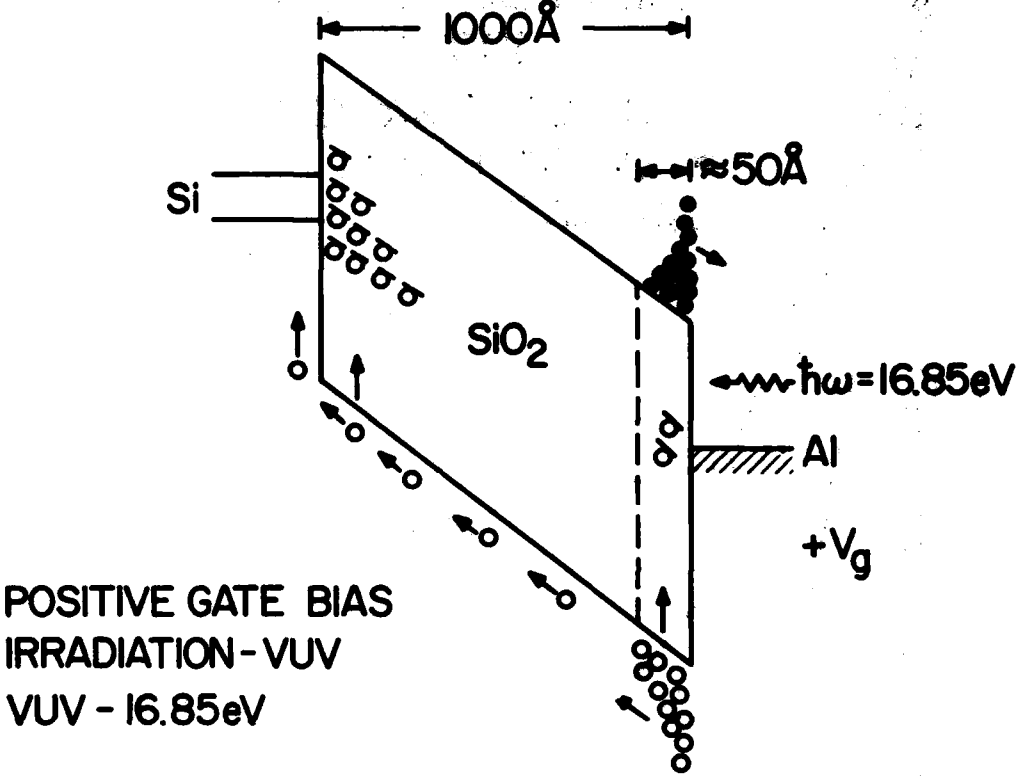
FIGURE 3



AVALANCHE INJECTION

FIGURE 4

FIGURE 5A



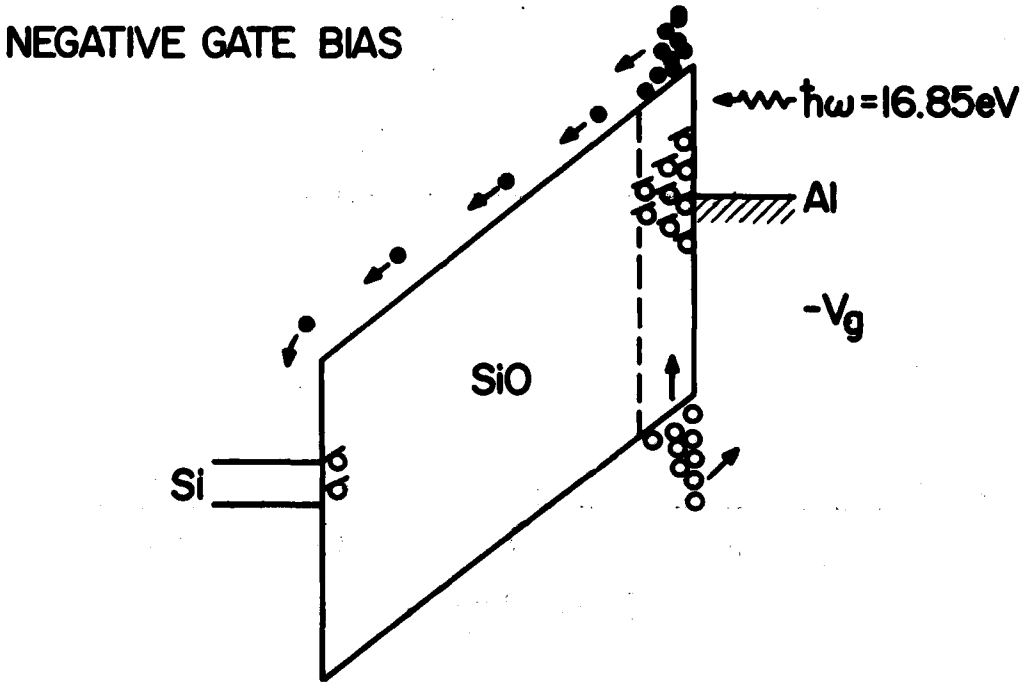


FIGURE 5B

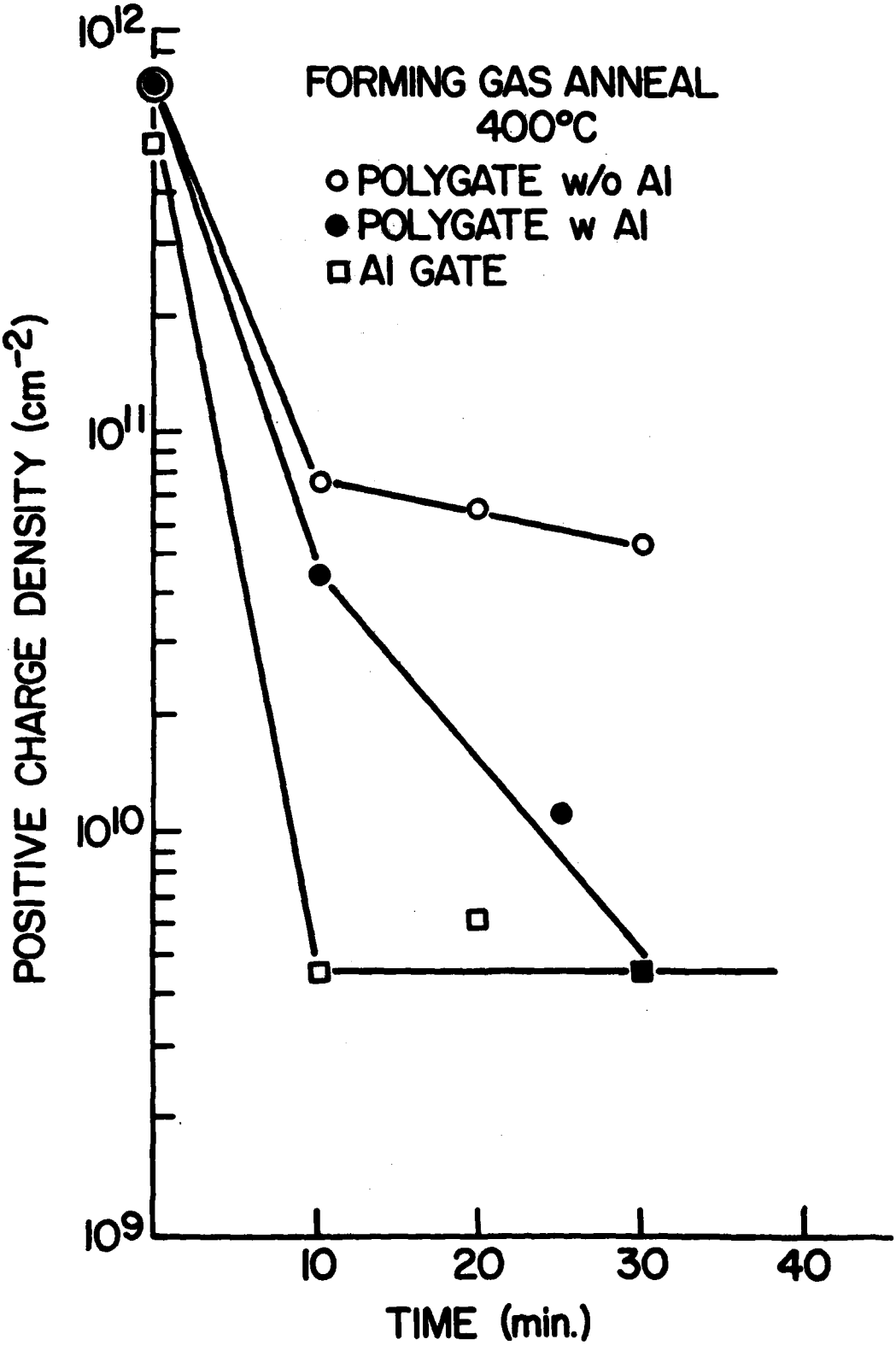

FORMING GAS ANNEAL
400°C
POLYGATE w/o Al
POLYGATE w Al
Al GATE
POSITIVE CHARGE DENSITY (cm⁻²)
10¹²
10¹¹
10¹⁰
10⁹
10
20
30
40
TIME (min.)

FIGURE 6

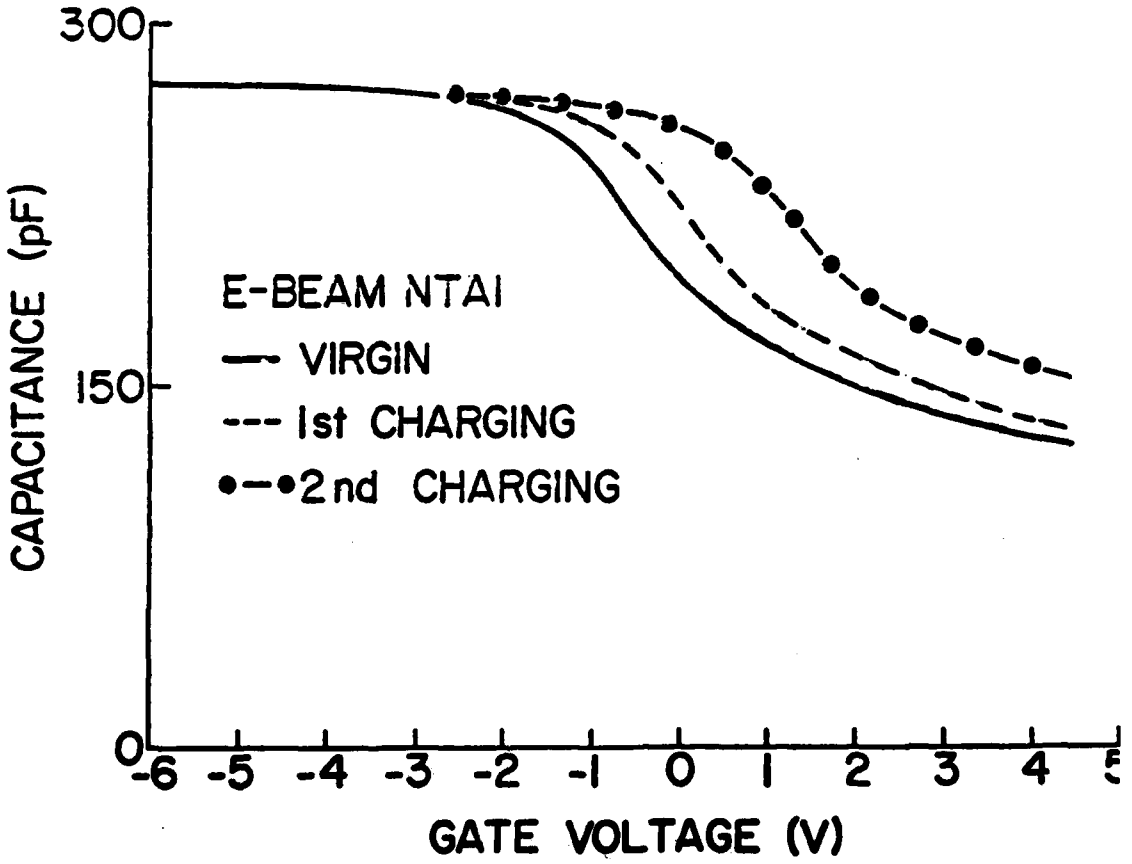

300
150
0
CAPACITANCE (pF)
E-BEAM NTAI
VIRGIN
1st CHARGING
2nd CHARGING
-6 -5 -4 -3 -2 -1 0 1 2 3 4
GATE VOLTAGE (V)

FIGURE 7A

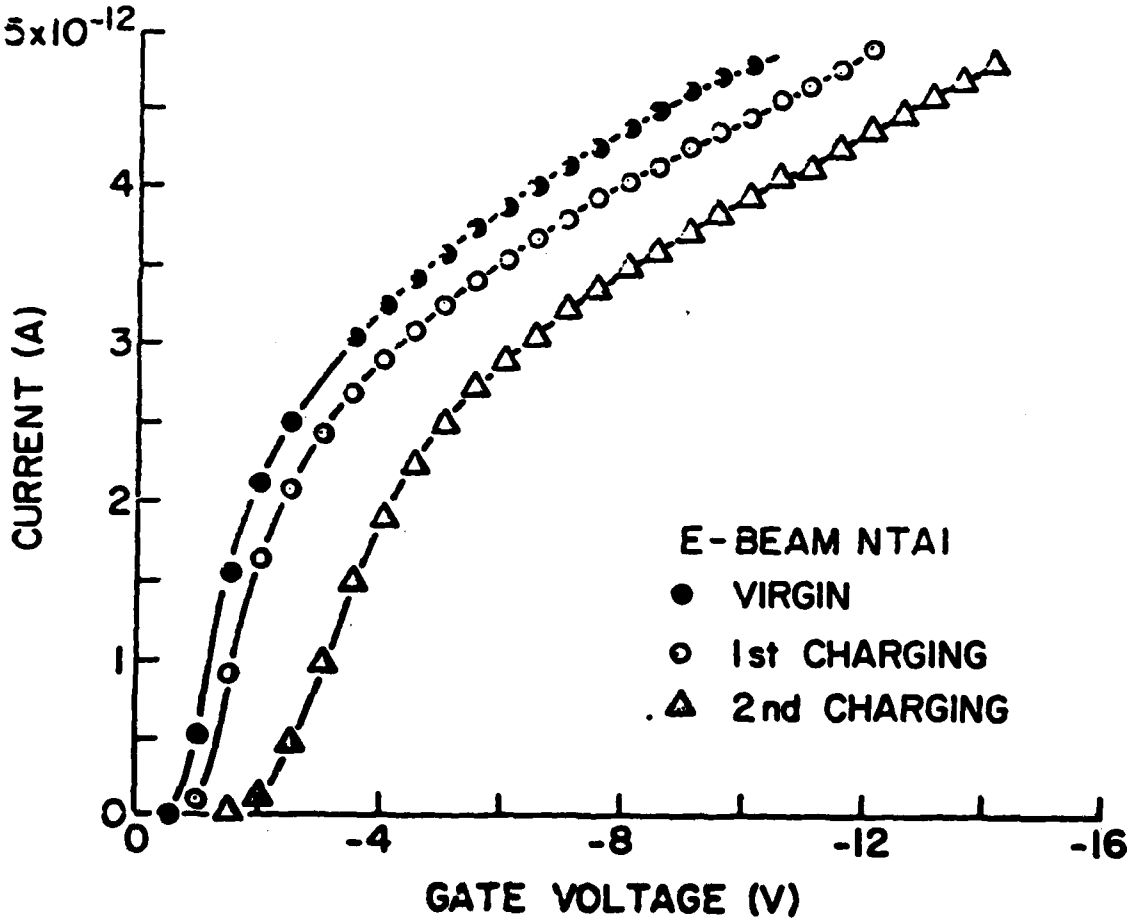

5x10-12
4
3
2
1
0
CURRENT (A)
0
-4
-8
-12
-16
GATE VOLTAGE (V)
E-BEAM NTAI
VIRGIN
1st CHARGING
2nd CHARGING

FIGURE 7B

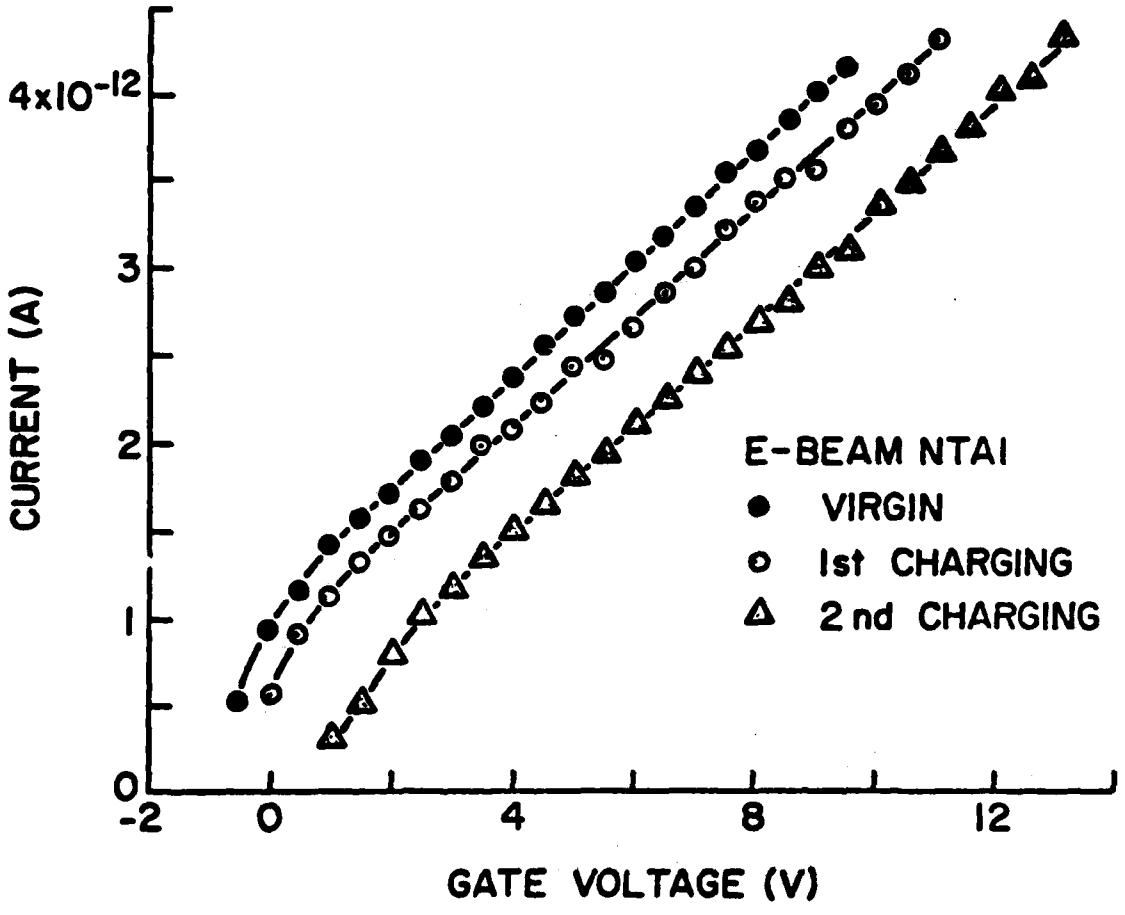

4x10-12
3
2
1
0
CURRENT (A)
-2
0
4
8
12
GATE VOLTAGE (V)
E-BEAM NTAI
VIRGIN
1st CHARGING
2nd CHARGING

FIGURE 7C

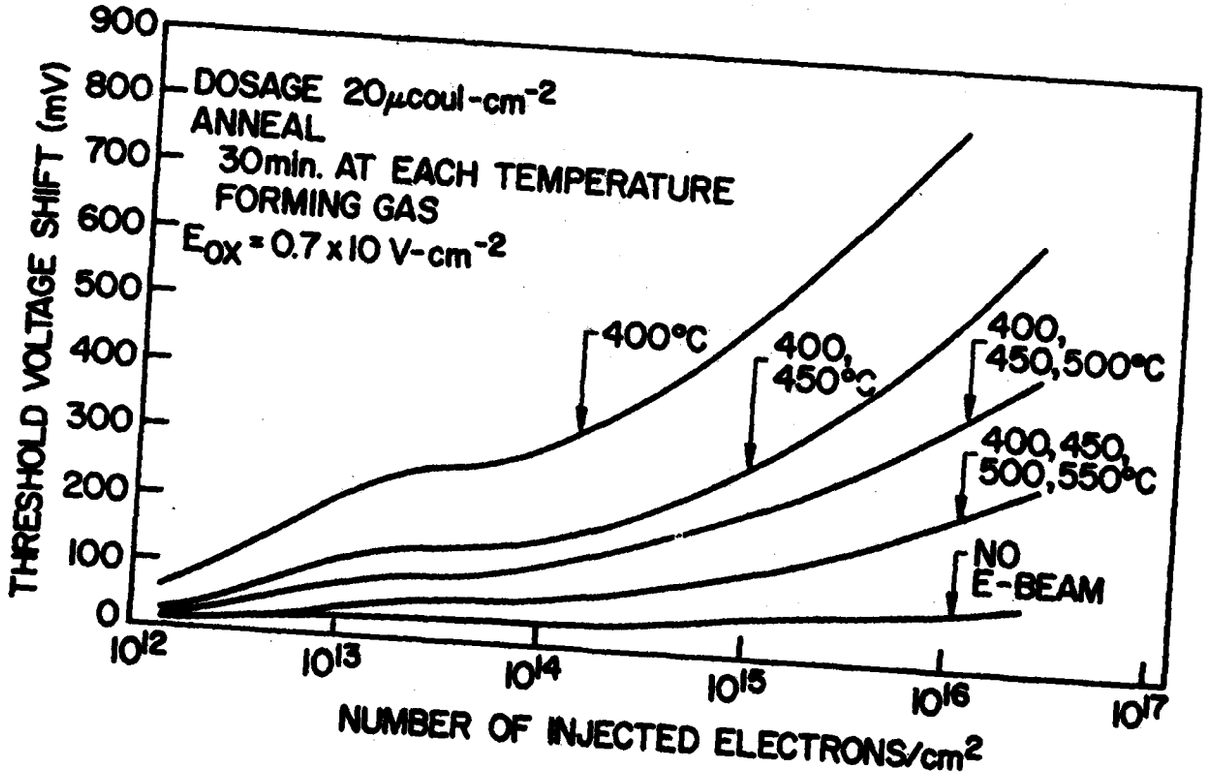

900
800
700
600
500
400
300
200
100
0
THRESHOLD VOLTAGE SHIFT (mV)
DOSAGE 20μcoul-cm-2
ANNEAL
30min. AT EACH TEMPERATURE
FORMING GAS
Eox = 0.7 x 10 V-cm-2
400°C
400, 450°C
400, 450, 500°C
400, 450, 500, 550°C
NO E-BEAM
10^12
10^13
10^14
10^15
10^16
10^17
NUMBER OF INJECTED ELECTRONS/cm2

FIGURE 8

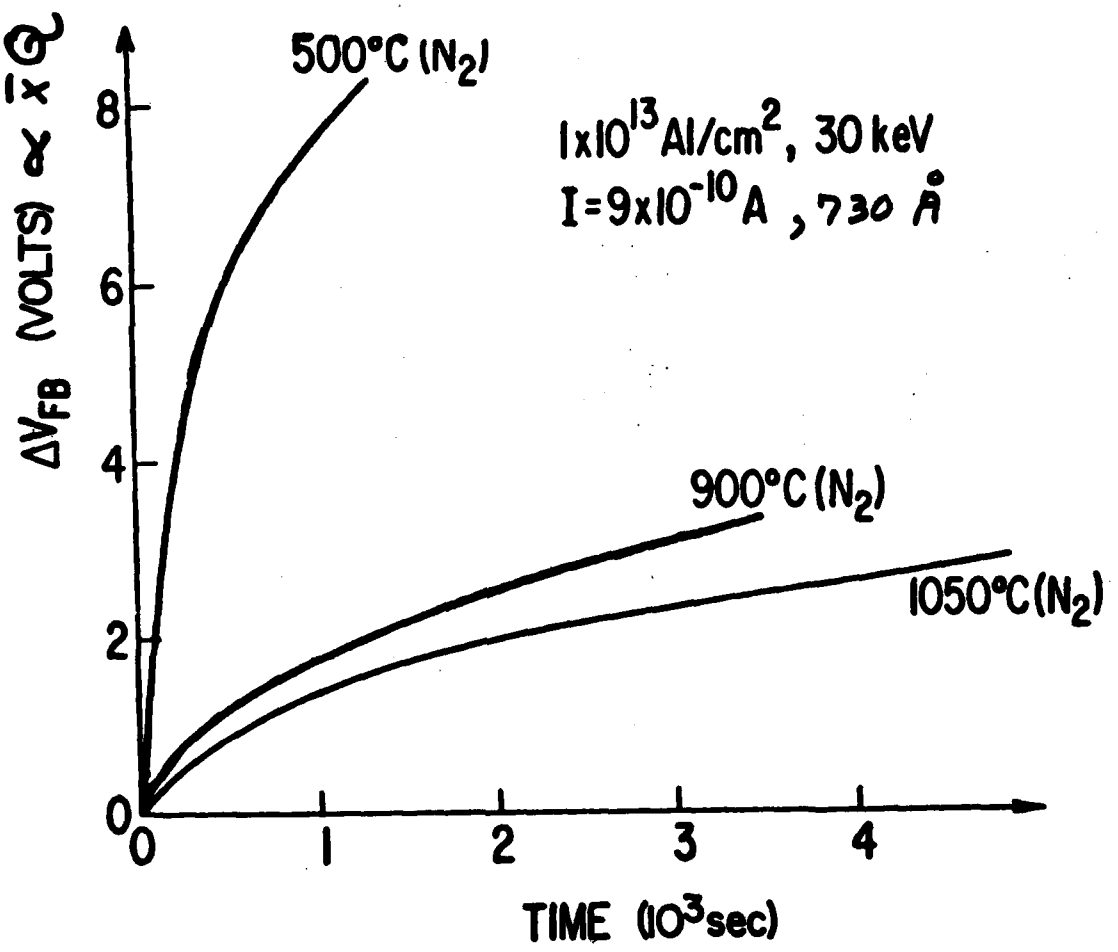


FIGURE 9

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