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IMPLEMENTATION OF DIGITAL QUADRATURE MODULATION,(U)
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UNCLASSIFIED MRI-149-11 NL

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TECH NOTE 105-037

27 JAN 78

Technical note,

MRI-TN-105-037

DAAH40-78-C-0131

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MARK RESOURCES INCORPORATED

IMPLEMENTATION OF DIGITAL QUADRATURE MODULATION

MRI REPORT 149-11

BY

I. P. BOTTLIK

27 January 1978

Contract DAAK40-78-C-0031

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IMPLEMENTATION OF DIGITAL QUADRATURE MODULATION

Two basic methods of implementing digital quadrature modulation have been proposed.[1] Although the multiplying D/A implementation appears at first look to be simpler than the digital multiplier implementation, a more detailed analysis favors the digital multiplier implementation. The digital multiplier implementation is about $9,500 less expensive since the multiplier may be easily multiplexed over 8 range gates. It is impractical to multiplex the analog reference voltage in the multiplying D/A implementation, and the required 4-quadrant multiplying DAC's are more expensive than the simple DAC's required for the digital multiplier implementation. Furthermore, the digital multiplying implementation may not be able to meet the performance requirements due to the slower setting time of multiplying DAC's and the unknown capability of the multiplying DAC to follow the rapid changes of the reference voltage. It is thus recommended that the implementation of digital quadrature modulation be the digital multiplier method.

Cost estimates for both methods of implementation are presented in Tables 1 and 2. The designs are for four channels of eight range gates each, including the interfacing to the array processor. The costs do not include conversion to 2's complement integers which might be accomplished in the array processor. Space requirement is 7 to 10 inches of 19" rack space for either implementation.

[1] Bottlik, I.P., "Digital Quadrature Modulation," MRI Report 149-7, dated 5 January 1978.

Table 1. Cost Estimate - Digital Multiplier Implementation

12-bit D/A	$100.00		
OP-AMP	60.00		
Holding registers, select logic, multiplexer	40.00		
	$200.00	× 32 range gates	$ 6,400.00
Multiplier (12×12 bit)	$200.00		
RAM, select logic, holding registers	40.00		
	$240.00	× 32/8 (1 per channel)	$ 960.00
Line drivers & receivers, bins, drivers, cabling	$200.00		
Interface control	150.00		
Timing, clock	200.00		
	$550.00		$ 550.00
Power supplies	$200.00		$ 200.00
		Total Electronic Parts	$ 8,110.00
Card file	$350.00		$ 350.00
Cards	100.00	× 14	1,400.00
Miscellaneous packaging (connectors, fans)	200.00		200.00
		Total Packaging Hardware	$ 1,950
		Parts Cost	$10,060 ≈ 10K
		Loaded Parts Cost	$12K

Mixer compensation test (to determine if mixer compensation is required, probably not required but costs do not reflect any compensation).

Breadboard D/A, OP-AMP & drive from Mini 6 at RFSS, & software for test signals	$ 4K + 0.5K travel
Design (including interface & timing)	$ 8K
Prototype (1 range gate fabrication & test & modifications)	$ 6K
Fabrication & test	$10K
Documentation (good engineering practice)	$ 2K
Hardware for tests to assure correct fabrication & design	$ 2K
	$32.5K
Total Unit Cost	$44.5K
(Optional) host, AP & PIOP programming for host signals	$ 7K + 0.5K travel
Tests at RFSS	$ 2K + 0.5K travel
	$10K
TOTAL COST	$54.5K

Table 2. Cost Estimate - Multiplying D/A Implementation

12-bit multiplying DAC	$250.00	
12-bit voltage DAC	160.00	
Holding registers, select logic, RAM, multiplexer	60.00	
	$470.00 × 32 range gates	$15,040.00
Line drivers & receivers, bus drivers, cabling	$200.00	
Interface control	150.00	
timing, clock	200.00	
	$550.00	$ 550.00
Power supplies	$200.00	$ 200.00
	Total Electronic Parts	$15,790.00
Card file	$350.00	$ 350.00
Cards	$100.00 × 14	$ 1,400.00
Misc. packaging (connectors, fans)	$200.00	$ 200.00
	Total Packaging Hardware	$ 1,950.00
	Parts Cost	$17,740.00
	Loaded Parts Cost	$21,288.00
		≈ 21.5K

Other costs are the same as for digital multiplier implementation.

Design fabrication and tests		$32.5K
	Total Unit Cost	$54.0K
(Optional) PIOP test programming & tests at RFSS		$10.0K
	TOTAL COST	$64.0K