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DIGITAL QUADRATURE MODULATION

MRI Report 149-7

I. P. Bottlik

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1. Introduction and Summary

Two methods of modulation, analog quadrature and amplitude-phase, are being considered for the near term implementation of clutter and extended targets. Due to the practical non-linearities and imbalances of the physical devices implementing these modulation methods a compensation method is required to achieve acceptable performance. Rather complicated compensation tables are required, a calibration procedure is required to determine the table values, and the stability of the compensation is in question due to its sensitivity on possible drifts of the physical device characteristics. The compensation must be performed in real time and requires a considerable amount of digital processing.

This report considers an alternate method of digitally processing the modulation signals to obtain a real signal which is then mixed up to the desired frequency. This mixing is the only operation subject to practical non-linearities and drifts. Such a simple mixing does not have the extreme sensitivity to mixer imbalances exhibited by analog quadrature modulation. It is anticipated that this mixing will require no compensation; however, should compensation be required it would be simple since only one signal (no cross-coupling) need by compensated.

The digital processing required for this method is rather sample and inexpensive. The baseline design of the digital processing achieves 61 dB suppression for the fourfold repetition of a 12 kHz wide (total width) input spectrum, requiring 12-bit 2's complement multiplies at a rate of 192 kHz, a 12-bit D/A operating at 384 kHz, 16 12-bit weight values, and some control circuitry. This allows the use of low cost D/A's for each range gate and the multiplexing of the 12-bit multiplier over many range gates.

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In Section 2 the cause of the extreme sensitivity of analog quadrature modulation to imbalances between the two mixers is shown. Section 3 presents the digital quadrature modulation method and Section 4 presents two implementations of the method. Section 5 presents simulation results of a baseline design using the 2's complement multiplier implementation.

2. Major Error Source in Analog Quadrature Modulation

It is shown that for a single sided spectrum the suppression of the image half of the spectrum is obtained by the cancellation of the reflected spectra obtained in each mixer. It is the difference of two large quantities obtained from different mixers and is thus highly sensitive to practical imbalances between the two mixers.

Figure 1 shows the schematic diagram of an analog quadrature modulator.

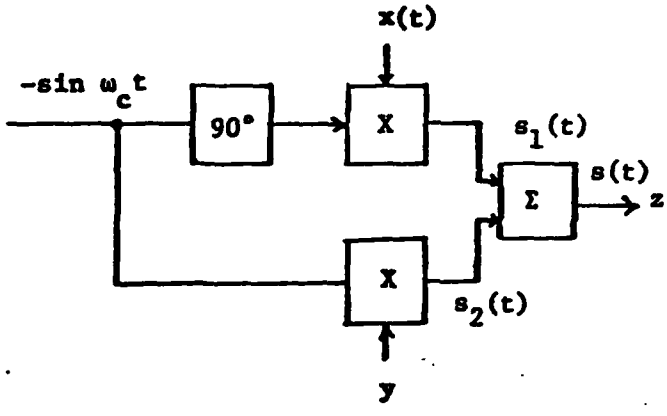


Figure 1. Analog Quadrature Modulator.

The output signal is given by:

$$s(t) = s_1(t) + s_2(t)$$

where

$$s_1(t) = x(t)\cos\omega_c t$$

$$s_2(t) = -y(t)\sin\omega_c t \qquad (1)$$

Let $z(t) = x(t) + jy(t)$ and let $Z(\omega)$ be the spectrum of $z(t)$. Then

$$s_1(t) = (z+z^*)(e^{j\omega_c t} + e^{-j\omega_c t})(1/4) \tag{2}$$

and its spectrum is

$$S_1(\omega) = (1/4)[Z(\omega-\omega_c)+Z^*(-\omega+\omega_c)+Z(\omega+\omega_c)+Z^*(-\omega-\omega_c)] \tag{3}$$

Similarly

$$S_2(\omega) = (1/4)[Z(\omega-\omega_c)-Z^*(-\omega+\omega_c)-Z(\omega+\omega_c)+Z^*(-\omega-\omega_c)] \tag{4}$$

Thus the spectrum of the output is

$$\begin{aligned} S(\omega) &= S_1(\omega) + S_2(\omega) \\ &= (1/4)[Z_1(\omega-\omega_c)+Z_2(\omega-\omega_c)+Z_1^*(-\omega-\omega_c)+Z_2^*(-\omega-\omega_c) \\ &\quad + Z_1^*(-\omega+\omega_c)-Z_2^*(-\omega+\omega_c)+Z_1(\omega+\omega_c)-Z_2(\omega+\omega_c)] \end{aligned} \tag{5}$$

The last four terms are the cause of the sensitivity to imbalance since they are the differences of large quantities obtained from different mixers. They would cancel exactly if there was no imbalance. Figure 2 shows the effect schematically.

3. Digital Quadrature Modulator - Method

Let $z(i) = x(i) + jy(i)$ be an input complex sequence with spectrum $Z(n)$. The digital quadrature modulator derives a sequence at N times the z signal given by

$$s(iN+k) = \begin{cases} x(i) \times w(k) & k \text{ even} \\ y(i) \times w(k) & k \text{ odd} \end{cases} \quad k \in [0,N) \tag{6}$$

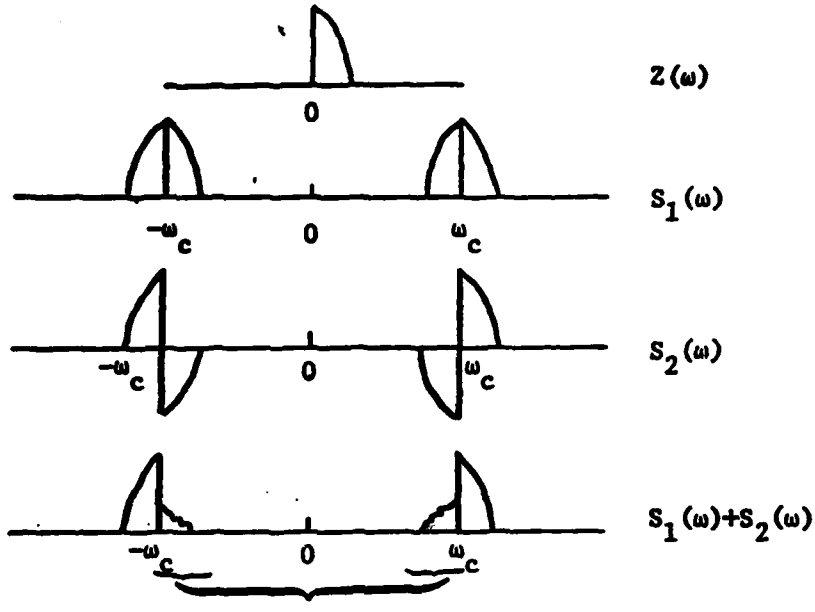
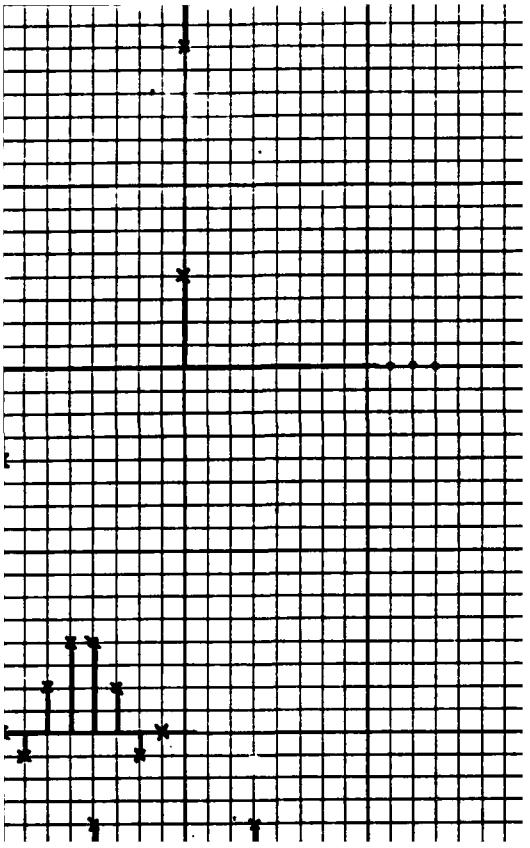


Figure 2. Analog Quadrature Modulation Sensitivity.

where w(k) is a set of N fixed weights. The rate of this signal is then doubled by simply inserting zeroes, i.e.,

$$s'(2(iN+k)+m) = \begin{cases} s(iN+k) & m=0 \\ 0 & m=1 \end{cases} \qquad (7)$$

This digital sequence is then converted to a sample and held analog signal. This process is illustrated in Figure 3 for N = 8 (the values for w are for illustration only). The analog signal then feeds a mixer. Figure 4 shows a block diagram of the digital quadrature modulator.



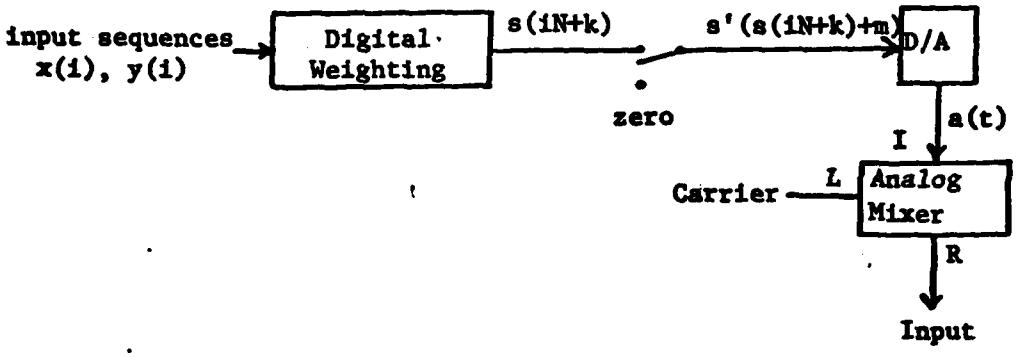


Figure 4. Digital Quadrature Modulator.

The quantity N and the weights w are chosen to give a fourfold repetition of the input spectrum Z(n) about a carrier at $N/4\Delta t$ where Δt is the time interval between the input samples z(i). Outside this region Z(n) still repeats but is degraded — in particular, it becomes more symmetrical. However, the receiver does no Doppler processing in this degraded region. In Section 5 a simulation example is shown.

4. Digital Quadrature Modulator - Implementation

Two basic methods of implementing the digital quadrature modulator are presented. The first method uses a digital multiplier while the second uses a multiplying D/A to accomplish the multiplication by the weights, w.

4.1 Digital Multiplier

Figure 5 shows a simplified block diagram of the digital multiplier method of implementation.

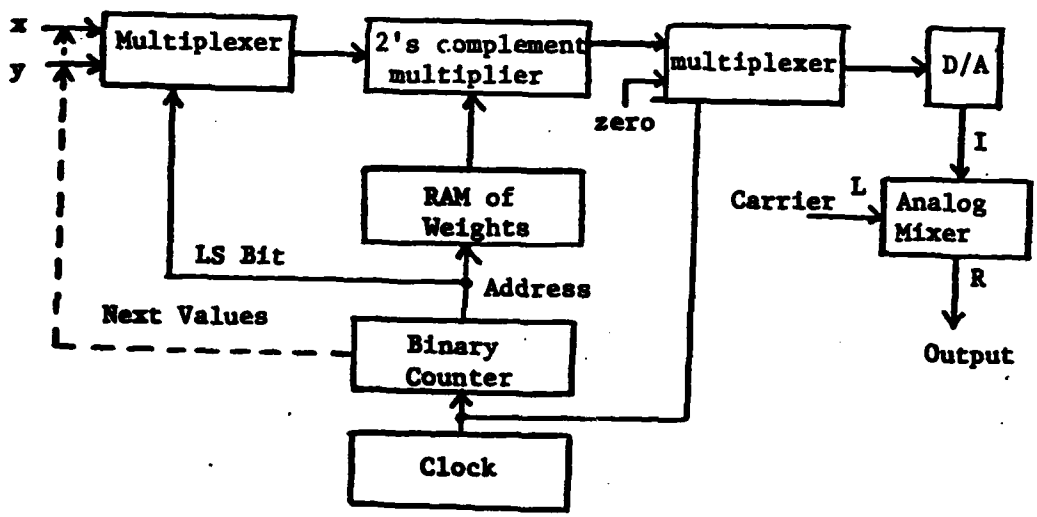


Figure 5. Digital Multiplier Implementation.

4.2 Multiplying D/A

Figure 6 shows a simplified block diagram of the multiplying D/A method of implementation. In this implementation the multiplication is accomplished by varying the reference voltage of a multiplying D/A by the output of a D/A driven by the table of weights.

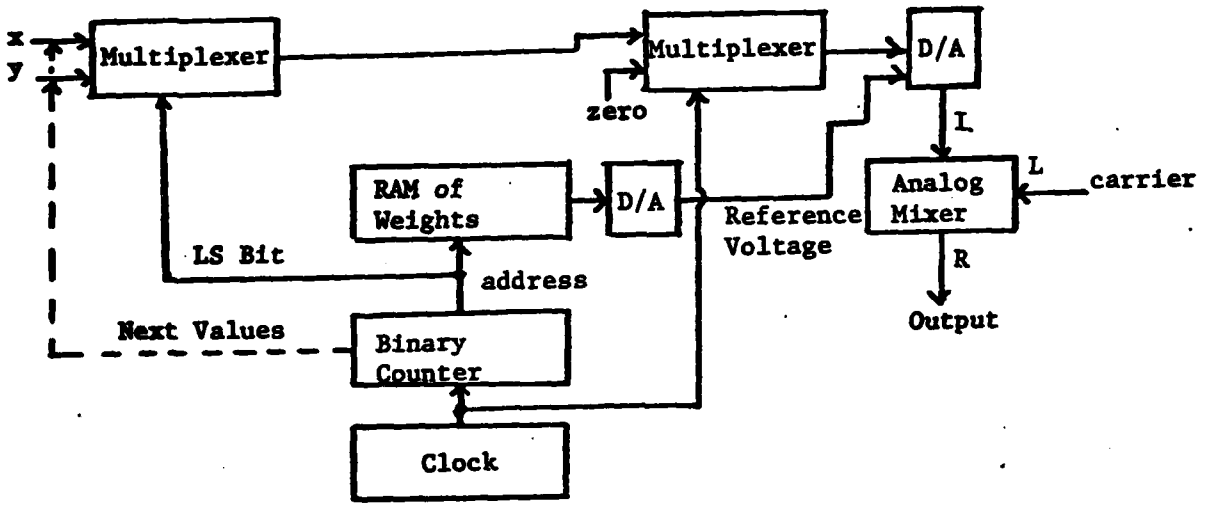


Figure 6. Digital Multiplier Implementation.

5. Simulation Results

The digital multiplier method using a 12-bit by 12-bit 2's complement multiplier with the product truncated to 12 bits driving a 12-bit D/A has been simulated. A baseline design with 16 12-bit weights achieved 61 dB suppression with fourfold repetition of the input spectrum. With the input spectrum repeating at 12 kHz this design requires multiplications at the rate of 192 kHz and requires the D/A to operate at 384 kHz. Thus a readily available multiplier (TRW MPY-12AJ 175 ns, $165) could be readily multiplexed over 8 range gates. D/A's at 384 kHz are inexpensive.

Figure 7 shows the typical random input spectrum used for the simulation. Figure 8 again shows this spectrum after quantizing the time signals to 12 bits (2's complement). Figure 9 shows the spectrum of the digitally processed signal s (see Section 3). Figure 10 is the detail of Figure 9 over

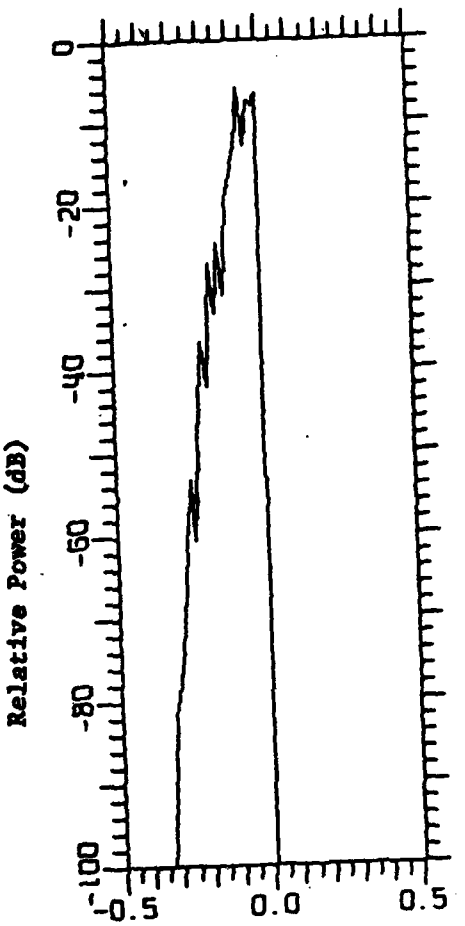


Figure 7. Input Spectrum.

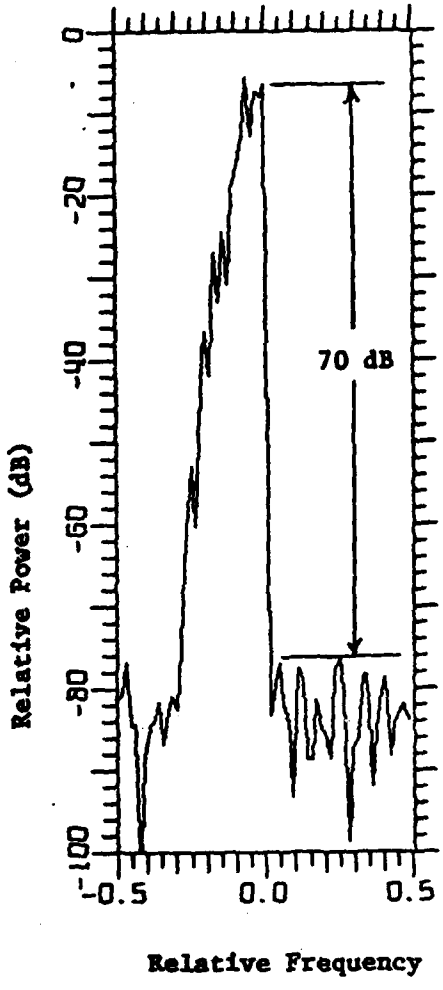


Figure 8. Input Spectrum, 12-bit Quantization.

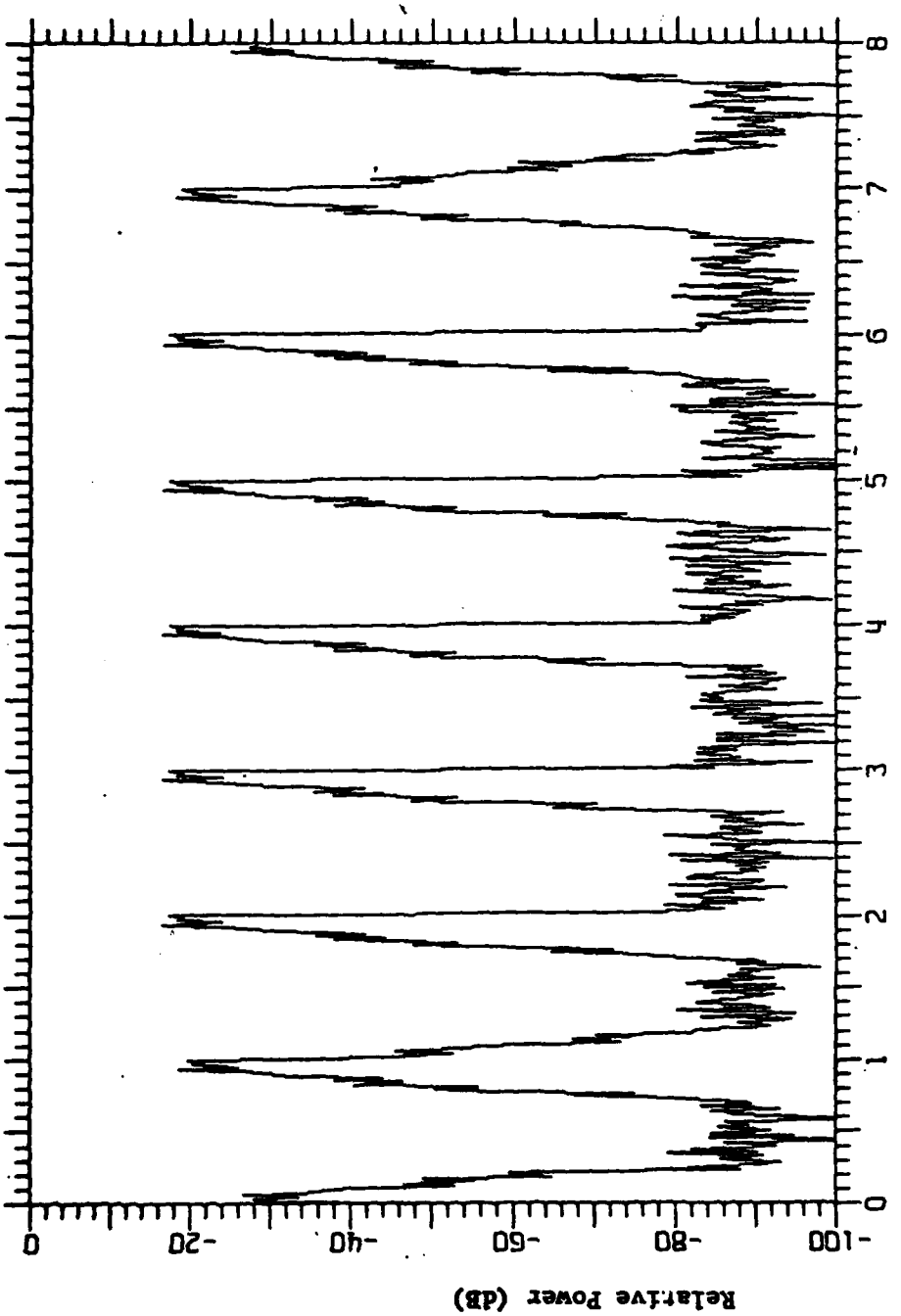


Figure 9. Output Spectrum.

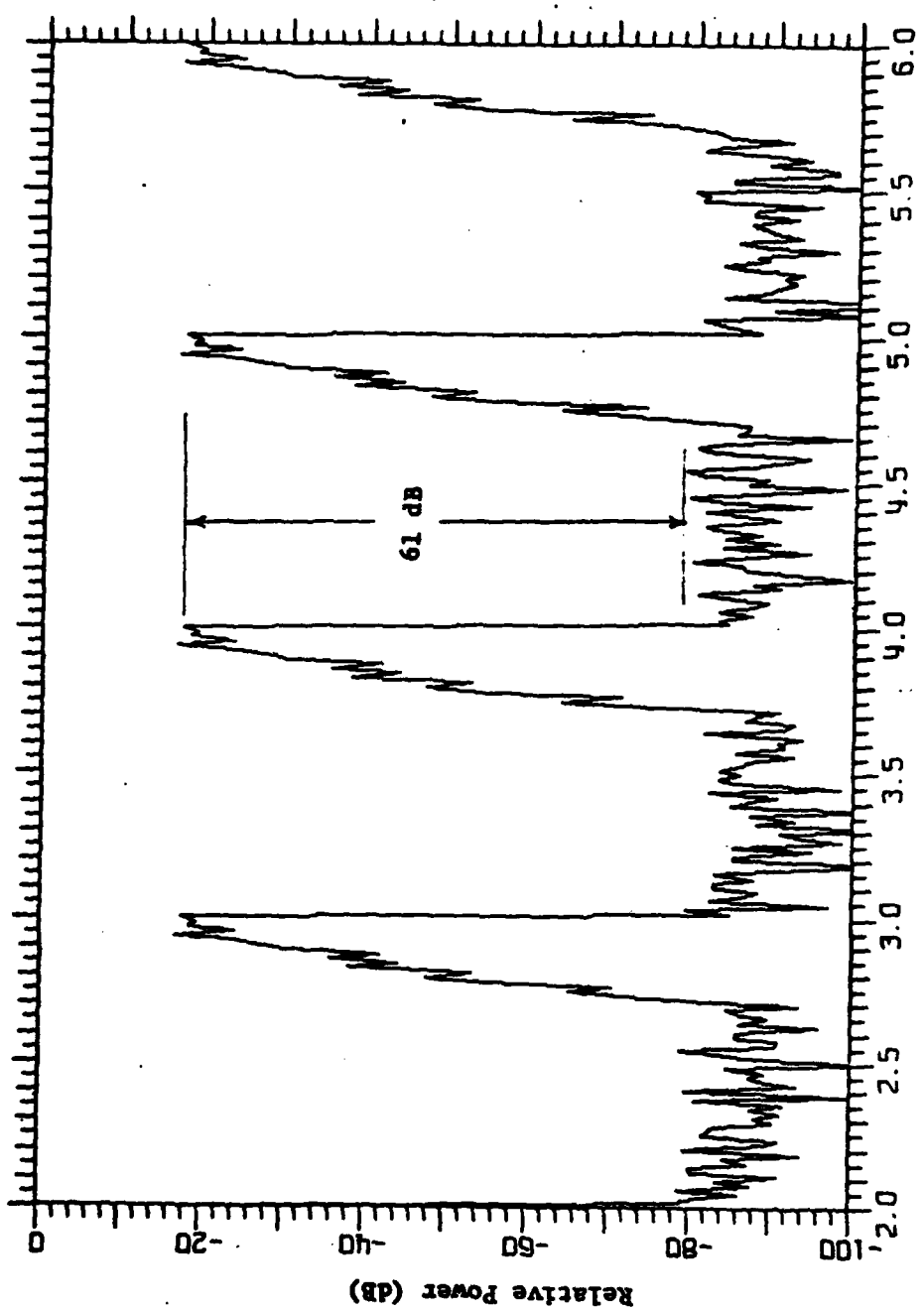


Figure 10. Detail of Output Spectrum Over Region of Interest.

the region of interest. It shows that the desired input spectrum is faithfully reproduced fourfold with 61 dB suppression of spurious sidelobes. The analog RF output signal will have essentially the same spectrum as Figure 10 (over the region of interest) except for two minor effects. First, the sample-and-hold on the D/A combined with the switching to zero will cause the spectrum to be multiplied by $\sin^2(x)/x^2$. This causes a gradual attenuation of 0.7 dB over the first two repetitions and an additional 1.2 dB attenuation over the last two repetitions. Secondly, the analog mixer will introduce intermodulation distortions which are anticipated to be sufficiently depressed when using a low-level drive signal.