AD-A089 523 COAST GUARD WASHINGTON DC OFFICE OF RESEARCH AND DEV--ETC F/G 17/7
MAGNETIC SENSOR FEASIBILITY TEST FOR COAST GUARD VESSEL TRAFFIC--ETC(U)
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Report No. CG-D-51-80 LEVEL (12) II B.S.

MAGNETIC SENSOR FEASIBILITY TEST FOR COAST GUARD VESSEL TRAFFIC SERVICES

LT T. M. DROWN

AUGUST 1980

Document is available to the U.S. public through the
National Technical Information Service,
Springfield, Virginia 22161

Prepared for

U.S. DEPARTMENT OF TRANSPORTATION
United States Coast Guard
Office of Research and Development
Washington, D.C. 20593

NOTICE

(14) USCG-D-51-80

Technical Report Documentation Page

1. Report No. CG-D-51-80	2. Government Accession No. AD-A089 533	3. Recipient's Catalog No.
4. Title and Subtitle (6) Magnetic Sensor Feasibility Test for Coast Guard Vessel Traffic Services		5. Report Date August 1980
		6. Performing Organization Code G-DST-3
7. Author(s) (10) T. M. DROWN	(11) Aug 80	8. Performing Organization Report No. (12) 76
9. Performing Organization Name and Address Office of Research and Development U. S. Coast Guard Washington, D. C. 20593		10. Work Unit No. (TRAIS)
		11. Contract or Grant No.
12. Sponsoring Agency Name and Address Office of Marine Environment and Systems U. S. Coast Guard Washington, D. C. 20593		13. Type of Report and Period Covered (9) Final Report
		14. Sponsoring Agency Code G-WWM-1

15. Supplementary Notes

16. Abstract

The Coast Guard Office of R & D has an on-going project to test the feasibility of using various sensors in the monitoring of vessel traffic in existing Vessel Traffic Service (VTS) operating areas. This report describes the effort involved in testing magnetic sensors. The report contains a description of both the sensor system configuration and the results of feasibility tests that were performed in Houston, Texas and Sault Ste Marie, MI.

17. Key Words Vessel Traffic Service, Passive Sensor Systems, Magnetometer, VTS Operations	18. Distribution Statement Available to the U. S. Public through the National Technical Information Service, Springfield, VA 22161

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price
Unclassified	Unclassified		

Form DOT F 1700.7 (8-72) Reproduction of completed page authorized

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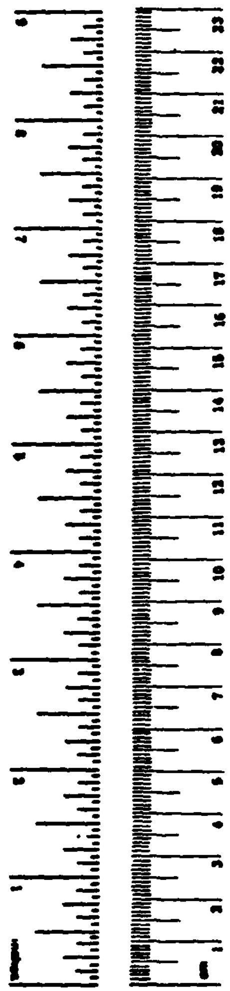
METRIC CONVERSION FACTORS

Approximate Conversions to Metric Measures

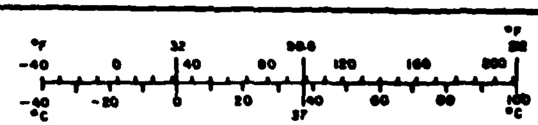
Symbol	When You Know	Multiply by	To Find	Symbol
		LENGTH		
in	inches	*2.5	centimeters	cm
ft	feet	30	centimeters	cm
yd	yards	0.9	meters	m
mi	miles	1.6	kilometers	km
		AREA		
in^2	square inches	6.5	square centimeters	cm^2
ft^2	square feet	0.09	square meters	m^2
yd^2	square yards	0.8	square meters	m^2
mi^2	square miles	2.6	square kilometers	km^2
	acres	0.4	hectares	ha
		MASS (weight)		
oz	ounces	28	grams	g
lb	pounds	0.45	kilograms	kg
	short tons (2000 lb)	0.9	tonnes	t
		VOLUME		
tsp	teaspoons	5	milliliters	ml
Tbsp	tablespoons	15	milliliters	ml
fl oz	fluid ounces	30	milliliters	ml
c	cups	0.24	liters	l
pt	pints	0.47	liters	l
qt	quarts	0.95	liters	l
gal	gallons	3.8	liters	l
ft^3	cubic feet	0.03	cubic meters	m^3
yd^3	cubic yards	0.76	cubic meters	m^3
		TEMPERATURE (exact)		
°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C

*1 in ≡ 2.54 (exactly). For other exact conversions and more detailed tables, see NBS Misc. Publ. 286, Units of Weights and Measures, Price $2.25, SD Catalog No. C13.10:286.



Approximate Conversions from Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
		LENGTH		
mm	millimeters	0.04	inches	in
cm	centimeters	0.4	inches	in
m	meters	3.3	feet	ft
m	meters	1.1	yards	yd
km	kilometers	0.6	miles	mi
		AREA		
cm^2	square centimeters	0.16	square inches	in^2
m^2	square meters	1.2	square yards	yd^2
km^2	square kilometers	0.4	square miles	mi^2
ha	hectares (10,000 m^2)	2.5	acres	
		MASS (weight)		
g	grams	0.035	ounces	oz
kg	kilograms	2.2	pounds	lb
t	tonnes (1000 kg)	1.1	short tons	
		VOLUME		
ml	milliliters	0.03	fluid ounces	fl oz
l	liters	2.1	pints	pt
l	liters	1.06	quarts	qt
l	liters	0.26	gallons	gal
m^3	cubic meters	35	cubic feet	ft^3
m^3	cubic meters	1.3	cubic yards	yd^3
		TEMPERATURE (exact)		
°C	Celsius temperature	9/5 (then add 32)	Fahrenheit temperature	°F



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MAGNETIC SENSOR FEASIBILITY TEST FOR COAST GUARD VESSEL TRAFFIC SERVICES

1.0 INTRODUCTION

1.1 BACKGROUND

In recognition of the increasing probability for the occurance of a vessel accident in U. S. waters, and of the increasing potential for such an accident to cause injury to personnel and/or damage to vessels, port facilities and the environment, congress passed "The Ports and Waterways Safety Act of 1972", Public Law 92-340. Under this act, the Department of Transportation has the authority to:

(a) "...Establish, operate and maintain Vessel Traffic Services and systems for ports, harbors and other waters subject to congested traffic

(b) Require vessels which operate in an area of a vessel traffic service or system to comply with that service or system

(c) Control vessel traffic in areas which (the Coast Guard) determines to be especially hazardous, or under conditions of reduced visibility, adverse weather, vessel congestion or other hazardous circumstances..."

The Coast Guard is the agency responsible for implementing the services mandated by this law.

In order for a Vessel Traffic Service (VTS) to operate efficiently, it must establish a surveillance system that provides updated information about ship traffic in its service area. Current VTS operations rely on two primary surveillance tools: radar and direct RF voice communications. Each tool has its practical limits. Radar can be used in a great many port areas, but it has a cost/benefit threshold that prevents it from being used in remote and/or restricted waterways. Direct voice communications are effective in determining the passage of vessels at predetermined checkpoints and to pass and obtain other pertinent information, but radio channels are already crowded in some ports. The Coast Guard Office of Research and Development has initiated a project to investigate surveillance systems that might be used to either augment radar and voice communications or efficiently replace them under certain circumstances.

Vessel Traffic Services (VTS) have been established in San Francisco CA, Pudget Sound, WA, St. Marys River MI, Houston TX, New Orleans LA, and Valdez AK. Their normal method of operation is to provide an advisory to vessels operating in each service area. Information contained in the advisory includes vessel movement, hazards to navigation and weather. The information is collected and disseminated by one station in each VTS area called the Vessel Traffic Center (VTC). The majority of the information on vessel movements is provided by the marine community on a cooperative basis.

The use of passive sensors in restricted waterways such as rivers, canals and some channels might provide additional surveillance capability. These restricted waterways present a unique circumstance whereby the flow of vessel traffic is well defined. The direction of flow is usually in two reciprocal directions, and there is limited room for deviation from the channel centerline. It appears that, by placing passive sensors at checkpoints along a restricted waterway, sufficient information can be developed to provide position information on vessels in transit. Careful site selection would insure that vessels always pass within a sensor's detection field.

As an initial attempt to demonstrate the feasibility of using passive sensors, currently available sensors in the acoustic and magnetic stimulus areas were considered. A cursory sampling of acoustic conditions in a candidate waterway revealed a complex array of acoustic signals from both distant and near-by sources. It was estimated that considerable effort would be necessary to develop a signal processor to accommodate the variety of acoustic signals and provide the necessary localized information. Such an effort was not considered appropriate for a feasibility demonstration. A similar sampling was performed using Vietnam War era magnetic sensing equipment. The results of this test indicated that magnetic sensing equipment was a promising candidate for the project.

1.2 CONCEPT

The primary means used by a VTS to monitor the progress of a vessel through the restricted waters of a service area is RF voice communications. Each VTS establishes checkpoints along its waterways and requires each participating vessel to report as it passes each checkpoint. Using the checkpoint information along with estimated speed of travel between checkpoints, the VTS personnel are able to maintain a dead reckoned position on all participating vessels. This surveillance scheme, called a Vessel Movement Reporting System (VMRS), is easily implemented and generally effective. There are, however, shortcomings. Sometimes vessels are late in making their checkpoint reports. Sometimes vessels cannot maintain the estimated speed of advance between checkpoints. These two factors serve to greatly reduce the accuracy of dead reckon positioning and, thereby, reduce the effectiveness of the VMRS. Two improvements that might increase the effectiveness of the VRMS are to: (1) increase the number of checkpoints to provide a more continuous flow of position information and (2) automate the reporting function both to make the reports more timely and to reduce human intervention.

Surveilling the VMRS checkpoint with some kind of sensor appears to have the potential to provide the following benefits: (1) vessel passages are automatically detected, thus eliminating the voice reporting requirement, (2) the output of a sensor system can be tailored to accomodate any data processing and display scheme ranging from a manual system to a fully automatic system and (3) in the proper configuration a sensor system would provide increased surveillance capability with decreased manpower requirements by allowing more checkpoints to be established. It appears that passive sensors would provide and additional advantage because of their potential lower cost compared to active sensors, their smaller size, and because their operation does not necessarily require additional equipment to be carried by a cooperating vessel.

1.3 OBJECTIVE

The primary objective of this project was to demonstrate the concept of using passive sensors as a VTS surveillance system. Without developing a separate system for each known passive sensor, it was intended to demonstrate a system that would be typical of such configurations with regard to data acquisition, data transfer and display.

The secondary objective was to demonstrate the feasibility of using the magnetic sensor system to enhance existing VTS operations by using it in conjunction with a VMRS.

1.4 APPROACH

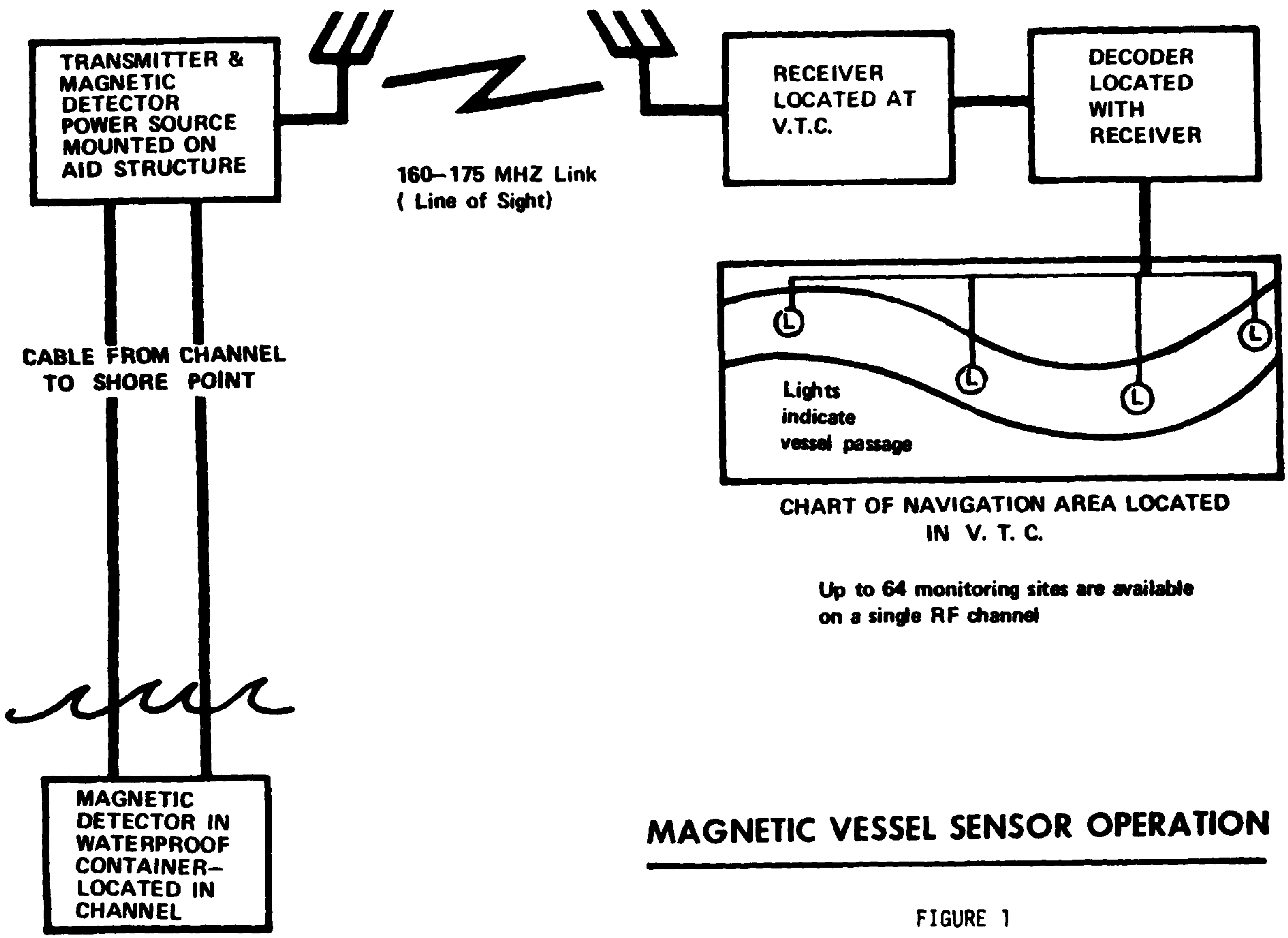
The demonstration system was based on equipment used in the Vietnam War. The Naval Surface Weapons Center (NSWC), White Oak: Silver Springs, MD was tasked with the adaptation and installation. The system was to be demonstrated in two waterways: (1) the Houston/Galveston Ship Channel, TX amd (2) the St. Marys River, MI. The demonstrations were intended to provide the opportunity to judge the feasibility of using passive sensors, in general, and magnetic sensors, in particular, as a VTS surveillance tool. The first demonstration took place in Houston, TX. The second demonstration took place in Sault Ste. Marie, MI.

2.0 SYSTEM DESCRIPTION

The experimental system was called the Remote Vessel Monitoring System (RVMS). The RVMS makes use of existing battlefield equipment used in the Vietnam War. The system components are: (1) The magnetic sensor, (2) a VHF radio transmitter, (3) a receiver/processor and (4) a display. Whenever a vessel triggers the magnetic sensor, the sensor turns on the transmitter. The transmitter emits a short digital message which contains a unique identification number. The receiver/processor interprets the message and causes a printer to print out both the identification number of the transmitter and time of receipt of the message. An indicator light is lit on a display to indicate the location of the transmitter. Figure 1 shows the concept of operations.

2.1 MAGNETIC SENSOR

The U. S. Army nomeclature for the sensor used in the system is: Magnetic Detector, GSQ 180(V). It is designed to detect a distrubance of the earth's magnetic field caused by the passage of some mass (such masses usually contain iron or steel). The sensor uses a single axis, ring core, flux gate magnetometer developed by R. E. Brown of NSWC. In additon to the magnetometer, the sensor package includes transistorized detection and output circuitry which generates a pulse to trigger an RF transmitter. The



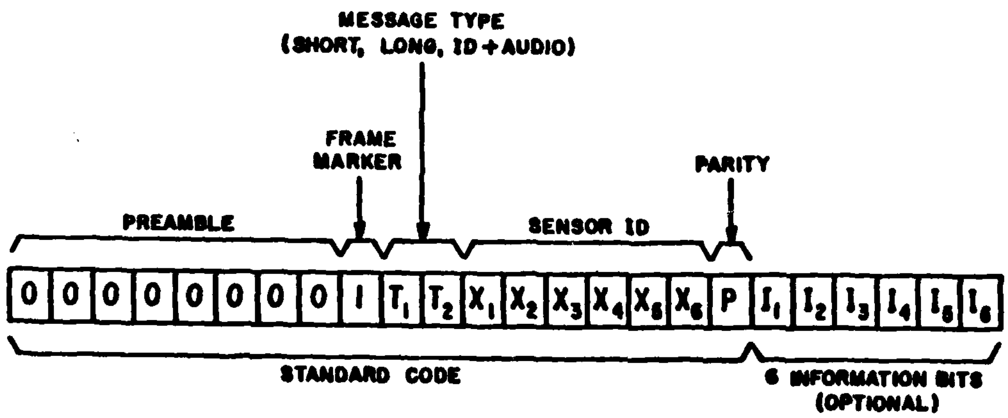
MAGNETIC VESSEL SENSOR OPERATION

FIGURE 1

detection circuity prevents the output of transmitter trigger pulses faster than one every ten seconds. The sensor was designed to detect a person carrying a rifle when the person passed within a few feet of the sensor. However, since detection by the magnetometer depends on sensing a disruption in the ambient magnetic environment, detection is a function of the mass of the target passing the sensor and the speed with which it passes. The estimated detection range for ships moving at five to eight knots is 100 yards for a 200 ton ship, 200 yards for a 1,000 ton ship and 400 yards for a 10,000 ton ship.

2.2 RADIO TRANSMITTER

The radio transmitter is a Model T1233, GSQ 154 (V), Minisid transmitter. Used in conjunction with a encoder, KY 678 (GSQ), the transmitter sends an 18 BIT digital message which contains the transmitter's unique identification number. The message is transmitted using bi-phase modulation at 300 bits per second. The nominal output power is 4 watts. The transmitter is triggered by a 6 volt pulse of 5 msec duration which is output by the magnetic sensor package. Figure 2 shows the message format.

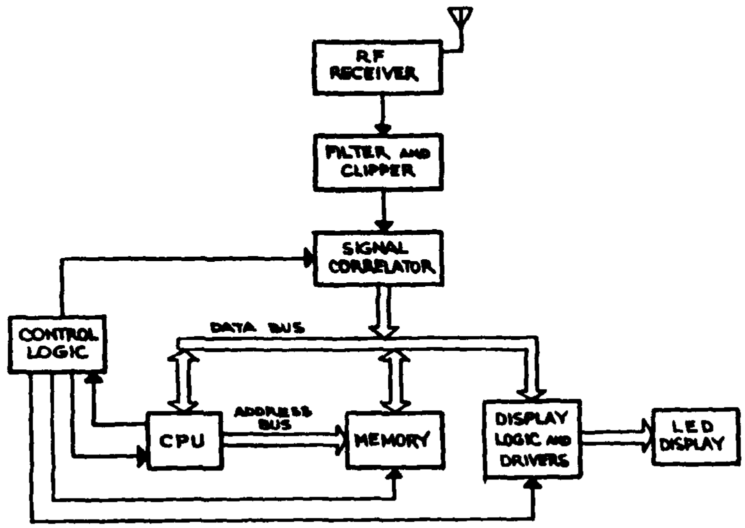


RF TRANSMISSION MESSAGE FORMAT

FIGURE 2

2.3 RECEIVER/PROCESSOR

The receiver/processor was patterned after the U. S. Army Radio Frequency Monitor, R16717Z/USQ 46Z. The frequency monitor was much more sophisticated than was required for the demonstration, and its price was high enough to justify building a receiver/processor for the demonstration system. Figure 3 shows the block diagram.



DECODER BLOCK DIAGRAM
FIGURE 3

The receiver is a commercially available VHF-FM, 6 channel, crystal controlled radio with an audio bandpass of 3kHz. The digital signal output to the processor is taken from the discriminator, filtered and hard clipped to form a digital data stream. The filter is AC coupled to the discriminator to prevent loading. Figure 4 is a schematic diagram of the clipper-filter circuit.

The processor is a software program implemented in an RCA CDP 1801 microprocessor. It performs radio frequency signal correlation, data decoding, message checking and information output for the display. Signal correlation is accomplished by sampling the digital data stream coming from the filter/clipper circuit in the discriminator at a rate that allows each bit to be sampled 8 times (sampling every 416 microseconds). The correlator uses any 8 successive samples to test for one information bit. If 8 successive samples contain the same binary value, the correlator passes an information bit of corresponding value through the data decode routine to the message checking routine.

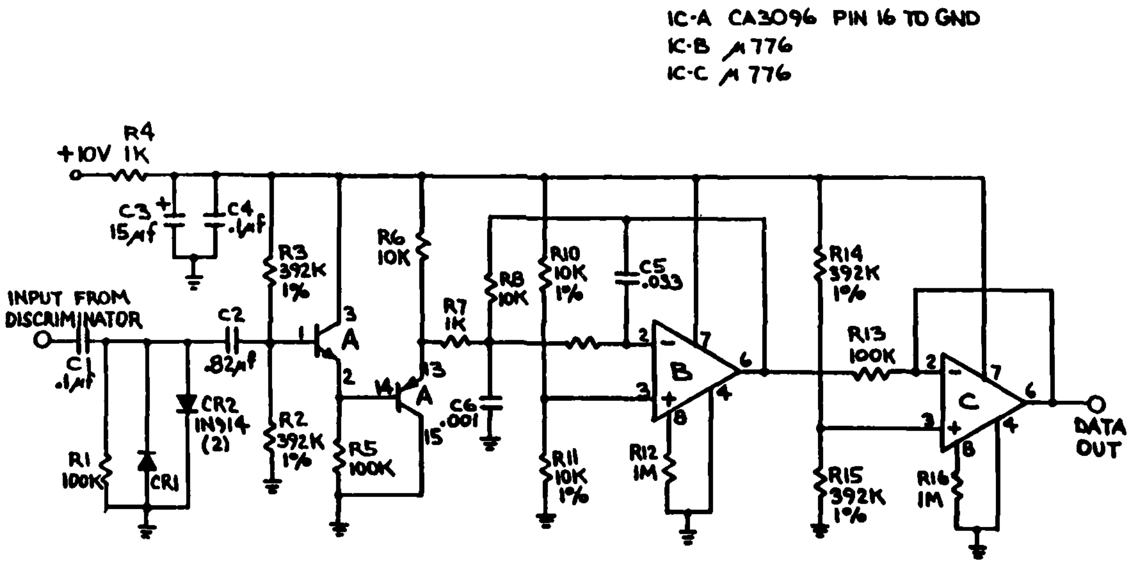
The data decode routine stores each information bit in an 8 bit register. If 8 consecutive "ZERO" bits occur, the routine recognizes them as a message preamble and calls the message routine.

The message routine shifts all bits following the preamble through the 8 bit register and processes the contents of the register to determine: (1) if the message is of normal length or of an optionally longer length and (2) if there is correct parity. A valid message is indicated when the register is initially filled with 8 "ZERO" bits. Message information is obtained by shifting all the message bits through the 8 bit register into an additional single bit register. A valid message contains a binary "one" bit immediately after the 8 "ZERO" bit preamble as a frame marker. When the "one" bit is shifted into the single bit register, the information can be read out of the 8 bit register. For the mangnetic sensor system, the identification number of an RF transmitter is the only information contained in the message.

A display routine operates using the transmitter identification number contained in the digital message. The value of the identification number can range from 0 to 63. The binary representation of the number, which is contained in the digital message is shifted into an output register by the message routine. The display routine outputs the binary number to a printer interface and energizes a lamp drive circuit corresponding to the transmitter identification number. Appendix A contains a more detailed description of the receiver/processor operation.

2.4 DISPLAY

The display consists of a 6 column printer and a number of LED indicator lights corresponding to each sensor location. A clock was interfaced to the printer so that a time annotation can be printed out along with the transmitter identification number.



CLIPPER-FILTER
FIGURE 4

3.0 INSTALLATION

This project involved two demonstrations, the first demonstration took place in Houston, TX in 1976. The second demonstration took place in Sault Ste. Marie, MI in 1978. Neither of the installations were exa tly alike due to the on-site environment.

3.1 HOUSTON INSTALLATION

The Houston-Galveston ship channel is aproximately 35 miles long. It averages 400 feet in width and has approximately a 40 foot depth. The sides and bottom of channel are mud. There is little, if no, current. The vessels that travel in the waterway range from pleasure craft to tugs with tows to large ocean-going ships. Because the sides and bottom are relatively soft, certain types of vessels can, and do, scrape the channel sides and bottom without fear of damage. In addition, the channel is constantly being dredged. The channel is lined with heavy industrial complexes along both sides. Appendix B contains a detailed description of the installation.

3.1.1 MAGNETIC SENSOR

The magnetic sensor packages were installed in a waterproof, aluminum (non-magnetic) housing, Figure 5. Although the sensors were unmodified, a

Figure 5 Magnetic Detector Housing

voltage regulator/output driver module was required to both reduce the supply voltage from the 36 VDC available to the 8.7 VDC required by the detector and to shape the sensor output pulse to match the RF transmitter trigger signal requirements. The sensors were deployed on the edge of the channel near aid to navigaiton towers. The weight of the aluminum housing caused the sensor to settle firmly into the mud, thereby preventing false alarms due to sensor movement. The orientation of the sensor in the housing caused the most sensitive axis of the magnetometer to be parallel to the plane of the channel and not directed toward the surface of the water where vessels would pass. This had no apparent effect due to the close detection ranges.

3.1.2 RADIO TRANSMITTER

The transmitter and encoder were housed in a cylindrical AN type metal shipping container measuring 10.5" in diameter by 42" high. The container also held a battery pack consisting of 25 Mallory mercuric oxide D size cells connected in series to provide 36 VDC, open circuit. Figure 6 shows the transmitter/encoder and the battery pack. The battery pack supplied power for both the transmitter and the magnetic sensor. A three conductor waterproof cable connected the sensor to the transmitter. The maximum tolerable cable resistance was 5,000 ohms. Figure 7 shows the transmitter container connected to the magnetic detector housing.

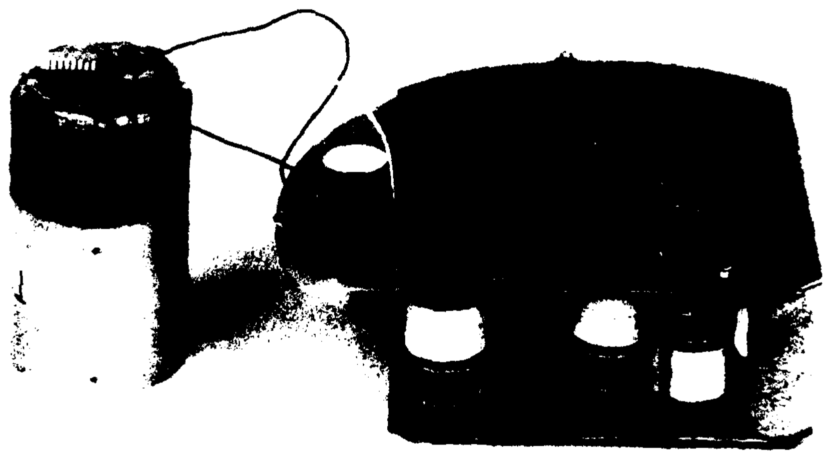


Figure 6 Transmitter/Encoder and Battery Pack

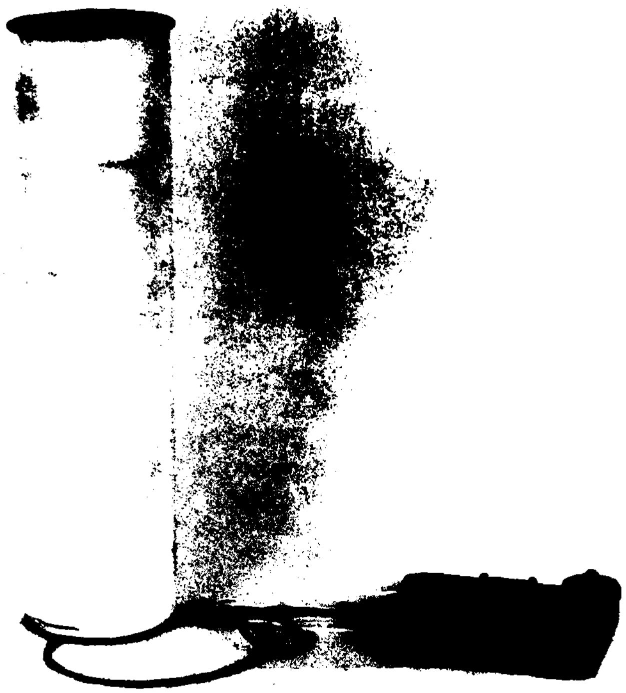
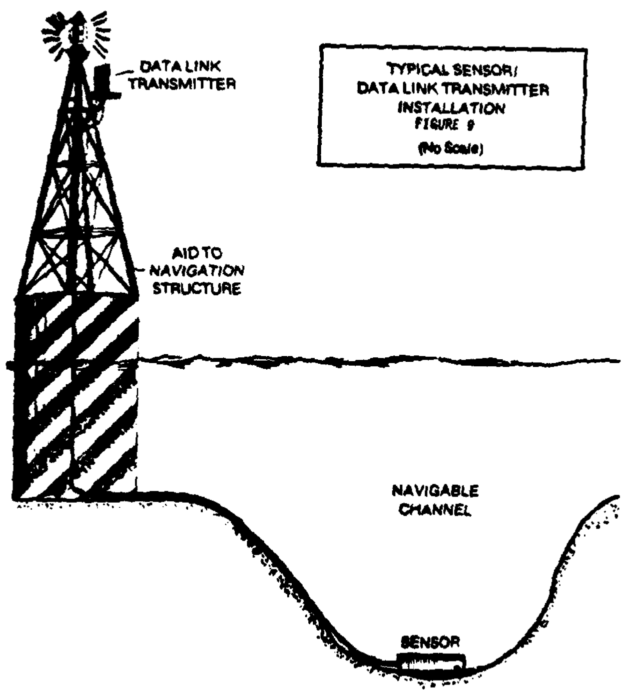


Figure 7
Transmitter and Detector Housing

A conformal patch antenna was attached to the outside of the metal container, Figure 8. The antenna was a magnetic microstrip dipole produced on a piece of copper clad teflon-fiberglass substrate 1/32" thick. It measured 12.25" high by 8.0" wide and was horizonally polarized. Antenna impedance was 50 ohms. At the 168.0625 MHz operating frequency, the VSWR was 1.5:1.

The transmitter assembly was installed on an aid-to-navigation tower by attaching the container to the tower platform safety railing. The transmitter identification number was set to correspond to the aid-to-navigation number. Six transmitters and sensors were deployed. Figure 9 depicts the concept of the sensor/transmitter deployment.

Figure 8 Conformal Patch Antenna



TYPICAL SENSOR/
DATA LINK TRANSMITTER
INSTALLATION
FIGURE 9
(No Scale)

3.1.3 RECEIVER/PROCESSOR

The receiver/processor was installed in the Vessel Traffic Center, located at the U. S. Coast Guard station in Galena Park, TX. The receiver/processor,the display printer and a digital clock were housed in a single metal cabinet, Figure 10. A corner reflecting receiving antenna with 10dB gain was installed on a 130 foot tower. The 16 nautical mile line of sight range provided by the tower was more than a' quate to accomodate the RF transmission path to the farthest transmitter which was 6 nautical miles away.

Figure 10 Receiver/Processor Cabinet

3.1.4 DISPLAY

The display consisted of the printer, installed as described above, and LED indicator lights located on the VTC plotting board.

3.2 ST. MARYS RIVER INSTALLATION

The St. Marys Rivers runs along the Canadian border of the upper pennin-sula of Lake Michigan. It is the single connection between Lake Huron and Lake Superior and carries a broad range of vessels from pleasure craft to ocean-going ships to iron ore carriers. The riverbed is rock and hard-pan.

The current ranges from 5 to 7 knots and is controlled from the St. Marys Falls to the river's mouth by a dam operated by the Army Corps of Engineers. The depth of the river is approximately 30 feet. Loaded ore carriers pass so close to the bottom that their propeller wash, at times, dislodges large rocks from the river bottom - some rocks are as large as a desk top.

3.2.1 MAGNETIC SENSOR

Initially, an attempt was made to deploy the magnetic sensors in the water, either in the channel or at the edge. To offset the effects of the current, the aluminum sensor housing was attached to an additional concrete weight. The total weight of the sensor package was too large for two men to handle, thus requiring the use of a boat with a lifting boom to deploy the sensors. The waterproof cable was also weighted. However, the cable was not weighted enough because the current moved the cable downstream, stressing it to a point where the cable connections at the sensor failed. Sensor deployement in the water was abandoned as being impractical for this particular demonstration.

An attempt was made to mount the existing detector housing out of the water. This was not successful.

Based on the premise that the best approach was to mount the sensor out of the water, a simple investigation of the operation of the sensing device was undertaken. This was accomplished by opening up a sensor package and observing the behavior of the detection circuit using an oscilloscope. A test set-up was established close to the river so that the reaction of the sensor to the stimulus of a passing ship could be observed. The test showed that the period of sensor stimulation lasted between 20 seconds and a minute, depending on the ship's speed. This indicated that a sensor bandpass of between 0.05 and 0.017 Hz was required for best operation. The bandpass of the magnetic sensor was 0.2 to 2.0 Hz. The sensor was modified to have a bandpass of 0.02 to 0.04 Hz. This modification improved the sensor operation.

Once the sensitivity of the sensor was improved, a high incidence of false alarms occured from sensors placed in areas near roads and where other nonrelated activity was on-going. This problem was also solved by observing sensor operation during the false alarms. The remedy implemented was to build a missing pulse detection circuit to replace the circuitry that prevented sensor transmitter trigger output faster than once every ten seconds. The design theory was that a real target would cause a continuous string of output pulses over the period of time it was passing the sensor. The false alarm stimulus would be of short duration. Therefore, a circuit that required a consistent train of pulses for a given period of time could be made to discriminate against stimuli of shorter duration. This modification eliminated approximately 95% of the false alarms.

The modified sensor and the anti-false alarm circuit were mounted in the RF transmitter housing. Maximum range of the sensor was observed to be 600 feet for a large, ore carrying vessel traveling 3 to 5 knots.

3.2.2 RF TRANSMITTER

The RF transmitter was repackaged to be contained in a stainless steel box measuring 20"X16"X6". The transmitter, battery, sensor and anti-false alarm circuit were mounted on a flat metal plate that was attached to metal stand-offs inside the box. A conformal patch antenna was attached to the lid of the box. A lithium sulfur dioxide battery replaced the mercuric oxide battery pack. The transmitter operating fr-quency was 171.3625 MHz.

3.2.3 RECEIVER/PROCESSOR

The receiver processor was installed in the Vessel Traffic Center located at the U. S. Coast Guard Base in Sault Ste. Marie, MI. The receiver/processor, the printer and the digital clock were contained in an electrical cabinet that was mounted in the 19" rack of a standard console arrangement. A yagi antenna mounted on a 85 foot pole, served as the receiving antenna. Appendix C contains a description of the receiver/processor software.

3.2.4 DISPLAY

The display consisted of the printer installed as described above and a straight line representating of the St. Marys River drawn on the face of the cabinet. LED indicator lights mounted on the representation showed the position of activated sensors, on the map.

4.0 OPERATIONS

4.1 INTRODUCTION

The Vessel Traffic Services (VTS) at both Houston and Sault Ste. Marie operated in a similar manner. Each service maintained a position plot of participating vessels by dead reckoning using strategically designated checkpoints to obtain vessel position and verify the plot. VTS Houston maintains a plot that is continuously updated. VTS Sault Ste. Marie only updates their plot when ships report at the checkpoints. The plot at Houston is maintained on a representation of the ship channel; cards, representing vessels, are advanced along a plotting board to simulate vessels proceeding in the channel. At Sault Ste. Marie, the plot is kept in a log which contains the time vessels reported passing the designated checkpoints. Both VTS service areas contain sections of waterway where two-way traffic is allowed and sectons where only one-way traffic is allowed. For the most part, passing due to one participating vessel overtaking another does not occur.

4.2 DEMONSTRATION

The demonstrations attempted to integrate the sensor system into regular operations. This attempt was not very successful. In Houston, there was three major problems:

(a) Passing vessels hit two of the six sensors and destroyed them.

(b) The false alarm rate was high enough to substantially reduce VTS watchstander confidence.

(c) The lack of positive identification of the vessel triggering the sensor eliminated any benefit to the VTS watchstander, especially in sections of waterway where two-way traffic existed.

In Sault Ste. Marie, the major problem was the lack of positive identification of the vessel triggering the sensor.

5.0 CONCLUSIONS

5.1 GENERAL

The unanimous conclusion among the VTS personnel who used the system was that, as implemented, it provided little or no benefit to VTS operations. Two major shortcomings were readily apparent:

(a) The lack of positive identification of vessels

(b) The lack of operator confidence due to false alarms.

It was suggested that such a sensor system would have application as a perimeter monitor whereby the sensor would alert a watchstander to the presence of a vessel in some sector of a service area. The watchstander could then use some other surveillance technique to gather any required information.

With regard to passive sensors in general, this project points out the fact that they cannot be selected at random for use in VTS operations. Unlike radar, which is a sensor whose operating characteristics are fairly well understood, passive sensors have a wide variety of operating parameters. Passive sensors appear to require a specific design effort to meet the needs of each desired application. Information obtained about other sensors, which respond to acoustic, electrostatic, infra-red and seismic stimuli, indicates that any applications engineering effort begins with an analysis of the environment in which the sensor must function. Such an analysis includes identifying both the stimulus signature of the object to be detected and character of the ambient noise in the area of operation. The analysis must provide sensor sensitivity and bandwidth requirements and indicate any additional requirements for signal processing to allow for both the required level of object identification and noise discrimination.

5.2 MINIMUM REQUIREMENTS FOR FUTURE EFFORTS

The results of the demonstration project indicate that any future passive sensor development systems meet the following minimum requirements:

(a) Provide a means of identifying the vessel that triggered the sensor. This is necessary both to resolve any ambiguities caused by vessels travelling in opposite directions and to identify vessels that are non-participants. It also provides additional discrimination against false alarms.

(b) Provide a means to discriminate against ambient noise. This is necessary to either eliminate false alarms or to reduce them to a level that is acceptable to a VTS watchstander.

(c) Allow for easy sensor deployment. It is apparent that deployment in a shipping channel will not work in every situation. Deployment by attachment to an aid to navigation structure or some other shore point appears to a much better approach. Deployment out of the water and either on or near shore has the dual benefit of easy initial installation and easy accessibility for maintenance.

APPENDIX A

RECEIVER/DECODER OPERATION

GENERAL OPERATION

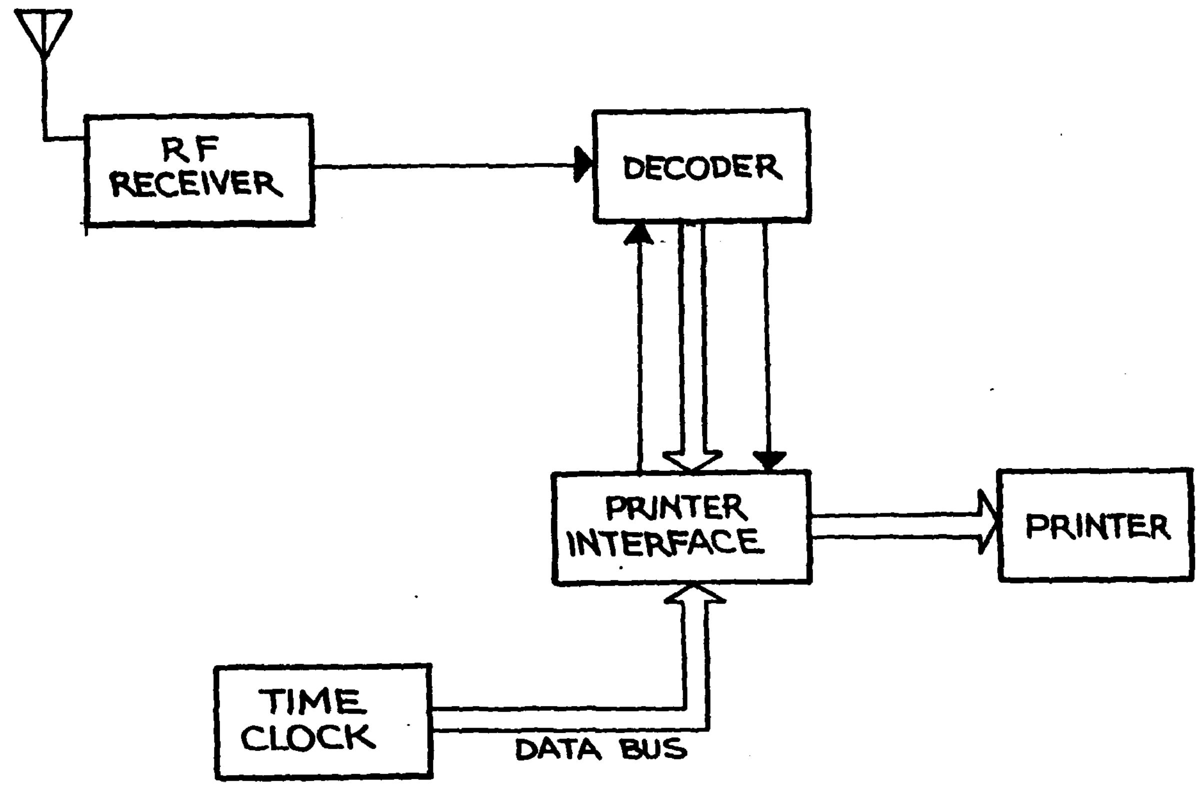
This system is comprised of three major sections: (1) a VHF-FM receiver, (2) decoder, and (3) time clock and printer. The block diagram of the system is shown in Figure 1.

The receiver, printer and time clock are commercially available pieces of equipment. The decoder consists of a signal clipper and correlator, a microprocessor, memory and control logic for the processor, and output display logic and LED drivers. A block diagram of the decoder is shown in Figure 2.

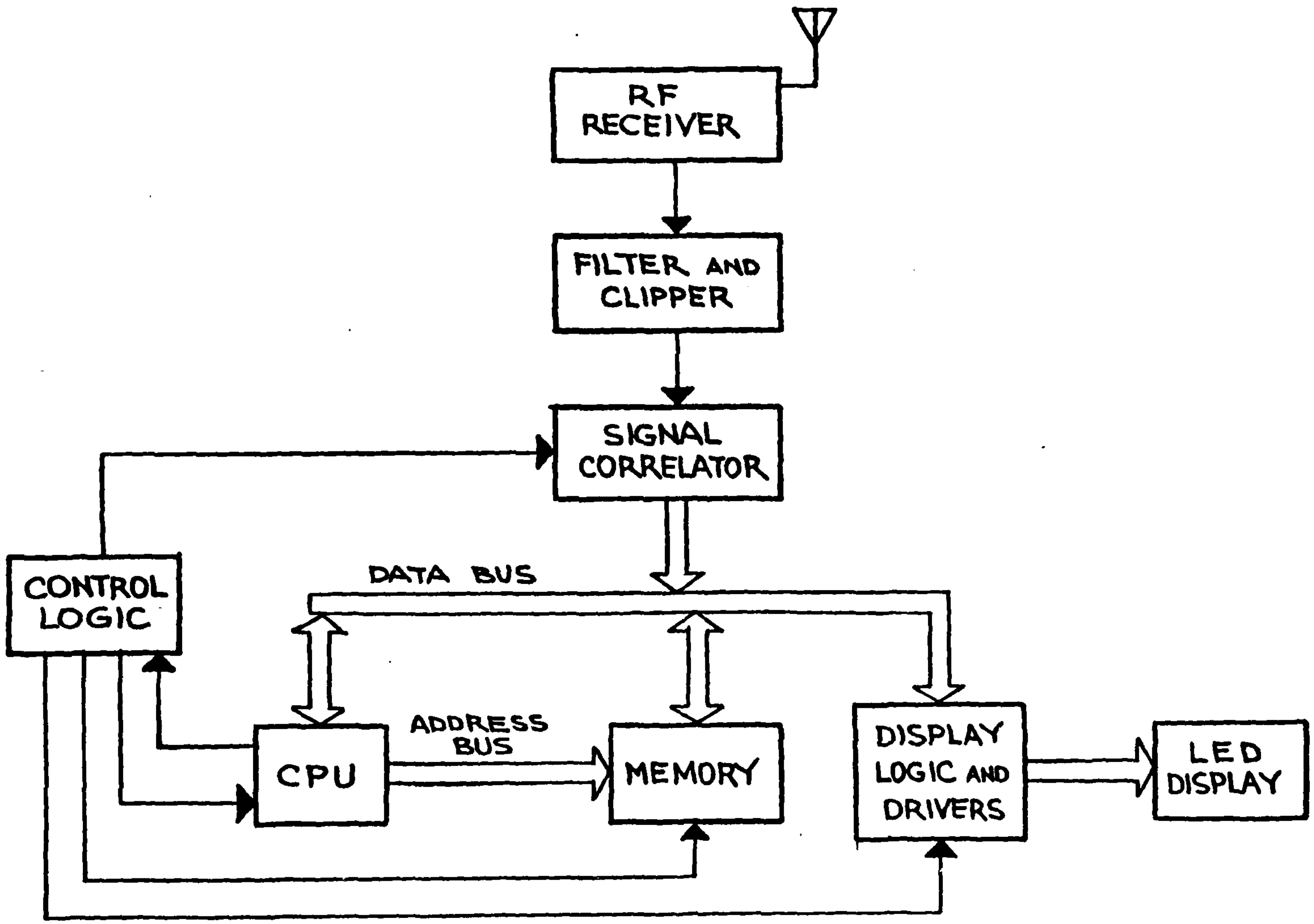
This unit was designed to be used in lieu of the USQ-46A Portatale Receiver in certain applications to detect and decode Phase III type RF messages. The Phase III RF link is a FSK 300 Hz biphase coded message. The Phase III RF transmission message format is shown in Figure 3. The decoder's software could be modified to decode any 300 Hz biphase coded message.

The receiver is a VHF-FM 6-channel crystal controlled radio. The discriminator output of the receiver is filtered and hard clipped into digital information to be sampled by the signal correlator.

The signal correlator compares the incoming digital data stream with a known digital data pattern (in this case a biphase zero) and calculates a value that indicates how much the incoming data represents the known data pattern. From this information, the microprocessor can determine if the signal is random noise or a valid transmitted message.



SYSTEM BLOCK DIAGRAM
FIGURE 1



DECODER BLOCK DIAGRAM
FIGURE 2

PHASE III RF TRANSMISSION MESSAGE FORMAT

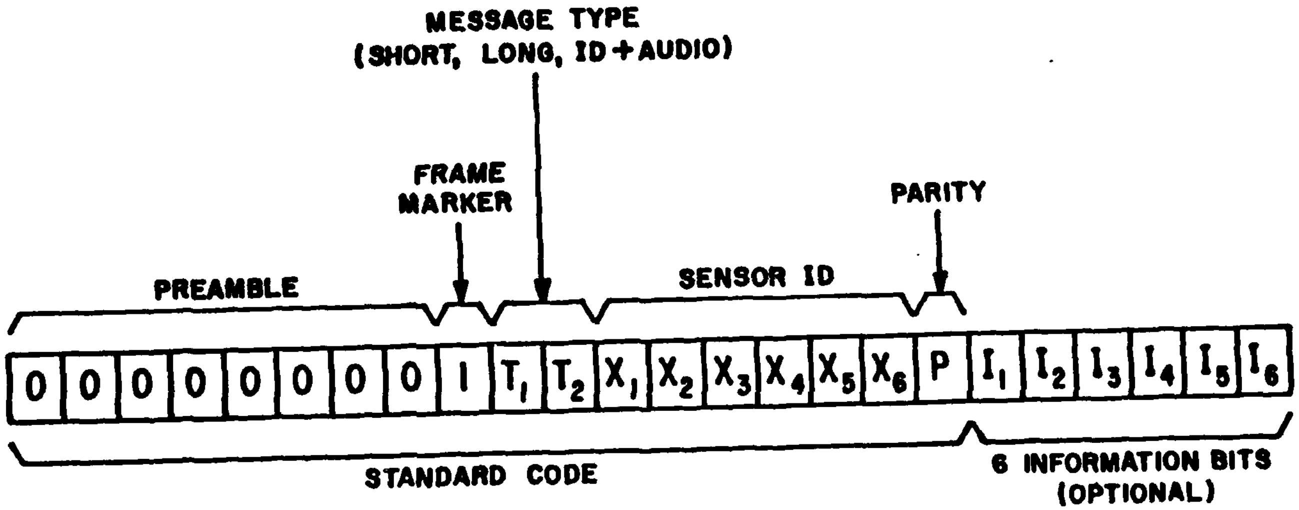


FIGURE 3

The central processing unit (CPU) is the RCA CDP 1801 microprocessor. The CPU performs the biphase data decoding, validity testing of received messages and information formatting for the LED display and printer.

When a transmitted message is received, the processor decodes the ID number associated with the message. The ID number and the time the message was received is printed and the corresponding display panel ID light is illuminated.

Decoder Circuit Description

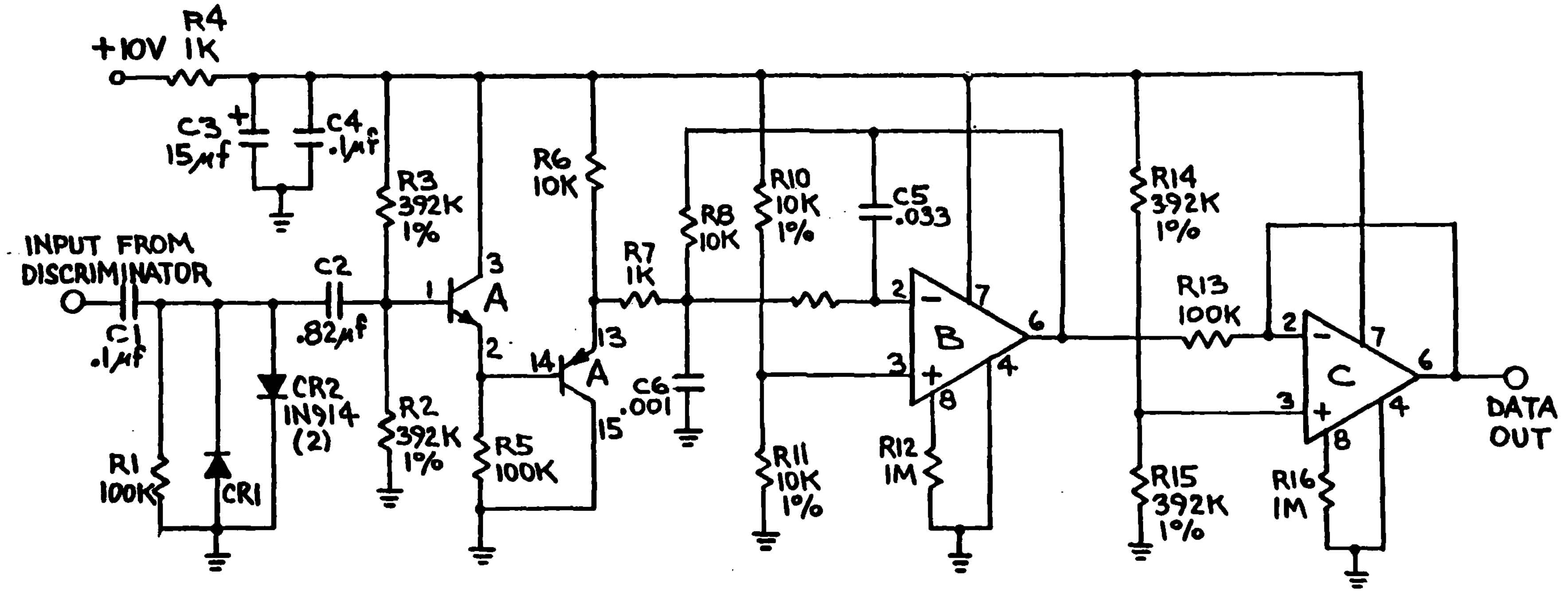
Filter-clipper. The discriminator output of the receiver is ac coupled to the filter to prevent loading. The signal, nominally one volt peak-to-peak, is passed through a 300 Hz, 2-pole, low pass filter with 20 dB of gain. Then the signal is hard clipped.

The schematic of the filter-clipper is shown in Figure 4. The first two transistors (IC-1) are used to buffer the signal from a ground reference to the +5 volt reference of the op-amps. The first op-amp (IC-2) amplifies and filters the signal and the second op-amp (IC-3) clips the filtered signal.

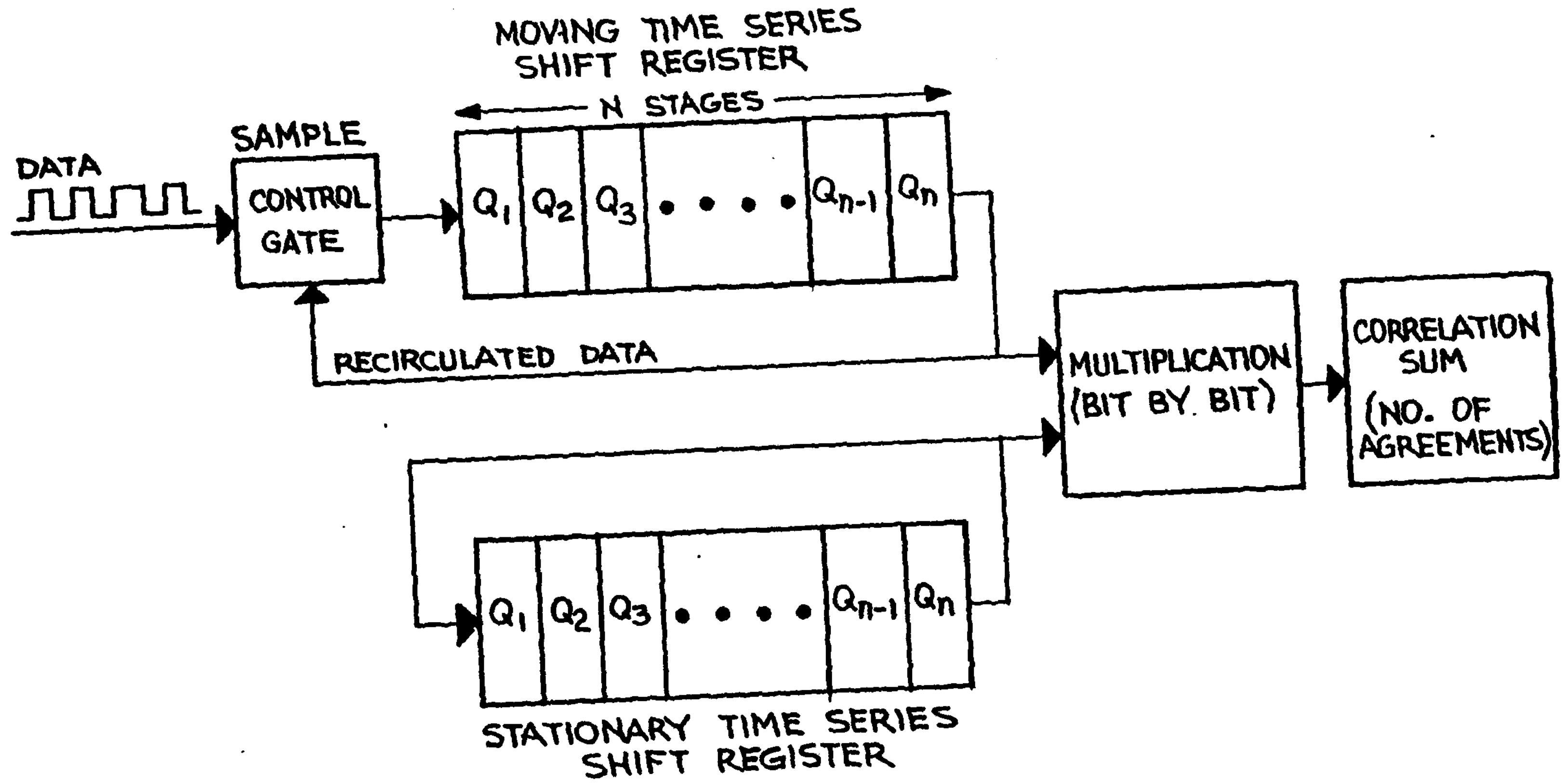
Signal Correlator. Signal correlation is a process in which two time functions are operated on to calculate a correlation sum. One method of doing this is a Delay Time Compressed (DELTIC) correlator. The DELTIC correlator stores a time compressed representation of the digital data in a serial memory, referred to as a Moving Time Series (MTS) shift register. The correlator compares the contents of this memory to the contents of the Stationary Time Series (STS) shift register, each sample period. Figure 5 shows a block diagram of the DELTIC correlator.

The contents of the MTS and STS shift register are recirculated during each sample period. By observing the outputs of the registers during this recirculation, a correlation sum can be calculated each sample period.

IC-A CA3096 PIN 16 TO GND
IC-B μ776
IC-C μ776



CLIPPER-FILTER
FIGURE 4



DELAY TIME COMPRESSION (DELTIC)
CORRELATOR
FIGURE 5

The length (N) of the serial memory is equal to the number of samples per data bit (level of quantization) necessary to extract the transmitted data from noise.

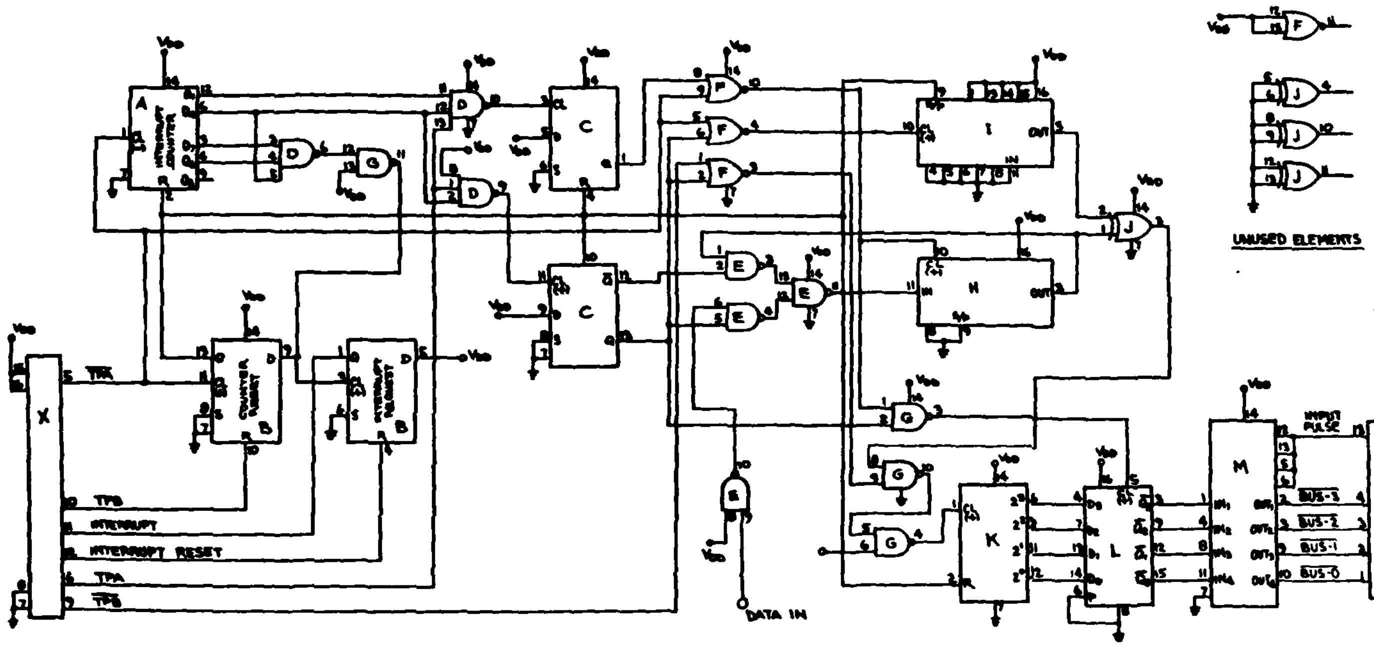
The sampling rate of the correlator is a function of the frequency of the data to be correlated and a function of the level of quantization (Q) that is required. The maximum frequency of the Phase III message being decoded is 300 Hz.

For this application, a quantization level of eight is sufficient to obtain enough information to decode an incoming message. The sampling rate (T_{SR}) = Q/signal period.

T_{SR} = 8/(1/300 Hz) or 416 microseconds. The timing pulses of the microprocessor, TPA and TPB, are counted for this time base. At each sampling period (every 416 microseconds) a correlation sum is calculated and the processor is interrupted to process the new sum.

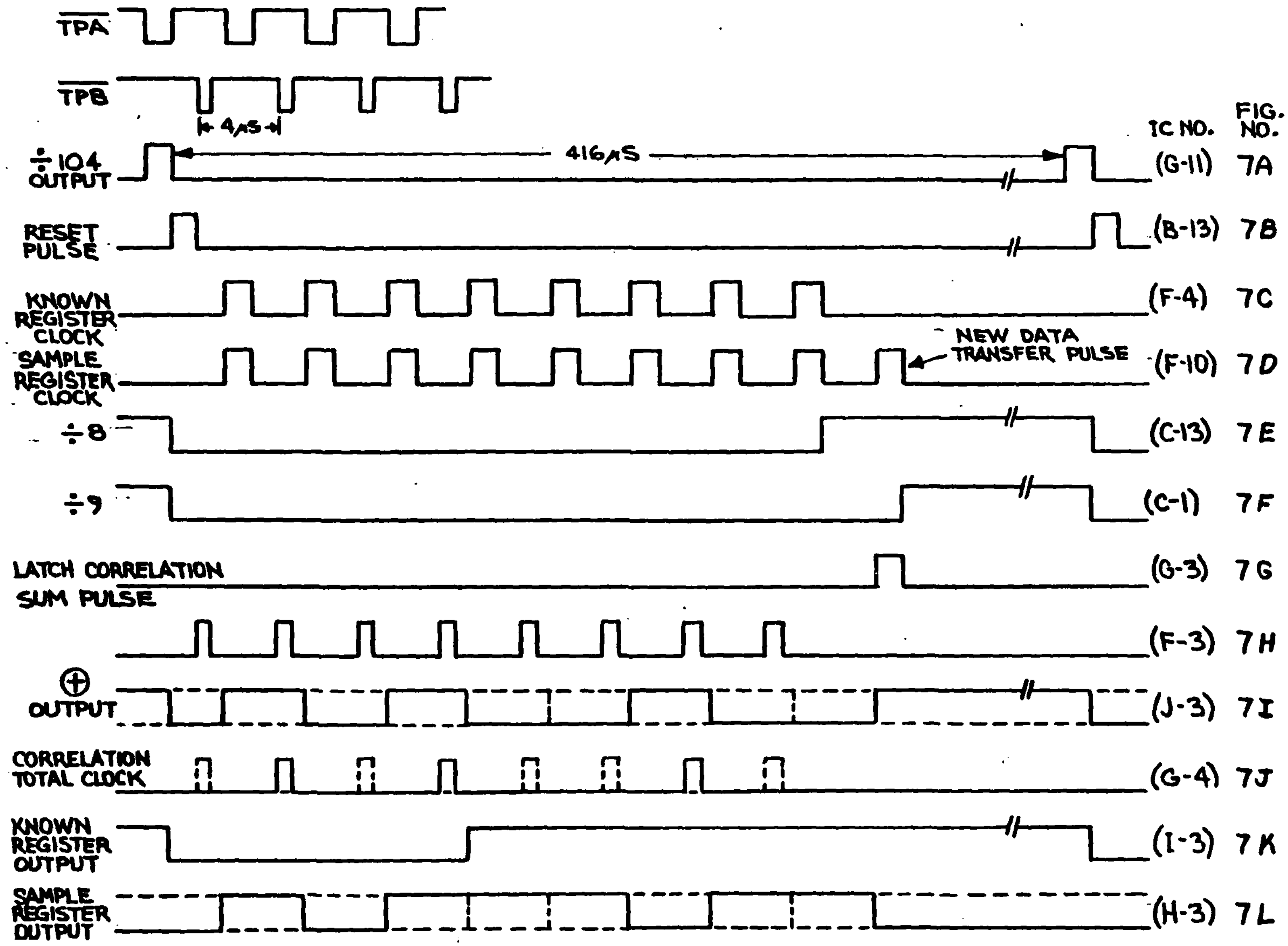
The schematic of the DELTIC correlator is shown in Figure 6. At the beginning of every sample period all counters are set to zero by the reset pulse, Figure 7. The first eight clock pulses of the known and sample shift register clocks (Fig 7) after the reset are used to shift the two data registers of the correlator. The ninth pulse of the sample register clock is used to transfer a new data sample into the sample data register (IC-H).

The data in the MTS shift register is circulated from the output to the input so that after eight clock pulses the register contains the same information it did at the start of the cycle. The ninth pulse stores a new sample bit in the first register location, shifting the other bits down one position, and causing the oldest sample bit to be lost. Therefore, every eight samples (3.3 msec) there is a completely new time compressed replica of the signal in the MTS shift register.



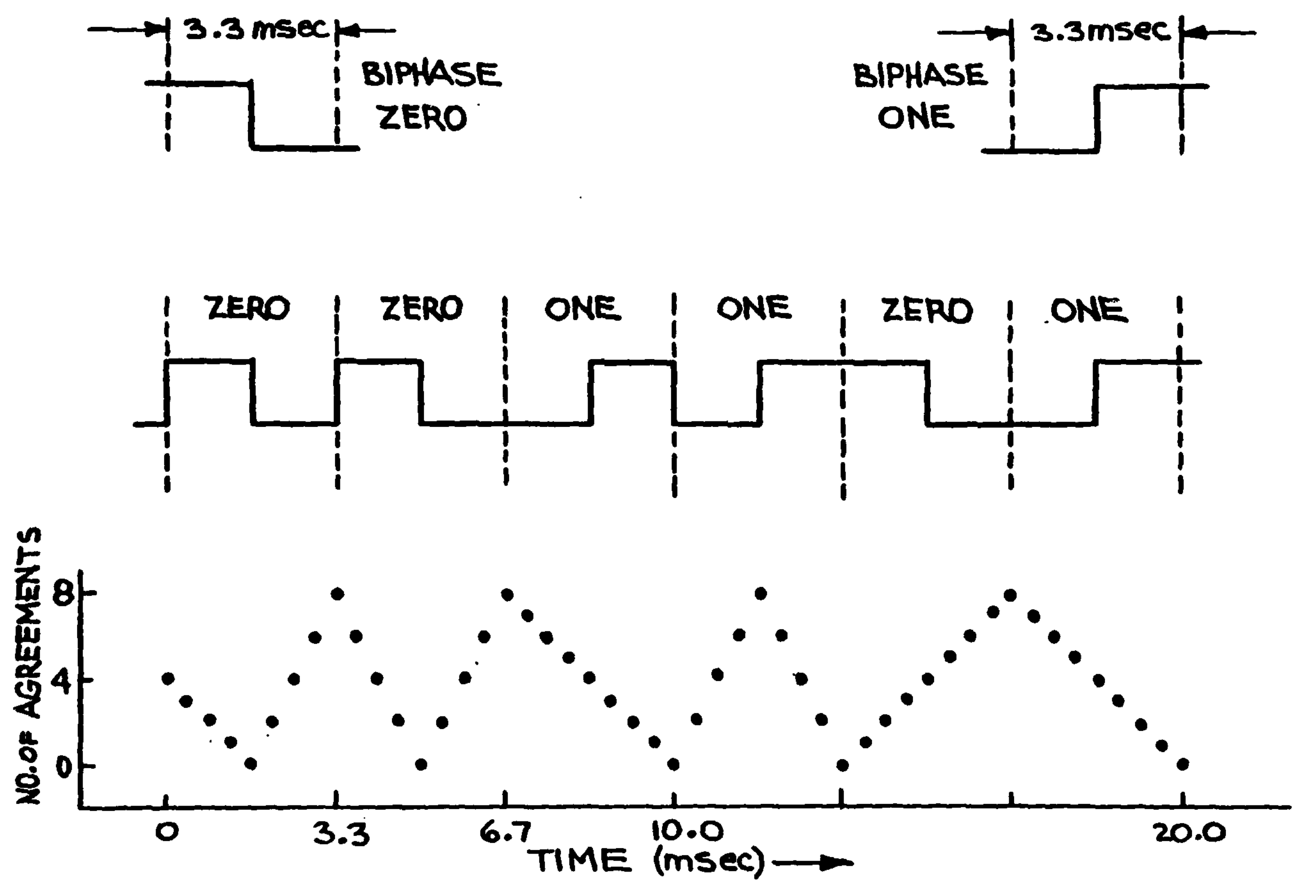
IC-A CD4024A
IC-B CD4013A
IC-C CD4013A
IC-D CD4023A
IC-E CD4011A
IC-F CD4001A
IC-G CD4011A
IC-H CD4021A
IC-I CD4021A
IC-J CD4030A
IC-K CD4024A
IC-L CD4042A
IC-M CD4016A
X 16 PIN DIP USED AS A CONNECTOR

INTERRUPT CONTROL & DELTIC CORRELATOR
FIGURE 6

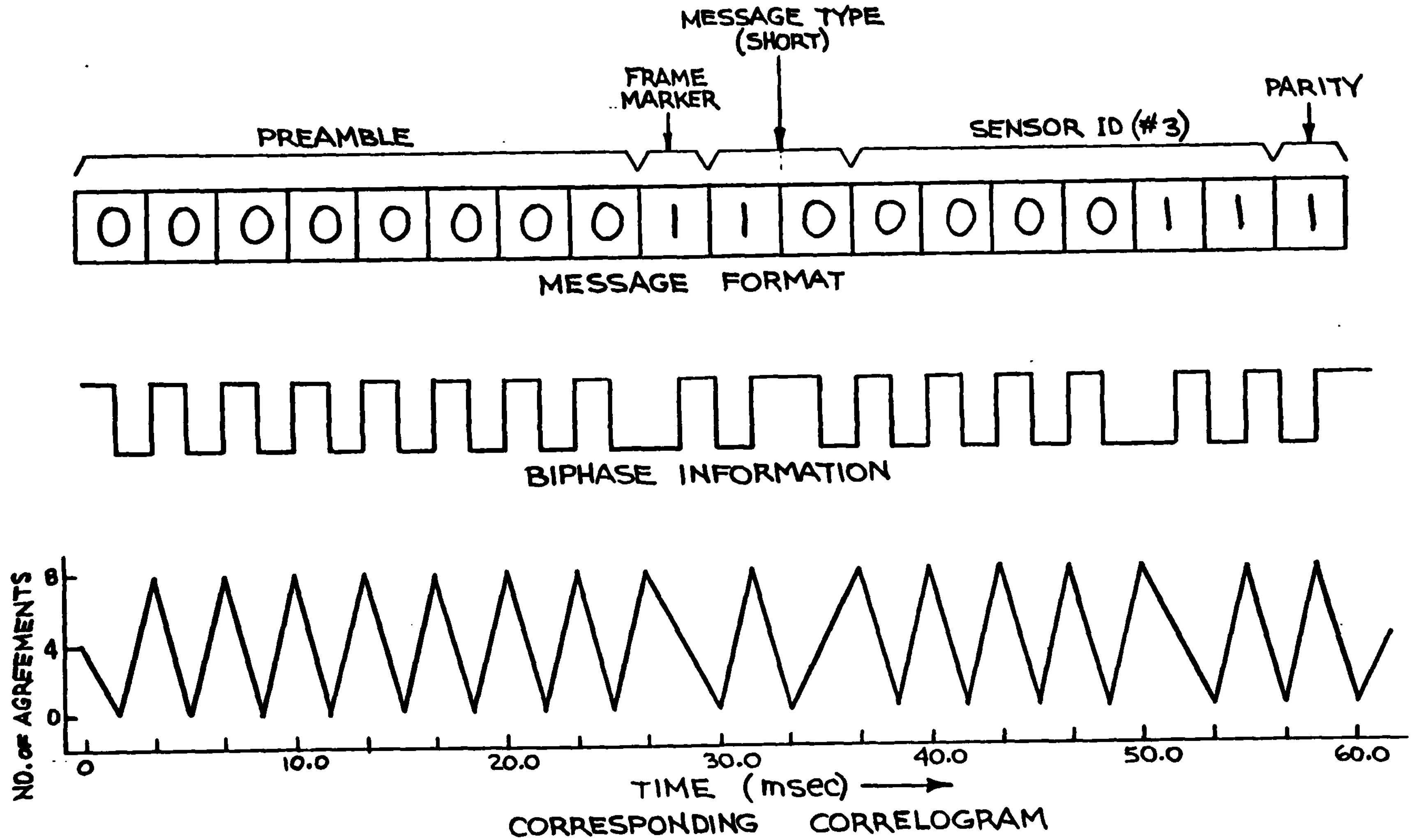


DELTIC CORRELATOR TIMING DIAGRAM

FIGURE 7



BIPHASE INFORMATION AND CORRELOGRAM
FIGURE 8A



SAMPLE MESSAGE

FIGURE 8B

At the start of the sample cycle, the biphase zero pattern is jammed into the STS shift register (IC-1) to be compared bit by bit to the MTS shift register.

The MTS shift register and STS shift register are multiplied and summed to calculate a correlation total for the sample period. In Figure 7 this is demonstrated by performing the exclusive or function on the known and sample register outputs. The correlation counter (IC-K) counts the number of correlation total clock pulses (Fig 7) and this sum is stored in a set of latches (IC-L) by the latch correlation sum pulse. The microprocessor can interrogate this sum when it is ready. A sum of zero is 100% correlation and eight would be 0% correlation. (0% correlation is interpreted as a binary zero and 100% correlation is a binary one.)

Figures 8A and 8B show examples of the biphase message format with the corresponding correlograms. This format is what is decoded into binary ones and zeros by the processor with the aid of the DELTIC correlator. Since a biphase one is of opposite polarity of a biphase zero, only one pattern must be recognized to distinguish both the one and the zero.

CPU Hardware. A microprocessor is used as the controller for the output display, output printer, and decoding the correlated biphase message information. The hardware needed to control the microprocessor is discussed in this section.

The processor hardware can be sectioned into three parts: (1) CPU, (2) memory, and (3) control logic.

The CPU is the RCA CDP 1801 CMOS microprocessor (COSMAC). Detailed explanation of this microprocessor can be obtained by reading RCA's literature on the 1801.

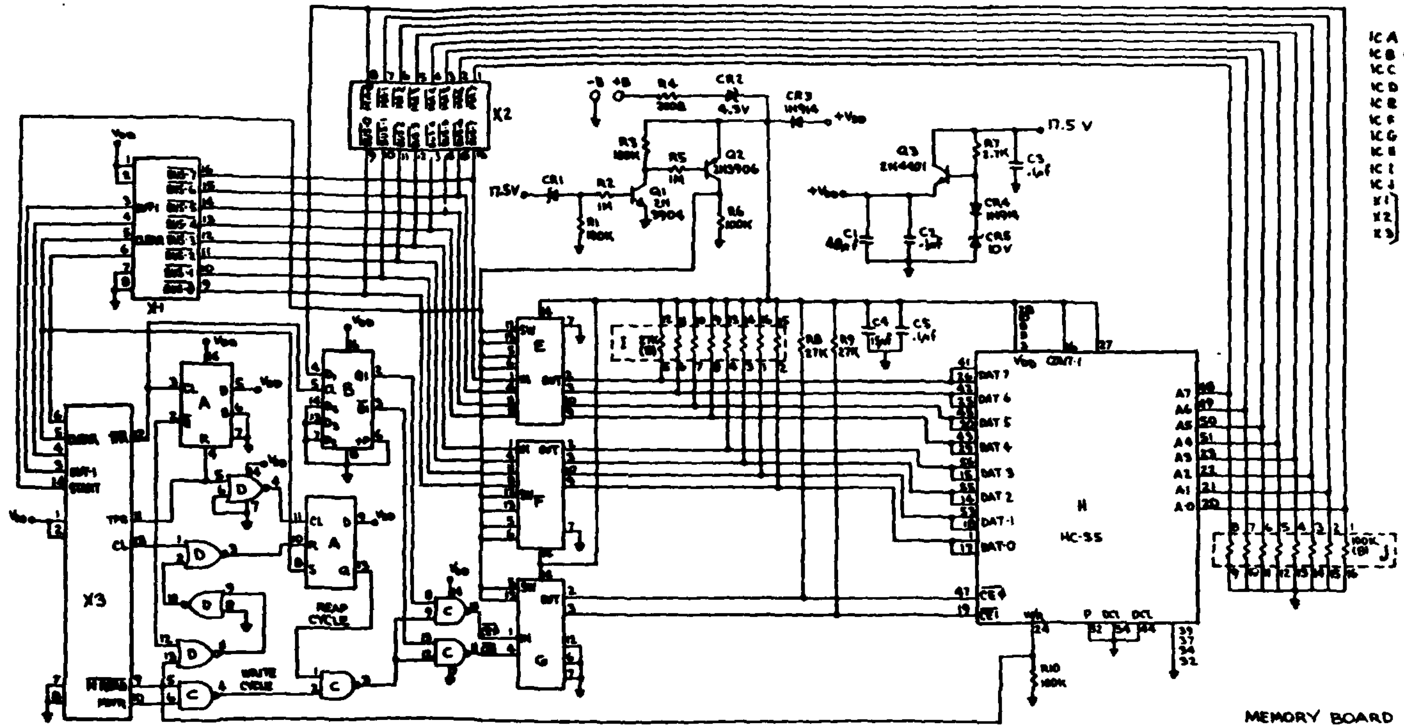
The memory is the HC-55, a hybrid package fabricated at the White Oak Laboratory. The HC-55 is a 512x8 bit array with the RCA CD4061AH static random-access memory (RAM) chips the basic building block. The memory board schematic is shown in Figure 9.

The memory is a non-volatile RAM by using a keep-alive battery. In this respect, the RAM functions both as the ROM and RAM for the system. To keep the memory alive, it is isolated from the rest of the system with switches (IC-E,F,G) in the bus lines and memory enable lines when power is lost. These isolation switches are controlled by a voltage level sensing switch (transistors Q1, Q2 and Zener CR1). This level sensing switch is to ensure that the memory will not be enabled during turn on and turn off transients.

The memory timing restrictions require some interfacing logic between the HC-55 memory and the COSMAC processor. The upper byte of the memory address is multiplexed on the address buss by COSMAC and latched by the $\overline{\text{TPA}}$ pulse (IC-B). Only $\overline{\text{MA0}}$ is latched in this case. The memory is enabled one clock cycle after $\overline{\text{TPA}}$ for a read cycle and enabled during the MWR (COSMAC created) pulse for a write cycle. The rising edge of $\overline{\text{TPB}}$ is used to disable the memory after each read cycle. $\overline{\text{CE}\emptyset}$ enables the lower half of the memory (bytes 0-255) and $\overline{\text{CE1}}$ enables the upper half of memory (bytes 256-511). The memory timing diagrams are shown in Figure 10.

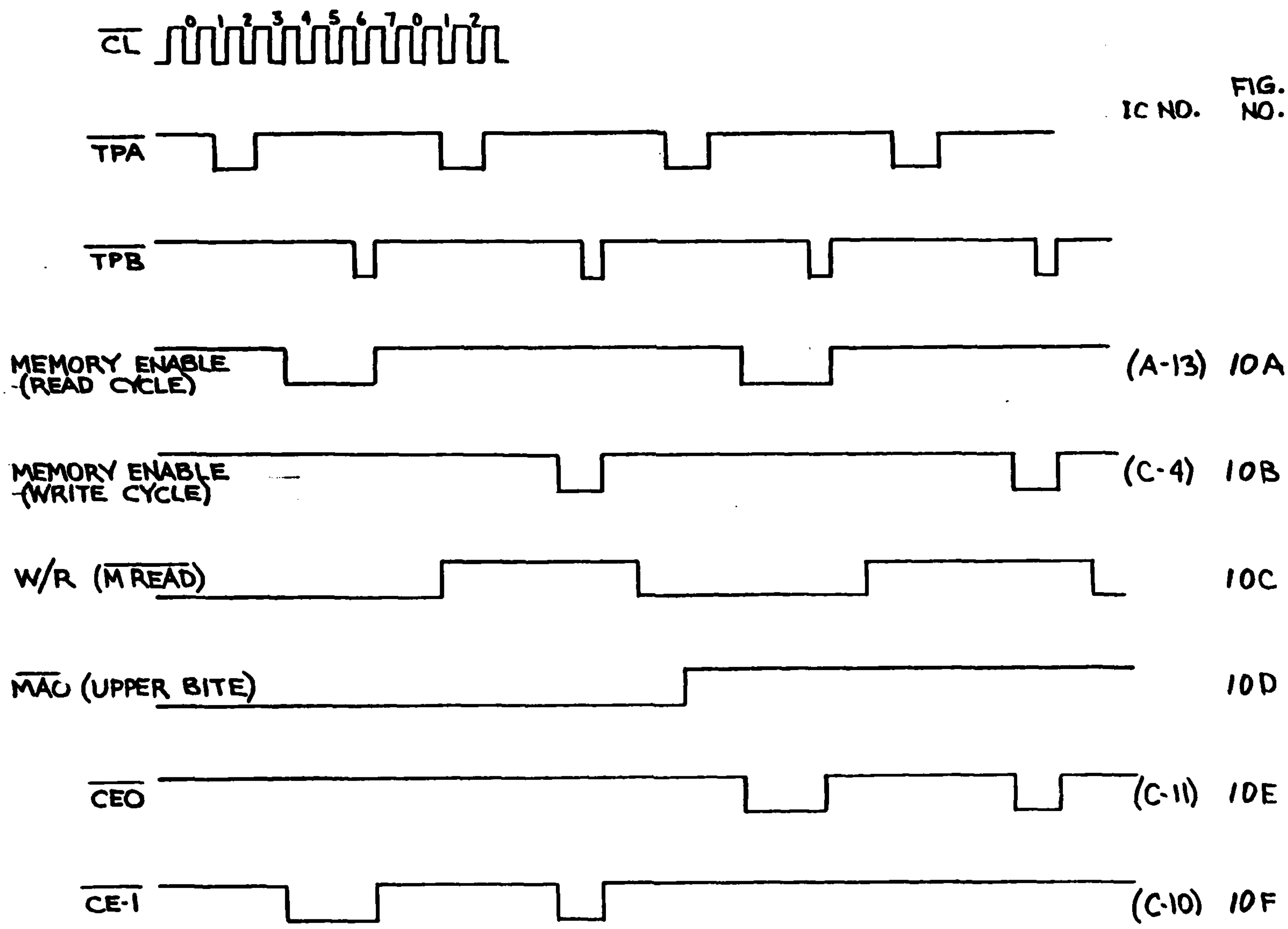
Control logic consists of start up, interrupt, and input-output control for the processor. The circuit diagram of the CPU board is shown in Figure 11. Figure 12 shows the timing diagrams of the CPU control.

At power turn on, a clear pulse is generated to clear the CPU (IC-A,B) and initialize the output data register IC-A of Figure 13. At the end of the clear pulse, an interrupt inhibit

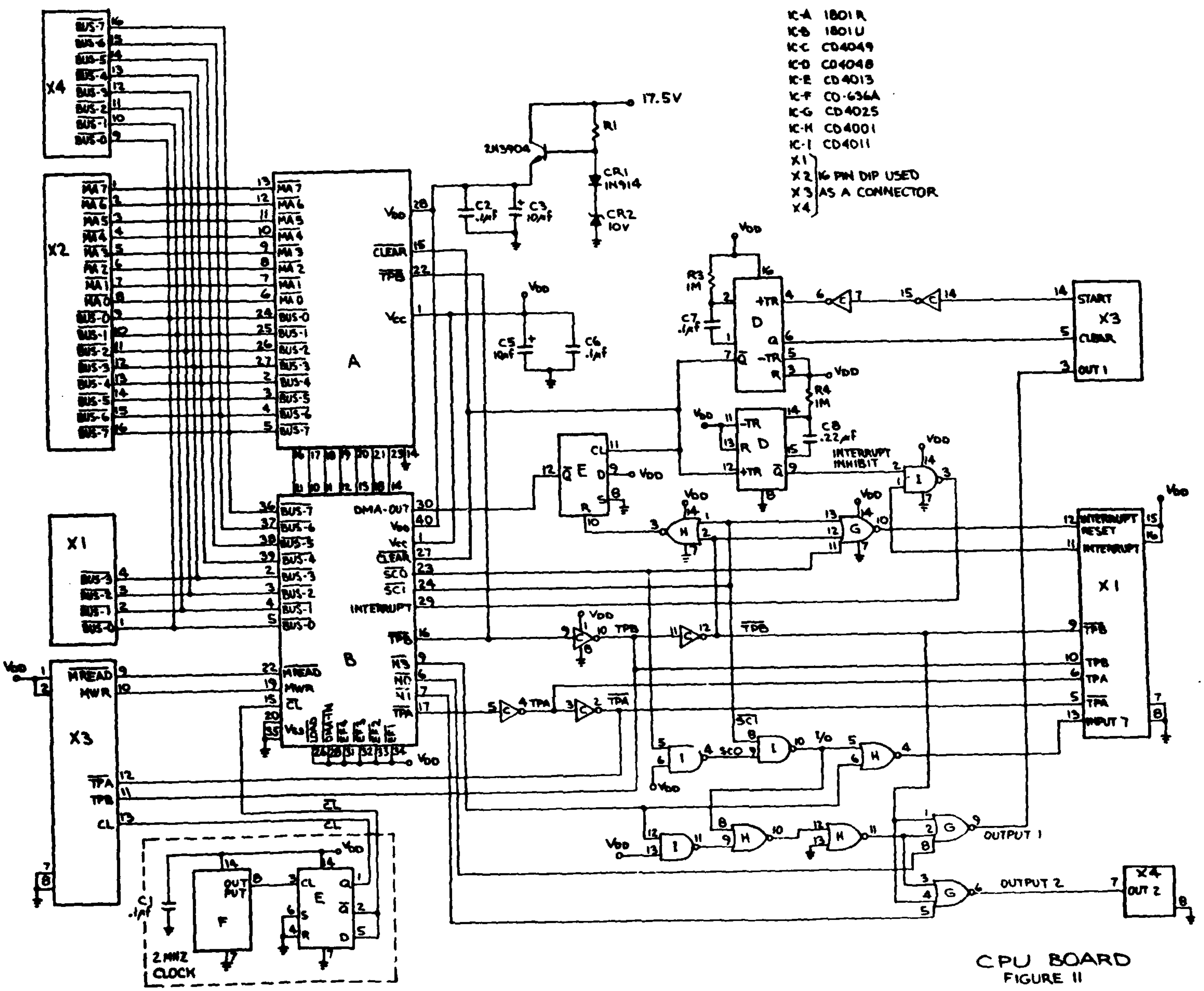


IC A CD4013
IC B CD4042
IC C CD4011
IC D CD4001
IC E CD4016
IC F CD4016
IC G CD4016
IC H 56 PIN HYBRID
IC I 16 PIN RESISTOR PACK
IC J 16 PIN RESISTOR PACK
X1, X2, X3: 16 PIN DIPS USED AS A CONNECTOR

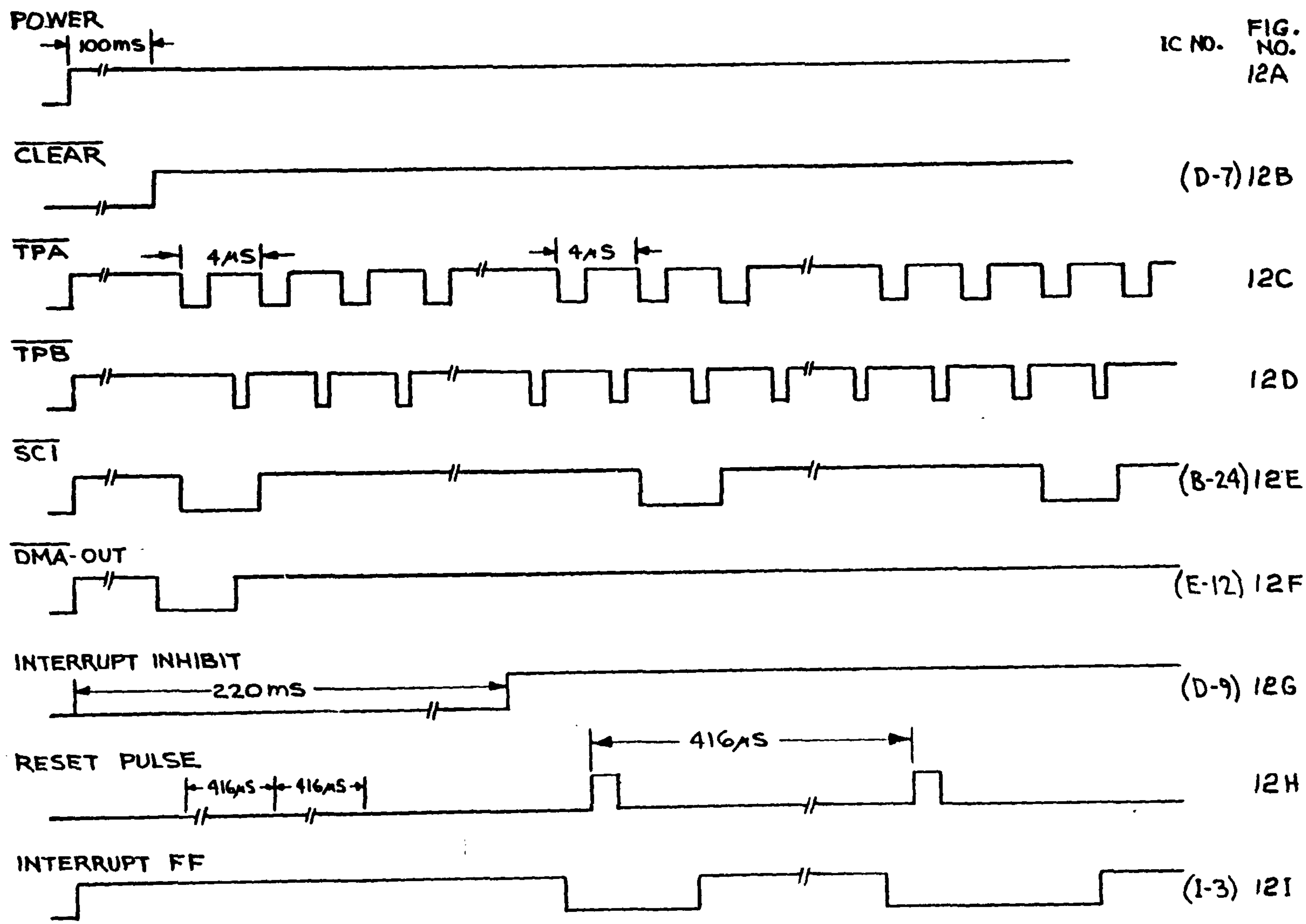
MEMORY BOARD
FIGURE 9



MEMORY TIMING DIAGRAMS
FIGURE 10



CPU BOARD
FIGURE 11



CPU CONTROL START SEQUENCE AND INTERRUPT
FIGURE 12

pulse is created to prevent interrupts during COSMAC register initialization. Also a DMA-OUT request is initiated to get the processor out of the IDLE state that the clear pulse puts it in. The DMA-OUT request flip-flop is reset as soon as the request has been operated on by the processor.

Interrupt control is performed by the same counter that controls the DELTIC correlator, IC-A of Figure 6. Every 416 usec, the interrupt request FF, IC-B1 of Figure 6 is set for an interrupt. Within the next eight usec (two machine cycles), the interrupt request is serviced by the processor, indicated by $\overline{SC1}$ and the request FF is reset.

Input-output control consists of decoding the state code ($\overline{SC0}$ and $\overline{SC1}$) and I/O lines ($\overline{N0}$-$\overline{N3}$) of the processor to determine if the instruction is an input or output command, and if it is, which input or output instruction it is.

When the processor is ready to read the correlation sum (an INPUT instruction), the input line (IC-H4) enables the tristate buffers IC-M of Figure 6. This allows the new sum in the correlation counter latch to be transferred to memory by the input instruction.

The two output instructions used, OUT 1 and OUT 2, control the output display and printer. During the output command, the processor puts an 8-bit word on the bus line and clocks the information into the appropriate latch; OUT 1 clocks the byte into the output data register and OUT 2 clocks the binary information into the printer interface latch.

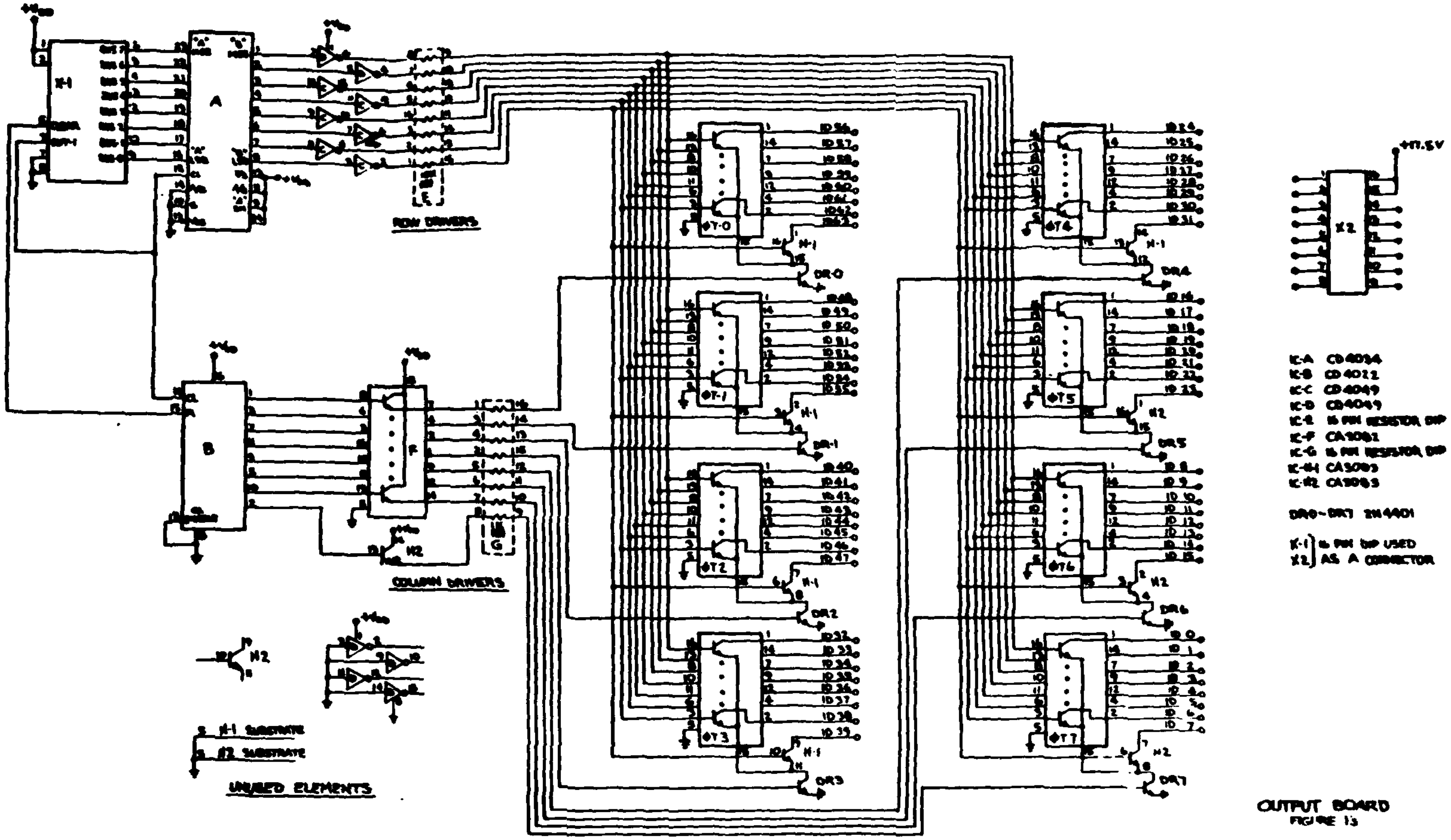
<u>Output Display</u>. The output display consists of LED drivers and multiplexing circuitry for the display LED's. There can be a total of 64 LED's that correspond to as many ID numbers. The

display is divided into an eight by eight matrix with the columns multiplexed on and off as the row information is changed accordingly. The schematic of the output board is shown in Figure 13.

The row information is clocked into the output row data register (IC-A) with the OUT 1 instruction. Each bit of the 8-bit word corresponds to one ID number. If the bit is a zero, the LED is on; if the bit is a one, the LED is off. IC's C and D of Figure 13 are the transistors for the LED row drivers (IC-ØTO,...ØT7).

The LED column drivers (transistors DRO...DR7) are enabled by the 8-bit column counter (IC-B) that is advanced one count with the same clock pulse that latches the row information. At each clock pulse (an OUT 1 instruction), one column driver (IC-F) is enabled, which supplies a ground path (through the LED column driver) for that row of LED row drivers. At the next clock pulse, new information is dumped into the row register and the column is advanced one column. When the counter reaches the count of eight, it is reset to one on the next clock pulse and then cycles through all eight columns again.

The clear pulse at system turn on sets the column counter to the first column for column and row synchronization. The duty cycle of the display LED output is 12.5% and the repetition rate is approximately 200 Hz (determined by software).



OUTPUT BOARD
FIGURE 13

FIGURE 14

PROGRAM
ASSEMBLY
LANGUAGE
LISTING

```
FL LOC  COSMAC CODE        SOURCE LINE
   0000                    ..DISPLAY PROGRAM CONTROLS OUTPUT DISPLAY
   0000                    ..MESSAGE PROGRAM FORMATS  AND CHECKS DECODED
   0000                    ..    MESSAGE FOR PROPER  INFORMATION
   0000                    ..INTERRUPT PROGRAM DECODES CORRELATED INCOMING
   0000                    ..   BIPHASE INFORMATION INTO BINARY INFORMATION
   0000                    ...
   0000                    ..PROGRAM ALLOCATES REGISTERS AND MEMORY
   0000                    ..  LOCATIONS AS FOLLOWS:
   0000                    ...
   0000                    ..R0: 00->0AF   DISPLAY PROGRAM POINTER
   0000                    ..R1:170->1FF   INTERRUPT    "     "
   0000                    ..R4:0B0->0FF   MESSAGE      "     "
   0000                    ...
   0000                    ..R2:150->15F   INTERRUPT DATA POINTER
   0000                    ..R3:140->147   OUTPUT ROW POINTER
   0000                    ..R5:148->14F   MESSAGE DATA POINTER
   0000                    ..RB:100->13F   ID TAG POINTER
   0000                    ...
   0000                    ..R8: TEMPORARY ROW POINTER
   0000                    ..R9: STORES DECODED INCOMING MESSAGE
   0000                    ..R6: R6.1--PREAMBLE ZERO COUNTER
   0000                    ..      R6.0--TIME INTERVAL FROM LAST CORRELATION
   0000                    ..              PEAK
   0000                    ..R7: R7.1--INCOMING MESSAGE BYTE
   0000                    ..      R7.0--POINTS INTERRUPT PROGRAM BACK TO
   0000                    ..                MESSAGE OR DISPLAY PROGRAM
   0000                    ..RA: RA.1--TEMPORARY ROW DATA REGISTER
   0000                    ..      RA.0--UPDATE TIME REGISTER
   0000                    ..RC: RC.0--DELAY REGISTER(HELPS KEEP DUTY
   0000                    ..              CYCLE OF MULTIPLEXED OUTPUT
   0000                    ..                CONSTANT)
   0000                    ...
   0000                    ..R2 STACK REGISTER INFORAMATION
   0000                    .. 15F:X AND P OF DISPLAY PROGRAM
   0000                    .. 15E: D  OF           "        "
   0000                    .. 15D: DF OF           "        "
   0000                    .. 15C: CORRELATION TOTAL
   0000                    .. 15B: --
   0000                    .. 15A: X AND P OF MESSAGE PROGRAM
   0000                    .. 159:  D  OF        "          "
   0000                    .. 158: DF  OF        "          "
   0000                    ..R5 STACK REGISTER INFORMATION
   0000                    .. 14F: MESSAGE LENGTH(0-SHORT;<0-LONG)
   0000                    .. 14E: PRINTER OUTPUT INFORMATION
   0000                     ....
   0000                     ....
   0000                    TIME=R6;MES=R7;ID=R9
   0001                    ORG+NUM1
   0001                    ...REGISTER INITIALIZATION...
   0001 F860A2A3F875A1     +NUM60->R2.0,R3.0;+NUM75->R1.0
   0008 F801B1B2B3B5B9BB   +NUM1->R1.1,R2.1,R3.1,R5.1,R9.1,RB.1,R8.1
   0011 90A6B6A7B7A9B4BC   R0.1->R6.0,R6.1,R7.0,R7.1,R9.0,R4.1,RC.0,RC.1
   001A F8B1A4F84FA5       +NUMB1->R4.0;+NUM4F->R5.0
   0020 23F8BF53           INT:DECR3;+NUMBF->+ATSR3
   0024 833A20             R3.0->#;IF>0 GO TO INT
   0027 F85AA3F85453       +NUM5A->R3.0;+NUM54->+ATSR3
   002D F840A3A8F880BAEB   +NUM40->R3.0,R8.0;+NUM80->RA.1;SEXB
   0035                     ..
   0035                     ..DISPLAY PROGRAM
   0035                     ..
   0035 F840ABA8           DS1: +NUM40->RB.0,R8.0  ..SET ID=64
   0039 F880AA             +NUM80->RA.0  ..SET UPDATE TIME
   003C 2BF0               DS2: DECRB;LDX  ..CK ID TAG FOR RECENT XMIT
```

```
F   003E 3230            IF =0 GO TO DS3 ..BR IF TAG=0
    0040 FF015B          -+NUM1:STR R3  ..SUPT 1 FROM ID TAG
    0043 9AF6            RA.1->#:/2
F   0045 F9803000        .OR.+NUM80: GO TO DS4..PUT 1 IN TEM ROW REG
    0049 9AF6            DS3: RA.1->#:/2      ..PUT 0 IN TEM ROW REG
    004B BA              DS4: #->RA.1
F   004C 3BCC            IF NDF GO TO DS5  ..BR IF TEM REG NOT FULL
    004E 5818            STR R8:INC R8  ..STR TEM REG IN DISPLAY REG
    0050 F880BA          +NUM80->RA.1
    0053 E361            DS5:SEX R3:OUT1  ..OUTPUT TO DISPLAY
    0055 83FF48          R3.0-+NUM48  ..CK IF LAST ROW
F   0058 3A00            IF >0 GO TO DS6  ..BR IF NOT LAST ROW
    005A F840A3          +NUM40->R3.0 ..SET DISPLAY TO 1ST ROW
    005D EB8B            DS6:SEXR8:R8.0->#  ..CK IF ID=0
    005F 3A3C            IF >0 GO TO DS2  ..BR IF ID>0
    0061 2A8A            DEC RA;RA.0->#
    0063 3235            DS8:IF =0 GO TO DS1  ..BR IF UPDATE TIME=0
    0065 F818AC          +NUM18->RC.0  ..SET DELAY TIME
    0068 2C8C3A68        DS7: DECRC:RC.0->#:IF>0 GO TO DS7..BR IF DELAY>
    006C 3053            GO TO DS5
    006E                  ..
    006E                  ..MESSAGE PROGRAM
    006E                  ..
    00B0                 ORG+NUMB0
    00B0 00              BEG:IDLE ..WAIT FOR INTERRUPT
    00B1 97F6B7          MES.1->#:/2:->MES.1
F   00B4 3300            IF DF GO TO TP1 ..BR IF FRAME MARK IS PRESENT
    00B6 2730B0          DEC MES:GO TO BEG..NO SYNC MARK
    00B9                 ... CK MESSAGE LENGTH
    00B9 FA03            TP1:#.AND.+NUM3
F   00BB 3200            IF =0 GO TO MM
    00BD FF0355          -+NUM3:MM:STR R5..IF 0,SHORT MESSAGE
    00C0 2700            DEC MES:IDLE ..WAIT FOR LSB OF ID
    00C2 97F6B7          MES.1->#:/2:->MES.1
    00C5 2700            DEC MES:IDLE..WAIT FOR PARITY BIT
    00C7 97F6B7          MES.1->#:/2:->MES.1
    00CA                 ...CK PARITY
F   00CA F63B00          TP2:/2:IF NDF GO TO TS2
    00CD 17              INC MES ..COUNT NUM OF 1 BITS
    00CE 3ACA            TS2: IF >0 GO TO TP2
    00D0 87F6            MES.0->#:/2 ..CK IF ODD
F   00D2 3300            IF DF GO TO RESET1..OR EVEN
    00D4 97FA3FA9        MES.1.AND.+NUM3F->ID.0..MESSAGE ID
    00D9 255562          DECR5:#->+ATSR5:OUT2
    00DB F86059          +NUM60->+ATSR9..SET DISPLAY TIME(5= 1 SEC DISPL
F   00DE F0320C          LDX:IF =0 GO TO RESET1..BR IF SHORT MESSAGE
    00E1 F820B7          +NUM 20-> MES.1
    00E4 F800A700        TP3:+NUM0->MES.0:IDLE..WAIT FOR EXTRA BITS
    00E8 97F63BE4        MES.1->#:/2:IF NDF GO TO TP3
    00EC F6AA            /2:->RA.0
    00EE F800A7E7B6      RESET1:+NUM0->MES.0,MES.1,TIME.1
    00F3 30B0            GO TO BEG
    00F5                  ..
    00F5                  ..INTERRUPT PROGRAM
    00F5                  ..
    0170                 ORG+NUM170
    0170 1242F6          RTN1:INCR2:LDAR2:/2
    0173 4270            LDAR2:RETURN..TO MAIN PROG.
    0175 227822          DECR2:SAVE:DECR2..SAVE X#P
    0178 5222            STRR2:DECR2 ..SAVE D
F   017A 3300            IF DF GO TO X
F   017C F8003C00        +NUM0->#:GO TO X1 ..SAVE DF
    0180 F8015222        X:+NUM1->#:X1:STRR2:DECR2
F   0184 3000            GO TO INPUT
```

```
    0186                    ...
    0186 F858A2             RTN2:+NUM58->R2.0
    0189 42F642             LDAR2:/2:LDAR2
    018C 70                 RETURN.. TO MESS PROG.
    018D 2278225222         DECR2:SAVE:DECR2:STRR2:DECR2
F   0192 3300               IF DF GO TO Y
F   0194 F8003000           +NUM0->#:GO TO Y1
    0198 F80152             Y:+NUM1->#:Y1:STRR2
    0199 F85CA2             +NUM5C->R2.0
    019E                    ...
    019E 6F                 INPUT:INP7  ..INPUT TOTAL
    019F 96FF05             Z5:TIME.1-+NUM5 ..CK IF ZERO=5
F   01A2 3200               IF #=0 GO TO DET..BR IF ZERO=5
    01A4 FDFF07             +ATS-+NUM7..SUBT THRESHOLD
F   01A7 3300               Z0:IF DF GO TO Z1..BR IF>TH
    01A9 96                 TIME.1->#  ..LOAD ZERO
    01AA 3270               IF #=0 GO TO RTN1
    01AC 86FF0A             TIME.0-+NUMA
F   01AF 3300               IF DF GO TO RESET..BR IF>TMAX
    01F1 163070             T1:INC TIME:GO TO RTN1
    01F4 96                 Z1:TIME.1->#  ..CK FOR 1ST ZERO
F   01F5 3200               IF =0 GO TO Z2..BR IF  1ST ZERO
    01F7 86FF03             TIME.0-+NUM3
    01BA 3BB1               IF MINUS GO TO T1..BR IF<TMIN
F   01BC FF043B00           -+NUM4:IF MINUS GO TO RESET..BR IF<TWINDOW
F   01C0 FD023B00           -++NUM2:IF MINUS GO TO RESET..BR IF>TMAX
    01C4                    ...
    01C4 96FC01B6           Z2:TIME.1++NUM1->TIME.1..ADD 1 TO ZERO
    01C8 F800A6             SYNC:+NUM0->TIME.0
    01CB 8716               S2: MES.0->#:INC TIME..ADD 1 TO TIME INTERVAL
    01CD 3270               IF #=0 GO TO RTN1
    01CF 3086               GO TO RTN2
    01D1                    ...
    01D1 86FD0A             DET:TIME.0-++NUMA..IS TIME IN WINDOW
F   01D4 3B00               IF MINUS GO TO RESET..BR IF >TMAX
F   01D6 FF033B00           -+NUM3:IF MINUS GO TO D1..BR IF >TWINDOW
    01DA 30CB               GO TO S2 ..RETURN
    01DC FCFF07             D1:+ATS-+NUM7 ..CK FOR +PEAK
F   01DF 3B00               IF MINUS GO TO D2..BR IF NOT>TH
F   01E1 3000               GO TO NEW   ..A 0 BIT
    01E3 FDFF02             D2:+ATS-+NUM2..CK FOR -PEAK
    01E6 33CB               IF DF GO TO S2..BR IF NOT <-TH
    01E8 97F980B7           MES.1.OR.+NUM80->MES.1..A 1 BIT
    01EC 1730C8             NEW:INC MES:GO TO SYNC
    01EF                    ....
    01EF F800B7A7B6         RESET:+NUM0->MES.1,MES.0,TIME.1..RESET SYSTEM
    01F4 F8B1A4             +NUMB1->R4.0
    01F7 3070               GO TO RTN1
    01F9                    END
```

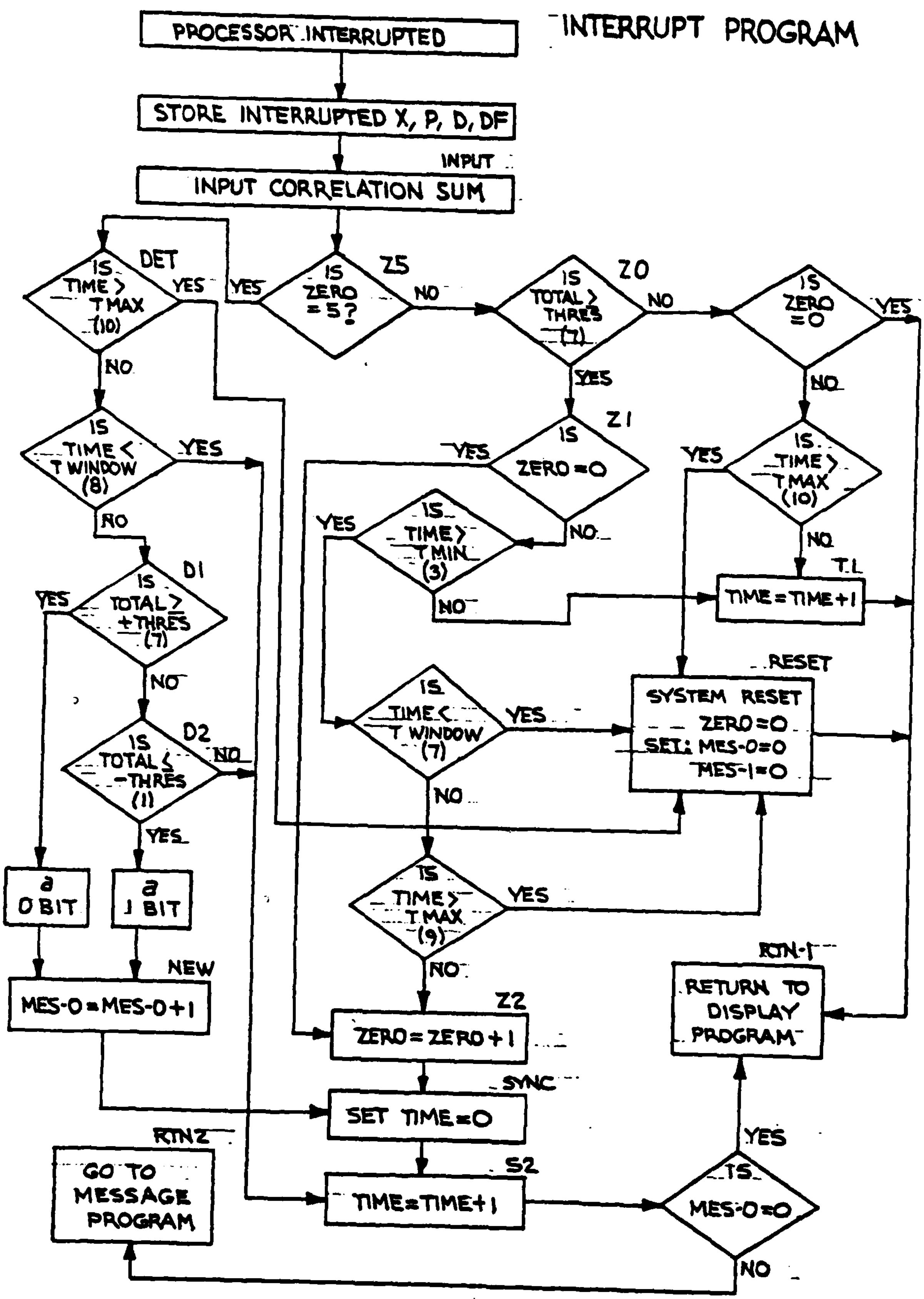

INTERRUPT PROGRAM
PROCESSOR INTERRUPTED
STORE INTERRUPTED X, P, D, DF
INPUT
INPUT CORRELATION SUM
DET
IS TIME > TMAX (10)
YES
NO
Z5
IS ZERO = 5?
YES
NO
Z0
IS TOTAL > THRES (7)
NO
YES
IS ZERO =0
YES
NO
IS TIME < T WINDOW (8)
YES
NO
Z1
IS ZERO =0
YES
NO
IS TIME > TMAX (10)
YES
NO
IS TIME > TMIN (3)
YES
NO
T.L
TIME = TIME+1
D1
IS TOTAL > +THRES (7)
YES
NO
RESET
SYSTEM RESET
ZERO=0
SET: MES-0=0
MES-1=0
D2
IS TOTAL < -THRES (1)
NO
YES
IS TIME < T WINDOW (7)
YES
NO
a 0 BIT
a 1 BIT
IS TIME > TMAX (9)
YES
NO
NEW
MES-0 = MES-0+1
RTN-1
RETURN TO DISPLAY PROGRAM
Z2
ZERO = ZERO + 1
SYNC
SET TIME=0
RTN2
GO TO MESSAGE PROGRAM
S2
TIME=TIME+1
YES
IS MES-0=0
NO

FIGURE 15

Decoder Software

The software is organized as three major programs: (1) the interrupt program which does the actual decoding of the correlated information, (2) the message program that checks the decoded binary data for the proper information, and (3) the display program which updates and controls the output display.

The assembly language listing of the programs along with comments and the assembly code is shown in Figure 14. Descriptions of each program will be discussed.

Interrupt Program. The interrupt program does the actual decoding of the correlated biphase data. An interrupt is created every 416 usec. At this time, the processor automatically jumps to the interrupt program (IP) where the most recent correlation sum is transferred to memory. Using the new sum, the IP checks for a correlation peak and the time interval from the last peak. The program determines from this information if the incoming data is biphase information or if the input signal is random noise. Depending on the results of these tests, the program sends the processor to either the display program or message program. The flow diagram of the interrupt program is shown in Figure 15.

At the time of the interrupt, the IP stores the information necessary to return the processor to the exact point from which it was interrupted. When this is done, the correlation sum is transferred to memory by the input instruction. The program is now at pt Z5 of the flow chart.

There are several paths that the IP can take depending on the value of the correlation sum (TOTAL), the preamble zero counter (ZERO), and the time interval counter (TIME). The preamble zero counter keeps track of how many biphase zeros are received in a row. The time interval counter is the elapsed time (number of interrupts) from the last correlation peak (a correlation peak being a correlation sum of 7 or 8 coincidences).

Referring to Figure 15A, assuming random noise as an input signal and ZERO = 0, the two paths that can be taken are shown. If TOTAL < 7, the processor returns to the display program (DP). If TOTAL ≥ 7, it appears as if a biphase zero has been received and ZERO is increased by one at pt Z2, TIME is set to one at pt SYNC, and the program returns to the DP.

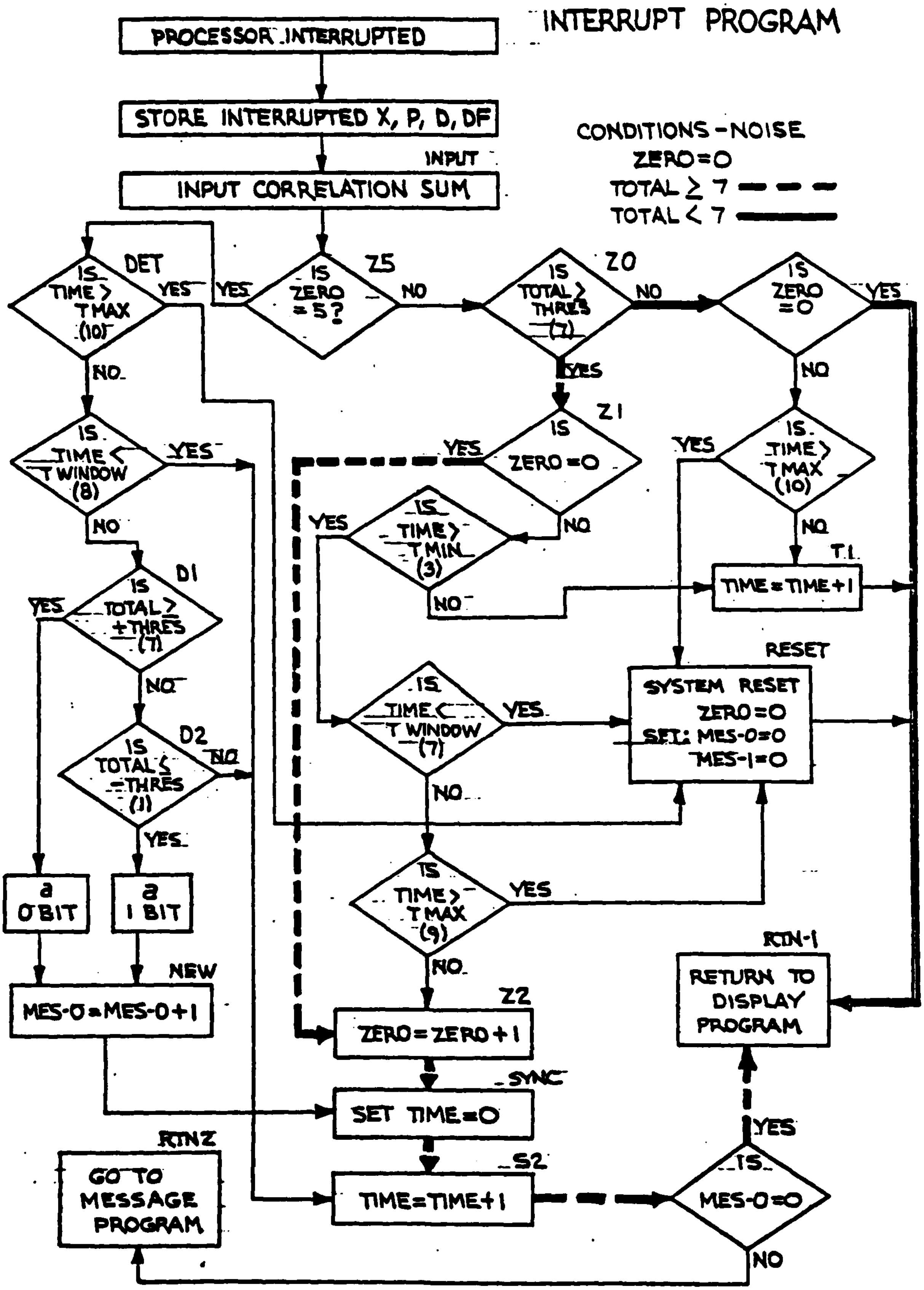
During the next several interrupts Figure 15B illustrates the paths that will be followed if the input signal is still noise and TIME < TMAX, TMAX being the maximum time allowed between correlation peaks before the system is reset.

For the case where TOTAL < 7, TIME is increased by one at pt T1 and the program returns to the DP. If TOTAL ≥ 7, a peak has occurred before it should for a biphase zero (indicating noise) and the system is reset and returns to the DP.

Figure 15C shows the two paths that are followed if TIME > TMAX, again indicating noise. In both cases, the system is reset and returns to the DP.

Now considering the case where a valid message is being received, Figure 15A (TOTAL ≥ 7) shows the path that results from the first biphase zero received from the preamble.

For the next four biphase zeros that are detected, Figure 15D illustrates the flow of the program. The TOTAL < 7 path will be followed until TOTAL is again ≥ 7, TIME being increased by one each time this route is taken.



INTERRUPT PROGRAM
PROCESSOR INTERRUPTED
STORE INTERRUPTED X, P, D, DF
INPUT
INPUT CORRELATION SUM
CONDITIONS - NOISE
ZERO = 0
TOTAL ≥ 7
TOTAL < 7
DET
IS TIME > TMAX (10)
YES
NO
Z5
IS ZERO = 5?
Z0
IS TOTAL > THRES (7)
IS ZERO = 0
Z1
IS ZERO = 0
IS TIME < T WINDOW (8)
IS TIME > TMAX (10)
IS TIME > TMIN (3)
T1
TIME = TIME + 1
D1
IS TOTAL ≥ +THRES (7)
RESET
SYSTEM RESET
ZERO = 0
SET: MES-0 = 0
MES-1 = 0
D2
IS TOTAL ≤ -THRES (1)
IS TIME < T WINDOW (7)
IS TIME > TMAX (9)
a 0 BIT
a 1 BIT
NEW
MES-0 = MES-0 + 1
RTN-1
RETURN TO DISPLAY PROGRAM
Z2
ZERO = ZERO + 1
SYNC
SET TIME = 0
RTN2
GO TO MESSAGE PROGRAM
S2
TIME = TIME + 1
IS MES-0 = 0

FIGURE 15A

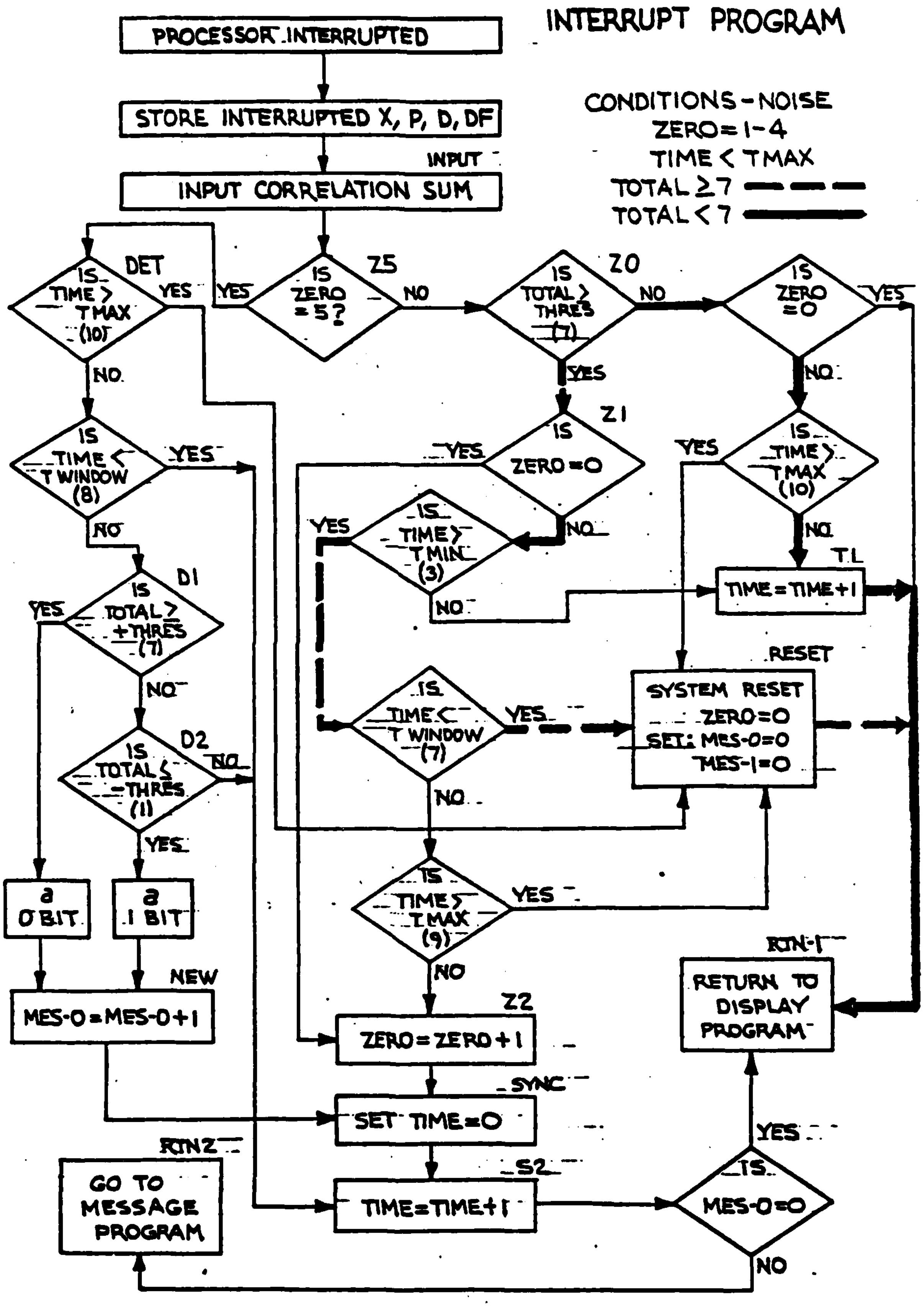
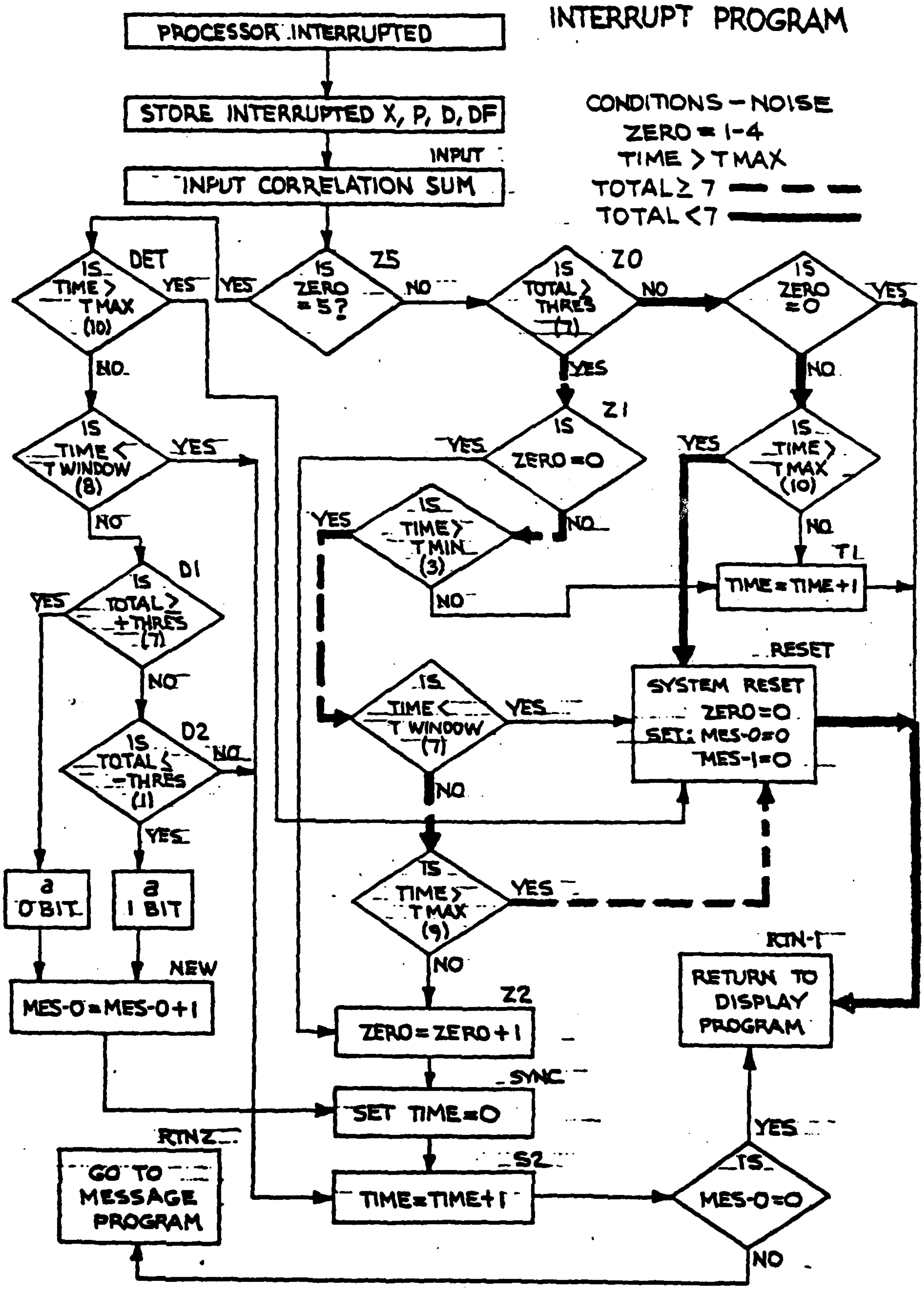
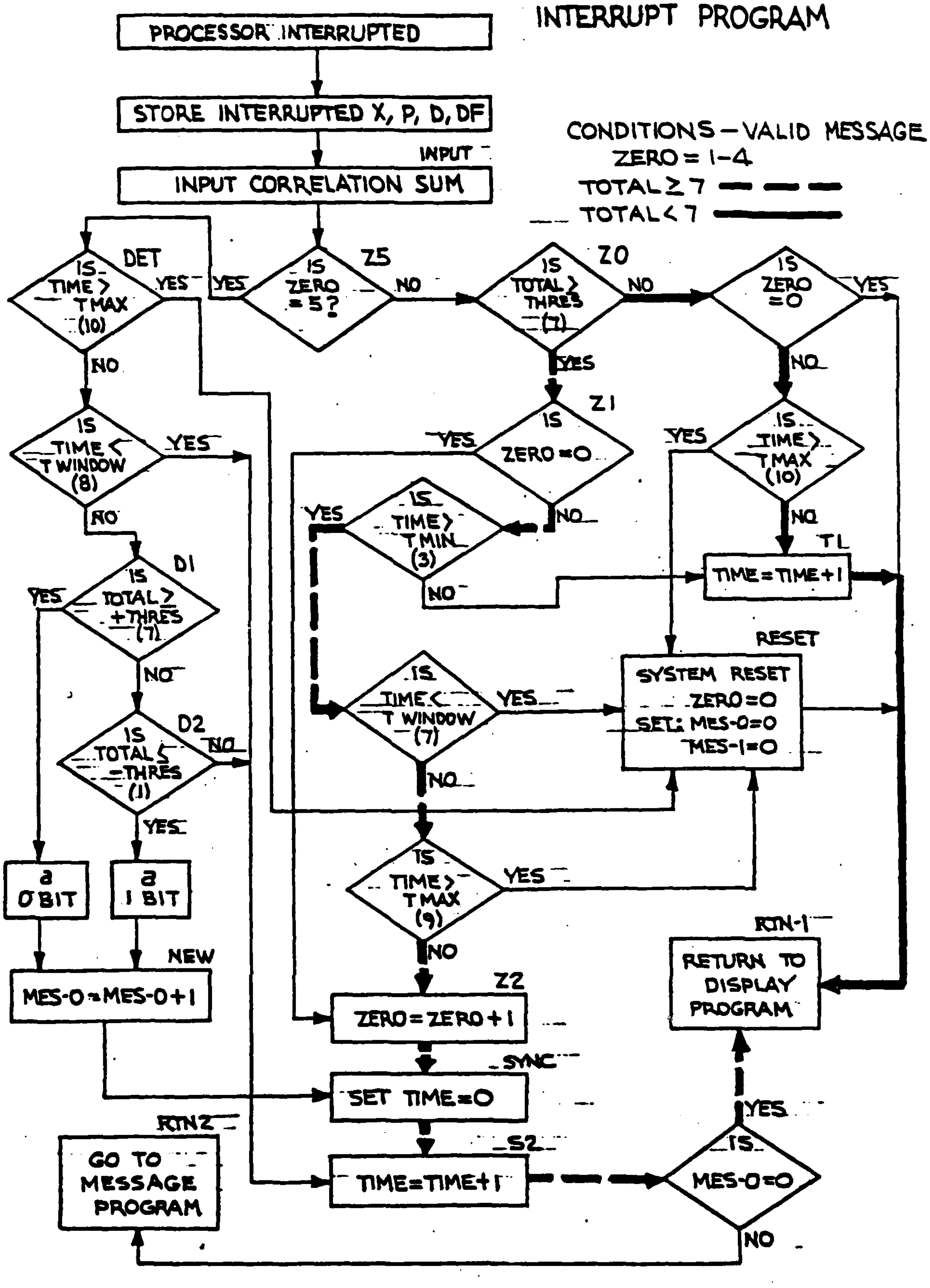

INTERRUPT PROGRAM
CONDITIONS - NOISE
ZERO = 1-4
TIME < TMAX
TOTAL ≥ 7
TOTAL < 7
PROCESSOR INTERRUPTED
STORE INTERRUPTED X, P, D, DF
INPUT
INPUT CORRELATION SUM
DET
IS TIME > TMAX (10)
Z5
IS ZERO = 5?
Z0
IS TOTAL > THRES (7)
IS ZERO = 0
Z1
IS ZERO = 0
IS TIME < T WINDOW (8)
IS TIME > TMIN (3)
IS TIME > TMAX (10)
T.L
TIME = TIME + 1
D1
IS TOTAL > +THRES (7)
RESET
SYSTEM RESET
SET: ZERO = 0
MES-0 = 0
MES-1 = 0
IS TIME < T WINDOW (7)
D2
IS TOTAL ≤ -THRES (1)
a 0 BIT
a 1 BIT
IS TIME > TMAX (9)
RTN-1
RETURN TO DISPLAY PROGRAM
NEW
MES-0 = MES-0 + 1
Z2
ZERO = ZERO + 1
SYNC
SET TIME = 0
RTN2
GO TO MESSAGE PROGRAM
S2
TIME = TIME + 1
IS MES-0 = 0
YES
NO

FIGURE 15B



INTERRUPT PROGRAM
CONDITIONS - NOISE
ZERO = 1-4
TIME > T MAX
TOTAL ≥ 7
TOTAL < 7
PROCESSOR INTERRUPTED
STORE INTERRUPTED X, P, D, DF
INPUT
INPUT CORRELATION SUM
DET
IS TIME > T MAX (10)
YES
NO
Z5
IS ZERO = 5?
Z0
IS TOTAL > THRES (7)
IS ZERO = 0
Z1
IS ZERO = 0
IS TIME < T WINDOW (8)
IS TIME > T MIN (3)
IS TIME > T MAX (10)
TL
TIME = TIME + 1
D1
IS TOTAL > + THRES (7)
D2
IS TOTAL ≤ - THRES (1)
IS TIME < T WINDOW (7)
RESET
SYSTEM RESET
ZERO = 0
SET: MES-0 = 0
MES-1 = 0
IS TIME > T MAX (9)
a 0 BIT
a 1 BIT
NEW
MES-0 = MES-0 + 1
RTN-1
RETURN TO DISPLAY PROGRAM
Z2
ZERO = ZERO + 1
SYNC
SET TIME = 0
RTN2
GO TO MESSAGE PROGRAM
S2
TIME = TIME + 1
IS MES-0 = 0

FIGURE 15C



INTERRUPT PROGRAM
PROCESSOR INTERRUPTED
STORE INTERRUPTED X, P, D, DF
INPUT
INPUT CORRELATION SUM
CONDITIONS — VALID MESSAGE
ZERO = 1-4
TOTAL ≥ 7
TOTAL < 7
DET
IS TIME > TMAX (10)
YES
NO
Z5
IS ZERO = 5?
Z0
IS TOTAL > THRES (7)
IS ZERO = 0
Z1
IS ZERO = 0
IS TIME < T WINDOW (8)
IS TIME > TMIN (3)
IS TIME > TMAX (10)
TL
TIME = TIME + 1
D1
IS TOTAL ≥ +THRES (7)
RESET
SYSTEM RESET
ZERO = 0
SET: MES-0 = 0
MES-1 = 0
IS TIME < T WINDOW (7)
D2
IS TOTAL ≤ −THRES (1)
a 0 BIT
a 1 BIT
IS TIME > TMAX (9)
RTN-1
RETURN TO DISPLAY PROGRAM
NEW
MES-0 = MES-0 + 1
Z2
ZERO = ZERO + 1
SYNC
SET TIME = 0
RTN2
GO TO MESSAGE PROGRAM
S2
TIME = TIME + 1
IS MES-0 = 0

FIGURE 15D

Ideally, a correlation peak should occur when TIME = 8. When TIME is 7, 8 or 9, allowing for a noisy signal, TOTAL should be $\geq$ 7. ZERO will be incremented by one and TIME will be set to one at pt SYNC. This process will be repeated for the first five biphase zeros of the preamble.

It is possible the correlation sum will remain above the threshold for two or maybe three sample periods because of noise. If this occurs, the Z0-Z1-T1 path will be taken for the second and third cycle instead of the Z0-T1-T2 path.

When five zeros have been detected, it is assumed a valid message is being received. From this point, the correlation sum is tested only during the proper time interval (TIME = 7, 8, or 9). Figure 15E demonstrates the flow of the program once the preamble has been recognized. If TIME < 7, TIME is incremented by one and the processor returns to the DP. When TIME $\geq$ 7, TOTAL is checked for a positive or negative peak. If there is no peak, TIME is incremented by one and the processor returns to the DP.

Figure 15F assumes there is a correlation peak in the proper time window, a positive peak indicating a zero bit and a negative peak being a one bit. This information is stored in the memory message register, MES 1. The program pointer, MES 0, is set to one at pt NEW which will direct the processor to the message program (MP) after TIME is set to one at pt S2.

As the message continues, the program flow should follow the paths of Figure 15E for 7 or 8 interrupts and then the path of 15F to determine if the most recent biphase bit was a binary zero or one.

The message program resets the program pointer, MES 0 to zero when it has finished processing the latest binary bit. This allows the processor to return to the display program as a message is being decoded.

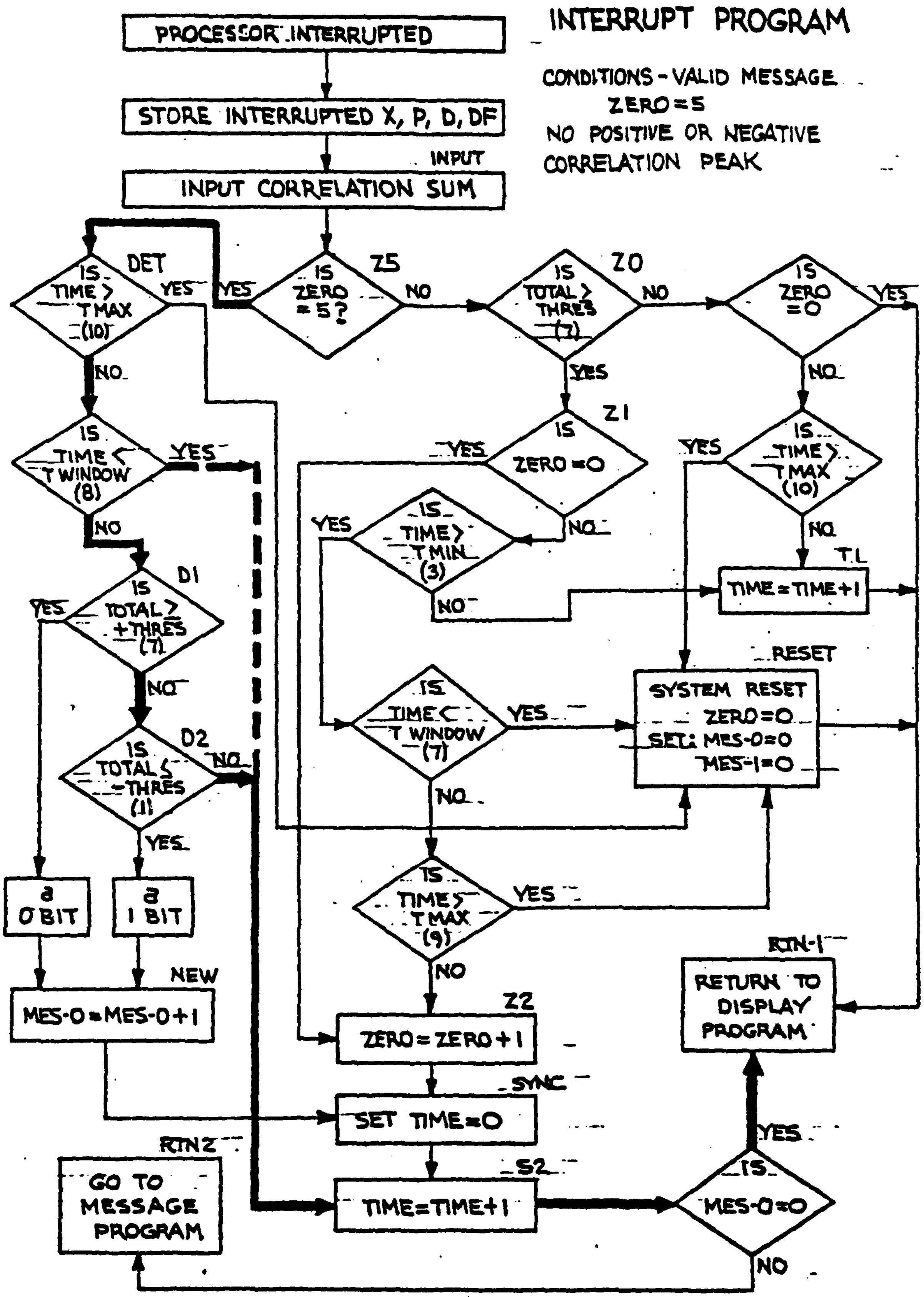

INTERRUPT PROGRAM
CONDITIONS - VALID MESSAGE
ZERO=5
NO POSITIVE OR NEGATIVE
CORRELATION PEAK
PROCESSOR INTERRUPTED
STORE INTERRUPTED X, P, D, DF
INPUT
INPUT CORRELATION SUM
DET
IS TIME > T MAX (10)
YES
NO
Z5
IS ZERO = 5?
Z0
IS TOTAL > THRES (7)
IS ZERO = 0
Z1
IS ZERO = 0
IS TIME < T WINDOW (8)
IS TIME > T MIN (3)
IS TIME > T MAX (10)
TL
TIME = TIME + 1
D1
IS TOTAL > + THRES (7)
D2
IS TOTAL ≤ - THRES (1)
RESET
SYSTEM RESET
ZERO = 0
SET: MES-0 = 0
MES-1 = 0
IS TIME < T WINDOW (7)
IS TIME > T MAX (9)
a 0 BIT
a 1 BIT
NEW
MES-0 = MES-0 + 1
RTN-1
RETURN TO DISPLAY PROGRAM
Z2
ZERO = ZERO + 1
SYNC
SET TIME = 0
RTN2
GO TO MESSAGE PROGRAM
S2
TIME = TIME + 1
IS MES-0 = 0

FIGURE 15E

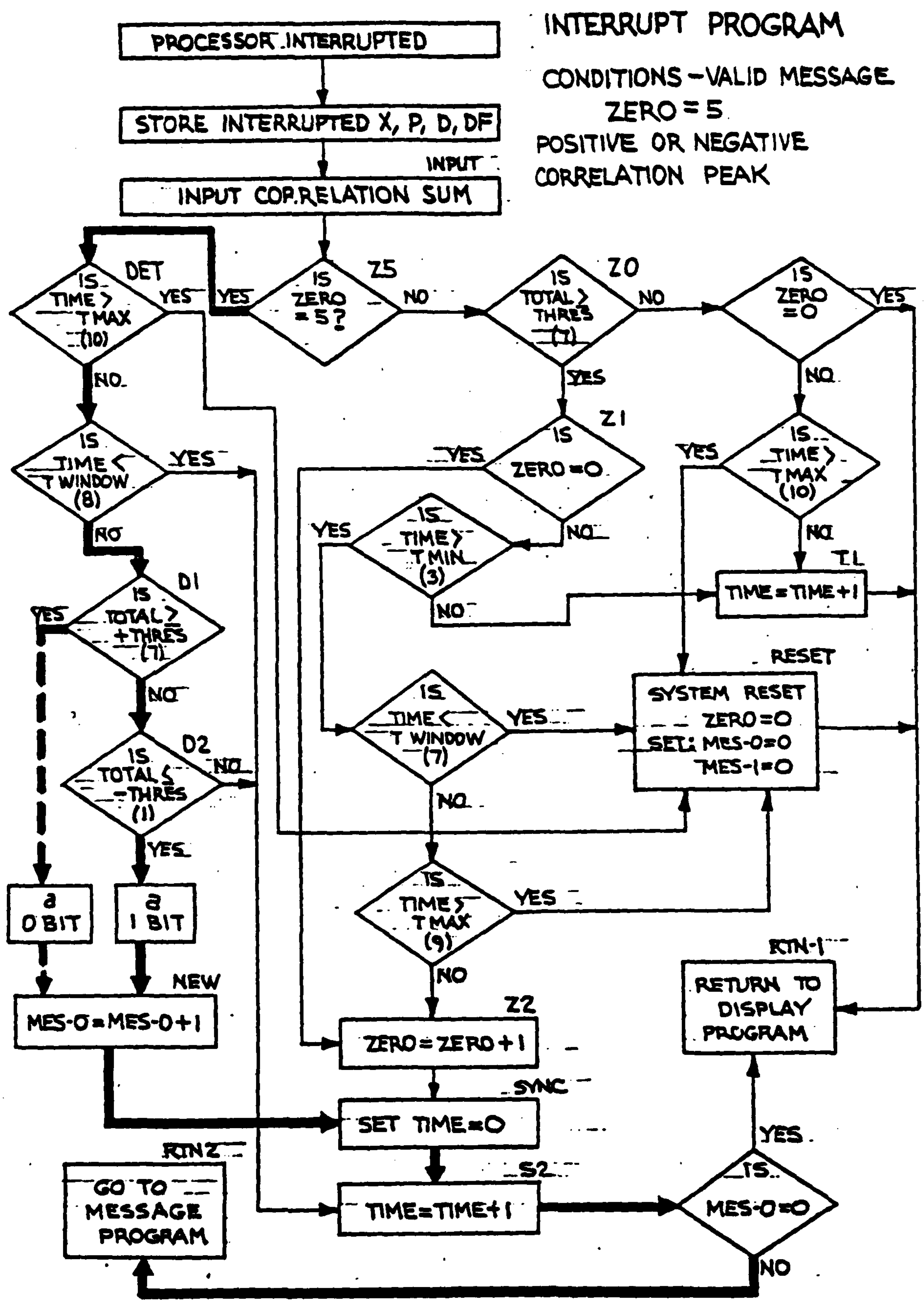

INTERRUPT PROGRAM
CONDITIONS - VALID MESSAGE
ZERO = 5
POSITIVE OR NEGATIVE
CORRELATION PEAK
PROCESSOR INTERRUPTED
STORE INTERRUPTED X, P, D, DF
INPUT
INPUT CORRELATION SUM
DET
IS TIME > T MAX (10)
Z5
IS ZERO = 5?
Z0
IS TOTAL > THRES (7)
IS ZERO = 0
Z1
IS ZERO = 0
IS TIME < T WINDOW (8)
IS TIME > T MIN (3)
IS TIME > T MAX (10)
T1
TIME = TIME + 1
D1
IS TOTAL > + THRES (7)
RESET
SYSTEM RESET
ZERO = 0
SET: MES-0 = 0
MES-1 = 0
D2
IS TOTAL < - THRES (1)
IS TIME < T WINDOW (7)
IS TIME > T MAX (9)
a 0 BIT
a 1 BIT
NEW
MES-0 = MES-0 + 1
Z2
ZERO = ZERO + 1
RTN-1
RETURN TO DISPLAY PROGRAM
SYNC
SET TIME = 0
RTN2
GO TO MESSAGE PROGRAM
S2
TIME = TIME + 1
IS MES-0 = 0
YES
NO

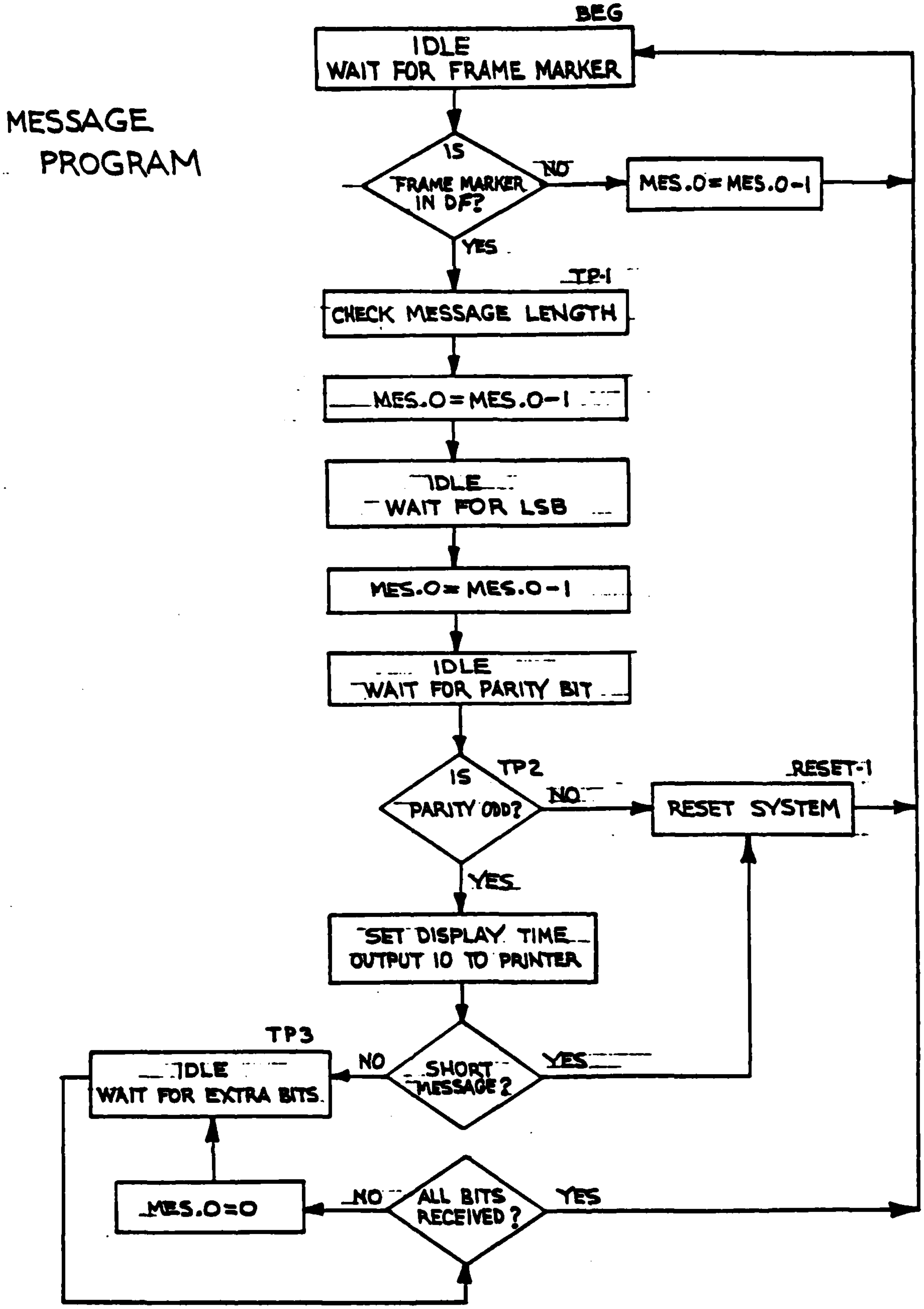
FIGURE 15F

Message Program. The message program collects the binary information that is stored in the message register MES 1 to determine if the incoming message is a short message (ID number only) or a long message (ID number, plus six additional information bits) and decides if the parity of the ID is correct. Once the message has been determined valid, the appropriate ID memory location is set to tell the display program a valid message has been received and sends the proper information to the printer. The message program (MP) flow chart is shown in Figure 16.

Once the IP has determined a valid message is being received, the IP will direct the processor to the MP each time another biphase bit has been decoded. The newest binary bit is stored in the MSB of the message register, MES 1 by the IP. When the MP is entered, this register is shifted right one bit, as shown in Figure 17A. As the register is shifted right, the right most bit of the register is put into the DF register. This register is checked for the frame marker, a binary one. If the frame marker is not in the DF register, the program will reset the program printer, MES 0, and return to pt BEG.

The processor will remain at this point until it is again interrupted and jumps to the IP.

Every time the MP is entered, which will be every eight or nine interrupts as a valid message is being received, a new bit has been decoded and the data in the MES 1 register is shifted right one bit, illustrated in Figure 17A, B, C. This will continue until the frame marker is shifted into the DF register, Figure 17D. With the frame marker in DF, the program will check the message length (pt TP1 of the flow diagram),reset the program pointer to zero, and wait at this point for the next interrupt.



MESSAGE PROGRAM
BEG
IDLE
WAIT FOR FRAME MARKER
IS FRAME MARKER IN DF?
NO
MES.O=MES.O-1
YES
TP-1
CHECK MESSAGE LENGTH
MES.O=MES.O-1
IDLE
WAIT FOR LSB
MES.O=MES.O-1
IDLE
WAIT FOR PARITY BIT
TP2
IS PARITY ODD?
NO
RESET-1
RESET SYSTEM
YES
SET DISPLAY TIME
OUTPUT 10 TO PRINTER
TP3
IDLE
WAIT FOR EXTRA BITS
NO
SHORT MESSAGE?
YES
MES.O=0
NO
ALL BITS RECEIVED?
YES

FIGURE 16

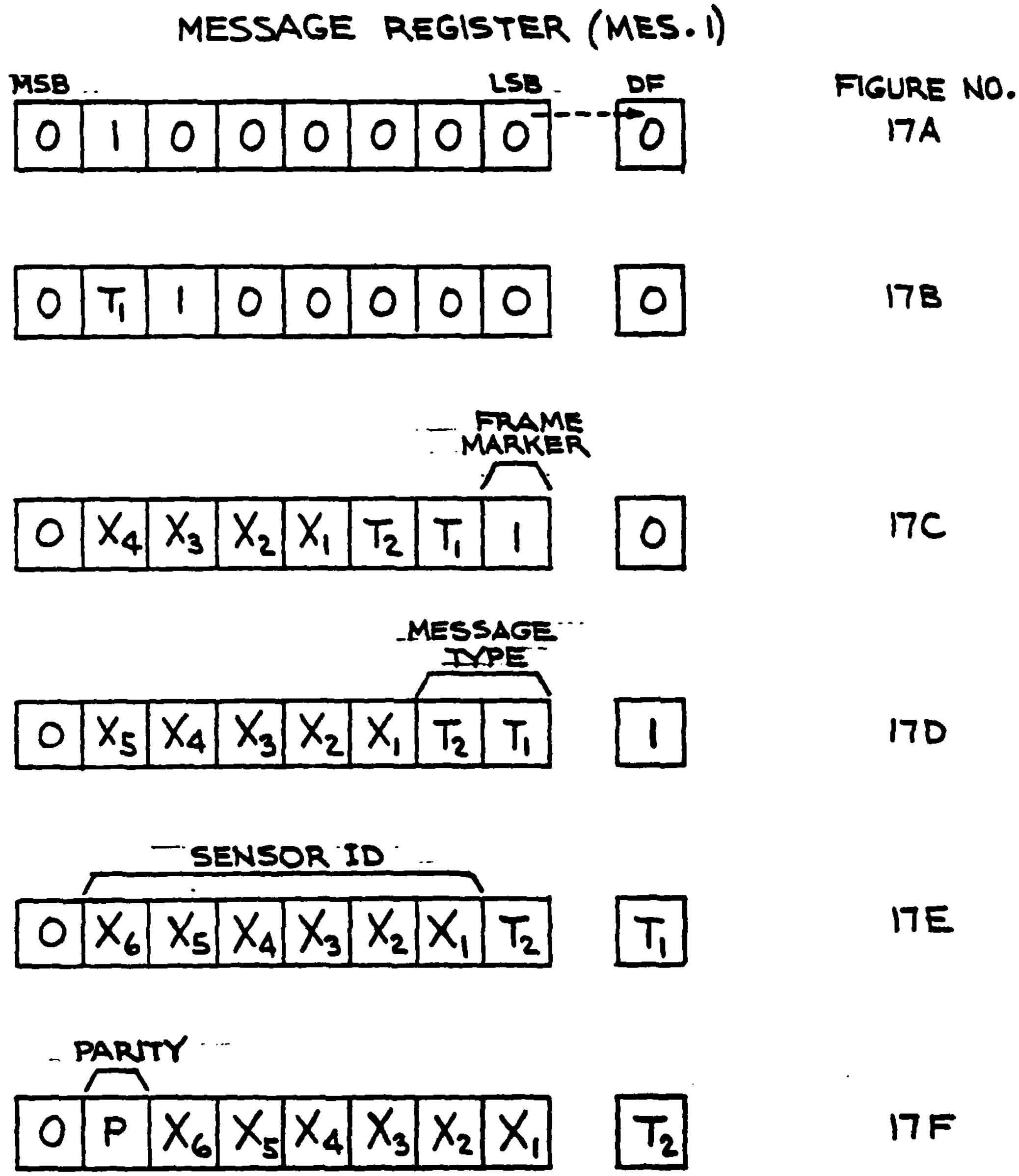


ILLUSTRATION OF DATA FORMATION
OF INCOMING MESSAGE
FIGURE 17

The next two bits that are received are the MSB of the ID and the message parity bit (Fig 17E, F). When the parity bit has been received, the parity of the message is tested at pt TP2. If parity is even, the message is not valid and the system is reset. If parity is odd, the program outputs the ID number to the printer and sets the approximate ID memory location to tell the display program a message has been received. The value of the number (ID tag) stored in the ID memory location determines the length of the display time.

If a short message was transmitted, the program will return to pt BEG. For a long message, the program will wait at pt TP3 for the six additional information bits before returning to pt BEG.

Display Program. The display program (DP) updates and controls the LED display. The flow diagram of the program is shown in Figure 18. There are 64 ID memory locations that are continually checked for recently received messages. The 64 ID memory locations are divided into an 8x8 matrix with each row of the matrix requiring one byte (eight bits) of memory. Each bit of a matrix row byte corresponds to one ID number.

The eight matrix rows are updated five times a second while the rows are multiplexed to the output register at about a 200 Hz rate.

Referring to Figure 18A, the update cycle of the program is shown. At pt DS2, the ID memory location is decremented by one. If it is the first time through the loop, the ID that is tested is ID#63. The ID tag (the value stored at the ID memory location) is checked. If the value is zero, no messages have been received with that ID and a zero is put in the temporary display register (A.1) at that ID's bit position.

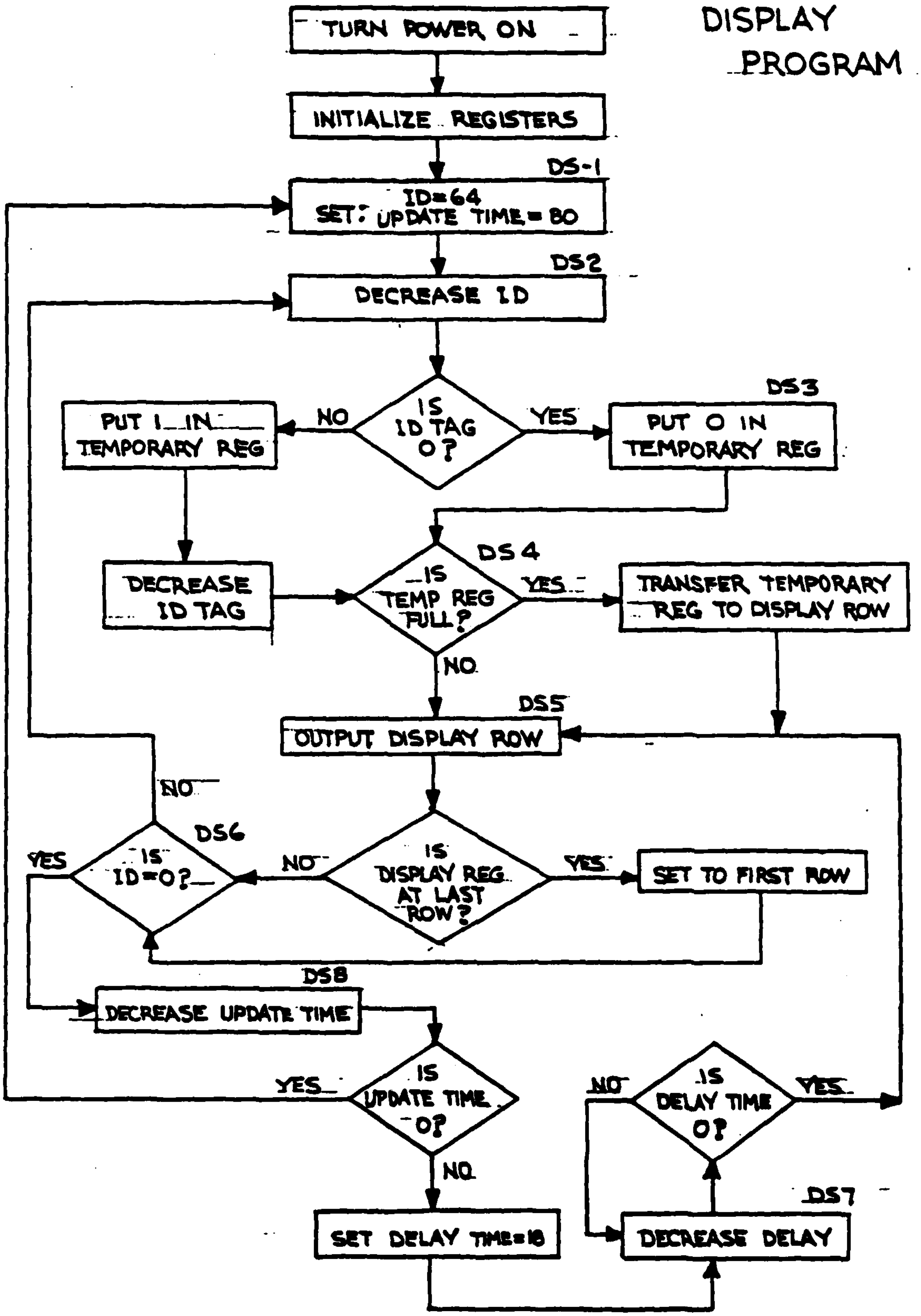
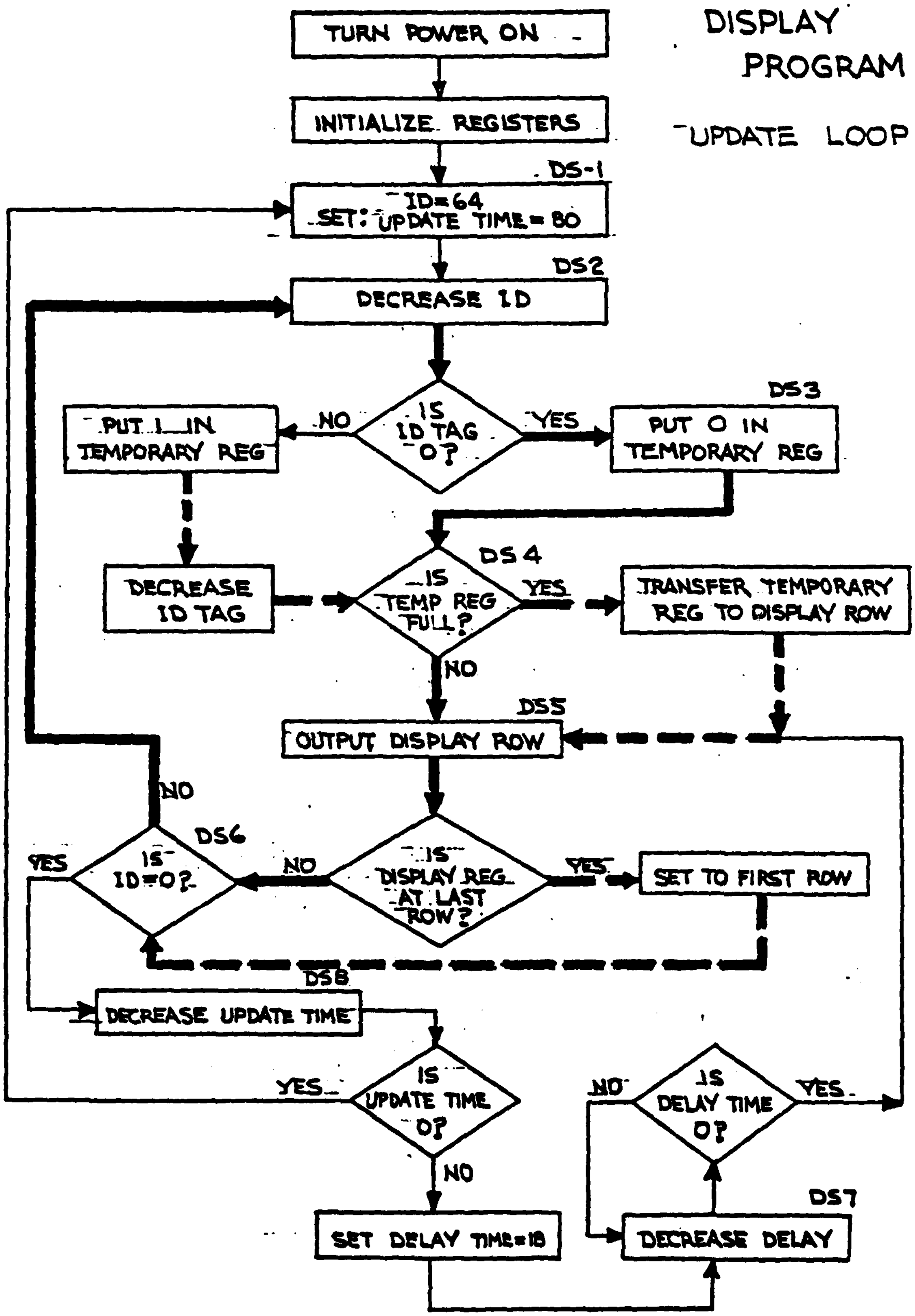
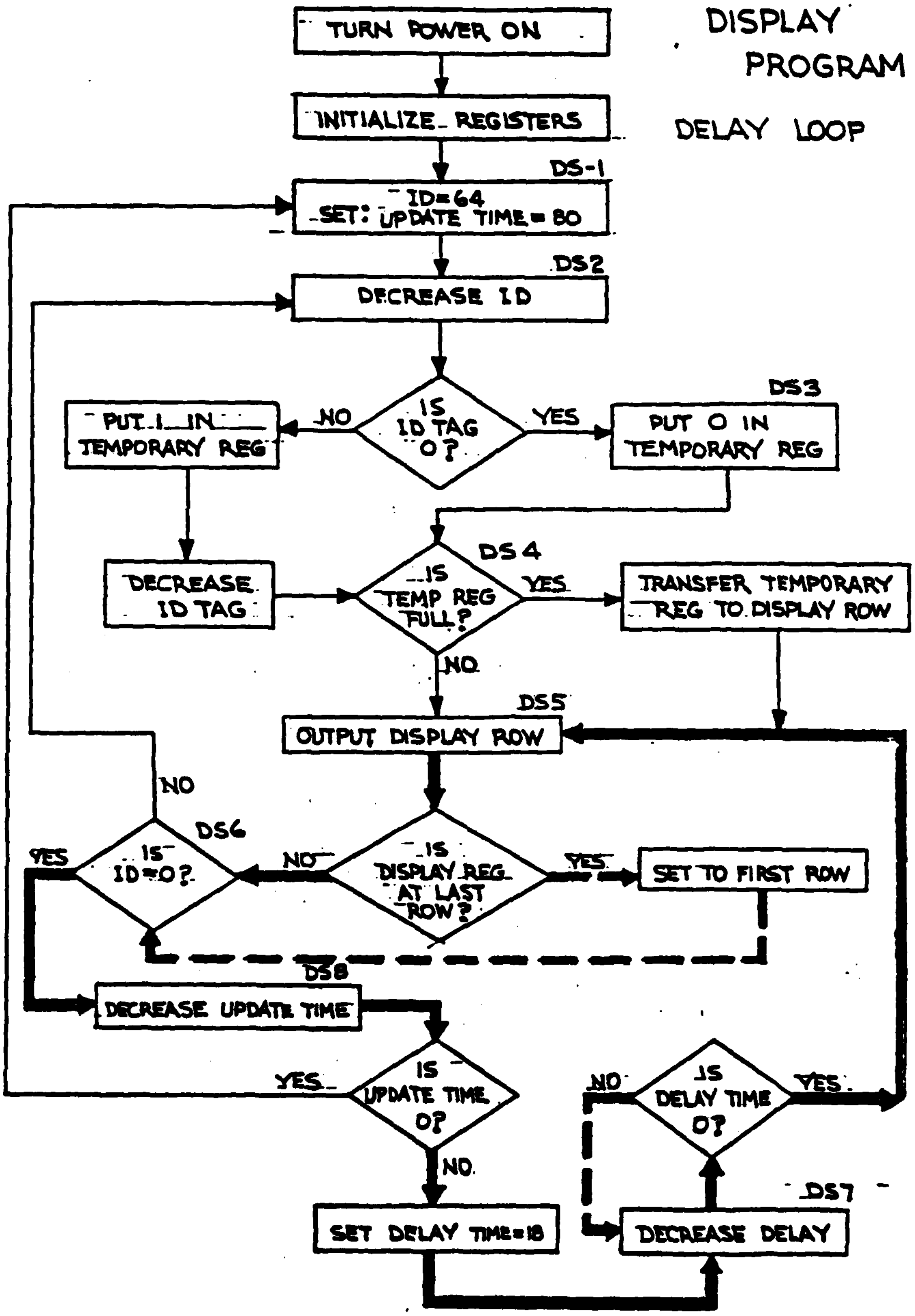

DISPLAY PROGRAM
TURN POWER ON
INITIALIZE REGISTERS
DS-1
SET: ID=64 UPDATE TIME=80
DS2
DECREASE ID
IS ID TAG 0?
NO
YES
DS3
PUT 1 IN TEMPORARY REG
PUT 0 IN TEMPORARY REG
DECREASE ID TAG
DS4
IS TEMP REG FULL?
YES
NO
TRANSFER TEMPORARY REG TO DISPLAY ROW
DS5
OUTPUT DISPLAY ROW
NO
DS6
YES
IS ID=0?
NO
IS DISPLAY REG AT LAST ROW?
YES
SET TO FIRST ROW
DS8
DECREASE UPDATE TIME
YES
IS UPDATE TIME 0?
NO
SET DELAY TIME=18
NO
IS DELAY TIME 0?
YES
DS7
DECREASE DELAY

FIGURE 18



DISPLAY PROGRAM
UPDATE LOOP
TURN POWER ON
INITIALIZE REGISTERS
DS-1
SET: ID=64 UPDATE TIME=80
DS2
DECREASE ID
IS ID TAG 0?
NO
YES
PUT 1 IN TEMPORARY REG
DS3
PUT 0 IN TEMPORARY REG
DECREASE ID TAG
DS4
IS TEMP REG FULL?
YES
TRANSFER TEMPORARY REG TO DISPLAY ROW
NO
DS5
OUTPUT DISPLAY ROW
NO
DS6
IS ID=0?
YES
NO
IS DISPLAY REG AT LAST ROW?
YES
SET TO FIRST ROW
DS8
DECREASE UPDATE TIME
YES
IS UPDATE TIME 0?
NO
NO
IS DELAY TIME 0?
YES
DS7
SET DELAY TIME=18
DECREASE DELAY

FIGURE 18A



DISPLAY PROGRAM
DELAY LOOP
TURN POWER ON
INITIALIZE REGISTERS
DS-1
SET: ID=64 UPDATE TIME=80
DS2
DECREASE ID
IS ID TAG 0?
NO
YES
PUT 1 IN TEMPORARY REG
DS3
PUT 0 IN TEMPORARY REG
DECREASE ID TAG
DS 4
IS TEMP REG FULL?
YES
TRANSFER TEMPORARY REG TO DISPLAY ROW
NO
DS5
OUTPUT DISPLAY ROW
NO
DS6
YES
IS ID=0?
NO
IS DISPLAY REG AT LAST ROW?
YES
SET TO FIRST ROW
DS8
DECREASE UPDATE TIME
YES
IS UPDATE TIME 0?
NO
SET DELAY TIME=18
NO
IS DELAY TIME 0?
YES
DS7
DECREASE DELAY

FIGURE 18B

The next time through the loop, ID#62 will be tested. If the ID tag has a value greater than zero, a one will be stored in the temporary display register and the ID tag will be decreased by one. This will continue for each cycle through the loop until a position bit, indicating the temporary register is full, is in the DF register. The contents of the temporary display register is transferred to the output display row memory location. An example illustrating the above procedure is shown in Figure 19.

The next eight ID locations will be tested in the same manner and the contents of the temporary display register will be stored in the next display row. This will continue until all 64 ID memory locations are tested.

Each time an ID memory location is checked, the value (if > 0) of the ID tag is decreased by one until its value is zero. Since the ID tags are checked approximately five times a second, a value of five for the ID tag will turn on the LED display light corresponding to the ID number for about one second.

During each cycle of the update loop, an output display row byte is transferred to the output display register by the OUT 1 instruction (pt DS5 on the flow diagram). If the last row has just been transferred to the output, the display row pointer is set to the first row. The program will step through the eight output rows during the next eight cycles of the update loop.

The update loop will continue until all 64 ID memory locations have been tested. Once this is completed, the program will begin the delay loop, illustrated in Figure 18B.

The delay loop controls the 200 Hz multiplexing rate of the LED display. The multiplexing is not a constant rate because the interrupt program will vary in time depending on the incoming data.

TEMPORARY DISPLAY REGISTER

CYCLE OF UPDATE LOOP		MSB							LSB	DF	OUTPUT ROW NO.
1		63	1 (POSITON BIT)	–	–	–	–	–	–	0	–
2		62	63	1 (POSITION BIT)	–	–	–	–	–	0	–
3		61	62	63	1 (POSITION BIT)	–	–	–	–	0	–
8	ID NO.	56	57	58	59	60	61	62	63	1 (POSITION BIT)	1
16	ID NO.	48	49	50	51	52	53	54	55	1	2
24	ID NO.	40	41	42	43	44	45	46	47	1	3
32	ID NO.	32	33	34	35	36	37	38	39	1	4
40	ID NO.	24	25	26	27	28	29	30	31	1	5
48	ID NO.	16	17	18	19	20	21	22	23	1	6
56	ID NO.	8	9	10	11	12	13	14	15	1	7
64	ID NO.	0	1	2	3	4	5	6	7	1	8

FORMATION OF OUTPUT DISPLAY ROWS
FIGURE 19

A varying multiplexing rate causes the output LED's to flicker when turned on. The delay loop lengthens the time between output instructions (which determines the multiplexing rate) so the varying rate caused by the interrupt program is not as noticeable.

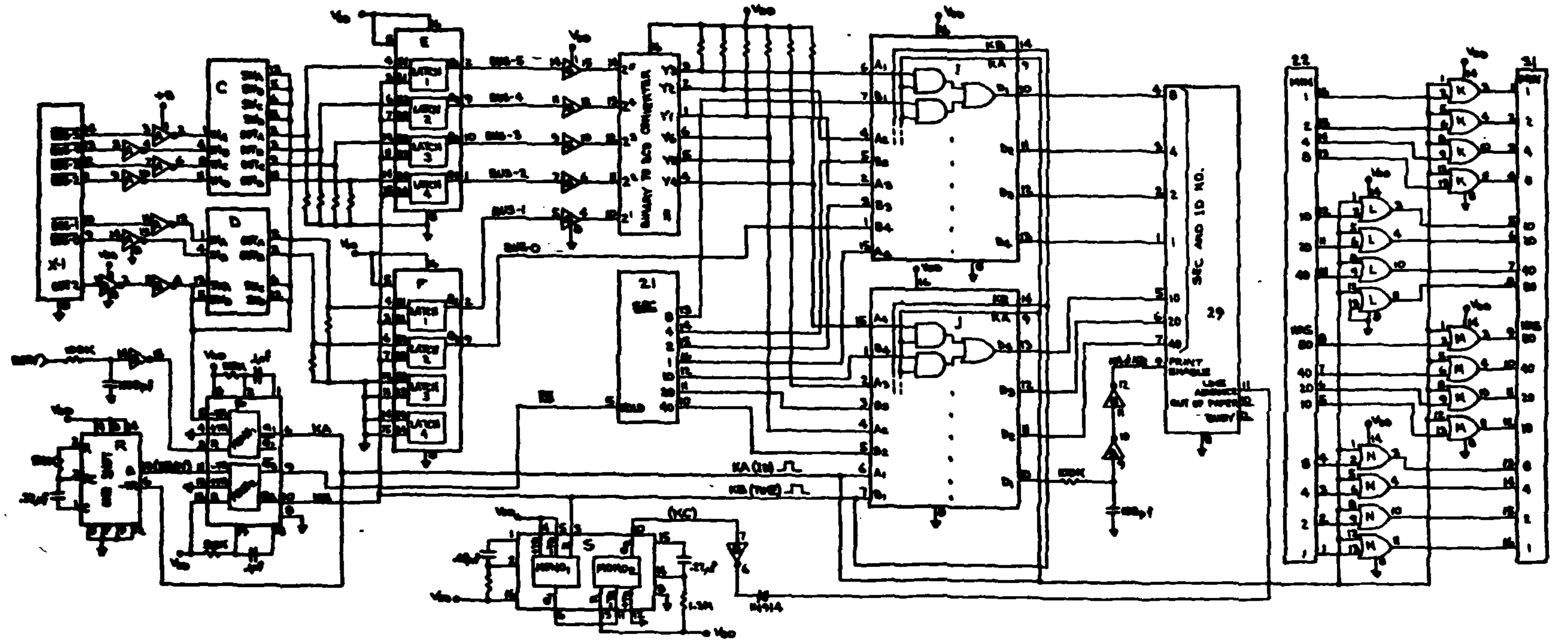
The length of time the display program will remain in the delay loop depends on the value of the update constant. During each cycle of this loop, the update constant is decreased by one at pt DS8. The delay loop will continue until the update constant is zero, allowing the program to enter the update loop again. With a value of 128 for the update constant, the update loop is entered about five times a second.

The update constant was an arbitrary value picked to allow some flexibility in the setting of the display time and still have the ID memory locations updated at a reasonable interval. The delay constant (pt DS7 on flow diagram) was chosen to reduce the flicker of the display LED's.

Peripheral Circuits

Printer Interface. The printer interface is necessary to convert the binary ID data the microprocessor outputs to BCD information required by the printer. The interface circuits also multiplexes the converted ID code and the clock BCD code onto the printer BCD input lines. The schematic of the printer interface is shown in Figure 20.

When a message has been received, the binary ID code is clocked into the printer interface latches (IC-E,F) by the OUT 2 instruction. The bus lines and command line are buffered (IC-C,D) to the printer operating voltage of five volts. The latched information is converted to BCD code and then routed to the printer multiplexing logic (IC-I, J). The latched outputs are buffered (IC-G) to drive the TTL binary to BCD converter (IC-H).



IC-A CD4049
IC-B CD4049
IC-C CD4016
IC-D CD4016
IC-E CD4043
IC-F CD4043
IC-I CD4019
IC-J CD4019
IC-K CD4071
IC-L CD4071
IC-M CD4071
IC-N CD4071
21, 22 TIME CLOCK CONNECTORS (16 PIN DIPS)
29, 31 PRINTER CONNECTORS (16 PIN DIPS)
X-1 DECODER CONNECTOR (16 PIN DIP) (FROM CPU BOARD)

PRINTER INTERFACE FIGURE 20

The printer can print six digits and therefore require 24 BCD input lines. The two least significant digits are used for the ID number or seconds of the time and the remaining four digits are used for minutes and hours.

When the binary ID information is clocked into the latches, the same clock pulse creates the ID print pulse KA (IC-P6) that will command the printer to print the ID number. The KA pulse also creates an invalid input (all ones) for the four most significant digits thereby blanking them out.

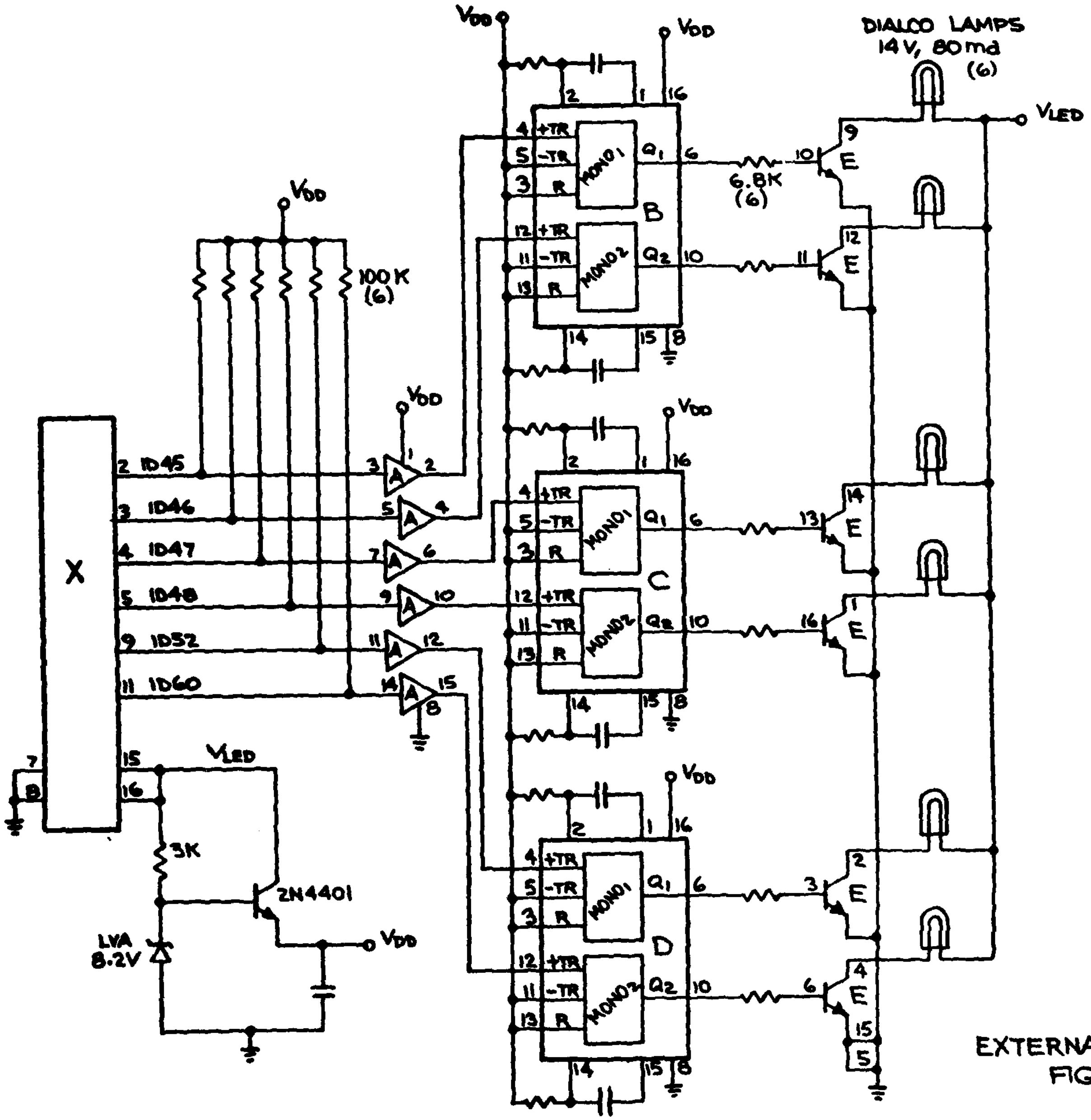
A minimum time of 330 ms is necessary for the printer to complete one line. This delay is produced by IC-R. When the printer is ready to print the second line, pulse KB (IC-P10) transfers the clock BCD output to the printer input lines (IC-I, J, K, L, M, N). IC-S creates another delay for the printing of the time and then advances the printer one line with pulse KC (IC-S10).

The printer output, BUSY, inhibits another ID to be printed before the above sequence is finished. One ID and related time can be printed per second.

External Lamp Drivers. In addition to the display LED's, there are display lights external to the display box. Incandescent lamps and drivers are needed because the LED's do not produce enough light if viewed from many different angles.

Miniature incandescent lamps are used because of their better visibility at greater angles of view. The multiplexing rate of the LED's is not sufficient to illuminate the miniature lamps; therefore, the need for non-multiplexed drivers. The schematic is shown in Figure 21.

To accomplish the non-multiplexing of the lights, one-shots (IC-B,C,D) of a length longer than the multiplexing rate are used to turn on the lamp's transistor drivers (IC-E). If the display LED is multiplexed on, the one-shot will be triggered at the multiplexing rate and provide the lamp drivers with a continuous ON signal for as long as the LED is pulsed ON and OFF.



IC·A CD4050B
IC·B CD4098
IC·C CD4098
IC·D CD4098
IC·E CA3081
X DISPLAY CONNECTOR (16 PIN DIP)

EXTERNAL LAMP DRIVERS
FIGURE 21

APPENDIX B

REMOTE VESSEL MONITORING SYSTEM (RVMS)

1. GENERAL DESCRIPTION

a. The RVMS utilizes a magnetic detector to signal the presence of ships within its detection envelope. The information is relayed via a VHF-FM link to the Vessel Traffic Service (VTS) where it is displayed and recorded.

b. The system consists of a magnetic detector enclosed in a waterproof housing connected to the above water transmitting station by a waterproof cable. The transmitting station is housed in an AN type shipping container 10.5" in diameter and 42" long. Inside the container are the transmitter, encoder, message identification selector, and battery pack. The antenna is attached to the outside of the container and is indistinguishable from the container.

c. At the VTS duty room, the messages from the detectors are received, decoded, and recorded. A receiving antenna is located about 130 feet above sea level on a tower at the VTS. A cabinet containing the receiver, decoder, printer and digital clock is located near the watch supoervisor's station. Each time a vessel triggers a magnetic detector, the printer indicates the time of occurrence and the location of the activated detector. Transmitting stations are located on Navigation Aids (NA) and the detectors are placed near the edge of the ship channel adjacent to the NA. This was necessary to insure sensor integrity during dredging operations.

2. COMPONENT DESCRIPTIONS

a. Receiver/Display Unit

(1) Antenna - A corner reflecting antenna with 10 dB gain, 30 dB front-to-back ratio, and a beam width of 40^o was mounted on the VTS tower atop the duty room. Estimated height above sea level is 130 feet, providing a nautical mile line of sight range of 1.4 130 ft or 16 nm to an antenna at sea level. Range to the farthest NA (146) is 6 nm. No problems were encountered with the RF transmission path. The antenna was connected to the receiver through 200 feet of RG 213 coaxial cable. Type N male coaxial connectors are used on both ends of the cable. The cable has an attenuation at 200 MHz of 3 dB/100 ft.

(2) Receiver - The receiver is a commercial VHF-FM 6 channel crystal controlled radio operated at 168.0625 MHz. Sensitivity is -100 dBm for 20 dB quieting. An audio bandpass of at least 3 kHz is required. The remote station signal is taken off the discriminator for processing. This allows the squelch and volume controls to be set for operator convenience without affecting operation of the decoder.

(3) Printer - The digital printer is activated each time a message is received from a transmitter. The printer indicates the time of receipt and the number of the NA the message originated from.

(4) Digital clock - The clock is used to provide the printer with real time for the printout. Clock outputs are directly compatible with the printer input requirements.

(5) Decoder - The decoder utilizes the RCA CDP 1801 microprocessor to decode the digital signal output from the receiver. The remote transmitter message is decoded and the NA number is printed along with the time of receipt. Small LED's on the front panel of the Receiver/Display unit are activated for 20 seconds each time a message from a NA location is received. The six LED's can be connected to represent any of the 64 NA numbers available. Connected in parallel with the LED's are small incandescent lights located on the VTS plotting board so that duty personnel can readily compare a vessel's dead reckoned position with the actual position.

b. Transmitter Unit

(1) The housing consists of a 10.5" diameter by 42" high AN type metal shipping container. A lucite platform is bolted across the diameter of the can 18" from the open end. The platform supports the battery pack and transmitter/encoder/NA number selector assembly.

(2) The transmitting antenna is a magnetic microstrip dipole commonly known as a quarter-wave patch radiator. It is a thin, conformal antenna which is easily comouflaged. The antenna is produced on a piece of copper clad teflon-fiberglass substrate 1/32" thick through a combination etching and plating process. After being riveted to the outside surface of the can, the antenna is coated with Epon 828 between 8 and 10 mils thick to provide protection against weather. It is then spray painted white to match the rest of the can. The antenna is 12.25" wide by 8.0" high and is horizontally polarized. Impedance is 50 ohms. VSWR is very sharp and is 1.5:1 or less at the transmitting frequency.

(3) The transmitter/encoder/NA number assembly receives a 6-volt, 5 ms pulse from the magnetic detector and sends an FSK transmission of an 18-bit word containing the NA number. The NA number is selected by setting the eight switches on the code board module. This binary word is fed to the encoder which actually modulates the transmitter. The transmitter is activated for 60 ms with each transmission and will not interfere with other RF transmissions. Nominal RF output is 4.0 watts with a supply voltage of 30 volts.

(4) The battery pack consists of 25 Mallory mecuric oxide D size cells connected in series to give 36 volts open circuit. These cells are specially made by Mallory to provide long life at low standby current with the capability of providing 600 ma transmitter current pulses without a drastic drop in voltage. Under these load conditions, and at 70°F, rated capacity is 12 AH. With the high current pulse lasting only 60 ms, the transmitter has little effect on battery life. Expected life with 250 transmissions per day is 172 days while life with no transmissions at all is 179 days. High temperatures, above 100°F, will shorten battery life and low temperature, below 30°F, will decrease load current by 30 percent. Choice of batteries will depend on geographical locaton. Lead time is normally 30 days ARO from Mallory for the 317745 cell. For colder climates, the new lithium organic cells would be preferred. Circuit requirements are

2.8 ma steady state drain with 630 ma, 60ms, pulses required for each transmission. Minimum transmitter voltage is 21 volts under load (3.7 watts output).

c. DETECTOR HOUSING

(1) The detector is housed in a well cut into a 2" thick aluminum plate along with a circuit board which contains a voltage regulator and output driver circuit. Power for the detector is provided by the battery pack at the transmitter unit. The regulator reduces the 36 volts from the battery to 8.7 volts for the detector. The output circuit is used to modify the detector output signal to match the transmitter turn on signal requirements. The detector circuitry contains a 10 second time constant which precludes output pulses spaced less than 10 seconds apart. A small tug will result in only one signal while a 300 foot ship at eight knots will provide two to four signals at 10-second intervals depending on the ship's distance from the detector.

(2) Magnetic Detector - The detector is the GSQ-180(V) originally developed for use in Vietnam for detection of troops carrying a rifle. The detector consists of a balanced magnetic coil, amplifier, and output circuit. The detector is sensitive only to a changing magnetic field. As long as the earth's magnetic field is not changing with respect to the detector, there is no output. As a general rule the detector will provide an output signal when a change of 10 gamma peak occurs over a 4 second period or 2 gamma peak over a 0.5 second period. (Specification threshold sensitivity is 2.5 gamma p-p at 1.0 Hz). As the distortion of the earth's magnetic field caused by passage of a ship is spherical, the range at which a 2-gamma change can be detected is a cubic function for a given size ship. Range tables for various ship sizes and speeds are not available and would be a rather large effort to obtain. In general, calculations show that a 200 ton ship moving at five to eight knots should be detected at 100 yards, a 1000-ton ship at 200 yards and a 10,000 ship at 400 yards. These extrapolations from other data have never been tested. Results will depend a great deal on the amount of permanent magnetism in the ship.

(3) The cable connecting the transmitter unit to the detector housing must be waterproof and water stopped. Three conductors are required of AWG 24 or larger wire. Electrical shielding is not known to be required but is preferred. Very limited tests with unshielded calbes were satisfactory. The VTS installation uses three shielded pairs with each pair connected in parallel. The shields are connected to the battery return at the transmitter unit and are not connected at the detector end. Maximum cable resistance that can be tolerated is 5,000 ohms. (AWG 24 wire has 25 ohms/1000 ft).

3. MAINTENANCE AND OPERATION

a. End of roll of paper in the printer is indicated by a pink stripe on the right side of paper near the end of the roll. If the paper is not replaced, the printer will cease to print. No harm will result to the system. Ship passings will then be indicated by the 20 second lights only.

b. If the receiver/display fails to operate at all - turn the volume up and the squelch off on receiver. Static and signals from interference should be present. The receiver is defective if nothing can be heard on the speaker.

c. Turn main power switch off. Wait a few moments and turn it back on. All indicator lights will come on briefly if decoder is operating properly.

d. Water in the detector housing will cause the transmitter to go into a rapid transmission rate and saturate the RF channel. The detector must be disconnected as soon as possible to remove interference from the RF channel and to prevent complete discharge of the battery pack. Slight leaks may cause the detector to signal every 10 seconds as will movement of housing on the side of the channel.

e. Occasionally, an erroneous digit will appear in the NA number printout. This is due to interference on the RF channel or to lowered battery voltage at the transmitter.

f. A major items parts list is provided.

MAJOR ITEM PARTS LIST

ITEM	MANUFACTURER	COST
Corner Relecting Antenna	Sinclair Radio Labs., Model 228	$ 268.00
Receiver	Sonar Radio Corp., Model FR105	180.00
Printer	Datel Systems Model DPP-7A5	475.00
Clock	Datel Systems Time Clock, 6 digit panel mount, Digital Model DTC8300A6A2	299.00
Enclosure	Treeko Sales, Beltsville, MD #171016-23-X	98.15
Batteries each	Mallory Battery Co., #317745T2 (25 cells req'd per pack)	(ea) 4.08
Transmitter Housing	Mirax Chemical Co., Drum, Steel MS 27684. Inside height 40", no reinforcing rings	24.50
Waterproof Cable Connectors	Rochester Corp., Houston, Texas Cable: Plug, connector, cable type HDL-3 CCP	(ea) 14.80
	Housing: Receptacle Bulkhead Type HDL-3 BCR	(ea) 14.80
Waterproof Cable	Times Wire & Cable Co., #MI 31099	300.00/1kft
Magnetic Detector	Dorsett Electronics, Tulsa, OK GSQ 180(V) NSWC 1018	100.00

MAJOR ITEM PARTS LIST

ITEM	MANUFACTURER	COST
Transmitter	T1233 Transmitter FSN 5820 - 421 - XXXX or - 451 - XXXX or - 784 - XXXX Last 4 digits specify channel No. Consult ECOM for digits corresponding to channel deisred	150.00
Encoder	KY678(GSQ)FSN 5820-00-484-8651	30.00
Connector for ID each Selection Circuit	TA 386 Bendix Corp., N.Y. (120 day delivery)	(ea) 33.00