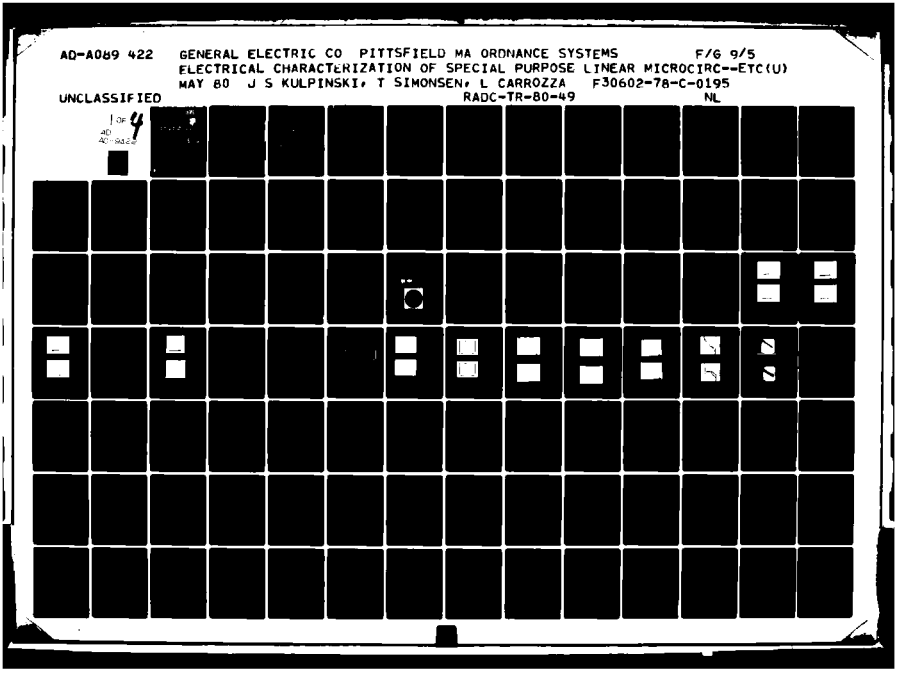
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Interim Report
May 1980

AD A089422

ELECTRICAL CHARACTERIZATION OF SPECIAL PURPOSE LINEAR MICROCIRCUITS

General Electric Ordnance Systems

J. S. Kulpinski, et al

14915

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

This report has been reviewed by the RADC Public Affairs Office (PA) and is releasable to the National Technical Information Service (NTIS). At NTIS it will be releasable to the general public, including foreign nations.

RADC-TR-80-49 has been reviewed and is approved for publication.

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report covers the work performed by General Electric Ordnance Systems pertaining to the electrical characterization and specification of linear microcircuits. The period of report is August 1978 to December 1979. This technical report is divided into chpaters covering specific device types with electrical characterization results. The following device types/families were characterized:

- Adjustable Positive Voltage Regulators,

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Adjustable Negative Voltage Regulators,
Precision BiFet Op Amps,
Multiple BiFet Op Amps,
12 Bit A/D Converters,
12 Bit D/A Converters,
Precision Voltage References, and
Precision Sample/Hold Amplifiers.

Data obtained during device characterization is published in handbook form obtainable under separate cover from this document. Samples of data sheets, histograms, and plots, are included in this report, however.

Acronyms and Symbols

A	Ampere
A/D	Analog to Digital
A_E	Gain Error
$A_{VS}(\pm)$	Open loop voltage gain (single-ended, 0 to +, 0 to -)
BPO	Bipolar offset
BPOE	Bipolar offset error
BW	Bandwidth
CM	Common mode
CMR	Common mode rejection
CPW	Clock pulse width
CS	Channel Separation
$C_T(n)$	A/D converter transition voltage - nth transition
D/A	Digital to Analog
dB	Decibel
DESC	Defense Electronics Supply Center
DUT	Device Under Test
E(n)	A/D converter transition voltage bit error in LSB, with transition
E(n)	Static A/D converter transition voltage less transient error contribution in LSBs
$E_o(n)$	Amplified difference voltage. Difference between reference D/A converter and the DUT output nth transition
FRR	Feedthrough Rejection Ratio
FSV	Full Scale Voltage
FSVR	Full Scale Voltage Range
G	Voltage gain
G_E	Voltage gain error
GE	General Electric Company
GEOS	General Electric Company, Ordnance Systems
GND	Ground
I_{adj}	Adjustment pin current
$+I_{CC}$	Positive supply current
$I_{CH}(+)$	Hold capacitor charging current (+ input)
$I_{CH}(-)$	Hold capacitor charging current (- input)
I_{cont}	Control pin current
ICs	Integrated Circuits
$I_{HL}(+)$	Leakage current into hold with + charge
$I_{HL}(-)$	Leakage current into hold with - charge
$+I_{IB}$	Input bias current, non-inverting input
$-I_{IB}$	Input bias current, inverting input
I_{IH}	High level input current
I_{IL}	Low level input current
I_{IO}	Input offset current
$\Delta I_{IO}/\Delta T$	Input offset current/temperature coefficient

I_{LOG}	Logic power supply current
$I_{OS(+)}$	Output short circuit current (for positive output)
$I_{OS(-)}$	Output short circuit current (for negative output)
I_Q	Quiescent current
I_{REF}	Reference voltage supply current
I_S	Temperature stabilizer supply current
I_{SI}	Initial temperature stabilizer supply current
JAN	Joint Army Navy
JC-41	JEDEC Committee on Linear Integrated Circuits
JEDEC	Joint Electron Devices Engineering Council
ln	Natural logarithm
LSB	Least significant bit of D/A or A/D converter
LSI	Large Scale Integration
LTPD	Lot Tolerance Percent Defective
mA	Milliampere
MCE (n)	Major carry error where n = 1 is major transition with all bits changing
MCE (n)	Major carry error less transient error contribution where n = 1 is major transition with all bits changing
MPCAG	Military Parts Control Advisory Group
mV	Millivolt
$N_i(BB)$	Broadband noise
N_o	Output noise voltage
$N_i(PC)$	Popcorn noise
OS	(GE) Ordnance Systems
P_D	Quiescent power dissipation
pk	Peak
PPM	Parts per million
+PSRR	Power Supply Rejection Ratio, positive supply
PSS	Power Supply Sensitivity
QPL	Qualified Product List
RADC	Rome Air Development Center
R_F	Amplifier feedback resistor
R_I	Amplifier input scanning resistor
S/H	Sample and Hold Circuit
S/N	Serial Number
SR(+)	Slew rate (max $\Delta V_o / \Delta t$), positive
T_A	Ambient temperature
t_{ac}	Acquisition time (S/H)
t_{ap}	Aperture time (S/H)
$TR(t_r)$	Transient response, rise time
TR(OS)	Transient response, overshoot
t_s	Settling time of step response to specified accuracy
t_{SLH}	Settling time, low-to-high
t_{SHL}	Settling time, high-to-low
TTL	Transistor - transistor logic
T^2L	Transistor - transistor logic
V_{ADCIN}	A/D converter input voltage

V_{adj}	Adjustment pin voltage
V_{BE}	Base-to-emitter voltage
V_{cc}	Supply voltage
V_{cont}	Control pin voltage
V_F	Forced voltage
V_{HS}	"Hold" step voltage
V_{IH}	Logic "1" input voltage
V_{IL}	Logic "0" input voltage
V_{IN}	Input voltage
V_{IO}	Input offset voltage
$V_{IO\ ADJ(+)}$	Adjustment for input offset voltage
V_{OH}	Output Voltage, high level
$V_{OI(n)}$	D/A output voltage on straight line between zero and FS for address n
V_{OL}	Output Voltage, low level
$V_{OM(n)}$	D/A output voltage measured for address n
V_{OP}	Output voltage swing (peak)
V_{OUT}	Voltage output
$V_{OUT(RECOV)}$	Regulator output recovery voltage after output short to ground
V_R	Reference Voltage
$V_{RDAC(n)}$	Reference D/A converter output for address n
$V_{R\ LINE}$	Line regulation
$V_{R\ LOAD}$	Load regulation
V_{ROS}	Reference D/A output offset voltage
V_{RTH}	Thermal voltage regulation
$+V_S$	Positive supply voltage
V_{START}	Voltage start-up
Z_i	Input Impedance
Z_o	Output Impedance
$\overline{X}$	Data mean of X
°C	Degrees centigrade
u	Micro
uF	Microfarad
uV	Microvolt
us	Microsecond
Δ	Delta
σ	Sigma
+ NL	Summation of maximum positive bit weight errors
- NL	Summation of maximum negative bit weight errors
$\Delta V_{IO}/\Delta T$	Input offset voltage temperature coefficient
$\Delta V_{IN}/\Delta V_{OUT}$	Ripple rejection
$\Delta V_{OUT}/\Delta V_{IN}$	Line transient response
$\Delta V_{OUT}/\Delta I_L$	Load transient response
$\Delta V_R/\Delta T$	Reference voltage temperature coefficient
θ	Thermal resistance

PREFACE

This report was prepared by General Electric Ordnance Systems, 100 Plastics Avenue, Pittsfield, Massachusetts, for Rome Air Development Center, Griffiss Air Force Base, New York, under contract F30602-78-C-0195. It covers the period Sept. 78 - Sept. 79. Work effort under this contract will continue for the period Sept. 1979 - Sept. 1980, followed by another technical report.

The work on this project was performed by the Electronic Circuits Engineering Operation and Components Engineering Unit. Project responsibility was held by Mr. John Kulpinski of Circuit Design Engineering. Key individuals who made significant contributions to this work effort were Messrs. Theodore Simonsen, Louis Carrozza, Donald Van Alstyne, Robert Mossman, John Dunn, Thomas Wetzel, and George Smith. Mr. Thomas Dellecave, RBRM is the Project Engineer at RADC for this contract.

LINEAR CHARACTERIZATION

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SECTION I

INTRODUCTION

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SECTION 1

INTRODUCTION

Objectives

The major objective of this work effort is to characterize certain linear microcircuit devices for inclusion in MIL-M-38510 ("General specification for Microcircuits") slash sheets.

Generally, "characterization" of a device type includes several related tasks:

- determination of test parameters and limits
- development of test procedures, compatible with automatic test systems
- verification of limits and test circuits via sample device testing/evaluation.
- generation of detailed burn-in and life test circuits
- preparation of rough draft slash sheets

A secondary objective of this effort is to provide follow-up support for maintaining existing linear MIL-M-38510 slash sheets to current status, including support to Rome Air Development Center for manufacturer qualification and related activities.

All of the characterization effort performed is guided by the fundamental objectives of the JAN 38510 program - namely quality, reliability, interchangeability, and standardization.

Scope of Applied Effort

The specific tasks included in this program are the characterization and specification of the following device types/families:

- Adjustable Positive Voltage Regulators, MIL-M-38510/117
- Adjustable Negative Voltage Regulators, MIL-M-38510/118
- Precision BiFET Op Amps, (LF155A etc), MIL-M-38510/114
- Multiple BiFET Op Amps (single, dual, quad), MIL-M-38510/119
- 12-bit A/D Converters, MIL-M-38510/120
- 12-bit D/A Converters, MIL-M-38510/121
- Precision Voltage References, MIL-M-38510/124
- Precision Sample/Holds, MIL-M-38510/125

Additional required tasks included were:

- Assess pending changes to existing slash sheets and recommend appropriate action.
- Support RADC in the evaluation of manufacturer qualification submittals.

- Interface with manufacturers in development of new specs, or changes to existing specs; attend JC-41 Committee and Subcommittee meetings.
- Complete slash sheets not issued at completion of previous contract.

Program Status

The following new slash sheets were developed on this program:

	Commercial Device Type
MIL-M-38510/117, Positive Adjustable Regulators	uA78MG, uA78G, LM117H, LM117K
MIL-M-38510/118, Negative Adjustable Regulators	uA79MG, uA79G, LM137H, LM137K
MIL-M-38510/119, Multiple BiFET Op Amps	TL061, -062, -064, TL071, 072, 074; uA771, -772, 774; LF151, -153, -147
MIL-M-38510/120, 12-Bit A/D Converters	MN 5200-5207, MN5210 - 5217
MIL-M-38510/121, 12-Bit D/A Converters	AD562, HI562
MIL-M-38510/124, Precision Voltage References	LM129, LM199
MIL-M-38510/125, Sample/Hold	LF198

Three device types were added to an existing slash sheet also:

MIL-M-38510/114, BiFET Op Amps	LF155A, LF156A, LF157A

Device characterization is essentially complete for the above specifications with the exception of /120 and /125. The A/D specification has been issued in preliminary form; test hardware and software have been developed, and data is expected soon after publication of this report. The Sample/Hold specification and characterization development is in very early stages; a Table I has been prepared, along with test circuits and a partial Table III, awaiting manufacturer comment. All other specifications and characterizations listed above are complete and include a prepared slash sheet, test adapter hardware and software, and automatic/manual test data.

In addition to the above characterizations, follow-up tasks to previous RADC characterizations were also included in the current contract. This effort included the following:

- Complete characterization of BiFET Op Amps, /114, (non-"A" 155 family), including testing of 68 devices, generation of data handbook, and negotiations at JC-41 Op Amp Subcommittee meeting in San José. Two burn-in circuits were evaluated, also. This is reported in Section II of this report.

- Reviewed and assessed proposed changes to parameters and limits for device type 01, (LM109), on /107, Positive Voltage Regulators. Two manufacturers requested changes via JC-41 Committee letter ballot; GE approved the changes with certain qualifications.

- Reviewed and assessed changes to /115, Negative Voltage Regulators; completed investigation of start-up problems observed earlier at GE. This item is reported upon in Section ____.

- Completed slash sheet for DAC08, /113, 8-bit D/A Converters; Tables III and IV were added; corrections/comments received from manufacturers were incorporated.

- Errors in /112, Quad Comparators, pointed out by one manufacturer were checked out and corrected at GE.

- A change to the slew rate test circuit for the 118 Op Amp, /101, was analyzed.

- A slash sheet written by NASA, MIL-M-38510/122, High Slew Rate and Wide Band Op Amps, was reviewed and comments were submitted to RADC.

Meetings Attended (GE internal meetings not included)

JC-41 Committee on Linear ICs
Nov. 1, 2, 1978 - Phoenix, AZ
Feb. 27, 28, 1979 - Monterey, CA
June 19, 20, 1979 - Washington, DC

JC-41 Subcommittee Meetings

Feb. 6, 1979	562 D/A Converter	Peabody, MA
Feb. 7, 1979	5200 A/D Converter	Peabody, MA
May 1, 1979	5200 A/D Converter	Pittsfield, MA
May 29, 1979	5200 A/D Converter	Sturbridge, MA
Aug. 14, 1979	CMOS D/A Converters	San Jose, CA
Aug. 15, 1979	Sample/Holds; Voltage References	San Jose, CA

RADC/GE Meetings

Sept. 21, 1979	Contract Plans	Pittsfield, MA
Feb. 22, 1979	Contract Status	Pittsfield, MA
May 2, 1979	Contract Status	Pittsfield, MA
May 22, 1979	Contract Status	Rome, NY
Aug. 8, 1979	Contract Status	Pittsfield, MA

Background

General Electric began this effort in September of 1978, having previously completed similar characterization and specification contracts in MIL-M-38510 Linears in 1976 and 1977. Philosophies for establishing parameters, limits, and test circuits for conventional devices like op amps, comparators, and regulators had been negotiated with RADC, DESC, and the device manufacturers in meetings of the JC-41 Committee on Linear Integrated Circuits.

This current effort extended past efforts to newer devices in similar generic families, and in addition established new frontiers in the development of automatic tests and specifications for 12-bit data converters. One slash sheet (/120, 12-bit A/D Converters) represents the first hybrid microcircuit to be specified in military JAN linears.

Whereas in 1976 and 1977 the JAN Linear Program has been "catching up" to the state-of-the-art in developing new specs for existing devices, it is now in some cases leading the development. Witness the slash sheet on single, dual, quad BiFET Op Amps, in which devices from three major manufacturers are just becoming available to users, and 3-terminal adjustable regulators where the JAN spec is ready soon after the market introduction.

Although hybrid A/D converters have been around for awhile, monolithics are just reaching that goal, and manufacturers are faced with new challenges for developing suitable automatic tests for high resolution data converters. Even more ambitious tasks are being planned for the near future, with analog LSI (video A/D converters), non-linear companding DACs, and data acquisition devices in the making.

Development of Slash Sheets

A procedure for developing new slash sheets to MIL-M-38510 has evolved through negotiations among all concerned parties. Device selection is influenced by user need, which is determined both by the marketplace and by organized committees, such as the Military Parts Control Group (MPCAG) at DESC, the G12 Solid State EIA Device Committee, and the Microelectronics Project Group of the Electronics Systems Committee of AIA. These recommendations are balanced with manufacturer recommendations obtained via the JC-41 Committee. Devices having high useage, multiple application potential in military systems, proven performance, and two or more sources are given priority. Single-source devices are acceptable, especially for hybrid devices, although multiple sources are preferred. Manufacturers typically recommend devices for slash sheet action in JC-41 Committees, and then chair a JC-41 Subcommittee for preparation of slash sheet parameters, limits, and test circuits.

The industry data sheet forms the basis for the military specification. Typically, such data sheets do not specify all of the necessary parameters over the military temperature range and over the common-mode voltage range. The JC-41 subcommittee, or the device originating company, usually prepares a proposed spec. Ideally, the device manufacturers would like to have these proposed specs incorporated without further consideration. However, RADC and General Electric experiences in this current program have shown that all of the proposed specs have required some rework, and are unsuitable for issuance "as is".

Data provides another base for determining parameters and limits. Devices for test are purchased from distributors, are also obtained from manufacturers via RADC request. In some cases, the industry-donated sample is tested by a single manufacturer on a volunteer basis. The entire sample

is tested further on a Tektronix S3263 Automatic Test System at GE Ordnance Systems Electronic Test Center. Data obtained at -55 C, +25 C, and +125 C ambient is statistically analyzed and reproduced in histogram format. Recommended limits are compared to the statistical sample data. Parameter limits which are grossly inconsistent with the data are readily identified.

Additions, changes, and alternate approaches are discussed at the committee level. Device anomalies are identified in lab bench tests, often using a curve tracer. Failure modes are also identified. User caution notes are added to the specification if it is deemed appropriate.

Burn-in circuits are usually recommended by the manufacturer and evaluated by RADC and/or GEOS on the available test samples. An objective is to minimize the number of external components while stressing the device near its limits.

Device schematics are presently included in MIL-M-38510 slash sheets. A recent JC-41 Committee recommendation is to delete the schematics and to replace them with a block diagram which shows the basic elements of the device, for devices which are very complex (e.g. data converters).

Rough-draft copies of the final slash sheet are prepared at GEOS and are forwarded to RADC for review. DESC distributes copies of this spec to manufacturers and users for final comments. Following assessment of the comments by all concerned parties, DESC prepares and issues the slash sheet

Characterization Data

Data obtained during device characterization is usually published in handbook form separate from this document. Samples of the data sheets, histograms, and plots, are included in this report, however.

SECTION II

Bi-FET OPERATIONAL AMPLIFIERS
MIL-M-38510/114

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SECTION II

Bi-FET OPERATIONAL AMPLIFIERS
MIL-M-38510/114

2.1 Background and Introduction

The initial characterization work on Bi-FET Op Amps was described in technical report RADC-TR-78-275. This report covers the completion of the characterization studies on the LF155 series devices and also includes the characterization of the LF155A precision series devices. The relationship between the generic industry and military device types is shown below:

Generic Industry Type	MIL-M-38510/114 Device Type
LF155	01
LF156	02
LF157	03
LF155A	04
LF156A	05
LF157A	06

As the name implies, "Bi-FET" stands for a mixed technology process in which bipolar and field effect transistors are combined on the same monolithic integrated circuit. Standard bipolar processing is used to make most of the circuit elements except for the top gate and channel of the J-FETs, which depend on the ion implantation process. Fabricating with matched input J-FETs which gives rise to low offset voltage and offset voltage drift is the big contribution of the ion implantation process. Obviously the Bi-FET process enables the best features of bi-polar and J-FET transistors to be incorporated into the design of the I.C. op amp.

With J-FET input transistors, the input bias currents are typically under 100 pA. Also, bandwidth and slew rate are not severely compromised by low input bias current as in the case with bipolar transistor front ends having low input bias currents.

A review of linear device applications in military systems as well as a JC-41 Committee priority list were important factors in characterizing and developing a slash sheet for this family of devices. There are seven semiconductor manufacturers making LF155 series Bi-FET op amps.

2.2 Description of Device Types

A typical schematic circuit of a Bi-FET op amp is shown in Figure 2-1. Matched J-FET transistors are used for the differential input gain stage, the input current source loads and the offset adjustment control. The drain outputs of the input P-channel J-FETs feed a differential bipolar transistor stage. Signal conversion from differential to single ended is made at the collector of Q8. Since current sources exist at both the source and drain terminals of the input J-FETs, some mechanism must also exist to deal with the excess common mode current which is sourced from Q1, but not sunk by J10 and J11. Common mode feedback from the differential bipolar stage current source to the source terminals of J1 and J2 solves this problem.

With J-FET input transistors the op amp bias currents + I_{iB}, and - I_{iB} are much smaller than is possible with bipolar transistors. Since these currents are leakage currents, they are temperature sensitive and approximately double for every 10°C increase in temperature. Low noise and good high frequency response are other benefits of the J-FET front end transistors. The single ended output signal from Q8 and its J3 current source load is further amplified by the class B output stage. This output stage is a little unusual in that a J-FET, J5, complements the other bipolar output transistors. Replacing the standard PNP output transistor with a J-FET increases the phase margin of the device and thus enhances the stability of the device for driving high capacitance loads.

Capacitor C2 is the compensation capacitor which establishes the dominant pole from which the open loop voltage gain is "rolled-off". This capacitor therefore affects the unity gain bandwidth and slew rate of the op amp. Another parameter which affects slew rate is the operating current which is available to drive the compensation capacitor. Both the operating current and the compensation capacitor are variables which the IC manufacturers can control in order to achieve a desired speed/power tradeoff. Device types 01, 02 and 03 are basically the same device with different values of compensating capacitance and/or operating current. Consequently, supply current, slew rate and gain bandwidth product are the parameters which are different between the three device types as outlined below:

Parameter	Device Type 01	02	03*	Units
Supply Current (max)	4	7	7	mA
Slew Rate (min)	2	7.5	30	V/us
Gain Bandwidth (typ) Product	5	12	50	MHz

*Device type 03 is under compensated and is not guaranteed to be stable for closed loop gains under 5 V/V.

There are design differences among the various vendor furnished LF155 series op amps. In order to reduce the effect of temperature on input bias current, one vendor has added a bias current compensation circuit as shown in Figure 2-2.

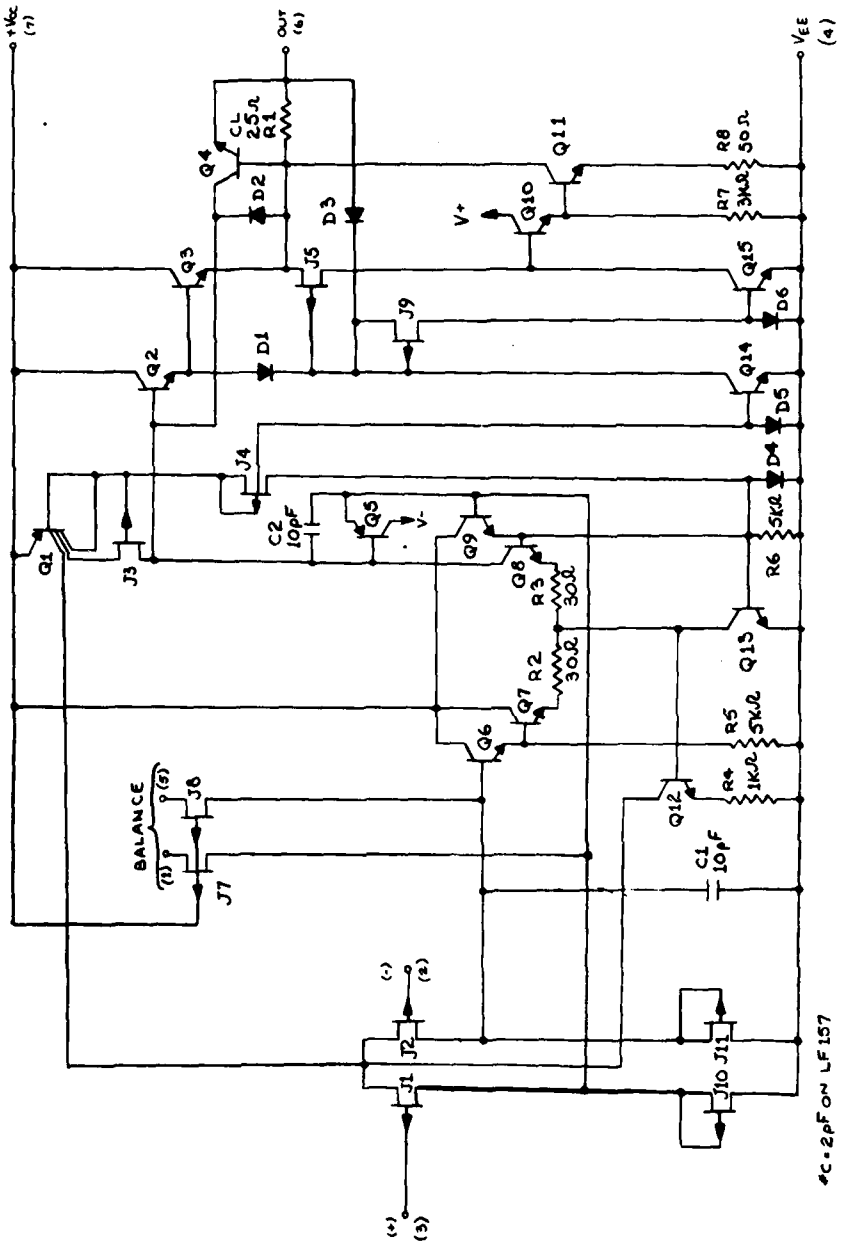


Figure 2-1. Typical Bi-FET Op Amp (LF155/156/157).

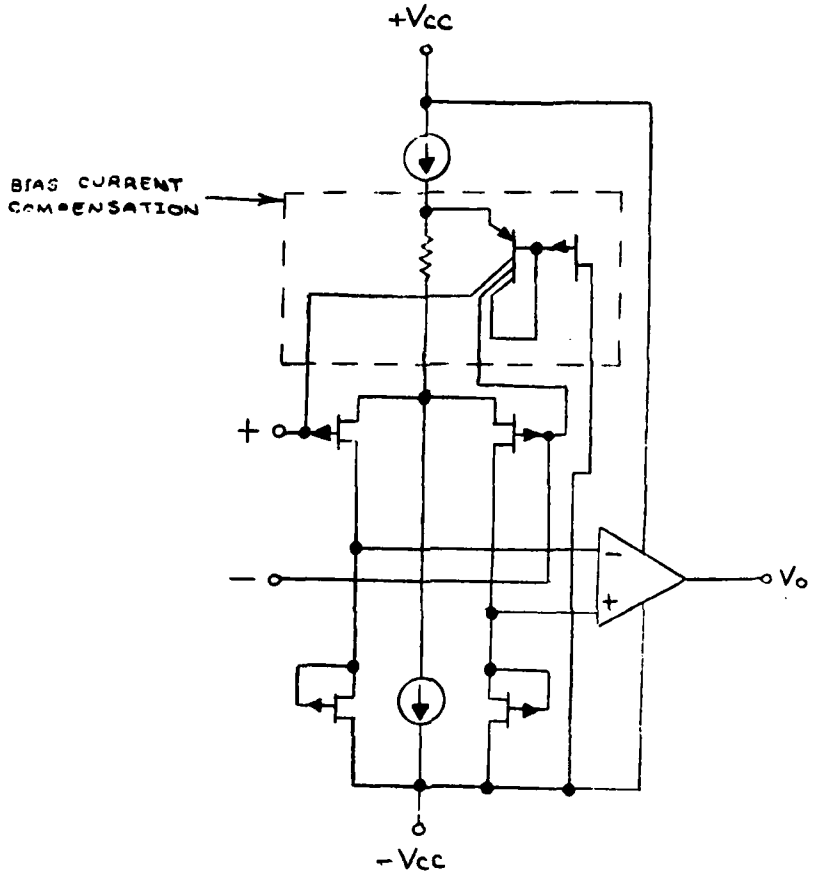


Figure 2-2. Bi-FET Op Amp With Bias Current Compensation.

2.3 Device Characterization

Developing the tests for the Bi-FET op amps was done in a manner similar to previous quad op amp characterization. A test program and an adapter card were developed in order to enable testing with GEOS' Tektronix S-3260 automatic IC test system. While the program and adapter were being developed several devices were analyzed on a Tektronix 577 curve tracer. This manual test phase was good for discovering anomalies and possible automatic tester problems.

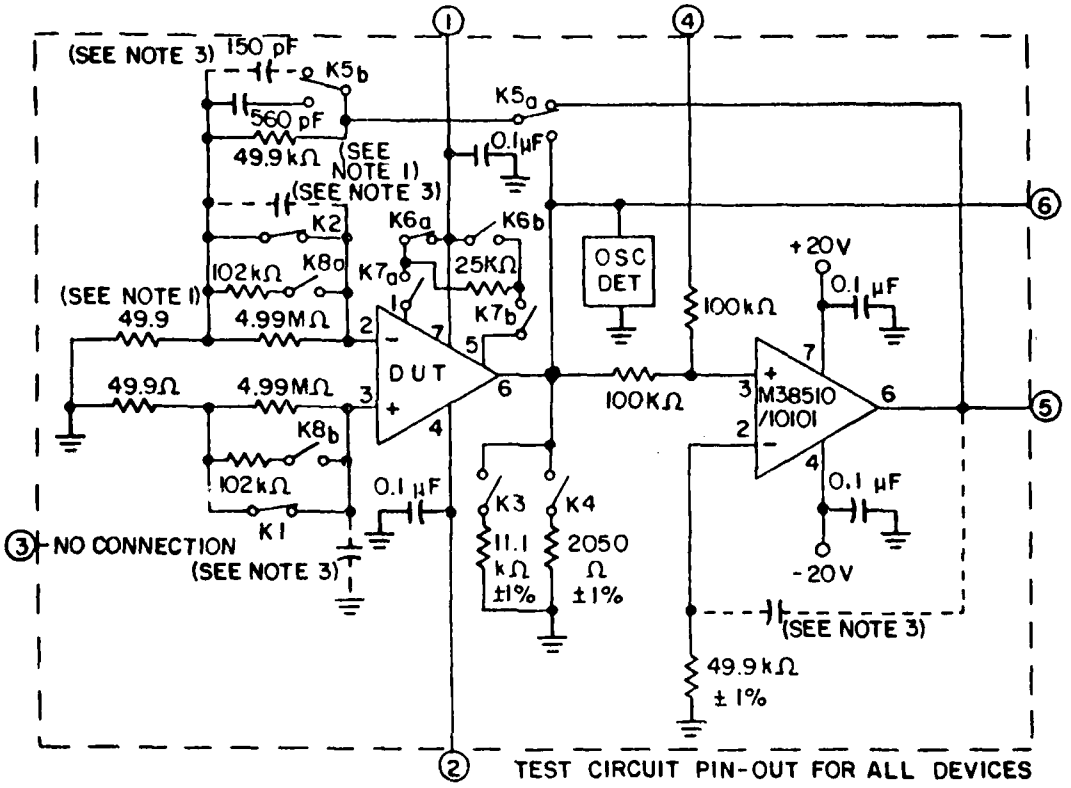
A schematic diagram of the static test circuit is shown in Figure 2-3. All relays are in the normal de-energized position. Operation of the test circuit is straight forward. The device under test (D.U.T) and the nulling amplifier are cascaded within a closed loop gain of 1000. This is done so that millivolts of error voltage with respect to the op amp input are translated into volts D.C. at the nulling amplifier output to the automatic measurement system. The D.U.T. output can be commanded to any voltage in its operating range by applying the negative of the desired voltage to terminal 4. When the non-inverting input to the nulling amplifier is at zero volts, the loop has stabilized and the correct output can be measured. Tests which require the D.U.T. to be exercised over the common mode range are mechanized by swinging the power supplies and commanding the D.U.T. output, while grounding the D.U.T. inputs through 50 ohms. The basic measurement performed by the static test circuit is V_{io} or offset voltage. Most of the other parameters are derived from this basic measurement. A schedule of parameters, test conditions and equations is shown in Table 2-1.

Because Bi-FET bias current can increase by a factor of 1000 in going from 25°C to 125°C, it is necessary to change the input sensing resistors from 5 MΩ to 100 KΩ. Relay K8 is programmed for the high temperature measurement in order to cause the resistor value to change.

Although slew rate is not a static test, it was tested automatically with the parameters listed in Table 2-1. The test circuit for slew rate and transient response is shown in Figure 2-4. It is an easy matter to incorporate this circuit into the Figure 2-3 test circuit, however, care must be taken in routing the connections to the op amp inputs. Table 2-2 shows the test conditions and equations for slew rate and transient response. Because of limitations with the S-3260 measurement system it was not possible to measure noise and transient response automatically with the other op amp parameters. Bench set ups had to be used for these measurements.

Another parameter which had to be tested manually using the circuit in Figure 2-5 is settling time.

The op amp test adapter is shown in Figure 2-6.



NOTES:

1. All resistors are ±0.1% tolerance and all capacitors are ±10%, tolerance unless otherwise specified.
2. Precautions shall be taken to prevent damage to the D.U.T. during insertion into socket and change of state of relays (i.e. disable voltage supplies, current limit ± V_{CC}, etc).
3. Compensation capacitors should be added as required for test circuit stability. Two general methods for stability compensation exist. One method is with a capacitor for nulling amp feed back. The other method is with a capacitor in parallel with the 49.9 kΩ closed loop feedback resistor. Both methods should not be used simultaneously. Proper wiring procedures shall be followed to prevent unwanted coupling and oscillations,etc. Loop response and setting time shall be consistent with the test rate such that any value has settled for at least 5 loop time constants before the value is measured.
4. Adequate settling time should be allowed such that each parameter has settled to within 5% of its final value.
5. All relays are shown in the normal de-energized state.
6. The nulling amplifier shall be a M38510/10101XXX. Saturation of the nulling amplifier is not allowed on tests where the E (pin 5) value is measured.
7. The load resistors 2050Ω and 11.1 kΩ yield effective load resistances of 2 kΩ and 10 kΩ respectively.
8. Any oscillation greater than 300 mV in amplitude (peak-to-peak) shall be cause for device failure.

Figure 2-3. Test Circuit For Static Tests

Parameter Symbol	Notes	Applied Voltages Adapter pin numbers 1	2	3	4	Energized Relays	Measured pin No.	Value	Units	Equation	Units
V_{IO}	2/	35 V	- 5 V	Open	-15 V	None	5	E_1	V	$V_{IO} = E_1$	mV
		5 V	-35 V		15 V			E_2		$V_{IO} = E_2$	
		20 V	-20 V		0 V			E_3		$V_{IO} = E_3$	
		5 V	- 5 V		0 V			E_4		$V_{IO} = E_4$	
$+I_{IB}$		5 V	-35 V		15 V	K1, K8		E_5		$-I_{IB} = 10{,}000\ (E_2 - E_5)$	pA
	8/	5 V	-25 V		10 V	None		E_6		$+I_{IB} = 200\ (E_6 - E_7)$	
		5 V	-25 V		10 V	K1		E_7			
		20 V	-20 V		0 V	K1		E_8		$+I_{IB} = 200\ (E_3 - E_8)$	
		35 V	- 5 V		-15 V	K1		E_9		$-I_{IB} = 200\ (E_1 - E_9)$	
$-I_{IB}$		5 V	-35 V		15 V	K2, K8		E_{10}		$-I_{IB} = 10{,}000\ (E_{10} - E_2)$	
	8/	5 V	-25 V		10 V	None		E_{11}		$-I_{IB} = 200\ (E_{12} - E_{11})$	
		5 V	-25 V		10 V	K2		E_{12}			
		20 V	-20 V		0 V	K2		E_{13}		$-I_{IB} = 200\ (E_{13} - E_3)$	
		35 V	- 5 V		-15 V	K2		E_{14}		$-I_{IB} = 200\ (E_{14} - E_1)$	
I_{IO}	Calculate value using V_{IO}, $+I_{IB}$ and $-I_{IB}$ data									$I_{IO} = 200\ (2E_3 - E_8 - E_{13})$	pA

Table 2-1. Test Table For Static Tests.

Parameter Symbol	Notes	Applied Voltages Adapter pin numbers 1	2	3	4	Energized Relays	Measured pin No.	Value	Units	Equation	Units
+PSRR		10 V	-20 V	Open	0 V	None	5	E_{15}	V	$+PSRR = 20 \log \frac{10^4}{(E_3 - E_{15})}$	dB
-PSRR		20 V	-10 V	Open	0 V	None		E_{16}		$-PSRR = 20 \log \frac{10^4}{(E_3 - E_{16})}$	
CMR	3/	Calculate value using V_{IO} data								$CMR = 20 \log \frac{3 \times 10^4}{(E_1 - E_2)}$	db
V_{IO} ADJ(+)		20 V	-20 V	Open	0 V	K7	5	E_{17}	V	V_{IO} ADJ(+) = $E_3 - E_{17}$	mV
V_{IO} ADJ(-)		20 V	-20 V	↓	0 V	K6, K7		E_{18}		V_{IO} ADJ(-) = $E_3 - E_{18}$	
$I_{OS}(+)$	5/	15 V	-15 V	↓	-10 V	None	6	I_1	mA	$I_{OS(+)} = I_1$	mA
$I_{OS}(-)$		15 V	-15 V	↓	10 V	None		I_2		$I_{OS(-)} = I_2$	
I_{CC}		15 V	-15 V	↓	0 V	None	2	I_3	mA	$I_{CC} = I_3$	mA
$+V_{OP}$		20 V	-20 V	Open	-20 V	K3	6	$(E_0)_1$	V	$+V_{OP} = (E_0)_1$	V
$-V_{OP}$		↓	↓	↓	20 V	K3	↓	$(E_0)_2$	↓	$-V_{OP} = (E_0)_2$	
$+V_{OP}$		↓	↓	↓	-20 V	K4	↓	$(E_0)_3$	↓	$+V_{OP} = (E_0)_3$	V
$-V_{OP}$		↓	↓	↓	20 V	K4	↓	$(E_0)_4$	↓	$-V_{OP} = (E_0)_4$	

Table 2-1. Test Table For Static Tests. (cont'd)

Table 2-1. Test Table For Static Tests. (cont'd.)

Parameter Symbol	Notes	Applied Voltages Adapter pin numbers 1	2	3	4	Energized Relays	Measured pin No.	Value	Units	Equation	Units
$A_{VS(+)}$	4/	20 V	-20 V	Open	-15 V	K4	5	E_{19}	V	$A_{VS(+)} = 15/(E_3 - E_{19})$	V/mV
$A_{VS(-)}$					15 V			E_{20}		$A_{VS(-)} = 15/(E_{20} - E_3)$	
A_{VS}		5 V	- 5 V		- 2 V			E_{21}		$A_{VS} = 4/(E_{22} - E_{21})$	V/mV
		5 V	- 5 V		2 V			E_{22}			
NI (BB)	6/	20 V	-20 V		0 V	K5	6	$(E_0)_5$	mVrms	NI (BB) = $(E_0)_5/1000$	uVrms
NI (PC)		20 V	-20 V		0 V	K1,K2,K5,K8		$(E_0)_6$	mVpk	NI (PC) = $(E_0)_6/1000$	uVpk
$\Delta V_{IO}/\Delta T$	7/	$\Delta V_{IO}/\Delta T = (V_{IO}$ @ 125°C - V_{IO} @ 25°C) /100°C									uV/°C

NOTES:

1/ The equations take into account both the closed loop gain of 1,000 and the scale factor multiplier so that the calculated value is in Table I units. The measured value units should, therefore, be used in the equation. (For example: If E_1 = 2 V and $V_{IO} = E_1$, then V_{IO} = 2 mV.)

2/ Each device shall be tested over the common mode range as specified in Table 2-1. V_{cm} conditions are achieved by grounding the inputs and algebracially subtracting V_{cm} from each supply. (For example: If V_{cm} = - 15 V, then + V_{cc} = + 20 V - (- 15) = + 35 V and - V_{cc} = - 20 V - (- 15) = - 5 V.

3/ Common mode rejection is calculated using the offset voltage values measured at the common mode range end points.

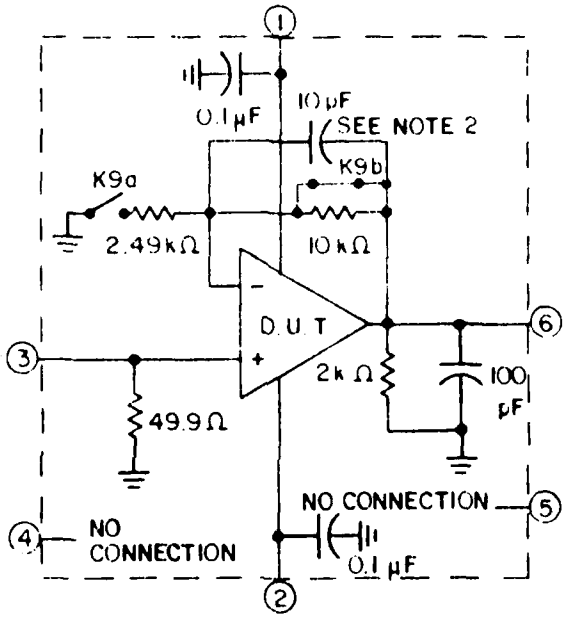
4/ To minimize thermal drift the reference voltage for the gain measurement (E_3) shall be taken immediately prior to or after the reading corresponding to device gain (E_{19}, E_{20}).

5/ The output shall be shorted to ground for 25 ms or less.

6/ Broadband noise NI(BB) shall be measured using an RMS voltmeter with a bandwidth of 10 Hz to 5 kHz. "Popcorn" noise NI(PC) shall be measured for 15 seconds.

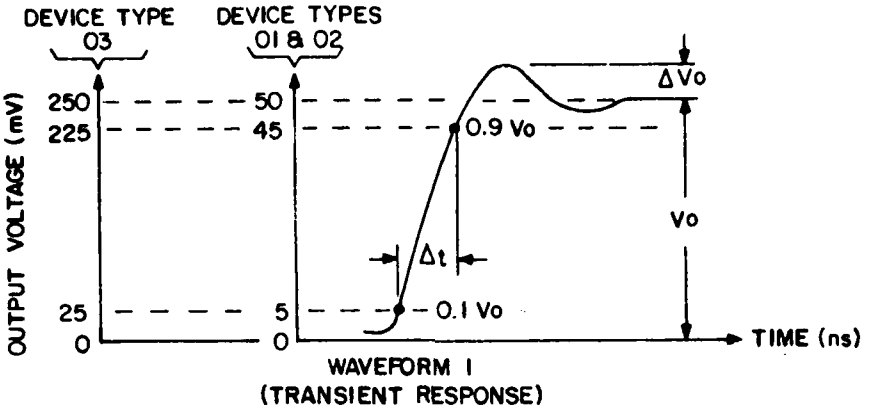
7/ $\Delta V_{io}/\Delta T$ drift between 125°C and 25°C is shown. $\Delta V_{io}/\Delta T$ drift between - 55°C and 25°C is calculated in a similar manner.

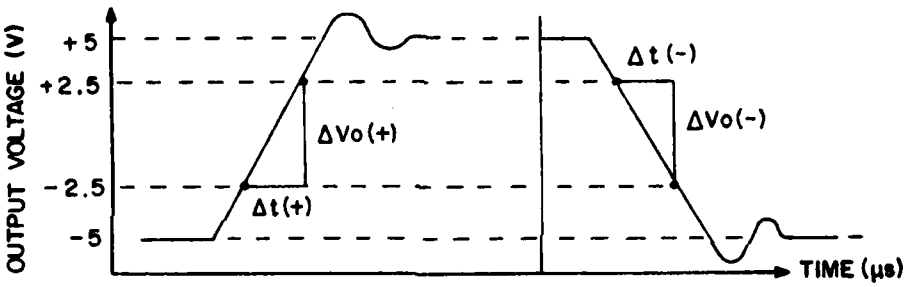
8/ For tests at 125°C, K8 is energized and the equation coefficient changes from 200 to 10,000.



NOTES:
1. Resistors are ±1.0% tolerance and capacitors are ±10% tolerance.
2. This capacitance includes the actual measured value with stray and wire capacitance.
3. Precautions shall be taken to prevent damage to the D.U.T. during insertion into socket and in applying power.
4. Pulse input and output characteristics are shown on the next page.

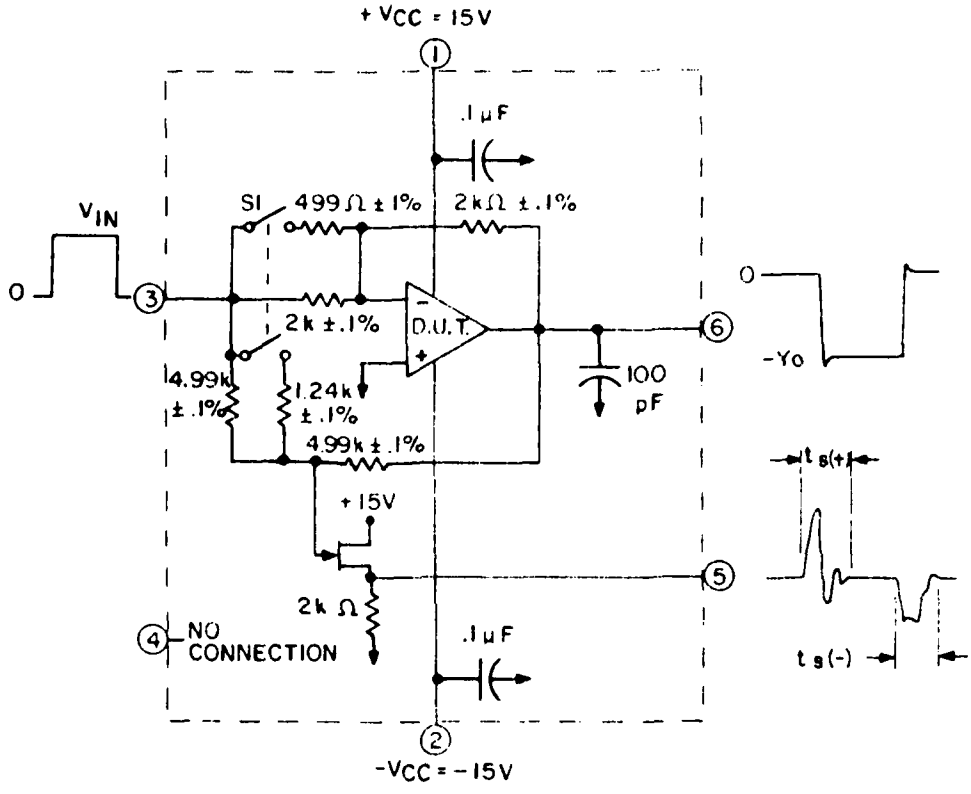
Figure 2-4. Test Circuit For Transient Response and Slew Rate.





Parameter symbol	Device type	Input pulse signal @ $t_r \leq 50$ ns	Output pulse signal	Equation
TR (t_r)	all	+50 mV	Waveform 1	TR (t_r) = Δt
TR (o_s)	all	+50 mV	Waveform 1	$TR_{(o_s)} = 100\ (^{\Delta Vo}/_{Vo})$
SR (+)	01,02	-5 V to +5 V step	Waveform 2	$SR(+) = {}^{\Delta Vo(+)}/_{\Delta t(+)}$
	03	-1 V to +1 V step	Waveform 2	
SR (-)	01,02	+5 V to -5 V step	Waveform 3	$SR(-) = {}^{\Delta Vo(-)}/_{\Delta t(-)}$
	03	-1 V to +1 V step	Waveform 3	

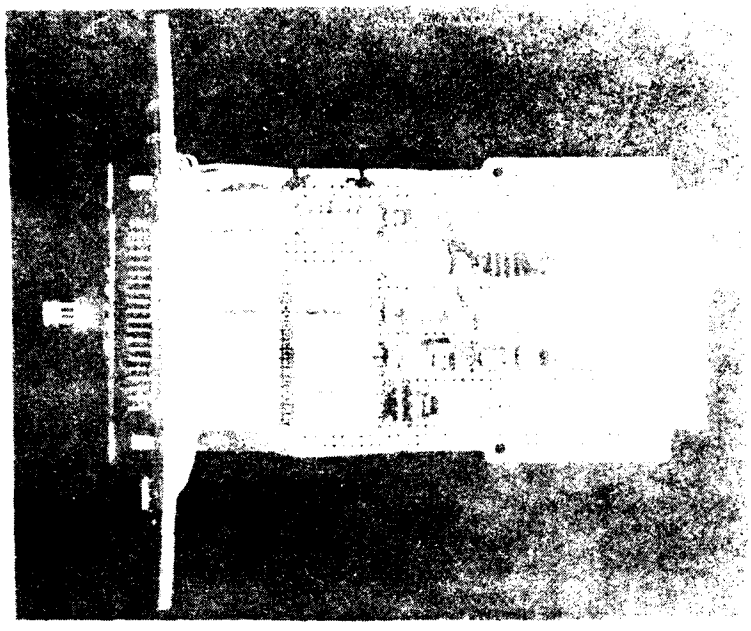
Table 2-2. Test Table For Transient Response and Slew Rate.



NOTES:

1. Resistors are ±1.0% and capacitors are ±10% unless otherwise specified.
2. Precaution shall be taken to prevent damage to the D.U.T. during insertion into socket and in applying power.
3. For device types 01 and 02, S1 is open, AV = -1 and V_{IN} = 10 V.
4. For device type 03, S1 is closed, AV = -5 and V_{IN} = 2 V.
5. Settling time t_s, measured on pin 5, is the interval during which the summing node is not nulled.

Figure 2-5. Test Circuit For Settling Time.



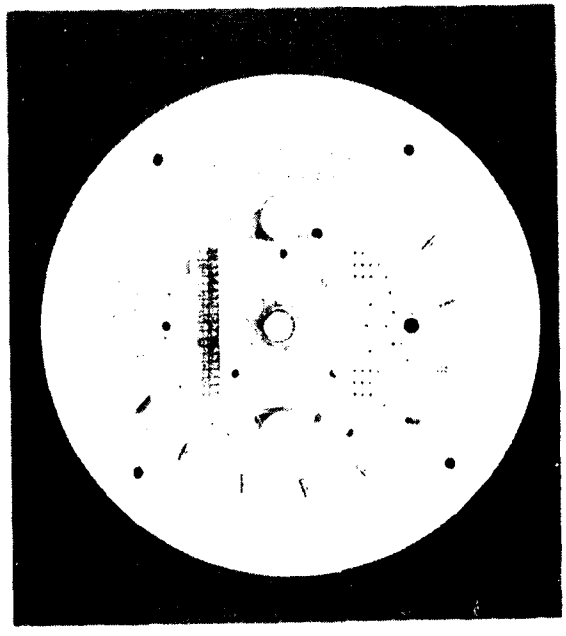


Figure 2-6. Bi-FET op amp test adapter.

2.4 Tabulation of Test Data

Shown below is a list of types and quantities of devices which were submitted by the I.C. manufacturers for characterization testing.

Device Type	Manufacturers *	Quantity
155	F, S	24
156	F, S, A	24
157	S, A, N	24
155A	N, P	9
156A	N, P, I	64
157A	P	20
355	T	9
	Total	204

* F = Fairchild
S = Signetics
A = AMD
N = National
P = P.M.I.
I = Intersil
T = Texas Instruments

The devices were tested in two groups with the distinction being A's or non-A's. The non-A's were tested first. Improved limits on offset voltage, $\Delta V_{io}/\Delta T$ and slew rate are the essential differences between the two groups. Within each group the 155's, 156's and 157's have identical limits except for supply current, transient response and slew rate. Also, the 157 is an undercompensated device for use in wideband applications with a minimum closed loop gain of 5V/V.

The 355 devices were tested with the precision A parts, but the data was not statistically grouped with those devices.

A typical data sheet of an LF155 op amp in the first group of testing is shown in Table 2-3. All of the data is within the initial JC-41 committee recommended limits, unless an asterisk (*) is displayed adjacent to the measured value. For this group, the data at all three temperatures (-55°C, 25°C and 125°C) is shown on a single table.

On the second group of devices (LF155A series), it was decided to change the format so that the data of up to ten devices could be displayed on a single sheet. Table 2-4 shows this scheme for different devices at a single temperature. With this method it is easier to make device-to-device comparisons and to check for common peculiarities, etc.

A third form of data common to both groups of devices are histograms. Figure 2-7 shows a histogram of offset voltage V_{io} at zero common mode voltage and 25°C for all of the devices in group 2. The raw data is too extensive for inclusion in this report, since each test group contains 114 histograms and over 30 individual data sheets. Besides showing the data elements v.s. frequency of occurence, the histograms also display the initial JC-41 parameter limits. Direct comparisons of the data to the proposed limits are useful in determining the relative test yields of the devices. The raw data was presented to industry representatives in two reports as follows:

1. Characterization Data for MIL-M-38510/114 Bi-FET Op Amps (Commercial Types LF155, LF156, and LF157) (21 November 1978).

2. Characterization Data for MIL-M-38510/114 Bi-FET Op Amps (Commercial Types LF155A, LF156A, and LF157A) (16 April 1979).

Within the static test parameters, the measurement and characterization of input bias current was the most difficult. Figures 2-8, 2-9 and 2-10 show how input bias current varies typically with common mode voltage, supply voltage and manufacturer. These figures were observed with a Tektronix Type 577 curve tracer. Figure 2-11 shows a similar bias current curve that was generated using the S-3260 with the op amp adapter. Increasing temperature can also cause an increase in input bias current as shown in Figures 2-12 and 2-13. The effect of common mode voltage on offset voltage is shown in figures 2-14 and 2-15. Figures 2-16 and 2-17 show typical small signal transient response waveforms of the LF155, LF156 and LF157. The effect of closed loop gain on the LF157 response is also shown.

Typical slew rate response for all device types is shown in figures 2-18 and 2-19. Settling time waveforms are shown in figure 2-20. Curve tracer displays of gain and noise are shown in figures 2-21 and 2-22.

Tables 2-5 to 2-10 are statistical data summaries of the LF155 and LF155A series devices at -55°C, 25°C and 125°C. These tables are useful in showing parameter yields to the initial specification limits.

Tables 2-11 and 2-12 show the distribution of data for most of the parameters in a cryptic histogram form.

Manual test methods were used to generate the dynamic data of the difference device types as shown in Tables 2-13, 2-14 and 2-15.

MANUFACTURER CODE: A ; DEVICE TYPE: 155 ; S/N: 4 ; DATE CODE: 0 ; 29 NOV 78 22:38:31

PARAMETER	-55 DEG C LO-LIM	-55 DEG C DATA	-55 DEG C HI-LIM	25 DEG C LO-LIM	25 DEG C DATA	25 DEG C HI-LIM	125 DEG C LO-LIM	125 DEG C DATA	125 DEG C HI-LIM	UNITS
VIO(-CM) AT 35V,-5V	-6.00	-3.26	6.00	-4.00	-1.33	4.00	-6.00	-13.3M	6.00	MV
VIO(+CM) AT 5V,-35V	-6.00	-2.62	6.00	-4.00	-840.M	4.00	-6.00	401.M	6.00	MV
VIO(@CM) AT 20V,-20V	-6.00	-2.90	6.00	-4.00	-1.10	4.00	-6.00	153.M	6.00	MV
VIO(@CM) AT 5V,-5V	-6.00	-3.23	6.00	-4.00	-1.35	4.00	-6.00	-44.9M	6.00	MV
D-VIO/D-T FROM 25 OC	-30.0	22.5	30.0				-30.0	12.5	30.0	UV/OC
IIO(-CM) AT 35V,-5V	0.00	0.00	0.00	-20.0	4.46	20.0	-20.0K	285.	20.0K	PA
IIO(+CM) AT 5V,-35V	0.00	0.00	0.00	-400.	-148.	400.	-30.0K	-3.24K	30.0K	PA
IIO(@CM) AT 20V,-20V	0.00	0.00	0.00	-20.0	-16.5	20.0	-20.0K	-1.34K	20.0K	PA
IIO(+CM) AT 5V,-25V	0.00	0.00	0.00	-20.0	-34.5	20.0	-20.0K	-1.66K	20.0K	PA
+IIB(-CM) AT 35V,-5V	0.00	0.00	0.00	-100.	11.2	100.	-10.0K	7.79K	50.0K	PA
+IIB(+CM) AT 5V,-35V	0.00	0.00	0.00	-100.	1.07K	2.00K	-10.0K	18.1K	60.0K	PA
+IIB(@CM) AT 20V,-20V	0.00	0.00	0.00	-100.	49.9	100.	-10.0K	11.8K	50.0K	PA
+IIB(+CM) AT 5V,-25V	0.00	0.00	0.00	-100.	68.8	300.	-10.0K	12.1K	50.0K	PA
-IIB(-CM) AT 35V,-5V	0.00	0.00	0.00	-100.	6.71	100.	-10.0K	7.51K	50.0K	PA
-IIB(+CM) AT 5V,-35V	0.00	0.00	0.00	-100.	1.21K	2.00K	-10.0K	21.4K	60.0K	PA
-IIB(@CM) AT 20V,-20V	0.00	0.00	0.00	-100.	66.4	100.	-10.0K	13.1K	50.0K	PA
-IIB(+CM) AT 5V,-25V	0.00	0.00	0.00	-100.	103.	300.	-10.0K	13.8K	50.0K	PA
+PSRR AT 10V,-20V	85.0	120.	0.00	85.0	110.	0.00	85.0	115.	0.00	dB
-PSRR AT 20V,-10V	85.0	112.	0.00	85.0	108.	0.00	85.0	114.	0.00	dB
CMR AT 20V,-20V	85.0	93.4	0.00	85.0	95.7	0.00	85.0	97.2	0.00	dB
V-ADJ(+) AT 20V,-20V	8.00	13.0	20.0	8.00	13.0	20.0	8.00	13.1	20.0	MV
V-ADJ(-) AT 20V,-20V	-20.0	-14.3	-8.00	-20.0	-14.3	-8.00	-20.0	-14.2	-8.00	MV
IOS(+) AT 15V,-15V	-60.0	-32.3	0.00	-60.0	-24.6	0.00	-60.0	-15.0	0.00	NA
IOS(-) AT 15V,-15V	0.00	32.9	60.0	0.00	25.2	60.0	0.00	16.7	60.0	NA
ICC AT 15V,-15V	0.00	4.49	6.00	0.00	3.60	4.00	0.00	2.95	4.00	MA
ICC AT 20V,-20V	0.00	5.56	7.00	0.00	4.11	5.00	0.00	3.31	5.00	MA
+VOP AT RL=10K	16.0	18.2	20.0	16.0	18.5	20.0	16.0	18.8	20.0	V
-VOP AT RL=10K	-20.0	-18.3	-16.0	-20.0	-18.6	-16.0	-20.0	-18.9	-16.0	V
+VOP AT RL=2K	15.0	18.0	20.0	15.0	18.2	20.0	15.0	18.5	20.0	V
-VOP AT RL=2K	-20.0	-17.6	-15.0	-20.0	-17.8	-15.0	-20.0	-17.5	-15.0	V
AVS(+) AT RL=10K	25.0	1.58K	0.00	50.0	1.00K	0.00	25.0	965.	0.00	V/MV
AVS(-) AT RL=10K	25.0	3.00K	0.00	50.0	100.K	0.00	25.0	3.33K	0.00	V/MV
AVS(+) AT RL=2K	25.0	1.50K	0.00	50.0	1.50K	0.00	25.0	690.	0.00	V/MV
AVS(-) AT RL=2K	25.0	1.50K	0.00	50.0	600.	0.00	25.0	212.	0.00	V/MV
AVS AT 5V,-5V,RL=10K	10.0	400.	0.00	10.0	100.K	0.00	10.0	173.	0.00	V/MV
AVS AT 5V,-5V,RL=2K	10.0	400.	0.00	10.0	800.	0.00	10.0	800.	0.00	V/MV
SR(+) AT 20V,-20V	2.00	11.8	0.00	2.00	9.35	0.00	2.00	7.81	0.00	V/US
SR(-) AT 20V,-20V	2.00	29.4	0.00	2.00	25.0	0.00	2.00	20.0	0.00	V/US

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 2-3 Typical LF155 Op Amp Data Sheet

BI-FET OPERATIONAL AMPLIFIERS - 155A ; TEMPERATURE: +25 DEG C ; 04 APR 79 14:46:16

Vendor Code A

PARAMETER	LO-LIM	85	86	87	88	89	90	91	92	93	94	HI-LIM	UNIT
VIO(-CM) AT 35V,-5V	-2.00	-1.68	1.38	3.47 *	436.M	-3.45 *	-678.M	8.69 *	-1.27	-3.93 *	675.M	2.00	MV
VIO(+CM) AT 5V,-35V	-2.00	-1.37	1.07	3.06 *	518.M	-3.22 *	-1.76	8.11 *	-2.00	-3.46 *	-45.8M	2.00	MV
VIO(0CM) AT 20V,-20V	-2.00	-1.43	1.13	3.23 *	489.M	-3.37 *	-1.26	8.33 *	-1.65	-3.59 *	49.4M	2.00	MV
VIO(0CM) AT 5V,-5V	-2.00	-1.69	1.34	3.41 *	615.M	-3.60 *	-816.M	2.64 *	-1.30	-4.05 *	589.M	2.00	MV
D-VIO/D-T FROM 25 OC	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	UV/C
IIO(-CM) AT 35V,-5V	-20.0	12.7	2.36	24.0 *	10.2	22.8 *	10.2	10.5	23.0 *	2.18	958.M	20.0	PA
IIO(+CM) AT 5V,-35V	-400.	-168.	-121.	-22.3	-91.2	-57.2	-96.4	-55.9	9.36	-208.	-101.	400.	PA
IIO(0CM) AT 20V,-20V	-20.0	1.26	809.M	19.4	-6.71	9.63	-7.70	5.92	18.5	-24.4 *	-8.91	20.0	PA
IIO(+CM) AT 5V,-25V	-20.0	-6.58	-3.38	18.3	-16.2	-235.M	-17.1	4.75	22.3 *	-35.4 *	-13.0	20.0	PA
+IIB(-CM) AT 35V,-5V	-100.	6.56	14.6	33.3	26.0	54.6	16.8	12.3	46.1	8.81	16.2	100.	PA
+IIB(+CM) AT 5V,-35V	-100.	1.64K	1.40K	856.	1.04K	1.17K	1.37K	1.27K	754.	1.65K	1.62K	3.50K	PA
+IIB(0CM) AT 20V,-20V	-100.	66.4	46.1	72.6	41.5	85.9	43.5	39.8	83.0	37.0	38.5	100.	PA
+IIB(+CM) AT 5V,-25V	-100.	128.	91.7	103.	74.1	118.	86.9	85.0	114.	93.7	82.7	300.	PA
-IIB(-CM) AT 35V,-5V	-100.	-6.14	12.2	9.36	15.7	31.8	6.58	1.76	23.1	6.62	15.2	100.	PA
-IIB(+CM) AT 5V,-35V	-100.	1.80K	1.52K	878.	1.13K	1.23K	1.47K	1.33K	745.	1.86K	1.62K	3.50K	PA
-IIB(0CM) AT 20V,-20V	-100.	65.1	45.3	53.2	48.2	76.2	51.2	33.9	64.5	61.3	47.4	100.	PA
-IIB(+CM) AT 5V,-25V	-100.	135.	95.1	84.8	90.3	119.	104.	80.3	91.9	129.	95.7	300.	PA
+PSRR AT 10V,-20V	85.0	117.	120.	111.	108.	108.	132.	109.	114.	115.	110.	0.00	dB
-PSRR AT 20V,-10V	85.0	110.	122.	108.	109.	106.	107.	106.	106.	200.	142.	0.00	dB
CMR AT 20V,-20V	85.0	99.7	100.	97.3	111.	102.	88.1	94.1	92.3	96.2	92.4	0.00	dB
IOS(+) AT 15V,-15V	-50.0	-19.0	-19.5	-20.9	-21.5	-20.9	-17.4	-20.4	-21.3	-19.9	-20.5	0.00	MA
IOS(-) AT 15V,-15V	0.00	18.7	19.5	21.1	21.2	18.7	17.3	20.5	20.7	19.4	20.0	50.0	MA
ICC AT 15V,-15V	0.00	3.23	3.16	3.25	3.23	2.30	3.32	3.74	3.60	2.75	3.43	4.00	MA
ICC AT 20V,-20V	0.00	3.66	3.58	3.64	3.61	2.47	3.76	4.26	4.12	3.09	3.81	5.00	MA
+VOP AT RL=10K	16.0	18.4	18.4	18.4	18.4	18.4	18.4	18.5	18.4	18.4	18.4	20.0	V
-VOP AT RL=10K	-20.0	-18.5	-18.5	-18.6	-18.5	-18.5	-18.4	-18.5	-18.6	-18.5	-18.5	-16.0	V
+VOP AT RL=2K	15.0	18.1	18.1	18.0	18.1	18.1	18.1	18.1	17.9	18.1	18.1	20.0	V
-VOP AT RL=2K	-20.0	-17.4	-17.4	-16.9	-17.1	-17.1	-17.2	-17.4	-16.5	-17.4	-17.4	-15.0	V
AVS(+) AT RL=10K	50.0	1.50K	3.00K	1.00K	1.76K	3.00K	1.50K	1.50K	750.	1.50K	968.	0.00	V/MV
AVS(-) AT RL=10K	50.0	3.00K	100.K	1.50K	6.00K	3.00K	100.K	100.K	100.K	100.K	30.0K	0.00	V/MV
AVS(+) AT RL=2K	50.0	3.00K	1.50K	1.50K	15.0K	3.00K	1.00K	1.00K	750.	1.50K	1.20K	0.00	V/MV
AVS(-) AT RL=2K	50.0	500.	600.	600.	429.	750.	429.	600.	273.	500.	508.	0.00	V/MV
AVS AT 5V,-5V,RL=10K	10.0	267.	800.	267.	148.	800.	258.	160.	114.	800.	471.	0.00	V/MV
AVS AT 5V,-5V,RL=2K	10.0	800.	800.	400.	400.	800.	1.14K	800.	267.	800.	667.	0.00	V/MV
SR(+) AT 20V,-20V	3.00	7.14	6.58	8.55	9.01	8.00	7.87	7.94	10.1	6.37	7.94	0.00	V/US
SR(-) AT 20V,-20V	3.00	18.2	14.5	21.3	23.8	21.3	18.5	18.9	21.3	13.9	16.9	0.00	V/US
V-ADJ(+) AT 20V,-20V	8.00	13.0	13.1	13.1	13.1	13.0	13.0	13.1	13.0	13.0	226.MS	20.0	MV
V-ADJ(-) AT 20V,-20V	-20.0	-14.3	-14.2	-14.2	-14.2	-14.3	-14.3	-14.2	-14.3	-14.3	-14.2	-8.00	MV

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 2-4 Typical LF155A Op Amp Data Sheet

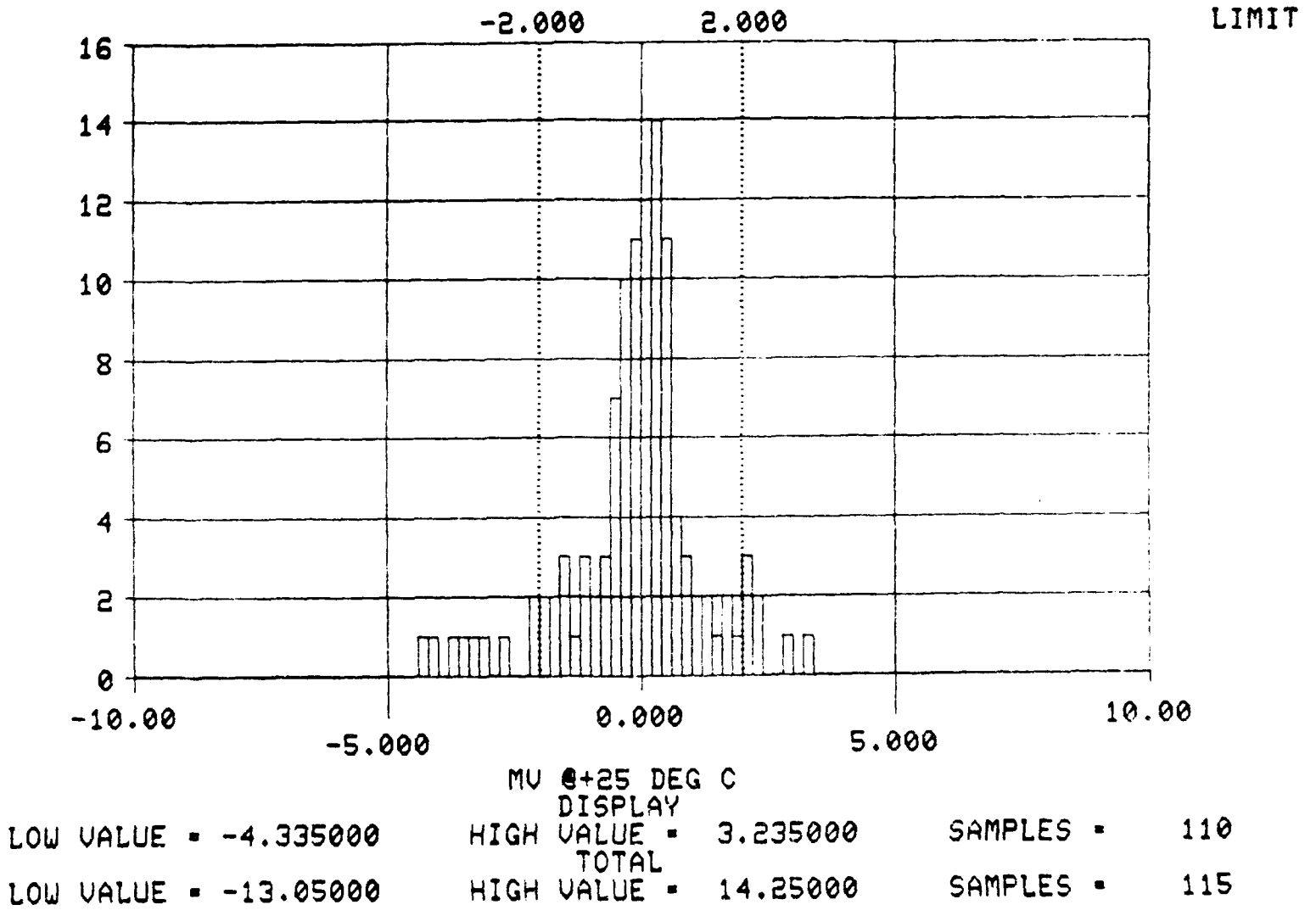
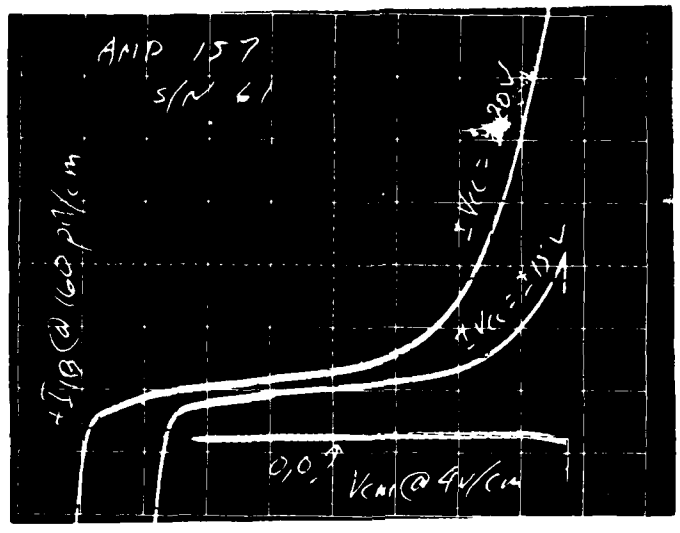
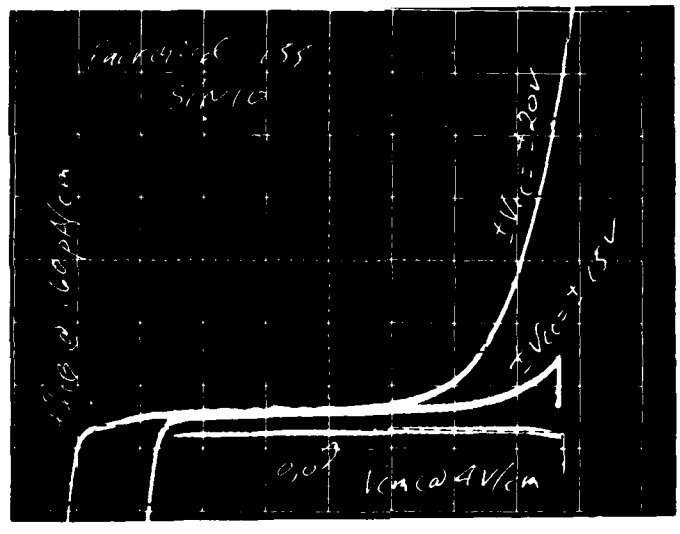


Figure 2-7 155A Series V_{IO} Histogram



$+I_{iB}$ @ 160 pA/cm

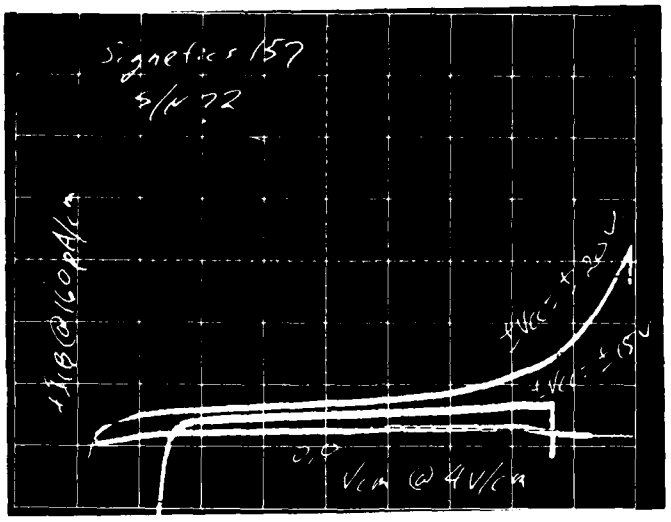
V_{cm} @ 4V/cm



$+I_{iB}$ @ 160 pA/cm

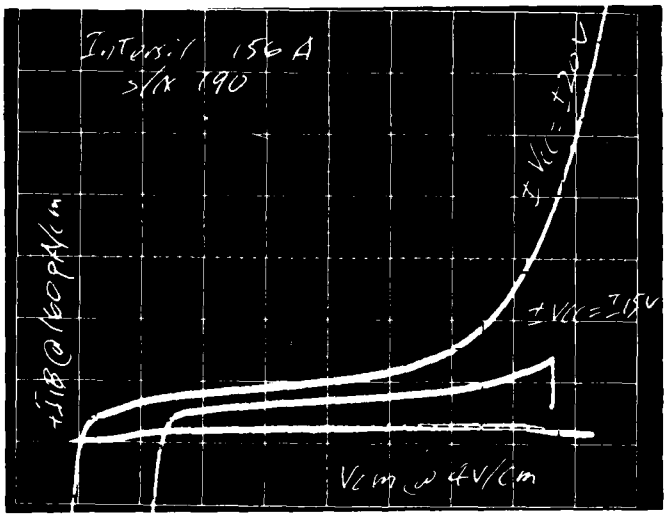
V_{cm} @ 4V/cm

Figure 2-8 Bi-FET Input Bias Current vs. Common Mode Voltage



$+I_{iB}$ @ 160 pA/cm

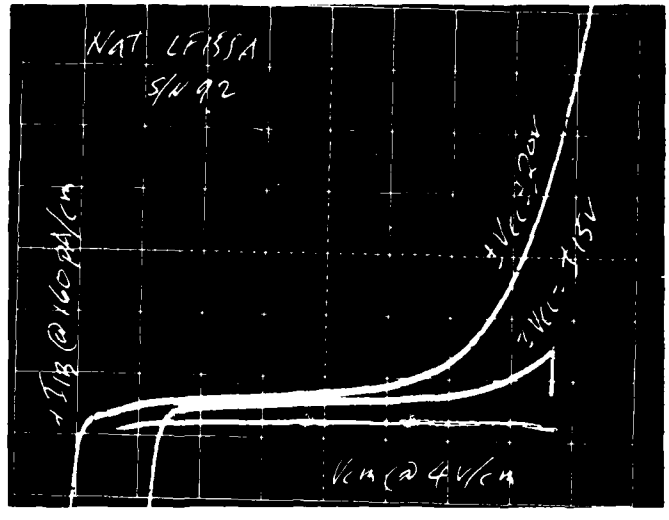
Vcm @ 4V/cm



$+I_{iB}$ @ 160 pA/cm

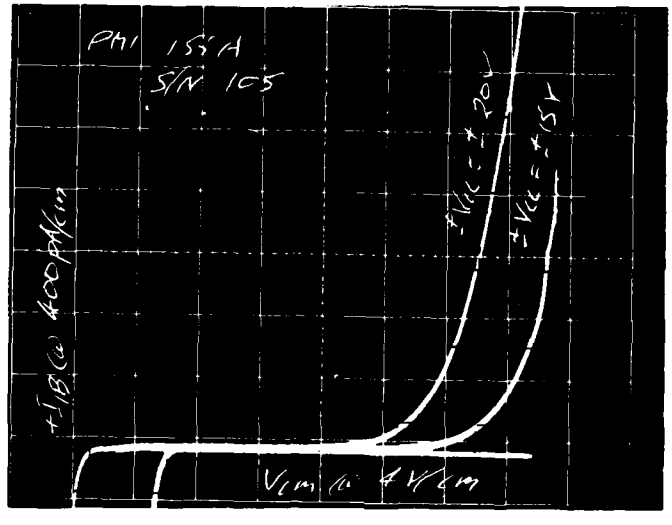
Vcm @ 4V/cm

Figure 2-9 Bi-FET Input Bias Current vs. Common Mode Voltage



$+I_{iB}$ @ 160 pA/cm

V_{cm} @ 4V/cm



$+I_{iB}$ @ 400 pA/cm

V_{cm} @ 4V/cm

Figure 2-10 Bi-FET Input Bias Current vs. Common Mode Voltage

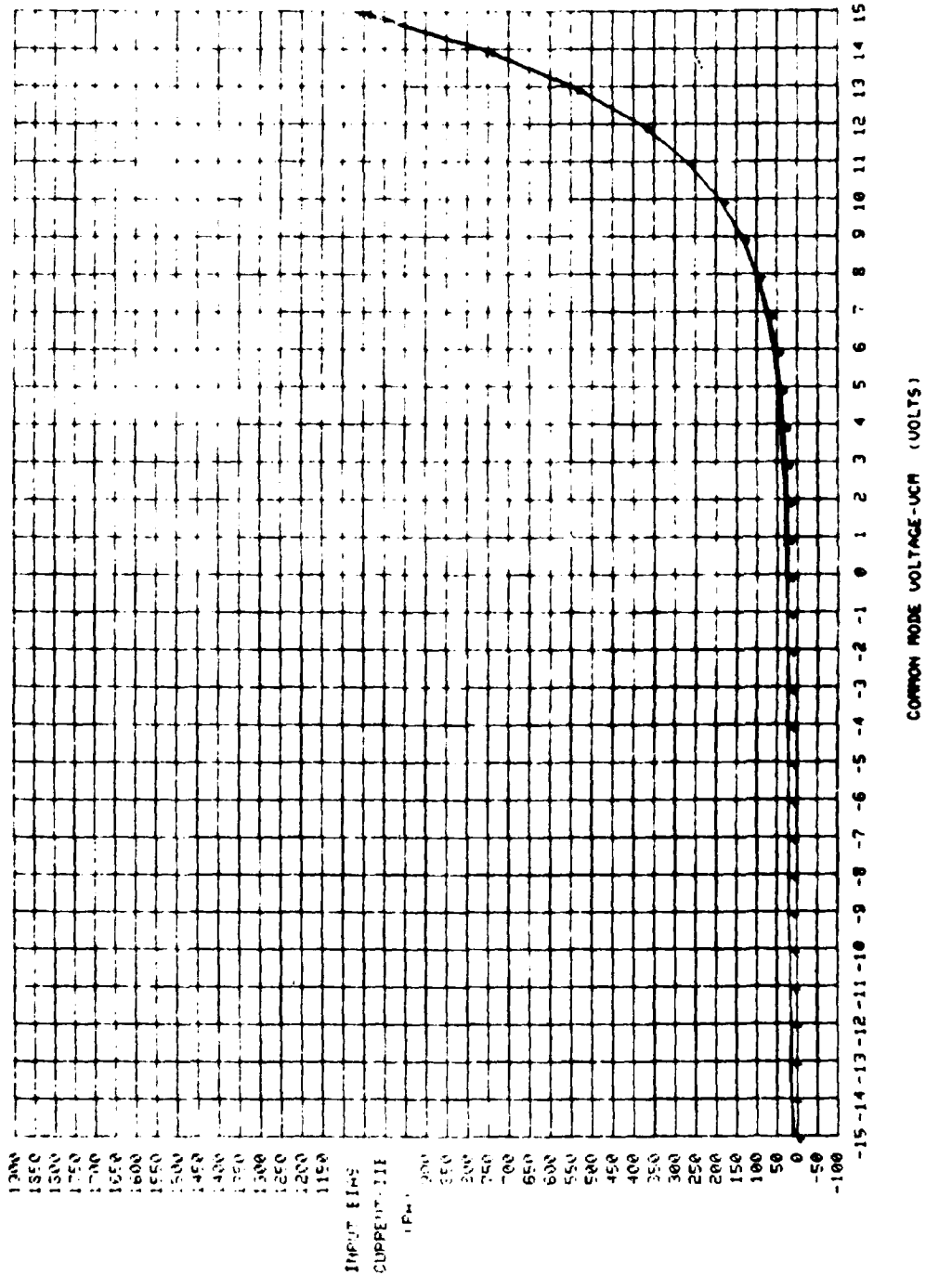
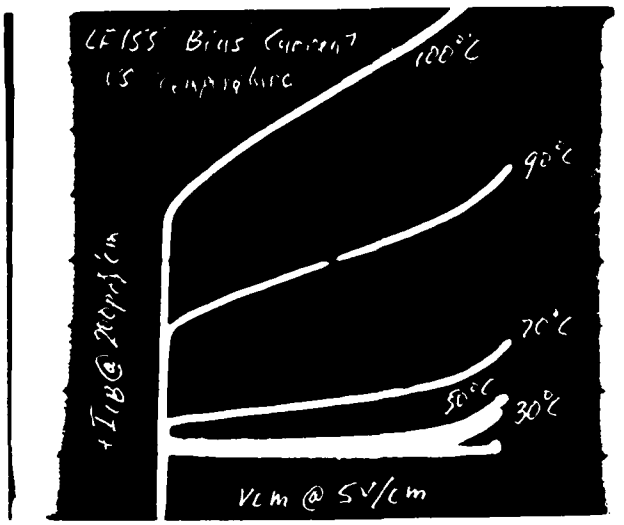


Figure 2-11 Bi-FET Input Bias Current vs. Common Mode Voltage



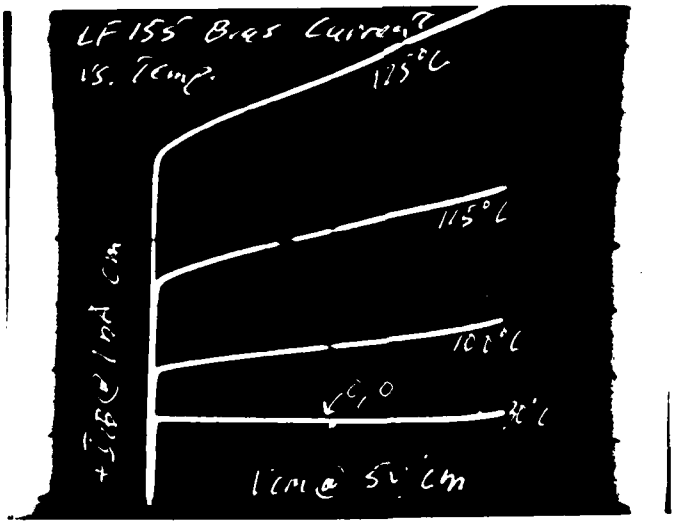
$+I_{iB}$ @ 200 pA/cm

$+I_{iB}$ = 1120 pA

@ 100°C, V_{cm} = 0V

V_{cm} @ 5V/cm

LF155 Bias Current from 30°C to 80°C



$+I_{iB}$ @ 1 nA/cm

$+I_{iB}$ = 5.2 nA

@ 125°C, V_{cm} = 0V

V_{cm} @ 5V/cm

LF155 Bias Current from 30°C to 125°C

Figure 2-12 Bi-FET Input Bias Current vs. Temperature

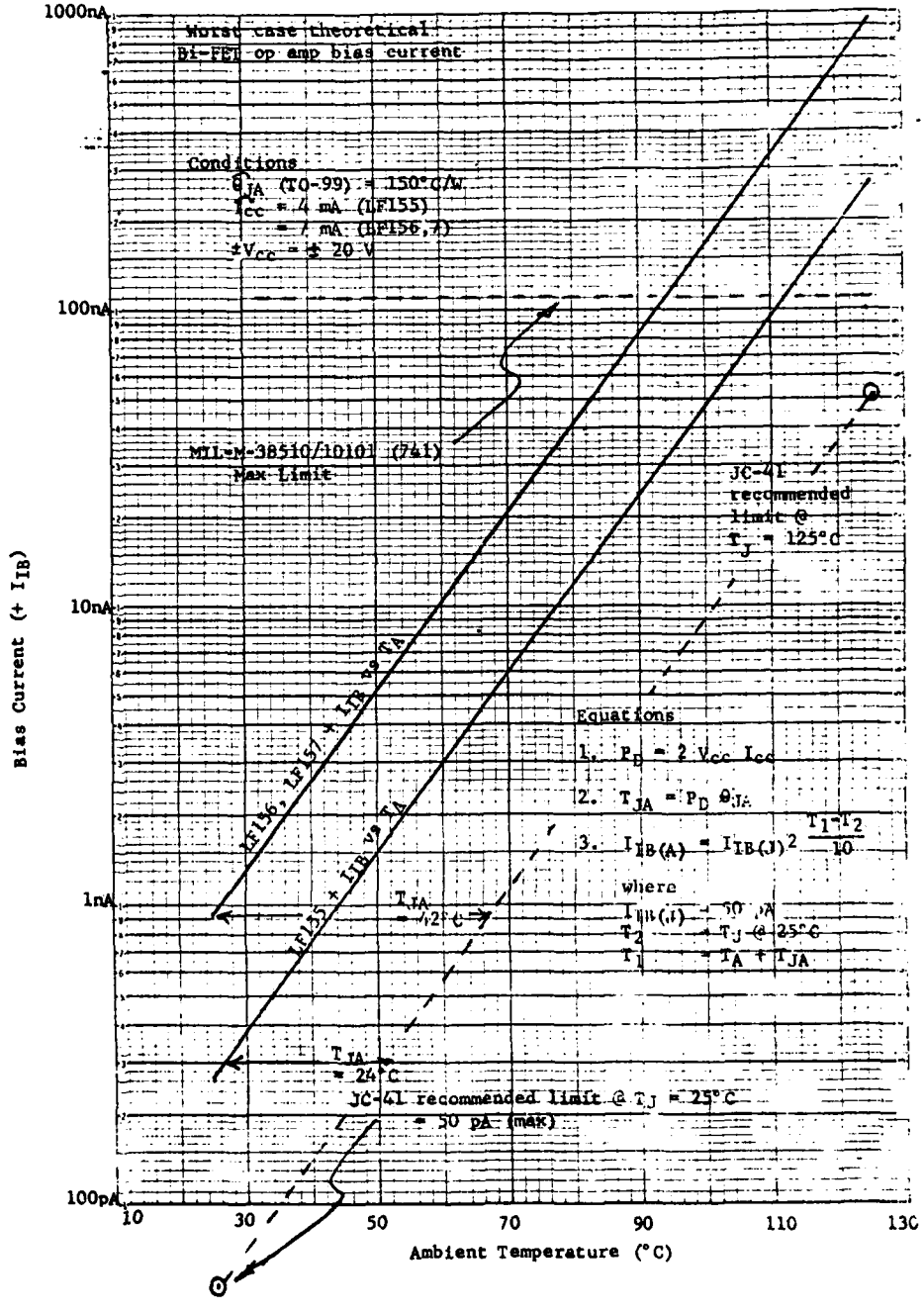


Figure 2-13. Worst Case Input Bias Current vs. Ambient Temperature.

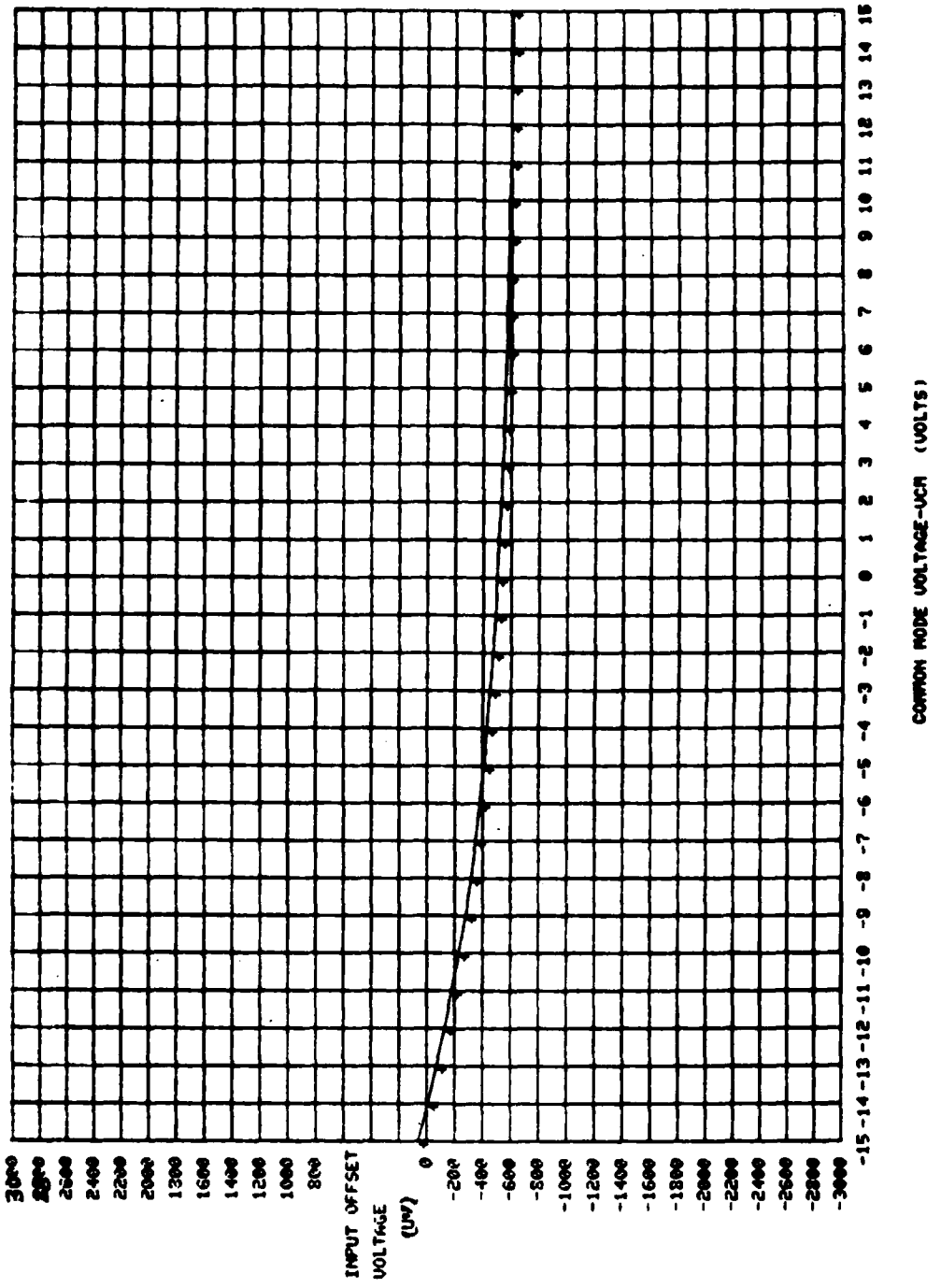


Figure 2-14. Offset Voltage vs Common Mode Voltage.

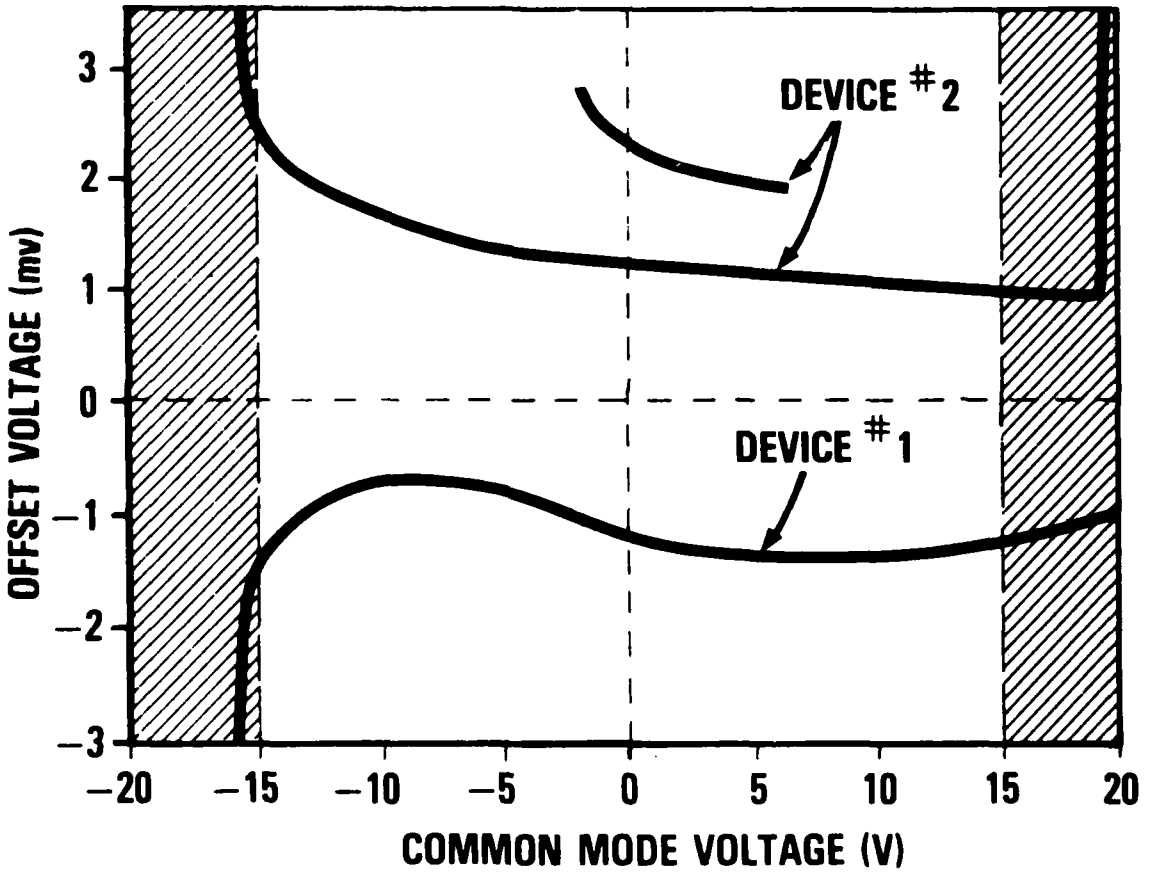
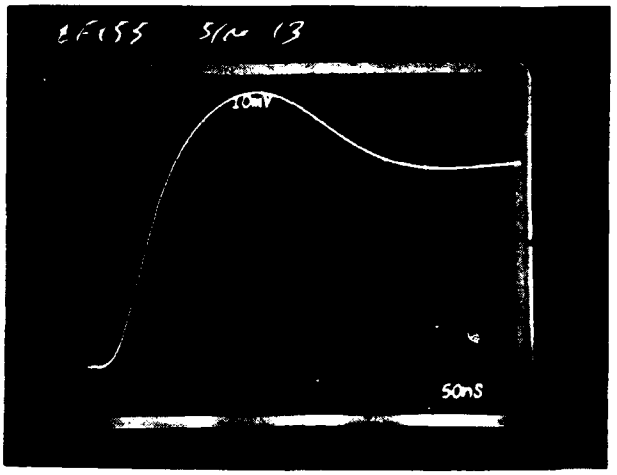
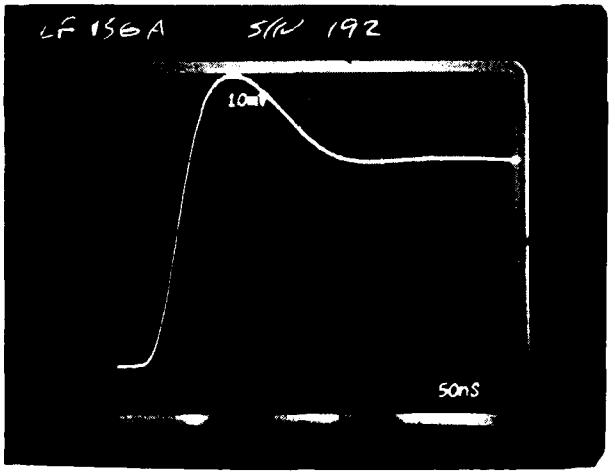


Figure 2-15. Offset Voltage vs Common Mode Voltage.

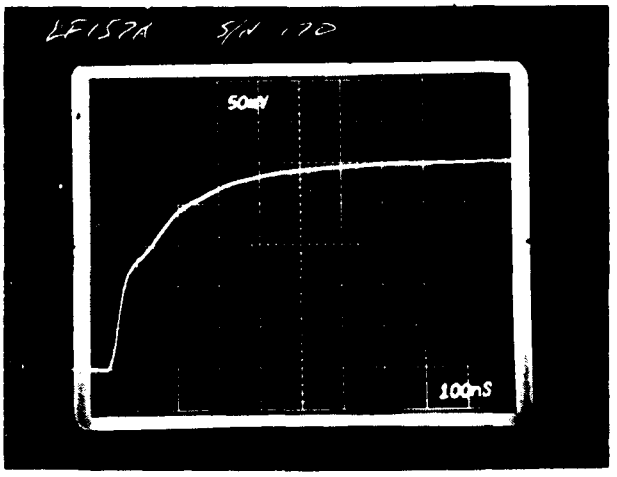


Typical LF155
TR (tr) = 60 ns
TR (OS) = 34%
GBW = 5.8 MHz
A_V = 1 V/V
TR (tr) x GBW = .348



Typical LF156A
TR (tr) = 40 ns
TR (OS) = 38%
GBW = 7 MHz
A_V = 1 V/V
TR (tr) x GBW = .350

Fig. 2-16. LF155 & LF156 Transient Response.



TR (tr) = 300 ns
TR (OS) = 0%
GBW = 1.1 MHz
A_V = 5 V/V
TR (tr) x GBW = .330

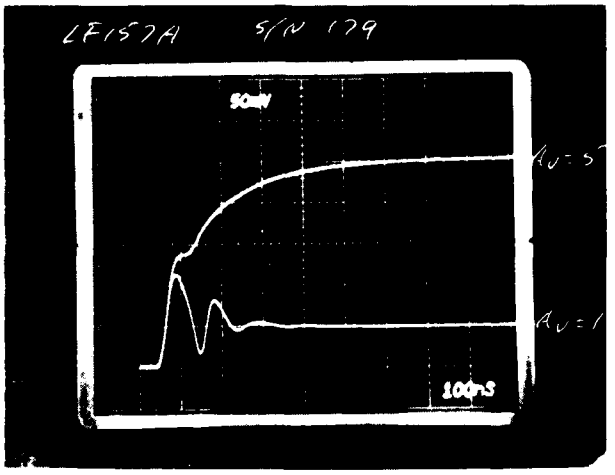
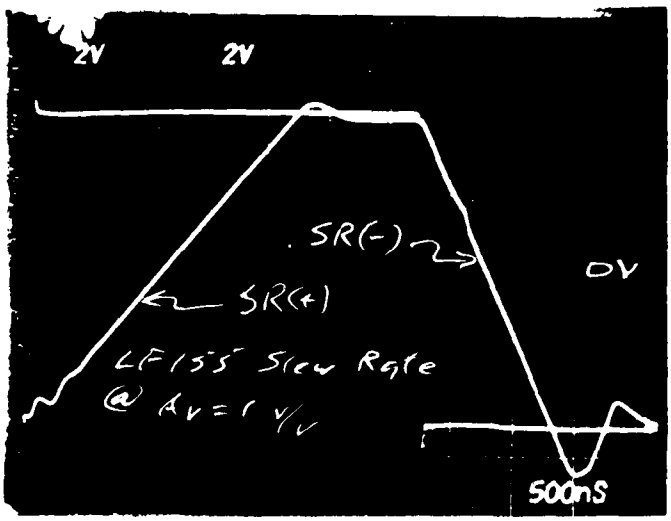


Fig. 2-17. LF157 Transient Response.



2 V/cm

500 ns/cm

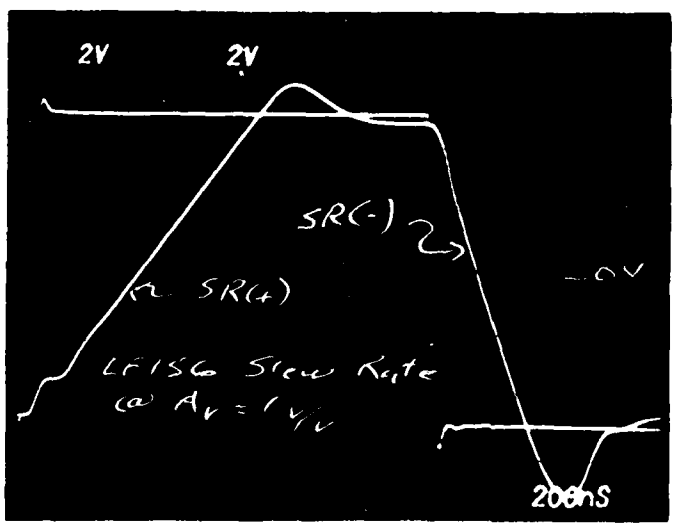
LF155 slew rates @ AV = 1 V/V

SR(+) = 4.7 V/us

SR(-) = 10 V/us

(SR = Δ V/ Δ T @

V from -2.5 V
to + 2.5 V)



2 V/cm

500 ns/cm

LF156 slew rates @ AV = 1V/V

SR(+) = 14.3 V/us

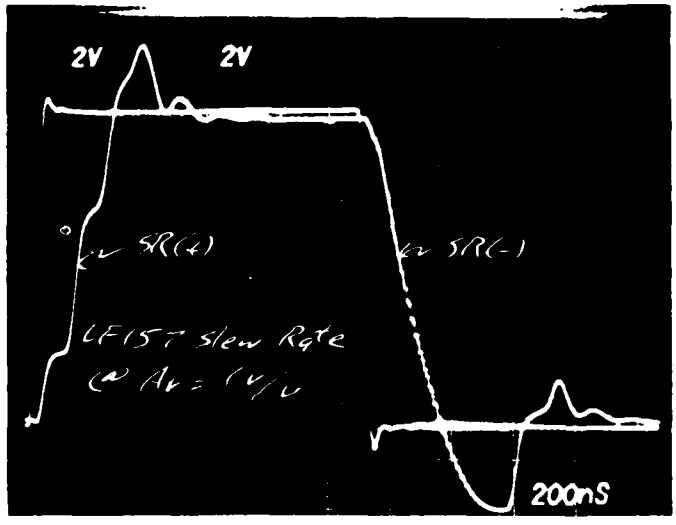
SR(-) = 33.3 V/us

(SR = Δ V/ Δ T @

V from -2.5 V to

+ 2.5 V)

Figure 2-18. LF155 and LF156 Slew Rates.

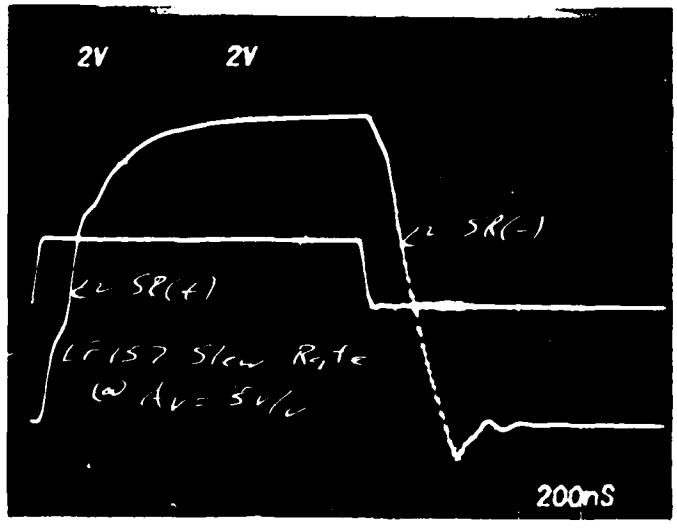


SR(+) = 40 V/us

SR(-) = 50 V/us

(SR = ΔV/ΔT @ V from - 2.5 V to + 2.5 V)

LF157 slew rates @ AV = 1 V/V



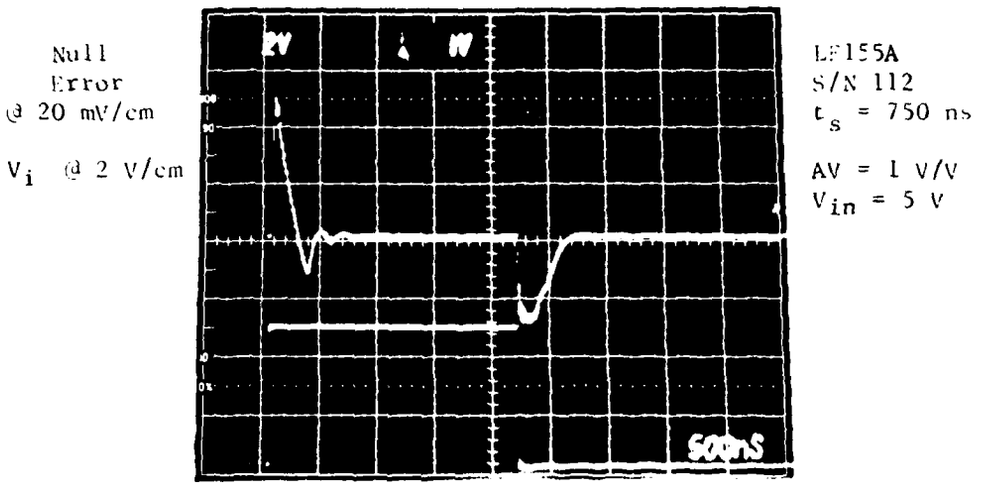
SR(+) = 33 V/us

SR(-) = 50 V/us

(SR = ΔV/ΔT @ V from - 2.5 V to + 2.5 V)

LF157 slew rates @ AV = 5 V/V

Figure 2-19. LF157 Slew Rate vs Gain.



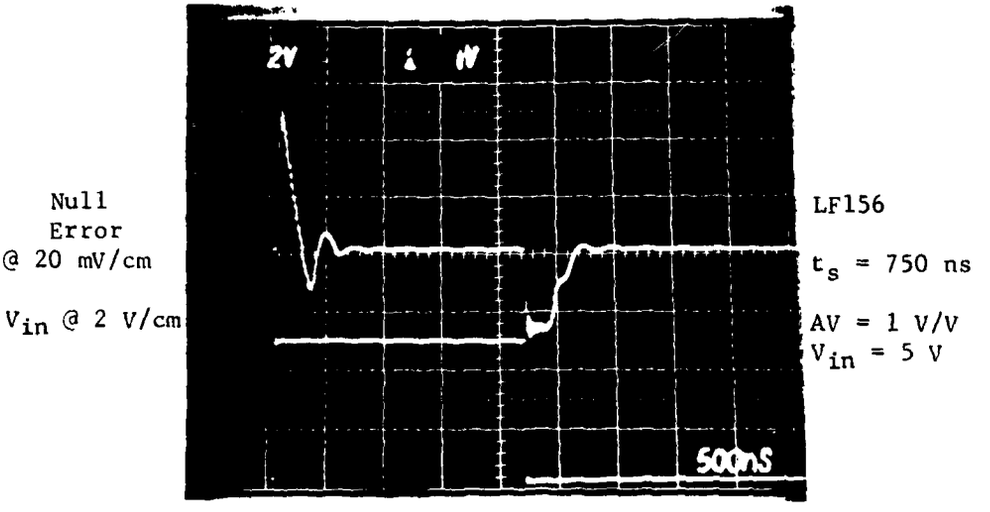
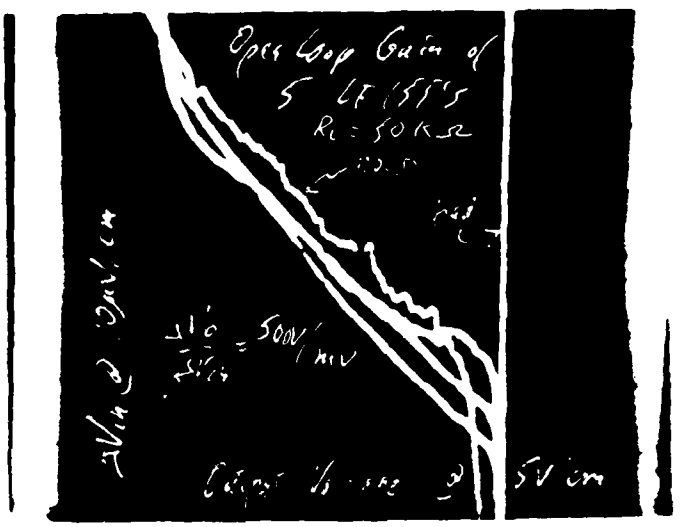


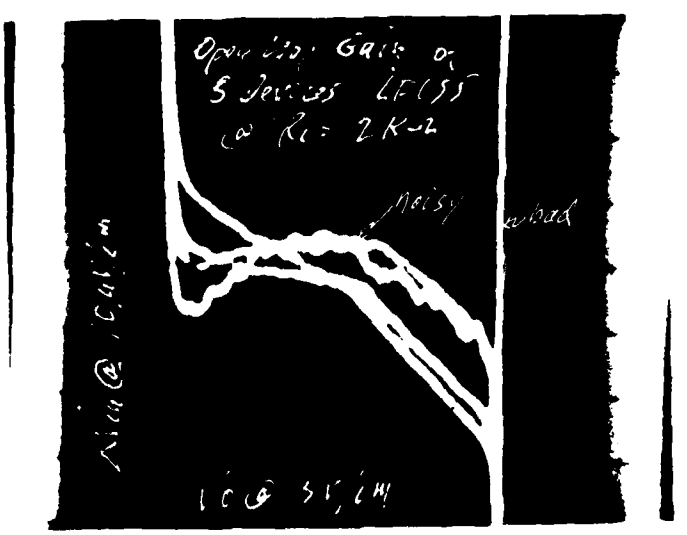
Figure 2-20. LF155 Series Bi-FET Settling Time.



V_{in} @ 10 uV/cm

V_o @ 5 V/cm

LF155 Open loop voltage gain A_{VS} (•) @ R_L = 50 KΩ

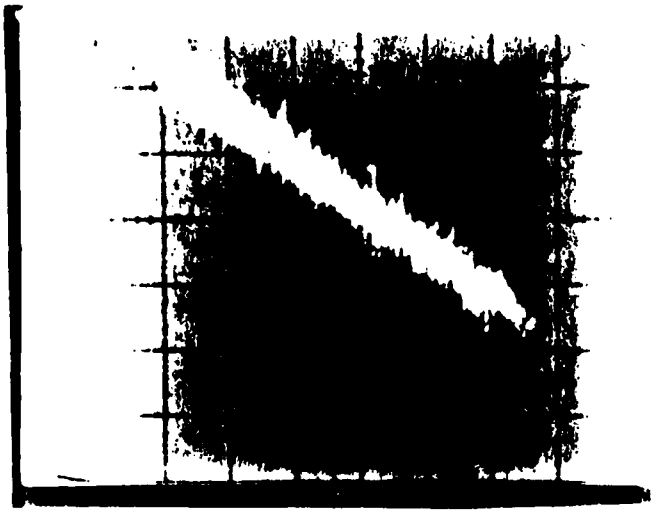


V_{in} @ 10 mV/cm

V_o @ 5 V/cm

LF155 Open loop voltage gain A_{VS} (•) @ R_L = 2 KΩ

Figure 2-21. Open Loop Voltage Gain vs Load.



ΔV_{in} @ 10 uV/cm

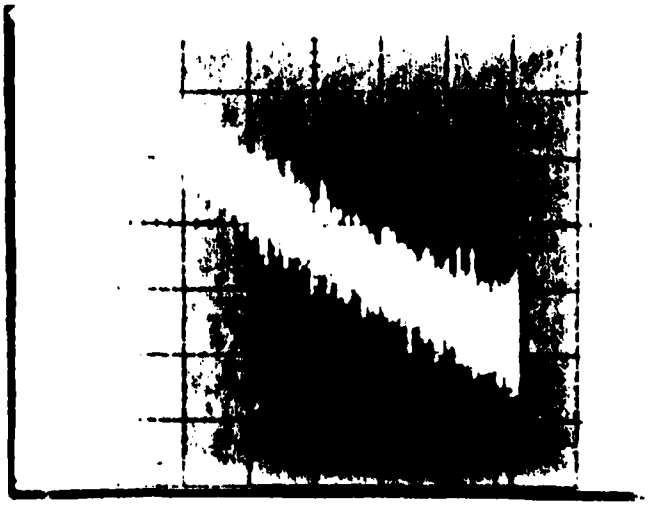
Vo @ 5V/cm

LF155
S/N 19
R_S = 50 Ω

NI(BB) = 10 uV_{pp}

= 1.67 uV_{rms}

* Note: Random noise has a Gaussian amplitude distribution such that the ratio of (peak to peak) over (rms) is 6 and will not be exceeded 99.37% of the time.



ΔV_{in} @ 10 uV/cm

Vo @ 5 V/cm

LF155
S/N 19
R_S = 50 KΩ

NI(PC) = 0 uV_{pp}

= 0 uV_{rms}

Figure 2-22. LF155 Series Bi-FET Noise Voltage.

STATISTICAL DATA [illegible] 27 JUN 79 16:29:19

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN $\bar{X}$ *	SIGMA σ *	SAMPLE SIZE *	% P/D @ 3 SIGMA	% P/D @ 3 SIGMA	% FAIL LOW 2/	LOW LIMIT	LOW REJ	LO-FM 3/ *	% FAIL HIGH 2/	HIGH LIMIT	HIGH REJ	HI-FM 3/ *	UNITS
VIO(+CM) AT 35V,-35	-4.90	4.37	574.E	2.09	52	95.2	100.	0.00	-5.00	-10.0	2.68	0.00	5.00	10.0	2.12	MV
VIO(+CM) AT 5V,-35	-4.95	7.42	701.E	2.14	52	93.5	98.0	0.00	-5.00	-10.0	2.62	1.61	5.00	10.0	1.97	MV
VIO(0CM) AT 20V,-2	-4.95	4.59	579.E	2.04	52	96.2	100.	0.00	-5.00	-10.0	2.74	0.00	5.00	10.0	2.17	MV
VIO(0CM) AT 5V,-3	-4.97	4.40	588.E	2.09	52	96.2	100.	0.00	-5.00	-10.0	2.65	0.00	5.00	10.0	2.13	MV
IIO(-CM) AT 35V,-3	-21.2	47.4	10.8	11.1	50	91.9	95.2	1.61	-20.0	-60.0	2.77	(17.7)	20.0	60.0	833.E	PA
IIO(+CM) AT 5V,-35	-594.	412.	-87.9	134.	51	93.5	93.5	3.41	-400.	-600.	2.33	1.61	400.	600.	3.64	PA
IIO(0CM) AT 20V,-2	-37.7	41.2	-7.18	10.9	52	91.9	96.2	(3.85)	-20.0	-60.0	1.18	3.23	20.0	60.0	2.50	PA
IIO(+CM) AT 5V,-35	-45.2	14.2	-20.5	11.1	50	84.7	95.2	(35.5)	-20.0	-60.0	-41.2E	1.61	20.0	60.0	3.44	PA
+IIB(-CM) AT 35V,-3	-23.5	134.	9.23	21.4	52	96.8	98.0	0.00	-100.	-100.	5.11	1.61	100.	200.	4.25	PA
+IIB(+CM) AT 5V,-35	122.	2.93K	947.	717.	52	95.2	100.	0.00	-100.	-300.	1.49	0.00	3.50K	5.00K	3.54	PA
+IIB(0CM) AT 20V,-2	1.10	97.9	27.4	19.9	52	91.9	93.5	0.00	-100.	-100.	6.40	3.23	100.	200.	3.44	PA
+IIB(+CM) AT 5V,-35	14.9	288.	55.2	46.8	51	93.5	96.1	0.00	-100.	-100.	3.32	1.61	300.	400.	5.23	PA
-IIB(-CM) AT 35V,-3	-27.7	34.5	-2.42	13.1	51	90.3	98.0	1.61	-100.	-100.	7.46	0.00	100.	200.	7.83	PA
-IIB(+CM) AT 5V,-35	152.	3.01K	1.07K	768.	52	98.0	100.	0.00	-100.	-300.	1.53	0.00	3.50K	5.00K	3.19	PA
-IIB(0CM) AT 20V,-2	-41.1	172.	34.8	25.8	51	95.2	96.8	0.00	-100.	-100.	5.30	3.23	100.	200.	2.85	PA
-IIB(+CM) AT 5V,-35	31.1	206.	73.8	38.5	51	91.9	95.2	0.00	-100.	-100.	4.52	1.61	300.	400.	5.88	PA
+PSRR AT 10V,-20V	100.	136.	118.	7.46	50	90.3	95.2	0.00	95.0	60.0	4.38	0.00	2.00K	140.	252.	DB
-PSRR AT 20V,-10V	98.0	140.	117.	8.52	50	90.3	95.2	0.00	85.0	60.0	3.71	0.00	2.00K	140.	221.	DB
CMR AT 20V,-20V	74.0	130.	102.	9.49	52	94.8	100.	1.61	85.0	60.0	1.80	0.00	2.00K	140.	196.	DB
V-ADJ(+) AT 20V,-2	13.0	13.1	13.1	2.04E	52	95.2	100.	0.00	8.00	0.00	2.48K	0.00	200.	20.0	91.7K	MV
V-ADJ(-) AT 20V,-2	-14.3	-14.2	-14.2	2.04E	52	95.2	100.	0.00	-200.	-20.0	91.1K	0.00	-8.00	0.00	3.07K	MV
IOS(+) AT 15V,-15	-27.9	-18.1	-22.1	1.81	52	93.5	98.0	0.00	-50.0	-60.0	15.2	0.00	1.00K	0.00	556.	NA
IOS(-) AT 15V,-15V	2.50	28.6	22.7	3.13	52	98.0	98.0	0.00	-1.00K	0.00	327.	0.00	50.0	60.0	8.72	NA
ICC AT 15V,-15V	2.20	6.75	4.37	1.21	51	98.0	98.0	----	----	2.00	----	58.1 4/	4.00	8.00	-308.E	MA
+VOP AT RL=10K	14.4	14.5	14.4	38.54	52	100.	100.	0.00	10.0	16.0	43.0	0.00	200.	20.0	8.71K	V
-VOP AT RL=10K	-14.7	-17.7	-14.5	152.4	52	96.8	98.0	0.00	-200.	-20.0	1.19K	0.00	-16.0	-16.0	16.0	V
+VOP AT RL=2K	14.1	14.3	14.2	47.6E	52	100.	100.	0.00	15.0	15.0	66.7	0.00	200.	20.0	3.82K	V
-VOP AT RL=2K	-17.8	-17.3	-17.6	114.4	51	98.0	98.0	0.00	-200.	-20.0	1.50K	1.61	-15.0	-15.0	22.8	V
AVS(+) AT RL=10K	375.	6.00K	1.82K	1.07K	50	90.3	91.9	0.00	50.0	0.00	1.66	4.84	100.K	10.0K	92.0	V/MV
AVS(-) AT RL=10K	1.50K	10.0K	3.29K	1.72K	51	54.5	59.7	0.00	50.0	0.00	1.88	29.0 5/	100.K	10.0K	54.2	V/MV
AVS(+) AT RL=2K	218.	4.29K	1.53K	918.	51	93.5	96.8	0.00	50.0	0.00	1.61	3.23	100.K	10.0K	107.	V/MV
AVS(-) AT RL=2K	1.0K	6.00K	930.	1.00K	50	87.1	95.2	1.61	50.0	0.00	878.E	0.00	100.K	10.0K	98.8	V/MV
AVS AT 5V,-5V,RL=10K	39.1	1.00K	271.	198.	57	85.5	88.7	0.00	10.0	0.00	1.32	1.84	10.0K	1.00K	49.1	V/MV
AVS AT 5V,-5V,RL=2K	80.0	800.	456.	286.	46	74.2	74.2	0.00	10.0	0.00	1.56	14.1	10.0K	1.00K	33.3	V/MV
SR(+) AT 20V,-20V	4.20	11.8	7.50	1.89	43	67.7	69.8	0.00	2.00	2.00	2.90	30.6 5/	25.0	25.0	9.25	V/US
SR(-) AT 20V,-20V	8.13	25.0	17.9	5.08	26	50.0	53.2	0.00	2.00	2.00	3.13	41.3	25.0	25.0	1.40	V/US

NOTES: 1/ * Excludes population outside of low rej and high rej

2/ % fail values $\geq$ 5% are circled ◯.

3/ Figure of merit definitions:

$$LO - FM = \frac{\bar{X} - \text{low limit}}{\sigma}$$

$$HI - FM = \frac{\text{High limit} - \bar{X}}{\sigma}$$

4/ The % fail for I_{cc} and SR on this table are not valid since all device types are compared to type 01 limits.

5/ There is no maximum fail limit for gain and slew rate.

Table 2-5. 25°C Statistical Summary for LF155 Series Devices.

STATISTICAL DATA FOR 2[illegible] LOT FET OP AMP @ -55 DEGREES C 27 JUN 79 14:35:27

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN $\bar{X}$ *	SIGMA σ *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW 2/	LOW LIMIT	LOW REJ	LO-FM 3/ *	% FAIL HIGH 2/	HIGH LIMIT	HIGH REJ	HI-FM 3/ *	UNITS
VIO(+) AT 15V,-5V	-4.74	5.21	501.M	2.71	62	98.4	100.	0.00	-7.00	-10.0	2.76	0.00	7.00	10.0	2.39	MV
VIO(+) AT 5V,-15V	-4.37	5.0K	522.M	2.41	61	95.2	98.4	0.00	-7.00	-10.0	3.12	1.61	7.00	10.0	2.AB	MV
VIO(20V) AT 20V,-20V	-4.59	5.11	493.M	2.5K	62	98.4	100.	0.00	-7.00	-10.0	2.93	0.00	7.00	10.0	2.5M	MV
VIO(20V) AT 5V,-5V	-5.1M	7.09	51K.M	2.83	62	95.2	100.	0.00	-7.00	-10.0	2.66	1.61	7.00	10.0	2.29	MV
V-AVIO(+) AT 20V,-20V	13.0	13.1	13.1	2.5M*	62	98.4	100.	0.00	8.00	0.00	1.97K	1.00	200.	20.0	73.0K	MV
V-AVIO(-) AT 20V,-20V	-14.3	-14.2	-14.2	2.5M*	62	98.4	100.	0.00	-200.	-20.0	72.4K	0.00	-8.00	0.00	2.00K	MV
IOS(+) AT 15V,-15V	-35.1	-23.0	-29.8	2.19	62	95.2	100.	0.00	-50.0	-60.0	8.53	0.00	1.00K	0.00	414.	MA
IOS(-) AT 15V,-15V	2.30	36.0	20.4	4.11	62	98.4	98.4	0.00	-1.00K	0.00	251.	0.00	50.0	50.0	5.01	MA
ICC AT 15V,-15V	2.4M	7.82	5.1M	1.40	56	90.3	98.4	----	----	2.00	----	3M.7 4/	4.00	4.00	5AQ.M	MA
+VOP AT RL=10K	14.1	14.3	14.2	30.94	62	93.5	100.	0.00	14.0	14.0	70.4	0.00	200.	20.0	5.89K	V
-VOP AT RL=10K	-14.0	-14.0	-14.3	80.3M	62	95.2	98.4	0.00	-200.	-20.0	2.2AK	0.00	-14.0	-14.3	28.3	V
+VOP AT RL=2K	17.0	18.0	17.9	27.3M	62	80.3	100.	0.00	15.0	15.0	108.	0.00	200.	20.0	6.AAK	V
-VOP AT RL=2K	-17.7	-17.3	-17.5	AA.11	61	96.8	98.4	0.00	-200.	-20.0	2.07K	1.61	-15.0	-15.0	28.3	V
AVS(+) AT RL=10K	273.	5.2AK	1.72K	9AA.	51	80.4	80.4	0.00	25.0	0.00	1.75	0.00	135.K	10.0K	107.	V/MV
AVS(-) AT RL=10K	375.	10.0K	3.00K	1.75K	42	64.5	66.1	0.00	25.0	0.00	1.75	0.00	135.K	10.0K	5A.4	V/MV
AVS(+) AT RL=2K	211.	4.20K	1.08K	949.	54	82.3	87.1	0.00	25.0	0.00	1.47	0.00	105.K	10.0K	105.	V/MV
AVS(-) AT RL=2K	1.91	7.50K	1.84K	1.52K	56	85.5	87.1	1.61	25.0	0.00	93A.M	0.00	135.K	10.0K	AA.3	V/MV
AVS AT 5V,-5V,RL=10K	27.0	400.	19A.	11A.	45	72.6	72.6	0.00	10.0	0.00	1.57	0.00	105.K	500.	8A7.	V/MV
AVS AT 5V,-5V,RL=2K	53.3	400.	25A.	119.	33	54.8	54.8	0.00	10.0	0.00	2.25	0.00	105.K	500.	940.	V/MV
SR(+) AT 20V,-20V	8.15	14.9	9.00	2.7M	43	67.7	69.3	0.00	1.00	0.00	2.AA	10.4 5/	50.0	25.0	14.A	V/US
SR(-) AT 20V,-20V	9.71	25.0	14.A	4.A7	16	30.6	46.A	0.00	1.00	0.00	3.24	33.9	50.0	25.0	A.A2	V/US

NOTES: 1/ * Excludes population outside of low rej and high rej

2/ % fail values $\geq$ 5% are circled ◯.

3/ Figure of merit definitions:

$$LO - FM = \frac{\bar{X} - \text{low limit}}{\sigma}$$

$$HI - FM = \frac{\text{High limit} - \bar{X}}{\sigma}$$

4/ The % fail for I_{cc} and SR on this table are not valid since all device types are compared to type 01 limits.

5/ There is no maximum fail limit for gain and slew rate.

Table 2-6. -55° Statistical Summary For [illegible]155 Series Devices.

STATISTICAL DATA FOR (REF) DUT FET OP AMP @ +125 DEGREES C 27 JUN 79 16:39:49

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN $\bar{X}$ *	SIGMA σ *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW 2/	LOW LIMIT	LOW REJ	LO-FM 3/ *	% FAIL HIGH 2/	HIGH LIMIT	HIGH REJ	HI-FM 3/ *	UNITS
VIO(+CM) AT 35V,-5V	-4.59	7.48	940.U	2.36	62	93.5	100.	0.00	-7.00	-10.0	3.36	1.61	7.00	10.0	2.56	MV
VIO(+CM) AT 5V,-35V	-4.53	5.20	329.U	2.27	60	90.3	96.8	1.61	-7.00	-10.0	3.45	1.61	7.00	10.0	2.72	MV
VIO(OCM) AT 20V,-20V	-5.12	4.73	689.U	2.23	61	93.5	98.4	0.00	-7.00	-10.0	3.44	1.61	7.00	10.0	2.82	MV
VIO(OCM) AT 5V,-5V	-4.72	8.14	868.U	2.26	62	95.2	98.4	0.00	-7.00	-10.0	3.48	1.61	7.00	10.0	2.72	MV
IIO(-CM) AT 35V,-5V	-36.1K	37.9K	2.31K	8.52K	61	91.9	95.2	1.61	-20.0K	-40.0K	2.62	8.84	20.0K	40.0K	2.07	PA
IIO(+CM) AT 5V,-35V	-39.6K	24.3K	140.	8.18K	58	88.7	90.3	6.45	-30.0K	-40.0K	3.69	1.61	30.0K	40.0K	3.65	PA
IIO(OCM) AT 20V,-20V	-32.4K	30.6K	1.00K	7.46K	61	93.5	93.5	1.61	-20.0K	-40.0K	2.82	8.84	20.0K	40.0K	2.54	PA
IIO(+CM) AT 5V,-25V	-31.2K	36.1K	176.	7.18K	60	91.9	93.5	1.61	-20.0K	-40.0K	2.81	8.84	20.0K	40.0K	2.76	PA
+IIB(-CM) AT 35V,-5V	2.01K	78.3K	20.4K	21.6K	53	90.3	96.8	0.00	-10.0K	-10.0K	1.43	17.7	50.0K	80.0K	1.35	PA
+IIB(+CM) AT 5V,-35V	-2.21	77.0K	21.1K	18.4K	48	72.6	75.8	0.00	-10.0K	-10.0K	1.69	27.4	50.0K	80.0K	2.12	PA
+IIB(OCM) AT 20V,-20V	3.04K	76.6K	22.4K	22.3K	55	80.6	90.3	0.00	-10.0K	-10.0K	1.45	21.0	50.0K	80.0K	1.24	PA
+IIB(+CM) AT 5V,-25V	3.10K	77.6K	20.4K	19.2K	55	83.9	90.3	0.00	-10.0K	-10.0K	1.59	21.0	50.0K	80.0K	1.50	PA
-IIB(-CM) AT 35V,-5V	2.30K	72.0K	19.1K	19.1K	60	91.9	96.8	0.00	-10.0K	-10.0K	1.52	11.3	50.0K	80.0K	1.62	PA
-IIB(+CM) AT 5V,-35V	6.45K	78.8K	24.0K	19.4K	51	75.8	82.3	0.00	-10.0K	-10.0K	1.77	25.8	50.0K	80.0K	1.83	PA
-IIB(OCM) AT 20V,-20V	3.54K	71.0K	21.8K	20.7K	56	82.3	90.3	0.00	-10.0K	-10.0K	1.54	24.2	50.0K	80.0K	1.37	PA
-IIB(+CM) AT 5V,-25V	3.76K	78.5K	22.5K	20.5K	53	88.7	95.2	0.00	-10.0K	-10.0K	1.57	21.0	50.0K	80.0K	1.35	PA
+PSRR AT 10V,-20V	84.0	146.	110.	9.79	61	93.5	96.8	1.61	85.0	50.0	3.47	0.00	2.00K	150.	192.	DB
-PSRR AT 20V,-10V	84.7	148.	110.	11.8	61	91.9	100.	3.23	85.0	50.0	2.90	0.00	2.00K	150.	159.	DB
CMR AT 20V,-20V	83.9	126.	97.8	11.8	62	91.9	100.	8.06	85.0	50.0	1.08	0.00	2.00K	150.	141.	DB
V-ADJ(+) AT 20V,-20V	13.0	13.1	13.1	2.81K	62	95.2	98.4	0.00	8.00	0.00	1.80K	0.00	200.	20.0	66.6K	MV
V-ADJ(-) AT 20V,-20V	-14.3	-14.2	-14.2	2.91K	62	95.2	98.4	0.00	-200.	-20.0	66.2K	0.00	-8.00	0.00	2.23K	MV
IOS(+) AT 15V,-15V	-10.1	-11.6	-13.7	1.21	62	95.2	98.4	0.00	-50.0	-60.0	30.2	0.00	1.00K	0.00	841.	NA
IOS(-) AT 15V,-15V	2.55	19.8	15.4	2.07	62	96.8	98.4	0.00	-1.00K	0.00	492.	0.00	50.0	60.0	16.8	NA
ICC AT 15V,-15V	2.43	4.96	3.91	1.13	58	95.2	100.	----	----	2.00	----	35.5 4/	4.00	7.00	80.1K	MA
+VOP AT RL=10K	14.4	18.9	18.7	91.1M	62	95.2	98.4	0.00	14.0	14.0	30.1	0.00	200.	20.0	1.99K	V
-VOP AT RL=10K	-19.0	-17.9	-18.7	265.4	62	96.8	98.4	0.00	-200.	-20.0	685.	0.00	-14.0	-14.0	10.2	V
+VOP AT RL=2K	17.4	18.5	18.2	221.4	62	98.4	100.	0.00	15.0	15.0	14.5	0.00	200.	20.0	822.	V
-VOP AT RL=2K	-17.8	-16.5	-17.2	277.4	61	93.5	98.4	0.00	-200.	-20.0	661.	1.61	-15.0	-15.0	7.89	V
AVS(+) AT RL=10K	65.2	5.00K	1.31K	1.11K	59	90.3	93.5	0.00	25.0	0.00	1.16	0.00	105.K	10.0K	93.5	V/MV
AVS(-) AT RL=10K	32.3	10.0K	2.05K	2.15K	51	77.4	79.0	0.00	25.0	0.00	943.U	0.00	105.K	10.0K	47.9	V/MV
AVS(+) AT RL=2K	88.4	8.33K	1.05K	1.42K	59	91.9	91.9	0.00	25.0	0.00	722.U	0.00	105.K	10.0K	73.4	V/MV
AVS(-) AT RL=2K	1.07	1.67K	308.	317.	62	95.2	95.2	1.61	25.0	0.00	893.U	0.00	105.K	10.0K	330.	V/MV
AVS AT 5V,-5V,RL=10K	3.92	800.	183.	198.	62	93.5	95.2	3.23	10.0	0.00	872.U	0.00	105.K	1.00K	530.	V/MV
AVS AT 5V,-5V,RL=2K	6.90	999.	292.	310.	53	85.5	85.5	1.61	10.0	0.00	910.U	0.00	105.K	1.00K	337.	V/MV
SR(+) AT 20V,-20V	4.27	9.43	6.52	1.31	43	67.7	69.4	0.00	1.00	0.00	4.21	11.3 5/	50.0	25.0	33.2	V/US
SR(-) AT 20V,-20V	7.63	22.7	16.9	3.57	41	60.5	69.4	0.00	1.00	0.00	4.45	27.4	50.0	25.0	9.24	V/US

NOTES: 1/ * Excludes population outside of low rej and high rej

2/ % fail values $\geq$ 5% are circled ◯.

3/ Figure of merit definitions:

$$\text{LO - FM} = \frac{\bar{X} - \text{low limit}}{\sigma}$$

$$\text{HI - FM} = \frac{\text{High limit} - \bar{X}}{\sigma}$$

4/ The % fail for I_{CC} and SR on this table are not valid since all device types are compared to type 01 limits.

5/ There is no maximum fail limit for gain and slew rate.

Table 2-7. 125°C Statistical Summary For LF155 Series Devices.

STATISTICAL DATA FOR WAFER LOT FET OP AMP @ +25 DEGREES C 26 JUN 79 15:14:59

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN $\bar{X}$ *	SIGMA σ *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW 2/	LOW LIMIT	LOW REJ	LO-FM 3/ *	% FAIL HIGH 2/	HIGH LIMIT	HIGH REJ	HI-FM 3/ *	UNITS
VIO(+CM) AT 15V,-5V	-4.45	3.87	-21.8V	1.33	111	83.8	91.9	(10.1)	-2.00	-10.0	1.48	3.48	2.00	10.0	1.52	MV
VIO(+CM) AT 5V,-15V	-4.21	3.04	-04.8M	1.34	110	87.8	94.8	(7.3)	-2.00	-10.0	1.43	(4.9)	2.00	10.0	1.52	MV
VIO(0CM) AT 20V,-20V	-4.34	3.24	-72.1M	1.32	110	87.8	95.9	(11.8)	-2.00	-10.0	1.44	(4.9)	2.00	10.0	1.57	MV
VIO(0CM) AT 5V,-5V	-4.12	3.41	-15.3V	1.34	111	90.0	98.2	(9.5)	-2.00	-10.0	1.43	4.35	2.00	10.0	1.51	MV
IIO(+CM) AT 35V,-5V	-46.0	51.0	1.18	21.2	74	60.9	85.2	(21.6)	-20.0	-60.0	1.00	(35.1)	20.0	60.0	2.0 M	PA
IIO(+CM) AT 5V,-35V	-557.	124.	-134.	151.	112	92.2	97.0	(9.5)	-400.	-400.	1.75	0.00	100.	400.	3.51	PA
IIO(0CM) AT 20V,-20V	-33.5	49.5	3.72	17.8	135	83.5	89.6	(14.8)	-20.0	-60.0	1.33	(22.2)	20.0	60.0	2.5 M	PA
IIO(+CM) AT 5V,-25V	-59.8	54.2	-2.07	23.0	101	80.0	94.7	(22.1)	-20.0	-60.0	766.M	(20.0)	20.0	60.0	2.3 M	PA
+IIB(+CM) AT 35V,-5V	-91.7	151.	13.1	57.1	92	67.8	87.0	(26.1)	-100.	-100.	1.98	(7.8)	100.	200.	1.62	PA
+IIB(+CM) AT 5V,-35V	-471.M	2.77K	1.77K	823.	115	35.7	100.	0.00	-100.	-300.	2.27	0.00	3.50K	5.00K	2.1	PA
+IIB(0CM) AT 20V,-20V	-94.1	197.	25.3	44.6	110	91.3	96.5	0.00	-100.	-100.	1.88	(1.8)	100.	200.	1.12	PA
+IIB(+CM) AT 5V,-25V	-454.M	372.	119.	54.7	112	89.6	96.5	0.00	-100.	-100.	4.00	3.48	300.	400.	3.32	PA
-IIB(-CM) AT 35V,-5V	-94.8	106.	-21.8	37.4	97	73.9	87.0	(21.5)	-100.	-100.	2.10	1.74	100.	200.	3.25	PA
-IIB(+CM) AT 5V,-35V	-9.42	3.11K	1.92K	211.	115	95.7	100.	0.00	-100.	-300.	2.21	0.00	3.50K	5.00K	1.72	PA
-IIB(0CM) AT 20V,-20V	-77.7	149.	21.5	51.9	113	95.7	98.3	0.00	-100.	-100.	2.21	(0.9)	100.	200.	1.43	PA
-IIB(+CM) AT 5V,-25V	-149.M	400.	128.	59.8	111	89.6	94.8	0.00	-100.	-100.	3.75	(2.2)	300.	400.	2.51	PA
+PSRR AT 10V,-20V	77.8	140.	118.	8.90	100	84.3	88.7	470.M	85.0	60.0	3.74	0.00	2.00K	140.	2.1	DB
-PSRR AT 20V,-10V	77.7	137.	116.	8.59	106	86.1	91.3	470.M	85.0	60.0	3.60	0.00	2.00K	140.	2.0	DB
CMR AT 20V,-20V	66.0	136.	100.	9.74	110	90.0	93.9	470.M	85.0	60.0	1.55	0.00	2.00K	140.	1.5	DB
V-ADJ(+) AT 20V,-20V	224.M	13.1	12.9	1.20	114	94.3	98.3	1.78	8.00	0.00	4.11	0.00	200.	20.0	1.5	MV
V-ADJ(-) AT 20V,-20V	-11.3	-1.88	-10.1	1.14	111	95.7	95.7	0.00	-200.	-20.0	158.	4.35	-3.00	0.00	5.21	MV
IOS(+) AT 15V,-15V	-29.5	0.00	-21.7	5.35	115	96.5	97.4	0.00	-50.0	-60.0	5.28	0.00	1.00K	0.00	1.3	NA
IOS(-) AT 15V,-15V	10.8	28.9	17.5	3.06	115	37.4	100.	0.00	-1.00K	0.00	333.	0.00	50.0	60.0	1.1	NA
ICC AT 15V,-15V	2.28	6.45	4.16	1.28	112	94.3	100.	----	----	2.00	----	10.9 4/	4.00	8.00	1.25	MA
+VOP AT RL=10K	13.3	14.5	14.4	57.4	111	96.1	96.5	3.48	16.0	16.0	41.1	0.00	200.	20.0	3.1	V
-VOP AT RL=10K	-13.7	-13.4	-13.5	70.0	114	97.4	99.1	0.00	-200.	-20.0	2.59K	870.M	-15.0	-14.0	3.1	V
+VOP AT RL=2K	12.2	13.1	12.9	213.4	111	91.3	93.0	3.48	15.0	15.0	13.7	0.00	200.	20.0	6.5	V
-VOP AT RL=2K	-13.0	-13.5	-12.5	309.M	114	93.0	99.1	0.00	-200.	-20.0	524.	870.M	-15.0	-15.0	7.2	V
AVS(+) AT RL=10K	300.	10.0K	2.64K	1.84K	91	75.7	78.3	0.00	50.0	0.00	1.39	7.83	100.K	10.0K	63.1	V/MV
AVS(-) AT RL=10K	652.	10.0K	3.27K	2.04K	88	67.8	69.6	0.00	50.0	0.00	1.56	20.0 5/	100.K	10.0K	57.1	V/MV
AVS(+) AT RL=2K	154.	10.0K	2.64K	2.26K	103	83.6	87.0	0.00	50.0	0.00	1.15	5.22	100.K	10.0K	51.1	V/MV
AVS(-) AT RL=2K	273.	7.50K	1.22K	1.17K	119	92.2	93.0	0.00	50.0	0.00	1.00	4.35	100.K	10.0K	51.1	V/MV
AVS AT 5V,-5V,RL=10K	33.2	1.00K	233.	217.	105	84.5	90.4	0.00	10.0	0.00	1.33	5.22	10.0K	1.00K	35.	V/MV
AVS AT 5V,-5V,RL=2K	24.7	920.	203.	259.	102	87.0	89.6	0.00	10.0	0.00	1.09	4.09	10.0K	1.10K	37.5	V/MV
SR(+) AT 20V,-20V	5.00	22.7	12.9	4.83	92	74.8	80.0	0.00	3.00	2.00	2.23	20.0 5/	25.0	25.0	2.7	V/US
SR(-) AT 20V,-20V	10.4	20.8	19.8	3.52	32	59.1	55.7	0.00	3.00	2.00	4.66	72.2	25.0	25.0	1.53	V/US

NOTES: 1/ * Excludes population outside of low rej and high rej

2/ % fail values $\geq$ 5% are circled ◯.

3/ Figure of merit definitions:

$$LO - FM = \frac{\bar{X} - \text{low limit}}{\sigma}$$

$$HI - FM = \frac{\text{High limit} - \bar{X}}{\sigma}$$

4/ The % fail for I_{CC} and SR on this table are not valid since all device types are compared to type 01 limits.

5/ There is no maximum fail limit for gain and slew rate.

Table 2-8. 25°C Statistical Summary For LF155A Series Devices.

STATISTICAL DATA F - [illegible] LOT PER OP AMP @ -55 DEGREES C 26 JUN 77 15:22:19

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN $\bar{X}$ *	SIGMA σ *	SAMPLE SIZE *	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW 2/	LOW LIMIT	LOW REJ	LO-FM 3/ *	% FAIL HIGH 2/	HIGH LIMIT	HIGH REJ	HI-FM 3/ *	UNITS
VIO(+CM) AT 15V,-15	-7.18	5.20	-1.24	2.17	109	87.8	94.8	(29.7)	-2.50	-10.0	578.M	(5.22)	2.50	10.0	1.72	MV
VIO(+CM) AT 5V,-15	-6.23	4.69	-832.M	1.45	110	87.4	95.7	(14.5)	-2.50	-10.0	902.M	(5.22)	2.50	10.0	1.80	MV
VIO(0CM) AT 20V,-2	-6.43	4.88	-1.21	2.12	110	88.7	95.7	(29.1)	-2.50	-10.0	606.M	(5.22)	2.50	10.0	1.75	MV
VIO(0CM) AT 5V,-5	-7.38	9.26	-300.M	2.13	111	88.7	94.8	(13.5)	-2.50	-10.0	1.03	(6.03)	2.50	10.0	1.32	MV
V-ADJ(+) AT 20V,-2	1.10	13.1	12.9	1.09	114	94.3	98.3	1.71	9.00	0.00	4.53	0.00	200.	20.0	171.	MV
V-ADJ(-) AT 20V,-2	-14.3	-1.70	-14.1	1.19	111	95.7	95.7	0.00	-200.	-20.0	154.	4.35	-8.00	0.00	5.15	MV
IOS(+) AT 15V,-15	-37.0	0.00	-28.2	6.95	115	96.5	97.4	1.71	-50.0	-60.0	3.14	0.00	1.00K	0.00	148.	NA
IOS(-) AT 15V,-15	15.3	33.1	21.7	4.45	115	94.3	100.	0.00	-1.00K	0.00	211.	0.00 4/	50.0	60.0	5.83	NA
ICC AT 15V,-15V	2.50	7.51	4.69	1.20	82	68.7	77.8	----	----	2.00	----	38.8	4.00	8.00	1.09	MA
+VOP AT RL=10K	13.0	13.2	13.1	36.74	111	94.8	95.7	3.48	10.0	10.0	57.7	0.00	200.	20.0	0.96K	V
-VOP AT RL=10K	-14.8	-14.8	-13.2	366.4	113	87.0	97.4	0.00	-200.	-20.0	496.	1.74	-10.0	-10.0	5.95	V
+VOP AT RL=2K	12.5	13.0	12.8	110.4	111	95.7	96.5	3.48	10.0	10.0	25.0	0.00	200.	20.0	1.65K	V
-VOP AT RL=2K	-12.7	-10.8	-12.4	194.4	114	97.4	98.3	0.00	-200.	-20.0	949.	870.M	-10.0	-10.0	12.2	V
AVS(+) AT RL=10K	4.10	10.0K	1.37K	1.61K	103	85.2	88.7	(23.5)	25.0	0.00	837.M	0.00	105.K	10.0K	64.3	V/MV
AVS(-) AT RL=10K	34.7	10.0K	1.66K	2.08K	92	74.8	79.1	0.00	25.0	0.00	748.M	0.00	105.K	10.0K	49.8	V/MV
AVS(+) AT RL=2K	1.96	10.0K	1.33K	1.72K	105	87.0	88.7	(24.7)	25.0	0.00	760.M	0.00	105.K	10.0K	60.4	V/MV
AVS(-) AT RL=2K	3.11	6.00K	736.	1.07K	103	87.0	93.0	(21.5)	25.0	0.00	662.M	0.00	105.K	10.0K	97.0	V/MV
AVS AT 5V,-5V,RL=1	595.M	400.	172.	130.	84	73.9	75.7	2.61	10.0	0.00	1.24	0.00	105.K	500.	804.	V/MV
AVS AT 5V,-5V,RL=2K	8.66	471.	171.	129.	74	63.5	64.3	471.M	10.0	0.00	1.25	0.00	105.K	500.	811.	V/MV
SR(+) AT 20V,-20V	819.M	25.0	15.5	5.40	83	77.8	92.2	1.74	1.50	0.00	2.57	4.09 5/	50.0	25.0	6.36	V/US
SR(-) AT 20V,-20V	11.5	25.0	21.3	3.73	29	58.6	61.7	0.00	1.50	0.00	5.31	17.4	50.0	25.0	7.70	V/US

NOTES: 1/ * Excludes population outside of low rej and high rej

2/ % fail values $\geq$ 5% are circled ◯.

3/ Figure of merit definitions:

$$LO - FM = \frac{\bar{X} - \text{low limit}}{\sigma}$$

$$HI - FM = \frac{\text{High limit} - \bar{X}}{\sigma}$$

4/ The % fail for I_{cc} and SR on this table are not valid since all device types are compared to type 01 limits.

5/ There is no maximum fail limit for gain and slew rate.

Table 2-9. -55°C Statistical Summary For LF155A Series Devices.

STATISTICAL DATA FOR MIXED LOT FET OP AMP @ +125 DEGREES C 25 JAN 79 13:41:03

PARAMETER	LOW VALUE *	HIGH VALUE *	MEAN $\bar{X}$ *	SIGMA σ *	SAMPLE SIZE *	% IN SIGMA	% IN SIGMA	% FAIL LOW 2/	LOW LIMIT	LOW REJ	LO-FM 3/ *	% FAIL HIGH	HIGH LIMIT	HIGH REJ	HI-FM 3/ *	UNITS
VIO(-CM) AT 35V,-5V	-1.9A	2.97	48.6%	1.61	132	92.2	99.0	(5.44)	+2.50	-10.0	1.94	2.94	2.50	10.0	1.87	MV
VIO(+CM) AT 5V,-35V	-3.3A	4.3A	59.4%	1.50	103	94.1	99.0	(3.91)	+2.50	-10.0	1.70	1.00	2.50	10.0	1.62	MV
VIO(OCM) AT 20V,-20V	-4.13	3.6A	-638.1%	1.3A	132	92.2	99.0	(3.91)	+2.50	-10.0	1.48	3.92	2.50	10.0	1.84	MV
VIO(OCM) AT 5V,- 5V	-4.1A	3.05	-25.4%	1.33	103	92.2	99.0	(3.91)	+2.50	-10.0	1.8A	2.94	2.50	10.0	1.99	MV
IIO(-CM) AT 35V,-5V	-1.9AK	19.3K	830.	2.11K	103	93.0	94.0	(9.90)	+21.0K	-40.0K	9.54	0.00	21.0K	40.0K	7.85	PA
IIO(+CM) AT 5V,-35V	-2.17K	18.4K	830.	2.31K	102	94.0	94.0	(9.90)	+30.0K	-40.0K	13.5	0.00	30.0K	40.0K	12.6	PA
IIO(OCM) AT 20V,-20V	-5.2AK	14.7K	505.	1.77K	102	97.1	94.0	(9.90)	+21.0K	-40.0K	11.6	0.00	21.0K	40.0K	11.0	PA
IIO(+CM) AT 5V,-35V	-1.35K	15.1K	529.	1.74K	102	94.0	99.0	(9.90)	+20.0K	-40.0K	11.5	0.00	20.0K	40.0K	10.9	PA
+IIB(-CM) AT 35V,-5V	-254.	44.4K	6.04K	7.92K	102	93.1	99.0	(9.90)	+10.0K	-10.0K	2.02	0.00	51.0K	40.0K	5.55	PA
+IIB(+CM) AT 5V,-35V	-54.2	61.9K	13.4K	11.7K	101	91.2	94.0	(9.90)	+10.0K	-10.0K	2.01	1.0A	40.0K	40.0K	4.00	PA
+IIB(OCM) AT 20V,-20V	-51.A	72.7K	8.44K	10.7K	102	93.1	98.0	(9.90)	+10.0K	-10.0K	1.78	980.V	50.0K	40.0K	3.8A	PA
+IIB(+CM) AT 5V,-35V	-51.7	71.9K	8.84K	10.5K	102	95.1	98.0	(9.90)	+10.0K	-10.0K	1.80	980.V	50.0K	40.0K	3.93	PA
-IIB(-CM) AT 35V,-5V	-815.	43.9K	5.21K	7.14K	102	95.1	99.0	(9.90)	+10.0K	-10.0K	2.12	0.00	50.0K	40.0K	6.2A	PA
-IIB(+CM) AT 5V,-35V	29.2	5A.9K	12.7K	11.4K	101	92.2	97.1	(9.90)	+10.0K	-10.0K	1.98	980.V	40.0K	40.0K	4.14	PA
-IIB(OCM) AT 20V,-20V	-217.	49.0K	8.15K	10.4K	102	95.1	99.0	(9.90)	+10.0K	-10.0K	1.79	980.V	50.0K	40.0K	4.01	PA
-IIB(+CM) AT 5V,-35V	21.2	48.4K	8.31K	10.1K	102	95.1	99.0	(9.90)	+10.0K	-10.0K	1.82	980.V	50.0K	40.0K	4.14	PA
+PSRR AT 10V,-20V	74.9	147.	122.	9.94	101	95.1	98.0	980.V	85.0	50.0	3.74	0.00	2.00K	150.	189.	DB
-PSRR AT 20V,-10V	74.9	134.	119.	10.5	101	93.2	98.0	980.V	85.0	50.0	3.33	0.00	2.00K	150.	170.	DB
CMR AT 20V,-20V	74.5	12A.	99.3	8.82	102	94.1	93.0	980.V	85.0	50.0	1.62	0.00	2.00K	150.	215.	DB
V-ADJ(+) AT 20V,-20V	10.7	13.1	13.0	317.V	101	96.1	96.1	980.V	8.00	0.00	15.7	0.00	210.	20.0	530.	MV
V-ADJ(-) AT 20V,-20V	-11.3	-9.65	-14.0	667.V	100	94.1	96.1	980.V	-200.	-20.0	279.	1.0A	-8.00	0.00	9.05	MV
IOS(+) AT 15V,-15V	-23.A	0.00	-14.7	3.43	102	94.0	99.0	980.V	-50.0	-60.0	10.3	0.00	1.00K	0.00	29A.	NA
IOS(-) AT 15V,-15V	2.35	18.0	13.6	2.5A	102	94.0	99.0	980.V	-1.00K	0.00	335.	0.00	50.0	60.0	18.2	NA
ICC AT 15V,-15V	2.19	6.1A	3.7A	1.10	103	97.1	99.0	-----	-----	2.00	-----	38.2 4/	1.00	7.30	209.V	MA
+VOP AT RL=10K	14.1	14.A	14.A	122.V	101	98.1	95.1	980.V	14.0	14.0	21.3	0.00	210.	20.0	1.08K	V
-VOP AT RL=10K	-14.0	-14.A	-14.A	93.9V	101	96.1	99.0	980.V	-20.0	-20.0	2.14K	980.V	-14.0	-14.0	33.3	V
+VOP AT RL=2K	15.7	16.A	17.A	534.V	101	98.0	98.0	980.V	15.0	15.0	4.42	0.00	210.	20.0	312.	V
-VOP AT RL=2K	-14.2	-15.4	-17.4	943.V	101	94.0	99.0	980.V	-200.	-20.0	194.	980.V	-15.0	-15.0	2.57	V
AVS(+) AT RL=10K	211.	7.50K	1.75K	1.47K	98	80.4	83.3	980.V	25.0	0.00	1.04	1.00	115.K	10.0K	61.9	V/MV
AVS(-) AT RL=10K	1.51	10.0K	1.93K	1.80K	98	86.3	87.3	980.V	25.0	0.00	1.0A	0.00	105.K	10.0K	57.2	V/MV
AVS(+) AT RL=2K	17.2	7.50K	1.41K	1.57K	97	88.2	93.1	980.V	25.0	0.00	1.01	0.00	115.K	10.0K	65.7	V/MV
AVS(-) AT RL=2K	551.V	10.0K	1.69K	1.74K	97	90.2	93.1	980.V	25.0	0.00	907.V	0.00	105.K	10.0K	58.4	V/MV
AVS AT 5V,-5V,RL=10K	13.5	800.	111.	134.	101	94.1	97.1	980.V	10.0	0.00	740.V	0.00	105.K	1.00K	749.	V/MV
AVS AT 5V,-5V,RL=2K	12.2	889.	109.	134.	100	93.2	95.1	980.V	10.0	0.00	693.V	0.00	105.K	1.00K	730.	V/MV
SR(+) AT 20V,-20V	5.0A	20.4	10.7	3.52	65	63.7	63.7	980.V	1.50	0.00	2.61	18.A 5/	51.0	25.0	11.2	V/US
SR(-) AT 20V,-20V	A.A2	25.0	19.9	3.A8	5A	60.A	62.7	980.V	1.50	0.00	5.01	18.A 5/	51.0	25.0	A.16	V/US

NOTES: 1/ * Excludes population outside of low rej and high rej

2/ % fail values $\geq$ 5% are circled (○).

3/ Figure of merit definitions:

$$LO - FM = \frac{\bar{X} - \text{low limit}}{\sigma}$$

$$HI - FM = \frac{\text{High limit} - \bar{X}}{\sigma}$$

4/ The % fail for I_{CC} and SR on this table are not valid since all device types are compared to type 01 limits.

5/ There is no maximum fail limit for gain and slew rate.

Table 2-10. 125°C Statistical Summary For LF155A Series Devices.

LF155/6/7 PARAMETER DISTRIBUTIONS & LIMITS

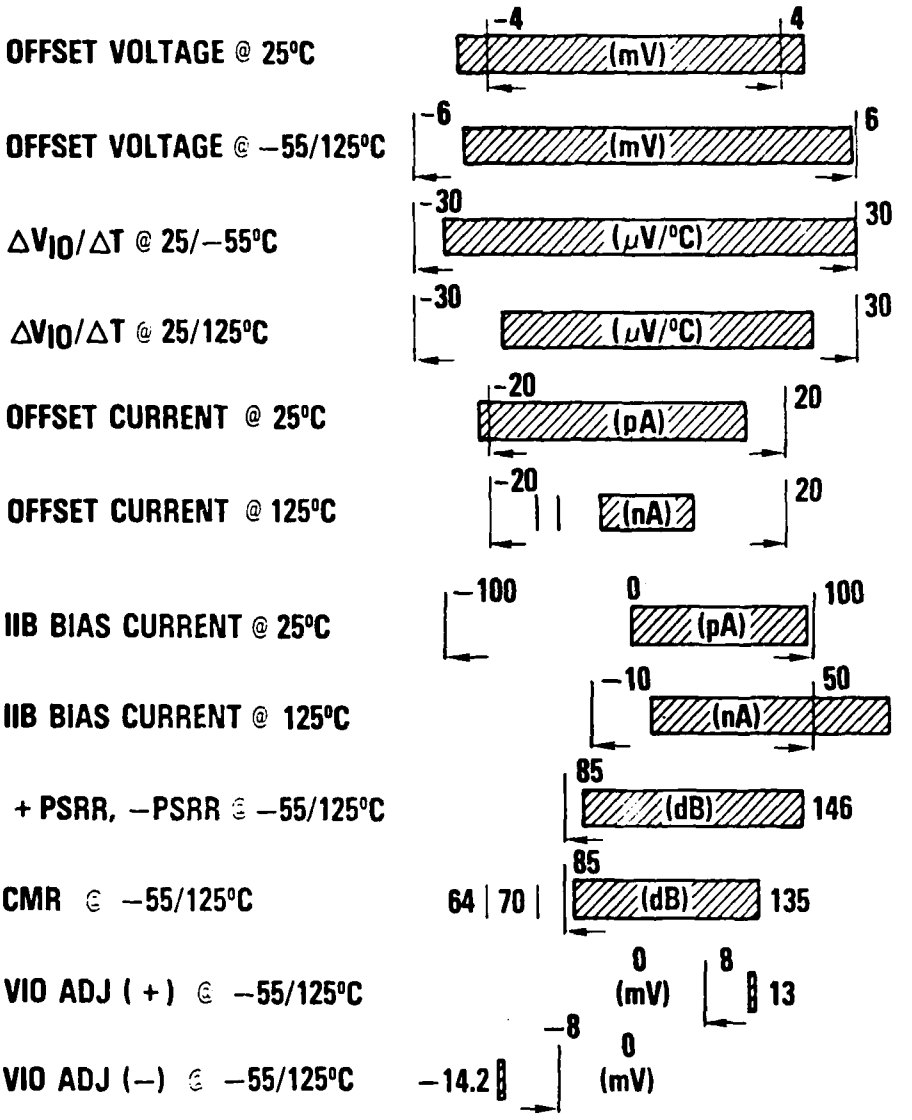


Table 2-11. LF155/6/7 Data Distributions.

LF 155/6/7 PARAMETER DISTRIBUTIONS & LIMITS

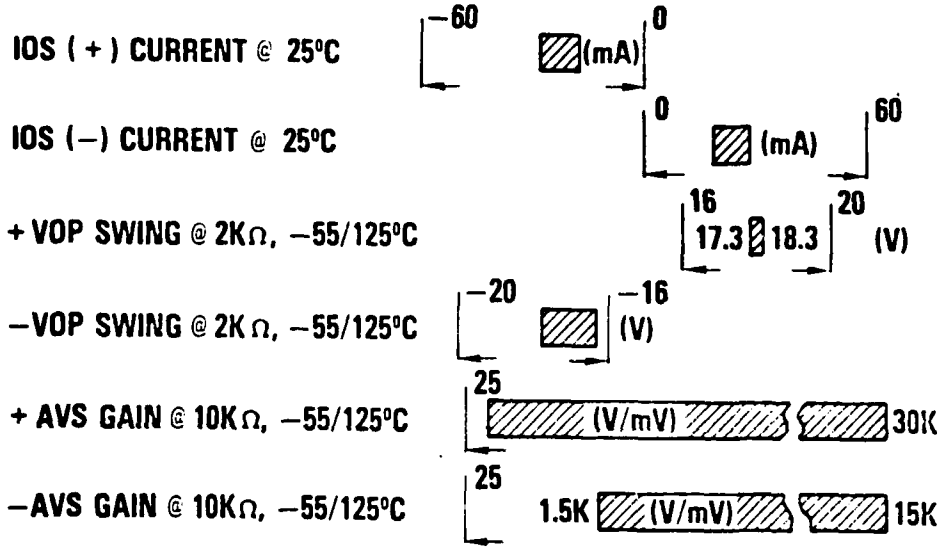
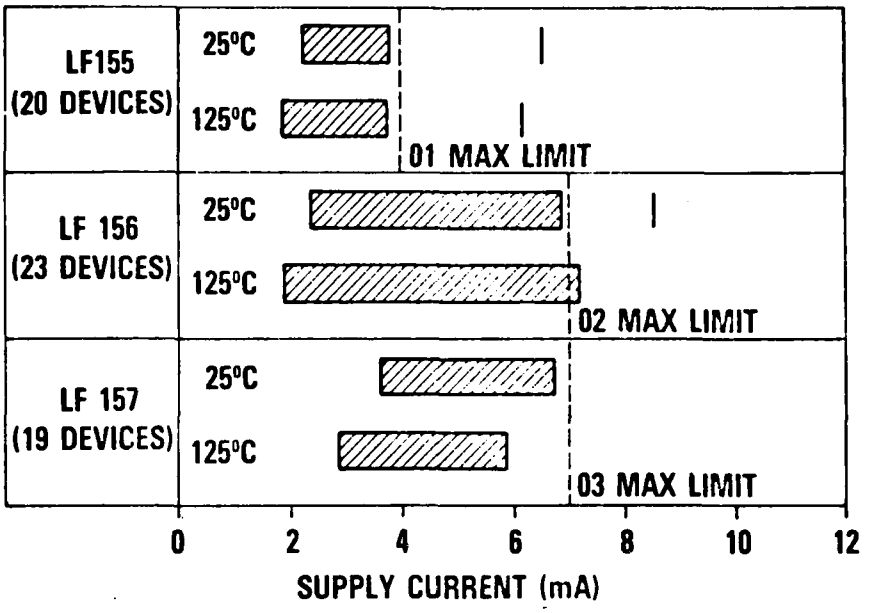


Table 2-11. LF155/6/7 Data Distributions (cont.).

SUPPLY CURRENT vs DEVICE TYPE @ $\pm V_{CC} = \pm 15V$



SLEW RATE RANGE vs DEVICE TYPE

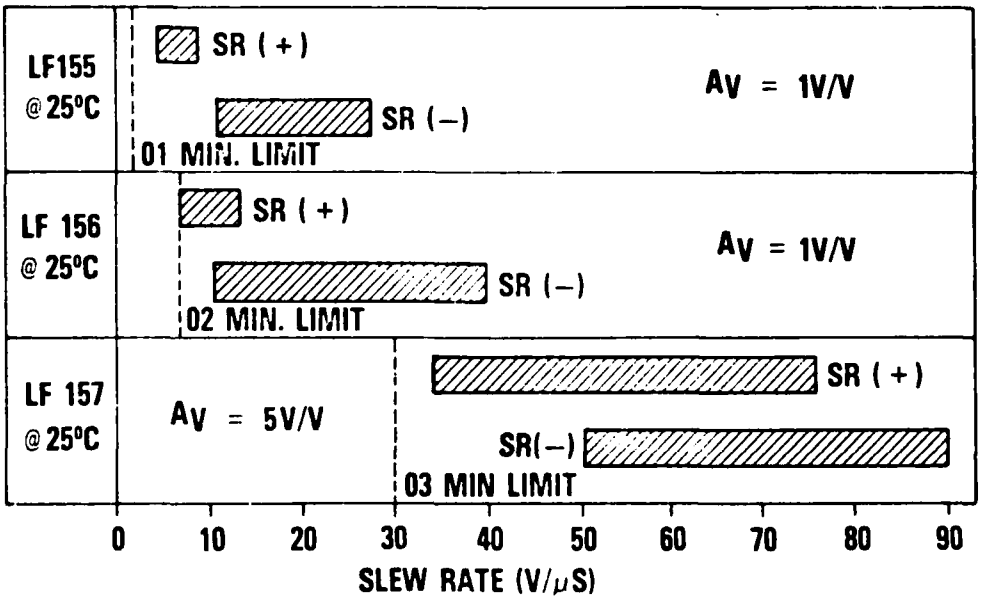


Table 2-12. LF155/6/7 Supply Current & Slew Rate vs Device Type.

A_V = 1 V/V

Parameter Symbol	Conditions AV = 1 V/V	VENDOR CODE A Serial No. 12	13	14	15	16	VENDOR CODE B* Serial No. 90	91	92	93	94	VENDOR CODE B Serial No. 83	86	87	88	89	UNITS
tR(tr)	VO = .05V	44	50	55	53	47	49	45	41	49	43	48	50	46	45	46	ns
	VO = .5V	48	58	76	64	63	52	48	42	56	48						
tR(os)	VO = .05V	43	42	38	40	47	38	35	35	33	36	36	36	38	36	44	%
	VO = .5V	46	38	30	34	36	33	31	34	29	32						
SR (+)	VO = -5V TO + 5V	7.5	5.0	11.5	12.0	11.0	9.0	8.5	11.5	7.0	8.0	8.0	7.5	9.0	10	8.0	V/us
SR (-)	VO = -5V TO + 5V	18.0	12.0	9.0	12.0	9.5	17.0	17.5	18.0	13.5	15.5	17.5	13.5	19.0	20.5	19.0	V/us
ts	VO = -5V TO + 5V	700	850	1000	900	1200	800	750	800	900	800	1300	1250	1000	1100	1200	ns

* LF155A

TABLE 2-13. LF155 Dynamic Data @ 25°C.

A_V = 1 V/V

Parameter Symbol	Conditions A_V = 1 V/V	VENDOR CODE B* Serial No.					VENDOR CODE A Serial No.					VENDOR CODE E* Serial No.					UNITS
		130	131	132	133	134	34	35	36	37	38	149	150	151	152	153	
TR (tr)	VO = .05V	28	28	35	39	35	45	44	42	45	42	33	39	38	34	30	ns
	VO = .5V	33	38	37	41	35	50	47	44	46	44	40	32	31	41	34	
TR (os)	VO = .05V	47	42	45	42	44	46	48	44	46	48	42	46	46	44	44	%
	VO = .5V	39	37	38	36	38	36	380	390	36	390	36	40	390	36	37	
SR (+)	VO = -5V TO + 5V	17.5	15.0	17.0	10.0	16.0	9.5	9.5	10.5	10.0	10.5	16.0	24.0	25.0	14.0	18.0	V/us
SR (-)	VO = -5V TO + 5V	34.0	33.0	31.0	23.0	30.0	20.0	20.0	19.0	18.5	19.0	26.0	29.5	29.0	20.5	28.0	V/us
ts	VO = -5V TO + 5V	900	950	900	1100	900	1100	1200	1250	1200	1300	1100	1000	1100	1300	1100	ns

* LF156A

TABLE 2-14. LF156 Dynamic Data @ 25°C.

A_V = 5 V/V

Parameter Symbol	Conditions A/V = 5 V/V	VENDOR CODE D Serial No. 60	61	62	67	68	VENDOR CODE C Serial No. 69	70	71	72	73	VENDOR CODE B Serial No. 78	79	80	81	82	UNIT
TR (tr)	VO = .05V VO = .5	270	260	290	290	260	290	300	280	310	290	240	260	250	260	280	ns
TR (os)	VO = .05V VO = .5V	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	%
SR (+)	VO = -5V TO + 5V	95.0	80.0	75.0	70.0	75.0	75.0	65.0	80.0	70.0	75.0	80.0	65.0	80.0	50.0	75.0	V/us
SR (-)	VO = -5V TO + 5V	90.0	85.0	95.0	80.0	75.0	85.0	85.0	110.0	90.0	95.0	95.0	80.0	85.0	85.0	90.0	V/us
ts	VO = -5V TO + 5V	450	450	450	550	500	400	300	300	400	300	550	600	600	650	600	ns

TABLE 2-15. LF157 Dynamic Data @ 25°C.

2.5 Discussion

On a parameter by parameter basis, a discussion of the device characteristics follows:

2.5.1 Input Offset Voltage (V_{IO})

LF155/156/157 Family

This family of devices had very good yields in passing the V_{IO} tests over the common mode voltage and military temperature range. The screening limits for these devices were ± 4 mV and ± 6 mV at 25°C and over the military temperature range respectively. These limits were subsequently expanded to ± 5 mV and ± 7 mV respectively, as part of a decision to include the LF155A series op amps as separate device types with low offset voltage in the slash sheet.

In early 1979 a GIDEP (Government Industry Data Exchange Program) alert was issued on Vendor Code E LF155 devices became of high offset voltage drift with time (greater than ± 10 mV). The vendor said that the problem was caused by contamination during the ion implant and cleaning procedures, which resulted in a surface inversion condition. A 168 hour burn-in test at GE Ordnance Systems on the LF155 series group from vendor codes A, B, C and D revealed a maximum offset voltage shift of less than 0.8 mV. Most devices had less than 0.3 mV of offset drift.

A related problem is with short term power turn-on offset voltage shift. The 1/15/79 edition of Circuit News reported on this phenomenon. Some sample testing was also done at GE Ordnance Systems without finding any devices having this problem.

LF155A/156A/157A Family

The test yields of the LF155A series devices to the tighter limits of ± 2 mV/ ± 2.5 mV were considerably lower than those for the non-A devices. Tables 2-8, 2-9 and 2-10 show this information in terms of percent fail high and percent fail low. Overall yields at 25°C, -55°C and 125°C were approximately 80%, 66% and 92% respectively.

2.5.2 Offset Voltage Temperature Sensitivity ($\Delta V_{IO}/\Delta T$)

LF155/156/157 Family

$\Delta V_{IO}/\Delta T$ is a very important parameter for applications having tight error specifications over a wide temperature range. Offset adjustment can not compensate for poor offset voltage drift. The user's only guarantee is to test for this parameter to screen out inferior devices.

With limits of ± 30 uV/°C, the non-A's had yields of 94% and 97% for the cold and hot excursions from 25°C.

LF155A/156A/157A Family

Even though the manufacturers' catalog limits of ± 5 uV/°C were relaxed to ± 10 uV/°C, the test yields for the A series devices were 43% and 90% for the cold and hot $\Delta V_{IO}/\Delta T$ measurements, respectively. It was later determined that the LF155A devices from vendor Code B were not prescreened to truly certify them as A's. Follow up tests with vendor Code B indicated that good yields could be achieved with the ± 10 uV/°C limits. From 25°C to 125°C V_{IO} is allowed to increase from ± 2 mV to ± 2.5 mV. This corresponds to an end point shift of 500 uV/100°C = 5 uV/°C.

2.5.3 Input Offset Current (I_{IO})

Since Bi-FET op amp offset current is the difference between the two input leakage bias currents, it is very small and also difficult to measure. Only the zero common mode voltage condition is covered by the /114 specification. Test yields were 93.5% and 64% for the non-A's and A's respectively, against the ± 20 pA limits.

Most of the failures were traced to 156 A's and 157 A's from Vendor Code E. Test yields were worse for the "unspecified" -15V common mode condition because of front end matching considerations. At + 15 V common mode the test yield is better because the acceptance limit is raised to compensate for the higher input bias current.

2.5.4 Input Bias Current (+ I_{IB}, - I_{IB})

Figures 2-8 thru 2-11 show the sensitivity of input bias current to common mode voltage and power supply voltage. The slash sheet specification is based on $\pm V_{CC} = \pm 20$ V because of a precedent established with previous military op amp specifications and a desire to maintain standards for comparison.

It should be obvious from these figures that if low I_{IB} is a necessary application requirement, the supply voltages should be no higher than ±15 V. Also with the lower supply voltages, the common mode voltage range is more evenly centered about zero. As the common mode voltage approaches the negative power supply voltage, the P-N junction between the gate and channel of the input J-FETs becomes forward biased and forward current is pulled out of the gate. The input common mode voltage corresponding to this "forbidden" condition is within three volts of $-V_{CC}$.

Increasing the common mode voltage in the positive direction causes reverse leakage current to flow into the J-FET gate terminals. The common mode voltage range over which the input J-FETs are technically in the leakage mode varies according to diffusion characteristics, geometry and minority carries concentrations. Also the leakage current is almost independent of reverse voltage.

The typical diode shape increase in bias current with common mode voltage occurs as the junction enters the avalanche or zener voltage range. Series resistance prevents the classical zener constant voltage characteristic from occurring.

Process differences among the device manufacturers cause the bias current vs common mode voltage characteristics to vary accordingly as can be seen in Figures 2-8 thru 2-10. Since the input bias current is J-FET gate leakage it is not surprising that this current is highly temperature sensitive. Typically, leakage current doubles for every 10°C rise in temperature. Figures 2-12 and 2-13 show this effect.

The test yields to the /114 specification limits were good except for the following:

1. Vendor Code E. LF155A series devices incorporating bias current compensation had a yield of only 16.6% for the negative common mode low limit of - 100 pA. Bias current compensation uses negative PNP collector current to cancel positive J-FET gate current. At the negative common mode condition an over cancelled situation is more likely to occur. The JC-41 Committee has not asked for relief on this limit.

2.5.4 Input Bias Current (continued)

2. Vendor Code C. LF155 series devices had a yield of 30.7% for the 125°C input bias current limits of 50 mA and 60 mA at the zero and positive common mode conditions respectively. No relief has been asked for this limit.

2.5.5 Power Supply Rejection Ratio (+ PSRR, - PSRR)

All of the devices had good yields in meeting the 85 dB minimum limit.

2.5.6 Common Mode Rejection (CMR)

Good yields were obtained in meeting the 85 dB minimum limit. This parameter is calculated from the V_{IO} change over the input common mode range. Consequently, there is a close relationship between V_{IO} and CMR failures.

2.5.7 Input Offset Voltage Adjustment (V_{IO} ADJ (+), V_{IO} ADJ (-)

Traditionally, the requirement for offset voltage adjustment is that it be capable of driving the input offset voltage one millivolt beyond the minimum and maximum limits of offset voltage. All functional devices far exceeded this requirement with typical values of 13 mV and - 14.3 mV for the positive and negative adjustments respectively.

2.5.8 Short Circuit Current (I_{OS} (+), I_{OS} (-))

The instantaneous short circuit current was considerably less than the 50 mA maximum requirement. The short circuit current magnitude decreases with increasing temperature for both output drive polarities. If the output is commanded to be at the positive swing limit and then a short circuit is made between the output and ground or the negative power supply, the short circuit current I_{OS} (+), will be current limited by Q_4 and R_1 in Figure 2-1. Accordingly, typical I_{OS} (+) $= \frac{V_{BEQ4}}{R_1} = \frac{600\ mV}{25} = 24$ mA. Since $\frac{\Delta V_{BE}}{\Delta T} \approx -2$ mV/°C, the self heating of the device and the output transistor, will cause the short circuit current to decrease by 80 uA/°C.

Output short circuit protection can not be guaranteed over the full - 55°C to 125°C military temperature range.

2.5.8 Short Circuit Current (continued)

Under worst case conditions, the maximum internal junction temperature of 175°C will be exceeded at ambient temperatures far below 125 C. The following equations apply:

1. $P_D = 2\ V_{cc}\ I_{cc} + |V_{cc} - V_o|\ I_{os}$

2. $T_J = T_A + P_D\ \theta_{JA}$

where P_D = device dissipation (mW)

V_{cc} = power supply voltage (V)

I_{cc} = power supply current (mA)

V_o = output short circuit voltage (V)

I_{os} = output short circuit current (mA)

T_J = junction temperature (°C)

T_A = ambient temperature (°C)

θ_{JA} = device junction to ambient thermal resistance (°C/mW)

Under worst case conditions and a "warmed-up" short circuit current of 30 mA, the devices have the following maximum safe ambient temperatures:

Device Type	Maximum Safe Ambient Temp *	
	"short" to ground	"short" to supply
01, 04	89.5°C	22°C
02, 03, 05, 06	76°C	9°C

*T_A @ T_J = 175°C

Several 02 and 03 devices were subjected to sustained output to power supply short circuits for several hours without incurring any damage. The real margin of safety depends on the differences between worst case and typical parameters.

2.5.9 Supply Current (I_{CC})

Supply current is one of the parameters which is different for each device type in the LF155 series family. The I_{CC} limits are well chosen for the device data distribution.

2.5.10 Output Voltage Swing ($+V_{OP}$, $-V_{OP}$)

Maximum output voltage swing is generally well behaved with a tight histogram pattern and a mean value which is two volts or better than the specification limit.

2.5.11 Open Loop Voltage Gain (A_{VS} (+), A_{VS} (-))

But for one exception, the data distribution of open loop voltage gain far exceeded the minimum specification. Characteristically, the gain histograms have a scattered distribution. There were no wrong polarity gains, thus indicating better management of thermal effects than were observed on many good op amps during previous characterization studies. LF155A devices from vendor Code B had many gain failures at -55°C. Vendor Code B test yields at -55°C were 50%, 15.8% and 16.0% for their LF155A, LF156A and LF157A devices respectively. These same devices had respectable gains at 25°C and 125°C.

2.5.12 Slew Rate (S_R (+), SR (-))

Each of the six device types is characterized by a different slew rate specification. Within the non-A and A groups of devices, slew rate is traded off with supply current to offer the user three design options. In most cases negative slew rate was faster than positive slew rate by almost 2:1.

LF155/156/157 Family

All of the devices had good yields to their respective specification limits, except for LF156's from Vendor Code C, which had yields of 22% and 0% at 25°C and 125°C respectively.

LF155A/156A/157A Family

With the exception of Vendor Code C, 156A devices, which had a test yield of 50%, all of the data was well within the specification limits. The failed 156A devices would pass the 15V limits (i.e. 7 V/us vs 10 V/us). Compared with bipolar op amps, BI-FET op amps have a much better combination of high slew rate and low input bias current.

2.5.13 Transient Response (TR (tr), TR (OS))

With a closed loop gain of 1 V/V, the transient response data of the LF155 and LF156 devices was significantly faster than the initial JC-41 committee recommended limits.

Also the LF157 devices at a closed loop gain of 5 V/V were slower than the JC-41 Committee recommended limits. The data and limits are summarized below:

Device Type @ AV	JC-41 Limits TR(tr) (ns) (min)	(max)	TR(OS) (%) (min)	(max)	Data @ 25 C TR(tr) (ns) (min)	(max)	TR(OS) (%) (min)	(max)	Sample Size
LF155 @ 1V/V	-	300	-	40	41	55	33	47	15
LF156 @ 1V/V	-	200	-	40	28	45	42	48	15
LF157 @ 5V/V	-	100	-	40	240	310	0	0	15

In order to resolve the differences between the recommend limits and the data, a second referee circuit was built and several devices were tested again. The new data correlated with the original data.

After verifying that the data matched, the sensitivity of the data to the circuit components was investigated. Not surprisingly, the feedback capacitor has a dominant effect. For instance a change from 10 pf to 18 pf caused the overshoot of an LF156A to decrease from 44% to 32%. Figure 2-16 shows the typical response of an LF155 and an LF156 device. The high TR(OS) overshoot failure rate was resolved by modifying the test circuit such that for A_V = 1 V/V, R_F = 0 . Normally closed K9 contacts in parallel with the 10 K Ω resistor of Figure 2-4 reduces the D.U.T. overshoot by making the device less susceptible to parasitic capacitance at the inverting input. Typically, depending on the D.U.T's characteristics, a reduction of 10% to 20% in overshoot was achieved.

2.5.13 Transient Response (continued)

Closed loop gain has a big effect on the transient response of an LF157 or can be seen in Figure 2-17.

Rise time and overshoot changed from 15 nanoseconds and 10% to 250 nanoseconds and 0%, respectively, when the closed loop gain was increased from 1 V/V to 5 V/V. In raising the closed loop gain, the open loop gain is reduced by 14 dB and the effect of the high frequency poles and zeros is greatly reduced.

The revised transient response specification limits are shown in Table 2-16

2.5.14 Settling Time (ts(+), ts(-))

Settling time as defined in the 7114 specification is a sampled large signal test for the time it takes the error voltage to settle within 0.1% of its final value. A phantom summing mode is monitored as shown in Figure 2-5 while the DUT is exercised to produce a 10 V output pulse. This summing mode voltage V_N is proportional to the error voltage difference V_E between the input and output voltage as shown below:

$$V_N = V_{IN} \frac{R_F}{R_1 + R_F} + V_o \frac{R_1}{R_1 + R_F}$$

$$V_N = V_{IN} \frac{R_F}{R_1 + R_F} - \left(\frac{R_F}{R_1}\right) \quad V_{IN} \left(\frac{R_1}{R_1 + R_F}\right)$$

$$V_N = \frac{R_F}{R_1 + R_F} \quad V_E$$

Thus for circuit gains of - 1 V/V and - 5 V/V, the null voltage is .5 V_E and .833 V_E, respectively. For a 10 V output and 0.1% error, the corresponding null voltage thresholds are 5 mV and 8.33 mV at A_V = 1 V/V and 5 V/V respectively.

Figure 2-20 shows the dynamic null error voltage of several typical devices. The settling time is composed of a slewing interval and transient response interval, which depend on different parameters and conditions. For a given device the slewing interval is pro-

2.5.14 Settling Time (continued)

portional to the output step change, whereas the transient response interval is dependent on the damping ratio of the device in the test circuit.

The circuit closed loop gain has a big effect on both the slewing interval and the transient response interval. Depending on how the response oscillations dampen, the difference between 0.1% and .01% settling time can vary from a fractional part of cycle to several cycles.

The relationship between the data and the proposed limits is tabulated below:

Device Type	Data @ 25°C ts in (ns)			/114 A ts in (ns)	
A_V	(min)	(max)	Sample Size	(min)	(max)
LF155 @ 1V/V	700	1300	15	-	1500
LF156 @ 1V/V	900	1300	15	-	1500
LF157 @ 5V/V	300	650	15	-	800

2.5.15 Noise (N_I (BB), N_I (PC))

Broadband and pop corn noise was measured with a Tektroniks Type 577 curve tracer. Typical data displays are shown in Figure 2-22.

Broadband noise was measured with a source resistance of 50Ω and the observed peak-to-peak readings were divided by six to yield Gaussian rms values.

This factor of six is used because op amp noise voltage is random and has a normal statistical distribution. One of the properties of a normal Gaussian distribution is that the ratio of the peak-to-peak value over the rms value is six with a probability of 99.7%.

2.5.15 Noise (continued)

The data is summarized as follows:

Broadband Noise (u Vrms)	Data Frequency
0.3	1
0.7	5
0.8	3
1.0	10
1.2	1
1.3	3
1.7	1
	Total: 24 data values

The data distribution is conservatively within the 10 u Vrms maximum limits of the /114 specification.

For the popcorn noise test only one device had an observed "pop" of 10 u Vpk. The remaining 23 devices had no trace of popcorn noise.

2.5.16 Burn-In Circuit Evaluation

After the initial characterization data was taken, sixty non-A devices were burned-in using two different circuit configurations. Twenty-eight devices were exercised in the original voltage follower circuit which uses a 2000 ohm load. During this 168 hour burn-in test, the input was changed from + 5 V to - 5 V after approximately half of the time had elapsed. The remaining 32 devices were exercised on a new simplified circuit which has the inputs grounded and the outputs open. Maximum supply voltages of ± 22 VDC were applied to these devices, whereas only ± 20 VDC was applied to the first group. The two sample populations were chosen such that they equal representation with regard to vendor and date code.

At the conclusion of the 168 hours, 125 C test, the devices were cooled down before power was removed. The serialized devices were again tested on the S-3260. The following observations were made after comparing the before and after test data:

1. For both test circuits the post burn-in data total failures did not exceed the total pre burn-in failures. In other words good devices, in general, are not harmed by either test circuit.

2.5.16 Burn-in Circuit Evaluation (cont.)

2. Quite often on particular devices pre burn-in failures did not appear at post burn-in. These were mainly I_{IO} and I_{IB} technical limit failures.

It was concluded that the new simplified burn-in circuit was equally effective with the old standard test circuit. Subsequently, it was recommended that the supply voltages be reduced to ± 20 V and the pin 5 offset adjust pin be connected to $+V_{cc}$.

2.6 Conclusions and Recommendations

204 LF155 series op amps were tested on GEOS' S-3263 to characterize their electrical parameters. Sampled bench test data was taken to characterize noise and some of the dynamic electrical characteristics, which could not be tested on the S-3263. It should be noted that the electrical characteristics are oriented toward automatic procurement testing. With the exceptions of input bias current, input offset current, and output short circuit current, the effects of device self heating will not cause the procurement values to differ from application values.

In order to minimize input bias currents and device power dissipation it is recommended that the power supply voltages be kept no higher than ± 15 V. Although these Bi-FET op amps are guaranteed to operate at 125 C ambient temperature, high temperature operation will cause the benefits of low input bias currents to be lost.

The LF155 series of Bi-FET op amps have several advantages over bipolar devices including a more optimum combination low bias current and high slew rate plus the ability to drive high capacitance loads.

Final recommended electrical specifications for the generic LF155 series op amps in MIL-M-38510/114 are shown in Table 2-16.

Characteristics	Symbol	Conditions (V_{CC} = 20 V unless otherwise specified)		Device	Limits Min.	Limits Max.	Units
Input offset voltage	V_{IO}	V_{CC} = 5 V, V_{CM} = 0 V	T_A = 25 C	04,05,06	- 2	2	mV
				01,02,03	- 5	5	mV
		V_{CC} = 20 V, V_{CM} = 15 V, 0 V	-55 C $\leq T_A \leq$ +125 C	04,05,06	-2.5	2.5	mV
				01,02,03	- 7	7	mV
Input offset voltage temperature sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	V_{CC} = 20 V, V_{CM} = 0 V		01,02,03	-30	30	uV/ C
				04,05,06	-10	10	
Input offset current	I_{IO}	V_{CC} = 20 V, V_{CM} = 0 V, t $\leq$ 25 ms	T_J = 25 C	all	-20	20	pA
			T_J = 125 C	all	-20	20	nA
Input bias current	+ I_{IB}	V_{CC} = 20 V, V_{CM} = + 15 V, t $\leq$ 25 ms	T_J = 25 C	all	-100	3500	pA
			T_J = 125 C	all	-10	60	nA
	- I_{IB} 1/	V_{CC} = 15 V, V_{CM} = + 10 V, t $\leq$ 25ms	T_J = 25 C	all	-100	300	pA
			T_J = 125 C	all	-10	50	nA
	2/	V_{CC} = 20 V, - 15 V $\leq V_{CM} \leq$ 0 V, t < 25 ms	T_J = 25 C	all	-100	100	pA
	3/		T_J = 125 C	all	-10	50	nA
Power supply	+PSRR	+ V_{CC} = 10 V, - V_{CC} = -20 V		all	85	---	dB
	-PSRR	+ V_{CC} = 20 V, - V_{CC} = -10 V		all	85	---	dB
Input voltage common mode rejection 4/	CMR	V_{CC} = 20 V, V_{IN} = 15 V		all	85	---	dB

See footnotes at end of table.

Table 2-16. Proposed Electrical performance Characteristics For MIL-M-38510/114.

Characteristics	Symbol	Conditions (V_{cc} = + 20 V unless otherwise specified)		Device	Limits Min.	Limits Max.	Units
Adjustment for input offset voltage	V_{IO} ADJ (+)	V_{CC} = + 20 V		all	+ 8	---	mV
	V_{IO} ADJ (-)	V_{CC} = + 20 V		all	---	- 8	mV
Output short circuit current (for positive output) 5/	I_{OS} (+)	V_{CC} = + 15 V t ≤ 25 mS (Short circuit to ground)		all	-50	---	mA
Output short circuit current (for negative output) 5/	I_{OS} (-)	V_{CC} = + 15 V t ≤ 25 mS (Short circuit to ground)		all	---	50	mA
Supply current	I_{CC}	V_{CC} = + 15 V	T_A = -55° C	01,04 02,03,05,06	--- ---	6 11	mA
			T_A = +25° C	01,04 02,03,05,06	--- ---	4 7	
			T_A = +125° C	01,04 02,03,05,06	--- ---	4 7	
Output voltage swing (maximum)	V_{OP}	V_{CC} = + 20 V, R_L = 10 KΩ		all	16	---	V
		V_{CC} = + 20 V, R_L = 2 KΩ		all	15	---	
Open loop voltage gain (single ended) 6/	A_{VS} (+)	V_{CC} = + 20 V R_L = 2 KΩ V_{OUT} = + 15 V	T_A = 25° C	all	50	---	V/mV
			-55° C ≤ T_A ≤ +125° C	all	25	---	
Open loop voltage gain (single ended) 6/	A_{VS}	V_{CC} = + 5 V R_L = 2 KΩ V_{OUT} = + 2 V		all	10	---	V/mV

See footnotes at end of table.

Table 2-16. Proposed Electrical Performance Characteristics For MIL-M-38510/114.

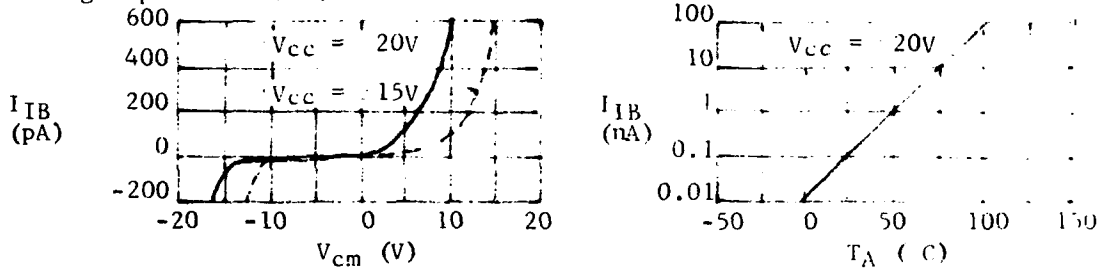
Characteristics	Symbol	Conditions (V_{CC} = ± 20 V unless otherwise specified)		Device	Limits Min.	Limits Max.	Units
Transient response rise time	$TR_{(tr)}$	V_{CC} = ± 15 V R_L = 2 KΩ C_L = 100 pf See Figure 8	A_V = 1	01,04	---	150	ns
				02,05	---	100	
			A_V = 5	03,06	---	450	
Transient response overshoot	$TR_{(OS)}$		A_V = 1	01,02,04,05	---	40	
			A_V = 5	03,06	---	25	
Slew rate	SR(+)	V_{IN} = ± 5 V V_{CC} = ± 15 V	T_A = 25° C	01	2	---	V/us
				02	7.5	---	
	and	A_V = 1		04	3	---	
		see Figure 8		05	10	---	
	SR(-)		T_A = -55 C, 125 C	01	1	---	
				02	5	---	
				04	1.5	---	
				05	7	---	
		V_{IN} = ± 5 V V_{CC} = ± 15 V A_V = 5 See Figure 8	T_A = 25° C	03	30	---	
				06	40	---	
			T_A = -55 C, 125° C	03	20	---	
				06	25	---	
Settling time	ts(+)	V_{CC} = ± 15 V (0.1% error)	A_V = 1	01,02,04,05	---	1500	ns
	and	T_A = 25 C					
	ts(-)	See Figure 9	A_V = 5	03,06	---	800	
Noise (referred to input) broad-band	N_I(BB)	V_{CC} = ± 20 V Bandwidth = 5kHz	T_A = 25 C	all	---	10	uVrms
Noise (referred to input) popcorn	N_I(PC)		T_A = 25 C	all	---	80	uV_{pk}

Table 2-16. Proposed Electrical Performance Characteristics For MIL-M-38510/114.

NOTES:

1/ Bias currents are actually junction leakage currents which double (approximately) for each 10 C increase in junction temperature T_J. Measurement of bias current is specified at T_J rather than T_A, since normal warmup thermal transients will affect the bias currents. The measurements for bias currents must be made within 25 ms after power is first applied to the device for test. Measurement at T_A = -55 C is not necessary since expected values are too small for typical test systems.

2/ Bias current is sensitive to power supply voltage, common mode voltage and temperature as shown by the following typical curves:



3/ Negative I_{IB} minimum limits reflect the characteristics of devices with bias current compensation.

4/ CMR is calculated from V_{IO} measurements at V_{CM} = + 15 V and - 15 V.

5/ Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that T_J (max) $\leq$ 175 C.

6/ Because of thermal feedback effects from output to input, open loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.

Table 2-16. Proposed Electrical Performance Characteristics For MIL-M-38510/114.

SECTION III

ADJUSTABLE POSITIVE VOLTAGE REGULATORS

MIL-M-38510/117

ADJUSTABLE NEGATIVE VOLTAGE REGULATORS

MIL-M-38510/118

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SECTION III

CHARACTERIZATION OF ADJUSTABLE POSITIVE VOLTAGE REGULATORS

MIL-M-38510/117

&

ADJUSTABLE NEGATIVE VOLTAGE REGULATORS

MIL-M-38510/118

3.1 Background and Introduction

Prior characterization efforts for RADC have resulted in the development of slash sheets for Fixed Positive Voltage Regulators and Fixed Negative Voltage Regulators. These slash sheets, combined, specify regulators with ± 5 Volts, ± 12 Volts, ± 15 Volts and ± 24 Volts which survey showed are the predominate supply voltage requirements for either digital or analog circuits.

Several new innovative IC and hybrid devices incorporate precision circuitry and as such require low tolerance supply voltages. In addition, most large systems require a variety of supply voltages to provide power for digital circuits, analog circuits, display circuits, transducers, etc. The logistic problems associated with the variety of voltage regulators needed to power these devices can be greatly reduced by use os one of more adjustable voltage regulators together with a few standard value resistors.

Adjustable voltage regulators are available either as 4-terminal adjustable voltage devices or as 3-terminal adjustable voltage devices. Each of these styles has been characterized and is included on both of the slash sheets.

The following table shows the voltage regulators included in these specifications:

TABLE 3.1 Device Types Specified.

Device Type	Output Voltage Range	Maximum Output Current	No. of Terminals	Case Type	Commercial Type
11701	$5V \leq V_O \leq 30$ V	- 0.5 A	4	[illegible]-5	78MG
11702	$5V \leq V_O \leq 30$ V	- 1.0 A	4	[illegible]-3	78G
11703	$1.25V \leq V_O \leq 37$ V	- 0.5 A	3	[illegible]-5	LM117H
11704	$1.25V \leq V_O \leq 37$ V	- 1.5 A	3	[illegible]-3	LM117K
11801	$-30V \leq V_O \leq -5$ V	0.5 A	4	[illegible]-5	79MG
11802	$-30V \leq V_O \leq -5$ V	1.0 A	4	[illegible]-3	79G
11803	$-37V \leq V_O \leq -1.25$ V	0.5 A	3	[illegible]-5	LM137H
11804	$-37V \leq V_O \leq -1.25$ V	1.5 A	3	[illegible]-3	LM137K

3.2 Description of Device Types

The major physical distinctions between the various voltage regulators characterized for these two slash sheets are shown in Table 3.1. The major distinguishing features are: 1) voltage range and polarity, 2) maximum output current, 3) number of terminals and 4) case size. Whereas, the 4-terminal adjustable regulators are evolved from their fixed voltage counterparts by deleting the two internal resistors used to set the output voltage and by bringing the error amplifier summing point out of the case, the 3-terminal adjustable regulators represent different approach in IC voltage regulator design and do not have 3-terminal fixed voltage counterparts.

All of these devices contain protective circuitry common to many of the available IC voltage regulators. These circuits include a) output current limiting, b) short circuit protection, c) safe operating area protection and d) thermal shut down. In addition, the regulators included in these slash sheets feature "band-gap" reference voltage circuitry to fix and stabilize the output voltage. These reference voltage circuits are characterized by improved noise and long-term-stability. Generally, these characteristics are 10-100 times better than those found in standard avalanche breakdown reference voltage zener diodes. A simplified schematic of a band-gap reference is shown in Figure 3.1.

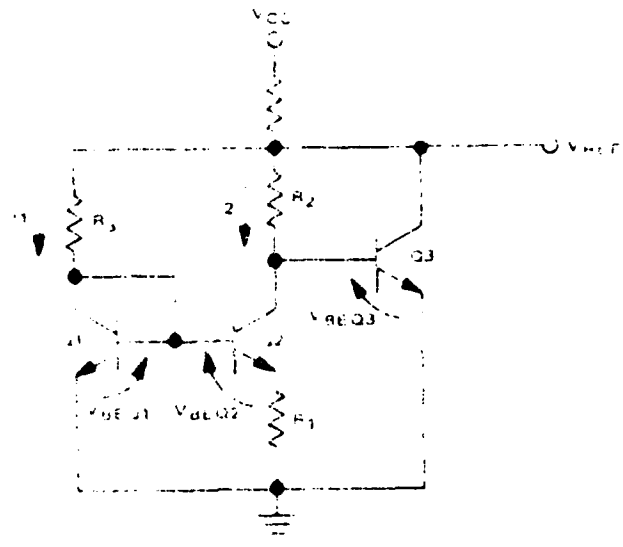


Figure 3.1. Bandgap reference

In this circuit, two monolithic transistors operating at different collector current densities develop a voltage ΔV_{BE}, at the emitter of Q2. This voltage has the relationship: $\Delta V_{BE} = \frac{KT}{q} \ln \frac{(I1)}{(I2)}$ and the temperature coefficient (TC) of this voltage is positive. When the voltage is amplified and added to the base-emitter voltage of Q3, which has a negative TC, the resultant output is:

$$V_{REF} = V_{BEQ3} + \frac{R2}{R1} \Delta V_{BE}.$$

By proper adjustment of the gain (R_2/R_1), the negative TC of V_{BEQ3} can be made to cancel the positive TC of ΔV_{BE}. The result is a voltage reference that has nearly zero temperature drift.

A simplified schematic of a positive voltage regulator showing the various protective circuits is shown in Figure 3.2. For the negative voltage regulators, circuit arrangement and performance is very similar.

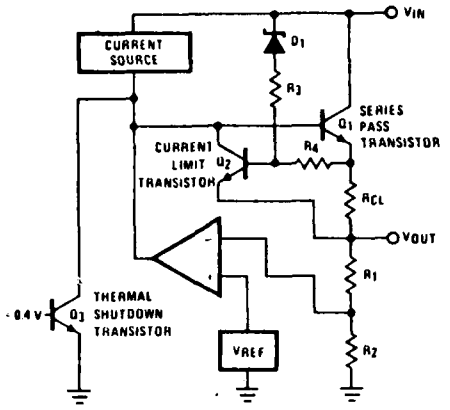


Figure 3.2. Ajustable Voltage Regulator with Protection Circuits.

The current limit circuit consists of Q2, R3 and R_{CL}. Resistor R_{CL} is in series with the output and carries the output current. Transistor Q2 is normally turned off; however, as the output current increases the voltage across R_{CL} increases and transistor Q2 begins to turn on. As Q2 conducts some of the series pass transistor base current is shunted around the transistor to the output and the current gain of the output circuit is effectively decreased. Thus, the total output current is degraded by the decrease in the output circuit current gain.

The safe area protection circuit consists of diode D1, transistor Q2 and resistors R3, R4 and R_{CL}. In the normal operating mode, Q2 is turned off and the current path for D1 is through resistors R3, R4 and R_{CL}. Since this is a high impedance path the diode current is insufficient to cause diode conduction. However, when the regulator is operating in a current limit mode, transistor Q2 is turned on, and diode D1 conducts through the transistor base-emitter junction. If the $V_{in} - V_{out}$ voltage is greater than the breakdown voltage of the diode (6-8 volts), large base currents flow through Q2 and current limiting adjust to a much lower current level. Thus, the output short circuit current is greatly reduced as the regulator input voltage is increased.

The thermal shut down circuit consist of a transistor Q3 that is normally biased with is base-emitter junction voltage just below conduction ($V_{BE} \approx .4$ V). The thermal shutdown transistor is physically located next to the series pass transistor so that the two transistor temperatures are approximately the same. As the series pass transistor temperature increases, the required base-emitter voltage, necessary to turn-on the thermal shut down transistor, decreases. At temperatures around 150° C - 190°C, transistor Q3 turns on and the base current to the series pass transistor is shorted to ground. With these built-in protection circuits, the voltage regulator is virtually fail proof under the most abnormal operating conditions.

3.2.1 Four-terminal Adjustable Voltage Regulators

General block diagrams for the 4-terminal adjustable positive voltage regulator and the 4-terminal adjustable negative voltage regulator are respectively shown in Figures 3.3 and 3.4.

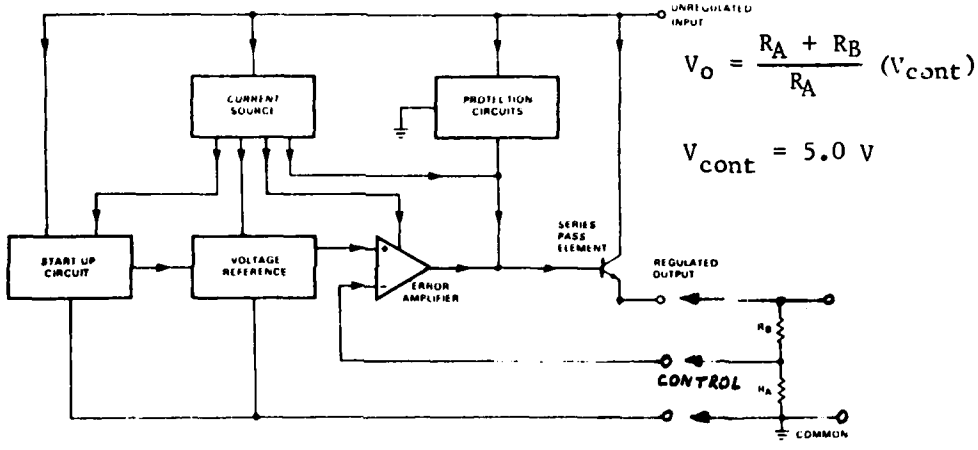


Figure 3.3. Block diagram of 4-terminal adjustable positive voltage regulators.

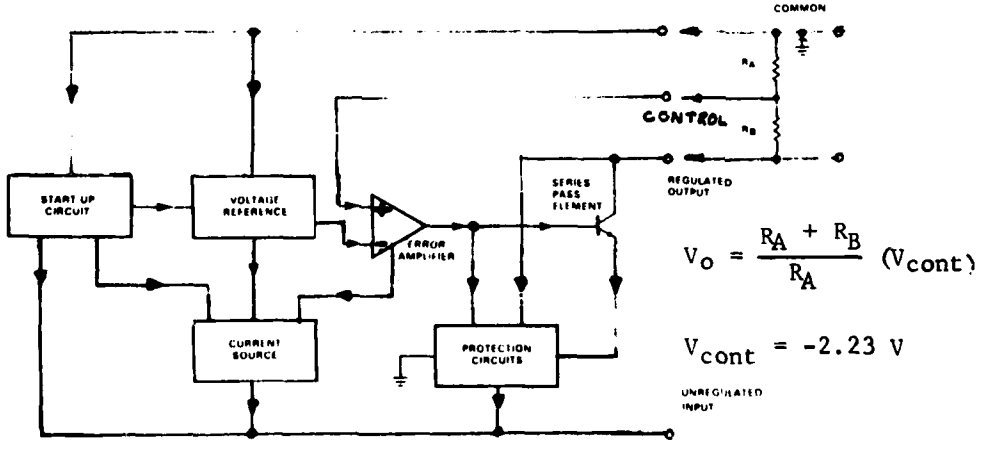


Figure 3.4. Block diagram of 4-terminal adjustable negative voltage regulators.

Both regulator circuits are made up of a) a start-up circuit to insure that the device is rapidly brought into regulation, b) a temperature-compensated voltage reference with a current source to eliminate the effect of the unregulated input voltage, c) an error amplifier that compares a fraction of the output voltage with the internal reference voltage, d) a series pass regulating transistor that controls the current output to the load, e) a series resistor and current limit to regulate the peak output current, f) a safe operating area circuit which operates with the current limit circuit to reduce the regulator's peak output current as the input voltage increases and g) a thermal shut-down circuit that turns off the pass transistor when its temperature exceeds 150°C - 190°C.

Circuit variations exist between each of the 4-terminal regulators as a result of the polarity differences and as a result of the maximum output current differences. A detailed discussion of the regulator circuits can be found in reference 1 listed in Section 3.6.

3.2.2 Three-terminal Adjustable Voltage Regulators

General block diagrams for the 3-terminal adjustable positive voltage regulator and the 3-terminal adjustable negative regulator are, respectively, shown in Figures 3.5 and 3.6.

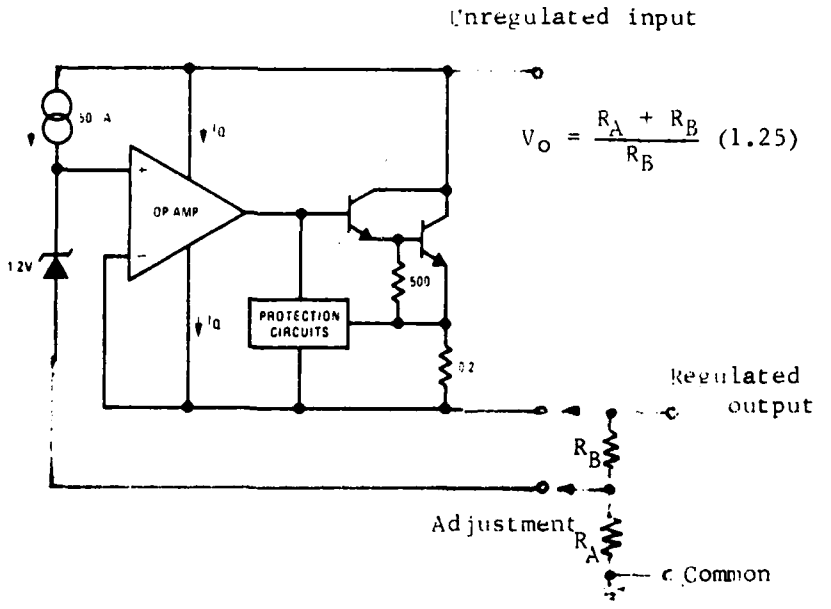


Figure 3.5 Block diagram of 3-terminal adjustable positive voltage regulators.

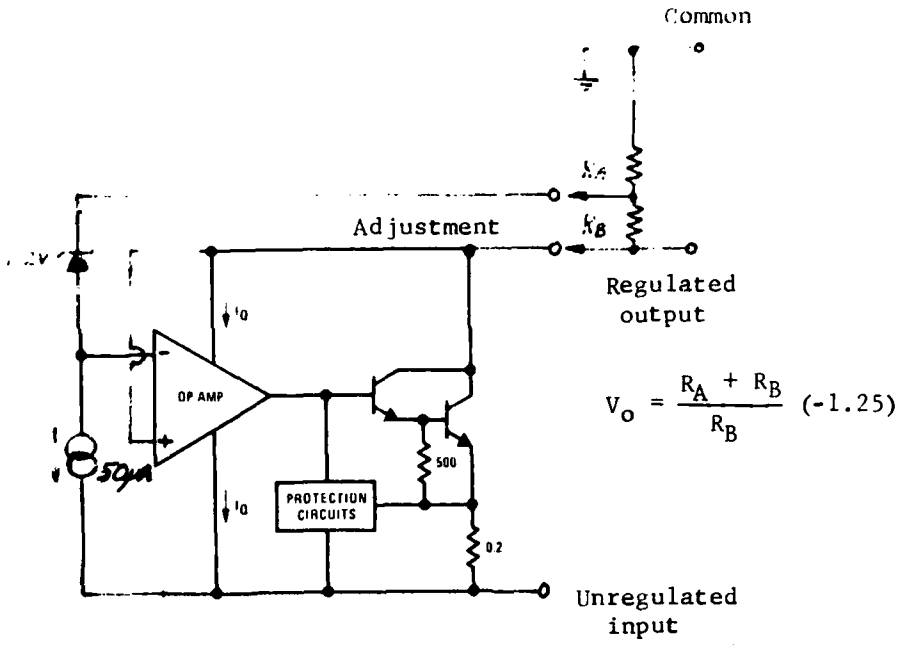


Figure 3.6. Block diagram of 3-terminal adjustable negative voltage regulators.

The 3-terminal adjustable voltage regulators vary markedly from the 4-terminal adjustable voltage regulators. The most outstanding feature of the 3-terminal regulators are that a) the quiescient current flows out of the regulator output pin instead of flowing out of the regulator adj (common) pin, b) the only current flowing out of the regulator adj pin is a low level current (50 uA) for the reference circuit, c) the error amplifier is a fixed unity gain amplifier and is therefore easily frequency stabilized, d) the voltage reference circuit does not require a special start-up circuit and e) large voltage stresses are restricted to the series pass transistor and to the on-chip current sources. The voltage (V_o - V_{adj}) is a constant 1.2 volts. In addition, circuit refinements have resulted in improved thermal and load regulation. A detailed discussion of the regulator circuits can be found in reference 2 listed in section 3.6.

3.3 Device Characterization

Characterization of the 3-terminal voltage regulators was performed in two parts. The static tests that measure the d.c. parameters were performed on the Tektromix S-3263 Automatic Test System at -55°C, 25°C and 125°C. The dynamic tests including transient tests and a.c. tests were performed in a bench test setup at 25°C. The characterization effort for the 4-terminal voltage regulators was greatly reduced because of the similarity in design between the 4-terminal adjustable regulators and their 3-terminal fixed counterparts. The 3-terminal fixed regulators have been characterized in previous contracts to RADC and a report on this effort is provided in references 3 and 4 of section 3.6.

3.3.1 Automatic Test Development

Software was developed for the Tektronix S-3263 test system to provide for automatic testing of both the positive and negative adjustable voltage regulators. All static tests recommended by the JC-41 Committee and some GEOS added static tests were included as part of the software package.

3.3.1.1 S-3263 Test Adapter

The test adapter, shown in Figures 3.7 and 3.8, was designed to provide an interface between the DUT and the Test System. The adapter has the ability to test positive and negative, 3-terminal and 4-terminal, 1/2 amp, 1 amp and 1.5 amp regulators. This capability is achieved by using a separate plug-in carrier for each type of DUT. The carrier contains the input and output capacitors for the DUT, and plugs into the S-3263 main test adapter. In addition, the DUT protection diodes, and the current regulators and transistor used in the start-up circuit are on a separate 16-pin DIP carrier and are changed when the voltage polarity of the DUT to be tested is changed. Also the main current carrying power Darlington transistors are plug-in and can be changed from NPN to PNP or vice versa when the voltage polarity of the DUT is changed. Other plug-ins include load resistors and output voltage fixing resistors. In addition, the voltage measurement system has made extensive use of Kelvin test leads to insure that measurements are made at the precise point of interest.

3.3.1.2 Test Circuits and Procedures

The static test circuits developed for these characterization efforts were designed to permit regulator testing by either automatic test systems or by bench test instrumentation. Schematics are shown in Figures 3.9 and 3.10 and the test circuit set ups are listed in Tables 3.3 through 3.10.

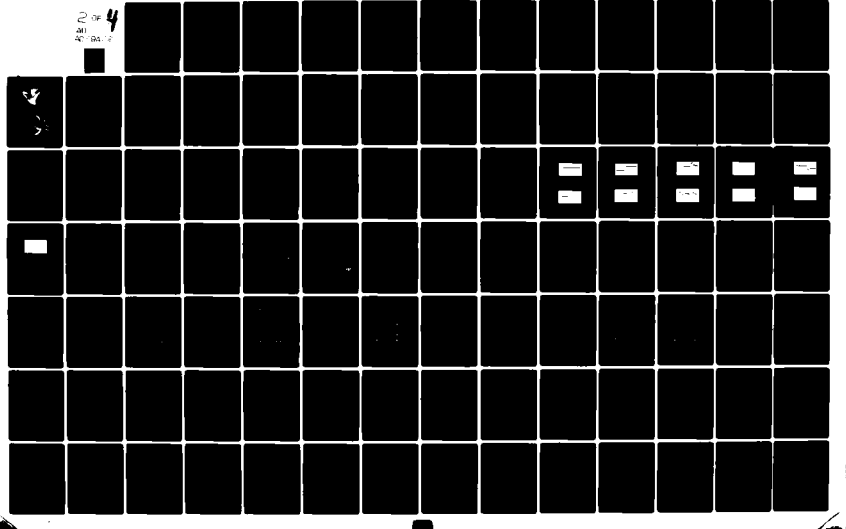
The main DUT currents are carried by separate buses and are controlled by the automatic test system via the power Darlington transistor circuits. Through use of external power supplies, the adapter test circuits permit control of currents that are larger than the current capacity of the automatic test system.

The input power Darlington transistor circuit can force the value of the DUT input voltage and can be used to control it for testing a) output voltage versus input voltage, b) line regulation, c) short circuit current versus input voltages, d) start up, e) line transient and f) ripple voltage rejection. The output power Darlington transistor circuit can be used to force a current and measure the voltage or to force a voltage and measure the current. The circuit can be controlled for testing a) output voltage versus load current, b) load regulation, c) thermal regulation, d) short circuit current, e) voltage recovery, and f) load transient. The current-to-voltage amplifier is used to measure the milliampere and microampere currents for a) the standby current drain tests, b) the control current tests, c) the adjust pin current tests and d) the quiescent current test under a forced voltage condition.

3.3.1.2.1 V_{OUT}, V_{RLINE}, V_{RLOAD} & V_{RTH} Tests

All of the output voltage measurements use Kelvin sense leads and are measured differentially to the DUT reference point. The sense lead for the output voltage, line and load regulation measurements is terminated with a test clip lead. The clip lead is clipped to the DUT output lead 1/8 inch from the case. The voltage measurements are differentially compared to the output of a d.c. voltage standard and the difference voltage is amplified to optimize the best test measurement accuracy. The test circuit is as shown in Figure 3.11.

AD-A089 422 GENERAL ELECTRIC CO PITTSFIELD MA ORDNANCE SYSTEMS F/G 9/5
ELECTRICAL CHARACTERIZATION OF SPECIAL PURPOSE LINEAR MICROCIRC--ETC(U)
MAY 80 J S KULPINSKI, T SIMONSEN, L CARROZZA F30602-78-C-0195
UNCLASSIFIED RADC-TR-80-49 NL



The circuit is used to measure line and load regulation on the LM117 and LM137 regulators. For the LM117 regulator the output voltage varies from 1.2 volts to 1.3 volts. With the voltage standard set to - 1.056 volts, the op amp output is

$$V_M = 4.42\ V_O - 1.056 \quad (4.42)$$

and for $1.2\ V \leq V_o \leq 1.3\ V$

$$.63\ 6 \text{ volts} \leq V_M \leq 1.078 \text{ volts}$$

When two successive measurements are made, the two measured values are

$$V_M' = 4.42\ V_o' - 4.66752$$

$$V_M'' = 4.42\ V_o'' - 4.66752$$

These measurements are subtracted to determine the differential voltage,

$$V_M' - V_M'' = 4.42\ (V_o' - V_o'')$$

and the voltage regulation is determined by the expression

$$\Delta V_o = \frac{V_M' - V_M''}{4.42}$$

Output voltage measurements are made by using a resistive voltage divider network. The network divides the voltage so that for an output voltage range $1.2\ V \leq V_o \leq 1.3\ V$, the measurement voltage range is $.923\ V \leq V_M \leq 1.0\ V$. This permits measurements to be made at the top end of the 1 volt range rather than at the bottom of the 10 volt range. An alternate test circuit for these measurements is discussed in Section 3.5.

3.3.1.2.2 I_{ADJ} and I_{SCD} *Current Tests (Line & Load)*

I_{ADJUST} currents of the LM117 & LM137 are measured while performing line and load regulation tests by using a current-to-voltage amplifier. The main reasons the S-3263 current measuring capability is not used is as follows:

1) inadequate accuracy & resolution for ΔI_{ADJ} measurements
2) reduces the chance of damage to test system if gross failure of device under test occurred.

The current-to-voltage amplifier uses an LF155 op amp which is selected because of its low input bias current and because this minimizes errors. The gain is selected for the best DVM measurement range. The output of the amplifier is then coupled to an external voltmeter under IEEE bus control. The relationship of the measured voltage to the current is

$$I_{ADJ} = \frac{V_M}{R_f}$$

The amplifier is also used to measure the I_{SCD} current for the 4-terminal regulators. Relays are used to control the currents applied to the op amp summing point.

3.3.1.2.3 I_Q Test and $I_{CONTROL}$ Test

The current-to-voltage amplifier design includes a mode of operation that allows forcing of its summing point to a specified voltage value. When the quiescent current (I_Q) is to be measured for the LM117, the summing point is forced to 1.4 volts and is connected to the regulator output terminal. The current that flows out of the regulator under these conditions is the quiescent current. The measured amplifier output voltage and the quiescent current have the relationship

$$I_Q = \frac{(V_M - V_F)}{R_f}$$

For the LM137 the forced voltage is - 1.4 volts and the circuit operation is as defined above.

The measurement of the $I_{CONTROL}$ current for the 4-terminal regulators is similar. The control pin is connected to the summing point and is forced to the proper voltage by setting the amplifier non-inverting input voltage (5.0 volts for the positive regulators and -2.23 volts for the negative regulators). The measured amplifier output voltage and the control current have the relationship

$$I_{CONTROL} = \frac{(V_M - V_F)}{R_f}$$

In addition to steering the proper currents to the summing point, relays are used to change the current-to-voltage gain for the control current measurement.

3.3.1.2.4 I_{OS}, I_{PEAK} & V_{OUT} Recovery Tests

Short circuit (I_{OS}) and peak output current (I_{PEAK}) tests are performed by programming the load circuit power Darlington network into a second mode via relay control & S-3263 system. This mode of operation forces the output voltage of the regulator for a given time into short circuit (V_{OUT} = Ø V) on I_{PEAK} current conditions (forces to predetermined regulator output voltage). The resultant currents are measured through a 1 ohm sensing resistor in series with the Darlington circuit via the S-3263 measurement subsystem.

The V_{OUT} (recovery) test is measured by first removing the regulator from the forced output condition and then allowing the output voltage to recover into a resistor, capacitor load after a given time. This test was added to determine if the regulator is capable of re-starting itself after short circuit conditions and provides important application information to the user of the regulators.

3.3.1.2.5 V_{START} Tests

The start-up circuit consists of an input Darlington circuit which provides the necessary fast turn-on characteristics as well as a programmed input voltage to the regulator's input. The start-up circuits shown in Figures 3.7 & 3.8 measure the ability of the regulator to respond to extreme combinations of input voltage, and load currents by measuring the output voltage after a predetermined time. The load resistance during testing is shunted by a 20 ufd capacitor to simulate total distributed by-pass capacitors found in many system applications.

Although, I_{OS}, I_{PEAK} & V_{OUT} (recovery) tests are listed separately they are, in fact, combined as part of the V_{START} tests and provide a very subjective set of conditions to the regulator. The order in which the tests are performed is shown in Figures 3.12 & 3.13 and is stated as follows:

1) Starting circuit applies input voltage to regulator.

2) I_{OS} or I_{PEAK} test forces the regulator output to the specified voltage value and

3) V_{OUT} recovery test allows the regulator to recover into a load circuit.

3.3.1.3 Test Accuracies And Correlation

All of the adapter test circuit gains and scaling factors are determined by using a precision voltage standard and a precision voltmeter. The precise gain value is used in the software program to calculate the test results from the measured data. Aside from some initial circuit stability problems, the most basic problems encountered while developing the test circuits and programs dealt with the S-3263 machine measurement accuracy. The S-3263 could not achieve, by itself, the accuracy or resolution necessary to meet the desired 10:1 test accuracy required for good test measurement systems. Essentially, the accuracy problems encountered during the measurement of the test parameters are overcome by increasing the gain of the signal to be measured and by level shifting the signal value to allow use of the most accurate portion of the most accurate measurement range.

Without the use of the current-to-voltage amplifier, the test system resolution on any current range would be sufficiently bad to render the ΔI_{ADJ} measurements meaningless. The current-to-voltage amplifier has a gain of 2000 V/A for all I_{ADJ}, I_{SCD} AND I_Q measurements and its gain is 33200 V/A for the $I_{CONTROL}$ current measurement. The desired measurement accuracy for measuring V_{out} was readily achieved by scaling the signal voltage to a more accurate part of the voltmeter range. However, because of resoltuion these measured values were too inaccurate to be used to calculate line and load regulation. The test circuit described in section 3.3.1.2.1 provides a gain of approximately 4.42 over the direct output voltage measurement and gives sufficient accuracy.

The results of the test accuracies achieved during characterization are shown in Table 3.11. There are few parameters where the S-3260 tests failed to meet the desired 10:1 test accuracy.

As can be seen from Table 3.11, the basic S-3263 measurement accuracy would have failed to meet the 10:1 test accuracy. However with the additional circuitry incorporated into the S-3263 test adapter, the desired results were achieved.

A plot of the measured voltage vs percent error voltage on the S-3263 shows the basic capability of each range. Factored into these curves are the following:

1) percent of range
2) offset voltage
3) resolution

Another concern in selecting measurement ranges is the time required to sample and the time for the measurement system to settle out. An example of the types of problems encountered while selecting S-3263 ranges is as follows:

1) 100 mV range: best resoltion, worst accuracy, worst settling time

2) 1 & 10 volt range: best accuracy, best settling time
However in making delta measurements of V_{out}, the resolution can be a significant error term, and a dominating factor when selecting ranges.

Over all, the S-3263 still has one of the best sampling rates (200 samples/sec) which exceeds an external IEEE DBM by at least an order of magnitude. However, it is still necessary to consult the S-3263 measurement accuracy table before developing S-3263 test capability. Figures 3.14 through 3.18 show the basic test system accuracies for each voltage range.

The initial attempts to correlate data on the S-3263 test system to bench data, brought to light the system inadequacies in making measurements discussed above. The predominate errors were the gross instabilities of the delta measurements as a result of the machine resolution. At this time, the machine accuracies were checked for each measurement and the need for special test circuits was determined. With the addition of the new circuits to the adapter, correlation was checked and found to be well within the 20% requirement for correlation (ie 10% measurement error for each test set up).

Bench measurements were made using the test adapter as a carrier for the DUT. The adapter was checked to determine that it was capable of forcing the proper voltages and currents by programming the test circuits. Currents were checked by inserting an ammeter in series with current to be measured. Voltage measurements were then converted to calculated current values and were compared with the measured values. Absolute voltage measurements were taken at the DUT pins and were compared with the measurements at the sense line outputs and finally load regulation measurements were checked on an oscilloscope using a differential input pre-amplifier capable of measuring 10 uV/cm while the load current was changed the specified amount. The actual output voltage measurements at the DUT were then compared to the differential amplifier output measurements.

3.3.2 Bench Tests

Dynamic tests for the voltage regulators include a) ripple rejection, b) line transient response, c) load transient response and d) output noise. These tests were run on the LM117 and LM137 adjustable voltage regulators. No dynamic tests were run on the 78MG, 78G, 79M9 and 79G because of their similarity to the 7800 and 7900 voltage regulator families which were characterized on a previous contract.

Bench test circuit schematics are shown in Figures 3.19 thru 3.26. The noise test circuit schematics are shown in Figures 3.19 & 3.20. The test is performed using an oscilloscope with a differential preamplifier that has bandwidth control. The bandwidth was set to have a pass band from 10 Hz to 10 kHz and the peak-to-peak measurement of the noise was made. The ripple rejection test circuit schematics are shown in Figures 3.21 & 3.22. The test was performed using the above oscilloscope. The bandwidth was adjusted to reduce the high frequency noise without affecting the 2400 Hz ripple frequency. The 2400 Hz ripple at the regulator was measured on the oscilloscope as a peak-to-peak voltage. Line transient response and load transient response test circuit schematics are shown in Figures 3.23 thru 3.26. The peak measurements were made on a high frequency oscilloscope.

3.4 Test Results and Evaluation of Data

3.4.1 LM117H Adjustable Positive Voltage Regulator

Tabulation of static test data taken on the S-3263 Automatic Tester for the LM117H Adjustable Positive Voltage Regulators is shown in Tables 3.12 thru 3.14. Because of the small sample of ten devices statistical analysis of the data was not performed. All of the devices save one met all of the parameter tolerances recommended by JC41 Sub-Committee on voltage regulators. The one device, serial number 4, failed load regulation. The specification for this parameter is ± 3.5 mV. The measured value was -4.75 mV. Analysis of this failure was done by measuring the device parameter in a bench set up using an oscilloscope. Pictures of the measurements were taken at the case, on the output lead 1/8 inch below the case, and on the output lead 3/8 inch below the case and are shown in Figures 3.27 thru 3.29, respectively. The load regulation measurements at these points were approximately 1 mV, 4.5 mV and 9 mV, respectively. As a result of contact with the vendor, on this and other similar failures reported herein, it was learned that the leads on the TO-5 type cases are made of Kovar. The resistivity of Kovar can be as much as 28 times that of copper (see reference 5 , section 3.6). This high resistivity is the reason for the high load regulation measurements. The results and recommendations associated with this problem are discussed in Section 3.5.2.

Two units, serial numbers 5 and 6, failed thermal regulation at -55 C. Since this measurement is not recommended at either -55 C or 125 C, these devices were not considered failures. However, these two units have been sent to the vendor for their measurement and analysis.

Tabulation of dynamic test data taken in a bench test set up for the LM117H Adjustable Positive Voltage Regulators is shown in Table 3.15. The tests were performed at 25 C and are of a) ripple rejection, b) output voltage noise, c) line transient response and d) load transient response. All of the bench measurements made on these devices were stable and showed reasonable safe margin for the recommended tolerances. Oscillographs of the Line and Load Transient Responses are shown in Figures 3.30 and 3.31.

3.4.2 LM117K Adjustable Positive Voltage Regulators

Tabulation of static test data taken on the S-3263 Automatic Tester for nine LM117K adjustable positive voltage regulators is shown in Tables 3.16 thru 3.18. All of the devices met the tolerances recommended by the JC41 Subcommittee on Voltage Regulators.

Tabulation of dynamic test data taken in a bench test set up is shown in Table 3.19. All of the devices met the tolerances recommended by the JC-41 Subcommittee on Voltage Regulators. Oscillographs of the line and load transient responses are shown in Figures 3.32 and 3.33.

3.4.3 LM137H Adjustable Negative Voltage Regulators

Tabulation of static test data taken on the S-3263 Automatic Tester for ten LM137H Adjustable Negative Voltage Regulators is shown in Tables 3.20 thru 3.22. All of the devices failed load regulation for current changes from 5-to-500 mA. The vendor was contacted on this matter and confirmed the problem. The vendor has issued a letter on this problem and recommends that the current changes be reduced to 5-to-200 mA. The devices met all other parameter tolerances recommended by the JC-41 Subcommittee on Voltage Regulators.

Tabulation of dynamic test data taken in a bench test set up is shown in Tables 3.23. The devices met all of the parameter tolerances recommended by the JC-41 Subcommittee. Oscillographs of the line and load transient responses are shown in Figures 3.34 and 3.35.

3.4.4 LM137K Adjustable Negative Voltage Regulators

Tabulation of static test data taken on the S-3263 Automatic Tester for eight LM137K Adjustable Negative Voltage Regulators is shown in Tables 3.24 thru 3.26. The devices met all of the parameter tolerances recommended by the JC-41 Subcommittee.

Tabulation of dynamic test data taken in a bench test setup is shown in Table 3.27. The devices met all of the recommended parameter tolerances. Oscillographs of the line and load transient response are shown in Figures 3.36 and 3.37.

3.4.5 Comparison of Test Data on 3-terminal Devices

The average values of the measurements of the 3-terminal adjustable voltage regulators is shown in Tables 3.28, 3.29 & 3.30 for temperatures of 25°C, - 55°C & 125°C, respectively.

3.4.6 Four-terminal Devices

Because of the similarity in the design of the 4-terminal adjustable regulators to their 3-terminal fixed voltage counterparts, a full characterization effort of these devices was not originally planned. Some one ampere negative adjustable regulators with date codes 7639 showed some anomalies in their electrical performance. Devices with more recent date codes have been requested from the vendor and data will be obtained on these parts for the next report.

3.5 Conclusions and Recommendations

3.5.1 Test Circuits

The large currents ($\geq$ 1 Amp) required to test these and future voltage regulators cannot be supplied or controlled by most automatic test systems. The test circuits designed for testing these voltage regulators are capable of interfacing with external power supplies and forcing the DUT input voltage levels and output load current levels. The power Darlington transistors can readily carry and control the 5 amps needed for the short circuit current and start-up tests; however, future voltage regulators needing 2-3 times this current will require different Darlington transistors than those used for these characterization efforts. The op amps used in these test circuits have relay switches connected to their inputs that change their operating mode during the test. Because of these switches, special stabilizing circuits may be required for the op amps.

The low level input circuits can be controlled by any automatic test system capable of forcing voltages between + 15 volts and - 15 volts. Although the test technique for measuring line, load and thermal regulation was adequate for these characterization efforts, it required a DC voltage standard. A more complex circuit is shown in Figure 3.38 which may be more desirable for production testing when additional resolution is needed by the test system.

The regulator output is simultaneously applied to the input of the sample/hold amplifier and to one input line of the summing amplifier. Prior to a time $t = t_o$, the S/H amplifier is in the sample mode. At $t = t_o$, the S/H amplifier is switched to the hold mode. After settling, the output voltage of the summing amplifier is measured. This voltage is an error signal (E) and is nominally 0 volts. At $t = t_1$, the regulator is stimulated to a new line/load condition. At a predetermined time after this (ie .5 ms), the output voltage (V_s) of the summing amplifier is measured. This measurement is proportional to the difference between the voltage regulator output at t_1 + .5 ms and the voltage regulator output at t_o. From these measurements we can calculate that the regulation is

$$\Delta V_R = \frac{V_s - E}{(R_f/R_i)}$$

3.5.2 Devices Under Test

The voltage regulators discussed in this section were tested on the S-3263 to determine their static electrical characteristics at 25°C, -55°C and 125°C. The devices were also tested in a bench type test setup to determine their dynamic (ie. transient AC) electrical characteristics at 25°C. The data shown in Tables 3.12 thru 3.27 indicates absence of data from some parts. These parts failed during test development as a result of improper voltages or polarity being applied to the regulators. None of the devices is known to have catastrophically failed in an operating test circuit.

The most significant parameter failure was the failure of load regulation for the LM137H voltage regulator. The vendor has confirmed these failures and suggests that load regulation, for V_{in} = - 6.25 V, be performed for 5 mA $\leq I_L \leq$ 200 mA. OS agrees with this decision; however, since the part is a 500 mA voltage regulator, it should also have a load regulation test performed for 5 mA $\leq I_L \leq$ 500 mA. OS also recommends that the limits shall be ± 20 mV at 25°C and ± 25 mV for - 55°C $\leq T_A \leq$ 125°C.

There is evidence in the published literature (reference 6, Section 3.5) that start-up and voltage recovery problems exist in some 3-terminal fixed voltage regulators. When the output of the regulator is shorted to ground under conditions of high input voltage, the safe area protection circuit turns on and may force the regulator output current to zero. Under these conditions, the safe area protection circuit maintains a zero current condition even after the short is removed. Consequently, the voltage regulator may not recover from a short circuit condition until the input voltage is removed and then reapplied. The timing sequence (shown in Figures 3.12 and 3.13) has been devised by OS to provide a rapid start-up condition into a maximum load resistance to insure start up with a voltage

step function, from 0 to V_{in}, at the DUT input, b) a short circuit condition at the output to measure the current limit and c) voltage recovery check to insure that the device will recover under a maximum resistive load co dition when the short circuit is removed. This test has been recommended by OS to provide functional assurance of the device's start-up capability under adverse system conditions. The test conditions and parameter tolerances recommended by OS and the JC-41 Subcommittee on Voltage Regulators are shown in Tables 3.29 thru 3.36.

3.6 Bibliography

1. Voltage Regulators Handbook: Andy Adanian, Fairchild Camera and Instrument Corporation, 1978.

2. Voltage Regulator Handbook: Nello Sevastopoulos et al, National Semiconductor Corporation, 1978.

3. RADC-TR-78-22 Final Technical Report: J. S. Kulpinski et al, General Electric Company 1978. (A052357)

4. RADC-TR-78-275 Final Technical Report: J. S. Kulpinski et al, General Electric Company, 1979. (A065997)

5. Reference Data for Radio Engineers; H. P. Westman, editor, International Telephone and Telegraph Corporation, 1957.

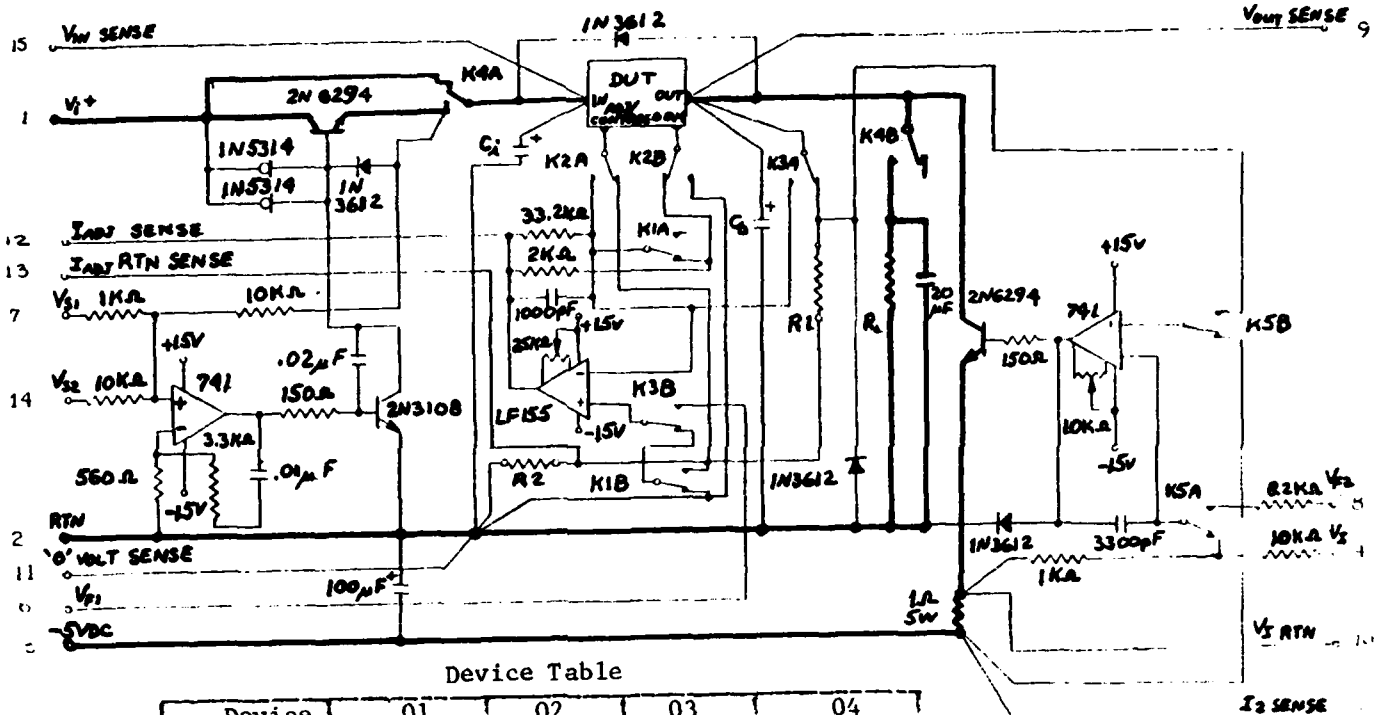
6. Designer's Guide To: IC voltage regulators: Robert C. Dobkin, National Semiconductor Corp., EDN August 20, 1979 and September 5, 1979.

(Top view)

Figure 3.7. Voltage Regulator Test Adapter.

(Bottom view)

Figure 3.8. Voltage Regulator Test Adapter.

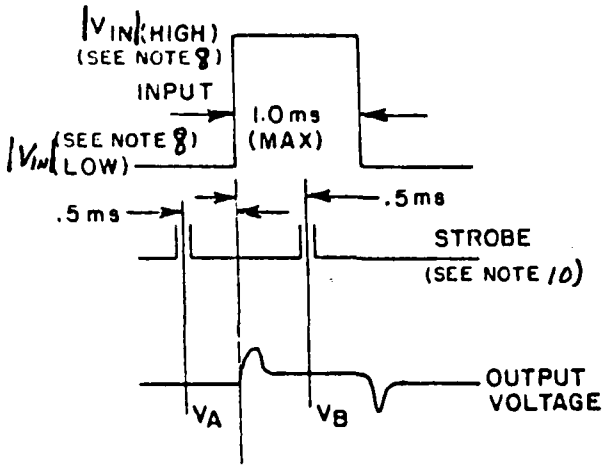


Device Table

Device Type	01 78MG	02 78G	03 LM117H	04 LM117K
R_1	0	0	249Ω	249Ω
R_2	5.0KΩ	5.0KΩ	0	0
R_L	10Ω	5Ω	2.5Ω	.833Ω
C_i	0.33uF	0.33uF	1.0uF	1.0uF
C_o	0.1uF	0.1uF	1.0uF	1.0uF

Figure 3.9. Positive voltage regulator test circuit for static tests.

LINE REGULATION WAVEFORMS



LOAD REGULATION WAVEFORMS

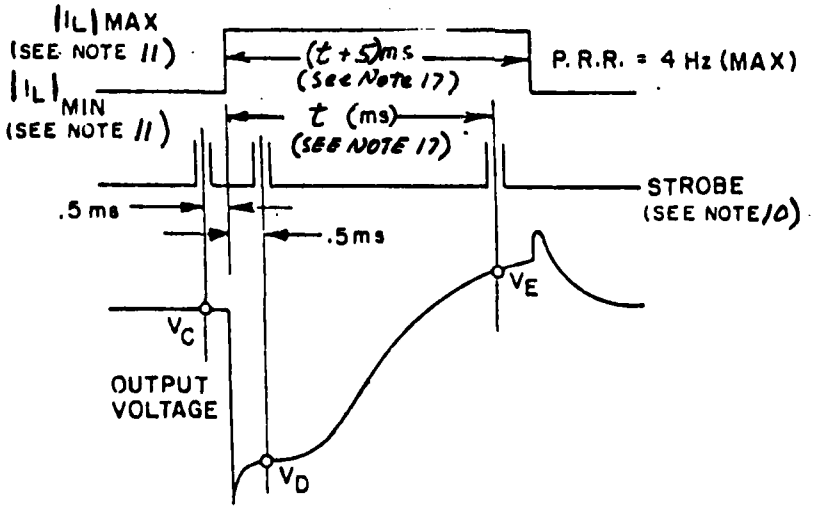
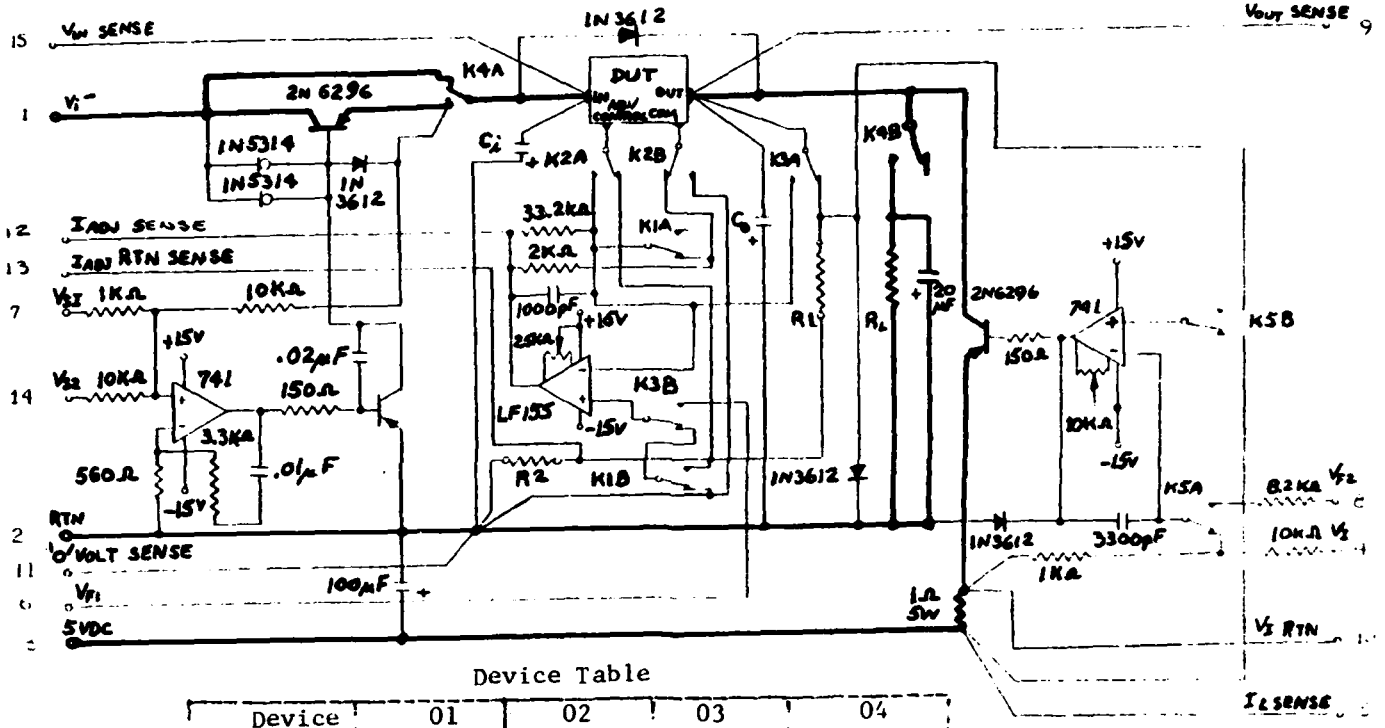


Figure 3.9. Positive voltage regulator test circuit for static tests (cont'd).

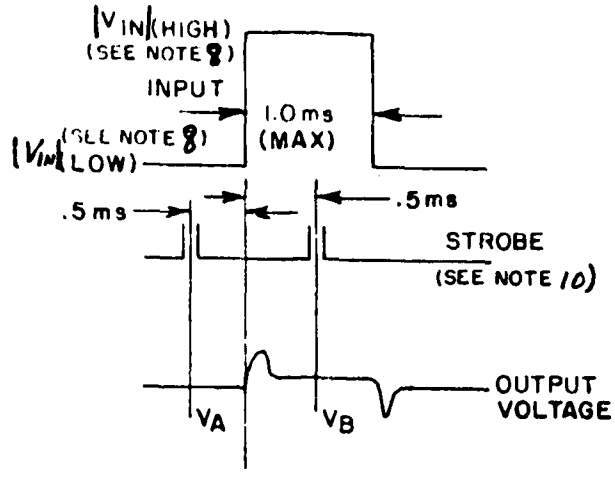


Device Table

Device	01	02	03	04
Type	79MG	79G	LM137H	LM137K
R_1	2.74KΩ	2.74KΩ	249Ω	249Ω
R_2	2.21KΩ	2.21KΩ	0	0
R_L	10Ω	5Ω	2.5Ω	.833Ω
C_i	2.0μF	2.0uF	1.0uF	1.0uF
C_o	2.0uF	2.0uF	1.0uF	1.0uF

Figure 3.10. Negative voltage regulator test circuit for static tests.

LINE REGULATION WAVEFORMS



LOAD REGULATION WAVEFORMS

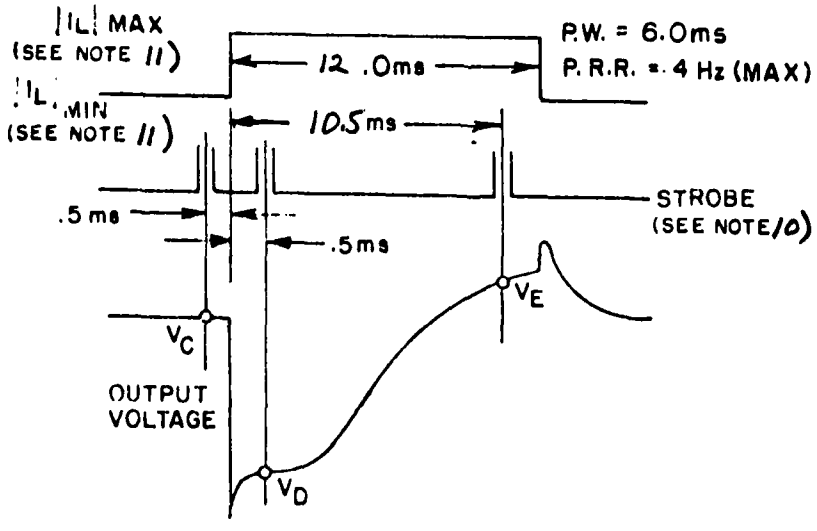


Figure 3.10. Negative voltage regulator test circuit for static tests (cont'd).

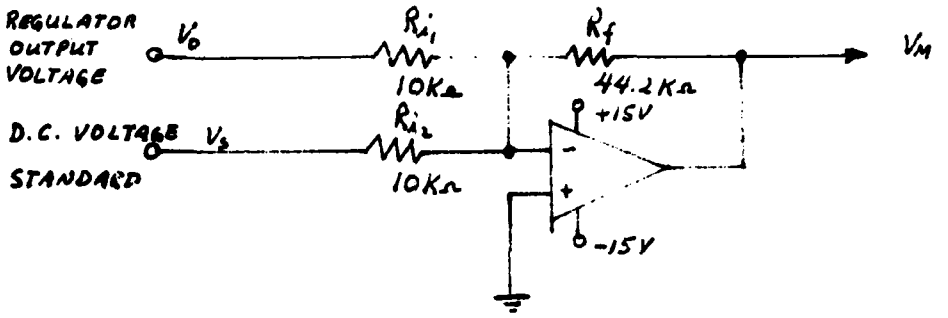


Figure 3.11. Level shift circuit and amplifier for V_{RLINE}, V_{RLOAD} & V_{RTH} tests.

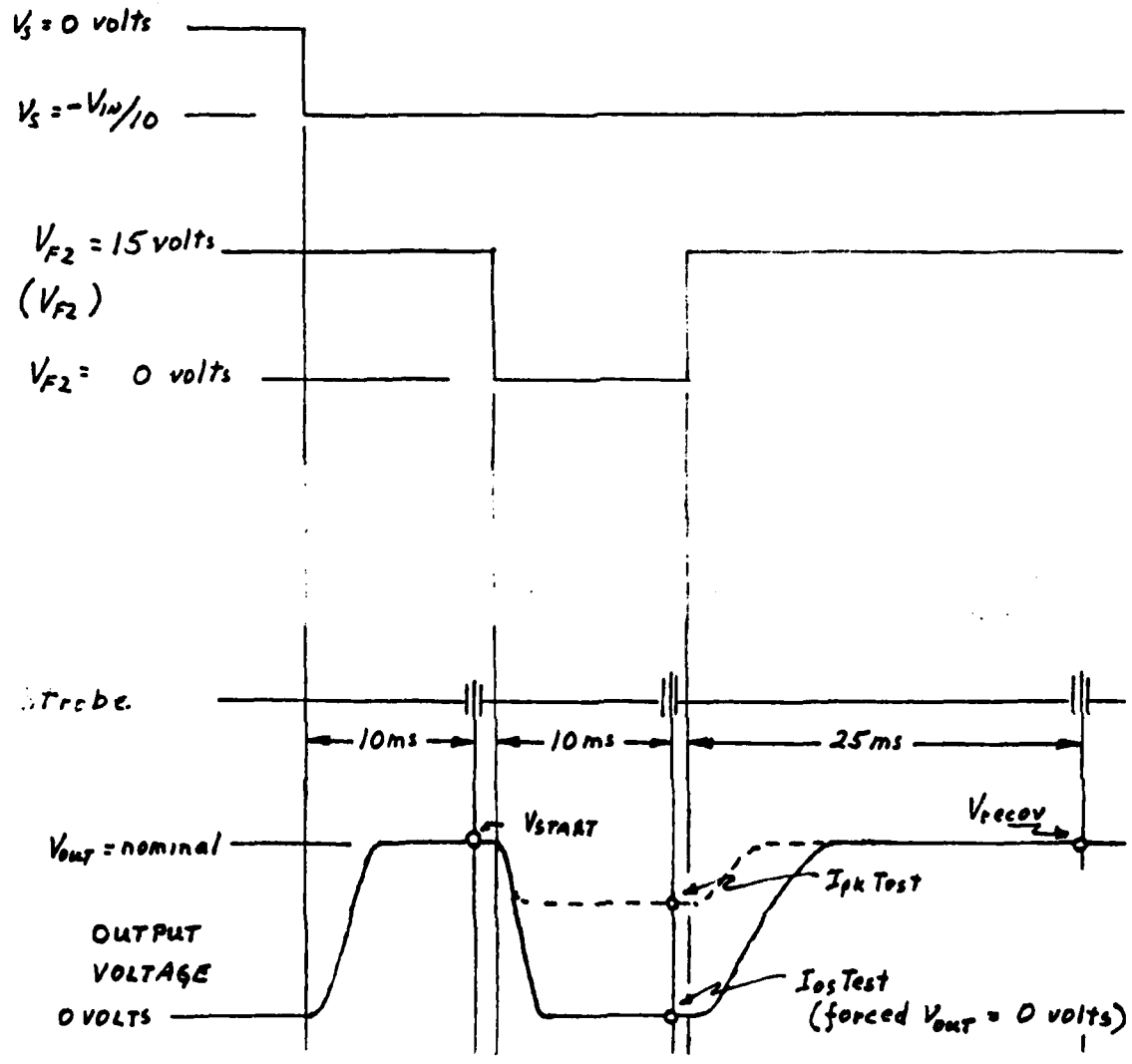


Figure 3.12. Positive voltage regulator timing sequence for V_{START}, I_{OS} & V_{OUT} RECOV.

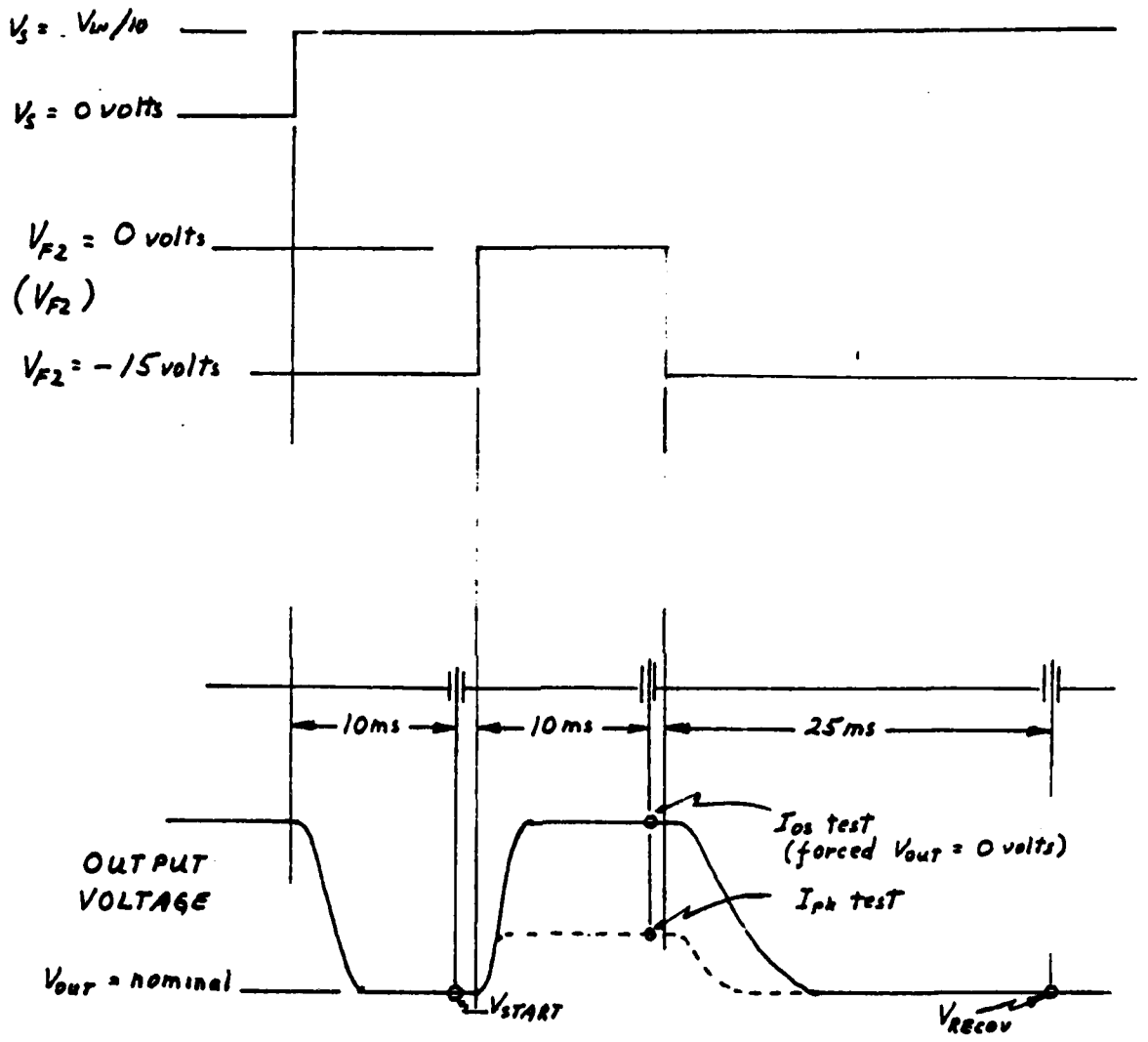


Figure 3.13. Negative voltage regulator timing sequence for V_{START}, I_{OS} & V_{OUT} RECOV.

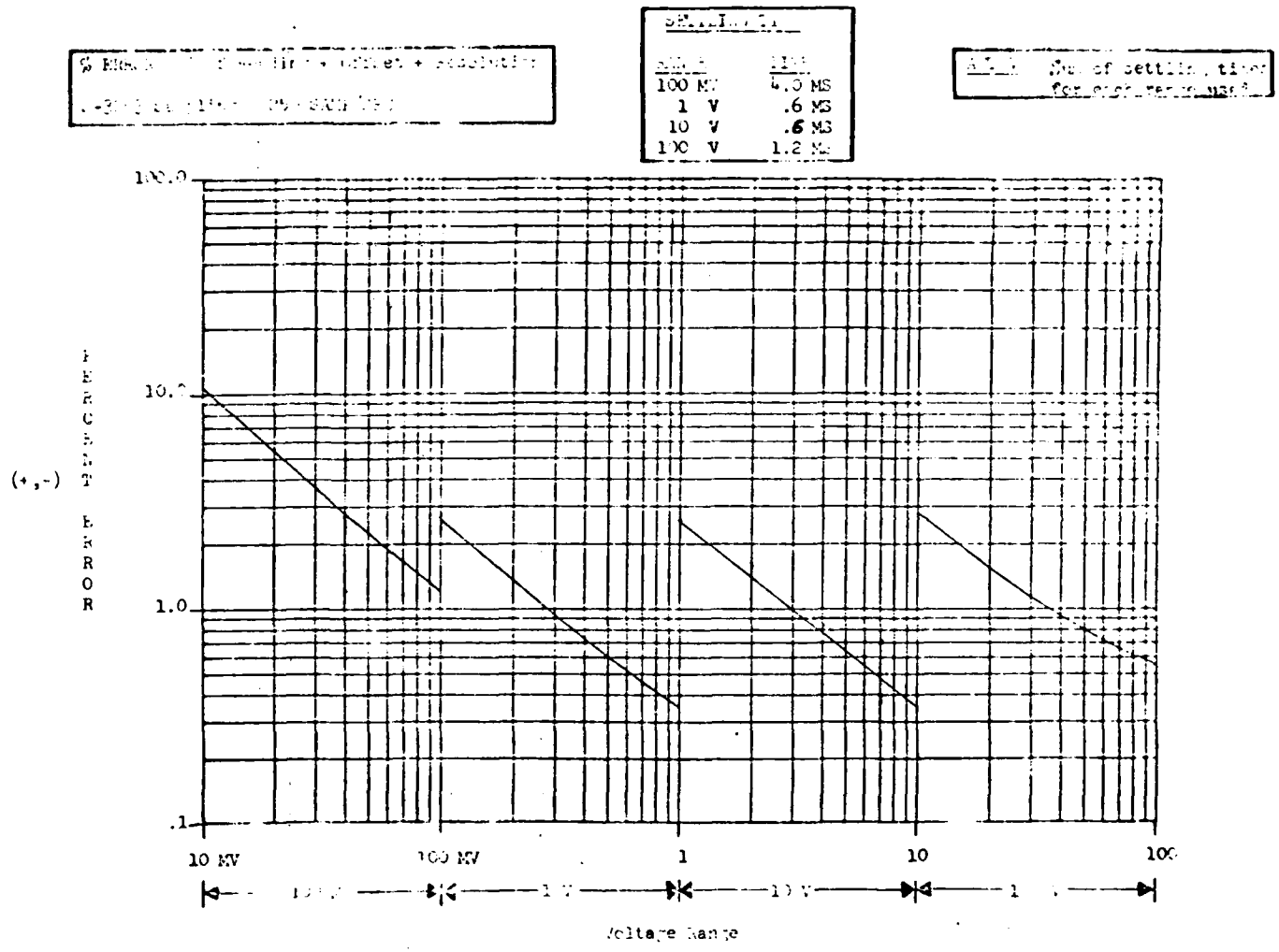
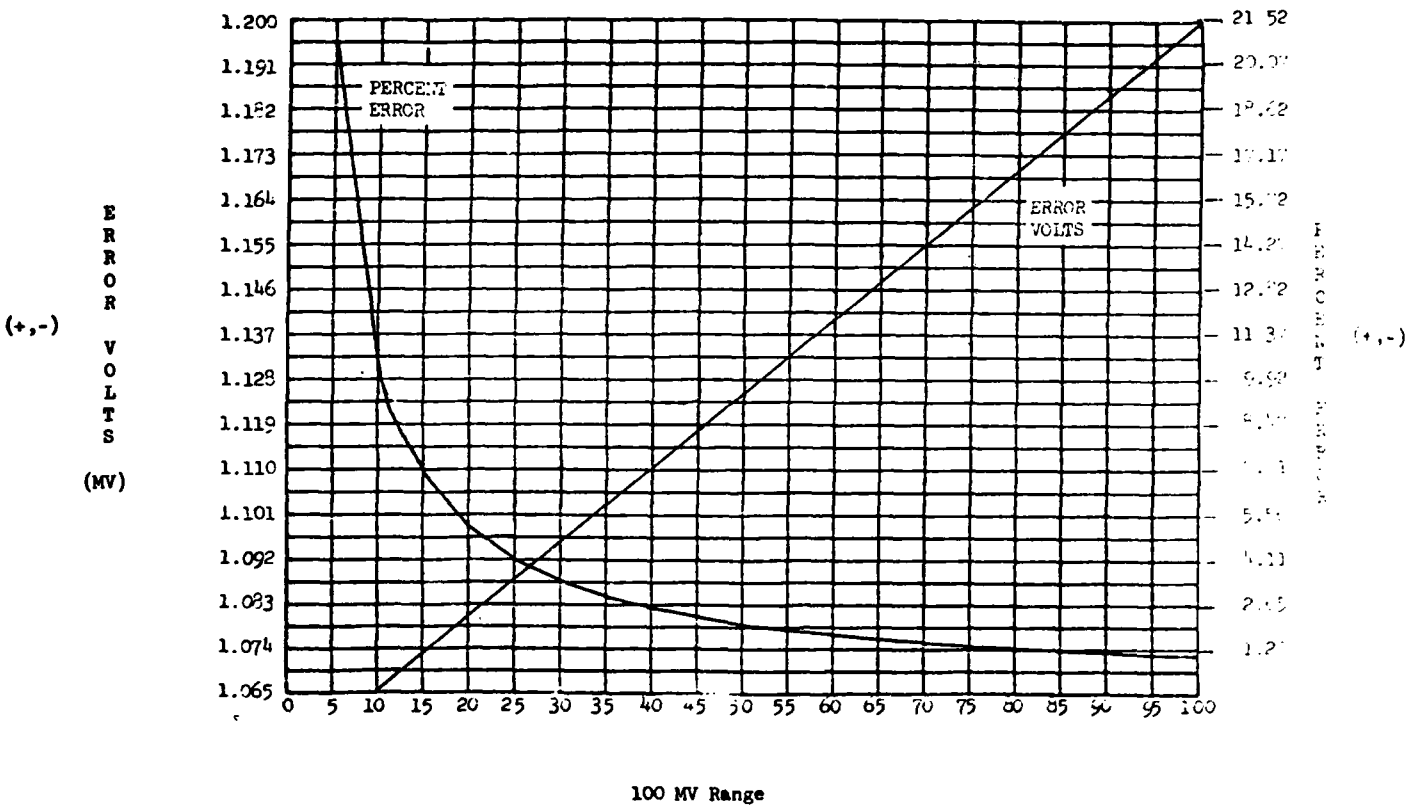


Figure 3.14. S-3263 Test System Differential Voltage Accuracy.

ACCURACY

100 MV Range = ±(0.15% of Reading + 1 MV + .05% of Range



(+,-) ERROR VOLTS (MV)

(+,-)

Figure 3.15. S-3263 Test System Differential Voltage Accuracy

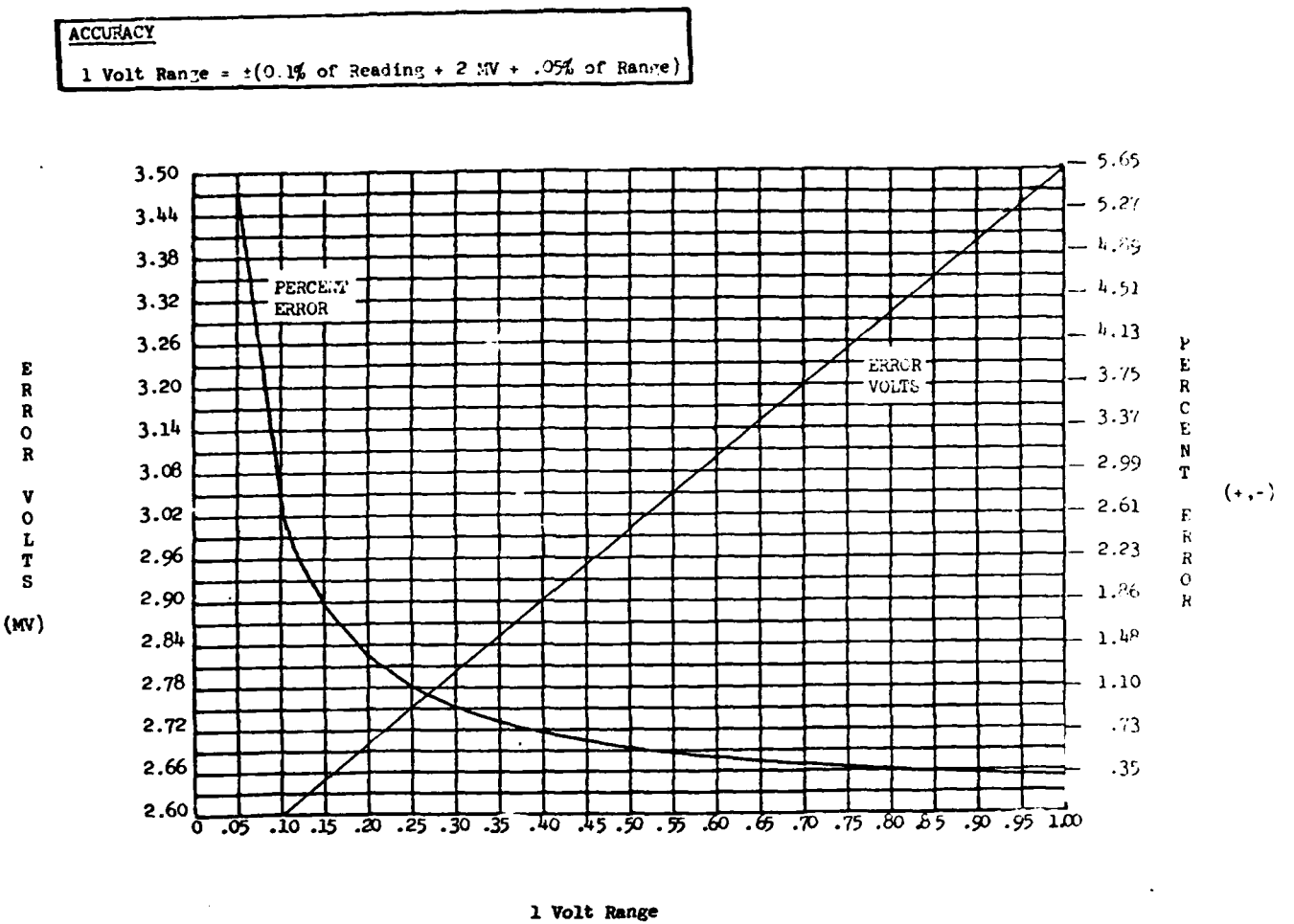


Figure 3.16. S-3263 Test System Differential Voltage Accuracy

ACCURACY

10 Volt Range = ±(0.1% of Reading + 20 MV + .05% of Range)

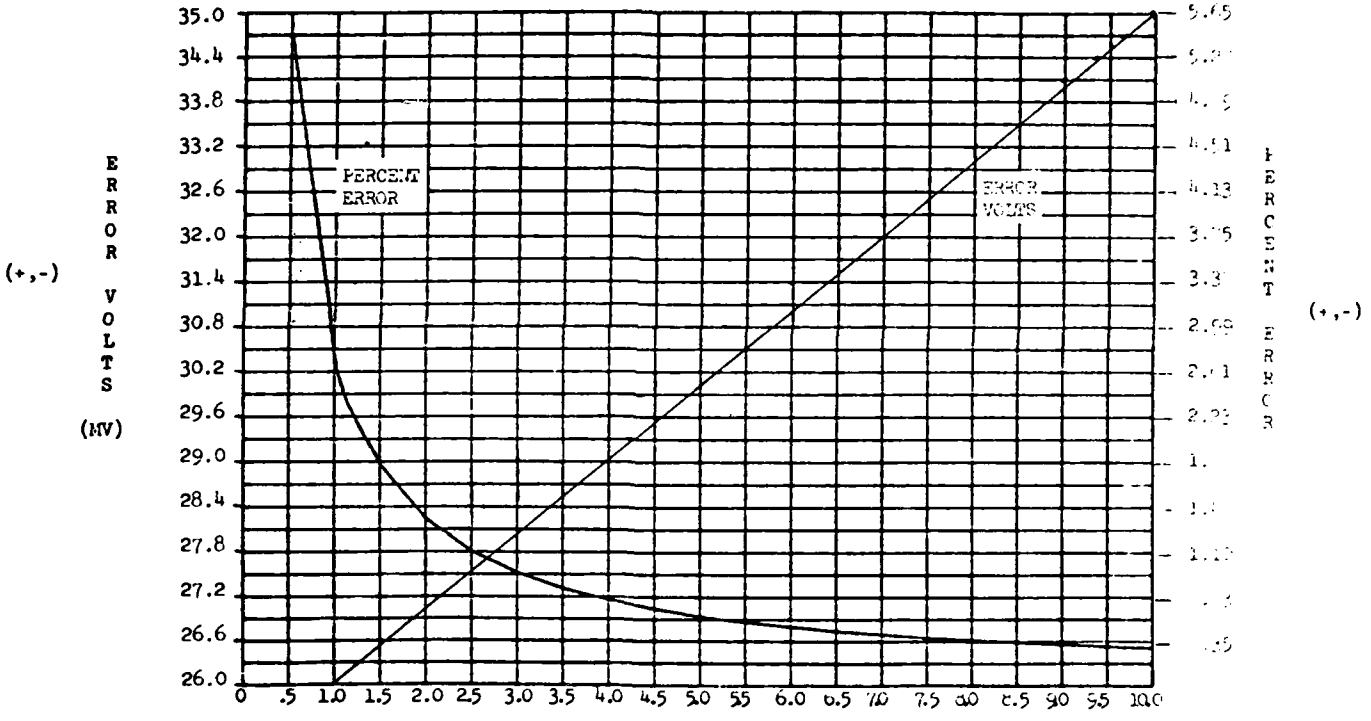


Figure 3.17. S-3263 Test System Differential Voltage Accuracy

ACCURACY

100 V Range = ±(0.3% of Reading + 200 MV + .05% of Range)

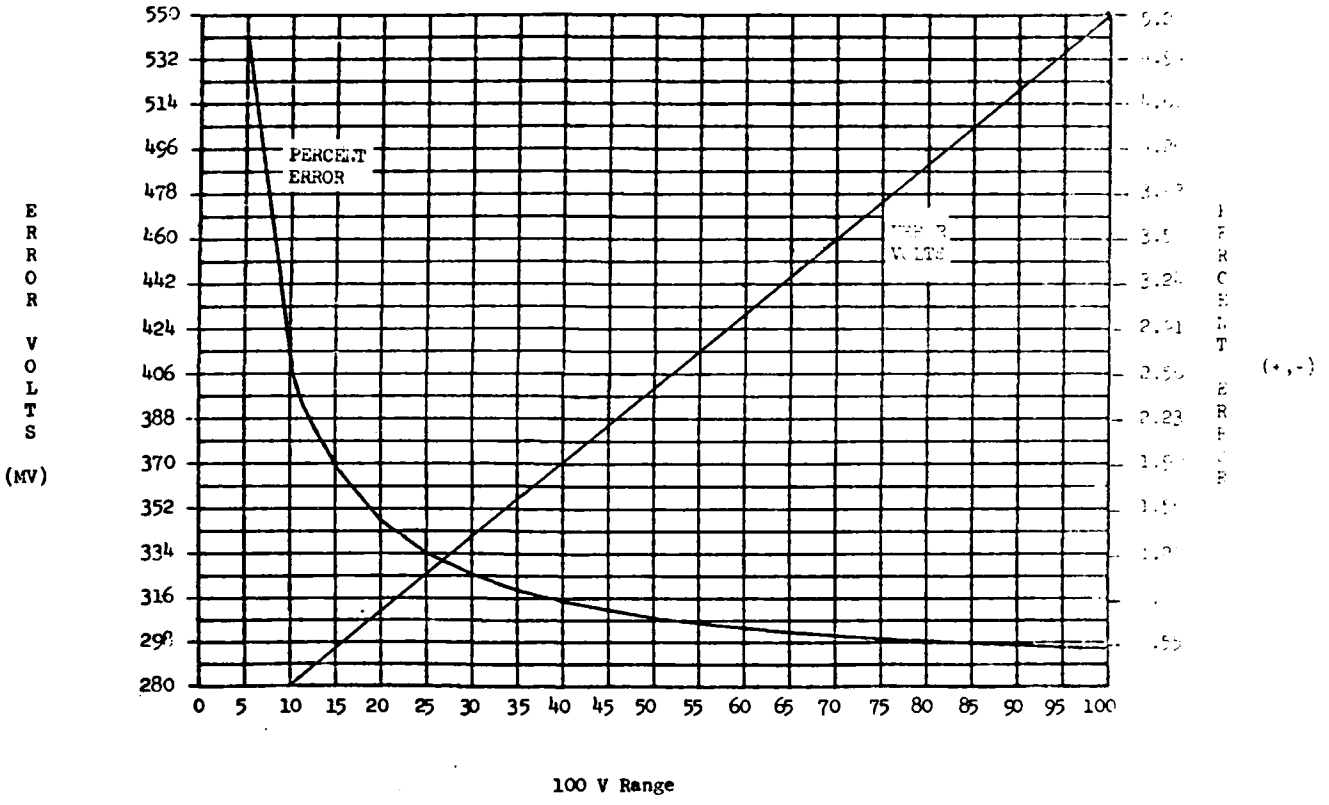
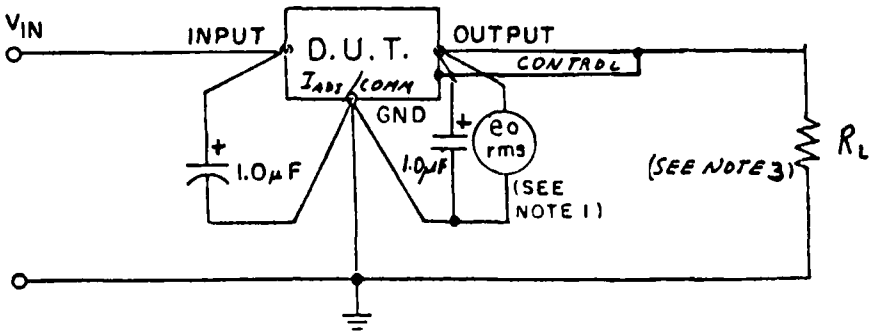


Figure 3.18. S-3263 Test System Differential Voltage Accuracy



Device Table

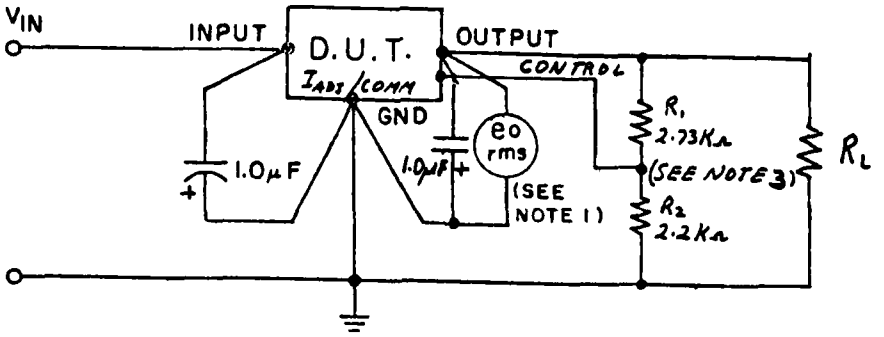
Device Type	01 78 MG	02 78 G	03 LM117H	04 LM117K
V_{IN}	10 V	10 V	6.25 V	6.25 V
R_L	100Ω	50Ω	25Ω	12.5Ω

R_L shall be type REF 70 or equivalent.

Notes:

1. The meter for measuring e_{orms} shall have a minimum bandwidth from 10 Hz to 10 kHz and shall measure true rms voltages.
2. $N_o = e_o$ rms.
3. The control pin connection is required for device types 01 and 02 only.

Figure 3.19. Noise test circuit for positive voltage regulators.



Device Table

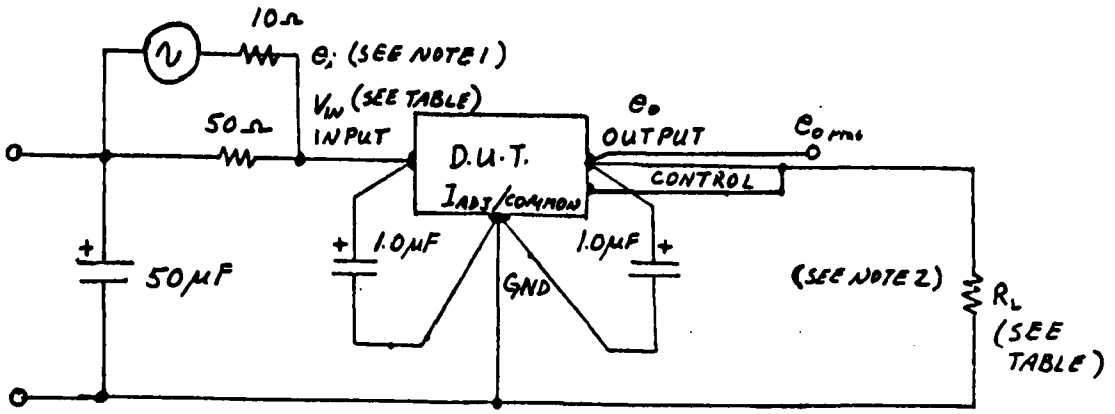
Device Type	01 79 MG	02 79 G	03 LM137H	04 LM137G
V_{IN}	-10 V	-10 V	-6.25V	-6.25 V
R_L	100Ω	50Ω	25Ω	12.5Ω

R_L shall be type RER 70 or equivalent.

Notes:

1. The meter for measuring e_{orms} shall have a minimum bandwidth from 10 Hz to 10 kHz and shall measure true rms voltages.
2. $N_o = e_o$ rms.
3. The control pin connections and resistors (R_1 and R_2) are required for device types 01 and 02 only.

Figure 3.20. Noise test circuit for negative voltage regulators.



Device Table

Device Type	01 78 MG	02 78 G	03 LM117H	04 LM117K
V_{IN}	10 V	10 V	6.25 V	6.25 V
R_L	40.2Ω	14.3Ω	10Ω	2.5Ω

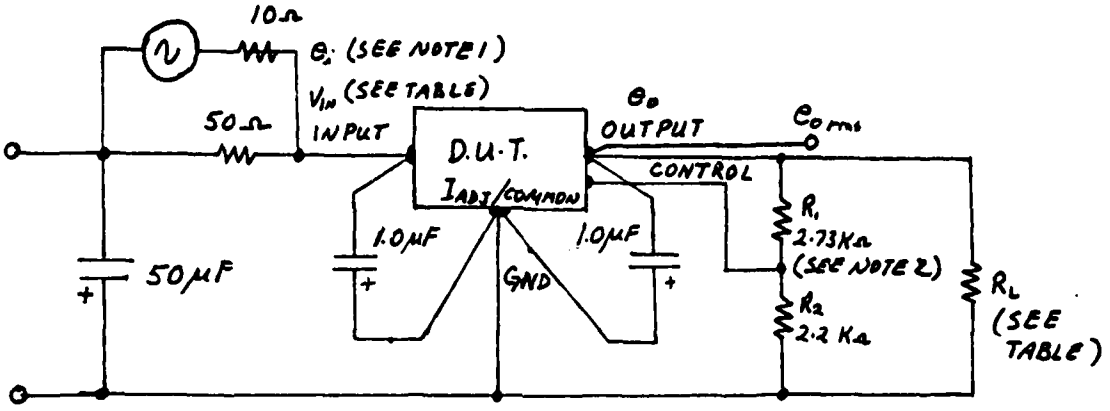
The input 50Ω resistor and R_L shall be type RER 70 or equivalent.

Notes:

1. e_i = 1 V_{rms} @ f = 2400 Hz (measured at the input terminals of the DUT)
   ripple rejection = $2 - \log \frac{e_i\,rms}{e_o\,rms}$

2. The control pin connection is required for device types 01 and 02 only.

Figure 3.21. Ripple rejection test circuit for positive voltage regulators.



Device Table

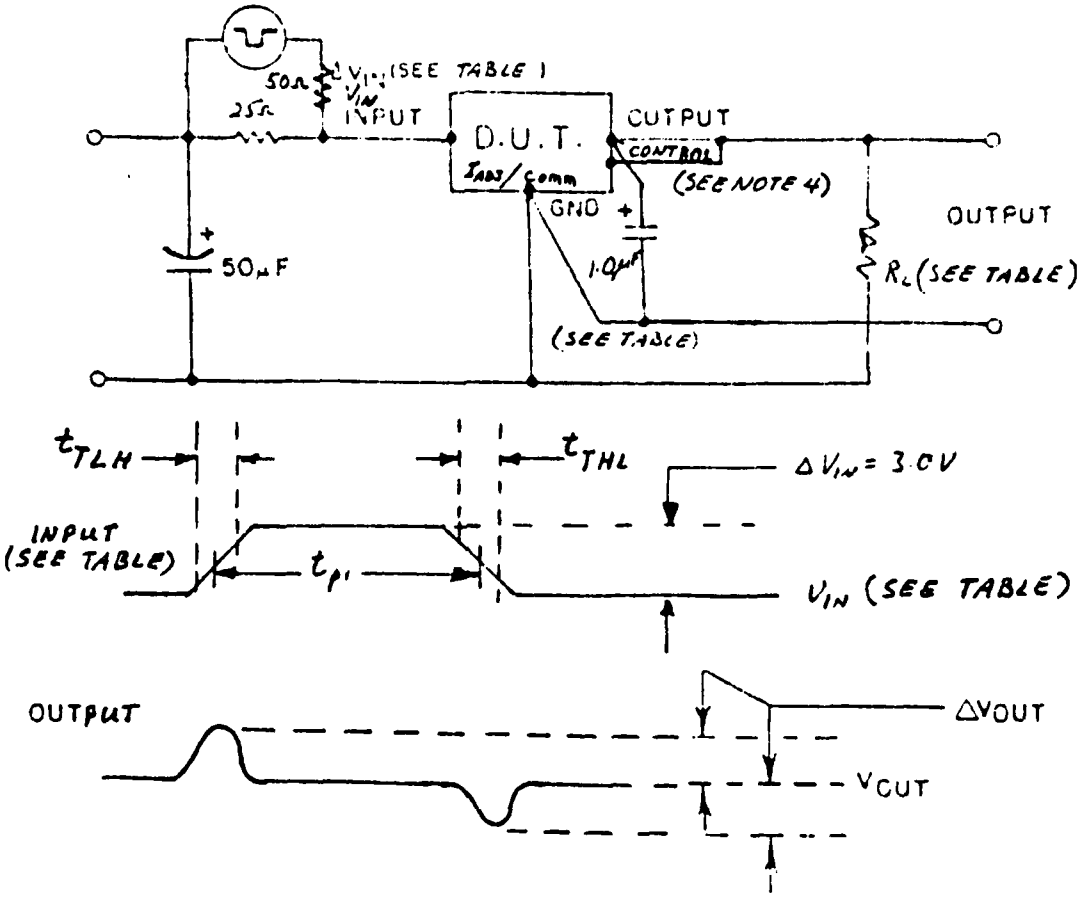
Device Type	01 79 MG	02 79 G	03 LM137H	04 LM137K
V_{IN}	-10 V	-10 V	-6.25 V	-6.25 V
R_L	40.2Ω	14.3Ω	10Ω	2.5Ω

The input 50Ω resistor and R_L shall be type RER 70 or equivalent.

Notes:

1. e_i = 1 V_{rms} @ f = 2400 Hz (measured at the input terminals of the DUT)
   ripple rejection = 20 log $\frac{e_{irms}}{e_{orms}}$
2. The control pin connection and resistors (R_1 and R_2) are required for device types 01 and 02 only.

Figure 3.22. Ripple rejection test circuit for negative voltage regulators.



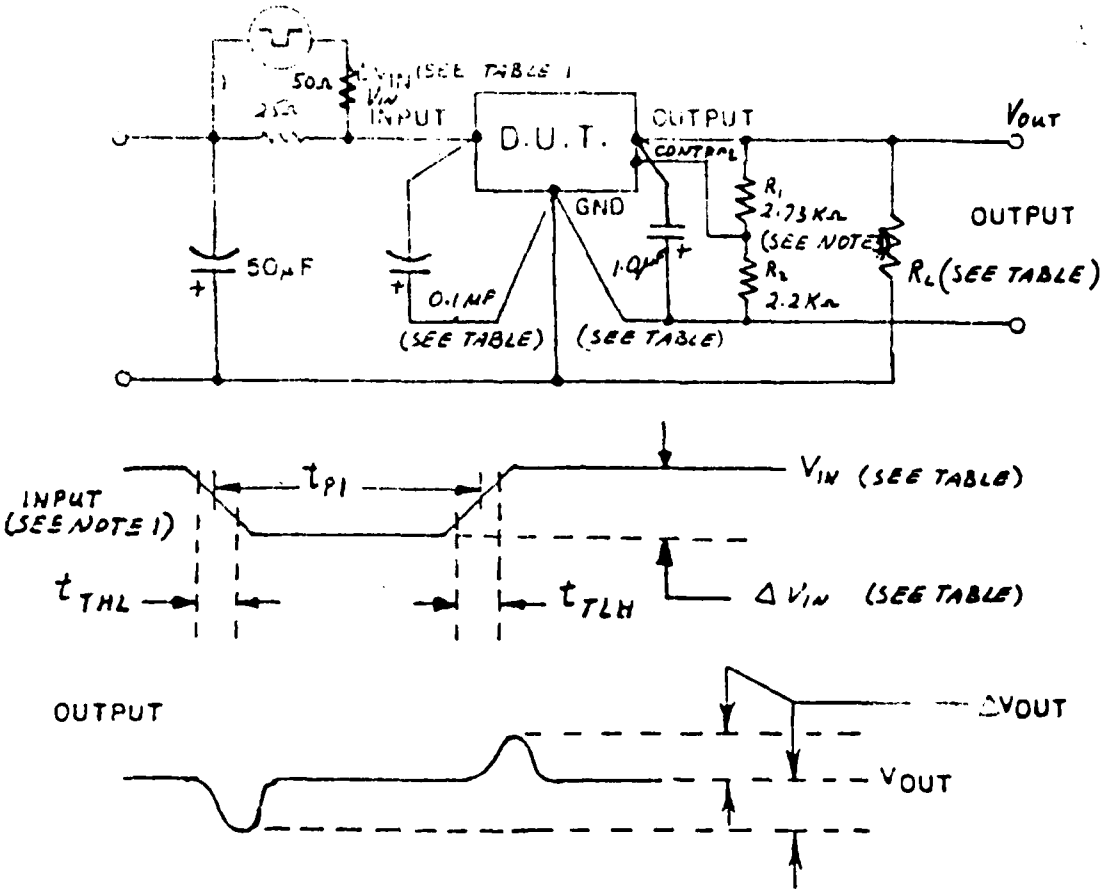
Device Table

Device Type	01 78 MG	02 78 G	03 LM117H	04 LM117G	NOTES
V_{IN}	10 V	10 V	6.25V	6.25V	1
V_{IN}	3.0 V	3.0 V	3.0 V	3.0 V	1
R_L	1.25KΩ	1.25KΩ	120Ω	120Ω	
$t_{PHL} = t_{PLH}$	5.0us	5.0us	5.0us	5.0us	1

Notes:

1. Measured at device input.
2. Pulse width t_{pl} = 25 us; duty cycle = 3. (maximum)
3. Oscilloscope bandwidth = 5 MHz to 15 MHz.
4. The control pin connection is required for device types 01 and 02.

Figure 3.23. Line transient response test circuit for positive voltage regulators.



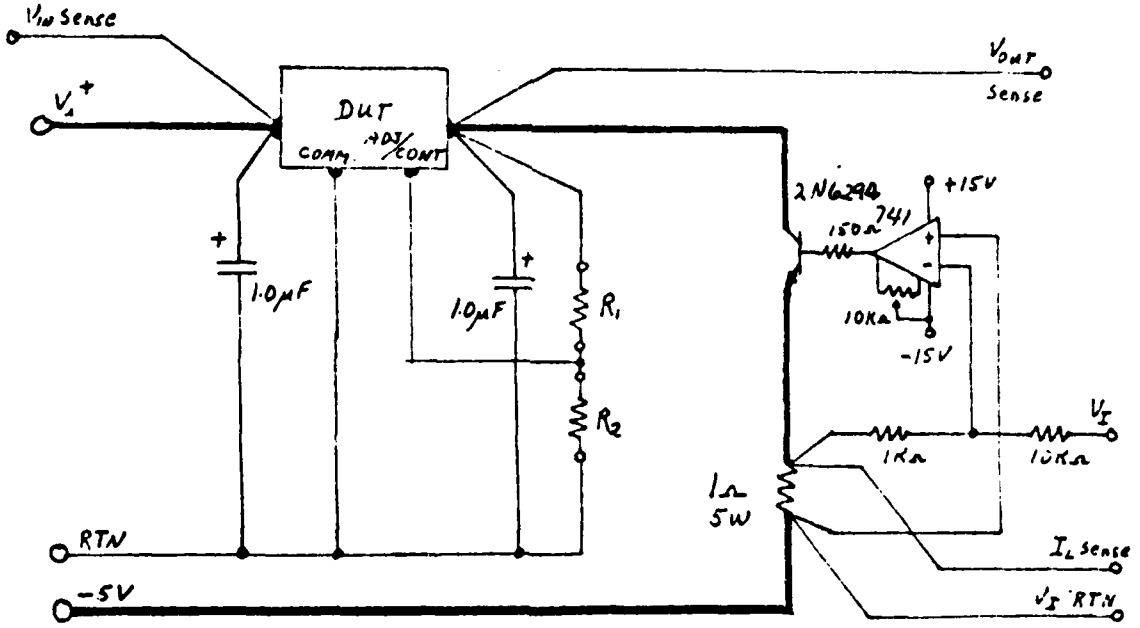
Device Table

Device Type	01 79MG	02 79G	03 LM137H	04 LM137K	NOTES
V_{IN}	-10V	-10V	-6.25V	-6.25V	1
V_{IN}	- 3V	- 3V	- 1V	1V	1
R_L	1.25KΩ	1.25KΩ	120Ω	120Ω	
$t_{THL}=t_{TLH}$	5.0us	5.0us	5.0us	5.0us	1

Notes:

1. Measured at device input.
2. Pulse width t_{p1} = 25 us; duty cycle = 3 % (maximum)
3. Oscilloscope bandwidth = 5 MHz to 15 MHz.
4. The control pin connection and resistors (R_1 and R_2) are required for device types 01 and 02.

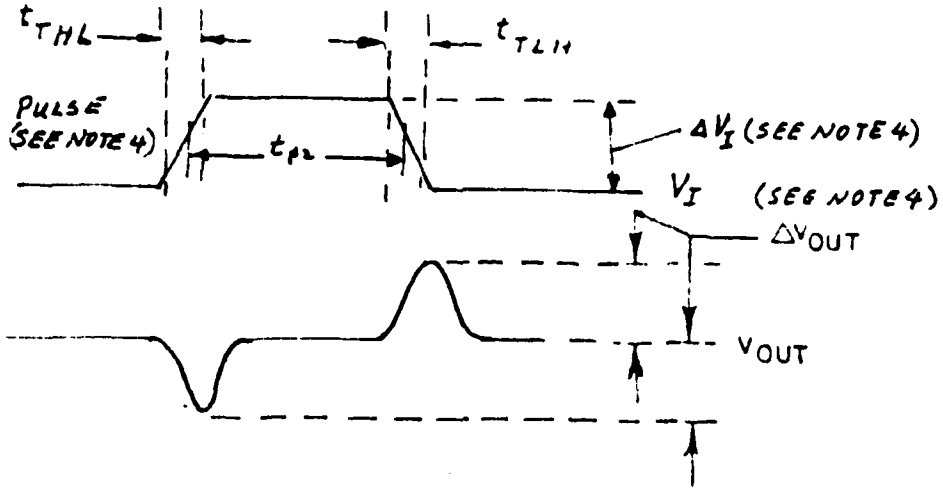
igure 3.24. Line transient response test circuit for negative voltage regulators.



Device Table

Device	01	02	03	04
Type	78MG	78G	LM117H	LM117G
R_1	0	0	249 Ω	249 Ω
R_2	5.0KΩ	5.0KΩ	0	0
I_L	-50mA	-100mA	-50mA	-100mA
I_L	-200mA	-400mA	-200mA	400mA
V_I	-0.49V	-0.99V	-0.45V	-0.95V
V_I	-2.0V	-4.0V	-2.0V	-4.0V

Figure 3.25. Load transient response test circuit for positive voltage regulators.



Notes:

1. Heavy current paths (I_L > 1.0A) are indicated by bold lines.

2. Kelvin connections must be used for all output current and voltage measurements.

3. Op amp stabilization networks may vary with test adapter construction. Alternate drive circuits for the 2N6294 may be used to develop the proper load current and input voltage pulses.

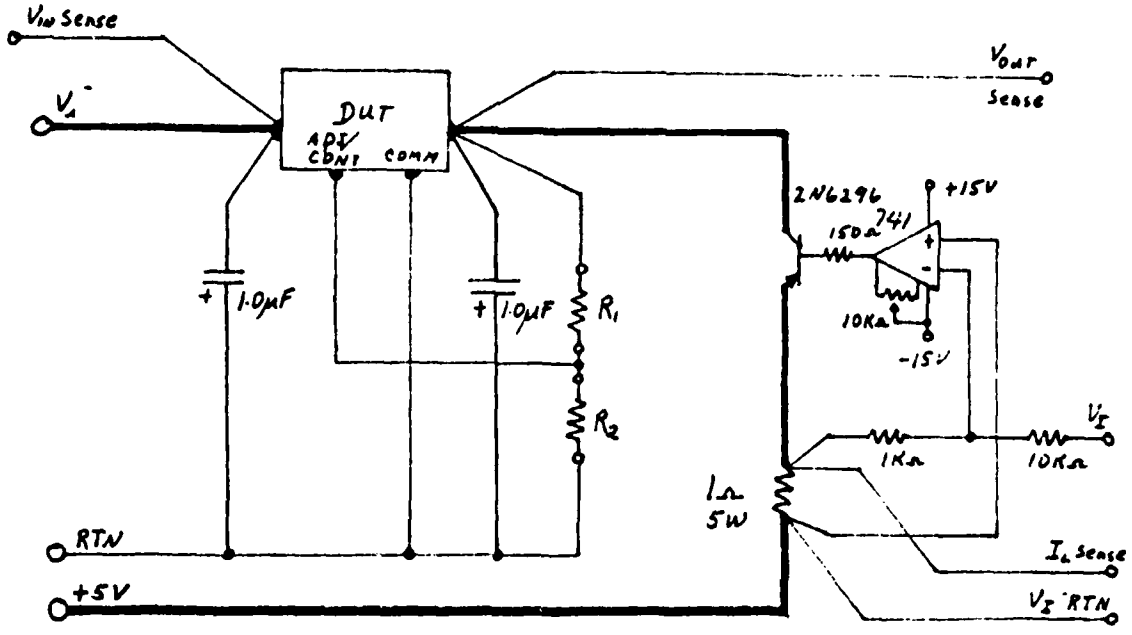
4. The pulse generator for the pulse load circuit shall have the following characteristics. (see device Table III)

   a. Voltage level (V_1) = - 10 (I_L - Vo/(R_1 + R_2) volts
   b. Pulse width (t_{p2}) = 25 u sec.
   c. Duty cycle = 3% (maximum)
   d. t_{THL} = t_{TLH} = 1.0 usec for device types 01 and 02
   e. t_{THL} = t_{TLH} = 5.0 usec for device types 03 and 04
   f. Difference voltage level (ΔV_1) = 10 (I_L) volts

5. a. ΔV_{out} = 500 mV maximum for device type 01
   b. ΔV_{out} = 1000 mV maximum for device type 02
   c. ΔV_{out} = 120 mV maximum for devices type 03 and 04
   (These values guarantee the specified limits for load transient response.)

6. Oscilloscope minimum bandwidth shall be 9 MHz to 15 MHz.

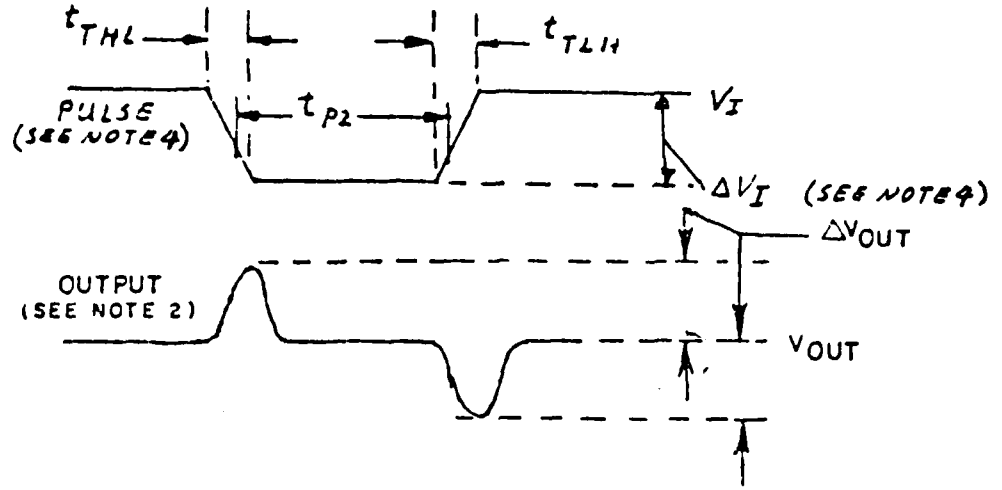
Figure 3.2-1. Load transient response test circuit for positive voltage regulators (cont'd.).



Device Table

Device Type	01 79MG	02 79[illegible]	03 LM137H	04 LM137K
R_1	2.21KΩ	2.21KΩ	249Ω	249Ω
R_2	2.74KΩ	2.74KΩ	0	0
I_L	50mA	100mA	50mA	100mA
I_L	200mA	400mA	200mA	400mA
V_I	0.49V	0.99V	0.45V	0.95V
V_I	2.0V	4.0V	2.0V	4.0V

Figure 3.26 Load transient response test circuit for negative voltage regulators.



Notes:

1. Heavy current path ($I \geq 1.0A$) are indicated by bold lines.

2. Kelvin connections must be used for all output current and voltage measurements.

3. Op amp stabilization networks may vary with test adapter construction. Alternate drive circuits for the 2N6296 may be used to develop the proper load current and input voltage pulses.

4. The pulse generator for the pulse load circuit shall have the following characteristics. (see device table)

   a. Voltage level (V_1) = 10 (I_L - Vo/(R_1 + R_2) volts
   b. Pulse width (t_{p2}) = 25 u sec
   c. Duty cycle = 3% (maximum)
   d. $t_{THL} = t_{TLH}$ = 1.0 u sec for device types 01 and 02
   e. $t_{THL} = t_{TLH}$ = 5.0 u sec for device types 03 and 04
   f. Difference voltage level (ΔV_I) = 10 (I_L) volts

5. a. ΔV_{out} = 500 mV maximum for device type 01
   b. ΔV_{out} = 1000 mV maximum for device type 02
   c. ΔV_{out} = 60 mV maximum for devices type 03 and 04
   (These values guarantee the specified limits for load transient response.)

6. Oscilloscope minimum bandwidth shall be 9 MHz to 15 MHz.

Figure 3.2b. Load transient response test circuit for negative voltage regulators (cont'd).

LM117H Load Regulation

V = 5 mV/cm
H = .2 ms/cm

Unit #4

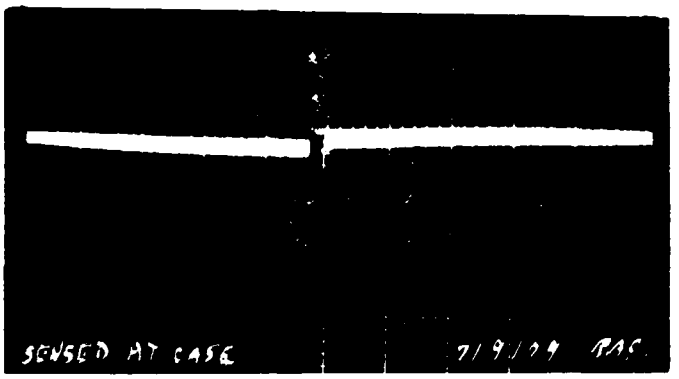


Figure 3.27. Oscillograph of LM117H load regulation measured at the case.

LM117K Load Regulation

V = 5 mV/cm
H = .2 ms/cm

Unit #4

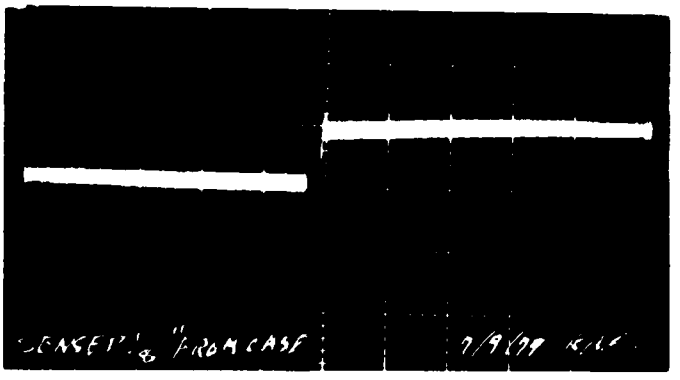
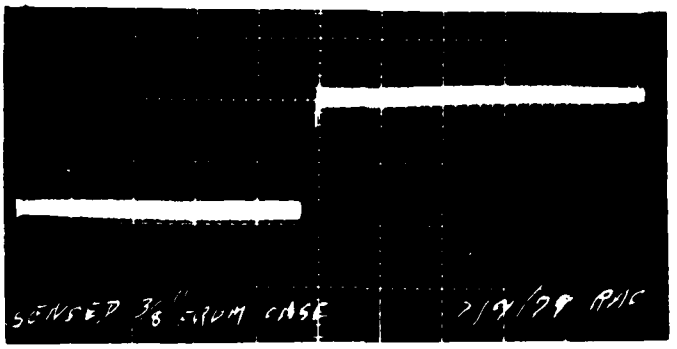


Figure 3.28. Oscillograph of LM117K load regulation measured at the case.

[illegible] Load Regulation

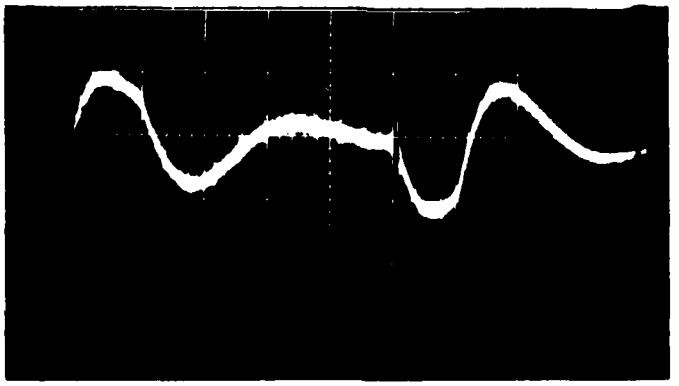
[illegible] mV/cm Unit #4
[illegible] 2 ms/cm



[illegible] Photograph of LM117H load regulation measured 3/8" below [illegible]

LM117H Line Transient Response

V/cm = 5 mV Unit #2
Time/cm = 5 us



[illegible] Photograph of LM117H line transient response test.

LM117 Load Transient Response

V/cm = .02 Unit = 20
Time/cm = 5 us

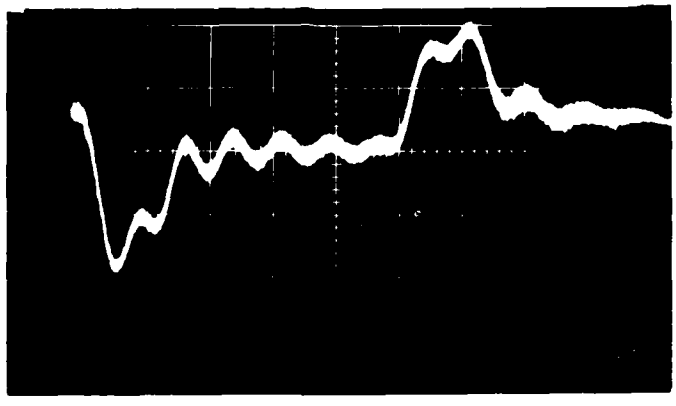


Figure 3.31. Oscillograph of LM117 load transient response test.

LM117K Line Transient Response

V/cm = 5 mV Unit = 2
Time/cm = 5 us

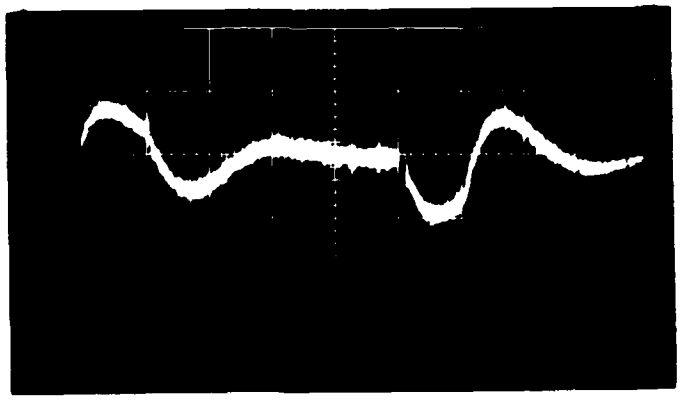
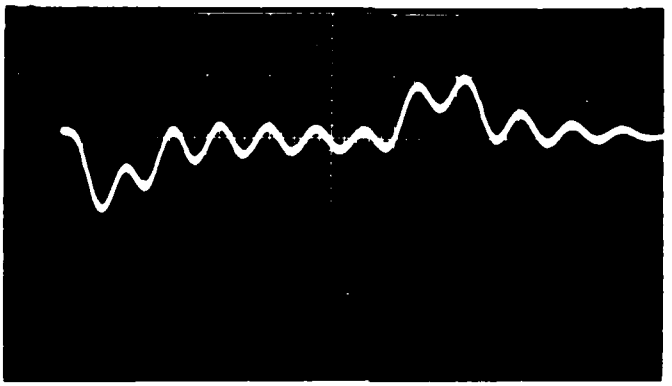


Figure 3.32. Oscillograph of LM117 line transient response test.

[illegible] Transient Response

[illegible] Unit #1
[illegible] us



[illegible] 3.33. Oscilloscope [illegible] load transient response test.

LM137H Line Transient Response

V/cm = .020 Unit #1
Time/cm = 5 us

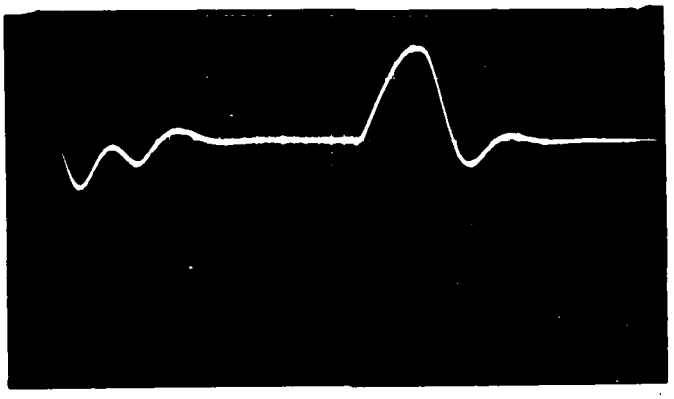


Figure 3.34. Oscilloscope of LM137H line transient response test.

LM137H Load Transient Response

V/cm = .01
Time/cm = [illegible] us

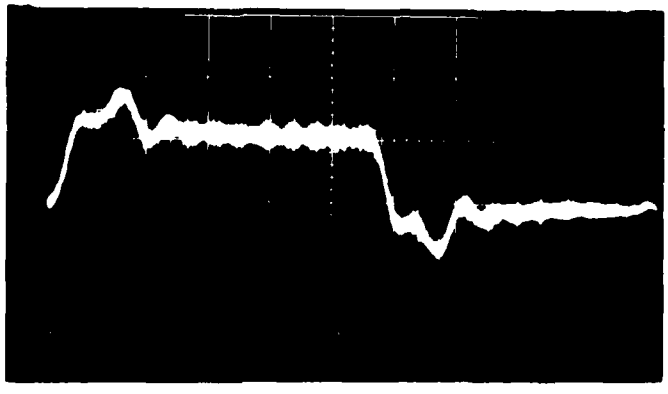


Figure 3.35. Oscillograph of LM137H load transient response test.

LM137K Line Transient Response

V/cm = .020
Time/cm = 5 us

Unit #1

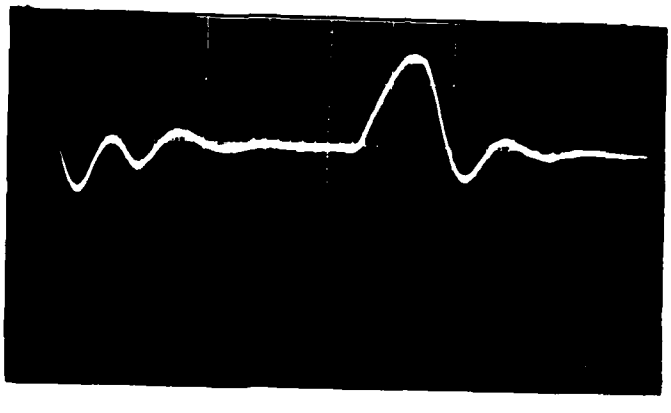


Figure 3.36. Oscillograph of LM137K line transient response test.

LM137K Load Transient Response

V/cm = .02 Unit #1
Time/cm = 5 us

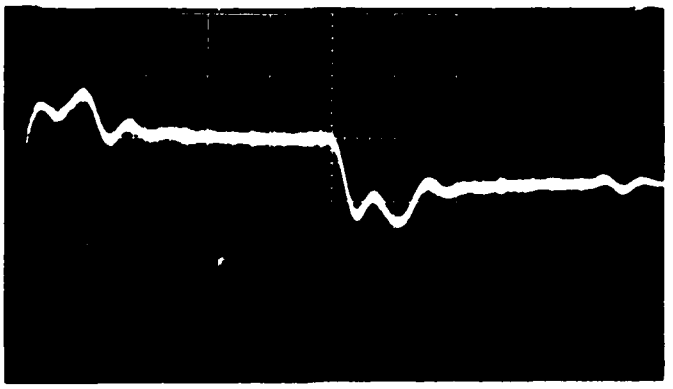


Figure 3.3 Oscillograph for LM137K load transient response test.

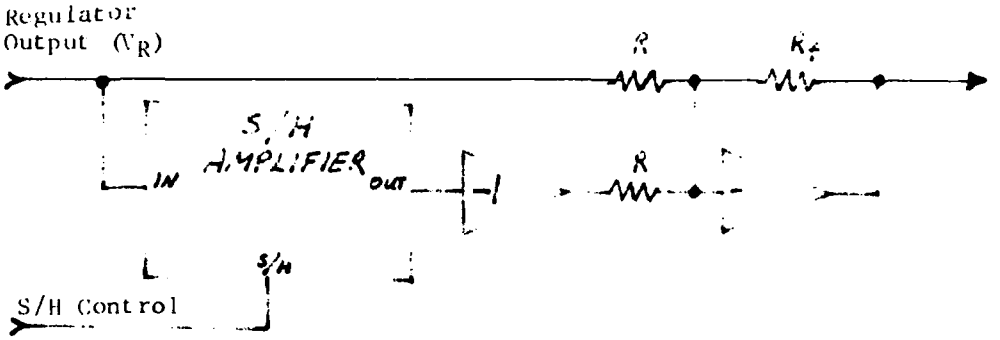


Figure 3.38. Alternate test circuit for V_{RLINE}, V_{RLINE}, V_{RLOAD} & V_{RTH} tests

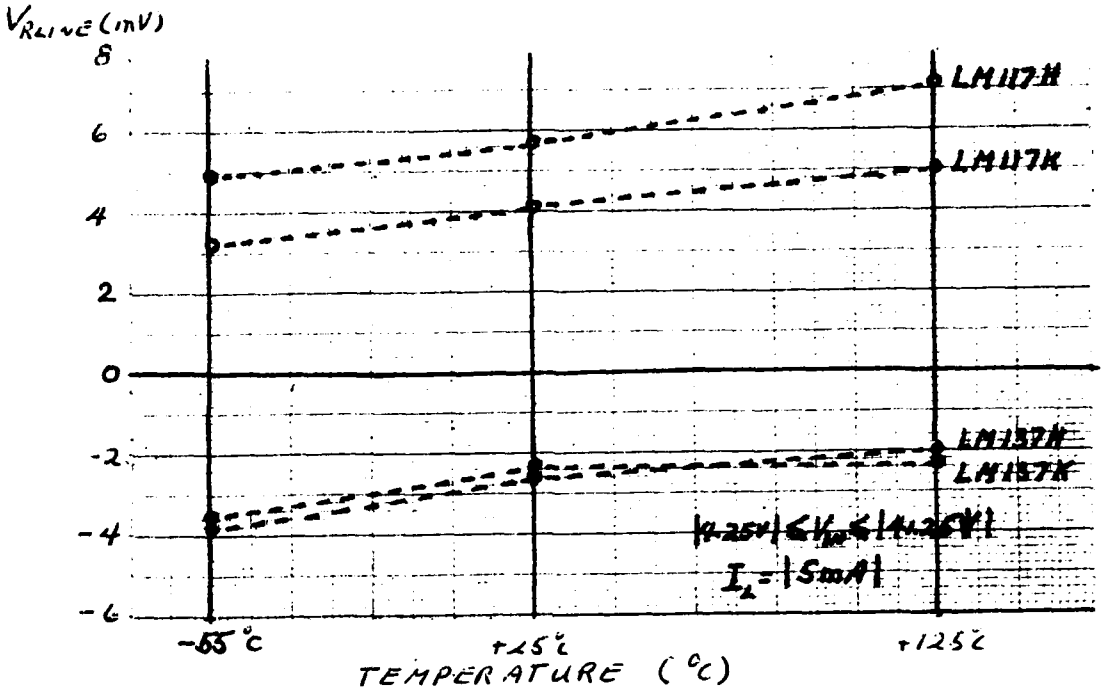


Figure 3.39. Average Line Regulation versus Temperature.

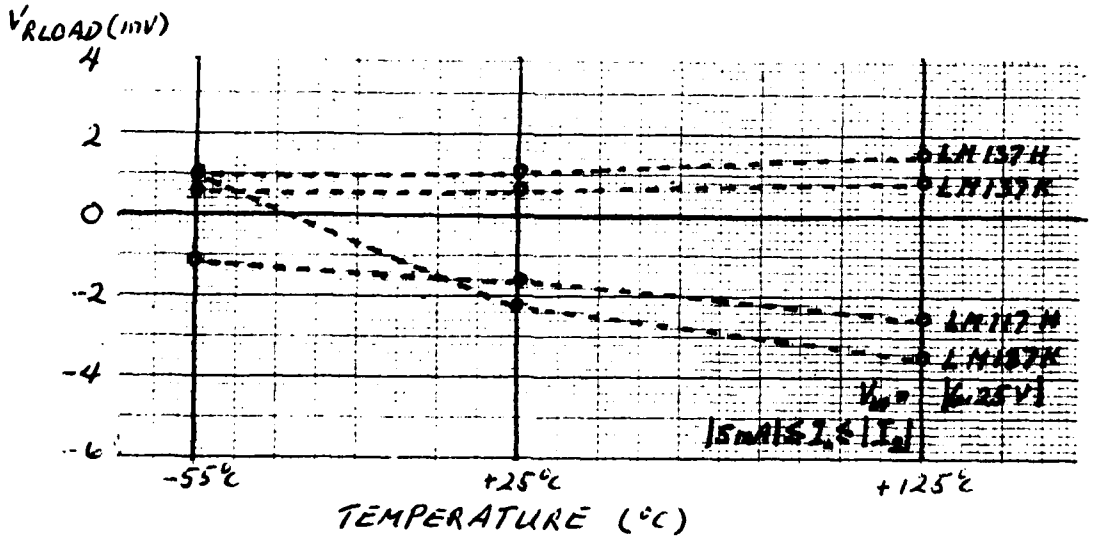


Figure 3.40. Average Load Regulation (#2) versus Temperature.

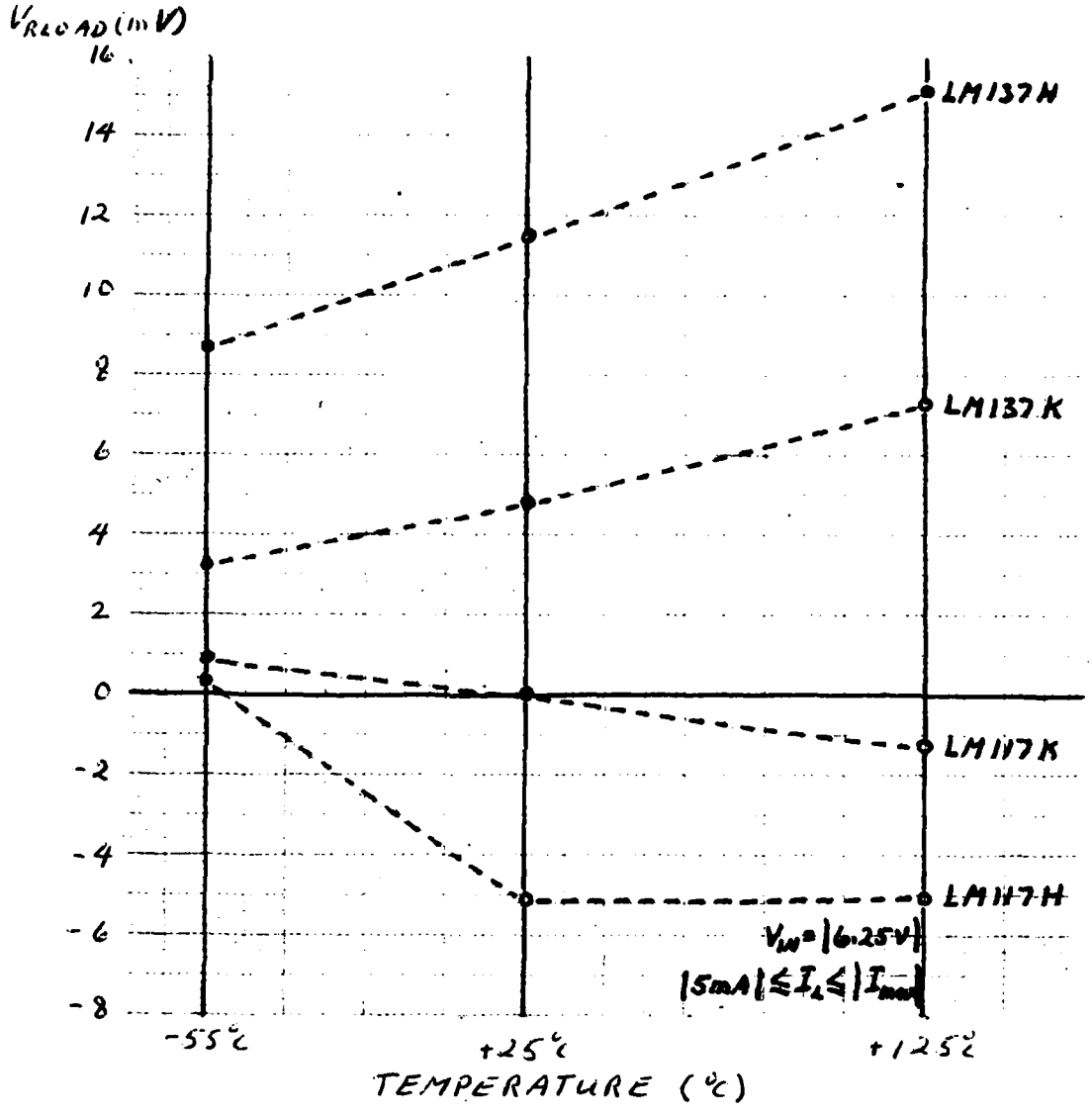


Figure 3.41. Average Load Regulation (#1) versus Temperature.

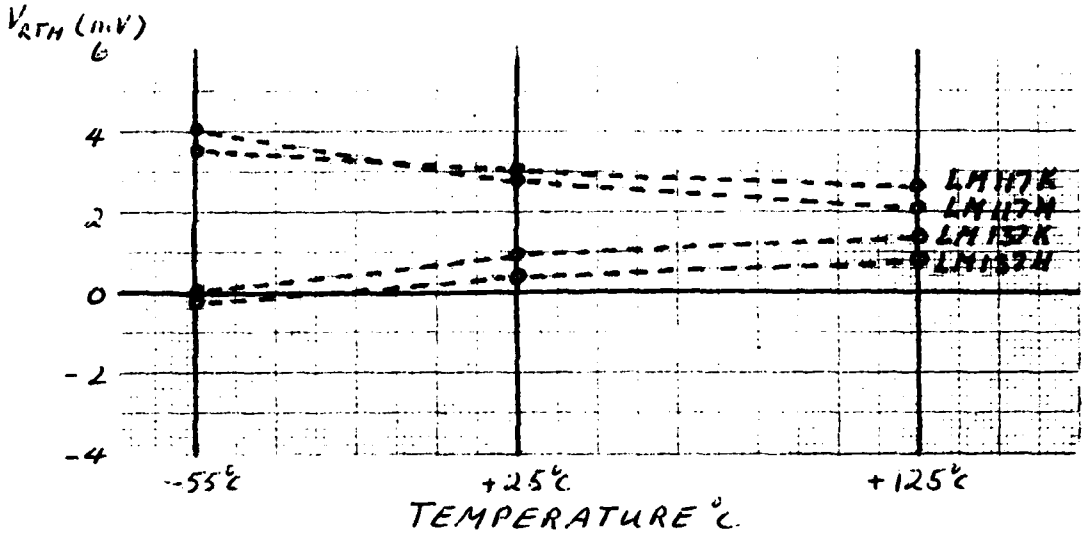


Figure 3.42. Average Thermal Regulation versus Temperature.

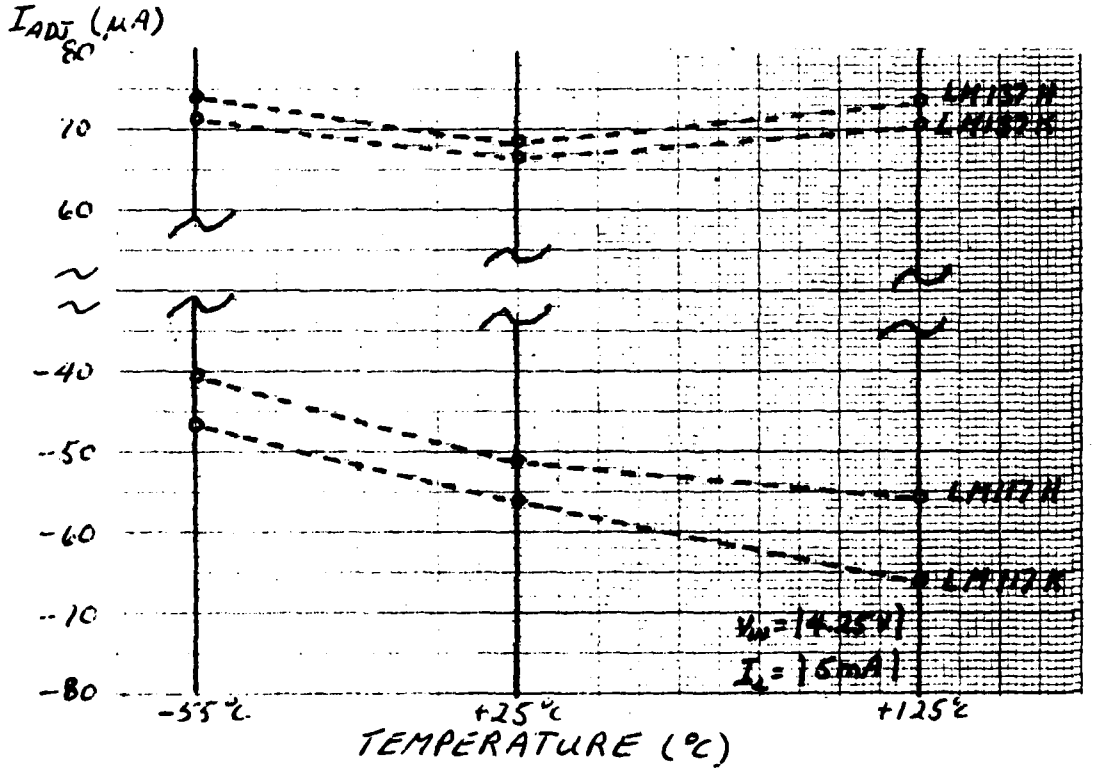


Figure 3.43. Average Adjustment Pin Current versus Temperature.

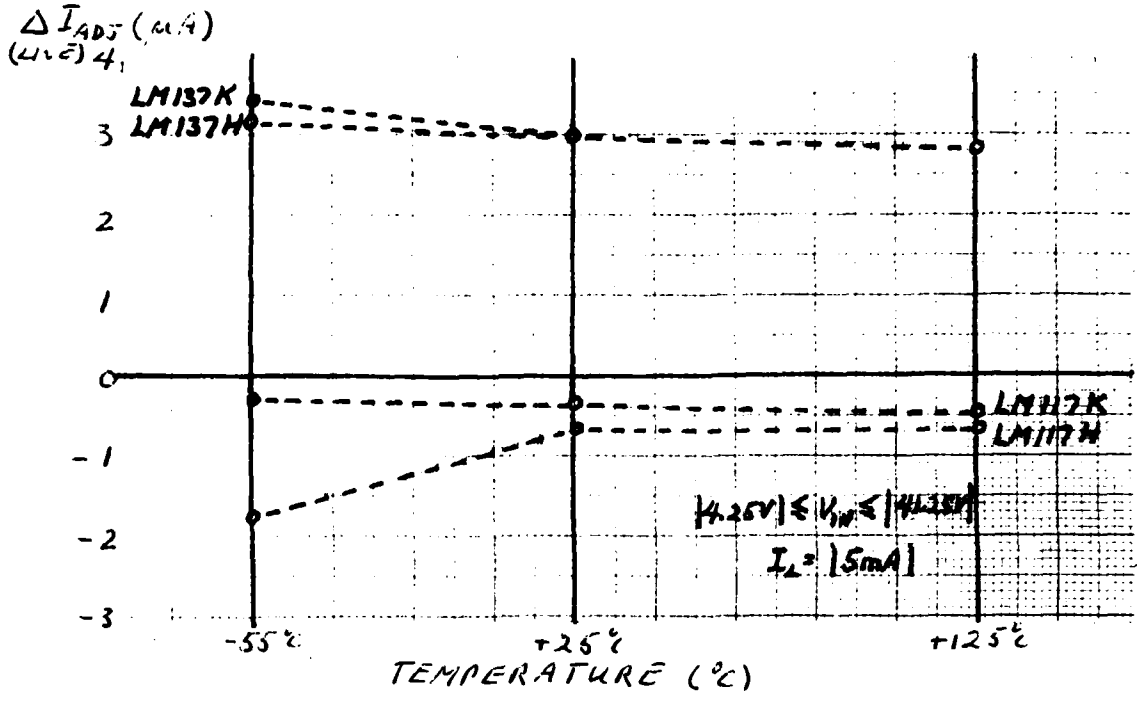


Figure 3.44. Average Change of I_{ADJ} with Line Voltage versus Temperature.

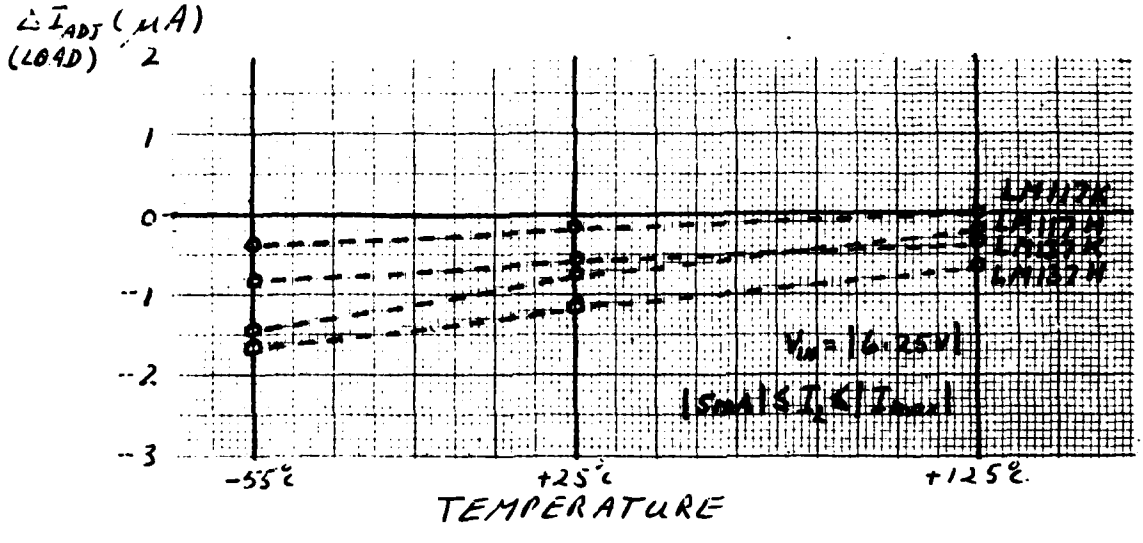


Figure 3.45. Average Change of I_{ADJ} with Load Current versus Temperature.

Symbol	Test Conditions		Applied Test Voltages (volts) [pins Hi-Lo]					Relays Energized	Measurement Sense Lines			Equation	Units
	V_{IN} (volts)	I_{OUT} (mA)	pins 1-2	pins 4-5	pins 6-11	pins 7-2	pins 8-2		pins Hi-Lo	Value	Units		
V_{OUT1}	8	-5	8	-.04	–	–	–	None	9-11	E_1	V	$V_{OUT1} = E_1$	V
V_{OUT2}	8	-500	8	-4.99	–	–	–			E_2		$V_{OUT2} = E_2$	
V_{OUT3}	20	-5	20	-.04	–	–	–			E_3		$V_{OUT3} = E_3$	
V_{OUT4}	20	-500	20	-4.99	–	–	–			E_4		$V_{OUT4} = E_4$	
V_{OUT5}	30	-5	30	-.04	–	–	–			E_5		$V_{OUT5} = E_5$	
V_{OUT6}	30	-50	30	-.49	–	–	–			E_6		$V_{OUT6} = E_6$	
V_{RLINE1}	8	-50	8	-.49	–	–	–			E_7		$V_{RLINE1} = E_7 - E_6$	mV
V_{RLINE2}	8	-350	8	-3.49	–	–	–			E_8			
V_{RLINE2}	25	-350	25	-3.49	–	–	–			E_9		$V_{RLINE2} = E_8 - E_9$	
V_{RLOAD1}	10	-5	10	-.04	–	–	–			E_{10}			
V_{RLOAD1}	10	-500	10	-4.99	–	–	–			E_{11}		$V_{RLOAD1} = E_{10} - E_{11}$	
V_{RLOAD2}	–	–	–	–	–	–	–			–		$V_{RLOAD2} = E_5 - E_6$	
V_{RTH}	15	-500	15	-4.99	–	–	–			E_{12}		$V_{RTH} = E_{12}$	
I_{SCD1}	10	-5	10	-.04	–	–	–		12-13	E_{13}		$I_{SCD1} = E_{13}/2000$	mA
I_{SCD2}	30	-5	30	-.04	–	–	–			E_{14}		$I_{SCD2} = E_{14}/2000$	
ΔI_{SCD} (LINE)	8	-5	8	-.04	–	–	–			E_{15}		$\Delta I_{SCD(LINE)} = \frac{E_{15} - E_{14}}{2000}$	
ΔI_{SCD} (LOAD)	10	-500	10	-4.99	–	–	–			E_{16}		$\Delta I_{SCD(LOAD)} = \frac{E_{13} - E_{16}}{2000}$	
I_{OS1}	10	–	15	–	–	1.0	0	K4, K5	10-5	E_{17}		$I_{OS1} = E_{17}$	A
V_{OUT} (RECOV)	10	–	15	–	–	1.0	0	K4, K5	9-11	E_{18}		$V_{OUT} = E_{18}$	V
I_{OS2}	25	–	30	–	–	2.5	0		10-5	E_{19}		$I_{OS2} = E_{19}$	A
V_{OUT} (RECOV)	25	–	30	–	–	2.5	0		9-11	E_{20}		$V_{OUT} = E_{20}$	V
I_{OS3}	30	–	40	–	–	3.5	0		10-5	E_{21}		$I_{OS3} = E_{21}$	A
V_{OUT} (RECOV)	30	–	40	–	–	3.5	0		9-11	E_{22}		$V_{OUT} = E_{22}$	V
I_{pk}	8	–	15	–	–	0.8		K4, K5	10-5	E_{23}		$I_{pk} = E_{23}$	A
V_{OUT} (RECOV)	8	–	15	–	–	0.8		K4, K5	9-11	E_{24}		$V_{OUT} = E_{24}$	V
I_{CONT}	10	-350	10	-3.49	–	–	–	K1, K2	12-13	E_{25}		$I_{CONT} = E_{25}/33200$	MA
V_{START}	8	-500	15	–	–	0.8	–	K4	9-11	E_{26}		$V_{OUT} = E_{26}$	V

Table 3.4. Test conditions for 3-terminal adjustable positive voltage regulator (78C).

Symbol	Test Conditions		Applied Test Voltages (Volts) [Pins Hi-Lo]					Relays Energized	Measurement Sense Lines			Equation	Limits
	V_{IN} (Volts)	I_L (mA)	pins 1-2	pins 4-5	pins 6-11	pins 7-2	pins 8-2		pins Hi-Lo	Value	units		
V_{OUT1}	8	-5	8	-.04	–	–	–	None	9-11	E_1	V	$V_{OUT1} = E_1$	
V_{OUT2}	8	-1000	8	-9.99	–	–	–			E_2		$V_{OUT2} = E_2$	
V_{OUT3}	20	-5	20	-.04	–	–	–			E_3		$V_{OUT3} = E_3$	
V_{OUT4}	20	-1000	20	-9.99	–	–	–			E_4		$V_{OUT4} = E_4$	
V_{OUT5}	30	-5	30	-.04	–	–	–			E_5		$V_{OUT5} = E_5$	
V_{OUT6}	30	-100	30	-.99	–	–	–			E_6		$V_{OUT6} = E_6$	
V_{RLINE1}	8	-100	8	-.99	–	–	–			E_7		$V_{RLINE1} = E_7 - E_6$	
V_{RLINE2}	8	-500	8	-4.99	–	–	–			E_8			
V_{RLINE2}	25	-500	25	-4.99	–	–	–			E_9		$V_{RLINE2} = E_8 - E_9$	
V_{RLOAD1}	10	-5	10	-.04	–	–	–			E_{10}			
V_{RLOAD}	10	-1000	10	-9.99	–	–	–			E_{11}		$V_{RLOAD1} = E_{10} - E_{11}$	
V_{RLOAD2}	–	–	–	–	–	–	–			–		$V_{RLOAD2} = E_5 - E_6$	
V_{RTH}	15	-1000	15	-9.99	–	–	–			E_{12}		$V_{RTH} = E_{12}$	
I_{SCD1}	10	-5	10	-.04	–	–	–		12-13	E_{13}		$I_{SCD1} = E_{13}/2000$	mA
I_{SCD2}	30	-5	30	-.04	–	–	–			E_{14}		$I_{SCD2} = E_{14}/2000$	
ΔI_{SCD} (LINE)	8	-5	8	-.04	–	–	–			E_{15}		ΔI_{SCD} (LINE) $= \frac{E_{15} - E_{\cdot}}{2000}$	
ΔI_{SCD} (LOAD)	10	-1000	10	-9.99	–	–	–			E_{16}		ΔI_{SCD} (LOAD) $= \frac{E_{13} - E_{16}}{2000}$	
I_{OS1}	10	–	15	–	–	1.0	0	K4, K5	10-5	E_{17}		$I_{OS1} = E_{17}$	
V_{OUT} (RECOV	10	–	15	–	–	1.0	0		9-11	E_{18}		$V_{OUT} = E_{18}$	
I_{OS2}	25	–	30	–	–	2.5	0		10-5	E_{19}		$I_{OS2} = E_{19}$	
V_{OUT} (RECOV	25	–	30	–	–	2.5	0		9-11	E_{20}		$V_{OUT} = E_{20}$	
I_{OS3}	30	–	40	–	–	3.5	0		10-5	E_{21}		$I_{OS3} = E_{21}$	
V_{OUT} (RECOV	30	–	40	–	–	3.5	0		9-11	E_{22}		$V_{OUT} = E_{22}$	
I_{pk}	8	–	15	–	–	0.8			10-5	E_{23}		$I_{pk} = E_{23}$	
V_{OUT} (RECOV)	8	–	15	–	–	0.8			9-11	E_{24}		$V_{OUT} = E_{24}$	
I_{CONT}	10	-500	10	-4.99	–	–	–	K1, K2	12-13	E_{25}		$I_{CONT} = E_{25}/3320$	mA
V_{START}	8	-1000	15	–	–	0.8	–	K4	9-11	E_{26}		$V_{OUT} = E_{26}$	

Table 3.2. Test conditions for 3-terminal adjustable positive voltage regulator (MIL).

Symbol	Test Conditions		Applied Test Voltages (Volts) [pins Hi-Lo]					Relays Energized	Measurement Sense Lines			Equation	
	V_{in} Volts	I_o mA	pins 1-2	pins 4-5	pins 6-11	pins 7-2	pins 8-2		pins Hi-Lo	Value	Units		
V_{OUT1}	4.25	-5	4.25	0	—	—	—	None	9-11	E_1	V	$V_{OUT1} = E_1$	V
V_{OUT2}	4.25	-500	4.25	-4.95	—	—	—			E_2		$V_{OUT2} = E_2$	
V_{OUT3}	41.25	-5	41.25	0	—	—	—			E_3		$V_{OUT3} = E_3$	
V_{OUT4}	41.25	-50	41.25	-0.45	—	—	—			E_4		$V_{OUT4} = E_4$	
V_{RLINE}	—	—	—	—	—	—	—			—		$V_{RLINE} = E_1 - E_3$	mV
V_{RLOAD}	6.25	-5	6.25	0	—	—	—			E_5		—	
V_{RLOAD}	6.25	-500	6.25	-4.95	—	—	—			E_6		$V_{RLOAD_1} = E_5 - E_6$	
V_{RLOAD}	—	—	—	—	—	—	—			—		$V_{RLOAD_2} = E_3 - E_4$	
V_{RTH}	14.6	-750	14.6	-7.45	—	—	—			E_7		$V_{RTH} = \Delta_e E_7$	
I_{ADJ}	4.25	-5	4.25	0	—	—	—	K2	12-13	E_8	mV	$I_{ADJ} = E_8/2000$	MA
I_{ADJ}	41.25	-5	41.25	0	—	—	—			E_9		$I_{ADJ} = E_9/2000$	
ΔI_{ADJ} (LINE)	—	—	—	—	—	—	—			—		$\Delta I_{ADJ}_{LINE} = \frac{E_8 - E_9}{2000}$	
ΔI_{ADJ} (LOAD)	6.25	-5	6.25	0	—	—	—			E_{10}		$\Delta I_{ADJ}_{(LOAD)} = \frac{E_{10} - E_{11}}{2000}$	
ΔI_{ADJ} (LOAD)	6.25	-500	6.25	-4.98	—	—	—			E_{11}			
I_{OS1}	4.25	—	10	—	—	0.425	0	K4, K5	10-5	E_{12}	V	$I_{OS} = E_{12}$	A
V_{OUT} (RECOV)	4.25	—	10	—	—	0.425	0	K4, K5	9-11	E_{13}		$V_{OUT}_{(RECOV)} = E_{13}$	V
I_{OS2}	40	—	40	—	—	—	0	K5	10-5	E_{14}		$I_{OS} = E_{14}$	A
V_{OUT} (RECOV)	40	—	40	—	—	—	0	K5	9-11	E_{15}		$V_{OUT}_{(RECOV)} = E_{15}$	V
I_{pk}	4.25	—	10	—	—	0.425	1.0	K4, K5	10-5	E_{16}		$I_{pk} = E_{16}$	A
V_{OUT} (RECOV)	4.25	—	10	—	—	0.425	1.0	K4, K5	9-11	E_{17}		$V_{OUT}_{(RECOV)} = E_{17}$	V
I_{Q1}	4.25	—	4.25	0	1.4	—	—	K_3	12-13	E_{18}		$I_{Q1} = E_{18}/2000$	mA
I_{Q2}	14.25	—	14.25	0	1.4	—	—			E_{19}		$I_{Q2} = E_{19}/2000$	
I_{Q3}	41.25	—	41.25	0	1.4	—	—			E_{20}		$I_{Q3} = E_{20}/2000$	
V_{START}	4.25	-500	10	0	—	0.425	—	K4	9-11	E_{21}		$V_{START} = E_{21}$	V

Table 3.6. Test conditions for 3-terminal adjustable positive voltage regulator (LM117K).

Symbol	Test Conditions		Applied Test Voltages (Volts) [Pins Hi-Lo]					Relays Energized	Measurement Sense Lines			Equation	Units
	V_{IN} Volts	I_L (mA)	pins 1-2	pins 4-5	pins 6-11	pins 7-2	pins 8-2		pins Hi-Lo	Value	units		
V_{OUT1}	4.25	-5	4.25	0	—	—	—	None	9-11	E_1	V	$V_{OUT1} = E_1$	V
V_{OUT2}	4.25	-1500	4.25	14.95	—	—	—			E_2		$V_{OUT2} = E_2$	
V_{OUT3}	41.25	-5	41.25	0	—	—	—			E_3		$V_{OUT3} = E_3$	
V_{OUT4}	41.25	-200	41.25	1.95	—	—	—			E_4		$V_{OUT4} = E_4$	
V_{RLINE}	—	—	—	—	—	—	—			—		$V_{RLINE} = E_1 - E_3$	mV
V_{RLOAD_1}	6.25	-5	6.25	0	—	—	—			E_5		—	
V_{RLOAD_1}	6.25	-1500	6.25	14.95	—	—	—			E_6		$V_{RLOAD_1} = E_5 - E_6$	
V_{RLOAD_2}	—	—	—	—	—	—	—			—		$V_{RLOAD_2} = E_3 - E_4$	
V_{RTH}	14.6	-1500	14.6	14.95	—	—	—			E_7		$V_{RTH} = \Delta_e E_7$	
I_{ADJ}	4.25	-5	4.25	0	—	—	—	K2	12-13	E_8	mV	$I_{ADJ} = E_8/2000$	mA
I_{ADJ}	41.25	-5	41.25	0	—	—	—			E_9		$I_{ADJ} = E_9/2000$	
ΔI_{ADJ} (LINE)	—	—	—	—	—	—	—			—		$\Delta I_{ADJ} = \frac{E_8 - E_9}{2000}$ LINE	
ΔI_{ADJ} (LOAD)	6.25	-5	6.25	0	—	—	—			E_{10}		$\Delta I_{ADJ} = \frac{E_{10} - E_{11}}{2000}$ (LOAD)	
ΔI_{ADJ} (LOAD)	6.25	-1500	6.25	14.95	—	—	—			E_{11}			
I_{OS1}	4.25	—	10	—	—	0.425	0	K4, K5	10-5	E_{12}	V	$I_{OS} = E_{12}$	mA
V_{OUT} (RECOV)	4.25	—	10	—	—	0.425	0	$K_{4,5}$	9-11	E_{13}		V_{OUT} (RECOV) $= E_{13}$	V
I_{OS2}	40	—	40	—	—	—	0	K5	10-5	E_{14}		$I_{OS} = E_{14}$	mA
V_{OUT} (RECOV)	40	—	40	—	—	—	0	"	9-11	E_{15}		V_{OUT} (RECOV) $= E_{15}$	V
I_{PR}	4.25	—	10	—	—	0.425	1.0	K4, K5	10-5	E_{16}		$I_{PR} = E_{16}$	mA
V_{OUT} (RECOV)	4.25	—	10	—	—	0.425	1.0	"	9-11	E_{17}		V_{OUT} (RECOV) $= E_{17}$	V
I_{Q1}	4.25	—	4.25	0	1.4	—	—	K_3	12-13	E_{18}		$I_{Q1} = E_{18}/2000$	mA
I_{Q2}	14.25	—	14.25	0	1.4	—	—			E_{19}		$I_{Q2} = E_{19}/2000$	
I_{Q3}	41.25	—	41.25	0	1.4	—	—			E_{20}		$I_{Q3} = E_{20}/2000$	
V_{START}	4.25	-1500	10	0	—	0425	—	K4	9-11	E_{21}		$V_{START} = E_{21}$	V

Table 3. Test condition for 4-terminal adjustable negative voltage regulators (79XX).

Symbol	Test Conditions		Applied Test Voltages (Volts) [Pins Hi-Lo]					Relays Energized	Measurement Sense Lines			Equation	Units
	V_{IN} (volts)	I_L (mA)	pins 1-2	pins 4-5	pins 6-11	pins 7-2	pins 8-2		pins Hi-Lo	Value	Units		
V_{OUT1}	-8	5	-8	.04	—	—	—	None	9-11	E_1	V	$V_{OUT1} = E_1$	V
V_{OUT2}	-8	500	-8	4.99	—	—	—			E_2		$V_{OUT2} = E_2$	
V_{OUT3}	-20	5	-20	.04	—	—	—			E_3		$V_{OUT3} = E_3$	
V_{OUT4}	-20	500	-20	4.99	—	—	—			E_4		$V_{OUT4} = E_4$	
V_{OUT5}	-30	5	-30	.04	—	—	—			E_5		$V_{OUT5} = E_5$	
V_{OUT6}	-30	50	-30	.49	—	—	—			E_6		$V_{OUT6} = E_6$	
V_{RLINE1}	-8	50	-8	.49	—	—	—			E_7		$V_{RLINE1} = E_7 - E_6$	mV
V_{RLINE1}	-8	350	-8	3.49	—	—	—			E_8			
V_{RLINE2}	-25	350	-25	3.49	—	—	—			E_9		$V_{RLINE2} = E_8 - E_9$	
V_{RLOAD1}	-10	5	-10	.04	—	—	—			E_{10}			
V_{RLOAD1}	-10	500	-10	4.99	—	—	—			E_{11}		$V_{RLOAD1} = E_{10} - E_{11}$	
V_{RLOAD2}	—	—	—	—	—	—	—			—		$V_{RLOAD2} = E_5 - E_6$	
V_{RTH}	-15	500	-15	4.99	—	—	—			E_{12}		$V_{RTH} = E_{12}$	
I_{SCD1}	-10	5	-10	.04	—	—	—		12-13	E_{13}		$I_{SCD1} = E_{13}/2000$	mA
I_{SCD2}	-30	5	-30	.04	—	—	—			E_{14}		$I_{SCD2} = E_{14}/2000$	
ΔI_{SCD} (LINE)	-8	5	-8	.04	—	—	—			E_{15}		$\Delta I_{SCD(LINE)} = \frac{E_{15} - E_{13}}{2000}$	
ΔI_{SCD} (LOAD)	-10	500	-10	4.99	—	—	—			E_{16}		$\Delta I_{SCD(LOAD)} = \frac{E_{13} - E_{16}}{2000}$	
I_{OS1}	-10	—	-15	—	—	-1.0	0	K4, K5	10-5	E_{17}		I_{OS1} E_{17}	A
V_{OUT} (RECOV)	-10	—	-15	—	—	-1.0	0		9-11	E_{18}		$V_{OUT} = E_{18}$	V
I_{OS2}	-25	—	-30	—	—	-2.5	0		10-5	E_{19}		$I_{OS2} = E_{19}$	A
V_{OUT} (RECOV)	-25	-	-30	—	—	-2.5	0		9-11	E_{20}		$V_{OUT} = E_{20}$	V
I_{OS3}	-30	-	-40	—	—	-3.5	0		10-5	E_{21}		$I_{OS3} = E_{21}$	A
V_{OUT} (RECOV)	-30	-	-40	—	—	-3.5	0		9-11	E_{22}		$V_{OUT} = E_{22}$	V
I_{PK}	-8	—	-15	—	—	-0.8			10-5	E_{23}		$I_{PK} = E_{23}$	A
V_{OUT} (RECOV)	-8	-	-15	—	—	-0.8			9-11	E_{24}		$V_{OUT} = E_{24}$	V
I_{CONT}	-10	350	-10	3.49	—	—	—	K1, K2	12-13	E_{25}		$I_{CONT} = E_{25}/33200$	uA
V_{START}	-8	500	-15	—	—	-0.8	—	K4	9-11	E_{26}		$V_{OUT} = E_{26}$	V

Table 3-8. Test conditions for 3-terminal adjustable negative voltage regulators (cont'd).

Symbol	Test Conditions		Applied Test Voltages (Volts) [Pins Hi - Lo]					Relays Energized	Measurement Sense Lines			Equation
	V_{IN} (Volts)	I_L (mA)	pins 1-2	pins 4-5	pins 6-11	pins 7-2	pins 8-2		pins Hi-Lo	Value	units	
V_{OUT1}	-8	5	-8	.04	—	—	—	None	9-11	E_1	V	$V_{OUT1} = E_1$
V_{OUT2}	-8	1000	-8	9.99	—	—	—			E_2		$V_{OUT2} = E_2$
V_{OUT3}	-20	5	-20	.04	—	—	—			E_3		$V_{OUT3} = E_3$
V_{OUT4}	-20	1000	-20	9.99	—	—	—			E_4		$V_{OUT4} = E_4$
V_{OUT5}	-30	5	-30	.04	—	—	—			E_5		$V_{OUT5} = E_5$
V_{OUT6}	-30	100	-30	.99	—	—	—			E_6		$V_{OUT6} = E_6$
V_{RLINE1}	-8	100	-8	.99	—	—	—			E_7		$V_{RLINE1} = E_7 - E_6$
V_{RLINE1}	-8	500	-8	4.99	—	—	—			E_8		
V_{RLINE2}	-25	500	-25	4.99	—	—	—			E_9		$V_{RLINE2} = E_8 - E_9$
V_{RLOAD1}	-10	5	-10	.04	—	—	—			E_{10}		
V_{RLOAD1}	-10	1000	-10	9.99	—	—	—			E_{11}		$V_{RLOAD1} = E_{10} - E_{11}$
V_{RLOAD2}	—	—	—	—	—	—	—			—		$V_{RLOAD2} = E_5 - E_6$
V_{RTH}	-15	1000	-15	9.99	—	—	—			E_{12}		$V_{RTH} = E_{12}$
I_{SCD1}	-10	5	-10	.04	—	—	—		12-13	E_{13}		$I_{SCD1} = E_{13}/2000$
I_{SCD2}	-30	5	-30	.04	—	—	—			E_{14}		$I_{SCD2} = E_{14}/2000$
ΔI_{SCD} (LINE)	-8	5	-8	.04	—	—	—			E_{15}		$\Delta I_{SCD(LINE)} = \frac{E_{15} - E}{2000}$
ΔI_{SCD} (LOAD)	-10	1000	-10	9.99	—	—	—			E_{16}		$\Delta I_{SCD(LOAD)} = \frac{E_{13} - E_{16}}{2000}$
I_{OS1}	-10	—	-15	—	—	-1.0	0	K4, K5	10-5	E_{17}		$I_{OS1} E_{17}$
V_{OUT} (RECOV)	-10	—	-15	—	—	-1.0	0		9-11	E_{18}		$V_{OUT} = E_{18}$
I_{OS2}	-25	—	-30	—	—	-2.5	0		10-5	E_{19}		$I_{OS2} = E_{19}$
V_{OUT} (RECOV)	-25	—	-30	—	—	-2.5	0		9-11	E_{20}		$V_{OUT} = E_{20}$
I_{OS3}	-30	—	-40	—	—	-3.5	0		10-5	E_{21}		$I_{OS3} = E_{21}$
V_{OUT} (RECOV)	-30	—	-40	—	—	-3.5	0		9-11	E_{22}		$V_{OUT} = E_{22}$
I_{PK}	-8	—	-15	—	—	-0.8			10-5	E_{23}		$I_{PK} = E_{23}$
V_{OUT} (RECOV)	-8	—	-15	—	—	-0.8			9-11	E_{24}		$V_{OUT} = E_{24}$
I_{CONT}	-10	500	-10	4.99	—	—	—	K1, K2	12-13	E_{25}		$I_{CONT} = E_{25}/33200$
V_{START}	-8	1000	-15	—	—	-0.8	—	K4	9-11	E_{26}		$V_{OUT} = E_{26}$

...-terminal adjustable negative voltage ...

Test	Test Conditions		Applied Test Voltages (Volts) [pins Hi-Lo]					Relays Energized	Measurement Sense Lines			Equation	Limits
	V_{IN} (Volts)	I_L (mA)	pins 1-2	pins 4-5	pins 6-11	pins 7-2	pins 8-2		pins Hi-Lo	Value	Units		
V_{OUT1}	-4.25	5	-4.25	0	—	—	—	None	9-11	E_1	V	$V_{OUT1} = E_1$	V
V_{OUT2}	-4.25	500	-4.25	4.95	—	—	—			E_2		$V_{OUT2} = E_2$	
V_{OUT3}	-4.25	5	-4.25	0	—	—	—			E_3		$V_{OUT3} = E_3$	
V_{OUT4}	-4.25	50	-4.25	0.45	—	—	—			E_4		$V_{OUT4} = E_4$	
V_{RLINE}	—	—	—	—	—	—	—			—		$V_{RLINE} = E_1 - E_3$	mV
V_{RLOAD}	-6.25	5	-6.25	0	—	—	—			E_5		—	
V_{RLOAD1}	-6.25	500	-6.25	4.95	—	—	—			E_6		$V_{RLOAD1} = E_5 - E_6$	
V_{RLOAD2}	—	—	—	—	—	—	—			—		$V_{RLOAD2} = E_3 - E_4$	
V_{RTH}	-14.6	750	-14.6	7.45	—	—	—			E_7		$V_{RTH} = \Delta_E E_7$	
I_{ADJ}	-4.25	5	-4.25	0	—	—	—	K2	12-13	E_8	mV	$I_{ADJ} = E_8/2000$	μA
I_{ADJ}	-4.25	5	-4.25	0	—	—	—			E_9		$I_{ADJ} = E_9/2000$	
ΔI_{ADJ} (LINE)	—	—	—	—	—	—	—			—		$\Delta I_{ADJ\ LINE} = \frac{E_8 - E_9}{2000}$	
ΔI_{ADJ} (LOAD)	-6.25	5	-6.25	0	—	—	—			E_{10}		$\Delta I_{ADJ\ (LOAD)} = \frac{E_{10} - E_{11}}{2000}$	
ΔI_{ADJ} (LOAD)	-6.25	500	-6.25	4.95	—	—	—			E_{11}			
I_{OS1}	-4.25	—	-10	—	—	+0.425	0	K4, K5	10-5	E_{12}	V	$I_{OS} = E_{12}$	A
V_{OUT} (RECOV)	-4.25	—	-10	—	—	+0.425	0	K4, K5	9-11	E_{13}		$V_{OUT\ (RECOV)} = E_{13}$	V
I_{OS2}	-40	—	-40	—	—	—	0	K5	10-5	E_{14}		$I_{OS} = E_{14}$	A
V_{OUT} (RECOV)	-40	—	-40	—	—	—	0	K5	9-11	E_{15}		$V_{OUT\ (RECOV)} = E_{15}$	V
I_{PK}	-4.25	—	-10	—	—	+0.425	-1.0	K4, K5	10-5	E_{16}		$I_{PK} = E_{16}$	A
V_{OUT} (RECOV)	-4.25	—	-10	—	—	+0.425	-1.0	K4, K5	9-11	E_{17}		$V_{OUT\ (RECOV)} = E_{17}$	V
I_{Q1}	-4.25	—	-4.25	0	-1.4	—	—	K3	12-13	E_{18}		$I_{Q1} = E_{18}/2000$	mA
I_{Q2}	-4.25	—	-4.25	0	-1.4	—	—			E_{19}		$I_{Q2} = E_{19}/2000$	
I_{Q3}	-4.25	—	-4.25	0	-1.4	—	—			E_{20}		$I_{Q3} = E_{20}/2000$	
V_{START}	-4.25	500	-10	0	—	+0.425	—	K4	9-11	E_{21}		$V_{START} = E_{21}$	V

Table 3.10. Test conditions for 3-terminal adjustable negative voltage regulators (LM137).

Symbol	Test Conditions		Applied Test Voltages (Volts) [pins Hi-Lo]					Relays Energized	Measurement Sense Lines			Equation
	V_{IN} Volts	I_L (mA)	pins 1-2	pins 4-5	pins 6-11	pins 7-2	pins 8-2		pins Hi-Lo	Value	Units	
V_{OUT1}	-4.25	5	-4.25	0	—	—	—	None	9-11	E_1	V	$V_{OUT1} = E_1$
V_{OUT2}	-4.25	1500	-4.25	14.95	—	—	—			E_2		$V_{OUT2} = E_2$
V_{OUT3}	-41.25	5	-41.25	0	—	—	—			E_3		$V_{OUT3} = E_3$
V_{OUT4}	-41.25	200	-41.25	1.95	—	—	—			E_4		$V_{OUT4} = E_4$
V_{RLINE}	—	—	—	—	—	—	—			—		$V_{RLINE} = E_1 - E_3$
V_{RLOAD1}	-6.25	5	-6.25	0	—	—	—			E_5		—
V_{RLOAD2}	-6.25	1500	-6.25	14.95	—	—	—			E_6		$V_{RLOAD1} = E_5 - E_6$
V_{RLOAD}	—	—	—	—	—	—	—			—		$V_{RLOAD2} = E_3 - E_4$
V_{RTH}	-14.6	1500	-14.6	14.95	—	—	—			E_7		$V_{RTH} = \Delta_t E_7$
I_{ADJ}	-4.25	5	-4.25	0	—	—	—	K2	12-13	E_8	mV	$I_{ADJ} = E_8/2000$
I_{ADJ}	-41.25	5	-41.25	0	—	—	—			E_9		$I_{ADJ} = E_9/2000$
ΔI_{ADJ} (LINE)	—	—	—	—	—	—	—			—		ΔI_{ADJ} LINE $= \frac{E_8 - E_9}{2000}$
ΔI_{ADJ} (LOAD)	-6.25	5	-6.25	0	—	—	—			E_{10}		ΔI_{ADJ} (LOAD) $= \frac{E_{10} - E_{11}}{2000}$
ΔI_{ADJ} (LOAD)	-6.25	1500	-6.25	14.95	—	—	—			E_{11}		
I_{OS1}	-4.25	—	-10	—	—	-0.425	0	K4, K5	10-5	E_{12}	V	$I_{OS} = E_{12}$
V_{OUT} (RECOV)	-4.25	—	-10	—	—	-0.425	0	K4, K5	9-11	E_{13}		V_{OUT} (RECOV) $= E_{13}$
I_{OS2}	-40	—	-40	—	—	—	0	K5	10-5	E_{14}		$I_{OS} = E_{14}$
V_{OUT} (RECOV)	-40	—	-40	—	—	—	0	K5	9-11	E_{15}		V_{OUT} (RECOV) $= E_{15}$
I_{PK}	-4.25	—	-10	—	—	-0.425	-1.0	K4, K5	10-5	E_{16}		$I_{PK} = E_{16}$
V_{OUT} (RECOV)	-4.25	—	-10	—	—	-0.425	-1.0	K4, K5	9-11	E_{17}		V_{OUT} (RECOV) $= E_{17}$
I_{Q1}	-4.25	—	-4.25	0	-1.4	—	—	K_3	12-13	E_{18}		$I_{Q1} = E_{18}/2000$
I_{Q2}	-14.25	—	-14.25	0	-1.4	—	—			E_{19}		$I_{Q2} = E_{19}/2000$
I_{Q3}	-41.25	—	-41.25	0	-1.4	—	—			E_{20}		$I_{Q3} = E_{20}/2000$
V_{START}	-4.25	1500	-10	0	—	-0.425	—	K4	9-11	E_{21}		$V_{START} = E_{21}$

TABLE 5.11. Summary of S-3260 Test Adapter Accuracies.

Parameter	Device	Limits Low	Limits High	Required Test Accuracy 10:1	Required Test Accuracy 4:1	S-3260 Basic Meas. Accuracy 1/	S-3260 Test Result Accuracy 2/	Units
VOUT1-VOUT4	LM137H, K	-1.275V	-1.225V	±2.5	±6.25	±26.2-26.3	±3.4-3.5	mV
	LM117H, K	-1.200V	-1.300V	±5	±12.5	±26.2-26.3	±3.4-3.6	
VRLINE	LM137H, K	+5	+9	±.9	±2.25	±52.4-52.6	±.42	
	LM117H, K			±.9	±2.25	±52.4-52.6	±.42	
VRLOAD1	LM137H, K	-6	+6	±0.6	±1.5	±52.4-52.6	±.42	
	LM117H, K	-3.5	+3.5	±0.35	±.88	±52.4-52.6	±.42	
VRLOAD2	LM137H, K	-6	+6	±.6	±1.5	±52.4-52.6	±.42	
	LM117H, K	-3.5	+3.5	±0.35	±.88	±52.4-52.6	±.42	
VRTH	LM137H, K	-5	+5	±.5	±1.25	±52.4-52.6	±.42	
	LM117H, K	-5	+5	±.5	±1.25	±52.4-52.6	±.42	
IADJ1	LM137H, K	+25	+100	±6.2	±15.6	±.425-.800	±.007-.014	uA
	LM117H, K	-100	-15	±5.75	±14.38	±.375-.800	±.005-.014	
IADJ2	LM137H, K	+25	+100	±6.2	±15.6	±.425-.800	±.007-.014	
	LM117H, K	-100	-15	±5.75	±14.38	±.375-.800	±.005-.014	
DIADJ1	LM137H, K	-5	+5	±.5	±1.25	±.85-1.6	±.014-.028	
	LM117H, K	-5	+5	±.5	±1.25	±.75-1.6	±.01-.028	
DIADJ2	LM137H, K	-5	+5	±.5	±1.25	±.85-1.6	±.014-.028	
	LM117H, K	-5	+5	±.5	±1.25	±.75-1.6	±.01-.028	
IOS1 & IPEAK	LM137H	500	1800	±65	±162.5	±.725-6.98	±.725-6.98	mA
	LM137K	1500	3500	±100	±250	±7.25-7.45	±7.25-7.45	
	LM117H	-1800	-500	±65	±162.5	±.725-6.98	±.725-6.98	
	LM117K	-3500	-1500	±100	±250	±7.25-7.45	±7.25-7.45	
IOS2	LM137H	50	500	±22.5	±56.25	±.16-.725	±.16-.725	
	LM137K	200	800	±60	±75	±.74-.76	±.74-.76	
	LM117H	-500	-50	±22.5	±56.25	±.725-.16	±.725-.16	
	LM117K	-800	-200	±30	±75.0	±.76-.74	±.76-.74	
IQ1, IQ2	LM137H, K	.200	3	±140	±350	±3.5-40	±.37-1.54	uA
	LM117H, K	-3	-.500	±125	±312.5	±5-40	±3.76-0.4	
IQ3	LM137H, K	1	5	±200	±500	±30-50	±3.6-4.15	
	LM117H, K	-5	-1	±200	±500	±30-50	±4.15-3.6	

NOTES: 1/ "S-3260 Basic Meas. Accuracy" indicates the accuracy obtainable using the S-3260 test system to measure the parameters directly.

2/ "S-3260 Test Result Accuracy" indicates the accuracy obtained using external circuitry and external measurement equipment under S-3260 control.

Table 3.12.

POS. ADJ. VOLTAGE REGULATORS-LM117H; TEMPERATURE: 25 DEG C ; 10 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	HI-LIMIT	UNITS
VOUT1	+4.25	-5	1.200	1.236	1.249	1.245	1.233	1.251	1.300	V
VOUT2	+4.25	-500	1.200	1.228	1.242	1.237	1.225	1.242	1.300	V
VOUT3	+41.25	-5	1.200	1.240	1.254	1.251	1.239	1.257	1.300	V
VOUT4	+41.25	-50	1.200	1.239	1.252	1.249	1.239	1.256	1.300	V
VRLINE	+4.25 +41.25	-5	-9.000M	5.203M	5.316M	6.334M	5.429M	6.334M	9.000M	V
VRLOAD1	+6.25	-5 -500	-3.500M	-1.697M	-1.244M	-2.488M	-4.750M#	-1.697M	3.500M	V
VRLOAD2	+41.25	-5 -50	-3.500M	-1.470M	-1.470M	-1.810M	-1.357M	-1.810M	3.500M	V
VRTH (IL APPLIED FOR 20.5Msec.)	+41.25	-125	-5.000M	2.715M	3.619M	2.941M	678.7U	4.298M	5.000M	V
IADJ1 (LINE)	+4.25	-5	-100.0U	-41.48U	-49.48U	-56.82U	-42.99U	-57.38U	-15.00U	A
IADJ2 (LINE)	+41.25	-5	-100.0U	-41.97U	-50.07U	-57.58U	-43.53U	-58.16U	-15.00U	A
DIADJ1 (LINE)	+4.25 +41.25	-5	-5.000U	-490.0N	-593.0N	-762.5N	-533.5N	-771.0N	5.000U	A
DIADJ2 (LOAD)	+6.25	-5 -500	-5.000U	-575.0N	-705.0N	-768.0N	-510.5N	-861.0N	5.000U	A
IOS1 (VOUT) RECOV.	+4.25	VF=0V	-1.800 1.200	-1.205 1.232	-1.240 1.244	-1.205 1.240	-1.255 1.227	-1.285 1.247	-500.0M 1.300	A V
IOS2 (VOUT) RECOV.	+40.00	VF=0V	-500.0M 1.200	-260.0M 1.243	-210.0M 1.256	-195.0M 1.254	-280.0M 1.241	-195.0M 1.260	-50.00M 1.300	A V
IPEAK (VOUT) RECOV.	+4.25	VF=+1.0V	-1.800 1.200	-1.210 1.232	-1.250 1.244	-1.200 1.239	-1.250 1.226	-1.285 1.246	-500.0M 1.300	A V
IQ1	+4.25	VF=+1.4V	-3.000M	-1.188M	-1.298M	-1.395M	-1.227M	-1.372M	-500.0U	A
IQ2	+14.25	VF=+1.4V	-3.000M	-1.440M	-1.568M	-1.713M	-1.498M	-1.685M	-500.0U	A
IQ3	+41.25	VF=+1.4V	-5.000M	-2.988M	-3.442M	-3.875M	-3.202M	-3.832M	-1.000M	A
VSTART	+4.25	-500	1.200	1.229	1.242	1.238	1.225	1.243	1.300	V

NOTE #1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.12. (cont'd).

POS. ADJ. VOLTAGE REGULATORS-LM117H; TEMPERATURE: 25 DEG C ; 10 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 6	S/N 7	S/N 8	S/N 9	S/N 10	HI-LIMIT	UNITS
VOUT1	+4.25	-5	1.200	1.245	1.260	1.226	1.229	1.232	1.300	V
VOUT2	+4.25	-500	1.200	1.239	1.251	1.218	1.221	1.224	1.300	V
VOUT3	+41.25	-5	1.200	1.253	1.266	1.232	1.235	1.240	1.300	V
VOUT4	+41.25	-50	1.200	1.250	1.264	1.230	1.233	1.237	1.300	V
VRLINE	+4.25 +41.25	-5	-9.000M	6.447M	6.108M	5.429M	4.977M	6.108M	9.000M	V
VRLOAD1	+6.25	-5 -500	-3.500M	-791.7U	-3.167M	-2.828M	-3.167M	-2.036M	3.500M	V
VRLOAD2	+41.25	-5 -50	-3.500M	-1.583M	-1.810M	-1.810M	-1.810M	-1.697M	3.500M	V
VRTH (IL APPLIED FOR 20.5Msec.)	+41.25	-125	-5.000M	3.619M	2.149M	3.280M	3.054M	3.054M	5.000M	V
IADJ1 (LINE)	+4.25	-5	-100.0U	-53.91U	-57.20U	-43.18U	-47.31U	-51.30U	-15.00U	A
IADJ2 (LINE)	+41.25	-5	-100.0U	-54.60U	-58.00U	-43.68U	-47.87U	-51.94U	-15.00U	A
DIADJ1 (LINE)	+4.25 +41.25	-5	-5.000U	-691.5N	-806.0N	-497.0N	-560.0N	-641.0N	5.000U	A
DIADJ2 (LOAD)	+6.25	-5 -500	-5.000U	-737.5N	-764.5N	-593.0N	-624.0N	-682.5N	5.000U	A
IOS1	+4.25	VF=0V	-1.800	-1.240	-1.215	-1.290	-1.220	-1.240	-500.0M	A
(VOUT)	RECOV.		1.200	1.242	1.255	1.222	1.226	1.229	1.300	V
IOS2	+40.00	VF=0V	-500.0M	-205.0M	-190.0M	-285.0M	-210.0M	-230.0M	-50.00M	A
(VOUT)	RECOV.		1.200	1.255	1.268	1.235	1.236	1.241	1.300	V
IPEAK	+4.25	VF=+1.0V	-1.800	-1.245	-1.210	-1.290	-1.220	-1.250	-500.0M	A
(VOUT)	RECOV.		1.200	1.243	1.253	1.223	1.224	1.229	1.300	V
IQ1	+4.25	VF=+1.4V	-3.000M	-1.440M	-1.347M	-1.137M	-1.240M	-1.283M	-500.0U	A
IQ2	+14.25	VF=+1.4V	-3.000M	-1.745M	-1.753M	-1.380M	-1.502M	-1.583M	-500.0U	A
IQ3	+41.25	VF=+1.4V	-5.000M	-3.777M	-3.903M	-3.017M	-3.322M	-3.515M	-1.000M	A
VSTART	+4.25	-500	1.200	1.240	1.252	1.219	1.222	1.227	1.300	V

NOTE #1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.13.

POS. ADJ. VOLTAGE REGULATORS-LM117H; TEMPERATURE: -55 DEG C ; 10 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	HI LIMIT	UNITS
VOUT1	+4.25	-5	1.200	1.235	1.245	1.243	1.233	1.244	1.300	V
VOUT2	+4.25	-500	1.200	1.238	1.240	1.238	1.228	1.239	1.300	V
VOUT3	+41.25	-5	1.200	1.240	1.250	1.249	1.239	1.251	1.300	V
VOUT4	+41.25	-50	1.200	1.239	1.249	1.247	1.237	1.249	1.300	V
VRLINE	+4.25 / +41.25	-5	-23.00M	4.637M	4.977M	4.977M	4.185M	4.977M	23.00M	V
VRLOAD1	+6.25	-5 / -500	-12.00M	904.9U	791.8U	678.5U	-2.036M	1.018M	12.00M	V
VRLOAD2	+41.25	-5 / -50	-12.00M	-791.8U	-904.9U	-1.131M	-1.018M	-1.018M	12.00M	V
VRTH (IL APPLIED FOR 20.5Msec.)	+41.25	-125	-5.000M	4.185M	4.524M	3.959M	1.810M	5.316M	5.000M	V
IADJ1 (LINE)	+4.25	-5	-100.0U	-33.88U	-48.56U	-46.59U	-35.32U	-45.74U	-15.00U	A
IADJ2 (LINE)	+41.25	-5	-100.0U	-34.40U	-44.75U	-49.92U	-38.24U	-46.55U	-15.00U	A
DIADJ1 (LINE)	+4.25 / +41.25	-5	-5.000U	-523.5N	-4.190U	-3.331U	-2.921U	-816.0N	5.000U	A
DIADJ2 (LOAD)	+6.25	-5 / -500	-5.000U	-1.141U	-1.455U	-1.573U	-1.165U	-1.722U	5.000U	A
IOS1 (VOUT)	+4.25 RECOV.	VF=0V	-1.800 / 1.200	-1.220 / 1.235	-1.275 / 1.244	-1.220 / 1.241	-1.265 / 1.230	-1.315 / 1.243	-500.0M / 1.300	A V
IOS2 (VOUT)	+40.00 RECOV.	VF=0V	-500.0M / 1.200	-365.0M / 1.243	-290.0M / 1.252	-260.0M / 1.251	-465.0M / 1.242	-275.0M / 1.253	-50.00M / 1.300	A V
IPEAK (VOUT)	+4.25 RECOV.	VF=+1.0V	-1.800 / 1.200	-1.220 / 1.233	-1.280 / 1.243	-1.225 / 1.241	-1.270 / 1.231	-1.325 / 1.242	-500.0M / 1.300	A V
IQ1	+4.25	VF=+1.4V	-3.000M	-950.0U	-1.048M	-1.103M	-987.5U	-1.053M	-500.0U	A
IQ2	+4.25	VF=+1.4V	-3.000M	-1.247M	-1.397M	-1.500M	-1.293M	-1.440M	-500.0U	A
IQ3	+41.25	VF=+1.4V	-5.000M	-2.823M	-3.360M	-3.745M	-3.142M	-3.672M	-1.000M	A
VSTART	+4.25	-500	1.200	1.230	1.240	1.239	1.229	1.240	1.300	V

NOTE #1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.13. (cont'd).

POS. ADJ. VOLTAGE REGULATORS-LM117H; TEMPERATURE: -55 DEG C ; 10 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 6	S/N 7	S/N 8	S/N 9	S/N 10	HI-LIMIT	UNITS
VOUT1	+4.25	-5	1.200	1.245	1.258	1.229	1.232	1.234	1.300	V
VOUT2	+4.25	-500	1.200	1.238	1.253	1.223	1.226	1.228	1.300	V
VOUT3	+41.25	-5	1.200	1.249	1.264	1.235	1.236	1.239	1.300	V
VOUT4	+41.25	-50	1.200	1.249	1.262	1.233	1.235	1.236	1.300	V
VRLINE	+4.25 +41.25	-5	-23.00M	5.429M	5.768M	4.411M	4.298M	4.637M	23.00M	U
VRLOAD1	+6.25	-5 -500	-12.00M	1.697M	452.4U	-226.3U	-339.3U	339.4U	12.00M	U
VRLOAD2	+41.25	-5 -50	-12.00M	-791.8U	-904.8U	-904.9U	-904.8U	-904.9U	12.00M	U
VRTH (IL APPLIED FOR 20.5msec.)	+41.25	-125	-5.000M	5.203M*	3.280M	4.298M	4.185M	4.072M	5.000M	U
IADJ1 (LINE)	+4.25	-5	-100.0U	-44.46U	-45.42U	-34.63U	-38.25U	-40.85U	-15.00U	A
IADJ2 (LINE)	+41.25	-5	-100.0U	-45.67U	-46.58U	-35.29U	-38.86U	-42.73U	-15.00U	A
DIADJ1 (LINE)	+4.25 +41.25	-5	-5.000U	-1.204U	-1.165U	-657.5N	-613.0N	-1.873U	5.000U	A
DIADJ2 (LOAD)	+6.25	-5 -500	-5.000U	-1.438U	-1.693U	-1.305U	-1.361U	-1.499U	5.000U	A
IOS1	+4.25	VF=0V	-1.800	-1.255	-1.215	-1.305	-1.255	-1.250	-500.0M	A
(VOUT) RECOV.			1.200	1.244	1.255	1.228	1.229	1.232	1.300	V
IOS2	+40.00	VF=0V	-500.0M	-270.0M	-270.0M	-480.0M	-300.0M	-310.0M	-50.00M	A
(VOUT) RECOV.			1.200	1.252	1.265	1.240	1.239	1.241	1.300	V
IPEAK	+4.25	VF=+1.0V	-1.800	-1.255	-1.210	-1.310	-1.265	-1.255	-500.0M	A
(VOUT) RECOV.			1.200	1.243	1.255	1.227	1.229	1.230	1.300	V
IQ1	+4.25	VF=+1.4V	-3.000M	-1.153M	-1.077M	-892.5U	-972.5U	-995.0U	-500.0U	A
IQ2	+14.25	VF=+1.4V	-3.000M	-1.520M	-1.602M	-1.173M	-1.288M	-1.342M	-500.0U	A
IQ3	+41.25	VF=+1.4V	-5.000M	-3.662M	-3.922M	-2.910M	-3.212M	-3.325M	-1.000M	A
VSTART	+4.25	-500	1.200	1.240	1.253	1.225	1.227	1.229	1.300	U

NOTE *1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.14

POS. ADJ. VOLTAGE REGULATORS-LM117H; TEMPERATURE: 125 DEG C ; 10 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	HI-LIMIT	UNITS
VOUT1	+4.25	-5	1.200	1.228	1.245	1.241	1.224	1.251	1.300	V
VOUT2	+4.25	-500	1.200	1.219	1.235	1.230	1.214	1.239	1.300	V
VOUT3	+41.25	-5	1.200	1.236	1.252	1.248	1.231	1.258	1.300	V
VOUT4	+41.25	-50	1.200	1.232	1.249	1.246	1.229	1.255	1.300	V
VRLINE	+4.25 +41.25	-5	-23.00M	6.447M	6.673M	7.691M	7.352M	8.031M	23.00M	V
VRLOAD1	+6.25	-5 -500	-12.00M	-4.411M	-3.619M	-4.637M	-7.126M	-5.542M	12.00M	V
VRLOAD2	+41.25	-5 -50	-12.00M	-2.601M	-1.697M	-2.715M	-2.602M	-2.828M	12.00M	V
VRTH (IL APPLIED FOR 20.5Msec.)	+41.25	-125	-5.000M	2.375M	2.828M	1.810M	678.7U	2.941M	5.000M	V
IADJ1 (LINE)	+4.25	-5	-100.0U	-46.20U	-54.35U	-62.68U	-47.69U	-64.08U	-15.00U	A
IADJ2 (LINE)	+41.25	-5	-100.0U	-46.63U	-54.91U	-63.41U	-48.16U	-64.80U	-15.00U	A
DIADJ1 (LINE)	+4.25 +41.25	-5	-5.000U	-435.5N	-555.0N	-728.0N	-473.0N	-720.0N	5.000U	A
DIADJ2 (LOAD)	+6.25	-5 -500	-5.000U	-189.5N	-286.5N	-274.0N	-100.0N	-325.0N	5.000U	A
IOS1	+4.25	VF=0V	-1.800	-1.165	-1.185	-1.150	-1.200	-1.220	-500.0M	A
(VOUT)	RECOV.		1.200	1.221	1.239	1.233	1.215	1.243	1.300	V
IOS2	+40.00	VF=0V	-500.0M	-280.0M	-200.0M	-195.0M	-310.0M	-190.0M	-50.00M	A
(VOUT)	RECOV.		1.200	1.236	1.253	1.249	1.233	1.260	1.300	V
IPEAK	+4.25	VF=+1.0V	-1.800	-1.170	-1.185	-1.140	-1.205	-1.215	-500.0M	A
(VOUT)	RECOV.		1.200	1.220	1.239	1.233	1.214	1.243	1.300	V
IQ1	+4.25	VF=+1.4V	-3.000M	-1.342M	-1.428M	-1.583M	-1.382M	-1.560M	-500.0U	A
IQ2	+14.25	VF=+1.4V	-3.000M	-1.570M	-1.683M	-1.850M	-1.640M	-1.832M	-500.0U	A
IQ3	+41.25	VF=+1.4V	-5.000M	-2.942M	-3.342M	-3.793M	-3.120M	-3.730M	-1.000M	A
VSTART	+4.25	-500	1.200	1.219	1.236	1.230	1.214	1.240	1.300	V

POS. ADJ. VOLTAGE REGULATORS-LM117H; TEMPERATURE: 150 DEG C ; 10 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	HI-LIMIT	UNITS
VOUT5	-6.25	5	1.200	1.227	1.244	1.240	1.223	1.251	1.300	V

NOTE #1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.14. (cont'd).

POS. ADJ. VOLTAGE REGULATORS-LM117H; TEMPERATURE: 125 DEG C ; 10 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 6	S/N 7	S/N 8	S/N 9	S/N 10	HI-LIMIT	UNITS
VOUT1	+4.25	-5	1.200	1.242	1.256	1.216	1.221	1.227	1.300	V
VOUT2	+4.25	-500	1.200	1.233	1.247	1.206	1.210	1.215	1.300	V
VOUT3	+41.25	-5	1.200	1.240	1.254	1.224	1.227	1.233	1.300	V
VOUT4	+41.25	-50	1.200	1.247	1.262	1.221	1.225	1.230	1.300	V
VRLINE	+4.25 +41.25	-5	-23.00M	7.691M	7.013M	7.239M	6.560M	7.804M	23.00M	V
VRLOAD1	+6.25	-5 -500	-12.00M	-2.715M	-4.750M	-5.882M	-6.447M	-5.882M	12.00M	V
VRLOAD2	+41.25	-5 -50	-12.00M	-2.262M	-2.488M	-2.602M	-2.601M	-2.602M	12.00M	V
VRTH (IL APPLIED FOR 20.5MSec.)	+41.25	-125	-5.000M	2.601M	1.131M	2.715M	1.923M	2.036M	5.000M	V
IADJ1 (LINE)	+4.25	-5	-100.0U	-59.25U	-63.37U	-47.44U	-51.91U	-56.66U	-15.00U	A
IADJ2 (LINE)	+41.25	-5	-100.0U	-59.90U	-64.06U	-47.91U	-52.40U	-57.30U	-15.00U	A
DIADJ1 (LINE)	+4.25 +41.25	-5	-5.000U	-653.5N	-688.5N	-466.0N	-493.5N	-635.0N	5.000U	A
DIADJ2 (LOAD)	+6.25	-5 -500	-5.000U	-296.5N	-238.5N	-208.5N	-208.5N	-220.5N	5.000U	A
IOS1 (VOUT)	+4.25 RECOV.	VF=0V	-1.800 1.200	-1.200 1.236	-1.165 1.249	-1.230 1.209	-1.150 1.212	-1.200 1.218	-500.0M 1.300	A V
IOS2 (VOUT)	+40.00 RECOV.	VF=0V	-500.0M 1.200	-215.0M 1.251	-200.0M 1.266	-315.0M 1.227	-205.0M 1.227	-235.0M 1.235	-50.00M 1.300	A V
IPEAK (VOUT)	+4.25 RECOV.	VF=+1.0V	-1.800 1.200	-1.195 1.236	-1.160 1.249	-1.235 1.207	-1.145 1.211	-1.210 1.218	-500.0M 1.300	A V
IO1	+4.25	VF=+1.4V	-3.000M	-1.620M	-1.507M	-1.263M	-1.375M	-1.443M	-500.0U	A
IO2	+14.25	VF=+1.4V	-3.000M	-1.890M	-1.840M	-1.502M	-1.607M	-1.727M	-500.0U	A
IO3	+41.25	VF=+1.4V	-5.000M	-3.720M	-3.705M	-2.953M	-3.200M	-3.450M	-1.000M	A
VSTART	+4.25	-500	1.200	1.233	1.247	1.206	1.210	1.215	1.300	V

POS. ADJ. VOLTAGE REGULATORS-LM117H; TEMPERATURE: 150 DEG C ; 10 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 6	S/N 7	S/N 8	S/N 9	S/N 10	HI-LIMIT	UNITS
VOUT5	-6.25	5	1.200	1.225	1.225	1.225	1.226	1.225	1.300	V

NOTE #1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

TABLE 3.15. POS. ADJ. VOLTAGE REGULATOR - LM117H T_A = 25°C 6-15-79

PARAMETER	CONDITIONS	LO - LIMIT	S/N7	S/N8	S/N9	S/N10	-	HI - LIMIT	UNITS
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN} = 6.25 V e_i = 1 V_{RMS} @ 2400 Hz I_L = -125 mA	65	> 80	> 80	> 80	> 80		-	dB
V_{NO}	V_{IN} = 6.25 V I_L = - 50 mA	-	100	95	100	95		120	uV_{RMS}
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN} = 6.25 V ΔV_{IN} = 3.0 V I_L = - 10 mA	-	1.6	2.0	1.6	1.6		6	mV/V
$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN} = 6.25 V I_L = - 50 mA ΔI_L = -200 mA	-	.20	.20	.20	.18		0.6	mV/mA

Table 3.15. POS. ADJ. VOLTAGE REGULATOR - LM117H T_A = 25°C 6-15-79 (cont'd).

PARAMETER	CONDITIONS	LO - LIMIT	S/N1	S/N2	S/N4	S/N5	S/N6	HI - LIMIT	UNITS
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN} = 6.25V e_i = 1 V_{RMS} @ 2400 Hz I_L = -125 mA	65	> 80	> 80	> 80	> 80	> 80	-	dB
V_{NO}	V_{IN} = 6.25 V I_L = -50 mA	-	100	100	95	100	100	120	uV_{RMS}
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN} = 6.25 V ΔV_{IN} = 3.0 V I_L = - 10 mA	-	1.6	1.6	1.6	2.0	1.6	6	mV/V
$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN} = 6.25 V I_L = - 50 mA ΔI_L = -200 mA	-	.25	.20	.20	.19	.18	0.6	mV/mA

Table 3.16.

POS. ADJ. VOLTAGE REGULATORS-LM117K; TEMPERATURE: 25 DEG C ; 10 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	HI LIMIT	UNITS
VOUT1	+4.25	-5	1.200	1.249	1.249	1.239	1.240	1.248	1.300	V
VOUT2	+4.25	-1500	1.200	1.249	1.247	1.236	1.239	1.247	1.300	V
VOUT3	+41.25	-5	1.200	1.253	1.254	1.242	1.247	1.253	1.300	V
VOUT4	+41.25	-200	1.200	1.251	1.251	1.240	1.244	1.249	1.300	V
VRLINE	+4.25 +41.25	-5	-9.000M	3.959M	4.298M	3.506M	6.221M	4.072M	9.000M	V
VRLOAD1	+6.25	-5 -1500	-3.500M	226.3U	565.5U	452.4U	-1.131M	-339.4U	3.500M	V
VRLOAD2	+41.25	-5 -200	-3.500M	-1.810M	-1.810M	-1.923M	-2.715M	-2.375M	3.500M	V
VRTH (IL APPLIED FOR 20.5Msec.)	+41.25	-500	-5.000M	3.846M	4.637M	3.280M	2.036M	2.488M	5.000M	V
IADJ1 (LINE)	+4.25	-5	-100.0U	-56.66U	-56.10U	-52.02U	-54.31U	-59.98U	-15.00U	A
IADJ2 (LINE)	+41.25	-5	-100.0U	-57.05U	-56.47U	-52.29U	-54.83U	-60.34U	-15.00U	A
DIADJ1 (LINE)	+4.25 +41.25	-5	-5.000U	-392.0N	-373.5N	-276.0N	-513.5N	-357.0N	5.000U	A
DIADJ2 (LOAD)	+6.25	-5 -1500	-5.000U	-214.5N	-272.5N	-152.0N	-63.50N	-141.0N	5.000U	A
IOS1 (VOUT)	+4.25 RECOV.	VF=0V	-3.500 1.200	-2.905 1.250	-2.495 1.251	-2.710 1.240	-2.565 1.241	-2.730 1.248	-1.500 1.300	A V
IOS2 (VOUT)	+40.00 RECOV.	VF=0V	-1.000 1.200	-495.0M 1.254	-445.0M 1.253	-455.0M 1.242	-465.0M 1.246	-400.0M 1.253	-180.0M 1.300	A V
IPEAK (VOUT)	+4.25 RECOV.	VF=+1.0V	-3.500 1.200	-2.490 1.251	-2.330 1.249	-2.430 1.239	-2.330 1.240	-2.220 1.248	-1.500 1.300	A V
IQ1	+4.25	VF=+1.4V	-3.000M	-1.370M	-1.392M	-1.252M	-1.117M	-1.443M	-500.0U	A
IQ2	+14.25	VF=+1.4V	-3.000M	-1.750M	-1.800M	-1.525M	-1.543M	-1.740M	-500.0U	A
IQ3	+41.25	VF=+1.4V	-5.000M	-3.845M	-3.903M	-3.395M	-3.593M	-3.922M	-1.000M	A
VSTART	+4.25	-1500	1.200	1.249	1.249	1.239	1.240	1.249	1.300	V

NOTE #1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.16. (cont'd).

POS. ADJ. VOLTAGE REGULATORS-LM117K; TEMPERATURE: 25 DEG C ; 10 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 6	S/N 7	S/N 8	S/N 9	HI LIMIT	UNITS
VOUT1	+4.25	-5	1.200	1.249	1.247	1.240	1.258	1.300	V
VOUT2	+4.25	-1500	1.200	1.247	1.245	1.239	1.256	1.300	V
VOUT3	+41.25	-5	1.200	1.254	1.251	1.243	1.261	1.300	V
VOUT4	+41.25	-200	1.200	1.251	1.248	1.241	1.259	1.300	V
VRLINE	+4.25 / +41.25	-5	-9.000M	4.411M	4.298M	3.393M	3.959M	9.000M	V
VRLOAD1	+6.25	-5 / -1500	-3.500M	-339.4U	565.5U	-452.4U	0.000	3.500M	V
VRLOAD2	+41.25	-5 / -200	-3.500M	-2.149M	-2.149M	-2.262M	-2.375M	3.500M	V
VRTH (IL APPLIED FOR 20.5Msec.)	+41.25	-500	-5.000M	3.054M	4.298M	1.810M	2.828M	5.000M	V
IADJ1 (LINE)	+4.25	-5	-100.0U	-56.09U	-52.19U	-55.18U	-59.32U	-15.00U	A
IADJ2 (LINE)	+41.25	-5	-100.0U	-56.42U	-52.52U	-55.51U	-59.71U	-15.00U	A
DIADJ1 (LINE)	+4.25 / +41.25	-5	-5.000U	-330.5N	-330.5N	-326.5N	-388.5N	5.000U	A
DIADJ2 (LOAD)	+6.25	-5 / -1500	-5.000U	-108.0N	-166.0N	-114.0N	-160.0N	5.000U	A
IOS1	+4.25	VF=0V	-3.500	-2.580	-3.090	-2.510	-2.815	-1.500	A
(VOUT)	RECOV.		1.200	1.249	1.247	1.239	1.256	1.300	V
IOS2	+40.00	VF=0V	-1.000	-480.0M	-545.0M	-460.0M	-500.0M	-180.0M	A
(VOUT)	RECOV.		1.200	1.253	1.251	1.243	1.260	1.300	V
IPEAK	+4.25	VF=+1.0V	-3.500	-2.540	-2.480	-2.565	-2.300	-1.500	A
(VOUT)	RECOV.		1.200	1.250	1.247	1.239	1.256	1.300	V
IQ1	+4.25	VF=+1.4V	-3.000M	-1.175M	-1.367M	-1.332M	-1.413M	-500.0U	A
IQ2	+14.25	VF=+1.4V	-3.000M	-1.553M	-1.673M	-1.683M	-1.762M	-500.0U	A
IQ3	+41.25	VF=+1.4V	-5.000M	-3.513M	-3.560M	-3.867M	-3.960M	-1.000M	A
VSTART	+4.25	-1500	1.200	1.249	1.246	1.239	1.257	1.300	V

NOTE :1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.17.

POS. ADJ. VOLTAGE REGULATORS-LM117K; TEMPERATURE: -55 DEG C ; 10 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	HI-LIMIT	UNITS
VOUT1	+4.25	-5	1.200	1.245	1.247	1.240	1.243	1.249	1.300	V
VOUT2	+4.25	-1500	1.200	1.246	1.245	1.240	1.241	1.247	1.300	V
VOUT3	+41.25	-5	1.200	1.250	1.249	1.244	1.247	1.252	1.300	V
VOUT4	+41.25	-180	1.200	1.248	1.248	1.242	1.245	1.249	1.300	V
VRLINE	+4.25 / +41.25	-5	-23.00M	3.280M	3.167M	2.828M	4.637M	2.488M	23.00M	V
VRLOAD1	+6.25	-5 / -1500	-12.00M	1.357M	1.244M	1.357M	-452.4U	678.5U	12.00M	V
VRLOAD2	+41.25	-5 / -180	-12.00M	-339.4U	-678.7U	-565.5U	-1.810M	-791.8U	12.00M	V
VRTH (IL APPLIED FOR 20.5Msec.)	+41.25	-500	-5.000M	4.185M	4.864M	4.298M	2.941M	3.167M	5.000M	V
IADJ1 (LINE)	+4.25	-5	-100.0U	-45.08U	-46.29U	-43.88U	-45.11U	-50.42U	-15.00U	A
IADJ2 (LINE)	+41.25	-5	-100.0U	-45.46U	-46.52U	-44.04U	-45.49U	-50.62U	-15.00U	A
DIADJ1 (LINE)	+4.25 / +41.25	-5	-5.000U	-384.5N	-234.5N	-163.0N	-375.5N	-197.0N	5.000U	A
DIADJ2 (LOAD)	+6.25	-5 / -1500	-5.000U	-509.5N	-535.5N	-377.0N	-276.0N	-369.0N	5.000U	A
IOS1 (VOUT)	+4.25 RECOV.	VF=0V	-3.500 / 1.200	-3.040 / 1.247	-2.540 / 1.246	-2.800 / 1.241	-2.645 / 1.241	-2.675 / 1.248	-1.500 / 1.300	A V
IOS2 (VOUT)	+40.00 RECOV.	VF=0V	-1.000 / 1.200	-770.0M / 1.249	-620.0M / 1.249	-635.0M / 1.242	-680.0M / 1.247	-575.0M / 1.251	-180.0M / 1.300	A V
IPEAK (VOUT)	+4.25 RECOV.	VF=+1.0V	-3.500 / 1.200	-2.355 / 1.247	-2.095 / 1.246	-2.385 / 1.240	-2.255 / 1.241	-2.135 / 1.247	-1.500 / 1.300	A V
IQ1	+4.25	VF=+1.4V	-3.000M	-1.075M	-1.130M	-1.000M	-935.0U	-1.122M	-500.0U	A
IQ2	+14.25	VF=+1.4V	-3.000M	-1.525M	-1.602M	-1.295M	-1.428M	-1.463M	-500.0U	A
IQ3	+41.25	VF=+1.4V	-5.000M	-3.752M	-3.793M	-3.222M	-3.613M	-3.707M	-1.000M	A
VSTART	+4.25	-1500	1.200	1.245	1.246	1.240	1.240	1.248	1.300	V

NOTE :1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.17. (cont'd).

POS. ADJ. VOLTAGE REGULATORS-LM117K; TEMPERATURE: -55 DEG C ; 10 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 6	S/N 7	S/N 8	S/N 9	HI-LIMIT	UNITS
VOUT1	+4.25	-5	1.200	1.248	1.247	1.242	1.255	1.300	V
VOUT2	+4.25	-1500	1.200	1.247	1.246	1.240	1.254	1.300	V
VOUT3	+41.25	-5	1.200	1.251	1.250	1.245	1.257	1.300	V
VOUT4	+41.25	-180	1.200	1.249	1.247	1.243	1.256	1.300	V
VRLINE	+4.25 +41.25	-5	-23.00M	3.280M	3.393M	2.828M	2.828M	23.00M	V
VRLOAD1	+6.25	-5 -1500	-12.00M	791.8U	1.697M	113.1U	791.8U	12.00M	V
VRLOAD2	+41.25	-5 -180	-12.00M	-1.018M	-678.7U	-1.357M	-1.244M	12.00M	V
VRTH (IL APPLIED FOR 20.5Msec.)	+41.25	-500	-5.000M	3.167M	4.637M	2.488M	3.167M	5.000M	V
IADJ1 (LINE)	+4.25	-5	-100.0U	-46.55U	-44.22U	-47.35U	-49.68U	-15.00U	A
IADJ2 (LINE)	+41.25	-5	-100.0U	-46.77U	-44.45U	-47.56U	-49.90U	-15.00U	A
DIADJ1 (LINE)	+4.25 +41.25	-5	-5.000U	-225.0N	-225.5N	-209.0N	-226.5N	5.000U	A
DIADJ2 (LOAD)	+6.25	-5 -1500	-5.000U	-320.5N	-389.5N	-286.5N	-371.0N	5.000U	A
IOS1 (VOUT)	+4.25	VF=0V	-3.500	-2.605	-3.155	-2.590	-2.705	-1.500	A
	RECOV.		1.200	1.247	1.247	1.241	1.253	1.300	V
IOS2 (VOUT)	+40.00	VF=0V	-1.000	-730.0M	-795.0M	-790.0M	-690.0M	-180.0M	A
	RECOV.		1.200	1.251	1.250	1.245	1.256	1.300	V
IPEAK (VOUT)	+4.25	VF=+1.0V	-3.500	-2.360	-2.470	-2.610	-2.170	-1.500	A
	RECOV.		1.200	1.246	1.247	1.241	1.253	1.300	V
IQ1	+4.25	VF=+1.4V	-3.000M	-920.0U	-1.113M	-1.082M	-1.095M	-500.0U	A
IQ2	+14.25	VF=+1.4V	-3.000M	-1.380M	-1.458M	-1.480M	-1.520M	-500.0U	A
IQ3	+41.25	VF=+1.4V	-5.000M	-3.445M	-3.440M	-3.940M	-3.780M	-1.000M	A
VSTART	+4.25	-1500	1.200	1.246	1.247	1.241	1.253	1.300	V

NOTE :1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.18.

POS. ADJ. VOLTAGE REGULATORS-LM117K; TEMPERATURE: 125 DEG C ; 10 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	HI-LIMIT	UNITS
VOUT1	+4.25	-5	1.200	1.242	1.243	1.230	1.230	1.240	1.300	V
VOUT2	+4.25	-1500	1.200	1.240	1.242	1.226	1.227	1.236	1.300	V
VOUT3	+41.25	-5	1.200	1.247	1.249	1.233	1.237	1.245	1.300	V
VOUT4	+41.25	-180	1.200	1.243	1.245	1.231	1.234	1.240	1.300	V
VRLINE	+4.25 / +41.25	-5	-23.00M	4.864M	4.864M	4.185M	7.691M	4.864M	23.00M	V
VRLOAD1	+6.25	-5 / -1500	-12.00M	-791.7U	-452.4U	-1.131M	-2.149M	-1.470M	12.00M	V
VRLOAD2	+41.25	-5 / -180	-12.00M	-3.506M	-3.054M	-3.167M	-3.733M	-4.411M	12.00M	V
VRTH (IL APPLIED FOR 20.5Msec.)	+41.25	-500	-5.000M	3.054M	4.637M	2.941M	1.810M	1.584M	5.000M	V
IADJ1 (LINE)	+4.25	-5	-100.0U	-62.27U	-61.78U	-56.11U	-58.65U	-65.02U	-15.00U	A
IADJ2 (LINE)	+41.25	-5	-100.0U	-62.67U	-62.20U	-56.44U	-59.21U	-65.43U	-15.00U	A
DIADJ1 (LINE)	+4.25 / +41.25	-5	-5.000U	-397.0N	-419.0N	-332.0N	-561.5N	-411.0N	5.000U	A
DIADJ2 (LOAD)	+6.25	-5 / -1500	-5.000U	-5.501N	-85.99N	21.50N	104.5N	61.00N	5.000U	A
IOS1 (VOUT)	+4.25 RECOV.	VF=0V	-3.500 1.200	-2.560 1.242	-2.355 1.244	-2.355 1.227	-2.285 1.227	-2.095 1.237	-1.500 1.300	A V
IOS2 (VOUT)	+40.00 RECOV.	VF=0V	-1.000 1.200	-435.0M 1.247	-420.0M 1.249	-410.0M 1.234	-425.0M 1.238	-355.0M 1.245	-180.0M 1.300	A V
IPEAK (VOUT)	+4.25 RECOV.	VF=+1.0V	-3.500 1.200	-2.090 1.241	-1.960 1.244	-1.940 1.228	-1.880 1.228	-1.730 1.237	-1.500 1.300	A V
IQ1	+4.25	VF=+1.4V	-3.000M	-1.545M	-1.568M	-1.413M	-1.207M	-1.645M	-500.0U	A
IQ2	+14.25	VF=+1.4V	-3.000M	-1.860M	-1.890M	-1.650M	-1.563M	-1.905M	-500.0U	A
IQ3	+41.25	VF=+1.4V	-5.000M	-3.690M	-3.750M	-3.318M	-3.368M	-3.860M	-1.000M	A
VSTART	+4.25	-1500	1.200	1.241	1.242	1.227	1.227	1.238	1.300	V

POS. ADJ. VOLTAGE REGULATOKS-LM117K; TEMPERATURE: 150 DEG C ; 10 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	HI-LIMIT	UNITS
VOUT5	-6.25	5	1.200	1.242	1.243	1.229	1.230	1.239	1.300	V

NOTE #1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.18. (cont'd).

POS. ADJ. VOLTAGE REGULATORS-LM117K; TEMPERATURE: 125 DEG C ; 10 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 6	S/N 7	S/N 8	S/N 9	HI LIMIT	UNITS
VOUT1	+4.25	-5	1.200	1.240	1.239	1.229	1.251	1.300	V
VOUT2	+4.25	-1500	1.200	1.239	1.238	1.227	1.247	1.300	V
VOUT3	+41.25	-5	1.200	1.245	1.243	1.233	1.254	1.300	V
VOUT4	+41.25	-180	1.200	1.240	1.240	1.229	1.252	1.300	V
VRLINE	+4.25 +41.25	-5	-23.00M	4.864M	5.429M	4.072M	4.864M	23.00M	V
VRLOAD1	+6.25	-5 -1500	-12.00M	-1.697M	-791.7U	-1.470M	-1.470M	12.00M	V
VRLOAD2	+41.25	-5 -180	-12.00M	-3.393M	-3.393M	-3.167M	-3.846M	12.00M	V
VRTH (IL APPLIED FOR 20.5Msec.)	+41.25	-500	-5.000M	2.602M	3.846M	1.810M	2.036M	5.000M	V
IADJ1 (LINE)	+4.25	-5	-100.0U	-60.31U	-56.22U	-60.10U	-65.18U	-15.00U	A
IADJ2 (LINE)	+41.25	-5	-100.0U	-60.69U	-56.61U	-60.44U	-65.62U	-15.00U	A
DIADJ1 (LINE)	+4.25 +41.25	-5	-5.000U	-383.0N	-388.0N	-343.5N	-438.0N	5.000U	A
DIADJ2 (LOAD)	+6.25	-5 -1500	-5.000U	47.00N	-5.501N	50.00N	22.50N	5.000U	A
IOS1 (VOUT)	+4.25 RECOV.	VF=0V	-3.500 1.200	-2.490 1.239	-2.460 1.238	-2.400 1.227	-2.190 1.248	-1.500 1.300	A V
IOS2 (VOUT)	+40.00 RECOV.	VF=0V	-1.000 1.200	-445.0M 1.244	-510.0M 1.244	-425.0M 1.233	-455.0M 1.255	-180.0M 1.300	A V
IPEAK (VOUT)	+4.25 RECOV.	VF=+1.0V	-3.500 1.200	-2.075 1.239	-2.015 1.237	-2.410 1.227	-1.810 1.247	-1.500 1.300	A V
IQ1	+4.25	VF=+1.4V	-3.000M	-1.322M	-1.517M	-1.490M	-1.595M	-500.0U	A
IQ2	+14.25	VF=+1.4V	-3.000M	-1.620M	-1.780M	-1.785M	-1.882M	-500.0U	A
IQ3	+41.25	VF=+1.4V	-5.000M	-3.380M	-3.478M	-3.650M	-3.828M	-1.000M	A
VSTART	+4.25	-1500	1.200	1.237	1.237	1.227	1.248	1.300	V

POS. ADJ. VOLTAGE REGULATORS-LM117K; TEMPERATURE: 150 DEG C ; 10 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 6	S/N 7	S/N 8	S/N 9	HI-LIMIT	UNITS
VOUT5	-6.25	5	1.200	1.249	1.249	1.249	1.249	1.300	V

NOTE :1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

TABLE 3.19. POS. ADJ. VOLTAGE REGULATOR - LM117K T_A = 25°C 6-15-79

PARAMETER	CONDITIONS	LO - LIMIT	S/N1	S/N2	S/N3	S/N4	S/N5	HI - LIMIT	UNITS
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN} = 6.25V e_i = 1 V_{RMS} @ 2400 Hz I_L = -500 mA	65	> 80	> 80	> 80	> 80	> 80	-	dB
V_{NO}	V_{IN} = 6.25V I_L = -100 mA	-	105	105	100	105	105	120	uV_{RMS}
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN} = 6.25V ΔV_{IN} = 3.0 V I_L = -10 mA	-	1.6	1.6	2.0	1.6	1.6	6	mV/V
$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN} = 6.25V I_L = -100 mA ΔI_L = -400 mA	-	.13	.13	.13	.14	.13	0.3	mV/mA

Table 3.19. POS. ADJ. VOLTAGE REGULATOR - LM117K T_A = 25°C 6-15-79 (cont'd).

PARAMETER	CONDITIONS	LO - LIMIT	S/N6	S/N7	S/N8	S/N9	-	HI - LIMIT	UNITS
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN} = 6.25V e_i = 1 V_{RMS} @ 2400 Hz I_L = -500 mA	65	> 80	> 80	> 80	> 80	-	-	dB
V_{NO}	V_{IN} = 6.25 V I_L = -100 mA	-	105	100	105	100	-	120	uV_{RMS}
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN} = 6.25 V ΔV_{IN} = 3.0 V I_L = - 10 mA	-	1.6	1.6	1.6	2.0	-	6	mV/V
$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN} = 6.25 V I_L = -100 mA ΔI_L = -400 mA	-	.14	.14	.13	.13	-	0.3	mV/mA

Table. 3.20.

NEG. ADJ. VOLTAGE REGULATORS-LM137H; TEMPERATURE: 25 DEG C ; 01 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	HI-LIMIT	UNITS
VOUT1	-4.25	5	-1.275	-1.252	-1.253	-1.252	-1.244	-1.249	-1.225	V
VOUT2	-4.25	500	-1.275	-1.240	-1.242	-1.242	-1.233	-1.238	-1.225	V
VOUT3	-41.25	5	-1.275	-1.255	-1.256	-1.255	-1.247	-1.252	-1.225	V
VOUT4	-41.25	50	-1.275	-1.255	-1.253	-1.254	-1.247	-1.250	-1.225	V
VRLINE	-4.25 -41.25	5	-9.000M	-2.715M	-2.262M	-2.262M	-2.375M	-2.375M	9.000M	V
VRLOAD1	-6.25	5 500	-6.000M	12.33M*	10.63M*	10.18M*	12.78M*	11.65M*	6.000M	V
VRLOAD2	-41.25	5 50	-6.000M	1.244M	1.018M	1.131M	1.018M	904.9U	6.000M	V
VRTH (IL APPLIED FOR 10.5Msec.)	-14.60	750	-5.000M	452.5U	339.3U	565.5U	339.3U	678.5U	5.000M	V
IADJ1 (LINE)	-4.25	5	25.00U	71.94U	64.68U	64.72U	74.77U	70.91U	100.0U	A
IADJ2 (LINE)	-41.25	5	25.00U	75.33U	67.38U	67.43U	78.07U	74.28U	100.0U	A
DIADJ1 (LINE)	-4.25 -41.25	5	-5.000U	3.396U	2.697U	2.709U	3.301U	3.369U	5.000U	A
DIADJ2 (LOAD)	-6.25	5 500	-5.000U	-1.256U	-937.0N	-1.017U	-1.153U	-1.103U	5.000U	A
IOS1	-4.25	VF=0V	500.0M	1.150	1.235	1.235	1.215	1.185	1.800	A
(VOUT) RECOV.			-1.275	-1.240	-1.242	-1.243	-1.232	-1.237	-1.225	V
IOS2	-40.00	VF=0V	50.00M	290.0M	365.0M	365.0M	310.0M	325.0M	500.0M	A
(VOUT) RECOV.			-1.275	-1.254	-1.254	-1.255	-1.247	-1.250	-1.225	V
IPEAK	-4.25	VF=-1.0V	500.0M	1.155	1.240	1.240	1.220	1.190	1.800	A
(VOUT) RECOV.			-1.275	-1.241	-1.243	-1.243	-1.232	-1.238	-1.225	V
IQ1	-4.25	VF=-1.4V	200.0U	400.0U	400.0U	400.0U	448.0U	432.0U	3.000M	A
IQ2	-14.25	VF=-1.4V	200.0U	480.0U	448.0U	464.0U	510.0U	508.0U	3.000M	A
IQ3	-41.25	VF=-1.4V	1.000M	1.980M	1.800M	1.800M	2.090M	2.020M	5.000M	A
VSTART	-4.25	500	-1.275	-1.241	-1.242	-1.243	-1.233	-1.238	-1.200	V

NOTE #1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.20. (cont'd).

NEG. ADJ. VOLTAGE REGULATORS-LM137H; TEMPERATURE: 25 DEG C ; 01 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 6	S/N 7	S/N 8	S/N 9	S/N 10	HI LIMIT	UNITS
VOUT1	-4.25	5	-1.275	-1.259	-1.254	-1.251	-1.254	-1.253	-1.225	V
VOUT2	-4.25	500	-1.275	-1.247	-1.243	-1.240	-1.243	-1.243	-1.225	V
VOUT3	-41.25	5	-1.275	-1.261	-1.256	-1.253	-1.256	-1.257	-1.225	V
VOUT4	-41.25	50	-1.275	-1.260	-1.256	-1.252	-1.255	-1.255	-1.225	V
VRLINE	-4.25 -41.25	5	-9.000M	-2.262M	-2.488M	-2.375M	-2.715M	-2.941M	9.000M	V
VRLOAD1	-6.25	5 500	-6.000M	11.20M*	10.18M*	12.33M*	11.65M*	10.97M*	6.000M	V
VRLOAD2	-41.25	5 50	-6.000M	904.8U	791.8U	1.244M	1.244M	904.8U	6.000M	V
VRTH (IL APPLIED FOR 10.5Msec.)	-14.60	750	-5.000M	226.1U	339.4U	791.8U	565.5U	0.000	5.000M	V
IADJ1 (LINE)	-4.25	5	25.00U	67.27U	68.99U	69.70U	63.47U	69.99U	100.0U	A
IADJ2 (LINE)	-41.25	5	25.00U	69.88U	72.39U	72.50U	65.99U	73.45U	100.0U	A
DIADJ1 (LINE)	-4.25 -41.25	5	-5.000U	2.619U	3.406U	2.796U	2.514U	3.451U	5.000U	A
DIADJ2 (LOAD)	-6.25	5 500	-5.000U	-1.086U	-1.178U	-1.098U	-976.5N	-1.095U	5.000U	A
IOS1 (VOUT) RECOV.	-4.25	VF=0V	500.0M -1.275	1.235 -1.249	1.245 -1.243	1.245 -1.239	1.235 -1.243	1.180 -1.243	1.800 -1.225	A V
IOS2 (VOUT) RECOV.	-40.00	VF=0V	50.00M -1.275	350.0M -1.262	350.0M -1.255	360.0M -1.253	360.0M -1.256	325.0M -1.256	500.0M -1.225	A V
IPEAK (VOUT) RECOV.	-4.25	VF=-1.0V	500.0M -1.275	1.240 -1.248	1.250 -1.243	1.250 -1.239	1.240 -1.242	1.185 -1.243	1.800 -1.225	A V
IQ1	-4.25	VF=-1.4V	200.0U	416.0U	384.0U	416.0U	384.0U	400.0U	3.000M	A
IQ2	-14.25	VF=-1.4V	200.0U	480.0U	456.0U	496.0U	456.0U	480.0U	3.000M	A
IQ3	-41.25	VF=-1.4V	1.000M	1.880M	1.920M	1.940M	1.760M	1.940M	5.000M	A
VSTART	-4.25	500	-1.275	-1.248	-1.243	-1.240	-1.243	-1.243	-1.200	V

NOTE *: VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.21.

NEG. ADJ. VOLTAGE REGULATORS-LM137H; TEMPERATURE: -55 DEG C ; 01 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(mA)	LO-LIMIT	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	HI LIMIT	UNITS
VOUT1	-4.25	5	-1.300	-1.252	-1.254	-1.244	-1.249	-1.258	-1.200	V
VOUT2	-4.25	500	-1.300	-1.243	-1.245	-1.234	-1.240	-1.249	-1.200	V
VOUT3	-41.25	5	-1.300	-1.256	-1.256	-1.247	-1.253	-1.262	-1.200	V
VOUT4	-41.25	50	-1.300	-1.256	-1.255	-1.247	-1.253	-1.261	-1.200	V
VRLINE	-4.25 / -41.25	5	-23.00M	-4.637M	-2.828M	-3.959M	-4.637M	-3.733M	23.00M	V
VRLOAD1	-6.25	5 / 500	-12.00M	9.275M	8.257M	10.07M	8.257M	7.578M	12.00M	V
VRLOAD2	-41.25	5 / 50	-12.00M	791.8U	678.7U	1.131M	1.357M	1.244M	12.00M	V
VRTH (IL APPLIED FOR 10.5Msec.)	-14.60	750	-5.000M	-226.3U	0.000	452.4U	-565.5U	-791.8U	5.000M	V
IADJ1 (LINE)	-4.25	5	25.00U	76.92U	67.77U	78.46U	76.05U	72.36U	100.0U	A
IADJ2 (LINE)	-41.25	5	25.00U	80.40U	70.50U	81.88U	79.49U	75.00U	100.0U	A
DIADJ1 (LINE)	-4.25 / -41.25	5	-5.000U	3.476U	2.729U	3.423U	3.444U	2.635U	5.000U	A
DIADJ2 (LOAD)	-6.25	5 / 500	-5.000U	-1.604U	-1.499U	-1.680U	-1.504U	-1.516U	5.000U	A
IOS1 (VOUT) RECOV.	-4.25	VF=0V	500.0M / -1.300	1.120 / -1.243	1.225 / -1.245	1.200 / -1.234	1.160 / -1.240	1.220 / -1.250	1.800 / -1.200	A / V
IOS2 (VOUT) RECOV.	-40.00	VF=0V	50.00M / -1.300	340.0M / -1.256	405.0M / -1.255	350.0M / -1.248	375.0M / -1.253	415.0M / -1.262	500.0M / -1.200	A / V
IPEAK (VOUT) RECOV.	-4.25	VF=-1.0V	500.0M / -1.300	1.125 / -1.243	1.230 / -1.245	1.210 / -1.234	1.170 / -1.240	1.230 / -1.249	1.800 / -1.200	A / V
IQ1	-4.25	VF=-1.4V	200.0U	288.0U	320.0U	352.0U	320.0U	304.0U	3.000M	A
IQ2	-14.25	VF=-1.4V	200.0U	416.0U	400.0U	448.0U	416.0U	400.0U	3.000M	A
IQ3	-41.25	VF=-1.4V	1.000M	2.000M	1.840M	2.120M	2.013M	1.920M	5.000M	A
VSTART	-4.25	500	-1.300	-1.243	-1.245	-1.235	-1.240	-1.249	-1.200	V

NOTE :1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.21. (cont'd).

NEG. ADJ. VOLTAGE REGULATORS-LM137H; TEMPERATURE: -55 DEG C ; 01 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 6	S/N 7	S/N 8	S/N 9	S/N 10	HI-LIMIT	UNITS
VOUT1	-4.25	5	-1.300	-1.255	-1.253	-1.255	-1.254	-1.255	-1.200	V
VOUT2	-4.25	500	-1.300	-1.247	-1.244	-1.247	-1.245	-1.247	-1.200	V
VOUT3	-41.25	5	-1.300	-1.258	-1.256	-1.258	-1.258	-1.259	-1.200	V
VOUT4	-41.25	50	-1.300	-1.258	-1.256	-1.258	-1.256	-1.258	-1.200	V
VRLINE	-4.25 -41.25	5	-23.00M	-4.185M	-3.619M	-3.167M	-3.393M	-4.298M	23.00M	V
VRLOAD1	-6.25	5 500	-12.00M	7.691M	8.935M	9.049M	8.709M	8.596M	12.00M	V
VRLOAD2	-41.25	5 50	-12.00M	1.018M	678.5U	791.8U	565.5U	1.018M	12.00M	V
VRTH (IL APPLIED FOR 10.5Msec.)	-14.60	750	-5.000M	-113.1U	226.3U	0.000	-339.4U	113.1U	5.000M	V
IADJ1 (LINE)	-4.25	5	25.00U	73.74U	74.95U	67.67U	73.98U	79.14U	100.0U	A
IADJ2 (LINE)	-41.25	5	25.00U	77.32U	77.81U	70.22U	77.56U	82.87U	100.0U	A
DIADJ1 (LINE)	-4.25 -41.25	5	-5.000U	3.581U	2.859U	2.553U	3.582U	3.722U	5.000U	A
DIADJ2 (LOAD)	-6.25	5 500	-5.000U	-1.692U	-1.523U	-1.430U	-1.650U	-1.580U	5.000U	A
IOS1 (VOUT)	-4.25 RECOV.	VF=0V	500.0M -1.300	1.220 -1.248	1.220 -1.245	1.225 -1.247	1.160 -1.245	1.170 -1.247	1.800 -1.200	A V
IOS2 (VOUT)	-40.00 RECOV.	VF=0V	50.00M -1.300	400.0M -1.260	425.0M -1.256	420.0M -1.258	365.0M -1.257	375.0M -1.258	500.0M -1.200	A V
IPEAK (VOUT)	-4.25 RECOV.	VF=-1.0V	500.0M -1.300	1.235 -1.248	1.235 -1.245	1.235 -1.247	1.170 -1.245	1.180 -1.247	1.800 -1.200	A V
IQ1	-4.25	VF=-1.4V	200.0U	304.0U	320.0U	304.0U	304.0U	336.0U	3.000M	A
IQ2	-14.25	VF=-1.4V	200.0U	384.0U	416.0U	400.0U	400.0U	424.0U	3.000M	A
IQ3	-41.25	VF=-1.4V	1.000M	1.940M	1.960M	1.805M	1.965M	2.080M	5.000M	A
VSTART	-4.25	500	-1.300	-1.247	-1.244	-1.246	-1.246	-1.248	-1.200	V

NOTE :1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.22.

NEG. ADJ. VOLTAGE REGULATORS-LM137H; TEMPERATURE: 125 DEG C ; 01 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	HI-LIMIT	UNITS
VOUT1	-4.25	5	-1.300	-1.255	-1.255	-1.247	-1.249	-1.264	-1.200	V
VOUT2	-4.25	500	-1.300	-1.240	-1.243	-1.232	-1.234	-1.249	-1.200	V
VOUT3	-41.25	5	-1.300	-1.257	-1.257	-1.249	-1.251	-1.267	-1.200	V
VOUT4	-41.25	50	-1.300	-1.255	-1.255	-1.246	-1.251	-1.265	-1.200	V
VRLINE	-4.25 -41.25	5	-23.00M	-2.602M	-1.810M	-1.810M	-1.470M	-2.149M	23.00M	V
VRLOAD1	-6.25	5 500	-12.00M	16.17M‡	12.67M‡	16.06M‡	15.61M‡	16.17M‡	12.00M	V
VRLOAD2	-41.25	5 50	-12.00M	1.583M	1.131M	1.357M	1.810M	2.149M	12.00M	V
VRTH (IL APPLIED FOR 10.5Msec.)	-14.60	750	-5.000M	565.5U	904.9U	1.018M	1.018M	1.131M	5.000M	V
IADJ1 (LINE)	-4.25	5	25.00U	76.33U	68.36U	79.38U	75.98U	72.31U	100.0U	A
IADJ2 (LINE)	-41.25	5	25.00U	79.30U	70.92U	82.50U	79.06U	74.73U	100.0U	A
DIADJ1 (LINE)	-4.25 -41.25	5	-5.000U	2.971U	2.554U	3.120U	3.075U	2.421U	5.000U	A
DIADJ2 (LOAD)	-6.25	5 500	-5.000U	-604.5N	-513.0N	-632.5N	-558.0N	-576.5N	5.000U	A
IOS1 (VOUT)	-4.25 RECOV.	VF=0V	500.0M -1.300	1.145 -1.240	1.220 -1.243	1.200 -1.232	1.170 -1.235	1.210 -1.249	1.800 -1.200	A V
IOS2 (VOUT)	-40.00 RECOV.	VF=0V	50.00M -1.300	275.0M -1.257	345.0M -1.256	300.0M -1.248	315.0M -1.251	325.0M -1.267	500.0M -1.200	A V
IPEAK (VOUT)	-4.25 RECOV.	VF=-1.0V	500.0M -1.300	1.145 -1.240	1.220 -1.243	1.205 -1.232	1.170 -1.234	1.205 -1.249	1.800 -1.200	A V
IQ1	-4.25	VF=-1.4V	200.0U	480.0U	448.0U	508.0U	496.0U	464.0U	3.000M	A
IQ2	-14.25	VF=-1.4V	200.0U	522.5U	496.0U	511.5U	540.0U	520.0U	3.000M	A
IQ3	-41.25	VF=-1.4V	1.000M	1.840M	1.688M	1.980M	1.857M	1.722M	5.000M	A
VSTART	-4.25	500	-1.300	-1.240	-1.243	-1.232	-1.236	-1.249	-1.200	V

NEG. ADJ. VOLTAGE REGULATORS-LM137H; TEMPERATURE: 150 DEG C ; 01 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	HI-LIMIT	UNITS
VOUT5	-6.25	5	-1.300	-1.255	-1.256	-1.246	-1.250	-1.266	-1.200	V

NOTE ‡1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.22. (cont'd).

NEG. ADJ. VOLTAGE REGULATORS-LM137H; TEMPERATURE: 125 DEG C ; 01 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 6	S/N 7	S/N 8	S/N 9	S/N 10	HI LIMIT	UNITS
VOUT1	-4.25	5	-1.300	-1.254	-1.251	-1.255	-1.256	-1.255	-1.200	V
VOUT2	-4.25	500	-1.300	-1.242	-1.236	-1.241	-1.243	-1.240	-1.200	V
VOUT3	-41.25	5	-1.300	-1.256	-1.252	-1.256	-1.259	-1.256	-1.200	V
VOUT4	-41.25	50	-1.300	-1.256	-1.252	-1.255	-1.258	-1.255	-1.200	V
VRLINE	-4.25 -41.25	5	-23.00M	-1.923M	-1.697M	-1.697M	-2.262M	-2.036M	23.00M	V
VRLOAD1	-6.25	5 500	-12.00M	13.35M*	16.51M*	15.27M*	14.14M*	14.93M*	12.00M	V
VRLOAD2	-41.25	5 50	-12.00M	1.470M	1.470M	1.357M	1.697M	1.923M	12.00M	V
VRTH (IL APPLIED FOR 10.5Msec.)	-14.60	750	-5.000M	791.8U	1.018M	1.018M	678.7U	678.7U	5.000M	V
IADJ1 (LINE)	-4.25	5	25.00U	72.52U	74.44U	67.07U	74.24U	79.34U	100.0U	A
IADJ2 (LINE)	-41.25	5	25.00U	75.56U	76.99U	69.36U	77.42U	82.60U	100.0U	A
DIADJ1 (LINE)	-4.25 -41.25	5	-5.000U	3.033U	2.551U	2.291U	3.182U	3.262U	5.000U	A
DIADJ2 (LOAD)	-6.25	5 500	-5.000U	-642.0N	-572.5N	-506.0N	-605.5N	-600.5N	5.000U	A
IOS1	-4.25	VF=0V	500.0M	1.230	1.220	1.215	1.165	1.175	1.800	A
(VOUT)	RECOV.		-1.300	-1.242	-1.237	-1.240	-1.243	-1.240	-1.200	V
IOS2	-40.00	VF=0V	50.00M	330.0M	335.0M	330.0M	315.0M	310.0M	500.0M	A
(VOUT)	RECOV.		-1.300	-1.257	-1.252	-1.256	-1.258	-1.256	-1.200	V
IPEAK	-4.25	VF=-1.0V	500.0M	1.235	1.220	1.215	1.170	1.175	1.800	A
(VOUT)	RECOV.		-1.300	-1.242	-1.237	-1.240	-1.243	-1.240	-1.200	V
IQ1	-4.25	VF=-1.4V	200.0U	448.0U	496.0U	448.0U	448.0U	504.0U	3.000M	A
IQ2	-14.25	VF=-1.4V	200.0U	504.0U	540.0U	504.0U	510.0U	560.0U	3.000M	A
IQ3	-41.25	VF=-1.4V	1.000M	1.760M	1.800M	1.640M	1.840M	1.925M	5.000M	A
VSTART	-4.25	500	-1.300	-1.242	-1.236	-1.242	-1.242	-1.241	-1.200	V

NEG. ADJ. VOLTAGE REGULATORS-LM137H; TEMPERATURE: 150 DEG C ; 01 MAY 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 6	S/N 7	S/N 8	S/N 9	S/N 10	HI-LIMIT	UNITS
VOUT5	-6.25	5	-1.300	-1.255	-1.255	-1.255	-1.255	-1.255	-1.200	V

NOTE *1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

TABLE 3.23. NEG. ADJ. VOLTAGE REGULATOR - LM137H T_A = 25°C 6-16-79

PARAMETER	CONDITONS	LO - LIMIT	S/N1	S/N2	S/N3	S/N4	S/N5	HI - LIMIT	UNITS
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN} = -6.25V e_i = 1 V_{RMS} @ 2400 Hz I_L = 125 mA	48	60.0	57.7	60	59.2	57.7	-	dB
V_{NO}	V_{IN} = -6.25V I_L = 50 mA	-	70	70	70	70	70	120	uV_{RMS}
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN} = -6.25V ΔV_{IN} = -1.0V I_L = 10 mA	-	30	36	35	30	38	80	mV/V
$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN} = -6.25V I_L = 50 mA ΔI_L = 200 mA	-	.05	.05	.04	.045	.05	0.3	mV/mA

Table 3.23. NEG. ADJ. VOLTAGE REGULATOR - LM137H T_A = 25°C 6-15-79 (cont'd).

PARAMETER	CONDITIONS	LO - LIMIT	S/N6	S/N7	S/N8	S/N9	S/N10	HI - LIMIT	UNITS
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN} = -6.25V e_i = 1 V_{RMS} @ 2400 Hz I_L = 125 mA	48	57.4	58.4	57.0	59.2	60.0	-	dB
V_{NO}	V_{IN} = -6.25V I_L = 50 mA	-	70	70	70	70	70	120	uV_{RMS}
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN} = -6.25V ΔV_{IN} = -1.0V I_L = 10 mA	-	36	35	28	30	28	80	mV/V
$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN} = -6.25 V I_L = 50 mA ΔI_L = 200 mA	-	.05	.05	.05	.04	.05	0.3	mV/mA

Table 3.24.

NEG. ADJ. VOLTAGE REGULATORS-LM137K; TEMPERATURE: 25 DEG C ; 30 APR 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 4	S/N 5	S/N 6	HI-LIMIT	UNITS
VOUT1	-4.25	5	-1.275	-1.254	-1.259	-1.267	-1.257	-1.256	-1.225	V
VOUT2	-4.25	1500	-1.275	-1.249	-1.254	-1.261	-1.252	-1.252	-1.225	V
VOUT3	-41.25	5	-1.275	-1.257	-1.261	-1.268	-1.259	-1.258	-1.225	V
VOUT4	-41.25	250	-1.275	-1.256	-1.260	-1.268	-1.258	-1.258	-1.225	V
VRLINE	-4.25 -41.25	5	-9.000M	-3.506M	-2.149M	-1.923M	-2.149M	-2.715M	9.000M	V
VRLOAD1	-6.25	5 1500	-6.000M	4.524M	4.864M	4.977M	5.090M	4.185M	6.000M	V
VRLOAD2	-41.25	5 250	-6.000M	1.018M	339.4U	791.8U	1.131M	452.4U	6.000M	V
VRTH (IL APPLIED FOR 10.5Msec.)	-14.60	1500	-5.000M	565.5U	1.131M	1.018M	1.470M	791.7U	5.000M	V
IADJ1 (LINE)	-4.25	5	25.00U	73.08U	67.70U	64.52U	62.90U	60.14U	100.0U	A
IADJ2 (LINE)	-41.25	5	25.00U	76.62U	70.51U	67.09U	65.47U	63.50U	100.0U	A
DIADJ1 (LINE)	-4.25 -41.25	5	-5.000U	3.541U	2.814U	2.572U	2.570U	3.358U	5.000U	A
DIADJ2 (LOAD)	-6.25	5 1500	-5.000U	-669.5N	-508.0N	-272.0N	-538.5N	-510.0N	5.000U	A
IOS1	-4.25	VF=0V	1.500	2.190	2.255	2.500	2.320	2.230	3.500	A
(VOUT) RECOV.			-1.275	-1.250	-1.253	-1.260	-1.253	-1.253	-1.225	V
IOS2	-40.00	VF=0V	200.0M	560.0M	570.0M	730.0M	590.0M	620.0M	800.0M	A
(VOUT) RECOV.			-1.275	-1.256	-1.260	-1.268	-1.258	-1.258	-1.225	V
IPEAK	-4.25	VF=-1.0V	1.500	2.245	2.300	2.530	2.365	2.285	3.500	A
(VOUT) RECOV.			-1.275	-1.250	-1.253	-1.260	-1.251	-1.253	-1.225	V
IQ1	-4.25	VF=-1.4V	200.0U	540.0U	400.0U	416.0U	352.0U	400.0U	3.000M	A
IQ2	-14.25	VF=-1.4V	200.0U	960.0U	480.0U	480.0U	448.0U	560.0U	3.000M	A
IQ3	-41.25	VF=-1.4V	1.000M	2.882M	1.920M	1.800M	1.720M	2.080M	5.000M	A
VSTART	-4.25	1500	-1.275	-1.250	-1.253	-1.260	-1.252	-1.253	-1.200	V

NOTE #1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.24. (cont'd).

NEG. ADJ. VOLTAGE REGULATORS-LM137K; TEMPERATURE: 25 DEG C ; 30 APR 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 7	S/N 8	S/N 9	HI-LIMIT	UNITS
VOUT1	-4.25	5	-1.275	-1.258	-1.241	-1.250	-1.225	V
VOUT2	-4.25	1500	-1.275	-1.253	-1.236	-1.245	-1.225	V
VOUT3	-41.25	5	-1.275	-1.258	-1.243	-1.252	-1.225	V
VOUT4	-41.25	250	-1.275	-1.258	-1.243	-1.252	-1.225	V
VRLINE	-4.25 -41.25	5	-9.000M	-2.828M	-2.601M	-1.470M	9.000M	V
VRLOAD1	-6.25	5 1500	-6.000M	4.750M	4.637M	4.750M	6.000M	V
VRLOAD2	-41.25	5 250	-6.000M	113.1U	1.244M	904.8U	6.000M	V
VRTH (IL APPLIED FOR 10.5Msec.)	-14.60	1500	-5.000M	791.7U	1.357M	1.131M	5.000M	V
IADJ1 (LINE)	-4.25	5	25.00U	70.72U	67.75U	67.39U	100.0U	A
IADJ2 (LINE)	-41.25	5	25.00U	73.62U	71.09U	70.31U	100.0U	A
DIADJ1 (LINE)	-4.25 -41.25	5	-5.000U	2.900U	3.343U	2.922U	5.000U	A
DIADJ2 (LOAD)	-6.25	5 1500	-5.000U	-538.5N	-598.5N	-518.0N	5.000U	A
IOS1	-4.25	UF=0V	1.500	2.345	2.275	2.240	3.500	A
(VOUT) RECOV.			-1.275	-1.252	-1.237	-1.244	-1.225	V
IOS2	-40.00	UF=0V	200.0M	600.0M	635.0M	605.0M	800.0M	A
(VOUT) RECOV.			-1.275	-1.259	-1.243	-1.253	-1.225	V
IPEAK	-4.25	UF=-1.0V	1.500	2.390	2.320	2.285	3.500	A
(VOUT) RECOV.			-1.275	-1.252	-1.237	-1.245	-1.225	V
IQ1	-4.25	UF=-1.4V	200.0U	416.0U	384.0U	400.0U	3.000M	A
IQ2	-14.25	UF=-1.4V	200.0U	510.0U	496.0U	496.0U	3.000M	A
IQ3	-41.25	UF=-1.4V	1.000M	1.982M	1.968M	1.920M	5.000M	A
VSTART	-4.25	1500	-1.275	-1.253	-1.236	-1.245	-1.200	V

NOTE #1 UF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.25.

NEG. ADJ. VOLTAGE REGULATORS-LM137K; TEMPERATURE: -55 DEG C ; 30 APR 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 4	S/N 5	S/N 6	HI-LIMIT	UNITS
VOUT1	-4.25	5	-1.300	-1.249	-1.254	-1.255	-1.253	-1.256	-1.200	V
VOUT2	-4.25	1500	-1.300	-1.244	-1.251	-1.253	-1.249	-1.255	-1.200	V
VOUT3	-41.25	5	-1.300	-1.254	-1.256	-1.259	-1.256	-1.262	-1.200	V
VOUT4	-41.25	200	-1.300	-1.254	-1.257	-1.258	-1.256	-1.262	-1.200	V
VRLINE	-4.25 -41.25	5	-23.00M	-5.882M	-3.167M	-3.167M	-2.828M	-3.733M	23.00M	V
VRLOAD1	-6.25	5 1500	-12.00M	3.393M	2.941M	2.488M	3.393M	3.619M	12.00M	V
VRLOAD2	-41.25	5 200	-12.00M	678.7U	452.4U	452.4U	791.7U	113.0U	12.00M	V
VRTH (IL APPLIED FOR 10.5Msec.)	-14.60	1500	-5.000M	-678.7U	-339.4U	0.000	113.0U	452.5U	5.000M	V
IADJ1 (LINE)	-4.25	5	25.00U	77.53U	71.94U	67.80U	66.24U	65.08U	100.0U	A
IADJ2 (LINE)	-41.25	5	25.00U	81.08U	75.02U	70.86U	69.14U	69.32U	100.0U	A
DIADJ1 (LINE)	-4.25 -41.25	5	-5.000U	3.551U	3.081U	3.062U	2.901U	4.241U	5.000U	A
DIADJ2 (LOAD)	-6.25	5 1500	-5.000U	-799.5N	-873.5N	-668.0N	-988.5N	-765.0N	5.000U	A
IOS1	-4.25	VF=0V	1.500	1.945	2.220	2.475	2.275	2.195	3.500	A
(VOUT) RECOV.			-1.300	-1.245	-1.249	-1.253	-1.248	-1.257	-1.200	V
IOS2	-40.00	VF=0V	200.0M	705.0M	690.0M	875.0M*	700.0M	730.0M	800.0M	A
(VOUT) RECOV.			-1.300	-1.254	-1.257	-1.258	-1.256	-1.262	-1.200	V
IPEAK	-4.25	VF=-1.0V	1.500	1.850	2.115	2.515	2.330	2.225	3.500	A
(VOUT) RECOV.			-1.300	-1.245	-1.249	-1.253	-1.248	-1.256	-1.200	V
IQ1	-4.25	VF=-1.4V	200.0U	480.0U	320.0U	320.0U	272.0U	320.0U	3.000M	A
IQ2	-14.25	VF=-1.4V	200.0U	920.0U	416.0U	368.0U	384.0U	520.0U	3.000M	A
IQ3	-41.25	VF=-1.4V	1.000M	3.000M	2.005M	1.870M	1.787M	2.200M	5.000M	A
VSTART	-4.25	1500	-1.300	-1.245	-1.250	-1.252	-1.249	-1.257	-1.200	V

NOTE F1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

NEG. ADJ. VOLTAGE REGULATORS-LM137K; TEMPERATURE: -55 DEG C ; 30 APR 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 7	S/N 8	S/N 9	HI-LIMIT	UNITS
VOUT1	-4.25	5	-1.300	-1.253	-1.242	-1.248	-1.200	V
VOUT2	-4.25	1500	-1.300	-1.249	-1.238	-1.244	-1.200	V
VOUT3	-41.25	5	-1.300	-1.255	-1.245	-1.251	-1.200	V
VOUT4	-41.25	200	-1.300	-1.255	-1.245	-1.250	-1.200	V
VRLINE	-4.25 -41.25	5	-23.00M	-2.828M	-4.072M	-3.280M	23.00M	V
VRLOAD1	-6.25	5 1500	-12.00M	2.941M	3.280M	3.506M	12.00M	V
VRLOAD2	-41.25	5 200	-12.00M	452.4U	452.5U	904.8U	12.00M	V
VRTH (IL APPLIED FOR 10.5Msec.)	-14.60	1500	-5.000M	113.1U	565.5U	226.3U	5.000M	V
IADJ1 (LINE)	-4.25	5	25.00U	74.67U	73.12U	71.41U	100.0U	A
IADJ2 (LINE)	-41.25	5	25.00U	77.87U	76.71U	74.84U	100.0U	A
DIADJ1 (LINE)	-4.25 -41.25	5	-5.000U	3.201U	3.583U	3.426U	5.000U	A
DIADJ2 (LOAD)	-6.25	5 1500	-5.000U	-866.0N	-847.0N	-851.5N	5.000U	A
IOS1	-4.25	VF=0V	1.500	2.320	2.270	2.225	3.500	A
(VOUT) RECOV.			-1.300	-1.247	-1.238	-1.245	-1.200	V
IOS2	-40.00	VF=0V	200.0M	720.0M	755.0M	715.0M	800.0M	A
(VOUT) RECOV.			-1.300	-1.255	-1.245	-1.250	-1.200	V
IPEAK	-4.25	VF=-1.0V	1.500	2.300	2.010	2.190	3.500	A
(VOUT) RECOV.			-1.300	-1.247	-1.239	-1.244	-1.200	V
IQ1	-4.25	VF=-1.4V	200.0U	320.0U	320.0U	320.0U	3.000M	A
IQ2	-14.25	VF=-1.4V	200.0U	432.0U	424.0U	424.0U	3.000M	A
IQ3	-41.25	VF=-1.4V	1.000M	2.023M	2.040M	1.930M	5.000M	A
VSTART	-4.25	1500	-1.300	-1.249	-1.239	-1.244	-1.200	V

NOTE :1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.26.

NEG. ADJ. VOLTAGE REGULATORS-LM137K; TEMPERATURE: 125 DEG C ; 30 APR 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 4	S/N 5	S/N 6	HI-LIMIT	UNITS
VOUT1	-4.25	5	-1.300	-1.260	-1.264	-1.270	-1.258	-1.256	-1.200	V
VOUT2	-4.25	1500	-1.300	-1.253	-1.256	-1.264	-1.251	-1.250	-1.200	V
VOUT3	-41.25	5	-1.300	-1.262	-1.265	-1.272	-1.260	-1.258	-1.200	V
VOUT4	-41.25	200	-1.300	-1.261	-1.263	-1.272	-1.259	-1.258	-1.200	V
VRLINE	-4.25 -41.25	5	-23.00M	-2.941M	-2.262M	-2.036M	-2.036M	-1.697M	23.00M	V
VRLOAD1	-6.25	5 1500	-12.00M	7.013M	6.900M	7.013M	7.465M	6.447M	12.00M	V
VRLOAD2	-41.25	5 200	-12.00M	1.357M	904.8U	1.131M	1.244M	1.018M	12.00M	V
VRTH (IL APPLIED FOR 10.5Msec.)	-14.60	1500	-5.000M	565.5U	1.583M	1.470M	1.923M	1.583M	5.000M	V
IADJ1 (LINE)	-4.25	5	25.00U	77.88U	72.68U	68.61U	66.71U	63.20U	100.0U	A
IADJ2 (LINE)	-41.25	5	25.00U	81.05U	75.33U	71.38U	69.32U	66.14U	100.0U	A
DIADJ1 (LINE)	-4.25 -41.25	5	-5.000U	3.169U	2.653U	2.762U	2.617U	2.940U	5.000U	A
DIADJ2 (LOAD)	-6.25	5 1500	-5.000U	-262.5N	-315.0N	-196.0N	-442.0N	-274.5N	5.000U	A
IOS1	-4.25	VF=0V	1.500	2.120	2.155	2.390	2.080	2.120	3.500	A
(VOUT) RECOV.			-1.300	-1.253	-1.256	-1.265	-1.251	-1.250	-1.200	V
IOS2	-40.00	VF=0V	200.0M	490.0M	510.0M	690.0M	550.0M	570.0M	800.0M	A
(VOUT) RECOV.			-1.300	-1.262	-1.264	-1.272	-1.260	-1.258	-1.200	V
IPEAK	-4.25	VF=-1.0V	1.500	2.125	2.045	2.245	2.045	2.145	3.500	A
(VOUT) RECOV.			-1.300	-1.254	-1.256	-1.265	-1.251	-1.251	-1.200	V
IQ1	-4.25	VF=-1.4V	200.0U	560.0U	448.0U	448.0U	416.0U	416.0U	3.000M	A
IQ2	-14.25	VF=-1.4V	200.0U	890.0U	508.0U	496.0U	480.0U	570.0U	3.000M	A
IQ3	-41.25	VF=-1.4V	1.000M	2.560M	1.760M	1.640M	1.560M	1.810M	5.000M	A
VSTART	-4.25	1500	-1.300	-1.254	-1.256	-1.264	-1.251	-1.251	-1.200	V

NEG. ADJ. VOLTAGE REGULATORS-LM137K; TEMPERATURE: 150 DEG C ; 30 APR 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 1	S/N 2	S/N 4	S/N 5	S/N 6	HI-LIMIT	UNITS
VOUT5	-6.25	5	-1.300	-1.260	-1.262	-1.271	-1.258	-1.256	-1.200	V

NOTE :1 VF=FORCING VOLTAGE ON OUTPUT OF DEVICE

Table 3.26. (cont'd).

NEG. ADJ. VOLTAGE REGULATORS-LM137K; TEMPERATURE: 125 DEG C ; 30 APR 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 7	S/N 8	S/N 9	HI-LIMIT	UNITS
VOUT1	-4.25	5	-1.300	-1.242	-1.242	-1.252	-1.200	V
VOUT2	-4.25	1500	-1.300	-1.235	-1.235	-1.245	-1.200	V
VOUT3	-41.25	5	-1.300	-1.244	-1.244	-1.254	-1.200	V
VOUT4	-41.25	200	-1.300	-1.243	-1.243	-1.253	-1.200	V
VRLINE	-4.25 -41.25	5	-23.00M	-2.262M	-2.262M	-1.923M	23.00M	V
VRLOAD1	-6.25	5 1500	-12.00M	7.352M	7.352M	7.917M	12.00M	V
VRLOAD2	-41.25	5 200	-12.00M	226.3U	226.3U	1.131M	12.00M	V
VRTH (IL APPLIED FOR 10.5Msec.)	-14.60	1500	-5.000M	1.583M	1.583M	1.584M	5.000M	V
IADJ1 (LINE)	-4.25	5	25.00U	71.83U	71.83U	72.42U	100.0U	A
IADJ2 (LINE)	-41.25	5	25.00U	74.79U	74.79U	75.17U	100.0U	A
DIADJ1 (LINE)	-4.25 -41.25	5	-5.000U	2.964U	2.964U	2.750U	5.000U	A
DIADJ2 (LOAD)	-6.25	5 1500	-5.000U	-311.0N	-311.0N	-254.5N	5.000U	A
IOS1	-4.25	VF=0V	1.500	2.190	2.190	2.115	3.500	A
(VOUT) RECOV.			-1.300	-1.235	-1.235	-1.245	-1.200	V
IOS2	-40.00	VF=0V	200.0M	570.0M	570.0M	550.0M	800.0M	A
(VOUT) RECOV.			-1.300	-1.244	-1.244	-1.255	-1.200	V
IPEAK	-4.25	VF=-1.0V	1.500	2.140	2.140	1.945	3.500	A
(VOUT) RECOV.			-1.300	-1.235	-1.235	-1.244	-1.200	V
IQ1	-4.25	VF=-1.4V	200.0U	448.0U	448.0U	456.0U	3.000M	A
IQ2	-14.25	VF=-1.4V	200.0U	508.0U	508.0U	510.0U	3.000M	A
IQ3	-41.25	VF=-1.4V	1.000M	1.760M	1.760M	1.690M	5.000M	A
VSTART	-4.25	1500	-1.300	-1.235	-1.235	-1.244	-1.200	V

NEG. ADJ. VOLTAGE REGULATORS-LM137K; TEMPERATURE: 150 DEG C ; 30 APR 79

PARAMETER	CONDITION VIN	CONDITION IL(MA)	LO-LIMIT	S/N 7	S/N 8	S/N 9	HI-LIMIT	UNITS
VOUT5	-6.25	5	-1.300	-1.262	-1.252	-1.252	-1.200	V

TABLE 3.27. NEG. ADJ. VOLTAGE REGULATOR - LM137K T_A = 25°C 6-15-79

PARAMETER	CONDITIONS	LO - LIMIT	S/N7	S/N8	S/N9	-	-	HI - LIMIT	UNITS
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN} = -6.25V e_i = 1 V_{RMS} @ 2400 Hz I_L = 500 mA	50	59.2	58.4	60.9	-	-	-	dB
V_{NO}	V_{IN} = -6.25V I_L = 100 mA	-	70	70	70	-	-	120	uV_{RMS}
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN} = -6.25V ΔV_{IN} =-1.0 V I_L = 10 mA	-	30	32	30	-	-	40	mV/V
$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN} = -6.25V I_L = 100 mA ΔI_L = 400 mA	-	.05	.063	.045	-	-	0.15	mV/mA

Table 3.27. NEG. ADJ. VOLTAGE REGULATOR - LM137K T_A = 25°C 6-15-79 (cont'd).

PARAMETER	CONDITIONS	I.O - LIMIT	S/N1	S/N2	S/N4	S/N5	S/N6	HI - LIMIT	UNITS
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN} = -6.25V e_i = 1 V_{rms} @ 2400 Hz I_L = 500 mA	50	60.9	60.9	58.8	59.2	59.2	-	dB
V_{NO}	V_{IN} = -6.25V I_L = 100 mA	-	70	70	70	70	70	120	uV_{RMS}
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN} = -6.25V ΔV_{IN} =-1.0 V I_L = 10 mA	-	30	30	34	35	38	40	mV/V
$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN} = -6.25V I_L = 100 mA ΔI_L = 400 mA	-	.045	.05	.045	.05	.07	0.15	mV/mA

Table 3.28. Comparison of 3-Terminal Device Data (25°C)

Parameter	Condition $\lvert V_{IN} \rvert$ (V)	Condition $\lvert I_L \rvert$ (mA)	LM117H	LM117K	LM137H	LM137K	Units
V_{OUT1}	4.25	5	+1.240	+1.246	-1.252	-1.255	V
V_{OUT2}	4.25	I_{MAX}	+1.233	+1.245	-1.245	-1.250	V
V_{OUT3}	41.25	5	+1.247	+1.251	-1.255	-1.257	V
V_{OUT4}	41.25	I_1	+1.245	+1.248	-1.254	-1.257	V
V_{RLINE}	4.25 / 41.25	5	+5.771	+4.235	-2.477	-2.418	mV
V_{RLOAD1}	6.25	5 / I_{MAX}	-5.237	- .050	+11.39	+4.722	mV
V_{RLOAD2}	41.25	5 / I_1	-1.663	-2.174	+1.041	+ .749	mV
V_{RTH}	41.25	I_2	+2.941	+3.142			mV
	14.60	I_3			+ .430	+1.032	mV
I_{ADJ1} (LINE)	4.25	5	-50.11	-55.761	+68.64	+66.78	uA
I_{ADJ2} (LINE)	41.25	5	-50.74	-56.127	+71.67	+69.78	uA
ΔI_{ADJ} (LINE)	4.25 / 41.25	5	- .635	- .365	+3.026	+3.003	uA
ΔI_{ADJ} (LOAD)	6.25	5 / I_{MAX}	- .682	- .155	-1.090	- .519	uA
I_{OS1}	4.25	V_{OUT}=0V	-1.240	-2.711	+1.216	+2.294	A
V_{OUT} RECOV			+1.236	+1.247	-1.241	-1.250	V
I_{OS2}	40.00	V_{OUT}=0V	- .226	- .471	+ .340	+ .614	A
V_{OUT} RECOV			+1.249	+1.251	-1.254	-1.257	V
I_{PEAK}	4.25	$\lvert V_{OUT} \rvert$=-1.0V	-1.241	-2.409	+1.221	+2.340	A
V_{OUT} RECOV			+1.236	+1.247	-1.241	-1.250	V
IQ1	4.25	$\lvert V_{OUT} \rvert$=1.4V	-1.293	-1.318	+ .408	+ .414	mA
IQ2	14.25	$\lvert V_{OUT} \rvert$=1.4V	-1.443	-1.670	+ .478	+ .554	mA
IQ3	41.25	$\lvert V_{OUT} \rvert$=1.4V	-3.487	-3.729	+1.913	+2.034	mA
V_{START}	4.25	I_{MAX}	+1.234	+1.246	-1.241	-1.250	V
I_{MAX} =			-500	-1500	+500	+1500	mA
I_1 =			- 50	- 200	+ 50	+ 250	mA
I_2 =			-125	- 500	-	-	mA
I_3 =			-	-	+750	+1500	mA

Table 3.29. Comparison of 3-Terminal Device Data (-55°C)

Parameter	Condition $\lvert V_{IN} \rvert$ (V)	Condition $\lvert I_L \rvert$ (mA)	LM117H	LM117K	LM137H	LM137K	Units
V_{OUT1}	4.25	5	+1.240	+1.246	-1.253	-1.252	V
V_{OUT2}	4.25	I_{MAX}	+1.234	+1.245	-1.244	-1.248	V
V_{OUT3}	41.25	5	+1.245	+1.249	-1.256	-1.255	V
V_{OUT4}	41.25	I_1	+1.244	+1.247	-1.256	-1.255	V
V_{RLINE}	4.25 / 41.25	5	+4.830	+3.192	-3.846	-3.620	mV
V_{RLOAD1}	6.25	5 / I_{MAX}	+ .328	+ .842	+8.642	+3.195	mV
V_{RLOAD2}	41.25	5 / I_1	- .927	+ .943	+ .927	+ .537	mV
V_{RTH}	41.25	I_2	+4.083	+3.657	—	—	mV
	14.60	I_3	—	—	- .124	+ .057	mV
I_{ADJ1} (LINE)	4.25	5	-40.57	-46.51	+74.10	+70.97	uA
I_{ADJ2} (LINE)	41.25	5	-42.30	-46.76	+77.31	+74.36	uA
ΔI_{ADJ} (LINE)	4.25 / 41.25	5	-1.729	- .249	+3.200	+3.381	uA
ΔI_{ADJ} (LOAD)	6.25	5 / I_{MAX}	-1.435	- .382	-1.568	- .832	uA
I_{OS1}	4.25	V_{OUT}=0V	-1.258	-2.751	+1.192	+2.241	A
V_{OUT} RECOV			+1.238	+1.246	-1.244	-1.248	V
I_{OS2}	40.00	V_{OUT}=0V	- .329	- .698	+ .387	+ .736	A
V_{OUT} RECOV			+1.248	+1.249	-1.256	-1.255	V
I_{PEAK}	4.25	ΔV_{OUT} =-1.0V	-1.262	-2.315	+1.202	+2.192	A
V_{OUT} RECOV			+1.237	+1.245	-1.244	-1.248	V
IQ1	4.25	$\lvert V_{OUT} \rvert$ =1.4V	-1.023	-1.052	+ .315	+ .334	mA
IQ2	14.25	$\lvert V_{OUT} \rvert$ =1.4V	-1.380	-1.461	+ .410	+ .486	mA
IQ3	41.25	$\lvert V_{OUT} \rvert$ =1.4V	-3.377	-3.632	+1.964	+2.107	mA
V_{START}	4.25	I_{MAX}	+1.235	+1.245	-1.244	-1.248	V
I_{MAX} =			-500	-1500	+500	+1500	mA
I_1 =			- 50	- 200	+ 50	+ 200	mA
I_2 =			-125	- 500	-	-	mA
I_3 =			-	-	+750	+1500	mA

Table 3.30. Comparison of 3-Terminal Device Data (125°C)

Parameter	Condition V_{IN} (V)	Condition I_2 (mA)	LM117H	LM117K	LM137H	LM137K	Units
V_{OUT1}	4.25	5	+1.235	+1.238	-1.254	-1.256	V
V_{OUT2}	4.25	I_{MAX}	+1.225	+1.235	-1.240	-1.249	V
V_{OUT3}	41.25	5	+1.242	+1.243	-1.256	-1.257	V
V_{OUT4}	41.25	I_1	+1.240	+1.239	-1.255	-1.257	V
V_{RLINE}	4.25 / 41.25	5	+7.250	+5.077	-1.946	-2.177	mV
V_{RLOAD1}	6.25	5 / I_{MAX}	-5.101	-1.269	+15.09	+7.182	mV
V_{RLOAD2}	41.25	5 / I_1	-2.500	-3.519	+1.595	+ .905	mV
V_{RTH}	41.25	I_2	+2.104	+2.702			mV
	14.60	I_3			+ .882	+1.484	mV
I_{ADJ1} (LINE)	4.25	5	-55.36	-60.63	+74.00	+70.65	uA
I_{ADJ2} (LINE)	41.25	5	-55.95	-61.03	+76.84	+73.50	uA
ΔI_{ADJ} (LINE)	4.25 / 41.25	5	- .585	- .408	+2.846	+2.852	uA
ΔI_{ADJ} (LOAD)	6.25	5 / I_{MAX}	- .235	+ .022	- .581	- .295	uA
I_{OS1}	4.25	V_{OUT}=0V	-1.187	-2.354	+1.195	+2.170	A
V_{OUT} RECOV			+1.228	+1.237	-1.240	-1.249	V
I_{OS2}	40.00	V_{OUT}=0V	- .235	- .431	+ .318	+ .563	A
V_{OUT} RECOV			+1.244	+1.243	-1.256	-1.257	V
I_{PEAK}	4.25	$\lvert\Delta V_{OUT}\rvert$ =-1.0V	-1.186	-1.990	+1.196	+2.104	A
V_{OUT} RECOV			+1.227	+1.236	-1.240	-1.249	V
IQ1	4.25	$\lvert V_{OUT}\rvert$=1.4V	-1.450	-1.478	+ .474	+ .455	mA
IQ2	14.25	$\lvert V_{OUT}\rvert$=1.4V	-1.714	-1.771	+ .521	+ .559	mA
IQ3	41.25	$\lvert V_{OUT}\rvert$=1.4V	-3.396	-3.591	+1.805	+1.818	mA
V_{START}	4.25	I_{MAX}	+1.225	+1.236	-1.240	-1.249	V
I_{MAX} =			-500	-1500	+500	+1500	mA
I_1 =			- 50	- 200	+ 50	+ 200	mA
I_2 =			-125	- 500	-	-	mA
I_3 =			-	-	+750	+1500	mA

Table 3.31. Electrical performance characteristics for device type 01 (78MG) (See 3.4 unless otherwise specified)

Characteristic	Symbol	Condition: (Fig. 12 unless otherwise stated)			Limits		
		Input Voltage	Load Current	Other	Min.	Max.	Units
Output Voltage	V_{OUT}	V_{IN}= 8V	I_L=-5mA,-500mA	3/	4.75	5.25	V
		V_{IN}=30V	I_L=-5mA,-50 mA				
		V_{IN}=10V	I_L=-5mA	T_A=150°C 1/			
		V_{IN}=38V	I_L=-500mA	R_1=24.9KΩ R_2= 4.99KΩ	28.5	31.5	
Line regulation	V_{RLINE}	8V≤V_{IN} 30V	I_L=- 50mA	Figure 12 Waveform	-150	150	mV
		8V≤V_{IN} 25V	I_L=-350mA		- 50	50	
Load regulation	V_{RLOAD}	V_{IN}= 10V	-500mA≤I_L≤-5mA	Figure 12 Waveform	-100	100	
		V_{IN}= 30V	- 50mA≤I_L≤-5mA		-150	150	
Thermal regulation	$V_{RTH.}$	V_{IN}= 15V	I_L=-500mA	T_A=25°C Figure 12 Waveform	- 50	50	
Standby current drain	I_{SCD}	V_{IN}= 10V	I_L=-5mA		-7.0	-0.5	mA
		V_{IN}= 30V	I_L=-5mA		-8.0	-0.5	
Standby current drain change versus line voltage	ΔI_{SCD} (Line)	8V≤V_{IN}≤30V	I_L=-5mA		-1.0	1.0	
Standby current drain change versus load current	ΔI_{SCD} (Load)	V_{IN} = 10V	-500mA≤I_L≤-5mA		-0.5	0.5	
Control pin current	I_{CTL}	V_{IN} = 10V	I_L=-350mA	T_A=25°C	-5.0	-0.01	μA
				-55°C≤T_A≤ 125°C	-8.0	-0.01	μA
Output short circuit current	I_{OS1}	V_{IN} = 10V		Figure 12 Waveforms	-2.0	-0.01	A
	I_{OS2}	V_{IN} = 30V			-1.0	-0.01	
Output voltage recovery after output short circuit current	V_{OUT} (RECOV)	V_{IN} = 10V	R_L=10Ω;C_L=20μF	2/ After I_{OS1}	4.75	5.25	V
		V_{IN} = 30V	R_L=1KΩ	After I_{OS2}			
Voltage start-up	V_{START}	V_{IN} = 20V	R_L=10Ω;C_L=20μF		4.75	5.25	
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN} = 10V C_i = 1V_{rms} @ f= 2400 Hz	I_L=-125mA	Figure 13 T_A=25°C	45	--	dB
Output noise voltage	V_{NO}	V_{IN}= 10V	I_L=-50mA	Figure 14 T_A=25°C BW=10Hz to 10kHz	--	125	μV_{rms}
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN}= 10V V_{PULSE}=3.0V	I_L=-5mA	Figure 15 T_A=25°C	--	30	mV/V
Load transient response	$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN}= 10V	I_L=-50mA ΔI_L=-200mA	Figure 16 T_A=25°C	--	2.5	mV/mA

Table 3.31. (Cont'd)

NOTES: 1. All tests performed at T_A=125°C may, at the manufacturer's option, be performed at T_A=150°C. Specifications for T_A= 125°C shall then apply at TA=150°C.

2. Output voltage recovery test shall be performed, with the designated load conditions, immediately after removal of the IOS test forced output voltage condition. Voltage recovery for conditions other than those specified is not guaranteed.

3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

Table 3.32. Electrical performance characteristics for device type 02 (78G) (See 3.4 unless otherwise specified)

Characteristic	Symbol	Condition: (Fig. 12 unless otherwise stated)			Limits		
		Input Voltage	Load Current	Other	Min.	Max.	Units
Output Voltage	V_{OUT}	V_{IN}= 8V	I_L=-5mA,-1000mA	3/	4.75	5.25	V
		V_{IN}=30V	I_L=-5mA,-100 mA				
		V_{IN}=10V	I_L=-5mA	T_A=150°C 1/			
		V_{IN}=38V	I_L=-1000mA	R_1=24.9KΩ R_2=4.99KΩ	28.5	31.5	
Line regulation	V_{RLINE}	8V≤V_{IN}≤30V	I_L=-100mA	Figure 12	-150	150	mV
		8V≤V_{IN}≤25V	I_L=-500mA	Waveforms	- 50	50	
Load regulation	V_{RLOAD}	V_{IN}=10V	-1000mA≤I_L≤-5mA	Figure 12	-100	100	
		V_{IN}=30V	-100mA≤I_L≤-5mA	Waveforms	-150	150	
Thermal regulation	$V_{RTH.}$	V_{IN}=15V	I_L=-1000mA	T_A=25°C Figure 12 Waveforms	- 50	50	
Standby current drain	I_{SCD}	V_{IN}=10V	I_L=-5mA		-7.0	-0.5	mA
		V_{IN}=30V	I_L=-5mA		-8.0	-0.5	
Standby current drain change versus line voltage	ΔI_{SCD} (LINE)	8V≤V_{IN}≤30V	I_L=-5mA		-1.0	1.0	
Standby current drain change versus load current	ΔI_{SCD} (LOAD)	V_{IN}=10V	-1000mA≤I_L≤-5mA		-0.5	0.5	
Control pin current	I_{CTL}	V_{IN}=10V	I_L=-500mA	T_A=25°C	-5.0	-0.01	μA
				-55°C≤T_A ≤125°C	-8.0	-0.01	μA
Output short circuit current	I_{OS1}	V_{IN}=10V		Figure 12	-4.0	-0.02	A
	I_{OS2}	V_{IN}=30V		Waveforms	-2.0	-0.02	
Output voltage recovery after output short circuit current	V_{OUT} (RECOV)	V_{IN}=10V	R_L=5Ω;C_L=20μF	After I_{OS1} 2/	4.75	5.25	V
		V_{IN}=30V	R_L= 1KΩ	After I_{OS2}			
Voltage start-up	V_{START}	VIN =20V	R_L=5Ω;C_L=20uF		4.75	5.25	
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN}=10V C_i=1V_{rms} @f=2400 Hz	I_L=-350mA	Figure 13 T_A=25°C	45	--	d B
Output noise voltage	V_{NO}	V_{IN}=10V	I_L=-100mA	Figure 14 T_A=25°C BW=10 Hz to 10kHz	--	250	μV_{rms}
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN}=10V V_{PULSE}=3.0V	I_L=-5mA	Figure 15 T_A=25°C	--	30	mV/V
Load transient response	$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN}=10V	I_L=-100mA I_L=-400mA	Figure 16 T_A=25°C	--	2.5	mV/mA

Table 3.32. (Cont'd)

NOTES: 1. All tests performed at T_A=125°C may, at the manufacturer's option, be performed at T_A=150°C. Specifications for T_A=125°C shall then apply at T_A=150°C.

2. Output voltage recovery test shall be performed, with the designed load conditions, immediately after removal of the I_{OS} test forced output voltage condition. Voltage recovery for conditions other than those specified is not guaranteed.

3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

Table 3.33. Electrical performance characteristics for device type 03 (LM117H) (See 3.4 unless otherwise specified

Characteristic	Symbol	Condition: (Fig. 12 unless otherwise stated)			Limits		
		Input Voltage	Load Current	Other	Min.	Max.	Units
Output Voltage	V_{OUT}	V_{IN}=4.25V	I_L=-5mA,-500mA	3/	1.200	1.300	V
		V_{IN}=41.25V	I_L=-5mA,- 50mA				
		V_{IN}=6.25V	I_L=-5mA	T_A=150°C 1/			
Line regulation	V_{RLINE}	4.25V≤V_{IN}≤41.25V	I_L=-5mA	T_A=25°C	- 9	9	mV
				-55°C≤T_A≤125°C	-23	23	
Load regulation	V_{RLOAD}	V_{IN}=6.25V	-500mA≤I_L≤-5mA	T_A=25°C	-3.5	3.5	
				-55°C≤T_A≤125°C	-12	12	
		V_{IN}=41.25V	-50mA≤I_L≤-5mA	T_A=25°C	-3.5	3.5	
				-55°C≤T_A≤125°C	-12	12	
Thermal regulation	$V_{RTH.}$	V_{IN}=14.6V	I_L=-750mA	T_A=25°C	- 5	5	
Adjust pin current	I_{ADJ}	V_{IN}=4.25V	I_L=-5mA		-100	-15	µA
		V_{IN}=41.25V	I_L=-5mA		-100	-15	
Adjust pin current change versus line voltage	ΔI_{ADJ} (LINE)	4.25V≤I_L≤41.25V	I_L=-5mA		- 5	5	
Adjust pin current change versus load current	ΔI_{ADJ} (LOAD)	V_{IN}=6.25V	-500mA≤I_L≤-5mA		-5	5	
Minimum load current	I_Q	4.25V≤V_{IN}≤14.25V forced V_{OUT}=1.4V			-3.00	-0.50	mA
		V_{IN}=41.25V forced V_{OUT}=1.4V			-5.00	-1.00	mA
Output short circuit current	I_{OS1}	V_{IN}=4.25V			-1.8	-0.5	A
	I_{OS2}	V_{IN}=40V			-0.5	-0.05	A
Output voltage recovery after output short circuit current	V_{OUT} (RECOV)	V_{IN}=4.25V	R_L=2.5Ω;C_L=20µF	After I_{OS1} 2/	1.200	1.300	V
		V_{IN}=40V	R_L=250Ω	After I_{OS2}			
Voltage start-up	V_{START}	V_{IN}=4.25V	R_L=2.5Ω;C_L=20µF		1.200	1.300	
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN}=6.25V Ci=1Vrms @fo=2400 Hz	I_L=-125mA	Figure 13 T_A=25°C	65	--	dB
Output noise voltage	V_{NO}	V_{IN}=6.25V	I_L=-50mA	Figure 14 T_A=25°C BW=10Hz to 10kHZ	--	120	µVrms

Table 3.33. Electrical performance characteristics for device type 03 (LM117H) (Cont'd) (See 3.4 unless otherwise specified

Characteristic	Symbol	Condition: (Fig. 12 unless otherwise stated)			Limits		
		Input Voltage	Load Current	Other	Min.	Max.	Units
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN}=6.25V V_{IN}=3.0V	I_L=-10mA	Figure 15 T_A=25°C	--	6	mV/V
Load transient response	$\frac{\Delta V_{IN}}{\Delta I_L}$	V_{IN}=6.25V	I_L=-50mA ΔI_L=-200mA	Figure 16 T_A=25°C	--	0.6	mV/mA

NOTES: 1. All tests performed at T_A=125°C may, at the manufacturer's option, be performed at T_A=150°C. Specifications for T_A=125°C shall then apply at T_A=150°C.

2. Output voltage recovery test shall be performed, with the designated load conditions, immediately after removal of the I_{OS} test forced output voltage condition. Voltage recovery for conditions other than those specified is not guaranteed.

3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

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ELECTRICAL CHARACTERIZATION OF SPECIAL PURPOSE LINEAR MICROCIRC--ETC(U)
MAY 80 J S KULPINSKI, T SIMONSEN, L CARROZZA F30602-78-C-0195
UNCLASSIFIED RADC-TR-80-49 NL

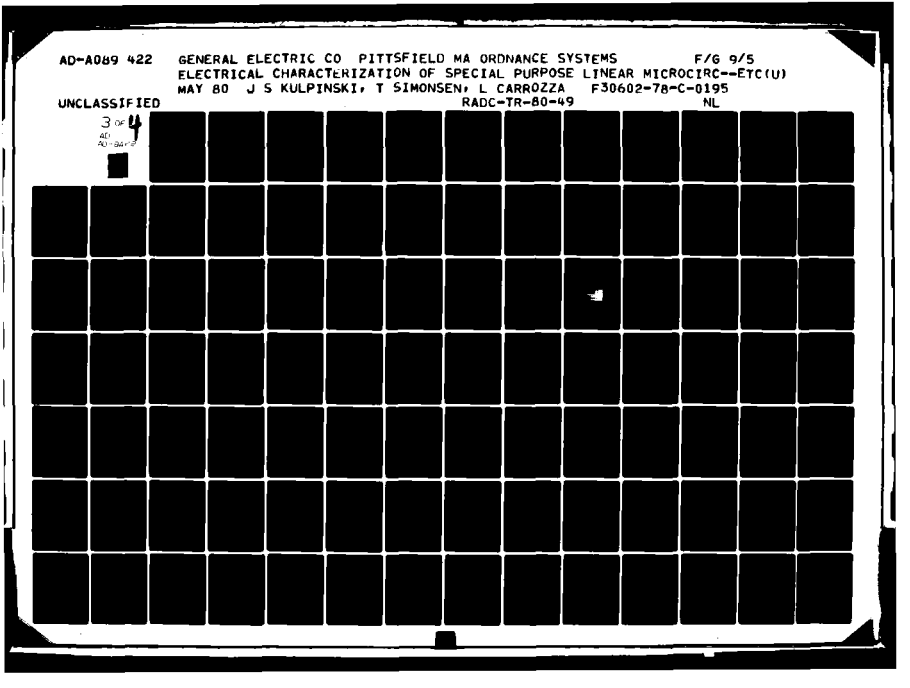

Table 3.34. Electrical performance characteristics for device type 04 (LM117K) (See 3.4 unless otherwise specified)

Characteristic	Symbol	Condition: (Fig. 12 unless otherwise stated)			Limits		
		Input Voltage	Load Current	Other	Min.	Max.	Units
Output Voltage	V_{OUT}	V_{IN}=4.25V	I_L=-5mA,-1500mA	3/	1.200	1.300	V
		V_{IN}=41.25V	I_L=-5mA,-200mA				
		V_{IN}=6.25V	I_L=-5mA	T_A=150°C 1/			
Line regulation	V_{RLINE}	4.25≤I_L ≤41.25V	I_L=-5mA	T_A=25°C	-9	9	mV
				-55°C≤T_A ≤125°C	-23	23	
Load regulation	V_{RLOAD}	V_{IN}=6.25V	-1500mA≤I_L≤-5mA	T_A=25°C	-3.5	3.5	
				-55°C≤T_A ≤125°C	-12	12	
		V_{IN}=41.25V	-150mA≤I_L≤-5mA	T_A=25°C	-3.5	3.5	
				-55°C≤T_A ≤125°C	-12	12	
Thermal regulation	$V_{RTH.}$	V_{IN}=14.6V	I_L=-1500mA	T_A=25°C	-5	5	
Adjust pin current	I_{ADJ}	V_{IN}=4.25V	I_L=-5mA		-100	-15	µA
		V_{IN}=41.25V	I_L=-5mA		-100	-15	
Adjust pin current change versus line voltage	ΔI_{ADJ} (LINE)	4.25V≤V_{IN} ≤41.25V	I_L=-5mA		-5	5	
Adjust pin current change versus load current	ΔI_{ADJ} (LOAD)	V_{IN}=6.25V	-1500mA≤I_L≤-5mA		-5	5	
Minimum load current	I_Q	4.25V≤I_L ≤14.25V forced V_{OUT} =1.4V			-3.00	-0.50	mA
		V_{IN}=41.25V forced V_{OUT} =1.4V			-5.00	-1.00	mA
Output short circuit current	I_{OS1}	V_{IN}=4.25V			-3.50	-1.50	A
	I_{OS2}	V_{IN}=40V			-1.00	-0.18	A
Output voltage recovery after output short circuit current	V_{OUT} (RECOV)	V_{IN}=4.25V	R_L=.833Ω;C_L=20µF	After I_{OS1} 2/	1.200	1.300	V
		V_{IN}=40V	R_L=250Ω	After I_{OS2}			
Voltage start-up	V_{START}	V_{IN}=4.25V	R_L=.833Ω;C_L=20µF		1.200	1.300	
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN}=6.25V Ci=1Vrms @fo=2400 Hz	I_L=-500mA	Figure 13 T_A=25°C	65	--	dB
Output noise voltage	V_{NO}	V_{IN}=6.25V	I_L=-100mA	Figure 14 T_A=25°C BW=10Hz to 10kHz	--	120	µVrms

Table 3.34. Electrical performance characteristics for device type 04 (LM117K) (Cont'd) (See 3.4 unless otherwise specified)

Characteristic	Symbol	Condition: (Fig. 12 unless otherwise stated)			Limits		
		Input Voltage	Load Current	Other	Min.	Max.	Units
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN}=6.25V ΔV_{IN}=1.0V	I_L=-10mA	Figure 15 T_A=25°C	--	6	mV/V
Load transient response	$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN}=6.25V	I_L=-100mA ΔI_L=-400mA	Figure 16 T_A=25°C	--	0.30	mV/mA

NOTES:

1. All tests performed at T_A=125°C may, at the manufacturer's option, be performed at T_A=150°C. Specifications for T_A=125°C shall then apply at T_A=150°C.

2. Output voltage recovery test shall be performed, with the designated load conditions, immediately after removal of the I_{OS} test forced output voltage condition. Voltage recovery for conditions other than those specified is not guaranteed.

3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

Table 3.35. Electrical performance characteristics for device type 01 (79MG) (See 3.4 unless otherwise specified)

Characteristic	Symbol	Condition: (Fig. 12 unless otherwise stated)			Limits		
		Input Voltage	Load Current	Other	Min.	Max.	Units
Output Voltage	V_{OUT}	V_{IN}=-8V V_{IN}=-30V V_{IN}=-10V	I_L=5mA,500mA I_L=5mA,50mA I_L=5mA	3/ T_A=150°C 1/	-5.25	-4.75	V
		V_{IN}=-38V	I_L=500mA	R_1=27.4kΩ R_2=2.21kΩ	-31.5	-28.5	
Line regulation	V_{RLINE}	-30V≤V_{IN}≤-8V -25V≤V_{IN}≤-8V	I_L=50mA I_L=350mA	Figure 12 Waveforms	-150 - 50	150 50	mV
Load regulation	V_{RLOAD}	V_{IN}=-10V V_{IN}=-30V	5mA≤I_L≤500mA 5mA≤I_L≤50mA	Figure 12 Waveforms	-100 -150	100 150	
Thermal regulation	$V_{RTH.}$	V_{IN}=-15V	I_L=500mA	T_A-25°C Figure 12 Waveforms	- 50	50	
Standby current drain	I_{SCD}	V_{IN}=-10V V_{IN}=-30V	I_L=5mA I_L=5mA		0.1 0.1	3.0 4.0	mA
Standby current drain change versus line voltage	ΔI_{SCD} (LINE)	-30V≤V_{IN}≤-8V	I_L=5mA		-1.0	1.0	
Standby current drain change versus load current	ΔI_{SCD} (LOAD)	V_{IN}=-10V	5mA≤I_L≤500mA		-0.5	0.5	
Control pin current	I_{CTL}	V_{IN}=-10V	I_L=350mA	T_A=25°C -55°C≤T_A≤125°C	0.001 0.001	2.00 3.00	µA µA
Output short circuit current	I_{OS1} I_{OS2}	V_{IN}=-10V V_{IN}=-30V		Figure 12 Waveforms	0.002 0.002	2.0 1.0	A
Output voltage recovery after output short circuit current	V_{OUT} (RECOV)	V_{IN}=-10V V_{IN}=-30V	R_L=10Ω;CL =20µf R_L=5kΩ	After I_{OS1} 2/ After I_{OS2}	-5.25	-4.75	V
Voltage Start-up	V_{START}	V_{IN}=-20V	R_L=10Ω;CL =20µF		-5.25	-4.75	
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN}=-10V Ci=1Vrms @f=2400 Hz	I_L=125mA	Figure 13 T_A=25°C	45	--	dB
Output noise voltage	V_{NO}	V_{IN}=-10V	I_L=50mA	Figure 14 T_A=25°C BW=10Hz to 10kHz	--	250	µVrms
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN}=-10V V_{PULSE}=-3.0V	I_L=5mA	Figure 15 T_A=25°C	--	30	mV/V
Load transient response	$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN}=-10V	I_L=50mA ΔI_L=200mA	Figure 16 T_A=25°C	--	2.5	mV/mA

Table 3.35. (Cont'd)

NOTES: 1. All tests performed at T_A=125°C may, at the manufacturer's option, be performed at T_A=150°C. Specifications for T_A=125°C shall then apply at T_A-150°C.

2. Output voltage recovery test shall be performed, with the designated load conditions, immediately after removal of the I_{OS} test forced output voltage condition. Voltage recovery for conditions other than those specified is not guaranteed.

3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

Table 3.36. Electrical performance characteristics for device type 02 (79G)
(See 3.4 unless otherwise specified)

Characteristic	Symbol	Condition: (Fig. 12 unless otherwise stated)			Limits		
		Input Voltage	Load Current	Other	Min.	Max.	Units
Output Voltage	V_{OUT}	V_{IN}=-8V	I_L=5ma,1000mA	3/	-5.25	-4.75	V
		V_{IN}=-30V	I_L=5mA,100mA				
		V_{IN}=-10V	I_L=5mA	T_A=150°C 1/			
		V_{IN}=-38V	I =1000mA	R_1=27.4kΩ R_2=2.21kΩ	-31.5	-28.5	
Line regulation	VRLINE	-30V≤V_{IN}≤-8V	I_L=100mA	Figure 12	-150	150	mV
		-25V≤V_{IN}≤-8V	I_L= 500mA	Waveforms	- 75	75	
Load regulation	VRLOAD	V_{IN}=-10V	5mA≤I_L≤1000mA	Figure 12	-100	100	
		V_{IN}=-30V	5mA≤I_L≤100mA	Waveforms	-150	150	
Thermal regulation	VRTH.	V_{IN}=-15V	I_L=1000mA	T_A=25°C Figure 12 Waveforms	- 50	50	
Standby current drain	I_{SCD}	V_{IN}=-10V	I_L=5mA		0.5	3.0	mA
		V_{IN}=-30V	I_L=5mA		0.5	4.0	
Standby current drain change versus line voltage	ΔISCD (LINE)	-30V≤V_{IN}≤-8V	I_L=5mA		-1.0	1.0	
Standby current drain change versus load current	ΔISCD (LOAD)	V_{IN}=-10V	5mA≤I_L≤1000mA		-0.5	0.5	
Control pin current	I_{CTL}	V_{IN}=-10V	I_L=500mA	T_A=25°C	0.01	2.00	μA
				-55°C≤T_A ≤125°C	0.001	3.00	μA
Output short circuit current	I_{OS1}	V_{IN}=-10V		Figure 12	0.002	4.5	A
	I_{OS2}	V_{IN}=-30V		Waveform	0.002	2.0	
Output voltage recovery after output short circuit current	V_{OUT} (RECOV)	V_{IN}=-10V	R_L=5Ω;C_L=20μF	After I_{OS1} 2/	-5.25	-4.75	V
		V_{IN}=-30V	R_L=5kΩ	After I_{OS2}			
Voltage start-up	V_{START}	V_{IN}=-20V	R_L=5Ω;C_L=20uF		-5.25	-4.75	
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN}=-10V C_1=1Vrms @f=2400Hz	I_L=350mA	Figure 13 T_A=25°C	45	--	dB
Output noise voltage	V_{NO}	V_{IN}=-10V	I_L=100mA	Figure 14 T_A=25°C BW=10Hz to 10kHz	--	250	μVrms
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN}=-10V V_{PULSE}=-3.0V	I_L=5mA	Figure 15 T_A=25°C	--	30	mV/V
Load transient response	$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN}=-10V	I_L=100mA ΔI_L=400mA	Figure 16 T_A=25°C	--	2.5	mV/mA

Table 3.36. (Cont'd)

NOTES: 1. All tests performed at T_A=125°C may, at the manufacturer's option, be performed at T_A=150°C. Specifications for T_A=125°C shall then apply at T_A=150°C.

2. Output voltage recovery test shall be performed, with the designated load conditions, immediately after removal of the I_{OS} test forced output condition. Voltage recovery for conditions other than those specified is not guaranteed.

3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

Table 3.37. Electrical performance characteristics for device type 03 (LM137H)
(See 3.4 unless otherwise specified)

Characteristic	Symbol	Condition: (Fig. 12 unless otherwise stated)			Limits		Units
		Input Voltage	Load Current	Other	Min.	Max.	
Output Voltage	V_{OUT}	V_{IN}=-4.25V	I_L=5mA,500mA	3/	-1.300	-1.200	V
		V_{IN}=-41.25V	I_L=5mA, 50mA				
		V_{IN}=-6.25V	I_L=5mA	T_A=150°C 1/			
Line regulation	V_{RLINE}	-41.25V≤V_{IN} ≤-4.25V	I_L=5mA	T_A=25°C	-9	9	mV
				-55°C T_A 125°C	-23	23	
Load regulation	V_{RLOAD}	V_{IN}=-6.25V	5mA≤I_L≤200mA	T_A=25°C	-6	6	
				-55°C≤T_A ≤125°C	-12	12	
			5mA≤I_L≤500mA	T_A=25°C	-12	12	
				-55°C≤T_A ≤125°C	-24	24	
		V_{IN}=-41.25V	5mA≤I_L≤50mA	T_A=25°C	- 6	6	
				-55°C≤T_A ≤125°C	-12	12	
Thermal regulation	$V_{RTH.}$	V_{IN}=-14.6V	I_L=750mA	T_A=25°C	- 5	5	
Adjust pin current	I_{ADJ}	V_{IN}=-4.25V	I_L=5mA		25	100	µA
		V_{IN}=-41.25V	I_L=5mA		25	100	
Adjust pin current change versus line voltage	ΔI_{ADJ} (LINE)	-41.25V≤I_L ≤-4.25V	I_L=5mA		- 5	5	
Adjust pin current change versus load current	ΔI_{ADJ} (LOAD)	V_{IN}=-6.25V	5mA≤I_L≤500mA		- 5	5	
Minimum load current	I_Q	-14.25V≤V_{IN} ≤-4.25V forced V_{OUT} =-1.4V			0.20	3.00	mA
		V_{IN}=41.25V forced V_{OUT} =-1.4V			1.00	5.00	
Output short circuit current	I_{OS1}	V_{IN}=-4.25V			0.5	1.8	A
	I_{OS2}	V_{IN}=-40V			0.05	0.5	A
Output voltage recovery after output short circuit current	V_{OUT} (RECOV)	V_{IN}=-4.25V	R_L=2.5Ω;C_L =20µF	After I_{OS1} 2/	-1.300	-1.200	V
		V_{IN}=-40V	R_L=250Ω	After I_{OS2}			
Voltage start-up	V_{START}	V_{IN}=-4.25V	R_L=2.5Ω;C_L =20µF		-1.300	-1.200	
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN}=-6.25V C_i=1Vrms @fo=2400 Hz	I_L=125mA	Figure 13 T_A=25°C	48	--	dB

Table 3.37. Electrical performance characteristics for device type 03 (LM137H) (Cont'd) (See 3.4 unless otherwise specified)

Characteristic	Symbol	Condition: (Fig. 12 unless otherwise stated)			Limits		
		Input Voltage	Load Current	Other	Min.	Max.	Units
Output noise voltage	V_{NO}	V_{IN}=-6.25V	I_L=50mA	Figure 14 T_A=25°C BW=10 Hz to 10kHz	--	120	μVrms
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN}=-6.25V ΔV_{IN}=-1.0V	I_L=10mA	Figure 15 T_A=25°C	--	80	mV/V
Load transient response	$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN}=-6.25V	I_L=50mA ΔI_L=200mA	Figure 16 T_A=25°C	--	0.30	mV/mA

NOTES: 1. All tests performed at T_A=125°C may, at the manufacturer's option, be performed at T_A=150°C.

2. Output voltage recovery test shall be performed, with the designated load conditions, immediately after removal of the I_{OS} test forced output voltage condition. Voltage recovery for conditions other than those specified is not guaranteed.

3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

Table 3.38. Electrical performance characteristics for device type 04 (LM137K) (See 3.4 unless otherwise specified)

Characteristic	Symbol	Condition: (Fig. 12 unless otherwise stated)			Limits		
		Input Voltage	Load Current	Other	Min.	Max.	Units
Output Voltage	V_{OUT}	V_{IN}=-4.25V V_{IN}=-41.25V V_{IN}=-6.25V	I_L=5mA,1500mA I_L=5mA,200mA I_L=5mA	3/ T_A=150°C 1/	-1.300	-1.200	V
Line regulation	V_{RLINE}	-41.25V≤ V_{IN} ≤-4.25V	I_L=5mA	T_A=25°C -55°C≤T_A ≤125°C	- 9 -23	9 23	mV
Load regulation	V_{RLOAD}	V_{IN}=-6.25V	5mA≤I_L≤1500mA	T_A=25°C -55°C≤T_A ≤125°C	- 6 -12	6 12	
		V_{IN}=-41.25V	5mA≤I_L≤150mA	T_A=25°C -55°C≤T_A ≤125°C	- 6 -12	6 12	
Thermal regulation	$V_{RTH.}$	V_{IN}=-14.6V	I_L=1500mA	T_A=25°C	- 5	5	
Adjust pin current	I_{ADJ}	V_{IN}=-4.25V V_{IN}=-41.25V	I_L=5mA I_L=5mA		25 25	100 100	µA
Adjust pin current change versus line voltage	ΔI_{ADJ} (LINE)	-41.25V≤I_L≤ 4.25V	I_L=5mA		- 5	5	
Adjust pin current change versus load current	ΔI_{ADJ} (LOAD)	V_{IN}=-6.25V	5mA≤I_L≤1500mA		- 5	5	
Minimum load current	I_Q	-14.25V≤V_{IN} ≤-4.25V forced V_{OUT} =-1.4			0.20 1.00	3.00 5.00	mA
		V_{IN}=-41.25V forced V_{OUT} =-1.4V			1.00	5.00	
Output short circuit current	I_{OS1} I_{OS2}	V_{IN}=-4.25V V_{IN}=-40V			1.5 0.2	3.5 0.8	A A
Output voltage recovery after output short circuit current	V_{OUT} (RECOV)	V_{IN}=-4.25V V_{IN}=-40V	R_L=.833Ω;C_L =20µF R_L=250Ω	After I_{OS1} 2/ After I_{OS2}	-1.300	-1.200	V
Voltage start-up	V_{START}	V_{IN}=-4.25V	R_L=.833Ω;C_L =20µF		-1.300	-1.200	
Ripple rejection	$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	V_{IN}=-6.25V C_i=1Vrms @fo=2400Hz	I_L=500mA	Figure 13 T_A=25°C	50	--	dB
Output noise voltage	V_{NO}	V_{IN}=-6.25V	I_L=100mA	Figure 14 T_A=25°C BW=10Hz to 10kHz	--	120	µVrms

Table 3.38. Electrical performance characteristics for device type 04 (LM137K) (Cont'd) (See 3.4 unless otherwise specified)

Characteristic	Symbol	Condition: (Fig. 12 unless otherwise stated)			Limits		
		Input Voltage	Load Current	Other	Min.	Max.	Units
Line transient response	$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	V_{IN}=-6.25V ΔV_{IN}=-1.0V	I_L=10mA	Figure 15 T_A=25°C	--	40	mV/V
Load transient response	$\frac{\Delta V_{OUT}}{\Delta I_L}$	V_{IN}=-6.25V	I_L=100mA ΔI_L=400mA	Figure 16 T_A=25°C	--	0.15	mV/mA

NOTES:

1. All tests performed at T_A=125°C may, at the manufacturer's option, be performed at T_A=150°C. Specifications for T_A=125°C shall then apply at T_A=150°C.

2. Output voltage recovery test shall be performed, with the designated load conditions, immediately after removal of the IOS test forced output voltage condition. Voltage recovery for conditions other than those specified is not guaranteed.

3. Static tests with load currents greater than 5mA are performed under pulsed conditions defined in Figure 12.

SECTION IV

MULTIPLE Bi-FET OP AMPS
MIL-M-38510/119

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SECTION IV

MULTIPLE Bi-FET OP AMPS
MIL-M-38510/119

4.1 Background and Introduction

The first op amps of this series which were introduced to RADC for characterization and possible slash sheet action were the TL061 and TL071 families from Texas Instruments. Each of these families included single, dual and quad device types. The TL061, TL062 and TL064 devices were offered as a low power category and the TL071, TL072 and TL074 devices were classified as low noise devices. Preliminary characterization studies at GEOS were encouraging and a recommendation for slash sheet action was made. Since these new Bi-FET op amps had lower absolute maximum ratings than the LF155 series devices, it was necessary to generate a new slash sheet. National Semiconductor and Fairchild were also introducing multiple Bi-FET op amp devices which could be included in the new slash sheet. MIL-M-38510/119 contains the following generic industry devices:

Generic Industry Type	Military Device Type
TL061 (single-low power)	01
TL062 (dual-low power)	02
TL064 (quad-low power)	03
TL071, uAF771, LF151 (single - general purpose)	04
TL072, uAF772, LF153 (dual - general purpose)	05
TL074, uAF774, LF147 (quad - general purpose)	06

The differences between the absolute maximum rating of the /114 and /119 military specifications are shown below:

Absolute Max Ratings	MIL-M-38510-/114	/119
Supply voltage	± 22V	± 18V
Input voltage 1/	± 20V	± 15V
Differential Input Voltage	± 40V	± 30V

1/ The absolute maximum negative input voltage is equal to the negative power supply voltage.

Whereas device types 01, 02 and 03 are intended for low power applications, device types 04, 05 and 06 are intended to be the future low cost "741 work horses" of the industry.

4.2 Description of Device Types

The op amps specified in /119 have fewer J-FETs per op amp than the LF155 series devices. As a result the chip real estate per function is approximately 2/3 that of an LF155 device. Consequently, the options for lower cost and multiple op amp devices are also more viable than with the LF155 series design.

Figures 4-1, 4-2, 4-3 and 4-4 show the schematic diagrams of these new second generation Bi-FET op amps. All of these devices feature J-FETs for the differential input stage and complementary bipolar transistors for the totem pole output stage. Unlike the LF155 series design a J-FET is not used to replace the output PNP transistor for stability improvement.

Another common difference between these devices and the LF155 series is that the input J-FETs are not loaded by matched J-FET current sources. Instead a bipolar current mirror is used with trim resistors in the emitter legs. Offset voltage can be internally laser trimmed or externally potentiometer trimmed. Because of pinout restrictions some of the duals and all of the quads do not have external offset voltage adjustment capability. Caution should be exercised in swapping /119 single with /114 devices in applications using the offset control pins.

Since the LF155 adjustment is connected to $+ V_{cc}$ and the /119 single device is connected to $- V_{cc}$ proper operation after swapping will not work and could lead to device destruction if the trim wiper gets too close to one of the potentiometer ends.

The input for the single ended high gain second stage is taken off the collector of the current mirror transistor.

Another current mirror connected to a zener regulated current source provides separate constant current biasing for the first and second amplifier stages of the TL071 series devices.

The current source stage biasing for the other devices are all different in design. Modifications of current mirrors and lateral PNP transistors are used extensively as can be seen in the circuit schematics. The degree of circuitry used for stage biasing enables the op amps to be used over a wide range of power supply voltages while maintaining excellent power supply rejection to noise and other disturbances. Further details are covered in the manuals, books and papers referenced in the bibliography of this report.

4.2 Description of Device Types (cont.)

All of the generic industry device types within the /119 specification have design differences which will tend to favor one parameter over another. As a consequence of this fact the margin of performance between the different vendor devices and the specification limits will vary accordingly.

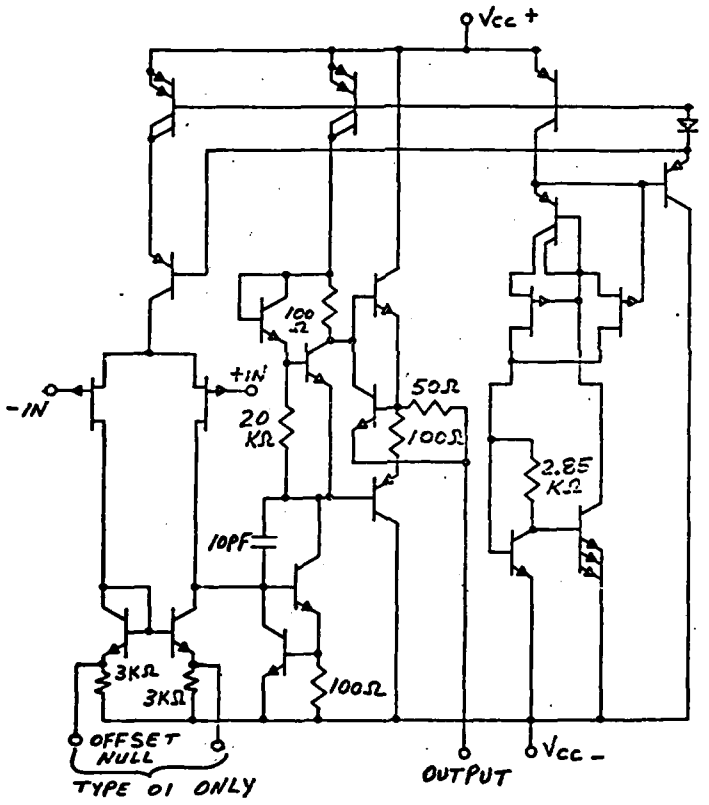


Figure 4-1. TL061 Series Op Amp Schematic.

4.2 Description of Device Types (cont.)

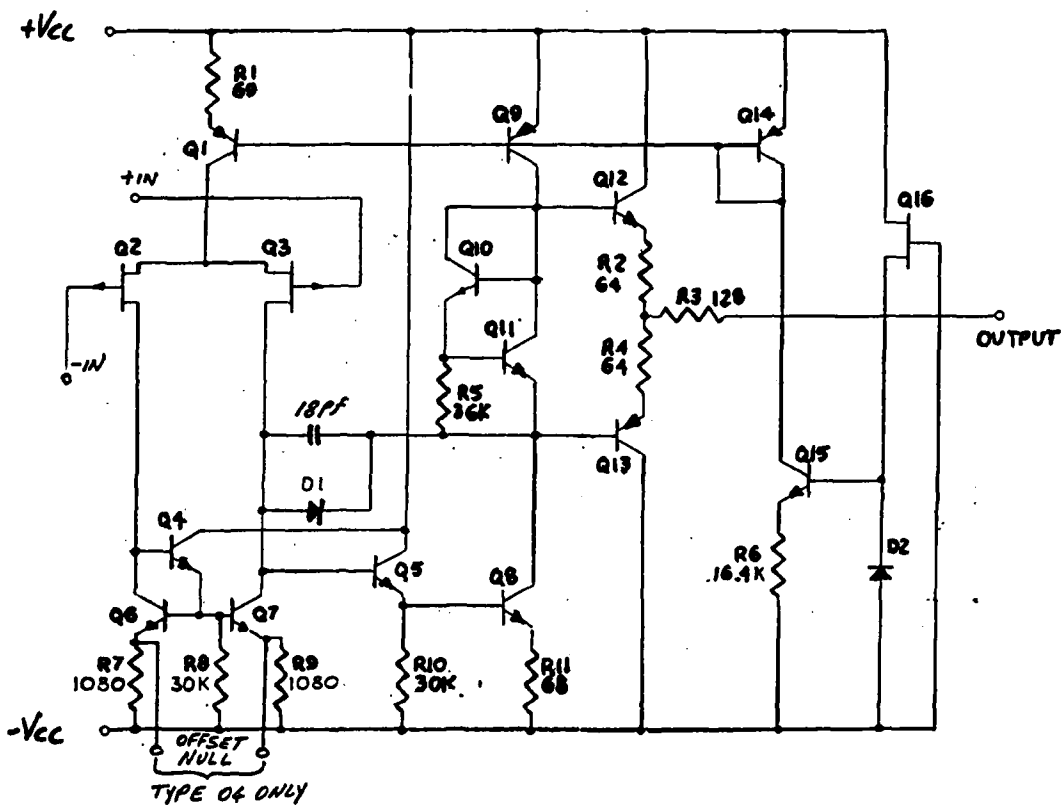


Figure 4-2. T1071 Series Op Amp Schematic.

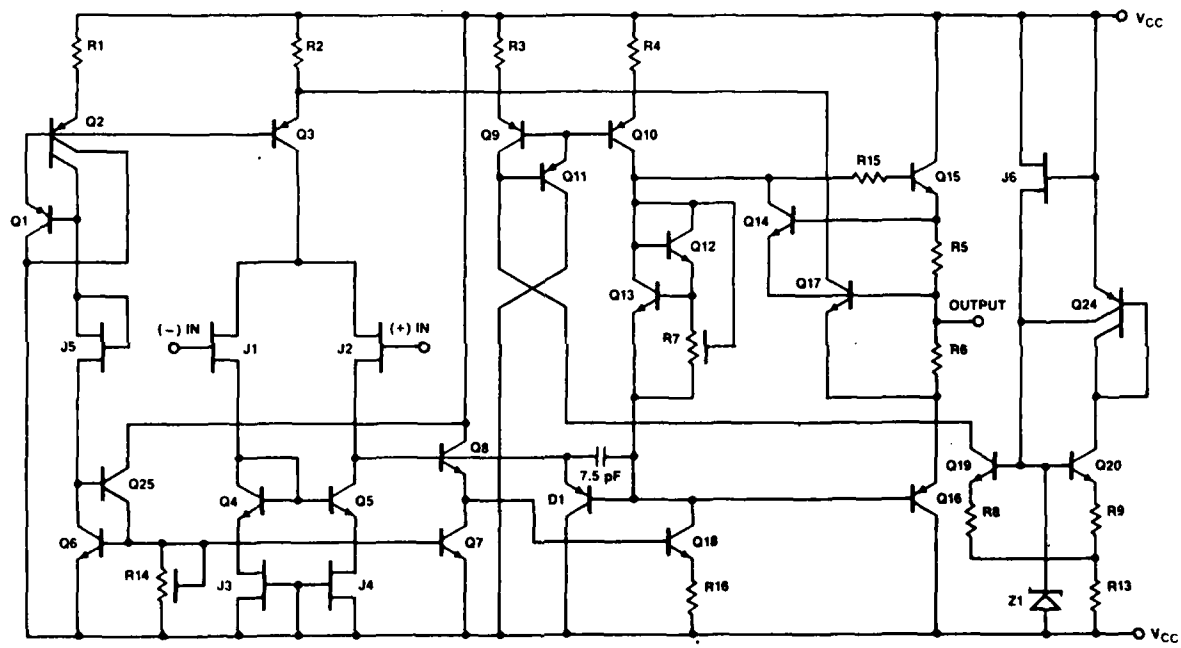


Figure 4-3. uAF771 Series Op Amp Schematic.

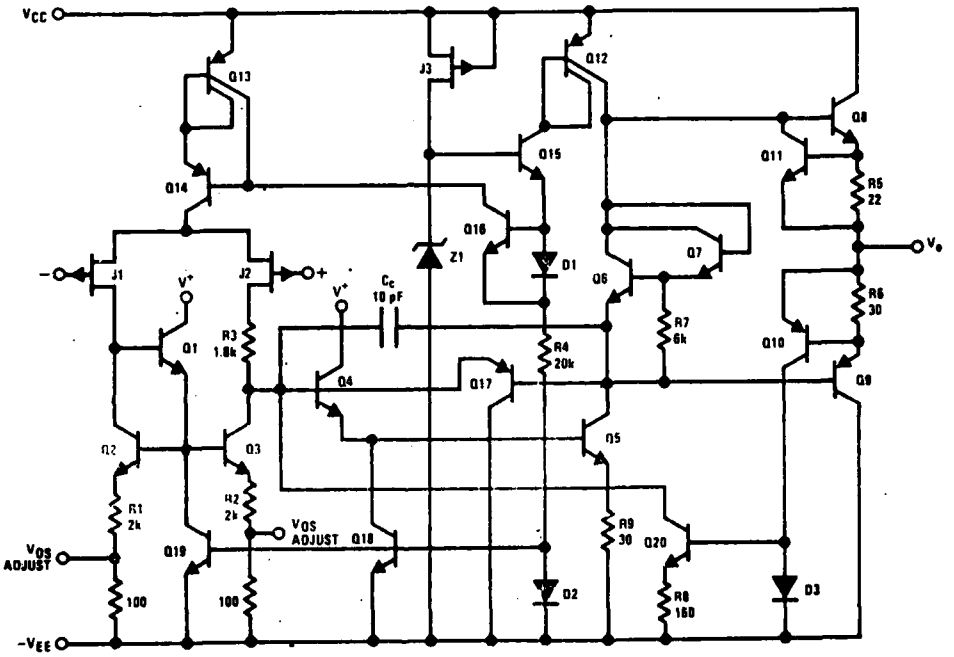


Figure 4-4. LF151, 153, 147 Op Amp Schematic.

4.3 Device Characterization

The characterization procedure for the multiple Bi-FET op amps was very similar to the procedure described in Section 2.3. A notable difference was that the test adapter had to be configured to accept dual and quad devices in addition to single devices. This was accomplished by building several DIP to TO5 pin-out converters with manual selection switches. Although this method was satisfactory in getting the data, a more elaborate relay controlled socket would have been more efficient for testing large quantities of devices, especially if this effort were required on a continuing basis.

Software changes were made to the program to reduce the power supply and command voltages to the specified values for these devices. Transient response, settling time and slew rate data were measured manually with a new test fixture having dedicated DIP sockets for single, dual and quad devices.

As with the LF155 series devices, a Tektronix 577 curve tracer was used to observe parameter to parameter characteristics of sample devices. Further details on op amp characterization test procedures are contained in Section 2.3.

4.4 Tabulation of Test Data

A representative tabulation of S-3260 characterization data is shown in Tables 4-1 through 4-6. Each of these data sheets show how the data values of 10 devices compares to the JC-41 Committee limits at a given test temperature. Most parameters were tested with ±16 volt power supplies over a ± 12 volt common mode range. Even though device types 01, 02, and 03 are not rated to drive a 2000 ohm load, data was taken with this condition for information only.

Statistical summaries of all the data are shown in Table 4-7 through 4-12.

Histograms were generated on an op amp basis for both device type families for all parameter-temperature combinations. One such histogram at 25°C of common mode rejection for device types 04, 05 and 06 is shown in Figure 4-5.

A complete tabulation of the data is being issued in handbook form to the JC-41 Committee representatives.

4.5 Discussion

The characterization data was carefully reviewed to determine how well it complies to the proposed JC-41 limits and the June 1979 Rev. 1 issue of MIL-M-38510/119. Where there is good agreement between the data and the limits, no further discussion will be given here. The proposed JC-41 parameter limits will then be carried over into Table 4-13. Where there is a discrepancy between the data and the JC-41 limits a discussion will be included with GEOS proposed limits. Because of the limited sample size (51 low power op amps and 81 low cost op amps), the GEOS data may not accurately reflect the data of all manufacturer lot samples.

Vendor feedback will be required before firm limits can be recommended for the proposed multiple op amp slash sheet MIL-M-38510/119. Table 4-13 is the best estimate of this time of the /119 Table I limits.

4.5.1 Input Offset Voltage (V_{io})

With the exception of vendor B Type 04 devices at 125°C, the offset voltage data agrees with the proposed limits of ± 5 mV and ± 7 mV at 25°C and over the military temperature range, respectively.

4.5.2 Input Offset Current (I_{io})

Early in the characterization program there were many device failures to the ± 50 pA JC-41 limits. Because of this the histogram and statistical analysis limits were loosened to ± 100 pA. A comparison of the 25°C, zero common mode offset current data against the data limits is as follows:

4.5.2 Input Offset Current (I_{io}) (cont.)

Device Type	Yield @ I_{io} = ± 100 pA (max)	Yield @ I_{io} ± 50 pA (max)
01,02,03	(51-8)/51 = 84%	(51-15)/51 = 70%
04,09,06	(81-18)/81 = 78%	(81-27)/81 = 67%

For reasonable yields the ± 100 pA limits should be used.

4.5.3 Input Bias Current (± I_{iB})

At the negative common mode condition at 25°C, both device families had yields of less than 70% against the -200 pA limit. The yields improve to better than 80% with a relaxed low limit of -400 pA. The high temperature high limits were too loose and it is suggested that they be changed from 100 nA to 70 nA at the positive common mode voltage and from 70 nA to 50 nA for the other common mode voltage conditions.

4.5.4 Short Circuit Current ($I_{os(+)}$, $I_{os(-)}$

Based on these devices alone limits of 30 mA would be recommended; however, other vendor type devices, not yet characterized, require the 40 mA limit for the low power category. The general purpose device limits of ± 80 mA are reasonable.

4.5.5 Supply Current (I_{cc})

Although the supply current is specified on an op amp basis, observations of the data show that duals and quads use less current per op amp than does a single device. An average "discount" for the multiple op amps based on histogram mean values is 20% for the duals and 30% for the quads. No change is recommended for /119.

4.5.6 Output Voltage Swing (+ V_{op}, - V_{op})

Based on the data, the voltage swing limits are specified very conservatively. For device types 01, 02 and 03 with a 10K ohm load, - V_{op} is the weakest drive. 50 out of 51 devices had less than 1.2 V of negative saturation. ($-V_{sat} = |-V_{cc} - (-V_{op})|$).

The single 01 maverick with 1.7 V of negative saturation also failed the V_{io}, -PSRR and the gain tests. For the 04, 05, and 06 device data the maximum saturation drops were 2.1 V at 10 KΩ and 3.5 V with 2KΩ loading.

4.5.6 Output Voltage Swing ($+V_{OP}$, $-V_{OP}$) (cont.)

It is recommended that the swing limits be increased to 12.5 V at 10K Ω and 11 V at 2K Ω. The characterization data was measured with $\pm V_{CC} = \pm 16$ V, whereas the proposed slash sheet is specified with $\pm V_{CC} = \pm 15$ V. Because of this difference the data was examined on an "output to rail" basis.

4.5.7 Open Loop Voltage Gain ($A_{VS(+)}$, $A_{VS(-)}$)

One of the tradeoffs for device types 01, 02 and 03 is that the low power option results in lower open loop gain. One change that can be recommended is that A_{VS} at $\pm V_{CC} = \pm 5$ V be increased from 2 to 3 V/mV (min.). The lowest corresponding data value was approximately 4.8 V/mV from a -55°C histogram.

As a general observation, device types 04, 05 and 06 have lower gains than the 155 series devices by a factor of from 1/4 to 1/3.

4.5.8 Slew Rate (SR(+), SR(-))

With the exception of several failures from vendor code B devices, all of the devices had slew rates greater than the specified minimum levels. No specification change is recommended, unless vendor code B determines that a relaxation in limits is necessary.

4.5.9 Transient Response ($TR_{(tr)}$, $TR_{(os)}$)

The previous parameters were measured automatically, but transient response was measured manually with a signal generator and an oscilloscope. Histograms were generated on the S-3260 from the manual data.

For the low power devices the data indicates that the rise time and overshoot should be changed from 600 nanoseconds and 40% to 400 nanoseconds and 20% respectively. These limits would still leave a 2:1 margin from the observed worst cases. Device types 04, 05 and 06 have data in good agreement with the limits.

4.5.10 Settling Time ($t_{s(+)}$, $t_{s(-)}$)

The data indicates that the settling time limit for device types 01, 02 and 03 need to be increased from 1500 ns to 6000 ns. The initial limits of 1500 ns was a tentative estimate without a JC-41 recommendation.

In view of the fact that device types 04, 05 and 06 have four to five times as fast a slew rate as the low power devices, it is not surprising that the data yields a similar conclusion with settling time.

4.6 Conclusions and Recommendations

A characterization study was conducted on a mix of single, dual and quad Bi-FET op amps. The data base consists of 51 low power op amps and 81 general purpose op amps. Minor changes in the JC-41 specifications were made to reflect GEOS's data observations, yield considerations and user priorities. These multiple Bi-FET op amps should find many useful applications in military systems.

4.7 Bibliography

4.7.1 R. Russell and T. Frederiksen, "How the Bi-FET process benefits linear circuits," Electronics, June 8, 1978.

4.7.2 Bi-FET op amp family from Texas Instruments, Bulletin CB-24B

4.7.3 Linear Applications Handbook, National Semiconductor (1978)

4.7.4 Linear Databook, National Semiconductor (1978)

4.7.5 Signetics Analog Data Manual (1977)

MANUFACTURER CODE: A ; DEVICE TYPE: 02 DUAL- 8 ; TEMPERATURE: +25 DEG C ; 21 SEP 79 15:52:22

PARAMETER	LO-LIM	001	002	003	004	005	006	007	008	009	010	HI-LIM	UNITS
VIO(-CM) AT 20V,-4V	-5.00	1.30	-443.M	-1.48	-104.M	-86.0M	-362.M	-1.76	-598.M	-1.82	-824.M	5.00	MV
VIO(+CM) AT 4V,-20V	-5.00	2.38	-343.M	-422.M	-275.M	146.M	-548.M	-1.98	-1.41	-1.18	-330.M	5.00	MV
VIO(0CM) AT 15V,-15V	-5.00	1.90	-621.M	-800.M	-306.M	-63.0M	-885.M	-1.91	-1.04	-1.15	-78.6M	5.00	MV
VIO(0CM) AT 5V,-5V	-5.00	1.60	-98.0M	-1.08	76.0M	-30.2M	-448.M	-1.51	-388.M	-1.18	17.8M	5.00	MV
D-VIO/D-T FROM 25 OC	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	UV/C
IIO(-CM) AT 20V,-4V	-100.	-51.8	-31.4	88.4	348. X	-3.34	5.80	-18.3	-61.2	-7.83	-13.8	100.	PA
IIO(+CM) AT 4V,-20V	-300.	73.8	189.	76.3	-233.	73.9	79.2	184.	147.	137.	81.6	300.	PA
IIO(0CM) AT 15V,-15V	-100.	-35.0	-748.M	1.05	17.2	2.83	3.36	-9.58	-6.60	-9.16	8.72	100.	PA
IIO(+CM) AT 5V,-24V	-100.	18.1	50.8	30.7	-161. X	33.2	29.3	52.2	43.5	56.4	34.3	100.	PA
+IIB(-CM) AT 20V,-4V	-200.	-140.	-163.	-98.0	-314. X	-122.	-98.8	-149.	-194.	-138.	-142.	200.	PA
+IIB(+CM) AT 4V,-20V	-200.	437.	436.	341.	691.	342.	307.	433.	465.	436.	364.	1.20K	PA
+IIB(0CM) AT 15V,-15V	-200.	-9.18	2.16	-7.74	82.0	-12.6	-19.1	-12.1	-13.4	-14.4	3.65	200.	PA
+IIB(+CM) AT 5V,-24V	-200.	175.	186.	134.	278.	132.	107.	177.	163.	178.	145.	500.	PA
-IIB(-CM) AT 20V,-4V	-200.	-89.1	-131.	-120.	-656. X	-118.	-104.	-137.	-133.	-130.	-128.	200.	PA
-IIB(+CM) AT 4V,-20V	-200.	364.	306.	265.	824.	268.	228.	309.	308.	299.	273.	1.20K	PA
-IIB(0CM) AT 15V,-15V	-200.	25.8	2.90	-8.79	4.80	-15.5	-22.4	-2.49	-6.79	-5.25	-5.07	200.	PA
-IIB(+CM) AT 5V,-24V	-200.	156.	135.	104.	438.	99.3	78.2	125.	120.	122.	110.	500.	PA
+PSRR AT 5V,-16V	80.0	89.9	107.	104.	93.6	90.9	90.5	115.	92.5	88.4	93.9	0.00	dB
-PSRR AT 16V,-5V	80.0	89.4	88.6	200.	91.3	99.0	91.3	84.5	83.1	93.0	91.6	0.00	dB
CMR AT 16V,-16V	80.0	87.7	108.	87.2	103.	99.9	102.	102.	89.3	116.	106.	0.00	dB
IOS(+) AT 15V,-15V	-40.0	-8.70	-8.15	-8.55	-8.10	-9.20	-9.10	-8.60	-8.45	-8.55	-8.75	0.00	MA
IOS(-) AT 15V,-15V	0.00	5.85	5.65	5.85	5.60	6.40	6.40	6.65	6.60	6.20	6.20	40.0	MA
ICC AT 15V,-15V	0.00	335.MX	300.M	310.MX	235.M	305.MX	355.MX	300.M	320.MX	300.M	335.MX	300.M	MA
+VOP AT RL=10K	12.0	15.2	15.2	15.1	15.2	15.2	15.2	15.2	15.2	15.2	15.2	0.00	V
-VOP AT RL=10K	0.00	-14.9	-14.8	-14.9	-14.8	-14.9	-14.9	-14.9	-14.9	-14.9	-14.9	-12.0	V
+VOP AT RL=2K	10.0	14.7	14.6	14.6	14.6	14.7	14.6	14.6	14.6	14.6	14.6	0.00	V
-VOP AT RL=2K	0.00	-8.95 X	-8.80 X	-9.10 X	-8.80 X	-9.05 X	-9.05 X	-10.0	-8.90 X	-9.65 X	-9.60 X	-10.0	V
AVS(+) AT RL=10K	5.00	13.1	15.3	12.8	15.2	14.3	13.8	15.3	13.2	13.6	14.4	0.00	V/MV
AVS(-) AT RL=10K	5.00	6.08	5.23	5.31	5.22	6.40	6.12	6.25	6.06	5.76	6.07	0.00	V/MV
AVS(+) AT RL=2K	5.00	8.12	7.85	6.67	7.47	7.99	7.92	8.63	7.84	7.69	7.88	0.00	V/MV
AVS(-) AT RL=2K	5.00	877.MX	817.MX	799.MX	883.MX	838.MX	903.MX	760.MX	784.MX	776.MX	839.MX	0.00	V/MV
AVS AT 5V,-5V,RL=10K	2.00	2.00	2.21	7.55	2.00	2.77	2.05	2.09	2.39	2.33	2.36	0.00	V/MV
AVS AT 5V,-5V,RL=2K	2.00	2.25	1.88 X	1.91 X	1.86 X	2.34	2.26	2.30	2.23	2.10	2.24	0.00	V/MV
SR(+) AT 16V,-16V	2.00	2.40	1.96 X	2.24	1.98 X	2.41	2.37	2.36	2.34	2.30	2.36	0.00	V/US
SR(-) AT 16V,-16V	2.00	4.24	2.89	4.82	2.96	4.67	4.63	4.55	4.44	4.30	4.67	0.00	V/US

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 4-1. Typical type 02 data at 25°C.

MANUFACTURER CODE: TT; DEVICE TYPE: 02 DUAL- 2 ; TEMPERATURE: -55 DEG C ; 27 SEP 79 10:26:32

PARAMETER	LO-LIM	001	002	003	004	005	006	007	008	009	010	HI-LIM	UNIT
VIO(-CM) AT 28V,-4V	-7.00	1.11	348.M	361.M	-936.M	-885.M	-484.M	-1.78	90.0M	-1.86	818.M	7.00	MV
VIO(+CM) AT 4V,-28V	-7.00	0.13	884.M	1.40	-1.06	-349.M	-663.M	-1.98	-886.M	-1.80	-88.0M	7.00	MV
VIO(0CM) AT 16V,-16V	-7.00	1.76	368.M	886.M	-1.06	-800.M	-736.M	-1.96	-845.M	-1.78	198.M	7.00	MV
VIO(0CM) AT 8V,-8V	-7.00	1.88	846.M	850.M	-720.M	-572.M	-574.M	-1.53	189.M	-1.56	382.M	7.00	MV
D-VIO/D-T FROM 25 OC	-30.0	8.94	-11.1	-23.1	9.51	6.83	825.M	562.M	-4.94	7.94	-3.47	30.0	UV/C
IIO(-CM) AT 28V,-4V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
IIO(+CM) AT 4V,-28V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
IIO(0CM) AT 16V,-16V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
IIO(+CM) AT 8V,-24V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+IIB(-CM) AT 28V,-4V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+IIB(+CM) AT 4V,-28V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+IIB(0CM) AT 16V,-16V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+IIB(+CM) AT 8V,-24V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
-IIB(-CM) AT 28V,-4V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
-IIB(+CM) AT 4V,-28V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
-IIB(0CM) AT 16V,-16V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
-IIB(+CM) AT 8V,-24V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+PSRR AT 8V,-16V	80.0	92.5	101.	94.5	101.	95.1	93.2	100.	94.5	93.2	96.3	0.00	dB
-PSRR AT 16V,-8V	80.0	91.6	91.7	103.	91.2	96.5	90.5	86.1	81.1	87.3	87.4	0.00	dB
CMR AT 16V,-16V	80.0	87.4	100.	87.2	106.	97.9	110.	99.3	87.0	105.	97.9	0.00	dB
IOS(+) AT 15V,-15V	-40.0	-11.9	-9.90	-9.65	-9.66	-11.5	-11.6	-11.4	-11.6	-11.1	-11.2	0.00	MA
IOS(-) AT 15V,-15V	0.00	6.15	5.35	4.90	5.75	6.50	6.40	6.70	6.65	6.45	6.15	40.0	MA
ICC AT 15V,-15V	0.00	305.M *	385.M *	290.M	360.M *	300.M *	285.M	305.M *	295.M	285.M	285,M	300.M	MA
+VOP AT RL=10K	12.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	0.00	V
-VOP AT RL=10K	0.00	-14.8	-14.8	-14.8	-14.8	-14.8	-14.8	-14.8	-14.8	-14.8	-14.8	-12.0	V
+VOP AT RL=2K	10.0	13.8	12.5	11.3	12.1	13.5	13.5	13.6	13.5	13.1	13.3	0.00	V
-VOP AT RL=2K	0.00	-9.00 *	-8.25 *	-7.35 *	-8.00 *	-9.00 *	-9.60 *	-9.90 *	-9.70 *	-9.60 *	-9.35 *	-10.0	V
AVS(+) AT RL=10K	4.00	11.2	12.2	7.66	12.1	11.9	11.7	12.9	11.3	11.5	12.2	0.00	V/MV
AVS(-) AT RL=10K	4.00	6.14	4.88	3.78 *	5.08	6.17	5.96	6.18	6.08	5.72	6.06	0.00	V/MV
AVS(+) AT RL=2K	4.00	5.25	4.00	858.M *	3.86 *	4.90	4.90	5.21	4.99	4.62	4.73	0.00	V/MV
AVS(-) AT RL=2K	4.00	988.M *	987.M *	906.M *	786.M *	811.M *	804.M *	744.M *	806.M *	751.M *	858.M *	0.00	V/MV
AVS AT 5V,-5V,RL=10K	2.50	3.42	7.88	4.68	7.33	8.08	8.02	8.33	8.15	7.92	7.96	0.00	V/MV
AVS AT 5V,-5V,RL=2K	2.00	2.07	1.83 *	1.18 *	1.88 *	2.07	2.01	2.09	2.04	1.91 *	2.02	0.00	V/MV
SR(+) AT 16V,-16V	1.00	1.90	1.68	1.83	1.87	1.89	1.97	1.96	1.94	1.88	1.96	0.00	V/US
SR(-) AT 16V,-16V	1.00	0.76	0.17	0.88	0.18	4.86	4.86	4.42	4.31	4.29	4.62	0.00	V/US

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 4-2. Typical type 02 data at -55°C.

MANUFACTURER CODE: A ; DEVICE TYPE: 08 DUAL- 1 ; TEMPERATURE: +125 DEG C ; 01 SEP 79 15:33:17

PARAMETER	LO-LIM	001	002	003	004	005	006	007	008	009	010	HI-LIM	UNITS
VIO(-CM) AT 20V,-4V	-7.00	2.69	1.01	2.48	2.61	-1.11	745.M	890.M	2.28	1.59	-1.18	7.00	MV
VIO(+CM) AT 4V,-20V	-7.00	1.96	1.30	2.04	3.88	-930.M	865.M	1.85	2.64	2.53	-466.M	7.00	MV
VIO(0CM) AT 10V,-10V	-7.00	2.16	1.20	2.01	3.16	-1.17	770.M	1.61	2.70	2.14	-655.M	7.00	MV
VIO(0CM) AT 5V,-5V	-7.00	2.02	1.08	2.41	2.93	-1.09	910.M	1.04	2.50	1.89	-1.07	7.00	MV
D-VIO/D-T FROM 25 OC	-30.0	2.50	8.00	9.00	18.3	3.20	2.19	7.36	9.70	10.2	6.30	30.0	UV/C
IIO(-CM) AT 20V,-4V	-20.0K	2.30K	-4.03K	-1.20K	-2.46K	490.	401.	-694.	-1.46K	-462.	-318.	20.0K	PA
IIO(+CM) AT 4V,-20V	-30.0K	-4.78K	3.36K	-1.43K	-3.34K	-1.78K	-2.36K	-1.59K	-3.13K	-1.73K	-1.67K	30.0K	PA
IIO(0CM) AT 10V,-10V	-20.0K	-3.07K	-1.78K	-2.11K	-3.46K	-530.	-793.	-936.	-2.64K	-1.13K	-988.	20.0K	PA
IIO(+CM) AT 5V,-24V	-20.0K	-3.04K	2.58K	-1.10K	-3.12K	-1.43K	-1.78K	-1.09K	-3.10K	-1.70K	-1.31K	20.0K	PA
+IIB(-CM) AT 20V,-4V	-10.0K	-24.4K	* -36.9K	* -34.5K	* -21.0K	* 140.	1.67K	1.54K	847.	2.40K	1.45K	70.0K	PA
+IIB(+CM) AT 4V,-20V	-10.0K	20.5K	35.7K	34.2K	27.8K	6.49K	9.89K	6.68K	7.54K	9.12K	8.49K	100.K	PA
+IIB(0CM) AT 10V,-10V	-10.0K	-7.65K	-4.07K	-3.52K	874.	2.69K	5.18K	3.83K	3.61K	5.43K	4.37K	70.0K	PA
+IIB(+CM) AT 5V,-24V	-10.0K	13.3K	25.0K	23.6K	20.5K	5.38K	8.63K	6.15K	6.42K	8.18K	7.45K	70.0K	PA
-IIB(-CM) AT 20V,-4V	-10.0K	-27.2K	* -32.1K	* -33.2K	* -18.5K	* -359.	1.17K	2.23K	2.31K	2.87K	1.77K	70.0K	PA
-IIB(+CM) AT 4V,-20V	-10.0K	25.2K	32.3K	35.6K	31.1K	8.21K	12.2K	8.27K	10.7K	10.9K	10.1K	100.K	PA
-IIB(0CM) AT 10V,-10V	-10.0K	-4.58K	-2.32K	-1.41K	4.33K	3.22K	5.98K	4.76K	6.15K	6.56K	5.36K	70.0K	PA
-IIB(+CM) AT 5V,-24V	-10.0K	16.4K	22.4K	24.7K	23.6K	6.81K	10.4K	7.23K	9.52K	9.89K	8.76K	70.0K	PA
+PSRR AT 5V,-15V	80.0	88.8	91.2	89.4	95.1	88.8	90.7	88.4	89.0	92.3	89.3	0.00	dB
-PSRR AT 15V,-5V	80.0	83.7	103.	84.5	103.	96.8	89.6	90.3	115.	118.	96.1	0.00	dB
CMR AT 15V,-15V	80.0	90.3	96.1	94.8	91.0	102.	109.	87.8	96.6	88.1	90.5	0.00	dB
IOS(+) AT 15V,-15V	-40.0	-5.25	-5.00	-5.05	-4.90	-6.05	-5.50	-5.70	-5.55	-5.50	-5.50	0.00	MA
IOS(-) AT 15V,-15V	0.00	4.45	4.10	4.15	3.75	5.30	4.75	4.80	4.50	4.45	4.95	40.0	MA
ICC AT 15V,-15V	0.00	315.M	* 235.M	280.M	300.M	380.M	* 300.M	300.M	300.M	300.M	300.M	300.M	MA
+VOP AT RL=10K	12.0	15.3	15.3	15.3	15.3	15.3	15.3	15.3	15.3	15.3	15.3	0.00	V
-VOP AT RL=10K	0.00	-14.8	-14.7	-14.8	-14.7	-14.8	-14.8	-14.8	-14.8	-14.8	-14.8	-12.0	V
+VOP AT RL=2K	10.0	10.4	9.86	* 9.90	* 9.65	* 11.9	10.8	11.2	10.9	10.8	10.8	0.00	V
-VOP AT RL=2K	0.00	-7.35	* -6.95	* -7.05	* -6.31	* -8.65	* -7.85	* -8.00	* -7.40	* -7.35	* -8.25	* -10.0	V
AVS(+) AT RL=10K	4.00	11.8	14.1	12.6	13.8	13.2	12.7	14.0	12.2	12.6	12.8	0.00	V/MV
AVS(-) AT RL=10K	4.00	4.49	4.08	4.29	3.90	* 4.94	4.67	5.02	4.66	4.57	4.67	0.00	V/MV
AVS(+) AT RL=2K	4.00	780.M	* 842.M	* 800.M	* 741.M	* 2.38	* 874.M	* 826.M	* 764.M	* 794.M	* 975.M	* 0.00	V/MV
AVS(-) AT RL=2K	4.00	995.M	* 925.M	* 984.M	* 1.00	* 776.M	* 891.M	* 946.M	* 1.05	* 992.M	* 806.M	* 0.00	V/MV
AVS AT 5V,-5V,RL=10K	2.00	6.84	6.90	6.56	6.40	7.34	7.08	7.55	6.90	6.96	6.96	0.00	V/MV
AVS AT 5V,-5V,RL=2K	2.00	1.72	* 1.49	* 1.60	* 1.43	* 1.86	* 1.77	* 1.91	* 1.77	* 1.78	* 1.76	* 0.00	V/MV
SR(+) AT 10V,-10V	1.00	2.48	1.87	2.85	1.96	2.48	2.41	2.39	2.38	2.35	2.40	0.00	V/US
SR(-) AT 10V,-10V	1.00	3.97	2.87	3.75	2.96	4.26	4.08	4.08	4.00	3.94	4.12	0.00	V/US

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 4-3. Typical type 02 data at 125°C.

MANUFACTURER CODE: TT; DEVICE TYPE: 153 DUAL ; TEMPERATURE: +25 DEG C ; 26 SEP 79 14:47:23

PARAMETER	LO-LIM	501-1	501-2	502-1	502-2	503-1	503-2	504-1	504-2	505-1	505-2	HI-LIM	UNIT
VIO(-CM) AT 25V,-4V	-5.00	8.60	-1.63	-3.36	3.19	-1.95	-2.30	-8.09	8.95	4.43	-1.99	5.00	MV
VIO(+CM) AT 4V,-25V	-5.00	8.08	-1.44	-8.83	4.53	-885.M	-2.08	-885.M	4.49	4.49	-1.55	5.00	MV
VIO(0CM) AT 15V,-15V	-5.00	8.10	-1.87	-3.15	3.93	-910.M	-8.13	-1.26	3.78	4.36	-1.81	5.00	MV
VIO(0CM) AT 5V,-5V	-5.00	8.46	-1.43	-3.81	3.53	-1.03	-8.86	-1.88	3.38	4.45	-1.80	5.00	MV
D-VIO/D-T FROM 25 OC	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	UV/C
IIO(-CM) AT 25V,-4V	-100.	11.0	29.5	98.0	-45.9	24.1	26.4	52.8	-18.9	79.9	30.4	100.	PA
IIO(+CM) AT 4V,-25V	-300.	-3.63	-45.9	-59.5	-144.	-61.3	217.	-23.4	-132.	-70.6	127.	300.	PA
IIO(0CM) AT 15V,-15V	-100.	-22.9	-23.7	1.10	-138. *	-31.5	216. *	-3.37	-24.8	36.3	62.0	100.	PA
IIO(+CM) AT 5V,-24V	-100.	-36.2	-31.1	-43.9	-208. *	-49.2	114. *	-13.6	-78.6	-27.5	69.2	100.	PA
+IIB(-CM) AT 25V,-4V	-200.	-19.9	-28.3	-103.	-85.8	-73.9	8.89	-117.	-23.2	-115.	8.66	200.	PA
+IIB(+CM) AT 4V,-25V	-200.	269.	223.	403.	122.	306.	436.	334.	71.8	333.	357.	1.20K	PA
+IIB(0CM) AT 15V,-15V	-200.	46.9	38.4	70.6	-78.0	44.8	274. *	32.2	33.6	83.1	128.	200.	PA
+IIB(+CM) AT 5V,-24V	-200.	126.	126.	212.	-61.7	154.	242.	162.	39.6	201.	209.	500.	PA
-IIB(-CM) AT 25V,-4V	-200.	-31.0	-57.7	-199.	-39.9	-98.0	-17.5	-169.	-4.31	-195.	-21.7	200.	PA
-IIB(+CM) AT 4V,-25V	-200.	272.	269.	463.	266.	367.	218.	357.	204.	403.	229.	1.20K	PA
-IIB(0CM) AT 15V,-15V	-200.	69.8	62.0	69.5	59.6	76.3	57.4	35.5	58.4	46.8	65.8	200.	PA
-IIB(+CM) AT 5V,-24V	-200.	162.	157.	256.	146.	203.	129.	175.	118.	228.	140.	500.	PA
+PSRR AT 5V,-15V	80.0	85.0	92.5	101.	100.	96.5	101.	98.5	118.	104.	200.	0.00	dB
-PSRR AT 15V,-5V	80.0	84.7	92.7	106.	88.2	96.1	104.	90.3	89.3	109.	101.	0.00	dB
CMR AT 15V,-15V	80.0	93.4	102.	93.1	85.1	102.	97.6	86.8	83.9	112.	94.9	0.00	dB
IOS(+) AT 15V,-15V	-80.0	-22.0	-22.2	-19.9	-20.7	-20.8	-20.6	-21.5	-21.4	-21.6	-21.6	0.00	MA
IOS(-) AT 15V,-15V	0.00	19.8	19.8	17.7	18.0	17.7	18.5	18.7	19.2	18.8	19.8	80.0	MA
ICC AT 15V,-15V	0.00	3.84 *	3.83 *	3.76 *	3.78 *	3.65 *	3.61 *	3.71 *	3.68 *	3.60 *	3.62 *	3.00	MA
+VOP AT RL=10K	12.0	15.1	15.1	15.1	15.2	15.2	15.1	15.2	15.2	15.2	15.2	0.00	V
-VOP AT RL=10K	0.00	-14.4	-14.4	-14.4	-14.4	-14.4	-14.4	-14.4	-14.4	-14.4	-14.4	-12.0	V
+VOP AT RL=2K	10.0	14.9	14.9	14.9	14.9	14.9	14.8	14.9	14.9	14.9	14.9	0.00	V
-VOP AT RL=2K	0.00	-14.2	-14.1	-14.2	-14.1	-14.2	-14.2	-14.2	-14.2	-14.2	-14.2	-10.0	V
AVS(+) AT RL=10K	50.0	300.	267.	600.	600.	545.	600.	600.	800.	600.	600.	0.00	V/MV
AVS(-) AT RL=10K	50.0	400.	400.	400.	400.	480.	600.	800.	600.	480.	343.	0.00	V/MV
AVS(+) AT RL=2K	50.0	218.	200.	300.	400.	480.	343.	400.	480.	480.	343.	0.00	V/MV
AVS(-) AT RL=2K	50.0	114.	100.	160.	185.	171.	160.	150.	800.	141.	141.	0.00	V/MV
AVS AT 5V,-5V,RL=10K	10.0	400.	160.	133.	88.9	267.	800.	133.	100.	160.	114.	0.00	V/MV
AVS AT 5V,-5V,RL=2K	10.0	88.9	80.0	114.	100.	114.	114.	88.9	114.	114.	88.9	0.00	V/MV
SR(+) AT 15V,-15V	7.00	16.7	15.4	16.4	17.2	16.1	16.1	16.7	16.9	16.4	16.1	0.00	V/US
SR(-) AT 15V,-15V	7.00	19.2	20.4	18.2	18.2	18.6	17.9	18.6	18.2	18.2	17.6	0.00	V/US

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 4-4. Typical type 05 data at 25°C.

MANUFACTURER CODE: TT; DEVICE TYPE: 153 DUAL ; TEMPERATURE: -55 DEG C ; 26 SEP 79 14:46:17

PARAMETER	LO-LIM	501-1	501-2	502-1	502-2	503-1	503-2	504-1	504-2	505-1	505-2	HI-LIM	UNIT
VIO(-CM) AT 25V,-4V	-7.00	-810.M	-3.33	-2.40	9.86 *	-1.89	-1.07	-487.M	8.95 *	4.35	885.M	7.00	MV
VIO(+CM) AT 4V,-25V	-7.00	-1.15	-2.84	-1.89	10.4 *	-800.M	-890.M	443.M	10.2 *	4.90	1.81	7.00	MV
VIO(DCM) AT 15V,-15V	-7.00	-1.23	-3.18	-2.18	9.85 *	-1.08	-875.M	318.M	9.61 *	4.84	885.M	7.00	MV
VIO(DCM) AT 5V,-5V	-7.00	-1.05	-3.14	-2.85	9.52 *	-1.22	-970.M	-374.M	9.36 *	4.28	1.00	7.00	MV
D-VIO/D-T FROM 25 OC	-30.0	41.6 *	80.1	-18.1	-74.1 *	8.12	-15.8	-10.7	-72.9 *	-6.12	-35.1 *	30.0	UV/C
IIO(-CM) AT 25V,-4V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
IIO(+CM) AT 4V,-25V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
IIO(DCM) AT 15V,-15V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
IIO(+CM) AT 5V,-25V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+IIB(-CM) AT 25V,-4V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+IIB(+CM) AT 4V,-25V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+IIB(DCM) AT 15V,-15V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+IIB(+CM) AT 5V,-25V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
-IIB(-CM) AT 25V,-4V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
-IIB(+CM) AT 4V,-25V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
-IIB(DCM) AT 15V,-15V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
-IIB(+CM) AT 5V,-25V	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	PA
+PSRR AT 5V,-15V	80.0	94.3	93.2	95.8	107.	95.5	97.6	95.1	103.	93.7	97.6	0.00	dB
-PSRR AT 15V,-5V	80.0	94.8	94.8	107.	94.8	96.5	96.5	105.	94.0	96.5	107.	0.00	dB
CMR AT 15V,-15V	80.0	100.	95.9	93.4	86.4	97.6	102.	88.1	85.9	104.	97.2	0.00	dB
IOS(+) AT 15V,-15V	-80.0	-26.0	-21.4	-25.7	-26.5	-26.9	-25.7	-27.9	-27.1	-27.7	-26.8	0.00	MA
IOS(-) AT 15V,-15V	0.00	27.4	27.0	25.0	25.0	25.3	25.6	26.5	26.4	26.7	27.0	80.0	MA
ICC AT 15V,-15V	0.00	3.96 *	3.93 *	3.88 *	3.85 *	3.76 *	3.65 *	3.81 *	3.79 *	3.68 *	3.67 *	3.50	MA
+VOP AT RL=10K	12.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	15.0	0.00	V
-VOP AT RL=10K	0.00	-14.2	-14.2	-14.2	-14.2	-14.2	-14.2	-14.2	-14.2	-14.2	-14.2	-12.0	V
+VOP AT RL=2K	10.0	14.8	14.8	14.8	14.8	14.8	14.8	14.8	14.8	14.8	14.8	0.00	V
-VOP AT RL=2K	0.00	-13.9	-13.9	-13.9	-13.9	-13.9	-13.9	-13.9	-13.9	-13.9	-13.9	-10.0	V
AVS(+) AT RL=10K	25.0	240.	218.	300.	600.	600.	511.	600.	300.	600.	750.	0.00	V/MV
AVS(-) AT RL=10K	25.0	267.	240.	600.	480.	600.	348.	615.	400.	400.	490.	0.00	V/MV
AVS(+) AT RL=2K	25.0	133.	104.	218.	343.	300.	231.	393.	480.	300.	320.	0.00	V/MV
AVS(-) AT RL=2K	25.0	96.0	82.8	200.	218.	218.	200.	198.	240.	150.	170.	0.00	V/MV
AVS AT 5V,-5V,RL=10K	10.0	400.	88.8	100.	80.0	200.	133.	190.	100.	160.	121.	0.00	V/MV
AVS AT 5V,-5V,RL=2K	10.0	80.0	57.1	80.0	88.9	200.	114.	183.	100.	133.	93.0	0.00	V/MV
SR(+) AT 15V,-15V	5.00	15.8	13.3	15.6	17.8	15.8	14.9	16.4	16.7	16.1	15.4	0.00	V/US
SR(-) AT 15V,-15V	5.00	17.9	18.6	17.9	17.5	17.5	16.9	17.6	17.9	17.2	16.9	0.00	V/US

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 4-5. Typical type 05 data at -55°C.

MANUFACTURER CODE: TT; DEVICE TYPE: 153 DUAL . ; TEMPERATURE: +125 DEG C ; 26 SEP 79 14:46:16

PARAMETER	LO-LIM	581-1	581-2	582-1	582-2	583-1	583-2	584-1	584-2	585-1	585-2	HI-LIM	UNITS
VIO(-CM) AT 28V,-4V	-7.00	5.65	-1.02	-3.63	-976.M	-1.24	-3.76	-3.64	-2.18	3.38	-4.86	7.00	MV
VIO(+CM) AT 4V,-28V	-7.00	4.86	-1.03	-3.17	400.M	-1.14	-3.36	-2.44	-467.M	3.39	-4.38	7.00	MV
VIO(0CM) AT 16V,-16V	-7.00	4.83	-1.08	-3.48	-841.M	-1.16	-3.60	-2.80	-1.27	3.24	-4.68	7.00	MV
VIO(0CM) AT 5V,-5V	-7.00	5.42	-876.M	-3.51	-876.M	-1.26	-3.63	-3.37	-1.72	3.38	-4.86	7.00	MV
D-VIO/D-T FROM 25 OC	-30.0	28.3	4.90	-3.30	-41.7	x -2.56	-13.7	-16.4	-60.6	x -11.1	-28.7	30.0	UV/C
IIO(-CM) AT 28V,-4V	-20.0K	-968.	-900.	-1.26K	-304.	-1.56K	-1.40K	-1.21K	-821.	-1.36K	-1.47K	20.0K	PA
IIO(+CM) AT 4V,-28V	-30.0K	-1.42K	-1.20K	-138.	-488.	-467.	-1.17K	-939.	-986.	-865.	-1.54K	30.0K	PA
IIO(0CM) AT 16V,-16V	-20.0K	-880.	-1.02K	-764.	-631.	-1.15K	-1.09K	-1.16K	-974.	-938.	-1.44K	20.0K	PA
IIO(+CM) AT 5V,-24V	-20.0K	-1.06K	-1.05K	-203.	-757.	-899.	-1.13K	-942.	-989.	-812.	-1.25K	20.0K	PA
+IIB(-CM) AT 28V,-4V	-10.0K	8.30K	4.36K	3.03K	4.20K	3.08K	6.98K	9.00K	3.30K	10.5K	9.92K	70.0K	PA
+IIB(+CM) AT 4V,-28V	-10.0K	19.6K	16.6K	14.6K	14.0K	12.3K	16.4K	20.5K	10.8K	25.2K	21.5K	100.K	PA
+IIB(0CM) AT 16V,-16V	-10.0K	14.6K	10.8K	8.96K	9.02K	7.63K	12.0K	15.0K	7.23K	18.5K	16.3K	70.0K	PA
+IIB(+CM) AT 5V,-24V	-10.0K	18.5K	15.0K	13.2K	12.3K	10.7K	15.0K	18.8K	9.81K	23.2K	20.1K	70.0K	PA
-IIB(-CM) AT 28V,-4V	-10.0K	9.25K	5.25K	4.29K	4.50K	4.64K	8.38K	10.2K	4.12K	11.9K	11.4K	70.0K	PA
-IIB(+CM) AT 4V,-28V	-10.0K	21.0K	17.8K	14.8K	14.5K	12.7K	17.5K	21.4K	11.8K	26.1K	23.0K	100.K	PA
-IIB(0CM) AT 16V,-16V	-10.0K	15.4K	11.8K	9.71K	9.65K	8.78K	13.1K	16.1K	8.21K	19.5K	17.8K	70.0K	PA
-IIB(+CM) AT 5V,-24V	-10.0K	19.6K	16.0K	13.4K	13.1K	11.6K	16.1K	19.7K	10.8K	24.0K	21.3K	70.0K	PA
+PSRR AT 5V,-16V	80.0	103.	105.	124.	95.4	110.	124.	103.	93.5	118.	106.	0.00	dB
-PSRR AT 16V,-5V	80.0	112.	110.	98.5	96.5	110.	102.	95.1	95.8	118.	105.	0.00	dB
CMR AT 16V,-16V	80.0	89.5	124.	94.3	84.8	109.	95.7	86.7	82.9	124.	93.9	0.00	dB
IOS(+) AT 15V,-15V	-80.0	-16.0	-15.4	-13.9	-14.1	-14.3	-13.5	-13.9	-14.6	-14.0	-14.1	0.00	MA
IOS(-) AT 15V,-15V	0.00	10.7	11.3	10.4	10.3	10.2	9.85	9.75	10.9	9.55	10.3	80.0	MA
ICC AT 15V,-15V	0.00	3.12 x	2.74	3.31 x	2.67	3.00 x	2.88	3.28 x	3.03 x	2.85	2.73	3.00	MA
+VOP AT RL=10K	12.0	15.3	15.3	15.3	15.3	15.3	15.3	15.3	15.3	15.3	15.3	0.00	V
-VOP AT RL=10K	0.00	-14.7	-14.7	-14.7	-14.7	-14.7	-14.7	-14.7	-14.7	-14.7	-14.7	-12.0	V
+VOP AT RL=2K	10.0	14.9	14.9	14.9	14.9	14.9	14.9	14.9	14.9	14.9	14.9	0.00	V
-VOP AT RL=2K	0.00	-14.3	-14.2	-14.2	-14.2	-14.2	-14.2	-14.3	-14.3	-14.3	-14.3	-10.0	V
AVS(+) AT RL=10K	25.0	300.	222.	343.	400.	343.	867.	343.	400.	867.	300.	0.00	V/MV
AVS(-) AT RL=10K	25.0	867.	867.	867.	363.	400.	867.	300.	300.	867.	867.	0.00	V/MV
AVS(+) AT RL=2K	25.0	218.	200.	867.	316.	300.	218.	840.	867.	840.	218.	0.00	V/MV
AVS(-) AT RL=2K	25.0	77.4	76.0	104.	117.	100.	88.9	88.9	100.	72.7	75.0	0.00	V/MV
AVS AT 5V,-5V,RL=10K	10.0	114.	100.	133.	113.	133.	114.	114.	100.	88.9	88.9	0.00	V/MV
AVS AT 5V,-5V,RL=2K	10.0	66.7	66.7	88.9	87.9	72.7	72.7	80.0	66.7	61.5	61.5	0.00	V/MV
SR(+) AT 16V,-16V	5.00	16.1	15.2	15.4	16.1	15.2	15.4	15.2	15.6	14.9	14.9	0.00	V/US
SR(-) AT 16V,-16V	5.00	18.2	19.6	17.5	17.2	17.2	16.7	17.5	17.2	16.9	16.7	0.00	V/US

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

Table 4-6. Typical type 05 data at 125°C.

STATISTICAL DATA FOR *DEVICE TYPES MIL/119-01, 02, 03 @ +25 DEGREES C 04 OCT 79 13:48:44

PARAMETER	LOW VALUE 1./	HIGH VALUE 1./	MEAN 1./	SIGMA 1./	SAMPLE SIZE 1./	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW 2./	LOW LIMIT	LOW REJ	LO-FM 3./ 1./	% FAIL HIGH 2./	HIGH LIMIT	HIGH REJ	UNITS
VIO(-CM) AT 28V,-4V	-6.76	6.99	-822.M	2.80	51	94.1	100.	3.92	-5.00	-10.0	1.49	3.92	5.00	10.0	MV
VIO(+CM) AT 4V,-28V	-6.50	6.77	-610.M	2.67	51	94.1	100.	1.96	-5.00	-10.0	1.64	1.96	5.00	10.0	MV
VIO(OCM) AT 16V,-16V	-6.67	6.70	-717.M	2.72	51	94.1	100.	1.96	-5.00	-10.0	1.57	1.96	5.00	10.0	MV
VIO(OCM) AT 5V,-5V	-6.15	7.68	-551.M	2.69	51	94.1	98.0	3.92	-5.00	-10.0	1.65	3.92	5.00	10.0	MV
IIO(-CM) AT 28V,-4V	-281.	205.	-3.20	94.2	46	84.3	90.2	(19.6)	-100.	-300.	1.03	(9.80)	100.	300.	PA
IIO(+CM) AT 4V,-28V	-323.	250.	62.0	95.5	49	92.2	92.2	1.96	-300.	-600.	3.79	3.92	300.	600.	PA
IIO(OCM) AT 16V,-16V	-230.	155.	-1.03	72.6	50	88.2	96.1	(7.84)	-100.	-300.	1.36	(9.80)	100.	300.	PA
IIO(+CM) AT 8V,-24V	-189.	175.	27.9	60.2	49	88.2	92.2	(7.84)	-100.	-300.	2.12	(11.8)	100.	300.	PA
+IIB(-CM) AT 28V,-4V	-465.	164.	-152.	140.	46	84.3	90.2	(33.3)	-200.	-500.	343.M	0.00	200.	400.	PA
+IIB(+CM) AT 4V,-28V	270.	2.06K	541.	359.	51	94.1	94.1	0.00	-200.	-500.	2.07	(5.88)	1.20K	2.50K	PA
+IIB(OCM) AT 16V,-16V	-222.	373.	3.43	86.6	51	92.2	98.0	1.96	-200.	-500.	2.35	3.92	200.	400.	PA
+IIB(+CM) AT 8V,-24V	-213.	324.	169.	84.5	47	90.2	92.2	1.96	-200.	-500.	4.37	(5.88)	500.	400.	PA
-IIB(-CM) AT 28V,-4V	-421.	-37.3	-163.	89.5	48	90.2	94.1	(33.3)	-200.	-500.	409.M	0.00	200.	400.	PA
-IIB(+CM) AT 4V,-28V	228.	1.92K	449.	275.	51	96.1	98.0	0.00	-200.	-500.	2.36	1.96	1.20K	2.50K	PA
-IIB(OCM) AT 16V,-16V	-76.2	170.	-3.00	39.5	51	96.1	98.0	0.00	-200.	-500.	4.98	0.00	200.	400.	PA
-IIB(+CM) AT 8V,-24V	70.3	312.	148.	52.3	47	86.3	90.2	0.00	-200.	-500.	6.66	3.92	500.	400.	PA
+PSRR AT 8V,-16V	79.4	118.	95.9	7.83	50	90.2	98.0	1.96	80.0	60.0	2.03	0.00	2.00K	140.	DB
-PSRR AT 16V,-8V	75.4	124.	91.0	9.49	50	92.2	96.1	3.92	80.0	60.0	1.16	0.00	2.00K	140.	DB
CMR AT 16V,-16V	84.3	128.	95.8	9.26	51	96.1	98.0	0.00	80.0	60.0	1.71	0.00	2.00K	140.	DB
IOS(+) AT 15V,-15V	-11.8	-8.10	-10.0	1.19	51	100.	100.	0.00	-40.0	-100.	25.2	0.00	1.00K	0.00	NA
IOS(-) AT 15V,-15V	4.55	9.45	6.93	1.21	51	98.0	100.	0.00	-1.00K	0.00	833.	0.00	40.0	100.	NA
+VOP AT RL=10K	15.1	15.2	15.2	27.1M	51	98.0	100.	0.00	12.0	8.00	117.	0.00	200.	16.0	V
-VOP AT RL=10K	-14.9	-14.3	-14.9	84.3M	51	98.0	98.0	0.00	-200.	-16.0	2.20K	0.00	-12.0	-8.00	V
+VOP AT RL=2K	14.8	14.8	14.6	78.9M	51	94.1	96.1	0.00	10.0	8.00	58.8	0.00	200.	16.0	V
-VOP AT RL=2K	-10.9	-8.00	-9.76	730.M	50	96.1	98.0	0.00	-200.	-16.0	261.	(62.7)	-10.0	-8.00	V
AVS(+) AT RL=10K	2.73	15.5	12.7	1.93	51	98.0	98.0	1.96	5.00	0.00	3.98	0.00	100.K	100.	V/MV
AVS(-) AT RL=10K	2.46	7.85	6.20	958.M	51	98.0	98.0	3.92	5.00	0.00	1.25	0.00	100.K	100.	V/MV
AVS(+) AT RL=2K	2.13	8.96	7.42	1.22	51	96.1	98.0	3.92	5.00	0.00	1.98	0.00	100.K	100.	V/MV
AVS(-) AT RL=2K	569.M	1.65	831.M	184.M	51	98.0	98.0	100.	5.00	0.00	-22.7	0.00	100.K	100.	V/MV
AVS AT 5V,-5V,RL=10K	2.58	9.30	7.95	1.03	51	98.0	98.0	0.00	2.00	0.00	5.79	0.00	10.0K	100.	V/MV
AVS AT 5V,-5V,RL=2K	964.M	3.08	2.30	396.M	51	98.0	98.0	(17.6)	2.00	0.00	764.M	0.00	10.0K	100.	V/MV
SR(+) AT 16V,-16V	762.M	3.38	2.70	492.M	51	98.0	98.0	(9.80)	2.00	0.00	1.42	0.00	25.0	40.0	V/US
SR(-) AT 16V,-16V	763.M	6.80	5.30	1.28	51	98.0	98.0	1.96	2.00	0.00	2.58	0.00	25.0	40.0	V/US

NOTES:
1./ EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ
2./ % FAIL VALUES >OR= 5% ARE CIRCLED
3./ FIGURE OF MERIT DEFINITIONS: LO-FM=(MEAN-LOW LIMIT)/SIGMA
HI-FM=(HI LIMIT-MEAN)/SIGMA
4./ THE % FAIL FOR ICC IS NOT VALID SINCE THE DUAL AND QUAD DEVICES ARE COMPARED TO THE SINGLE LIMIT
5./ THERE IS NO MAXIMUM FAIL LIMIT FOR GAIN AND SLEW RATE

Table 4-7. Statistical summary of types 01, 02 & 03 at 25°C.

STATISTICAL DATA FOR *DEVICE TYPES MIL/119-01, 02, 03 @ -55 DEGREES C 04 OCT 79 13:55:11

PARAMETER	LOW VALUE 1./	HIGH VALUE 1./	MEAN 1./	SIGMA 1./	SAMPLE SIZE 1./	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW 2./	LOW LIMIT	LOW REJ	LO-FM 3./ 1./	% FAIL HIGH 2./	HIGH LIMIT	HIGH REJ	UNITS
VIO(-CM) AT 24V,-4V	-7.91	2.87	-1.40	2.47	49	88.2	96.1	(5.88)	-7.00	-10.0	2.26	1.96	7.00	10.0	MV
VIO(+CM) AT 4V,-24V	-9.38	3.69	-1.30	2.59	50	92.2	96.1	1.96	-7.00	-10.0	2.20	1.96	7.00	10.0	MV
VIO(OCM) AT 16V,-16V	-9.73	3.49	-1.46	2.68	50	92.2	96.1	3.92	-7.00	-10.0	2.07	1.96	7.00	10.0	MV
VIO(OCM) AT 5V,-5V	-9.03	2.93	-1.29	2.61	50	92.2	98.0	3.92	-7.00	-10.0	2.19	1.96	7.00	10.0	MV
+PSRR AT 8V,-16V	84.1	115.	96.2	5.55	50	92.2	96.1	0.00	80.0	60.0	2.91	0.00	2.00K	100.	DB
-PSRR AT 16V,-8V	71.8	118.	91.1	7.98	51	96.1	98.0	1.96	80.0	60.0	1.39	0.00	2.00K	100.	DB
CMR AT 16V,-16V	82.6	128.	97.3	10.7	51	94.1	100.	0.00	80.0	60.0	1.62	0.00	2.00K	100.	DB
IOS(+) AT 15V,-15V	-14.7	-8.00	-11.9	1.68	51	96.1	100.	0.00	-40.0	-100.	16.7	0.00	1.00K	0.00	NA
IOS(-) AT 15V,-15V	2.80	9.90	7.00	1.39	51	96.1	98.0	0.00	-1.00K	0.00	724.	0.00	40.0	100.	NA
+VOP AT RL=10K	15.0	15.1	15.0	7.00M	51	98.0	98.0	0.00	12.0	8.00	429.	0.00	200.	16.0	V
-VOP AT RL=10K	-14.9	-14.8	-14.8	28.9M	50	94.1	98.0	0.00	-200.	-16.0	6.42K	1.96	-12.0	-8.00	V
+VOP AT RL=2K	10.2	14.7	13.5	1.09	51	94.1	100.	0.00	10.0	8.00	3.18	0.00	200.	16.0	V
-VOP AT RL=2K	-11.4	-8.25	-9.89	861.M	48	94.1	98.0	0.00	-200.	-16.0	221.	(58.8)	-10.0	-8.00	V
AVS(+) AT RL=10K	1.67	12.9	10.5	1.94	51	96.1	98.0	1.96	4.00	0.00	3.36	0.00	105.K	100.	V/MV
AVS(-) AT RL=10K	3.78	7.67	5.92	854.M	51	96.1	100.	1.96	4.00	0.00	2.25	0.00	105.K	100.	V/MV
AVS(+) AT RL=2K	858.M	7.52	4.55	1.50	51	92.2	100.	(25.5)	4.00	0.00	364.M	0.00	105.K	100.	V/MV
AVS(-) AT RL=2K	567.M	5.22	878.M	631.M	51	98.0	98.0	(98.0)	4.00	0.00	-4.95	0.00	105.K	100.	V/MV
AVS AT 5V,-5V,RL=10K	1.95	9.52	7.19	1.31	51	98.0	98.0	1.96	2.00	0.00	3.96	0.00	105.K	100.	V/MV
AVS AT 5V,-5V,RL=2K	1.14	2.58	1.96	344.M	51	96.1	100.	(45.1)	2.00	0.00	-105.M	0.00	105.K	100.	V/MV
SR(+) AT 16V,-16V	733.M	2.62	2.19	359.M	51	98.0	98.0	1.96	1.00	0.00	3.31	0.00	50.0	40.0	V/US
SR(-) AT 16V,-16V	739.M	6.54	5.00	1.49	51	98.0	100.	1.96	1.00	0.00	2.69	0.00	50.0	40.0	V/US

NOTES:
1./ EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ
2./ % FAIL VALUES >OR= 5% ARE CIRCLED
3./ FIGURE OF MERIT DEFINITIONS: LO-FM=(MEAN-LOW LIMIT)/SIGMA
HI-FM=(HI LIMIT-MEAN)/SIGMA
4./ THE % FAIL FOR ICC IS NOT VALID SINCE THE DUAL AND QUAD DEVICES ARE COMPARED TO THE SINGLE LIMIT
5./ THERE IS NO MAXIMUM FAIL LIMIT FOR GAIN AND SLEW RATE

Table 4-8. Statistical summary of types 01, 02 & 03 at -55°C.

STATISTICAL DATA FOR *DEVICE TYPES MIL/119-01, 02, 03 @ +125 DEGREES C 04 OCT 79 14:02:54

PARAMETER	LOW VALUE 1./	HIGH VALUE 1./	MEAN 1./	SIGMA 1./	SAMPLE SIZE 1./	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW 2./	LOW LIMIT	LOW REJ	LO-FM 3./	% FAIL HIGH 2./	HIGH LIMIT	HIGH REJ	UNITS
VIO(-CM) AT 2[illegible],-4V	-5.41	7.12	-615.M	3.10	50	92.2	98.0	1.96	-7.00	-10.0	2.06	1.96	7.00	10.0	MV
VIO(+CM) AT [illegible],-28V	-5.40	6.64	-346.M	2.90	50	90.2	98.0	0.00	-7.00	-10.0	2.29	1.96	7.00	10.0	MV
VIO(0CM) AT 15V,-16V	-5.52	6.50	-472.M	2.96	50	92.2	98.0	0.00	-7.00	-10.0	2.20	1.96	7.00	10.0	MV
VIO(0CM) AT 5V,-5V	-5.01	7.32	-281.M	2.90	50	92.2	98.0	1.96	-7.00	-10.0	2.32	1.96	7.00	10.0	MV
D-VIO/D-T FROM 25 OC	-10.9	24.6	1.98	8.61	50	94.1	98.0	0.00	-30.0	-50.0	3.72	1.96	30.0	50.0	PA
IIO(-CM) AT 2[illegible],-4V	-4.97K	8.00K	-943.	2.43K	51	96.1	98.0	0.00	-20.0K	-40.0K	7.83	0.00	20.0K	40.0K	PA
IIO(+CM) AT [illegible],-28V	-10.6K	19.3K	-2.75K	5.12K	50	96.1	96.1	0.00	-30.0K	-40.0K	5.32	1.96	30.0K	40.0K	PA
IIO(0CM) AT 16V,-16V	-8.02K	5.10K	-2.36K	2.70K	49	90.2	96.1	0.00	-20.0K	-40.0K	6.54	3.92	20.0K	40.0K	PA
IIO(+CM) AT [illegible],-24V	-17.2K	6.56K	-2.96K	4.12K	50	94.1	96.1	0.00	-20.0K	-40.0K	4.14	1.96	20.0K	40.0K	PA
+IIB(-CM) AT 28V,-4V	-365.	36.5K	9.10K	8.16K	47	88.2	90.2	(7.84)	-10.0K	-10.0K	2.34	0.00	70.0K	110.K	PA
+IIB(+CM) AT 4V,-28V	-276.	55.5K	22.4K	10.9K	50	92.2	96.1	0.00	-10.0K	-10.0K	2.98	1.96	100.K	110.K	PA
+IIB(0CM) AT 16V,-16V	-7.65K	71.0K	14.7K	12.8K	51	96.1	98.0	0.00	-10.0K	-10.0K	1.93	1.96	70.0K	110.K	PA
+IIB(+CM) AT 8V,-24V	237.	53.7K	19.7K	10.0K	50	94.1	96.1	0.00	-10.0K	-10.0K	2.96	1.96	70.0K	110.K	PA
-IIB(-CM) AT 28V,-4V	-359.	41.5K	10.0K	9.32K	47	88.2	90.2	(7.84)	-10.0K	-10.0K	2.15	0.00	70.0K	110.K	PA
-IIB(+CM) AT 4V,-28V	-209.	66.1K	24.9K	12.2K	51	94.1	98.0	0.00	-10.0K	-10.0K	2.85	0.00	100.K	110.K	PA
-IIB(0CM) AT 16V,-16V	-4.58K	55.3K	16.0K	11.4K	50	94.1	96.1	1.96	-10.0K	-10.0K	2.28	0.00	70.0K	110.K	PA
-IIB(+CM) AT 8V,-24V	313.	63.8K	22.4K	11.5K	51	96.1	98.0	0.00	-10.0K	-10.0K	2.81	0.00	70.0K	110.K	DB
+PSRR AT 8V,-16V	82.0	124.	97.4	9.99	49	88.2	96.1	1.96	80.0	50.0	1.74	0.00	2.00K	150.	DB
-PSRR AT 16V,-8V	78.0	118.	91.6	8.79	50	92.2	96.1	(5.88)	80.0	50.0	1.32	0.00	2.00K	150.	DB
CMR AT 16V,-16V	58.9	128.	94.6	10.3	51	96.1	96.1	1.96	80.0	50.0	1.42	0.00	2.00K	150.	MA
IOS(+) AT 15V,-15V	-7.55	0.00	-6.11	1.19	51	98.0	98.0	0.00	-40.0	-100.	28.4	0.00	1.00K	0.00	MA
IOS(-) AT 15V,-15V	0.00	7.10	5.20	1.38	51	96.1	96.1	0.00	-1.00K	0.00	728.	0.00	40.0	100.	MA
+VOP AT RL=10K	15.3	15.3	15.3	21.7M	49	96.1	96.1	3.92	12.0	8.00	150.	0.00	200.	16.0	V
-VOP AT RL=10K	-14.9	-13.6	-14.8	189.M	49	94.1	94.1	0.00	-200.	-16.0	980.	3.92	-12.0	-8.00	V
+VOP AT RL=2K	9.65	14.4	12.2	1.51	49	96.1	96.1	(13.7)	10.0	8.00	1.43	0.00	200.	16.0	V
-VOP AT RL=2K	-9.65	-8.00	-8.70	436.M	34	70.6	80.4	0.00	-200.	-16.0	439.	100.	-10.0	-8.00	V
AVS(+) AT RL=10K	440.M	14.5	11.3	2.33	51	96.1	96.1	3.92	4.00	0.00	3.15	0.00	105.K	100.	V/MV
AVS(-) AT RL=10K	455.M	6.42	4.71	1.14	51	94.1	96.1	(9.80)	4.00	0.00	627.M	0.00	105.K	100.	V/MV
AVS(+) AT RL=2K	440.M	7.27	3.29	2.17	51	100.	100.	(52.9)	4.00	0.00	-326.M	0.00	105.K	100.	V/MV
AVS(-) AT RL=2K	571.M	1.55	856.M	230.M	51	92.2	98.0	(100)	4.00	0.00	-13.7	0.00	105.K	100.	V/MV
AVS AT 5V,-5V,RL=10K	147.M	7.55	6.39	1.38	51	94.1	96.1	3.92	2.00	0.00	3.18	0.00	105.K	100.	V/MV
AVS AT 5V,-5V,RL=2K	147.M	2.55	1.80	465.M	51	96.1	96.1	(72.5)	2.00	0.00	-429.M	0.00	105.K	100.	V/MV
SR(+) AT 16V,-16V	5.00U	3.58	2.70	659.M	51	96.1	98.0	3.92	1.00	0.00	2.58	0.00	50.0	40.0	V/US
SR(-) AT 16V,-16V	5.00U	6.25	4.58	1.31	51	96.1	98.0	3.92	1.00	0.00	2.74	0.00	50.0	40.0	V/US

NOTES:
1./ EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ
2./ % FAIL VALUES >OR= 5% ARE CIRCLED
3./ FIGURE OF MERIT DEFINITIONS: LO-FM=(MEAN-LOW LIMIT)/SIGMA
HI-FM=(HI LIMIT-MEAN)/SIGMA
4./ THE % FAIL FOR ICC IS NOT VALID SINCE THE DUAL AND QUAD DEVICES ARE COMPARED TO THE SINGLE LIMIT
5./ THERE IS NO MAXIMUM FAIL LIMIT FOR GAIN AND SLEW RATE

Table 4-9. Statistical summary of types 01, 02 & 03 at 125°C.

STATISTICAL DATA FOR *DEVICE TYPES MIL/119-04, 05, 06 @ +25 DEGREES C 03 OCT 79 15:06:20

PARAMETER	LOW VALUE 1./	HIGH VALUE 1./	MEAN 1./	SIGMA 1./	SAMPLE SIZE 1./	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW 2./	LOW LIMIT	LOW REJ	LO-FM 3./ 1./	% FAIL HIGH 2./	HIGH LIMIT	HIGH REJ	HI-FM 3./ 1./	UNITS
VIO(-CM) AT 28V,-4V	-5.37	5.96	-83.3M	2.29	81	95.1	100.	1.23	-5.00	-10.0	2.15	1.23	5.00	10.0	2.22	MV
VIO(+CM) AT 4V,-28V	-4.59	4.60	-183.M	2.35	81	97.5	100.	0.00	-5.00	-10.0	2.05	0.00	5.00	10.0	2.20	MV
VIO(0CM) AT 16V,-16V	-4.84	4.49	-288.M	2.37	81	98.8	100.	0.00	-5.00	-10.0	1.98	0.00	5.00	10.0	2.23	MV
VIO(0CM) AT 5V,-5V	-5.13	6.16	133.M	2.34	81	96.3	100.	1.23	-5.00	-10.0	2.19	2.47	5.00	10.0	2.08	MV
IIO(-CM) AT 28V,-4V	-295.	204.	20.6	102.	74	86.4	91.4	12.3	-100.	-300.	1.18	19.8	100.	300.	778.M	PA
IIO(+CM) AT 4V,-28V	-290.	513.	59.2	140.	74	87.7	88.9	2.47	-300.	-600.	2.56	11.1	300.	600.	1.72	PA
IIO(0CM) AT 16V,-16V	-283.	216.	7.47	83.0	75	82.7	90.1	11.1	-100.	-300.	1.29	11.1	100.	300.	1.11	PA
IIO(+CM) AT 8V,-24V	-208.	278.	21.7	83.4	73	84.0	88.9	8.64	-100.	-300.	1.46	21.0	100.	300.	939.M	PA
+IIB(-CM) AT 28V,-4V	-426.	377.	-78.9	147.	73	85.2	90.1	32.1	-200.	-500.	822.M	3.70	200.	400.	1.89	PA
+IIB(+CM) AT 4V,-28V	-407.	2.27K	703.	558.	79	93.8	98.8	2.47	-200.	-500.	1.62	19.8	1.20K	2.50K	892.M	PA
+IIB(0CM) AT 16V,-16V	-332.	318.	63.9	109.	75	86.4	91.4	6.17	-200.	-500.	2.43	9.88	200.	400.	1.25	PA
+IIB(+CM) AT 8V,-24V	-358.	388.	161.	133.	54	66.7	81.5	2.47	-200.	-500.	2.72	21.0	500.	400.	2.56	PA
-IIB(-CM) AT 28V,-4V	-494.	53.7	-148.	130.	79	93.8	97.5	30.9	-200.	-500.	402.M	0.00	200.	400.	2.69	PA
-IIB(+CM) AT 4V,-28V	57.6	1.94K	618.	459.	81	95.1	100.	0.00	-200.	-500.	1.78	12.3	1.20K	2.50K	1.27	PA
-IIB(0CM) AT 16V,-16V	-49.4	281.	52.9	54.4	81	98.8	98.8	0.00	-200.	-500.	4.65	1.23	200.	400.	2.71	PA
-IIB(+CM) AT 8V,-24V	21.5	399.	194.	101.	67	80.2	90.1	0.00	-200.	-500.	3.89	9.88	500.	400.	3.02	PA
+PSRR AT 8V,-16V	84.9	124.	99.7	9.73	78	92.6	96.3	0.00	80.0	60.0	2.02	0.00	2.00K	140.	195.	DB
-PSRR AT 16V,-8V	81.0	124.	95.8	10.5	81	91.4	100.	0.00	80.0	60.0	1.50	0.00	2.00K	140.	182.	DB
CMR AT 16V,-16V	81.8	134.	94.1	9.78	80	93.8	96.3	0.00	80.0	60.0	1.44	0.00	2.00K	140.	195.	DB
IOS(+) AT 15V,-15V	-50.1	-19.9	-35.0	12.0	81	100.	100.	0.00	-80.0	-100.	3.75	0.00	1.00K	0.00	86.2	MA
IOS(-) AT 15V,-15V	15.7	39.6	27.5	6.87	81	100.	100.	0.00	-1.00K	0.00	150.	0.00	80.0	100.	7.64	MA
ICC AT 15V,-15V	2.02	7.51	3.88	1.39	75	96.3	100.	----	----	2.00	----	67.9 4/	3.00	10.0	-632.M	MA
+VOP AT RL=10K	14.7	15.2	15.0	104.M	81	97.5	100.	0.00	12.0	8.00	28.4	0.00	200.	16.0	1.78K	V
-VOP AT RL=10K	-14.6	-14.2	-14.4	106.M	81	100.	100.	0.00	-200.	-16.0	1.75K	0.00	-12.0	-8.00	22.3	V
+VOP AT RL=2K	13.4	14.9	14.2	582.M	81	100.	100.	0.00	10.0	8.00	7.26	0.00	200.	16.0	319.	V
-VOP AT RL=2K	-14.2	-12.7	-13.6	655.M	81	100.	100.	0.00	-200.	-16.0	285.	0.00	-10.0	-8.00	5.45	V
AVS(+) AT RL=10K	72.7	1.26K	510.	341.	75	82.7	92.6	0.00	50.0	0.00	1.35	2.47	100.K	2.00K	291.	V/MV
AVS(-) AT RL=10K	70.6	1.60K	553.	387.	70	84.0	86.4	0.00	50.0	0.00	1.30	2.47	100.K	2.00K	257.	V/MV
AVS(+) AT RL=2K	66.7	1.20K	356.	299.	77	87.7	95.1	0.00	50.0	0.00	1.02	2.47	100.K	2.00K	333.	V/MV
AVS(-) AT RL=2K	21.8	1.20K	169.	189.	80	92.6	97.5	22.2	50.0	0.00	626.M	0.00	100.K	2.00K	527.	V/MV
AVS AT 5V,-5V,RL=10K	42.1	448.	209.	122.	80	98.8	98.8	0.00	10.0	0.00	1.63	1.23	10.0K	2.00K	80.4	V/MV
AVS AT 5V,-5V,RL=2K	31.2	800.	159.	135.	80	97.5	97.5	0.00	10.0	0.00	1.11	1.23	10.0K	2.00K	72.9	V/MV
SR(+) AT 16V,-16V	1.54	29.4	12.8	6.07	79	93.8	97.5	21.0	7.00	0.00	957.M	4.94	25.0	40.0	2.01	V/US
SR(-) AT 16V,-16V	1.44	23.8	13.3	5.20	81	93.8	100.	14.8	7.00	0.00	1.21	0.00	25.0	40.0	2.26	V/US

NOTES:
1./ EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ
2./ % FAIL VALUES >OR= 5% ARE CIRCLED
3./ FIGURE OF MERIT DEFINITIONS: LO-FM=(MEAN-LOW LIMIT)/SIGMA
HI-FM=(HI LIMIT-MEAN)/SIGMA
4./ THE % FAIL FOR ICC IS NOT VALID SINCE THE DUAL AND QUAD DEVICES ARE COMPARED TO THE SINGLE LIMIT
5./ THERE IS NO MAXIMUM FAIL LIMIT FOR GAIN AND SLEW RATE

Table 4-10. Statistical summary of types 04, 05 & 06 at 25°C.

STATISTICAL DATA FOR DEVICE TYPES MIL/119-04, 05, 06 @ -55 DEGREES C 04 OCT 79 13:21:21

PARAMETER	LOW VALUE 1./	HIGH VALUE 1./	MEAN 1./	SIGMA 1./	SAMPLE SIZE 1./	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW 2./	LOW LIMIT	LOW REJ	LO-FM 3./ 1./	% FAIL HIGH 2./	HIGH LIMIT	HIGH REJ	UNITS
VIO(-CM) AT 28V,-8V	-6.78	9.26	-152.M	2.95	80	92.6	96.3	0.00	-7.00	-10.0	2.32	3.70	7.00	10.0	MV
VIO(+CM) AT 4V,-28V	-8.40	4.99	-536.M	2.63	79	92.6	97.5	2.47	-7.00	-10.0	2.45	2.47	7.00	10.0	MV
VIO(OCM) AT 16V,-16V	-5.36	9.85	-285.M	3.26	81	93.8	97.5	2.47	-7.00	-10.0	2.07	3.70	7.00	10.0	MV
VIO(OCM) AT 5V,-5V	-6.51	9.52	70.4M	3.03	77	88.9	92.6	0.00	-7.00	-10.0	2.33	(8.44)	7.00	10.0	MV
+PSRR AT 8V,-16V	72.2	127.	95.5	9.61	81	91.4	100.	2.47	80.0	60.0	1.92	0.00	2.00K	140.	DB
-PSRR AT 16V,-8V	72.0	124.	95.2	9.83	81	95.1	100.	2.47	80.0	60.0	1.55	0.00	2.00K	140.	DB
CMR AT 16V,-16V	65.9	120.	93.6	9.46	81	96.3	100.	4.94	80.0	60.0	1.44	0.00	2.00K	140.	DB
IOS(+) AT 15V,-15V	-50.6	-21.0	-38.8	9.00	81	100.	100.	0.00	-80.0	-100.	4.57	0.00	1.00K	0.00	NA
IOS(-) AT 15V,-15V	9.05	51.5	36.6	10.8	81	97.5	100.	0.00	-1.00K	0.00	95.9	0.00	80.0	100.	NA
ICC AT 15V,-15V	2.07	8.57	4.38	1.66	78	95.1	100.	----	----	2.00	----	(67.9) 4/	3.50	10.0	MA
+VOP AT RL=10K	14.6	15.1	14.8	100.M	81	96.3	100.	0.00	12.0	8.00	28.1	0.00	200.	16.0	V
-VOP AT RL=10K	-14.2	-13.9	-14.1	126.M	79	97.5	97.5	0.00	-200.	-16.0	1.48K	2.47	-12.0	-8.00	V
+VOP AT RL=2K	8.70	14.8	14.0	1.00	81	97.5	97.5	2.47	10.0	8.00	4.02	0.00	200.	16.0	V
-VOP AT RL=2K	-14.0	-12.6	-13.4	594.M	79	97.5	97.5	0.00	-200.	-16.0	314.	2.47	-10.0	-8.00	V
AVS(+) AT RL=10K	2.70	1.60K	492.	402.	68	82.7	84.0	2.47	25.0	0.00	1.16	0.00	105.K	2.00K	V/MV
AVS(-) AT RL=10K	16.3	1.20K	451.	382.	59	72.8	72.8	1.23	25.0	0.00	1.19	0.00	105.K	2.00K	V/MV
AVS(+) AT RL=2K	3.24	1.20K	337.	265.	73	87.7	87.7	2.47	25.0	0.00	1.17	0.00	105.K	2.00K	V/MV
AVS(-) AT RL=2K	4.80	1.41K	221.	259.	79	91.4	93.8	3.70	25.0	0.00	755.M	0.00	105.K	2.00K	V/MV
AVS AT 5V,-5V,RL=10K	25.8	800.	255.	193.	76	87.7	93.8	0.00	10.0	0.00	1.27	0.00	105.K	2.00K	V/MV
AVS AT 5V,-5V,RL=2K	16.7	800.	222.	232.	79	86.4	97.5	0.00	10.0	0.00	916.M	0.00	105.K	2.00K	V/MV
SR(+) AT 16V,-16V	2.56	37.0	13.3	7.29	74	86.4	87.7	4.94	5.00	0.00	1.14	4.94	50.0	40.0	V/US
SR(-) AT 16V,-16V	1.31	32.3	13.9	6.21	81	91.4	100.	(8.64)	5.00	0.00	1.44	0.00	50.0	40.0	V/US

NOTES:
1./ EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ
2./ % FAIL VALUES >OR= 5% ARE CIRCLED
3./ FIGURE OF MERIT DEFINITIONS: LO-FM=(MEAN-LOW LIMIT)/SIGMA
HI-FM=(HI LIMIT-MEAN)/SIGMA
4./ THE % FAIL FOR ICC IS NOT VALID SINCE THE DUAL AND QUAD DEVICES ARE COMPARED TO THE SINGLE LIMIT
5./ THERE IS NO MAXIMUM FAIL LIMIT FOR GAIN AND SLEW RATE

Table 4-11. Statistical summary of types 04, 05 & 06 at -55°C.

STATISTICAL DATA FOR *DEVICE TYPES MIL/119-04, 05, 06 @ +125 DEGREES C 05 OCT 79 14:33:08

PARAMETER	LOW VALUE 1./	HIGH VALUE 1./	MEAN 1./	SIGMA 1./	SAMPLE SIZE 1./	% IN 2 SIGMA	% IN 3 SIGMA	% FAIL LOW 2./	LOW LIMIT	LOW REJ	LO-FM 3./	% FAIL HIGH 2./	HIGH LIMIT	HIGH REJ	UNITS
VIO(-CM) AT 28V,-4V	-7.64	8.88	102.M	2.65	77	91.4	93.8	(6.17)	-7.00	-10.0	2.68	1.23	7.00	10.0	MV
VIO(+CM) AT 4V,-28V	-8.26	7.17	98.1M	2.45	77	91.4	93.8	(6.17)	-7.00	-10.0	2.90	1.23	7.00	10.0	MV
VIO(DCM) AT 16V,-16V	-8.60	7.49	2.69M	2.52	77	91.4	93.8	(6.17)	-7.00	-10.0	2.78	1.23	7.00	10.0	MV
VIO(DCM) AT 5V,-5V	-8.94	7.28	11.6M	3.02	80	91.4	98.8	4.94	-7.00	-10.0	2.33	1.23	7.00	10.0	MV
D-VIO/D-T FROM 25 DC	-41.8	43.2	1.60	11.8	76	86.4	90.1	8.64	-30.0	-50.0	2.67	2.47	30.0	50.0	
IIO(-CM) AT 28V,-4V	-5.04K	4.27K	-859.	2.01K	81	93.8	100.	0.00	-20.0K	-40.0K	9.52	0.00	20.0K	40.0K	PA
IIO(+CM) AT 4V,-28V	-19.6K	13.9K	-2.00K	5.44K	81	95.1	97.5	0.00	-30.0K	-40.0K	5.15	0.00	30.0K	40.0K	PA
IIO(DCM) AT 16V,-16V	-21.8K	6.13K	-1.41K	3.56K	81	97.5	98.8	1.23	-20.0K	-40.0K	5.22	0.00	20.0K	40.0K	PA
IIO(+CM) AT 8V,-24V	-22.4K	11.7K	-1.78K	4.94K	81	93.8	98.8	1.23	-20.0K	-40.0K	3.69	0.00	20.0K	40.0K	PA
+IIB(-CM) AT 28V,-4V	-5.61K	23.7K	6.73K	6.91K	81	97.5	100.	0.00	-10.0K	-10.0K	2.42	0.00	70.0K	110.K	PA
+IIB(+CM) AT 4V,-28V	0.00	47.9K	19.9K	12.4K	81	97.5	100.	0.00	-10.0K	-10.0K	2.42	0.00	100.K	110.K	PA
+IIB(DCM) AT 16V,-16V	513.M	35.5K	13.0K	9.01K	81	96.3	100.	0.00	-10.0K	-10.0K	2.55	0.00	70.0K	110.K	PA
+IIB(+CM) AT 8V,-24V	503.M	44.3K	18.0K	11.3K	81	96.3	100.	0.00	-10.0K	-10.0K	2.48	0.00	70.0K	110.K	PA
-IIB(-CM) AT 28V,-4V	-5.72K	26.4K	7.59K	7.46K	81	98.8	100.	0.00	-10.0K	-10.0K	2.36	0.00	70.0K	110.K	PA
-IIB(+CM) AT 4V,-28V	1.99K	50.6K	21.9K	14.0K	81	97.5	100.	0.00	-10.0K	-10.0K	2.28	0.00	100.K	110.K	PA
-IIB(DCM) AT 16V,-16V	945.	36.2K	14.4K	10.1K	81	97.5	100.	0.00	-10.0K	-10.0K	2.41	0.00	70.0K	110.K	PA
-IIB(+CM) AT 8V,-24V	1.63K	46.3K	19.8K	12.6K	81	98.8	100.	0.00	-10.0K	-10.0K	2.36	0.00	70.0K	110.K	PA
+PSRR AT 8V,-16V	79.0	124.	101.	9.57	79	91.4	97.5	1.23	80.0	50.0	2.23	0.00	2.00K	150.	DB
-PSRR AT 16V,-8V	79.5	124.	98.2	10.5	78	92.6	96.3	2.47	80.0	50.0	1.73	0.00	2.00K	150.	DB
CMR AT 16V,-16V	81.4	124.	95.8	10.4	80	92.6	98.8	0.00	80.0	50.0	1.51	0.00	2.00K	150.	DB
IOS(+) AT 15V,-15V	-50.0	-13.5	-30.9	15.8	78	96.3	100.	0.00	-80.0	-100.	3.11	0.00	1.00K	0.00	MA
IOS(-) AT 15V,-15V	9.10	30.1	18.8	6.14	81	100.	100.	0.00	-1.00K	0.00	166.	0.00	80.0	100.	MA
ICC AT 15V,-15V	1.55	6.16	3.14	1.20	81	98.8	100.	----	----	0.00	----	(43.2) 4/	3.00	10.0	MA
+VOP AT RL=10K	14.9	15.3	15.1	104.M	78	95.1	96.3	3.70	12.0	8.00	29.4	0.00	200.	16.0	V
-VOP AT RL=10K	-14.8	-14.4	-14.6	115.M	81	98.8	100.	0.00	-200.	-16.0	1.62K	0.00	-12.0	-8.00	V
+VOP AT RL=2K	13.2	14.9	14.1	644.M	78	96.3	96.3	3.70	10.0	8.00	6.42	0.00	200.	16.0	V
-VOP AT RL=2K	-14.3	-12.5	-13.6	760.M	81	100.	100.	0.00	-200.	-16.0	245.	0.00	-10.0	-8.00	V
AVS(+) AT RL=10K	50.7	1.20K	360.	263.	79	93.8	93.8	0.00	25.0	0.00	1.27	0.00	105.K	2.00K	V/MV
AVS(-) AT RL=10K	34.3	1.20K	280.	187.	79	96.3	96.3	0.00	25.0	0.00	1.36	0.00	105.K	2.00K	V/MV
AVS(+) AT RL=2K	44.0	1.60K	248.	276.	73	82.7	86.4	0.00	25.0	0.00	806.M	0.00	105.K	2.00K	V/MV
AVS(-) AT RL=2K	8.70	1.20K	89.0	141.	79	96.3	96.3	(12.0)	25.0	0.00	453.M	0.00	105.K	2.00K	V/MV
AVS AT 5V,-5V,RL=10K	29.6	800.	148.	119.	81	95.1	98.8	0.00	10.0	0.00	1.16	0.00	105.K	2.00K	V/MV
AVS AT 5V,-5V,RL=2K	21.1	800.	116.	139.	81	95.1	97.5	0.00	10.0	0.00	764.M	0.00	105.K	2.00K	V/MV
SR(+) AT 16V,-16V	875.M	23.8	12.3	5.48	81	93.8	100.	(9.88)	5.00	0.00	1.34	0.00	50.0	40.0	V/US
SR(-) AT 16V,-16V	1.90	19.6	11.8	4.34	81	95.1	100.	(7.41)	5.00	0.00	1.57	0.00	50.0	40.0	V/US

NOTES:
1./ EXCLUDES POPULATION OUTSIDE OF LOW REJ AND HIGH REJ
2./ % FAIL VALUES >OR= 5% ARE CIRCLED
3./ FIGURE OF MERIT DEFINITIONS: LO-FM=(MEAN-LOW LIMIT)/SIGMA
HI-FM=(HI LIMIT-MEAN)/SIGMA
4./ THE % FAIL FOR ICC IS NOT VALID SINCE THE DUAL AND QUAD DEVICES ARE COMPARED TO THE SINGLE LIMIT
5./ THERE IS NO MAXIMUM FAIL LIMIT FOR GAIN AND SLEW RATE

Table 4-12. Statistical summary of types 04, 05 & 06 at 125°C.

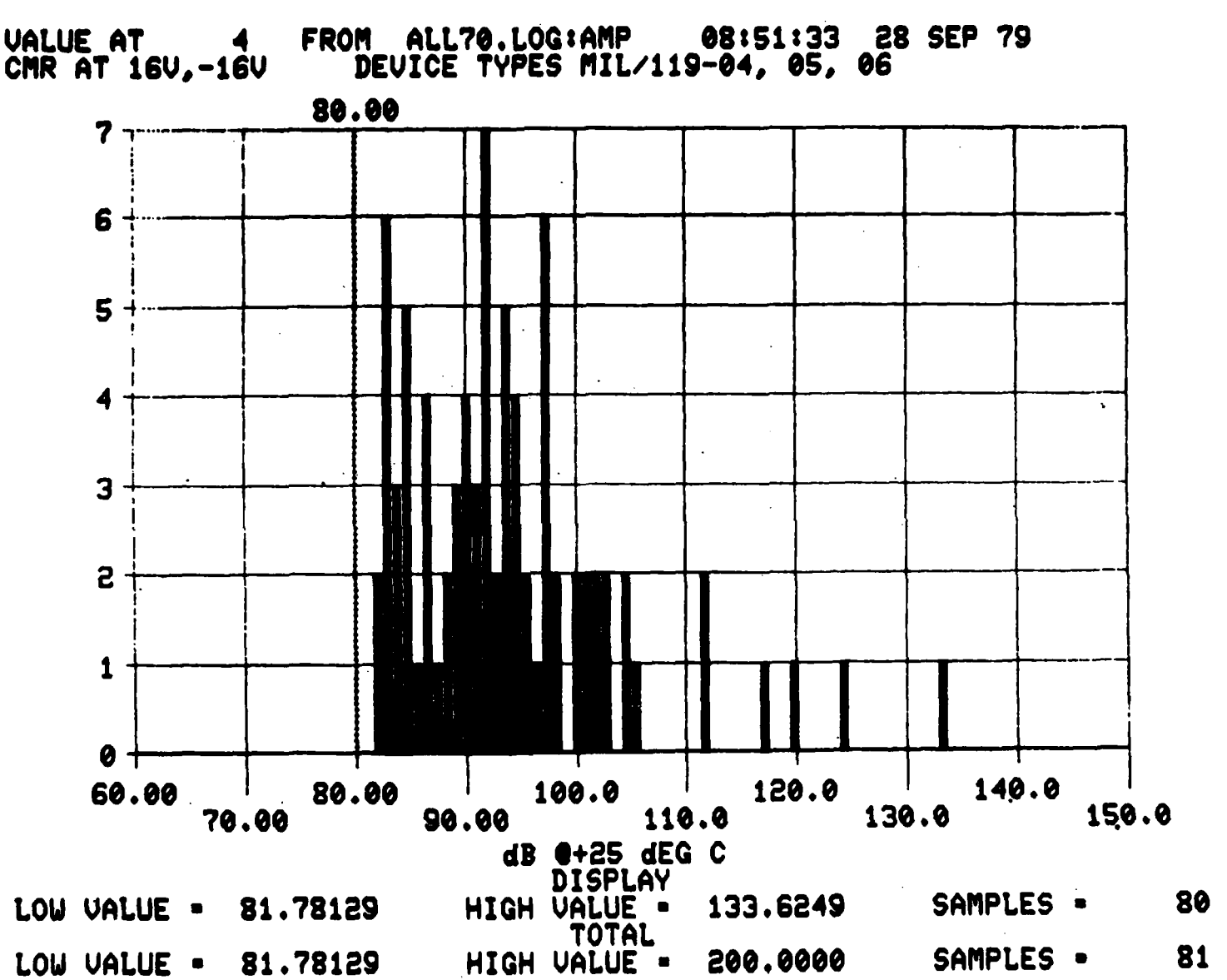


Figure 4-5. Common mode rejection at 25°C.

Characteristics	Symbol	Conditions $\pm V_{CC} = \pm 15$ V (paragraph 3.4 and Figure 7, unless otherwise specified)		Devices	Limits Min	Limits Max	Units
Input offset voltage	V_{IO}	$\pm V_{CC} = \pm 5$ V at $V_{CM} = 0$ V	$T_A = 25°C$	ALL	-5	5	mV
		$\pm V_{CC} = \pm 15$V at $V_{CM} = \pm 11$ V, 0 V	$-55°C \leq T_A \leq +125°C$	ALL	-7	7	mV
Input offset voltage temperature sensitivity	$\frac{\Delta V_{IO}}{\Delta T}$	$V_{CM} = 0$ V		ALL	-30	30	uV/°C
Input offset current	I_{IO} 3/	$V_{CM} = 0$ V $t \leq 25$ ms	$T_J = 25°C$	ALL	-100	100	pA
			$T_J = 125°C$	ALL	-20	20	nA
Input bias current	$+I_{IB}$	$V_{CM} = +11$V $t \leq 25$ms	$T_J = 25°C$	ALL	-200	1200	pA
			$T_J = 125°C$	ALL	-10	70	nA
	$-I_{IB}$ 1/	$\pm V_{CC} = \pm 15$ V	$T_J = 25°C$	ALL	-200	200	pA
		$V_{CM} = 0$ V, $t \leq 25$ms	$T_J = 125°C$	ALL	-10	50	nA
	2/	$V_{CM} = -11$V $t \leq 25$ms	$T_J = 25°C$	ALL	-400	200	pA
			$T_J = 125°C$	ALL	-10	50	nA
Power supply rejection ratio	+PSRR	$+V_{CC} = 20$V, 10V; $-V_{CC} = -15$V		ALL	80	-	dB
	-PSRR	$+V_{CC} = 15$V; $-V_{CC} = -20$V, -10V		ALL	80	-	dB
Input voltage common mode rejection 4/	CMR	$-11V \leq V_{CM} \leq 11V$		ALL	80	-	dB

See footnotes at end of table.

Table 4-13. Proposed MIL-M-38510/119 electrical characteristics.

Characteristics	Symbol	Conditions $\pm V_{CC} = \pm 15$ V (paragraph 3.4 and Figure 7, unless otherwise specified)		Devices	Limits Min	Limits Max	Units
Adjustment for input offset voltage 7/	$V_{IO\ ADJ(+)}$			01, 02, 04, 05	+8	-	mV
	$V_{IO\ ADJ(-)}$			01, 02, 04, 05	-	-8	mV
Output short circuit current (for positive output) 5/	$I_{OS(+)}$	$t \leq 25$ mS (Short circuit to ground)		01,02,03	-40	-	mA
				04,05,06	-80	-	
Output short circuit current (for negative output) 5/	$I_{OS(-)}$	$t \leq 25$ mS (Short circuit to ground)		01,02,03	-	40	mA
				04,05,06	-	80	
Supply current (per amplifier)	I_{CC}		$T_A = -55°C$	01,02,03	-	0.3	mA
				04,05,06	-	3.5	
			$25°C \leq T_A \leq 125°C$	01,02,03	-	0.3	
				04,05,06	-	3	
Output voltage swing (maximum)	$+V_{OP}$, $-V_{OP}$		$R_L = 10$ KΩ	ALL	±12.5	-	V
			$R_L = 2$ KΩ	04,05,06	±11	-	
Open loop voltage gain (single ended) 6/	$A_{VS(+)}$, $A_{VS(-)}$	$V_{out} = \pm 10$ V 01-03, $R_L = 10$ K 04-06, $R_L = 2$ K	$T_A = 25°C$	01,02,03	5	-	V/mV
				04,05,06	50	-	
			$-55°C \leq T_A \leq +125°C$	01,02,03	4	-	
				04,05,06	25	-	
Open loop voltage gain (single ended) 6/	A_{VS}	$\pm V_{CC} = \pm 5$ V $R_L = 10$ KΩ	$V_{out} = \pm 2$V	01,02,03	3	-	V/mV
				04,05,06	10	-	

Table 4-13. Proposed MIL-M-38510/119 electrical characteristics (cont.).

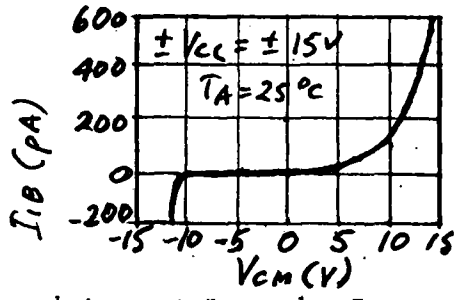
Characteristics	Symbol	Conditions $\pm V_{CC} = \pm 15$ V (paragraph 3.4 and figure 7, unless otherwise specified)		Device	Limits Min	Limits Max	Units
Transient response Rise time	$TR_{(tr)}$	V_{IN} = 50 mV, A_V = 1	R_L = 10 KΩ	01,02,03	-	400	ns
		C_L = 100 pF	R_L = 2 KΩ	04,05,06	-	200	
Transient response Overshoot	$TR_{(os)}$	See Figure 8	R_L = 10 KΩ	01,02,03	-	20	%
			R_L = 2 KΩ	04,05,06	-	40	
Slew rate	SR(+) and SR(-)	V_{IN} = ± 5 V	T_A = 25°C	01,02,03	2	-	V/us
				04,05,06	7	-	
		AV = 1	T_A = -55°C, 125°C	01,02,03	1	-	
		see Figure 8		04,05,06	5	-	
Settling time	ts(+) and ts(-)	(0.1% error) T_A = 25°C see Figure 9	AV = 1	01,02,03	-	6000	ns
				04,05,06	-	1500	
Noise (referred to input) broad-band	N_I(BB)	Bandwidth = 10 kHz see Figure 10	T_A = 25°C	ALL	-	15	uV_{rms}
Noise (referred to input) popcorn	N_I(PC)		T_A = 25°C	ALL	-	80	uV_{pk}
Channel separation	CS	see Figure 11	T_A = 25°C	02,03,05, 06	80	-	dB

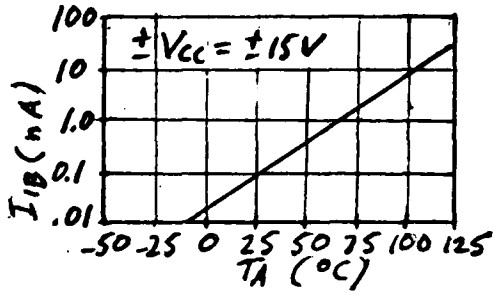
Table 4-13. Proposed MIL-M-38510/119 electrical characteristics (cont'd).

NOTES:

1/ Bias currents are actually junction leakage currents which double (approximately) for each 10°C increase in junction temperature T_J. Measurement of bias current is specified at T_J rather than T_A, since normal warmup thermal transients will affect the bias currents. The measurements for bias currents must be made within 25 ms after power is first applied to the device for test. Measurement at T_A = -55°C is not necessary since expected values are too small for typical test systems.

2/ Bias current is sensitive to power supply voltage, common mode voltage and temperature as shown by the following typical curves:





3/ I_{IO} is calculated as the difference between + I_{IB} and - I_{IB}.

4/ CMR is calculated from V_{IO} measurements at V_{CM} = + 11V and - 11V.

5/ Continuous limits shall be considerably lower. Protection for shorts to either supply exists providing that T_J(max) $\leq$ 175°C.

6/ Because of thermal feedback effects from output to input, open loop gain is not guaranteed to be linear or positive over the operating range. These requirements, if needed, should be specified by the user in additional procurement documents.

7/ Offset adjustment pins do not exist for 8 pin dual and 14 pin quad packages.

8/ Channel separation is only applicable for the dual and quad devices.

Table 4-13. Proposed MIL-M-38510/119 electrical characteristics (cont'd).

SECTION V

12 BIT A/D CONVERTER

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SECTION V

CHARACTERIZATION OF 12-BIT A/D CONVERTERS

MIL-M-38510/120

5.1 Background and Introduction

This JAN 38510 specification development for A/D converters is new in at least two respects: it is the first slash sheet devoted to A/D converters, and the specified devices are the first linear hybrids to be designated for military usage in the JAN program. The need for data converters in military systems is well-established, not only for new microprocessors-based digital systems, but for retrofit into upgraded existing systems. For example, a system using resolvers to transmit angular position/rate data to other analog computing subsystems may be upgraded by retaining the sensing resolvers, converting their outputs to digital numbers, and replacing the analog computing subsystems with digital counterparts. High-resolution, high accuracy converters would be required to accommodate the wide dynamic range and typical system accuracy required.

At this time, high speed (e.g. 13 to 50 usec conversion time) 12-bit A/D converters do not exist as monolithic devices, although lower speed and/or lower resolution monolithics are becoming available from several manufacturers. The hybrid devices selected for this slash sheet are already used in numerous military systems. They were developed by Micro Networks Corporation, and at least some of the device types will also be available from other hybrid manufacturers ... Analog Devices and Hybrid Systems. Generally, the devices offer choice of external or internal references, two conversion times, and four input voltage ranges.

There is valid concern amongst all device manufacturers regarding the required testing of A/D converters. Test capabilities may range from bench tests, to custom test boxes, to fully automatic test systems. At GE, two levels of test were planned ... both a bench test and a fully automatic test using the Tektronix S3260 system. Admittedly, the latter system is not used by any manufacturer, but GE's test development has a dual purpose ... to verify the test circuit and to characterize the device. Since both D/A and A/D test developments were proceeding in parallel, a common precision reference D/A section was developed to share with both test adapters. The test circuit recommended for the slash sheet should be compatible with a variety of automatic test systems. Deviations from the test circuit are permitted but must be justified by the manufacturer at the time of qualification submittal.

Test philosophy regarding linearity and monotonicity is another controversial subject. One manufacturer verifies linearity by measuring deviations from a best-fit straight line, while another measures deviations from a line connecting end points. Since users cannot calibrate to some unknown best-fit line, but can calibrate to full-scale end points, GE strongly favors the latter method. (There is further discussion on these topics within the text.)

At this report tine, the A/D characterization effort is not yet complete. A slash sheet has been prepared in preliminary status, and has been issued to interested people for comment. Test philosophy has been established, and test circuits and adapters were designed and fabricated for both bench testing and Tektronix S3260 testing. Test software has been developed and has been debugged. The remaining effort to complete the characterization is to complete the data taking, analyze the data, recommend changes (if any) for the slash sheet, issue the data, and finalize the slash sheet.

5.2 Description of Device Types

There are two series of device types included in /120, the Micro Networks MN5200 series and the MN 5210 series. In each series there are eight device types, four pair having input voltage ranges of 0 to -10V, -5V to +5V, -10V to +10V, 0 to +10V, with each pair having either an internal or an external reference. Both series are 12-bit successive-approximation converters having both serial and parallel digital outputs. They are packaged in miniature 24-pin glass/ceramic DIPs, are self-contained and internally laser-trimmed (no external adjustments). The two series differ only in maximum conversion time ... the 5200 series (device types 01-08) requiring 50 usec max for a complete conversion, and the 5210 series (device types 09-16) requiring 13 usec max.

The hybrid devices have several chips; there are significant differences in the number of chips used by different manufacturers. Basically, the successive approximation converter consists of a D/A converter (ladder network and switches), a successive approximation register and logic, and a comparator. An approximate diagram of the 5200 A/D converter is shown in Figure 5-1, which includes functional level information only, not detailed schematics of all sections. The 12-bit converter must make 12 successive approximations of the applied input voltage. While this is occurring, the input cannot change (unless it were to change so as not to affect previous trials, which is too restrictive), so a sample/hold circuit is normally used to hold the input constant during the conversion time. The 12 comparisons are made between the input voltage and a feedback voltage obtained from the internal 12-bit parallel D/A converter, beginning first with the MSB and ending with the LSB. The comparator output determines whether a "1" or a "0" should be entered in the register for each bit comparison. In the figure, this function is performed with a high-gain precision comparator A2.

The 25L04 successive approximation register contains most of the digital control and storage necessary to operate the converter. It contains a set of master latches acting as control elements which change state when the external clock input is low, and a set of slave latches that hold the register data and change state on a low-high transition of the input clock. It acts as a serial-to-parallel converter for information from the comparator A_2, sending it to the appropriate slave latch to appear at the register output (serial output) when the clock transition goes from low-to-high. When that data enters the register, the next less significant bit is set to a low, ready for the next iteration.

A timing diagram is shown in Figure 5-2. For parallel data outputs, the shaded areas shown denote states determined by data input immediately prior to the shaded area. Parallel data is valid for the entire time that the EOC signal is low, i.e., until the converter is reset. The converter is reset by holding the "start" signal low during a low-to-high transition of the clock, beginning at least 25 nsec prior to the clock transition. When the start is again set high, the conversion will begin on the next low-to-high clock transition. The start signal can be set low at any time during a conversion and it will reset the converter. A complete conversion takes place in 13 clock pulses. For continuous operation, the user has to connect "start convert" to EOC, pin 1 to pin 22. The ground terminals must be externally connected together as close as possible to the device.

Op Amp A_1 buffers the input reference voltage and in conjunction with transistor Q14 provides the base line voltage to all switching transistors. The base line voltage varies to compensate for the variation in the switching transistor V_{BE}'s with temperature, thereby providing a constant voltage to the ladder resistors. Similar compensation exists for variations in the minus supply voltage, which would change ladder currents.

It should be noted that the 5210 series of devices manufactured by Micro Networks require a 2.2 uF solid tantalum capacitor connected between DUT pins 15 and 10 for operation with conversion times of 24 usecs or less.

The user should be aware that there are differences in the supply currents among vendors, and also differences in power supply sensitivity. The specification tolerances have essentially been widened to accommodate both vendors. Proper system design considerations by the user will permit interchangeability by using the specified limits. Tighter performance may be obtained from a single vendor on power supply sensitivity, but this is not guaranteed or controlled within the spec, except as stated.

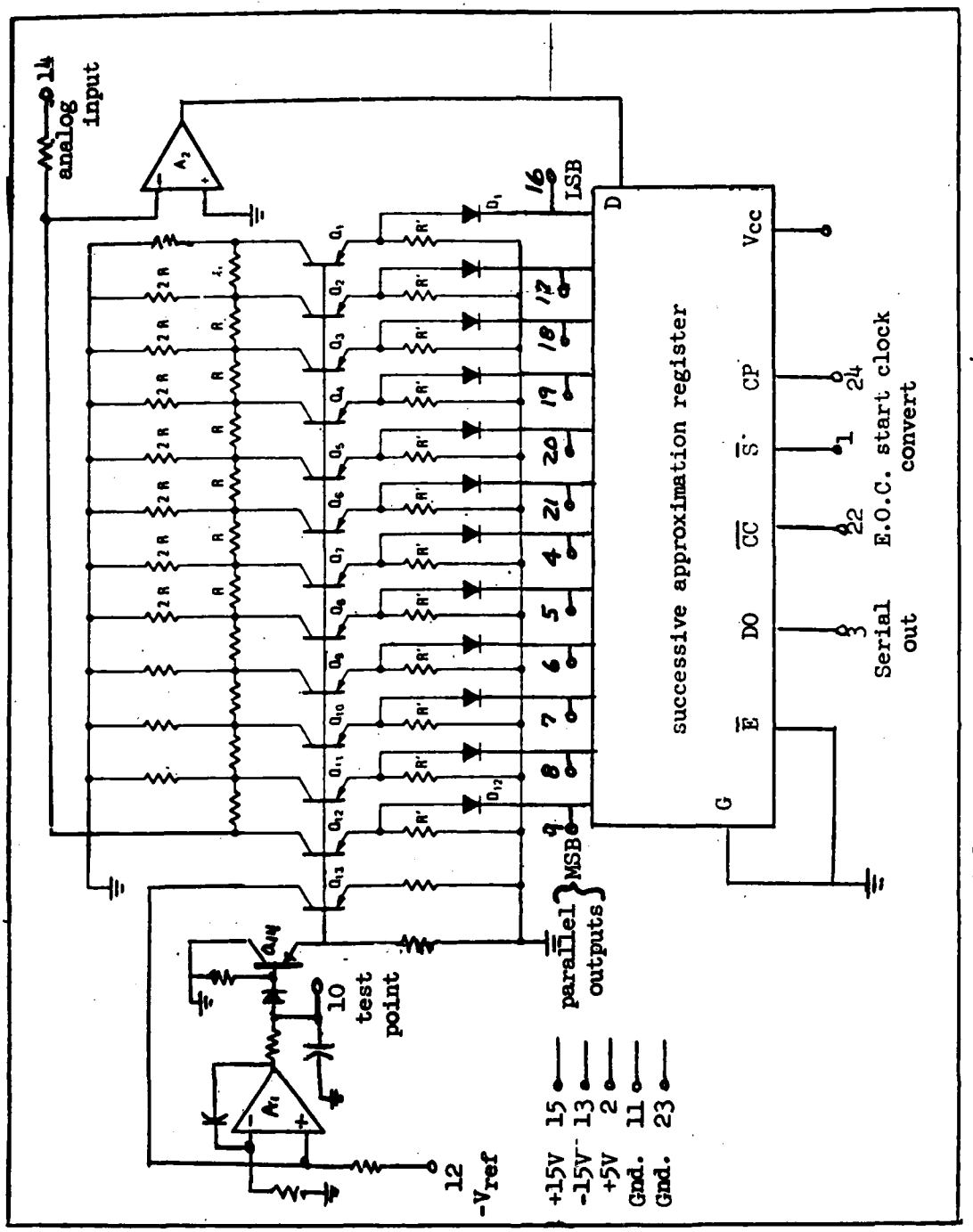


Figure 5-1. Approximate schematic of MN5200 A/D Converter with external reference.

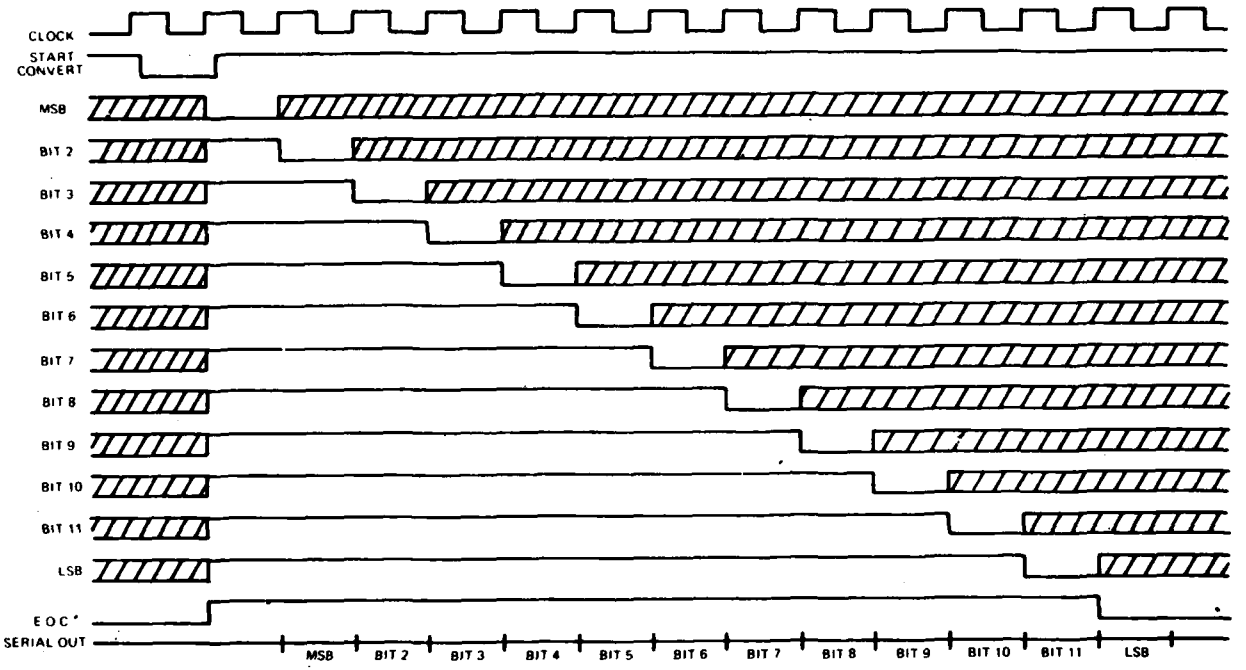


Figure 5-2. Timing Diagram for the 5200 series A/D Converter

5.3 Characterization of the 5200 and 5210 Series A/D Converters

5.3.1 Static Test Parameters

Power Supply Currents

Power supply currents limits have been enlarged to encompass all device manufacturers designs since no two devices are implemented identically. Each must, however, satisfy the maximum power dissipation requirements.

Power Dissipation

The device power dissipation is the sum total of the products of the power supply currents and their respective voltages plus, for devices with external reference voltage only, the product of the reference input current and voltage.

$$P_D = V_{cc}\ I_{cc} + V_{EE}\ I_{EE} + I_{LOG} + \underbrace{V_{REF}\ I_{REF}}_{(\text{EXT REF. ONLY})} \qquad [5.1]$$

Input Logic Voltage Levels

Logic "1" input voltage levels is + 2 V minimum and Logic "0" input voltage levels is + .8 V maximum, typical digital logic levels. Inputs are: S.C. and Clock.

Output Logic Voltage Levels

Output logic "1" voltage is 2.4 V minimum when loaded with 320 uA (source). Output logic "0" voltage is 0.4 V maximum loaded with 3.2 mA (sink). Outputs are: 12 address outputs; E.O.C; and SDO.

Output Short Circuit Current

All outputs are tested with a short circuit applied. Output current shall not exceed - 25 mA.

Input Low Current

Input low current is the maximum sink current the device will sink with the input at 0 V.

Input High Current

Input high current is the maximum current the device will source with the input voltage at + 5 V.

Input Impedance

The specification calls for input impedance measurement. On the S3260 a dc resistance will be measured.

Clock Input Pulse Width

Clock input pulse width is specified as 200 ns. The positive portion of the clock pulse (logic 1) must be equal to or greater than 200 ns wide for all device types.

Minimum Conversion Time

Minimum conversion time is a function of the speed of the converter and limits specified are maximum values. The maximum value of minimum conversion time represents the maximum conversion speed the device must be capable of at rated accuracy.

Power Supply Sensitivity

Power supply sensitivity is specified as the percent of full scale voltage range change per percent change in power supply voltage.

Zero Error

For a unipolar device the straight line between the first and last transition voltage is extended beyond the first transition voltage 1/2 LSB. The difference between the resulting voltage and zero volts is unipolar zero error.

For a bipolar device add 1/2 LSB to the transition voltage for the 0111 1111 1111 to 1000 0000 0000 transition and difference between the resulting voltage and zero volts is the bipolar zero error. If "Best Fit Linearity" is employed the offset employed to shift the curve will have to be factored into the zero errors, unipolar and bipolar.

Absolute Accuracy

Absolute accuracy is accuracy with which the A/D converter will measure and convert an analog voltage to a digital equivalent, relative to an accurate voltage standard. Quantization error is reduced to ± 1/2 LSB by offsetting the transition voltages by 1/2 LSB.

Table 5.1 Device Specifications

Characterizations	Symbol	Conditions/Remarks	Device Types 01 - 13 Limits MIN	Device Types 01 - 13 Limits MAX	Units
Power Supply Current from V_{CC}	I_{CC}		3	28	mA
Power Supply Current from V_{EE}	I_{EE}		-35	-1	mA
Power Supply Current from V_{LOG}	I_{LOG}		1	42	mA
Power Dissipation	P_D	Device Types - 02, 04, 06, 08, 10, 12, 16 Device Types - 01, 03, 05, 07, 09, 11, 13, 15		0.8 1	w w
Ref. Input	I_{REF}	Device Types with External Ref. Only - 02, 04, 06, 08, 10, 12, 14, 16	0.1	2	mA
Input Logic Voltage Levels Logic "1" Logic "0"	 V_{IH} V_{IL}		 2	 0.8	 V V
Output Logic Voltage Levels Logic "1" Logic "0"	 V_{CH} V_{OL}	 I_L = 320 uA I_L = 3.2 mA	 2.4	 0.4	 V V
Output Short Circuit Current	I_{OSC}	T_A = +25°C, V_{IN} = + 10.5 V	-25	0	mA
Input Low Current	I_{IL}	V_{IN} = 0 V		-.6	mA

Table 5.1 Device Specifications (Cont.)

Characterizations	Symbol	Conditions/Remarks	Device Types 01 - 13 Limits MIN	MAX	Units
Input High Current	I_{IH}	V_{IN} = + 5 V		40	uA
Input Impedance	Z_I	Device Types - 01 to 04, 07 to 12, 15, 16 Device Types - 05, 06, 13, 14	3.5 7.0	10 20	k k
Clock Input Pulse Width	CPW		200		ns
Minimum Conversion Time	t_{CT}	Device Types - 01-08 Device Types - 09-16		50 13	us us
Power Supply Sensitivity V_{CC}	PSS1	Device Types - 01,03,05,07,09,11,13,15 Device Types - 02,04,06,08,10,12,14,16		±.02 ±.02	%FSR/ %P.S.
Power Supply Sensitivity V_{EE}	PSS2	Device Types - 01,03,05,07,09,11,13,15 Device Types - 02,04,06,08,10,12,14,16		±.05 ±.02	%FSR/ %P.S.
Resolution		The device shall exhibit no missing codes		12	BITS
Zero Error		V_{CC} = + 15 V ± .015 V V_{EE} = -15 V ± .015 V		2	LSB
Absolute Accuracy " "		V_{CC} = + 15 V ± .015 V Ext. Ref. V_{EE} = - 15 V ± .015 V Int. Ref.		±.1 ±.4	%FSVR
Integral Linearity Error		V_{CC} = + 15 V ± .015 V V_{EE} = - 15 V ± .015 V		±1/2	LSB
Major Carry Errors	MCI - MCII	4000 - 377 (Octa) to 2 - 1 Relative to REF DAC Major Transition Voltage		±1	LSB

Integral Linearity Error

Integral linearity is the deviation from the ideal linearity curve (a straight line). The ideal linearity curve would be a straight line between the first and last transition voltages if linearity was specified as "End Point". If, however, "Best Fit Linearity" is employed, linearity is the deviation from the "Best Fit" straight line.

Major Carry Errors

Major Carry Errors are a measure of the differential non-linearity of the A/D converter. If major carry errors are less than ± 1 LSB and the device is linear, there will be no missing codes.

5.3.2 Static Test Circuit

The circuitry used to test the MN5200 series of A/D converters is shown in Figures 4 and 5. Figure 5.3 shows a simplified block diagram of the schematic. The transition to be tested - 1 LSB is entered into the A_n register, where it is applied to the reference DAC and a digital comparator. The digital comparator's other input comes from the device under test, a 12 bit A/D converter. The latch inserted between the ADC and the digital comparator insures that only valid data is applied to the comparators, i.e. it is strobed when an end of convert signal is received from the ADC.

The digital comparator has 3 possible outputs, $A \lessdot B$, $A=B$, or $A \gtrdot B$ depending on the relative magnitude of the transition to be tested and the present state of the A/D converter. If $A \lessdot B$, the input to an integrator is connected to + 5 volts through an analog switch. This causes the integrator to ramp downwards. The output of the integrator is summed with the analog output of the reference DAC. Since the DAC output is a constant DC level and the integrator's output is decreasing their inverted sum is rising, which forms the analog input to the ADC. The ADC's input voltage will continue to increase and its digital output word will continue to decrease until the digital comparator decides that $A=B$ or $A \gtrdot B$. When this happens, the analog switch changes state, connecting -5 volts to the input of the integrator. This causes the output of the integrator to ramp upwards. When summed with the DAC output, this forces the ADC input voltage to decrease, which increases its digital output word.

In this way it can be seen that the ADC digital output word locks onto the word present in the A_n register, and couples between $A \lessdot B$ and $A \eqgtr B$.

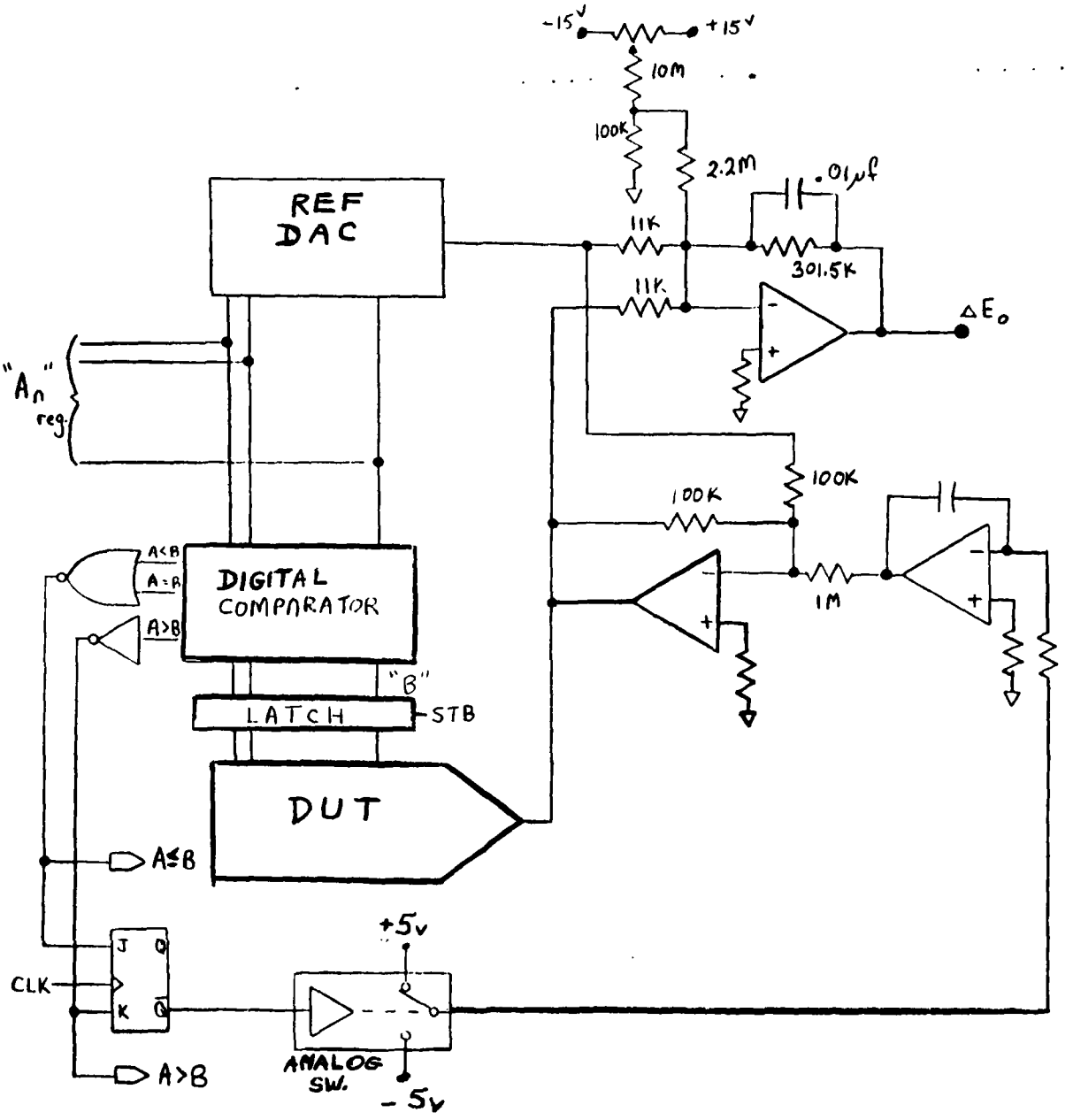
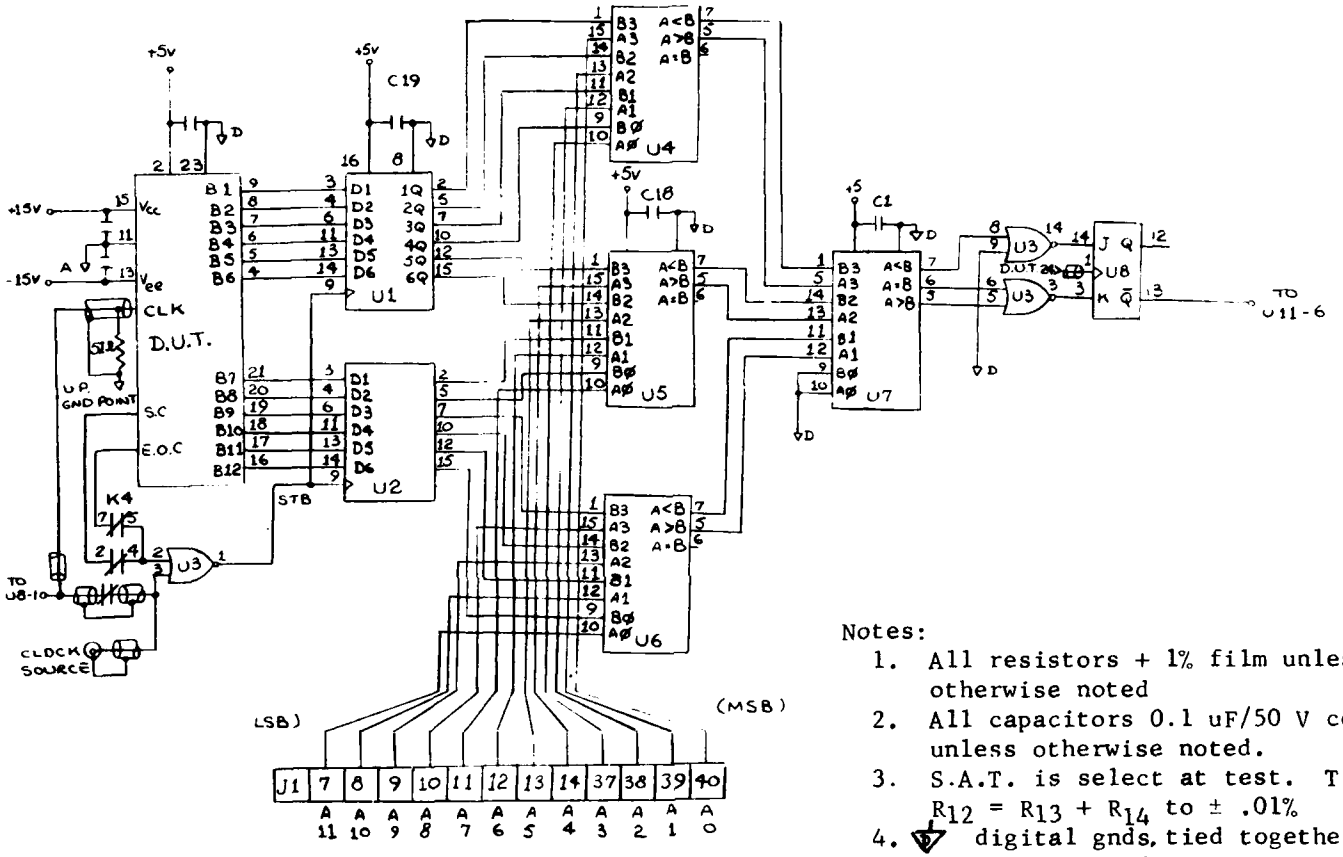


Figure 5.3. Block diagram, 12 Bit A/D Converter test circuit.



Notes:

1. All resistors + 1% film unless otherwise noted
2. All capacitors 0.1 uF/50 V ceramic unless otherwise noted.
3. S.A.T. is select at test. Trim for $R_{12} = R_{13} + R_{14}$ to ± .01%
4. ▽ digital gnds, tied together to + 5V return and one jumper made to unipoint analog gnd.
   ⏚ system gnd. (not connected to anal. gnd. or adapter)

Figure 5.4. Static Test Circuit. (cont'd next page)

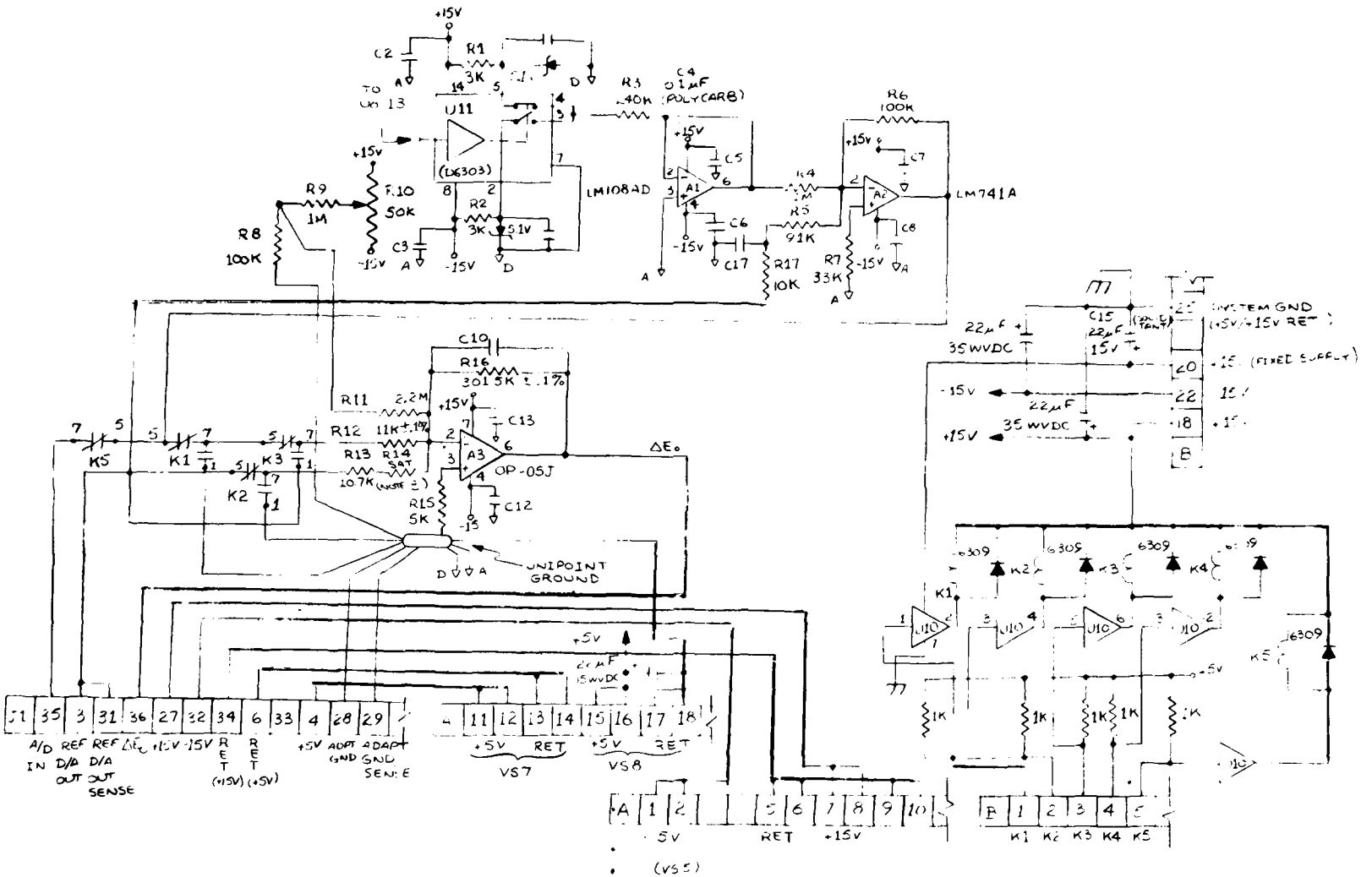


Figure 5.4. Static Test Circuit. (cont'd)

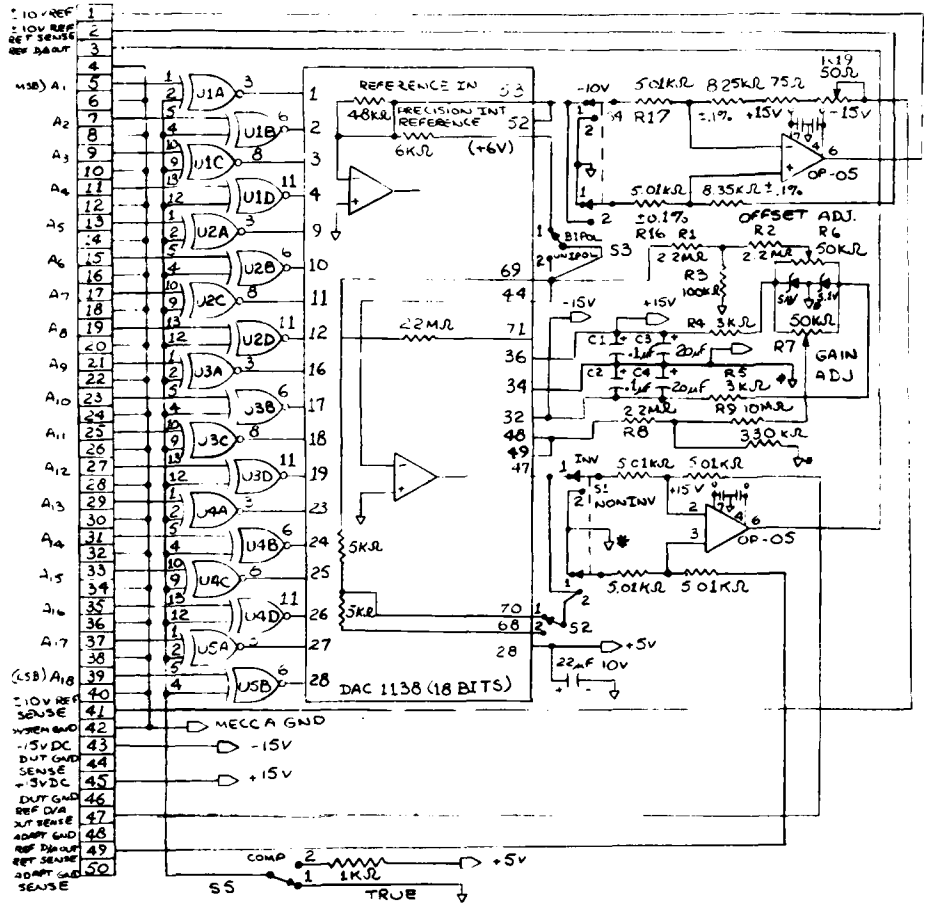


Figure 5-5. Reference module schematic.

Notes:

1. For use in conjunction with the 12 bit D/A converter S3260 Test Adapter

S1	in position	2 (Non Inv)
S2	" "	1 for unipolar & +5V range
S2	" "	2 for ± 10V range
S3	" "	1 for bipolar operation
S3	" "	2 for unipolar operation
S4	" "	2 for +10V Ref volt
S5	" "	2 for comp logic

2. For use in conjunction with the 12 bit A/D converter S3260 Test Adapter

S1	in position	1 (Inv) for MN5206, MN5207 MN5216, MN5217
S1	" "	2 (Non Inv) for MN5200 - MN5205 MN5210 - MN5215
S2	" "	1 for MN5200, MN5201, MN5203, MN5204, MN5206, MN5207, MN5210, MN5211, MN5213, MN5214, MN5216
S2	" "	2 MN5202, MN5205, MN5212, MN5215
S3	" "	1 MN5201, MN5202, MN5204, MN5205, MN5211, MN5212, MN5214, MN5200
S3	" "	2 MN5203, MN5206, MN5207, MN5210, MN5213, MN5216, MN5217
S4	" "	1 for -10V Ref. Volt
S5	" "	1 for MN5206, MN5207, MN5216, MN5217
S5	" "	2 MN5200 - MN5205, MN5210 - MN5215

3. S3260 must apply a logic "1" to A_{13} - A_{18} when S5 is in pos 2 and logic "0" when in pos 1.
4. Ref. D/A output offset, gain, and 10 V reference voltage are adjusted at the start of testing on the S3263. Measurements to be made at predetermined locations at the S3263 Test Adapter
5. ⏚* represents analog ground
   ⏚ represents digital ground

The output of the reference DAC and the analog input to the ADC are summed in the error amplifier. A potentiometer is used to null the offset of this amplifier to zero. The capacitor in the feedback loop tends to average out the fluctuations in the A/D input voltage due to the ramping effect of the integrator. The ADC transition voltage can be calculated by dividing $\triangle E_o$ by the gain of the error amplifier, and then subtracting the reference DAC voltage.

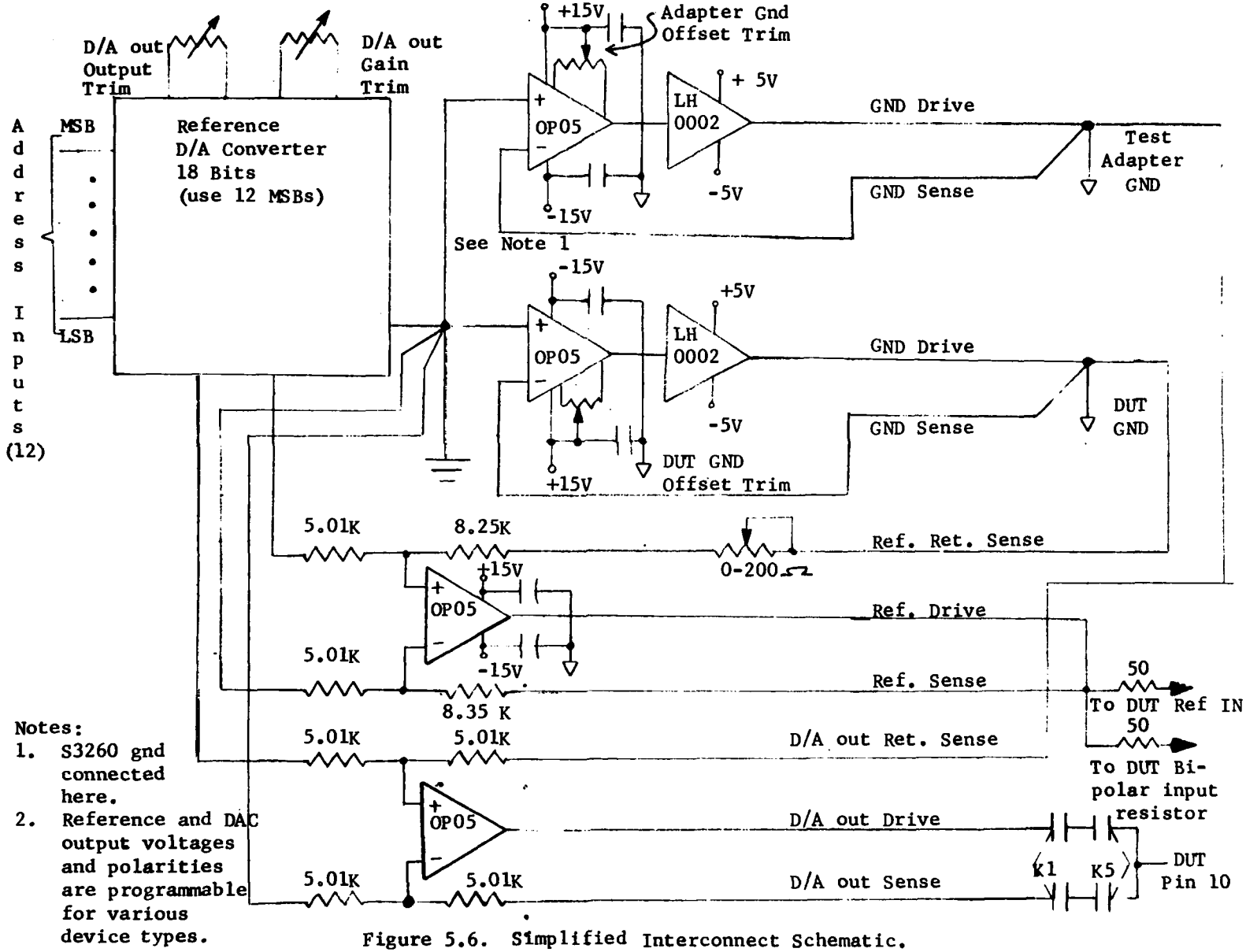
Figure 5.7 shows the ADC input voltage vs time when the transition voltage from 0110 to 0111 is to be measured. It is assumed that the ADC performs a conversion every 10 usec and the analog input to the A/D converter ramps up or down at a rate of .005 LSB/usec. When conversion #1 is complete, the reference DAC input (0110) is equal to the ADC output so the integrator continues to ramp upward. The same thing is true when conversion #2 is completed, 10 usec later. When conversion #3 is complete, however, the ADC output is greater than the DAC input, so that A<B and the integrator begins to ramp downward. The ADC input voltage will continue to cycle around the transition voltage from this point onward. It should be noted that in Figures 5.7&5.8 downward refers to increasing, and upward decreasing A/D input voltage.

In the previous example the maximum difference between the actual transition voltage and the input to the ADC at any time was .05 LSB. In measuring some transitions this difference may become as large as .1 LSB due to the way in which the ADC performs conversions. Because the MN5200 series of ADC's are successive approximation devices they perform conversions by setting one bit at a time, starting with the MSB. Figure 5.8 shows the ADC input voltage vs time when measuring the 0111 to 1000 transition voltage. After conversion #1 is completed the ADC input voltage will ramp upwards because A=B. The same thing is true when conversion #2 is completed 10 usec later. Conversion #3 is now begun, starting with the MSB. Because the analog input to the ADC immediately following conversion #2 is still less than 1000, the MSB will be set to a 0. The remainder of the bits will be set to 1, resulting in an ADC output of 0111 at the end of conversion #3. Since this is still equal to the input to the DAC, the integrator continues to ramp upwards. Conversion #4 will result in a value of 1000, and the integrator will begin to ramp downwards. Conversion #5 also results in a value of 1000, and the integrator continues downward. Conversion 6 is now begun, starting with the MSB. Because the input to the ADC immediately following conversion #5 is still greater than 1000, the MSB will be set to a 1. The remainder of the bits will be set to 0, resulting in an ADC output of 1000 at the end of conversion #6. Since this is still greater than the input to the DAC, the integrator continues to ramp downwards.

The ADC input will continue to cycle around the transition voltage from this point onward. The reason that the ADC input voltage did not stray as far from the actual transition voltage when measuring the 0110 to 0111 transition was that in that case only the least significant bit was changing, which is the last to be set in a conversion. In both cases the sawtooth around the actual transition voltage is filtered out in the error amplifier by a capacitor in the feedback loop.

5.3.3 Devices Used For Testing

(later)



Notes:

1. S3260 gnd connected here.
2. Reference and DAC output voltages and polarities are programmable for various device types.

Figure 5.6. Simplified Interconnect Schematic.

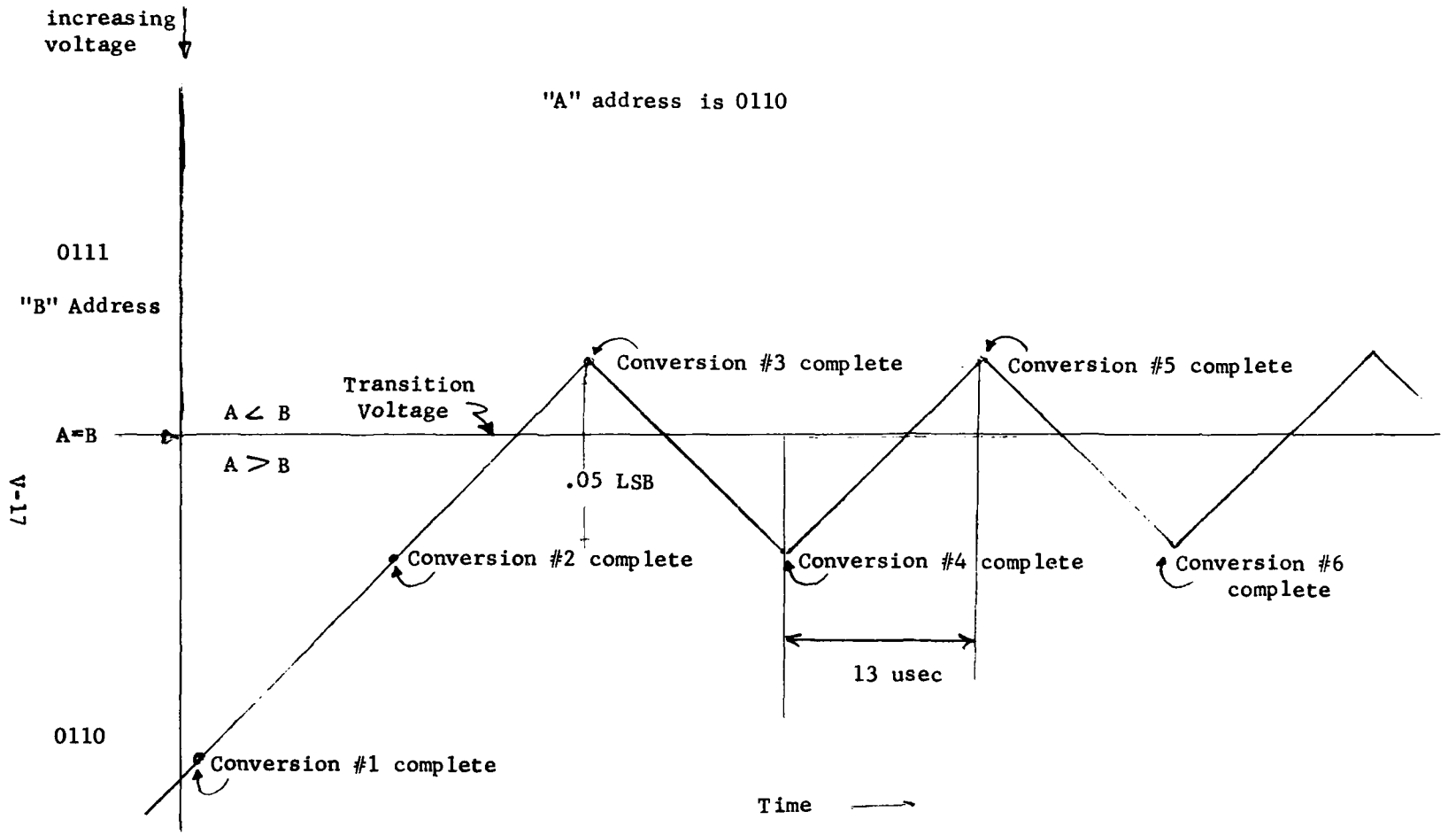


Figure 5.7. ADC input voltage vs time when measuring 0110 to 0111 transition voltage.

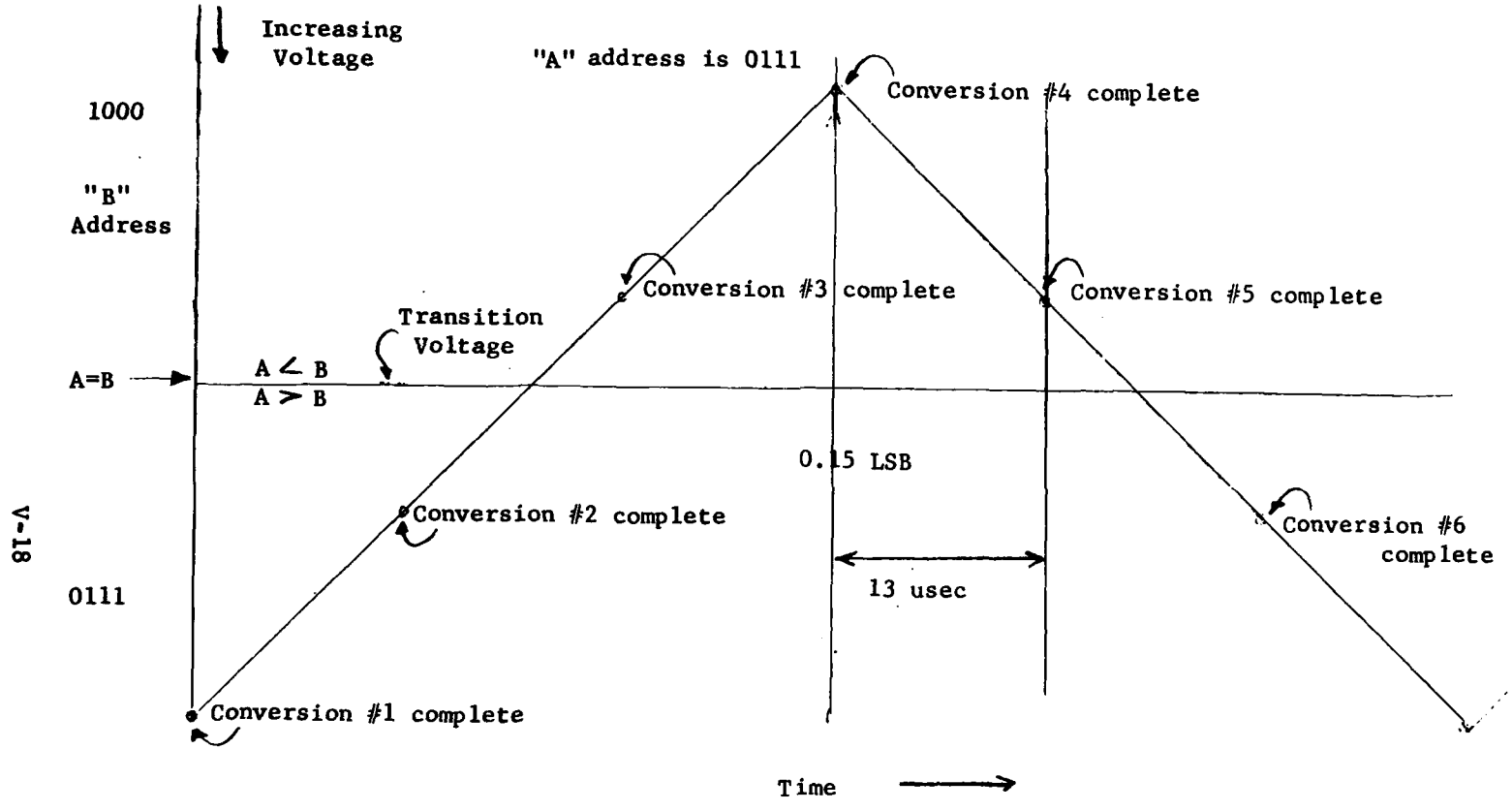


Figure 5.8. ADC input voltage vs time when measuring 0111 to 1000 transition voltage.

5.4 Automatic Test Development

Testing A/D converters, particularly 12 bits or more, is a difficult task and is generally only performed by the most sophistocated of the users. Traditionally, A/D converters were tested using a D/A converter in conjuction with an oscilloscope. The D/A converter generally had at least 4 bits more than the device to be tested. The implementation varied but in all cases the testing was tedious, time consuming, and required human data logging. Manufacturers of the devices, in an effort to reduce test time and costs, are attempting to automate the testing of A/D converters. Some already have.

A major portion of this characterization effort was devoted to the development of an automatic test capability for the S3260.

Once the decision was made to test A/D converters automatically, the next decision to be made was how to implement the testing. Did all transitions have to be tested or could an abbreviated test method be employed which tests bit errors and utilizes superposition to test the worst case linearity? Unlike the D/A converters for which the abbreviated test method has been used successfully by most manufacturers, the A/D converter transition voltages are not so clearly defined. A/D converters are tested at maximum rated speed which results in transient errors that will distort static bit weight errors. One of the objectives of the 5200 characterization effort will be to determine whether or not an abbreviated test method could be employed with sufficient confidence that devices with missing codes would be detected. It should be noted that when testing A/D converters, transition voltages are measured and not dc voltage levels. Transition voltages are nominally set at 1/2 LSB below nominal voltage levels to reduce quantization errors to $\pm$ 1/2 LSB.

Linearity is, without a doubt, the most difficult A/D converter parameter to measure accurately and unless clearly defined may confuse the user. Some vendors choose to use "Best Fit Linearity" as opposed to "End Point Linearity". One could argue that "Best Fit Linearity" would be achieved by utilizing a Least Squares Straight Line[1] but that would most certainly confound the less sophistocated user. GE would prefer to utilize "End Point Linearity" but, since high speed successive approximation A/D converters are not necessarily linear, "Best Fit Linearity" will be employed. "Best Fit Linearity" will be defined as the straight line parallel to the "End Point Linearity" straight line that distributes maximum positive and negative linearity errors equidistantly from it. This is a definition that the user can easily comprehend and apply.

To make the testing of a 12 bit A/D converter accurate utilizing a Tektronix S3260, it was necessary to design a reference module which contains an 18 bit reference DAC, buffer, active ground drives, and switching to provide the proper voltages and logic levels to test all of the device types in the slash sheet. Since the characterization efforts for the 562, 12 bit D/A converter, was performed concurrently with the 5200 series A/D converters, the reference module was designed to accommodate both testers. The reference module, in conjunction with the S3260 test adapter, can be utilized on the bench if the S3260 under-socket connections, power supplies and relay actuators, are implemented in the bench setup. Manual addressing of the reference DAC is provided via toggle switches. Display of the DUT output address can be accomplished by connecting a buffered 12 bit LED display to the DUT output address register via a pair of DIP clips.

The technique employed to measure transition voltage employs a dither which ramps slowly above and below the transition voltage. A more detailed description of the test circuit is contained within the text of this report. Part of the test development will be to select the proper dither voltage for the devices being tested. Too low a dither voltage and it will be down in the noise level. Too high a dither voltage and it will limit the range of differential non-linearity measurement. A finite amount of dither will provide some guard banding for detecting devices that might marginally exhibit missing codes.

5.4.1 Test Program Development

Software was developed for the Tektronix S3260 test system to provide for automatic testing of the MN5200 series of Analog-to-Digital converters. The test circuit used in conjunction with the S3260 is shown in Figures 5.4, 5.5 and 5.6.

Power Supply Currents

Supply currents are measured first with all bits off and then again with all bits on. + 15 VDC is forced on pin 15 and the current flow, I_{cc}, is measured. + 5 VDC is forced on pin 2 and the current flow, I_{LOG}, is measured. - 15 VDC is forced on pin 13 and the current flow, I_{ee}, is measured. For device types with an external reference - 10 VDC is applied to the external reference input and the current flow, I_{REF}, is measured. The limits for power supply currents were enlarged to encompass all manufacturer's devices. Due to differences in implementation of the A/D converter, the loads on the positive and negative supplies will vary from one manufacturer's device to another. The limitations on power supply currents will largely be imposed by the maximum power dissipation specified.

Power Dissipation

Power dissipation can be calculated from the supply currents according to the following equation:

$$P_D = (15\ I_{CC}) + (5\ I_{LOG}) - (15\ I_{EE}) - \underbrace{(10\ I_{REF})}_{\text{(for devices with external references only)}} \qquad [5.2]$$

Input Logic Voltage Levels

In order to test the limits on the input logic levels at which the device will still perform conversions, one conversion is attempted with "clock" and "start convert" inputs at logic "1" = + 2.0 V and logic "0"0 = + 0.8 V. Accuracy of the final conversion must be insured.

Output Logic Voltage Levels

The output logic levels are checked with all bits on and with all bits off. A 320 uA load is placed at the output with all bits on and the voltage, V_{OH}, is measured. Then a 3.2 mA load is placed on the output with all bits off and the voltage, V_{OL}, is measured.

Output Short Circuit Current

The "A" register is set to 1111 1111 1110 and short circuit output current, is measured for (1) address bits, (2) "End of Convert", and (3) "Serial Data Out".

Input Low Current

Force 0 volts on the "clock" and "start convert" inputs and the current flow, I_{IL}, is measured for each respectively.

Input High Current

Force + 5 volts on the "clock" and "start convert" inputs and the current flow, I_{IH} is measured for each respectively.

Clock Input Pulse Width

All static tests on the ADC will be performed with the minimum input clock pulse width, 200 ns.

Conversion Time

Conversion time is the minimum time required to perform a complete 12 bit successive approximation conversion. A + 2.2 uf solid tantalum capacitor should be connected between DUT pins 15 (+) and 10 (-) for conversion times less than 24 usec. All static tests will be performed at the maximum rated conversion speed.

Power Supply Sensitivity Tests

Power supply sensitivity tests will be performed both with all bits on and all bits off. V_{cc} is varied ± .45 V and the variation in the ADC transition voltage is recorded, PSS1. V_{ee} is varied ± .45 V and the variation in the ADC transition voltage is recorded, PSS2. V_{LOG} is varied ± 0.5 V and the variation in the ADC transition voltage is recorded, PSS3.

Absolute Accuracy

For unipolar devices accuracy will be measured with all bits on only. For bipolar devices accuracy will be measured with all bits on and again with all bits off. The "A" register is set to 1111 1111 1110 and the last transition voltage is measured. Then the "A" register is set to 0000 0000 0000 and the first transition voltage is measured. The accuracy of these measured transition voltages are compared with the specification limits on accuracy.

Zero Error

For a unipolar device zero error cannot be measured directly, extrapolation is required. First and last transition voltages are measured. A straight line is drawn between these points and extended to the voltage corresponding to the ADC address of 0000 0000 0000. Calculated voltage there + 1/2 LSB is the zero error, where an LSB = (Last transition voltage - First transition voltage)/4094. Zero Error = C_{T1} + LSB/2 - 0 where C_{T1} is negative for device types 1, 2, 9 and 10. Device types 7, 8, 15, and 16 are complementary to device types 1, 2, 9 and 10 so logic inputs to reference DAC (address) are complemented and 1/2 LSB is subtracted from the first transition voltage.

$$C_{T1} - \frac{LSB}{2} - 0 = \text{zero error}$$

where C_{T1} is positive

Linearity Testing

The circuit used to measure linearity of the MN5200 series of Analog to Digital converters is shown in Figures 5.4 & 5.5. The S3260 places an address in the "A" register, the input to the reference DAC. The output of the ADC then cycles between the address in the "A" register and that address plus 1 LSB. For example, if S3260 placed 0111 1111 1111 on the input to the reference DAC, the outputs from the ADC will alternate between 0111 1111 1111 and 1000 0000 0000. An abbreviated way of representing this transition is to place an asterisk after the address, i.e. 1000 0000 0000*. The output from the reference DAC is then summed with the input to the ADC in the error amplifier. The resulting error voltage is the amplified sum of the output of the DAC at one particular address and the ADC's transition voltage to the next address. Since the output of the DAC can be calculated at any address, the next ADC transition voltage can be determined by first dividing the error amplifier reading by the amplifier's gain, and then adding the output voltage of the DAC. Linearity for the 5200 ADC is specified as best fit straight line. Linearity will be measured as end point straight line. Best fit linearity will be obtained by adding max positive and max negative deviation from the straight line, dividing the result by two and offsetting the linearity curve accordingly. To measure the end point linearity of the ADC, the first and last transition voltages are used to establish an ideal straight line. All other transition voltages are compared to the ideal straight line.

Two basic techniques for measuring linearity error are employed. The first, called the abbreviated test method, tests only the 42 addresses listed in Table 5.2. These addresses consist of all of the major carries in addition to the two addresses below the major carries and one address above the major carries (where possible). The second, tests all transitions between 0 and full scale. In both cases the calculated ADC transition voltages are compared to the ideal straight line determined by the first and last ADC transition voltages to calculate the linearity of the device.

The initial measurements and adjustments for the "abbreviated test" and the "test all codes" method are identical. At the start of the test the "A" address is set to 0000 0000 0000 and the buffered reference DAC output is set to - 10.0000 V by adjusting the DAC offset potentiometer. This establishes V_{RDAC} (0). A Fluke model 8500A 5 1/2 digit DVM is used to take the measurements with an IEEE bus to interface it to the S3260. The "A" address is then set to 1111 1111 1111 and the buffered reference DAC output is set to + 9.9951V by adjusting the gain potentiometer. This establishes V_{RDAC} (FS). The general expression for the buffered reference DAC output is:

TABLES 5.2. Abbreviated Test - A Address Input Codes

A_{IN}			B^*			M
REF. DAC. ADDRESS			ADC TRANSITION VOLT			BIT #
0000	0000	0000	0000	0000	0001	1
		0001			0010	2
		0010			0011	3
		0011			0100	4
		0100			0101	5
		0101			0110	6
		0110			0111	7
		0111			1000	8
		1000			1001	9
		1101			1110	14
		1110			1111	15
	0000	1111		0001	0000	16
	0001	0000		0001	0001	17
	0001	1101		0001	1110	30
	0001	1110		0001	1111	31
	0001	1111		0010	0000	32
	0010	0000		0010	0001	33
	0011	1101		0011	1110	62
	0011	1110		0011	1111	63
	0011	1111		0100	0000	64
	0100	0000		0100	0001	65
	0111	1101		0111	1110	126
	0111	1110		0111	1111	127
	0111	1111		1000	0000	128
	1000	0000		1000	0001	129
0000	1111	1101	0000	1111	1110	254
0000	1111	1110	0000	1111	1111	255
0000	1111	1111	0001	0000	0000	256
0001	0000	0000	0001	0000	0001	257
0001	1111	1101	0001	1111	1110	510
0001	1111	1110	0001	1111	1111	511
0001	1111	1111	0010	0000	0000	512
0010	0000	0000	0010	0000	0001	513
0011	1111	1101	0011	1111	1110	1022
0011	1111	1110	0011	1111	1111	1023
0011	1111	1111	0100	0000	0000	1024
0100	0000	0000	0100	0000	0001	1025
0111	1111	1101	0111	1111	1110	2046
0111	1111	1110	0111	1111	1111	2047
0111	1111	1111	1000	0000	0000	2048
1000	0000	0000	1000	0000	0001	2049

$$V_{RDAC}\ (N) = V_{RDAC}\ (0) + \frac{V_{RDAC}\ (FS) - V_{RDAC}\ (0)}{4095} N \qquad [5.3]$$

$$V_{RDAC}\ (N-1) = V_{RDAC}\ (0) + \frac{V_{RDAC}\ (FS) - V_{RDAC}\ (0)}{4095} (N-1) \qquad [5.4]$$

The voltage V_{RDAC} (N-1) is derived because the ADC cycles between A $\geq$ Band A $<$ B, where B is the ADC output address.

Next, with all relays deenergized, both inputs to the error amplifier are grounded and the output offset voltage, E_o (0), is set as close to 0 as possible by adjusting the op-amp offset potentiometer, R 10 . E_o (0) is then recorded. This completes the initialization portion of of the "abbreviated test" and the "test all codes".

Abbreviated Test Method

In the abbreviated test the 42 addresses listed in Table 5.2 are generated by the S3260 and sequentially applied to the inputs of the reference DAC. The voltage at the output of the error amplifier, E_o (N), is recorded. Now that V_{RDAC} (N-1) and E_o (0) are known, the ADC transition voltages can be calculated from E_o (N).

$$E_o\ (N) - E_o\ (0) = - \left(\frac{R_F}{R_I}\right) (V_{RDAC}\ (N-1) + V_{ADCIN}\ (N)) \qquad [5.5]$$

$$\text{or } V_{ADCIN}\ (N) = - \left(\frac{R_I}{R_F}\right) (E_o\ (N) - E_o\ (0)) - V_{RDAC}\ (N-1) \qquad [5.6]$$

Transition voltages on the ideal linearity curve will hereafter be referred to as C_T (N). C_T (1) = V_{ADCIN} (1) and C_T (4095) = V_{ADCIN} (4095) since the first and last transition voltages establish the ideal end point linearity curve. The other transition voltages on the ideal linearity curve can be calculated from the expression:

$$C_T\ (N) = \frac{C_T\ (4095) - C_T\ (1)}{4094}\ (N-1) + C_T\ (1) \qquad 5\text{-}7$$

Bit errors (deviations from the ideal straight line) can now be determined:

$$\in (N) = \frac{V_{ADCIN}\ (N) - C_T\ (N)}{LSB} \quad \text{in LSB's} \qquad 5\text{-}8$$

where $$LSB = \frac{V_{ADCIN}\ (4095) - V_{ADCIN}\ (1)}{4094} \qquad 5\text{-}9$$

After all bit errors have been calculated, the addresses of the maximum positive bit weight error and the maximum negative bit weight error can be determined.

To generate the word for maximum positive bit weight errors a logic "1" is placed in the address if the corresponding bit weight error is positive. All other address bits are set to logic "0".

To generate the word for maximum negative bit weight errors a logic "1" is placed in the address if the corresponding bit weight error is positive. All other address bits are set to logic "0".

The latter two addresses (-1 LSB) are applied to the "A" address register in turn and the error voltages are measured. ADC transition voltages and bit errors are calculated as before.

The offset voltage, BFOE, to achieve "Best Fit Linearity" will be obtained as follows:

$$BFOE = \frac{\Sigma + NL + \Sigma - NL}{2} \quad \text{in mV} \qquad 5\text{-}10$$

Allow 1 sec before each measurement (or more if necessary).

Major Carry Errors (MCE_N) are the differences in size between an LSB at a major carry and an LSB averaged over the entire range of the ADC. They are calculated from the ADC transition voltages according to the following equation:

$$MCE\ (N) = \frac{V_{ADCIN}\ (N + 1) - V_{ADCIN}\ (N) - LSB}{LSB}$$

The LSB carry, MCE (12), cannot be calculated

The previous measurements and calculations of bit weight errors and major carry errors are affected by hysteresis. The following calculations derive static bit weight errors and static major carry errors. The major carry transition is ignored and the transition after the major carry is measured. The difference between the two transitions before the major carry provides the valve used for an LSB. The static bit weight errors are calculated as follows:

$$(N)_{STATIC} = \frac{V_{ADCIN}\ (N)_{STATIC} - C_T\ (N)}{LSB_{STATIC}}$$

where $LSB_{STATIC} = V_{ADCIN}\ (N-1) - V_{ADCIN}\ (N-2)$

and $V_{ADCIN}\ (N)_{STATIC} = V_{ADCIN}\ (N + 1) - LSB_{STATIC}$

From the equation for LSB_{STATIC} it can be seen that static bit weight errors cannot be determined for the 2 last significant bits of an address.

Static major carry errors can be calculated in a similar fashion:

$$MCE_{STATIC}\ (N) = V_{ADCIN}\ (N + 1) - V_{ADCIN}\ (N-1) - LSB_{STATIC}$$

where LSB_{STATIC} is calculated as it was for static bit weight errors.

Measure All Transitions

After the ADC is allowed to warm up for a sufficient amount of time, the S3260 sequentially applies all addresses to the "A" register. The error voltage is measured and recorded at each address, and from these error voltages the ADC transition voltages can be determined as before. Bit Errors (static and dynamic), maximum positive and negative bit weight errors, nonlinearity, and major carry errors (static and dynamic) are all determined as they were in the abbreviated test method.

SECTION VI

12 Bit D/A Converter

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SECTION VI

CHARACTERIZATION OF 12-BIT D/A CONVERTERS

MIL-M-38510/121

6.1 Background and Introduction

The increased use of microprocessors in military systems has stimulated interest in JAN 38510 specification development of data converters and associated devices which are needed to interface analog sources, sensors, loads, and displays with digital processing hardware. In 1978, the first JAN D/A Converter slash sheet was developed, MIL-M-38510/113. The DAC08 and DAC08A devices, 8-bit monolithics with dual complementary current outputs, fully voltage compliant, low cost and multi-sourced were selected for the slash sheet.

The need for higher-resolution D/A Converters will be filled by MIL-M-38510/121, 12-bit D/A Converters. Monolithic 12-bit converters have only recently begun to displace the hybrid devices which have predominated the marketplace in past years, and there is reason to believe this trend will continue. The 562 is one of the first 12-bit monolithics that is multi-sourced and has been identified by users as a desirable component for military systems.

While multi-sourcing has many advantages, it presents some difficulty in preparing a common specification, at least for linear devices and in particular for data converters. Of three manufacturers which offer the 562, no reasonable compromise of specifications could be negotiated to include even two manufacturers on one device type. Consequently, there are two device types in the slash sheet, each sourced by only one manufacturer; the third device is not included at this time for reasons explained within the following text.

The development of test circuits and techniques for 12-bit data converters has been a considerably more difficult task than that for 8-bit devices. For example, when one is measuring linearity to limits of 1/2 LSB, it is desirable to have a test method accurate to $\pm$0.05 LSB, or approximately $\pm$0.001%. Noise and differences in ground voltages alone can degrade the measurements, not to mention drift and meter accuracy/linearity. These concepts are also addressed within the text.

An attempt was made in this device characterization to measure linearity both with the "Abbreviated Linearity Test Method", using bit weight errors and superposition, and with the "All Codes Linearity Test Method" to see if the data correlated well. How well the data correlates will

be largely determined by how much superposition error is present. Superposition errors referred to here are bit interactive errors. The devices tested correlated well but it is to be expected that some manufacturers devices will not correlate well. Devices with appreciable interactive errors may not pass the Abbreviated Linearity Test because of the Σ(+) NL + Σ(-) NL test. Restricting the summation of Bit Weight Errors to ± 0.1 LSB will be difficult to pass if interactive errors are appreciable. However, failing to meet this requirement does not necessarily mean that the device will not meet the overall linearity requirement of ± 0.5 LSB. It is for that reason that the device then be subjected to an "All Codes Linearity Test." A failure therein would be final.

In like manner implementation of a ± 0.9 LSB differential non-linearity (MCE) insures that a device with a marginal error will not be judged monotonic (or non-monotonic) when non-linearities and measurement errors may make the device look better (or worse) than it really is. If the MCE is within the range ± 0.9 to ± 1.1 LSB the device then would be subjected to an all codes linearity and monotonicity test. The all codes monotonicity test as implemented herein is much more accurate. A failure therein would be final.

6.2 Description of Device

The 562 is a monolithic 12 bit D/A Converter with guaranteed monotonicity over the full military operating temperature range, -55 to 125°C. The device is mounted in a hermetically sealed ceramic 24 lead dual in-line package. The 562 accepts a reference voltage of 0 to + 10 V and provides a binary weighted output current proportional to the product of the digital address input and the reference voltage. When the reference voltage is variable the device is a two quadrant DAC. On the other hand, when the reference voltage is fixed the device is simply a DAC with a nominal output current of -2 mA. Laser-trimmed internal gain , voltage-range and bipolar offset resistors are incorporated to provide accurate output voltages when used in conjunction with an external amplifier. Scaling errors are minimized because of low resistor tracking TCR; approximately 1 ppm/C°. The following ranges can be pin-programmed:

0 to + 10 V,	0 to + 5 V ,
- 5 to + 5 V,	-2.5 to + 2.5 V,
-10 to + 10 V	

The digital code for the device is natural binary "positive true". In the bipolar mode the digital code is offset binary

Address In	Unipolar	Bipolar
0000 0000 0000	0 V	- 10.000 V
1000 0000 0000	+ 5.000 V	0 V
1111 1111 1111	+ 9.99878 V	+ 9.99572 V

The device is CMOS or TTL compatible. With pin 2 connected to pin 1 the device is CMOS compatible and the internal logic threshold is $\frac{V_{cc}}{2}$ and the voltage may be 4.75 to + 15.8 V. With pin 2 open for device type 01 and grounded for device type 02 the logic threshold is approximately + 1.4 V and the device is TTL compatible with V_{cc} = + 5 V ± 10%. The 562 is available in both binary and BCD versions.

The 562 current output is the weighted sum of the outputs of three similar groups of binary scaled quad current generators, controlled by V_R. The logic inputs steer these currents through non-saturating bipolar-transistor current switches to either ground or the respective quad output bus. The output currents from the 2nd and 3rd quads are attenuated by 16:1 and 256:1 respectively for binary and by 10:1 and 100:1 respectively for BCD. The attenuated outputs are then summed with the unattenuated output of the 1st quad. The output current is then the sum of 12 individually switched currents having a binary relationship.

The current generating transistors from each quad group have emitter areas in the ratio of 8:4:2:1. The ladder network resistances are in the ratio of 1:2:4:8. With equal voltages applied to the resistors, the emitter currents are therefore in a binary ratio. Because of the weighted emitter area, the transistors operate at equal emitter current densities and therefore have nearly equal V_{BE}'s and h_{FE}'s. The control amplifier (A1) drives the bases of the constant current transistors and a reference transistor, which has h_{FE} and V_{BE} matched to those of the constant current and bit switching transistors.

V_R is applied to the externally trimmable gain resistor (R1) to set a reference current of 0.5 mA. Amplifier A1 establishes the appropriate base voltage to force collector current of Q1 equal to I_R. Variations in h_{FE}, V_{BE}, or supply voltage with time and/or temperature are sensed in the reference amplifier circuit and the reference amplifier adjusts V_{BE} to maintain the collector current of Q1 (and therefore the bit currents) constant in the presence of these variations.

6.3 Characterization of the 562

6.3.1 STATIC TEST PARAMETERS (See Table 6.1)

Supply Current (I_{CC})

The current drain on the V_{CC} supply is measured with all bits on in the CMOS made since it represents the worst case. V_{CC} = + 15 V.

Supply Current (I_{EE})

The current drain on the V_{EE} supply is measured with all bits on in the CMOS mode. V_{EE} = - 15 V.

Logic "1" Input Current (I_{IH})

Logic "1" input current is measured in the CMOS mode with V_{CC} = + 15 V since it represents a worst case.

Logic "0" Input Current (I_{IL})

Logic "0" input current is measured in the CMOS mode with V_{CC} = + 15 V. Since it represents a worst case.

Full Scale Current (I_{RS})

DUT output current is measured with all bits on. Subtracting the value of output current with all bits off from that obtained with all bits on provides a measure of I_{FS}.

Unipolar Zero Current (I_{oz})

Unipolar zero current is leakage current in the unipolar mode with all bits off. It is specified as a percent of measured full scale current (I_{FS}) at + 25°C and is specified separately for CMOS and TTL modes.

Unipolar Zero Current Drift $\left(\frac{\Delta I_{FS}}{I_{FS}\,\Delta T}\right)$

Unipolar zero current drift is the average temperature coefficient of unipolar zero current. The average temperature coefficient is measured from + 25 to + 125°C and from -55 to + 25°C. Neither value shall exceed the limits specified in Table II. I_{FS} in the expression for unipolar zero current drift is I_{FS} at + 25°C.

Gain Error (G_{ϵ})

The 562 D/A converter provides a current output that is proportional to the digital address applied to it. The output current has a ± 25% tolerance but provided within the device is a tapped span resistor which may be used in conjunction with an external operational amplifier. The span resistor is laser trimmed to offset the loose tolerance on output current and provide a voltage gain tolerance of ± .25% at the amplifier output. Unipolar gain is measured and it is defined as the difference between the output voltage with all bits on and the output voltage with all bits off with an applied reference voltage of + 10.000 VDC. Gain error is specified in ppm of Full Scale Voltage (FSV), + 10V. Gain error is specified separately for CMOS and TTL modes.

Gain Error Drift $\left(\frac{\Delta G_{\epsilon}}{FSV\ \Delta T}\right)$

Gain Error Drift is the average change in gain as a function of temperature. The average temperature coefficient is measured from +25 to +125°C and from -55 to +125°C. Neither value shall exceed the limits specified.

Bipolar Offset Error (BPOE)

Bipolar Offset Error is the voltage measured at the DUT output (pin 9) with + 10.000 V applied to the bipolar offset resistor (pin 7) and - 10.000 V applied to the 20 volt span resistor (pin 11) with DUT pins 8 and 9 connected together. BPOE includes the effects of unipolar zero (leakage) current.

Bipolar Offset Drift $\left(\frac{\Delta BPO}{FSVR\,\Delta T}\right)$

Bipolar Offset Drift is defined as the change in offset voltage with respect to full scale per centigrade degree temperature change.

Power Supply Sensitivity From V_{CC} In TTL Mode (+PSS1)

The change in output voltage is measured for a ± 10% change in V_{CC} from nominal + 5 VDC with V_{EE} at nominal - 15 VDC. Measurement is made with all bits off and also with all bits on. Neither change in output voltage shall exceed the limits specified in Table 6.1.

Power Supply Sensitivity From V_{CC} in CMOS Mode (+PSS2)

Same as PSS1 except V_{CC} nominal is + 15 VDC and DUT pins 1 and 2 jumpered together.

Power Supply Sensitivity From V_{EE} in TTL Mode (-PSS1)

The change in output voltage is measured for a ± 10% change in V_{EE} from nominal - 15 VDC with V_{CC} at + 5 VDC. Measurement is made with all bits off and also with all bits on. Neither change in output voltage shall exceed the limits specified in Table 6.1.

Power Supply Sensitivity From V_{EE} IN CMOS Mode (-PSS2)

Same as -PSS1 except that V_{cc} is set at a nominal value of + 15 VDC and DUT pins 1 and 2 are connected together.

Summation of Positive Bit Errors (Σ NL+)

Assuming negligible superposition errors, the application of the address with logic "1"s for those bits which when tested alone exhibited positive bit errors should yield the maximum positive deviation from the ideal linearity curve, a straight line between zero and full scale.

Summation of Negative Bit Errors (ΣNL-)

Assuming negligible superposition errors, the application of the address with logic "1"s for those bits which when tested alone exhibited negative bit errors should yield the maximum negative deviation from the ideal linearity curve, a straight line between zero and full scale.

Bit Interaction (Σ NL(+) + Σ NL(-))

At full scale Σ NL(+) + Σ NL(-) is assumed to be zero. It follows that this relationship shall hold over the full range of the DUT. Any deviation from this relationship, aside from measurement error, shall be assumed to be due to non-linearity (superposition errors). Devices which exhibit a bow in the linearity curve from zero to full scale will exhibit superposition errors. Assuming a measurement accuracy of ± .05 LSB, the limits applied to this parameter were chosen to be large enough to measure the existence of superposition errors. Failure to pass this test does not constitute a module failure but requires the additional all codes linearity and monotonicity testing. A failure to pass

the latter constitutes a module failure. Successful completion of the all codes tests insures that the device is linear to within specified limits and is monotonic.

Major Carry Errors (MCE)

The major carry test is intended to insure that the DUT is monotonic. To be monotonic the output voltage increment must be greater than 0 V for each increment of DUT address from all "0"s to all "1"s (0 to 4095). Assuming negligible superposition errors and no dynamic errors, the incremental voltages at the major carries, MC1-MC11, should represent the worst case differential nonlinearity. A differential non-linearity of less than ± 1 LSB insures monotonicity. Since non-monotonicity can be disastrous in many device applications and the measurement accuracy of the tester is ± .05 LSB (max), a tolerance of ± 0.9LSB is placed on this parameter. Failure to pass this test within ± 0.1 LSB will not constitute a failure but will require the vendor to test all codes monotonicity and linearity. Successful completion of the latter insures that the device is monotonic.

6.3.2 DYNAMIC TEST PARAMETERS (+ 25°C only)

The settling time test measures the response time between the 50% point of the input transition (all bits on to all bits off or all bits off to all bits on) and the point in time at which the output settles to within ± 1/2 LSB of final value. For a device type 01, ± 0.24 uA = ± 1/2 LSB corresponds to ± 1.22 mV. For a device type 02, ± 0.61 uA = ± 1/2 LSB and with a 2K load ± 1/2 LSB corresponds to ± 1.22 mV.

6.3.3 STATIC TEST CIRCUIT

The static test circuit shown in Fig. 6.2 is a simplified version of the test circuit utilized on the S3260. Not shown are the ground drivers that were required because of the physical separation of the reference DAC, the test adapter circuitry and the DUT. Also not shown is a voltage follower buffer inserted between the reference DAC reference voltage output (pins 52, 53 on DAC 1138) to minimize output voltage shifts due to loading. Table 6.2 indicates the relay states for the various parameters to be tested.

A1 is the error amplifier which converts the DUT output current to voltage and compares it to the corresponding Ref. DAC output and amplifies the difference. The amplified difference voltage is used to provide an accurate measure of DUT gain, linearity, power supply sensitivity, and in a slightly different circuit configuration to test BPOE. With all relays deenergized the error amplifier inputs are both connected to ground the through 3KΩ resistors and the amplifier offset voltage may be trimmed to zero. The offset trim is a 20 KΩ potentiometer connected between amplifier pins 1 and 8 with the wiper tied to + 15 V.

A2 is a unity gain inverting amplifier that is employed only for BPOE measurements. It provides an accurate -10.000 VDC.

A3 and A4 are Reference Voltage and Reference DAC output buffer amplifiers. They are tested and trimmed (if necessary) at the start of any sequence of device testing, utilizing a Fluke 8500 DVM (or equiv.). Once done the test/cal. need not be repeated for subsequent DUT tests.

Input and output currents were measured by forcing the appropriate voltage levels and measuring currents. Just how these tests are implemented will be governed by the equipment available to the tester.

6.3.4 SETTLING TIME TEST CIRCUIT

Figure 6.3 shows the settling time test circuit employed by GEOS to test device types 01. D1 biases Q1 such that the emitter of Q1 (DUT output) is maintained approximately at 0V. Q1 is a common base amplifier which converts DAC output current variations to voltage variations. The common base amplifier was selected because of its excellent high frequency response. The collector voltage swing is clamped to within a Schottky voltage drop of + 5 VDC. Capacitance in the collector circuit of the Q1 transistor should be minimized because of the large value of R. For a device type 01 R = 5K and for a device type 02 R = 2K. V_L ≈ + 15 V for "turn on" (all bits off to all bits on) and + 5 V for "turn off" (all bits on to all bits off). Q2 and Q3 provide differential buffering of the Q1 output.

To test all bits off to all bits on settling time V_L is adjusted for a Q1 output voltage of +5V with all bits on (V_C ≈ + 15 V) and R_L = 5K. A square wave voltage is applied to the DUT address inputs (Vins) and the scope preamp is adjusted so the flat portion of the waveform corresponding to all bits on is on the center line of the screen with a sensitivity of 1 mV/cm. The positive edge of V_{in} is used to trigger the scope and the sweep start is marked on a vertical graticule of the scope trace. Settling time is then measured, the time required for the output to settle to within ± 0.5 LSB (or ± 1.22 mV).

To test "all bits on to all bits off" settling time, V_L is adjusted for a Q1 output voltage of +5V with all bits off and R_L = 5K. A square wave voltage is then applied to the address inputs (V_{in}). The scope trace is adjusted to locate the flat portion of the output waveform corresponding to "all bits off" on the center line with a vertical sensitivity of 1 mV/cm. The sweep trigger alignment may need readjustment since the scope must trigger on the negative edge of V_{in}. Settling time is then measured, the time required for the output voltage to settle to within ± 1/2 LSB (± 1.22 mV). Figure 6.3 shows the waveforms and Figure 6.7 shows photographs of typical settling times measured.

6.3.5 DEVICES USED FOR TESTING

There were 13 devices tested of which 6 were obtained directly from Analog Devices, 6 were obtained from Analog Devices through RADC, and 1 was purchased by GEOS. Data is only tabulated for 12 devices because one of the six devices obtained directly from Analog Devices with + 25°C data failed during the course of test program development. Repeated rapid cycling between + 25°C, + 125°C and - 55°C may have been responsible for the failure: Device S/N 4311 failed.

S/Ns 4310 - 4315	Samples obtained from Analog Devices with + 25°C data
S/Ns 19, 20, 21, 25, 36 & 48	Samples obtained from RADC
S/N 5	Purchased sample

All devices characterized were Analog Devices only.

The devices with S/Ns 4310 - 4315 appeared to be significantly better than the others in settling otherwise differences were not significant.

Three device type 02s were tested and found to be out of specification. However, the origin of the devices is unknown. Harris has been asked to submit samples with data (if possible) for characterization.

6.4 Automatic Test Development

One of the primary considerations in attempting to test a 12 bit D/A Converter on the Tektronix S3260 is, "How does one measure DAC output linearity to ± .001% and fast enough" that the S3260 isn't tied up for long periods of time. GEOS chose to implement a comparative type test which utilizes a Reference Module in conjunction with the S3260 test adapter to test the device's linearity and accuracy. The reference module contains an 18 bit D/A Converter (12 MSBs used) some switches, some buffer amplifiers, and active ground drivers. It was designed to interface with D/A and A/D Converters with 12 bits or more. It contains switching, logic, and buffer amplifiers and is capable of interfacing accurately with A/D and D/A converters of various ranges and codes. It was primarily designed to interface with the 562 series of 12 bit D/A Converters and the 5200 series of 12 bit A/D Converters. See Figure 6.6.

Another consideration in testing devices with such accuracy on the S3260, or any other automatic tester for that matter, is grounding and line drops. If the test circuits were designed for bench test, the circuitry would be kept close together and unipoint grounding employed. All of the precautions would be taken to minimize voltage drops on critical wires, avoid ground loops, and prevent oscillations. However, maintaining the close proximity and unipoint grounding on the S3260 is next to impossible. Therefore an alternate approach was taken. Active ground drivers (See Fig. 6.1) consisting of a cascaded connection of an OP 05 amplifier and a hybrid driver (LH0002) in the voltage follower configuration were employed to drive the DUT and adapter grounds separately to the same ground potential as the reference module ground. Care was taken in the selection of adapter devices to minimize power consumption (by using low power Schottky for example) and keeping the driven grounds disconnected from machine ground. Offset voltage trims were implemented on the OP 05s to enable adjustment of the DUT and adapter grounds to 0 V relative to the Ref. D/A ground. The technique worked exceptionally well and contributed largely to the ultimate success in obtaining better than ± .05 LSB measurement accuracy on linearity measurements. A 12 bit D/A converter in the unipolar mode on the 0 to 10 V range has an LSB voltage increment value of 2.44 mV. ± .05 LSB equals ± 122 mV, a very small voltage.

Also employed, as shown in Figure 6.2 are buffer amplifiers for the Reference D/A output and the Reference Voltage output. The amplifiers are differential and remote ground and output sense lines are employed to prevent line drop from deteriorating measurement accuracies.

It should be noted that the reference module when used with the S3260 test adapter provides a simple setup for bench testing. Aside from some test equipment, all that is required is the undersocket card interface. This feature enables the DUT to be tested with access to all of the adapter circuitry on the under socket card that is not readily accessible on the S3260.

The method employed for testing the linearity and accuracy of the 562 is illustrated in Figure 6.2. The Reference D/A output voltage is fed to the 10 volt span resistor (DUT pin 10) via relays K1 and K5. Both Reference D/A output drive and Reference D/A output sense lines are switched separately and connected together at DUT pin 10. For any given DUT address the difference between the DUT output and the Reference D/A output are compared, inverted and amplified. Use of the 10 volt span resistor is possible because the span resistors are laser trimmed to compensate for full scale current deviations from nominal and provide nominal output voltage when used in conjunction with a zero offset external op amp. If full scale current is low by 10% from nominal then the span resistor will be high by 10%. With

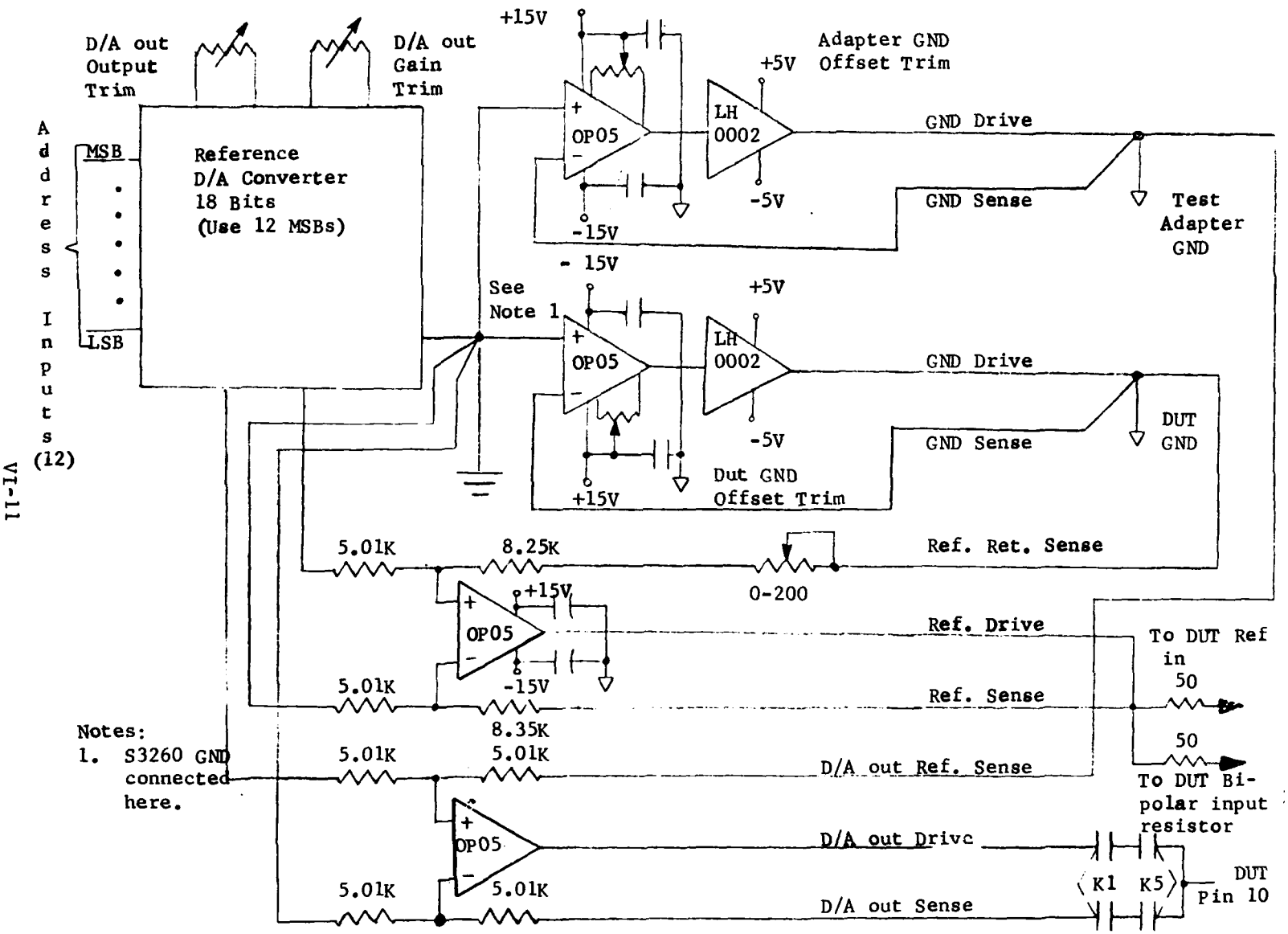


Figure 6.1. Simplified Interconnect Schematic.

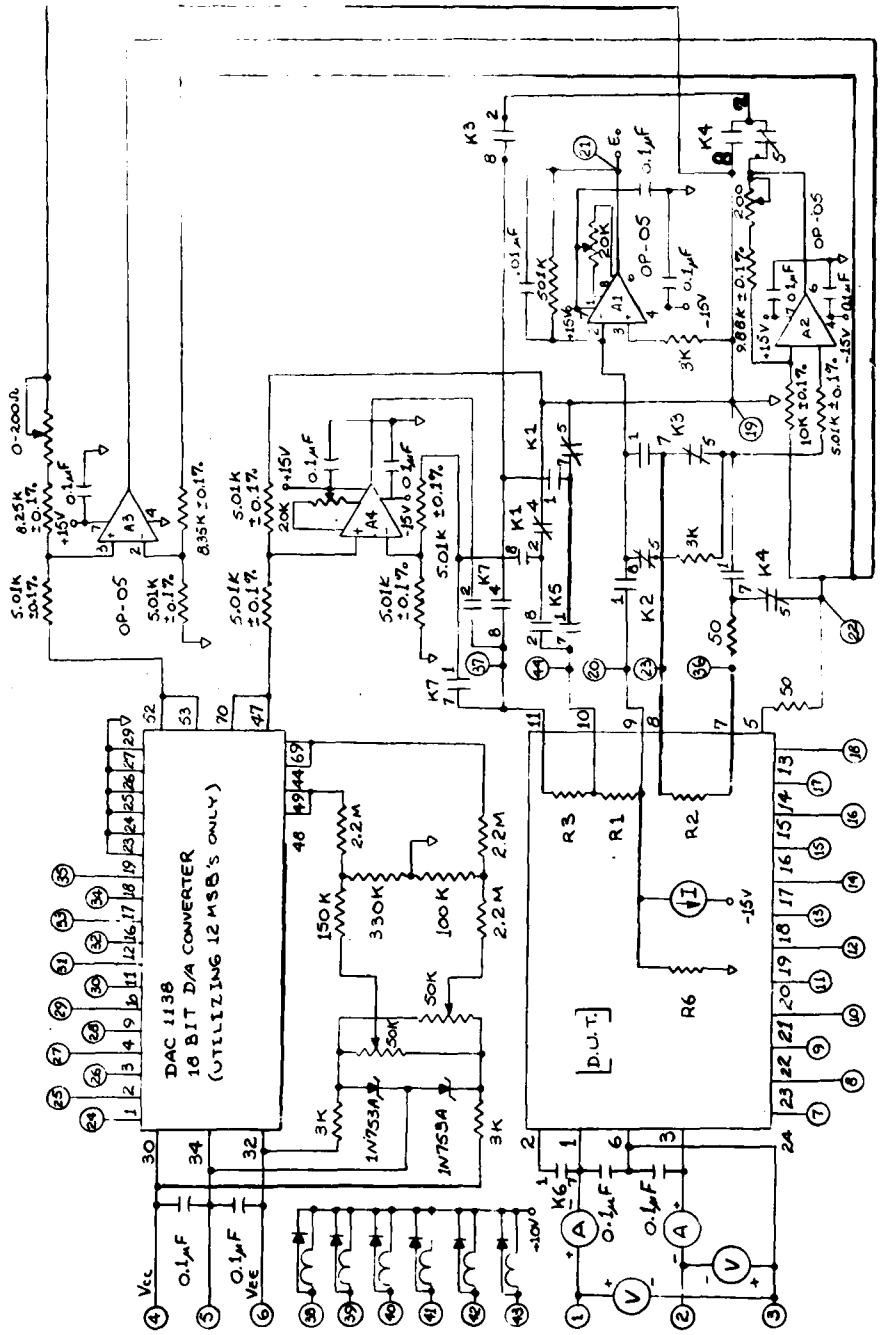


Figure 6.2. Test Circuit For Static Tests.

all relays deenergized the error amplifier offset voltage is trimmed to 0V, E_o = 0 V. The Reference voltage is adjusted to + 10.0000 V a adapter pin 22, as read on a Fluke 8500A DVM. The Reference D/A address inputs are set to all zeros, relays K1 and K5 are energized and the Reference D/A output voltage at DUT pin 10 is adjusted to (offset adj) to - 10,000 V, as read on the Fluke 8500. The Reference D/A address inputs are then set to all ones and the Reference D/A output voltage at DUT pin 10 is adjusted (gain adj) to + 9.9951 V, as read on the Fluke 8500. The Reference D/A output voltage, the Reference voltage, and the error amplifier have been calibrated and the test proceeds. With the DUT address bits all zeros, the Reference D/A output voltage is incremented by a small but finite voltage and the change in voltage at the error amplifier output noted. Dividing the change in output voltage by the change in input voltage provides the error amplifier gain (inverted) which is necessary to accurately measure the Reference D/A output voltage divided by the 10 V span resistance for a given address is compared to the DUT output current for a corresponding address. It should be noted here that the Reference DAC employed required complimentary logic. In Table the codes are shown as such, eg all 0's applied to the DUT provides a nominal - 9.997 KV (equivalent) output. All 1's applied to the Reference D/A provides a nominal + 9.9975 V output and all "0"s applied to the Reference D/A provides a nominal 0 V output. The reference module enables a complimentary of the Reference D/A address inputs to enable the same address codes to be applied to both.

To measure linearity, the DUT equivalent output voltages (I_o R_1) at zero and full scale are obtained by measuring E_o (adapter pin 31) for all DUT and Reference D/A out bits off and for all DUT and Reference D/A out bits on respectively. The DUT equivalent output voltages are calculated using the following relationship

$$I_o R_1 = - \left(\frac{E}{G} + \text{Reference D/A out} \right)$$

A straight line is established between these two points and subsequent measurements of DUT outputs for any given address can be compared to the straight line which is the ideal linearity curve. The equations for linearity and gain accuracy are given in more detail written the automatic test program development portion of this report.

One other important factor to consider in testing 12 bit D/A converters is temperature stability. Warm up time before test varies from vendor to vendor. The device dissipates as much as 600 mW and it will take a finite amount of time for temperature to stabilize upon turn on. Just how long the stabilization period allowed should be depends upon how fast the codes are tested. Vendors using the abbreviated test method for measuring linearity are not as sensitive but not insensative to thermal shifts. In testing the devices on the S3260

in the all codes linearity test mode the data obtained was very sensitive to stabilization time just as the data would be in a bench test setup. All final test data was taken, abbreviated and all codes, after a soak at temperature of 12 minutes. The long stabilization period was probably due to the fact that the temptronics unit cools the DUT directly but does not cool the lower portion of the DUT connector: There is a steady flow of room underneath. The stabilization time is probably related to the time it takes for some equilibrium condition to occur.

6.4.1 Test Program Development

A test program was developed for the Tektronix S-3263 to enable automatic testing of the 562, 12 bit monolithic D/A converter. Figure 6.2 shows the schematic diagram of the test circuit which includes the Reference Module and the S-3263 Test Adapter (see Figure 6.5 and 6.6 for photographs).

A calibration sequence is always run at the start of testing to insure that the zero and full scale output voltages of the Reference DAC and the DUT reference voltage are accurate. Adjustments are provided on the Reference Module for trimming the latter voltages. For calibration there are jacks provided on the Test Adapter to connect an external, highly accurate, DVM (e.g. Fluke Model 8500A or HP Model 3455A).

The test program proceeds as follows:

1. Power Supply Current from V_{cc} (I_{cc})

   I_{cc} is measured with all DUT address inputs at logic 1's. +15VDC is forced to pin 1 and I_{cc} is measured. (K5 is energized)

2. Power Supply Current from V_{ee} (I_{EE})

   I_{EE} is measured with all DUT address inputs at logic 1's. -15 VDC is forced to pin 6 and I_{EE} is measured. (K5 is energized)

3. Logic "1" Input Current, I_{LH} (CMOS)

   Logic "1" input current is measured by forcing +15 VDC on I/O pins 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, and 35, one at a time and measuring I_{LH}. (K6 energized)

4. Logic "0" Input Current, I_{LL} (CMOS)

   Logic "0" input current is measured by forcing 0 VDC on pins 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, and 35, one at a time, and measuring I_{LL}. (K6 energized)

5. Full Scale Output Current, I_{oFS} (TTL)

   Full scale out current is measured by setting the DUT address inputs to all 1's, forcing the output pin 22 to 0 VDC, and measuring the current flow, I_{oFS}. V_{cc} = + 5 V (No relays energized)

6. Zero Scale Output Current, I_{oZ}. (TTL)

   Zero scale output current is measured by setting the DUT address inputs to all 0's, forcing the output pin 22 to 0 VDC, and measuring the current flow, I_{oZ}. V_{cc} = + 5 V (No relays energized)

7. Zero Scale Current, I_{oZ} (CMOS)

   Same as 6, except V_{cc} = + 15 V and (K6 energized)

8. Zero Scale Drift $\left(\frac{I_{OZ}}{I_{FS}(25°C)\Delta T}\right)$

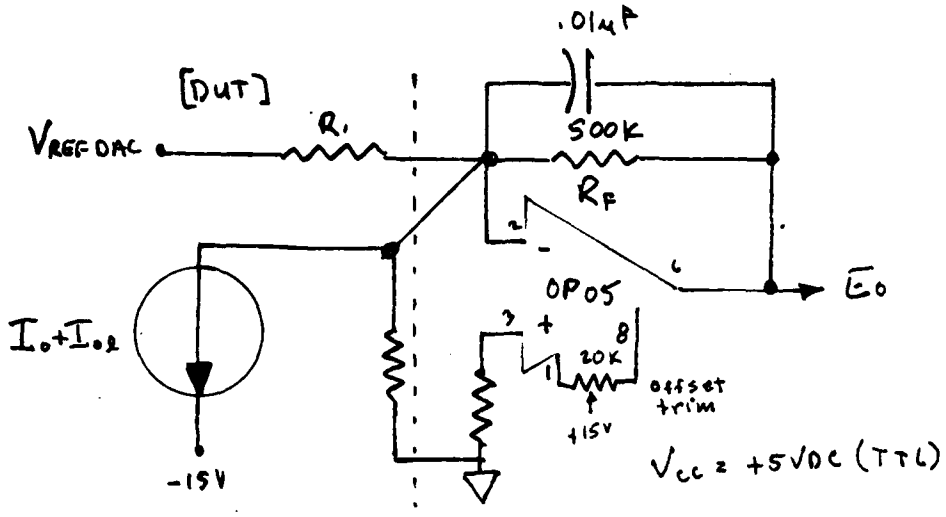
   Test is performed as in 6 & 7 and the value of I_{oZ} noted for each temperature at which test is performed. For temperature ranges tested within the operating temperature range of -55 to +125°C the drift shall not exceed the limit specified in Table 1.

9. Bipolar Offset Current, I_{BIP}.

   The reference voltage, + 10 V, is applied at pin 19 and appears across the bipolar offset resistor (R_2) and a 50 Ω series resistor with K3 and K 4 deenergized. $I_{BIP} = \frac{V_R}{.05K}$ where V_R is the measured voltage drop across the 50 Ω resistor.

10. Gain Error (GE) in TTL mode

    Unipolar gain error is measured with the test circuit configured as in Fig. 2 (K1, K2 and K5 energized)



Simplified schematic.

(a) Set DUT and REF DAC address inputs to all zeros (output off) and measure $E_o(o)$. This voltage included REF DAC offset, OP05 offset, and DUT Unipolar Offset.

(b) Set DUT and REF DAC address inputs to all ones (outputs on) and measure $E_o(FS)$.

$$E_o = E_o(FS) - E_o(o) \qquad [6\text{-}1]$$

Let $\frac{1}{R_x} = \frac{1}{R_I} + \frac{1}{R_o}$

The equation for output voltage can then be written:

$$E_o = G1\left[V_{REF}(\bar{n}) + V_{ROS} + (I_o(n) + I_{oZ})\,R1\right] \pm \left[\frac{R_x + R_F}{R_x}\right] V_{xo}$$

$$= -I_o(n)\,R_F + G1\,V_{REF}\,(\bar{n}) + \underbrace{\frac{V_{ROS}\,G1 - I_{oZ}\,R_F \pm \left(\frac{R_F + R_x}{R_x}\right) V_{xo}}{\text{FIXED OFFSET}}} \qquad [6\text{-}2]$$

for any address . Amplified noise, offset current, offset drift, and Zi are neglected.

where

I_{oZ} = DUT leakage current (all bits off)

V_{ROS} = REF DAC offset voltage

and V_{xo} = external op amplifier input offset voltage (OP-05). Combining offset and leakage terms:

$$E_o(o) = - I_{oZ} R_F - V_{ROS} \left(\frac{R_F}{R_1}\right) \pm \left[\frac{R_F + R_x}{R_x}\right] \qquad [6\text{-}3]$$

Substituting in eq 6-2

$$E_o = I_o R_F - V_{REF} \frac{R_F}{R_1} + E_o(o) \qquad [6\text{-}4]$$

Since the exact value of R_1 is not known, the gain $\frac{R_F}{R_1}$ must be measured. With all bits off on the DUT and the REF DAC measure $E_o(o)$. Leaving the DUT in off state, address REF DAC input with 0000 0000 1110 and measure E_o (14).

$$G1 = \frac{R_F}{R_1} = - \frac{(E_o(14) - E_o(o))}{(\frac{+10}{4096})(2^3 + 2^2 + 2^1)} \qquad [6\text{-}5]$$

Assuming that $+\frac{10.00}{4096}$ is an LSB of REF DAC

S3260 measurement accuracy for G1 $\approx \pm$ 0.4%

then

$$E_o = E_o\ (FS) - E_o(o) = - \left[(I_o(FS) - I_o(o))\ R_F + V_{REF}(FS) \frac{R_F}{R_1}\right]$$

FS output voltage = $I_o(FS) - I_o(o)\ R_1 =$

(referred to error amp. input) $\approx \frac{E_o(FS) - E_o(o)}{G1} - V_{REF}\ (FS)$

$$= V_{REF}\ (FS) + I_o\ (FS)\ R_1 \qquad [6\text{-}6]$$

$$G_{\epsilon} = \frac{E_o(FS) - E_o(o)}{G1} \quad (6\text{-}7)$$

(spec. is given in mV)

Device Types 01 Max error amplifier output voltage .

If R_F = .5M and R_1 = 5 K ± 25% (Init. Tol.)

E_o (max) = G1 (max) x Unipolar gain error (max)

$$= - \frac{0.5M}{(3.75K)} \pm 25 \times 10^{-3} = \pm 3.333 \text{ V for max. unipolar gain error and max. gain.} \quad (6\text{-}8)$$

Error amplifier is not going to saturate.

Device Types 02

If R_F = 500K and R_1 = 25K ± 25% (Init. Tol.)

E_o (max) = G1 (max) Unipolar gain error (max)

$$= - F\ 8.333 \text{ V for max unipolar gain error and max gain .} \quad (6\text{-}9)$$

Error amplifier is not going to saturate .

Machine error contribution to the latter measurements is less than 2% of the unipolar gain error (negligible).

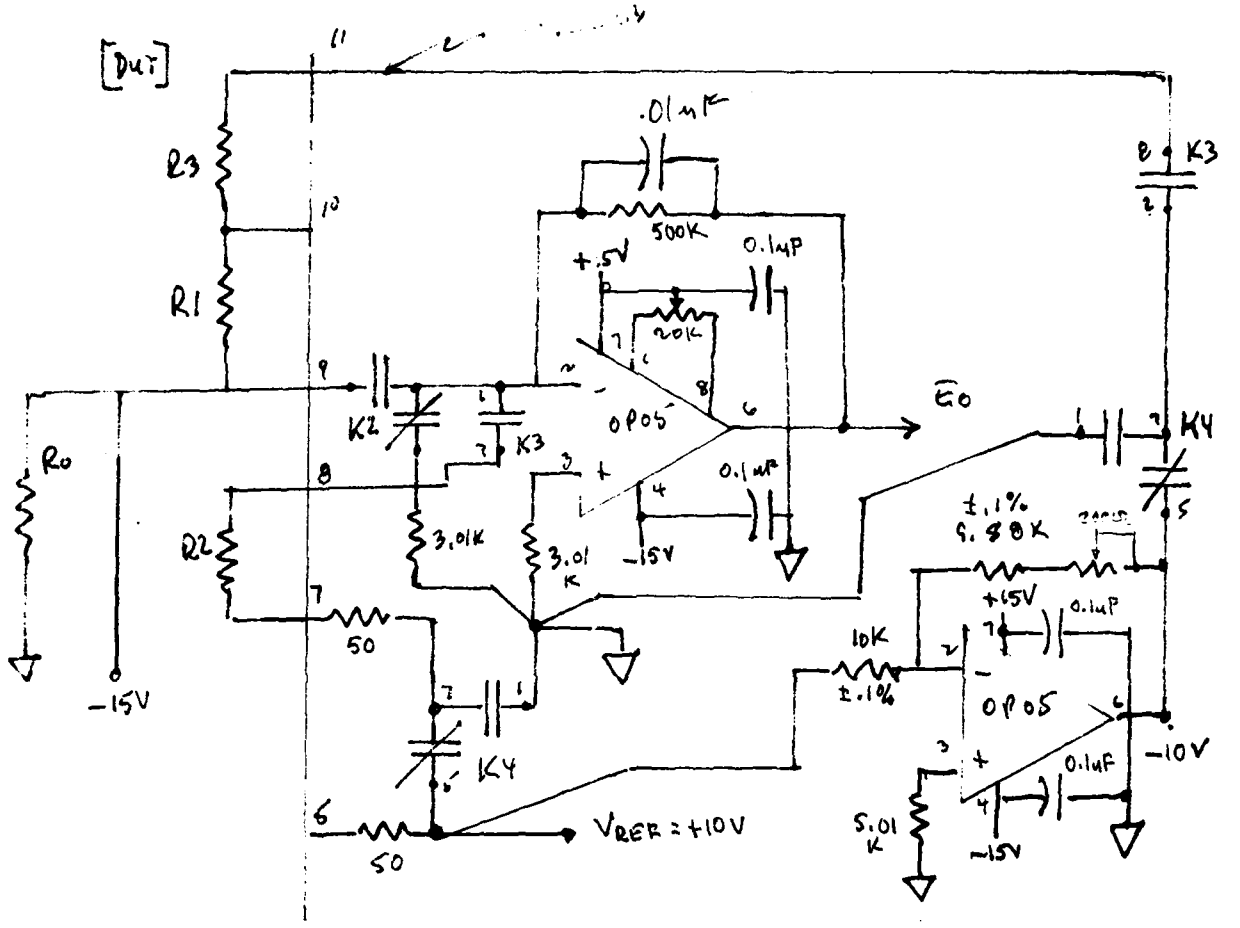
11. Gain Error (G_{ϵ}) in CMOS mode

This measurement is performed similar to (10), but with V_{cc} = + 15 VDC, V_{IH} = + 10.4 , and K6 energized.

12. Gain Error Drift $\left(\frac{G_{\epsilon}}{FSVR\ \Delta T}\right)$

The unipolar gain error drift is derived by measuring unipolar gain at the -55°C, + 25°C, and +125°C and calculating the average temperature coefficient for each excursion from +25°C separately. Namely, the temperature coefficient from + 25°C to -55°C and the temperature coefficient from + 25°C to + 125°C. The largest of the two measured values is displayed. Step 10 or 11 describes the method used for measuring unipolar gain for TTL or CMOS interfaces respectively.

13. Bipolar Offset Error, BPOE



BPOE test circuit.

BPOE, as specified in Table I is the DUT output offset voltage will all bits off, + 10 V ± .01% applied through 50 Ω to the bipolar offset resistor (DUT pin 7), and - 10 V ± .01% applied to the 20 V span resistor (DUT pin 11) with relays K2 and K3 energized. BPOE includes the effects of unipolar zero offset current.

Prior to proceeding with this test the following conditions must be met or adjustments made to bring the voltages into tolerance

V_{REF} = + 10.000 V ± .01%

$\overline{V_{REF}}$ = - 10.000 V ± .01%

E_o = 0 ± 5 mV with all relays deenergized. If not, trim offset adjust pot. For E_o = 0 ± 5 mV.

(a) Set all DUT address inputs to "0"s and all Ref DAC address inputs to "1"s. Energize K7, K2, K3, and K4 in that order (K6 also if in CMOS mode) and measure V_6 (adapter pin 21).

(b) Set Ref DAC address inputs to 1111 1111 0001 and measure V_7 (adapter pin 21)

$$G_2 = 1 - \frac{(V_7 - V_6)}{(\frac{10}{4096})\ 14} \qquad [6\text{-}10]$$

(c) De-energize K4 and energize K7 and measure V8 (adapter pin 21).

$$BPOE = \frac{V_8}{G_2}$$

14. BPOE Drift

Repeat 13 for temperatures within the range of -55 to + 125°C and calculate $\frac{\Delta BPOE}{\Delta T}$ measured values shall be equal to or less than the values specified in Table I.

15. Power Supply Sensitvity Full Scale Due to V_{cc} (TTL).

With the DUT in the unipolar mode, K1, K2, and K5 energized, V_{cc} = + 5.0 V, and V_{EE} = - 15 VDC power supply sensitivity is tested.

(a) Set all DUT address inputs to logic "1"s and all Ref DAC address inputs to logic "0"s (outputs on).

$$-\frac{E_o}{R_F/R_1} = V_{REF\ DAC}\ (FS) - I_o(FS)R_1 \text{ neglecting offsets}$$

$$\text{or } I_o(FS)R_1 - V_{REF\ DAC}\ (FS) = E_o\left(\frac{R_1}{R_F}\right) = \frac{E_o}{G1} \qquad [6\text{-}11]$$

Ideally $E_o \frac{(R_1)}{R_F} = 0$ and $V_{REF\ DAC}$ (FS) = + 9.9976 = V_{DUT}(FS)

Varying the positive supply voltage, V_{cc}, by ± 10% will cause E_o to vary by some ΔE_o.

$$+ PSS1^1 = \begin{array}{l}\text{change in DUT output} \\ \text{for ± 10\% change in} \\ V_{cc} \text{ with all bits on}\end{array} = \left| \frac{\Delta E_o}{G} \right| \text{ where in Table III}$$

$$\Delta E_o = V_{10} - V_9$$

$$= \left| \frac{V_{10} - V_9}{G} \right| \text{ or } \left| \frac{V_{10} - V_1}{G} \right| \quad [6\text{-}12]$$

The resulting values shall not exceed the limits specified in Table I.

(b) Set all DUT address inputs to logic "0"s and all REF DAC address inputs to logic "1"s (outputs off).

Varying the positive supply voltage, V_{cc}, by ± 10% will cause E_o to change by some amount, ΔE_o.

$$+ PSS1 = \left[\begin{array}{l}\text{change in DUT output} \\ \text{for 10\% change in } V_{cc} \\ \text{with all bits off.}\end{array} \right] = \left| \frac{\Delta E_o}{G} \right| = \left| \frac{V_{13} - V_{12}}{G} \right|$$

$$\text{or} = \left| \frac{V_{13} - V_{14}}{G} \right| \quad [6\text{-}13]$$

The largest resulting value shall not exceed the limits specified in Table I.

The largest of the two errors (+ PSS1' or + PSS1") will be printed out and the conditions along with it. (V_{cc} & address)

16. Power Supply Sensitivity at Full Scale Due to V_{cc} (CMOS)

With the DUT in the Unipolar Mode, K1, K2, K5, and K6 energized, V_{cc} = + 15 V and V_{EE} = - 15 VDC power supply sensitivity is tested. Procedure is same as in 15, but with V_{cc} varied ± 10%.

17. Power Supply Sensitivity at Full Scale Due to V_{EE} (CMOS)

With the DUT in the Unipolar Mode, K1, K2, K5, and K6, energized, V_{cc} = + 15 V, and V_{EE} = - 15 VDC power supply sensitivity is tested. Procedure is same as 15, but with V_{EE} varied ± 10%.

18. Linearity

Some manufacturers use bit weight errors to determine the maximum positive and negative linearity errors with respect to a straight line between zero and full scale outputs. This method is valid for testing linearity if there is no appreciable bit interaction, thermal or other. Excessive bit interaction is apt to result in bit weight errors that are all in one direction. The maximum error would then seemingly occur at DUT input address of all ones. However, the DUT errors are calibrated to zero at full scale so the technique is not valid.

At this point in the test program development it appears that a vendor whose devices exhibit appreciable bit interaction would be required to test all 4095 outputs. The answer to this question and others will be a result of the characterization study.

As a part of this characterization the bit weight errors and corresponding linearity will be measured repetitively starting from initial turn on to acquire some data on the effects of thermal interaction on linearity measurement accuracy.

Linearity will also be measured for all 4095 codes after suitable warm up. A number of measurements will be made to check for repeatability.

1) Abbreviated Linearity Test Using Bit Weight Errors

Measure E_o and store for each of the following digital address inputs with same address applied to DUT and Reference Module:

1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	0	0	0	1	0	0
0	0	0	0	0	0	0	0	0	1	1	1
0	0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	0	0	1	1	1	1
0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	1	1	1	1	1
0	0	0	0	0	0	1	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	1	1
0	0	0	0	0	1	0	0	0	0	0	0
0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	0	1	0	0	0	0	0	0	0
0	0	0	0	1	1	1	1	1	1	1	1
0	0	0	1	0	0	0	0	0	0	0	0
0	0	0	1	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	1	1	1	1	1
0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	0

Establish a straight line with zero and full scale measured values. Calculate bit weight errors and derive addresses for both maximum positive bit weight error and maximum negative bit weight error.

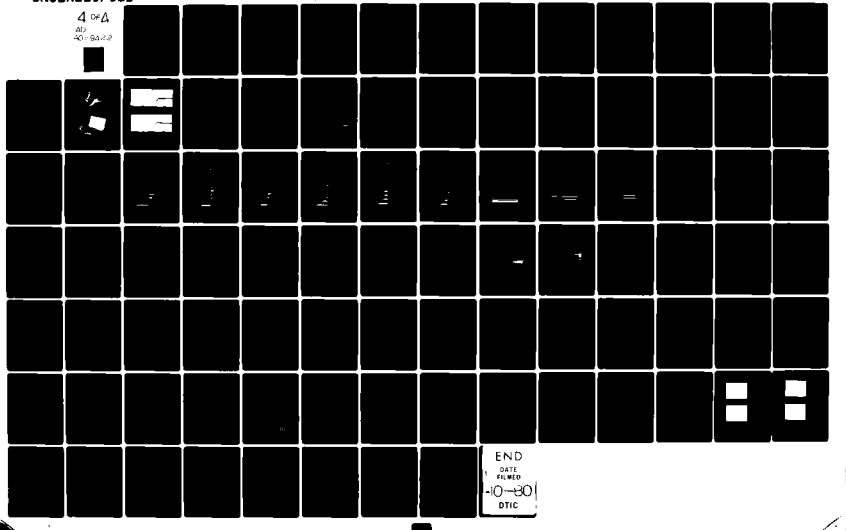
All measured outputs for the above listed input addresses shall be linear to within ± 1/2 LSB.

Apply the address for maximum positive bit errors and output shall be linear to within 1/2 LSB.

Apply the address for maximum negative bit errors and output shall be linear to within 1/2 LSB.

Subtract Pos. BWE from Neg. BWE store and record. Major Carry Errors (MCE) shall be less than ± 0.9 LSB (-55 to + 125°C).

AD-A089 422 GENERAL ELECTRIC CO PITTSFIELD MA ORDNANCE SYSTEMS F/G 9/5
ELECTRICAL CHARACTERIZATION OF SPECIAL PURPOSE LINEAR MICROCIRC--ETC(U)
MAY 80 J S KULPINSKI, T SIMONSEN, L CARROZZA F30602-78-C-0195
UNCLASSIFIED RADC-TR-80-49 NL



6.4.2 Monotonicity

One of the most important parameters of a D/A converter, if not the most important, is monotonicity. A D/A converter is monotonic if, for an increasing address (eg 0 - 4095), the output voltage/current continuously increases (or decreases if logic is complementary) and if, for a decreasing address eg (4095 - 0), the output voltage/current continuously decreases (or increases if logic is complementary).

The manufacturers recommending the abbreviated test method measure differential nonlinearity and claim that monotonicity is assured if the differential nonlinearity is $\leq \pm$ 1 LSB. eg D.N.L. $\leq \frac{\Delta E - LSB_N}{LSB_N}$

where LSB_N is normalized LSB.

and ΔE is the value $E_{o(n)} - E_{o(n-1)}$

and $0 \leq n \leq 4095$.

Part of the characterization task will be to examine the validity of testing monotonicity via major carries.

Monotonicity will be tested by the following sequence:

(a) Set. Ref. module and DUT addresses to all 0's and measure the error amplifier output voltage, $E_{o(0)}$.

(b) Increment DUT address by one count and measure the error amplifier output voltage, $E_{o(0)}{}^{1}$. $E_{o(0)} - E_{o(0)}{}^{1}$ must be greater than 0 V.

(c) Increment Ref. Module address by one count and measure $E_{o(1)}$. Then increment DUT address by one count and measure $E_{o(1)}{}^{1}$. $E_{o(1)} - E_{o(1)}{}^{1}$ must be greater than 0 V.

(d) Repeat for all 4095 addresses. If for all addresses $E_{o(n)} - E_{o(n)}{}^{1} \geq 0$. The D/A converter (DUT) is monotonic.

NOTE: Linearity can also be measured at the same time without utilizing much memory.

Linearity - (All addresses)

Linearity can be measured along with monotonicity by first measuring the zero and full scale error voltages $E_{o(0)}$ and $E_{o(4095)}$, to establish a straight line and then measuring error voltages for all addresses in between relative to the straight line. Only max positive

and max negative deviations and respective addresses need be stored. However, for the purposes of characterization, the bit weight errors will be stored for comparison to BWEs measured in the abbreviated linearity test. After measuring linearity of all codes, repeat $E_o(4095)$ and $E_o(0)$. If $E_o(4095) - E_o(0)$ differs from the earlier measured values by $\pm$ .05 LSB, repeat the sequence. If the latter condition is not met after two passes, stop the test, and indicate that DUT outputs are not stabilizing.

Appendix "A"

Linearity Equations

V_{REF} (m) = Ref. D/A output voltage at address "M".

E_o (m) = Amplified difference voltage. Difference between Ref D/A and DUT output which includes offset voltage.

E_o (0) = Amplified offset voltage which includes contributions from Ref D/A, DUT, and difference amplifier.

V_{OI} (m) = DUT output voltage on ideal straight line between zero and full scale for address "M". (referred to error amp. input)

V_{OM} (m) = Measured DUT output voltage for address "M". (referred to error amp. input)

and V_o (DUT) = I_o (DUT) R_1 (referred to error amp. input)

$$E_o\ (m) = I_o\ (m)\ R_1 + V_{REF}\ (m)\ G1$$

$$V_{REF}\ (m) = \left(\frac{V_{REF}\ (FS) - V_{REF}\ (o)}{4095}\right) n + V_{REF}\ (o)$$

$$(V_{REF}\ (n) + I_o\ (n)\ R_1)\ \ G1 = E_o\ (n)$$

$$V_{OM}\ (m)1 = I_o\ (n)\ R_1 = \frac{E_o\ (n)}{G1} - V_{REF}\ (n)$$

$$V_{OI}\ (n) = \left(\frac{V_{OM}\ (FS) - V_{OM}\ (o)}{4095}\right) n + V_{OM}\ (o)$$

$$\text{Linearity Error} = V_{OM}\ (n) - V_{OI}\ (m)$$

where n is any address from 0 - 4095 and FS is 4095

6.5 Evaluation of Data

6.5.1 Dynamic Test Data

Settling time data was measured on 13 devices (Device Type 01) and the resulting data is listed in Table 6.2. Photographs were also taken and a typical set for a given device are shown in Figure 6.7. Settling time ranged from 400 to 600 nsec. The six devices supplied by Vendor "13" to GEOS with data (S/N, 4310 - 4315) exhibited settling times that were significantly less than the other devices tested, approximately 400 nsec settling time compared to 600 nsecs for the others. For all devices the "on to off" settling times were appreciably less than the "off to on" settling times, as much as 45% less for the slower devices and 30% less for the faster ones.

In the expanded photos shown in Fig. 6.7 there is some high frequency ac (damped) riding on the envelope of the signal. This ac is almost certainly a contribution from the test circuit, probably due to layout and wiring. The test circuit and the oscilloscope (plus preamplifier) employed appears to be adequate for testing device types 01. A sampling type preamplifier might be required to test device type 02s because of the lower settling times.

6.5.2 Static Test Data

Power Supply Currents

The supply current limits for the 562 appear to be adequate. I_{CC} seems to run towards the high side of the limits but it doesn't seem to change much from device to device.

Logic Input Currents

Devices tested seem to fall well within the limits specified. I_{IH} seems to increase randomly from one device to another at -55°C and occasionally over-ranges. This problem is almost certainly due to some slight condensation on the bottom of the DUT connector. Currents measured are low nano-amperes and should decrease at -55°C. Repeat tests on a sampling of devices has shown that it is not a device problem.

Logic "0" input currents (I_{IL}) all measured well below the specified limits. Measured values were in the low nano-amperes range while specified limits are + 1 to - 200 uA.

Full Scale Current

Devices tested seemed to fall well within the limits specified. Limits specified are adquate.

Zero Scale Current

All devices passed these tests comfortably. Limits are reasonable.

Zero Current Drift

All devices passed these tests by good margins. Adequately specified limits.

Bipolar Offset Current

All devices passed this test with wide margins. This test is largely a measure of the bipolar offset resistor. If full scale output current is below nominal this resistor value will measure above nominal by almost the same amount. Although not tested directly the span resistor values will track the bipolar offset resistor values. It is because of this relationship between the resistance values and the F.S. output current value that the gain error is so low in spite of a ± 25% tolerance on full scale output current.

Gain Error

All devices pass these tests with comfortable margins. Limits are adequate.

Gain Error Drift

Four devices failed this test over the range + 25 to - 55°C and six others came quite close to the limit. A couple of devices that failed measured slightly more than twice the limit specified. It should be noted that the maximum average temperature coefficient tabulated is not the average over the full temperature range but the worst case of the two averages over the temperature ranges of + 25 to + 125°C and + 25 to - 55°C. Averaging over the full operating temperature range would probably make the devices look better and some might even pass.

Bipolar Offset Error

All devices passed this test and it appears that this parameter is conservatively specified. It should be noted that the manufacturer sets the bipolar offset resistance 50 ohms low to allow for the insertion of a 100Ω potentiometer in series with the resistor to adjust bipolar offset error to zero if so desired. A 50Ω resistor was inserted in series with the bipolar offset resistor for this test to achieve nominal value.

Bipolar Offset Drift

All devices passed this test, most by a comfortable margin, but from + 25°C to - 55°C. A couple of devices came to within approximately 50% of the specified limit.

Power Supply Sensitivity

Power supply sensitivity was tested for CMOS and TTL operation with all bits on and with all bits off. CMOS power supply sensitivities were tested at V_{cc} = + 5 V and V_{cc} = + 15 V. Measured values of output voltage variation were in no case greater than ± 100 uV with ± 10% supply voltage variations. This parameter appears to be ultra conservatively specified, especially for V_{EE}. It would appear that a ± 500 uV limit for all supplies would suffice over the full operating temperature range.

Bit Weight Errors

All devices tested passed the Bit Weight Errors (BWE) tests. BWEs were generally quite low at + 25°C. At + 125°C BWE degraded slightly but the most significant changes occurred at -55°C. It appears that the manufacturers do their screening at + 25°C and select devices with low bit errors to allow a safe margin for variation at -55°C. Figures 6.8 - 6.10 and Figures 6.14 - 6.16 illustrate this feature.

It is interesting to note that there seems to be a recurring pattern to the Bit Weight Errors and Major Carry Errors, as shown in Figures 6.8 - 6.13. The current switches in this device are identical quads with scaling resistors at the outputs of the two lower order quads. The recurring pattern seems to reflect scaling resistor errors and drifts.

The Bit Weight Errors measured in the "Abbreviated Linearity Test" correlated quite well with the Bit Weight Errors extracted during the extended linearity test. Some of the differences noted, however small, were probably related to temperature stabilization time, especially at - 55°C. Bit Weight Errors and Major Carry Errors for both the abbreviated and extended linearity tests are displayed side by side for comparison.

Summation Bit Weight Errors

The accuracy of the summation of (+) Bit Weight Errors and the summation of (-) Bit Weight Errors in defining the worst case positive and negative linearity errors respectively is dependent upon how much interactive error is present in the device. The devices

tested exhibited very little interactive error, as demonstrated by the low values of $\sum$ (+) NL + $\sum$ (-) NL. Typically the values were $\angle \pm$ .05 LSB. Confirmation of the low interactive errors was achieved by the close correlation of the Extended Linearity Test data with the Abbreviated Linearity Test data. In the extended test all codes were tested and the addresses of the maximum positive and maximum negative linearity errors were recorded. Although the addresses of the maximum positive error and the maximum negative error were not always exact complements, the $\sum$ (+) NL + $\sum$ (-) NL were always within 0.1 LSB. The smaller the bit errors the more unpredictable the addresses will be. Better correlation would be achieved if all bits with measured bit weight errors of $\angle \pm$ .05 LSB were weighted as logic "0"s. Figures 6.8 - 6.10 illustrate Bit Weight errors for abbreviated and the extended tests and the addresses of the worst case positive and negative linearity errors for each test are tabulated below the graph. Extended Linearity test data is not listed in Table III. It only shows up in the data plots for comparison purposes.

Major Carry Errors

Major Carry Errors were generally well within the specified limits of ± 0.9 LSB in the abbreviated test. Although monotonicity is tested accurately for all codes in the extended tests, major carry errors were extracted from the extended test data for comparison to the abbreviated test data. Comparisons were good as shown in typical device MCE graphs in Figures 6.11 - 6.13.

6.6 Conclusions and Recommendations

The characterization of the 562 was successful in accomplishing all of its primary objectives. Although only one Device Type (01) made by only one vendor was characterized, its performance over the full military operating temperature range was evaluated and it performed well. Twelve devices doesn't constitute a large sample but it's enough to indicate potentially sensitive parameters. The only parameter that appeared to be marginal was gain error drift with temperature. 5 ppw/°C is not large enough. The limits should be increased to 10 ppw/°C at the least. Generally, parameter tolerances tended to be conservative. Logic "0" Input Current appears to be much too loosely specified. None of the values measured were in excess of ± 20 nA, yet the specified limits are + 1 ⟶ - 200 mA. It is recommended that the limits be reduced to + 1 ⟶ - 200 nA. Another parameter that appeared to be much too conservatively specified was Power Supply Sensitivity. Generally, the output variations in response to ± 10% power supply variations were less than ± 100 mV and in no case did they exceed ± 200 uV over the full operating temperature range. Also, the sensitivity to the negative power supply was no worse than to the positive. It is recommended, therefore, that one limit be applied to both the positive and negative power supplies over the full temperature range, ± 800 uV. Linearity was good and superposition (interactive) errors were extremely low, $<$ ± .05 LSB. The device tested is an excellent candidate for performing "Abbreviated Linearity Testing" since the device is linear and superposition applies. A device that is not linear and exhibits interactive errors that should be compelled to perform "All Codes Linearity Testing," unfortunately devices of this nature were not available for characterization. Nevertheless, anticipating that such devices will eventually be tested, the following recommendations are offered:

1. Devices that exhibit low interactive errors ($\Sigma + NL + \Sigma - NL \leq 0.1$ LSB) be permitted to perform "Abbreviated Linearity Tests" while those that do not must perform all codes testing.

2. The device slash sheets be modified to include at least one and possibly two more interactive error tests at half scale and three quarters full scale. e.g.

   0111 1111 1111 + 1000 0000 0000 0.1 LSB and

   0100 0000 0000 + 1011 1111 1111 0.1 LSB

   Without the inclusion of one or both of the latter tests a device with interactive errors in excess of ± 0.1 LSB but whose bit weight errors each are $<$ 0.5 LSB could pass the "Abbreviated Linearity Test". If all bit errors are negative the address of Σ - NL would

be all 1s and the address of Σ + NL would be all 0's. Both of the latter addresses are calibration points on the ideal linearity curve so Σ + NL + Σ - NL = 0.

Some vendors have suggested walking a zero through the test pattern but that is not as effective as the proposed two tests. Addition of the walking zero codes, if implemented, should be in addition to the proposed test addition.

Another recommendation pertaining to guaranteed monotonicity is to apply a ± 0.9 LSB limit to Major Carry Errors in the "Abbreviated Linearity Test" to allow for measurement error and interactive errors, however slight, that could make a marginally non-monotonic device appear to be monotonic or vice versa. Failure to meet this requirement would not necessarily constitute a device failure. If MCE is in the range of $0.9\ LSB \leq MCE \leq 1.1\ LSB$ the device must be subjected to "All Codes Linearity Test" in which monotonicity is more accurately tested for all codes. Inability to pass this test would constitute a failure.

Settling time measurements appeared to be valid but without the manufacturer's test data the results could not be correlated. Results appear to be significantly better than manufacturers indicated they would be.

Another objective of the 562 characterization effort was the development of automatic test capability for testing the device on a Tektronix S3260. This was made possible by the use of a Reference Module which contains an 18 Bit Reference DAC, buffers, and active ground drivers. A Fluke 8500A (5 1/2 Digit DVM) was employed via IEEE bus simply to calibrate the test setup at the start of testing. Once calibration is done it is not repeated for subsequent DUT testing. The accuracy of the tester is excellent and so was correlation with manufacturer's 25°C test data on devices S/Ns 4310 - 4315. Correlation was within ± .05 LSB.

Table 6.1 Electrical Performance Characteristics

Characteristics	Symbol	Conditions:	Device 01 limits Min	01 limits Max	02 limits Min	02 limits Max	Units
Supply Current from Vcc	Icc	All input bits logic "1"	3	18	3	18	mA
Supply Current from Vee	Iee	All input bits logic "1"	-25	-5	-40	-5	mA
Logic "1" Input Current	I_{IH}	V_{in} (Logic "1") = + 15 V, Each input measured separately	- 1	+100	- 1	+100	µA
Logic "0" Input Current	I_{IL}	V_{in} (Logic "0") = 0 V, Each input measured separately	-200	+1	-200	+1	µA
Full Scale Current	I_{FS}	All inputs logic "1" [1] V_o = 0 V	-2.5	-1.5	-6	-4	mA
Zero Scale Current (TTL)	I_{ZS1}	All inputs logic "0" V_o = 0 V, Vcc = + 5 V, T_A = +25°C	-.05	+.05	-.05	+.05	% FS Current
Zero Scale Current (CMOS)	I_{ZS2}	All inputs logic "0" V_o = 0 V, Vcc = +15 V, T_A = +25°C	-.05	+.05	-.05	+.05	% FS Current
Zero Scale Drift	$\Delta I_{ZS}/\Delta T$	All inputs logic "0" Vcc = + 15 V	-2	+2	-2	+2	PPM I_{FS}/C°
Bipolar Offset Current	I_{BIP}		0.75	1.25	2	3	mA
Gain Error (TTL)	V_{FSI1}	All inputs logic "1" $V_{FSI} = V_o$ - 9.99756 Vcc = + 5 V, T_A = + 25°C	-25	+25	-25	+25	mV
Gain Error (CMOS)	V_{FSI2}	All inputs logic "1" $V_{FSI} = V_o$ - 9.99756 Vcc = + 15 V T_A = + 25°C	-25	+25	-25	+25	mV
Gain Error Drift	$\Delta V_{FSI}/\Delta T$	All inputs logic "1" Vcc =	-5	+5	-5	+5	PPM V_{FS}/C°
Bipolar Offset Error	BPOE	Bit 1 = logic "1" Bits 2 - 12 = logic "0" Measure V_o - 0 V T_A = + 25°C	-20	+20	-20	+20	mV
Bipolar Offset Error Drift	Δ BPOE	All inputs logic "0" Measure ΔV_o	-4	+4	-4	+4	PPM V_{FS}/C°
Power Supply Sensitivity At Full Scale From Vcc (TTL)	+PSS1	Vcc = + 5 V ± 0.5 V [2] T_A = +25°C.	-800	+800	-800	+800	µV
		T_A = - 55 to + 125°C	-1.6	+1.6	-1.6	+1.6	mV
Power Supply Sensitivity At Full Scale From Vcc (CMOS)	+PSS2	Vcc = + 15 V ± 1.5 V [2] T_A = + 25°C	-800	+800	-800	+800	µV
		T_A = - 55 to + 125°C	-1.6	+1.6	-1.6	+1.6	mV

Table 6.1 Electrical Performance Characteristics

Characteristics	Symbol	Conditions: See Note 3	Device 01 limits Min	Max	Device 02 limits Min	Max	Units
Power Supply Sensitivity At Full Scale From V_{EE}	-PSS1	V_{EE} = - 15 V ± 1.5 V [2] All inputs logic "1" T_A = + 25°C	-1.6	+1.6	-1.6	+1.6	mV
		T_A = - 55 to + 125°C	-3.2	+3.2	-3.2	+3.2	mV
Bit Errors	B1 - B12	Turn on 1 bit at a time and measure [2] V_o relative to REF. DAC output. T_A = - 55 to + 125°C	-1.22	+1.22	-1.22	+1.22	mV
Summation of Positive Bit Weight Errors	$\sum$(+) BWE	Turn on all bits with Positive bit [2] errors and measure V_o relative to REF. DAC T_A = - 55 to + 125°C	-1.22	+1.22	-1.22	+1.22	mV
Summation of Negative Bit Weight Errors	$\sum$(-) BWE	Turn on all bits with Negative bit [2] errors and measure V_o relative to REF. DAC T_A = - 55 to + 125°C	-1.22	+1.22	-1.22	+1.22	mV
Major Carry Errors	MC1 - MC11	4000 - 3777 (Octal) to 2 - 1 [2] T_A = - 55 to + 125°C	-2.2	+2.2	-2.2	+2.2	mV
Output Current Settling Time 0 to FS	t_{SLH}	All inputs switched simultaneously. Time to settle to within 1/2 LSB of final value	-	1	-	0.4	µsec
Output Current Settling Time FS to 0	t_{SHL}	All inputs switched simultaneously. Time to settle to within 1/2 LSB of final value	-	1	-	0.4	µsec
Bit Interaction	(+) BWE + (-) BWE		-0.25	+0.25	-0.25	+0.25	mV

Notes:

1. The compliance voltage range varies from one vendor to another. Devices with a finite output resistance will draw additional current proportional to compliance voltage. eg. If R_o = 6 K Ω and compliance voltage equals + 1 V the output current will increase by 0.167 mA. This current is a fixed offset current. This device is not a multiplying DAC.

2. This test is performed in the unipolar mode over a 0 to + 10 V range. One LSB is 2.44 mV.

3. The operating temperature range is - 55 to 125°C unless otherwise stated.
   Vcc = + 15 ± .15 V
   V_{EE} = - 15 ± .15 V

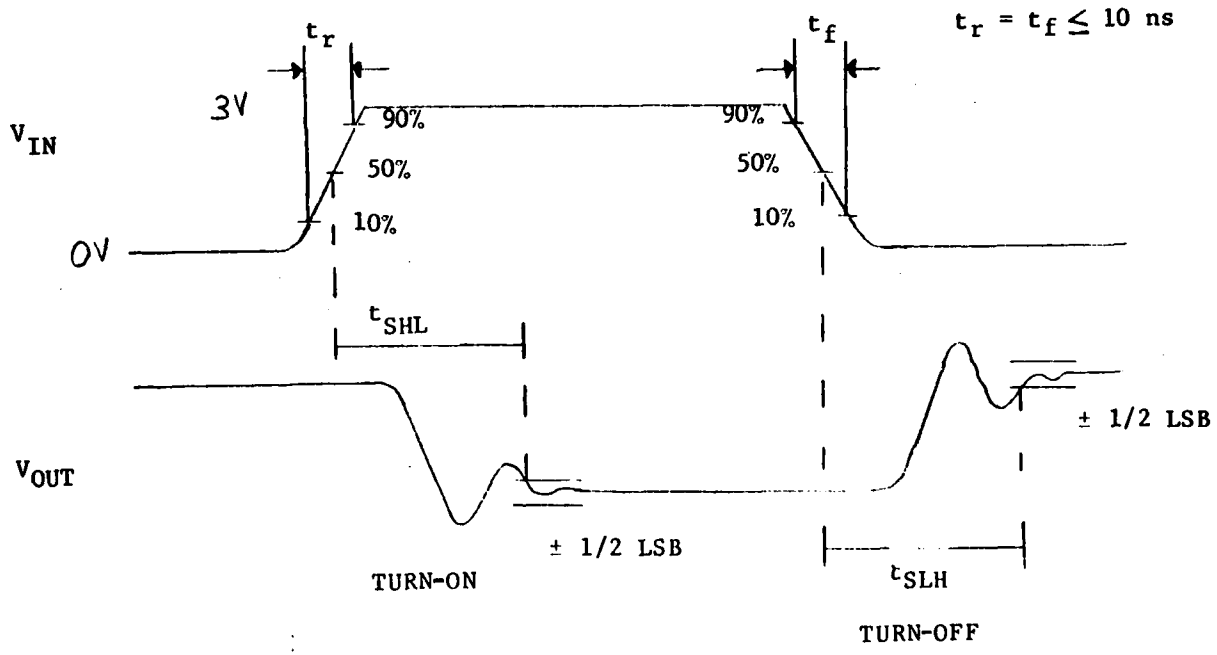
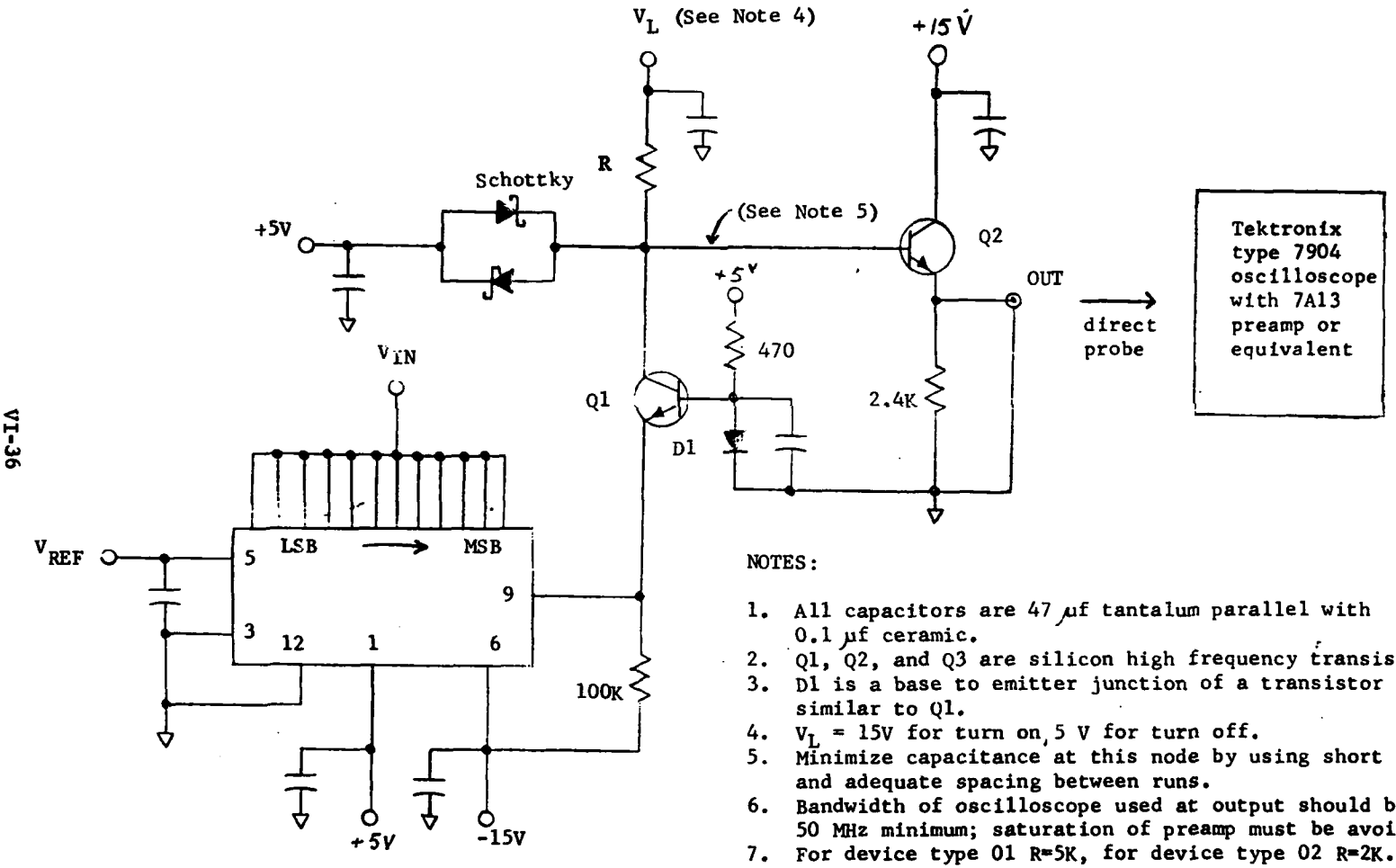


Figure 6.3. Waveforms For Settling Time, Device Types 01 and 02.



NOTES:

1. All capacitors are 47 μf tantalum parallel with 0.1 μf ceramic.
2. Q1, Q2, and Q3 are silicon high frequency transistors.
3. D1 is a base to emitter junction of a transistor similar to Q1.
4. V_L = 15V for turn on, 5 V for turn off.
5. Minimize capacitance at this node by using short runs and adequate spacing between runs.
6. Bandwidth of oscilloscope used at output should be 50 MHz minimum; saturation of preamp must be avoided.
7. For device type 01 R=5K, for device type 02 R=2K.

Figure 6.4. Test Circuit For Settling Time, Device Types 01 and 02.

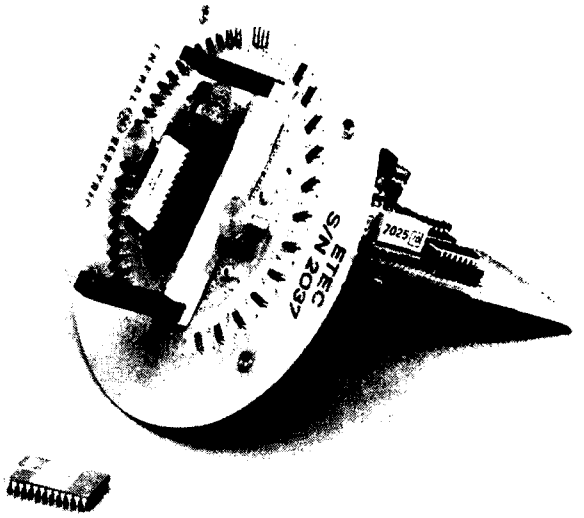


Figure 6.5. S3260 test adapter for the 562, D/A Converter.

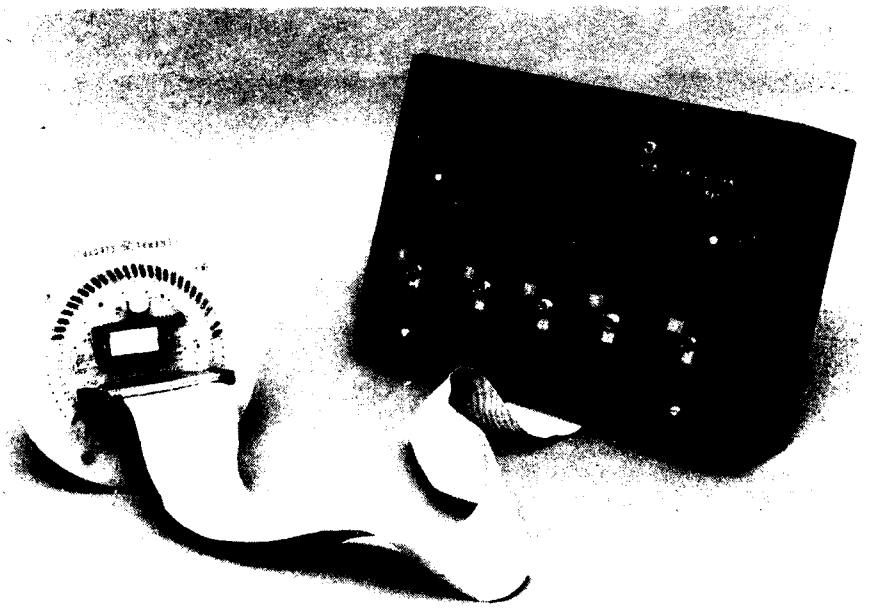
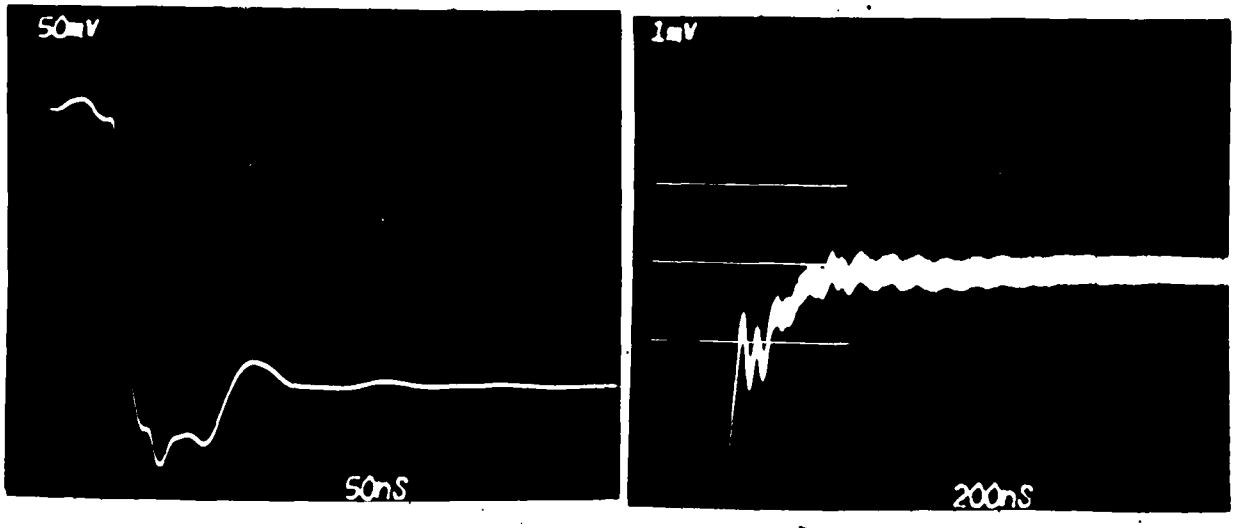
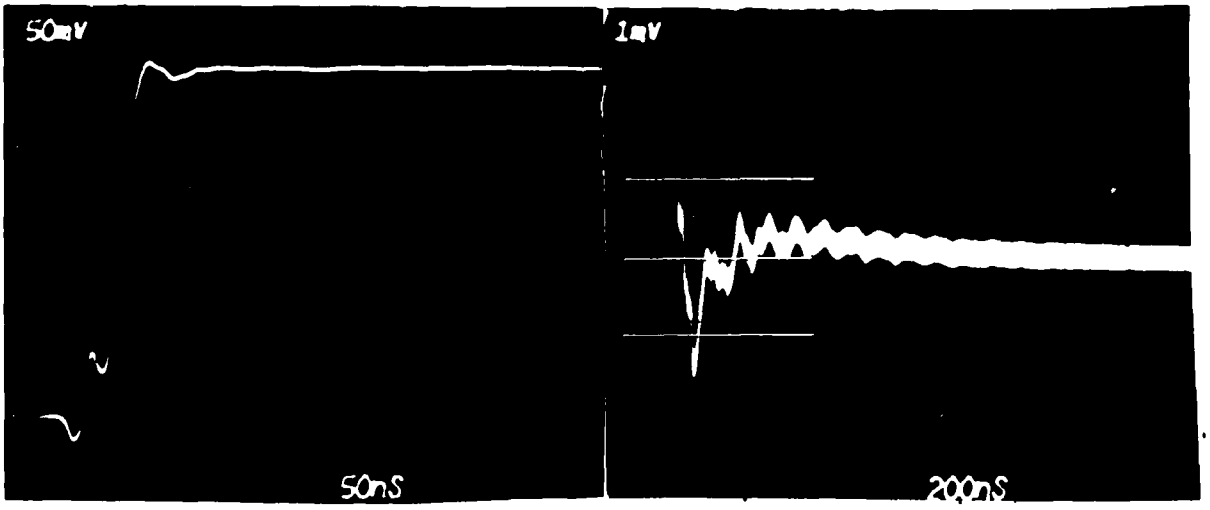


Figure 6.6. Reference module connected to the S3260 test adapter.



0-1 Transition Overall
(a)

0-1 Transition Expanded
(b)



1-0 Transition Overall
(c)

1-0 Transition Expanded
(d)

Figure 6.7. Settling time waveforms (typical device type 01).

TABLE 6.2. Output Settling Time Data

Device Type 01

Serial Number of Device	All Bits Off to All Bits On	All Bits On to All Bits Off
00005	500 ns	260 ns
00019	480 ns	300 ns
00020	500 ns	260 ns
00021	480 ns	260 ns
00025	480 ns	220 ns
00035	480 ns	360 ns
00048	480 ns	245 ns
04310	400 ns	290 ns
04311	370 ns	240 ns
04312	360 ns	240 ns
04313	370 ns	245 ns
04314	380 ns	245 ns
04315	400 ns	240 ns

TABLE 6.3. Device Type 01 Data at + 25°C.

MANUFACTURER CODE: ; DEVICE TYPE: 883; TEMPERATURE: 25 DEG C ; 25 OCT 79 10:58:02

PARAMETER	LO-LIM	4310	4312	4313	4314	4315	5	19	20	21	25	HI-LIM	UNITS
ICC-SUPPLY CURRENT	3.00	11.8	12.3	12.0	11.8	11.8	12.3	12.3	13.9	13.1	13.7	18.0	MA
IEE-SUPPLY CURRENT	-25.0	-15.5	-16.3	-15.8	-15.6	-15.7	-17.3	-16.9	-17.8	-17.3	-18.3	-6.00	MA
IIH FOR BIT# 1	-1.00	2.00	1.95	2.40	1.95	1.90	1.80	2.05	2.10	1.95	1.95	100.	NA
IIH FOR BIT# 2	-1.00	1.65	1.80	1.95	2.10	1.75	1.70	1.65	1.75	1.80	1.90	100.	NA
IIH FOR BIT# 3	-1.00	1.85	2.20	1.80	1.65	1.90	1.95	2.00	1.95	1.85	1.95	100.	NA
IIH FOR BIT# 4	-1.00	1.90	2.05	1.95	1.85	1.80	1.95	1.80	2.05	1.70	1.90	100.	NA
IIH FOR BIT# 5	-1.00	1.95	2.25	2.10	2.05	1.75	1.90	1.95	2.20	2.05	1.95	100.	NA
IIH FOR BIT# 6	-1.00	1.80	2.20	1.85	2.05	2.05	1.95	1.65	1.85	1.60	1.95	100.	NA
IIH FOR BIT# 7	-1.00	2.05	2.40	1.90	1.80	2.20	2.20	1.95	1.95	1.95	1.95	100.	NA
IIH FOR BIT# 8	-1.00	1.95	2.15	2.25	1.90	1.90	2.20	1.90	2.10	1.90	2.00	100.	NA
IIH FOR BIT# 9	-1.00	2.35	2.45	2.35	2.30	2.15	2.20	2.30	2.20	2.35	2.20	100.	NA
IIH FOR BIT# 10	-1.00	2.35	2.40	2.30	2.25	2.45	2.40	1.95	2.20	1.90	2.40	100.	NA
IIH FOR BIT# 11	-1.00	2.55	2.40	2.55	2.60	2.55	2.65	2.50	2.35	2.35	2.75	100.	NA
IIH FOR BIT# 12	-1.00	3.80	4.00	3.70	3.55	3.40	3.55	3.60	3.75	3.50	3.60	100.	NA
IIL FOR BIT# 1	-200.	-8.40	-9.10	-8.65	-8.85	-8.55	-9.35	-8.45	-8.70	-10.8	-10.6	1.00	UA
IIL FOR BIT# 2	-200.	-8.60	-8.95	-8.80	-9.80	-8.80	-9.55	-9.05	-7.30	-9.70	-10.2	1.00	UA
IIL FOR BIT# 3	-200.	-8.45	-8.85	-8.65	-8.75	-8.55	-11.3	-8.55	-7.20	-9.55	-10.2	1.00	UA
IIL FOR BIT# 4	-200.	-8.50	-8.75	-8.75	-8.70	-8.70	-8.75	-8.25	-7.15	-9.45	-10.3	1.00	UA
IIL FOR BIT# 5	-200.	-8.30	-8.80	-8.55	-8.60	-8.80	-11.4	-8.85	-7.10	-9.35	-10.0	1.00	UA
IIL FOR BIT# 6	-200.	-8.35	-8.80	-8.70	-8.50	-8.75	-10.1	-13.6	-7.05	-9.40	-9.95	1.00	UA
IIL FOR BIT# 7	-200.	-8.30	-8.75	-8.60	-8.55	-8.65	-8.70	-9.15	-6.95	-9.25	-9.70	1.00	UA
IIL FOR BIT# 8	-200.	-8.25	-8.55	-8.60	-8.50	-8.70	-14.0	-9.60	-7.20	-9.30	-9.70	1.00	UA
IIL FOR BIT# 9	-200.	-8.05	-8.75	-8.55	-8.55	-8.55	-9.55	-9.05	-7.05	-8.95	-9.50	1.00	UA
IIL FOR BIT# 10	-200.	-8.25	-9.50	-8.65	-8.45	-8.55	-8.60	-9.05	-6.75	-9.05	-9.35	1.00	UA
IIL FOR BIT# 11	-200.	-7.95	-9.65	-8.45	-8.45	-8.65	-8.55	-8.80	-6.65	-8.95	-14.5	1.00	UA
IIL FOR BIT# 12	-200.	-7.95	-8.65	-8.45	-8.50	-8.55	-9.10	-8.70	-6.75	-9.00	-15.1	1.00	UA
FULL SCALE CURR.-TTL	1.50	1.93	1.94	1.92	1.93	1.91	2.28	2.17	1.94	2.01	2.20	2.50	MA
FULL SCALE CURR.-CMOS	1.50	1.93	1.94	1.93	1.93	1.93	2.29	2.18	1.94	2.00	2.20	2.50	MA
ZERO SCALE CURR.-TTL	-1.00K	-58.0	-23.5	-38.0	-31.5	-41.0	-72.0	-108.	-97.5	-95.0	5.00	1.00K	NA
ZERO SCALE CURR.-CMOS	-1.00K	-72.0	-60.5	-68.5	-38.5	-85.0	-114.	-122.	-123.	-100.	-54.0	1.00K	NA
IOZ-DRIFT	-2.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	2.00	PPM/C
BIPOLAR OFFSET CURR.	750.M	975.M	975.M	965.M	970.M	960.M	1.14	1.09	970.M	1.01	1.10	1.25	MA
+PSS2 (CMOS) [+10%]	-800.	-31.0	-66.6	0.00	-15.4	26.0	-78.6	-22.9	10.3	-29.7	-77.0	800.	UV
+PSS2 (CMOS) [-10%]	-800.	-87.8	-71.8	-31.2	-36.0	-67.5	52.4	-13.8	-61.7	-19.8	-4.53	800.	UV
-PSS1 (TTL) [+10%]	-1.60K	-82.7	-15.4	5.21	-10.3	-5.19	0.00	-27.5	-5.14	-24.8	-77.0	1.60K	UV
-PSS1 (TTL) [-10%]	-1.60K	62.0	35.9	80.8	20.6	15.6	-8.74	55.0	0.00	29.7	81.6	1.60K	UV
BIT WGHT ERR-BIT# 1	-500.M	-20.7M	-1.56M	4.30M	-48.5M	26.6M	-13.5M	-6.05M	205.M	252.M	-67.9M	500.M	LSB
BIT WGHT ERR-BIT# 2	-500.M	37.0M	11.5M	49.7M	43.4M	46.5M	73.9M	49.6M	-27.9M	48.9M	66.2M	500.M	LSB
BIT WGHT ERR-BIT# 3	-500.M	-56.7M	-49.9M	-40.8M	-28.3M	-82.7M	102.M	48.6M	-68.2M	97.6U	77.6M	500.M	LSB
BIT WGHT ERR-BIT# 4	-500.M	6.94M	1.34M	81.5M	1.61M	-31.4M	-84.9M	-43.4M	-83.8M	-37.5M	-6.71M	500.M	LSB
BIT WGHT ERR-BIT# 5	-500.M	37.3M	-49.7M	36.4M	96.6M	18.4M	-63.6M	87.1M	-7.70M	-85.7M	41.7M	500.M	LSB
BIT WGHT ERR-BIT# 6	-500.M	-6.68M	-37.5M	-63.3M	-18.8M	-8.37M	-90.3M	-7.11M	-16.5M	-44.9M	-14.4M	500.M	LSB
BIT WGHT ERR-BIT# 7	-500.M	-8.13M	10.7M	-18.1M	48.3M	15.0M	-38.0M	-5.43M	8.60M	-6.19M	18.3M	500.M	LSB
BIT WGHT ERR-BIT# 8	-500.M	-13.8M	8.49M	-41.1M	39.1M	-8.09M	-83.5M	80.7M	-961.U	-6.66M	7.99M	500.M	LSB
BIT WGHT ERR-BIT# 9	-500.M	-38.2M	13.7M	-84.8M	85.8M	-5.30M	-5.47M	-8.39M	6.88M	81.0M	-81.0M	500.M	LSB
BIT WGHT ERR-BIT# 10	-500.M	1.89M	17.3M	8.64M	80.3M	-1.69M	86.9M	-1.38M	-86.0M	10.5M	-4.03M	500.M	LSB
BIT WGHT ERR-BIT# 11	-500.M	-7.52M	4.47M	-14.7M	-16.2M	-87.4M	7.57M	-16.8M	-19.8M	-8.98M	-1.09M	500.M	LSB
BIT WGHT ERR-BIT# 12	-500.M	4.71M	4.34M	4.37M	81.4M	-1.99M	17.8M	85.5M	-465.U	40.8M	87.3M	500.M	LSB

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

TABLE 6.3. Device Type 01 Data at + 25°C.

MANUFACTURER CODE: ; DEVICE TYPE: 888; TEMPERATURE: 25 DEG C ; 25 OCT 79 10:55:24

PARAMETER	LO-LIM	36	48	HI-LIM	UNITS
ICC-SUPPLY CURRENT	3.00	13.6	13.3	18.0	MA
IEE-SUPPLY CURRENT	-25.0	-17.8	-17.1	-6.00	MA
IIH FOR BITS 1	-1.00	1.85	1.75	100.	MA
IIH FOR BITS 2	-1.00	1.85	2.10	100.	MA
IIH FOR BITS 3	-1.00	1.85	1.35	100.	MA
IIH FOR BITS 4	-1.00	1.95	1.85	100.	MA
IIH FOR BITS 5	-1.00	1.85	1.80	100.	MA
IIH FOR BITS 6	-1.00	2.10	2.15	100.	MA
IIH FOR BITS 7	-1.00	1.85	1.90	100.	MA
IIH FOR BITS 8	-1.00	2.10	1.90	100.	MA
IIH FOR BITS 9	-1.00	1.95	2.20	100.	MA
IIH FOR BITS 10	-1.00	2.30	2.35	100.	MA
IIH FOR BITS 11	-1.00	2.35	2.30	100.	MA
IIH FOR BITS 12	-1.00	3.80	3.35	100.	MA
IIL FOR BITS 1	-200.	-11.1	-7.90	1.00	UA
IIL FOR BITS 2	-200.	-11.0	-8.35	1.00	UA
IIL FOR BITS 3	-200.	-11.1	-7.90	1.00	UA
IIL FOR BITS 4	-200.	-11.0	-7.95	1.00	UA
IIL FOR BITS 5	-200.	-10.8	-7.90	1.00	UA
IIL FOR BITS 6	-200.	-10.8	-7.95	1.00	UA
IIL FOR BITS 7	-200.	-10.7	-7.95	1.00	UA
IIL FOR BITS 8	-200.	-10.7	-7.85	1.00	UA
IIL FOR BITS 9	-200.	-10.6	-7.65	1.00	UA
IIL FOR BITS 10	-200.	-10.7	-7.75	1.00	UA
IIL FOR BITS 11	-200.	-10.1	-7.60	1.00	UA
IIL FOR BITS 12	-200.	-10.1	-7.60	1.00	UA
FULL SCALE CURR.-TTL	1.50	2.09	1.99	2.50	MA
FULL SCALE CURR.-CMOS	1.50	2.09	1.99	2.50	MA
ZERO SCALE CURR.-TTL	-1.00K	-94.5	-134.	1.00K	NA
ZERO SCALE CURR.-CMOS	-1.00K	-124.	-119.	1.00K	NA
IOZ-DRIFT	-2.00	0.00	0.00	2.00	PPM/C
BIPOLAR OFFSET CURR.	750.M	1.05	995.M	1.25	MA
+PSS2 (CMOS) [+10%]	-800.	-81.2	-15.1	800.	UV
+PSS2 (CMOS) [-10%]	-800.	-33.4	-45.2	800.	UV
-PSS1 (TTL) [+10%]	-1.60K	-96.5	-60.3	1.60K	UV
-PSS1 (TTL) [-10%]	-1.60K	33.4	10.0	1.60K	UV
BIT WGHT ERR-BITS 1	-500.M	48.0M	231.M	500.M	LSB
BIT WGHT ERR-BITS 2	-500.M	-82.6M	293.U	500.M	LSB
BIT WGHT ERR-BITS 3	-500.M	-73.5M	-73.8M	500.M	LSB
BIT WGHT ERR-BITS 4	-500.M	-67.3M	-113.M	500.M	LSB
BIT WGHT ERR-BITS 5	-500.M	67.8M	-31.8M	500.M	LSB
BIT WGHT ERR-BITS 6	-500.M	17.9M	-8.64M	500.M	LSB
BIT WGHT ERR-BITS 7	-500.M	88.7M	-15.7M	500.M	LSB
BIT WGHT ERR-BITS 8	-500.M	874.U	-11.0M	500.M	LSB
BIT WGHT ERR-BITS 9	-500.M	-890.U	-18.1M	500.M	LSB
BIT WGHT ERR-BITS 10	-500.M	-13.1M	-10.8M	500.M	LSB
BIT WGHT ERR-BITS 11	-500.M	-45.8M	-13.3M	500.M	LSB
BIT WGHT ERR-BITS 12	-500.M	-8.80M	18.0M	500.M	LSB

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

TABLE 6.3. Device Type 01 Data at + 25°C.

MANUFACTURER CODE: ; DEVICE TYPE: 882; TEMPERATURE: 25 DEG C ; 26 OCT 79 10:58:45

PARAMETER	LO-LIM	4310	4312	4313	4314	4315	5	19	20	21	25	HI-LIM	UNITS
SUM BIT ERROR(+)	-500.M	39.7M	48.7M	78.1M	138.M	80.7M	166.M	104.M	186.M	833.M	146.M	500.M	LSB
SUM BIT ERROR(-)	-500.M	-78.6M	-36.7M	-108.M	-126.M	-93.6M	-154.M	-117.M	-201.M	-216.M	-111.M	500.M	LSB
SUM-ERROR(+)+ERROR(-)	-100.M	-38.8M	12.0M	-30.2M	11.3M	-12.8M	11.6M	-13.1M	-16.4M	17.8M	35.4M	100.M	LSB
GAIN ERROR (TTL)	-25.0	-4.48	-1.18	-861.M	-3.24	-1.18	6.83	8.36	4.90	4.18	5.63	25.0	MV
GAIN ERROR (CMOS)	-25.0	-4.78	-1.50	-1.02	-3.36	-1.36	6.81	8.14	4.49	4.15	5.40	25.0	MV
GAIN ERROR DRIFT (TTL) C	-5.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	5.00	PPM/
BIPOLAR OFFSET ERROR	-20.0	-2.70	-3.40	-731.M	-4.16	-3.43	-3.57	-4.59	-722.M	-3.20	-3.80	20.0	MV
BPOE DRIFT C	-4.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	4.00	PPM/
+PSS1 (TTL) [+10%]	-800.	-165.	-97.4	-78.1	-30.8	-31.2	-78.6	-68.8	-113.	-104.	-95.2	800.	UV
+PSS1 (TTL) [-10%]	-800.	87.8	0.00	-10.4	30.8	0.00	30.6	0.00	0.00	49.6	36.3	800.	UV
MJR CARRY ERR-BITS 1	-900.M	-3.63M	45.1M	18.9M	-113.M	64.0M	-13.4M	-30.9M	389.M	456.M	-162.M	900.M	LSB
MJR CARRY ERR-BITS 2	-900.M	95.5M	117.M	128.M	-935.U	126.M	151.M	76.1M	151.M	251.M	60.7M	900.M	LSB
MJR CARRY ERR-BITS 3	-900.M	-54.4M	48.4M	2.20M	-101.M	-31.8M	250.M	101.M	85.8M	198.M	135.M	900.M	LSB
MJR CARRY ERR-BITS 4	-900.M	21.7M	94.6M	89.7M	-50.2M	-6.26M	121.M	-815.U	1.64M	113.M	42.1M	900.M	LSB
MJR CARRY ERR-BITS 5	-900.M	76.7M	-6.16M	120.M	129.M	70.4M	45.8M	112.M	56.4M	1.62M	114.M	900.M	LSB
MJR CARRY ERR-BITS 6	-900.M	21.7M	-31.4M	-2.03M	-27.0M	23.5M	-61.5M	55.5M	5.86M	13.8M	-19.1M	900.M	LSB
MJR CARRY ERR-BITS 7	-900.M	36.5M	21.1M	23.6M	42.5M	51.2M	-2.47M	44.2M	5.86M	19.9M	34.7M	900.M	LSB
MJR CARRY ERR-BITS 8	-900.M	21.6M	14.8M	-4.17M	6.65M	-6.25M	-20.4M	38.6M	5.86M	-416.U	23.6M	900.M	LSB
MJR CARRY ERR-BITS 9	-900.M	6.83M	14.8M	27.8M	8.76M	-1.99M	-15.0M	-6.44M	10.1M	17.9M	-6.11M	900.M	LSB
MJR CARRY ERR-BITS 10	-900.M	38.6M	21.1M	25.7M	19.3M	19.3M	31.5M	2.94M	-13.1M	-22.7M	21.7M	900.M	LSB
MJR CARRY ERR-BITS 11	-900.M	-12.2M	136.U	-19.1M	-37.6M	-25.4M	-9.63M	-42.1M	-19.4M	-47.1M	-28.4M	900.M	LSB

TABLE 6.3. Device Type 01 Data at + 25°C.

MANUFACTURER CODE: ; DEVICE TYPE: 568; TEMPERATURE: 25 DEG C ; 25 OCT 79 10:58:59

PARAMETER	LO-LIM	3S	4S	HI-LIM	UNITS
SUM BIT ERROR(+)	-500.M	151.M	800.M	500.M	LSB
SUM BIT ERROR(-)	-500.M	-189.M	-868.M	500.M	LSB
SUM-ERROR(+)+ERROR(-)	-100.M	-38.3M	-68.0M	100.M	LSB
GAIN ERROR (TTL)	-25.0	3.53	5.05	25.0	MV
GAIN ERROR (CMOS)	-25.0	3.17	4.88	25.0	MV
GAIN ERROR DRIFT (TTL)	-5.00	0.00	0.00	5.00	PPM/C
BIPOLAR OFFSET ERROR	-20.0	-2.11	-3.12	20.0	MV
BPOE DRIFT	-4.00	0.00	0.00	4.00	PPM/C
+PSS1 (TTL) [+10%]	-800.	-43.0	-20.1	800.	UV
+PSS1 (TTL) [-10%]	-800.	-23.9	-15.1	800.	UV
MJR CARRY ERR-BITS 1	-900.M	111.M	464.M	900.M	LSB
MJR CARRY ERR-BITS 2	-900.M	-80.6M	242.M	900.M	LSB
MJR CARRY ERR-BITS 3	-900.M	-112.M	98.1M	900.M	LSB
MJR CARRY ERR-BITS 4	-900.M	-133.M	-35.4M	900.M	LSB
MJR CARRY ERR-BITS 5	-900.M	52.5M	48.8M	900.M	LSB
MJR CARRY ERR-BITS 6	-900.M	23.1M	50.9M	900.M	LSB
MJR CARRY ERR-BITS 7	-900.M	19.2M	20.1M	900.M	LSB
MJR CARRY ERR-BITS 8	-900.M	-6.20M	7.73M	900.M	LSB
MJR CARRY ERR-BITS 9	-900.M	13.4M	-25.2M	900.M	LSB
MJR CARRY ERR-BITS 10	-900.M	-6.20M	-12.8M	900.M	LSB
MJR CARRY ERR-BITS 11	-900.M	-39.4M	-29.3M	900.M	LSB

TABLE 6.4. Device Type 01 Data at + 125°C.

MANUFACTURER CODE: ; DEVICE TYPE: 882; TEMPERATURE: 125 DEG C ; 26 OCT 79 11:06:04

PARAMETER	LO-LIM	4310	4312	4313	4314	4315	5	19	20	21	25	HI-LIM	UNITS
ICC-SUPPLY CURRENT	3.00	9.75	10.4	10.2	10.1	10.1	11.1	10.8	10.6	11.0	10.7	10.0	MA
IEE-SUPPLY CURRENT	-25.0	-14.0	-14.2	-14.1	-14.1	-14.1	-16.0	-15.4	-16.5	-15.9	-17.1	-6.00	MA
IIH FOR BITS 1	-1.00	10.0	9.30	9.15	8.75	10.7	19.0	20.4	13.6	10.2	27.5	100.	MA
IIH FOR BITS 2	-1.00	12.1	11.1	9.80	9.65	10.1	15.1	24.3	12.4	11.3	28.3	100.	MA
IIH FOR BITS 3	-1.00	11.5	9.65	10.0	9.40	9.65	17.7	25.3	13.3	10.5	25.9	100.	MA
IIH FOR BITS 4	-1.00	16.7	9.75	9.80	9.15	9.95	14.7	24.8	12.9	11.0	30.2	100.	MA
IIH FOR BITS 5	-1.00	18.1	12.1	9.60	9.10	9.85	23.5	24.3	15.3	10.8	26.4	100.	MA
IIH FOR BITS 6	-1.00	12.1	10.6	9.85	10.0	9.95	22.5	27.2	13.7	11.4	28.0	100.	MA
IIH FOR BITS 7	-1.00	11.7	9.65	9.95	9.80	9.65	18.4	27.4	12.4	10.5	26.5	100.	MA
IIH FOR BITS 8	-1.00	12.2	9.90	9.75	9.15	9.95	32.4	30.0	11.9	11.2	26.4	100.	MA
IIH FOR BITS 9	-1.00	11.4	10.4	9.45	9.80	9.95	19.4	32.8	12.0	11.5	23.3	100.	MA
IIH FOR BITS 10	-1.00	12.9	10.8	9.85	9.90	13.2	17.9	26.5	13.7	12.1	24.2	100.	MA
IIH FOR BITS 11	-1.00	14.5	10.6	9.95	10.5	10.1	18.4	30.6	12.4	11.5	27.8	100.	MA
IIH FOR BITS 12	-1.00	13.5	12.1	11.5	11.3	10.6	13.7	28.0	12.3	14.5	28.0	100.	MA
IIL FOR BITS 1	-200.	-6.95	-7.65	-7.25	-7.55	-7.05	-9.40	-8.70	-8.85	-10.7	-11.3	1.00	UA
IIL FOR BITS 2	-200.	-7.05	-7.50	-7.35	-8.15	-7.20	-9.55	-9.15	-7.70	-9.90	-11.1	1.00	UA
IIL FOR BITS 3	-200.	-6.90	-7.50	-7.20	-7.45	-7.05	-10.6	-8.75	-7.55	-9.70	-11.0	1.00	UA
IIL FOR BITS 4	-200.	-6.85	-7.45	-7.30	-7.40	-7.20	-9.00	-8.50	-7.55	-9.65	-11.1	1.00	UA
IIL FOR BITS 5	-200.	-6.85	-7.40	-7.10	-7.35	-7.25	-10.6	-8.95	-7.45	-9.50	-10.7	1.00	UA
IIL FOR BITS 6	-200.	-6.85	-7.40	-7.25	-7.25	-7.25	-9.85	-12.8	-7.40	-9.55	-10.7	1.00	UA
IIL FOR BITS 7	-200.	-6.85	-7.40	-7.15	-7.20	-7.15	-9.00	-9.30	-7.30	-9.40	-10.4	1.00	UA
IIL FOR BITS 8	-200.	-6.65	-7.30	-7.15	-7.20	-7.30	-11.9	-9.65	-7.45	-9.45	-10.5	1.00	UA
IIL FOR BITS 9	-200.	-6.50	-7.40	-7.05	-7.25	-7.05	-9.50	-9.25	-7.35	-9.20	-10.2	1.00	UA
IIL FOR BITS 10	-200.	-6.70	-7.90	-7.20	-7.25	-7.05	-8.95	-9.20	-7.15	-9.30	-10.1	1.00	UA
IIL FOR BITS 11	-200.	-6.50	-8.05	-7.05	-7.20	-7.20	-8.85	-9.10	-7.05	-9.30	-14.6	1.00	UA
IIL FOR BITS 12	-200.	-6.50	-7.30	-7.05	-7.25	-7.10	-9.25	-9.10	-7.20	-9.35	-15.0	1.00	UA
FULL SCALE CURR.-TTL	1.50	1.94	1.95	1.93	1.94	1.93	2.29	2.18	1.95	2.01	2.20	2.50	MA
FULL SCALE CURR.-CMOS	1.50	1.94	1.95	1.93	1.94	1.93	2.28	2.18	1.94	2.02	2.21	2.50	MA
ZERO SCALE CURR.-TTL	-1.00K	13.5	3.50	-7.50	27.5	-6.00	16.0	-15.0	-44.5	-59.0	58.0	1.00K	NA
ZERO SCALE CURR.-CMOS	-1.00K	-40.5	-30.0	-38.5	-22.5	-30.5	-30.5	-48.0	-69.0	-48.5	12.0	1.00K	NA
IO2-DRIFT	-2.00	370.M	139.M	159.M	306.M	183.M	385.M	428.M	273.M	179.M	240.M	2.00	PPM/C
BIPOLAR OFFSET CURR.	750.M	975.M	975.M	970.M	970.M	970.M	1.15	1.09	980.M	1.01	1.11	1.25	MA
+PSS2 (CMOS) [+10%]	-800.	-51.4	-20.6	5.18	-15.5	20.7	-30.4	-68.6	-20.5	4.96	-40.7	800.	UV
+PSS2 (CMOS) [-10%]	-800.	15.4	-20.6	-36.3	-72.1	-56.8	-65.2	-41.2	-51.3	-4.96	-72.3	800.	UV
-PSS1 (TTL) [+10%]	-1.60K	0.00	41.1	0.00	-36.1	-15.5	-91.3	-101.	-35.9	-9.91	-72.3	1.60K	UV
-PSS1 (TTL) [-10%]	-1.60K	15.4	30.8	-5.18	15.5	-5.17	43.5	73.2	25.6	39.7	0.00	1.60K	UV
BIT WGHT ERR-BITS 1	-500.M	20.3M	5.08M	-15.2M	46.9M	18.4M	-138.M	-113.M	176.M	126.M	-105.M	500.M	LSB
BIT WGHT ERR-BITS 2	-500.M	55.3M	73.1M	51.9M	51.8M	38.8M	203.M	178.M	488.U	61.1M	92.7M	500.M	LSB
BIT WGHT ERR-BITS 3	-500.M	-27.6M	-31.8M	9.96M	34.9M	-26.2M	25.0M	63.9M	7.57M	14.3M	112.M	500.M	LSB
BIT WGHT ERR-BITS 4	-500.M	70.6M	30.4M	44.3M	50.2M	7.06M	57.9M	31.9M	8.00M	88.6M	43.1M	500.M	LSB
BIT WGHT ERR-BITS 5	-500.M	-24.8M	-161.M	-81.4M	-79.4M	-84.0M	-57.4M	-30.8M	-41.1M	-90.3M	-22.0M	500.M	LSB
BIT WGHT ERR-BITS 6	-500.M	-34.8M	-87.1M	-82.9M	-110.M	-84.7M	-29.6M	-25.7M	-24.8M	-60.4M	-86.9M	500.M	LSB
BIT WGHT ERR-BITS 7	-500.M	-16.3M	-89.9M	-68.6M	-36.8M	6.70M	67.1M	-14.7M	17.0M	262.U	9.20M	500.M	LSB
BIT WGHT ERR-BITS 8	-500.M	-18.6M	-19.2M	-26.0M	-6.97M	-1.94M	5.96M	88.2M	8.50M	-4.94M	-6.46M	500.M	LSB
BIT WGHT ERR-BITS 9	-500.M	-25.1M	-10.6M	-3.46M	8.63M	87.7U	27.9M	1.93M	28.1M	9.71M	-8.78M	500.M	LSB
BIT WGHT ERR-BITS 10	-500.M	1.13M	-8.47M	-3.85M	7.42M	4.28M	35.3M	1.90M	-1.55M	-21.6M	8.57M	500.M	LSB
BIT WGHT ERR-BITS 11	-500.M	-12.1M	-19.0M	-1.93M	-7.87M	-29.6M	-8.16M	-17.8M	-7.07M	-41.2M	-15.2M	500.M	LSB
BIT WGHT ERR-BITS 12	-500.M	12.0M	-13.0U	-4.15M	13.0M	10.6M	19.1M	29.5M	18.5M	5.78M	27.6M	500.M	LSB

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

TABLE 6.4. Device Type 01 Data at 125°C.

MANUFACTURER CODE: ; DEVICE TYPE: 882; TEMPERATURE: 125 DEG C ; 25 OCT 79 1:06:33

PARAMETER	LO-LIM	36	48	HI-LIM	UNITS
ICC-SUPPLY CURRENT	3.00	18.6	18.1	18.0	MA
IEE-SUPPLY CURRENT	-25.0	-17.0	-16.2	-5.00	MA
IIH FOR BIT# 1	-1.00	26.2	10.7	100.	NA
IIH FOR BIT# 2	-1.00	27.5	11.5	100.	NA
IIH FOR BIT# 3	-1.00	31.8	11.4	100.	NA
IIH FOR BIT# 4	-1.00	24.8	10.8	100.	NA
IIH FOR BIT# 5	-1.00	24.8	11.6	100.	NA
IIH FOR BIT# 6	-1.00	28.6	10.7	100.	NA
IIH FOR BIT# 7	-1.00	24.3	10.7	100.	NA
IIH FOR BIT# 8	-1.00	26.5	10.7	100.	NA
IIH FOR BIT# 9	-1.00	25.1	10.6	100.	NA
IIH FOR BIT# 10	-1.00	22.4	12.0	100.	NA
IIH FOR BIT# 11	-1.00	22.9	13.5	100.	NA
IIH FOR BIT# 12	-1.00	26.9	10.8	100.	NA
IIL FOR BIT# 1	-200.	-12.5	-8.20	1.00	UA
IIL FOR BIT# 2	-200.	-11.9	-8.60	1.00	UA
IIL FOR BIT# 3	-200.	-11.9	-8.15	1.00	UA
IIL FOR BIT# 4	-200.	-11.9	-8.25	1.00	UA
IIL FOR BIT# 5	-200.	-11.8	-8.15	1.00	UA
IIL FOR BIT# 6	-200.	-11.7	-8.30	1.00	UA
IIL FOR BIT# 7	-200.	-11.7	-8.25	1.00	UA
IIL FOR BIT# 8	-200.	-11.7	-8.15	1.00	UA
IIL FOR BIT# 9	-200.	-11.7	-8.00	1.00	UA
IIL FOR BIT# 10	-200.	-11.7	-8.00	1.00	UA
IIL FOR BIT# 11	-200.	-11.3	-7.80	1.00	UA
IIL FOR BIT# 12	-200.	-11.3	-7.85	1.00	UA
FULL SCALE CURR.-TTL	1.50	2.09	2.00	2.50	MA
FULL SCALE CURR.-CMOS	1.50	2.09	1.99	2.50	MA
ZERO SCALE CURR.-TTL	-1.00K	-14.0	-97.0	1.00K	NA
ZERO SCALE CURR.-CMOS	-1.00K	-43.0	-85.5	1.00K	NA
IOZ-DRIFT	-2.00	385.M	185.M	2.00	PPM/C
BIPOLAR OFFSET CURR.	750.M	1.05	1.00	1.25	MA
+PSS2 (CMOS) [+10%]	-800.	-14.3	-25.0	800.	UV
+PSS2 (CMOS) [-10%]	-800.	0.00	-40.1	800.	UV
-PSS1 (TTL) [+10%]	-1.60K	33.3	-30.0	1.60K	UV
-PSS1 (TTL) [-10%]	-1.60K	0.00	45.1	1.60K	UV
BIT WGHT ERR-BIT# 1	-500.M	52.3M	185.M	500.M	LSB
BIT WGHT ERR-BIT# 2	-500.M	-66.5M	25.0M	500.M	LSB
BIT WGHT ERR-BIT# 3	-500.M	14.6M	-41.8M	500.M	LSB
BIT WGHT ERR-BIT# 4	-500.M	24.8M	-33.8M	500.M	LSB
BIT WGHT ERR-BIT# 5	-500.M	87.1M	-66.9M	500.M	LSB
BIT WGHT ERR-BIT# 6	-500.M	6.70M	-89.3M	500.M	LSB
BIT WGHT ERR-BIT# 7	-500.M	16.1M	-19.8M	500.M	LSB
BIT WGHT ERR-BIT# 8	-500.M	7.63M	358.U	500.M	LSB
BIT WGHT ERR-BIT# 9	-500.M	16.6M	-13.1M	500.M	LSB
BIT WGHT ERR-BIT# 10	-500.M	81.4M	603.U	500.M	LSB
BIT WGHT ERR-BIT# 11	-500.M	-5.89M	-83.3M	500.M	LSB
BIT WGHT ERR-BIT# 12	-500.M	89.3M	86.3M	500.M	LSB

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

TABLE 6.4. Device Type 01 Data at + 125°C.

MANUFACTURER CODE: ; DEVICE TYPE: 888; TEMPERATURE: 125 DEG C ; 25 OCT 78 11:06:53

PARAMETER	LO-LIM	4310	4318	4313	4314	4315	5	19	20	21	26	HI-LIM	UNITS
SUM BIT ERROR(+)	-500.M	126.M	176.M	106.M	163.M	68.4M	296.M	248.M	127.M	198.M	225.M	500.M	LSB
SUM BIT ERROR(-)	-500.M	-174.M	-196.M	-137.M	-209.M	-104.M	-276.M	-270.M	-99.7M	-200.M	-230.M	500.M	LSB
SUM-ERROR(+)+ERROR(-)	-100.M	-48.9M	-18.9M	-30.9M	-46.0M	-37.9M	21.3M	-22.1M	27.6M	-2.10M	-4.88M	100.M	LSB
GAIN ERROR (TTL)	-25.0	-2.56	272.M	-964.M	-2.71	-36.8M	5.39	4.83	4.36	3.06	1.90	25.0	MV
GAIN ERROR (CMOS)	-25.0	-2.91	82.8M	-974.M	-2.92	-155.M	5.18	4.58	3.84	3.08	1.68	25.0	MV
GAIN ERROR DRIFT (TTL) C	-5.00	1.92	1.46	-103.M	538.M	1.14	-1.44	-3.53	-546.M	-1.12	-3.72	5.00	PPM/
BIPOLAR OFFSET ERROR	-20.0	-3.10	-2.67	-625.M	-3.42	-3.00	-5.06	-5.46	0.00	-3.17	-4.80	20.0	MV
BPOE DRIFT C	-4.00	-198.M	363.M	52.8M	367.M	217.M	-745.M	-439.M	361.M	15.8M	-498.M	4.00	PPM/
+PSS1 (TTL) [+10%]	-800.	-36.0	-92.5	-119.	-165.	-51.7	-17.4	-4.57	-133.	-124.	-36.2	800.	UV
+PSS1 (TTL) [-10%]	-800.	0.00	30.8	-15.5	103.	41.3	0.00	4.57	15.4	0.00	-18.1	800.	UV
MJR CARRY ERR-BIT# 1	-900.M	74.7M	103.M	4.40M	108.M	52.9M	-337.M	-255.M	310.M	207.M	-195.M	900.M	LSB
MJR CARRY ERR-BIT# 2	-900.M	157.M	259.M	140.M	189.M	114.M	183.M	211.M	138.M	195.M	83.1M	900.M	LSB
MJR CARRY ERR-BIT# 3	-900.M	40.3M	170.M	110.M	195.M	42.3M	33.3M	162.M	163.M	211.M	189.M	900.M	LSB
MJR CARRY ERR-BIT# 4	-900.M	207.M	272.M	183.M	258.M	116.M	149.M	177.M	151.M	257.M	176.M	900.M	LSB
MJR CARRY ERR-BIT# 5	-900.M	55.0M	-23.2M	121.M	63.6M	72.0M	-45.0M	96.9M	35.3M	34.2M	96.1M	900.M	LSB
MJR CARRY ERR-BIT# 6	-900.M	2.39M	-27.4M	-4.15M	-52.5M	25.4M	-64.6M	52.0M	-17.2M	-2.34M	-27.9M	900.M	LSB
MJR CARRY ERR-BIT# 7	-900.M	25.6M	16.8M	98.1U	27.7M	50.8M	60.0M	25.8M	-2.49M	-4.37M	53.5M	900.M	LSB
MJR CARRY ERR-BIT# 8	-900.M	12.9M	6.30M	38.3M	40.4M	-10.6M	-57.5M	42.6M	-2.49M	-2.34M	3.53M	900.M	LSB
MJR CARRY ERR-BIT# 9	-900.M	6.60M	10.5M	10.7M	21.4M	-2.11M	-5.86M	-15.4M	10.1M	15.9M	-2.02M	900.M	LSB
MJR CARRY ERR-BIT# 10	-900.M	34.0M	23.1M	8.59M	29.8M	16.9M	24.4M	-4.21M	-10.9M	-26.7M	9.09M	900.M	LSB
MJR CARRY ERR-BIT# 11	-900.M	-25.0M	-19.0M	2.22M	-20.8M	-40.2M	-27.2M	-47.3M	-25.6M	-47.0M	-42.8M	900.M	LSB

TABLE 6.4. Device Type 01 Data at + 125°C.

MANUFACTURER CODE: ; DEVICE TYPE: 968; TEMPERATURE: 125 DEG C ; 05 OCT 78 11:07:07

PARAMETER	LO-LIM	36	48	HI-LIM	UNITS
SUM BIT ERROR(+)	-500.M	114.M	198.M	500.M	LSB
SUM BIT ERROR(-)	-500.M	-125.M	-199.M	500.M	LSB
SUM-ERROR(+)+ERROR(-)	-100.M	-10.8M	-8.34M	100.M	LSB
GAIN ERROR (TTL)	-25.0	414.M	3.87	25.0	MV
GAIN ERROR (CMOS)	-25.0	19.1M	3.61	25.0	MV
GAIN ERROR DRIFT (TTL)	-5.00	-3.12	-1.18	5.00	PPM/C
BIPOLAR OFFSET ERROR	-20.0	-3.54	-3.91	20.0	MV
BPOE DRIFT	-4.00	-715.M	-395.M	4.00	PPM/C
+PSS1 (TTL) [+10%]	-800.	-61.9	-100.	800.	UV
+PSS1 (TTL) [-10%]	-800.	-9.53	10.0	800.	UV
MJR CARRY ERR-BIT# 1	-900.M	111.M	379.M	900.M	LSB
MJR CARRY ERR-BIT# 2	-900.M	-131.M	235.M	900.M	LSB
MJR CARRY ERR-BIT# 3	-900.M	-48.8M	141.M	900.M	LSB
MJR CARRY ERR-BIT# 4	-900.M	-23.4M	139.M	900.M	LSB
MJR CARRY ERR-BIT# 5	-900.M	9.74M	7.84M	900.M	LSB
MJR CARRY ERR-BIT# 6	-900.M	27.3M	7.84M	900.M	LSB
MJR CARRY ERR-BIT# 7	-900.M	7.79M	-362.U	900.M	LSB
MJR CARRY ERR-BIT# 8	-900.M	-7.82M	-12.7M	900.M	LSB
MJR CARRY ERR-BIT# 9	-900.M	7.79M	-22.9M	900.M	LSB
MJR CARRY ERR-BIT# 10	-900.M	-3.92M	-12.7M	900.M	LSB
MJR CARRY ERR-BIT# 11	-900.M	-35.1M	-49.6M	900.M	LSB

TABLE 6.5. Device Type 01 Data at - 55°C.

MANUFACTURER CODE: ; DEVICE TYPE: 568; TEMPERATURE: -55 DEG C ; 05 OCT 79 11:13:07

PARAMETER	LO-LIM	4310	4318	4313	4314	4315	5	10	80	81	85	HI-LIM	UNITS
ICC-SUPPLY CURRENT	3.00	18.8	13.0	18.0	18.7	18.7	13.1	13.3	14.9	14.8	14.6	18.0	MA
IEE-SUPPLY CURRENT	-26.0	-18.4	-17.0	-16.7	-16.4	-16.6	-18.3	-17.9	-18.7	-18.4	-19.3	-6.00	MA
IIH FOR BIT# 1	-1.00	1.80	8.35	38.8	102. *	102. *	10.4	10.1	8.00	1.95	1.90	100.	MA
IIH FOR BIT# 2	-1.00	8.15	10.6	24.2	4.55	34.4	8.00	1.95	1.55	1.85	1.90	100.	MA
IIH FOR BIT# 3	-1.00	1.35	18.3	11.7	18.5	77.9	1.90	1.80	1.95	1.80	1.70	100.	MA
IIH FOR BIT# 4	-1.00	1.85	3.30	6.90	1.75	6.90	1.95	2.00	1.75	1.95	1.85	100.	MA
IIH FOR BIT# 5	-1.00	1.75	6.70	3.20	1.95	7.85	2.45	1.95	1.90	1.40	1.85	100.	MA
IIH FOR BIT# 6	-1.00	2.15	20.3	3.20	2.30	3.00	8.90	2.30	102. *	2.05	2.25	100.	MA
IIH FOR BIT# 7	-1.00	2.25	2.40	4.15	1.80	3.55	1.95	2.00	102. *	6.90	10.4	100.	MA
IIH FOR BIT# 8	-1.00	2.05	2.40	2.00	2.00	2.60	2.25	2.20	1.95	2.50	2.30	100.	MA
IIH FOR BIT# 9	-1.00	2.10	2.40	2.05	2.20	1.95	2.40	1.95	2.40	1.85	2.15	100.	MA
IIH FOR BIT# 10	-1.00	2.55	2.75	2.40	2.55	5.10	2.45	2.35	2.20	2.90	2.40	100.	MA
IIH FOR BIT# 11	-1.00	2.40	3.35	3.55	2.65	4.45	27.9	5.15	2.65	3.50	7.05	100.	MA
IIH FOR BIT# 12	-1.00	5.55	9.90	8.25	6.60	9.00	3.80	6.40	4.25	6.60	13.3	100.	MA
IIL FOR BIT# 1	-200.	-8.45	-9.15	-8.75	-9.05	-8.65	-8.95	-6.90	-7.90	-9.85	-8.70	1.00	UA
IIL FOR BIT# 2	-200.	-8.70	-9.00	-8.90	-10.1	-8.90	-8.75	-8.00	-6.20	-8.30	-8.45	1.00	UA
IIL FOR BIT# 3	-200.	-8.60	-8.85	-8.75	-8.90	-8.65	-11.5	-7.20	-6.00	-8.20	-8.50	1.00	UA
IIL FOR BIT# 4	-200.	-8.65	-8.70	-8.80	-8.85	-8.80	-7.75	-6.85	-6.05	-8.15	-8.55	1.00	UA
IIL FOR BIT# 5	-200.	-8.50	-8.75	-8.65	-8.80	-8.90	-12.3	-7.50	-5.95	-8.05	-8.30	1.00	UA
IIL FOR BIT# 6	-200.	-8.45	-8.75	-8.80	-8.60	-8.95	-10.2	-13.3	-5.95	-8.10	-8.25	1.00	UA
IIL FOR BIT# 7	-200.	-8.45	-8.75	-8.75	-8.80	-8.75	-7.80	-7.70	-5.90	-8.00	-8.05	1.00	UA
IIL FOR BIT# 8	-200.	-8.35	-8.55	-8.70	-8.65	-8.90	-18.2	-8.40	-6.20	-8.05	-8.10	1.00	UA
IIL FOR BIT# 9	-200.	-8.25	-8.70	-8.70	-8.70	-8.65	-9.25	-7.60	-6.05	-7.70	-7.90	1.00	UA
IIL FOR BIT# 10	-200.	-8.40	-9.85	-8.75	-8.65	-8.65	-7.65	-7.60	-5.70	-7.80	-7.70	1.00	UA
IIL FOR BIT# 11	-200.	-8.10	-9.85	-8.65	-8.60	-8.80	-7.75	-7.20	-5.50	-7.60	-13.8	1.00	UA
IIL FOR BIT# 12	-200.	-8.15	-8.65	-8.60	-8.70	-8.65	-8.50	-7.15	-5.75	-7.65	-14.7	1.00	UA
FULL SCALE CURR.-TTL	1.50	1.93	1.93	1.92	1.93	1.92	2.28	2.17	1.94	2.00	2.21	2.50	MA
FULL SCALE CURR.-CMOS	1.50	1.93	1.94	1.92	1.93	1.92	2.27	2.17	1.94	2.00	2.20	2.50	MA
ZERO SCALE CURR.-TTL	-1.00K	-107.	-57.5	-53.0	-54.5	-53.0	-136.	-124.	-132.	-101.	6.00	1.00K	NA
ZERO SCALE CURR.-CMOS	-1.00K	-104.	-85.5	-86.5	-70.5	-100.	-127.	-150.	-119.	-138.	-14.0	1.00K	NA
IOZ-DRIFT	-2.00	-317.M	-219.M	-97.7M	-149.M	-78.3M	-347.M	-94.8M	-226.M	-40.4M	5.67M	2.00	PPM/C
BIPOLAR OFFSET CURR.	750.M	970.M	975.M	960.M	965.M	965.M	1.14	1.09	975.M	1.00	1.10	1.25	MA
+PSS2 (CMOS) [+10%]	-800.	-31.1	-82.2	6.21	-124.	-104.	-35.0	-73.5	-62.0	34.9	-127.	800.	UV
+PSS2 (CMOS) [-10%]	-800.	-10.4	-20.6	26.0	51.8	31.2	-43.8	46.0	-72.3	14.9	58.9	800.	UV
-PSS1 (TTL) [+10%]	-1.60K	-62.2	-5.14	62.5	-36.3	-15.6	0.00	-9.19	-114.	29.9	0.00	1.60K	UV
-PSS1 (TTL) [-10%]	-1.60K	62.2	77.1	-20.8	20.7	46.8	0.00	0.00	67.2	24.9	-13.6	1.60K	UV
BIT WGHT ERR-BIT# 1	-500.M	87.0M	23.0M	-9.37M	-168.M	36.5M	475.M	227.M	245.M	381.M	-17.6M	500.M	LSB
BIT WGHT ERR-BIT# 2	-500.M	58.5M	8.73M	13.4M	-71.5M	35.3M	-166.M	-221.M	-20.1M	-85.9M	52.5M	500.M	LSB
BIT WGHT ERR-BIT# 3	-500.M	-66.7M	-71.8M	-91.5M	-83.7M	-85.5M	412.M	108.M	-77.7M	-22.5M	61.3M	500.M	LSB
BIT WGHT ERR-BIT# 4	-500.M	-98.2M	16.7M	-68.1M	-34.5M	-38.5M	-149.M	-131.M	-117.M	-86.7M	-55.0M	500.M	LSB
BIT WGHT ERR-BIT# 5	-500.M	48.5M	-30.1M	31.6M	177.M	80.1M	-119.M	66.7M	-36.4M	-88.2M	-18.7M	500.M	LSB
BIT WGHT ERR-BIT# 6	-500.M	-17.7M	80.8M	-44.0M	-30.4M	-88.9M	-895.M	-7.36M	-60.5M	-48.8M	-36.9M	500.M	LSB
BIT WGHT ERR-BIT# 7	-500.M	-13.1M	11.4M	-5.98M	-18.0M	-14.7M	-380.M	-36.6M	-14.4M	-49.6M	73.2U	500.M	LSB
BIT WGHT ERR-BIT# 8	-500.M	-188.U	30.4M	-9.39M	-36.8M	-48.4M	-34.3M	-30.5M	-15.6M	-21.7M	-10.2M	500.M	LSB
BIT WGHT ERR-BIT# 9	-500.M	-8.59M	34.4M	-15.4M	-8.71M	-87.6M	-18.7M	-80.9M	-6.77M	-8.71M	6.97M	500.M	LSB
BIT WGHT ERR-BIT# 10	-500.M	10.8M	42.6M	-15.1M	-7.60M	-4.83M	7.12M	-15.1M	6.13M	-80.7M	-9.49M	500.M	LSB
BIT WGHT ERR-BIT# 11	-500.M	1.04M	86.5M	-40.6M	-14.4M	-19.1M	-18.0M	-6.63M	-18.1M	-1.19M	-18.7M	500.M	LSB
BIT WGHT ERR-BIT# 12	-500.M	18.6M	40.1M	-18.9M	-25.2M	-10.6M	-12.6M	11.7M	82.7M	19.9M	12.0M	500.M	LSB

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

TABLE 6.5. Device Type 01 Data at - 55°C.

MANUFACTURER CODE: ; DEVICE TYPE: 582; TEMPERATURE: -55 DEG C ; 25 OCT 79 1:16:30

PARAMETER	LO-LIM	36	48	HI-LIM	UNITS
ICC-SUPPLY CURRENT	3.00	14.5	13.8	18.0	MA
IEE-SUPPLY CURRENT	-86.0	-18.9	-17.6	-6.00	MA
IIH FOR BITS 1	-1.00	3.00	1.70	100.	NA
IIH FOR BITS 2	-1.00	1.80	1.80	100.	NA
IIH FOR BITS 3	-1.00	1.95	1.95	100.	NA
IIH FOR BITS 4	-1.00	1.65	1.70	100.	NA
IIH FOR BITS 5	-1.00	1.90	1.90	100.	NA
IIH FOR BITS 6	-1.00	2.50	2.15	100.	NA
IIH FOR BITS 7	-1.00	102.	* 21.7	100.	NA
IIH FOR BITS 8	-1.00	2.30	2.00	100.	NA
IIH FOR BITS 9	-1.00	2.70	2.20	100.	NA
IIH FOR BITS 10	-1.00	2.45	2.45	100.	NA
IIH FOR BITS 11	-1.00	3.30	2.90	100.	NA
IIH FOR BITS 12	-1.00	7.55	6.65	100.	NA
IIL FOR BITS 1	-200.	-9.00	-6.75	1.00	UA
IIL FOR BITS 2	-200.	-8.75	-7.20	1.00	UA
IIL FOR BITS 3	-200.	-9.00	-6.85	1.00	UA
IIL FOR BITS 4	-200.	-8.80	-6.95	1.00	UA
IIL FOR BITS 5	-200.	-8.85	-6.85	1.00	UA
IIL FOR BITS 6	-200.	-8.75	-6.95	1.00	UA
IIL FOR BITS 7	-200.	-8.70	-6.90	1.00	UA
IIL FOR BITS 8	-200.	-8.70	-6.90	1.00	UA
IIL FOR BITS 9	-200.	-8.65	-6.70	1.00	UA
IIL FOR BITS 10	-200.	-8.75	-6.85	1.00	UA
IIL FOR BITS 11	-200.	-8.10	-6.65	1.00	UA
IIL FOR BITS 12	-200.	-8.15	-6.65	1.00	UA
FULL SCALE CURR.-TTL	1.50	2.09	1.99	2.50	MA
FULL SCALE CURR.-CMOS	1.50	2.08	1.99	2.50	MA
ZERO SCALE CURR.-TTL	-1.00K	-124.	-138.	1.00K	NA
ZERO SCALE CURR.-CMOS	-1.00K	-132.	-151.	1.00K	NA
IOZ-DRIFT	-2.00	-176.M	-21.9M	2.00	PPM/C
BIPOLAR OFFSET CURR.	750.M	1.05	995.M	1.25	MA
+PSS2 (CMOS) [+10%]	-800.	-90.7	-85.4	800.	UV
+PSS2 (CMOS) [-10%]	-800.	-19.1	60.3	800.	UV
-PSS1 (TTL) [+10%]	-1.60K	-105.	-20.1	1.60K	UV
-PSS1 (TTL) [-10%]	-1.60K	81.2	15.1	1.60K	UV
BIT WGHT ERR-BITS 1	-500.M	-118.M	273.M	500.M	LSB
BIT WGHT ERR-BITS 2	-500.M	109.M	-8.44M	500.M	LSB
BIT WGHT ERR-BITS 3	-500.M	27.1M	-83.3M	500.M	LSB
BIT WGHT ERR-BITS 4	-500.M	-78.3M	-145.M	500.M	LSB
BIT WGHT ERR-BITS 5	-500.M	97.6M	838.U	500.M	LSB
BIT WGHT ERR-BITS 6	-500.M	58.7M	-8.97M	500.M	LSB
BIT WGHT ERR-BITS 7	-500.M	38.1M	-89.2M	500.M	LSB
BIT WGHT ERR-BITS 8	-500.M	39.6M	-18.6M	500.M	LSB
BIT WGHT ERR-BITS 9	-500.M	18.8M	-15.6M	500.M	LSB
BIT WGHT ERR-BITS 10	-500.M	80.8M	-6.74M	500.M	LSB
BIT WGHT ERR-BITS 11	-500.M	-11.4M	8.80M	500.M	LSB
BIT WGHT ERR-BITS 12	-500.M	40.2M	88.0M	500.M	LSB

NOTES:1.ZERO (0) IN LIMITS COLUMN MEANS NO LIMIT.IT CAN BE INTERPRETED AS A DASH (-).

TABLE 6.5. Device Type 01 Data at - 55°C.

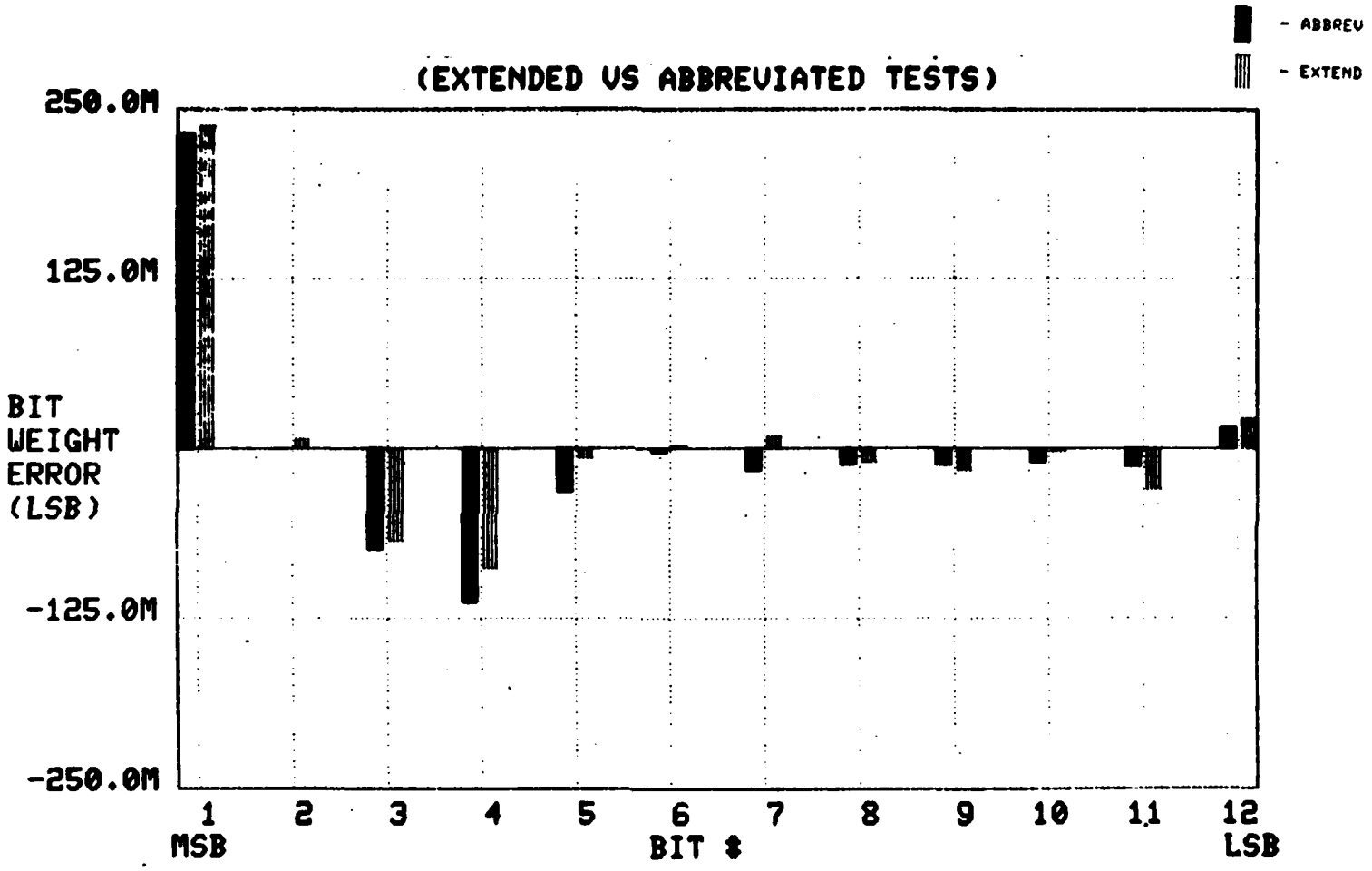
MANUFACTURER CODE: ; DEVICE TYPE: 582; TEMPERATURE: -55 DEG C ; 25 OCT 79 11:16:50

PARAMETER	LO-LIM	4310	4312	4313	4314	4315	5	10	80	81	85	HI-LIM	UNITS
SUM BIT ERROR(+)	-600.M	125.M	34.0M	42.8M	190.M	138.M	939.M	406.M	249.M	407.M	96.9M	600.M	LSB
SUM BIT ERROR(-)	-600.M	-165.M	-84.9M	-113.M	-215.M	-134.M	-987.M	-406.M	-276.M	-391.M	-159.M	600.M	LSB
SUM-ERROR(+)+ERROR(-)	-100.M	-40.2M	9.13M	-70.1M	-25.2M	4.39M	-47.6M	97.7U	-27.0M	15.8M	-61.9M	100.M	LSB
GAIN ERROR (TTL)	-25.0	-4.88	-811.M	510.M	-2.20	-514.M	-13.1M	13.3	6.06	5.80	9.79	25.0	MV
GAIN ERROR (CMOS)	-25.0	-5.21	-1.02	536.M	-2.17	-130.M	162.M	14.3	5.77	5.93	9.73	25.0	MV
GAIN ERROR DRIFT (TTL) C	-5.00	-494.M	465.M	1.71	1.31	828.M	-8.56	6.21	1.46	2.02	5.21	5.00	PPM/
BIPOLAR OFFSET ERROR	-20.0	-1.35	-3.40	-1.25	-5.11	-3.98	-2.36	-4.59	-1.56	-3.41	-3.47	20.0	MV
BPOE DRIFT C	-4.00	848.M	0.00	-326.M	-598.M	-346.M	754.M	0.00	-517.M	-134.M	211.M	4.00	PPM/
+PSS1 (TTL) [+10%]	-800.	-82.9	-118.	-99.0	-135.	-119.	-61.3	-133.	-51.7	-154.	-22.7	800.	UV
+PSS1 (TTL) [-10%]	-800.	-15.5	25.7	-31.2	-51.8	72.7	4.38	41.4	31.0	-14.9	-13.6	800.	UV
MJR CARRY ERR-BIT# 1	-900.M	96.1M	70.0M	51.1M	-286.M	121.M	1.04	469.M	535.M	766.M	-38.1M	900.M	LSB
MJR CARRY ERR-BIT# 2	-900.M	184.M	80.2M	126.M	-199.M	162.M	236.M	-186.M	245.M	220.M	71.3M	900.M	LSB
MJR CARRY ERR-BIT# 3	-900.M	-4.56M	-39.9M	-36.3M	-274.M	-31.9M	1.27	249.M	92.5M	263.M	136.M	900.M	LSB
MJR CARRY ERR-BIT# 4	-900.M	-127.M	40.1M	-8.57M	-252.M	-14.9M	569.M	-124.M	-40.8M	85.1M	-4.69M	900.M	LSB
MJR CARRY ERR-BIT# 5	-900.M	70.6M	-37.8M	134.M	162.M	55.3M	483.M	132.M	31.2M	13.7M	76.9M	900.M	LSB
MJR CARRY ERR-BIT# 6	-900.M	11.1M	-10.4M	14.9M	-40.1M	12.8M	30.8M	68.1M	-17.5M	13.7M	34.2M	900.M	LSB
MJR CARRY ERR-BIT# 7	-900.M	34.5M	-12.5M	44.7M	6.59M	31.9M	-265.M	32.4M	46.0M	-4.67M	58.4M	900.M	LSB
MJR CARRY ERR-BIT# 8	-900.M	30.2M	19.0M	-53.6U	2.34M	-10.6M	-10.8M	38.0M	14.2M	30.0M	36.1M	900.M	LSB
MJR CARRY ERR-BIT# 9	-900.M	519.U	10.6M	-53.6U	46.9M	21.3M	7.16M	11.7M	16.3M	19.8M	10.1M	900.M	LSB
MJR CARRY ERR-BIT# 10	-900.M	17.5M	16.9M	19.1M	23.6M	27.7M	10.7M	443.U	5.76M	-16.9M	-10.3M	900.M	LSB
MJR CARRY ERR-BIT# 11	-900.M	-18.6M	-14.6M	-27.8M	10.8M	-8.50M	-5.40M	-18.4M	-40.8M	-21.0M	-30.7M	900.M	LSB

TABLE 6.5. Device Type 01 Data at -55°C.

MANUFACTURER CODE: ; DEVICE TYPE: 862; TEMPERATURE: -55 DEG C ; 25 OCT '89 11:17:0

PARAMETER		LO-LIM	36	48	HI-LIM	UNITS
SUM BIT ERROR(+)		-500.M	285.M	261.M	500.M	LSB
SUM BIT ERROR(-)		-500.M	-286.M	-296.M	500.M	LSB
SUM-ERROR(+)+ERROR(-)		-100.M	-977.U	-35.2M	100.M	LSB
GAIN ERROR (TTL)		-25.0	8.42	6.67	25.0	MV
GAIN ERROR (CMOS)		-25.0	8.19	6.59	25.0	MV
GAIN ERROR DRIFT (TTL)		-5.00	6.11	2.02	5.00	PPM/C
BIPOLAR OFFSET ERROR		-20.0	-1.63	-2.32	20.0	MV
BPOE DRIFT		-4.00	295.M	497.M	4.00	PPM/C
+PSS1 (TTL) [+10%]		-800.	-100.	-131.	800.	UV
+PSS1 (TTL) [-10%]		-800.	57.3	-5.02	800.	UV
MJR CARRY ERR-BITS	1	-900.M	-278.M	562.M	900.M	LSB
MJR CARRY ERR-BITS	2	-900.M	46.0M	279.M	900.M	LSB
MJR CARRY ERR-BITS	3	-900.M	-26.2M	89.8M	900.M	LSB
MJR CARRY ERR-BITS	4	-900.M	-192.M	-118.M	900.M	LSB
MJR CARRY ERR-BITS	5	-900.M	83.2M	46.6M	900.M	LSB
MJR CARRY ERR-BITS	6	-900.M	48.0M	50.7M	900.M	LSB
MJR CARRY ERR-BITS	7	-900.M	51.9M	38.4M	900.M	LSB
MJR CARRY ERR-BITS	8	-900.M	20.7M	38.4M	900.M	LSB
MJR CARRY ERR-BITS	9	-900.M	-6.69M	-8.88M	900.M	LSB
MJR CARRY ERR-BITS	10	-900.M	8.95M	-6.82M	900.M	LSB
MJR CARRY ERR-BITS	11	-900.M	-51.6M	-19.2M	900.M	LSB



ABBREVIATED TEST

WORST CASE BIT ERROR (+)= 200.0MLSB @ 100000000011

WORST CASE BIT ERROR (-)= -262.0MLSB @ 011111111100

SUM-WORST CASE BIT ERRORS= -62.01MLSB

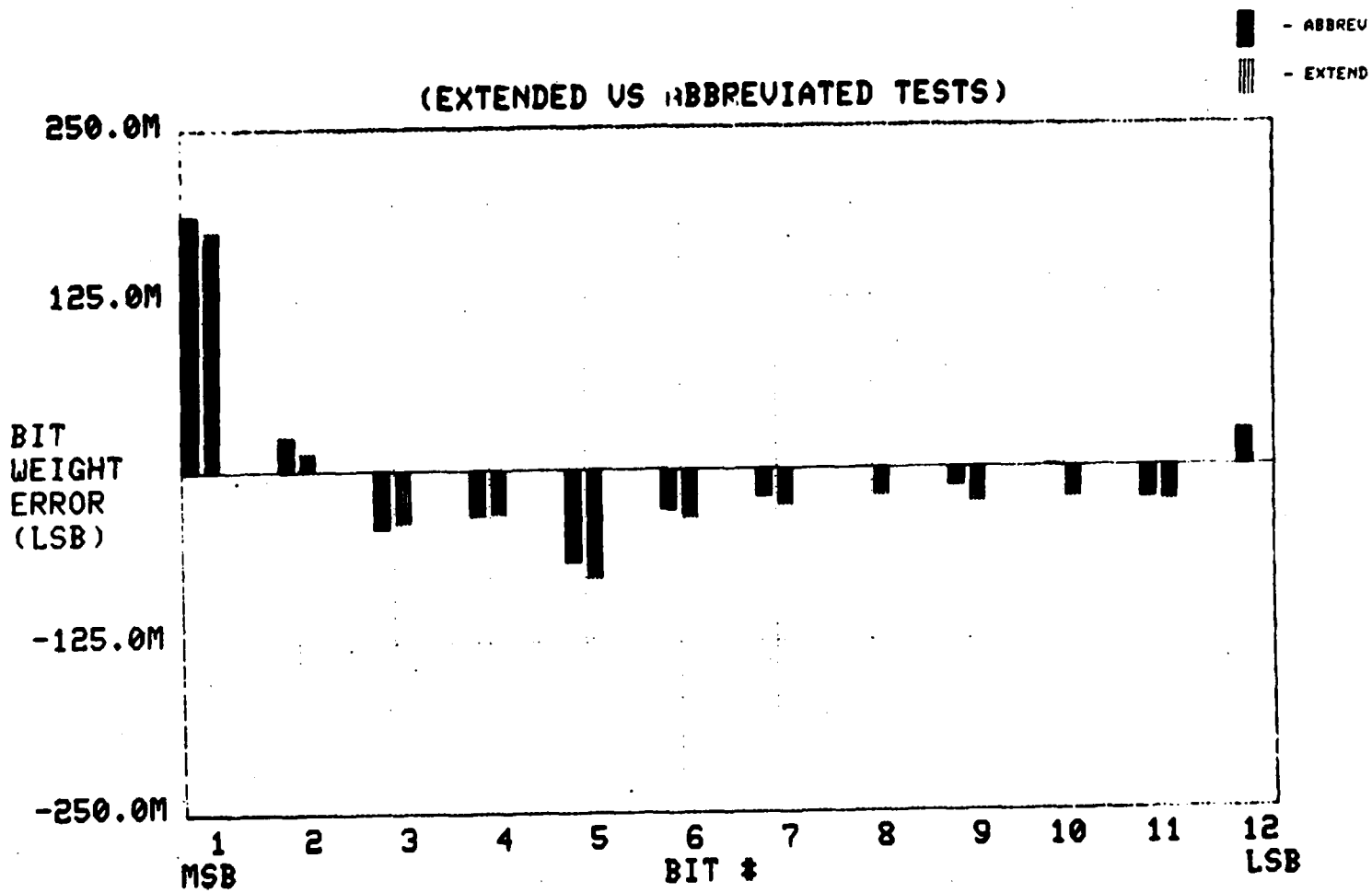
EXTENDED TEST

WORST CASE BIT ERROR (+)= 263.7MLSB @ 100001100011

WORST CASE BIT ERROR (-)= -257.2MLSB @ 011111011100

SUM-WORST CASE BIT ERRORS= 6.540MLSB

Figure 6.8. Bit Weight Error Display (+ 25°C).



ABBREVIATED TEST

WORST CASE BIT ERROR (+)= 196.5MLSB @ 101010000011

WORST CASE BIT ERROR (-)= -198.8MLSB @ 010101111100

SUM-WORST CASE BIT ERRORS= -8.344MLSB

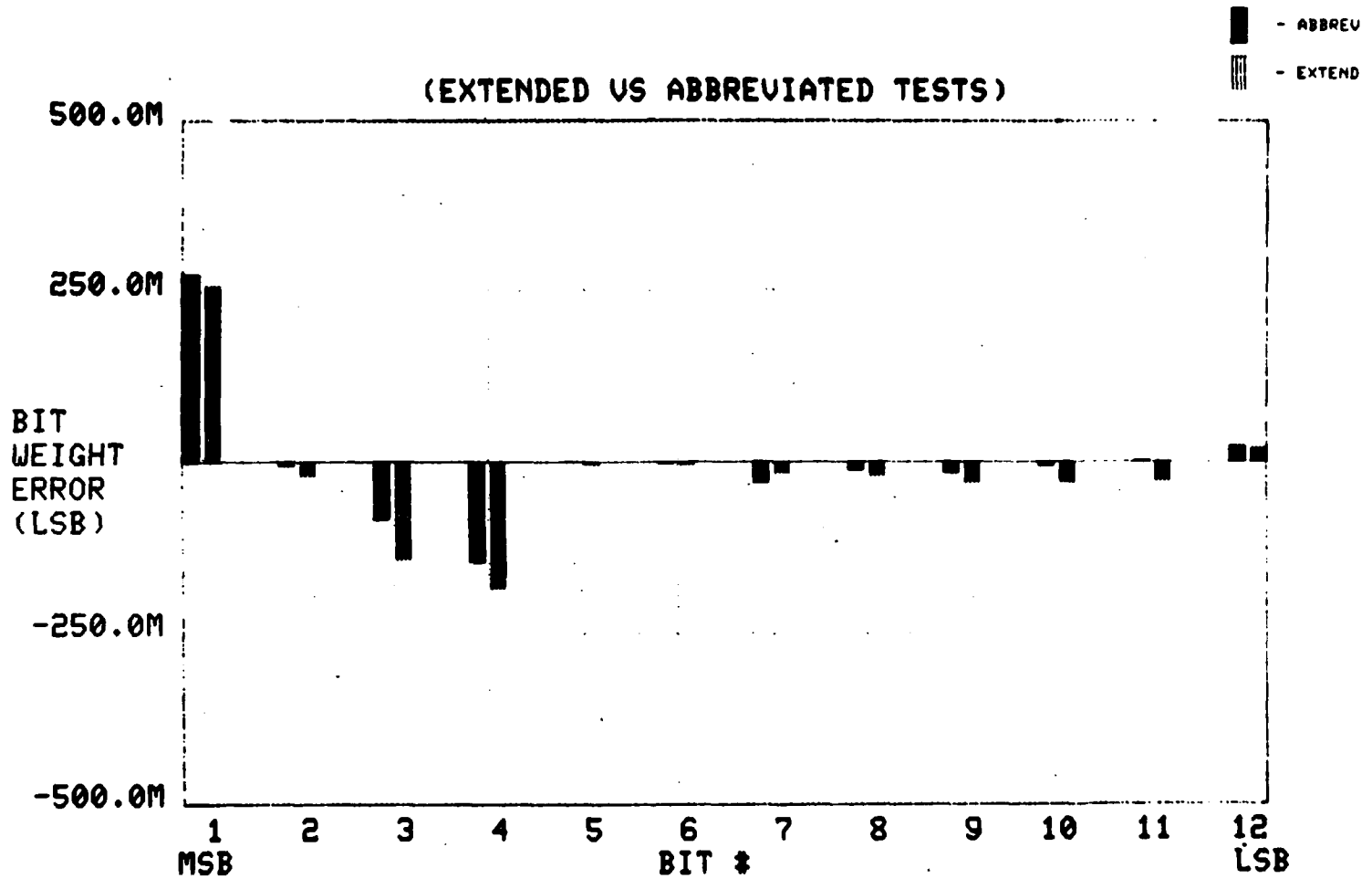
EXTENDED TEST

WORST CASE BIT ERROR (+)= 223.4MLSB @ 100000000011

WORST CASE BIT ERROR (-)= -228.1MLSB @ 011111111100

SUM-WORST CASE BIT ERRORS= -4.783MLSB

Figure 6.9. Bit Weight Error Display (+ 125°C).



ABBREVIATED TEST

WORST CASE BIT ERROR (+)= 261.1MLSB @ 110000010001

WORST CASE BIT ERROR (-)= -296.3MLSB @ 001111101110

SUM-WORST CASE BIT ERRORS= -35.16MLSB

EXTENDED TEST

WORST CASE BIT ERROR (+)= 288.1MLSB @ 100001100001

WORST CASE BIT ERROR (-)= -354.3MLSB @ 011110011110

SUM-WORST CASE BIT ERRORS= -66.17MLSB

Figure 6.10. Bit Weight Error Display (- 55°C).

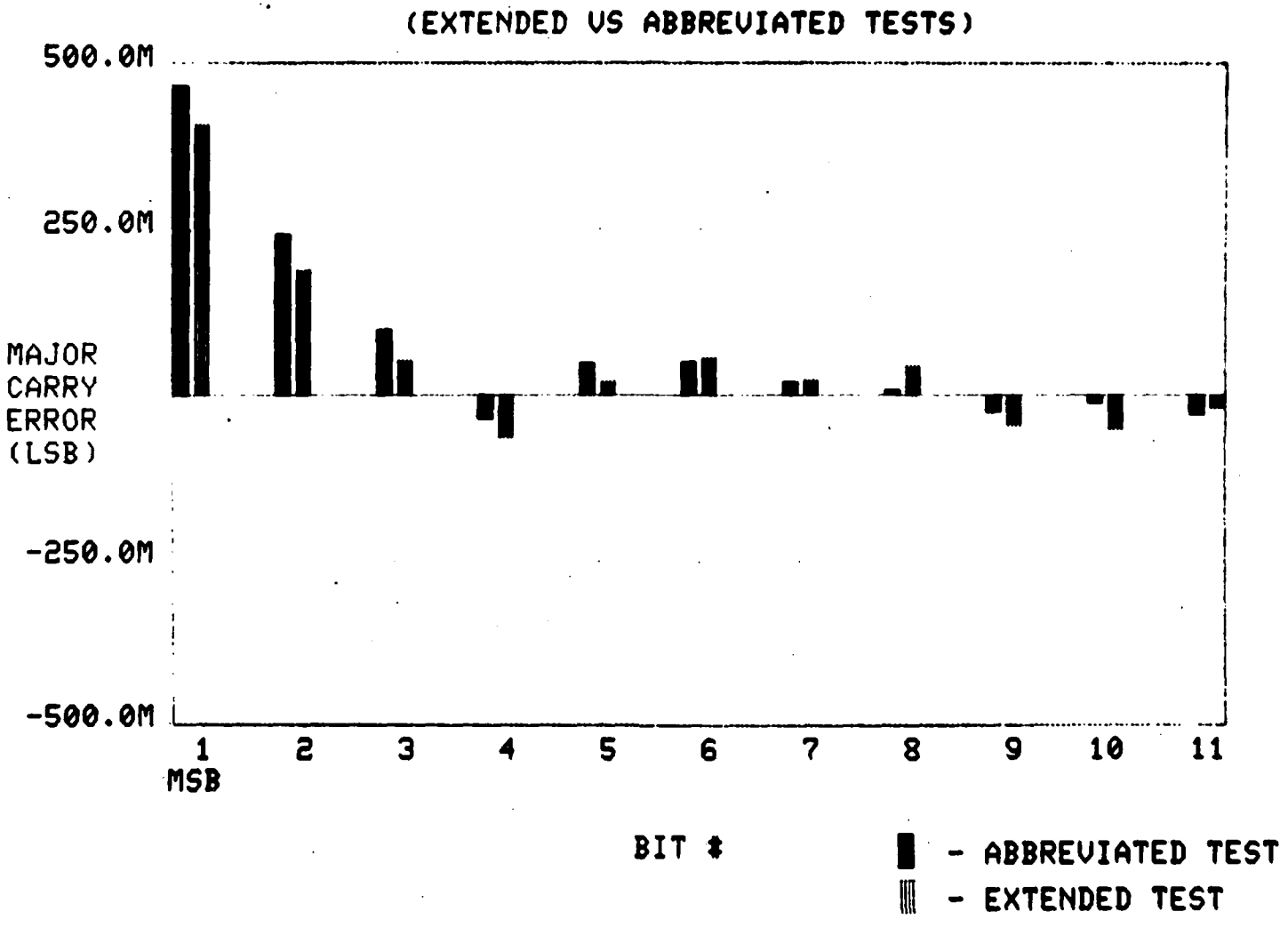


Figure 6.11. Major Carry Error Display (+ 25°C).

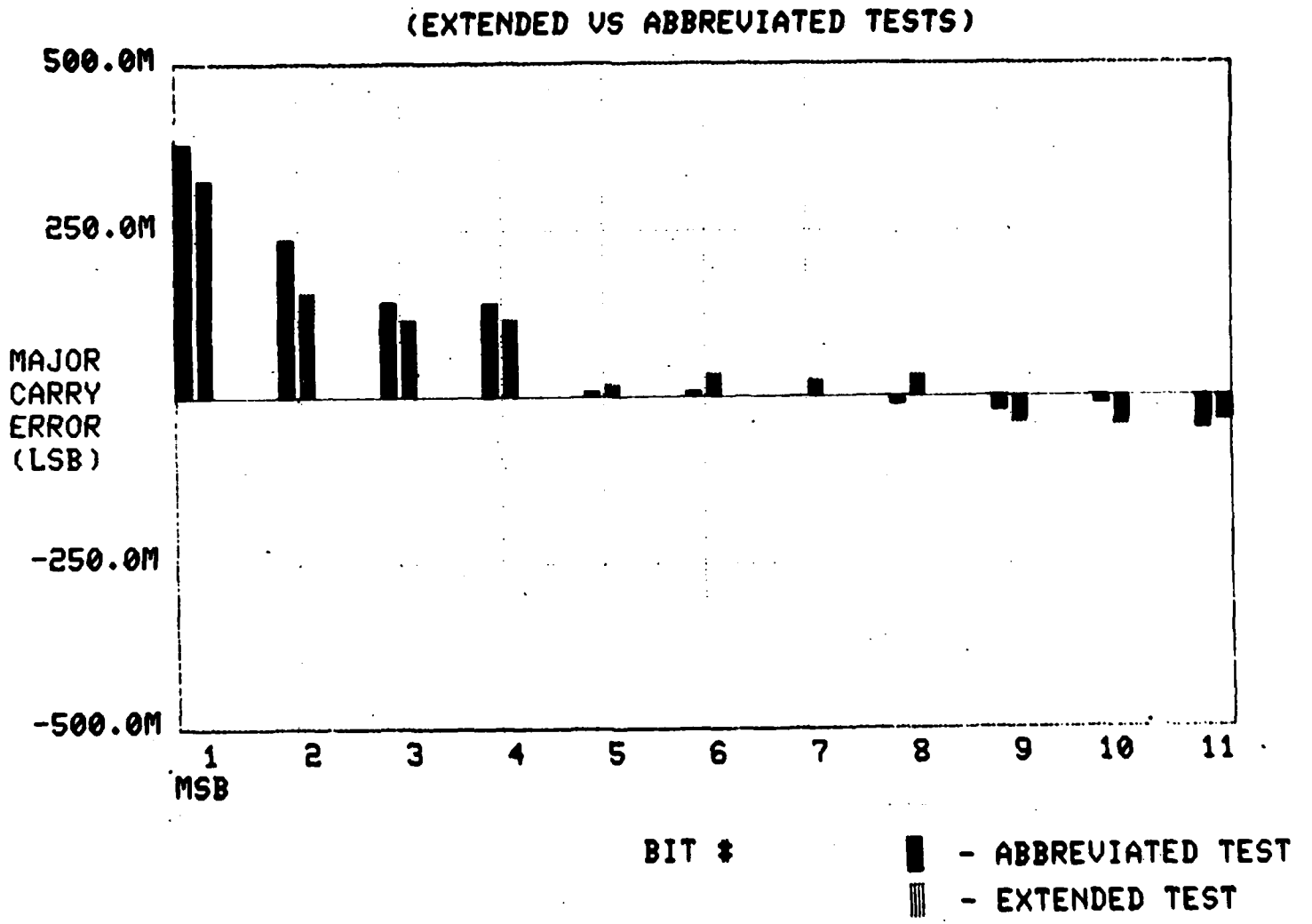


Figure 6.12. Major Carry Error Display (+ 125°C).

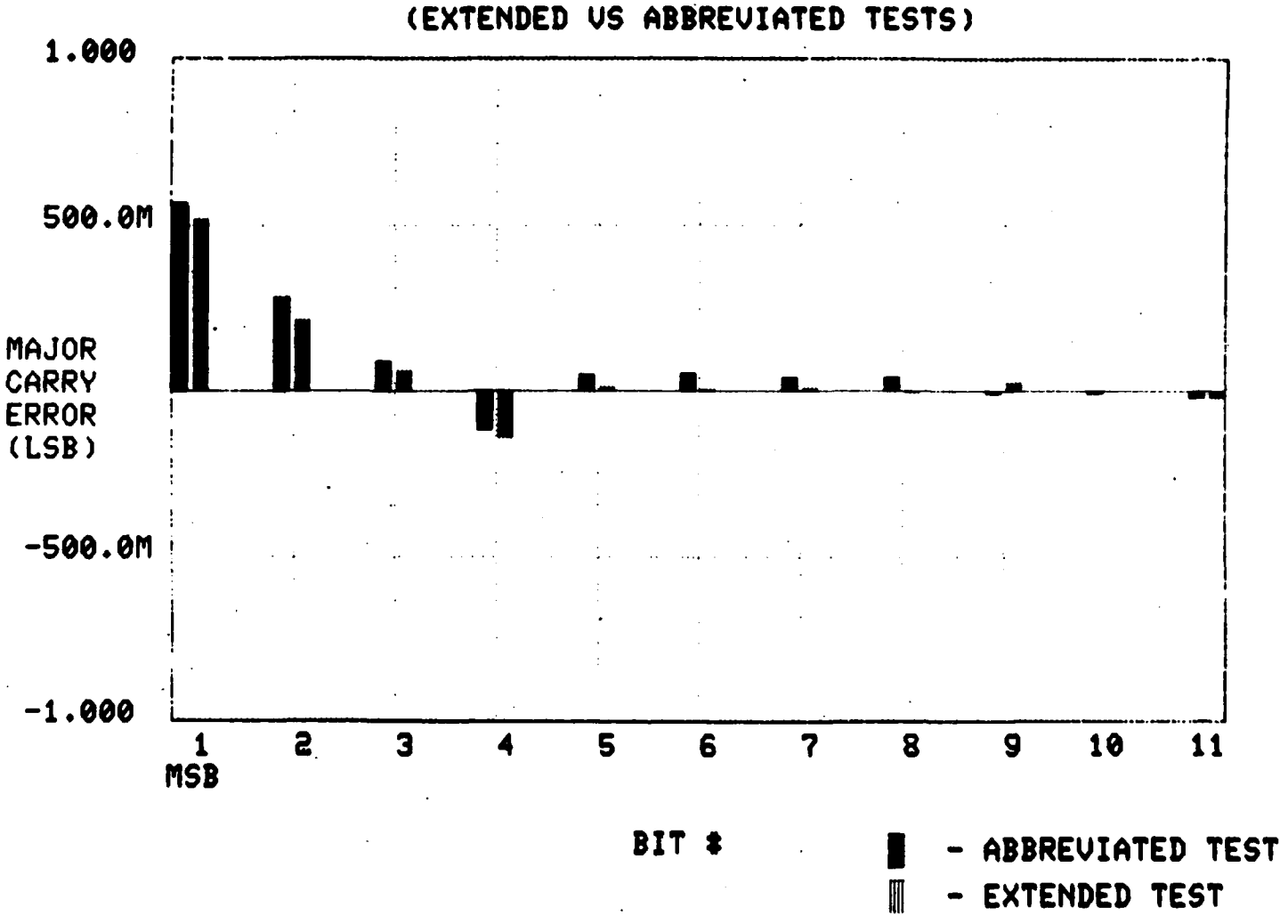


Figure 6.13. Major Carry Error Display (- 55°C).

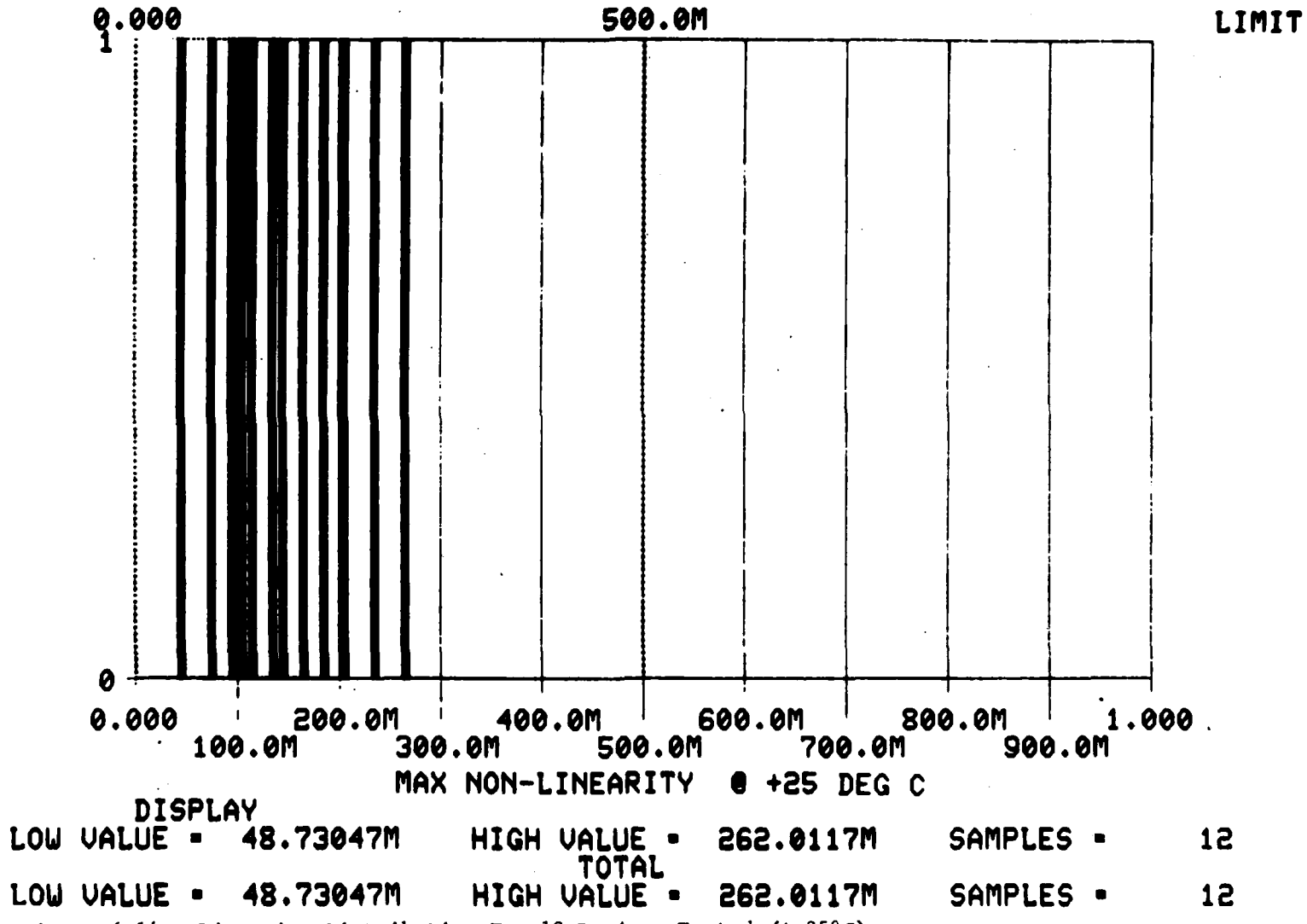


Figure 6.14. Linearity Distribution For 12 Devices Tested (+ 25°C).

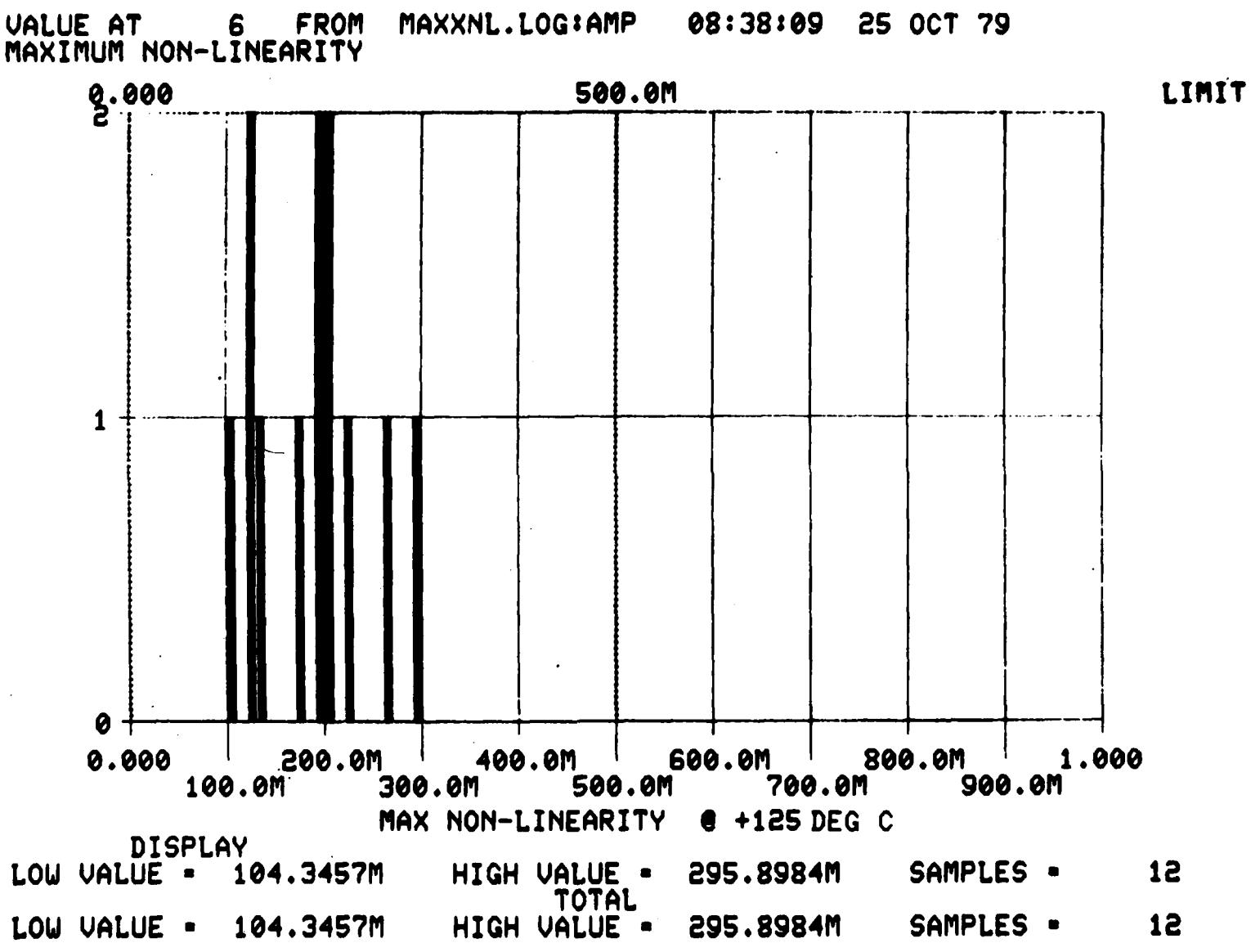


Figure 6.15. Linearity Distribution For 12 Devices Tested (+ 125°C).

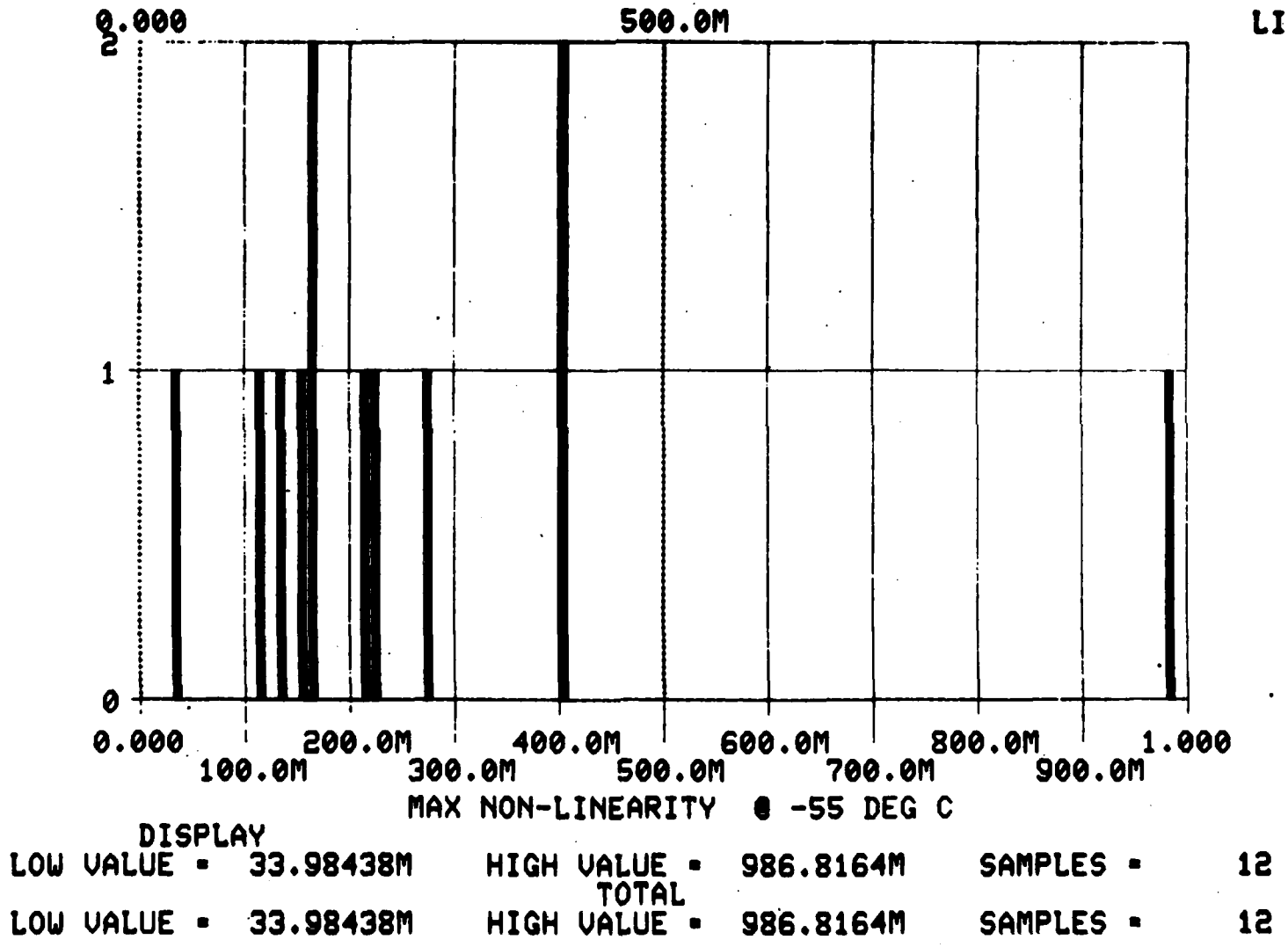


Figure 6.16. Linearity Distribution For 12 Devices Tested (- 55°C).

SECTION VII

PRECISION VOLTAGE REFERENCES

MIL-M-38510/124

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SECTION VII

CHARACTERIZATION OF PRECISION VOLTAGE REFERENCES

MIL-M-38510/124

7.1 Introduction and Background

As precision and accuracy of control systems increase, the need for a stable, precise voltage reference becomes apparent.

Precision voltage references are used in ratiometeric measurement syste as a reference against which all signal voltages can be compared, and especially for high accuracy data converters.
The two precision voltage references characterized for this slash sheet are the LM129A and the LM199A. These devices were selected by RADC, GEOS and members of the JC-41 Committee for characterization. The LM129A's and LM199A's were tested in test circuits devised to check each parameter at all of the specified temperatures.

7.2 Description of Device Types

The LM129A and LM199A precision voltage references each incorporate precision temperature compensated 6.9 volt zener references. The desig of the silicon chips uses a subsurface zener diode reference to reduce noise and long term stability. This construction shown in Figure 7.1, is accomplished using a relatively new technique known as ion implantation. The subsurface diode is buried below the chip surface and is therefore shielded from surface contamination and from ion inversion and noise problems common to regular zener breakdown diodes.

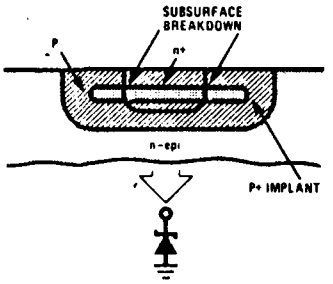

Figure 7.1. Subsurface Avalanche Zener Reference Diode

The voltage reference, additionally, contains circuitry to buffer the temperature compensated zener diode from current variations that accompany load current changes. The circuit for the LM199A precision voltage reference is shown in Figure 7.2.

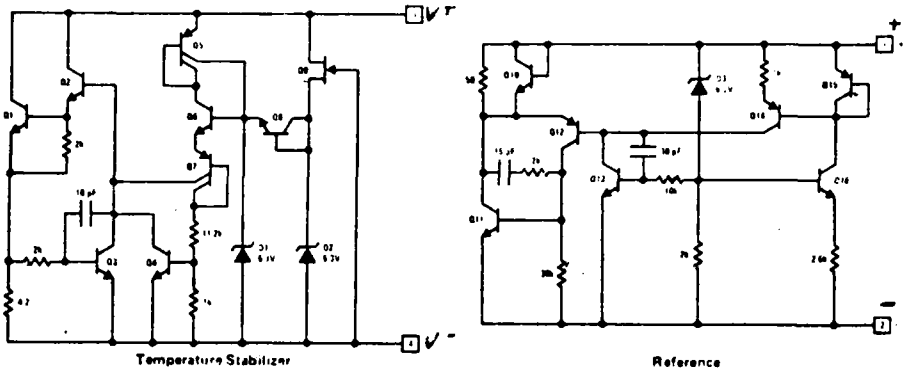

Figure 7.2. Schematic of LM199A Voltage Reference.

The precision reference circuit in this figure is comprised of two circuits on a single monolithic silicon chip. One circuit is a temperature stabilizer. The other circuit is the voltage reference. The voltage reference consists of a reference diode, D3, a current shunt circuit, Q10-Q13 and a current mirror, Q14-Q16. The reference diode is temperature compensated by adjusting the diode current for 0-T.C. This is accomplished by adjusting the 10K Ω resistor in the base of transistor Q13. Transistor Q13 serves to buffer any reference circuit current variations from the reference diode. For example, if the external load current suddenly decreases, the current through the external series resistance from the main supply will tend to decrease, and the voltage across the reference will tend to increase. The increased voltage across the reference will cause more current to flow in the base of transistor Q13. Since transistor Q13 supplies base current for the current shunt, the current shunt also conducts more current. By adjusting the 30 K Ω resistor in the collector of Q12, the increase in shunt current can be made approximately equal to the decrease in current supplied to the load. The only current change to the reference diode is due to the small change in transistor Q13 base current. Transistors Q14-Q16

form a current mirror and serve as a constant current, active load for transistor Q13. Because the reference diode is temperature compensated and because the current shunt handles the main variations in current, the reference circuit maintains a stable output voltage for large variations of both temperature and current. This stability is observed in both the LM129A and LM199A precision references.

The LM199A differs from the LM129A in that it also contains a temperature stabilizer circuit. The temperature stabilizer circuit operates from a separate supply voltage that can range from 9V to 40 V. The circuit draws current from this supply so as to maintain a constant chip temperature of approximately 85°C. As the chip ambient temperature decreases, the stabilizer draws more current from the supply and increases the power dissipation on the chip. Thus, the chip temperature tends to remain constant. A plot of average power dissipation versus temperature and supply voltage is shown in Figure 7.3. A thermal insulator housing is used with the LM199A to aid in the maintenance of a constant chip temperature. For temperatures above 85°C, the temperature stabilizer is no longer effective and the LM199A precision reference performance is essentially degraded to that of the LM129A.

7.3 Device Characterization

All evaluation and characterization of the precision voltage references was performed in bench test set-ups, and measurements were made on an HP3455 using Kelvin connections to the DUT. Breakdown voltage measurements were made at different current levels and at different temperatures, -55°C, 25°C, (85°C) and 125°C. Noise, Dynamic Impedance and Warm-up were performed at one current level at 25°C.

Figure 7.4 shows the test circuit used to measure breakdown voltage. The breakdown voltage measurements on the LM129A devices were made at current levels of 0.6 mA, 1.0 mA and 15 mA. For the LM199A, these measurements were made at current levels of 0.5 mA, 1.8 mA, 5 mA, 10.0 mA and 11.3 mA with the temperature stabilizer supply voltages set at 30 volts. Additional measurements were made with the temperature stabilizer supply voltages set at 9 volts and 40 volts.

The noise test circuit is shown in Figure 7.4. Measurements were made on a Tektronix model 7904 oscilloscope with a model 7A22 differential input preamplifier. The bandwidth on the preamp was adjusted for $10\ \text{Hz} \leq \text{BW} \leq 10\ \text{kHz}$ and peak-to-peak measurements were made on the oscilloscope.

The dynamic impedance test circuit is shown in Figure 7.5. Measurements were made using a 400 Hz signal source and a voltmeter with a 400 Hz narrow band filter. AC signal levels were low in order to insure small signal impedance measurements. Kelvin connections were used and contact was made 1/8" below the reference case.

The initial temperature stabilizer supply current was measured using a Tektronix model storage oscilloscope with a current probe. The peak current was recorded from the oscilloscope.

7.4 Test Results and Evaluation of Data

The data taken on these devices was analyzed to determine the average value and standard deviation. The results of this analysis are shown in Tables 7.1 through 7.15.

The tables show two columns for average value and two columns for standard deviation. The two columns to the extreme right of each table indicate the final average value and the final standard deviation value after the non-typical data is removed from the analysis. The other two columns for average value and standard deviation value are computed from all of the data measurements.

The data was obtained from 21 parts and 13 parts for the LM129A and the LM199A. Statistical analysis on these devices is inconclusive because of the small sample size, however, the characterization failed to uncover any major devices anomalies, and some of the measurements were out of the specified tolerance. Some of the data taken was strictly for characterization and provides data on conditions not specified by the vendor or recommended for the device slash sheet.

Tables 7.1 through 7.4 tabulate the analyzed, measured data taken on the LM129A. Measurements were made on the devices with supply currents of .6 mA, 1.0 mA and 15 mA. The reference voltage measurements were all well within the manufacturer's specified limits and a population hystogram of these voltages is shown in Figure 7.6 . The devices all had measured output voltages slightly below the nominal of 6.95 ± .25 volts. The mean value for I_1 = 1 mA was 6.8724 with a standard devication of .02 volts.

Data for the evaluation of temperature coefficient was obtained by measuring the output voltage at the various specified temperatures and determining the measurement differences in PPM/°C. The mean temperature coefficient for this current was - 0.3 PPM/°C with a standard deviation

of 3.1 PPM/°C for a temperature range from - 55°C to 25°C. The mean temperature coefficient over the temperature range from 25°C to 125°C was + 3.8 PPM/°C with a standard deviation of 2.8 PPM/°C. These numbers are well within the specification of ± 10 PPM/°C. For this characterization effort similar data was obtained for device currents of .5 mA and 15 mA. This data was used in the analysis of temperature coefficient change with current. The analysis shows that the data for T.C. change with current, over the temperature range from 25°C to 125°C, is greater than the vendor's "typical" specification. The mean value was determined as - 1.9 PPM/°C and the standard deviation was 1.3 PPM/°C, however, the parts received by OS were not screened for this parameter.

Tables 7.5 through 7.15 tabulate the analysis of the measured data for the LM199A. Data was taken to determine the power dissipation of the thermal stabilizer versus temperature. The results of this data are tabulated in Table 7.5 and are graphed on Figure 7.3 . The graph shows the linearity of the change in power dissipation versus temperature for zero current in the reference voltage circuit. From this information the average thermal resistance is calculated as

$$\theta = \frac{538.7 - 78.0}{85 + 55} = 3.29 \text{ mW/°C}$$

The vendor was contacted on this matter and confirmed that the figure should be 2 - 5 mV/°C. The vendor recommends that the thermal resistance should be nominally specified at 5 mW/°C. The total device power dissipation is the sum of the thermal stabilizer circuit power and the reference voltage circuit power. ($P_T = P_{TS} + P_R$). The graph in Figure 7.3 shows how the thermal stabilizer power dissipation is affected by the added power dissipation of the voltage reference.

Data taken for various reference voltage currents was taken with the thermal stabilizer supply voltage set to 30 volts. The reference voltage current values varied from .5 mA to 11.3 mA. Since the thermal stabilizer temperature is not regulated to the maximum temperature of 125°C, two temperature coefficient specifications are required. One T.C. tolerance of .5 PPM/°C covers the temperature range from -55°C to 85°C. The other tolerance of 10 PPM/°C covers the temperature range from 85°C to 125°C. Data presented in Tables 7.6 to 7.10 shows that T.C. range increases as the current through the reference voltage circuit increases. For currents of 5 mA and larger, the standard deviation of the temperature coefficients is larger than the 1 mA limit for a temperature range from 25°C to 85°C, however, these devices will be tested only at I_1 = 1 mA. The vendor was contacted and stated that this and other parameters can be screened for special applications.

Table 7.11 tabulates the results of the analyzed data for dynamic impedance, noise and T.C. changes with current. Noise measurements were made by determining the peak-to-peak value of the noise. The mean value of these measurements was 73.5 uV p-p. For broad-band white noise, (RMS value)= (peak-to-peak value)/6. Therefore, the mean RMS value is 12.25 uV, which is less than the manufacturer's specification. As previously described, the temperature coefficient increases with reference voltage current. The affects of this anomally on temperature coefficient change with current are shown in Table 7.11. The most significant tolerance variation occurs for a temperature range of 25°C to 85°C where the standard deviation is 1.3 PPM/°C.

Tables 7.12 through 7.15 provide additional data on the measurement of reference voltage, temperature coefficient and thermal stabilizer power dissipation. For these measurements the reference voltage current was set to 1.8 mA and 11.8 mA and the thermal stabilizer voltage was set to 9 volts and 40 volts. The data results were consistent with previous measurements and no anomalies were observed.

Table 7.16 tabulates the analysis of measured data for LM199A Thermal Stabilizer Initial current, Reference Voltage Warm-up Stability and Reference Voltage Temperature Cycling Hysteresis.

7.5 Conclusions and Recommendations

The data obtained for these analyses showed that the reference voltage devices met the specifications published by the manufacturer. Other parameters, not one hundred percent guaranteed by the manufacturer but recommended by the JC-41 Committee, were measured and the data was analyzed. Data taken on the temperature coefficient change with current showed that some devices had values much greater than the published typical value. The manufacturer states that this parameter can be guaranteed but the additional tests will add extra cost to the parts. It was decided not to recommend specification of this parameter.

Additional tests, such as, power off/on repeatibility, warm-up stability, and temperature cycling hysteresis have been checked. These parameters require extreme care in order to obtain reliable test data. The power off/on data was obtained as a consequence of the warm-up test data at time = 5 min. These data are shown in Table 7-16. OS does not recommend that the power off/on and warm-up test be a part of the slash sheet.

No major anomalies were uncovered during this characterization. A minor anomaly was observed in the measurement of temperature coefficient change with current. As the voltage reference current and temperature were increased simultaneously to their maximum, the T.C. change increased until it was 2-3 times the value at low current and temperature.

Table 7.17 lists the recommended parameters for these devices.

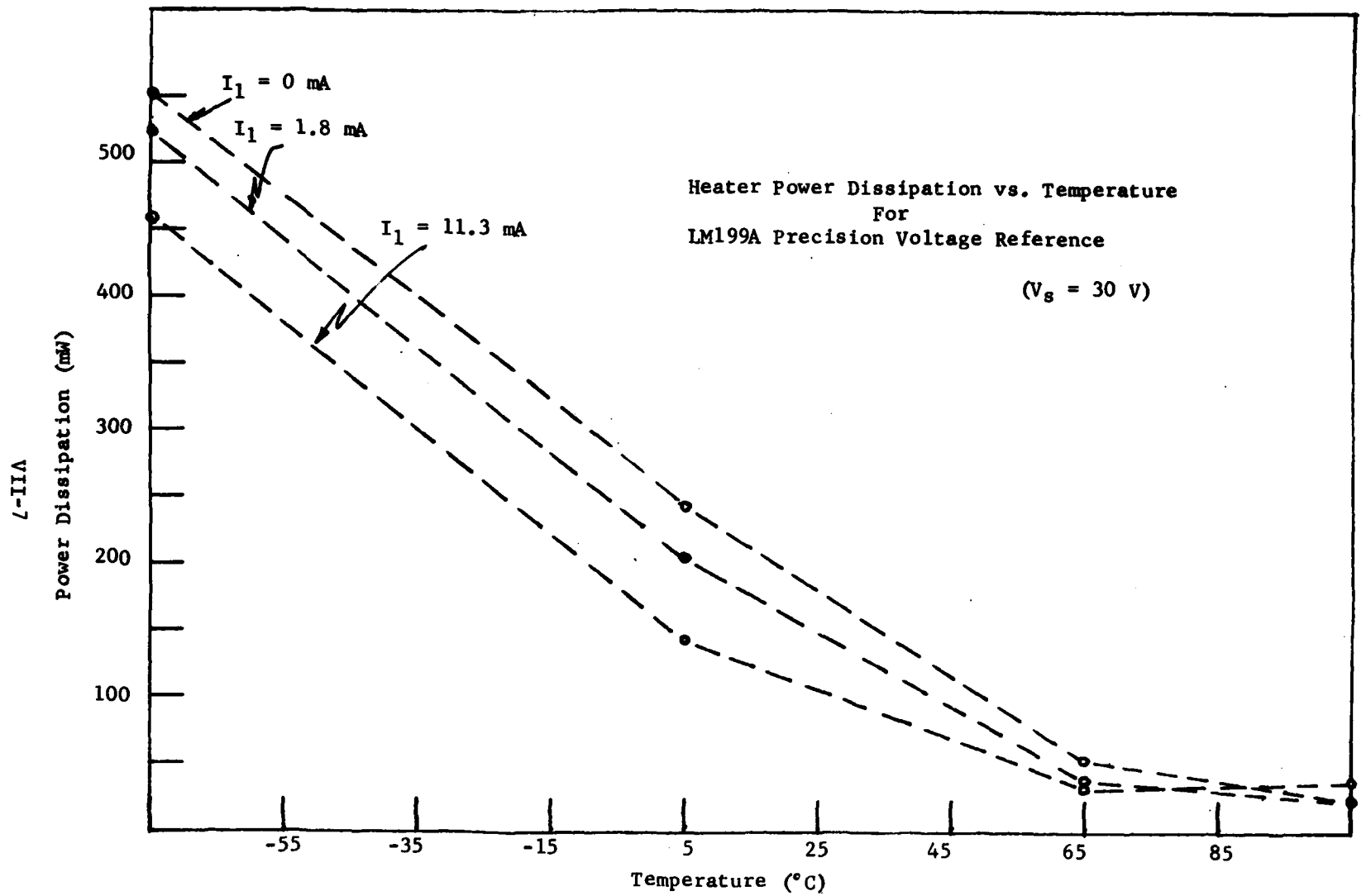

Figure 7.3. Heater power dissipation versus temperature for different reference currents.

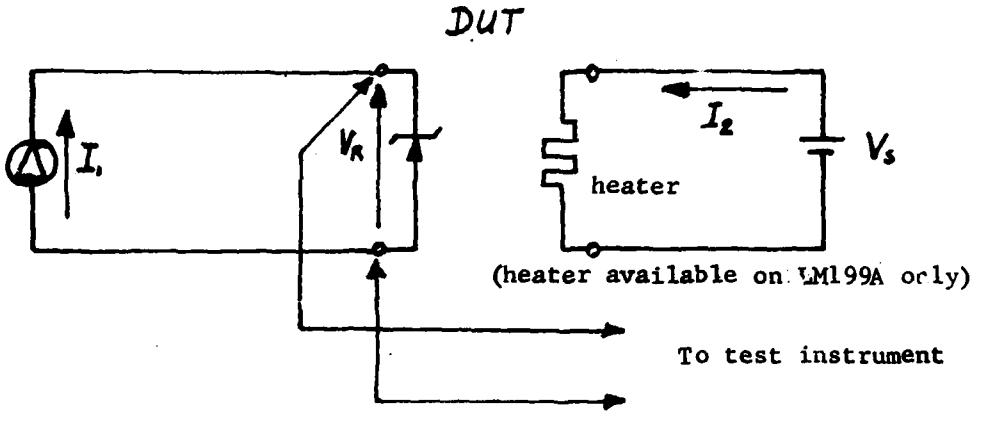

Figure 7.4. Reference voltage and noise test circuit.

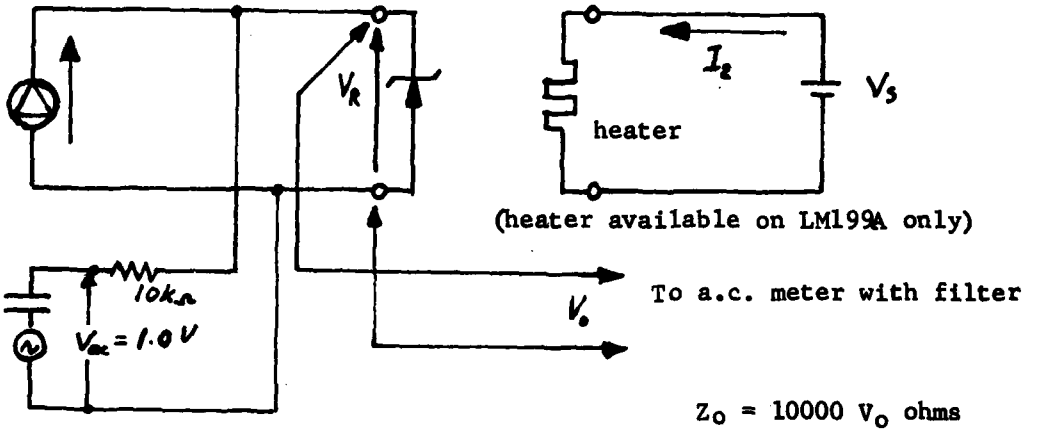

Figure 7.5. Dynamic impedance test circuit.

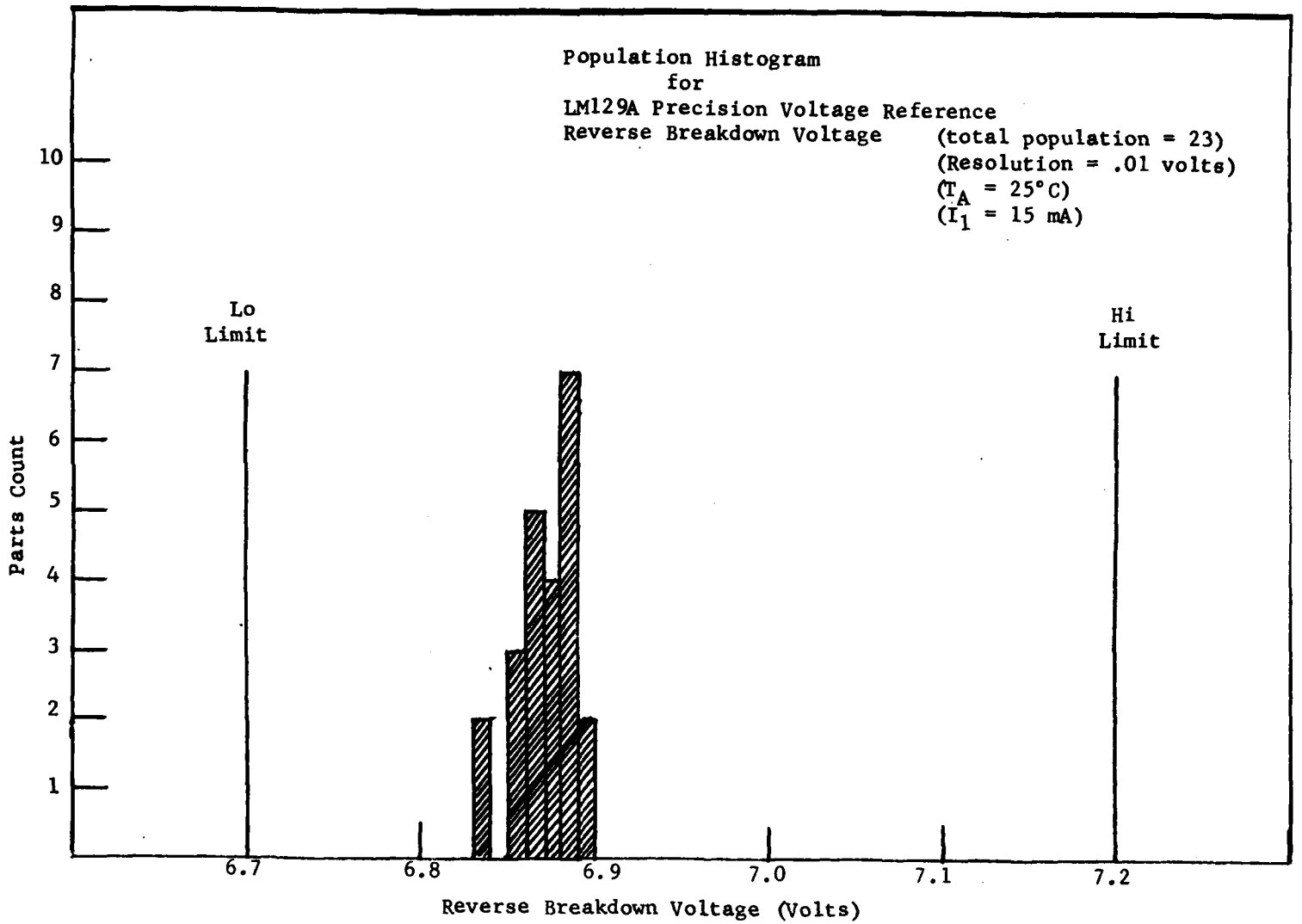

Figure 7.6. Population histogram for LM129A precision voltage reference.

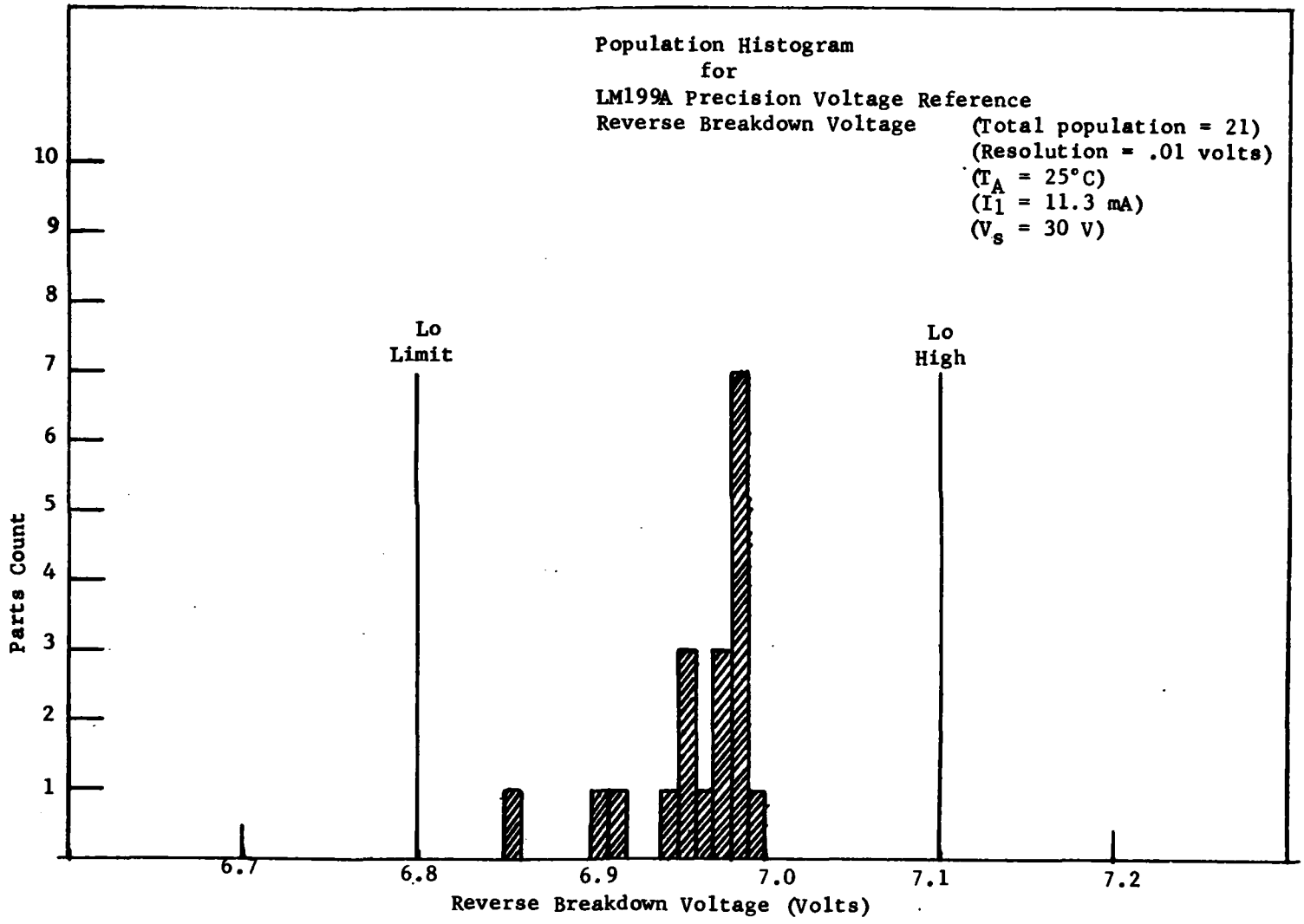

Figure 7.7. Population histogram for LM199A precision voltage reference.

Table 7.1. Summary of Measurements at I_1 = 0.6 mA[1/] (LM129A)

Parameter	Overall Average[2/]	Overall σ	Parameter values not included in Final Average and Final σ, and associated devices	Final Average[2/]	Final σ
Reference Voltage at 25°C (volts)	High = +6.8922 +6.8718 Low = +6.8360	.02	None Manufacturer's spec = 6.95 ± .25 V	High = +6.8922 +6.8718 Low = +6.8360	.02
T_c over range $-55°C \leq T_A \leq 25°C$ (PPM/°C)	High = +4.2 -0.5 Low = -6.1	3.0	None Manufacturer's spec = ± 10 PPM/°C	High = +4.2 -0.5 Low = -6.1	3.0
T_c over range $25°C \leq T_A \leq 25°C$ (PPM/°C)	High = +8.0 + 3.8 Low = -7.7	3.6	None Manufacturer's spec = ±10PPM/°C	High = +8.0 +3.8 Low = -7.7	3.6

Notes: 1. I_1 = current through voltage reference.

2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.2. Summary of Measurements at I_1 = 1 mA[1/] (LM129A)

Parameter	Overall[2/] Voltage	Overall σ	Parameter values not included in Final Average and Final σ, and associated device #	Final[2/] Average	Final σ
Reference Voltage at 25°C (volts)	High = +6.8927 +6.8724 Low = +6.8365	.02	None Manufacturer's spec = 6.95 ± .25V	High = +6.8927 +6.8724 Low = +6.8365	.02
T_C over range $-55°C \leq T_A \leq 25°C$ (PPM/°C)	High = +4.2 -0.3 Low = -6.8	3.1	None Manufacturer's spec = ± 10 PPM/°C	High = +4.2 -0.3 Low = -6.8	3.1
T_C over range $25°C \leq T_A \leq 125°C$	High = +7.4 +3.8 Low = -2.5	2.8	None Manufacturer's spec = ± 10 PPM/°C	High = +7.2 +3.8 Low = -2.5	2.8

Notes: 1. I_1 = current through voltage reference.

2. *Each block in the average column indicates the high value, the* computed average value and the low value for the specified parameter.

Table 7.3. Summary of Measurements at I_1 = 15 mA[1/] (LM129A)

Parameter	Overall Average[2/]	Overall σ	Parameter values not included in Final Average and Final σ, and associated device #	Final Average[2/]	Final σ
Reference Voltage at 25°C (volts)	High = +6.9036 +6.8852 Low = +6.8455	.02	None Manufacturer's spec = 6.95 ± .25V	High = +6.9036 +6.8852 Low = +6.8455	.02
T_c over range $-55°C \leq T_A \leq 25°C$ (PPM/°C)	High = +2.3 -1.8 Low = -7.3	2.8	None Manufacturer's spec = ± 10 PPM/°C	High = +2.3 -1.8 Low = -7.3	2.8
T_c over range $25°C \leq T_A \leq 125°C$ (PPM/°C)	High = +8.4 +4.5 Low = -1.2	2.7	None Manufacturer's spec = ± 10 PPM/°C	High = +8.4 +4.5 Low = -1.2	2.7

Notes: 1. I_1 = current through voltage reference.

2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.4. Summary of Measurements (LM129A)

Parameter	2/ Overall Average	Overall σ	Parameter values not included in Final Average and Final σ, and associated device #	2/ Final Average	Final σ
P-P Noise (uV)	69.8	4.9	None Manufacturer's spec = 20 (RMS max)	69.8	4.9
Change in reverse breakdown temperature coefficient with current 1 mA $\leq I_1 \leq$ 15 mA 1/ -55°C $\leq T_A \leq$ 25°C	High = +2.1 +0.8 Low = -1.2	0.8	None Manufacturer's spec = ± 1 PPM/°C ($T_{typical}$)	High = +2.1 +0.8 Low = -1.2	0.8
Change in reverse breakdown temperature coefficient 1 mA $\leq I_1 \leq$ 15 mA 1/ 25°C $\leq T_A \leq$ 125°C	High = +0.6 -1.9 Low = -5.2	1.3	None Manufacturer's spec = ± 1 PPM/°C ($T_{typical}$)	High = +0.6 -1.9 Low = -5.2	1.3
Dynamic Impedance (ohms)	.74	.24	None Manufacturer's spec = 1 Ω	.74	.24

Notes: 1. I_1 = current through voltage reference.
2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.5. Summary of Measurements at I_1 = 0 mA; V_s = 30 V[1/] .(LM199A)

Parameter	Overall Average[2/]	Overall σ	Parameter values not included in Final Average and Final σ, and associated device #	Final Average[2/]	Final σ
Reference Voltage at 25°C (volts)	-	-	-	-	-
T_C over range -55°C ≤ T_A ≤ 25°C (PPM/°C)	-	-	-	-	-
T_C over range 25°C ≤ T_A ≤ 85°C (PPM/°C)	-	-	-	-	-
T_C over range 85°C ≤ T_A ≤ 125°C (PPM/°C)	-	-	-	-	-
Heater Power dissipation at T_A = -55°C (mW)	High = 578.3 538.7 Low = 512.4	21.1	None	High = 579.3 538.7 Low = 512.4	21.1
Heater Power dissipation at T_A = 25°C (mW)	High = 252.6 229.4 Low = 213.3	13.0	None	High = 252.6 229.4 Low = 213.3	13.0
Heater Power dissipation at T_A = 85°C (mW)	High = 78.0 52.8 Low = 28.5	18.1	None	High = 78.0 52.8 Low = 28.5	18.1
Heater Power dissipation at T_A = 125°C (mW)	High = 25.5 22.7 Low = 20.2	1.7	None	High = 25.5 22.7 Low = 20.2	1.7

Notes: 1. I_1 = current through voltage reference.
V_s = temperature stabilizer voltage.

2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.6. Summary of Measurements at I_1 = .5 mA; V_s = 30 V[1/] (LM199A)

Parameter	Overall Average[2/]	Overall σ	Parameter values not included in Final Average and Final σ, and associated device #	Final Average[2/]	Final σ
Reference Voltage at 25°C (volts)	High = +6.9899 +6.9582 Low = +6.9025	.03	None Manufacturer's spec = +6.95 ± .15	High = +6.9899 +6.9582 Low = +6.9025	.03
T_c over range $-55°C \leq T_A \leq 25°C$ (PPM/°C)	High = 0.0 -.31 Low = -.54	.17	None Manufacturer's spec = .5	High = 0.0 -.31 Low = -.54	.17
T_c over range $25°C \leq T_A \leq 85°C$ (PPM/°C)	High = + .24 -.50 Low = -.95	.34	None Manufacturer's spec = .5	High = +.24 -.50 Low = -.95	.34
T_c over range $85°C \leq T_A \leq 125°C$ (PPM/°C)	High = +7.5 +1.7 Low = -9.4	5.0	None Manufacturer's spec = 10	High = +7.5 +1.7 Low = -9.4	5.0

Notes: 1. I_1 = current through voltage reference
V_s = temperature stabilizer voltage
2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.7. Summary of Measurements at I_1 = 1.8 mA; V_S = 30 V[1/] (LM199A)

Parameter	Overall Average[2/]	Overall σ	Parameter values not included in Final Average and Final σ, and associated device #	Final Average[2/]	Final σ
Reference Voltage at 25°C (volts)	High = +6.99376 +6.95932 Low = +6.84427	.03	None Manufacturer's spec = 6.95 ± .15 V	High = +6.99376 +6.95932 Low = +6.84427	.03
T_C over range $-55°C \leq T_A \leq 25°C$ (PPM/°C)	High = +.72 -0.4 Low = -10.0	2.4	-3.2, device #12 -10.0, device #15 Manufacturer's spec = 5	High = +.72 +0.3 Low = 0.0	0.2
T_C over range $25°C \leq T_A \leq 85°C$ (PPM/°C)	High = +0.7 +.32 Low = 0.0	0.3	None Manufacturer's spec = 5	High = +0.7 +.32 Low = 0.0	0.3
T_C over range $85°C \leq T_A \leq 125°C$ (PPM/°C)	High = +9.3 +0.6 Low = -11.3	6.6	None Manufacturer's spec = 10	High = +9.3 +0.6 Low = -11.3	6.6
Heater Power dissipation at T_A = -55°C (mW)	High = 567.0 522.0 Low = 491.7	22.3	None	High = 567.0 522.0 Low = 491.7	22.3
Heater Power dissipation at T_A = 25°C (mW)	High = 240.9 213.6 Low = 192.0	14.8	None	High = 240.9 213.6 Low = 192.0	14.8
Heater Power dissipation at T_A = 85°C (mW)	High = 65.7 41.3 Low = 20.7	18.0	None	High = 65.7 41.3 Low = 20.7	18.0
Heater Power dissipation at T_A = 125°C (mW)	High = 25.2 22.5 Low = 20.0	1.7	None	High = 25.2 22.5 Low = 20.0	1.7

Notes: 1. I_1 = current through voltage reference.
V_S = temperature stabilizer voltage.

2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.8. Summary of Measurements at I_1 = 5 mA; V_s = 30 V [1/] (LM199A)

Parameter	[2/] Overall Average	Overall	Parameter values not included in Final Average and Final σ, and associated device #	[2/] Final Average	Final
Reference Voltage at 25°C (volts)	High = +6.9929 +6.9613 Low = +6.9055	.03	None Manufacturer's spec =	High = +6.9929 +6.9613 Low = +6.9055	.03
T_C over range $-55°C \leq T_A \leq 25°C$ (PPM/°C)	High = +.54 .03 Low = -.54	.25	None Manufacturer's spec = .5	High = +.54 .03 Low = -.54	.25
T_C over range $25°C \leq T_A \leq 85°C$ (PPM/°C)	High = +1.9 +.28 Low = -.72	.80	None Manufacturer's spec = .5	High = +1.9 +.28 Low = -.72	.80
T_C = over range $85°C \leq T_A \leq 125°C$ (PPM/°C)	High = +9.7 +3.0 Low = -8.7	5.5	None Manufacturer's spec = 10 . . .	High = +9.7 +3.0 Low = -8.7	5.5

Notes: 1. I_1 = current through voltage reference
V_s = temperature stabilizer voltage

2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.9. Summary of Measurements at I_1 = 10 mA ; V_s = 30 V[1/] (LM199A)

Parameter	[2/] Overall Average	Overall	Parameter values not included in Final Average and Final σ, and associated device #	[2/] Final Average	Final
Reference Voltage at 25°C (volts)	High = +6.9955 +6.9640 Low = +6.9085	.03	None Manufacturer's spec = +6.95 ± .15	High = +6.9955 +6.9640 Low = +6.9085	.03
T_C over range $-55°C \leq T_A \leq 25°C$ (PPM/°C)	High = +.72 +.36 Low = -.18	.23	None Manufacturer's spec = .5	High = +.72 +.36 Low = -.18	.23
T_C over range $25°C \leq T_A \leq 85°C$ (PPM/°C)	High = +1.9 +.91 Low = -1.2	.90	None Manufacturer's spec = .5	High = +1.9 +.91 Low = -1.2	.90
T_C over range $85°C \leq T_A \leq 125°C$ (PPM/°C)	High = +10.0 +2.8 Low = -10.5	6.4	None Manufacturer's spec = 10	High = +10.0 +2.8 Low = -10.5	6.4

Notes: 1. I_1 = current through voltage reference
V_s = temperature stabilizer voltage
2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.10. Summary of Measurements at I_1 = 11.3 mA; V_s = 30 V [1/] (LM199A)

Parameter	[2/] Overall Average	Overall σ	Parameter values not included in Final Average and Final σ, and associated device #	[2/] Final Average	Final σ
Reference Voltage at 25°C (volts)	High = +6.99934 +6.96484 Low = +6.85108	0.3	None Manufacturer's spec = 6.95 ± .15 V	High = +6.99934 +6.96484 Low = +6.85108	.03
T_c over range $-55°C \leq T_A \leq 25°C$ (PPM/°C)	High = +9.5 +0.9 Low = -4.3	2.4	-4.3, device #12 +9.5, device #13	High = +1.6 +0.7 Low = -.36	0.4
T_c over range $25°C \leq T_A \leq 85°C$ (PPM/°C)	High = +4.8 +2.5 Low = -0.7	1.5	+4.8, device #5 +3.6, device #17	High = +3.3 +2.2 Low = -0.7	1.4
T_c over range $85°C \leq T_A \leq 125°C$ (PPM/°C)	High = +7.3 -1.0 Low = -15.7	5.5	-15.7 device #1	High = +7.3 +.05 Low = -7.6	4.1
Heater Power dissipation at T_A = -55°C (mW)	High = 501.9 458.4 Low = 425.7	24.2	None	High = 501.9 458.4 Low = 425.7	24.4
Heater Power dissipation at T_A = 25°C (mW)	High = 174.6 146.8 Low = 121.8	14.9	None	High = 174.6 146.8 Low = 121.8	14.9
Heater Power dissipation at T_A = 85°C	High = 42.9 32.8 Low = 23.4	6.2	None	High = 42.9 32.8 Low = 23.4	6.2
Heater Power dissipation at T_A = 125°C (mW)	High = 51.1 41.7 Low = 32.3	6.1	None	High = 51.1 41.7 Low = 32.3	6.1

Notes: 1. I_1 = current through voltage reference.
V_s = temperature stabilizer voltage.

2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.11. Summary of Measurements (LM199A)

Parameter	1/ Overall Average	Overall σ	Parameter values not included in Final Average and Final σ, and associated device #	1/ Final Average	Final σ
Dynamic Impedance (ohms)	High = .83 .66 Low = .3	.12	None Manufacturer's spec = 1 (max)	High = .83 .66 Low = .3	.12
Peak to Peak Noise (uV)	High = 80 73.5 Low = 50	6.9	None Manufacturer's spec = 20 (RMS max)	High = 80 73.5 Low = 50	6.9
Change in reverse breakdown temperature coefficient with current $1.8mA \leq I_1 \leq 11.3mA$ $-55°C \leq T_A \leq 25°C$	High = +10.7 +1.4 Low = -1.1	3.1	+9.1, device #14 +10.7, device #16	High = +1.1 +0.3 Low = -1.1	0.5
Change in reverse breakdown temperature coefficient with current $1.8mA \leq I_1 \leq 11.3mA$ $25°C \leq T_A \leq 85°C$	High = +4.8 +2.2 Low = -0.7	1.4	+4.8, device #17	High = +3.6 +2.0 Low = -0.7	1.3
Change in reverse breakdown temperature coefficient with current $1.8mA \leq I_1 \leq 11.3mA$ $85°C \leq T_A \leq 125°C$	High = +8.6 -1.7 Low = -4.5	3.4	None	High = +8.6 -1.7 Low = -4.5	3.4

Note: 1. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.12. Summary of Measurements at I_1 = 1.8 mA ; V_s = 9 V[1/] (LM199A)

Parameter	Overall Average[2/]	Overall σ	Parameter values not included in Final Average and Final σ, and associated device #	Final Average[2/]	Final σ
Reference Voltage at 25°C (volts)	High = +6.99343 +6.95897 Low = +6.84392	.03	None Manufacturer's spec = 6.95 ± .15 V	High = +6.93343 +6.95897 Low = +6.84392	.03
T_C over range -55°C ≤ T_A ≤ 25°C (PPM/°C)	High = +1.6 +0.2 Low = -16.3	3.9	-16.3, device #15	High = +1.6 +1.2 Low = +.72	0.3
T_C over range 25°C ≤ T_A ≤ 85°C (PPM/°C)	High = +1.4 +1.1 Low = +0.5	0.3	None	High = +1.4 +1.1 Low = +0.5	0.3
T_C over range 85°C ≤ T_A ≤ 125°C (PPM/°C)	High = +10.0 -3.0 Low = -63.0	17.1	-19.0, device #1 -63.0, device #19	High = +10.0 +2.4 Low = -9.4	5.6
Heater Power dissipation at T_A = -55°C (mW)	High = 569.7 521.6 Low = 476.1	27.1	None	High = 569.7 521.6 Low = 476.1	27.1
Heater Power dissipation at T_A = 25°C (mW)	High = 243.0 214.6 Low = 190.8	15.2	None	High = 243.0 214.6 Low = 190.8	15.2
Heater Power dissipation at T_A = 85°C (mW)	High = 67.2 41.6 Low = 14.4	19.1	None	High = 67.2 41.6 Low = 14.4	19.1
Heater Power dissipation at T_A = 125°C (mW)	High = 7.2 6.4 Low = 5.5	0.6	None	High = 7.2 6.4 Low = 5.5	0.6

Notes: 1. I_1 = current through voltage reference.
V_s = temperature stabilizer voltage.

2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.13. Summary of Measurements at I_1 = 11.3 mA ; V_s = 9 V[1/] (LM199A)

Parameter	[2/] Overall Average	Overall σ	Parameter values not included in Final Average and Final σ, and associated device #	[2/] Final Average	Final σ
Reference Voltage at 25°C (volts)	High = +6.99912 +6.96457 Low = +6.85086	.03	None Manufacturer's spec = 6.95 ± .15 V	High = +6.99912 +6.96457 Low = +6.85086	.03
T_C over range -55°C ≤ T_A ≤ 25°C (PPM/°C)	High = +1.8 +1.5 Low = +.54	0.3	None	High = +1.8 +1.5 Low = +.54	0.3
T_C over range 25°C ≤ T_A ≤ 85°C (PPM/°C)	High = +5.5 +2.6 Low = +.5	1.3	+4.1, device #5 +5.5, device #17	High = +3.4 +2.3 Low = +.5	1.0
T_C over range 85°C ≤ T_A ≤ 125°C (PPM/°C)	High = +148.7 +8.8 Low = -28.5	38.6	-28.5, device #1 +148.7, device #16	High = +11.4 +0.9 Low = -13.7	7.2
Heater Power dissipation at T_A = -55°C (mW)	High = 504.0 457.6 Low = 421.2	24.5	None	High = 504.0 457.6 Low = 421.2	24.5
Heater Power dissipation at T_A = 25°C (mW)	High = 179.8 150.4 Low = 124.6	15.7	None	High = 179.8 150.4 Low = 124.6	15.7
Heater Power dissipation at T_A = 85°C (mW)	High = 12.1 9.0 Low = 6.9	1.8	None	High = 12.1 9.0 Low = 6.9	1.8
Heater Power dissipation at T_A = 125°C (mW)	High = 14.2 11.5 Low = 8.8	1.8	None	High = 14.2 11.5 Low = 8.8	1.8

Notes: 1. I_1 = current through voltage reference.
V_s = temperature stabilizer voltage.

2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.14. Summary of Measurements at I_1 = 1.8 mA ; V_s = 40 V[1/] (LM199A)

Parameter	Overall Average[2/]	Overall σ	Parameter values not included in Final Average and Final σ, add associated device #	Final Average[2/]	Final σ
Reference Voltage at 25°C (volts)	High = +6.99383 +6.95949 Low = +6.84433	.03	None Manufacturer's spec = 6.95 ± .15 V	High = +6.99383 +6.95949 Low = +6.84433	.03
T_C over range -55°C ≤ T_A ≤ 25°C (PPM/°C)	High = +.54 +.23 Low = -.18	0.2	None	High = +.59 +.23 Low = -.18	0.2
T_C over range 25°C ≤ T_A ≤ 85°C (PPM/°C)	High = +0.7 +.3 Low = +0.2	0.3	None	High = +0.7 +.3 Low = +0.2	0.3
T_C over range 85°C ≤ T_A ≤ 125°C (PPM/°C)	High = +7.9 -4.9 Low = -78.1	20.1	-19.7, device #1 -78.1, device #19	High = +7.9 +1.4 Low = -9.8	5.3
Heater Power dissipated at T_A = -55°C (mW)	High = 566.4 521.6 Low = 486.0	23.9	None	High = 566.4 521.6 Low = 486.0	23.9
Heater Power dissipated at T_A = 25°C (mW)	High = 239.6 212.3 Low = 189.2	15.0	None	High = 239.6 212.3 Low = 189.2	15.0
Heater Power dissipation at T_A = 85°C (mW)	High = 64.8 43.8 Low = 28.0	14.7	None	High = 64.8 43.8 Low = 28.0	14.7
Heater Power dissipated at T_A = 125°C (mW)	High = 33.9 30.5 Low = 26.9	2.2	None	High = 33.9 30.5 Low = 26.9	2.2

Notes: 1. I_1 = current through voltage reference.
V_s = temperature stabilizer voltage.
2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.15. Summary of Measurements at I_1 = 11.3 mA ; V_S = 40 V [1/] (LM199A)

Parameter	Overall Average	Overall σ	Parameter values not included in Final Average and Final σ, and associated device #	Final Average	Final σ
Reference Voltage at 25°C (volts)	High = +6.99938 +6.96488 Low = +6.85109	.03	None Manufacturer's spec	High = +6.99938 +6.96488 Low = +6.85109	.03
T_C over range $-55°C \leq T_A \leq 25°C$ (PPM/°C)	High = +9.3 +1.1 Low = +.18	2.0	+9.3, device #13	High = +1.1 +0.6 Low = +.18	0.3
T_C over range $25°C \leq T_A \leq 85°C$ (PPM/°C)	High = +6.4 +2.6 Low = -1.2	2.1	+6.0, device #5 +6.4, device #17	High = +3.8 +2.0 Low = -1.2	1.6
T_C over range $85°C \leq T_A \leq 125°C$ (PPM/°C)	High = +13.9 -3.8 Low = -35.4	11.4	-35.4, device #1 -16.6, device #2	High = +13.9 -0.3 Low = -12.3	7.3
Heater Power dissipation at T_A = -55°C (mW)	High = 503.2 457.0 Low = 411.6	25.6	None	High = 503.2 457.0 Low = 411.6	25.6
Heater Power dissipation at T_A = 25°C (mW)	High = 173.6 145.8 Low = 120.4	15.0	None	High = 173.6 145.8 Low = 120.4	15.0
Heater Power dissipation at T_A = 85°C (mW)	High = 61.6 45.5 Low = 34.8	8.5	None	High = 61.6 45.5 Low = 34.8	8.5
Heater Power dissipation at T_A = 125°C (mW)	High = 70.9 57.7 Low = 44.3	8.4	None	High = 70.9 57.7 Low = 44.3	8.4

Notes: 1. I_1 = current through voltage reference.
V_S = temperature stabilizer voltage.
2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.16. Summary of Measurements at I_1 = 1 mA; V_s = 30 V [1/] (LM199A)

Parameter	[2/] Overall Average	Overall σ	Parameter values not included in Final Average and Final σ, and associated device #	[2/] Final Average	Final σ
Initial Heater Current (mA)	High = 120 108.5 Low = 95	9.0	None	High = 120 108.5 Low = 95	9.0
Reference Voltage Warm-up Stability t = 10 sec (PPM)	High = 15.2 9.05 Low = - 5.6	5.4	None	High = 15.2 7.05 Low = - 5.6	5.4
Reference Voltage Warm-up Stability t = 1 min (PPM)	High = 5.07 0.35 Low = -9.74	3.8	None	High = 5.07 0.35 Low = -9.74	3.8
Reference Voltage Warm-up Stability t = 5 min (PPM)	High = 1.3 - 2.4 Low = - 9.74	2.8	None	High = 1.3 - 2.4 Low = - 9.74	2.8
Reference Voltage Temperature Cycling Hysteresis (Positive Temp) (PPM)	High = 2.03 -0.57 Low = -2.4	1.29	None	High = 2.03 -0.57 Low = -2.4	1.29
Reference Voltage Temperature Cycling Hysteresis (Negative Temp) (PPM)	High = 1.3 -2.4 Low = -9.74	2.8	None	High = 1.3 -2.4 Low = -9.74	2.8

Notes: 1. I_1 = current through voltage reference.
V_s = temperature stabilizer voltage.
2. Each block in the average column includes the high value, the computed average value and the low value for the specified parameter.

Table 7.17. Electrical performance characteristics for device types 01 & 02 (See 3.4 unless otherwise specified)

Characteristics	Symbol	Conditions		Device Type	Limits Min.	Limits Max.	Units
Reference Voltage	V_R	$0.5mA \leq I_R \leq 10mA$ $V_S=30V$	$T_A=25°C$	01	6.800	7.100	V
		$0.6mA \leq I_R \leq 15mA$	$T_A=25°C$	02	6.70	7.20	
Reference Voltage change with current	ΔV_R (CURRENT)	$0.5mA \leq I_R \leq 10mA$ $V_S=30V$	$T_A=25°C$	01	- 9	9	mV
			$-55°C \leq T_A \leq 125°C$	01	-12	12	
		$0.6mA \leq I_R \leq 15mA$ --	$T_A=25°C$	02	-14	14	
			$-55°C \leq T_A \leq 125°C$	02	-18	18	
Reference Voltage Temperature	$\frac{\Delta V_R}{\Delta T}$	$I_R=1.0mA$ $V_S=30V$	$-55°C \leq T_A \leq 85°C$	01	-.5	.5	PPM/°C
			$85°C \leq T_A \leq 125°C$	01	-10	10	
		$I_R=1.0mA$	$-55°C \leq T_A \leq 125°C$	02	-10	10	
Dynamic Impedance	Z_D	$I_R=1mA$ $e_i=.3V; f=400Hz$	$V_S=30V; T_A=25°C$	01	0	1	Ohms
			$T_A=25°C$	02	0	1	
Noise	N_O	$I_R=1mA$ $BW=10Hz$ to $10kHz$	$V_S=30V; T_A=25°C$	01	0	20	μVrms
			$T_A=25°C$	02	0	20	
		$I_R=1mA$ $BW=0.1Hz$ to $10Hz$	$V_S=30V; T_A=25°C$	01	0	7	μVp-p
			$T_A=25°C$	02	0	7	
Temperature stabilizer supply current	I_S	$9V \leq V_S \leq 40V$ $I_R=0mA$	$T_A=25°C$	01	2.5	14	mA
			$T_A=-55°C$	01	6.6	28	
Initial Temperature stabilizer supply current	I_{SI}	$9V \leq V_S \leq 40V$ $I_R=0mA$	$T_A=25°C$	01	--	200	
Reference Voltage temperature cycling hysteresis	ΔV_R (TEMP CYCLE)	$I_R=1mA$ $-55°C \leq T_A \leq 125°C$	$V_S=30V$ --	01	-10	10	mV
				02	- 1	1	
Reference Voltage Long term stability	$\frac{\Delta V_R}{\Delta t}$	$I_R=1mA$ $\Delta t=1000$ hrs	$V_S=30V; T_A=25°C$	01	-20	20	PPM
			$T_A=45°C$	02	-20	20	PPM

SECTION VIII

SAMPLE/HOLD CIRCUITS
MIL-M-38510/125

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LIST OF FIGURES AND TABLES

SECTION VIII

SAMPLE/HOLD CIRCUITS
MIL-M-38510/125

8.1 Background and Introduction

With the advent of monolithic sample/hold circuits and their use in the expanding fields of data acquisition and data distribution, the time was right to characterize and specify these devices for military systems. National Semiconductor's LF198 was the first characterization candidate to be proposed by the JC-41 Committee. Although this report only covers the LF198, a variety of other devices may eventually be added to the future slash sheet MIL-M-38510/125.

A list of popular sample/hold circuits is shown below:

Generic Industry Type	Manufacturer
LF198	NSC, AMD, Signetics
SMP-11, -81	PMI
HA2420	Harris
IH5115	Intersil
LH0023, 0043, 0053	NSC
AD582	Analog Devices

At the time of this writing (October 1979) characterization work on the LF198 is only in the beginning stages. Most device parameters and test conditions have been identified. Test results, data analysis and final slash sheet recommendations will not be included in this report.

8.2 Device Type Description

The LF198 is a monolithic, unity gain, closed loop type sample/hold circuit. A functional schematic is shown in Figure 8-1. When this device is in the sample mode with the switch closed, the hold capacitor charges to whatever level it takes to make the output equal to the input. Gain accuracy of ± .02% is guaranteed over the military temperature range with a typical acquisition time of 6 us. Bi-FET technology is used to make the J-FET input transistors of the output buffer amplifier and thus minimize the loading on the external hold

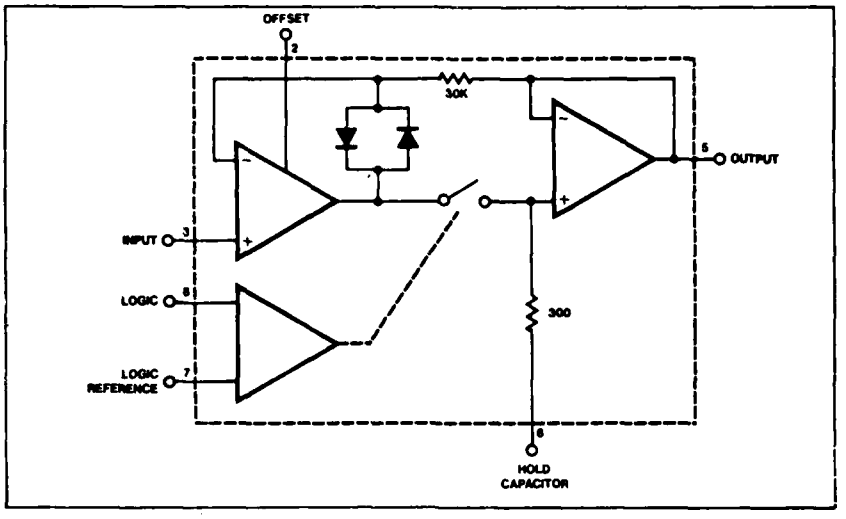


Figure 8-1. LF198 S/H functional schematic.

capacitor. Bi-polar transistors are used for the inputs of the signal amplifier to obtain low offset voltage and wide bandwidth. Unlike many hybrid and modular sample/holds, this device has an operating power supply range from ± 5 V to ± 18 V. Feed through in the hold mode has been minimized to 0.1 pf from input to output. Mode control is exercised through a TTL compatible differential comparator with a nominal threshold of 1.2 V. Acquisition time, droop rate, hold step and dynamic sampling error are important sample/hold parameters which are very much dependent on the hold capacitor as well as the device itself.

It is almost obvious to see that a smaller capacitor will yield a faster acquisition time and small dynamic sampling error at the expense of higher hold step and droop rate. The quality of the storage capacitor is also critical to sample/hold circuit performance. Only capacitors with low dielectric absorption will resist excessive "sag back" after being subjected to a quick charge of input voltage. Teflon, polypropylene and polystyrene capacitors have this low hysteresis feature whereas mica and ceramic types do not.

The back-to-back diodes and the 30 K ohm resistor maintain a feed back path for the input buffer when the device is in the hold mode.

Without this feature, the buffer input impedance could change as a function of being in the sample or hold mode. Also with the input buffer loop open, there would be a greater tendency for overload recovery time problems and acquisition time would be compromised.

8.3 Device Characterization

The LF198 is the first sample/hold circuit to be characterized and specified for a MIL-M-38510 slash sheet. Therefore, the commercial data sheet had to be critically examined to determine what additional parameters and test conditions, if any, would be required for an adequate military specification. Table 8-1 shows the generic LF198 electrical specifications. Further details on additional parameters and conditions to satisfy a slash sheet specification are shown in the JC-41 Committee electrical performance characteristics of Table 8-2. Next, a test procedure had to be formulated on how to measure the various sample/hold parameters.

Some very useful ideas and procedures were provided by National Semiconductor and Advanced Micro Devices. This manufacturer information was then used in developing a test circuit and a quasi Table III for the proposed MIL-M-38510/125 specification. Copies of the GEOS information were submitted to the JC-41 Committee for review and comment. The test circuit and test procedure are shown in Figure 8-2 and Table 8-3, respectively. Most of the sample/hold electrical characteristics will be measured on the S-3263 test system, automatically.

Some oscilloscope waveforms which show the relationships between the input, output and logic signals as a function of hold capacitance and signal level are shown in Figures 8-3 and 8-4.

8.4 Discussion

The LF198 characterization work will be covered completely in the next final report. At this time the device looks very promising and no major characterization problems are foreseen.

8.5 Bibliography

8.5.1 Linear Databook, National Semiconductor (1978)

8.5.2 C. Nelson, "I.C. Sample and Hold is 0.01% Accurate", E. E. Times I.C. Applications Conference Proceedings, 1977.

8.5.3 C. Nelson, National Semiconductor, LF198 Test Information (not published).

8.5.4 M. Mullen, Advanced Micro Devices, LF198 Test Information (not published).

absolute maximum ratings

Supply Voltage	±18V	Input Voltage	Equal to Supply Voltage
Power Dissipation (Package Limitation) (Note 1)	500 mW	Logic To Logic Reference Differential Voltage (Note 2)	+7V, −30V
Operating Ambient Temperature Range		Output Short Circuit Duration	Indefinite
LF198	−55°C to +125°C	Hold Capacitor Short Circuit Duration	10 sec
LF298	−25°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C
LF398	0°C to +70°C		
Storage Temperature Range	−65°C to +150°C		

electrical characteristics (Note 3)

PARAMETER	CONDITIONS	LF198/LF298			LF398			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage, (Note 6)	T_j = 25°C		1	3		2	7	mV
	Full Temperature Range			5			10	mV
Input Bias Current, (Note 6)	T_j = 25°C		5	25		10	50	nA
	Full Temperature Range			75			100	nA
Input Impedance	T_j = 25°C		10^{10}			10^{10}		Ω
Gain Error	T_j = 25°C, R_L = 10k		0.002	0.005		0.004	0.01	%
	Full Temperature Range			0.02			0.02	%
Feedthrough Attenuation Ratio at 1 kHz	T_j = 25°C, C_h = 0.01μF	86	96		80	90		dB
Output Impedance	T_j = 25°C, "HOLD" mode		0.5	2		0.5	4	Ω
	Full Temperature Range			4			6	Ω
"HOLD" Step, (Note 4)	T_j = 25°C, C_h = 0.01μF, V_{OUT} = 0		0.5	2.0		1.0	2.5	mV
Supply Current, (Note 6)	$T_j \geq 25°C$		4.5	5.5		4.5	6.5	mA
Logic and Logic Reference Input Current	T_j = 25°C		2	10		2	10	μA
Leakage Current into Hold Capacitor (Note 6)	T_j = 25°C, (Note 5) Hold Mode		30	100		30	200	pA
Acquisition Time to 0.1%	ΔV_{OUT} = 10V, C_h = 1000 pF		4			4		μs
	C_h = 0.01μF		20			20		μs
Hold Capacitor Charging Current	$V_{IN} - V_{OUT}$ = 2V		5			5		mA
Supply Voltage Rejection Ratio	V_{OUT} = 0	80	110		80	110		dB
Differential Logic Threshold	T_j = 25°C	0.8	1.4	2.4	0.8	1.4	2.4	V

Note 1: The maximum junction temperature of the LF198 is 150°C, for the LF298, 115°C, and for the LF398, 100°C. When operating at elevated ambient temperature, the TO-5 package must be derated based on a thermal resistance (Θ_{jA}) of 150°C/W.

Note 2: Although the differential voltage may not exceed the limits given, the common-mode voltage on the logic pins may be equal to the supply voltages without causing damage to the circuit. For proper logic operation, however, one of the logic pins must always be at least 2V below the positive supply and 3V above the negative supply.

Note 3: Unless otherwise specified, the following conditions apply. Unit is in "sample" mode, V_S = ±15V, T_j = 25°C, −11.5V ≤ V_{IN} ≤ +11.5V, C_h = 0.01μF, and R_L = 10 kΩ. Logic reference voltage = 0V and logic voltage = 2.5V.

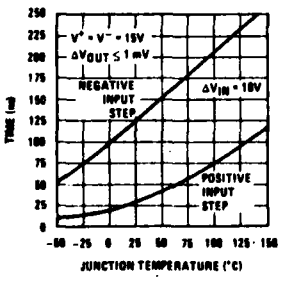
Note 4: Hold step is sensitive to stray capacitive coupling between input logic signals and the hold capacitor. 1 pF, for instance, will create an additional 0.5 mV step with a 5V logic swing and a 0.01μF hold capacitor. Magnitude of the hold step is inversely proportional to hold capacitor value.

Note 5: Leakage current is measured at a *junction* temperature of 25°C. The effects of junction temperature rise due to power dissipation or elevated ambient can be calculated by doubling the 25°C value for each 11°C increase in chip temperature. Leakage is guaranteed over full input signal range.

Note 6: These parameters guaranteed over a supply voltage range of ±5 to ±18V.

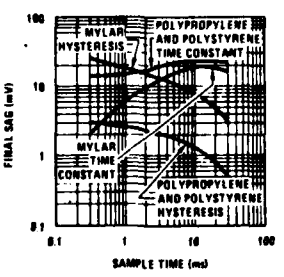
typical performance characteristics

Aperture Time*



*See definition

Capacitor Hysteresis



Dynamic Sampling Error

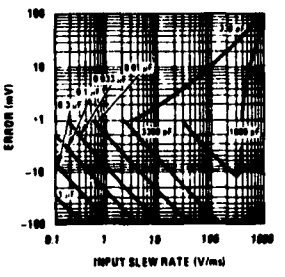


Table 8-1. Generic LF198 electrical specification.

LF 198
ELECTRICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified the device is in the sample mode
T_A = - 55°C to + 125°C, V_s + 15, Vin - 11.5 to + 11.5 V, Ch = .01 uf

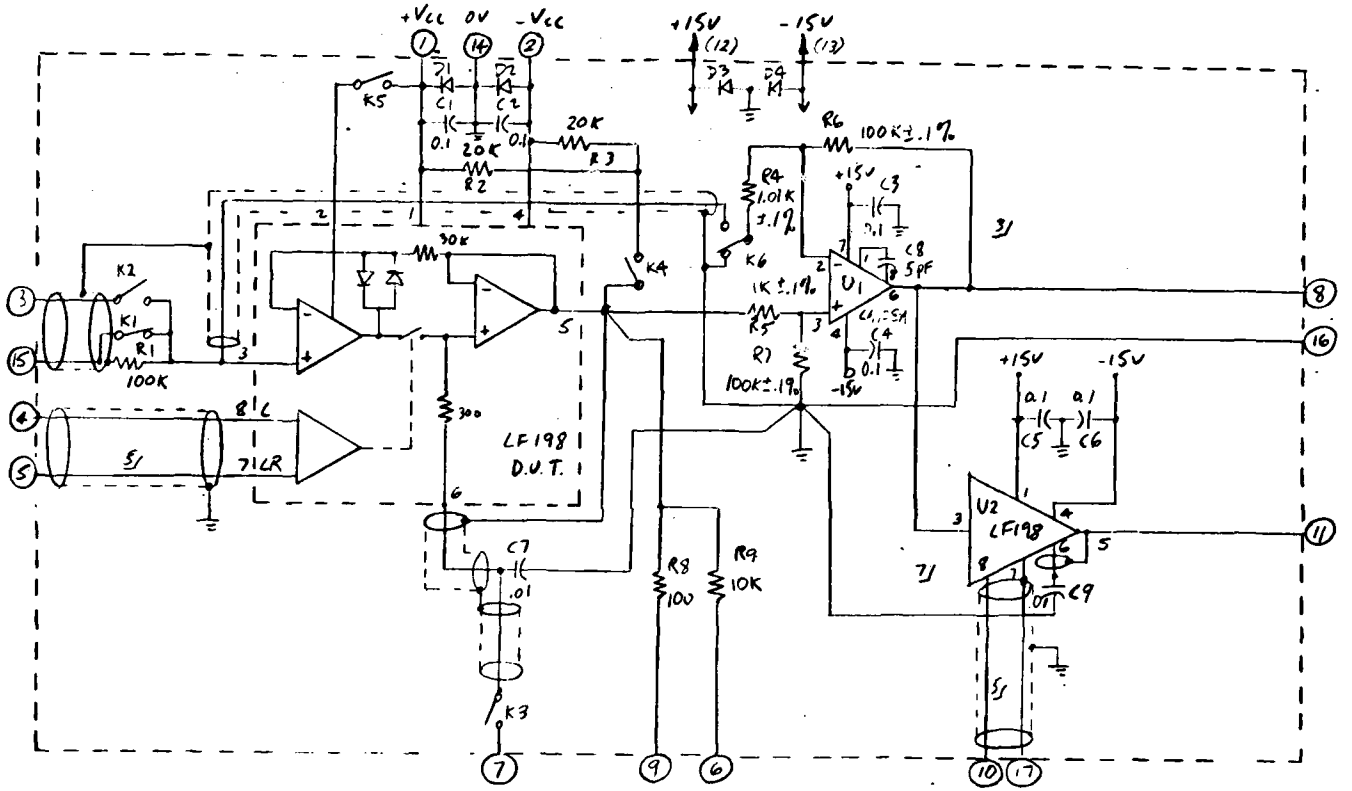
Characteristic	Symbol	Conditions		Limits Min	Max	Units
Input Offset Voltage	V_{IO}	V_s ±5V to ±15V V_{in}=0V	T_A = 25°C	-3	+3	mV
		-55°C ≤	T_A ≤ + 125°C	-5	+5	mV
Input Bias Current	I_{IB}		T_A = 25°C	-1	25	mA
				-75	75	mA
Input Impedance	Z_i		T_A = 25°C	2	-	GΩ
				1	-	GΩ
Gain Error	A_e	V_{in}=0 to -11.5V, V_{in}=0 to +11.5V, R_L=10K	T_A = 25°C	-.005	+.005	%
				-.02	+.02	%
Gain Error	A_e	V_s=±5V V_{in}=0 to -2V, V_{in}=0 to +2V, R_L=10K	T_A = 25°C	-.02	+.02	%
				-.04	+.04	%
Feedthrough Attenuator Ratio	FRR_1	V_{out}= -11.5V, +11.5V V_{in}= ±15C Ch= .01uf DC Test, Hold Mode	T_A = 25°C	86	-	dB
				80	-	dB
Feedthrough Attenuator Ratio at 1 kHz	FRR_2	V_{in}= 10 Vpp V_{out}=0V, Ch= .01 uf	T_A = 25°C	86	-	dB
Output Impedance	Z_{out}	Hold Mode Ch=0V		-	4	Ω
		V_{out}=0V, I_o=±1mA, V_{in}=0V	T_A = 25°C	-	2	Ω
"Hold" Step	V_{hs}	V_{lg} = 0 to 4V, T_r 50 ns V_{out}= ±11.5V		-5	5	
			T_A = 25°C	-2	2	mV
Supply Current	I_{cc}	V_s= ± 18V Sample Mode	T_A = -55°C	-	6.5	mA
		+25°C ≤	T_A ≤ 125°C	-	5.5	mA
Logic Input Current	I_{IH}, I_{IL}	V_{in}=0V V_L=0V, V_{LR}=5.5V; V_L=5.5V V_{LR}=0V	T_A = 25°C	-10	+10	uA
				-20	+20	uA

TABLE 8-2. JC-41 Committee LF198 electrical performance characteristics.

ELECTRICAL PERFORMANCE CHARACTERISTICS (cont.)

Characteristic	Symbol	Conditions	Limits Min	Limits Max	Units
Hold Mode Leakage Current	I_L	V_{out}= ± 11.5V T_J = 25°C	-100	100	pA
Hold Mode Leakage Current	I_L	V_{out}= ± 11.5V -55°C ≤ T_J ≤ 125°C	-100	100	nA
Hold Cap Charge Current	I_{ch}	$V_{in} - V_{out}$ = 2V V_{out} = ± 11.5V T_A = 25°C	3 2	- -	mA mA
Power Supply Rejection Ratio	+PSRR	V- = -18V, V+ = +12 to +18V, V_{in} = 0	80	-	dB
Power Supply Rejection Ratio	-PSRR	V+ = 18V, V- = -12 to -18V, V_{in} = 0	80	-	dB
Diff Logic Threshold	V_{th}	V_{LR} = 0V, V_{in} = 0V	0.8	2.0	V
Acquisition Time to .01%	t_{aq}	V_{in} = 0 to + 10V CL = 100 uf V_{in} = 0 to - 10V Ch = .01 uf T_A = 25°C	-	25	us
Noise	e_n	10 to 100 K Hold mode, sample mode T_A = 25°C	-	25	uVaV
Hold Mode Settling Time	t_s	0 to 10 V input V_{in} = 0 , V_{out} < 1 mV T_A = 25°C	-	1.5	us
Aperture Time	t_{ap}	Ch = .01, V_{out} ≤ 1 mV V_{in} = 10V T_A = 25°C	-	200	ns

TABLE 8-2. JC-41 Committee LF198 electrical performance characteristics.



Notes:
1. Last component designations are R9, C9, U2, D4 and K6.
2. All resistors are ± 1% film unless otherwise stated.
3. U1 offset error shall be measured with pin 9 grounded. This error shall be removed in the software calculations.
4. Relay control inputs are not shown.
5. A speed up circuit is required in series with the logic input for rise times greater than 0,5 us.
6. Circled pin numbers are top socket connections. All other pins are undersocket connections.
7. The adapter S/H U2 is required for T_A=125°C testing of some parameters.

Figure 8-2. LF198 S/H test circuit.

TABLE III. Group A inspection for all device types

Subgroup (S)	Symbol	MIL-STD -883 Method	Test No.	Notes	Adapter Pin Numbers (see Fig. 7) 1	2	3	4	5	6	7	Energized Relays	Measured Pin No	Measured Pin Value	Measured Pin Units	Equation 2/	Limits Min	Limits Max	Units
1,2,3	V_{IO}	4001	1	1/ 3/	3.5V	-26.5V	Open	- 9V	-11.5V	Open	Open	None	8	E1	V	V_{IO} = 10 E1	- 3	3	mV
			2		26.5V	- 3.5V		14V	11.5V					E2		V_{IO} = 10 E2			
			3		15 V	-15V		2.5V	0V					E3		V_{IO} = 10 E3			
			4		7 V	- 3V		4.5V	2V					E4		V_{IO} = 10 E4			
			5		3 V	- 7V		0.5V	- 2V					E5		V_{IO} = 10 E5			
	$+I_{IB}$		6		3.5V	-26.5V		- 9V	-11.5V			K1		E6		$+I_{IB}$ = 100 (E6-E1)	1	25	nA
			7		26.5V	- 3.5V		14V	11.5V					E7		$+I_{IB}$ = 100 (E7-E2)			
			8		15 V	-15V		2.5V	0 V					E8		$+I_{IB}$ = 100 (E8-E3)			
	Z1		9		Calculate using data from tests 1,2,6, and 7											Z1 = 0.23/(E1+E7-E2-E6)	2	-	Ω
	A_E		10		3.5V	-26.5V	Open	- 9V	-11.5V	Open	Open	K4	8	E9	V	A_E = (E9-E10)/23	-.005	.005	%
			11		26.5V	- 3.5V		14V	11.5V					E10					
			12		3 V	- 7V		0.5V	-2V					E11		A_E = (E11-E12)/4	- .02	.02	
			13		7 V	- 3V		4.5V	2V					E12					
	V_{IO}(ADJ)		14		15 V	-15V		2.5V	0V			K5		E13		V_{IO}(ADJ) = 10 (E3-E13)	10	-	mV
	+PSRR	4003	15		18 V	-18V						None		E14		+PSRR = 20 log |600/(E14-E15)|	80	-	dB
					12 V	-18V								E15					
	-PSRR		16		18 V	-12V								E16		-PSRR = 20 log |600/(E14-E16)|			
	FRR		17	4/, 7/	15 V	-15V	See Fig. 8					K1, K2		E17		FRR = 20 log |1500/(E18-E17)|	86	-	dB
			18				timing							E18		FRR = 20 log |1500/(E19-E18)|			
			19				waveforms							E19		FRR = 20 log |1500/(E20-E19)|			
			20											E20		FRR = 20 log |1500/(E21-E20)|			
														E21					
	Z_o		21	5/			See Fig. 9			-10 V	0V	K3		E22		Z_o = 5 (E23 -E22)	-	2	Ω
							timing			10 V	0V			E23					
	V_{HS}		22	6/, 7/	3.5V	-26.5V	See Fig. 10		-11.5V	Open	Open	K6		E24		V_{HS} = 10 (E25-E24)	- 2	2	mV
			23	6/, 7/	26.5V	-3.5V	timing		11.5V					E25					
														E26		V_{HS} = 10 (E27-E26)			
														E27					
	I_{CC}		24		15V	-15V	Open	2.5V	0V			None	2	I_1	mA	I_{CC} = I_1	-	5.5	mA
	I_{IH}		25	8/	8.5V	-21.5V		5.5V	5.5V				4	I_2	uA	I_{IH} = I_2	0	10	uA
			26										5	I_3		I_{IH} = I_3			
	I_{IL}		27		21.5V	- 8.5V		0V	0V					I_4		I_{IL} = I_4	-1.0	1.0	
			28						5.5V				4	I_5		I_{IL} = I_5			

Table 8-3. LF198 sample/hold test procedure.

TABLE III. Group A inspection for all device types

Subgroup (S)	Symbol	MIL-STD -883 Method	Test No.	Notes	Adapter Pin Numbers (See Fig. 7) 1	2	3	4	5	6	7	Energized Relays	Measured Pin No	Value	Units	Equation	@ 25°C Limits Min	Max	Units
1,2,3	I_{OS}(+) I_{OS}(-)	3011	29 30	9/	15V	-15V	10V -10V	2.5V	0V	Open	Open	K1, K2	9	I6 I7	mA	I_{OS} (+) = I6 I_{OS} (-) = I7	-20 -	- 20	mA
	I_{HL}(+)		31	10/	3.5V	-26.5V	See Fig. 11 timing waveforms		-11.5V			None	8	E28 E29	V	I_{HL}(+) = 100 (E29 - E28)	-100	100	pA
	I_{HL}(-)		32	10/	26.5V	-3.5V			11.5V					E30 E31		I_{HL}(-) = 100 (E31 - E30)			
	I_{CH}(+)		33	11/	15V	-15V	11.5V	2.5V	0V		9.5V	K1,K2,K3	7	I8	mA	I_{CH}(+) = I8	-	-3	mA
	I_{CH}(-)		34	11/			-11.5V				-9.5V			I9		I_{CH}(-) = I9	3	-	
	V_{TH}(H)		35	12/			- 2V	2.0V			0V			I10	mA	V_{TH}(H) $\leq$ 2.0V if $I_{IO} \geq$ 1 mA	1	-	mA
	V_{TH}(L)		36	12/			- 2V	0.8V						I11	nA	V_{TH}(L) $\geq$ 0.8V if -1< I11<.1nA	-1	1	nA
1,2,3	$\Delta V_{IO}/\Delta T$		37		$\Delta V_{IO}/\Delta T$ = (V_{IO} @ T & OCM - V_{IO} @ 25°C & OCM)/ (T - 25°C)												-20	20	uV/°C
4	tac		38 39 40 41	13/	15V	-15V	See Fig. 12 timing waveforms & flow chart		0V	Open	Open	K1,K2,K6	8	t1 t2 t3 t4	us	tac = t1 tac = t2 tac = t3 tac = t4	-	25	us
	tap		42 43 44 45	14/			See Fig. 13 timing waveforms & flow chart							t5 t6 t7 t8	ns	tap = t5 tap = t6 tap = t7 tap = t8	-	200	ns
12	ts		46 47	15/			See Fig. 14					None		t9 t10	us	ts = t9 ts = t10	-	1.5	us
7	FRRac		48	16/			20VPP	0V						E41	VPP	FRRac = 20 log | 2000/E41 | (See Fig. 15)	86	-	dB
	TR(tr)		49	17/			50mV	2.5V						t1	ns	TR(tr) = t1 (see Fig. 16)			ns
	TR(os)		50											V01, V01	mV	TR(os) = 100 (ΔV01/V01)			%
	NI(BB)		51 52	18/			0V	2.5V 0V						E42 E43	uVrms	NI(BB) = E42/100 NI(BB) = E43/100	- -	25 25	uVrms

Table 8-3. LF198 sample/hold test procedure (cont'd).

LF198 Sample/Hold Test Procedure Notes

1/ In order to remove test amplifier offset from the data values measure the offset of U1 on pin 8 with pin 9 grounded.

Software subtraction techniques should be used to correct the data.

2/ The equations take into account the test amplifier gain of 100 and other circuit constants so that the calculated value is in Table I units.

3/ Common mode input range conditions are exercised by grounding the signal input and swinging the power supplies to their nominal levels minus the common mode voltage. For example for V_{CM} = + 11.5 V, + V_{CC} = 15 V - 11.5 = 3.5 and - V_{CC} = - 15 V - 11.5 V = - 26.5 V.

4/ With a 0 V signal input the D.U.T. logic input is switched from 2.5 V to 0 V. This resets the system in the hold mode. The test amplifier output is measured immediately after each 15 V change at the signal input.

5/ E22 and E23 are measured with the D.U.T. in the hold mode.

6/ For the hold step test, the first and second measurements are made with the D.U.T. in the sample and hold modes respectively.

7/ Logic input step changes should have a rise time of 0.5 u seconds or less.

8/ High and low state logic input currents shall be measured over the common mode voltage range as shown.

9/ The output shall be shorted to ground for 25 milliseconds or less.

10/ Hold leakage current at 25°C is determined by measuring the droop referred to the test amplifier output over a one second interval.

11/ The charge current measurements on pin 7 is referenced to forced voltages of 9.5 V and - 9.5 V respectively.

12/ With worst case logic threshold voltages applied, the hold cap terminal output current is measured to determine if the device is in the correct operating mode.

13/ Step the signal input from 0 V to + 10 V. After a delay of $\approx$ 100 usec generate a 100 usec sample mode pulse. The difference between the input and D.U.T. output is monitored with a high differential amplifier. Reduce the sample mode pulse width until there is a 10 mV (0.1%) change from the 100 usec pulse value. The sample mode pulse width for this condition is the acquisition time. Repeat the above procedure for input signal transitions of 10 V to 0 V, 0 V to - 10 V and - 10 V to 0 V. Figure 12 shows an automatic flow chart method and a simplified manual method for determining acquisition time.

Table 8-3. LF198 sample/hold test procedure (cont.).

14/ Step the logic input from 5 V to 0 V with the input at 0 V. After a 2 usec time delay step the signal input up to 10 V. For this condition the D.U.T. output should be $\approx$ 0 V. Gradually decrease the delay until a 10 mV (.1%) shift occurs at the D.U.T. output. Repeat the above procedure for input signal transitions of 10 V to 0 V, 0 V to - 10 V and - 10 V to 0 V. The delay corresponding to the 10 mV shift is equal to the aperture time.

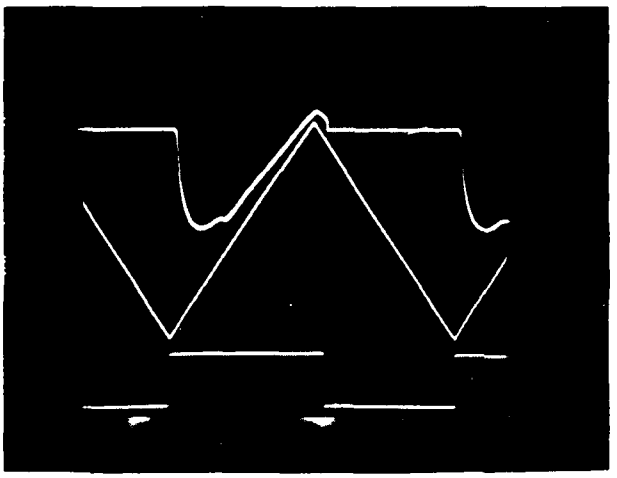
15/ Settling time is determined by adding the aperture time to the additional increment of time during which the output in the hold mode is greater than one millivolt from final value.

16/ Dynamic feedthrough rejection is determined in the hold mode with a signal input of 20 V_{pp} at a frequency of 1 kHz.

17/ Overshoot TR (OS) and rise time TR (tr) are indicative of the stability and bandwidth of the device, respectively.

18/ Broadband noise NI (BB) of the D.U.T. is extracted from the total noise of the D.U.T. and a low noise op amp such as the SE5534.

Table 8-3. LF198 sample/hold test procedure (cont.)



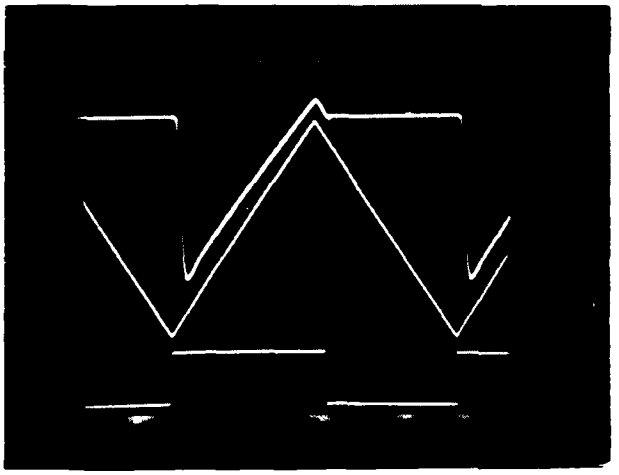
V_{out} @ 5 V/div.

V_{in} @ 5 V/div.
(Triangle Freq = 30 kHz)

V_{LOG} @ 2 V/div.

Time @ 5 usec/div.

C_{HOLD} = 0.01 uF



V_{out} @ 5 V/div.

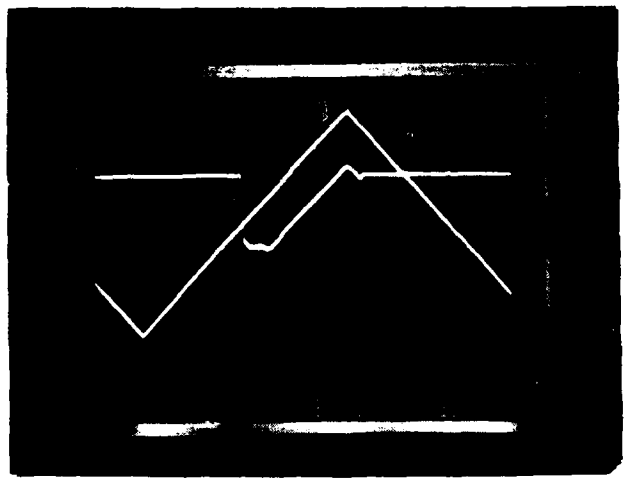
V_{in} @ 5 V/div.
(Triangle Freq = 30 kHz)

V_{LOG} @ 2 V/div.

Time @ 5 usec/div.

C_{HOLD} = 0.001 uF

Figure 8-3. LF198 sample/hold waveforms vs. hold capacitor.

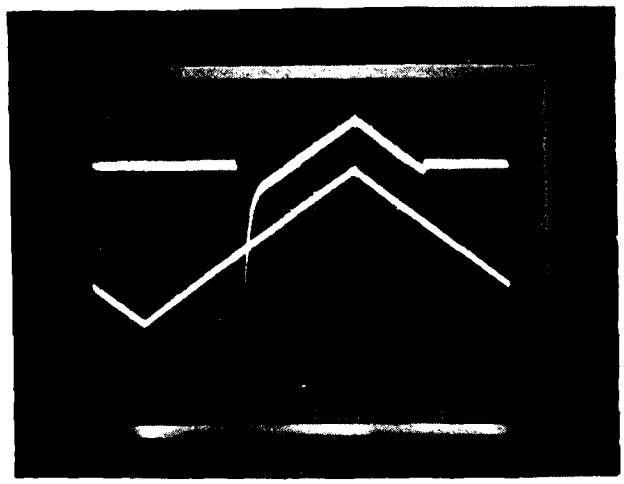


V_{out} @ 5 V/div.

V_{in} @ 5 V/div.

Time @ 10 us/div.

C = .01 uF



V_{out} @ 50 mV/div.

V_{in} @ 50 mV/div.

Time @ 10 us/div.

C = .01 uF

Figure 8-4. LF198 sample/hold waveforms vs. signal level.

SECTION IX

VOLTAGE REGULATORS, NEGATIVE

MIL-M-38510/115

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SECTION IX

VOLTAGE REGULATORS, NEGATIVE

MIL-M-38510/115

9.1 Background and Introduction

The characterization effort of fixed negative voltage regulators was undertaken in 1978 and is reported in RADC-TR-78-275 Final Technical Report. The report noted observations that indicated several device anomalies, such as; a) start-up and output short circuit current problems under different input voltages and load currents, b) emitter-follower type oscillations and c) hot-socket insertion/extraction failures. Emitter-follower type oscillations and hot-socket insertion/extraction failures were investigated and solutions to these problems were presented. Information relation to problems of this type may be found in an article "Designer's Guide to: I.C. Voltage Regulators" by Robert Dobkin published in EDN August 20, 1979 and September 5, 1979. The start-up anomaly was observed immediately prior to the writing of the above mentioned report. Investigations were continued after the report was issued for publication and are presented herein.

9.2 Start-up Investigations and Results

The investigation of the start-up problem was initiated as a result of comments made at a JC-41 Committee meeting in March of 1978. At this meeting various members disclosed that some regulators failed to start or were specified in such a way that devices that would not start would not be detected. The investigation at OS began with the construction of the test circuit shown in Figure 9.1. The switch, S-1, was connected to a stiff high current power supply and the test was performed under various load conditions. The test was performed repeatedly and occasional failures were observed by three individuals at OS test facilities. As simple as this test appeared, it had the drawback that the on/off duty cycle, for power to the device, was uncontrolled; and, since these devices are tested without a heat sink, it is quite possible that with this over-simplified test circuit they were driven into their thermal shut-down mode.

In order to eliminate the suspected thermal shut down problem, a special solid state start-up circuit was constructed and is shown in its final form in Figure 9.2. This circuit was used to test devices that had previously failed start-up at OS, but could not be confirmed at the manufacturer's test facility. The use of relays for this test was rejected because it was felt that relay chatter would introduce an uncontrolled test condition. The pass transistor, used in the circuit in

Figure 9.2, is a power darlington transistor and can provide sufficiently high initial current for the start-up test. A current regulator is used in the base of the power darlington, and the current into the base of the transistor is regulated by the op amp and the shunt transistor to ground. Because of the high capacitive load circuit at the power darlington emitter and the high impedance input circuit at the power darlington base, it was necessary to add stabilizing capacitors to the control circuit in order to eliminate emitter-follower oscillations. The closed loop gain of the start-up circuit has a gain of 10 so that voltages as high as 40 can be easily programmed by either an automatic tester or a pulse generator. With this start-up circuit, the duty cycle of the regulator on-time was set for 2%. No start up failures were observed on the oscilloscope; so, the duty cycle was increased. As the duty cycle increased, intermittent start-up problems were observed. This circuit confirmed the suspicion that the initial observation was due to uncontrolled heating of the device which went into thermal shut-down.

At a later meeting of the JC-41 Committee, it was learned that the start-up problem could occur if the regulator output was momentarily shorted to ground. To test this parameter the circuit, shown in Figure 9.2, at the output of the regulator was developed. With this circuit, the output is forced to zero volts. The forcing voltage is then removed and the device is allowed to recover into a resistive capacitive load. OS recommends that this anomaly be called voltage recovery. Both start-up and voltage recovery tests are discussed in Section 3.

Some negative voltage regulators with date code 7619 and 7639 were tested in this test circuit. The devices all started-up at 25°C with input voltages between - 30V and -8 Volts and with load conditions in accordance with the test specification. However, with the input voltage magnitude greater than 25 volts and the case temperature greater than 60°C, a few of these regulators failed to recover with the specified load current. Negative regulators with date codes 78XX were also tested and passed the voltage recovery test with a case temperature of 125°C.

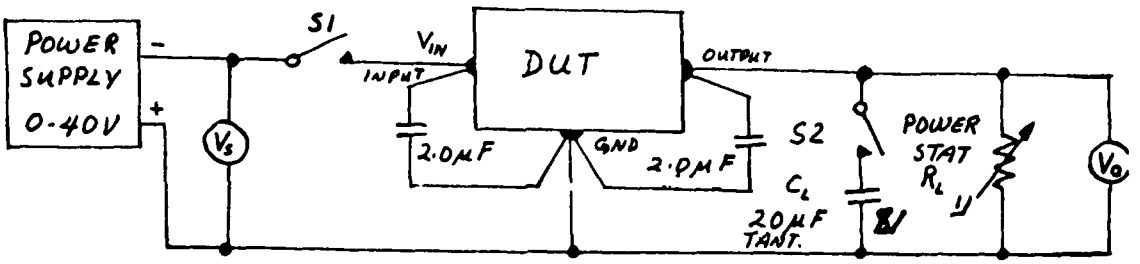
Additional testing on the 76XX data code devices that failed the voltage recovery test revealed that the input-to-output voltage differential is very critical. For case temperatures above 60°C and with a specified load condition, these devices shut down when the input-to-output voltage magnitude was greater than 20 volts. None of the tested negative voltage regulators, with date codes 78XX, showed this anomaly.

9.3 Conclusions

Start-up problems originally identified by GEOS in 1978 apparently were due to the use of an uncontrolled ON-time duty cycle of the regulator, causing random thermal shutdown to occur. Present testing indicates that start-up problems do not exist with any regulators specified in MIL-M-38510/115, /117, /118.

Voltage recovery problems may exist with devices from one vendor, having date codes prior to 1978. Devices qualified to MIL-M-38510 will not exhibit voltage recovery problems, which have been designed out by the vendor in question.

Hot socket & emitter follower oscillations were resolved in the aforementioned report. The findings and resolutions for these anomalies are still valid.



Device Type	01	02	03	04	05	06	07	08	Test Condition Group
R_L for I_L = 5mA	1.0KΩ	2.4KΩ	3.0KΩ	4.8KΩ	1.0KΩ	2.4KΩ	3.0KΩ	4.8KΩ	1
$\|V_{IN(min)}\|$	8 Vdc	15 Vdc	18.5Vdc	28Vdc	8 Vdc	15 Vdc	18.5Vdc	28Vdc	
$\|V_{IN(max)}\|$	35Vdc	35Vdc	35Vdc	40Vdc	35Vdc	35Vdc	35Vdc	40Vdc	
R_L for I_L = 350mA/500mA	14.3Ω	34Ω	43Ω	68Ω	10Ω	24Ω	30Ω	48Ω	2
$\|V_{IN(min)}\|$	8 Vdc	15 Vdc	18.5Vdc	28Vdc	8 Vdc	15 Vdc	18.5Vdc	28Vdc	
$\|V_{IN(max)}\|$	25Vdc	32Vdc	35Vdc	40Vdc	25Vdc	32Vdc	35Vdc	40Vdc	
R_L for $I_L = I_{L(max)}$	10Ω	24Ω	30Ω	48Ω	5Ω	12Ω	15Ω	24Ω	3
$\|V_{IN(min)}\|$	8 Vdc	15Vdc	18.5Vdc	28Vdc	8 Vdc	15Vdc	18.5Vdc	28Vdc	
$\|V_{in(max)}\|$	20Vdc	27Vdc	30 Vdc	38Vdc	20Vdc	27Vdc	30Vdc	38 Vdc	

NOTES:

1/ For each device type, adjust R_L for a typical load current of 5 mA.

2/ Adjust $V_s = -|V_{in(min)}|$ for the device type under test. Close switch S1 and observe that the proper voltage is at V_o. Open S1.

3/ Repeat the conditions defined in 1/ and 2/ with $V_s = -|V_{in(max)}|$ for each device type under test.

4/ For each device type, adjust R_L for a load current of 350 mA or 500 mA per Group 2.

5/ Repeat the conditions defined in 2/ and 3/ with the load current conditions defined in 4/.

6/ For each device type, adjust R_L for a typical maximum load current.

7/ Repeat the conditions defined in 2/ and 3/ with the load current conditions defined in 6/.

8/ With S2 closed, repeat the conditions defined in 1/ through 7/.

Figure 9.1. Manually controlled start-up test circuit.

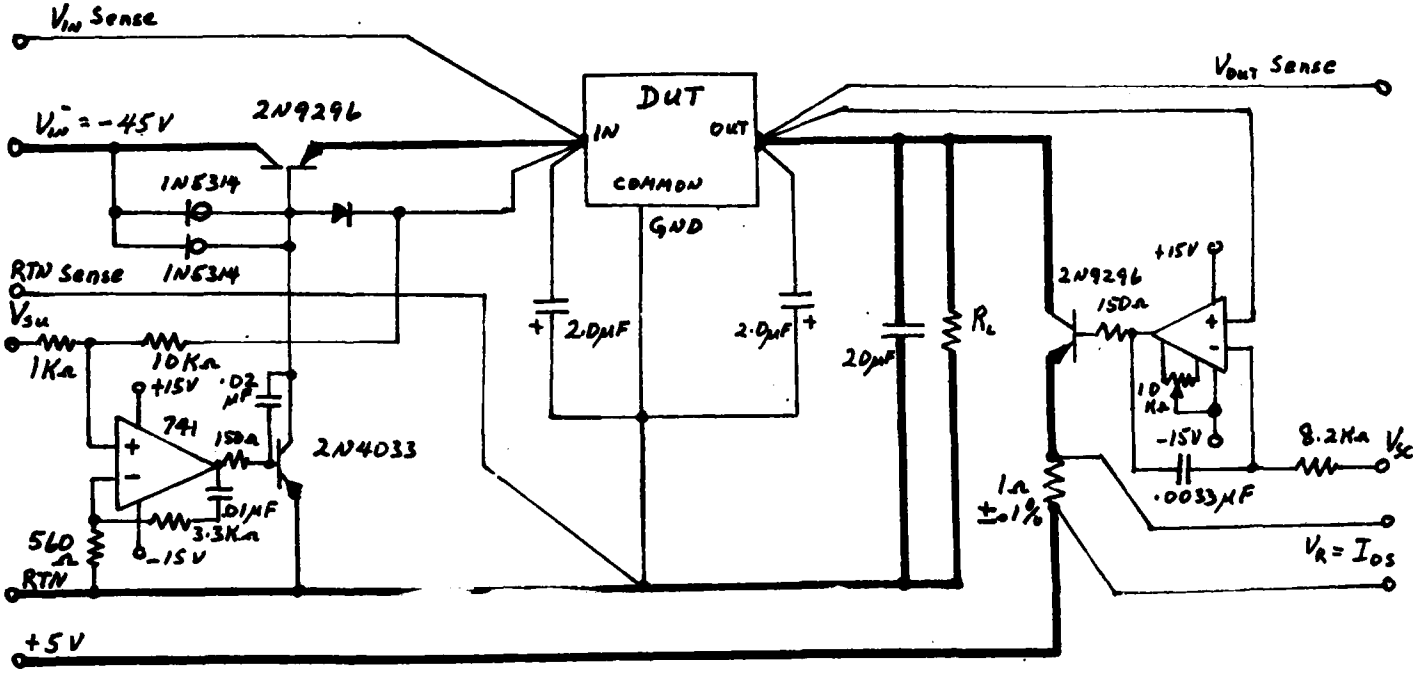


Figure 9.2. Solid-state controlled start-up and recovery voltage circuit.

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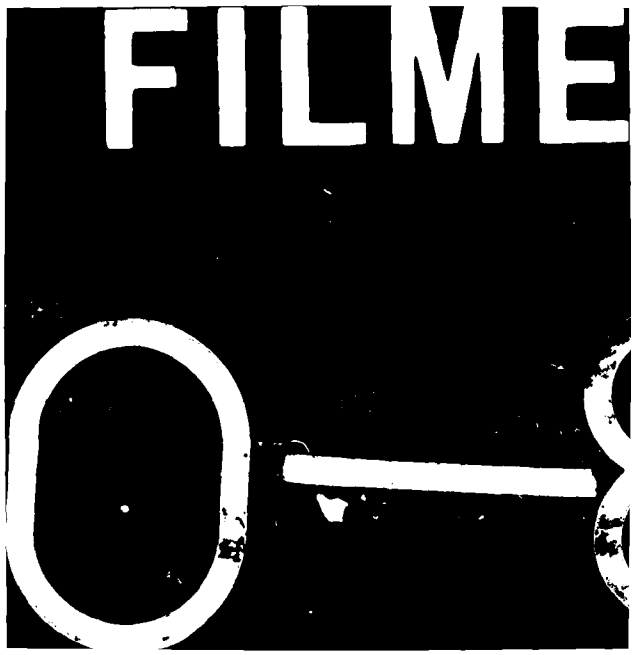
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