Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: ESD-TR-80-130	2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle): DESIGN OF A PROTOTYPE MICROCOMPUTER DRIVEN TRAINING DEVICE FOR AN AIR FORCE MAINTENANCE SCHOOL	5. TYPE OF REPORT & PERIOD COVERED: Thesis, Final rept, Jan 78 – Nov 78
	6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s): Michael F. Winthrop, Capt, USAF	8. CONTRACT OR GRANT NUMBER(s): 189
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Hq Electronic Systems Division (TOI), Hanscom AFB, Massachusetts 01731	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS: Hq Electronic Systems Division (TOI), Hanscom AFB, Massachusetts 01731	12. REPORT DATE: August 1979 13. NUMBER OF PAGES: 187
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	15. SECURITY CLASS. (of this report): Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

LEVEL II

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

DTIC ELECTE SEP 17 1980 D C

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

Patents Pending on devices shown as Air Force Invention No. 13632. Work accomplished under funding and auspices of Keesler Technical Training Center (KTTC/TTVET), Keesler AFB, Mississippi.

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Simulator	Line Replaceable Unit (LRU)	Signal Generator
Maintenance	Built in Test (BIT)	TPS-43E Radar
Trainer	Built in Test Equipment (BITE)	Commercial
Microcomputer	Programmable	Off the Shelf
Radar	Waveform Generator	

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Microcomputers are no longer toys, they are cheap computers. This project proved that a commercial, "off the shelf" microcomputer could run a simulator used in an Air Force Technical Training school. Research through the Defense Documentation Center (now the Defense Technical Information Center) showed nothing comparable in DoD. Commercial producers of trainers were also unable to show equivalent capability.

A reproducible method to evaluate microcomputers is shown and used. Circuits are shown and discussed which provide control of the trainer

DD FORM 1 JAN 73 1473 — Unclassified

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

and implement outputs. An invention is detailed which produces waveshapes for oscilloscope under program control. Software is provided, with full documentation, that generates waveshapes for the invention (above) which can then run independent of computer inputs.

ESD-TR-80-130

University of Southern Mississippi

DESIGN OF A PROTOTYPE MICROCOMPUTER DRIVEN TRAINING DEVICE FOR AN AIR FORCE MAINTENANCE SCHOOL

BY

Michael F. Winthrop

A Thesis
Submitted to the Graduate School
of the University of Southern Mississippi
in Partial Fulfillment of the Requirements
for the Degree of Master of Science

Approved:

_____
Director

_____

_____

_____
Dean of the Graduate School

August, 1979

ACKNOWLEDGEMENTS

The author wishes to acknowledge that this work was supported by the United States Air Force, Keesler Air Force Base, in Biloxi, Mississippi. Final typing was provided by the Main Plant, Second Floor, Correspondence Center at the Martin Marietta Corporation of Orlando, Florida, with whom the author is serving an extended temporary duty assignment for the Air Force.

The writer is deeply indebted to Professor Cecil D. Burge, Ph.D., P.E., major advisor, for his valuable assistance and direction. Also, the author would like to express appreciation to the people in the chain of command of Air Training Command for their confidence in this project as expressed in money, facilities and personnel. The author wishes to make special note of Lt. Col. selectee James R. Bridges, Jr., Chief of Training Service Division, and prime mover in this project; Mr. Buddy L. Holmes, master technician; and especially the entire group of craftsmen and artisans with whom he had the privilege of working.

I wish also to use this space to thank my wife, Jeanne Elizabeth, and my two sons, Michael Francis and Daniel Scott, for their support and understanding during the many months of 16 hour days and family separation they have endured during this study and its final preparation.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF DRAWINGS

LIST OF FIGURES

CHAPTER I

INTRODUCTION

Background of the project

Maintenance training traditionally has been considered an area that requires the actual equipment (end item). The reasons usually advanced are (a) the "realism" of the equipment, (b) user acceptance, and (c) the availability of such devices.[1] Problems that have been encountered are (a) the end item is costly, (b) the end item is frequently more sophisticated than training needs dictate, and (c) the end item is not specifically designed to be "student proof" for training.

Simulation of end items is a method to reduce the costs of training equipment. The object is to design training equipment which will respond to a student the way the real equipment would insofar as training is concerned, but cost less initially and not have the overhead of maintenance and operation of the original equipment. In this document, maintenance simulation is the application of simulation techniques to the area of maintenance training.

The nature of simulation is applicable to operational training because designers are limited to mimicing the outward functions of the original equipment. Of importance today is maintenance simulation which requires mimicing the inner functions of the original equipment.

General purpose computers were used in maintenance simulators as early as the mid-50's.[2] Unfortunately the costs exceeded the benefits of maintenance simulation because of the dedicated computer

requirement. Lately, the price of computers has dropped to the point where maintenance simulation is practical. Cost and the current state of the art are reasons this problem has been attacked.

Much of the Department of Defense work in simulation has been in the operations area, such as pilot and communication operator training. The maintenance training area has been largely ignored because of the belief that a maintenance simulator needs to be a 100 percent duplication of the end item to be effective. Kargo and Steffen[3] have designed and built a computer assisted performance training carrel, and their conclusion was "The system as developed has proven to be feasible for use in performance training and could be expanded to simulate larger and more complex circuits used in higher level courses."

A United States Navy study[4] in 1978 advocated "providing an alternative to the use of operational equipment for intermediate level maintenance training." Literature[5] indicates that no further work has been undertaken on this project. Maintenance simulation as an end item alternative can potentially save large amounts of money when applied to high cost systems, such as radar sets, weapon control systems and power systems.

Electronic maintenance simulation is desirable, and has been for some time.[6] Lack of capability to cheaply produce circuit waveforms for electronics training (i.e., dynamically-controllable, high-speed complex outputs) has prevented maintenance simulation from achieving widespread use. Industrial system control concepts - using large scale integration (LSI) devices such as: eight bit microprocessors [6,7] and cheap transistor memory devices - have changed the picture drastically in favor of maintenance simulation.

Purpose

The specific purpose of this project was to develop a microcomputer-controlled trainer. The vehicle chosen was the AN/TPS-43E radar set. (See Figure 1.)

Objective

The objective is to perform a design study to demonstrate the feasibility of using maintenance simulation for electronic maintenance training.

Scope

The scope of this project will be limited to designing and constructing a maintenance simulator covering the tasks of the Built-In-Test Equipment (BITE). This is illustrated to the right of the operators in Figure 1 and shown, as actually constructed, in Figure 2. The particular training area that is being investigated is major component replacement maintenance; however, the investigation is not limited to just major component problems. Point-by-point circuit tracing can be easily simulated. This simulator not only reads analog inputs but also is able to create analog outputs which heretofore have only been possible using a mini or a full scale computer.

Documentation specifications of the BITE which the computer driven trainer must mimic came from the documentation available from Westinghouse through 3395 TCHTG/TTEOR on the AN/TPS-43E radar set. The work done was specifically in coordination with the training division at Keesler Technical Training Center, Biloxi, Mississippi, where the E3ABR30332 000 course is in preparation to be taught. The beginning date for the course to use this trainer will be April of 1979.

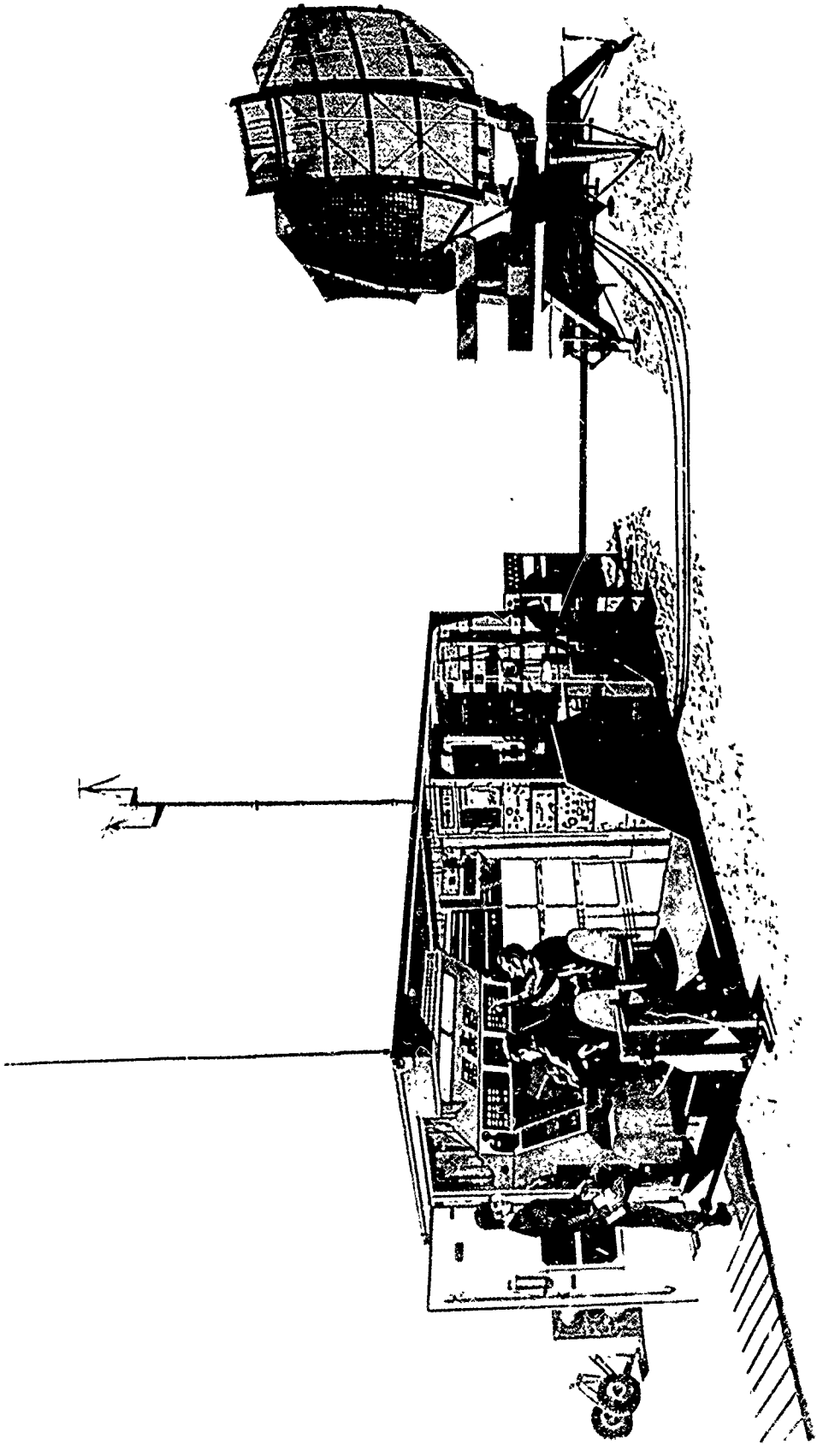


Figure 1. TPS-43E Radar Set

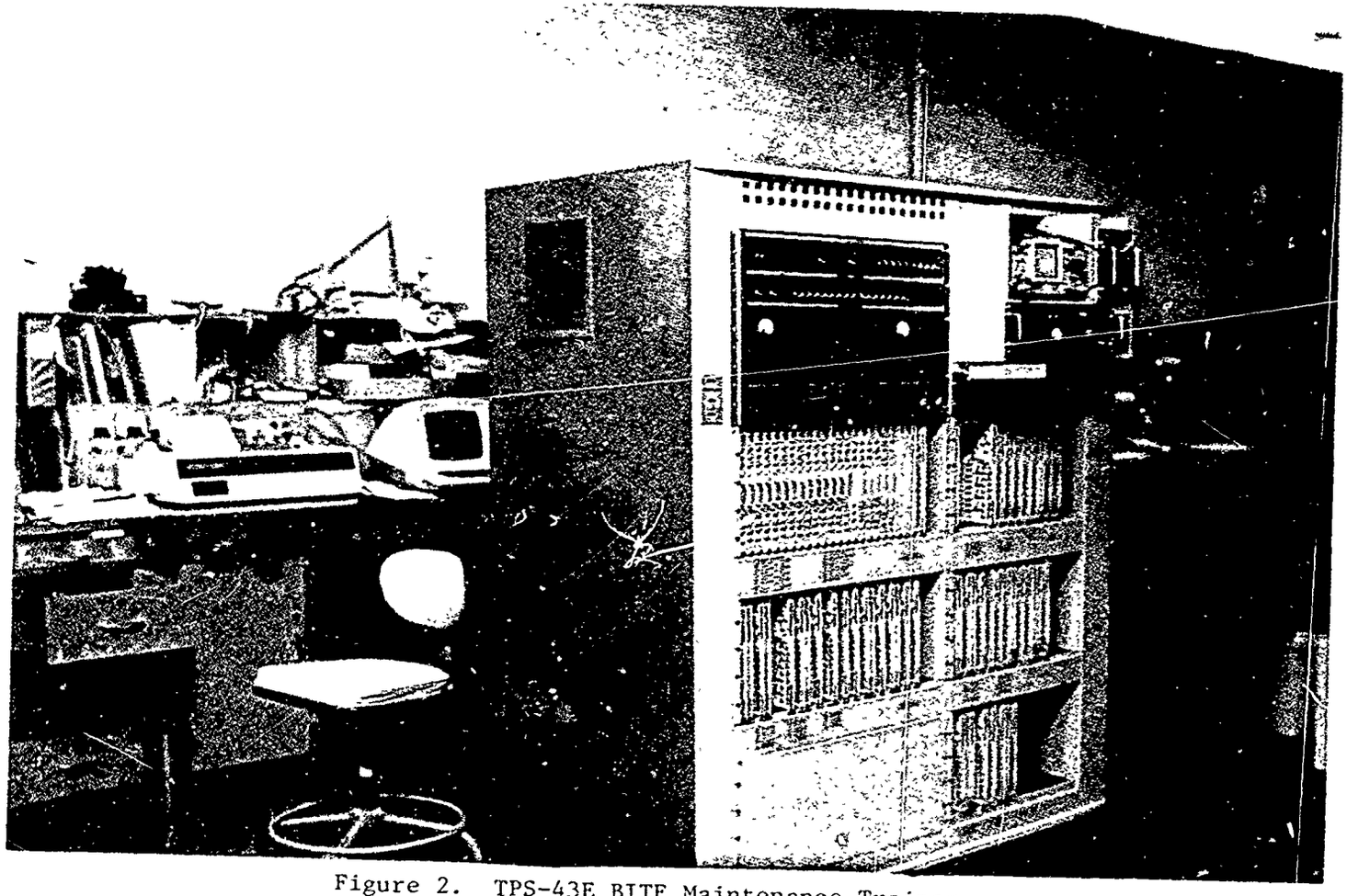


Figure 2. TPS-43E BITE Maintenance Trainer

In brief, the rest of this document is composed of four main divisions: (1) Performance specifications in Chapter 2, (2) Selection of Equipment in Chapter 3, (3) Design Implementation in Chapter 4, and (4) Conclusions in Chapter 5.

Chapter 2 deals with the performance specifications that the maintenance simulator must meet. Methods of instruction, derived by the instructional systems development (ISD) process of course construction, are implemented using a judicious choice of commercial and locally manufactured hardware and software. The tradeoffs of "cost to develop" vs "cost to purchase" are examined and explain the early decision to develop only a limited group of electronic equipment capable of interfacing the greatest number of trainers to the greatest number of microcomputer vendors at the lowest prices and with the greatest ease. As a consequence of the constraints noted above, detailed specifications of hardware and software essential for the design and development of this project are presented in conjunction with the performance specification in Chapter 2 rather than with the selection of equipment in Chapter 3.

Chapter 3 develops the selection of equipment from commercial sources. Technical criteria are evaluated in light of the performance specifications of Chapter 2. Institutional constraints imposed by the Department of Defense (DOD) and the United States Air Force (USAF) are described. Due to the number of criteria and commerical vendors, a decision matrix is used to give each vendor's wares a figure of merit (FOM) useful in the final procurement decision.

Chapter 4 is an annotated operations and maintenance manual of the hardware and software locally developed for this project. Careful

consideration is given to the interface of each to the commercially selected equipment.

Chapter 5 states the conclusions of this work. A review of the institutional and engineering decision factors point to the actions required to provide electronic maintenance simulators in the future. Possible application of the products of this project are enumerated wherein the investment of effort is either largely or exclusively software.

A major effort of this thesis concerns the design and implementation of a programmable waveform generator (PWG) to provide one and two MHz data display rates. This PWG was essential because no single commercially available microprocessor can perform such output rates continuously and direct a microcomputer system at the same time. The PWG is therefore a self-contained output device slaved to the host microcomputer which gives the microcomputer the ability to output unlimited iterations of arbitrary waveforms.

Appendix A provides works accessible to the general public if specifically requested under the Freedom of Information Act. These attachments are volatile in nature and yet represented the grounds for the ISD process at the time of this work. Technological advances continuously redefine a military training system's effectiveness, or lack of it; therefore, the elements or the attachments provided may be obsolete when this work is published. Further information concerning the currency and availability of documents used as attachements to this work may be obtained by written request to Community College of the Air Force, Keesler Technical Training Center, Keesler Air Force Base, Mississippi 39530.

END NOTES

1. Keesler AFB Study, TTVET. Staff Study on the Feasibility of Using Simulation in Maintenance Training, 3 Oct 77

2. Boyle, E.B. Aircraft Armaments, Inc. Trends in Digital Simulation NAVTRADEVCEN IH-1B (1967), pg 39

   "Digital simulation, as used in simulation and trainers we know today, has followed directly from the larger analog simulators of the 1950s.

   "What was probably the first digital simulation system built for training purposes was the UDOFT, Universal Digital Operational Flight Trainer. This system, which was primarily an experimental device, was built by Sylvania under contract to NIDC. It provided much of the experience and education which led to the development of other digital system."

3. Kargo, Donald W. and Steffen, Dale A. Performance Training Carrel for Electronics Principles Course, Sept 76, AFHRL-TR 76-62(1), pg 1, Air Force Human Relations Laboratory

4. King, William J. Performance Specification for a Maintenance Simulator for the AN/ALQ 126 Transceiver, June 74, Technical Report NAVTRADEVCEN 74-C-0128-1 by Honeywell, Inc., ADA020588

5. Defense Documentation Center. Simulation and Training, 2 Feb 78, A Report Biblioghraphy prepared by Defense Documentation Center Defense Supply Agency, Cameron Station, Alexandria, Virginia

6. Boyle, E.B. op. cit, on citing "Simulation Computer Specifications", notes that MIL-STD-876, which USAF is responsible for, permits only second generation medium and large main frame computers to meet requirements. He noted, "While these requirements will be met for all systems of medium and larger sizes, there seems to be some possiblity that some simplification ..." will be required for "...systems of very small size in the next decades." Ironically most mini and a few microcomputer systems meet MIL-STD-876, 11 years later. Pg 39

7. Boyle, E.B. op. cit. pg. 40

CHAPTER II

PERFORMANCE SPECIFICATIONS

General

The maintenance simulator is to be used to provide training to the U.S. Air Force 3-skill level. The "3-skill level" training required in the Air Force constitutes an apprentice level, a person capable of working under the direction of another more skilled person and not expected to work on his (or her) own.

Circuit card replacement is the highest level of maintenance required of the student and will be the student's capability at the end of this course. The student will learn to identify any given circuit which is not working within the radar set covered by the BITE. The student will then be required to identify, remove and replace any particular circuit card within a satisfactory time period and with a minimum of mistakes. Methods of training used during instruction are laboratory performance and class demonstration. The student will be placed in a BITE maintenance situation with a predetermined dysfunction within the equipment. The student will determine what the dysfunction is using standardized Air Force Technical Orders. Satisfactory identification is shown by removing and replacing the dysfunctional circuit card. Length of the course is 12 weeks.

Hardware

The hardware is organized into four major areas: (Figure 3) the microcomputer, the associated test equipment, the output circuitry, and the input circuitry.

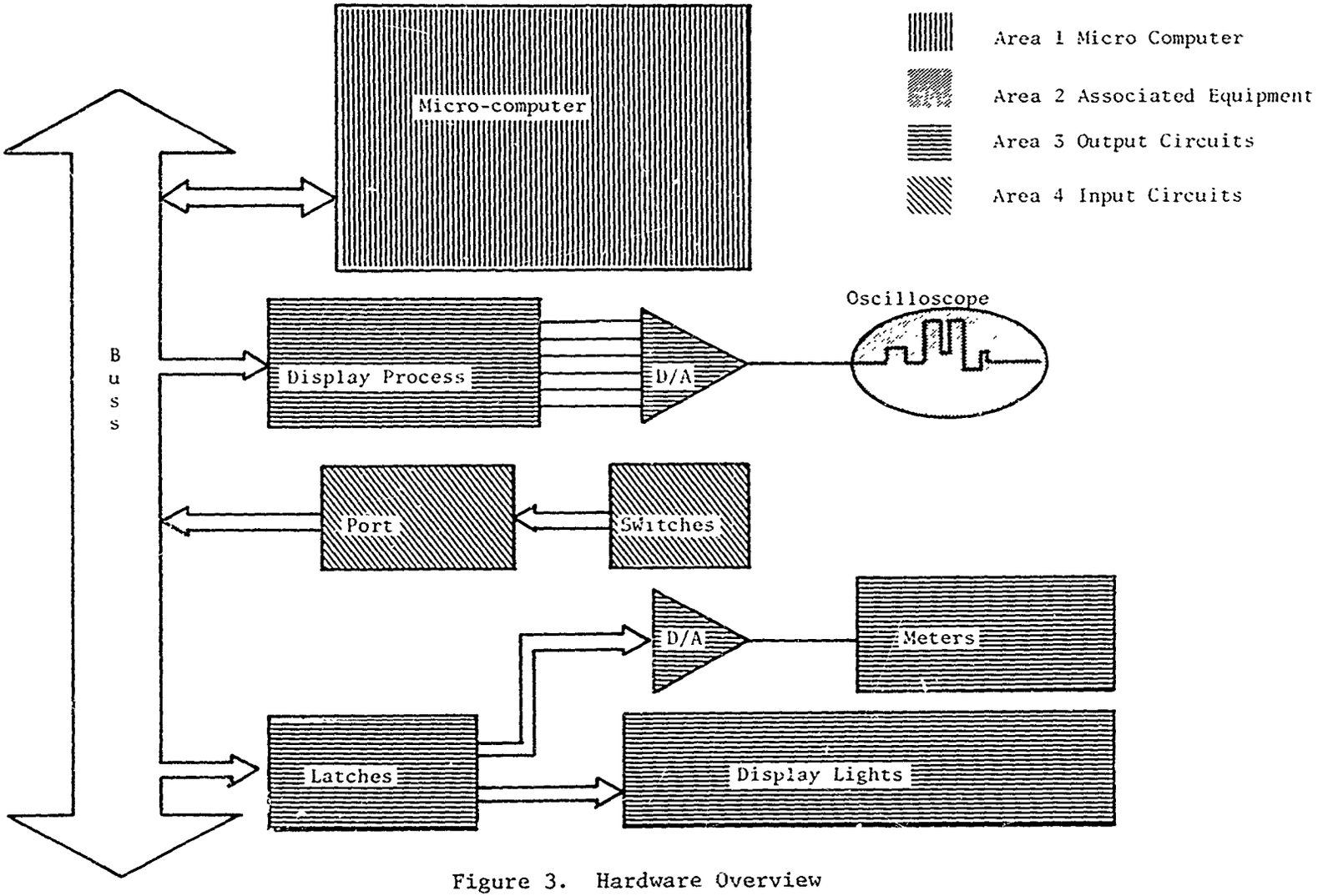


Figure 3. Hardware Overview

The first major area is the microcomputer (Figure 4). The computer's power supply should have the ability to power all the associated external digital equipment as well as its own set of internal digital equipment. The operational clock of the computer should be switch selectable at 2 or 4 MHz to accept slower memories. Faceplate access and rack mountable design are desired to simplify cabinet engineering design. The computer should be one of several commercially available and should be capable of directing all the functions necessary within the trainer to achieve the general performance specifications previously outlined.

The second major area is the associated test equipment (Figure 5). Associated test equipment consists of a Tektronix Triservice 100 MHz Dual-Trace Oscilloscope and two faceplate meters. The oscilloscope is the actual radar maintenance oscilloscope. Considerable training results by using this instrument; therefore, the maintenance simulator emphasizes using the actual test equipment where economically feasible.

The third group of equipment is the output circuitry (Figures 6a and 6b) which creates the necessary displays on the oscilloscope and faceplate devices. The output devices have been designed at Keesler Training Services Branch, Keesler Technical Training Center (KTTC), since it was not cost effective to purchase comparable equipment.

Fixed pattern waveform generators have been available for some time, and nonfixed pattern programmable waveform generators have become available recently.[1] The former are unsuitable to the dynamically-controllable complex waveform application and the latter cost between $3,000 and $25,000 per unit. The 3AZR30352 003 course requires two (or

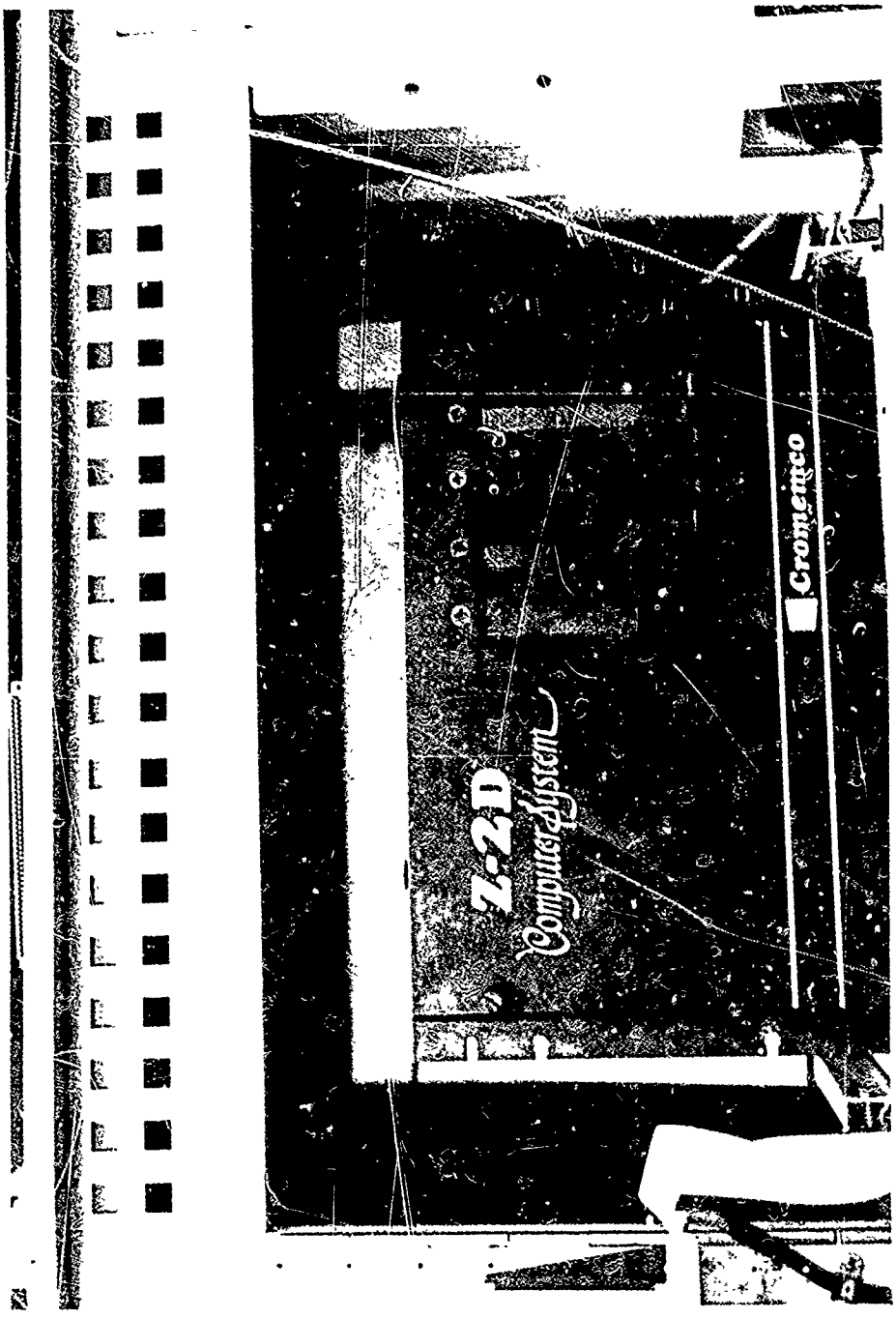


Figure 4. Computer With Disk Drives

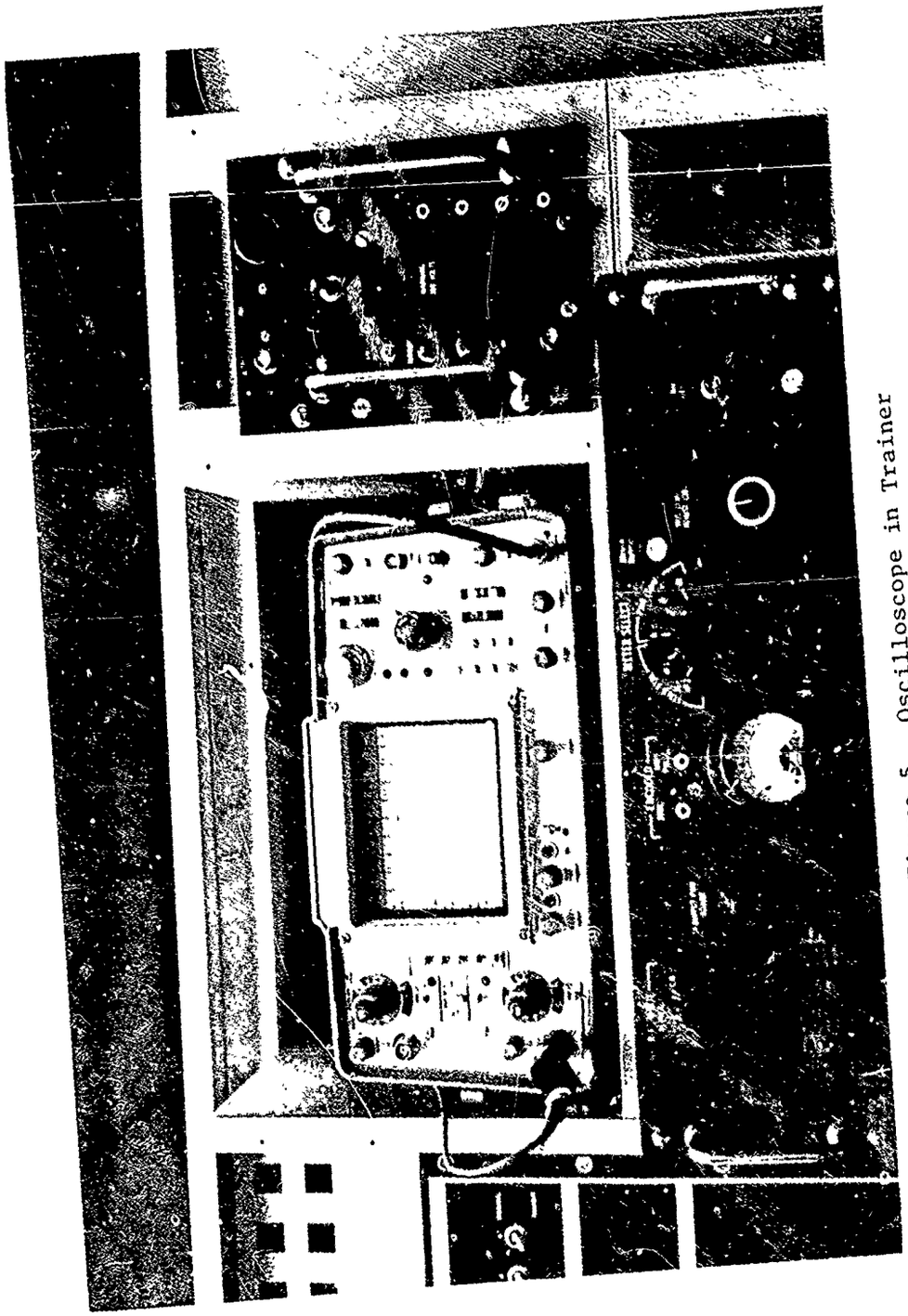


Figure 5. Oscilloscope in Trainer

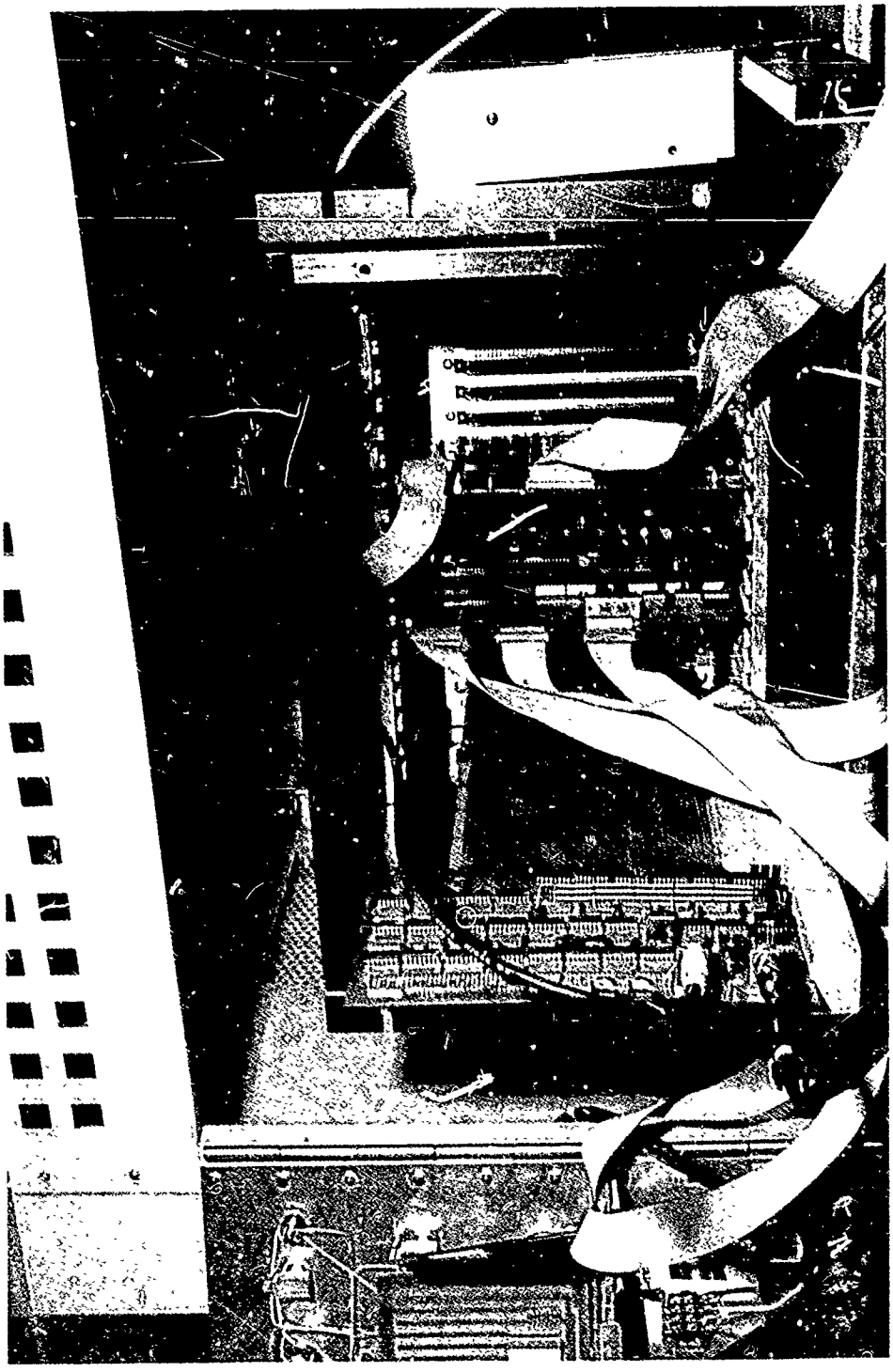


Figure 6a. Programmable Waveform Generator on Extender Card

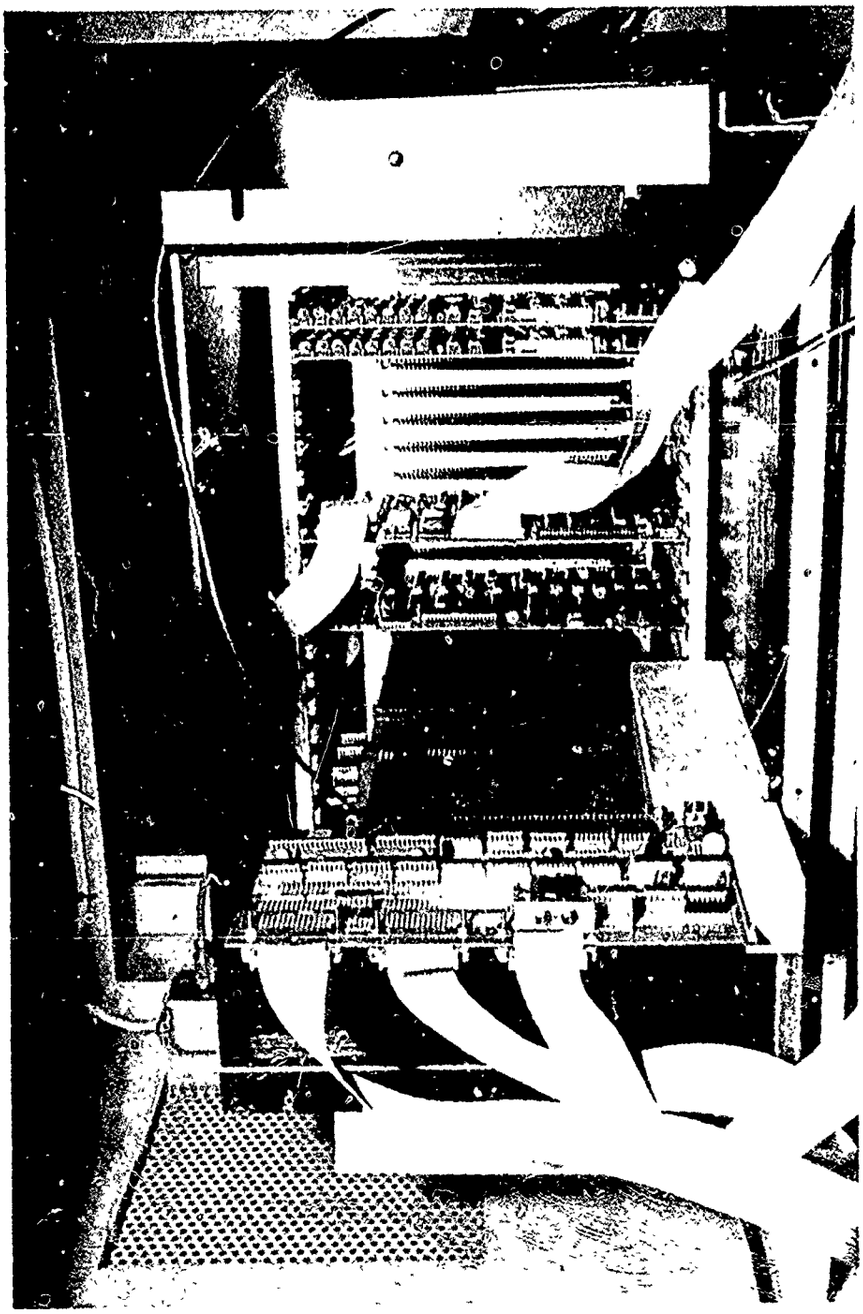


Figure 6b. Input/Output Controller on Extender Card

more) extra simulators necessitating at least three of these instruments. The cost to develop the display hardware is approximately the same as it would be to purchase two ;ess capable commercial instruments. Training Services expects to make more than two waveform generators which justifies the local design effort.

The devices that output to the faceplate are simple to design and do not justify purchasing. Simple addressable latching devices enabled from the input device, described below, provide controlled value inputs to two digital-to-analog (D/A) converter input meters and 15 indicator lights.

The fourth major group of equipment needed must be able to input those things that the student is investigating via the BITE simulator switches. For the computer to be able to recognize these actions, it is essential to have an input-output (I/O) device utilizing the trainer's faceplate and card cages as if they were the computer's keyboard and display (Figures 7a, 7b and 7c). Instead of using a terminal, the functional training equipment concept shall be implemented by designing the I/O device to sequencially scan the switches and senseing their states. Devices, to input data shall include various kinds of switches and an A/D converter. There will be over 105 inputs available between the faceplate and the card cages. This gives the possibility of 105! combinations and permutations.

The training cabinet shall be a locally fabricated box (Figure 8) containing the rest of the equipment. The faceplate shall be a duplication of the face plate on the actual radar set. Instead of purchasing the radar faceplate from Westinghouse, Training Services

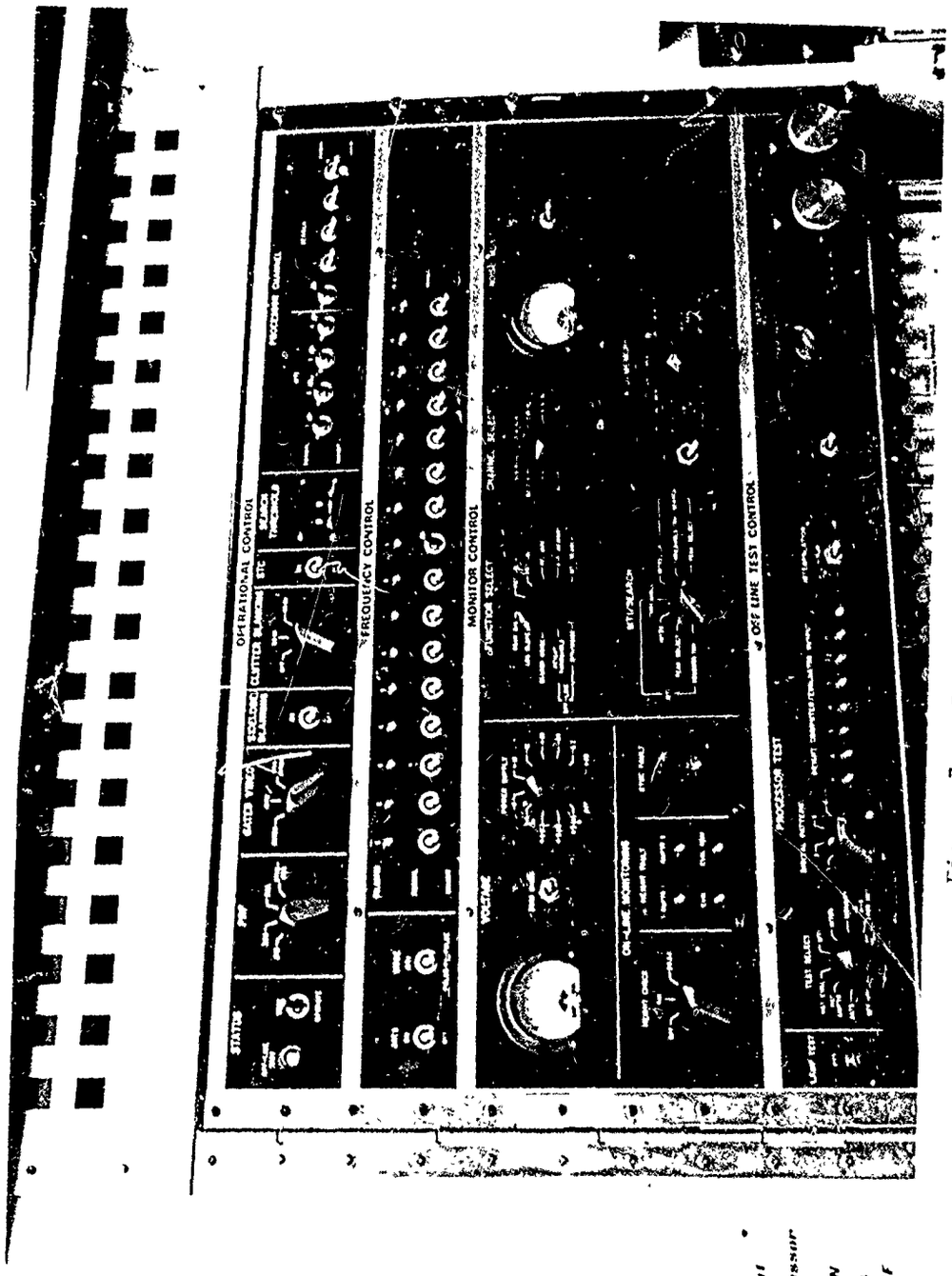


Figure 7a. Faceplate

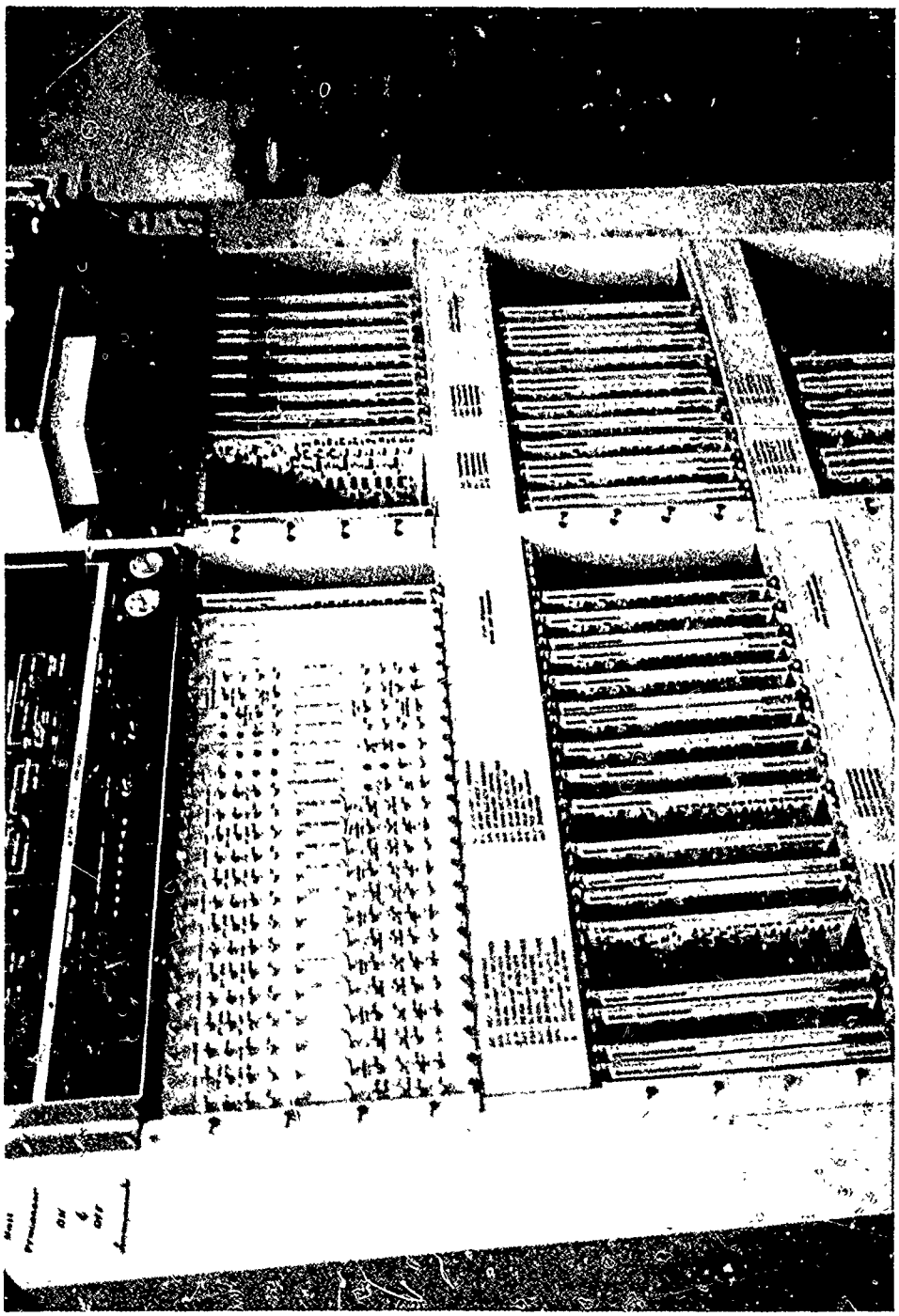


Figure 7b. Trainer Card Cages

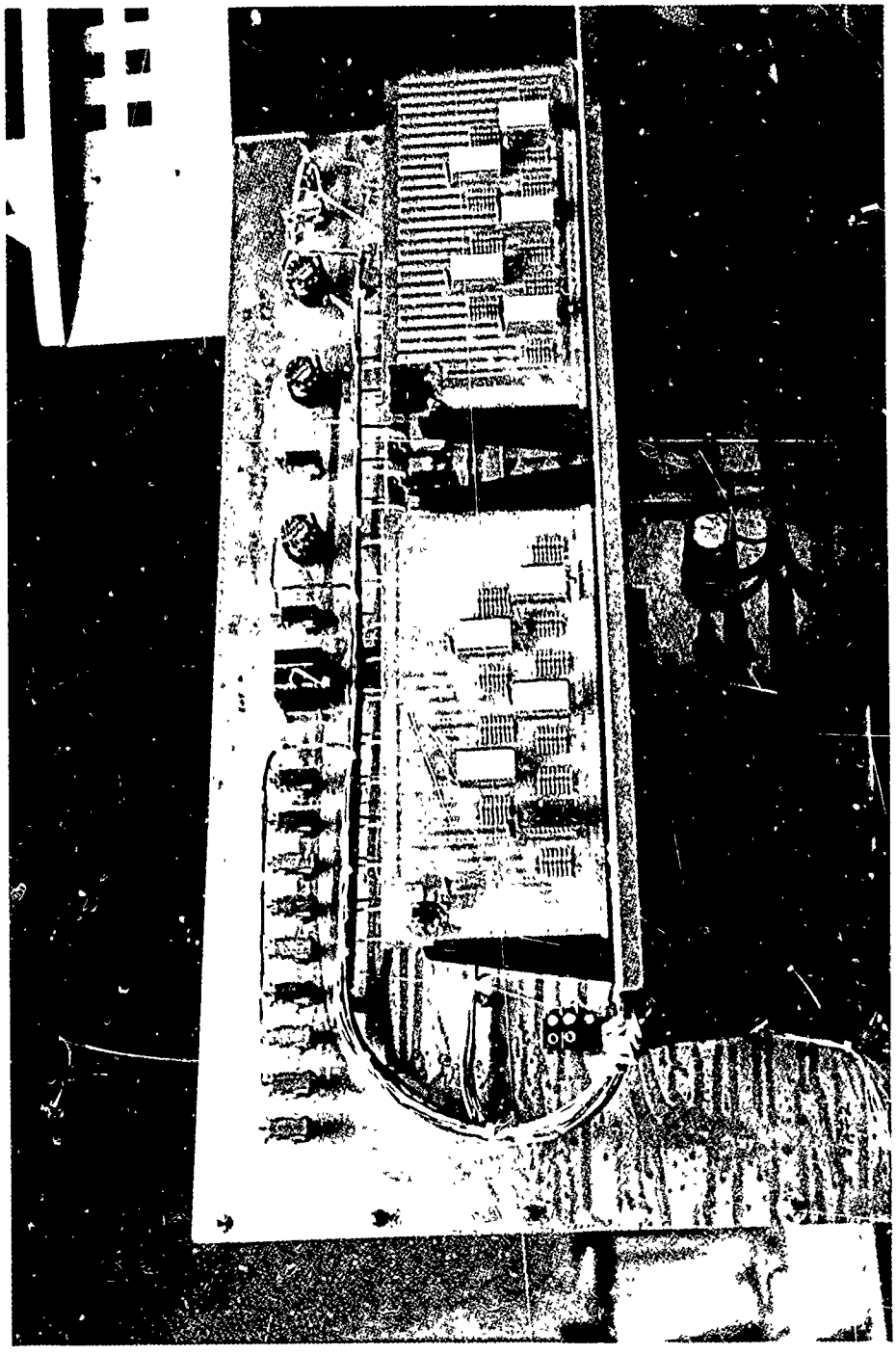


Figure 7c. Faceplate MUX Input Circuits

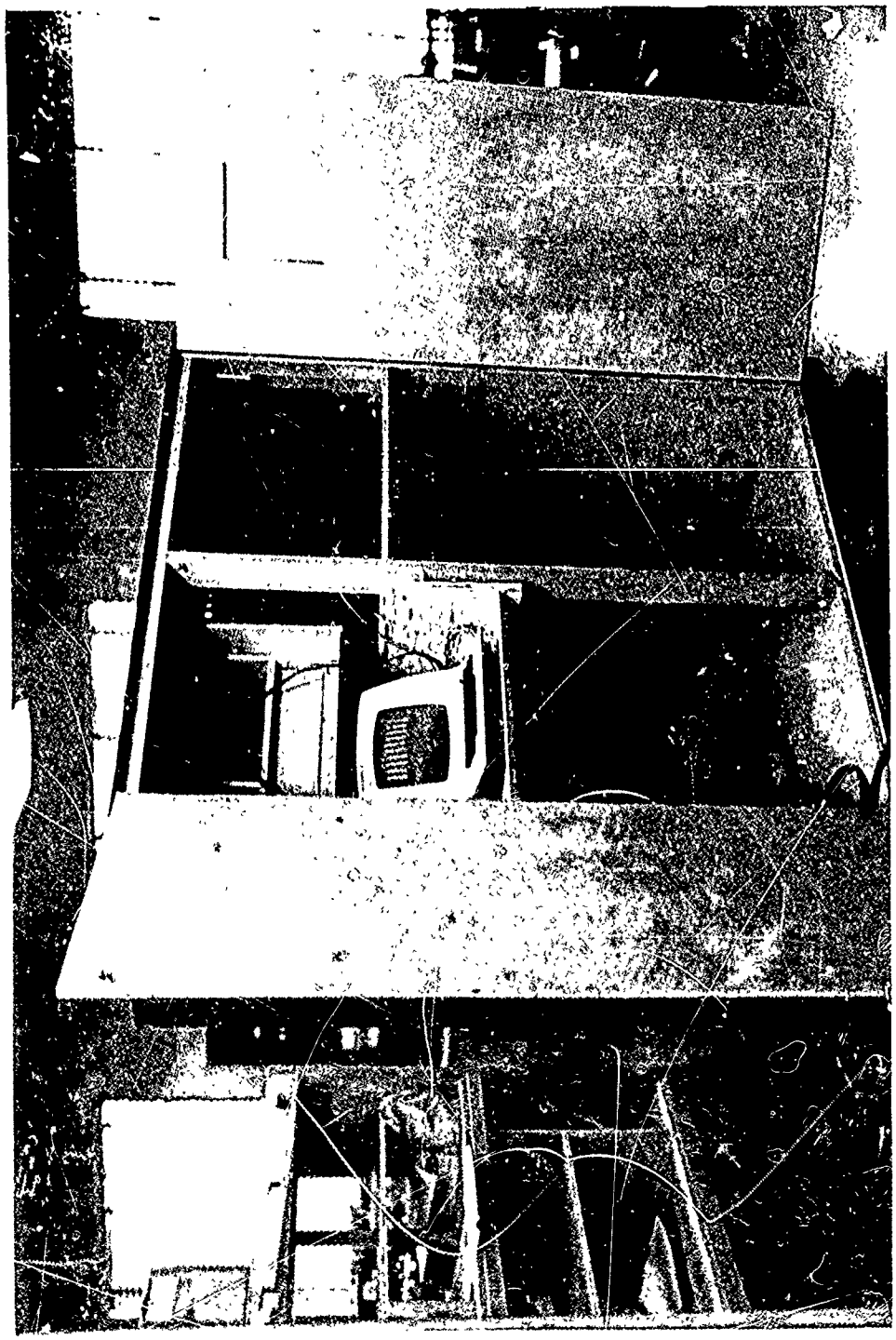


Figure 8. Rear View of Trainer Cabinet

Division shall design and photoprint one using metal photometal techniques that are available at that facility.

The Cabinet Electronics (Figures 9a and 9b) shall be defined as the electronics to which the computer I/O hardware is attached. These include various kinds of lights, relays and connective wiring. These electronics should also be able to read a potentiometer's analog data and convert it to digital data compatable to the computer. The faceplate in the cabinet shall be used as a chassis to hold an A/D converter.

Software

The software falls into two classes - that which is commercially available and that which shall be developed by this project. By selecting a fairly comprehensive microcomputer system, software available should include an ANSI Standard FORTRAN[2] compiler, a Relocatable Assembler, an Extended Basic, a Link Loader, an Editor, a Disk Operating System, a Disk Loaded Monitor (with a disassembler and in-line assembler), and a Power-on Monitor in read only memory (ROM). The latter will allow the user to be able to start a user program without intervention on a terminal. Developed software shall consist of the program BITE and some hardware and software maintenance programs.

Of all the software needed for this project, the most useful will be a high level compiler. FORTRAN IV should meet this requirement better than other options and should prove an essential vehicle for timely completion of this project. The reasons FORTRAN should prove so valuable are (1) the trainer architecture should lend itself particularly well to a word (byte) oriented language, (2) execution time should be close to real time (subjective), (3) no assembler learning

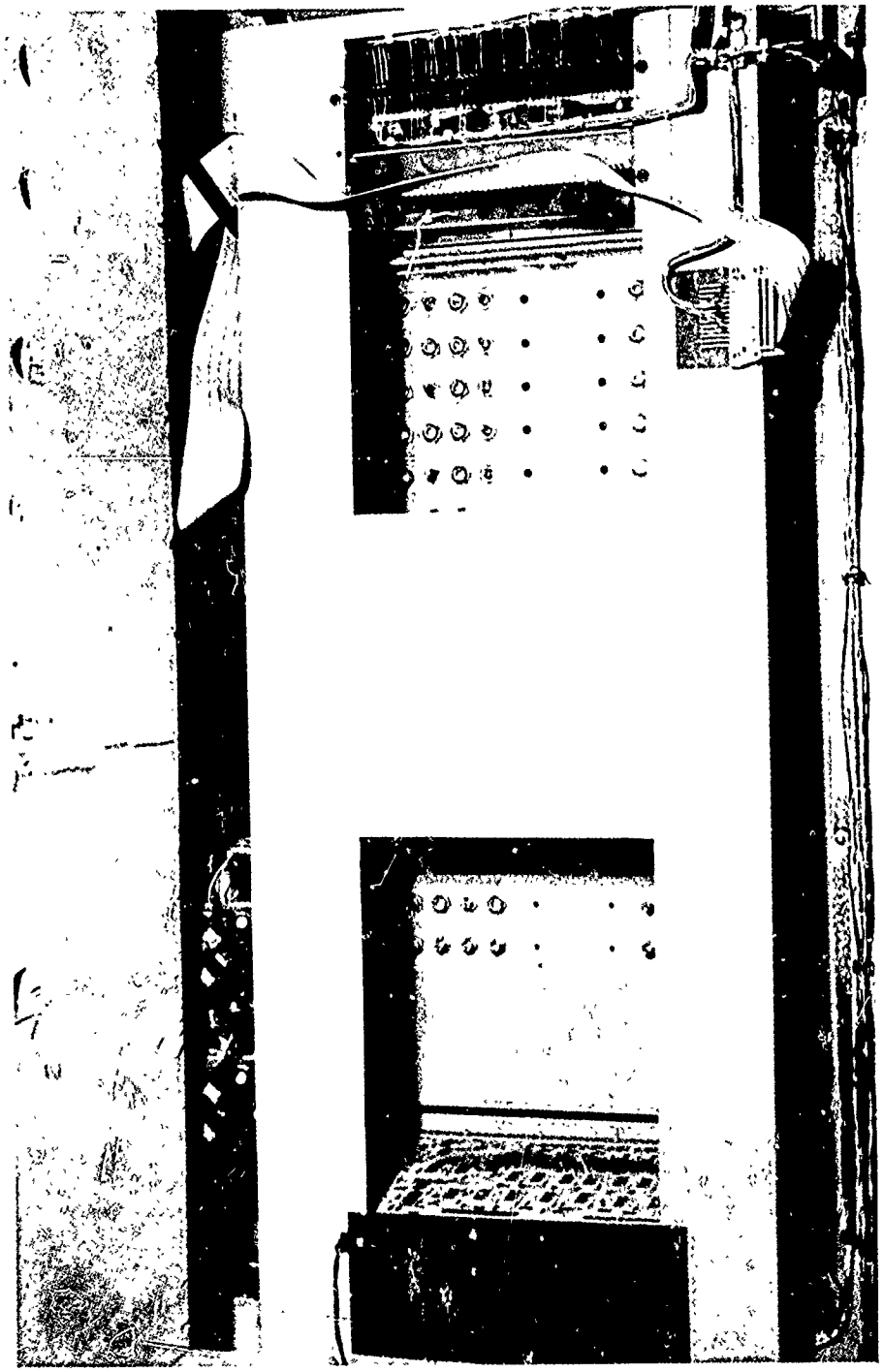


Figure 9a. Rear View Trainer/Input Card Cage

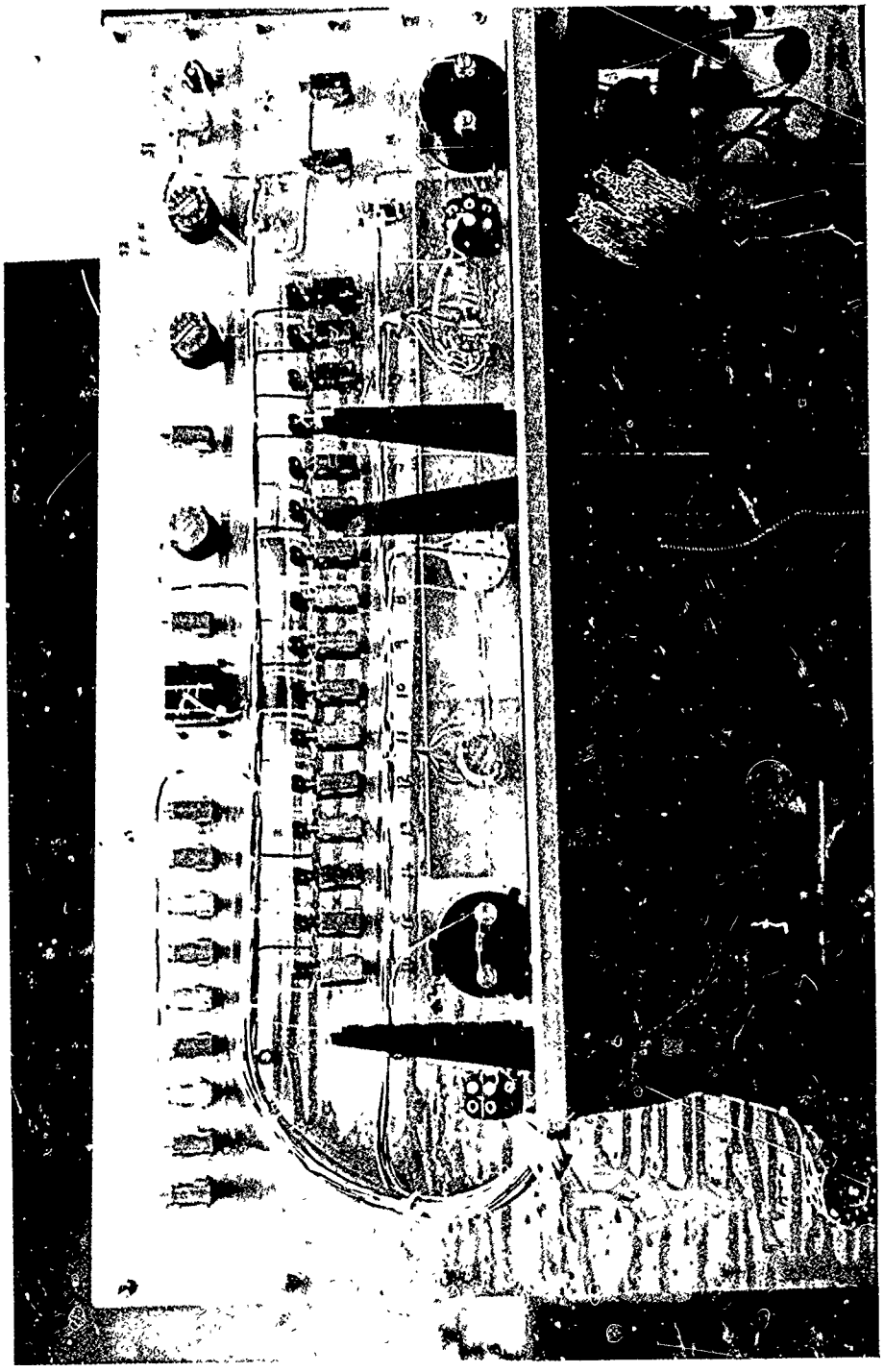


Figure 9b. Rear View of Faceplate

curve should be encountered, and (4) 32K memory will hold the object code.

Hopefully, the assembler, which must be conditional, relocatable, and macrocapable will prove unneeded in this project if the compiler is adequate. Various hardware test routines can be assembled by hand with the ROM monitor, or with the disk monitor, which does in-line mnemonic assembly as well as disassembly.

The Link-Loader should aid use of the FORTRAN compiler. One of its most desired features is the listing of undefined variables. This feature will identify all library subroutines used prior to the use of the FORTRAN library (FORLIB), and locate all undefined calls.

The Editor should be similar to on-line editors on Honeywell 6060 systems and the ZEROX Sigma 9. The full range of internal commands must be available within EDIT. External system commands are also desirable. While lack of external EDIT commands is a serious liability because there is no recovery from a bad disk write, careful consideration to this drawback can prevent the unintentional loss of large amounts of completed EDIT work.[3]

The Disk Operating System (CDOS) shall be a complete I/O system for many common peripherals. CDOS shall be designed to interface with 5-1/4 inch and 8 inch floppy disks as well as hard disks. RS-232 and parallel outputs must be provided to interface both a printer and a terminal. A single byte modification to CDOS should permit RS-232 signals to the keyboard-terminal to also go to a dot matrix printer with sufficient time delay to allow for a carriage return. This feature is to provide screen records.[4] CDOS must also contain a load-and-go capability once the system has been booted.

The ROM Disk Operating System (RDOS) must actually be a Power-on Monitor, activated by the reset function when the system is first turned on or when the reset is entered manually to the computer. Such an RDOS will wait for the keyboard to enter up to four RETURNS and use them as data to derive the baud rate of the terminal. Without the returns the cold boot mentioned above shall not occur. When a modified ROM[5] is used for RDOS with the baud rate already established, the entire system shall be cold booted to a user program from power on, or a reset. This particular feature will eliminate the use of a terminal in the trainer.

Project Developed

Among the project developed software, a variety of types of programming will be needed. The required programs will be a program control module, an input device control module, a tree search identify and decide module, an error insertion module and an oscilloscope picture output display/device module.

The program control module shall be a loop which centralizes the activities of the software. The various functions shall be called, as needed, and the student activities will be noted. Improper solutions, or unsafe (simulated) equipment operations, shall cause the oscilloscope to display the word NO, with no student recovery.

The input control module shall be a hardware control subroutine which selects the inputs from the training cabinet electronics. This module shall scan the multiplexed inputs, of the faceplate and card cages, sequentially and shall store the information, as found, for later evaluation. Evaluated input scans shall occur at a rate of no less than 30 times a second.

The tree search identify and decide module shall be a cascade search. Each of more than six switches, when taken in several possible orders shall provide up to 26 different pictures. Sixteen switches must be evaluated wherein each each switch has from two to ten possible positions. The natural order and multiple choices available at each switch are similar to telephone switching systems, which shall provide the model. Each switch shall be evaluated on a "DO CASE" basis which should progress very rapidly to picture selection.

The error insertion module shall be a subroutine which applies selected dysfunctions to the displays. The error conditions shall be dependent and/or independent. Error types are to include: changing correct pictures, and replacing one display with another.

The picture display program shall actually be a point display graphics subroutine. It must calculate enough points to produce vectors. Data will be passed encoded and PICTUR will decode it during picture generation.

Maintenance training requires that dysfunctions must be put into the equipment (real or simulated) so that the student has something to repair. In the past, designers were precluded from doing this with the real equipment because the malfunctions they wished to show could have done some harm to the actual equipment. With microprocessor controlled programmable errors, there is no particular reason to avoid catastrophic dysfunctions, making an error simulation module feasible. Project-developed software shall be able to handle a number of trainers. Requirements should be additional LBUF, MESUP and IPUT buffers, plus independent cabinet electronics.

END NOTES

1. Programmable Waveform Digitizers are now available, such as the Tektronix (7912AD) that connects to the IEEE-488 bus, as noted in Digital Design, Sep 77, Products Review. Cost is $22,000. Horizontal resolution (HR) is 512 points. Another is the HP 8170A available from Hewett-Packard (HP) with an HR of up to 4096 and speed up to 1 MHz; however delivery was not before late September 1978. Price is $5,430 for 1024X8 memory where each 1024X8 extra costs $545 as noted in Electronic Design, Vol 18, Sep 78, pg 149. While both test units are programmable, only the HP8170A is programmable to 4096 words; and it was not even announced until after the author's programmable Waveform Generator (PWG) was built and working in final form. Another problem with the T7912AD and HP817A is that both are only IEEE-488 bus compatible. Only the low production PET microcomputer is IEEE-488 compatable as of this writing other than HP computers of the miniclass.

2. ANSI document X3.9 - 1966

3. To prevent loss of a program, all editing work is done on an empty disk and transferred to a master disk on completion. Frequent down loading of the current file keeps modification re-edits to a minimum. The CDOS automatically maintains a backup file which is actually the old file, so the above procedures work reasonably well.

4. CDOS has a timing loop constant at location 7C7F (Hex) which normally contains ØØ (Hex). Replacing this with C5 (Hex) causes a pause of about one second which allows for a carriage return. This can be accomplished by typing in BYE at the CDOS level and then SM7C7F at the RDOS level. SM means substitute memory. When done, enter RETURN and

then GØ and another RETURN. This jumps directly to the already booted CDOS just modified.

5. The ROM modification is accomplished by replacing 5 bytes of the RDOS. Modification is done by loading DEBUG, then M (move) CØØØ S4ØØ (to) 1ØØØ. At location 1ØEE insert via SM 1ØEE: 3E 88 D3 ØØ C9. With the BYTESAVER TM on, make a new ROM at E4ØØ using slot 1 and the command P 1ØØØ S4ØØ E4ØØ. The code shown tells the computer it has a 12ØØ baud I/O device.

CHAPTER III

SELECTION OF EQUIPMENT

Two major areas of concern during the equipment selection phase were technical criteria and USAF constraints. Among the most prominent technical criteria were speed, cost, effectiveness, plug compatibility, reliability, vendor capability, and power. Among the USAF constraints were budget, submission procedures, device designation, engineering procedures, and maintenance after delivery.

Technical Criteria

The student expects a real time response. Therefore, speed of response is first in significance among criteria. Equipment is needed that will allow presentation of a display, or some other response, quickly enough to maintain comparability of the trainer's fidelity to the actual BITE. In Nov. 1977, the fastest complete microcomputer system available operated at 250 nanoseconds (ns) per clock pulse (using a 4 MHz clock) and using 12 clocks per instruction yields about 333,333 instructions per second. In the microcomputer area, this was approximately the best that could be purchased without considerable expense. A 2 MHz operation was acceptable.

The second criterion is cost. This project could not consider a computer in the minicomputer or the main frame class primarily because of the $20,000 total hardware cost ceiling imposed. The relatively low cost of microcomputers provided the only acceptable option for the project. Virtually all the microcomputer systems considered were within a $2,000 to $10,000 price range. The cost of the hardware

to be locally fabricated was initially estimated to be $5,000. The computer system selected had to be best in its class and still leave a reserve equal to its own cost in case of unforseen complications. This method of optimizing financial resources, and good luck, eventually resulted in $6,500 of hardware funds being saved.

The third criterion is user effectiveness. This is determined by whether or not the equipment is going to serve the training purpose and work well in the training environment. In the training situation simplicity of use is a major asset. Neither student nor instructor are expected to be computer qualified in any sense of the word; therefore, the software-hardware mix must function with the ease of a television game to be effective.

The fourth criterion is plug compatibility. Plug compatibility is used here to mean that a computer will take add-on equipment from a variety of vendors. It would be impractical to purchase a computer supported by one, or at the most, only a few vendors. Such vendors represent a single source market and could consider their prices from the captive market point of view. Even worse is the possibility that a sole source vendor could go out of business; i.e., vendor capability.

The fifth question is vendor capability. Is the USAF dealing with a vendor that has a relatively safe future? Some companies have closed their doors within a short time after opening for business. USAF could not afford to have a single business bankruptcy obsolete a considerable investment in training hardware. At any rate, the cost of development would have to be borne all over again when the next training simulator is made.

The sixth criterion is reliaiblity. If the equipment is going to be in use constantly in a student situation, it is expected to be on line almost continuously. Therefore a high mean time between failures is a virtual necessity.

The seventh and final important area is power. Economy of design makes it desirable to have a piece of equipment planned in such a way that there is only one power supply for all the computer related units. Looking at the computer's power supply and the amount of power that is required for the entire trainer, exclusive of the oscilloscope, it becomes possible to consider letting the computer provide all the power required. Meeting the entire trainer's power requirements implies a large and reliabile power supply.

USAF Institutional Constraints

Air Training Command Regulation (ATCR) 50-221 provides that educational centers, such as Keesler Technical Training Center (KTTC), construct training devices as required, provided that they are "not available elsewhere." "Elsewhere" implies a series of concentric circles of search beginning with a check of existing and/or older modifiable devices. The circle of search then widens to the resources of other training centers and finally to all DOD training resources. When no satisfactory device is available from these sources, feasibility studies are instituted to look at the viability of alternatives.

The feasibility study is a staff report intended as an in-house evaluation of capability to produce and/or procure. In certain special cases, protctypes are authorized as an extension of the feasibility study. Such prototypes become design studies.

The feasibility study, if it has sufficient promise (Appendix B), can be considered for funding. If funding is approved, a schedule is submitted, along with milestones to be met (Figure 10). Personnel are assigned and reports are provided periodically by the project officer to the approving authority until completion, or curtailment, of the project. At completion, a final report is tendered. This document may also become an annex to that final report.

Usually the design study is undertaken to provide a statement of work (SOW) which defines the criterion the trainer must meet when subsequent copies are made. ATCR 52-332 requires that KTTC Training Services Division (KTTC/TTVET) meet the "functional statement of the requirement, specifications and statement of work. . ." of the requestor. In this case the requestor was Headquarters Air Training Command, TTYR. The request was based on the continuing drive of DOD to reduce costs. A design study, where resources permit, provides SOW guidelines for the whole class of devices within its scope.

Device designation and purchase procedures run parallel in training device design. AFR 300-22, paragraph 3e, requires "computers" be purchased through channels designed to control office data processing equipment and/or communications equipment. This project does neither. Instead the computer is designated as a training device component and falls outside those regulations and under Military Standard 876A, Digital Computing System for Real-Time Training Simulators.[4]

By virtue of the designation selected, the computer chosen cannot be used in any capacity outside of the trainer, but may be used as a module component in any number of different types of trainers. To

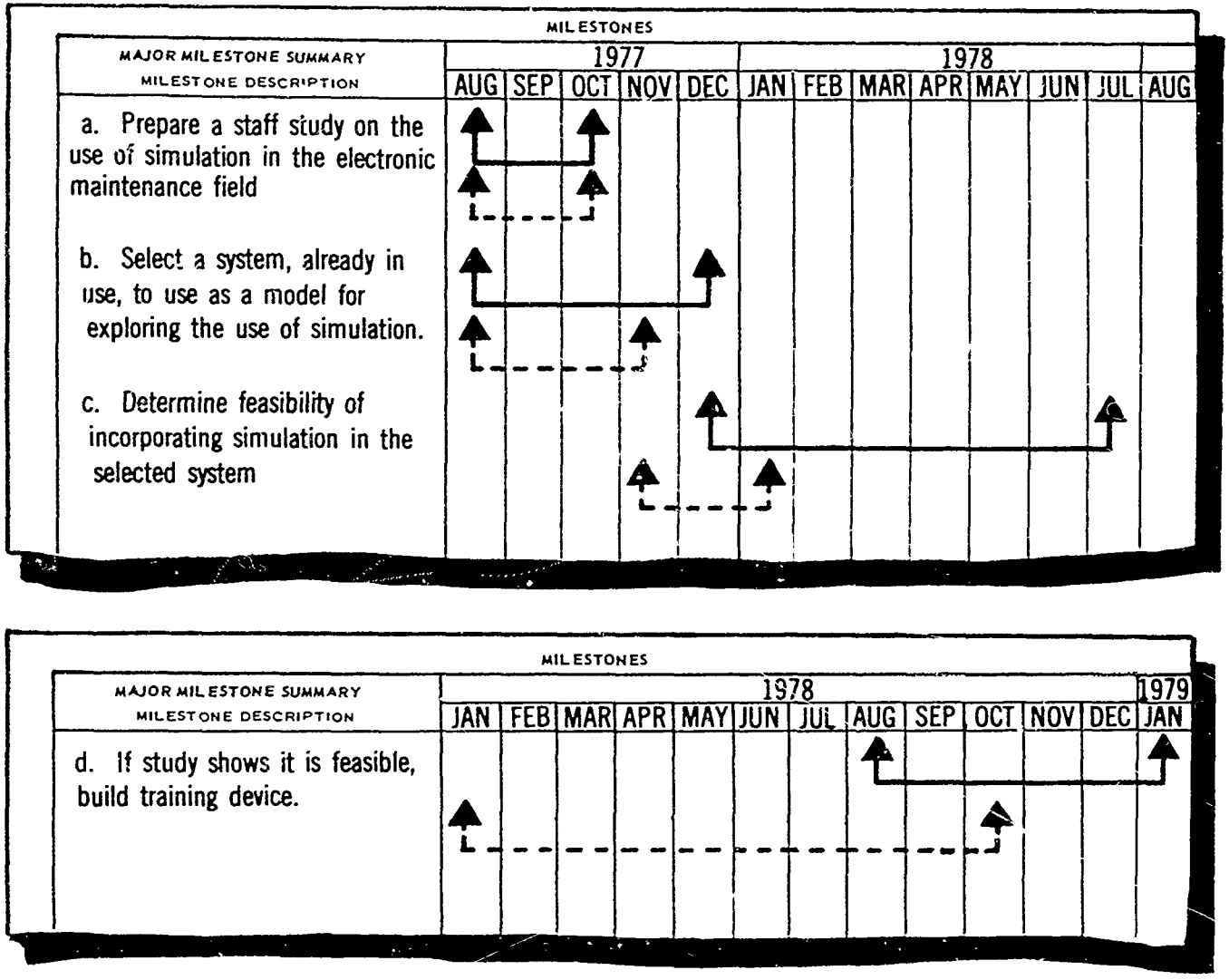


Figure 10. Milestone Chart

exploit the "trainer only" constraint, the system chosen needed to be easily moved from one type trainer to another and, when properly plugged in and the appropriate program loaded, be able to take control of the new trainer with no internal hardware modifications at all. Rack-mountable, totally enclosed front access equipment was indicated in this situation as well as "Power On" loading of software.

Engineering procedures require that the training device be reproducible from drawings and other documents. This could provide a "statement of work" if a large number of such trainers were to be made and contracts were advertised for bid. Simultaneously the engineering documents serve the maintenance personnel well in the event of a breakdown.

Commonly available components with many sources are used to prevent parts obsolescence. Competition among microcomputer and LSI-MSI component manufacturers provides a wide selection of circuits, application notes, technical articles and (surprisingly) personal computing source magazines, from which were extracted many of the solutions to the precise use of the elementary components used in the final design. Frequently the Government procurement system returns military standard substitutes for generically named parts, because they are already in the system. It is actually cheaper to use the more expensive part than to special order cheaper ones not in the system. When a part type is not in the system, and normal procurement channels prove to severely impede work, project acquisition priority is increased to permit ten day buy cycles. The ten day buy cycle starts with a three day computer aided search of resources DOD wide. Undeliverable parts from within resources are purchased on a competetive basis among supply

houses within 100 miles distance of Keesler. Due to the steady drop in the cost of LSI-MSl components an occasional windfall savings may be realized over the standard military inventory priced item. A good purchasing rule is to buy in lots of 10^+, 20^+, 50^+, and 100^+ wherever possible to get the volume discount. All basic components worked as advertised, whereas every major preassemoled unit failed due to poor assembly.

The major institutional problems encountered in this project were uncertainties caused by project funding and DOD reductions in force (RIF). The problem of funding revolved around budget planning. An error at headquarters level deleted the project money by forgetting to ask for it. Keesler Technical Training Center decided to use unsure local funding resources rather than drop the project thus causing continuous uncertainty. DOD reductions in force were two-fold: first was an impending potential for mass civilian lay offs caused by a study of methods to convert TTV into a contracted service. Second was a directive to reduce manning using attrition as a tool. The attrition positions were first allowed to absorb tenured civil servents RIFed for other causes. The positions were redesignated with a one pay grade reduction. A ranked list of applicants was to be sent to TTV from which a selection had to be made. Internal informal discussions led to the conclusion that by dropping and/or stalling lower priority projects TTV could accomplish more without training old substandard personnel than it could otherwise. Unsure money and insufficient people presented a formidable management challenge.

Maintenance is provided by the 2052 Communications Group who assure that during acceptance procedures the trainer is debugged of

conditions which could cause premature failure. Training Services Division, the designer/fabricator, provides maintenance procedures which are used by 2052 personnel to detect and correct problems that arise.

The Decision Matrix

In order to determine the relative merits of microcomputers to the task at hand, an extensive evaluation was needed. Both purchased and self-generated data sources were used.

Datapro's "All About Microcomputer Specifications"[5] was purchased. This source, while quite extensive, was disappointing in that many companies considered significant in the market were ignored, including the one chosen for this project. Since some of the technical information needed was also not included in the report, all the companies on the Datapro list were contacted. At the same time a canvas of the trade journals, such as BYTE, provided the names of about a dozen other companies.

Over 80 letters of inquiry were sent (Appendix C) asking for information considered needed to build the trainer. Fourty-four companies (Appendix D) responded with everything from tearsheets on future products to the complete instruction set of a new language supported by the vendor.

A program was devised (see Appendix E) which developed a figure of merit (FOM) for each of the 44 companies that responded to this author's inquiry. The equation used was:

$$Y = (I.B+K+N+L+D+P+W+C+S+N).R.A.O.T \qquad (1)$$

Where:

Y = Figure of merit (decision value)

I = Number instructions available (Basic Instruction set count)

B = Bus used by several companies (10 = yes, 5 = no)

K = Kit or preassembled (Yes = 5, No = 10)

N = Industrial use? (Yes = 10, No = 5, ? = Ø)

L = Logistical Support? (Yes = 10, No = 5, ? = Ø)

D = Documentation? (Yes = 10, No = 5, ? = Ø)

P = Sufficient power (Yes = 10, No = 5, ? = Ø)

W = Number of bits in a word (Actual Count)

C = Number of parallel ports up to 4 (Actual Count)

S = Number of serial ports up to 2 (Actual Count)

M = Nonvolatile memory? (Yes = 10, No = 3, ? = 0)

R = Total usefulness of software (Yes = 1, No = Ø: Boolean)

A = Total usefulness of peripherals (Yes = 1, No = Ø: Boolean)

O = Total usefulness of off-line memory (Disk = 5, M Tape = 3, P. Tape = 1: Boolean)

T = Software at all? (1 = yes, Ø = no: Boolean)

The rationale behind equation (1) is as follows: The number of instructions (I) a microprocessor has in its hardware is a count of the number of options available to a programmer without resorting to algorithms. All other things equal, each extra instruction that microprocessor A has that B lacks is equivalent to a custom-wired macro assembly subroutine in A. Given an upwardly compatible series of microprocessors, it is a virtual certainty that the more primitive members of the series will take both more instructions and more time to execute macros equivalent to instructions defined only on the more current members of the same series.

Different architectures do not compare easily, but comparison of clock cycle times shows that the smaller the number of instructions a microprocessor has (such as the MS 6502 vs the Z80), the smaller the clock cycle count, as a measure of time, needed to execute them. Yet, the smaller the working set, the greater the count of low order instructions needed to accomplish a high order function. Another place for comparison is where clock cycle times of two to one are found in competitive units, such as the 8080 vs the MC 6800. The fact not immediately evident is that the 8080 uses a 500 ns clock while the MC 6800 uses a one microsecond (us) clock, which causes equivalent individual instruction execution times to actually be comparable (being 2-12us and 2-9us, respectively).

Given equivalence in speed of instruction execution and instruction sets adequate to perform the tasks demanded, the greater the instruction repertory a micrprocessor possesses, the stronger a position it commands in terms of processing power.

Bits per word (B/W, encoded W) is both important and complex. The importance of B/W revolves around instructions and data formats. The complexity of B/W comes from the ingenuity of bit employment within the B/W CPU architectural constraint.

The importance of B/W is illustrated by the generalization that, for a given processor, instruction formats that are single word oriented usually execute much faster than those which use multiple word formats. The primary cause of this speed differential is the presence, or absence, of extra memory fetches. Short bit length words constrain the CPU architect to use a limited number of simple primitive operation codes (POC) and this in turn forces choice of either selected simple

POCs without a full number of register (or memory) variants, or multiple word POCs. The same argument applies to data formats. Each bit added to B/W increases the possible number of POCs, and/or register-memory variants, by a power of two thereby increasing speed of instruction execution.

The importance of B/W to ingenuity in CPU design becomes apparent when software is being developed. The ultimate POC system, i.e.; a Turing machine, theoretically could generate any conceivable software macro-primitive operation code, but the number of instruction steps would be prohibitive. The critical questions is: which of the macro-primitive operation codes, directly encodable in multi-bit CPU hardware, represent an optimum set to map onto the universe of user sets such that the number of instruction steps, per software macro-primitive, is minimal. The answer to this question is currently empirical and is best answered by matching the architecture to its employment. Within this constraint it is clearly evident that B/W are again a measure of the spectrum available of hardware macro operation codes.

B/W and the bus were multiplied together to give great weight to the software-hardware mix of the system. It is believed that the initial choice is critical to a system's potential and thus is internalized whence it may be brought to bear on other components effectiveness later on.

The Bus (B) assumes the S-100 as the defacto available standard versus the poorly accepted IEEE-488, as an engineering consideration that enhances the power of an instruction set whenever unusual interface requirements can be satisfied with "off the shelf code" rather than by special "in-house design."

Kit (K) verses pre-built deals with parts reliability. Experience indicates that kits contain component parts that were only checked during production (maybe) and may have an unacceptable failure rate. Preassembled systems have been (or should have been) tested for system operation. A system is not considered preassembled unless it has been run (burnt in) continuously for 72 hours.

Industrial use (N) is a measure of confidence, research, reliability and many other intangibles. Industrial use is difficult to measure; thus, a minor role was assigned to it. If a better measure could be had, the role of N would have been expanded to a major one.

Logistic support (L) is an estimate of deliverability of initial and support equipment on demand. The rule elected in this project was to look at the numbers and locations of authorized outlets for sales and/or repairs along with warranty procedures. If logistic support did not indicate a 14 day repair cycle, or a seven day acquisition cycle, from identification of a defective board to its replacement, then the support was considered weak. Weak logistic support, in the technical training school environment, amounts to loss of training due to lack of facilities.

Documentation (D) includes the data provided on both hardware and software. Any system will fail repeatedly until its operators and programmers understand its capabilities and limitations.

Power sufficiency (P) is a useful and desirable feature that provides expansion capability. A system cannot grow easily when constant consideration to new power design must be made. If power is adequate for growth the system may be put to multiple uses such that when one trainer no longer uses it another may be built that can.

Number of parallel (C) and serial (S) ports are related to the numbers and kinds of peripherals a system can support. Assuming controllers are available for each type of equipment in hardware compatible to the system, a minimum configuration, exclusive of keyboard and monitor, is:

- Four general purpose parallel I/O ports
- One port for magnetic bulk storage media (disk or tape)
- Two serial I/O ports for
  a. One RS-232 port for terminal and/or printer
  b. One TTL port, general purpose

Mass storage (M) is critical to the system, and was considered partially above under parallel and serial ports. In the present case, some form must exist, and its form is a multiple against the whole system's power. The ability to process data is wholly dependent upon access to the data. Therefore, mass storage is not only necessary for a small system to operate, indeed the amount (and type) are a measure of its sufficiency as well.

From the arguments above it is seen that all the elements other than the Boolian values RAO and T simply inflate the final value. With the elements B and I inside the parenthesis there is no likelihood that a value of zero could be generated there, thus the deciding variables are R, A, O and T.

Total usefulness of software (R) is a summation of the various types of software available (Appendix E, lines 145 to 180) commercially. The software must run without any modification requirement to the rest of the system.

The total value of peripherals (A) looks at company supplied peripherals, or plug-in support from peripheral vendors. The particular peripherals examined are: monitor, keyboard and printer. Lack of a clear ability to use any of these immediately precludes a decision value other than zero.

Total value of Off Line Memory (O) looks at which storable memory media are available. Disk ranks highest and paper tape ranks lowest. Since these values are additive, the more, the better because each medium available becomes a source of software input other than that which the vendor supplies.

The variable (T) is another Boolian factor concerned with any available software. The requirement of meeting completion dates precludes developing the development software of the vendor's system.

Equation (1) states that a system's effectiveness, i.e., its usefulness, is equal to the sum of its features and directly proportional to the number of ways and ease with which these features may be manipulated to perform useful tasks for the system's owner.

For the small system user who has immediate engineering and/or industrial controlling in mind, the above evaluation should prove useful. It is not supposed that this is an ultimate or even a reasonable algorithm. Rather this is a convenient and reproducible method to evaluate many systems using an arbitrary yardstick.

The problem of discrimination became simpler as the simulator requirements became better defined. The ISD process, during course construction, identified the requirements of classroom usage. In the classroom the trainer needed to be quickly and easily loadable with the trainer program, have close physical and operational fidelity to the

BITE, have simple power requirements, and be easily moved from one room to another.

The ISD requirements led to the idea of a box on wheels that used a single 120 volt AC supply. The box should be completely front loadable and controlled. Program loading could be either cassette tape or 5 inch floppy disk using an automatic cold boot system from power on or reset condition.

Discrimination from the design point of view required well documented, well known hardwares and softwares with proven good performance. If possible, software portability should be incorporated. These design views led to the 8080 and Z-80 microprocessors utilizing an S-100 bus. Acceptable languages would be FORTRAN, APL, Compiler BASIC and PASCAL.

The companies identified in Appendix D are, for the most part, producers of viable equipment for a variety of projects; however, only a few could meet the needs of the TPS-43E project. Table 1 is a list of the companies with a FOM of 100,000 or more.

At the time the decision was to be made, only companies with deliverable products were considered. Deliverability was determined by the written advertisements asked for in the letter of inquiry. Presumably those companies choosing to deal with the USAF answered the inquiry, those not answering were considered de facto, undeliverable.

At this point it should be interjected that purchase procedures require competitive bidding for items such as a microcomputer, unless justification is available for a sole source purchase. Such justification was the result, not the object, of the decision matrix.

Companies	FOM	8080-Z80	S-100
Control Logic	133224	Yes	No
Cromemco	355104	Yes	Yes
Digital Equip	447768	No	No
EL Mem & Magnet Co.	182448	Yes	Yes
IMSAI	136640	Yes	Yes
MICRO KIT	162048	Yes	NO
MITS	184464	Yes	Yes
Processor Tech	157626	Yes	Yes
Radio Shack	192124	Yes	No
Zilog	262854	Yes	No

Table 1. Computer Companies Over 100,000

Companies	Processor	Software	Off Line Mem	FOM
Cromemco	Z80	34	6	355104
MITS	Z80-8080	24	9	184464
El Mem & Mgnet Co	Z80	14	8	182448
Processor Tech	8080	21	9	157626
IMSAI	8080	20	8	136640
TEI, Inc.	Z80	11	5	90145
E & L Instruments	8080	3	3	7551

Table 2. S-100 Companies

The only anomaly of Table 2 is Digital Equipment Corporation (DEC). This company offers the LSI-11/03 micro-processor which uses 16 B/W, and has over 400 instructions. The first problem this company presented was cost. DECs prices then were twice anyone else's and their bus is also nonstandard. More important than price, however, was the large number of competitive 8080/Z-80/S-100 companies. The latter was the deciding factor in not selecting DEC.

Tables 2, 3, and 4 clearly indicate that as of early 1978 the only standard bus was the S-100. The Z-80 and 8080 processors were the primary users of that bus. Since the Z-80 is upward compatible from the 8080, it is a logical choice of the two if all other factors are equal. The wealth of 8080 software available in print, from trade journals, and from vendors, virtually assured suitable software tools for either processor.

Of the other companies in Table 1, only Cromemco was in the same class as DEC. MITS had not begun sale of their announced FORTRAN compiler, and no one else had even announced one. BASIC, however sophisticated, is simply too slow for the application, and a BASIC compiler was not yet available. APL appears only in IBM equipment on SYSTEM-1, and, as yet, this system is beyond the acceptable price range. A FORTH interpreter was available, however when the author requested access to a demonstration given locally at NASA none was given. FOCAL and C were not available, nor was PASCAL.

The final decision was thus one based on computer bus, instruction set, and software tool standardization. The question of cost only concerned a few companies which were eliminated for the reasons mentioned above. As a result of the decision matrix, via the figure of

Companies	S-100
Applied Systems	No
E & L Instruments	Yes
IMSAI	Yes
INTEL	No
Micro Comp	No
NEC Micro Comp	No
Process Comp System	No
Process Tech	Yes
Pro-Log Corp	No
Wyle Comp Prod	No
MITS	Yes

Table 3. 8080 Sets

Companies	S-100
Control Logic	No
Cromemco, Inc.	Yes
EL Mem & Magnet Co	Yes
Martin Research	No
Micro Kit, Inc.	No
Monolithic System	No
Mostec Corp	No
TEI, Inc	Yes
Zilog	No
Radio Shack	No
Wave Mate	No

Table 4. Z-80 Sets

merit, a sole source purchase was justified to USAF Procurement Division.

END NOTES

1. ATCR 50-22 Training Services, 15 Apr 77, Change 1, 29 Jul 77, KTTC Sup, 29 Sept 77

2. ATCR 52-33 Operation of Training Services Activities and UPT Visual Services and Functions, 1 Apr 77, Change 29 Jul 77, KTTC Sup, 27 Sept 76

3. AFR 300-2 Management of the USAF Automatic Data Processing Program, 19 Aug 77, Change 1 (No date available)

4. MILITARY STANDARD DIGITAL COMPUTING SYSTEMS FOR REAL-TIME TRAINING SIMULATORS MIL-STD-876A (USAF), 8 July 1971, SUPERSEDING MIL-STD-876 (USAF), 21 February 1967.

5. All About Microcomputer Specifications, Datapro Research Corporation, 1805 Underwood Blvd, Delran, N.J. 08075, June 1977

6. Osborne, Adam, An Introduction to Microcomputers, Vol. II, Some Real Products. Osborne & Associates, Inc, Berkeley, CA. C. 1976

CHAPTER IV

DESIGN IMPLEMENTATION

Hardware

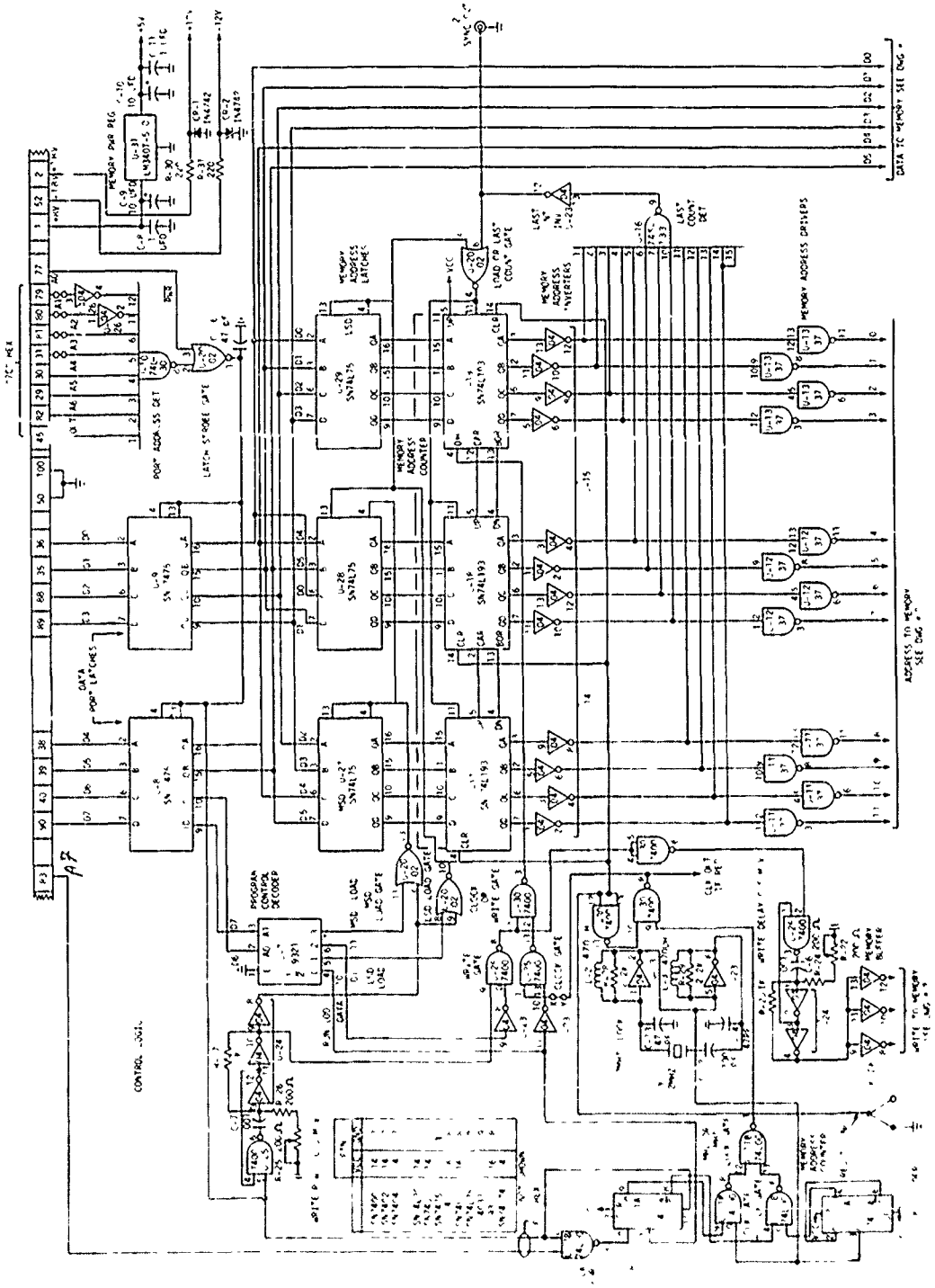
The main piece of hardware is the Cromemco Model Z2-D Microcomputer (Figure 4) which acts as a switching center for this Simulator/Trainer. Virtually all simulator activity is directed by the Microcomputer. All of the Trainer switches are read by the computer and all of the visual outputs are controlled by the computer.

The Programmable Waveshape Generator P.C. Board

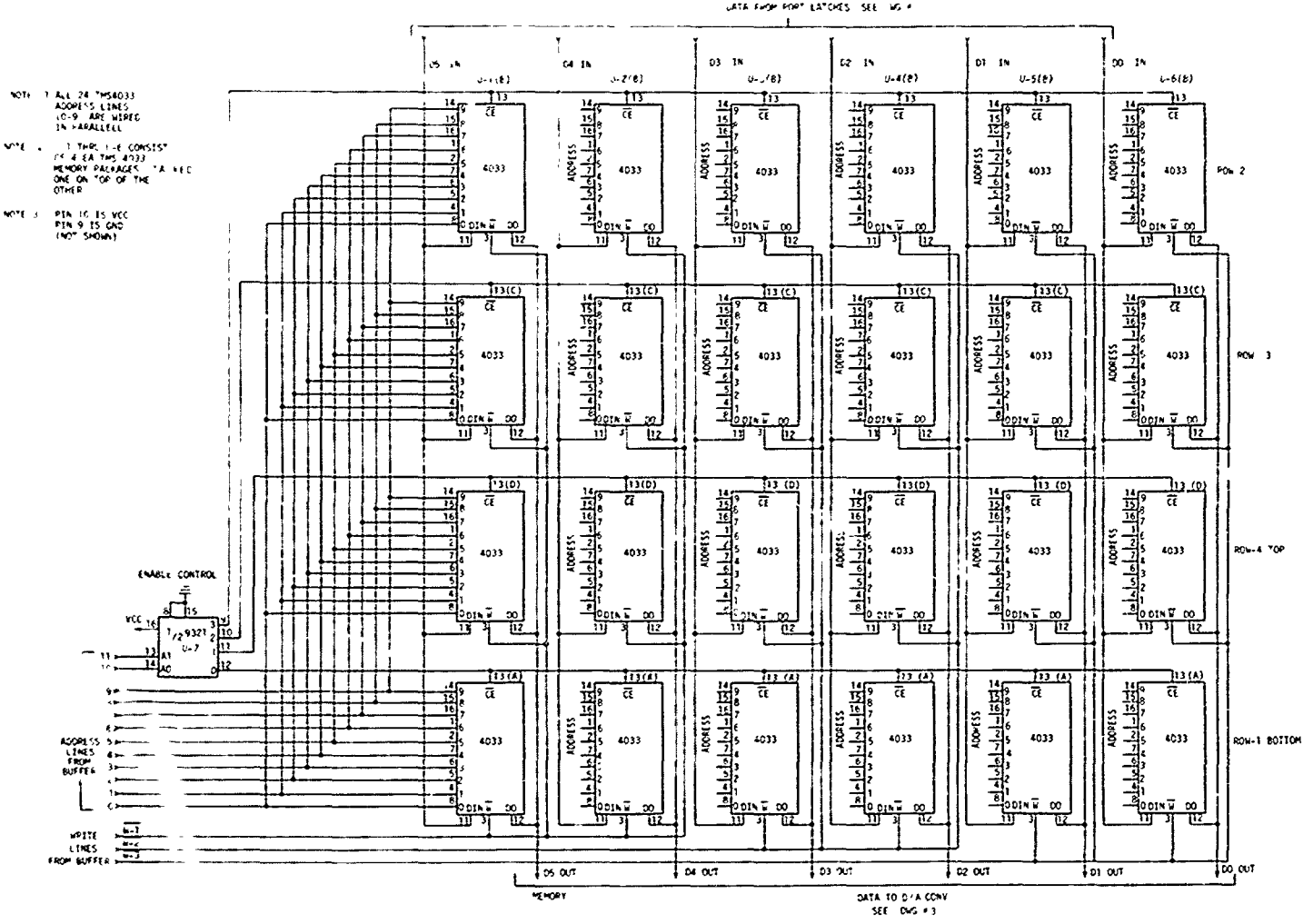
The Programmable Waveshape Generator (PWG) Card is located inside the Microcomputer. Refer to the three schematic drawings (Drawings 1, 2, and 3) of this circuit card. The PWG circuitry is port-addressed. It is capable of generating 64 analog voltages, from 0 to 5 volts in amplitude, in groups from one to 4096 pulses in length, and at rates of either one MHz, or two MHz. It is S-100 bus-compatible (a standard pin out configuration) and may be loaded, under computer program control, at continuous transfer rates of up to two MHz. The PWG, when Loaded and Enabled to run, operates independently of the computer unless action is taken to cause the computer to regain control.

The System Input/Output Interface Card

The System Input/Output (I/O) Interface Card (refer to schematic drawings 4 and 5) is a special purpose memory-mapped I/O controller, located inside the microcomputer. Four memory addresses are used to select the operation of the Data-Out-Port (U-7) and Data-In-Port (U-6) integrated circuits. The 8255 (U-7) uses Port A for



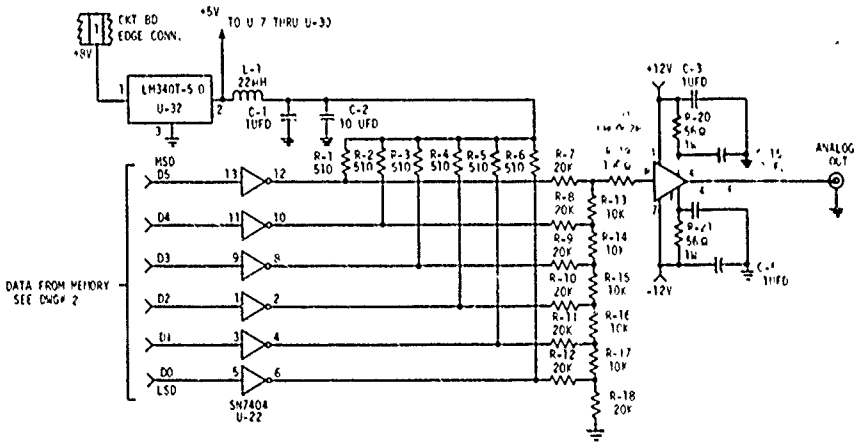
Drawing -1. AN/TPS-43E Simulator Programmable Waveshape Generator - Control Circuits



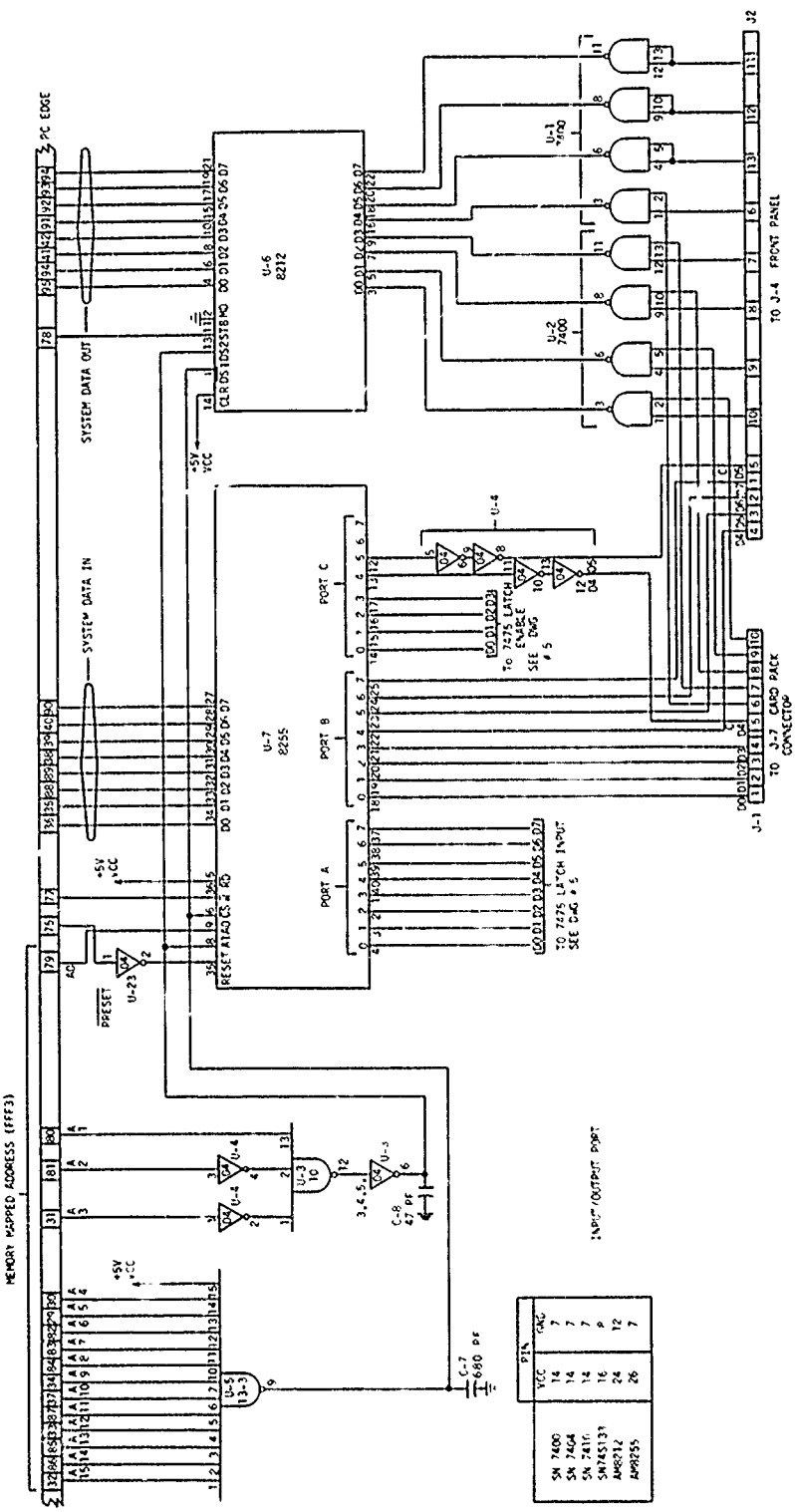
Drawing -2. AN/TPS-43E Simulator Programmable Waveshape Generator - Memory Circuits

NOTE 1 C-16 THRU C-39 (NOT SHOWN) ARE .01 CER DISC. DECOUPLING CAP. DISTRIBUTED THRU OUT THE POWER BUSS ON THE CKT BOARD

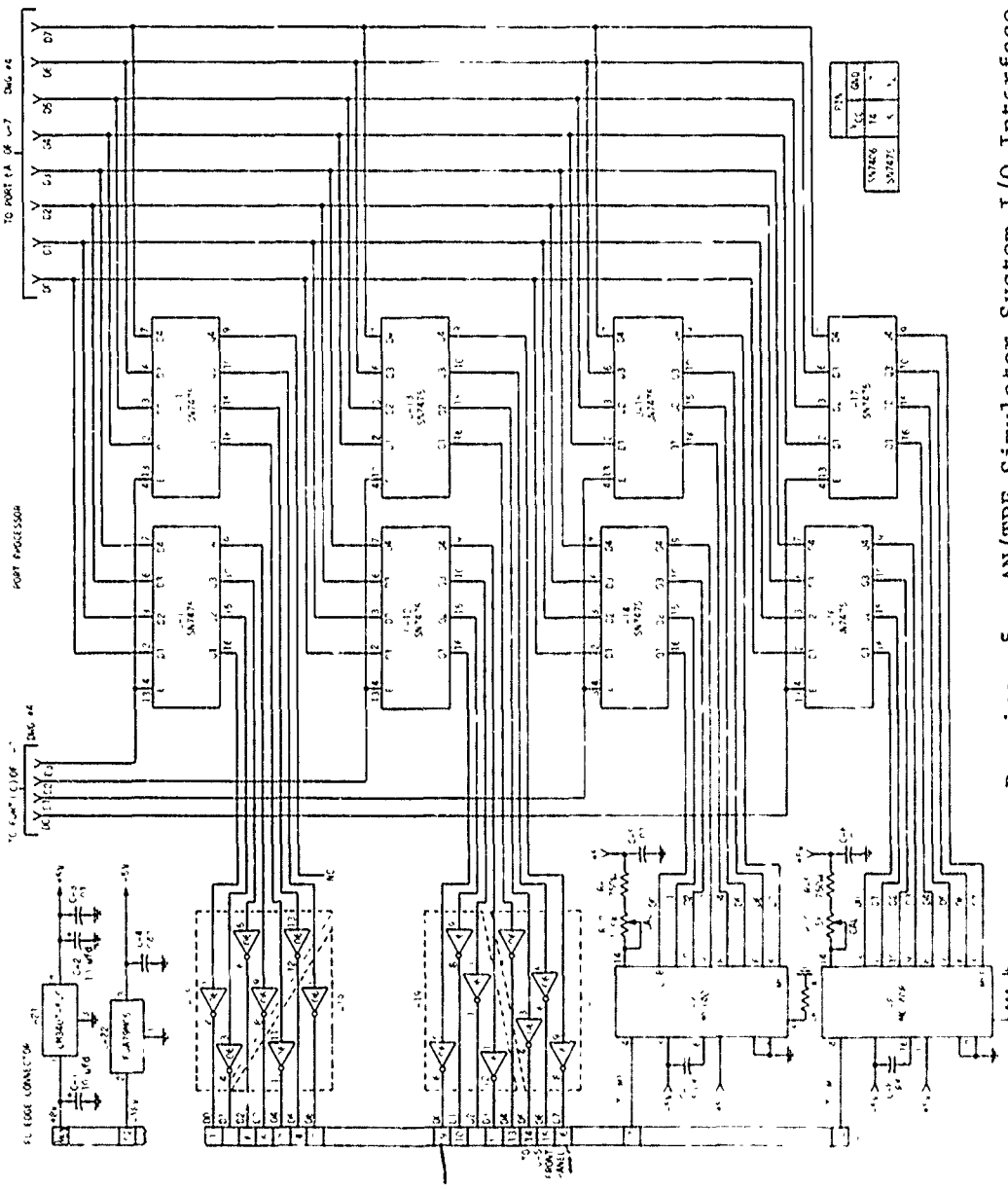
NOTE 2 ALL RESISTORS ARE 1/4 W UNLESS OTHER WISE SPECIFIED



Drawing -3. AN/TPS-43E Simulator Programmable Waveshape Generator - D/A Converter



Drawing -4. AN/TPS-43E Simulator System I/O Interface - Control Circuits and S-100 Port



Drawing -5. AN/TPE Simulator System I/O Interface - Light and Meter Display Circuit

computer data output. Ports B and C are control lines to the data select circuits. This integrated circuit (IC) also controls the meters and the display light circuits. The 8212 (U-6) is the computer input IC from the data select circuits.

The I/O interface card uses addresses FFFØ through FFFF to acquire control of four input/output states. In a future modification, pin 13 of U-3 will be connected to pin 4 of U-4 with the output of pin 6 of U-3 going to pin 15 of U-5. The A1 input from pin 80 of the PC card edge connector will be connected to pin 8 of U-7. These changes will cause the memory addresses to be FFFO through FFF3 resulting in better memory management.

The outputs of pins 14-17 of U-7 are used as latch enables (Drawing 5) for U-10 through U-17, in groups of two, respectively. Whatever values are at port A of U-7 (Drawing 4) are fed directly through the enabled latches to the meters and/or lights. When pins 14-17 of U-7 go low, those values in the latches remain, resulting in a continuous display.

The Simulator System Front Panel

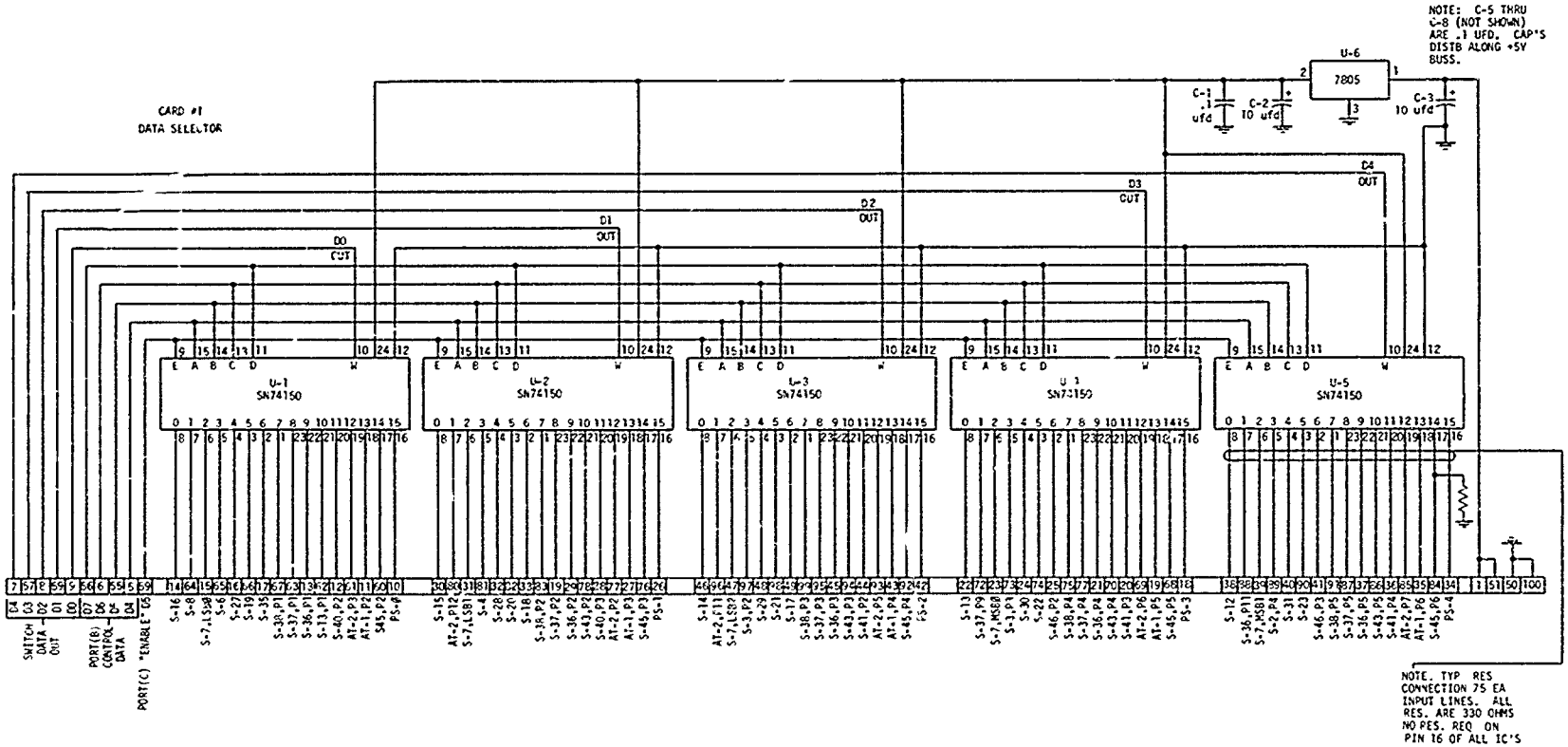
This front panel is identical in appearance to the BITE section control panel of the AN/TPS-43E Radar Set. Refer to the schematic drawing of the panel, Drawing 10. The outputs of the I/O interface card, described in the preceding paragraph, are wired directly to the panel lights and panel meters. The outputs from the switches (highs or lows) are routed through the data select card circuits to the I/O interface card.

Data Select Cards

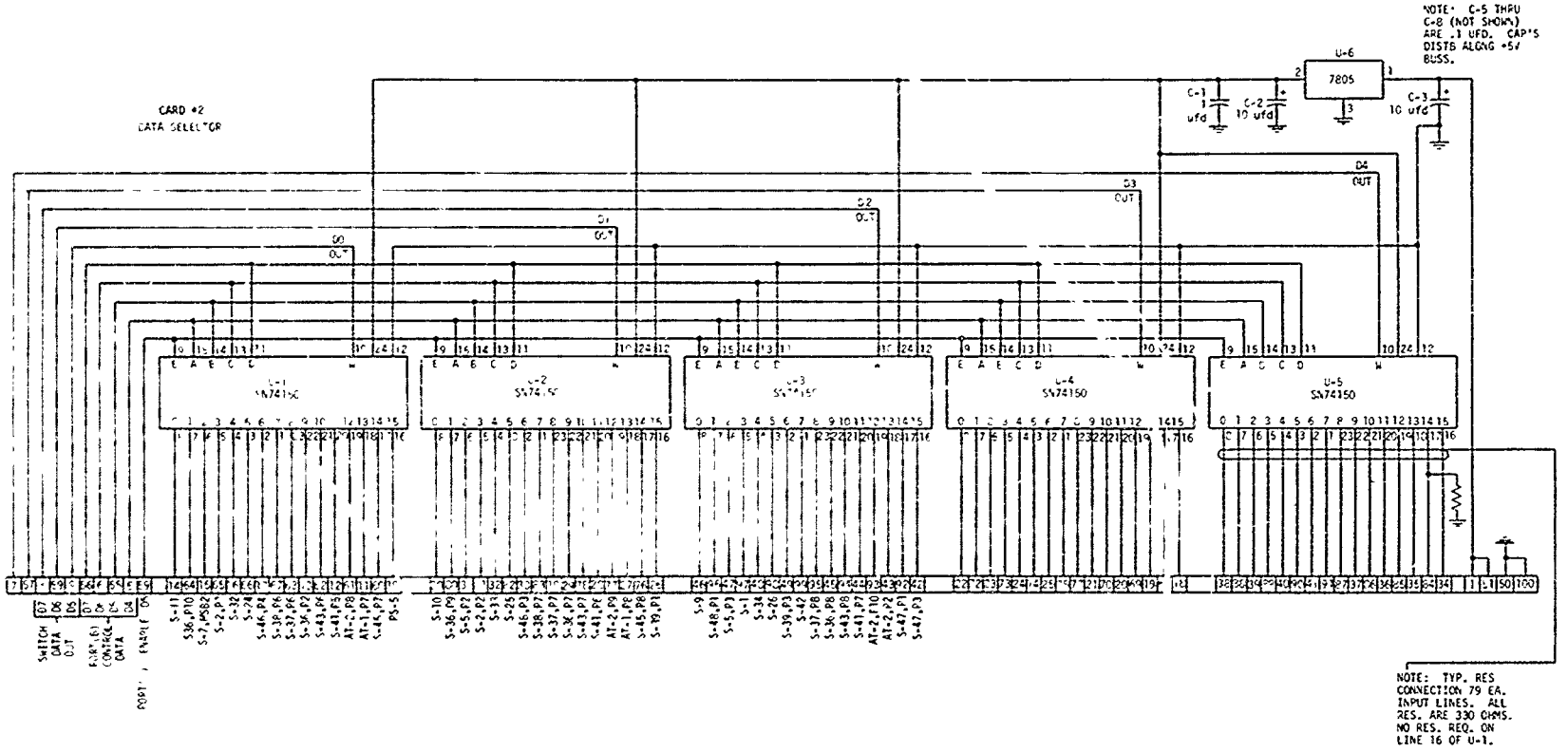
The two data select cards (DSC), (Cards #1 and #2), mounted on the simulator front panel are identical. Refer to the schematic (Drawings 6 and 7). The circuitry for each card includes five integrated circuits 16 to 1 multiplexers (16 to 1 MUX). When a simulator front panel switch is in an ON position, +5 volts is applied through the switch contacts, providing a logical one (high), as a multiplexer input. Multiplexer input is grounded through a 330 ohm resistor (logical zero) when +5 volts is not applied (switch OFF position).

The 16 to 1 MUXs select the line to be read by means of pins 11, 13, 14 and 15 which are controlled by lines 22-25 of port B on U-7 of Drawing 4. When pin 13 of port C goes high, the 16 to 1 MUXs are enabled and pass the logic level of the line selected. Connections from the computer to the DSCs is by way of J-4. Connections from the front panel to the DSCs is by way of J-7 and J-8 on Drawing 11.

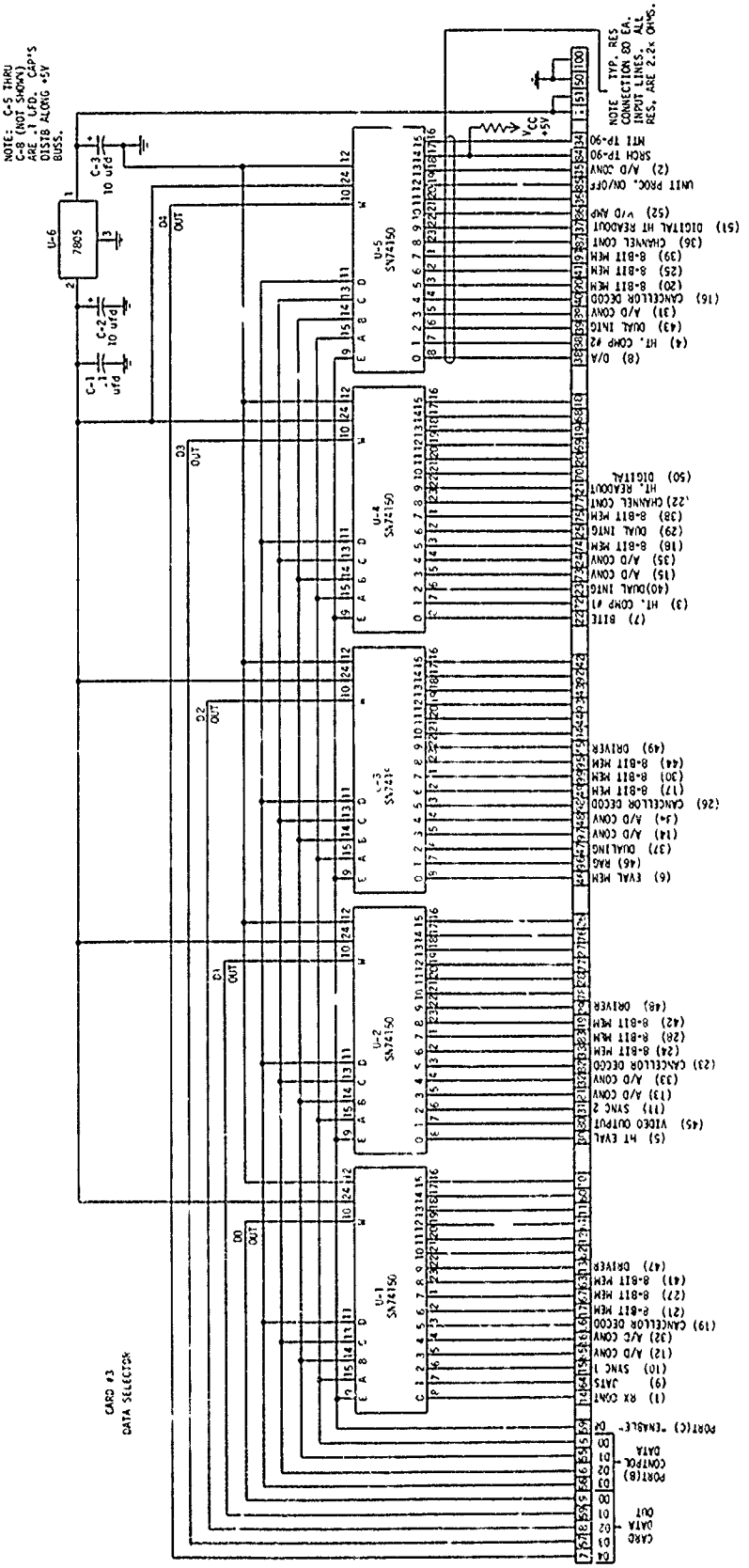
The third data select card (Card #3) is located in the PC board card rack. The circuitry is similar to that of the data select cards described in the preceding paragraph. (Refer to Drawing 8 for the schematic drawing of this card.) Logical ones and zeros to this card result from the ON or OFF (open or closed) condition of 52 reed switches in the card racks. The trainer card rack simulation is composed of four card racks, (Figure 7b), into which 52 dummy AN/TPS-43E circuit cards are inserted. Magnets, which are attached to the socket ends of the dummy circuit cards, magnetically close the reed switches when the cards are properly seated. A closed switch applies ground (Logical Zero) to a multiplexer input. If a card is not properly seated, or is not inserted, the reed switch remains open and +5 volts



Drawing -6. AN/TPS-43E Simulator Card #1 Data Select



Drawing -7. AN/TPS-43E Simulator Card #2 Data Select



Drawing -8. AN/TPS-43E Simulator Card #3 Data Select

(Logical One) is applied as a multiplexer input. The +5 volts is applied through 2.2K ohm resistors to 80 input lines of the five multiplexers on the data select circuit card.

The Phase Shift Analog/Digital Converter

The phase shift A/D converter PC card is mounted on the simulator front panel. Refer to Drawing 9 for the schematic drawing of this card. This circuit converts positive voltages of from zero to +5 volts into binary values from 0 to 63. These binary values are read by the microcomputer by way of the data select cards on the simulator front panel.

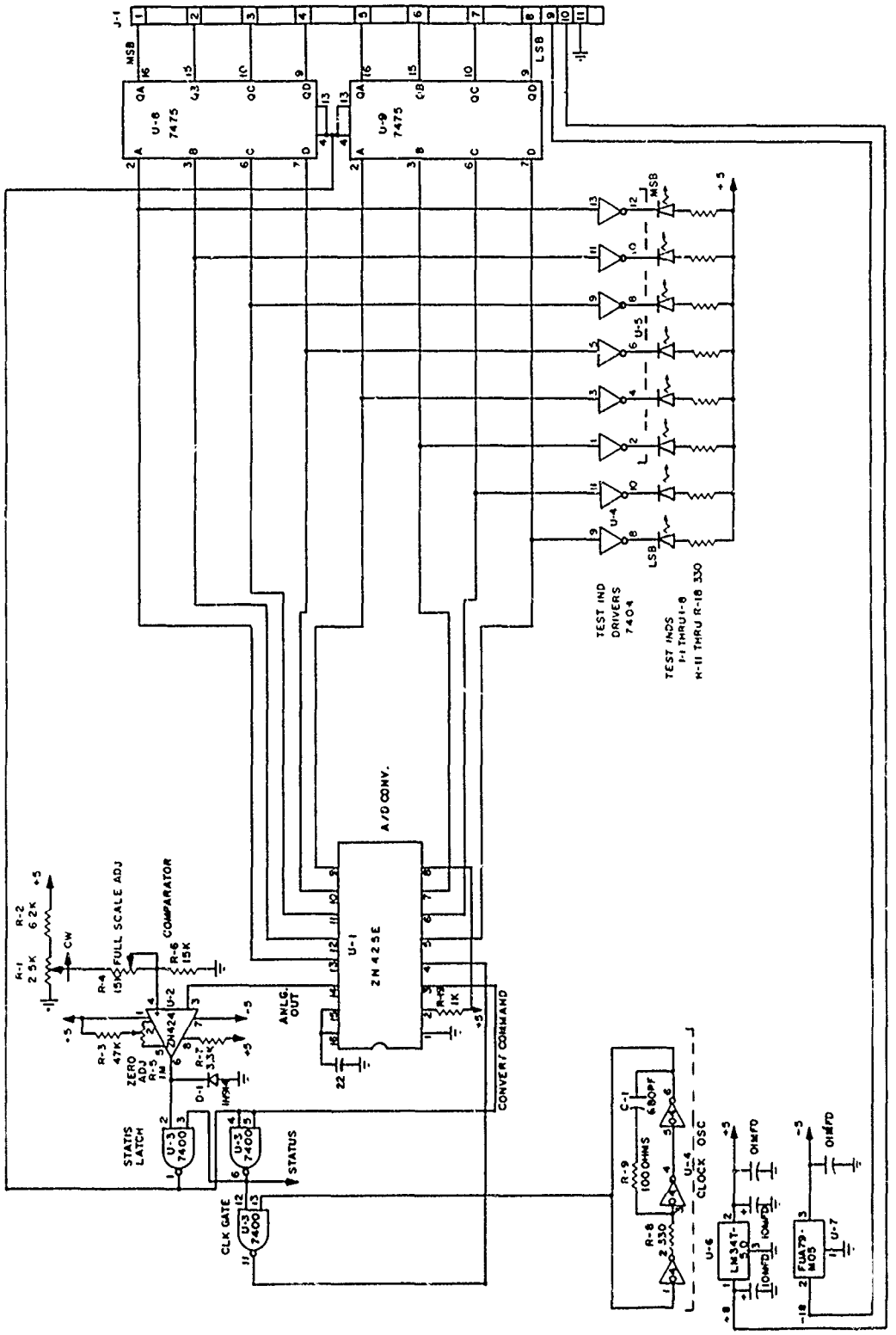
The microcomputer program in use at this time does not utilize the data acquired from the phase shift A/D converter. The utilization of this data may be incorporated into a different microcomputer program at some time in the future.

The oscilloscope used during the operation/maintenance of the simulator/trainer is a Tektronix 465M, or equivalent, equipped with a ten-to-one probe. An adapter, probe tip to BNC, Tektronix P/N 013-0084-01, is used to connect the oscilloscope input jack to the programmable waveshape generator analog output jack (J-1) inside the microcomputer.

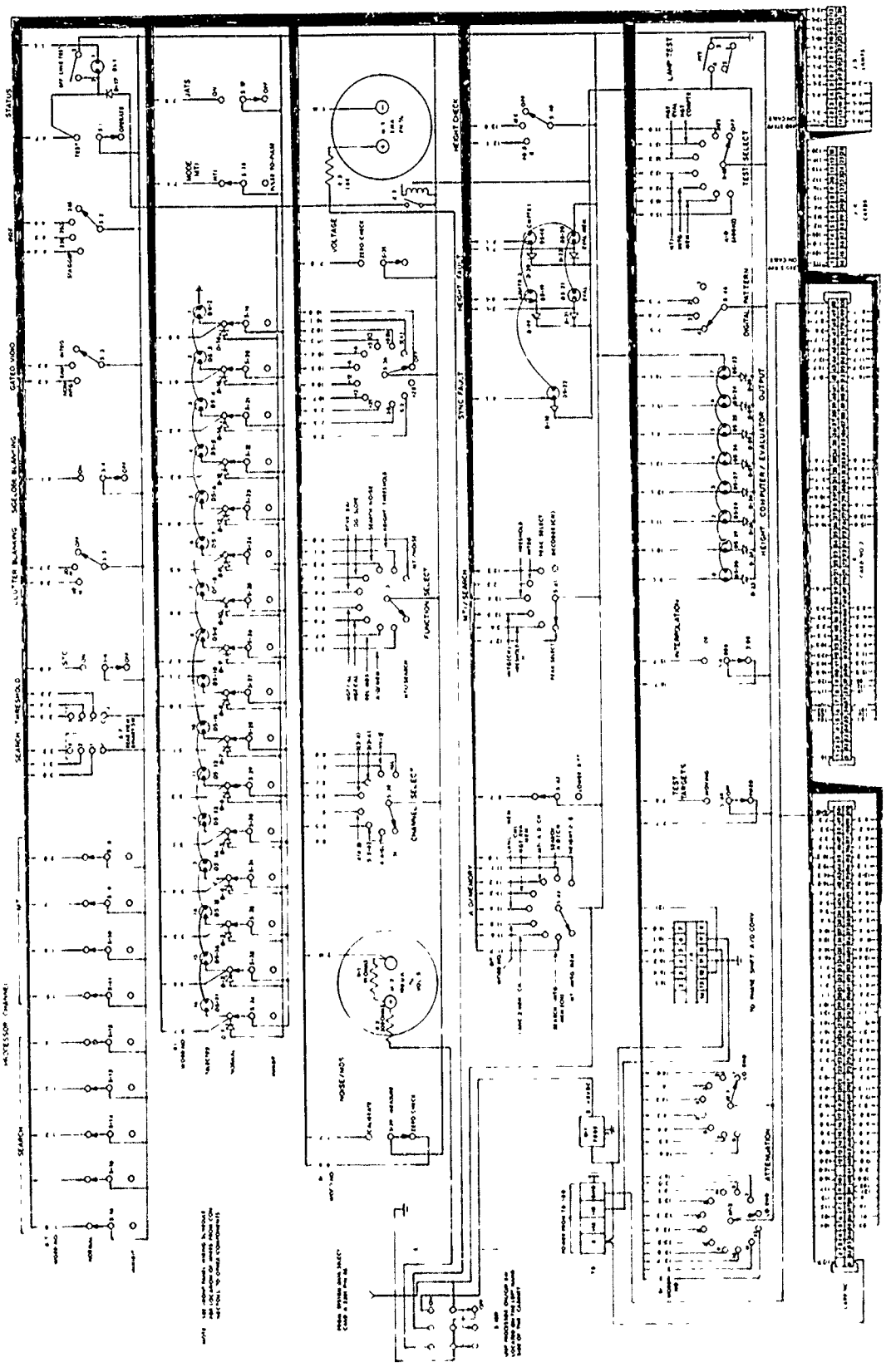
The terminal, TV monitor and keyboard is used for maintenance only. This terminal, Lear-Siegler Model ADM-3A, is equipped with an RS-232 connector, which is connected through a cable to the microcomputer during maintenance for floppy disk loading operations.

Trainer Turn-On and Turn-Off Procedures

The following procedures should be followed each time the trainer is operated:



Drawing -9. AN/TPS-43E Simulator A/D Converter



Drawing-10. AN/TPS-43E Simulator System Front Panel

1. Open the hinged front panel of the trainer.

2. Open the disk drive door on the microcomputer front panel.

3. Connect the AC power plug (P-1) to a 120 VAC, 60 Hz source.

4. Turn on CB-1, the switch/circuit breaker marked POWER. This switch is located on the right front side of the trainer cabinet. A red indicator light on the disk drive inside the microcomputer, and all the indicator lights on the trainer front panel will turn on. Both meters (M-1 and M-2) on the trainer front panel will read full scale.

5. Place the floppy disk (BITE program) into the disk drive with the silver tab down to the ground and towards the operator. Close the disk drive door. A series of clicking sounds from the disk drive, lasting approximately 45 seconds, indicates that the BITE program is being loaded into the microcomputer. At the end of the loading cycle, all of the indicators will turn off and meters M-1 and M-2 will read less than full scale.

6. Open the disk drive door and remove the BITE program disk. Place the BITE program disk in a storage container. Close the disk drive door and the trainer front panel.

7. The trainer is ready for use.

8. The trainer is turned off by placing circuit breaker CB-1 in the OFF position and disconnecting power plug P-1 from the 120 VAC source.

Caution

If an indication described in this procedure does not occur at the designated time, there is a malfunction within the trainer which must be corrected before continuing with the procedure. Power plug P-1 should be disconnected from the 120 VAC source before troubleshooting

the trainer. If circuit breaker CB-1 trips, do not reset it without determining the cause. If any fuse blows, do not replace the fuse without determing the cause.

Additional Precautions

1. Power plug P-1 should always be disconnected from the power source when the trainer is not in use and during electrical storms.

2. The trainer should not be rolled on soft surfaces such as grass or sand.

3. The microcomputer inside the trainer cabinet should be secured before moving the trainer.

4. The oscilloscope, terminal (TV monitor and keyboard) and all unsecured cabinet drawers should be removed from the cabinet before the trainer is moved.

5. Precautions should be taken to prevent overturning the trainer while rolling or fork-lifting.

6. Only narrow skids should be used when fork-lifting the trainer.

Trainer Power Requirements

The trainer power requirements are as follows:

110 VAC, 60 Hz at 15 amps

+8 VDC at 30 amps*

+18 VDC at 15 amps*

-18 VCD at 15 amps*

*output by the microcomputer's power supply.

Programmable Waveshape Generator PC Card

Refer to the three programmable waveshape generator (PWG) schematic drawings, Drawings 1, 2, and 3 during the following descriptions.

Drawing 2 shows the memory section of the card (U-1 through U-6). Each of these integrated circuits consists of 4 each RAM memories (TMS 4033 integrated circuits) stacked vertically and wired in parallel. The enable control decoder (U-7) is also shown on the Drawing 2. Drawing 1 shows the circuits from which U-1 through U-7 receive their inputs (write lines, address lines and data lines). Drawing 3 shows the D/A converter (U-22), which received data from the data port latches (U-8 and U-9) during the data load mode and reads (senses) the data in the IC memories during the run mode. The 6 outputs of U-22 are applied to the summing network (R-1 through R-19). The analog voltage output from the summing network is applied to the input of Op Amp U-21. The output of the Op Amp is connected to J-1, which is the analog output jack for the PWG.

Clock Control Circuitry

The circuitry for the 2 MHz clock, which is used as the timing source for the PWG during the run mode of operation, is located in the lower left section of drawing 1. The clock circuitry is discussed at this time since the clock output pulses from the clock or write gate (pin 3 of U-30) will be referred to many times in the body of this manual. The frequency of these pulses will be 2 MHz or less and their polarity will be plus at any frequency.

The microcomputer operates at 4 MHz; therefore, the PWG must be able to load at a 4 MHz rate during the MSD, LSD and data load modes. The microcomputer clock and write gate output pulses are both 250 nanoseconds (ns) long. During the run mode, the frequency of these pulses

comes from a 2 MHz crystal and is controlled by the ÷ by 2 clock circuit to be 1 MHz or 2 MHz. The microcomputer in this trainer is programmed to send trigger pulses to the ÷ by 2 clock circuit to change the running frequency of the PWG clock pulses from 2 MHz to 1 MHz and vice versa. These clock frequency changes are caused by the design limitations of the trainer. The ÷ by 2 clock circuit is used during the run mode of operation to control the frequency at which the memory is read (1 MHz to 2 MHz). The waveshape pulse width seen on the oscilloscope connected to analog output jack J-1 is an indication of the frequency which is being used.

The state (set or clear) in which the ÷ by 2 control FF (U-11A) is operating determines the frequency of the clock pulses from clock or write gate pin 8 of U-30. The state of this FF can be changed by triggers from the microcomputer on edge-connector pin 83. These triggers are applied to pin 1 of the ÷ by 2 clock port NAND gate U-11B.

The input to pin 2 of ÷ by 2 clock port is the latch strobe, from latch strobe gate U-20 (pin 1), which will be described later in this discussion. When these two inputs to the ÷ by 2 clock port are Hi, the output at pin 3 goes Lo. This Lo is applied to pin 12 of the ÷ by 2 control FF at the same time a Lo from U-7 (pin 4) occurs which enables Q' of U11A for a 1 MHz operation. Each input pulse triggers the ÷ by 2 control FF to change states (set to clear, or clear to set).

At the beginning of the turn-on/turn-off procedures, the output of latch strobe gate U-20 (pin 1) is a steady-state Lo, which is applied to pin 2 of the ÷ by 2 clock port and also to the set input (pin 10) of the ÷ by 2 control FF. This Lo keeps it in the set state until the first trigger from the ÷ by 2 clock port is applied to pin 12

of the ÷ by 2 control FF. Thus, Q is enabled on initialization to provide 2 MHz operation until a trigger pulse make Q' go Hi.

The run (00_2) output transition from Hi to Lo causes the ÷ by 2 control FF to change states when pin 12 is Lo also. Pin 4 of U-7 is high during the run state; therefore, when a new waveshape begins loading it goes low and clears U-11A for 2 MHz operation. The clear mechanism insures a baseline starting value in U-11A for each new data load. When a load is completed, a run mode (00_2) signal, sent to port 7F (Hex), leaves the 2 MHz controls as is while an identical signal sent to FF (Hex) puts the ÷ by 2 control to 1 MHz operation. Each of the inputs described above triggers the ÷ by 2 control FF to change states and each change causes the output pulses from the clock or write gate to change frequency.

The PWG does not change frequency during the run mode. The state (set or clear) of the ÷ by 2 control FF at the beginning of the run mode will determine the timing pulse frequency (2 MHz or 1 MHz) during the run mode. The 2 MHz clock oscillator is crystal-controlled by crystal Y-1.

The 2 MHz clock pulses from pin 2 output of U-23 are applied to pin 10 of the clock gate (U-11B) and to pin 3 of the ÷ by 2 clock divider FF (U-11A). The other input to clock gate pin 9 (U-11B) is the Q' output from pin 9 of the ÷ by 2 control FF (U-11A). The Q' output from the ÷ by 2 control FF (pin 8) is one input to the ÷ by 2 clock gate (pin 4) and the other input (to pin 5) is the Q output (pin 5) of the ÷ by 2 clock divider FF, which changes states at the 1/2 PWG clock oscillator frequency (1 MHz). When the ÷ by 2 control FF is set, the Q output from pin 9 (U11A) is Hi and the Q' output from pin 8 is Lo. The

clock gate is enabled by the Hi to pin 9 (U11B) while the ÷ by 2 clock gate is inhibited by the Lo to pin 4. Thus, the Hi 2 MHz clock pulses to pin 10 are passed through the clock gate at the original frequency.

The FF (Hex) input trigger to the ÷ by 2 control FF causes it to change from set to clear (Q goes Lo and Q' goes Hi). The clock gate is inhibited by the Lo Q input to pin 9 while the ÷ by 2 clock gate is enabled by the Hi Q' input to pin 4. Since the ÷ by 2 clock divider FF changes states at the 1 MHz clock frequency, the Q output (pin 5) is Hi on alternate clock input pulses. Thus, the input to pin 5 of the ÷ by 2 clock gate is at 1 MHz.

The 1 MHz or 2 MHz clock gate (U-11B) passes either frequency that is applied as an input because one of the unselected clock gates is always outputing a steady state Hi. The clock pulses at output pin 11 are applied to input pin 9 of NAND gates U-30. The other input to this NAND gate (pin 10) is a steady-state Hi from the output (pin 11) of another NAND gate of U-30, which has its inputs (pins 12 and 13) tied together and grounded through the reset line. The clock pulses at the output of U-30 (pin 8) are the timing pulses for the PWG.

Power

At the top of Drawing -1 are shown the DC power circuits for the PWG circuits. Voltage regulator U-31 has +8 VDC input from edge connector pin 1. The output of U-31 is +5 regulated. Resistors R-30 and R-31, and Zener diodes CR-1 and CR-2, are used to reduce and regulate +18 VDC and -18 VDC inputs to +12 VDC and -12 VDC respectively. The 18 volt inputs are from edge connector pins 2 and 52. These three voltages (+8 VDC, +18 VDC and -18 VDC) are supplied by power supplies

in the microcomputer. All of the other inputs to the programmable waveshape generator (PWG) are also from the microcomputer.

Port Addressing

The eight inputs (D-0 through D-7) to data port latches U-8 and U-9 are sources of the data loaded into the memories. When these two latches are enabled by the latch strobe from pin 1 of latch strobe gate U-20, data and/or address instructions can be brought into the PWG and loaded into the PWG memory. The first six of the inputs to U-8 and U-9 (D-0 through D-5) are data input lines and the last two (D-6 and D-7) are used as mode control lines to program control decoder U-7. The inputs from the microcomputer are TTL logic levels (+5V highs or 0V lows). The value "7C" hexadecimal ("7C" Hex), used to address port address detector U-10, along with SOUT from the S-100 buss, causes highs at all eight U-10 inputs. The output at pin 8 goes Lo and is applied to input pin 2 of latch strobe gate U-20. The PWR write strobe from edge connector pin 77 is the second input to U-20 (at pin 3). These two Lo inputs cause pin 1 of this NOR gate to go Hi. This is the latch strobe and is used in three places in the PWG. Lo inputs A-0 and A-1 of the "7C" hex address are inverted by two sections of inverter U-26 and applied as Hi inputs to NAND gate U-10. The other "7C" hex address inputs to U-10 are Hi. The PWR write strobe (Lo) and SOUT (Hi) occur at the same time as the "7C" hex address. The latch strobe from pin 1 of U-20 goes to pins 4 and 13 of both data port latches U-8 and U-0. These latches are then enabled to bring data from the microcomputer into the PWG.

PWG Timing Frequencies

The microcomputer operates at a 4 MHz clock rate while the PWG, due to the slower speed of its own memories, must operate at a 2 MHz (or less) clock rate. However, due to the time intervals during non-output instructions in the microcomputer, there is sufficient time for the slower PWG memories to be loaded. The memory address latches and memory address counters must be enabled for longer periods of time (after the port address latches are no longer enabled). This is accomplished by using the latch strobe gate, described above, to generate a 500 ns pulse which is used to keep the memory address latches and counters enabled after the termination of a legal port address of "7C" or "FC" (Hex). The Hi latch strobe is applied to pin 5 of U-25 in the write pulse widening one shot multivibrator (OSMV) circuit, shown on the top left section of the referenced schematic. The OSMV is triggered by the trailing edge of the latch strobe. The OSMV is part of the control logic circuit which is made up of one NAND gate of U-25 and three inverters of U-24. Resistors R-26 and R-25 and capacitor C-7 comprise the RC time constant circuit. Rheostat R-25 is adjusted so that the output pulse from the OSMV is approximately 500 ns in duration. The Hi output of U-25 (pin 6) is inverted through three inverter stages of U-24 in succession. Pin 10 output is a Hi 500 ns pulse and pin 8 is a Lo 500 ns pulse. The Hi at pin 10 is the write strobe which is applied to input pin 9 of write gate U-25. The other input to the write gate is the data line (10_2) from pin 6 of the program control decoder (1/2 of U-7) which is Lo during the data load mode. The data line input is inverted by one inverter of U-23 and pin 8 output of U-23 is applied to pin 10 of the write gate as a Hi.

Program Control Decoder

Lines D-6 and D-7 from the microcomputer to data port latch U-8 are mode control lines to the PWG. When U-8 is enabled by the latch strobe, the outputs (pins 9 and 10) will be in one of four possible combinations of highs and lows, (11_2, 01_2, 10_2 or 00_2), which are applied as inputs to pins 2 and 3 of program control decoder U-7. The outputs of U-7 are used to select one of the four modes in which the PWG operates. The PWG can be in the run mode (00_2); it can be in the data accepting mode (10_2); it can be accepting an address load of the least significant digit (01_2); or it can be accepting an address load of the most signficant digit (11_2). The outputs of U-7 are Hi until selected. The mode selected will cause that mode output line to go Lo. The four modes are selected in the following sequences: MSD (11_2), LSD (01_2), Data (10_2) and Run (00_2).

Memory Address Latches

Since only six data lines from the data port latches are used to load 12 bits of address into the MSD and LSD memory address latches, the 12 bits are loaded in two groups of six each. This is done by enabling the MSD memory address latches (U-27 and 1/2 of U-28) during the MSD mode (11_2), and the LSD memory address latches (U-29 and the other 1/2 of U-28) during the LSD mode. When the input combination from U-8 (11_2) causes the MSD load output of the program control decoder to go Lo, this Lo is applied as an input to Pin 11 of MSD load gate U-20. The inverted write strobe (Lo) from pin 8 of inverter U-24 is the other input (pin 12). These two Lo inputs cause the output of the NOR gate (pin 13) to go Hi. This Hi is applied to pins 4 and 13 of U-27 and to pin 4 only of U-28 (memory address latches). U-27 and 1/2 of U-28 are

then enabled to load six MSD address bits from the six output of the data port latches.

When the program control decoder is sequenced to the LSD load mode (01_2) by the microcomputer the MSD load output goes Hi and pin 13 of MSD load gate U-2 goes Lo, so that the previously loaded memory address latches (U-27 and 1/2 of U-28) are no longer enabled. The LSD load output goes Lo. This Lo LSD output (01_2) is applied to Pin 8 of the LSD load gate U-20. The reinverted write strobe (Lo) from pin 8 of inverter U-24 is used as the second input to this NOR gate (at pin 9) also. The resultant Hi output at pin 10 is applied to pins 4 and 13 of U-29 and to pin 13 only of U-28. The second half of U-28 and all of U-20 are then enabled to load six LSD address bits from the same six outputs of the data port latches. The 12 output lines of the three memory address latches are connected to 12 inputs of the memory address counters (U-17, U-18, and U-19). These counters are inhibited from receiving the 12 address bits from the latches by the Lo input from pin 4 of NOR gate U-20 (load or last count gate). When the output of the LSD load gate transitions from Hi to Lo, after approximately 500 ns, this Lo inhibits the LSD memory address latches (U-29 and 1/2 of U-28) and is also applied to input pin 5 of the load or last count gate (U-20). The input to pin 6 is normally Lo from pin 12 of the last count inverter (U-23). These two Lo inputs cause a transition from Lo to Hi at output pin 4. This Hi is applied to pins 11 of the three memory address counters as an enabling pulse and the 12 address bits from the memory address latches are loaded into the three memory address counters. The address numbers from the three counters will determine the

duration of the waveshapes observed on the oscilloscope at analog output jack J-1 when the PWG is in the run mode.

Memory Address Counters

The three counters are wired in series so that, when downcounting, the outputs form a series of 12 bit numbers, starting with the maximum binary address value and downcounting to zero. The Hi clock pulses from pin 3 of U-30 (clock or write gate) are applied to pin 4 of U-19. (Refer to paragraph on clock control circuitry for the description of the generation and control of the clock pulses.) Each pulse downclocks the three counters to a different binary address value. The SM74193 counters are designed to be used in multidecade operations, without additional logic, by using the borrow output of one counter as the downclock input to the following counter. When U-19 has counted to 00, a Hi from U-19 (pin 13) to U-18 (pin 4) starts the countdown of U-18. When U-18 counts down to 00, a Hi from U-18 (pin 13) to U-17 (pin 4) starts the countdown of U-17. When U-17 counts down to 00, all of the 12 outputs of the counters are Lo. These outputs are inverted by U-14 and U-15 and applied as Hi inputs to multiple NAND gate U-16, the last count detector. The Lo output at pin 9 of U-16 is inverted by last count inverter U-23 and is applied as a Hi to U-20, pin 6, the load or last count gate. The resultant Lo output at pin 4 of U-20 is applied to pins 11 of the three memory address counters. This Lo inhibits the counters from being loaded from the three memory address latches, as described in paragraph 2-13, until the LSD load gate output (U-20, pin 10) transitions to Lo.

The output of the last count inverter is also applied to sync output jack J-2 and is used to synchronize the oscilloscope. The

countdown pulses used to downcount the memory address counters are Hi outputs of clock or write gate U-30 at pin 3.

Memory Load Control

It was stated earlier in this chapter that the PWG, when loaded and in the run mode, could operate independently of the microcomputer. During the data load mode, the data line (10_2) from the program control decoder is Lo. This Lo is applied to input pin 9 of inverter U-23. The Hi output of U-23 at pin 8 is one input (pin 10) to write gate U-25. The write strobe (alternately Hi or Lo) from pin 10 of U-24 is the other input (to pin 9) of the write gate. Pin 8 output of the write gate is therefore alternately Lo or Hi. It goes Lo in coincidence with the leading edge of the 500 nanosecond write strobe. Clock gate U-25 is inhibited by the Lo at pin 13 from inverter U-23 (pin 10). The input to this inverter (pin 11) is the Hi run (00_2) output of the program control decoder.

The PWG clock pulses at input pin 12 of the clock gate, from U-30 pin 8, are not passed through the clock gate. The output of the clock gate at pin 11 is the input to pin 2 of clock or write gate U-30 and remains Hi during the data mode. The input to pin 1 of the clock or write gate is the output of the write gate (pin 8). When this input goes Lo, the output at pin 3 goes Hi, in coincidence with the leading edge of the write strobe. The output pulses at pin 3 of the clock or write gate are the pulses used to downclock the memory address counters, and are generated and controlled by the microcomputer program. However, during the run mode there are no inputs, other than the three power supply voltages, from the microcomputer.

The write gate (U-25) is inhibited by a steady state Lo at pin 9 from pin 10 of U-24 (there are no write strobes during the run mode). The data line (10_2) input to pin 9 of inverter U-23 is Hi in the run mode. The Lo output of the inverter (pin 8) is applied to input pin 10 of write gate U-25 resulting in a steady state Hi at output pin 8. This Hi is applied as an input to pin 1 of clock or write gate U-30, and also to input pins 4 and 5 of NAND gate U-30 in the write delay OSMV circuit. Since this is a steady state voltage, there are no write pulses generated in the write delay OSMV circuitry during the run mode. Clock gate U-25 is enabled by the Lo output of the run (00_2) line from program control decoder U-7 during the run mode. This Lo output is inverted to a Hi by inverter U-23. The Hi output at pin 10 is applied to pin 13 of clock gate U-25. The Hi PWG clock pulses (1 MHz or 2 MHz) from pin 8 of U-30 are applied to pin 12 of the clock gate. The clock gate output (pin 11) goes Lo with each pulse. These Lo pulses are applied to pin 2 of clock or write gate U-30. The Hi output pulses at pin 3 are the same frequency as the PWG clock pulses (1 MHz or 2 MHz). These are the downclock pulses used to downclock the memory address counters. They are generated and controlled without inputs from the microcomputer. During the data mode, the downclocking of the memory address counters assures that each data bit is loaded into a different address in the memory. During the run mode, the downloading assures that the data bits in the memory are correctly addressed for reading.

Write Delay One Shot Multivibrator (OSMV)

During the data mode, the output pulses from pin 8 of write gate U-25, described in paragraph 2-15, are also used to trigger the

write delay OSMV. This output is applied to input pins 4 and 5 and NAND gate U-30 which acts as an inverter. The output at pin 6 (Hi) is applied to pin 2 of U-25, the OSMV NAND gate. The OSMV is triggered by the trailing edge of the pulse (negative-going), so the OSMV output pulse is delayed approximately 500 ns after the leading edge of the input pulse.

The OSMV circuit is made up of NAND gate U-25 and two inverters of U-24. The RC time constant circuitry is identical to that of the pulse widening OSMV described above. Rheostat R-22 is adjusted so that the output pulse is approximately 500 ns in duration. The Hi output at pin 4 of the second inverter is applied to the inputs of three inverters (U-26) in parallel. These three inverter/buffers are needed to supply the driving power to the write lines to the 24 random access memories (RAMs).

Each inverter/buffer output is applied to the write (pin 3) input of eight RAMs in parallel. The inputs occur after the RAMs are addressed and enable all 24 RAMs to be loaded with data from the data port latches (U-8 and U-9). Lo write input pulses occur 500 ns after the down clock pulses to the memory address counters described earlier. The write delay OSMV is used to compensate for transit time losses in the memory address latches and counters, and to assure that there is sufficient time for the RAMs to be correctly addressed for incoming data and for that data to be correctly loaded into the memory.

Memory Loading

It was explained that the memory address latches (U-27, U-28 and U-29) were enabled to accept address data by the Hi outputs from the MSD and LSD load gates, pins 13 and 10 respectively of the two NOR

gates of U-20. Both of these outputs are Lo during the data mode since the MSD (11_2) and the LSD (01_2) outputs from program control decoder U-7 are Hi. Therefore, the memory address latches are inhibited from receiving data of any kind. Any data in the data port latches (U-8 and U-9) will go directly to the RAMs.

Data from U-8 and U-9 is routed to the RAMs on data lines D-0 through D-5, with each of the six data lines connected to the pins 11 (DIN) of one IC (four each TMS4033 RAMs stacked and wired in parallel). The 12 outputs of the memory address counters (U-17, U-18, and U-19), after being inverted by 12 inverters of U-14 and U-15, are each applied to both inputs of one of the 12 NAND gates of memory address drivers U-11, U-12 and U-13. Address lines 0 through 9 from the memory address drivers are wired so that each address line goes to the same input pin of each of the 24 RAMs in parallel. The other two outputs from the memory address drivers (U-11, pins 3 and 6) on lines 10 and 11, are applied as control inputs to enable control decoder U-7 (pins 13 and 14).

One half of U-7 was described in paragraph 2-10 as the program control decoder. This half of U-7 operates in the same manner. The inputs to pins 13 and 14 are four possible combinations of highs and lows (00_2, 01_2, 10_2 and 11_2). The four outputs at pins 9 through 12 are Hi until selected by one of the binary inputs. At that time, the selected output goes Lo. The four outputs are the Row-Addressing Strobes, with each output connected to pins 13 (CE) of the six RAMs in each of the four rows. The selected Lo output enables six RAMs in one row to load data. Six data bits on the six data line (D-0 through D-5) are loaded into six RAMs in the selected row. Since all 24 RAMs are

addressed identically from the address lines at each address, the electrical locations of the six memory cells in six selected RAMs is also identical. A data bit on any one of the six data input lines can be loaded into only one specific RAM, as determined by the enable control decoder configuration. Each of the 1024 memory cells in each RAM is individually addressed and selected for loading by the combinations of address line inputs from the memory address drivers. The delayed write strobe assures that there is sufficient time for the selected/addressed memories to be loaded.

Oscilloscope Monitoring

As the data from the data port latches (U-8 and U-9) is being loaded into the RAMs, it is also applied to the input of six inverters of U-22 in the D/A converter. The outputs of the six inverters are applied to the summing network, composed of resistors R-1 through R-19.

This network is provided with +5 VDC from voltage regulator U-22, which is supplied with +8 VDC from the microcomputer through the PWG circuit board edge connector. The output of the summing network is applied to input pin 8 of operational amplifier (Op Amp) U-21. The output of the Op Amp at pin 4 is connected to analog output jack J-1 which is the monitor point (oscilloscope display) for the trainer/simulator.

The D/A circuit is identical to that in the AN/TPS-43E radar system and has the same response time. The waveshapes seen on the oscilloscope are made up of 64 analog voltages of from 0 volts to 5 volts in amplitude. During the run mode of operation, data loaded into the memory is read sensed by the D/A circuit and applied to the oscilloscope through the same circuitry. As in the AN/TPS-43E radar system,

the oscilloscope display is an indication of the positions of all of the switches in the system, as read by the microcomputer.

Run Mode

The binary inputs to program control decoder U-7 from the microcomputer (11_2, 01_2, 10_2 and 00_2) determine the mode in which the PWG is operating at all times. After the data has been loaded into the memories, inputs to the program control decoder (00_2) from the microcomputer switch the PWG to the run mode. The run (00_2) output from U-7 goes Lo and the other U-7 outputs are hi.

The three memory address latches (U-27, U-28 and U-29) continue to be inhibited from receiving additional address and the address already in these latches is controlled by the PWG clock (1 MHz or 2 MHz). This frequency (1 MHz or 2 MHz) is controlled by the ÷ by 2 clock circuitry. There are no microcomputer inputs so the PWG is operating independently of the microcomputer.

The clock pulses from clock or write (U-30, pin 3) count down the memory address counters (U-17, U-18 and U-19), as described in paragraph 2-14, but the clock pulses are generated in the PWG clock oscillator circuit and the frequency (1 MHz or 2 MHz) of the pulses is controlled by the ÷ by 2 clock circuitry. The counters count down one digit on each clock pulse, from the maximum binary address value down to zero. The combination of Hi and Lo outputs on the 12 output lines changes at each down count and each different combination becomes a different address; to selected memory cells; in selected RAMs; in selected rows of RAMs.

Since there are no inputs from the microcomputer during the run mode, there are no outputs from the write pulse widening OSMV circuit

and consequently, no input to pin 9 of write gate U-25 which is therefore inoperative. The output of the write gate (pin 8) was used to trigger the write delay OSMV during the data load mode, to generate the delayed write strobes to the memory. The write strobes are not required during the run mode. The Lo write strobes enabled the addressed locations to be loaded with data during the data mode. The write lines inputs to the RAMs remain Hi during the run mode. This enables the RAMs to be read (sensed) so that data already loaded into the addressed locations is read as each location is addressed during the run mode. This data is routed through the output lines (D-0 through D-5) to the D/A converter circuitry, which was described above. As in the data read mode, the D/A converter output goes to analog output jack J-1 for oscilloscope monitoring. On the last output all the counter values are zero. At this time a pulse from U-16 reloads the counters and also strobes J-2, the sync line of the oscilloscope.

Software Locally Developed

The software created for this project were: the application program in FORTRAN, the support programs in FORTRAN and BASIC and the maintenance programs in BASIC and direct machine code. The application program (Appendix F) is a structured design which easily accommodates testing of program modules. The other programs are very simple and did not require the elaborate planning afforded to the application program.

First consider the control (TPSPGM) module (Figure 11). This particular module has the purposes of bringing the program on line and controlling all other modules, i.e., to provide a central source of control over the other modules. Without this, the structuring of the

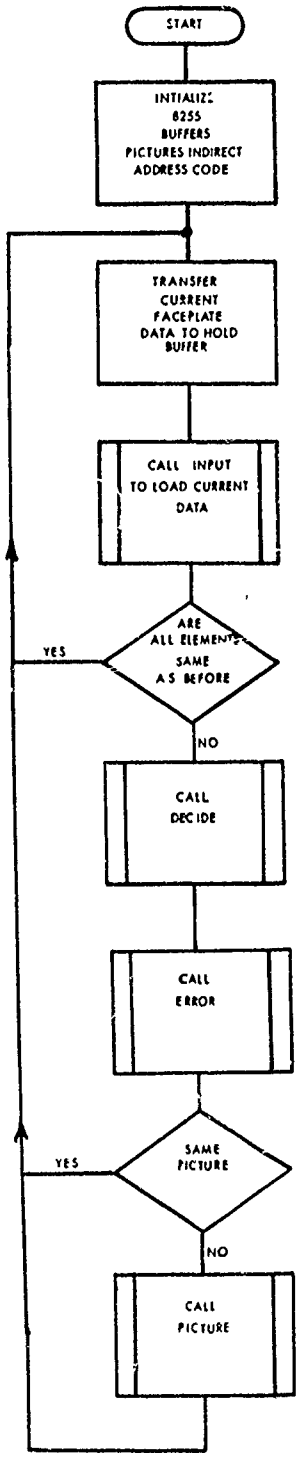


Figure 11. TPSPGM Flowchart

program would have been impossible. The software design is intended to have a structure that is not ambiguous to the user. Since software maintenance consumes manpower, and the user expects that the maintenance of the maintenance simulator should be low, a modular design provides "to the module" problem identification.

The input module (INPUT) is a relatively simple subprogram. Its purpose is to go to the necessary ports and memory addresses to acquire information from the trainer itself. Information acquisition actually is broken into two parts. First is the acquisition of data from the faceplate and second, from the equipment of the card cage.

From the faceplate, the computer selects information about the settings of the various switches so that it can determine what particular display needs to be output to the oscilloscope. From the card cages, the computer must determine which card, if any, has been replaced to simulate fault repair. The computer will then respond by presenting a corrected picture. The data acquisition module must distinguish between the faceplate and the card cages in order to be able to get data from these two groups in the correct order.

Due to hardware constraints, it is necessary for the acquisition module to make two searches, one search of the faceplate and one search of the card gages. (See Figure 12.) Each search consists of reading a set of 16 eight-bit bytes representing 128 bit positons controlled by eight 1 of 16 multiplexers (MUX) in parallel. A search is initiated by enabling a data set with a bit in port C and addressing that set via port B. Two sets of data are currently searchable, where the first data set uses all 128 bits and the second data set contains only 55 bits used out of 80 possible wired positions. Once a data set

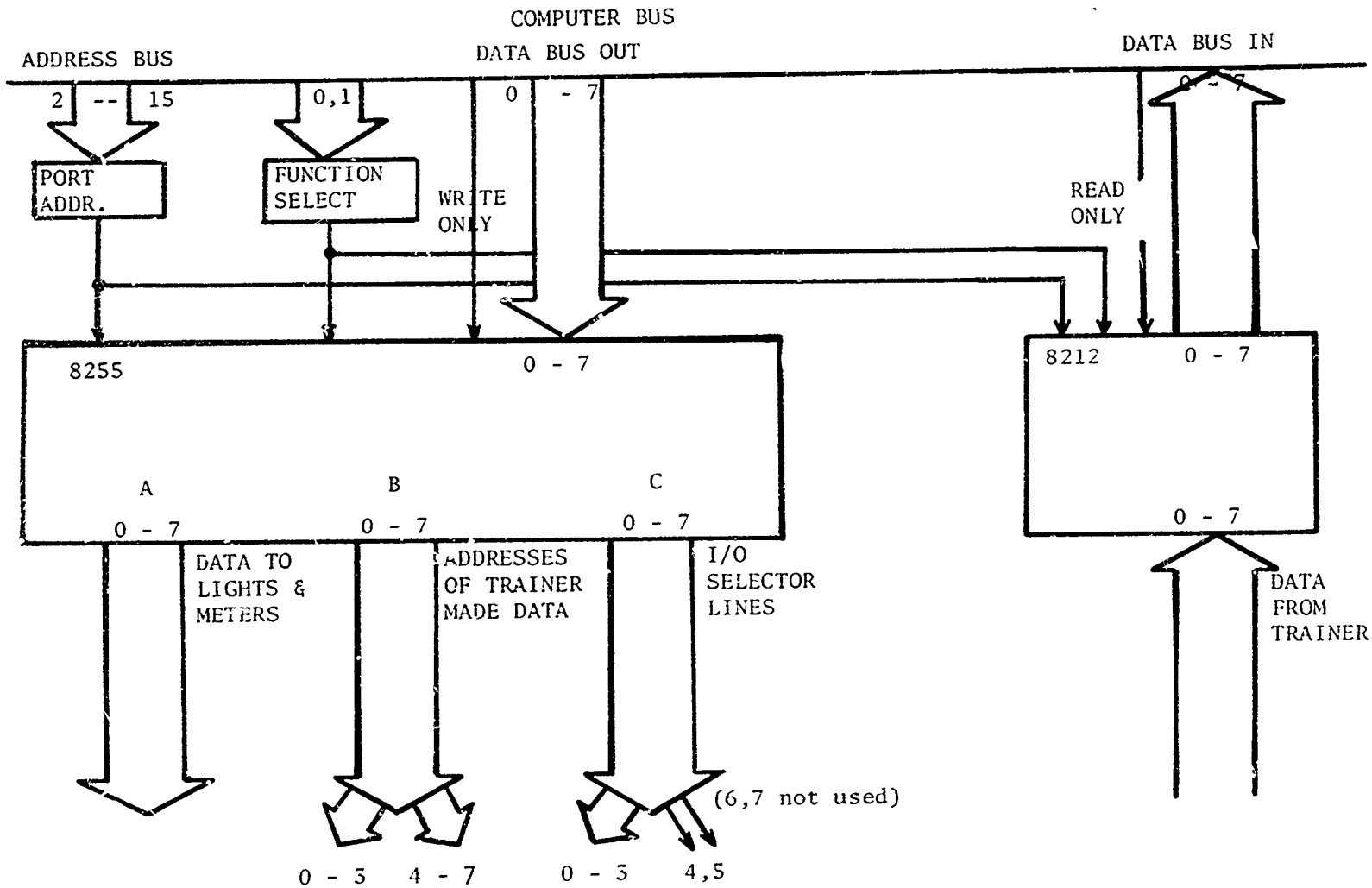


Figure 12. Block Diagram of I/O Controller

is enabled and a byte within it addressed, it is read from the 8212 at port C.

The ports described thus far are memory mapped rather than actual port addresses. Memory addresses serve to activate the 8255, which is a software programmable I/O device. In systems which do not have large memory requirements, and do have extensive I/O requirements, this procedure is very convenient. For the purpose of this project, both memory map and port addressing are used in the hardware. The reason for using memory map addressing for I/O and regular port addressing elsewhere for the output of the oscilloscope is that the project desired to demonstrate that it can be done both ways. The data acquisition module serves as a method of getting information into the computer. The next thing that is necessary is evaluation modules.

The evaluation module(s) (DECIDE and ADMEN) is (are) designed to look through all the information that has been collected by the data acquisition module. Decisions are made by cascade logic evaluation. This equates to a tree search wherein the keys to the branching are taken from the faceplate switch positions. The general flow, shown in Figure 13, is a series of, at most, ten decisions leading to correct picture determination. Of those ten decisions, five were 'Do Case' decisions, which represent the cascade concept utilized. Most of the pre-decision evaluation is done in terms of boolean logic programming as opposed to arithmetic programming. The reason for using LOGICAL code is speed.

The computer uses an eight-bit data word. If arithmetic means of dealing with these words are chosen, the lead bit is reserved for a sign bit. If that one bit happens to be turned on, automatic two's

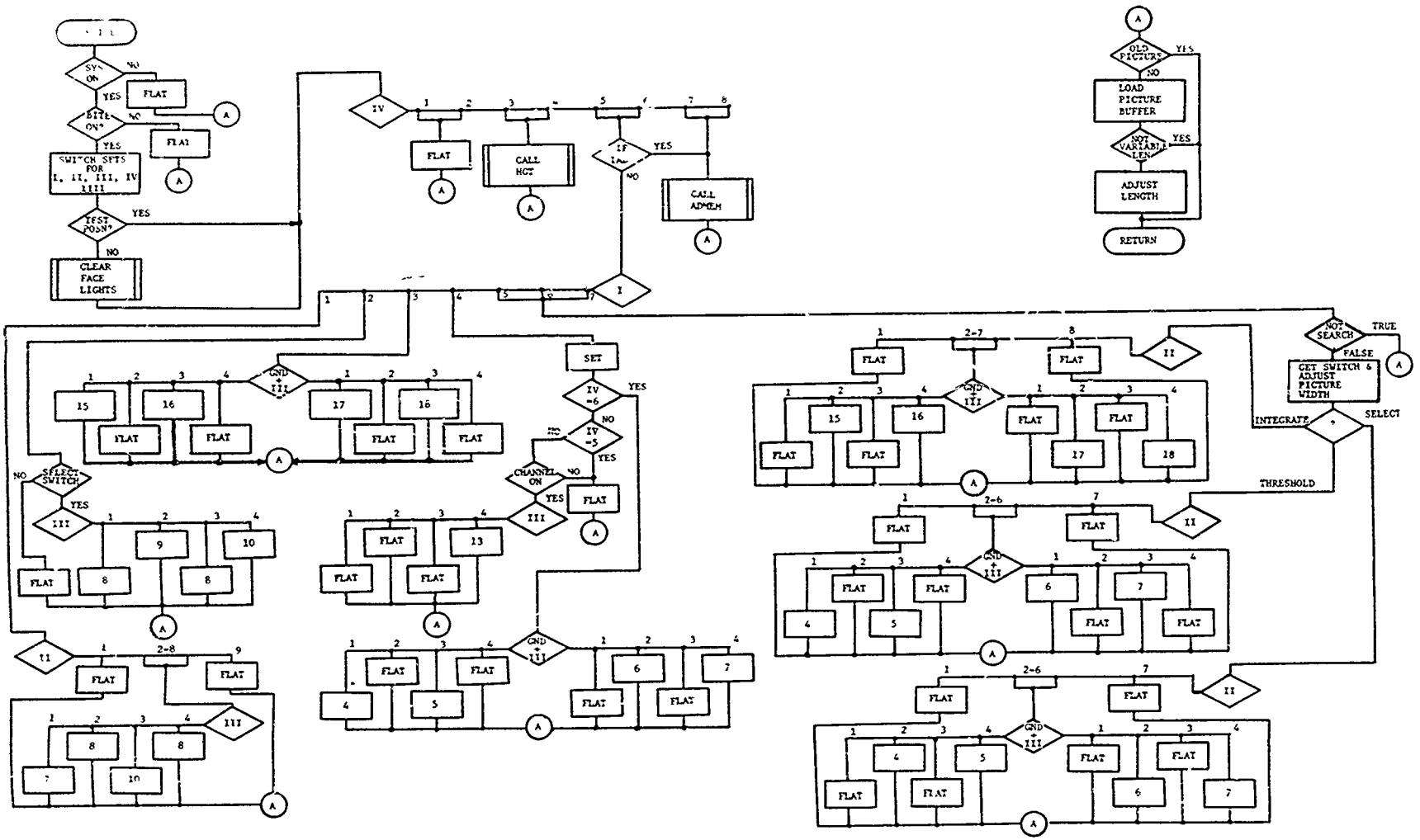


Figure 13. DECIDE Flowchart

complement arithmetic takes place making it very difficult to control using simple code. By making everything single-bit LOGICAL, the computer effectively converts every LOGICAL word manipulation in the computer to eight-bit paralleled gating, such as an eight-bit AND, OR, or NOT gate. By performing logical AND, logical ORs, exclusive ORs, and inversions, each point is testable using relatively fast straightforward logic. Another good feature of LOGICAL code is that it is very easily followed by electronic maintenance people who, presumably, are going to be the ones who will look at this program and see whether it is functioning. Boolean logic then is the basis of the evaluation module.

DECIDE and ADMEN conserve memory by examining 32 eight-bit words which form a 328 array of switch conditions on the trainer. Determination that a particular word bit is turned on is accomplished by doing a logical AND with a word that contains only that bit turned on - a true return means that the bit tested is turned on. Conserving memory space is essential since the trainer has a 32,000 word computer and a training program space of approximately 25,000 words. There is not much space for extensive arrays when the 7000 word disk operating system and a 22,000 to 24,000 word program must co-exist there. The evaluation module determines which picture will be displayed by looking at all the switches and then supplying the necessary information to the display module PICTUR. Prior to picture display TPSPGM calls ERROR.

ERROR is called to determine if the student should be given a malfunction dependent on the current settings of the BITE. If such an error should be required, it is inserted into the text of the picture buffer (IODAT) or is passed directly to PICTUR as a systemic error.

The data display module (PICTUR) is a subprogram which functions to create pictures that can be displayed on the oscilloscope (Figure 14). It is broken into three major areas: point-by-point displays, point-to-point vectors, and random point displays.

Area one is the point-by-point displays. This area is specifically intended to allow any individual voltage to be displayed on the oscilloscope followed by another one of a different level without any regard to vector calculation. Therefore an arbitrary point pattern can be displayed.

Area two is the vector display component of this module, which allows display of a line which rises or falls from a baseline of (and to) any of nine predetermined heights (maximum of 4 volts, minimum of zero volts). Display of a level line of any length (e.g., from 1/2 microsecond (us) to 2450 us) at any given voltage desired (e.g., at any of 64 possible voltage levels between zero and 5 volts) is also available. Area one is the special case of the level line where length equals one clock pulse. Each of these is a vector so that only the beginning and the end points need be given and the rest will be calculated, assembled, and transmitted to the PWG.

The reason for this method is that most of the pictures to be generated can be done using a two byte, single integer word. On the rare occasion when one cannot be done this way, as yet not encountered, an option exists which uses two integer words (of 16 bits each), prefixed with a negative sign, to provide any vector whatsoever. The modifications to PICTUR are tc be found at the end of Appendix F.

Area three is a random number generator (RNG) used to create digital noise. The RNG is a simple multiplying type which provides

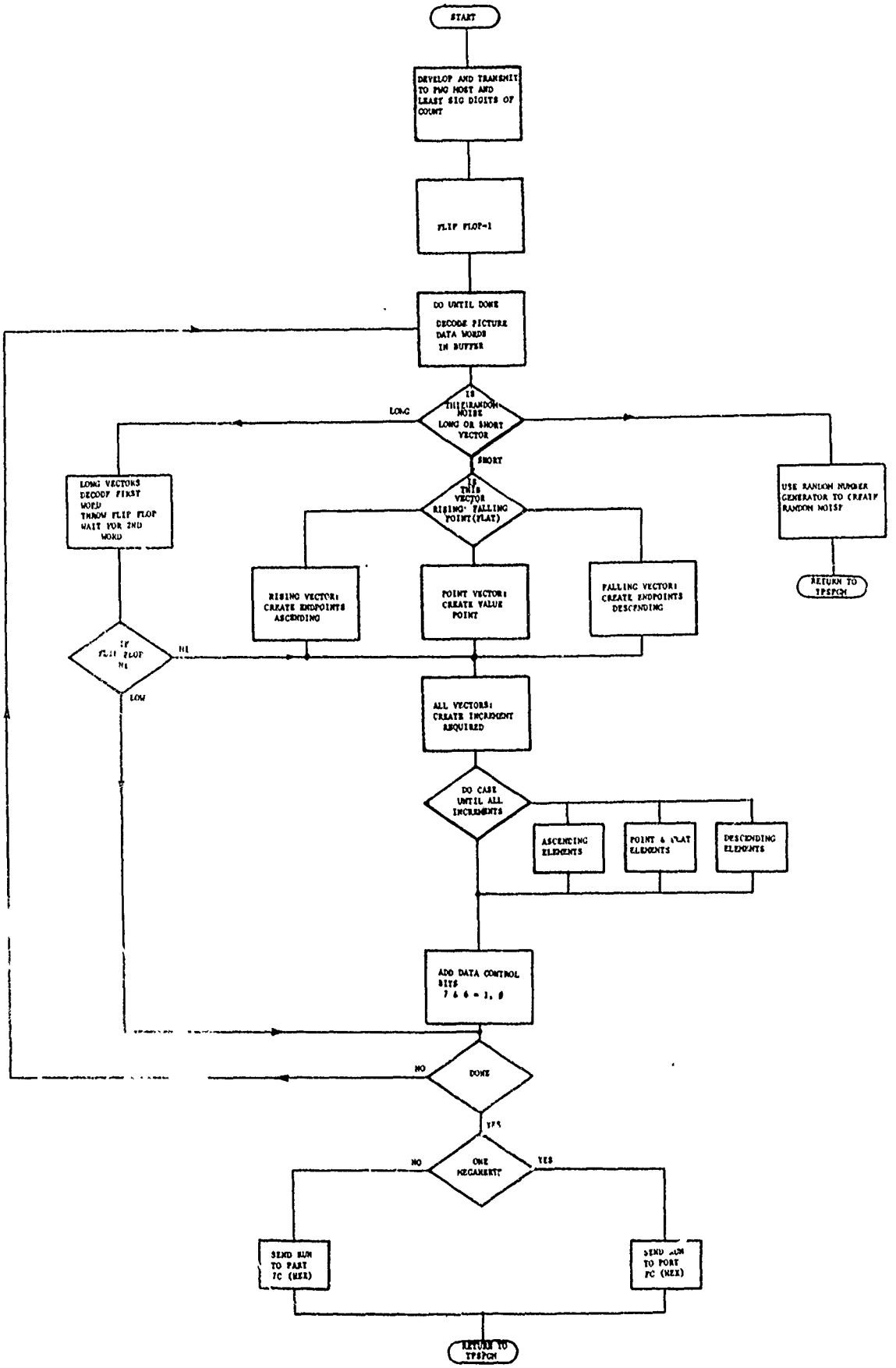


Figure 14. PICTUR Flowchart

random values from 1/2 volt to 3 volts in 1/2 volt steps. The picture module puts a particular picture into the display hardware and allows insertion of any ERROR chosen dysfunction.

As an example, consider a digital to analog converter. Input is 1 of 64 discrete voltage levels encoded in 6 parallel bits. (Drawing 3.) If one of the parallel bit drivers is on, then that driver's output is continuously high regardless of what the input to it is. Thus a malfunction exists that should be demonstratable. One place to inject this malfunction is during the creation of the picture by logically ORing in that bit before data transmission. All the rest of the data will be correct but the error bit will always be on and behave exactly as the actual equipment will when broken as described above.

Another example malfunction exists when a bit is turned off continuously. This is mimicked by using a one's complement of the bit to be removed, logically ANDed with the data. By guaranteeing that the data is logically ANDed with a zero in a particular bit, assurances are made that all of what is in the original picture passes except for the chosen bit. The errors described above are common failures within the actual equipment.

The support software consists of a short program which creates a unique disk record within an error file (Appendix G). Each record is a specific problem which the student will be required to solve. The program consists of two data sets, created using the editor, that are immediately put to disk. The program then terminates. This program is simple enough to preclude serious problems in its own maintenance. FORTRAN was chosen because BASIC files are not compatible with the FORTRAN application program.

The data statement NAME is filled with the file name. The name ERRS??DAT is the file name with the ?? being the particular record number under consideration. The application program will take the octal number of the faceplate's thumb wheel switch and insert an alphanumeric representation of it into the error file-record request.

The data statement IPUT is a coded error record. The nature of the error routine is that multiple dependent and independent dysfunctions are easily created, given the correct error file. The first element in the file is the length of the file, in addressable words. The next seven elements are seven different switches and their associated positions. Because the list is constant, the switch numbers are implied and only the positions appear on the list. The appearance of a zero indicates a "don't care" switch position. The last three values are the error type, card to be replaced, and picture affected respectively.

Of the last three values, the first has a dual role. If it is greater than 49 it is used as a selector of a bit stuck on, or off, as described above. The formula used is:

$$\text{Bit } \# = \text{Value} - 56 \qquad (2)$$

where $49 < \text{Value} < 63$.

When this value is coded less than 50, it is taken as the assignment of a new picture, not in the normal set, in place of the one usually found at this switch setting. A separate list is required for each picture affected. The length of the record is 91 words composed of a maximum of nine error lists of ten elements each, plus the record size itself.

Currently there are over 30 different error records on the system. The potential is for 63, with the ØØ record being the null record for normal operation. All error records were decided upon and encoded by instructor personnel.

The second support program is the picture code generator (Appendix H). This program is written in BASIC to provide ease of use and/or possible maintenance. There are five elements within the program covering points, vectors, and random noise pictures. Due to the extensive documentation within the program all that needs to be said here is that the output is a picture code printout which must be inserted manually into the application program prior to compilation.

Performance Evaluation Test Procedures

The testing of this system consisted of taking a class of new TPS-43E instructors as students when they were about to enter the BITE training phase of the course. The class was broken into two groups. One group was trained on the actual radar, while the other group trained on the BITE simulator. At the conclusion of training each group was tested on knowledge and performance using the alternate equipment trained on. Each group was then given a questionnaire concerning observations of each environment.

Results

The maintenance simulator compared well on ease of use and fidelity of waveforms; the simulator was superior in terms of space and flexibility. The negative remarks were that it drew some waveforms slowly and currently only covered BITE functions. The instructors were unanimous in recommending the trainer be used in place of actual BITE equipment.

Observations

The maintenance simulator (at delivery) performed the BITE functions requested by the user at the beginning of this project. Upon turnover to the user, one of the instructors suggested another BITE function which the simulator hardware could already support. The software was generated in two days (in final form) which indicates the expansion capabilities of the equipment. This fact was not lost on the user who has ordered an expanded model this fiscal year, and another next fiscal year.

CHAPTER V

CONCLUSIONS

Microcomputer driven simulators are feasible for electronic maintenance training. Computers are available from vendors which can be interfaced to maintenance mockups using conservative, yet current, technological concepts. The interfaces resulting from this study permit S-100 bussed microcomputers to be used in a wide variety of training simulators. The TPS-43E BITE is only one example of the ways in which the microcomputer driven maintenance simulator may be used.

In the TPS-43E BITE simulator design phase, concurrent hardware and software construction was an absolute requirement. The potentials of hardware and software design each constrained and aided the other to such an extent that neither could be created alone. The hardware versus software dichotomy of the past three decades vanished in the face of a portable and cheap microcomputer in the hands of the programmer-designer.

Selection of commercial equipment is greatly assisted by decision matrices, since the equipment sought is not expensive enough to support a request for proposal from the vendors. In this case the commercial equipment selected, via an interaction of maximum CPU architectural power, bus utility, and software power, led to a Z-80 processor with an S-100 bus which supports FORTRAN IV. Source data for the decision matrices was frequently supplemented by user reports found in trade journals.

The prototype BITE simulator, (from the design, financial and training points of view), is an unqualified success. The equipment has met, or exceeded, every expectation envisioned at the outset for performance, reliablity and maintainability. The overall cost of the project, exclusive of labor and initial design equipment, was $6,500. The total prototype investment was about $65,000. The simulator was delivered two months earlier than projected and began use as a trainer within the first week after delivery. The early decision to develop hardware and software concepts concurrently is the source of the success enjoyed by this project.

The lack of a DOD mandate to Electronic Systems Division (ESD) to pursue the maintenance simulator concept created the source of the management challenge. When a system programming office (SPO) within ESD is created to address maintenance simulators, the project monies and personnel will become reliable resources. Until such a SPO, or its equivalent, is created, projects such as this should be viewed in terms of the person who has the courage to take primary responsiblity to ensure project completion. This same person must also be considered in terms of ability to deliver command supported investment of resources to a special activity outside of normal resource allocation channels.

Within the engineering area of concern, the most important thing found was the need for reliable, current data. The trade journals, notably BITE and Electronics, plus the applications notes of the parts manufacturers, were the only reliable source documents available. A single S-100 documentation from the original equipment manufacturers was either incomplete or non-existent; however, the combined data of MITS and CROMENCO, plus INTEL's 8080 timing charts and the

aforementioned journals, were a good substitute. Parts catalogues must be no more than one year old to be useful; therefore, a wise investment was the purchase of several major companies TTL digital components catalogues with cross references for substitutions.

The next most important finding in the engineering area was that the top down design of the hardware-software speeded the development of both. From the programming point of view, hardware became frozen software and the electronic technician's view became "software is temporary hardware." With the views described above, the software acquired hardware overtones, uncommon to higher order languages such as FORTRAN, that generated very fast, efficient code. Similarly, the hardware was basically designed as an algorithm and then was implemented using the appropriate components. By conceiving of the entire device, hardware-software, as a single concept, a top down perspective of design made project planning a trivial exercise outside of the already described institutional problems.

The results of this project indicate an interesting variety of areas for future work. Further military applications include simulation of high voltage power panels, critical circuit troubleshooting, radar maintenance display generation, morse code intercept and transmit training, and oscilloscope wave form demonstrations and training. In the medical area, using a much slowed waveform generator with a voice coil loudspeaker would enable coronary nursing personnel to train with simulated abnormal wave forms. At this lower speed level simulations of EKGs, EEGs and other medical monitor scopes could be made of any known pattern. Used exactly as constructed, the hardware could monitor and control a very sophisticated security system, or run heating

systems or even a traffic light system. The control set could run a MOOG synthesizer. Some modification of the D/A converter would make the PWG a function generator of major value as a test instrument. Used in conjunction with communication equipment, the hardware could test and monitor a variety of circuit parameters with all manner of traffic and report abnormal system behavior.

Maintenance training, traditionally taught using actual equipment, is now being taught using a microcomputer driven simulator. The system hardware-software for this project can be used in a variety of training and nontraining environments where cheap and rugged process control is desired. Cost and training effectiveness make the maintenance simulator a valuable tool for technical schools everywhere.

BIBLIOGRAPHY

Boyle, E.B. Trends in Digital Simulation, NAVTRADEVCEN IH-1B, 1967.

Datapro Research Corporation, All About Microcomputer Specifications, 1805 Underwood Blvd., Delran, N.J. 08075, June 1977

Kargo, Donald W. and Steffen, Dale A. Performance Training Corral for Electronics Principles Course, AFHRL-TR 76-62(i), Air Force Human Relations Laboratory, Sept 76.

Keesler AFB Study, TTV. Staff Study on the Feasibility of Using Simulation in Maintenance Training, 3 Oct 77.

King, William J. Performance Specifications for a Maintenance Simulator for the AN/ACQ 126 Transceiver, Technical Report NAVTRADEVCAN 77-C-0128-1 by Honeywell, Inc., ADA020588, June 74.

Osborne, Adam, An Introduction to Microcomputers, Vol. II, Some Real Products. Osborne & Associates, Inc., Berkeley, CA. C. 1976

United States Air Force, Management of the USAF Automatic Data Processing Program, AFR 300-2, 19 Aug 77, Change 1 (No date available)

United States Air Force, MILITARY STANDARD DIGITAL COMPUTING SYSTEMS FOR REAL-TIME TRAINING SIMULATORS MIL-STD-876A (USAF), 8 July 1971, SUPERSEDING MIL-STD-876 (USAF), 21 February 1967

United States Air Force, Keesler Technical Training Center, Operation of Training Services Activities and UPT Visual Services and Functions, ATCR 52-33, 1 Apr 77, Change 29, Jul 77, KTTC Sup, 27 Sept 76

United States Air Force, Keesler Technical Training Center, Training Services, ATCR 50-22, 15 Apr 77, Change 1, 29 Jul 77, KTTC Sup, 29 Sept 77

APPENDIX A

TRAINING DOCUMENT FORMATS

DEPARTMENT OF THE AIR FORCE
Headquarters, Air Training Command (ATC)
Randolph Air Force Base, Texas 78148

CTS 52-E3AZR30352 003
(PDS Code NZF)
23 October 1978

AN/TPS-43E O/I Maintenance

1. Purpose. This course training standard as prescribed in ATCR 52-17:

a. Established the tasks, knowledge and proficiency level of training to be provided by Course E3AZR30352 003, AN/TPS-43E, O/I Maintenance.

b. Provides the basis for the development of more detailed training materials and objectives, and training evaluation instruments for the course.

2. Course Description. The course covered by this standard is designed to provide training for Air Force personnel who possess AFSC 30352/72 and the skills and knowledge necessary to perform organizational and intermediate maintenance on the AN/TPS-43E radar. Scope of training includes circuit analysis, theory of operation, performance tests, adjustment operation, troubleshooting, and repair and the use of pertinent test equipment.

NOTE: Trainees entering this course at a level below that specified by AFR 50-9, and/or other established prerequisites cannot be expected to achieve levels indicated.

3. Qualitative requirements. Attachment 1 contains the list of tasks, knowledge, and proficiency reference in paragraph 1.

4. Recommendations. Comments and recommendations are invited concerning quality of ATC training and graduates (AFP 50-38). Use this CTS as a reference and address correspondence to ATC/TT, Randolph Air Force Base, Texas 78148.

OFFICIAL

JOHN W. ROBERTS, General, USAF
Commander

DOUGLAS S. HEART, Colonel, USAF
Director of Administration

1 Attachment
Qualitative Requirements

This Supersedes CTS 52-2ASR30352-006, 22 March 1978
Approval Date: TTGXE, 23 October 1978
DISTRIBUTION: X
ATC/TTOE-2; CINCUSAFE/DPAT-3; TAC/DPPTT-3; NGB/DPT-1; Keesler: TTGXE-10; 3395 TCHTG/TTGD-B-20.

QUALITATIVE REQUIREMENTS

CTS 52-3AZR30352 003

PROFICIENCY CODE KEY		
	SCALE VALUE	DEFINITION: The Individual
TASK PERFORMANCE LEVELS	1	Can do simple parts of the task. Needs to be told or shown how to do most of the task. (EXTREMELY LIMITED)
	2	Can do most parts of the task. Needs help only on hardest parts. May not meet local demands for speed or accuracy. (PARTIALLY PROFICIENT)
	3	Can do all parts of the task. Needs only a spot check of completed work. Meets minimum local demands for speed and accuracy. (COMPETENT)
	4	Can do the complete task quickly and accurately. Can tell or show others how to do the task. (HIGHLY PROFICIENT)
*TASK KNOWLEDGE LEVELS	a	Can name parts, tools, and simple facts about the task. (NOMENCLATURE)
	b	Can determine step by step procedures for doing the task. (PROCEDURES)
	c	Can explain why and when the task must be done and why each step is needed. (OPERATING PRINCIPLES)
	d	Can predict, identify, and resolve problems about the task. (COMPLETE THEORY)
**SUBJECT KNOWLEDGE LEVELS	A	Can identify basic facts and terms about the subject. (FACTS)
	B	Can explain relationship of basic facts and state general principles about the subject. (PRINCIPLES)
	C	Can analyze facts and principles and draw conclusions about the subject. (ANALYSIS)
	D	Can evaluate conditions and make proper decisions about the subject. (EVALUATION)

– EXPLANATIONS –

* A task knowledge scale value may be used alone or with a task performance scale value to define a level of knowledge for a specific task. (Examples: b and 1b)

** A subject knowledge scale value is used alone to define a level of knowledge for a subject not directly related to any specific task, or for a subject common to several tasks.

– This mark is used alone instead of a scale value to show that no proficiency training is provided in the course, or that no proficiency is required at this skill level.

X This mark is used alone in course columns to show that training is not given due to limitations in resources.

ATC Keesler 7-3081

Attachment 1

Tasks, Knowledge and Proficiency Level	
1. GENERAL	
a. Purpose, characteristics and capabilities	
(1) AN/TPS-43E Radar System	C
(2) Ancillary Equipment	C
(3) Site Test Equipment	B
b. Locate and Identify all Assemblies, Subassemblies, and major components	3c
c. AN/TPS-43E Digital and Analog Techniques	C
d. Utilize Schematic, and Functional Diagrams to determine circuit operation and component function	3c
e. Practice proper Safety Procedures	3c
f. Remove and replace subassemblies, printed circuits and planar array boards	3c
2. ALIGNMENT AND THEORETICAL TROUBLESHOOTING OF THE SYNCRONIZER AND SYSTEM TIMING	2c
3. ALIGNMENT AND THEORETICAL TROUBLESHOOTING OF THE TRANSMITTER	
a. Frequency Generator	3c
b. Driver Amplifier	3c
c. Pulser	3c
d. Power Amplifier	3c
4. ALIGNMENT AND THEORETICAL TROUBLESHOOTING OF THE RECEIVERS	
a. Analog Receivers	3c
b. Jamming Analysis Transmission Selection (JATS) Processor	3c
c. Search Receiver	3c
d. Search Processor and Integrator	3c

Tasks, Knowledge and Proficiency Level	
e. Search built-in-test-equipment (BITE)	2b
f. MTI Receiver	3c
g. MTI Processor and Integrator	2b
h. MTI Processor BITE	2b
5. ALIGNMENT, AND THEORETICAL TROUBLESHOOTING OF THE HEIGHT COMPUTERS AND EVALUATOR	
a. Height Processor	3c
b. Height Computers	3c
c. Height Evaluator	3c
d. Height Computers and Evaluator BITE	2b
6. ALIGNMENT, AND THEORETICAL TROUBLESHOOTING OF THE SIGNAL DISTRIBUTION UNIT (SDU)	
a. Video Gating	3c
b. Range Azimuth Gating	3c
c. Digital Height Readout (DHRO)	3c
d. SDU BITE	2b
7. ALIGNMENT, AND THEORETICAL TROUBLESHOOTING OF THE AN/UPA-62C	
a. Range and Timing	3c
b. Azimuth Circuits	3c
c. Deflection Circuits	3c
d. Video Circuits	3c
8. ALIGNMENT, AND THEORETICAL TROUBLESHOOTING OF THE IFF/SIF SYSTEM	
a. AN/TPS-43F IFF/SIF Distribution Cabinet	3c

Tasks, Knowledge and Proficiency Level	
b. AN/GPS-13A Interference Blanker	3c
c. OK-217/UPX RF Switching Group	3c
d. AN/UPX-23 IFF/SIF Interrogrator/Responder	3c
e. AN/UPA-59A Coder/Decoder	3c
9. ANTENNA SYSTEM	
a. Locate and Identify all assemblies and subassemblies	3c
b. Erection and Mechanical Antenna Orientation	c
10. MEASURE AND ADJUST AC AND DC POWER SUPPLIES	3c
11. UTILIZE SCHEMATICS AND FUNCTIONAL DIAGRAMS FOR SIGNAL FLOW AND SYSTEM INTERCABLING	3c
12. PARTICIPATE IN USAF GRADUATE EVALUATION PROGRAM	a

COURSE CHART

NUMBER	POS CODE	DATE
E3AZR30352 003	NZF	24 October 1978

COURSE TITLE
AN/TPS-43E O/I Maintenance

SUPERSEDES COURSE CHART	CENTER/DEPARTMENT/GROUP
*E2ASR30352 006, 19 June 1978	Keesler, 3395 TCHTG

APPLICABLE TRAINING STANDARD
CTS 52-E3AZR30352 003, 23 October 1978

OPR AND APPROVAL DATE	COURSE SECURITY CLASSIFICATION
KTTC/TTGXE, 24 October 1978	CONFIDENTIAL

INSTRUCTIONAL DESIGN	LOCATION OF TRAINING	TABLE ATTACHMENTS
Group-Paced	Keesler AFB MS	II

COURSE LENGTH (79 ACADEMIC DAYS) (WARTIME COURSE LENGTH 64 ACADEMIC DAYS)

		HOURS
Technical Training		624
Military Training		8
Commander's Calls/Briefings (AFRs 30-1 and 190-18)	3	
Local Conditions Course, Course II (AFR 50-24)	2	
End-of-Course Appointments; Predepature Safety Briering (ATCR 127-1)	3	
TOTAL		632

REMARKS
Effective Date: 9 Nov 1978 with class 781109.

*Course Chart E2ASR30352 006, 19 June 78, applies to all classes prior to 781109.

TABLE I - MAJOR ITEMS OF EQUIPMENT

Training Equipment - AN/TPS-43E Radar Set; AN/UPA-62C Indicator; AN/UPA-59A Decoder; AN/GPS-13A Interference Blanker; AN/UPX-23 Interrogator; RF Switching Group and Monitor; OK-217.

Test Equipment: AN/UPM-37, Test Set; TK-465, Oscilloscope; DM-43-DD40, Digital Multimeter and Display Unit.

ATC FORM APR 78 449 REPLACES ATC FORM 449, MAR 76 AND ATC FORM 449 A, MAR 76

COURSE CHART E3AZR30352 003 - TABLE II - TRAINING CONTENT

Course Material - UNCLASSIFIED — 88 Hours

BLOCK I - System Introduction and Synchronizer

Orientation (1 hr); Training Evaluation Feedback System (0.5 hrs); System Description and Block Diagram (6.5 hrs); Digital Techniques and Logic Symbology (34 hrs); System Synchronizer and Timing Circuits (27 hrs); System Maintenance and Performance Procedures (14 hrs); Measurement and Critique (3 hrs); Military Training (2 hrs).

(Equipment Hazards and Personnel Safety Integrated with Above Subjects)

Course Material - UNCLASSIFIED — 56 Hours

BLOCK II - Transmitter

Transmitter System Block Diagram (4 hrs); Frequency Generator (5 hrs); High Voltage Driver (6 hrs); Pulser (10 hrs); Power Amplifier (6 hrs); Power Distribution (5 hrs); Heat Exchanger and Waveguide Pressurizer/Dehumidifier (2 hrs); Transmitter Performance Testing (14 hrs); Measurement and Critique (3 hrs); Military Training (1 hr).

(Equipment Hazards and Personnel Safety Integrated with Above Subjects)

Course Material - UNCLASSIFIED — 88 Hours

BLOCK III - RF/IF Receivers and Jats

Receiver System Block Diagram (6 hrs); Receiver Timing and Gating (9 hrs); Analog Receivers, (23 hrs); Receiver Checks and Alignments (16 hrs); JATS Processor Theory (24 hrs); JATS Performance Tests and Alignments (7 hrs); Measurement and Critique (3 hrs).

(Equipment Hazards and Personnel Safety Integrated with Above Subjects)

Course Material - UNCLASSIFIED — 96 Hours

BLOCK IV - Digital Search and MTI

Digital Search (18 hrs); Search BITE (12 hrs); Digital MTI Processor and Integrator (29 hrs); MTI BITE (19 hrs); MTI and Search Performance Testing (14 hrs); Measurement and Critique (3 hrs); Military Training (1 hr).

(Equipment Hazards and Personnel Safety Integrated with Above Subjects;

COURSE CHART E3AZR30352 003 - TABLE II - TRAINING CONTENT

Course Material - UNCLASSIFIED — 96 Hours

BLOCK V - Height Processing System

Height Processing System Block Diagram (16 hrs); Height Computers Theory (24 hrs); Height Evaluator Theory (24 hrs); Height System BITE (18 hrs); Height System Performance Testing (11 hrs); Measurement and Critique (3 hrs).

(Equipment Hazards and Personnel Safety Integrated with Above Subjects)

Course Material - UNCLASSIFIED — 80 Hours

BLOCK VI - SDU and AN/UPA-62C

SDU Theory (24 hrs); SDU Performance Checks (6 hrs); AN/UPA-62C Functional Block Diagram (4 hrs); Indicator Range and Timing (12 hrs); Azimuth Circuits (13 hrs); Deflection Cirtuits (6 hrs); Video Circuits (2 hrs); D.C. Power Distribution (3 hrs); Indicator Performance Testing and Alignments (6 hrs); Measurement and Critique (3 hrs); Military Training (1 hr).

(Equipment Hazards and Personnel Safety Integrated with Above Subjects)

Course Material - UNCLASSIFIED — 56 Hours

BLOCK VII - AN/UPX-23

AN/UPX-23 Block Diagram (4 hrs); Trigger and Timing Circuits (16 hrs); Transmitter (6 hrs); Receiver Circuits (8 hrs); Video Circuits (8 hrs); Performance Testing and Alignments (11 hrs); Measurement and Critique (3 hrs).

(Equipment Hazards and Personnel Safety Integrated with Above Subjects)

Course Material - CLASSIFIED — 72 Hours

BLOCK VIII - IFF/SIF System

IFF/SIF Functional Block Diagram (3 hrs)(U); OK-217/UPX RF Switching Unit (6 hrs)(U); AN/GPS-13A Interference Blanker (7 hrs)(U); AN/UPA-59A Decoder Group (22 hrs)(U); IFF/SIF System Performance Testing and Alignments (9 hrs)(U); Measurement and Critique (3 hrs)(U); MODE 4 KIR (18 hrs)(C); Course Critique and Graduation (1 hr)(U); Military Training (3 hrs)(U).

(Equipment Hazards and Personnel Safety Integrated with Above Subjects)
(Above Titles are Unclassified)

APPENDIX B

LETTER OF TECHNICAL RECOMMENDATIONS

TO STAFF STUDY

3390 TCHTG/TTMKP (1st Lt Winthrop, 4290) 26 August 1977

Recommendation to Use a Micro-Processor to Drive A TPS-43 Training Simulator

3300 TCHTW/TTV

1. This letter explores the basis for recommending use of a micro-processor to simulate the output of a TPS-43 radar matintenance panel, Built in Test Equipment (BITE). This letter shows that a micro-processor simulation of the BITE is inherently the equal of the original BITE by: describing the BITE to be simulated; the BITE inputs/outputs (I/O) to be generated; types of micro-processor equipment needed to simulate BITE and I/O; the developmental support required; and, a list of parameters to be used when considering acquistion.

2. Micro-processor simulation of the BITE is inherently the equal of the original BITE (for training purposes) because the TPS-43 radar currently has a micro-computer as its BITE system. The BITE is scattered throughout the radar to sample selected essential signals which illustrate the state of repair of the system. The BITE is controlled by a panel containing several sets of multi-switch selecting knobs that direct sample signals from the radar, through a series of converters and counters, to an oscilloscope for signal display. This panel contains arrays of lights which also display certain signals from the system. The BITE presents about 20 standard displays for over 100 possible BITE test positions (when the radar is working correctly). The maintenance person uses this information to pin-point the functional subsystem of the radar that is not working right. Repair is accomplished by "Black Box" replacement of the component at fault. The BITE micro-computer system described above is built into the TPS-43 Radar.

3. BITE I/O is digital, and lends itself to digital simulation. Inputs are from the system in analog form through an analog to digital converter, which enables simple arithmetic testing operations to be performed on the inputs. The tested signals are now sent to an oscilloscope, through a digital to analog converter for display. The radar signals to be sampled are slected via the BITE control panel. Display lights are indicators of digital data taken after the BITE system has captured its sample for testing.

4. The BITE system can be simulated by a variety of micro-computers now on the market, or soon to be announced onto the market, used in a dedicated manner. Any such micro-computer system would keep arrays of signals in memory to sample instead of using a real radar for source data. Such a system would output these signals under control of a training program, in accordance to the commands input from switch settings on a simulated BITE control panel. The BITE control panel

simulation would be sampled frequently by the system, under program control, and would also show light displays appropriate to the data area being sampled. Equipment analysis taken from available journals and other commercial literature indicate that many micro-computer systems can operate at speeds high enough to produce an identical output to the actual radar system when BITE is engaged. One output line (PORT) of the micro-computer system would go directly into a digital to analog converter and then to an oscilloscope. Use of the oscilloscope is part of the training environment, thus it has not been simulated. On other systems to be simulated video presentation can be substituted directly for the D/A converter-oscilloscope combination to include captions and/or other word displays. Power meters, frequency indicators, etc., not functionally within the BITE system can be simulatd by using digital displays also driven by the micro-computer.

5. Any micro-computer system chosen will be able to operate with less equipment than will be needed to develop it. Development support will include features needed to write and check computer programs (software). Equipment (hardware) for mass storage in the form of: magnetic tape or disc, beyond the needs of the final system; Erasable Programmable Read Only Memory (EPROM), and its associated equipment; larger power supplies and special controller units to use this hardware. These one time purchases will carry over as benefits into development of other simulators configure around this micro-processor. Precisely because the on-going use of equipment and other software materials used in future developmental support, careful attention must be paid to continued availability and support of both equipment and software.

6. The list below represents parameters considered essential to a prudent selection of equipment:

a. Hardware Requirements

(1) Modular Interchangeability (Compatibility with various plug-in units)

(2) Industrial/Military Standard

(3) Stable Logistic Support

(4) Documentation (Schematics and Operating Characteristics)

(5) Maintenance Support

(6) D/A Converter Capability (with acceptable benchmark criteria)

(7) Sufficient Power Capability

(8) I/O (Input/Output) capability is described based on eight bit word system or else comparable equipment for 16 bit systems

(a) Parallel Ports (2 ea) for D/A Converter Unit (8-bit words)

(b) Serial Ports (3 ea) for Paper Tape, Keyboard, Cassette, etc. (Audio cassette requires a modem interface)

(c) Parallel Port (1 ea) for Control of Training Console Panel Functions (meters, lights, and input requests)

(9) Mass Storage

(a) Off-line (Paper Tape, Disc, or Magnetic Tape)

(10) Peripherals (Disc, TV Monitor, Cassette, Keyboard)

b. Software Support

(1) Assembler and/or Higher-Level Language (AF accepted or Industrial Standard)

(2) Library or User's Group Sources

(3) Operating System/Editor Capability

(4) Resident Software Programmer

c. Costs of Equpment

(1) Micro-processor Hardware (Off-Shelf): $1000 - $2000

(2) Software (Off-Shelf): $1000 maximum

(3) Firmware (Programming PROMs, etc.): $1000 - $2000

(4) Trainer Specific Hardware (O-Scope, Mockup, etc)

(5) Peripherals

(a) Disc $1000 - $2000

(b) TV Monitor: $500 (with Interface Board)

(c) Keyboard - $100

(d) Audio Cassette: $300 (with tape unit)

This list is constructed to provide flexibility in terms of choice, support and price while insuring against non-standard equipment and/or software. The system maintenance and development should be within the abilities of a programmer with assembly programming experience and also some electronics experience.

7. Prospects of using a micro-computer to simulate the output of a TPS-43 Radar BITE system are clearly excellent, as described above. The criteria described in paragraph 6 represent realistic goals that are available in today's market.

MICHAEL F. WINTHROP, 1ST LT, USAF
Computer Technology Branch
3390TCHGP

APPENDIX C

LETTER OF INQUIRY

DEPARTMENT OF THE AIR FORCE
HEADQUARTERS 3300 TECHNICAL TRAINING WING (ATC)
KEESLER AIR FORCE BASE, MISSISSIPPI 39534

REPLY TO ATTN OF HQ, 3300TCHTW/TTVET

SUBJECT Request for Information

TO

1. This letter is a request for information about your product line of micro-computers. My organization is conducting a feasibility study concerning the use of a micro-computer as an interactive and interrupt driven training device. The information that I need concerns your 'off-theshelf' products, specifically; data about capabilities, compatabilities and costs.

2. The requirements of my use are:

a. Hardware Requirements

(1) Modular Interchangeability (compatibility with various plug-in units)

(2) Industrial Standard

(3) Stable Logistic Support

(4) Documentation (Schematics and Operating Characteristics)

(5) Maintenance Support

(6) D/A Converter capability with acceptable benchmark criteria of 2 MHz (parallel input, serial output)

(7) Sufficient Power Capability

(8) I/O (Input/Output) Capability (Minimum examples below are 8 bit oriented)

(a) Parallel Ports (2 ea) for D/A Converter Unit (8-bit words)

(b) Serial Ports (3 ea) for paper tape, keyboard, cassette, etc. (audio cassette requires a modem interface)

(c) Parallel Port (1 ea) for Control of Training Console Panel Functions (meters, lights, and input requests)

(9) Mass Storage

(a) Non-Volitale Memory (resident, i.e. EPROM chips)

(b) Off-line (Paper Tape, Disc, or magnetic Tape)

(10) Peripherials (Disc, TV Monitor, Cassette, Keyboard)

b. Software Support

(1) Assembler and/or Higher-level Language (AF accepted or Industrial Standard)

(2) Library or User's-Group Source

(3) Operating System/Editor Capacility

3. This information is being requested without obligation to the United States Government.

4. Please reply to: HQ, USAF 3300 Technical Training Wing
Training Equipment Branch/TTVET
Keesler Air Force Base, MS 39534

JAMES R. BRIDGES, Jr., Major, USAF
Chief, Training Services Division
HQ, 3300 Technical Training Wing

APPENDIX D

DECISION MATRIX

COMPANIES QUERIED

AND RESPONDENTS (*)

MICROCOMPUTER MANUFACTURERS Listed below, for your convenience in obtaining additional information are the full names, addresses, and telephone numbers of the manufacturers whose products can be compared in the comparison charts. More details about most of these computers can be found in the Directory of Products in Binder 2		American Microsystems, Inc 3800 Homestead Rd Santa Clara, CA 95051 Tel (408) 246 0330	Applied Systems Corporation 26401 Harper Ave St Clair Shores, MI 48081 Tel (313) 779-8700	Computer Automation, Inc 18651 Von Karman Ave Irvine, CA 92664 Tel (714) 833-8830	Control Logic, Inc Nine Linscott Rd Natick, MA 01760 Tel (617) 655-1920	CROMEMCO Incorporated 2432 Charleston Rd Mountainview, CA 94043 Tel (415) 964-7400	Digital Electronics Corporation 415 Pierson Street Oakland, CA 94601 Tel (415) 532-6920	Digital Equipment Corporation 146 Main Street Maynard, MA 01754 Tel (617) 897-5111	Diversified Technology P O Box 465 Mendenhall, MS 39157 Tel (601) 856-4121
DESCRIPTION OF EQUIPMENT (FIGURE OF MERIT FOM)	Y	70308	46872	53136	133224	315648	0	487768	71944
a Hardware Requirements									
(1) Modular Interchangeability (compatibility with various plug-in cards)	R	No	No	No	No	Yes	No	No	No
(2) Industrial standard	N	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
(3) Stable Control Source	L	Yes	No	No	No	No Data	No Data	No Data	No Data
(4) Documentation Schematics and Operating Diagrams(certified)	O	Yes	No Data	Yes	Yes	Yes	Yes	Yes	Yes
(5) Maintenance Support Warrantee Data with Documentation	K	Yes	No Data	No Data	No Data	Yes	Yes	Yes	Yes
(6) A/D Converter Capability with acceptable benchmark criteria of 2 MHz (parallel input, serial output)	N/A								
(7) Sufficient Power Capability	V	No Data	Yes	Yes	Yes	Yes	Yes	Yes	Yes
(8) I/O (Input Output) Capability (Minimum examples below are 8 bit oriented)									
(a) Parallel Ports (1 ea) for A/A Converter unit (8 bit word)	N/A								
(b) Serial Ports (1 ea) for paper tape, keyboard, cassette, etc (audio cassette requires a modem interface) (Range to 2)	S	2	2	2	2	2	2	2	2
(c) Parallel Port (1 ea) for control of Training Console Panel Functions (meters, lights, and input requests) (Increase to 4)	C	4	4	4	4	4	4	4	4
(9) Mass Storage									
(a) Non-volatile Memory (eg Hard, i.e., FF&M disk)	M	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
(b) Off line (Paper tape, FD, or Magnetic tape)	O	OM	OM	OM	OM	OM	OM	OM	OM
(10) Peripherals (Keyboard, monitor, printer)	A	Yes	Yes	Yes	Yes	Yes	*No Data	Yes	Yes
b Software Support	R	OK (18)	OK (18)	OK (16)	OK (24)	OK (24)	OK (24)	OK (8)	OK (17)
(1) Assembler and/or Higher Level Language (All accepted or Industrial Standard)		Yes	Yes	Yes	Yes	Yes	Yes	No	Yes
(2) Library of User's Program Source	I	Yes	Yes	No	Yes	Yes	Yes	No	Yes
(3) Operating System/Editor Capability		Yes	Yes	Yes	Yd.	Yes	Yes	No	Yes
Instructions	I	72	78	84	158	152	91	450	91
Bits in a Word	W	8	8	16	8	8	8	16	8

Remarks

*No I/O Interface

Legend: OK All Right
NG No Good
D Disk
M Magnetic Tape
P Paper Tape

MICROCOMPUTER MANUFACT REPS

Listed below, for your convenience in obtaining additional information, are the full names, addresses, and telephone numbers of the manufacturers whose products are summarized in the comparison charts. More details about most of these companies can be found in the Directory of Vendors in Reader 2

DESCRIPTION OF EQUIPMENT (FIGURE OF MERIT FOM)		[illegible] Instruments Inc [illegible]	Electronic Memories & Magnetics Corp, 12621 Chadron Ave, Hawthorne, CA [illegible], Tel (213) [illegible]	[illegible] Inc [illegible]	General Automation [illegible]	[illegible] Company [illegible]	[illegible] Blvd, San Leandro, CA 94577, (415) 483 2093	[illegible] CA 95051 [illegible]	International Microsystems Inc, 22 [illegible]
	Y	7551	182448	0	3600	0	136640	78241	0
a Hardware Requirements									
(1) Modular Interchangeability (Compatibility with various plug in units)	R	Yes	Yes	N	No	No	Yes	N	No
(2) Industrial Standard	A	No	No	Yes	Yes	Yes	Yes	Y	No Data
(3) Simple Logistic Support	L	No	No	No Data	No Data	No	No Data	No Data	No Data
(4) Documentation (Schematic, and Operational Characteristics)	D	Yes	No	Yes	Yes	Yes	Yes	[illegible]	No Data
(5) Maintenance Support (Warrantee only with preassembled)	F	Yes	No	Yes	Yes	Yes	Yes	Yes	No Data
(6) D/A converter capability with acceptable benchmark criteria of 2 MHz (parallel input, serial output)	N/A								
(7) Sufficient Power Capability	P	Yes	Yes	Yes	Yes	Ye[s]	Yes	Yes	No Data
(8) I/O (Input/Output) Capability (Minimum examples below are 8 bit oriented)									
(a) Parallel Ports (? ea) for D/A Converter Unit (8 bit words)	N/A								
(b) Serial Ports (1 ea for paper tape, keyboard, cassette, etc (audio cassette requires a modem interface) (Reduce to 2)	S	2	2	2	2	2	2	[illegible]	No Data (0)
(c) Parallel Port (1 ea) for Control of Training Console Panel functions (meters, lights, and input requests) (Increase to 4)	C	4	4	4	4	4	4	4	No Data (0)
(9) Mass Storage									
(a) Non-volatile Memory (resident, i.e., EPROM chips)	M	Yes	No Data	No Data	Yes	Yes	Yes	Yes	Yes
(b) Off-line (Paper Tape, Disk, or Magnetic Tape)	D	M	DM	D	T	D	DM	DM	No Data
(10) Peripherals (Keyboard, Monitor, Printer)	A	Yes	Yes	No	Y	No Data	Yes	Yes	No Data
b Software Support	R	NG*(3)	NG (14)	NG (15)	AK (31)	NG (9)	AK (20)	AK (20)	No Data
(1) Assembler and/or Higher Level Language (AF accepted or Industrial Standard)		No	Yes	Yes*	Yes		Yes	Yes	No Data
(2) Library or User's Group Support	I	No	No	No	Yes	Y	Yes	Y	No Data
(3) Operating System Editor Capacity		No	No	No	Yes	N	Yes	[illegible]	No Data
Instructions		78	158	27	91		78	7[illegible]	No Data
Bits in a Word	W	8	8	12	16		8	8	No Data
Remarks		*External Sourced Software		*Only has Assembler				Sold by [illegible] Electronics Inc., also	

Legend:
AK All Alert
NG No Good
D Disk
M Magnetic Tape
P Paper Tape

MICROCOMPUTER MANUFACTURERS Listed below, for your convenience are the full names, addresses, and telephone numbers of the manufacturers whose products are summarized in the comparison charts. More data is contained in the complete descriptions of vendors in Binder 2		Intersil, Inc 10900 N Tantau Ave Cupertino, CA 95014 Tel (408) 257-5450	Martin Research, Ltd 3336 Commercial Ave Northbrook, IL 60062 Tel (312) 498-5067	Microcomputer Associates, Inc 2589 Scott Blvd Santa Clara, CA 95050 Tel (408) 247-4440	Microdata Corporation 17481 Red Hill Ave Irvine, CA 92705 Tel (714) 540-6730	Microsoft, Inc 2180 Colorado Ave Santa Monica, CA 90404 Tel (213) 828-8539	Millennium Information Systems 420 Mathew St Santa Clara, CA 95050 Tel (408) 243-6652	MOS 2450 Alamo St Albuquerque, New Mexico 87106 Tel (505) 265-7553	Monolithic Memories, Inc 1165 E Arques Ave Sunnyvale, CA Tel (408) 739-3535
DESCRIPTION OF EQUIPMENT (FIGURE OF MERIT) →	Y	0	0	0	0	162048	0	124461	0
a. Hardware Requirements									
(1) Modular Interchangeability (compatibility of various plug-in units)	B	No	No	Yes	No	No	No	Yes	No
(2) Industrial Standard	N	No	No	No	Yes	No	Yes	Yes	Yes
(3) Single Logistic Source	L	No Data	No	No	No	No	No	No	No Data
(4) Documentation (Schematic and Operating Characteristics)	H	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
(5) Maintenance Support (up to 5 yrs w/o with good service)	K	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
(6) D/A Converter Capability with Accessible Benchmark Criteria of 2 MHz (parallel) or 1 MHz serial output)	N/A								
(7) Efficient Power Capability	P	No Data	No Data	Yes	Yes	No Data	No Data	Yes	No Data
(8) I/O (Input/Output Capability (Minimum examples below are 8 bit oriented)									
(a) Parallel Ports (2 ea) for D/A Converter Unit (8 bit words)	N/A								
(b) Serial Ports (3 ea) for paper tape, keyboard, cassette, etc (audio cassette requires a modem interface) (reduce to 2)	S	2	8	2	2	2	2	2	2
(c) Parallel Port (1 ea) for Front Panel Functions (enters, clears, and reset request) (increase to 4)		4	8	4	4	4	4	4	4
(9) Mass Storage									
(a) Non Volatile Memory (cassette, tape, [ROM chip])	M	No Data	Yes	Yes	Yes	Yes	Yes	Yes	Yes
(b) Off Line (Paper Tape, Disk, or Magnetic Tape)	O	P	No	M	O	DM	None	DM	None
(10) Peripherals (Keyboard, Monitor, Printer)	A	No Data	No	No	No	Yes	No Data	Yes	No Data
b. Software Support	P	No Data	No Data	No Data	No Data	No Data	No Data	No Data	No Data
(1) Availability of the Higher Level Language (AP accepted or Industrial Standard)	I	Some	No	Some	Yes	Yes	No	Yes	Yes
(2) Library of User's Group Source		No	No	Yes	No	Yes	No	Yes	Yes
(3) Operating System's Filter Capacity		No	No	No	No	Yes	No	Yes	Yes
(4) Functions	I	79	78	78	130	150	150	78	150
(5) In a Word	W	12	8	8	16	8	8	8	8

Remarks

Legend: Ok All right
NG No good
D Disk
M Magnetic
P Paper Tape

DESCRIPTION OF EQUIPMENT (FEATURE OR MERIT ITEM)	X	8370	8	8	56640	8	23380	37845	67560
A. Hardware Requirements									
(1) Modular Interchangeability (Can all CPU, I/O, and memory cards be interchanged?)	E	No	No	No	No	No	No	No	No
(2) Integrated Circuits	X	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
(3) Single Supply Voltage	L	No	Yes	Yes	No	No	No	No	No
(4) Power Switch (Automatic switching of backup power)	U	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes
(5) Maintenance Switch (Isolates CPU for use with diagnostics)	E	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes
(6) CPU Diagnostic Capabilities, with recognized benchmark criteria of 2 MHz (parallel in at least output)	N/A								
(7) Keyboard Scan Capability	Y	No (all)	Yes	Yes	Yes	Yes	Yes	Yes	Yes
(8) I/O (Input/Output) Capability, (Minimum requirements below are P list oriented)									
(a) Parallel Ports (2 req. for T/A Computer unit if not on CPU)	N/A								
(1) Serial Port (1 req. for Tape, Text and, Cassette, etc	S	0	2	2	2	2	2	2	0 Data
Audio Cassette Recorder & Video Interface (Point to 4)									
(c) Parallel Port (1 req. for Control of Training Console Panel Function, Meters, Lights, and so on as required) (Increase to 4)	L	0	4	4	4	4	4	4	4
(9) Mass Storage									
(a) Type Available (Floppy, Hard, Bubble, CCD, etc)	M	No Info	Yes	Yes	Yes	Yes	Yes	Ye	Yes
(b) Off-line (Tape, Disk, Mass, or Magnetic Bubble)	O	M	None	None	OM	M	M	M/A	OM
(10) Terminals (Keyboard, Monitor, Printer)	A	Yes	None	Yes	Yes	No Data	Ye	Yes	Yes
B. Software Support	B	SX (3)	No (0)	SX (12)	SX (12)	SX (11)	SX (11)	SX (12)	SX (11)
(1) A compiler and/or high level language (At a lesser or industrial use level)	T	Yes	No	Yes	Yes	Yes	Yes	Ye	Yes
(2) Library of User Stored Source		Yes	No	Yes	Yes	Yes	Yes	Y	Yes
(3) Operating System (Utility Cassette		Yes	No	Yes	Yes	Yes	No	Yes	Yes
Total Points	T	56	70	158	56	45	78	76	78
Merit Number	V	M	M	M	F	IE	F	12	M

Remarks

Legend: SX All of the
N None
Y Yes
M Magnetic Tape
F Floppy Disk

MICROCOMPUTER MANUFACTURERS

Listed below, for your convenience, are data ... additional information are the full names, addresses, and telephone numbers of the manufacturers whose products are summarized in the computer son charts. More data ... about most of these companies can be found in the Directory of Vendors in Chapter ...

		Processor Technology Corp, 6200 Hollis Street, Emeryville, CA 94608, Tel 415 652-8080	Pro-Log Corporation, 2411 Garden Rd, Monterey, CA 93940, Tel (408) 372-4593	Radio Shack, Dept 78-90, 205 N W 7th Street, Fort Worth, TX 76101, Tel (817) 390-3595	Signetics Corporation, 811 East Arques Avenue, Sunnyvale, CA 94086, Tel (408) 739-7700	Southwest Technical Products Corp, 219 West Rhapsody, San Antonio, TX 78284, Tel (512) 344-0241	TEI Incorporated, c/o CMC Marketing Corp, 7231 Fondren Rd, Houston, TX 77036, Tel (713) 774-9526	Texas Instruments Inc, Components Group, P O Box 1443, Houston, TX 77001, Tel (713) 494-5115	Wave Mate, 1015 West 190th Street, Gardena, CA 90248, Tel (213) 329-8941
DESCRIPTION OF EQUIPMENT (FIGURE OF MERIT FOM)	Y	157426	0	192416	0	67878	90145	11529	73015
a Hardware Requirements									
(1) Modular Interchangeability, Compatibility with various plug in units	E	Yes	No	No	No	No	Yes	No	No
(2) Industrial Standard	N	No	Yes	No	Yes	No	Yes	Yes	Yes
(3) Stable Logistic Support	L	No	No Data	Yes	No	No Data	No	No	No
(4) Documentation (Schematics and Operating Characteristics)	D	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
(5) Maintenance Support (Warrantee only with cross engine)	R	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
(6) D/A Converter capability with acceptable benchmark criteria of 2 MHz (parallel input, serial output)	N/A								
(7) Sufficient Power Capability	P	Yes	Yes	Yes	No Data	Yes	Yes	Yes	Yes
(8) I/O (Input/Output) Capability (Minimum examples below are 8 bit oriented)									
(a) Parallel Ports (2 ea) for D/A Converter Unit (8 bit words)	N/A								
(b) Serial Ports (3 ea) for paper tape, keyboard, cassette, etc (audio cassette requires a modem interface) (Reduce to 2)	S	2	2	2	2	2	2	2	2
(c) Parallel Port (1 ea) for control of Training Console Panel functions (meters, lights, and input requests) (Increase to 4)	C	4	4	4	4	4	4	4	4
(9) Mass Storage									
(a) Non Volatile Memory (Read Only, e.g., PROM units)	M	No Data	Yes	Yes	No Data	Yes	No Data	Yes	Yes
(b) Off line (e.g., Tape, Disc, or Magnetic Tape)	O	DPM	None	DM	None	DPM	D	M	D
(10) Peripherals (Keyboard, Monitor, Printer)	A	Yes	No Data	Yes	No Data	Yes	Yes	Yes	Yes
b Software Support	R	OK (21)	NG (3)	OK (26)	NG (12)	OK (18)	NG (1)	NG (9)	OK (17)
(1) Assembler and/or Higher level Language (AF accepted or Industrial Standard)		Yes	No	Yes	Yes	Yes	Yes	Yes	Yes
(2) Library or User's Group Source	T	Yes	No	Yes	Yes	Yes	Yes	No	Yes
(3) Operating System/Editor Capacity		Yes	No	Yes	No Data	Yes	Yes	Yes	Yes
Instructions	I	78	78	158	72	72	158	69	158
Bits in a Word	X	8	8	8	8	8	8	16	8

Remarks:

Legend: (A) All Mfg t
N No Good
D Disk
M Magnetic Tape
P Paper Tape

MICROCOMPUTER MANUFACTURERS Listed below, for your convenience in obtaining additional information, are the names, addresses and telephone numbers of the manufacturers whose products are summarized in the comparison charts. More details about most of these computers can be found in the Directory of Vendors in Volume 2.		Western Digital Corporation 3128 Red Hill Avenue Newport Beach, CA 92663 Tel (714) 557-3550	Wyle Computer Products 2200 Hapwood Boulevard Hawthorn, VA 22066 Tel (804) 838-0122	ZILOG 10460 Bubb Road Cupertino, CA 95014 Tel (408) 446-4666					
DESCRIPTION OF EQUIPMENT (FIGURE OF MERIT-FOM)	Y	0	0	262858					
a Hardware Requirements									
(1) Modular Interchangeability (compatibility with various plug in units)	R	No	No	No					
(2) Industrial Standard	M	No Data	No Data	Yes					
(3) Stable Logistic Support	L	No Data	No Data	No					
(4) Documentation (Schematics and Operating Characteristics)	D	No Data	No Data	Yes					
(5) Maintenance Support (Warranty, Data with assistance)	A	No Data	No Data	Yes					
(6) D/A Converter capability with acceptable benchmark criteria of 2 MHz (parallel input, serial output)	N/A								
(7) Sufficient Power Capability	P	No Data	No Data	Yes					
(8) I/O (Input/Output) Capability (Minimum examples below are 8 bit oriented)									
(a) Parallel Ports (2 ea) for D/A Converter Unit (8 bit words)	N/A								
(b) Serial Ports (3 ea) for paper tape, keyboard, cassette, etc (audio cassette requires a modem interface) (Reduce to 2)	S	0	2	2					
(c) Parallel Port (1 ea) for Control of Training Console Panel Functions (meters, lights, and input requests) (Increase to 4)	C	0	4	4					
(9) Mass Storage									
(a) Non Volatile Memory (resident, i.e., PROM chips)	M	No Data	Yes	Yes					
(b) Off Line (Paper Tape, Disc, or Magnetic Tape)	O	No Data	None	Yes					
(10) Peripherals (Keyboard, Monitor, Printer)	A	No Data	No Data	Yes					
b Software Support	R	As (9)	No (0)	OK (14)					
(1) Assembler and/or Higher-level Language (All accepted or Industrial Standard)	I	No	No	Yes					
(2) Library or User's Source Source		No	No	Yes					
(3) Operating System/Editor Capacity		No	No	Yes					
Instructions	I	No Data	79	158					
Bits in a Word	W	No Data	8	8					

Remarks

Legend OK All Right
NG No Good
D Disk
M Magnetic Tape
P Paper Tape

MICROCOMPUTER MANUFACTURERS

Name, Address and Telephone number	Mfr Fed Code
Advanced Memory Systems 1215 Hammerwood Rd Sunnyvale, CA 94083 Tel (408) 734-4330	
Advanced Micro Devices 901 Thompson Pl Sunnyvale, CA 94086 Tel (408) 732-2400	
American Microsystems, Inc.* 3800 Homestead Rd Santa Clara, CA 95051 Tel (408) 246-0330	31471
Applied Computing Technology 17961 Sky Park Circle Irvine, CA 92707 Tel (714) 557-9972	
Applied Data Communications 1509 E. McFadden Ave Santa Clara, CA 91705 Tel (714) 547-6954	
Applied Systems Corporation* 26401 Harper Ave St Clair Shores, MI 48081 Tel (313) 779-8700	
Auotmated Computer Systems 2361 E. Foothill Blvd Pasadena, CA 91107 Tel (213) 449-0616	
Computer Automation, Inc.* 18651 Von Karman Ave Irvine, CA 92664 Tel (714) 833-8830	53908

Name, Address and Telephone number	Mfr Fed Code
Control Logic, Inc.* 9 Tech Circle Natick, MA 01760 Tel (617) 655-1170	14931
Cramer Electronics, Inc.* 85 Wells Avenue Newton, MA 02159 Tel (617) 969-7700	
CROMECO Incorporated* 1432 Charleston Rd Mountainview, CA 94143 Tel (415) 964-7400	
Data General Corporation Route 9 Southboro, MA 01772 Tel (617) 485-9100	34984
Data Numerics, Inc 141-A Central Avenue Farmingdale, NY 11735 Tel (516) 293-6600	
Data Translation, Inc 23 Strathmore Rd Natrick, MA 01760 Tel	
Digital Electronics Corporation 415 Peterson Street Oakland, CA 94601 Tel (415) 532-2920	
Digital Equipment Corporation* 146 Main St Maynard, MA 01754 Tel (617) 897-5111	15476
Digital Laboratories 377 Ptnam Avenue Cambridge, MA 02139 Tel (617) 876-6220	
Diversified Technology* P.O. Box 465 Ridgeland, MS 39157 Tel (601) 856-4121	

Name, Address and Telephone number	Mfr Fed Code
EBKA Industries Inc 6920 Melrose Lane Oklahoma City, OK 73127 Tel (405) 787-3671	
Educational Data Systems 17891 Sky Park Circle Irvine, CA 92707 Tel (714) 556-4242	
E & L Instruments, Inc* 61 First Street Derby, CT 06418 Tel (203) 735-8774	
Electronic Memories & Magnetics Corp* 12621 Chadron Ave Hawthoren, CA 90250 Tel (213) 556-2323	16224
Electronic Product Associates* 1157 Vega Street San Diego, CA 92110 Tel (714) 276-8911	
Essex International 564 Alpha Dr Pittsburg, PA 15238 Tel (412) 963-9322	
Fabri-Tek, Inc* 5901 South Country Road 18 Minnmeapolis, MN 55436 Tel (612) 935-8811	21542
Fairchild Semiconductor Components 1725 Technology Drive San Jose, CA 95110 Tel (408) 998-0123	
Fairchild Semiconductor 464 Ellis St Mountain View, CA 94042 Tel (415) 962-3816	
General Automation, Inc* 1055 South East Street Araheim, CA 92805 Tel (714) 788-4800	32453

Name, Address and Telephone number	Mfr Fed Code
General Instrument 600 W. John St Hicksville, NY 11802 Tel (516) 733-3130	
GTE Information Systems, Inc 5300 E. LaPalma Anaheim, CA 92807 Tel (714) 524-3131	
Harris Semiconductor P.O. Box 883 Melbourne, FL 32901 Tel (305) 727-5400	
Heurikon Corporation 700 W Badger Road Madison, WI 53713 Tel (608) 155-9075	
Hughes Aircraft Company* Aerospace Group Culver city, CA 90230 Tel (213) 391-0711	
Hughes Solid State Div 2601 Campus Dr Irvine, CA 92715 Tel (714) 752-6396	
IMS Associates* 14800 Wicks Blvd San Leandro, CA 94577 Tel (415) 483-2093	
Intel Corporation* 3065 Bowers Ave Santa Clara, CA 95051 Tel (408) 246-7501	34649
International Microsystems, Inc* 122 Hutton St Gaithersburg, MD 10760 Tel (301) 840-1078	
Intersil, Inc* 10900 N. Tantau Avenue Cupertino, CA 95014 Tel (408) 257-5450	32293

Name, Address and Telephone number	Mfr Fed Code
ITT Semiconductor 74 Commerce Way Woburn, MA 01801 Tel (617) 935-7910	
Martin Research, Ltd* 3336 Commercial Ave Northbrook, IL 60062 Tel (312) 498-5060	
Microcomputer Associates, Inc* 2589 Scott Blvd Santa Clara, CA 95050 Tel (408) 247-8940	
Microdata Corporation* 14781 Red Hill Ave Irvine, CA 92705 Tel (714) 540-6730	52936
Microkit, Inc* 2180 Colorado Ave Santa Monica, CA 90404 Tel (213) 828-8539	
Millennium Information Systems 420 Mathew St Santa Clara, CA 95050 Tel (408) 243-6652	
MITS* 2450 Alamo SE Albuquerque, New Mexico 87106 Tel (505) 265-7553	55844
Monolithic Memories, Inc* 1165 E. Arques Ave Sunnyvale, CA Tel (408) 739-3535	50364
Monolithic Systems Corp 14 Iverness Drive East (Bldg 4-J) Englewood, CO 80110 Tel (303) 770-7400	51513
MOS Technology, Inc* 950 Rittenhouse Rd Norristown, PA 19401 Tel (215) 666-7950	51284

Name, Address and Telephone number	Mfr Fed Code
Mostek Corporation* 1400 Upfield Drive Carrolton, TX 75006 Tel (214) 242-0444	50088
Motorola Semiconductor Products, Inc* P.O. Box 10912 Phoenix, AZ 85036 Tel (602) 244-6900	04713
Multisonics, Inc 3300 Crow Canyon Road Box 350, San Ramon, CA 94583 Tel (415) 837-8111	
MycroTek, Inc 216 North Washington Wicthita, KA 67201 Tel (316) 265-5277	
National Semiconductor Corporation* 2900 Semiconductor Drive Santa Clara, CA 95051 Tel (408) 732-5000	27014
NEC Microcomputers, Inc* 5 Militia Drive Lexington, MA 02173 Tel (617) 862-6410	
Panafacom Ltd P.O. Box 4637 Mountain View, CA 94040 Tel (415) 854-7050	
Panasonic 50 Meadowland Parkway Secaucus, NJ 07094 Tel (201) 348-7276	
PCM, Inc* P.O. Box 215 San Ramon, CA 94583 Tel (415) 837-5400	
Plessey Microsystems 1674 McCaw Ave Irvine, CA 92714 Tel (714) 540-9945	55154

Name, Address and Telephone number	Mfr Fed Code
Process Computer Systems* 5467 Hill 23 Drive Flint, MI 48502 Tel (313) 767-8920	55530
Processor Applications Ltd 2801 E. Valley View Ave West Covina, CA 91792 Tel (213) 965-8865	
Processor Technology Corp* 6200 Hollis Street Emeryville, CA 94608 Tel (415) 652-8080	
Pro-Log Corporation* 2411 Garden Rd Monterey, CA 93940 Tel (408) 372-4593	
Radio Shack* Dept TRS-80 205 N.W. 7trh St Fort Worth, TX 76101 Tel (817) 390-3595	
Raytheon Semiconductor 350 Ellis Street Mountain View, CA 94040 Tel (415) 968-9211	07933
RCA Solid State Division Route 202 Sommerville, NU 08875 Tel (201) 685-6000	18723 26720
Rockwell International P.O. Box 3669 RCOI Dept 720 Anaheim, CA 92803 Tel (714) 632-2321	
Scientific Micro Systems 520 Clyde Avenue Mountain View, CA 94043 Tel (415) 964-5700	
Signetics Corporation* 811 East Arques Avenue Sunnyvale, CA 94086 Tel (408) 739-7700	18324

Name, Address and Telephone number	Mfr Fed Code
Solid State Scientific Montgomeryville Industrial Park Montgomeryville, PA 18936 Tel (215) 855-8400	
Southwest Technical Products Corp* 219 West Rhapsody San Antonio, TX 78284 Tel (512) 344-0241	
Sphere Corporation 791 S. 500 West Bountiful, UT 84010 Tel (801) 292-8466	
Syneitek 3030 Coronado Dr Santa Clara, CA 95051 Tel (408) 241-4800	
System Integration Associates RD 1, Box 126 Glenmore, PA 19343 Tel (215) 286-5136	
TEI Incorporated % CMC Marketing Corp 7231 Fondren Rd Houston, TX 77036 Tel (713) 774-9526	
Teledyne Systems Company 19601 Nordhoff Street Northridge, CA 91324 Tel (213) 886-2211	17863
Tektronix, Inc* P.O. Box 500 Beaverton, OR 97077 Tel	
Texas Instruments Inc* Components Group, PO Box 1443 Houston, TX 77001 Tel (713) 494-5115	01295
Three Phoenix Company 10632 North 21st Avenue Phoenix, AZ 85029 Tel (602) 944-2221	

Name, Address and Telephone number	Mfr Fed Code
Transitron Electronic Corporation Microcomputer Division 168 Albion Street Wakefield, MA 01880 Tel (617) 245-4500	24046
Warner & Swasey Company 30300 Solon Industrial Parkway Solon, OH 44139 Tel (216) 368-6200	63800
Wave Mate* 1015 West 190th Street Gardena, CA 90248 Tel (213) 329-8941	
Western Digital Corporation* 3128 Red Hill Avenue Newport Beach, CA 92663 Tel (714) 557-3550	52840
Wintex Computer Corporation 544 Lunt Avenue Schaumberg, IL 60172 Tel (312) 529-3080	
Wyle Computer Products* 3200 Magruder Boulevard Hampton, VA 23666 Tel (804) 838-0122	
ZILOG* 10460 Bubb Road Cupertino, CA 95014 Tel (408) 446-4666	

*Data received and evaluated

APPENDIX E

FIGURE OF MERIT PROGRAM

```
1 DIM A(5Ø)
5 CLS
1Ø PRINT 'YOU CAN: REPAIR, START A NEW LIST, OR ADD TO AN OLD ONE"
11 INPUT "REPAIR = 2, START NEW = Ø, READ AND ADD = 1"; Q
14 IFQ = Ø THEN 5Ø
15 IF Q = 2 THEN 1ØØ
16 IF Q = 1 THEN GOSUB 1ØØØ: GOTO 5Ø
5Ø FOR U = 1 TO 1ØØ
8Ø INPUT "THE COMPANY NAME?"; A$
9Ø PRINT #-1, A$
1ØØ INPUT "# INST': I
1Ø5 INPUT "TYPE BUS (S1ØØ=1Ø. . . OTHER = 5)";B
11Ø INPUT "KIT (YES=5. . . NO=1Ø)"; K
115 INPUT "INDUSTRIAL, LOGISTIC, DOCUMENT (1Ø=Y, 5=N, Ø=?) "; N, L, D
12Ø INPUT "POWER (1Ø=ENOUGH. . .-1Ø=NOT ENOUGH. . Ø=?)"; P
125 INPUT "# BITS IN A WORD"; W
13Ø INPUT "#OF PARALLEL PORTS"; C
135 INPUT "#OF SERIAL I/O PORTS"; S
14Ø INPUT "NON-VOL MEM.? (Y =1Ø, N =3, ?=Ø)"; M
145 PRINT "SOFTWARE SUPPORT"
15Ø PRINT "MACHINE ONLY = Ø              NON-STD HI-LEVEL = Ø
155 PRINT "ASSEMBLER (ABS)=1             COMPILER=5"
16Ø PRINT "RELOC. ASSEMBLER = 3          CROSS ASSEMBLER = 2"
165 PRINT "HI-LEVEL INTERP=3             CROSS COMPILER = 4"
17Ø PRINT "EDITOR = 3                    OPERATING SYS = 3"
175 INPUT "ENTER # OF SOFTWARE SUPPORTS AVAILABLE"; X
18Ø FOR Z=1 TO X: INPUT "VALUE OF SOFTWARE": A(Z): NEXT Z
```

```
184 INPUT "PERIFERALS - - MONITOR"; A" IF A=Ø THEN 19Ø
185 INPUT "PERIFERALS - - KEYBOARD"; A: IF A=Ø THEN 19Ø
186 INPUT "PERIFERALS - - TELEPRINTER"; A
19Ø INPUT "OFF LINE MEM (ADD VALUES) - PAPER T =1, MAG T =3, DISC =5,
NONE =Ø"; O
2ØØ INPUT "DOES THIS COMPANY HAVE ANY SOFTWARE, OR DOES ANYONE?",T
205 R=0
31Ø FOR Z=1 TO X: R=R+A(X): NEXT Z
32Ø GOSUB 7ØØØ
33Ø GOSUB 2ØØØ
4ØØ PRINT #-1, I;",";B;",";K;",";N;",";L;",";D;",";P;",";W
41Ø PRINT #-1, C;",";S;",";M;",";R;","A;A",";O;",";T
43Ø RETURN
1ØØØ INPUT "READ HOW MANY FILES BEFORE YOU ENTER DATA?"; F
1ØØ1 FOR E=1 TO F
1ØØ2 REM
1ØØ3INPUT #-1, A$: INPUT #-1,I,B,K,N,L,D,P,W
1ØØ4 INPUT #-1,C,S,M,R,A,O,T
1ØØ5 GOSUB 7ØØØ
1ØØ6 GOSUB 2ØØØ
1Ø4Ø NEXT E
1Ø5Ø RETURN
2ØØØ GOSUB 5ØØØ: REM THIS GETS THE ALGORITHM
2ØØ2 G = G + 1: A(G) = Y
2ØØ3 PRINT "THE NAME OF THE COMPANY IS"; A$
2ØØ6 PRINT "INSTR", "BUS", "IND. USE", "LOGISTICS": PRINT I, B, N, L
```

```
2ØØ7 PRINT "DOCUMENTS", "POWER O.K.", "BITS/WD", "PARALLEL PTS": PRI
NT  D, P, W, C
2ØØ8 PRINT "SERIAL PTS", "NON-VOL MEM", "SOFTWARE #", "PERIFERALS":
PRINT S, M, R, A
2ØØ9 PRINT "OFF-LINE MEM", "SFTWRE AT ALL", "DECISION VALUE": PRINT
O, T, Y
2Ø1Ø IF A(Ø) = 999 THEN RETURN
2Ø2Ø PRINT: PRINT: PRINT: INPUT "ANOTHER COMPANY??, YES = 1, NO = 2
ALL = 999";A(Ø)
2Ø25 IF A(Ø) = 999 THEN RETURN
2Ø3Ø IF A(Ø) - 1 THEN RETURN
2Ø4Ø END
5ØØØ Y=(I*B+K+N+L+D+P+W+C+S+M)*R*A*O*T
6ØØØ RETURN
7ØØØ REM THIS PUTS IT IN COPY FORMAT
7ØØ5 CLS:PRINT A$;"'S HARDWARE"
7Ø2Ø PRINT "COMPATABLE", "IND STD", "SCHEMATICS", "MAINTAINABLE"
7Ø3Ø IF (I=72) + (I=78) + (I=158)THEN PRINT "YES" : GOTO 7Ø5Ø
7Ø4Ø PRINT "NO"
7Ø5Ø Z=N; GOSUB 1ØØØØ
7Ø6Ø Z=D: GOSUB 1ØØØØ
7Ø7Ø Z=L: IF D + L>14 THEN Z = 1Ø
7Ø75 GOSUB 1ØØØØ
7Ø85 PRINT
7Ø9Ø PRINT "POWER", "I/O PORTS OK?", "PARALLEL", "SERIAL"
8ØØØ Z=P: GOSUB 1ØØØØ
8Ø1Ø Z=2*(S+C): GOSUB 1ØØØØ
```

```
8Ø2Ø Z=C*5: GOSUB 1ØØØØ
8Ø3Ø Z=S*3: GOSUB 1ØØØØ
8Ø35 PRINT
8Ø4Ø PRINT "STRG OK?", "NON-VOL", "OFF LINE", "PERIPHERALS"
8Ø5Ø Z=1Ø*(M/M)*(A/A): GOSUB 1ØØØ
8Ø6Ø Z=M: GOSUB 1ØØØØ
8Ø69 Z=O+1
8Ø7Ø RESTORE: FOR U=1 TO Z: READ B$: NEXT U: PRINT B$
8Ø71 DATA "NONE", "P. TAPE", " ", "M. TAPE, "P & M TAPE, "DISK",
"DISK & P. TAPE"
8Ø72 DATA " ", "DISK & M TAPE", "DISK, P & M TAPE"
8Ø8Ø Z=A*1Ø: GOSUB 1ØØØØ
8Ø85 PRINT
8Ø9Ø PRINT A$;"'S SOFTWARE"
81ØØ IF (R*T)(17PRINT"INSUFFICIENT SOFTWARE SUPPORT": GOTO 8145
811Ø PRINT "SOFTWARE SUFFICIENT:"
8115 PRINT "ASSEMBLER, EDITOR, INTERPERTER, DISK O/S, STD HI-LEVEL
LANG"
812Ø PRINT "ALL STANDARD.!!!!!!!"
814Ø IF A(Ø)<>999 THEN 815Ø
8145 FOR U=1 "PRESS ENTER TO GET NUMERIC VALUE";B$
815Ø INPUT "PRESS ENTER TO GET NUMERIC VALUES";B$
816Ø CLS:RETURN
1ØØØØ IF Z <Ø THEN Z=Ø
1ØØ1Ø ON (INT(Z/5)+1) GOTO 1Ø1ØØ, 1Ø2ØØ, 1Ø3ØØ
1Ø1ØØ PRINT "NO DATA", :RETURN
1Ø2ØØ PRINT "NO",:RETURN
1Ø3ØØ PRINT "YES",:RETURN
```

APPENDIX F

APPLICATION PROGRAM BITE

```
*
      BLOCK DATA KEEPER
     LOGICAL*1  LNBIT(8),  LBUF(32), IPUT(91)
      DIMENSION IODAT(100), IPICT(450), LIST(27)
      COMMON/POOL/LASTP, ISW, INIT, LIST, LNBIT, LBUF, IODAT, IPICT,
     *IPRG, IGOA, IGOB, IGOC, IPUT, I, II, III, IV, IIII, IX, IPRT, LUBIT
      DATA LNBIT/Z'01', Z'02', Z'04', Z'08', Z'10', Z'20', Z'40', Z'80'/,
     * IPRG/Z'FFF3'/, IGOA/Z'FFF0'/, IGOB/Z'FFF1'/, IGOC/Z'FFF2'/,
     * IPRT/2/,
     A IPICT/4, 2400, 1, 5804, 15827, 25840, 17400,
     B 10, 2400, 1, 5209, 5209, 5209,
     * 5209, 15855, 25290, 25290, 25290, 25290, 17400,
     C 4, 2400, 1, 6609, 15855, 26690, 15800,
     D 18, 2400, 1,
     * 5209, 5209, 5209, 5209, 5209, 5209, 5209, 5209,
     * 15855, 25290, 25290, 25290, 25290, 25290,
     * 25290, 25290, 25290, 15800,
     E 26, 246, 1, 11600, 10155, 10100,
     * 10155, 10155, 10155, 10100, 10155, 10155, 10155, 10155, 10155,
     * 10155, 10155, 10155, 10100, 10155, 10155, 11555,
     * 10100, 12555, 10100, 13655, 20190, 15200, 13600,
     F 25, 246, 1, 12000, 13655, 10100, 12555, 10100, 11555,
     * 10155, 10155, 10100, 10155, 10155, 10155, 10155, 10155, 10155, 10155,
     * 10155, 10100, 10155, 10155, 10155, 10100, 10155, 15200, 13100,
     G 7, 256, 1, 13200, 11800, 10355 12455, 15155, 12800, 15200,
     H 7, 256, 1, 11700, 15200, 15155, 12455, 10355, 11800, 14400,
```

```
I 3,128.1,0.0.
J 14,128.1.10122.10216,10122.10128.10122.10116.
* 10122,10128,10122,10128,10122,10128,11528.15200.
P 11,32,1.10219.10209,10203,10109.10103.10155,10101.
* 10211.10319,10111.11419.
L 2.4,1,10203.10255.
M 2,4,1.10255.10203.
N 3,32.1.11500,10155.11600.
O 2,60.1,12000.13000.
P 84.3458.1.
* 10163.14600,04009.11055,15155.15200.
* 10163.14600,04309.10755,15155.15200.
* 10163,14600,05109,15155,15200.
* 10163.14600.04607.01479,14055.15200.
* 10163.14600.04606.02469,13055.15200.
* 10163.14600,04605,03759.11755,15200,
* 10163.14600.05207,15200,
* 10163.14600,05204.15200.
* 10163.14600.04007.1104. .15143.15200.
* 10163.14600.10600.02404.11013.15113.15200.
* 10163.14600.11100.02903.11022,15122.15200.
* 10163.14600.11900.02102.11013,15113,15200.
* 10163.14600,12600,01401.11007,15107,15200.
* 10163.14600,13200,10800.11007.15103.15200.
```

```
Q 84.3458.1,
* 10163,15200,15155,11055.24090.14600,
* 10163,15200.15155,10755.24290.14600,
* 10163,15200,15155,25190.14600,
* 10163,15200,14055,21492,24620,14600,
* 10163,15200,13055.22496.24660,14600,
* 1016_.15200.11755,23795.24650.14600,
* 10163.15200,25270.14600,
* 10163,15200,25240.14600,
* 10163.15200,1514_,11043.24070,14600,
* 10163.15200.1513_.11023.25440,10600.14600,
* 10163.15200.15122,11022,24930,11100.14600,
* 10163.15200.1511_.11013.22120.11900.14600,
* 10163.15200.15107,11007.21410.12600.14600,
* 10163.15200.15103.1100..10800.13200.14600,
R 6,246.1.11600,0_009,13055,15155.15200,12000,
S 6.246.1,11600,15155.13055.23090,15200,12000,
T 2,16,1,10855.10855,
U 2,16,1,10800,10855,
V 2,8,1,10400.10455,
W 2,8.1,10428,10428,
X 2,4.1.10228.10229,
Y 2,4,1,10229.10228,
Z 18,26_.1.15000,00109.20190.00109.25090.00109,20190,
* 00109.20190.15000,00109,20190.00109,15052,20190,
```

```
ØØ109.20190,15000/
      DATA IODAT/255,0,0,0,0,1,17128,1,61/
      END
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      SUBROUTINE ERROR(MESUP,ICLST)
      LOGICAL KBIT
      LOGICAL*1 ICLST(14)
      DIMENSION MESUP(101)
    LOGICAL*1  LNBIT(8),  LBUF(32),IPUT(91)
      DIMENSION IODAT(100),IPICT(450),LIST(27)
      COMMON/POOL/LASTP,ISW,INIT,LIST,LNBIT,LBUF,IODAT,IPICT,
     *IPRG,IGOA,IGOB,IGOC,IPUT,I,II,III,IV,IIII,IX,IPRT,LUBIT
      DATA KINIT/1/,MPICT/0/,  ICWAS/0/,IWAS/0/,KOOL/0/
      ASSIGN 1234 TO NO
       ISW=0
C
      KINIT=INIT
C
1     JZ=MESUP(1)
      DO 2 KIX=2,JZ,10
       IVZ=MESUP(KIX)
       IIIZ=MESUP(KIX+1)
       IZ=MESUP(KIX+2)
       LUBIZ=MESUP(KIX+3)
       IXZ=MESUP(KIX+4)
```

```
*
          IIZ=MESUP(KIX+5)
          IIIIZ=MESUP(KIX+6)
         IF(IVZ.NE.IV.AND.IVZ.NE.0)GO TO 2
         IF(IIIZ.NE.III.AND.IIIZ.NE.0)GO TO 2
         IF(IZ.NE.I.AND.IZ.NE.0)GO TO 2
         IF(LUBIZ.NE.LUBIT.AND.LUBIZ.NE.0)GO TO 2
         IF(IXZ.NE.IX.AND.IXZ.NE.0)GO TO 2
         IF(IIZ.NE.II.AND.IIZ.NE.0)GO TO 2
         IF(IIIIZ.NE.IIII.AND.IIIIZ.NE.0)GO TO 2
C
         IF(IVZ+IIIZ+IXZ+LUBIZ+IZ+IIZ+IIIIZ.EQ.0)GO TO 2
C
         ISOLN=MESUP(KIX+8)
         MBIT=MESUP(KIX+9)
         MPICT=MESUP(KIX+7)
         KINIT=LIST(MPICT)
         GO TO 1000
2        CONTINUE
C
C
1000     IIS=1
         IF(LBUF(29).AND.LNBIT(5))IIS=0
         ICIS=0-IIS
         DO 99 K=17,30
          IF(LBUF(K).XOR.ICLST(K-16))GO TO 98
```

```
*
          GO TO 99
98       ICIS=ICIS+1
          IF(LBUF(ISOLN).AND.LNBIT(MBIT))GO TO 991
          GO TO 99
991        DO 22 KIX=2,JZ,10
            IF(ISOLN.EQ.MESUP(KIX+8).AND.MBIT.EQ.MESUP(KIX+9))GO TO 221
            GO TO 22
221         LIX=KIX+9
             DO 222 JIX=KIX,LIX
222          MESUP(JIX)=0
22         CONTINUE
99       CONTINUE
C
         IF(ICWAS.NE.ICIS.AND IIS.EQ.0)GO TO NO
         IF(ICIS.EQ.ICWAS)GO TO 80
          KOOL=KOOL+ICIS
         IF(KOOL.GT.1)GO TO NO
C
80       ICWAS=ICIS
         IWAS=IIS
          IF(ICIS)1401,1401,801
801       KINIT=LIST(15)
         GO TO 1401
1234     KINIT=LIST(26)
         GO TO 1402
```

```
*
1401    IF(KINIT.EQ.INIT)GO TO 10000
C
        IF(MPICT.GT.49)GO TO 1500
        GO TO 1402
1402    L=IPICT(KINIT)+3
        DO 99998 ID=1,L
        IP=KINIT+ID-1
99998   IODAT(ID)=IPICT(IP)
        GO TO 9999
1500    ISW=56-MPICT
9999    LASTP=KINIT
10000   RETURN
        END
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
        SUBROUTINE PICTUR
        INTEGER*1 INTWD,ISTIK
        LOGICAL*1 LWD,MIKE,IKE,KWD    .
       LOGICAL*1  LNBIT(8),  LBUF(32),IPUT(91)
        DIMENSION IODAT(100),IPICT(450),LIST(27)
        COMMON/POOL/LASTP,ISW,INIT,LIST,LNBIT,LBUF,IODAT,IPICT,
     *IPRG,IGOA,IGOB,IGOC,IPUT,I,II,III,IV,IIII,IX,IPRT,LUBIT
                EQUIVALENCE (LWD,INTWD),(KWD,ISTIK)
        DATA NPORT/Z'007C'/,IPORT/Z'00FC'/,P5/.05/
        IA2=IODAT(2)
C
```

```
*
C
C       GET COUNT OF PULSES TO BE LOADED
C
        MSB2=IA2/64
        IB2=MSB2*64
        LSB2=IA2-IB2
CSPLIT COUNT INTO TWO 6 BIT PARTS MOST AND LEAST SIG BITS
C
C
        INTWD=MSB2
        MIKE=LWD
        INTWD=LSB2
        IKE=LWD
C16 TO 8 BIT WORDS
C
C
        MIKE=MIKE.OR.LNBIT(8).OR.LNBIT(7)
        IKE=IKE.OR.LNBIT(7)
CTHAT PUTS THE CONTROLS IN
C
C
        CALL OUT(NPORT,MIKE)
        CALL OUT(NPORT,IKE)
        IA2=IODAT(1)+3
        MSB2=IODAT(2)
```

```
      *
      C
            DO 1 ID=4,IA2
            K=IODAT(ID)
                  IF(K.EQ.0)GO TO 99999
                  N=K/10000
                  L=K-N*10000
                  M=L/100
                  L=L-M*100
                  LL=L
                  K=L/10
                  L=L-K*10
                  IF(M.GT.50)M=50*(M-50)
      C   A FIVE DIGIT POSITIVE INTEGER NUMBER ( <=32767) DECODES THUS:
      C N////  -> A'/',/-/,OR'\' LINE WITH 0,1,OR 2 VALUE
      C /MM//  -> A LINE OF LENGTH 0 TO 50 OR A LINE LENGTH 50, TIMES THE
      C              DIFFERENCE OF 50 TO 100
      C ,'//KL  -> A LINE FROM FROM ONE OF NINE EQUALLY INCREMENTED LEVELS (K)
      C           TO ANOTHER SUCH LEVEL (L) DERIVED FROM THE SPACE REMAINING
      C           ABOVE (OR BELOW) THE START LEVEL
                  ZK=K
                  ZK=ZK+6.3+P5
                  ZL=L
            IF(N-1)101,104,103
      101         ZL=(ABS(56.7-ZK)/9.)+ZL+P5+ZK
                  GO TO 102
```

```
*
102             ZL=ZK-((ZK/9.)*(9-ZL)+P5)
102             ZM=M
                IF(M.EQ.0)ZM=1.
                Z=ABS(ZK-ZL)/ZM
                        ISTIK=IABS(ISW)
104             DO 55 J=1,M
                 ZJ=J
C
C
          IF(N.EQ.0)INTWD=ZK+Z*ZJ+P5
          IF(N.EQ.1)INTWD=LL
          IF(N.EQ.2)INTWD=ZK-Z*ZJ-P5
C
C
                  MIKE=KWD
                 IF(ISW)5500,5533,5522
5500             MIKE=MIKE.AND..NOT.(LNBIT(ISTIK))
                 GO TO 5533
5522             MIKE=MIKE.OR.LNBIT(ISTIK)
5533              MIKE=.NOT.(LNBIT(7).OR.MIKE)
                  CALL OUT(NPORT,MIKE)
55               CONTINUE
1       CONTINUE
        WRITE(5,69)MIKE,ISW
69      FORMAT(1X,'MIKE=',I8,/,'ISW=',I8,/)
```

```
*
C       SWITCH FOR ONE VERSES TWO MHZ OPERATION
C
        IF(INIT.GT.LIST(4))GO TO 6
        CALL OUT(IPORT,0)
        RETURN

C THIS IS THE RANDOM NOISE GENERATOR
99999   ISEED=12345
        DO 5 ID=1,MSB2
        ISEED=ISEED*31623
        RAN=ABS(ISEED*(1./(2.**15-1.)))
        RAN=RAN*31.5+2.
        IID=RAN
        IF(MOD(IID,2).EQ.0)GO TO 5
C                DIG NOISE NEEDS A "SQUARED LOOK"
C
        INTWD=IID
        IKE=LWD
        IKE=.NOT.(LNBIT(7).OR.IKE)
5       CALL OUT(NPORT,IKE)
6       CALL OUT(NPORT,0)
        RETURN
        END
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
       PROGRAM TPSPGM
```

```
*
        LOGICAL*1 JBITS,IPANL(9),NAME(11),NUMB(10),ICLST(14)
        DIMENSION MESUP(101)
      LOGICAL*1  LNBIT(8),LBUF(32),IPUT(91)
        DIMENSION IODAT(100),IPICT(450),LIST(27)
        COMMON/POOL/LASTP,ISW,INIT,LIST,LNBIT,LBUF,IODAT,IPICT,
     *IPRG,IGOA,IGOB,IGOC,IPUT,I,II,III,IV,IIII,IX,IPRT,LUBIT
        DATA IPANL/64,7,6,128,1,0,128,3,2/,JBITS/Z'3F'/,
     *NAME/'E','R','R','O','R','S',' ',' ','D','A','T'/,
     *NUMB/'0','1','2','3','4','5','6','7','8','9'/
C
C*INITIALIZE THE BITE I/O FACEPLATE WITH PORTS A,B,AND C OUTPUT ONLY.*
C
        CALL POKE(IPRG,128)
C
        CALL POKE(IGOA,0)
          DO 4 ID=2,16,2
             K=ID+1
                CALL POKE(IPRG,K)
                CALL POKE(IPRG,ID)
4         CONTINUE
                CALL POKE(IPRG,9)
                CALL POKE(IPRG,11)
        DO 5 ID=1,9,3
                CALL POKE(IGOA,IPANL(ID))
                CALL POKE(IPRG,IPANL(ID+1))
```

```
*
5               CALL POKE(IPRG,IPANL(ID+2))
C
C*GET ERROR FOR STUDENT TO FIX*
C
        CALL INOUT
        IF(LBUF(5).AND.LNBIT(8))IPRT=1
        IF(LBUF(5).AND.LNBIT(7))CALL POKE(21871,197)
        LBUF(1)=LBUF(3).AND.JBITS
        L=LBUF(1)
          IF(L.EQ.0)GO TO 101
        KL=L/10
        JL=L-KL*10
        NAME(7)=NUMB(KL+1)
        NAME(8)=NUMB(JL+1)
        CALL OPEN(6,NAME,0)
        READ(6,2323)(MESUP(ID),ID=1,91)
2323    FORMAT(9(10I5,1X,/),1I5)
        DO 7 ID=1,101
7       MESUP(ID)=MESUP(ID)/10
        ENDFILE 6
C
        DO 6 ID=1,14
6       ICLST(ID)=LBUF(ID+16)
C
        WRITE(5,1232)(MESUP(ID),ID=1,91)
```

```
*
1232    FORMAT(1X,11I5,/,9(1X,10I5,3X,/))
101     DO 10 ID=1,100
10      IODAT(ID)=0
        ID=0
        ISW=0
        DO 20 K=1,450
        IF(IPICT(K).NE.1)GO TO 20
        ID=ID+1
        LIST(ID)=K-2
20      CONTINUE
        DO 2 ID=1,12
        LBUF(ID)= FALSE.
2       IPUT(ID)= FALSE
C
C****THIS IS WHERE THE FACE PLATE AND CARD SWITCHES ARE READ ****
C
100     CONTINUE
C
          DO 3 IJK=1,12
          IPUT(IJK)=LBUF(IJK)
3         CONTINUE
        CALL INOUT
C
C  ---THE SWITCHES ARE NOW READ--
C
```

```
*
C
C****THIS IS WHERE THE FACE PLATE AND CARD SWITCHES ARE ANALYZED.****
        LOOK=0
C
      DO 1 ID=1,32
      IF(LBUF(ID) .XOR.  IPUT(ID))LOOK=1
    1 CONTINUE
        IF(LOOK.EQ.0)GO TO 100
        CALL DECIDE
        IF(L.NE.0)CALL ERROR(MESUP,ICLST)
        IF(LASTP.EQ.INIT)GO TO 100
        CALL PICTUR
        IF(LASTP.EQ.LIST(26))GO TO 9999
        LASTP=INIT
C
C START AGAIN AND LOOK AT THE FACE PLATE AND SWITCHES
        GO TO 100
C
9999  STOP
      END
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
        SUBROUTINE INOUT
        INTEGER*1 INTWD,NBIT(8)
        LOGICAL*1 LWD
        LOGICAL LLWD
```

```
*
                DIMENSION IB1(2), IB2(2)
       LOGICAL*1  LNBIT(8),  LBUF(32), IPUT(91)
         DIMENSION IODAT(100), IPICT(450), LIST(27)
         COMMON/POOL/LASTP, ISW, INIT, LIST, LNBIT, LBUF, IODAT, IPICT,
      *IPRG, IGOA, IGOB, IGOC, IPUT, I, II, III, IV, IIII, IX, IPRT, LUBIT
                DATA IB1/10, 8/, IB2/11, 9/
C
C
C
                J=0
           DO 400 ID=1, 2
                DO 401 IK=1, 16
                J=J+1
                K=IK-1
                K1=K
                  IF(ID. EQ.  1)K1=K*16
                CALL POKE(IGOB, K1)
                CALL POKE(IPRG, IB1(ID))
                LBUF(J)=PEEK(IGOC)
                CALL POKE(IPRG, IB2(ID))
401             CUNTINUE
400        CONTINUE
           GO TO (500, 501), IPRT
500        DO 5 ID=1, 32
           LWD=LBUF(ID)
```

```
*
      IF(LWD .EQ. IPUT(ID))GO TO 5
      I2=LWD
        DO 4 IY=1,8
            NBIT(IY)=0
            IF(LWD .AND. LNBIT(IY))NBIT(IY)=1
4       CONTINUE
      WRITE(5,1233)(LNBIT(IXX),IXX=1,8)
      WRITE(5,1232)(NBIT(IY),IY=1,8),LWD,ID
1233  FORMAT(/,1X,8I7)
1232  FORMAT(1X,10I7)
5     CONTINUE
501   RETURN
      END
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      SUBROUTINE DECIDE
      INTEGER*1 LEN
      LOGICAL*1 LTEST,MTEST,LENTH,LENT
     LOGICAL*1  LNBIT(8), LBUF(32),IPUT(91)
      DIMENSION IODAT(100),IPICT(450),LIST(27)
      DIMENSION MTIPS(4)
      COMMON /POOL/LASTP,ISW,INIT,LIST,LNBIT,LBUF,IODAT,IPICT,
     +IPPG,IGOA,IGOB,IGOC,IPUT,I,II,III,IV,IIII,IX,IPRT,LUBIT
      EQU.VALENCE (LEN,LENT)
     DATA LENTH/'F'/
     ASSIGN 9999 TO IFLAT
```

```
*
      ASSIGN 4500 TO IAD
      ASSIGN 99999 TO LESGO
C
C
C
C            /* TURN ON THE BITE TESTER */
C//*S1*//
      IF(LBUF(4) .AND. LNBIT(8))GO TO 3700
                        CALL CLEAR
                              GO TO IFLAT
C
C
C
C//*S37*//        /*USES POSNS 9&10...LBUF(9) HOLDS POSNS 1-8 OF S37*/
3700  IF(LBUF(9))GO TO IFLAT
C/*POSNS 1 THRU 8 OF SW37 ARE INVALID*/
C
C
C                   /*ELSE GO TO S37 POSN 9 OR 10*/
C/*FIND OUT POSN OF SW45*/
        LTEST=LBUF(15)
        DO 451 IV=1,7
        IF(LTEST.AND.LNBIT(IV))GO TO 452
451     CONTINUE
        IV=0
```

```
452     IV=IV+1
C
C
C
      LTEST=LBUF(7)
            DO 460 III=4,6
460         IF(LTEST.AND.LNBIT(III))GO TO 461
      III=3
461   III=III-2
C
C       /(S46) PATTERN SETS III/
      MTEST=LBUF(8)
            DO 3800 II=1,7
3800              IF(MTEST.AND.LNBIT(II))GO TO 4100
            II=II+1
C
C       (S38) CHANNEL SEL SET=II
C
C
C
C       MTI/SCH(S41) NEED TO SET DP AND CHR ' SEL
C       (S41) SETS ALL MTI/SCH FUNCTIONS
4100  LTEST=LBUF(12)
            DO 4141 I=3,8
4141        IF(LTEST.AND.LNBIT(I))GO TO 4142
```

```
*
      I=2
4142  I=I-1
C
C
C
        MTEST=.FALSE.
        LTEST=MTEST
        IF(LBUF(31).AND.LNBIT(5))MTEST=.TRUE.
        IF(LBUF(32).AND.LNBIT(5))LTEST=.TRUE.
        DO 41022 IIII=1,4
C
C
C
41022   MTIPS(IIII)=0
        IF(LBUF(2).AND.LNBIT(1))MTIPS(1)=2
        DO 41020 IIIX=1,3
        IIII=9-IIIX
41020   IF(LBUF(1).AND.LNBIT(IIII))MTIPS(IIIX+1)=IIIX+2
C
C
        IF(IV.NE.3.OR.IV.NE.4)CALL CLEAR
        GO TO(9999,9999,4630,4640,45000,45000,4500,4500),IV
45000   CONTINUE
C/*53709-3710*//  /*MUST NOT BE IN MTI/SEARCH FOR A/D MEMORY*/
      IF(LBUF(2).AND.LNBIT(4))GO TO IAD
```

```
C                    /*ELSE DO MTI/SEARCH(S3710)-BELOW-*/
C
      GO TO (4101,4102,4103,4104,4150,4150,4150),I
C/*MTI DECODER*/
4101  GO TO(9999,4651,4651,4651,4651,4651,4651,4651,9999),II
C
C
C/*THE II AND III 'GO TO'S' CAN BE EXTENDED TO SHOW ERRORS*/
4651  GO TO(1080,1090,1080,1100),III
C
C
C/* MTI PEAK SELECT*/
C
C       CHAN SEL MUST= PROCESSOR CHAN OTHERS NOT REQ
C
4102    CONTINUE
        DO 41023 IIII=1,4
41023   IF(MTIPS(IIII) EQ. II)GO TO 41024
        GO TO IFLAT
41024 GO TO (1080,1090,1080,1100),III
C
C
C/*THRESHOLD*/*MTI*/* MTI? OR INTEGRATORS?*/
4104  KLEN=0
        IF(IV.EQ 6)GO TO 4505
```

```
*
        IF(IV.NE.5)GO TO IFLAT
        DO 46540 IIII=1,4
        IF(MTIPS(IIII).NE.0)GO TO 4654
46540   CONTINUE
        GO TO IFLAT
4654  GO TO(9999,9999,9999,1130),III
C
C
C/*INTEGRATOR(MTI(THRESHOLD OR INTEGRATOR))*/
C/*INTEGRATOR*/
4103  IF(MTEST)GO TO(1150,9999,1160,9999),III
      GO TO(1170,9999,1180,9999),III
C
C
C/*MTI/THRESHOLD*/*INTEGRATOR*/
4505  IF(MTEST)GO TO(1040,9999,1050,9999),III
      GO TO(1060,9999,1070,9999),III
C
C
C*/MTI INTEGRATOR*/
C------------------
C/*SEARCH BEGINS HERE*/
4150    IF(IV.NE.6)GO TO IFLAT
C
C
```

```
C
        DO 41500 IIII=1,5
        IF(LBUF(1).AND.LNBIT(IIII))GO TO 41501
41500   CONTINUE
        GO TO IFLAT
41501 J=I-6
        LENT=LBUF(3).AND.LENTH
        IF(KLEN.NE.LEN)LASTP=0
        KLEN=LEN
        KLEN=1+KLEN*.25
        KLEN=KLEN*100
        IF(J)4155,4156,4157
C
C/*SEARCH INTEGRATOR*/
4155  GO TO (9999,4655,4655,4655,4655,4655,4655,9999),II
4655  IF(LTEST)GO TO(1150,9999,1160,9999),III
      GO TO (1170,9999,1180,9999),III
C
C/*SEARCH THRESHOLD*/
4156  GO TO (9999,4656,4656,4656,4656,4656,4656,9999),II
4656    IF(LTEST)GO TO(1040,9999,1050,9999),III
      GO TO (1060,9999,1070,9999),III
C
C/*SEARCH PEAK SELECT*/
4157    GO TO(9999,4657,4657,4657,4657,4657,4657,9999),II
4657    IF(LTEST)GO TO(1040,9999,1050,9999),III
```

```
      GO TO(1060,9999,1070,9999),III
C          /*THIS ENDS MT1/SEARCH*/
C
C     /*THIS BEGINS A/D MEMORY*/
C
C
4500  CALL ADMEM
      GO TO LESGO
C
4600  CONTINUE
4640  CALL HGT
      GO TO LESGO
C
1040  INIT=LIST(5)
      GO TO LESGO
1050  INIT=LIST(6)
      GO TO LESGO
1060  INIT=LIST(7)
      GO TO LESGO
1070  INIT=LIST(8)
      GO TO LESGO
1080  INIT=LIST(9)
      GO TO LESGO
1090  INIT=LIST(10)
      GO TO LESGO
```

```
1100    INIT=LIST(11)
        GO TO LESGO
1130    INIT=LIST(14)
        GO TO LESGO
9999    CONTINUE
1140    INIT=LIST(15)
        GO TO LESGO
1150    INIT=LIST(16)
        GO TO LESGO
1160    INIT=LIST(17)
        GO TO LESGO
1170    INIT=LIST(18)
        GO TO LESGO
1180    INIT=LIST(19)
C
99999 IF(LASTP.EQ.INIT)RETURN
      L=IPICT(INIT)+3
      DO 99998 ID=1,L
      IP=INIT+ID-1
99998 IODAT(ID)=IPICT(IP)
        IF(INIT.GT.LIST(8).OR.INIT.LT.LIST(5))GO TO 1111
        K1=KLEN/100.+1.05
        IF(INIT.NE.LIST(5))GO TO 1051
          DO 1042 N=1,K1
1042      IODAT(N+4)=10100
```

```
*
        GO TO 1111
1051    IF(INIT.NE.LIST(6))GO TO 1061
          DO 1052 N=1,K1
          NN=27-N
1052       IODAT(NN)=10100
        GO TO 1111
1061    IF(INIT.NE.LIST(7))GO TO 1071
        IODAT(5)=IODAT(5)-KLEN
        IODAT(6)=IODAT(6)+KLEN
        GO TO 1111
1071    IODAT(8)=IODAT(8)+KLEN
        IODAT(9)=IODAT(9)-KLEN
1111    RETURN
        END
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
        SUBROUTINE ADMEM
        LOGICAL*1 LTEST,MTEST,LENTH,LENT
      LOGICAL*1  LNBIT(8), LBUF(32),IPUT(91)
        DIMENSION IODAT(100),IPICT(450),LIST(27)
        COMMON/POOL/LASTP,ISW,INIT,LIST,LNBIT,LBUF,IODAT,IPICT,
     *IPRG,IGOA,IGOB,IGOC,IPUT,I,II,III,IV,IIII,IX,IPRT,LUBIT
        ASSIGN 1111 TO LESGO
        ASSIGN 9999 TO IFLAT
        IF(LBUF(2) AND.LNBIT(4))GO TO 400
        GO TO 9999
```

```
*
400     LTEST=LBUF(11)
        DO 430 IX=1,8
        IF(LTEST.AND.LNBIT(IX))GO TO 431
430     CONTINUE
        IX=IX+1
431     LUBIT=1
        IF(LBUF(8) AND.LNBIT(8))LUBIT=2
C
        GO TO(9999,9999,9999,9999,9999,9999,4507,4508),IV
4507    GO TO(9999,9999,9999,4304,4305,4306,9999,4307,4308),IX
4508    GO TO(4301,4302,4302,9999,9999,9999,9999,9999,9999),IX
C/*HEIGHT A-D*/
4301    GO TO(1030,1020),LUBIT
C/*SEARCH A-D*/
4302    GO TO(9999,4352,4352,4352,4252,4352,4352,9999),II
4352    GO TO(1010,1000),LUBIT
C/*MTI A-D*/
4303    GO TO(9999,4353,4353,4353,4353,4353,4353,9999),II
4353    GO TO(1030,1020),LUBIT
C/*     MEMORIES   */
C/*HEIGHT EVAL MEM*/
4304    GO TO(9999,1190,1200,1210),III
C/*CANC #1 AND 2 */
4305    CONTINUE
4306    GO TO(9999,4345,4345,4345,4345,4345,4345,9999),II
```

```
*
4345    GO TO(4355,4365),LUBIT
4355    GO TO(9999,1190,1110,1120),III
4365    GO TO(1220,1220,1230,1240),III
C/*SEARCH INT MEM*/
4307    GO TO(9999,4357,4357,4357,4357,4357,4357,9999),II
4357    GO TO(9999,1190,1110,1120),III
C/*MTI  INT MEM*/
4308    GO TO(9999,1190,1110,1120),III
C
C
CTHIS ENDS A-D/MEMORY
C
C
1000    INIT=LIST(1)
        GO TO LESGO
1010    INIT=LIST(2)
        GO TO LESGO
1020    INIT=LIST(3)
        GO TO LESGO
1030    INIT=LIST(4)
        GO TO LESGO
1110    INIT=LIST(12)
        GO TO LESGO
1120    INIT=LIST(13)
        GO TO LESGO
```

```
*
9999    CONTINUE
1140    INIT=LIST(15)
        GO TO LESGO
1190    INIT=LIST(20)
        GO TO LESGO
1200    INIT=LIST(21)
        GO TO LESGO
1210    INIT=LIST(22)
        GO TO LESGO
1220    INIT=LIST(23)
        GO TO LESGO
1230    INIT=LIST(24)
        GO TO LESGO
1240    INIT=LIST(25)
1111    RETURN
        END
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
        SUBROUTINE CLEAR
        DATA I/Z'FFF0'/,J/Z'FFF3'/
        CALL POKE(I,0)
        CALL POKE(J,5)
        CALL POKE(J,4)
        RETURN
        END
```

```
      SUBROUTINE HGT
      LOGICAL*1 LTEST
     LOGICAL*1  LNBIT(8), LBUF(32), IPUT(91)
      DIMENSION IODAT(100), IPICT(450), LIST(27)
      LOGICAL*1 IPATN(4), JPATN(4), KPATN(4), LPATN(4)
      COMMON /POOL/ LASTP, ISW, INIT, LIST, LNBIT, LBUF, IODAT, IPICT,
     *IPRG, IGOA, IGOB, IGOC, IPUT, I, II, III, IV, IIII, IX, IPRT, LUBIT
      DATA IPATN/Z'6E', Z'56', Z'29', Z'95'/,
     *     JPATN/Z'31', Z'76', Z'5C', Z'25'/,
     *     KPATN/Z'22', Z'5E', Z'4B', Z'E1'/,
     *     LPATN/Z'1A', Z'44', Z'35', Z'A6'/
      IF(IV.EQ.3)GO TO 1000
      CALL POKE(IGOA, IPATN(III))
      GO TO 9999
C
1000  IF(LBUF(16).AND.LNBIT(8))GO TO 167
      IF(LBUF(15).AND.LNBIT(8))GO TO 157
      CALL POKE(IGOA, KPATN(III))
      GO TO 9999
C
167   CALL POKE(IGOA, LPATN(III))
      GO TO 9999
C
157   CALL POKE(IGOA, JPATN(III))
C
9999  CALL POKE(IPRG, 5)
      CALL POKE(IPRG, 4)
      INIT=LIST(15)
      RETURN
      END
```

```
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
      SUBROUTINE PICTUR
      INTEGER*1INTWD,ISTIK
      LOGICAL*1 LWD,MIKE,KWD,IKE
     LOGICAL*1  LNBIT(9), LBUF(32),IPUT(91)
      DIMENSION IODAT(100),IPICT(470),LIST(30)
      COMMON/POOL/LASTP,ISW,INIT,LIST,LNBIT,LBUF,IODAT,IPICT,
     *IPRG,IGOA,IGOB,IGOC,IPUT,I,II,III,IV,IIII,IX,IPRT,LUBIT
            EQUIVALENCE (LWD,INTWD),(KWD,ISTIK)
      DATA NPORT/Z'007C'/,IPORT/Z'00FC'/,P5/.05/
      DATA IFLIP/-1/

      IA2=IODAT(2)
      IFLP0=0
C
C     GET COUNT OF PULSES TO BE LOADED
C
      MSB2=IA2/64
      IB2=MSB2*64
      LSB2=IA2-IB2
CSPLIT COUNT INTO TWO 6 BIT PARTS MOST AND LEAST SIG BITS
C
C
      INTWD=MSB2
      MIKE=LWD
      INTWD=LSB2
      IKE=LWD
```

```
C16 TO 8 BIT WORDS
C
C
        MIKE=MIKE.OR.LNBIT(8).OR.LNBIT(7)
        IKE=IKE.OR.LNBIT(7)
CTHAT PUTS THE CONTROLS IN
C
C
        CALL OUT(NPORT,MIKE)
        CALL OUT(NPORT,IKE)
        IA2=IODAT(1)+3
        MSB2=IODAT(2)
C
        DO 1 ID=4,IA2
        K=IODAT(ID)
                IFLG=K
                K=IABS(K)

                N=K/10000.

                L=K-N*10000
                M=L/100
                L=L-M*100
                LL=L

                IF(IFLG)7,99999,8
7               ICK=IFLP**IFLP0
```

```
C       SWITCH FOR ONE VERSES TWO MHZ OPERATION
C
        IF(INIT.GT.LIST(4))GO TO 6
        CALL OUT(IPORT,0)
        RETURN

CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
C THIS IS THE RANDOM NOISE GENERATOR
99999   ISEED=12345

        DO 5 ID=1,MSB2

        ISEED=ISEED*31623
        RAN=ABS(ISEED*(1./2.**15-1.))
        RAN=RAN*31.5+2.

        IID=RAN
        IF(MOD(IID,2).EQ.0)GO TO 5
C               DIG NOISE NEEDS A "SQUARED LOOK"
C
        INTWD=IID

        IKE=LWD
        IKE=.NOT.(LNBIT(7).OR IKE)
5       CALL OUT(NPORT,IKE)
6       CALL OUT(NPORT,0)

        RETURN

        END

CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC
```

```
      IF(ICK.GE.0) GO TO 70
      IFLP0=1

      M=MM*100+M
      ZM=M

      ZL=LL
      IFLP0 2


      GO TO  10./1
70    MM=M
      ZK=LL
      GO TU 1
8     CONTINUE
      K=L/10
      L=L-K*10
      IF(M.GT 50)M=50*(M-50)
      ZK=K
      ZK=ZK*6 3+P5

      ZL=L
      IF(N-1)101 104,103
101   ZL=(ABS(56 7-ZK)/9 )*ZL+P5+ZL
      GO TO 102
10    ZL=ZL-((ZK/9. )*(9-ZL)+P5)
```

```
102             ZM=M
                IF(M.EQ.0)ZM=1.
1021            CONTINUE
                Z=ABS(ZK-ZL)/ZM
                      ISTIK=IABS(ISW)
104             DO 55 J=1,M
                 ZJ=J
C
C
          IF(N.EQ.0)INTWD=ZK+Z*ZJ+PS
          IF(N.EQ.1)INTWD=LL
          IF(N.EQ.2)INTWD=ZK-Z*ZJ-PS
C
C
                  MIKE=KWD
                IF(ISW)5500,5533,5522
5500             MIKE=MIKE.AND. NOT (LNBIT(ISTIK))
                 GO TO 5533
5522             MIKE=MIKE.OR.LNBIT(ISTIK)
5533              MIKE=.NOT.(LNBIT(7).OR.MIKE)
                  CALL OUT(NPORT,MIKE)
55              CONTINUE
1       CONTINUE
```

APPENDIX G

STUDENT ERROR FILE PROGRAM

```
B
        PROGRAM ERRS 20
        DIMENSION IPUT(91)
        LOGICAL*1 NAME(9)
        DATA NAME/'E','R','R','S','2','0','D','A','T'/
        DATA IPUT/41,7,1,0,0,8,3,0,61,24,5,
     +            7,2,0,0,8,3,0,61,24,5,
     +            7,3,0,0,8,3,0,61,24,5,
     +            7,4,0,0,8,3,0,61,24,5,50*0/
C
        CALL OPEN(6,NAME,0)
1       FORMAT(9(10I5,1X,/),1I5)
        WRITE(6,1)(IPUT(I),I=1,91)
        ENDFILE 6
        STOP
        END
CCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCCC

B TYPE ERRORS20.DAT
   41    7    1    0    0    8    3    0   61   24
    5    7    2    0    0    8    3    0   61   24
    5    7    3    0    0    8    3    0   61   24
    5    7    4    0    0    8    3    0   61   24
    5    0    0    0    0    0    0    0    0    0
    0    0    0    0    0    0    0    0    0    0
    0    0    0    0    0    0    0    0    0    0
    0    0    0    0    0    0    0    0    0    0
    0    0    0    0    0    0    0    0    0    0
    0
```

APPENDIX H

PICTURE CODE GENERATOR

```
1220  LET W1=INT((63*W1)/5+.05)
1230  LET L2=L/100
1240  LET L3=INT(L2+.05)*100
1250  LET L2=(L-L3)*100
1260  LET C1=(Z+L3+W9)*-1
1270  LET C2=(Z+L2+W1)*-1
1280  LET L0=L0+1
1290  LET I[L0]=C1
1300  LET L0=L0+1
1310  LET I[L0]=C2
1330  RETURN
1340  REM*******************RANDOM NOISE*******************
1350  LET L0=L0+1
1360  LET I[L0]=0
1370  LET L0=L0+1
1380  LET I[L0]=0
1400  RETURN
1410  REM*************REGULAR AND RANDOM NOISE MIXTURE*******
1420  PRINT "DO THE REST OF THE PICTURE WITH RANDOM NOISE LAST"
1430  PRINT "THEN USE MENU 4"
1440  RETURN
1450  REM***********NICE PRIN' ROUTINE**********
1460  LET M=L0
1470    FOR J=1 TO M
1480    PRINT I[J];
1482    NEXT J
1484  PRINT "IS THAT SATISFACTORY? (YES-NO)"
1490  INPUT B$
1500  IF B$="YES" RETURN
1510  LET L0=T3
1520  PRINT "TRY AGAIN"
1530  LET S=S+L5
9035  RETURN
9036  GOSUB 1460
9040  STOP
9999  END
```