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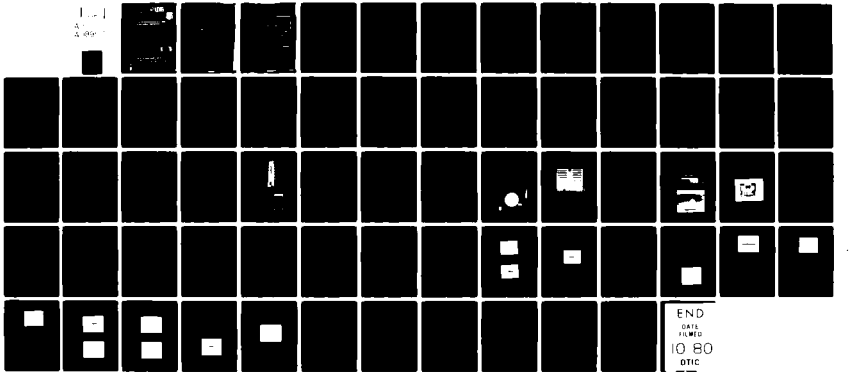

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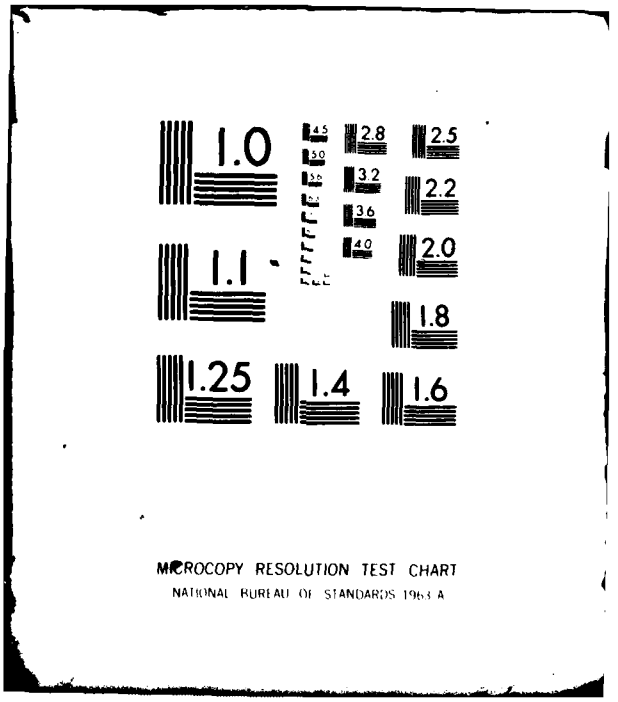
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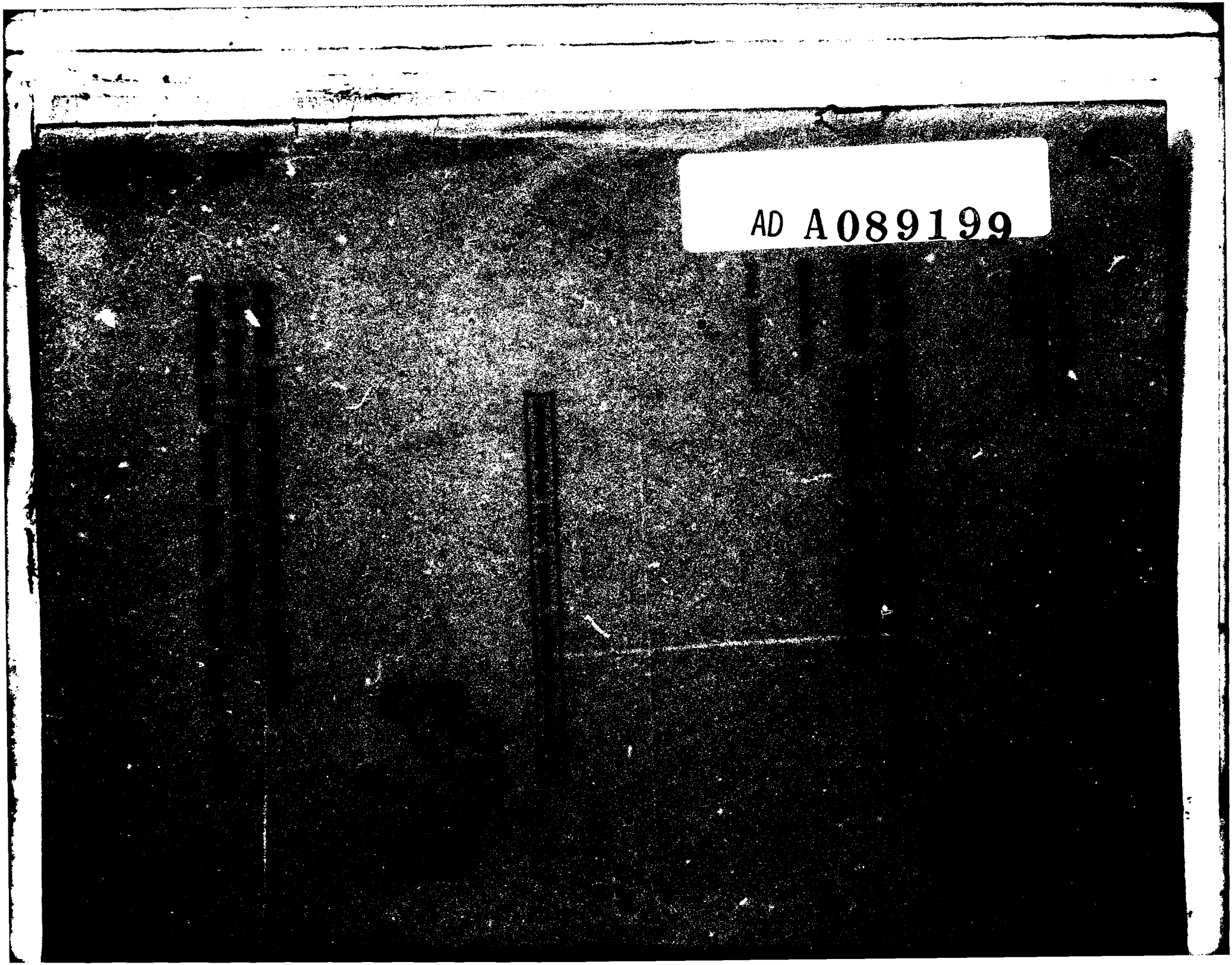
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A monolithic surface wave programmable matched filter signal processor operating at 100 MHz was designed, fabricated and evaluated. The semiconductor and acoustic elements were developed on (001) n-type silicon oriented for acoustic transmission along the [100] direction. Surface acoustic waves at 100 MHz were generated by a zinc oxide film layer transducer into an array of 31 silicon-gate NMOS piezoresistive FET taps spaced at 10 ns intervals. The drain lines of all taps were connected

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to serve as the rf output. The phase and amplitude of each tap was controlled by a digital shift register and analog voltage to the tap gates. The die size for a single 31-bit filter was 0.980 inch by 0.120 inch.

The general performance characteristics of the device were as follows: The conversion loss of the 8.5 finger pair zinc oxide film layer transducers was 15 dB. The 3 dB bandwidth was 9.5 MHz. The piezoresistive tap coupling efficiency was in the 35 to 40 dB region under normal operating conditions. The overall device efficieny in developing a spread waveform from a short (100 ns) rf input pulse was 75 dB which included losses due to acoustic reflections, matching and parasitics. The direct coupled signal level could be brought to 90 dB below the input signal level and the signal to noise ratio of the spread pulse was greater than 20 dB. The analog voltage to the device gates was effective in controlling tap amplitude over a 20 dB range and the digital shift register provided for random bi-phase coding of the taps, within a 3 μs time period.

A single matched filter device was used to correlate 31-bit bi-phase coded sequences on a continuous encoding basis. The peak-to-sidelobe ratio was 6:1 or 15 dB. Alternating coded sequences were correlated within an acoustic transit time (3.1 μs). The correlated peak was greater than 30 dB above the noise level of the test system. The arbitrary phase and amplitude control permitted optimization of the correlated pulse under conditions of signal distortion.

This development represented a significant step toward the realization of a compact, low cost highly versatile matched filter device for signal processing applications in communications equipment. Specific problem areas were solved. A quantitative assessment of various aspects of ZnO/Si-MOSFET technology was made and the viability of the monolithic integration of SAW and semiconductor circuitry on silicon was demonstrated.

PREFACE

This report was prepared by the Government Electronics Division of Motorola Inc. under Air Force Contract F30602-78-C-0209. The work was administered by the Rome Air Development Center, Griffiss AFB, New York. Henry J. Bush was the technical program monitor for RADC.

Technical work on the program began 22 September 1978 and was completed 22 January 1980. The project was a cooperative effort involving various groups and facilities at the Government Electronics Division (GED) and Semiconductor Group (SG) of Motorola Inc. Fred Hickernell of the Integrated Circuit Facility (ICF) of GED was the project leader. DeWitt Ong of the Motorola Integrated Circuits Applications Research Laboratory (MICARL) coordinated the SG efforts. Major device design and layout work was done by Ron DeLong of GED. Mask generation, material growth and wafer preparation, wafer processing and testing was the responsibility of SG. Transducer design and fabrication, logic and rf system design and fabrication, packaging and final rf testing was the responsibility of GED. Dean Goodnight (GED) was the Program Manager.

The following individuals made significant technical contributions to the program: Bob Barcon (SG), wafer fabrication; Don Mungai and Scott Anderson, device layout and digitization; Ron Hayman, Jennifer Brown and Ellie Mason (MICARL), mask check and fabrication interface; Ken Pindur (SG), mask fabrication; De Witt Ong (MICARL), process development and coordination; Ed Barron (MICARL), wafer processing; Dan Higgins and Jerry Janes (MICARL), wafer electrical evaluation; Fred Hickernell (GED), ZnO transducer fabrication; Jim Hinsdale (GED), test circuitry; Dave Leeson (GED), test circuit fabrication; Lee Maciejewski (GED), device packaging; Mike Adamo and Fred Hickernell, rf test and device analysis; and Dave Leeson and Randy Caputo (GED), assembly and rf test.

The final report was prepared by Fred Hickernell.

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EVALUATION

This report presents the results of the latest attempt to integrate SAW signal processing, digital control and silicon LSI fabrication into an arbitrarily programmable tapped delay line monolithic structure. This effort has been highly successful, having overcome the major problem areas of the previous two efforts and demonstrating a realizable, low cost and powerful communications signal processing technique.

The device represents a single, monolithic, massproducible tapped structure for correlating binary, phase coded RF signals where both the code and amplitude response of the tapped line may be reprogrammed on a burst-to-burst basis. The dynamic range is sufficient, the amplitude variation range (20 dB) is within the range of a majority of fade depths of interest, and the speed of reprogramming an amplitude taper across the line is more than sufficient to accommodate the rate of channel variations for line-of-sight communications. In fact, the speed of the on-chip digital control logic to totally reprogram the device (code and amplitude) within the acoustic transient time has large implication. Thus, while the device itself has a small time-bandwidth product (31), it can be used, in conjunction with a recirculating delay line (coherent integrator), to correlate extremely long binary codes without having to resort to parallel correlator channels.

The ability to operate on the analog signal, compatible with digital control and implemented as a single chip LSI device holds promise for ECCM applications at low cost.

HENRY J. BUSH
Project Engineer

SECTION I

INTRODUCTION

1. MONOLITHIC PROGRAMMABLE MATCHED FILTER CONCEPT

There is an increasing need for acoustic components to be used in microwave communications and radar systems which acquire and process large amounts of signal data. These acoustic components require a wide bandwidth capability, a long storage or delay time, and a built-in filter or coding function. A substantial number of current requirements for signal processing systems can be met using tapped surface acoustic wave devices. Such devices can simplify processing circuitry and represent a reliable, low cost alternative to present electronic techniques.

Surface wave devices are being used to perform matched filter functions in communications and radar systems where it is desirable to unambiguously transmit data in the presence of noise and/or jamming signals. There have been three levels of development. First there are fixed code devices, where a series of phased interdigital metallic electrodes are implemented on a piezoelectric substrate and packaged as a discrete component. Electronic switching and logic functions in lumped circuit and hybrid form have been incorporated with the fixed coded devices to develop a second level of surface wave encoders and decoders which are programmable. While integrated circuits can be used in such hybrid configurations, the separate manufacture and interconnection of acoustic and electronic devices creates cost inefficiencies and reliability problems due to circuit complexity. Because the development trend in signal processing subsystems is toward a higher degree of component integration in a miniaturized form factor and ultimately requires production in substantial quantities, monolithic building blocks combining the acoustic encoding and decoding functions with electronic functions such as switching, mixing and amplification on a single substrate should lead to considerable cost savings, improved reliability and size reduction. It is this third level of development, the monolithic programmable matched filter device, which will provide the greatest opportunities and challenges for the future.

Silicon provides an excellent base material for the development of a monolithic programmable matched filter. Rayleigh waves can be efficiently generated on its surface using piezoelectric film layer transducers. MOSFETs provide a convenient means for broadband detection of the surface waves through the piezoresistive effect. The output signal level can be controlled through gate voltage bias. The piezoresistive tap can be addressed through control circuitry for arbitrary phase selection and amplitude level. Silicon also provides the basis for the integration of other semiconductor circuit elements.

A conceptual representation of the three main functional parts of a silicon based monolithic programmable device is shown in Figure 1. The various acoustic and electronic functions are developed on a properly oriented and doped silicon substrate using semiconductor process compatible-fabrication techniques.

At each end of the device is a film layer transducer composed of a thin aluminum interdigital electrode structure with an overlay of piezoelectrically active sputtered zinc oxide. The transducers are the electrical inputs for rf pulses in the encoding mode and the rf bi-phase sequences in the decoding mode.

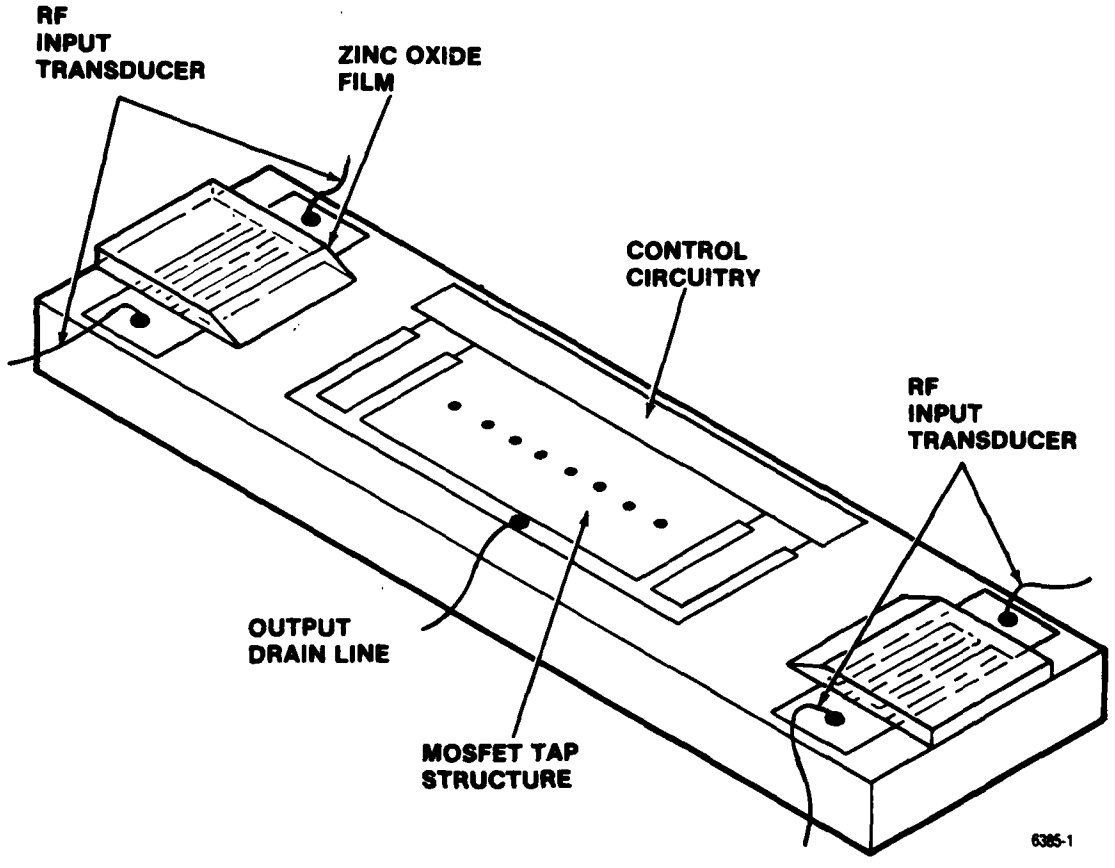


Figure 1. Monolithic ZnO/Si-MOSFET Programmable Surface Acoustic Wave Matched Filter

Between the two transducers are the MOSFET device taps which serve as the piezoresistive detectors of the surface acoustic wave energy generated by the transducers. These MOSFET cells are placed in geometric arrangements corresponding to the desired phase coding. Binary and quadraphase coding can be easily implemented. The device output is taken from the parallel connected drain lines of the MOSFET device taps.

The third major feature is the semiconductor circuitry controlling the phase and amplitude of the MOSFET detector taps. The information in this control circuitry may be statically or dynamically programmed. It codes and weights the taps according to the desired signal processing function.

There have been three developments to date under Air Force contract based on the concepts just described. The first was a 31-bit bi-phase matched filter with a 6 X 31 ROM stored code address to the

piezoresistive taps.[1-3] In the second development shift register and bucket brigade circuitry were added to control tap phase and amplitude.[4-7] The most recent development, described in this report, addressed the limitations uncovered in the previous programs. In order to realize the advantages of this potentially low-cost matched filter technology it was necessary on the third device development to make improvements in the following areas: 1) reduce the reflections of surface wave energy at the MOSFET detector taps due to the high profile of metal and oxide step regions, 2) improve the tap phase and amplitude control circuitry so that it could be microprocessor interfaced and would lead to overall programming speeds consistent with acoustic wave transit times and 3) improve the transducer quality and MOSFET tap detector efficiency. The main thrust of the third development was to produce a signal correlator which would be attractive to the systems engineer for use in spread spectrum communications

2. PROGRAM OBJECTIVES, SCOPE AND TASKS

2.1 OBJECTIVE

The objective of the program was to continue the development of the programmable matched filter signal processor technique based upon surface acoustic wave ZnO/Si-MOSFET technology. In particular, the effort was to increase the operational performance of the signal processing technique started under F30602-76-C-0134 through refinement of certain aspects of the technology.

2.2 SCOPE

The main interest of the effort was to derive a realistically producible matched filter signal processing technique which provided tap amplitude weighting of a programmable phase coded surface wave multiple tap delay line. The technique was to be derived by refinements in the design and processing employed in the previous effort, F30602-76-C-0134. The scope of the effort was limited to matched filter functions. The rf bi-phase coded sequence generation required for demonstrating the performance of the matched filter was to be provided by either a digital or surface wave source. It was necessary for the demonstration that the total monolithic circuit be fabricated.

2.3 TASKS/TECHNICAL REQUIREMENTS

The task/technical requirements as given in the works statement were the following:

The contractor shall provide engineering services, materials, and facilities to design, fabricate and demonstrate a bread- board model of a programmable, matched filter, signal processor module. The main signal processing element of the module shall be a monolithic (silicon substrate) surface acoustic wave (SAW) matched filter whose taps can be both phase and amplitude weighted. The monolithic SAW matched filter shall be designed and fabricated utilizing the technology developed under Contract F30602-76-C-0134.

1. The monolithic SAW matched filter shall be fabricated with tap phase and amplitude programmability. A silicon substrate shall be utilized for the surface wave tapped delay line and tap phase control logic/circuits, as a minimum.

2. A zinc oxide/aluminum interdigital composite input transducer shall be utilized.

3. Metal oxide-semiconductor field effect transistors (MOSFETs) shall be utilized for the surface wave detector array.

4. Tap phase coding shall be achieved by on-substrate shift register circuitry rather than an on-substrate library.

5. Tap amplitude control mechanism shall be determined.

The following performance goals were established for the breadboard model:

Frequency	100 MHz
Bandwidth	10 MHz
Number of Taps	31
Tap Spacing	100 ns
Burst Length	3.1 μ s
Reprogramming Speed	3 μ s
Tap Phase Modulation	Binary
Phase Control	Arbitrary
Amplitude Control Range	20 dB
Tap Amplitude Uniformity	±1 dB
Correlation Peak/Sidelobe	16 dB
MOSFET Tap Efficiency	35 dB
Transducer Efficiency	15 dB
Direct RF Feedthrough	-90 dB

To meet the performance goals of the module and continuing from the accomplishments of F30602-76-C-0134, the following aspects of the monolithic SAW matched filter shall be analyzed as a minimum during the design process:

Transducer — methods for improving the quality of the thick ZnO film configuration to achieve coupling factors in excess of 1%.

MOSFET Tap Function — methods for reducing the reflections of surface acoustic wave energy at each tap due to metal and oxide step regions.

Device Efficiency — methods for reducing the overall power drain per coded bit at maximum efficiency.

Tap Phase Control Circuitry — methods for improving off-on ratios in the shift register circuitry.

Tap Amplitude Control Circuitry — methods, including off-substrate parallel inputs, which will lead to an overall device reprogramming speed commensurate with the acoustic transit time through the tap structure.

Silicon Substrate/Processing — continued use of (001) p-type silicon with SAW propagation along the [100] direction and detection with NMOS FET cells.

Based upon the design aspects noted, a breadboard programmable, matched filter, signal processor module shall be fabricated. The contractor shall demonstrate/evaluate operation of the breadboard module fabricated. The demonstration/evaluation of the breadboard shall be made against each of the performance goals listed. The contractor shall breadboard all circuits necessary for performing the demonstration/evaluation.

For purposes of the demonstration/evaluation, the following procedures are acceptable: Common clocking and bias sources may be used; a common pseudo-random code generator may be used to modulate the input signal and program the filter taps if suitable.

3. PROGRAM SUMMARY

Figure 2 shows the basic features of the programmable correlator fabricated under contract F30602-78-C-0209. The device architecture is developed on (001) silicon with propagation of the surface waves along the [100] direction. The coded rf signal is converted to the surface acoustic wave mode by the zinc oxide film layer transducer on the glassivated surface of the silicon at the end of the structure. The zinc oxide film is sputter deposited on the interdigital electrode pattern to a thickness of approximately five-hundredths of an acoustic wavelength. A floating aluminum electrode is deposited on the zinc oxide over the interdigital region and a high conductivity diffused region in the silicon underlies the structure. The fingerwidths and spacings are calculated to generate a signal frequency of 100 MHz on the composite SiO_2/Si layer.

The series of 31 N-channel silicon gate MOSFET detectors taps in line with the transducer are spaced at 10 wavelength intervals. Each tap has a common central drain line with channel detector regions on each side spaced at one-half wavelength, approximately 24 microns. The width of the detector taps is 42 mils and the channel length is 8 microns. A low profile silicon gate CMOS process was used with thin aluminum metallization so that changes in elevation along the acoustic path were kept to approximately 8000 Å. Quarter wavelength

discontinuities were avoided and step regions tapered where possible. The source metallization contact lines were broadened to carry the current load. To arrive at the final dimensions of the gate length to be used in the detection process, factors such as detection efficiency and geometric constraints were taken into consideration.

The design philosophy for the on-chip circuitry controlling the taps was governed by the requirement for the rapid change of bi-phased codes within an acoustic transit time (3.1 μ s) and the ease of analog voltage control for individual taps. The analog voltage control was designed as 31 parallel inputs which could be addressed by a serial to parallel off-chip processor. The 31 bi-phase taps were addressed in groups of 4 by eight parallel phase data input points to the shift register. The clock driver circuits were integrated on the device. Once the phase data was clocked in it was stored in a second register for a parallel dump to the taps when required. With the 31 bits of phase information stored in the second register, the next code could be clocked into the first register without disturbing the stored code. Such an arrangement was designed to permit the continuous correlation of codes using a single device.

The devices were processed on a 3-inch diameter 20 mil thick wafer which could accommodate up to forty of the 980 mil by 120 mil die. Silicon gate CMOS technology was chosen for semiconductor device implementation because it offers high speed, low power dissipation and good chip density. Because SiGCMOS is a self aligning process it is not performance limited by parasitic gate overlap capacitance such as metal gate MOS processes are. The SiGCMOS process permitted the side-by-side channel detector regions with a common drain and development of a low surface profile. The processing of the semiconductor devices was standard with the exception of the thinner aluminum contact metal. Semiconductor processing was carried to the glass passivation step prior to transducer fabrication.

The aluminum interdigital electrodes were photolithographically patterned on the passivation glass and a 1.8 micron zinc oxide film sputtered on the electrodes through an aluminum aperture mask. The aperture mask shielded the MOSFET areas and was offset from the wafer by a few mils to develop a tapered region between the ZnO film and the glass passivation. A metal plane of aluminum was then photoreplicated on the zinc oxide. The final process step was cutting through the oxides to expose the aluminum contact pads.

Processed wafers were visually and electrically evaluated in order to select suitable devices for packaging. A commercially available 1.5 inch by 0.75 inch all metal flat pack (Isotronics 1605) was chosen to house the transversal filter chip and the ceramic thick film metallized substrates used for interconnecting the device to the package leads. The interconnections between the device, metallized ceramic and package leads were made with 1 mil aluminum wire ultrasonically bonded. There were a total of 52 leads interfacing with the device, five rf and the remaining 47 associated with the digital circuitry.

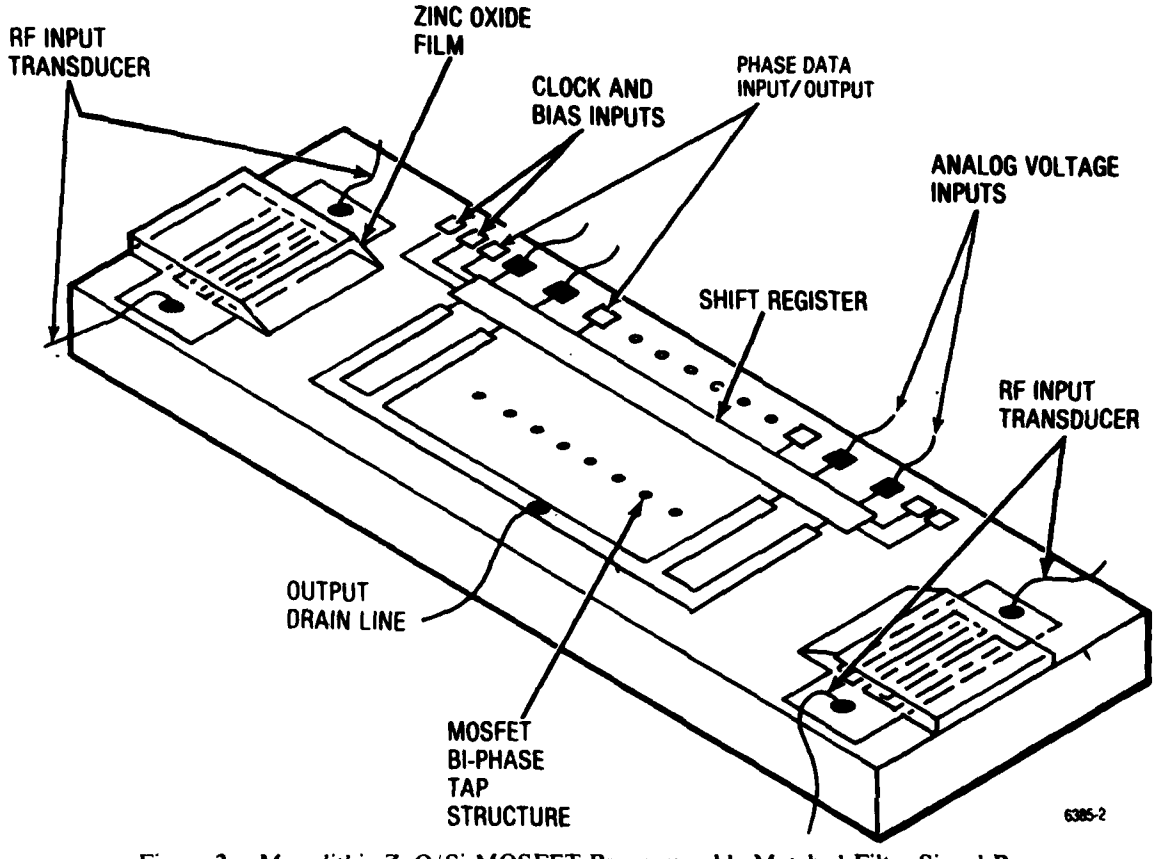


Figure 2. Monolithic ZnO/Si-MOSFET Programmable Matched Filter Signal Processor.

A brass test fixture with OSM and pin connectors was used to house the packaged device and matching circuit elements during rf testing. It was coupled to a digitally controlled test box which generated the coded sequences. Special care was taken to maintain good ground conditions and electrical isolation of the dc and rf lines to prevent any direct feed-through signals.

RF pulse testing was used to determine transducer and tap conversion efficiencies, the propagation loss through the array, the characteristics of the phase and amplitude of the output waveform and the signal feed-through level. A 100ns pulse of rf at 100 MHz was used in the measurements. The transducer loss was 15dB including bidirectionality, with a 3 dB bandwidth of 9.5 MHz. The acoustic propagation loss through the 31 element tap array as determined by reflection measurements was 3 dB. The conversion efficiency for a single MOSFET tap was in the 35 to 40 dB range for a tap current of approximately 30 mA. The direct signal feed-through level was 85 to 90 dB below the signal input. The amplitude decay across 31 equally biased taps was measured between 2 and 3 dB confirming the reflection measurements. There was good amplitude uniformity between switched phase states.

The digitally controlled test box was fabricated for evaluating the correlation properties of the device.

Two 31 bit codes could be developed by manually setting two-way switches on the box. The digital logic circuitry was timed to clock in the code sequences and generated the 100 MHz bi-phased codes. The box could be set to generate either code within the acoustic transit time.

The correlated waveform using a 31-bit maximal length code was 225 nanoseconds to the null points with a peak-to-sidelobe of approximately 6:1 or 15 dB. The device was capable of correlating continuous 31 chip coded inputs as demonstrated by alternating between two different codes. The correlated peak was 30 dB above the noise level of the test system. Control of the amplitude of individual taps by gate voltage variation was in excess of 20 dB. This voltage control permitted adjustments in phase and amplitude for optimization of the peak-to-side-lobe ratios during correlation.

SECTION II

DESIGN

1. BASIC DESIGN REQUIREMENTS

The monolithic surface wave matched filter signal processor required design in three functional areas; 1) the film layer transducer for SAW generation, 2) the MOSFET piezoresistive taps for SAW detection, and 3) the logic control circuitry for phase seleetion and tap amplitude weighting. In each of these areas there were some critical design choices made based upon improvements required over the previous programmable matched filter efforts. There were five basic problem areas which were addressed:

- Improved transducer quality for achieving higher coupling factors.
- Methods for reducing the reflections of SAW energy at each MOSFET tap due to the high profile of metal and oxide step regions.
- Improved MOSFET device efficiency and reduced overall power drain per coded bit at maximum efficiency.
- Improved off-on ratios in the shift register circuitry to isolate adjacent taps and prevent signal degradation.
- Methods for improved tap amplitude control circuitry, including off-substrate inputs, leading to an overall device reprogramming speed consistent with acoustic wave transit times.

The following sections describe the designs implemented in each of the three functional areas.

2. ZnO Film Layer Transducer Design

The zinc oxide film layer transducer configuration selected was that with the interdigital electrode at the zinc oxide-silicon dioxide boundary and a floating metal plane on top of the zinc oxide. (See Figure 3) Operation was to be at the lower maximum (~0.05λ) film thickness region. This choice was based upon achieving a zinc oxide film quality consistent with the 10 MHz bandwidth requirement and having good conversion efficiency. The thin film geometry also minimizes the topography of the transition between transducer film and detector region and minimizes any beam steering effects in this transition region. Ease of fabrication was also a consideration.

An iterative procedure was used for determining an optimum thickness of the zinc oxide for maximum coupling efficiency with a given silicon dioxide thickness and transducer periodicity. The optimum ratio was 55% zinc oxide to 45% silicon dioxide with a total thickness value of Hk = 0.45 corresponding to a thickness to wavelength ratio of 0.07.

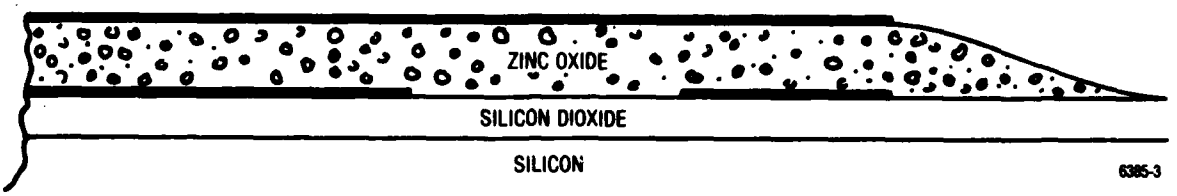


Figure 3. Zinc Oxide Film Layer Transducer Structure

The velocity is dispersive and will affect the bandwidth of the device. To offset the effects of bandwidth narrowing, it is necessary to choose the number of interdigital finger pairs less than that for a nondispersive velocity condition. Using the fact that the bandwidth varies as $(\sin \pi ft/\pi ft)^2$ and the calculated velocity relationship, the number of finger pairs selected was 8.5 to achieve a 10 MHz 3 dB bandwidth.

A standard transducer configuration was chosen with $\lambda/4$ finger widths and spaces of 11 microns to generate the required 100 MHz frequency. This uses a Rayleigh velocity of 4400 m/s which is the closest value for Hk = 0.45 consistent with maintaining the pattern generating accuracy to 1 micron. The active overlap dimension (transducer aperture) was chosen to be approximately 28λ to meet the conditions of a uniform beam across the 3.1 μs tap region and have a reasonable concentration of the acoustic beam energy. This aperture width also maintains an impedance level near 50 ohms for ease of matching broadband inductive matching.

In order to minimize direct signal coupling from the input transducer to the output drain line through the substrate, a P+ region is diffused in the silicon directly beneath the interdigital transducer area. This diffused region is contacted directly to ground in order to eliminate any resistive paths for the electrical fields generated by the transducer. This has proven very effective in the previous development to obtain isolation levels of 85 to 90 dB.

The design selected establishes a limit on the coupling factor value. Since one of the main objectives was to achieve a high coupling factor zinc oxide film, an evaluation was made of deposition parameters to obtain a film quality which would approach the theoretical condition for single crystal zinc oxide. This was done through an evaluation of the optical properties of the ZnO films.

3. PIEZORESISTIVE MOSFET TAP DESIGN

The two major objectives in the design of the MOSFET taps were improved device efficiency and reduction in the structural profile. The choice of a (100) [100] silicon with silicon-gate N-channel MOSFET devices was based upon mobility, speed, profile and gauge factor considerations. There were other design guidelines which placed boundary conditions on the channel detector width and length. The width was minimized based upon having no diffraction of the acoustic beam across the 31 taps. This size, set by the acoustic aperture, was 40 mils or 1 millimeter. The channel length had a lower minimum of 4 microns consistent with silicon gate processing. The choice was made to have side-by-side detector structures with a common drain which

placed an upper bound of approximately $\lambda/3$ or 15 microns. The choice of adjacent tap pairs gives a more uniform structural geometry in the acoustic path than the split channel geometry previously used. It also means that 3 dB in tap conversion efficiency is gained.

The following two sections discuss the selection of the channel length and the structural geometry of the MOSFET taps.

3.1 Channel Length Selection

In order to determine the gate length for best efficiency consistent with the foregoing boundary conditions, the MOSFET tap structure was modeled. Several factors were taken into account. One such factor is the Q of the output tap circuit. For design considerations this Q is a function of the channel conductance and the reactance of the tap capacitance. The capacitive condition that must be satisfied to prevent Q spoiling and an associated increase in detector loss is $C \leq 20\ Ng/\omega_o$ where Ng is the total conductance of the N taps and ω_o is the radian frequency.

The various sources of capacitance can be identified and based upon reasonable assumptions for the silicon gate process equivalent capacitance derived. The capacitance values are fixed by the design geometry and will vary with the MOSFET detector size.

The g value is a function of the channel properties and values may be obtained by modeling the drain current, I_D, versus drain to source voltage V_{DS}. A theoretical computer plot for selected gate voltages from 2-8 volts is shown in Figure 4 for a gate length of 7.5 μm and a worst case temperature of 120°C. The gate width is assumed to be 1 millimeter. The values of g for a single detector tap are shown.

Assuming an average operating value of g = 150 micromhos to avoid additional output loss due to Q spoiling the capacitance must be less than 150 pf. This value was used as a design guideline in the device layout.

The dependence of gate length on detector output has been plotted in Figure 5 taking into account the various capacitive, conductive and piezoresistive effects. The zero dB reference output level is the 16 micron gate value which represents an upper limit based upon geometry considerations. It is also close to the 0.37λ value for minimum loss and maximum bandwidth response. The lower gate length is restricted by processing and mask alignment limitations.

It can be seen that the detection efficiency increases as gate length increases. The major contributing factor is the decrease in the channel conductance with gate length. The actual value obtained is sensitive to processing and would be lower than the ideal case. As the gate length becomes larger, processing induced leakage could result in a leveling off or decrease in the detector efficiency. Also, as the gate length increases in a side-by-side tap configuration the common drain region is reduced resulting in an increased parasitic series resistance and possibility of electromigration effects at high current levels.

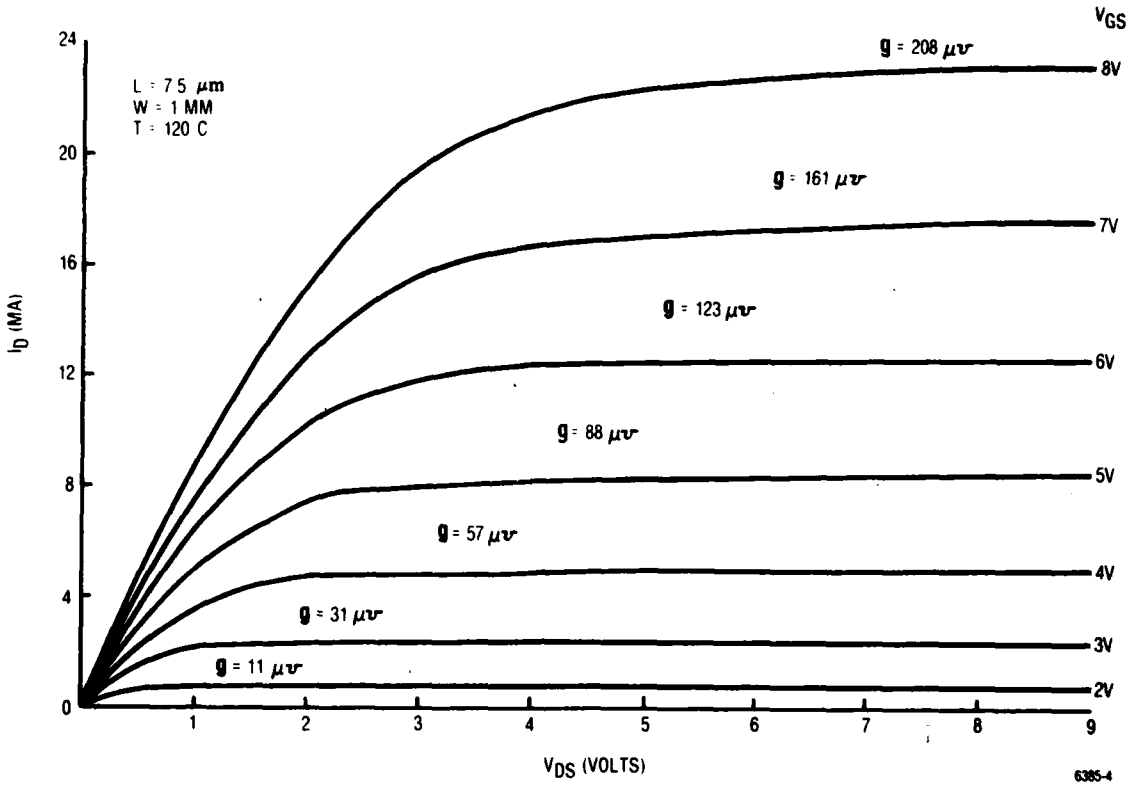


Figure 4. Predicted Voltage-Current Relationships as a Function of Gate Voltage for an N-Channel MOSFET Device.

Another consideration is the detector power consumption. The detectors are operated in the saturated mode with signal output proportional to the square of the detector current. In a MOSFET device as gate-length increases the voltage required to produce the saturated output condition increases proportionately. This effect makes the ratio of signal output to power input less favorable as gate-length is increased.

Taking these various factors into consideration and the advantages of a side-by-side detector structure, a gate length of approximately 8 μm was chosen for development.

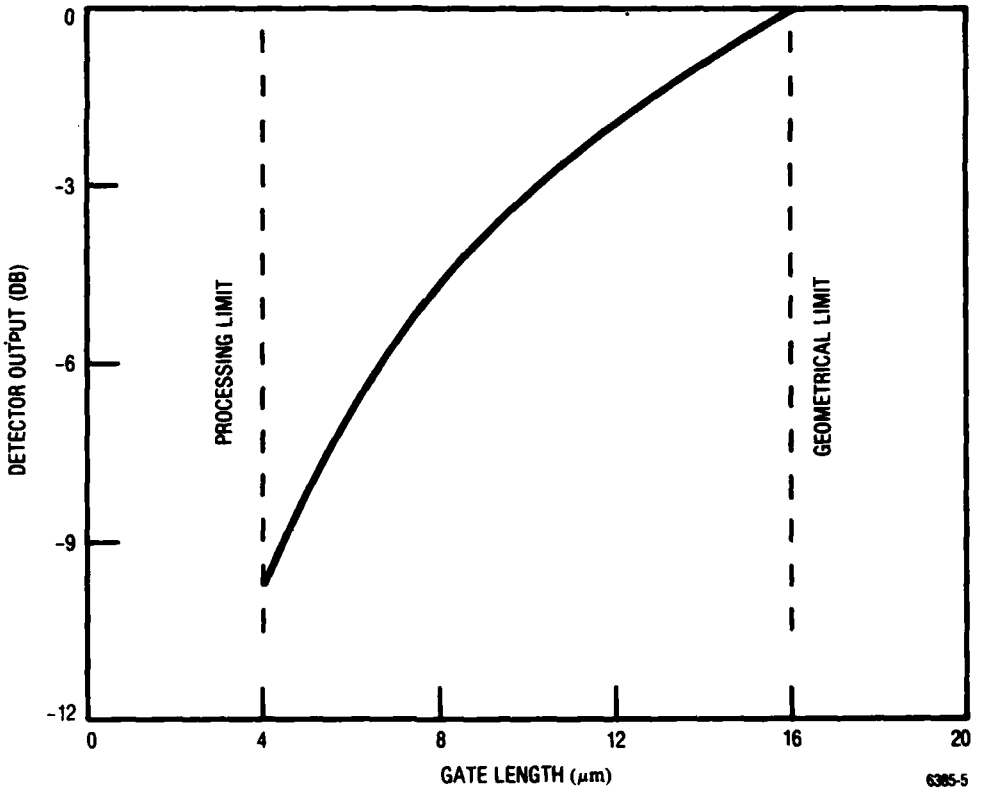


Figure 5. Piezoresistive Detector Tap Relative Power Efficiency Vs Gate Length

3.2 Tap Structure Selection

The second major design consideration is the vertical structuring of the detector tap geometry to limit the scattering losses in the acoustic path to as low a value as possible. For a mass type discontinuity the reflection coefficient to first order is given by[8] $r = c(h/\lambda)$ where h is the thickness of the discontinuity, λ the acoustic wavelength and c is an experimentally determined constant dependent upon the material properties of the layer. Measurements on different simple periodic structures shows that c varies from 0.5 to 3.0.[9] A rough estimate of the value of r can be made from the velocity difference between layer and substrate for small h/λ using the relationship $r = (v_0 - v_1)/(v_0 + v_1)$ where v_0 is the substrate velocity and v_1 is the layer velocity. With an average velocity for the oxide and aluminum combination of 4750 m/s at an h/λ of 0.03 compared to the silicon substrate velocity of 4920 m/s the predicted reflection coefficient is 0.018. With two major reflection discontinuities per tap representing the two gate regions the reflection coefficient per tap would be 0.036. This would result in a c value of 1.2 and a relationship of first order of the form $r = 1.2(h/\lambda)$.

The complexity of the MOSFET topography makes it difficult to trust such a simple measure. From the previous development an effective reflection coefficient was calculated using the observed value of attenuation of acoustic waves through the 31 tap array. This gave an average c constant of 1.6 which is larger than the value

using the velocity difference model. A maximum thickness to wavelength ratio can be specified to reduce the reflections to at least the 3 dB level. For 3 dB the reflection coefficient using c = 1.6 must be less than 0.028. Therefore, the h/λ ratio becomes 0.0175 and at a wavelength of 48 microns the discontinuity heights must be maintained less than 8400 Å. This compares to the previous development where the tap structure was 20,000Å resulting in a 10 dB loss due to reflections.

It was necessary to realize a sharp reduction in the physical size of the MOSFET detector cross-section while maintaining standard processing techniques. The use of a low profile silicon-gate MOSFET technique was selected. The cross-sectional geometry of such a structure with side-by-side gate regions is shown in Figure 6. It is basically a five layer structure with gate oxide, poly-silicon gate, reflow glass, aluminum metal and passivation glass. From the minimum to maximum point on the passivation glass it is approximately 8500 A°. Quarter-wavelength discontinuties have been avoided as much as possible by using $\lambda/6$ channel lengths and a $2\lambda/6$ drain region.

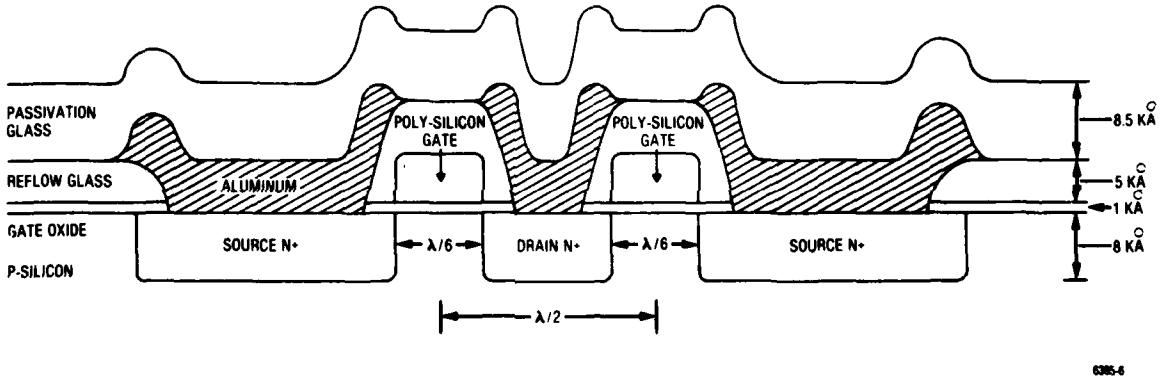


Figure 6. Cross Section of Silicon - Gate N-Channel MOSFET Surface Acoustic Wave Detector.

4. TAP CONTROL CIRCUITRY

There were two major objectives in the design of the logic circuitry controlling the detector taps; 1) to improve the off-on ratio of the shift register circuitry controlling the taps to provide good isolation and prevent signal degradation, and 2) to develop phase and amplitude control circuits leading to a device reprogramming speed consistent with acoustic wave transit times. It was determined that the best control circuit configuration meeting these requirements would be a parallel feed of 31 analog voltages and a parallel-series feed for the phase data. The configuration would permit a microprocessor type of data interface.

Figure 7 shows the primary cell block diagram selected for design. The static shift register circutry controlling tap phase is formed using two basic cells having transmission gates and inverters controlled by the phase 1 clock. The phase 2 clock controls a latching circuit into which the binary data selecting the tap phase is held and isolated from the shift register. This latch couples to the analog switch into which the gate voltage is

applied to the selected detector tap. The switch is designed to pull the tap not being used to ground providing the required tap isolation. Bringing the analog voltage as a direct feed provides for rapid setting of the tap amplitude level. Figure 8 shows a schematic of the individual logic devices required to perform the data and analog voltage transfer, storage and control.

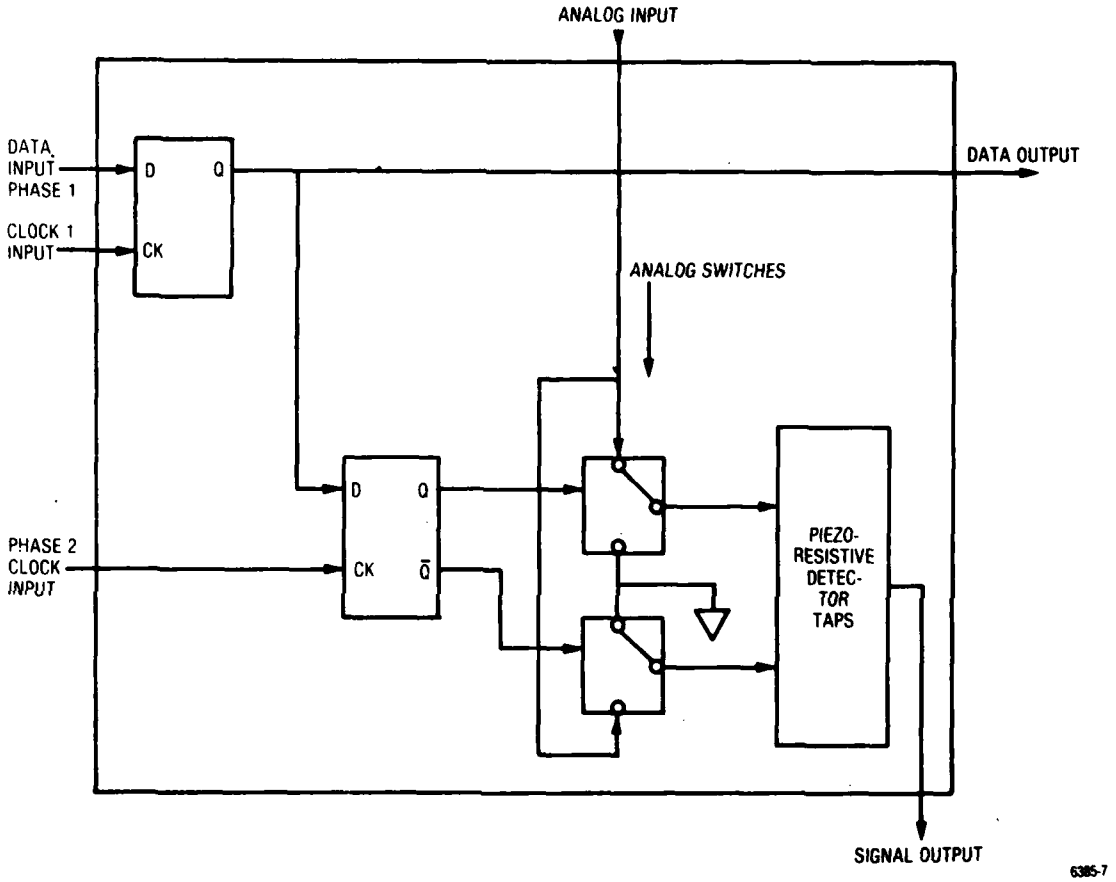


Figure 7. Primary Cell Block Diagram

The overall block diagram is shown in Figure 9 which gives the serial and parallel arrangements for the various input functions. The static shift register is divided into groups of four serial shifts with eight data input and output points. This allows an easy interface with microprocessor controlled external circuits for developing the desired code changes. The latch operates in parallel off the shift register to store the desired code for tap selection. Its ouput is parallel to the transmission gates which direct the analog voltage to the selected tap while grounding its pair.

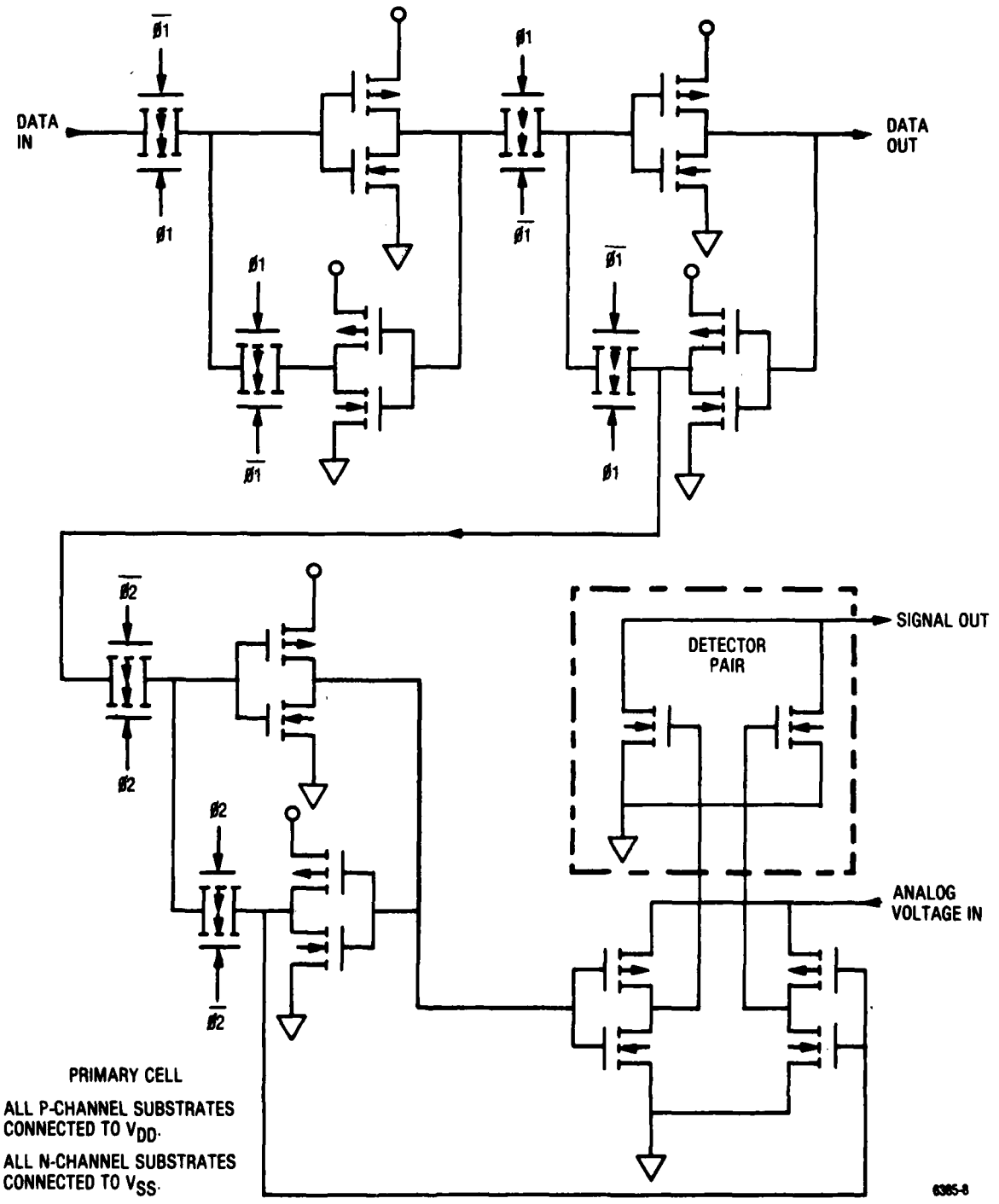
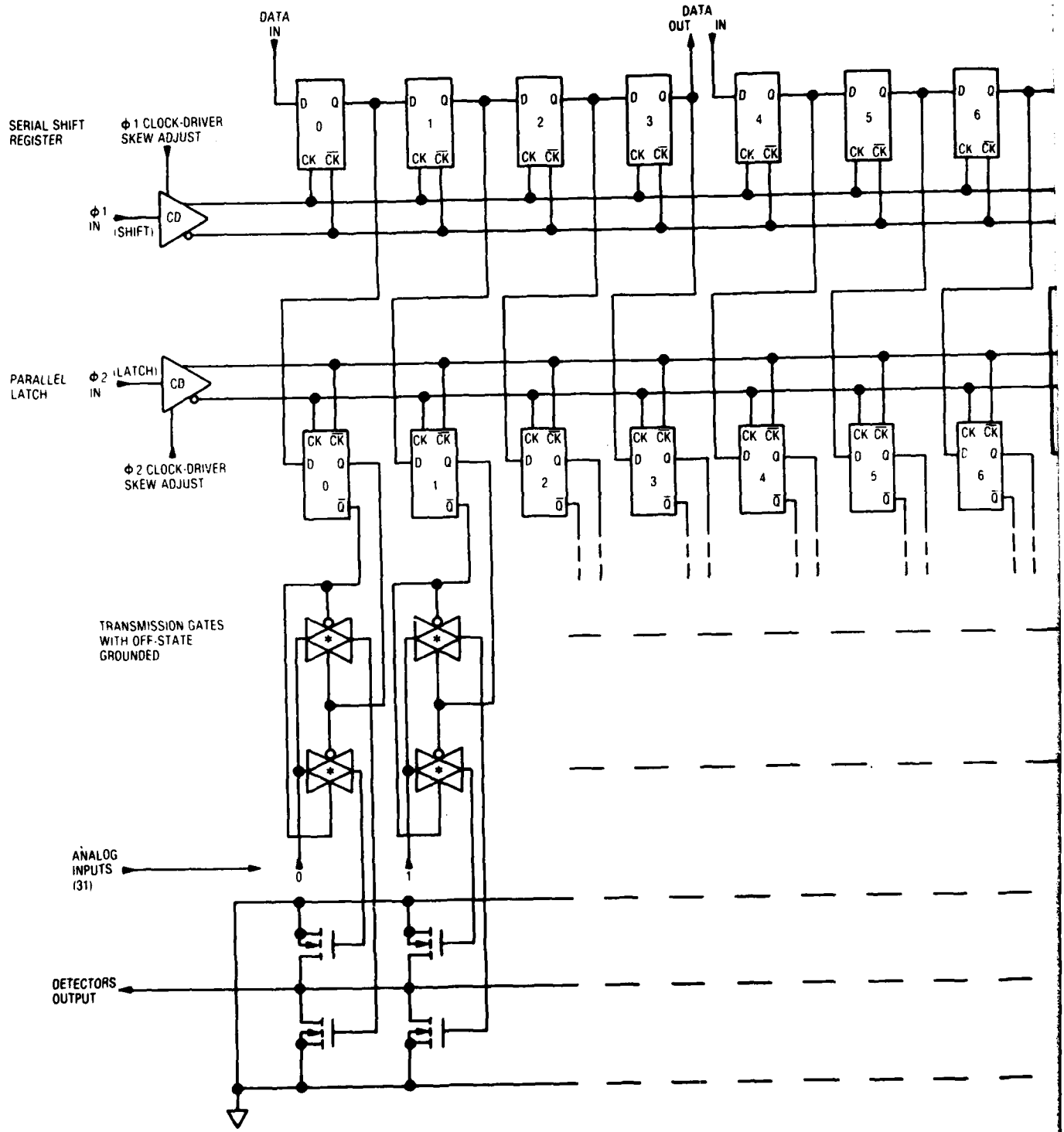


Figure 8. Device Schematic of Logic Circuitry Controlling the Detector Tap Pairs


DATA IN
DATA OUT IN
SERIAL SHIFT REGISTER
Φ1 CLOCK-DRIVER SKEW ADJUST
Φ1 IN (SHIFT)
CD
PARALLEL LATCH
Φ2 (LATCH) IN
CB
Φ2 CLOCK-DRIVER SKEW ADJUST
TRANSMISSION GATES WITH OFF-STATE GROUNDED
ANALOG INPUTS (31)
DETECTORS OUTPUT
D Q
CK CK
0
1
2
3
4
5
6

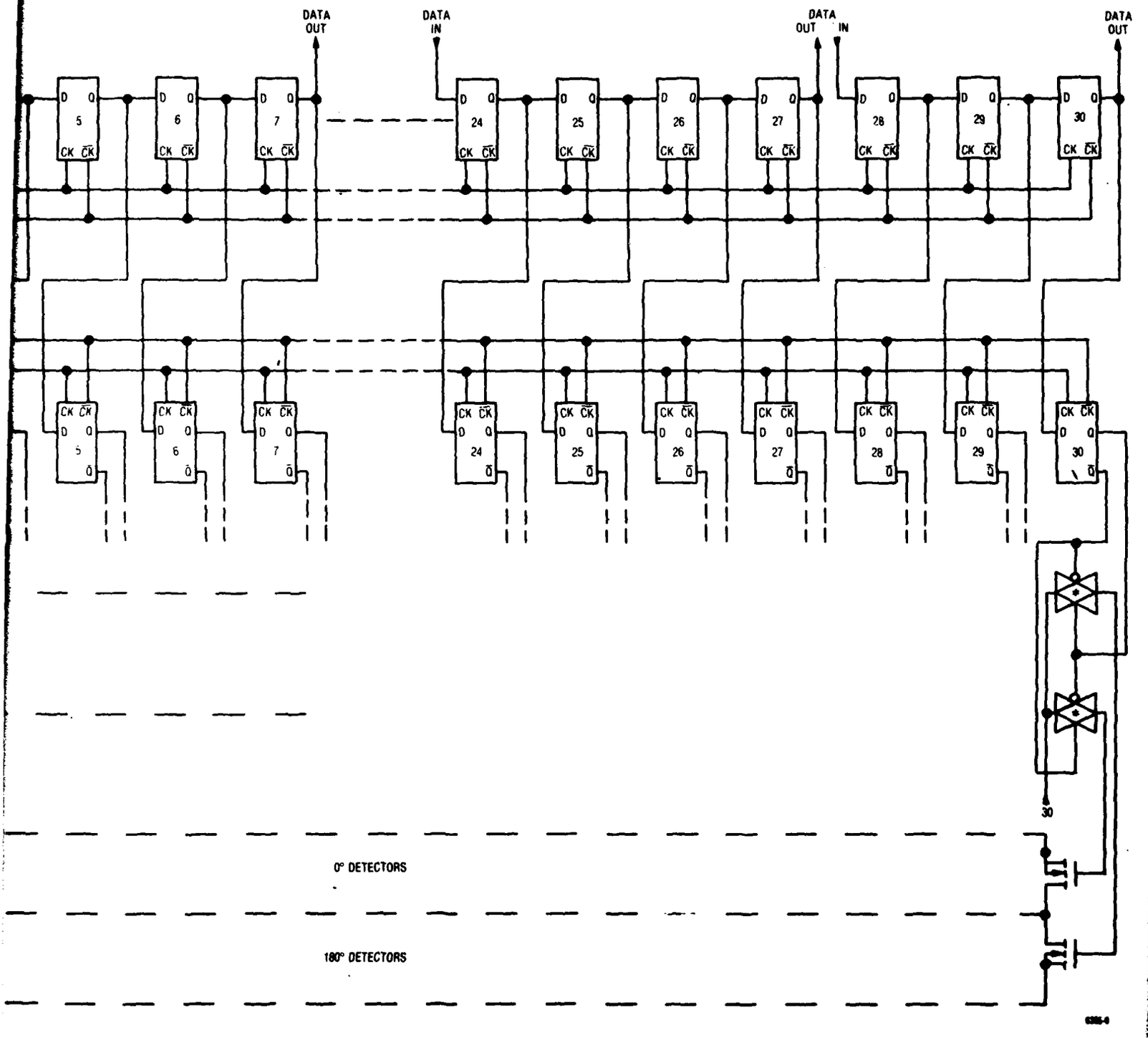


Figure 9. Schematic of Overall Logic Circuit Layout

Computer simulations were made of the tap control circuitry to determine the operating time for the logic functions over the temperature range from -40°C to 125°C at a drain voltage level of V_{DD} = 6 volts. The following summarizes the results of the simulation:

1) Maximum data shift-register clock rate was greater than 10 MHz.

2) Data to the shift-registers and latch were present at least 6 ns before and at least 26 ns after the clock input signal reached 50% of V_{DD} during its high-to-low transition.

3) Data was transfered to the output of each shift-register within 54 ns after the clock input signal reached 50% of V_{DD} during its low-to-high transition.

4) Analog gate voltage to the detectors settled to within 2% within 87 ns after the latch input signal reached 50% of V_{DD} during its low-to-high transition.

5) Input signal rise and fall times were less than 20 ns.

The transfer of data and voltages within a 100 ns time interval assures that the device can be easily encoded within the 3.1 μs time interval.

SECTION III

DEVICE LAYOUT AND MASK FABRICATION

The first one-third of the device layout is shown in Figure 10. The layout of the device centers around the MOSFET detectors which are required to have a specific tap-to-tap spacing based upon the operational parameters and the acoustic velocity.These 31 taps were spaced on 480 micron centers spread across an area which is approximately 600 mils along the propagation direction and one millimeter in width. Each shift register element, containing several MOSFET devices, must address each tap pair. This restricts the dimension of each logic control element along the tap array to less than 0.5 millimeter. The other dimension was not so restricted. A linear dimension of approximately 1 mm normal to the tap array was required for the shift register, latch and analog voltage switches. Clock drivers were incorporated directly on the device.

The transducer electrode structures were placed at each end of the MOSFET tap array with sufficient distance to minimize direct electrical coupling to the tap output line. The contacts were extended into the region behind the transducer to lengthen the distance between the wire contacts from rf-in to rf-out.

The required bias, clock and ground lines addressing the active elements had their contact pads on the periphery of the chip. The rf lines were on the bottom side of the chip and the dc-data lines on the top. There were 47 lines addressing the logic circuitry. Test devices were placed in a region adjacent to the tap control circuitry.

The original layout of each device element was first done on gridded paper in pencil using a scale of one grid element equals one micron. Subsequently the device geometries were digitized and combined into basic cells necessary to make-up the total device. Each basic cell was layered representing the various processing steps and was displayed and examined on a CRT. Finally paper plots were made in an enlarged size for accurately checking device dimensions and line placements before submitting the tapes to the mask shop for pattern generation.

It was necessary to compose the various mask layers from stepped and repeated cells such as those represented by the logic and tap geometries. It was necessary to make 107 reticles for the Electromask stepper to compose the final 10 mask layers. The overall layout had a final division into thirds like that shown in Figure 10. The mask layers required for processing are given in Table 1.

The final chip size was 980 mils by 120 mils. This size accommodated two columns of devices on a three-inch wafer with a total of 36 good devices possible.

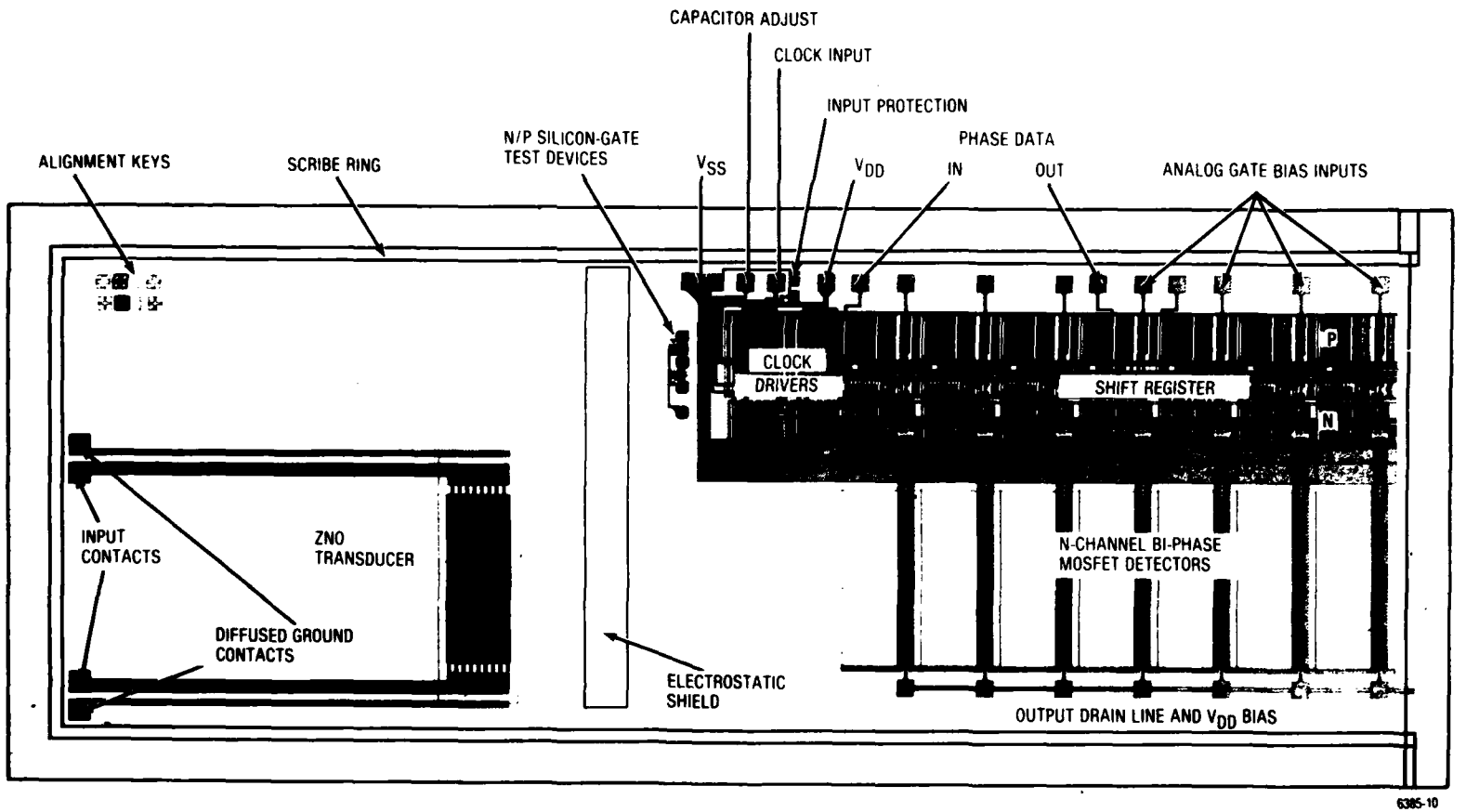


Figure 10. Layout of SAW Programmable Correlator Illustrating Device Features.

Table 1. Mask Layers Required for Processing the Monolithic SAW Programmable Correlator

LAYER	DESCRIPTION
01	P-Tub
02	Thick Oxide
03	Gate-Poly
04	P+ Diffusion
05	N+ Diffusion
06	Pre-Ohmic
08	Metal Definition
08A	Transducer Electrode
08B	Transducer Metal
09	Passivation Cut

SECTION IV

WAFER PROCESSING AND CHARACTERIZATION

An (001) oriented silicon boule, doped with phosphorous was grown for the resistivity range 8-12 ohm-cm. The (001) face was established to an accuracy of 0.5 degree and the boule rounded to a three inch diameter. The (100) face was X-ray oriented to within 0.25 degree and a one inch flat ground on the boule. Wafers were sliced from the boule, ground and polished to a thickness of 20 mils. The polished face was free of any visible defects and subsurface damage. Two wafers were randomly selected from the lot of 50 and the orientation accuracy verified using a Laué backscatter X-ray technique. A special concern for orientational accuracy is necessary to prevent beam steering of the acoustic waves.

The alignment of the first mask layer to the wafer flat is the most critical. The highest accuracy attainable on the projection aligner was determined to be 0.01 degree. The worst case was estimated at 0.25 degree. Such accuracies preclude amplitude degradation due to beam steering.

A low-profile silicon gate CMOS process was used to develop the semiconductor devices. The major process steps are shown in Table 2. No special process steps were developed. A thinner aluminum contact metal was used. Before implementing this step there was a test part processed with thin metal. It was examined by SEM for step coverage reliability and tested at current densities to determine power handling capability. There were no problems observed.

Table 2. Significant Process Steps in Fabricating the Monolithic SAW Programmable Correlator

1. Initial Oxide Growth	8. Vapor Glass Deposition
2. P-Tub Pattern and Implant	9. Aluminum Deposition, and Pattern
3. Gate Oxide Growth	10. Gold Back
4. Channel Implant for Threshold Adjust.	11 Passivation Glass Deposition
5. Deposit Polysilicon Gates	12. Electrode Pattern
6. P+ Pattern and Implant	13. ZnO Deposition
7. N+ Pattern and Implant	14. Aluminum Pad Contact, Pattern and Etch.

The zinc oxide transducer processing was done on the wafers after the MOSFET processing was completed and the wafer was glass passivated. The wafer was aluminized (1000Å) and the interdigital electrodes replicated using standard photolithographic techniques. The zinc oxide was dc triode sputtered through an aperture mask over the electrode structures. The sputtering conditions are given in Table 3. The final steps in the processing of the zinc oxide transducers were 1) the deposition of 1000Å of aluminum on the wafer 2) photoreplication of the aluminum metal plane directly over the interdigital electrode region, and 3) a final etch definition of the zinc oxide around the pad region. The final wafer processing step was the etching of the glass passivation to expose bond pads for electrical contact.

Table 3. Sputtering Conditions For Zinc Oxide Film Layer Transducers

Pressure	3.0 μ m
Gas Mixture	90% Ar-10% O_2
Substrate Temperature	250°C
Deposition Rate	220 Å/min
Target-Substrate Distance	4 cm
Target	4.0 inch diameter ZnO pressed cake
Target Voltage	2.3 KV
Target Current	50 mA

A photograph of a processed wafer is shown in Figure 11 and a closer view in Figure 12. The wafer has a potential for 36 good die. There was one wafer lot of 10 started through processing. Two wafers were processed to completion and die selected for fabrication and testing from one of the wafers.

A comprehensive probe test was developed, the test program written and a probe card fabricated. However budget limitations prevented the full characterization of wafers using the test set. One wafer was manually probed to assure that there were no apparent catastrophic device failures and that working die could be expected. The results of the manual probe tests showed that:

1. Approximately 50% of the 20 die tested were functional
2. The quiescent leakage currents were less than 1 micro-amp.
3. Data could be clocked through the shift register at rates of at least 4 MHz which was the limit of the pulse generator used.

4. The drain current at V_{DD} = 6V and a clock frequency of 4 MHz was 30 mA which was anticipated.

5. The cross-data latches responded to a clock input virtually identical to the serial shift register.

6. Proper operation of the analog switch and detectors was indicated by FET response produced on a curve tracer.

The basic FET characteristics were measured using the test pattern on the die. They showed a reasonable processing uniformity within the desired specifications with threshold values of 0.8 volts for N-channel devices and 0.4 volts for P-channel devices.

The quality of the zinc oxide transducers was measured by a recently developed optical technique.[10] There is strong experimental evidence that a film with low optical propagation loss will have high coupling efficiency and low acoustic propagation loss. There was sufficient room on the side of each wafer to permit a measurement of optical loss in the waveguide propagation mode. The optical losses were less than 10 dB/cm indicating coupling efficiencies in the range of 80 to 90 percent of theroretical.

The final basis for selection of die for packaging was a very careful Class A visual inspection of one of the two processed wafers. On this wafer 14 of the 34 die inspected had no visual defects, 8 had defects sufficient for rejection and the remainder had foreign matter smears or defects which alone would not have prevented their satisfactory operation.

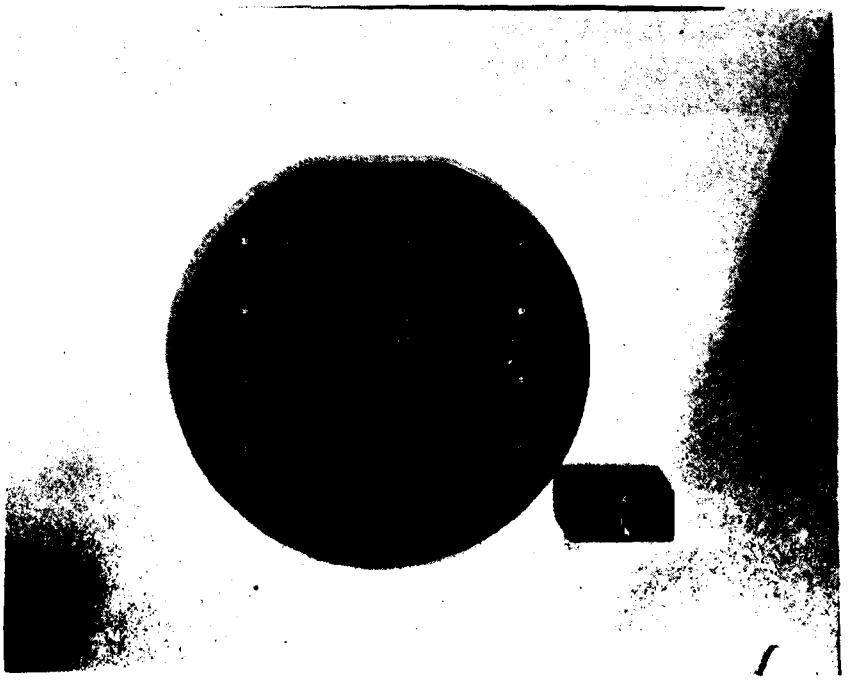


Figure 11. SAW Programmable Correlator Wafer.

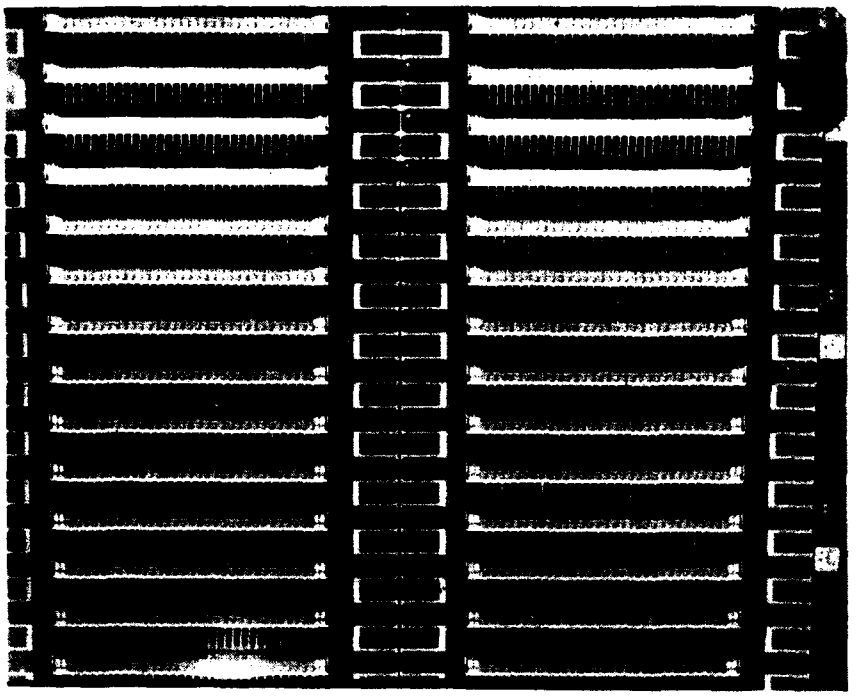


Figure 12. Closeup of SAW Programmable Correlator Wafer.

SECTION V

DEVICE FABRICATION

1. WAFER SCRIBE

After the potentially good die were identified on the wafer, a Disco dicing saw was used to cut the wafer for subsequent breaking. The 1.5 mil thin diamond impregnated blade of the saw rotates at 31,000 rpm while a continuous flow of D.I. water rinses the surface. The cutting speed reduces edge chipping to an absolute minimum, while the D.I. water rinse eliminates silicon dust contamination on the surface. Die identity was maintained with a semi-adhesive plastic backing.

2. DEVICE PACKAGING

A commercially available all metal flat-pack, the Isotronics IP 1605, was used to house the transversal filter chip. A pin out configuration was chosen to accomodate all necessary dc and rf interconnections to the package pins. To allow proper routing of the dc and rf voltages and maintain short wire bonds, two aluminum oxide substrate circuit boards were used. The alumina substrates had thick film gold metallization for the conductor paths. The positioning of the alumina substrates and the device chip in the package are shown in Figure 13. The upper alumina substrate routes all of the bias, clock analog voltages and ground connections to the shift register circuits. The other alumina substrate is used to route the drain voltage and rf output of the MOSFET taps. The transducers are connected directly to the package pin leads and the ground connections of the transducer structure go directly to the bottom of the metal package.

3. DEVICE ASSEMBLY

The alumina substrates and the MOSFET chip were secured to the bottom of the flat pack using a high conductivity silver adhesive, Ablestik 36-2. The adhesive provides a strong bond but allows substrate removal by heating above 125°C. After the ceramic substrate and MOSFET chip had been attached to the package and the adhesive cured, the device was ultrasonically wire bonded with 0.001 inch aluminum wire. Using an ultrasonic wire bonder avoids the damaging temperatures presented by ordinary thermo-compression (TC) bonding techniques. The final step was to place an acoustic absorber on the surface of the chip at each end behind the ZnO transducers. The absorber eliminates surface waves that reflect from the ends of the chip, thereby reducing the level of spurious outputs. The material used as the absorber is made by Dow Corning (RTV 3145). The package could be hermetically sealed if required. For testing the lid was simply held in place to prevent mechanical damage. A close-up of the packaged die is shown in Figure 14. A total of six die were packaged for evaluation.

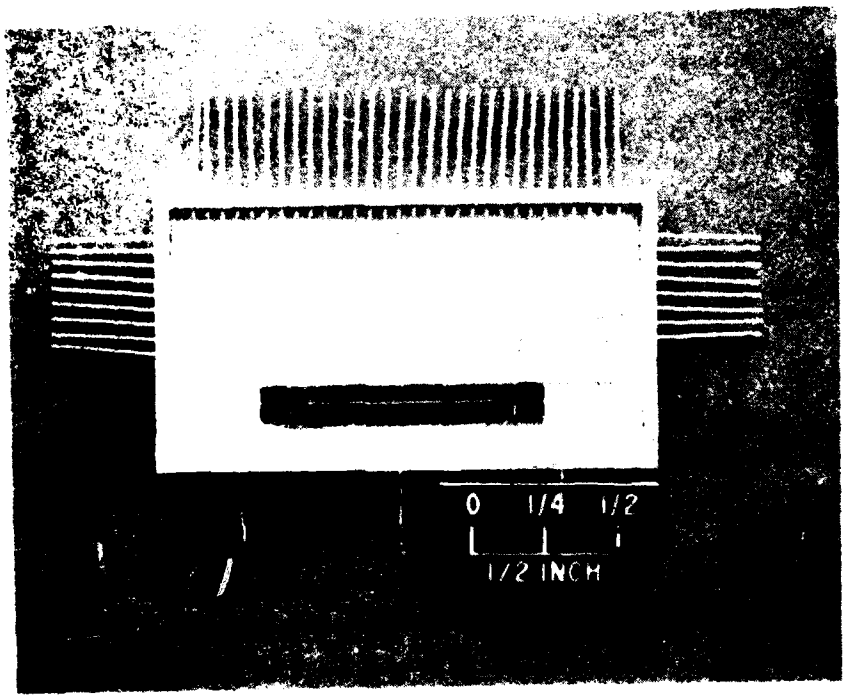


Figure 13. Packaged SAW Programmable Correlator.

Figure 14. Closeup of Package SAW Programmable Correlator.

4. PACKAGE HOLDER

The device package holder used for testing serves the purpose of 1) providing a simple means of connection to dc and rf sources, 2) accommodating rf matching networks while maintaining input-output isolation, and 3) heat sinking. The brass test fixture with printed circuit board is shown in Figure 15. The microstrip circuit board with soldered package pin connections routed the various bias, clock, data and analog voltages to the proper pins. The input connectors to the zinc oxide transducers have isolated compartments for the matching which was a series coil. The detector output lead was fed directly through a small hole to the opposite side of the package holder where an isolated compartment for the matching circuit could be accommodated. The rf connectors were standard OSM. It was possible to achieve a 90 dB level of isolation between input and output with the device operating in this package holder. The multipin connector mated directly with a connector on the test-set box.

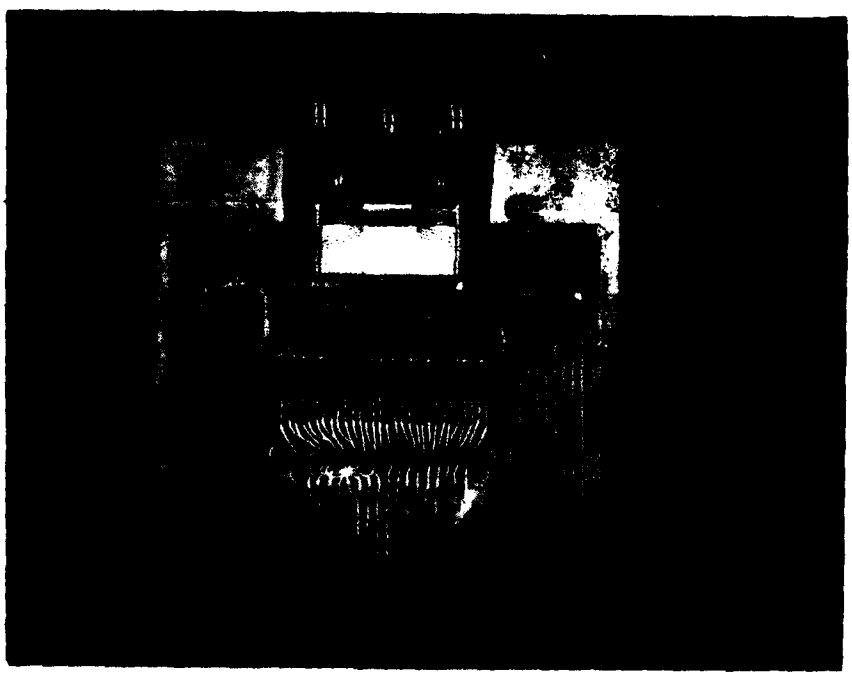


Figure 15. Housing for Programmable Filter For Rf Testing.

SECTION VI

TEST SET AND TEST PROCEDURE

1. TEST SET

In order to evaluate the phase and amplitude programmability features of the monolithic surface wave programmable matched filter signal processor it was necessary to develop controlled logic and rf signal inputs to the device. A digitally controlled test set was developed because it best met the criteria for ease of signal control and versatility of signal output.

An overall block diagram of the equipment used in the test mode is shown in Figure 16. The basic test configuration consists of an appropriate rf signal source, switch, pulse generator, the programmable matched filter, bias supplies, amplifiers, attenuator, oscilloscope display and a specially designed rf/dc encoder test box. The auxiliary support equipment is standard test gear normally available in any electronic test area. The rf/dc encoder test box used for the correlation tests was designed using standard piece-parts and a breadboard housing. Its operation is described in the following section.

2. PROGRAMMABLE TEST BOX

The digital portion of the test fixture provides all digital signals and controls to enable the SAW processor to be evaluated. Figure 17 shows the unit under test with all of its digital inputs. A 100 MHz signal generator, whose frequency is slightly variable, supplies about 0 dBm to the modulator. The modulator produces a 0° to 180° shift of the 100 MHz as determined by an "0" or "1" at the digital input "B" as shown in Figure 17. The following amplifier provides up to +30 dBm to the transducer of the SAW processor. The 100 MHz from the signal generator is divided by 10 to produce the basic clocks for all of the digital circuitry.

One 31 bit shift register and eight 4 bit shift registers are provided to store the 31 bit code from the code switches. The 31 bits are shifted out at 10 Mb/sec into a 100 ns delay F/F to supply the digital signal to the modulator. The eight 4 bit shift registers are shifted 8 bits in parallel into DO-D7, thereby providing the 31 bit word in storage within the processor. At the appropriate time, all 31 bits will be dumped into the internal control F/F's of the processor.

A set of two bi-phase code switches are provided for setting two arbitrary 31-bit codes. They may be selected one at a time or alternately. In addition, at any time, an all "1's" code, or all "0's" code may be set in order to test tap uniformity.

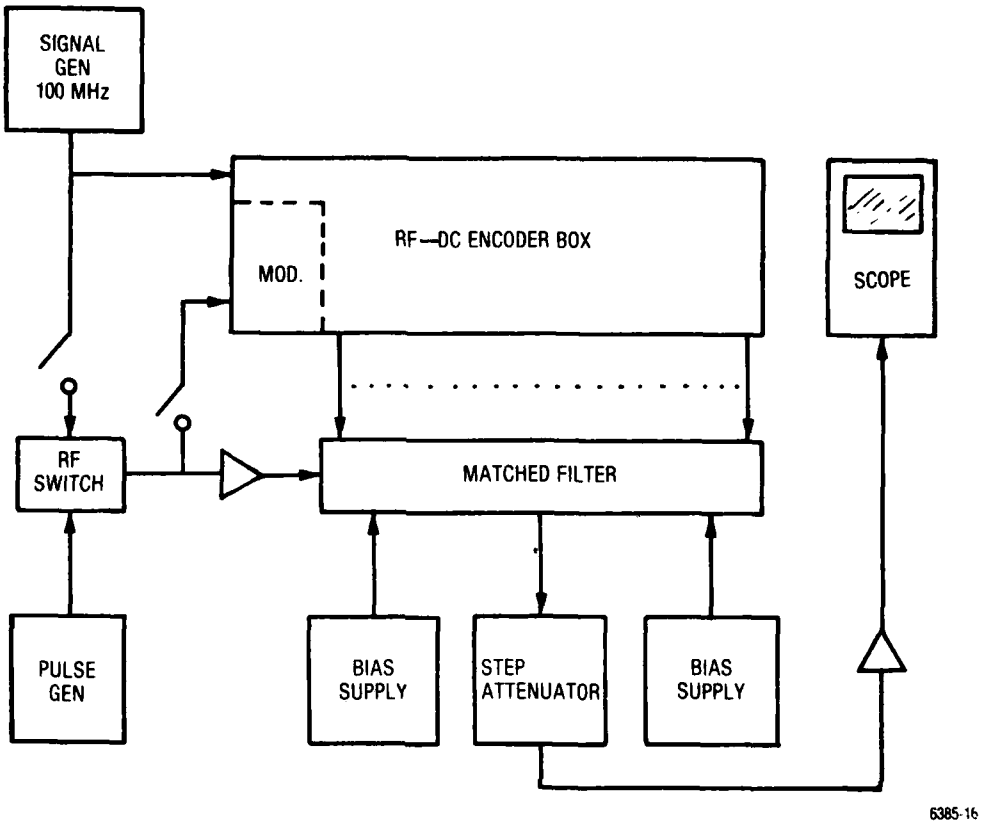


Figure 16. Block Diagram of Test Set

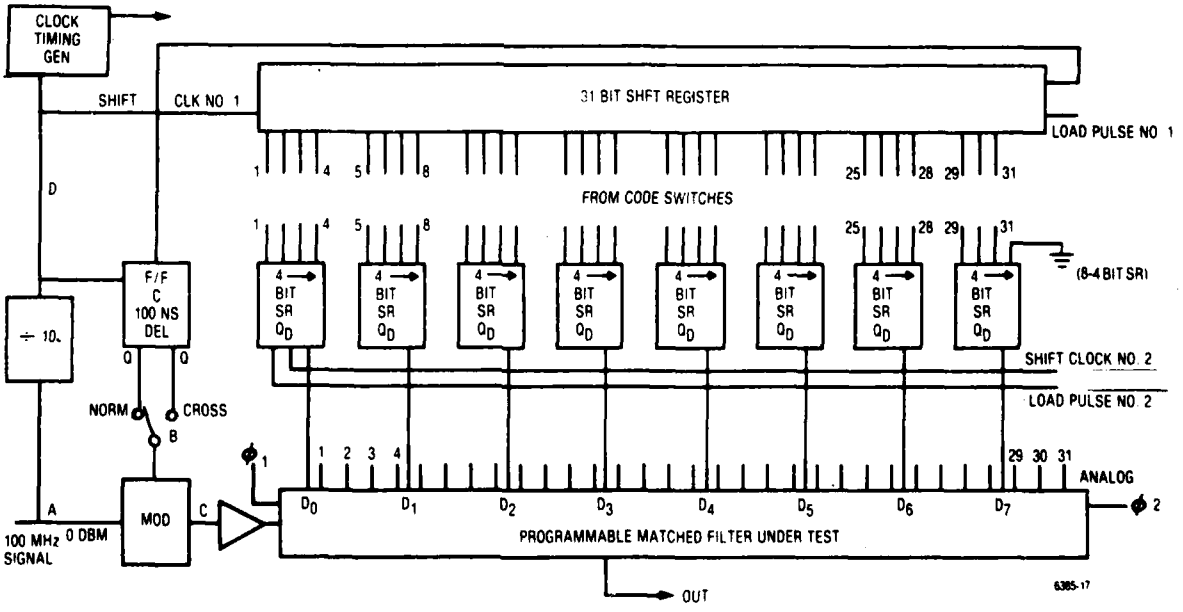


Figure 17. Basic Digital Test Interface

Figure 18 is a block diagram of the clock and control signal generation; while, Figure 19 shows the timing and waveforms. As indicated the 10 Mb/s is the source for all signal generation. It is divided by 31 to produce waveform E, which controls the basic 31 bit word counting; and, it is divided by 2 to produce the alternating A/B code.

The E output (10 Mb/s÷31) is delayed 100 ns and used to generate a 25 ns pulse which allows a delay for setting up the two 31 bit codes before applying load pulses #1 and #2 for loading SR#1 and SR#2 of Figure 17. At the time the registers are loaded, the sequence of operation begins. Bit 31 starts out SR#1 and is delayed by 100 ns before going to the modulator as shown by I & B waveforms. The 16 bit SR for timing of the clocks is initiated by H which has been delayed $\simeq 1\mu s$ to produce waveform J and subsequently causes a "1" to be shifted down the 16 bit shift register.

As the "1" shifts down the shift register, Q2-Q5 are "or'ed" to produce a 400 ns "D" input to a F/F which in turn produces a 400 ns wide pulse. This pulse is "and'ed" with the 10 Mb/s clock to produce shift clock #2, as shown in L. Shift clock #2 produces the DO-D7 code sequences to the eight 4 bit registers. The inverted (as shown by M) shift clock #2 is applied to the $\phi 1$ clock of the processor to shift the eight 4 bits as presented to DO-D7 into memory in the processor.

The ϕ 2 clock is produced by delaying the "1" in the 16 bit shift register as it passes by Q10, by 100 ns. The pulse dumps the internal memory of the processor into the gate memory cells and therefore enables the desired gate switches. This dumping occurs after the code begins inputing into the modulator, as shown in N.

From the above it can readily be seen that a 100 MHz pulse train modulated by 31 bits is fed into the transducer of the programmable matched filter signal processor. At the time the first bit enters the transducer the 31 bit shift register and the 84 bit shift registers are loaded with the same 31 bits. No other action occurs for 1 μs at which time the first bit of the 31 bits is approximately at pickoff tap #4 of the processor. This allows 0.6 μs delay from the input transducer to the first tap. During the next 700 ns the 4 bits of code for each 8 bit shift register is shifted into the processor and at the end of this period are dumped into the processors switch memories. The correlation occurs when the 1st bit arrives at tap 31. Timing flexibility was built into the circuit to allow for variations as required.

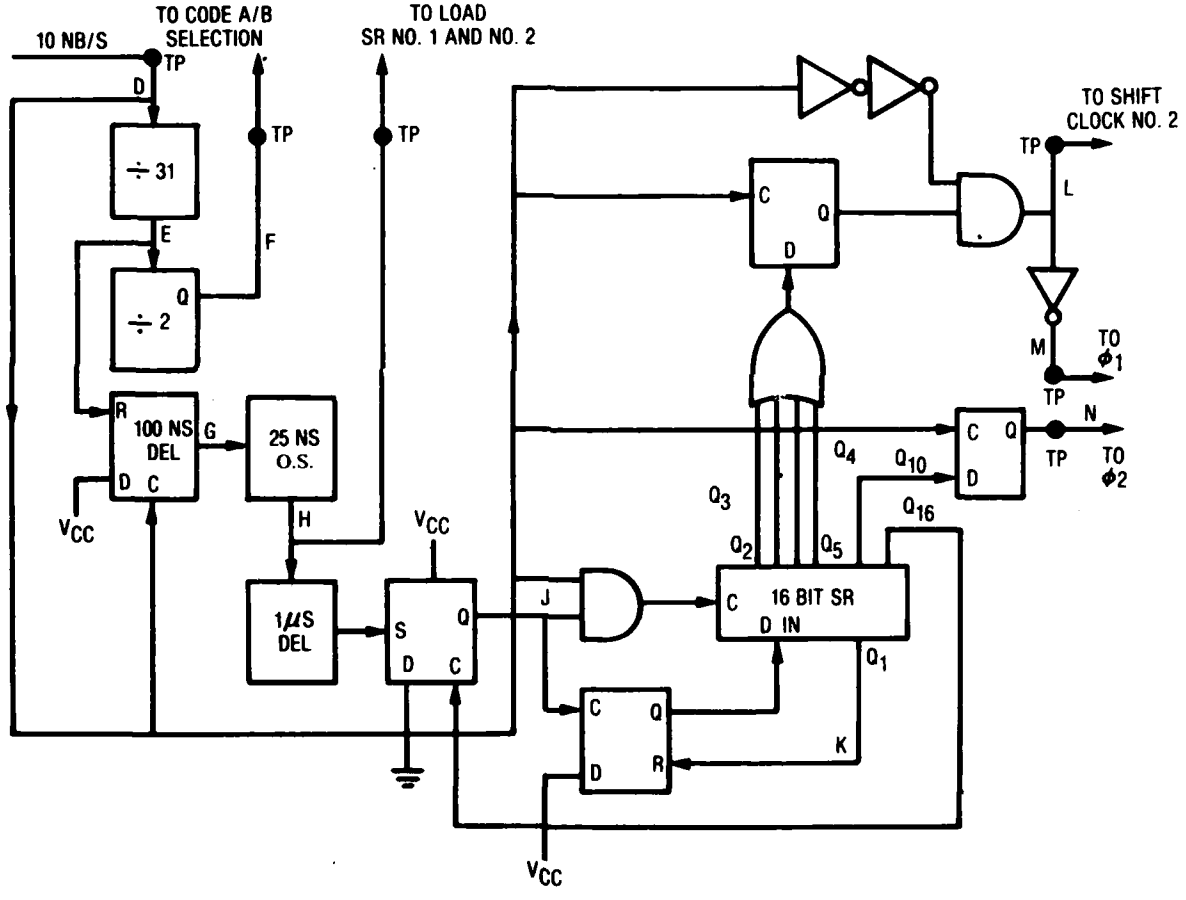


Figure 18. Clock Timing Generator

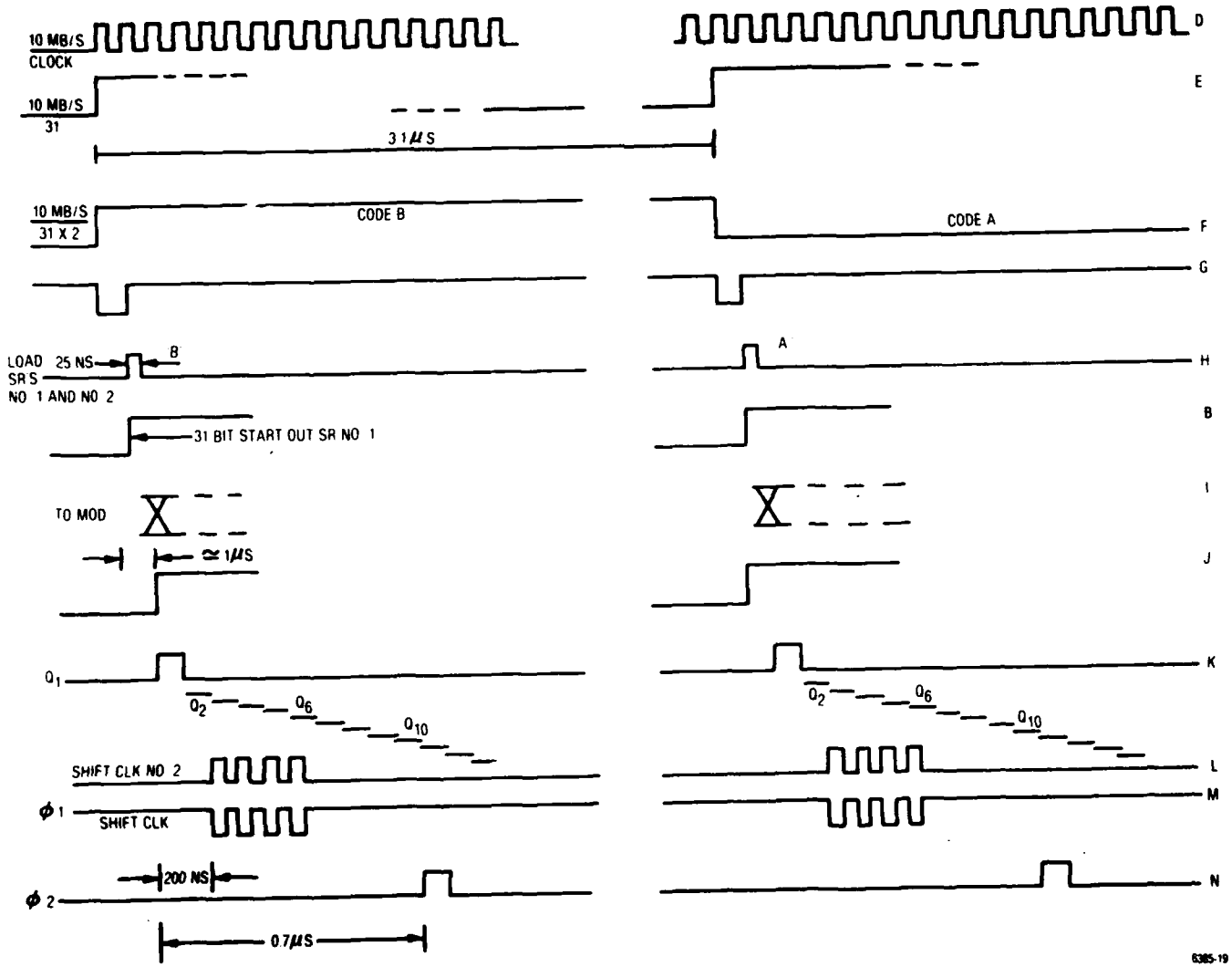


Figure 19. Timing Diagram

3. TEST PLAN/PROCEDURE

The following key electroacoustic device control circuit and correlation processing properties were to be evaluated to delineate the basic operational characteristics of the surface acoustic wave programmable matched filter.

a. Transducer efficiency

b. MOSFET tap efficiency

c. Tap amplitude uniformity

d. Direct rf feedthrough level

e. Tap phase modulation

f. Amplitude control range

g. Correlation peak/sidelobe

h. Programming speed

The measurements were divided into three phases relating to the type of test, device interconnection scheme and test equipment and procedure required. Properties a,b,c and d are basic electroacoustic device measurements involving a pulsed rf signal drive to the transducer with the MOSFET taps selectively activated by the shift register and analog voltage supply. Properties e and f evaluate the detector tap response to the digital shift register and analog voltage control. The purity of the phase modulation and amplitude control range can be determined by code selection, pulse excitation and display of the coded sequences. The full rf/dc encoder test box is used for the final g) correlation and h) programming tests with the packaged device to measure the correlated pulse properties together with a demonstration of its signal processing capabilities by cycling between two contiguous codes.

Table 4 shows the organization of the measurements under the three different test conditions. The following briefly summarizes the basic procedure used for each test.

a. The transducer efficiency is determined from rf pulse insertion loss measurements made on packaged two transducer devices. The transducer electromechanical coupling coefficient, k^2, is determined by calculation from the transducer efficiency measurements.

b. The conversion efficiency of the MOSFET tap structure is measured by varying the analog voltage supply to selected taps of a packaged device with a pulsed rf input to the transducer. The loss per tap is determined as a function of drain current and the power consumption necessary for efficient detection is established.

c. The tap amplitude uniformity is determined by setting the detectors to all "1s" or "0s" with a

uniform gate voltage applied and measuring the displayed amplitude change across the 31 taps. The tap amplitude uniformity can also be determined by selective tap biasing through the detector array, by pulse echo techniques and by the frequency bandpass characteristic.

Table 4. Surface Wave Transversal Filter Tests

Device	Control/Detector Circuit	Signal Processing
Parameters	Parameters	Parameters
a) Transducer Efficiency	e) Tap Phase Modulation	g) Correlation Properties
b) MOSFET Tap Efficiency	f) Amplitude Control Range	h) Programming Speed
c) Tap Amplitude Uniformity		
d) Direct RF Feedthrough		
Equipment	Equipment	Equipment
1) RF Pulse Source	1) DC Part of Encoder Test Box	1) RF/DC Encoder Test Box
2) Pulse Generator	2) RF Signal Source	2) RF Signal Source
3) Bias Supplies	3) Bias Supplies	3) Bias Supplies
4) Amplifiers	4) Amplifiers	4) Amplifiers
5) Display	5) Display	5) Display
6) DC Part of Encoder Text Box	6) Pulse Generator	

d) The direct feed-through signal level is determined by applying an rf pulse to the input transducer and measuring the amplitude of any undelayed pulse at the detector output.

e) Tap phase modulation characteristics are evaluated by displaying on a high frequency oscilloscope the coded response of the detector taps to a pulsed rf signal. The time span for each chip is determined, the purity of phase reversals observed and the chip characteristics under phase reversal examined.

f) The amplitude control range is determined from the coded output signal response to a pulsed input by measuring the displayed amplitude under voltage variations. The effect of voltage control on a single tap to its nearest neighbors is also determined. Voltage control is used to level the output pulse response and determine the dynamic range control available.

g) The autocorrelation properties of the programmable matched filter are determined by introducing encoded 31 bit sequences through the input transducer and measuring the correlated output response for the

same code introduced to the taps. The time response of the peak to the sidelobe characteristics is displayed. Peak to sidelobe ratios are determined and the time width and envelope characteristics of the correlated pulse measured.

h) The programming speed is determined by cycling between two codes at a 3.1 microsecond time rate and observing coded and correlated signals. The autocorrelated signals are displayed and measured for coded sequences to determine if the characteristics observed in g) have been preserved under this contiguous operating condition.

SECTION VII

RF DEVICE TESTING

1. INTRODUCTION

Device testing was carried out on six of the packaged correlators taken from one wafer. Two devices were selected from the six for full testing. The results are considered representative of the performance characteristics to be observed in a typical device since there was no electrical screening at the wafer level to select the best devices.

2. TRANSDUCER CHARACTERIZATION

RF signal testing between transducers at each end of the device helped characterize loss and bandwidth properties. The response of the output transducer to a 100 MHz pulse of 100 ns duration applied at the input transducer is shown in Figure 20. It consists of the output pulse plus low level trailing pulses indicative of reflection centers in the transmission path. The matched loss which included two transductions plus propagation loss was 32 dB. The first trailing pulse was 28 dB below the output. An expanded display of the trailing pulses coming from MOSFET tap reflections is shown in Figure 20 (b). The level of reflections has been reduced considerably over the previous device development where the first trailing pulse was only 6 dB down.

Pulse echo measurements were made using one transducer as input and output, to observe the time reflections of the MOSFET taps. Figure 21 is a scope photograph of such a measurement. The first reflection occurs at 1.2 μ sec, (round trip position of the first MOSFET tap), and there is a decay of 6 dB across 62 reflection centers. The single pulse at the end of the reflection train is from the transducer at the opposite end which has not been dampened out. The decay rate is 0.1 dB per pulse which would indicate approximately 3 dB of loss for transmission through the MOSFET taps. By using the reflection data from both transducers the conversion loss of each transducer could be ratioed and from transmission data a loss assigned. Typically, the conversion losses were equally divided, approximately 15 dB, however in some cases transducer conversion losses as low as 12 dB were obtained.

Figure 22 shows a swept frequency response for two ZnO transducers on a 2.5 MHz division scale and on an expanded 1.0 MHz per division scale. The minimum insertion loss of 32 dB is at a frequency of 99 MHz and the 6 dB bandwidth is 9 MHz. The characteristic shows some asymmetry at the high frequency end. The notches at 95.5 MHz and 100.5 MHz are due to the MOSFET tap reflections and are 3.5 and 3.0 dB respectively. This is a second indication of the signal droop expected through the 31 taps. On the previous development the notches were in the 10 to 15 dB range. The 5 MHz spread of the major dips is consistent with a 200 ns reflection time between adjacent MOSFET taps. There was also a fine ripple response (< 0.5 dB peak to peak) superimposed on the frequency characteristic which had a periodicity of approximately 1 MHz representative of the 1 μ s delay between the transducer and the tap array.

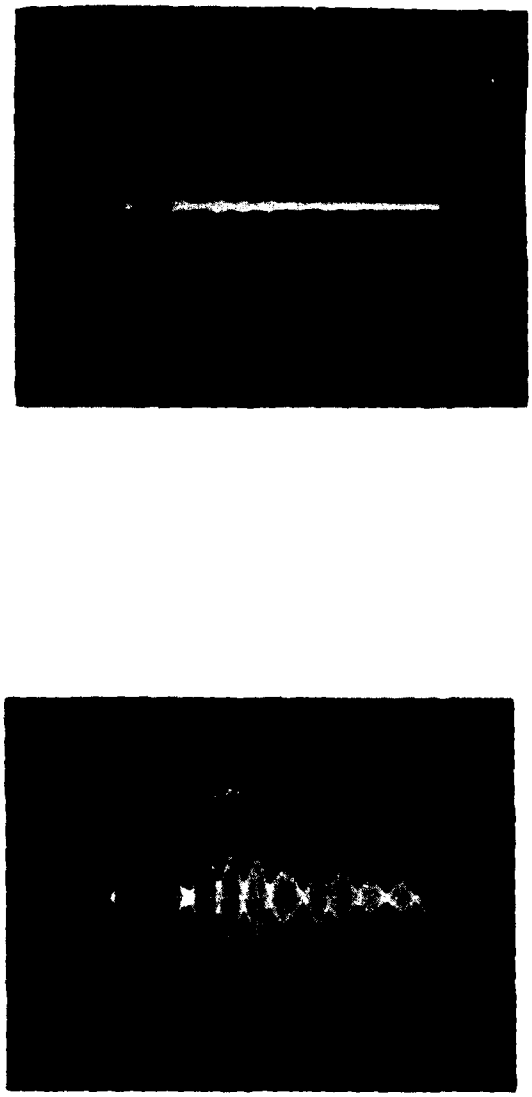


Figure 20. Oscilloscope Display of Pulse Output Waveform Between Transducers

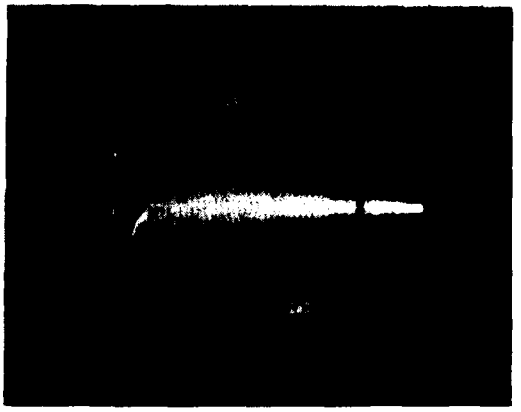


Figure 21. Pulse Echo Reflection from MOSFET Taps and Transducer

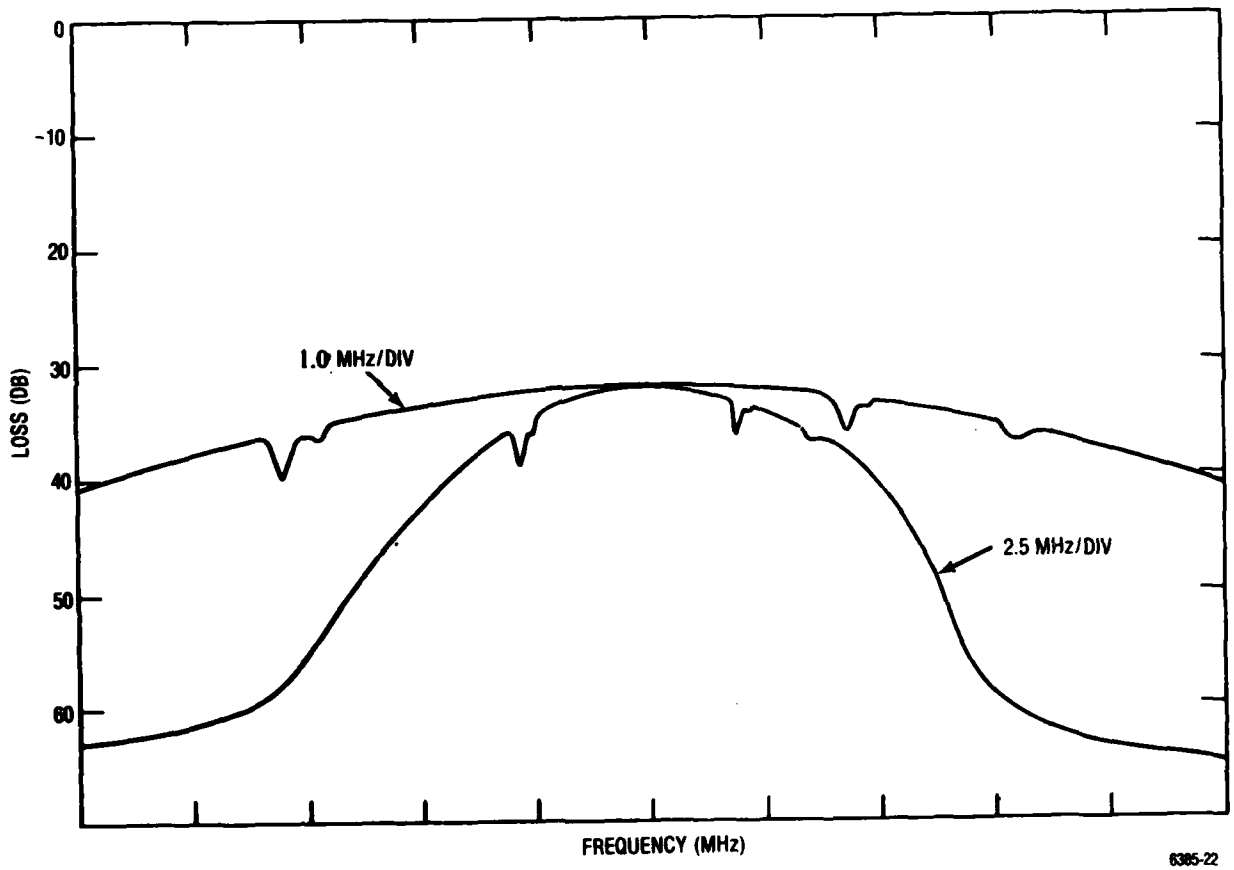


Figure 22. Bandpass Characteristic of Two ZnO Film Layer Transducers

The results of characterizing the transducer response of the six devices showed an average conversion loss of 15 dB per transducer and a 3 dB bandwidth of 9 to 9.5 MHz per transducer. Calculating the k^2 coupling factor gave values in 0.6 to 0.7% range compared to an optimum single crystal value of 0.8%.

3. MOSFET TAP CHARACTERIZATION

The input impedance of the 31 tap MOSFET detector array was measured on an HP Network Analyzer and used to develop a matching circuit for the detector array. A broadband matching circuit was fabricated based on the measurements. The matching circuit was not optimized for the lowest loss over a 10 MHz bandwidth.

Individual MOSFET taps were activated by applying gate bias and pulsing the ZnO transducer. By applying equal voltages to taps throughout the array an additional measure of the amplitude degradation due to reflections could be obtained.

Figure 23 shows taps 1 and 24 activated on a single device. The amplitude difference is 2.5 dB which is approximately 0.1 dB reflection per tap.

Displaying the output response to a pulsed input from all taps under equal gate voltage conditions permits an assessment of tap amplitude uniformity and a calculation of tap efficiency. Figure 24 shows such a sequence of outputs taken from the center portion of the detector taps. The peak to peak variation across the coded tap output is 3 dB. The time waveform could be leveled to less than 1 dB by adjusting individual gate voltages.

Figure 23. MOSFET Detector Outputs from Two Isolated Taps

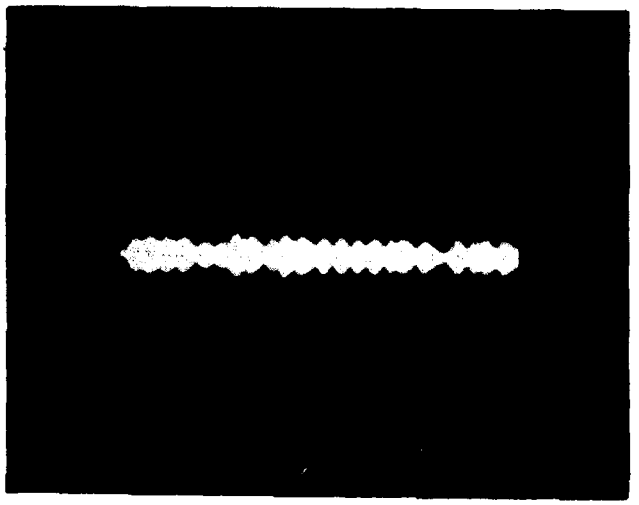


Figure 24. Output from a Group of MOSFET Detector Taps

The conversion efficiency of the MOSFET taps is calculated from the transducer conversion efficiency taking into account the spreading loss. The calculated conversion efficiency of the taps is in the range of 40 to 45 dB under nominal operating conditions of a drain current per tap of 30 mA. By operating under higher drain currents the loss could be brought under 40 dB. Since good correlation properties were obtained at channel current densities in the 30 A/m range the detectors were generally not operated above this level.

The detection efficiency was a function of the drain current and was independent of the gate-voltage and drain voltage levels used to achieve a particular drain current level. The detection efficiency followed the drain current squared law as predicted by theoretical considerations.

The phases of individual taps under switched conditions was examined using the oscilloscope displayed waveforms. Figure 25 shows the switched phases of a single tap pair. This was taken on the thirty-first detector tap of the array to observe if there was any signal degradation due to the transit of the pulse through the other taps. The amplitude of the two taps is the same to within the measurement accuracy. The phase reversal of 180 degrees is clearly evident with a slight offset due to time synchronization.

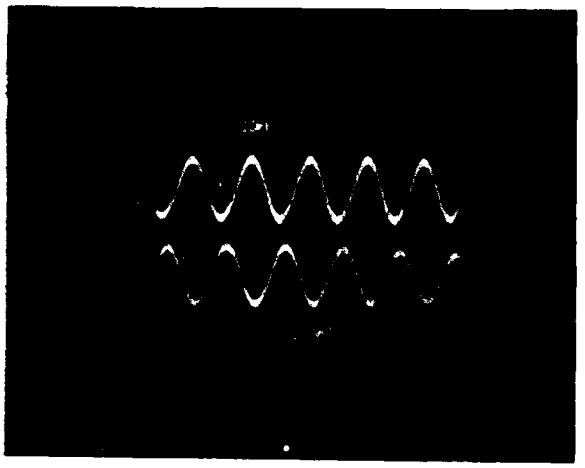


Figure 25. Switched Phase State of MOSFET Detector Tap

Figure 26 displays the detector output of two adjacent taps at positions 28 and 29 of the array. In the upper trace the taps are in phase and in the lower trace tap 29, output at the left, has been switched to its alternate phase. The switching has lowered the amplitude of the first few cycles immediately adjacent to the phase reversal but has not degraded the overall amplitude of the detector tap.

The amplitude control range of individual taps was measured and found to be over 20 dB for a current control from 3 mA to above 30 mA. The 3 mA current level gave a detected signal of approximately in the 5 to 10 mV range which was distinctly observable above the noise level of the system.

The preceding measurements were made on a pulsed basis and it was not necessary to be concerned about signal feedthrough levels. For the testing of the correlation properties it was necessary to make changes in the digital data and rf interface to isolate switching spikes and rf signals. This was accomplished with the result that the direct pulsed feedthrough from transducer input to MOSFET tap output was greater than 85 dB and the switching transients and low frequency signals were brought to the 5 mV level.

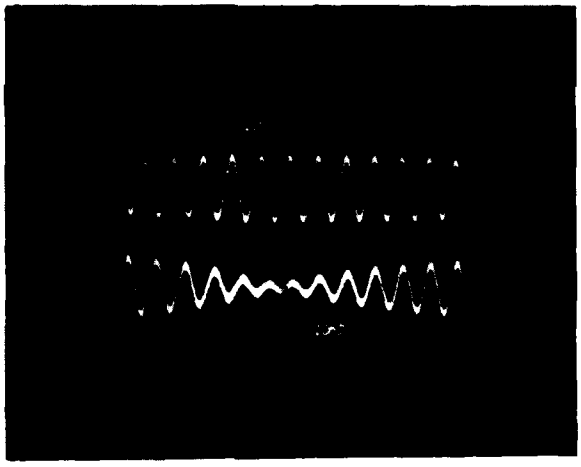


Figure 26. Switched Phase State Showing Phase Reversal of Adjacent Tap

4. CORRELATOR OPERATION

Two of the devices were operated as matched filter signal correlators. Selected 31 chip maximal length sequences were generated by the programmable test box and applied to the input transducer. The applied signal waveforms are shown in Figure 27. Figure 27(a) shows a 1 microsecond portion of the coded sequence and Figure 27(b) is an expanded time waveform showing the transitions between the 180 degree phase reversals.

Figures 28 and 29 show the correlated signal waveforms. In Figure 28 the 1 microsecond interval surrounding the correlation peak is shown. The correlation peak is seen to have excellent symmetry with null points at just beyond 200 ns in width. The spikes are from switching transits from the digital box which could not be completely eliminated. The average peak to sidelobe ratio is in the 13 to 15 dB range. Figure 34 is an expanded view of the correlation pulse showing the individual cycles. The correlated pulse has good uniform amplitude and frequency cycles. The null positions are 250 ns.

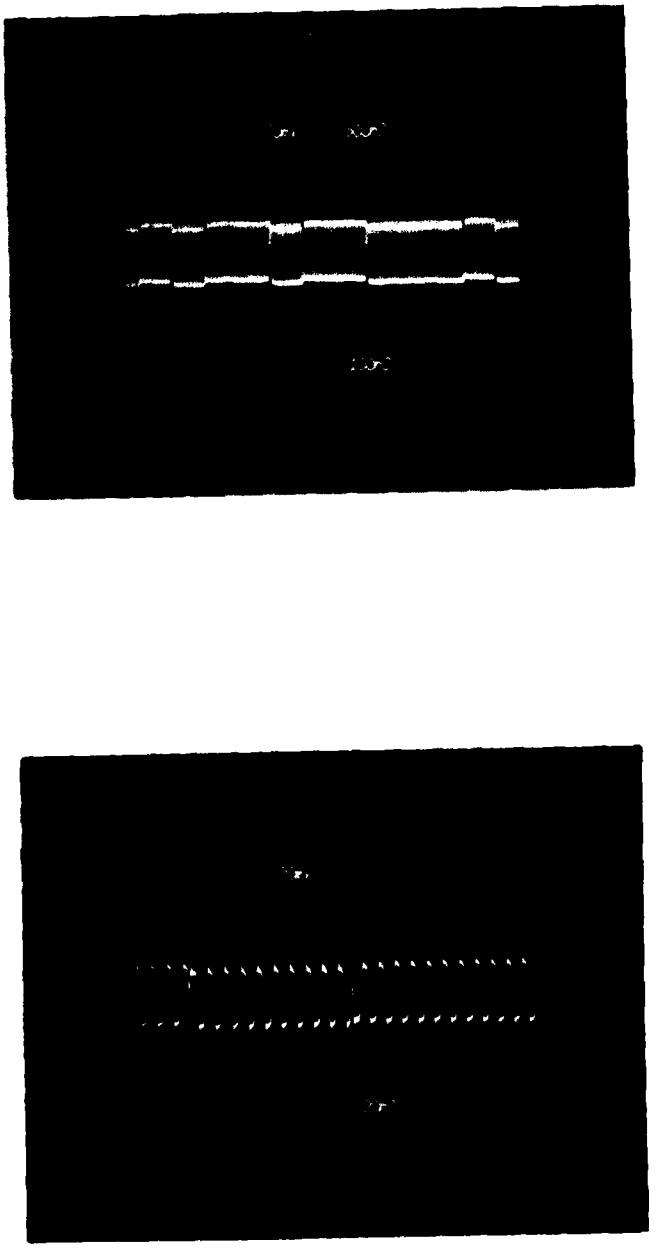


Figure 27. Coded Input Sequences to the Programmable Correlator

Figure 28. Correlation Waveform for a 31-Chip Bi-Phase Coded Sequence

Figure 29. Expanded View of Correlated Waveform

The second device had similar correlation properties with peak-to-sidelobe ratios in the 13 to 15 dB. Changes in phase and amplitude of individual chips could be used to degrade or improve the correlator properties. The frequency of operation was 100.1 MHz. Deviations from this frequency by 0.1 MHz resulted in a noticable skewing and amplitude reduction of the correlated peak.

The change in correlated peak amplitude with current was slightly less than square law. This may have been due to increased temperature and decreased channel conductance. The correlated signal was detectable from 5 millivolts to 200 millivolts, a range of greater than 30 dB.

To assess the capability of the device to correlate continuous code sequences at a rate of 3.1 μs, (the acoustic transit time), the device was tested by alternating between two different coded sequences. Figures 30 and 31 are oscilloscope photographs of the continuous correlation process. Figure 30 shows the continuous correlation over a 50 μs time interval and Figure 31 is an expanded view showing the autocorrelation spikes of the two codes. The device was readily programmed within the 3.1 μs interval and there was no degradation of correlator performance over that in which the codes were not alternated.

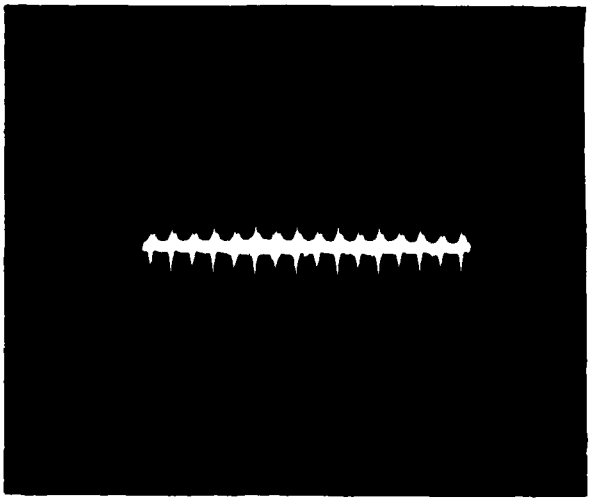


Figure 30. Continuous Correlation of Alternating Codes at 3.1 μs Intervals Using a Single Programmable Device

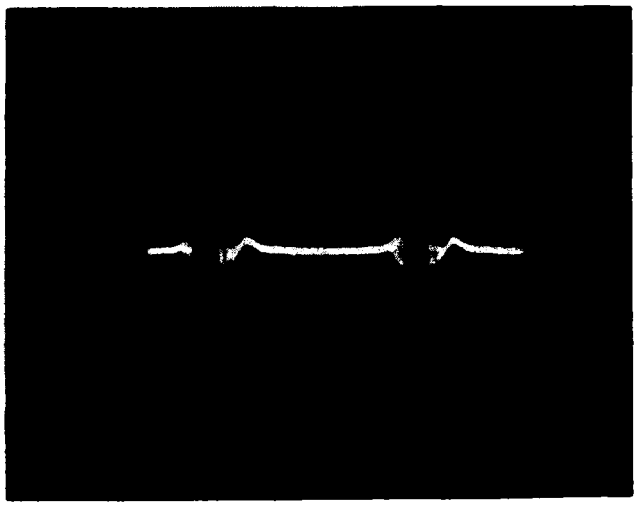


Figure 31. Expanded View of the Correlation of Alternating Codes

SECTION VIII

PERFORMANCE ANALYSIS

1. THIN FILM ZnO TRANSDUCERS

The thin film zinc oxide transducers had matched insertion loss values in the 12-15 dB region with a 3 dB bandwidth of 9 to 9.5 MHz. The number of interdigital finger pairs to achieve the desired 10 MHz bandwidth was calculated based upon the effects of velocity dispersion due to the zinc oxide and silicon dioxide layers. However it does appear that the number of pairs should be reduced from 8.5 to 7.5 to achieve the full 10 MHz bandwidth without Q spoiling.

The coupling factor for the films was calculated to be approximately 0.7% compared to a theoretical value of 0.8%. The improved coupling efficiency was attributed to improved deposition parameters and techniques as monitored by optical probing of the films. The coupling efficiency was reasonably uniform over the wafer area although the very best transducers were in the central area of the wafer.

2. MOSFET DETECTOR TAPS

The insertion loss for an individual tap under typical drain current operating conditions was in the 40 dB region. This is somewhat higher than the best conversion efficiencies of 35 dB obtained under the previous development. For an ideal MOSFET the predicted loss was 30 dB. The differences appear to come from the following sources. First, the measured channel conductance values were about 3 times higher than the values assumed in the original design calculations. Secondly, the shorter channel lengths as compared to the previous development, have increased the loss. Third, it appears that the capacitance on the detector tap network was higher and the output impedance match may not have been optimized. Finally, increased parasitic resistance would have contributed a small amount of dissipative loss because of the longer drain lines and thinner metallization.

The MOSFET taps had a low threshold (<1.0 V) and operated under a drain voltage condition of 8-10 volts. The signal output was a function of the tap current which followed the predicted square-law relationship.

The taps were operated at a 30 mA drain current level corresponding to a current density of 30 A/m. This is in line with the previous developments in which the taps were operated at current densities in the 20-30 A/m region. The saturation level of the detectors was above the 30 mA level. The power required per unit tap was in the 100 to 120 mW range.

The restructuring of the MOSFET tap topography to present a low profile to the traveling acoustic wave was effective in substantially reducing the amplitude droop across the detector array. A probe of the surface

contours showed a height differential of 8000 Å as compared to 20,000 Å on previous developments. A reflection coefficient per tap in the range of 0.022 to 0.028 was calculated from the pulse echo and transmission data. This gives an empirical relationship between the reflectivity and the discontinuity thickness to acoustic wavelength ratio of approximately $r = 1.5\ h/\lambda$. This agrees reasonably well with the calculated data from the previous development. It represents a useful tool in assessing the limitations of the technology in future developments.

3. LOGIC CONTROL CIRCUITRY

The tap logic circuitry performed the functions of switching tap phases and amplitude weighting in a very controlled and high speed manner. Arbitrary biphase sequences were used to encode the taps within a period of substantially less than 3 microseconds. The predicted time for setting and stabilizing was less than 2 microseconds. The circuitry was designed to have a capability for clocking in the phase information at a 20 MHz rate. There was no major interference effects observed between taps in switched states.

The analog voltage was used to control the tap amplitudes over a 20 dB range. This could be done in a continuously variable manner.

The code storage circuitry performed well permitting good isolation between the clocking of the next code and the setting of the detector taps.

The dc power required to operate the logic circuitry was approximately 0.2 watt.

4. CORRELATION PROPERTIES

The correlation properties of this device were the best observed in the three developments. The peak to sidelobe ratios were 15 dB. There was excellent amplitude symmetry and frequency clarity in the correlated peak. The direct feedthrough level was 80-90 dB and did not affect the correlation properties of the device. There was a better than 30 dB dynamic range for the correlated pulse. The phase coding and amplitude level of each chip could be set to adjust for the best correlation properties. Budget limitations focused the final testing on the demonstration of the basic correlation properties and did not permit the investigation of diverse codes or a comparison to theoretical properties.

5. COMPARISON WITH PREVIOUS DEVELOPMENTS

Table 5 presents a comparison of the correlator properties with the previous technology developments. Various performance aspects have already been discussed in the foregoing paragraphs and the Table is self explanatory. A comment can be made regarding potential yield.

It was only possible to estimate the device yield from the manual probe measurements and visual selection. The fact that there was only one pass for design and fabrication and that working devices were picked by visual inspection indicates that there should be a good yield. The probe measurements indicated that at least half of the devices tested performed the basic functions. It is estimated that the yield is at least as good as the previous development and could possibly be higher. The semiconductor processes were standard and the zinc oxide technology is reaching a state of maturity where it may also be considered a standard process.

TABLE 5. COMPARISON OF SAW CORRELATOR TECHNOLOGIES

PARAMETER	TECHNOLOGY		
ZnO Transducer	THICK FILM	THIN FILM	THIN FILM
Matched Loss	15 dB	15 dB	12-15 dB
Bandwidth	9.5 MHz	9 MHz	9 MHz
k^2 Coupling	0.74%	0.6%	0.7%
MOSFET Tap	MGPMOS	MGNMOS	SGNMOS
Loss/Tap	40 dB	35-40 dB	40
Gate Threshold	2-2.5 V	1.0-1.25 V	1.0 V
Drain Voltage	6-8 V	8-10 V	8-10 V
Tap Current Density	20-25 A/m	20-30 A/m	30 A/m
Saturation	>20 mA	>30 mA	>30 mA
Power/Tap	60-100 mW	64-160 mW	100-120 mW
Control Circuitry	ROM	BBD-DSR	ANALOG-SR
Code	Fixed	Arbitrary	Arbitrary
Speed	3 μs	50 μs	3 μs
Phase Control	Good	Fair	Good
Amplitude Control	None	~10 dB	>20 dB
Device Parameters	PMOS	NMOS	CMOS
Impulse Loss	78-80 dE	75-80 dB	75-85 dB
Loss to Peak	44 dB	Not Determined	45 dB
Peak to Side Lobe	12 dB	Not Determined	13-15 dB
Feed Through	70 dB	80-90 dB	80-90 dB
Signal to Noise	20 dB	20 dB	>30 dB
Amplitude Droop	8 dB	10 dB	3 dB
Power	3.2 W	3.5 W	3.5 W
YIELD	20%	40-50%	est.40-50%

SECTION IX

CONCLUSIONS AND RECOMMENDATIONS

A monolithic surface acoustic wave programmable matched filter signal processor with tap phase and amplitude control was developed on silicon using piezoelectric film transducer and semiconductor MOSFET technologies. This development is significant in providing a versatile signal processing chip for use in spread spectrum communications. There are several unique features which set this development apart from other programmable matched filter developments. It is truly monolithic, using a silicon substrate upon which the MOSFET detecting structures and control circuitry are semiconductor processed and the zinc oxide transducer structures are developed. Film metalization interconnects are used throughout. The use of gate voltage controlled MOSFET taps for code phasing and amplitude weighting eliminates the necessity for complex hybrid switching structures which require a substantial number of bond interconnections. The zinc oxide film transducers permit a wideband signal to be generated with relatively low loss. The bandwidth characteristic of the MOSFET detectors is extremely broad, and detection efficiency increases with increasing frequency. The reliability and reproducibility of the device, which uses standard MOSFET processing, is good and the potential cost in high volume will be substantially better than hybrid or more fabricationally complex epitaxial structures. The temperature coefficient of delay should be reasonably good because of the relatively low negative coefficients of zinc oxide and silicon, and the postive coefficient of SiO_2. Compared to digital electronic technology, it represents a simpler device structure. It presently requires somewhat higher power per bit than electronic counterparts but offers the advantages of operating directly at rf frequencies.

The overall performance of the ZnO/Si-MOSFET programmable correlator devices developed under this program is considered extremely encouraging. The MOSFET tap generated and detected waveforms are clean and phase reversals are distinct. Autocorrelated waveforms approach theoretical values. A high degree of rf tap-to-tap isolation was achieved. The rate of coded data flow permitted continuous correlation in a single device. Signal degradation problems connected with tap topography have been minimized. There is a good dynamic range over which tap amplitude may be adjusted to enhance correlation capabilities.

Increasing the device efficiency is the major area of concern for future development. There is room for improved zinc oxide transduction efficiency by using the thick film mode. The MOSFET conversion efficiency could be improved through the use of a higher concentration of acoustic power in the channel region. This would help reduce the amount of drain current required to obtain usable signal levels. The use of piezoelectric gate oxides appears to be a viable approach for significantly reducing the conversion loss at the piezoresistive MOSFET taps.[11]

From a systems point of view, the programmable correlator provides a modest time-bandwidth device. Time-bandwidth products of approximately 100 (20 MHz bandwidth, 5 μsec delay) appear feasible. The potential low-cost of the device makes it attractive for expendable missions. Several devices operating at different frequencies permits frequency hopping strategies to be developed. The programmable correlator was demonstrated to be compatible with digital logic interfaces.

SECTION X

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