

AD-A088 237

ROCKWELL INTERNATIONAL THOUSAND OAKS CA ELECTRONICS--ETC F/G 14/2
HIGH-CONTRAST ELECTROLUMINESCENT READOUT DEVICE. (U)

AUG 80 M K KILCOYNE

DAAB07-78-C-2996

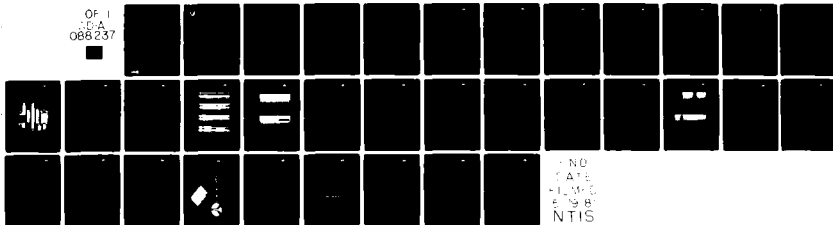
UNCLASSIFIED

ERC41016.9IRF

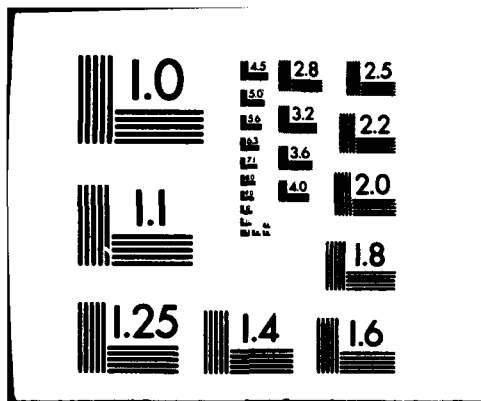
DELET-TR-78-2996-1

NL

OF 1
DIA
088237



NO
DATE
FILMED
SERIAL
NTIS

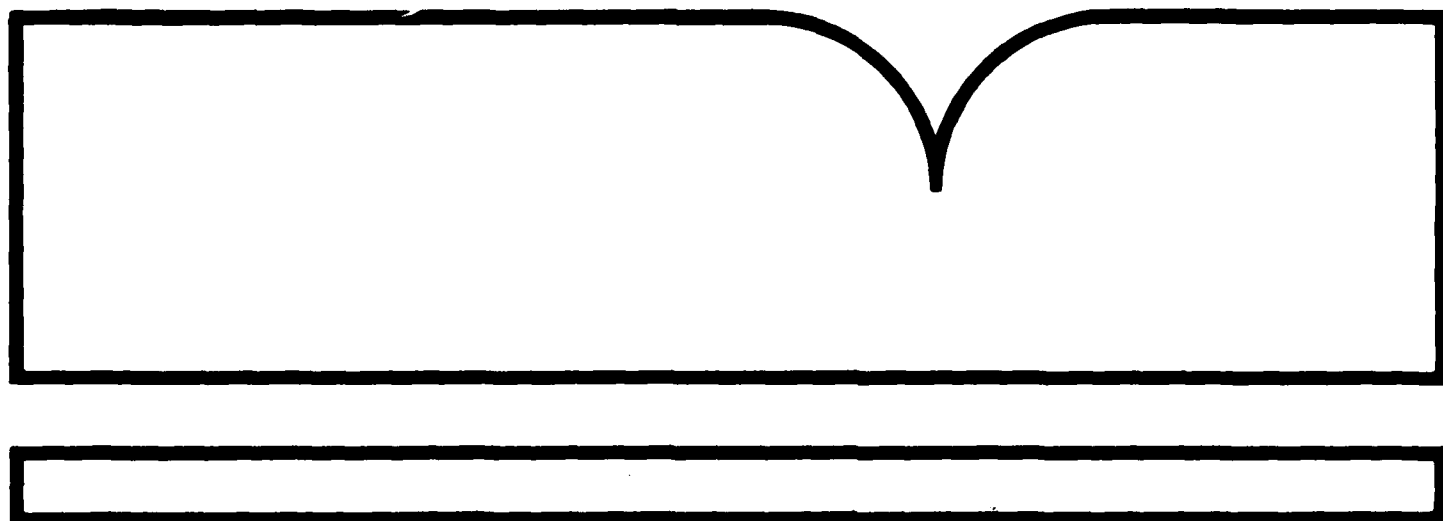


High-Contrast Electroluminescent Readout Device

M. K. Kilcoyne

Rockwell International
Thousand Oaks, California

August 1980





Research and Development Technical Report

DELET-TR-78-2996-1

AD A088237

HIGH-CONTRAST ELECTROLUMINESCENT READOUT DEVICE

**M. K. Kilcoyne
ROCKWELL INTERNATIONAL
Thousand Oaks, CA 91360**

August 1980

First Interim Report for Period 2 Oct. 78 - 31 Jan. 79

DISTRIBUTION STATEMENT

Approved for public release; distribution unlimited.

**Prepared for:
ELECTRONICS TECHNOLOGY & DEVICES LABORATORY**

ERADCOM

**US ARMY ELECTRONICS RESEARCH AND DEVELOPMENT COMMAND
FORT MONMOUTH, NEW JERSEY 07703**

**REPRODUCED BY
NATIONAL TECHNICAL
INFORMATION SERVICE
U.S. DEPARTMENT OF COMMERCE
SPRINGFIELD, VA. 22161**

HLSA-FM 195-78

NOTICES

Disclaimers

The citation of trade names and names of manufacturers in this report is not to be construed as official Government indorsement or approval of commercial products or services referenced herein.

Disposition

Destroy this report when it is no longer needed. Do not return it to the originator.

NOTICE

THIS DOCUMENT HAS BEEN REPRODUCED FROM THE BEST COPY FURNISHED US BY THE SPONSORING AGENCY. ALTHOUGH IT IS RECOGNIZED THAT CERTAIN PORTIONS ARE ILLEGIBLE, IT IS BEING RELEASED IN THE INTEREST OF MAKING AVAILABLE AS MUCH INFORMATION AS POSSIBLE.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER DELET-TR-78-2996-1	2. GOVT ACCESSION NO. AD-A088237	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) HIGH-CONTRAST ELECTROLUMINESCENT READOUT DEVICE		5. TYPE OF REPORT & PERIOD COVERED Interim Technical Report 2 Oct 1978 thru 31 Jan 1979
7. AUTHOR(s) M. K. Kilcoyne		6. PERFORMING ORG. REPORT NUMBER ERC41016.9IRF
9. PERFORMING ORGANIZATION NAME AND ADDRESS Science Center Rockwell International Thousand Oaks, California 91360		8. CONTRACT OR GRANT NUMBER(s) DAAB07-78-C-2996
11. CONTROLLING OFFICE NAME AND ADDRESS Electronic Technology & Devices Laboratory ATTN: DELET-BD, Fort Monmouth, NJ 07703		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 62705A ILI62705AH94 03 DIIC8
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		12. REPORT DATE August, 1980
		13. NUMBER OF PAGES 32
		15. SECURITY CLASS. (of this report) Unclassified
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE
16. DISTRIBUTION STATEMENT (of this Report) Approved for public release; distribution unlimited		
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)		
18. SUPPLEMENTARY NOTES		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) Thin film High-contrast Numeric Display		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) The Rockwell Science Center has completed the first phase of the development program encompassing the design, fabrication and characterization of experimental models of a high-contrast numeric electroluminescent readout device. This device consists of two digits of seven-segment numeric displays using a transparent electroluminescent thin film with a high-contrast background layer. It contains within its hermetically-sealed package logic and drive circuitry to operate the numeric displays from typical computer output data processing information, with typical 5-volt T ² L logic-level and BCD input.		

DD FORM 1473 EDITION OF 1 NOV 68 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)



TABLE OF CONTENTS

	<u>Page</u>
1. SUMMARY	1
2. PROGRAM AIMS AND OBJECTIVES	2
3. DECODER-DRIVER CIRCUIT DESIGN	3
4. PROTOTYPE TEST AND ANALYSIS	8
5. HIGH-CONTRAST DISPLAY PERFORMANCE	12
6. HERMETIC SEAL DESIGN AND FABRICATION	19
APPENDIX A	24



LIST OF FIGURES

	<u>Page</u>
Fig. 1 Master Logic Chip Circuit	4
Fig. 2 Prototype Breadboard.	6
Fig. 3 Brightness vs Voltage	9
Fig. 4 Luminous Efficiency vs Voltage.	10
Fig. 5 Reflectance of EL Structures.	13
Fig. 6 Contrast vs Ambient Illumination.	17
Fig. 7 Package Design.	20
Fig. 8 Prototype Photograph	23
Fig. 9 Specular Reflection Components	25



1. SUMMARY

The Rockwell Science Center has completed the first phase of the development program encompassing the design, fabrication and characterization of experimental models of a high-contrast numeric electroluminescent readout device. This device consists of two digits of seven-segment numeric displays using a transparent electroluminescent thin film with a high-contrast background layer. It also contains within its hermetically-sealed package logic and drive circuitry to operate the numeric displays from typical computer output data processing information, with typical 5-volt T²L logic-level and BCD input. The package design also allows the devices to be embodied so that a multi-digit computer-type terminal readout may be fabricated from a series of individual packages.

This report covers the work completed during the first four months of effort. During this period, the design of driver and decode electronics has been completed, various high-contrast electroluminescent segment displays have been built, tested and evaluated. A breadboard circuit to evaluate the initial driver and decoder electronic circuit design parameters has been constructed and tested. Designs for hermetically-sealed packages have been completed, parts ordered, and initial seals evaluated. Electrical and optical tests have been conducted on initial prototypes using breadboard drive circuitry. Evaluation and analysis of these results are given. An evaluation in testing high-contrast performances of these prototype models is reviewed.



2. PROGRAM AIMS AND OBJECTIVES

The objective of this program is to design and fabricate a quantity of numeric EL display devices containing two-digits consisting of seven segments and a decimal point. Four (4) exploratory development models will be fabricated each consisting of a ten-digit display made up of five of the two-digit numeric devices assembled into a suitable socket or printed circuitboard. Drive circuitry and decoding logic will be included in the device to allow operation directly from computer level logic inputs at TTL voltage levels. The display medium shall be a transparent AC thin film electroluminescent type with a high-contrast background layer for viewing in high-light ambience. The operational characteristics of the devices shall be designed to allow uniform electronic dimming of the display to luminance levels in the order of the 10^{-3} ft-L for compatibility with night vision applications. The display shall be capable of sufficient contrast to be viewed in an ambient illumination of 10,000 ft-C without additional contrast enhancement techniques. The devices shall be capable of operation for a minimum of 3,000 hours at a luminance level that satisfies the condition of visibility under high-ambient illumination described above. Also, the devices shall operate without the loss of significant light emitting areas due to any failure or degradation mechanism during the 3,000 hour/lifetime.



3. DECODER-DRIVER CIRCUIT DESIGN

The design for the onboard decoder-driver circuit has been completed, tested and evaluated. Figure 1 shows a schematic diagram for the onboard decoder driver circuit to be utilized in the two-digit thin film EL display. The pinouts for the circuit are shown at the left of the circuit diagram. The circuit consists of all of the necessary logic building blocks for decode and drive from T^2L BCD input signals.

The functions consists basically as follows: A 5 kHz clock is used to generate the drive frequency for the AC operation of the TFEL display. The circuit uses a specialized latched seven-segment decoder/driver signal circuit that provides level shifting functions on the chip. This feature permits the BCD input signal swings to be the same as or different from the seven-segment output signal swings.

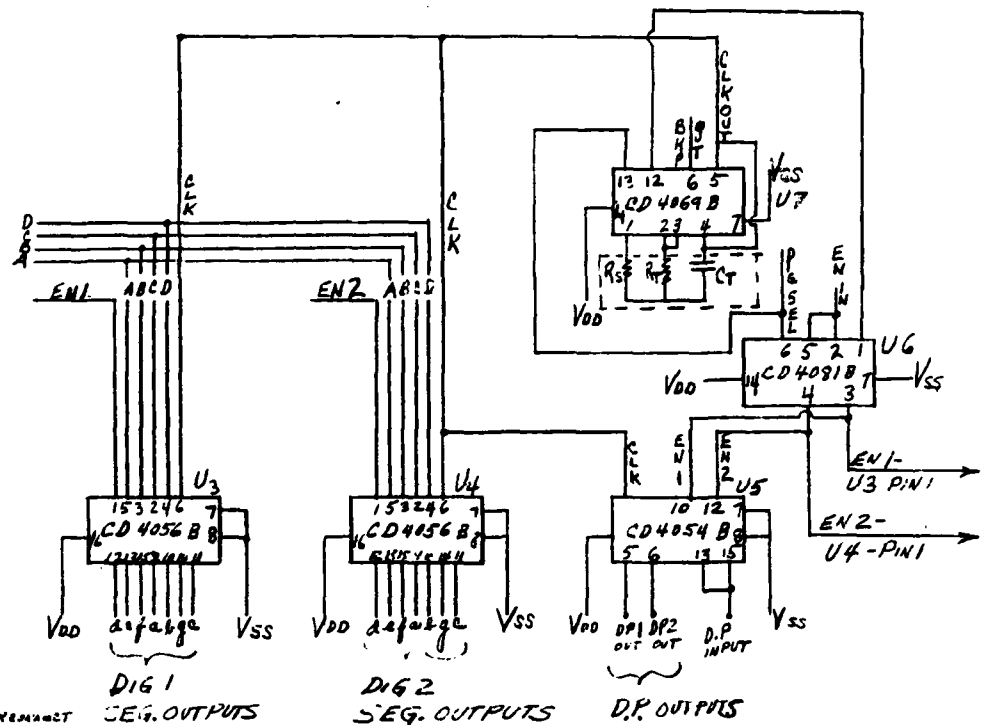
The seven-segment output signals are toggled by the display frequency input which causes the selected segment outputs to be a square wave at the clock input frequency. With the clock frequency square wave present, the selected segments will have a square wave output that is 180° out of phase with the display frequency input. Those segments which are not selected will have a square wave output that is in-phase with the input.

The display frequency input square wave is required to provide equivalent AC drive to electroluminescent displays. It should be noted that unselected segments are driven exactly in-phase with the backplane potential resulting in no potential difference on undriven segments, and no DC offsets which might be associated with undesirable polarization within the thin film EL material.



- INPUTS**
- 1 □ A - BCD1
 - 2 □ B BCD2
 - 3 □ C BCD3
 - 4 □ D BCD4
 - 5 □ ENABLE
 - 6 □ DIG. SEL.
 - 7 □ VDD
 - 8 □ N.C.
 - 9 □ VSS-GND.
 - 10 □ DEC. POINT

- OUTPUTS**
- DIG 1-SEG. 2-9 + D.P.
 - DIG 2-SEG. 7-9 + D.P.
 - BACKPLANE DRIVER
 - CLOCK OUT U7-4,5
 - U7-3 (RT)
 - U7-1 (RS)
- INTERCONNECT TO EXTERNAL R'S & C



ROCKWELL SCIENCE CENTER
 TFEL 2 DIGIT DISPLAY
 MASTER LOGIC CIRCUIT
 DRAWN MKK-3-27-79 CHK'D _____
 DWG. NO. 022 SK1012 REV. N.U.

NOT REPRODUCIBLE

Figure 1



Decoding all the input combinations in the logic provides displays of 0 to 9 as well as L, P, H, A, -, and a blank position. The decimal point drive has a display frequency control circuit similar to the segment drives.

The output signals from the display logic are fed directly into the input signal stage of the high-voltage driver circuits. In the original proposal (reference Proposal No. SC3009T) a Dionics DI702 high-voltage driver array chip was proposed for the driver. However, test driver arrays provided by Dionics did not meet the voltage requirements of the display. Therefore, a discrete transistor driver arrays were used in the prototype evaluation. The discrete circuits were essentially identical to the backplane driver circuit utilizing MPSA92 (PNP) and MPS-A42 (NPN) high-voltage driver transistors.

Currently other driver stage circuits are being evaluated using off-the-shelf high-voltage (250V) bipolar transistor arrays as a replacement for the DI702 driver array in order that the driver chips will fit into the hybrid package.

Figure 2 shows the photograph of a prototype breadboard utilized to evaluate the display decoder driver circuit design. This breadboard consisted of a high-contrast, two-digit EL numeric display driven by the driver circuitry described above. In addition to the basic onboard driver circuit, some additional ICs were used to generate counter signals for the BCD inputs as well as digit select and decimal point functions. Our tests and evaluations of this breadboard under dynamic driving conditions

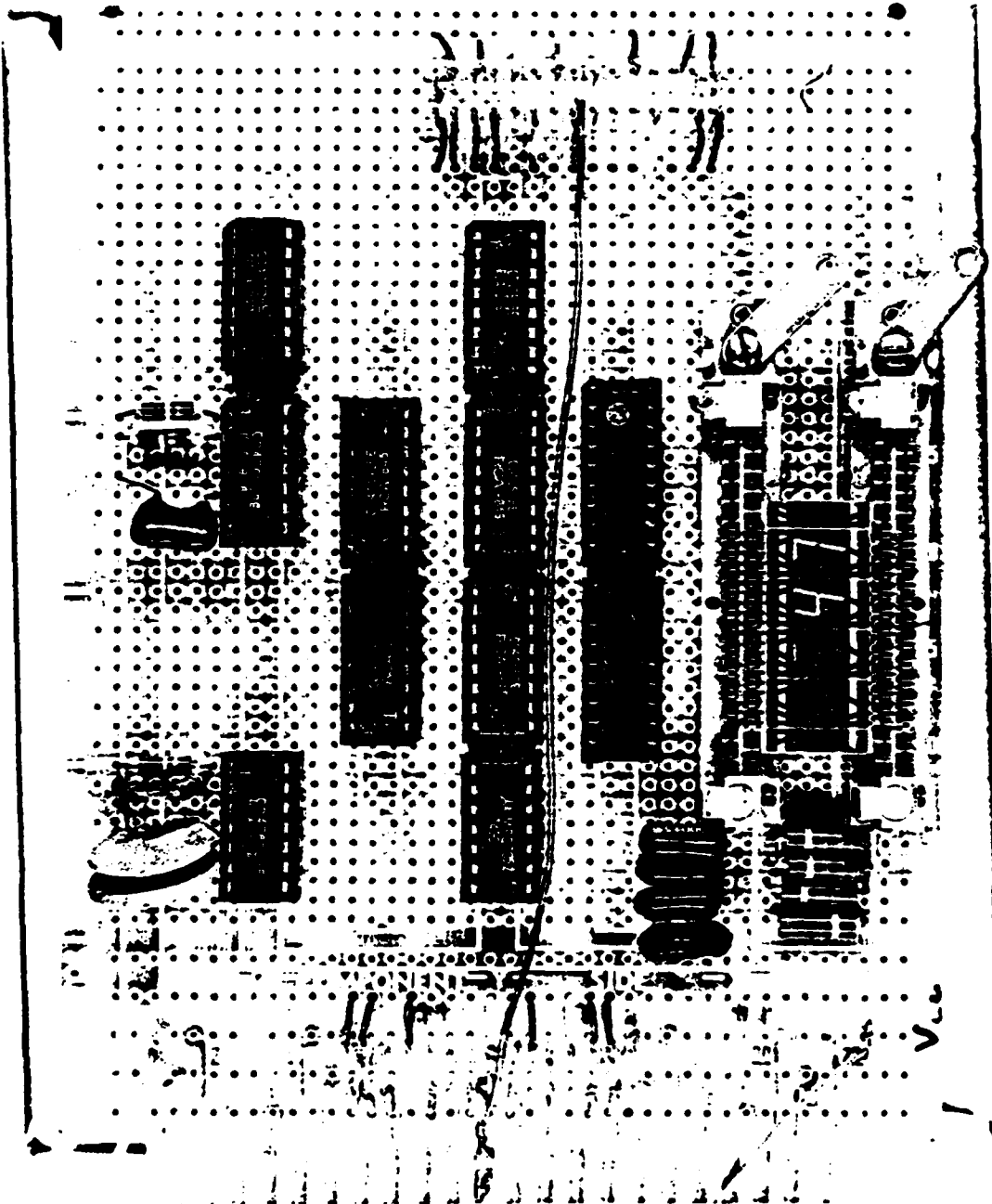


Figure 2

NOT REPRODUCIBLE



with conventional T²L BCD input levels, have shown the circuit to function exactly as required. Accordingly, work has begun on the layout of the semi-custom master logic chip in a CMOS design format. Because of the uncertainty of the final driver chip configuration, the semi-custom master logic chip will have a wire bonding option allowing phase reversal to the backplane driver depending on whether or not a phase reversal exists on the final chips selected for the high-voltage driver configuration.

The custom logic ship is expected to be delivered in the latter part of June, 1979.



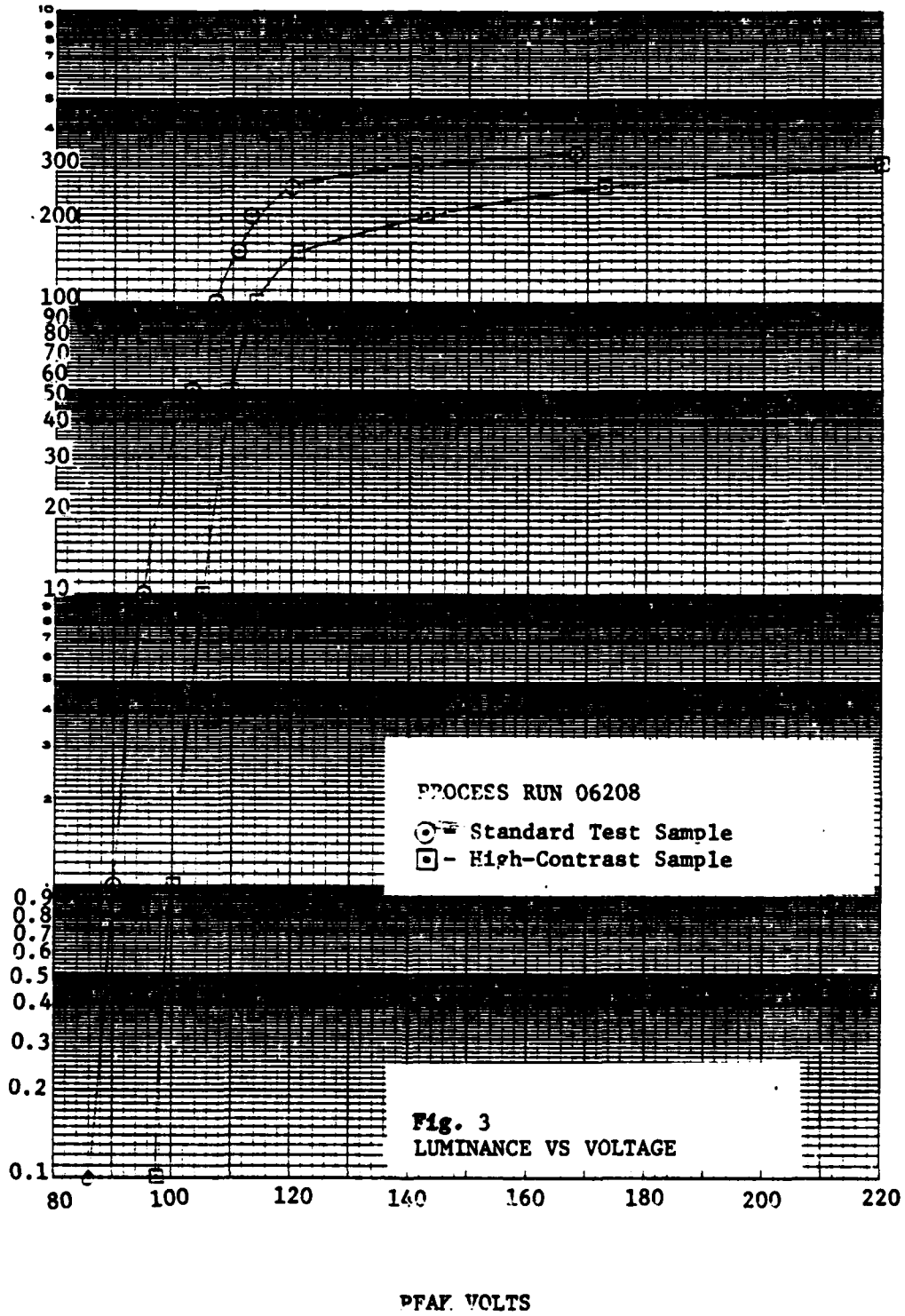
4. PROTOTYPE TEST AND ANALYSIS

Figure 3 shows the brightness vs voltage characteristics for samples built with and without the standard high-contrast layer. From the curves it can be seen that the devices without high-contrast layers have a threshold voltage of approximately 80 volts and a peak brightness of 325 ft-L. High-contrast devices from the same EL processing run had threshold voltages of 100 volts and a peak brightness of 300 ft-L. By operating these devices at 200 ft-L, the voltage safety factor is a conservative 50% over voltage rating. Devices operated in this way have little concern with high-voltage breakdown or failures even during long operating lifetime. With a threshold voltage of 100 volts, no effective light output is observed below this level. This high threshold voltage level makes the segmented displays virtually immune from stray light emission from adjacent unlighted segments. The stray fields are far below the level that would give rise to any emission because of the high threshold voltage level.

Figure 4 shows a plot of luminous efficiency vs excitation voltage for a standard film and a high-contrast film. Because of the additional layer, the high-contrast film requires a greater excitation voltage for the same brightness. The operating currents are lower, however, for the same fields in this film resulting in approximately equal luminous efficiencies. The curve shows that for lower voltages high-contrast film equaled or exceeded the performance of the standard film, and only near saturation did the luminous efficiency fall somewhat below that of the standard film. Even in this region, the high-contrast film had luminous output efficiencies of approximately 90% of those of the standard film without a high-contrast



DISPLAY LUMINANCE - FT-L



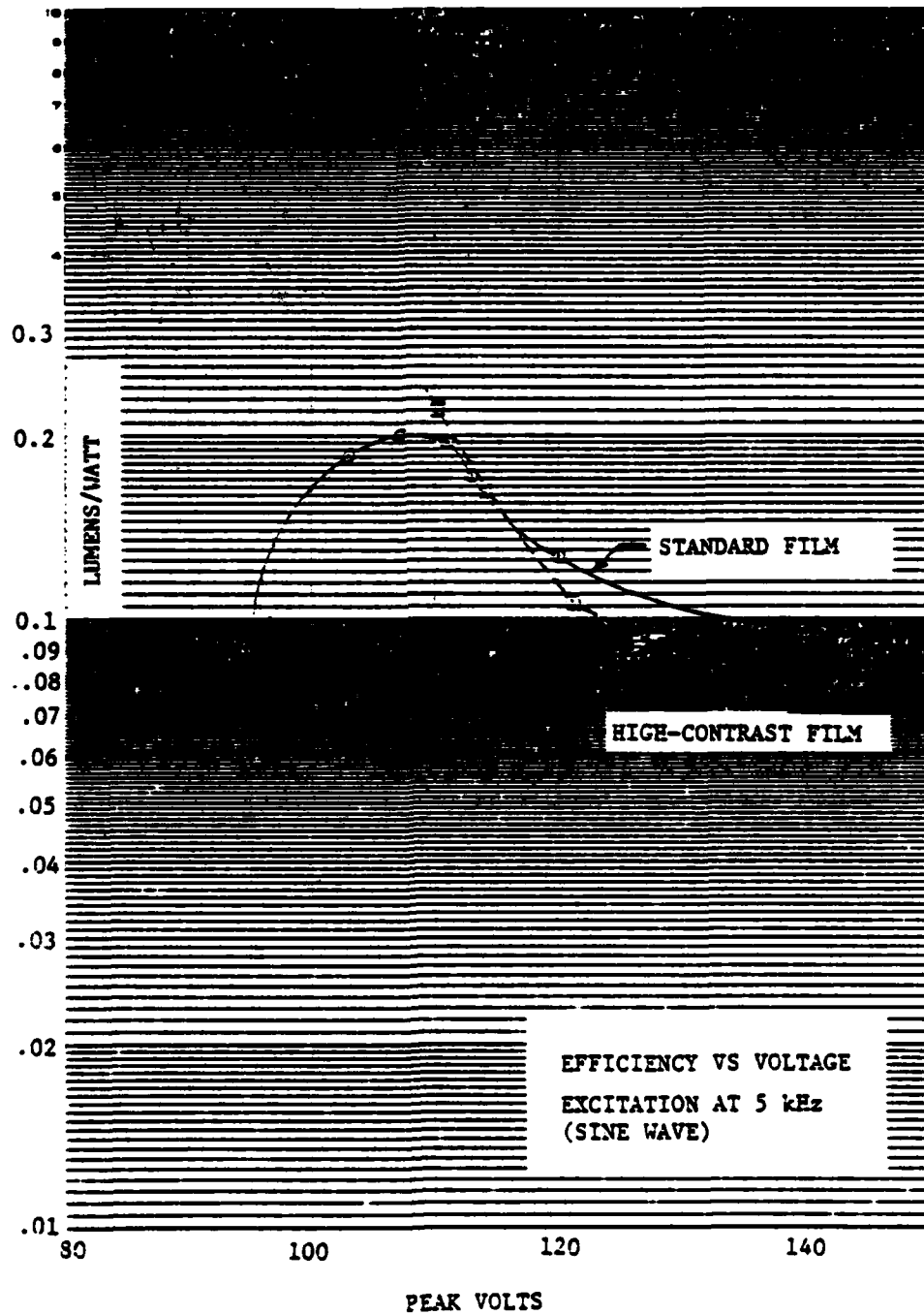


Figure 4



Rockwell International

ERC41016.9IRF

layer. While peak efficiencies as high as 0.5 ℓ/w have been observed in some films, these efficiencies have not been achieved yet in a high-contrast numeric format. As shown by the curves, typical operating efficiencies for this particular phosphor run approximately 100 ml/w.



5. HIGH-CONTRAST DISPLAY PERFORMANCE

Figure 5 shows the multi-layer structure of the Rockwell high-contrast EL display. A major objective of this contractual effort is the achievement of a display which is viewable in a 10,000 ft-C ambient light level condition. Based on inputs from potential avionics users of this display (Collins Radio/Cedar Rapids) and reports in the literature, it appears that a minimum of 200 ft-L output from the display device is necessary in a high-contrast structure so that the eye can easily accommodate to high-intensity ambient in the far scene as well as viewing the instrument panel under the direct sunlight. Therefore, a 10,000 ft-C diffuse ambient is more typical than a 10,000 ft-C parallel flux condition. Carroll¹ describes the condition as a 10,000 ft-L ambient rather than a 10,000 ft-C since the flux is diffuse. In this case, specular reflections are very important.

Measurements and theory indicate the major sources of reflection are the front-surface air-to-glass interface, the substrate-glass-to-InO interface, and the ZnS-to-Y₂O₃. The Y₂O₃-to-black-layer interface has been measured and is small with respect to the above factors. The front surface of the display can be coated with a multi-layer low-reflectance dielectric coating resulting in an effective front-surface reflection approximately 0.25%. The InO-to-glass interface reflection is due to the refractive index mismatch between the glass (n = 1.53) and the InO (n = 2.0). Experimentally, an optimum InO thickness can be observed for minimum reflection in the active area.

¹G. Carroll, "Contrast Enhancement of CRT Displays," Digest of SID International Symposium, pp. 118-119 (1977).

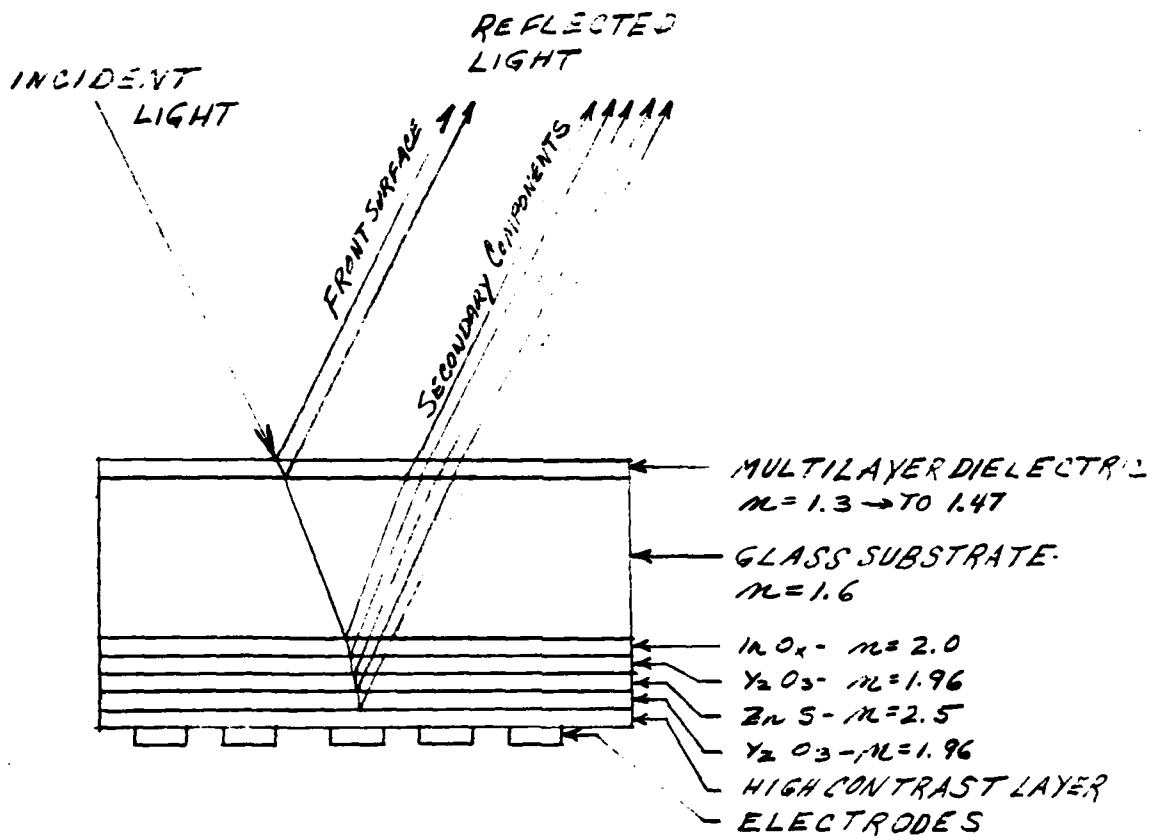


Figure 5



At near normal incidence, an expression for the reflection at the interface between two media can be given as follows:

$$\rho = (n_2 - n_1/n_2 + n_1)^2$$

where n_1 equals the index of refraction in the first medium and n_2 the index of refraction in the second medium. Using this expression, one can look empirically and mathematically at the contributions of the various interfaces toward the total reflected light. As mentioned above, light reflection for suitably-coated glass substrates with an anti-reflecting multi-layer dielectric is typically 0.25%. The remaining reflected light components can be summarized as follows:

Glass-to-indium interface:	$\rho = 1.77\%$
InO-to- Y_2O_3 interface:	$\rho = 0.0\%$
Y_2O_3 -to-ZnS interface:	$\rho = 0.83\%$
ZnS-to- Y_2O_3 interface:	$\rho = 0.83\%$
Y_2O_3 -to-high-contrast layer:	$\rho = .02\%$

As described in the proposal (reference Proposal No. SC3009T), black conductor materials have been developed at the Science Center which exhibit a diffuse reflectivity of less than 0.7% (recent materials show 0.06% diffuse reflectivity). While these materials will satisfy the viewability requirement of this contract under the specified 10,000 ft-C ambient, a continuous black blocking such as possible with a black dielectric would provide superior display performance. Therefore, work is continuing under Rockwell IR&D funding on a dielectric black material. The



requirements of the dielectric black backing are as follows:

1. Optical match of index of refraction with the emitter material,
2. Pinhole failure mode,
3. Adequate lateral resistance to avoid lighting adjacent electrode areas,
4. High-optical absorption coefficient,
5. Electrical match to emitter in order to provide symmetrical voltage-current and voltage-brightness characteristics as a function of voltage polarity on the emitter as required for long-life characteristics.

Thus far all these requirements have not been met by one material.

At this time work has been concentrated on the black layer properties; the individual emitter thin film thickness (InO , Y_2O_3 , ZnS) has not been optimized in terms of interference cancellation of internal reflections. Present displays show a 2.5% reflection due to the internal film structure. Interference cancellation is required to reduce the specular reflection as described above. Based on experimental measurements of some low brightness emitters, it appears that a specular reflection as low as 0.5% can be achieved through film thickness optimization.

An expression for exact cancellation of the multi-layer reflections is derived in Appendix A. For a reasonable film thickness based on voltage and brightness requirements of the emitter, a minimum specular reflection (<0.1%) for normal incidence light peaked at 5800\AA (peak emission wavelength for the emitter) results for a ZnS thickness of 3940\AA and a combined $\text{ITO} + \text{Y}_2\text{O}_3$ thickness of 2348\AA . Since the index of refraction of each



layer can be influenced somewhat by the fabrication technique, experimental verification of these calculated values are planned for the coming period.

Figure 6 shows contrast vs ambient illumination for presently-constructed EL displays and also shows an estimated curve for an optimized high-contrast emitter assuming a 0.5% internal reflection and 0.25% front surface reflection. In these curves contrast is defined as $(B + R_T)/(R_T + R_{int})$ where the values are defined as follows:

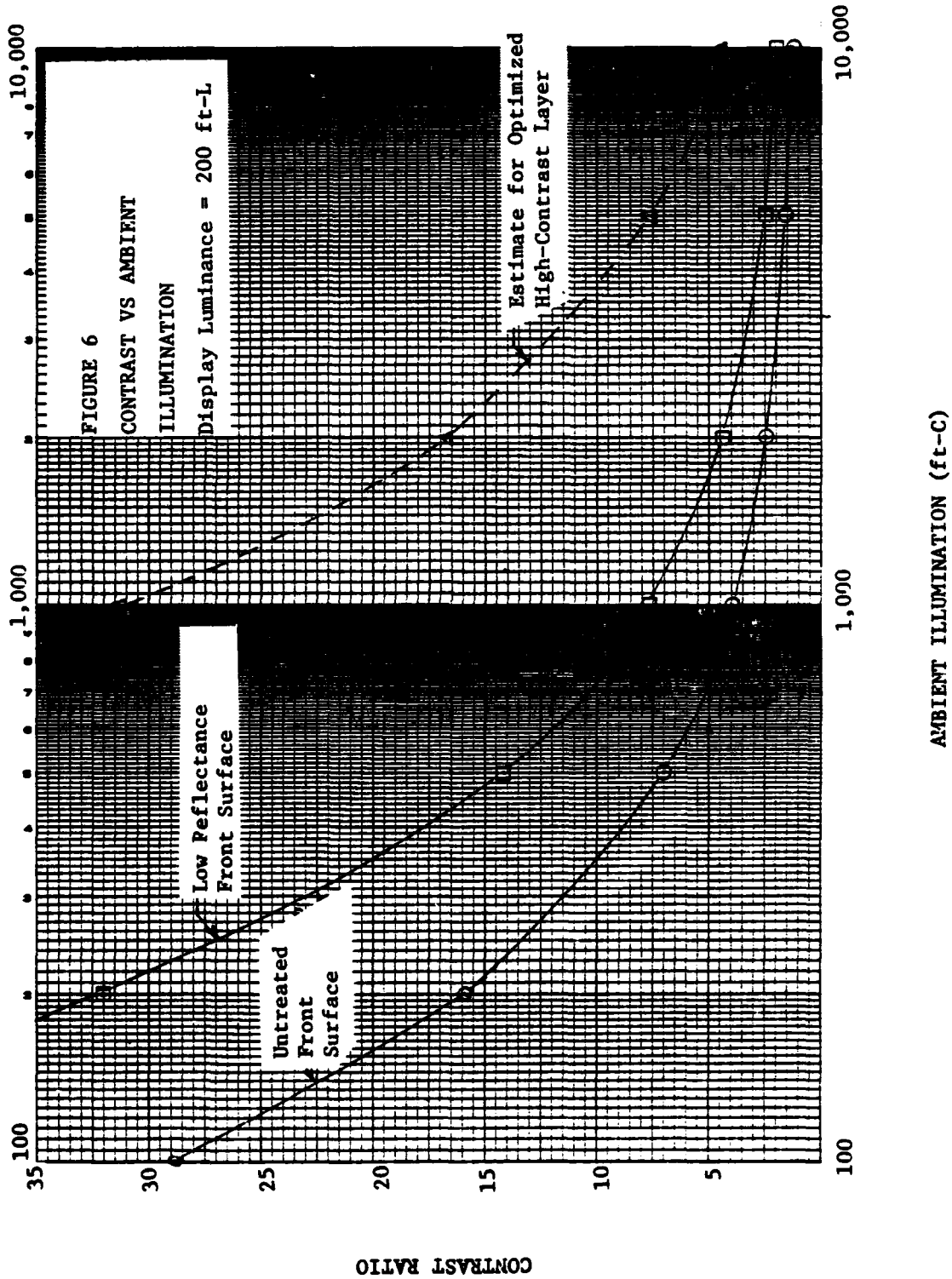
B = measured display luminance in ft-L

R_T = total effective reflectance

$R_{internal}$ = internally reflected luminance at an unexcited segment.

As can be seen from the figure, even displays with untreated surfaces have relatively high contrasts at illumination levels below 500 ft-C. Our present displays with a low reflectance front surface coating have reasonable contrasts up to 2,000 ft-C. The optimized display shown in the dotted curve is expected to have good contrast up to 10,000 ft-C with a limiting contrast of 7.5 at 5,000 ft-C ambient, and 4.3:1 at 10,000 ft-C ambient.

Figures in contrast curves as plotted are sometimes deceiving. Despite the fact that our untreated front surface displays measured relatively low contrast, they were still easily discernible under 10,000 ft-C by the human eye. Part of this is explained by the fact that the emission spectrum of the EL material is concentrated at 5800Å in the peak visibility area of the human eye. Whereas the ambient illumination had a relatively broad spectrum from a tungsten source at 3200°K. Thus, the EL emission had a distinct yellow color where the ambient light level was a broad white spectrum.





Rockwell International

ERC41016.9IRF

Since we are presently able to easily see displays even with untreated front surfaces, and displays which have been fabricated with a low reflectance front surface appear even more visible, the expected contrast performance from the optimized high-contrast layer described above should be adequate to meet the 10,000 ft-C ambient visibility requirements for the Army applications anticipated.



6. HERMETIC SEAL DESIGN AND FABRICATION

The package design for the two-digit electroluminescent display with on-board decoder-driver electronics is shown in Fig. 7. The package consists basically of a Corning 7059 borosilicate glass substrate on which the EL display thin films and high-contrast layers plus backing electrodes are deposited. This glass substrate is brazed by means of a low temperature metal seal to a ceramic assembly containing the on-board decoder-driver circuitry. This package represents a unique approach in packaging design. This approach is required since the display including all of the thin film EL layers are contained directly on the top glass substrate which is also the front surface window of the display. The drive circuitry, on the other hand, is contained on the lower ceramic substrate and vertical interconnections are required to connect the drive circuitry output voltages to the display segments and common backplane in the EL thin film display.

Thus, the seal area is first prepared on the display surface by metalization prior to the phosphor fabrication. After the phosphor deposition, the rear ceramic cover containing the drive electronics is sealed to the display surface using a low temperature (280°C) metal braze so that minimum heating of the completed phosphor film is required.

The drive circuitry is applied to the ceramic substrate as follows:

1. Screen circuit conductor pattern on ceramic substrate
2. Screen Frit-seal pattern on ceramic sidewall preform
3. Fire both ceramic substrate and ceramic sidewall in conveyor furnace at 850°C to cure PtAu conductors

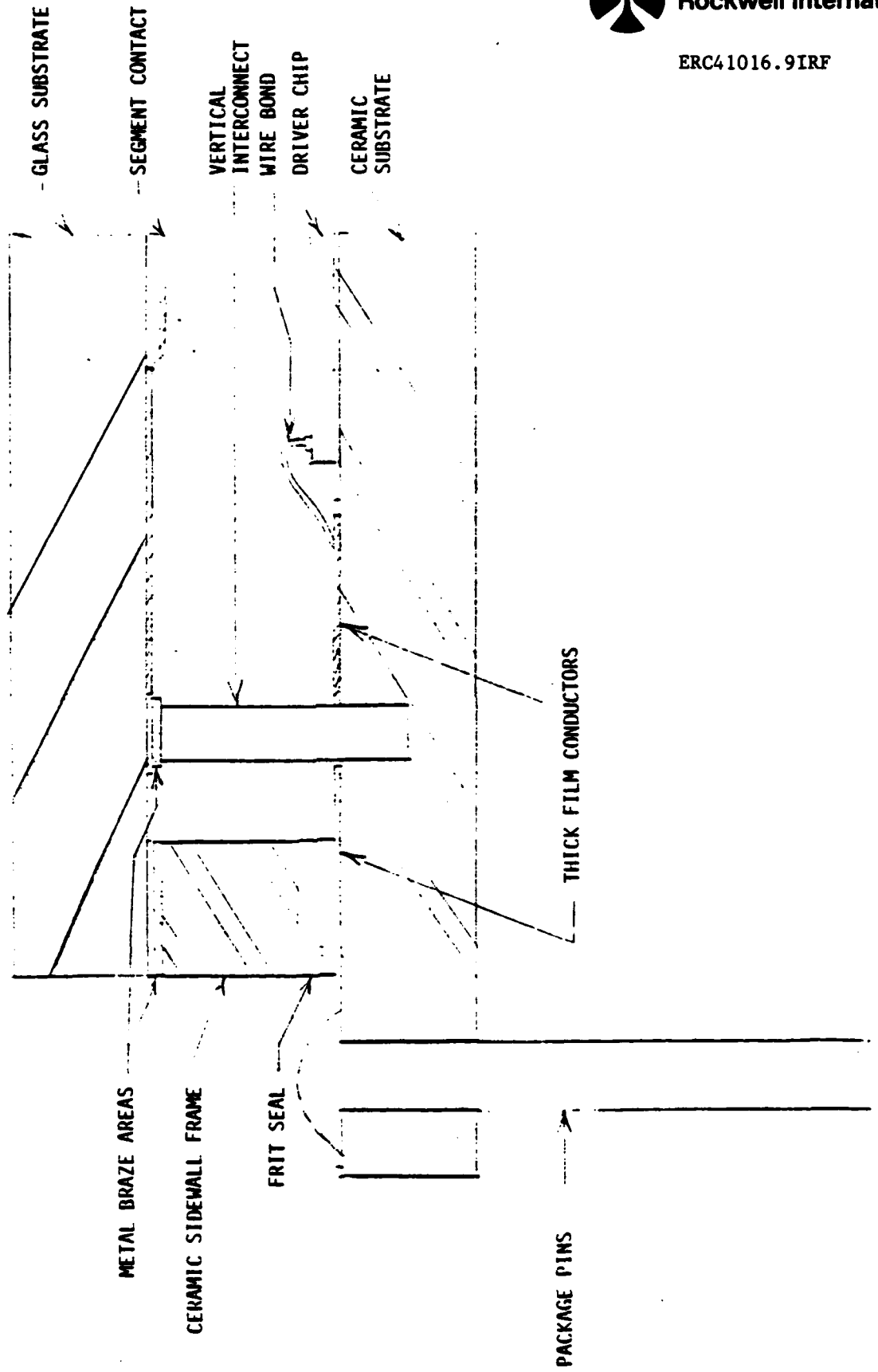


Figure 7



4. Frit-seal sidewall ceramic to ceramic substrate at 580°C
5. Die-bond integrated circuits and other hybrid components to ceramic substrate
6. Interconnect ICs to circuit pattern by thermosonic wire bonding
7. Probe test wired circuit for functionality
8. Braze vertical pins to ceramic substrate (320°C)
9. Braze vertical interconnects and ceramic seal to EL display (280°C)
10. Solder connector pins to ceramic substrate (250°C)
11. Back-fill assembly with desired gas mixture and perform final platelet seal
12. Leak-test display for hermeticity
13. Perform electrical tests to assure proper functioning of display.

These are the basic steps involved in fabrication and assembly of the two-digit numeric EL display with on-board decoder-driver circuitry. As one can see, there are many steps in the process and care must be taken so that all steps in the process are compatible with previous steps, and that materials used do not affect the performance of the EL thin film materials. For example, all brazing compounds must be compatible with the thin film EL materials and all other elements used in the fabrication of the hybrid circuitry should be compatible with the materials of the EL thin film display. It is important to note that no organic materials are used anywhere in this device. It is a truly hermetically-sealed device capable of passing leak tests of 10^{-8} standard cc's per second or better. This approach was used to assure a high reliability operation of the device under the most adverse



temperatures, mechanical, shock, and vibration, as well as other environmental conditions. The hermetic package is also a requirement for long-life operation for the thin film EL display.

Figure 8 shows a photograph of a prototype of this display. Processing is now underway to develop procedures for effecting reliable interconnects in the vertical cross-overs between the decoder-driver circuitry and the EL display segments. Basically, it is a solder reflow process in which the tolerances are slightly interfering until the braze or solder material melts at which time it reflows to segment connections on the glass substrate which are connected to the EL segments themselves. The remainder of the packaging steps are relatively straightforward hybrid assembly processes. While these steps should be quite straightforward, final evaluation will be delayed somewhat until the custom logic integrated circuit chips are received and usable driver circuitry becomes available.



Rockwell International

Science Center
SC5189.5IRD

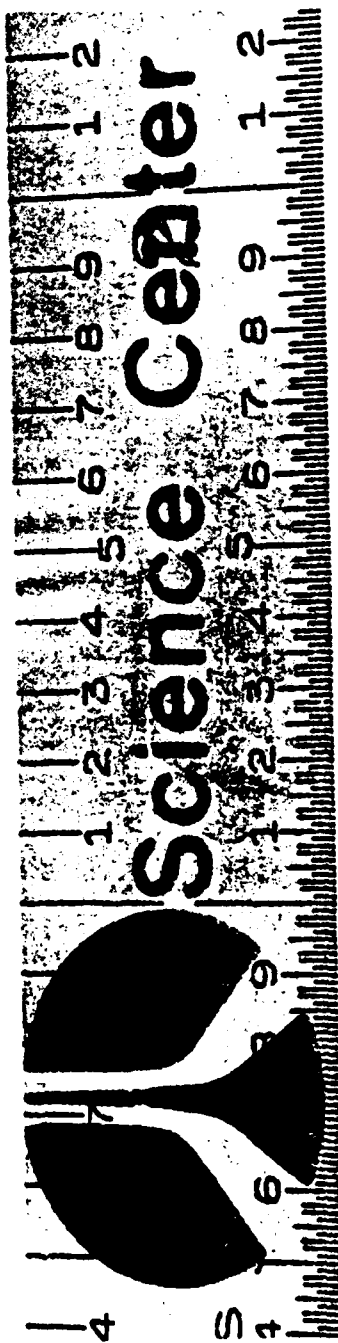
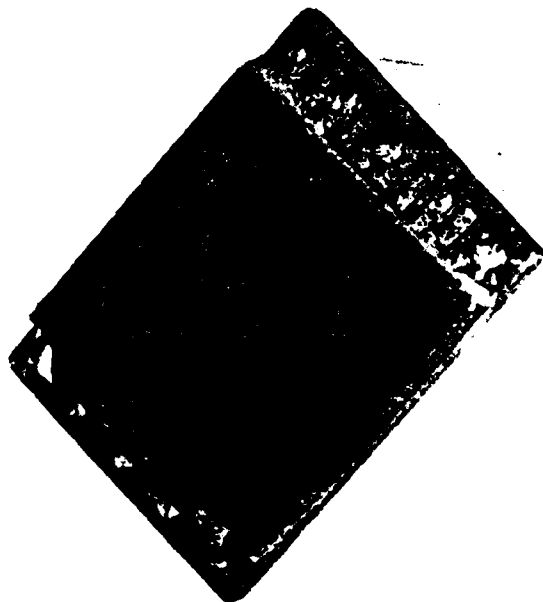


Fig. 8 Prototype



APPENDIX A

Figure 9 schematically illustrates the specular reflection components from the multi-layer TFEL emitter. In this case it is assumed that the reflection at the glass-air interface is minimized by an external anti-reflection coating; therefore the front surface reflection is not shown in Fig. 9. It is also assumed that the black backing is a perfect absorber so $R_4=0$. Therefore, in order to minimize the major reflection R_1 at the glass-ITO interface, the magnitude and phase of successive reflection components R_2 and R_3 are adjusted by means of thickness control of d_2 and d_3 to exactly cancel R_1 . The ITO and first Y_2O_3 are lumped as a single layer since the index of refraction for each are similar.

The following discussion develops an expression for optimum thicknesses of d_2 and d_3 .

Using Ruocard's Method² one can calculate the reflectivity of a multi-layer system by a recursive procedure. In the present case the reflection R_1 (glass-ITO interface) can be expressed in terms of the Fresnel coefficients (r) and the accumulated phase in each layer as follows:

$$R_1 = \frac{r_1 + s_2 R_2}{1 + r_1 s_2 R_2} ; \quad r_1 = \frac{n_1 - n_2}{n_1 + n_2}, \quad (1a)$$

$$s_2 = e^{4\pi i n_2 d_2 / \lambda}$$

²OS Heavens Optical Properties of Thin Solid Films, Dover Publications, 1965.

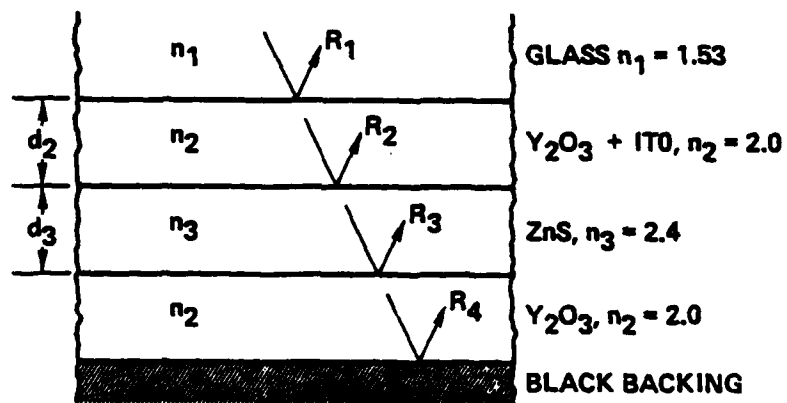


Fig. 9 Specular reflection components from multilayer TFEL emitter.



$$R_2 = \frac{r_2 + s_3 R_3}{1 + r_2 s_3 R_3} ; \quad r_2 = \frac{n_2 - n_3}{n_2 + n_3} = -R_3 , \quad (1b)$$

$$s_3 = e^{4\pi i n_3 d_3 / \lambda}$$

The coefficient R_i represents the total reflectivity contributed by all the layers below the i^{th} layer.

The requirement that R_1 vanish reduces to:

$$R_1 = \frac{r_1 + s_2 R_2}{1 + r_1 s_2 R_2} = 0 \quad (2)$$

or

$$r_1 + s_2 \left[\frac{(1-s_3)r_2}{1-s_3 r_2^2} \right] = 0$$

$$r_1(1-s_3 r_2^2) + s_2(1-s_3)r_2 = 0 \quad (3)$$

assuming $s_3 r_2^2 \ll 1$

$$\frac{r_1}{r_2} \approx -s_2(1-s_3) = -e^{i\phi_2} (1-e^{i\phi_3}) \quad (4)$$

$$= -e^{i\phi_2} [1 - \cos \phi_3 - i \sin \phi_3]$$



$$\begin{aligned} &= -2e^{i\phi_2} \left[\sin^2 \frac{\phi_3}{2} - i \sin \frac{\phi_3}{2} \cos \frac{\phi_3}{2} \right] \\ &= 2ie^{i\phi_2} \sin \frac{\phi_3}{2} \left[\cos \frac{\phi_3}{2} + i \sin \frac{\phi_3}{2} \right] \\ &= 2e^{i\frac{\pi}{2}} e^{i\phi_2} e^{i\frac{\phi_3}{2}} \end{aligned}$$

Since r_1/r_2 is real, in order to satisfy the equation it is necessary that the right-hand side be a real number; this means that the total phase $(\frac{\pi}{2} + \phi_2 + \frac{\phi_3}{2})$ must be an integer multiple of π . When it is an even multiple, one has

$$\frac{r_1}{r_2} = 2 \sin \frac{\phi_3}{2}, \text{ which has solutions} \quad (5)$$

$$\phi_3 = 2 \left[2n\pi + \sin^{-1} \left(\frac{r_1}{2r_2} \right) \right], \text{ or} \quad (6a)$$

$$\phi_3 = 2 \left[(2n+1)\pi - \sin^{-1} \left(\frac{r_1}{2r_2} \right) \right]. \quad (6b)$$

When the phase is an odd multiple of π , one has

$$\frac{r_1}{r_2} = -2 \sin \frac{\phi_3}{2}, \text{ which has solutions} \quad (7)$$

$$\phi_3 = 2 \left[2n\pi - \sin^{-1} \left(\frac{r_1}{2r_2} \right) \right], \text{ or} \quad (8a)$$

$$\phi_3 = 2 \left[(2n+1)\pi + \sin^{-1} \left(\frac{r_1}{2r_2} \right) \right]. \quad (8b)$$



In the present case $n_1 = 1.53$, $n_2 = 2.0$, and $n_3 = 2.4$, so that $\sin^{-1}(r_1/2r_2) = 0.82$ radian. We seek a solution wherein the ZnS layer is roughly 4000\AA thick and the composite ITO- Y_2O_3 layer is about 2800\AA thick, as determined by other device constraints. Taking $d_3 \approx 4000\text{\AA}$ and an operating wavelength $\lambda \approx 5800\text{\AA}$ gives $\phi_3 = 20.48$ radians, corresponding to $d_3 = 3940\text{\AA}$.

This choice forces the total phase to be an odd multiple of π , which gives the relation

$$\phi_2 = (2m + 1)\pi - \frac{\pi}{2} - 10.24 \quad (9)$$

On the otherhand, we seek a solution near $d_2 = 2800\text{\AA}$, for which

$\phi_2 = 12.2$ radians. The closest one can come is $m = 3$, which gives

$\phi_2 = 10.18$ radians, corresponding to $d_2 = 2348\text{\AA}$.

