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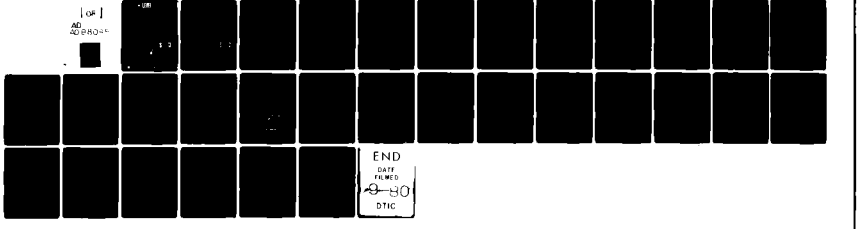

NRL Memorandum Report

Present and Future Trends in Signal Processing Technologies

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11 August 1980

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This report is intended to provide a quick overview of various signal processing technologies and to evaluate their impact on modern radar design in the 1980's. Although primary emphasis is placed on conventional solid-state technologies, a serious effort has been made to review more exotic physical phenomena and related technologies which have attracted, recently, a great deal of interest and are no longer viewed as scientific curiosities. The later group includes surface acoustic waves (SAW), charge-coupled devices (CCD), magnetic bubble memories (MBM), Josephson junction (JJ) devices, and acousto-optics.

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CONTENTS

PRESENT AND FUTURE TRENDS IN SIGNAL PROCESSING TECHNOLOGIES

1. INTRODUCTION

This study is intended to provide a quick overview of various signal processing technologies, primarily from the standpoint of radar system designers who need to know not only the state-of-the-art but also important technological developments which are projected into the 1980's. Such knowledge is extremely important if the designer is to attain the maximum possible improvement in system performance, mission dependability and cost.

The evolution of signal processing parallels very closely the evolution of component technologies, and during the past twenty-five years semi-conductor technologies have been, in very significant ways, responsible for the wide selection of components presently in use. Another key consideration, of course, is the series of advances which have been made in system architecture and algorithm design. Some of these advances were due to advances in component technologies, but many were made independently of technology and are still awaiting for further technological developments to demonstrate their feasibility. Therefore, a brief review of certain key semiconductor based technologies is in order, and this is accomplished in the two sections that follow.

First, we review the physical phenomena and/or processes which give rise to the various relevant technologies, considering at the same time state-of-the-art devices supported by these technologies, and then we concentrate on the impact advanced technologies are likely to have on signal processing.

An extensive, relevant bibliography is provided covering primarily the period 1977-1979.

2. SIGNAL PROCESSING TECHNOLOGIES

During the past twenty-five years, the fabrication of solid-state devices has been dominated by the elemental semiconductor material silicon (Si) and the associated technology which has brought us large-scale-integrated (LSI) circuits and more recently very-large-scale integration (VLSI) capable of supporting tens of thousands of electronic devices on a chip. This so-called silicon revolution is about to be followed by another even more promising technology utilizing the compound gallium arsenide (GaAs) with a far greater impact on system design than silicon technologies ever had.

Gallium arsenide is a semiconductor compound well-known to microwave engineers who make use of Gunn and Impatt diodes and Schottky-barrier GaAs

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FET's (MESFET) to design solid-state microwave equipment. However, the promise of GaAs device technology is multifaceted and covers not only microwave transistors and solar cells, but also integrated circuits, CCD's , diode lasers, and photodiodes. Therefore, its potential applications range from signal and data processing to microwave and optical communications and solar cell design.

Other technologies of particular importance to signal processing are those based on surface acoustic waves (SAW), magnetic bubbles, acousto-optics, and cryogenic Josephson junctions. In this report, we offer a brief description of the various technologies and the manner in which they are most likely to impact the field of signal processing in the 1980's and beyond.

2.1 Silicon Technologies [2-5, 9, 11, 12, 17, 20, 21, 49]

The two major silicon technologies which have dominated the fabrication of integrated circuits over the past several years are the MOS and BIPOLAR technologies. Within each one of these, we identify well-known specializations such as CMOS, PMOS and NMOS of the MOS family, and I^2L, ISOPLANAR and COLLECTOR DIFFUSED ISOLATION of the Bipolar type. These technologies are based on fabrication techniques which result in about 4 microns feature sizes (i.e., mask dimensions), and they are therefore very limited in alleviating the continuing pressure exerted by integrated circuit users for increasing capabilities per chip in terms of improvements in speed, device density, power consumption, yield, reliability, and cost reduction.

Improvements in silicon based technologies are possible and there are underway major efforts to reduce feature sizes (i.e., mask dimensions) to 1 micron in the very near term (i.e., early 1980's) and to submicron dimensions (i.e., 1.0 to 0.1 micron) in later phases (circa 1985). This is feasible through the use of electron beams and X-rays in forming patterns on semiconductor wafers. These processes require manufacturers to perform major retooling and learn new procedures and fabrication techniques. Although submicron IC's are technologically feasible, their availability in volume may come as late as 1985.

It should be added that submicron technology is well-suited to the manufacture of both Bipolar injection Logic and MOS devices, and its most dramatic effect on IC's will be its ability to accommodate on the same size wafers presently in use (i.e., 3-5 inch diameter) 50 to 100 times the present number of devices, thus making possible the realization of complete systems on a chip. This, of course, translates into improved reliability because of the fewer interconnections needed from chip-to-chip and the fact that wafer fabrication faults are minimized by maintaining present wafer sizes while increasing device density.

The projected improvements in speed in going from 4-microns to a 1-micron technology is by a factor of 4, with power requirements remaining essentially the same in spite of the increase by a factor of 10 or so in the number of devices per chip. With respect to cost, the projection is that by 1985 the cost per circuit function for submicron IC's will be as low as 10^{-6} with conventional MOS and BIPOLAR technologies one order and two orders of magnitude higher, respectively.

Semiconductor houses committed to submicron IC development include IBM, Signetics, Motorola, TRW, Fairchild, Texas Instruments, Hughes, Bell Laboratories/Western Electric, and Northern Telecom. IBM researchers are confident that logic-function microcircuits with minimum device dimensions of 0.5 micron can be achieved by 1985 with satisfactory production yields, and that 0.25 micron dimensions are also feasible. In fact, IBM through its pioneering efforts in micro-microcircuits technology has already designed and fabricated a microprocessor with 1-micron minimum dimension using silicon-gate type MOSFET technology.

The following table summarizes the relative merits of 1-micron to 4-micron technology:

TABLE

Technology	Relative Speed	Relative Device Count	Relative Power Consumption	Relative Cost per Circuit Function	Reliability	Availability
4-micron	1	1	1	1	Good	Now
1-micron	4	16	1	0.1	Better	1985

Silicon technologies with a 1-micron features will result in very-high-speed integrated circuits (VHSIC) and will make possible device densities well within what is presently defined as very-large-scale-integration (VLSI).

2.2 GaAs Technologies [1, 6-8, 14, 15, 22]

If the projections made about the semiconductor compound gallium arsenide (GaAs) come true, integrated circuits and system design will undergo a dramatic change in the 1980's. Monolithic GaAs circuits with a small number of components per chip are presently fabricated in the U.S.A., Europe and Japan, and efforts aiming at VLSI are underway here and abroad.

As pointed out earlier, GaAs devices have been in wide use by microwave engineers for many years, but the current attraction to this semiconductor compound is due to the fact that one can now integrate into the same chip both digital logic and analog functions in a way that makes the boundaries between microwave and digital technology indistinguishable. Another equally important reason for the widespread interest in GaAs is the fact that GaAs digital IC's made with depletion-mode MESFETS and Schottky diodes have demonstrated gate propagation delays of less than 100 psec, breaking the gigabit barrier and moving directly into the microwave region. The low-power, higher immunity to radiation, and high-speed of GaAs over silicon (Si) devices is a clear advantage of the GaAs technology. Fabrication problems, however, are much more serious with GaAs, and it was not until Rockwell International had introduced the planar, silicon-like process of ion-implantation that the feasibility of GaAs digital LSI circuits became apparent. Rockwell is presently testing MSI GaAs circuits operated at clock frequencies of 1-2 GHz.

LSI and VLSI circuits utilizing GaAs, although technology intensive, should be available in production quantities by 1985. Furthermore, development of analog LSI circuits and combinations of analog and digital LSI functions on the same chip are clearly feasible in the 1980's, and therefore the designer will be able to assemble entire systems such as high-speed filters, high-speed A/D converters, microprocessors, and needed interfaces all on the same chip using the same technology. The recently demonstrated GaAs charge-coupled devices (CCD) constitute an important step in this direction.

Another important property of GaAs is its ability to efficiently emit and detect light, and one can expect in the 1980's monolithic, single-chip optical receivers and transmitters. This will make possible the merger of optical and electronic signal processing, in itself a major breakthrough particularly from the standpoint of processing speeds and secure data handling.

2.3 Surface-Acoustic Wave (SAW) Technologies [30-39, 42, 55, 57-60]

Surface-acoustic-wave (SAW) devices utilize the interaction between an electric field and a piezoelectric material, which takes place when such a field is placed across the piezoelectric material. The result of this interaction is an induced mechanical strain which is propagated along the surface of the piezoelectric material, and, by reciprocity, this disturbance is detectable by the same electrode configuration that was responsible for its generation. What is of great importance here is the fact that the propagation of the wave is dispersionless which is a necessary condition for making devices with a linear phase response. [60]

The interest in this device is due to the fact that it permits generation of complex waveforms with device dimensions orders of magnitude smaller than preceding electromagnetic (EM) devices (that is, 100 psec delay lines with short physical lengths are very common); in addition, SAW devices are more reliable, easily reproducible, have loss per wavelength several orders of magnitude less than media such as coax cables, and are fairly inexpensive when compared to EM devices they replace.

The surface-acoustic-wave is generated by a pair of electrodes with a center-to-center spacing of one-half wavelength at the desired center frequency of operation. This implies that the maximum frequency at which a SAW device can be expected to operate is determined by the fineness with which the electrodes can be fabricated. Using electron-beam techniques, SAW devices have been made to operate as high as 3 GHz.

Similar devices are possible by exploiting magnetostatic surface waves induced on magnetic materials. The resulting MSW devices have strong similarities to their SAW counterparts with the added advantages that operation is tunable in the 1-20 GHz region and bandwidth is greater than 2 GHz.

2.4 Charge-Coupled Device (CCD) Technologies [23, 31, 44, 56, 57]

Charge-coupled devices constitute a new family of semiconductor components capable of performing the general functions of analog signal processing, image sensing, and digital or analog memory.

The CCD operating principle is known as "charge-coupling," and consists of electrical charge "packets" created in specific locations in the semiconductor material (i.e., Si or GaAs). Each location, called a storage element, is created by the field of a pair of gate electrodes very close to the surface of the semiconductor at that location. By placing the storage elements adjacent to each other in a line, voltages on the adjacent gate electrodes can be alternately raised and lowered to cause the individual charge packets beneath them to be passed from one storage element to the next. Since each charge packet may be of different size, the line of elements becomes a very simple analog shift register. The shift register performance is the basic characteristic of CCDs used in analog signal processing and memory devices. New GaAs CCD's use Schottky barrier gates rather than the conventional MOS gates, and display better than 0.9994 charge transfer efficiency. Rockwell will be soon testing GaAs CCDs at 500 MHz.

2.5 SAW-CCD Technologies [31, 57]

New signal processing capabilities are possible by integrating a SAW device with a suitable charge-coupled device (CCD) wherein the piezoelectric fields associated with the surface wave are coupled directly to the charge in the CCD. Such a combination could make use of the advantages and compensate for the limitations of each of the two types of devices.

2.6 Acousto-Optical Technologies [41, 52]

Acousto-optical devices depend on the interaction of coherent light with SAW propagating in a piezoelectric material such as lithium niobate ($LiNbO_3$). The light is diffracted by index of refraction changes induced in the material by the SAW. The principle of conservation of both momentum and energy requires that the frequency of the diffracted light be shifted by an amount equal to the SAW frequency. [66]

Signal processors based on such devices are possible for use in areas such as advanced radar systems, secure communications networks, large sonar arrays, signal-warfare and any similar situations which require real-time signal processing with large bandwidth ($>10,000$) and large dynamic range (60 db).

2.7 Josephson Junction Technology [60, p. 181, 61]

The Josephson junction, a superconducting device discovered by Brian Josephson in 1962, opens the door to a new digital technology capable of less than 10 psec switching times and extremely low power dissipation (less than 5 mW/circuit) which permits very dense chip packaging with attendant short interchip signal delays. The superconductive nature of Josephson devices implies operation near absolute zero temperature, a fact usually regarded as a drawback due to the added cost and inconvenience associated with the refrigeration system.

2.8 Magnetic Bubble Memory (MBM) Technology [18]

Magnetic-bubble-memory (MBM) utilizes small cylindrical domains formed in either single-crystal thin films of synthetic ferrites or garnets,

or in thin amorphous magnetic metal films, when a stationary external magnetic bias field is applied perpendicular to the plane of the films. These domains are mobile in the presence of magnetic field gradient, and their direction of movement can be controlled by special structures deposited on top of the film and by a moving magnetic field.

MBM technology promises designers and users of military systems unprecedented levels of non-volatility, ultra-high packing density, ruggedness, and radiation tolerance along with a wide temperature operating range.

3. THE IMPACT OF ADVANCED TECHNOLOGIES ON SIGNAL PROCESSING

Although many technologies predict gigabit logic and whole systems on a chip, there are a few key subsystems which may limit the full capability of these technologies. A good example of this is the A/D converter. Operating speeds of modern radar signal processors and storage densities of digital logic are increasing at such a rate that the processing of wider video bandwidths and dynamic ranges is beginning to be limited by the sampling rates and bits of resolution available in A/D converters, respectively.

In order to gain a better insight into the limitations and capabilities of the various technologies discussed in the preceding section, the same technologies will be now examined in concert with the different types of subsystems appearing in modern signal processors, and an attempt will be made to estimate the impact of advances in these technologies on signal processing.

In order to facilitate the presentation which follows, a brief discussion of certain terms such as very-large-scale-integration (VLSI), very-high-speed-integrated-circuits (VHSIC), and low-power-large-scale-integration (LPLSI) becomes necessary.

3.1 VLSI, VHSIC and LPLSI

3.1.1 Very-Large-Scale-Integration (VLSI)

There is no single recognized definition for VLSI. Actually there are many levels of very-large-scale-integration, and Figs. 1 and 2 offer a more concise picture of the LSI domain and its hierarchies in terms of various technologies and system functions. In other words, VLSI implies a level of complexity and sophistication possible with a given technology not only in terms of gate count but also in terms of line width, storage density and circuit complexity. Line width appears to be one of the most important factors, and Fig. 3 offers a projection of what one should anticipate over the next five years. For instance, current levels of line widths are 3.5 microns for 16K dynamic RAMs and 2.5 microns for 64K RAMs; 0.5 micron line widths have been achieved in the laboratory, but they are not yet suitable for high volume manufacturing. It should be pointed out that VLSI implies a factor of 10 increases in speed and 100-to-1000 gates per chip.

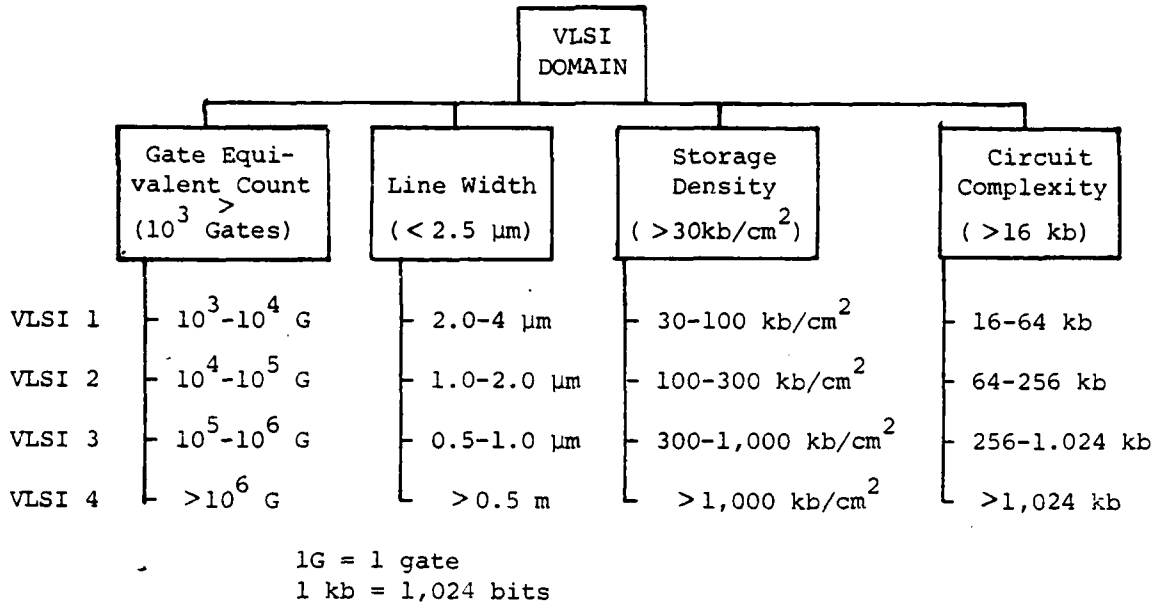


Fig. 1 — Alternate definitions of very-large-scale-integration VLSI phases [24]

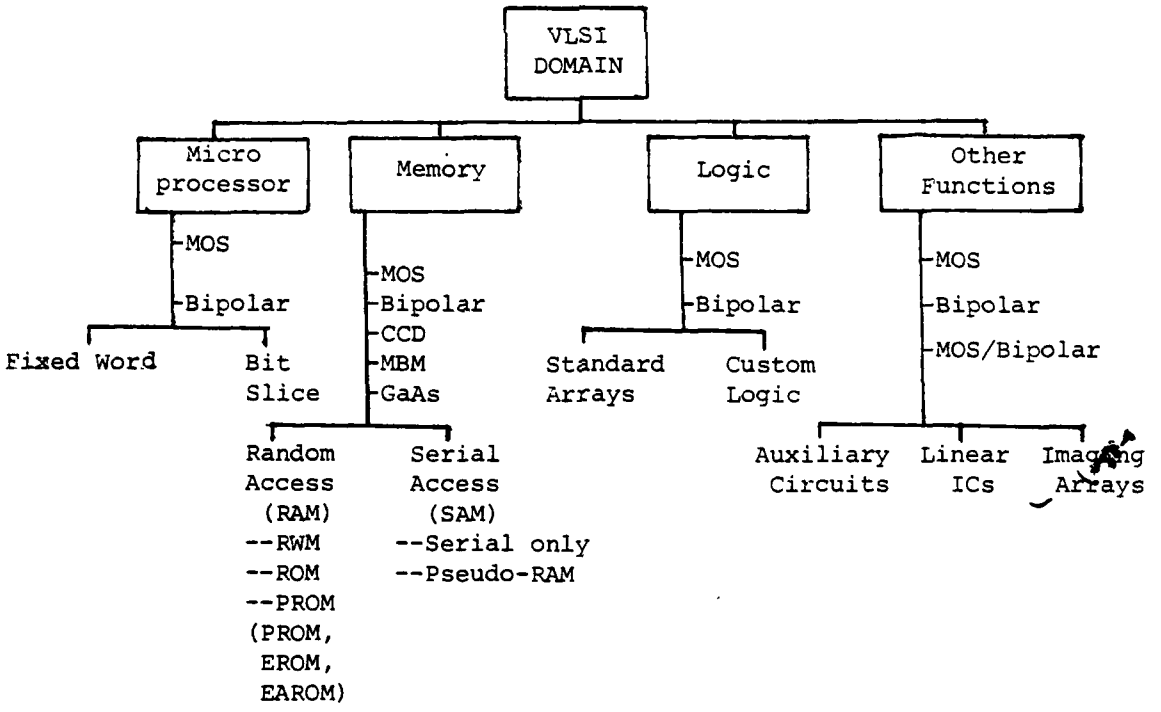


Fig. 2 — Definition of VLSI hierarchy [24]

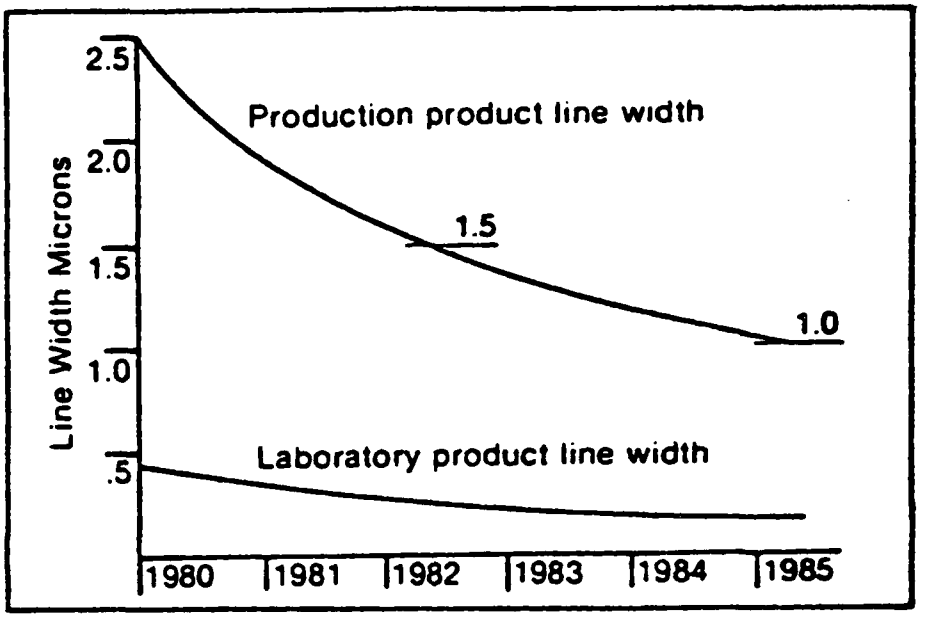


Fig. 3 — Line width versus time [3]

3.1.2 Very-High-Speed-Integration-Circuits (VHSIC)

Very-high-speed-integrated circuits span a wide spectrum of technologies from small-scale-integration (SSI) to medium (MSI) and large-scale-integration (LSI), and eventually all the way to VLSI. The objective here is to achieve a factor of 100 or better improvement in speed at VLSI levels.

3.1.3 Low-Power-Large-Scale-Integration (LPLSI)

Low-power-LSI require less power, by a factor of 10, than conventional LSI and the goal here is to achieve similar results at VLSI levels.

VLSI, VHSIC and LPLSI will undoubtedly increase signal processor performance significantly in terms of functional capability and throughput rates as well as in terms of weight and size reductions. Military applications to be impacted the most by these advances in technology are:

A. Undersea surveillance where one is confronted with a multitude of signals including background noise, signal clutter due to sea life and other ships, and other forms of interference. In such an environment, the signal processing task is of such a magnitude that even the most powerful processor available today cannot satisfy;

B. Signal Intelligence where it is essential that one is able to keep track of, identify, and locate the myriad of signals that can exist in a battlefield. This task becomes difficult when the number of signals climbs into the hundreds or even thousands and when their waveforms become complex. Presently, the weight and size of the equipment needed to satisfy this task are prohibitively out of range, and most of what is urgently needed in this area goes unsatisfied. VLSI and VHSIC will eventually provide great relief toward developing cost-effective and practical solutions to these problems, but this is still three to five years into the future;

C. Missile Seekers is another area for introducing VLSI, VHSIC, and LPLSI technologies. A missile that could distinguish one object from another could be a powerful addition to our arsenal. A missile, for instance, that could distinguish among several targets and strike the target of interest with precision is what we are looking for. The algorithm for this is a straightforward three-dimensional correlation between a stored image and viewed image. However, this computation must be perfomred in real-time while the missile is closing in on its target, and therein lies the problem. In other words, the computational need is so great that even a CRAY-1-like computer would be inadequate. Attaining the required computational speed is not enough since the processor must also be small enough to fit into the missile and sufficiently inexpensive to dispose of it destructively.

It is generally accepted that VLSI, VHSIC and LPLSI technologies constitute a force multiplier from a military standpoint, and their advance and immediate incorporation in military systems should be a matter of highest priority. How future military needs shape up in terms of VLSI, VHSIC and LPLSI is best illustrated by Fig. 4 which offers an outline of levels of technology considered necessary for the implementation, in a cost-effective way, of various military systems.

In what follows, the reader will find how the various technologies presented earlier will affect signal processor design and performance.

SYSTEM/ SUBSYSTEM	TECHNOLOGICAL IMPROVEMENTS NEEDED		
	VLSI	VHSIC	LPLSI
SEEKERS:			
-- IR/EO PASSIVE --			
1. Intelligent tracker	NO	YES	YES
2. Auto cueing	NO	YES	NO
3. Autonomous Acquisition (ACQ)	NO	YES	YES
4. Terminal Homing via solid-state imaging	YES	YES	YES
-- RF ACTIVE --	YES	NO*	NO**
(* VHSIC required only in situations in which the seeker has to cope with a multi-environment target space and sophisticated algorithms are needed for target recognition. ** LPLSI needed when operating in the millimeter region.)			
SENSORS:			
1. LPI-like Radars	YES	NO*	NO
2. Bistatic Radars	NO	YES	NO
3. Simultaneous Beam Radars	NO	YES	NO
(* May require VHSIC if its mission is defined to be beyond the original LPI concept.)			
CONTROL AND GUIDANCE SYSTEMS:			
1. Flight CGS*	YES	YES	YES
2. Weapon control**	YES	NO	NO
(* Includes CGS computers aboard small, low cost missiles; ** Assumes large platform based systems under computer control.)			

Fig. 4 — System requirements in terms of VLSI, VHSIC and LPLSI [62]

3.2 Silicon Technologies

Most of the digital VLSI and VHSIC components over the next five years will be utilizing the well-understood and very well-developed silicon technologies. This is motivated by three principal reasons:

A. The enormous investment in laboratory and production facilities in support of Si technologies,

B. the demonstrated ability of achieving submicron device features with Si, and

C. the fact that we can still squeeze out of Si about two orders of magnitude improvement in speed using its well-understood technologies.

In terms of signal processing power, Si technology will continue to contribute in the foreseeable future most of the digital random logic, and fast solid-state memory at higher densities and speeds. Figures 5 through 10 establish the trend of things to come in the 1980's. The reader should pay close attention to Fig. 9 which clearly indicates that in future systems it is the cost of defining and designing a system that will dominate overall costs rather than the cost of manufacturing the system which has almost always been the case in the past.

The A/D converter which is the key element in any modern digital signal processor configuration will benefit greatly from advances in silicon technologies. TRW predicts A/D units clocked at near 1 GHz rates and providing 5-bit resolution in the near future. However, state-of-the-art places a silicon unit at 400 MHz with 5-bit resolution. Based on this information one can deduce what might be possible in terms of signal processing both now and in the future (i.e., 1980's).

The defense establishment has tended to group signal processor development into three regions according to speed requirements; namely, signal processors operating at clock rates of 10 MHz, 60 MHz, and 250 MHz. [63]

At 10 MHz, existing Si technologies are capable of satisfying all processor needs inexpensively including eight-bit, 10 MHz, A/D converters. Concepts like digital beamforming and sidelobe cancellation are possible in this region because of the availability of relatively inexpensive A/D converters. This is not true at higher frequencies such as 60 MHz where the componenets have been developed, but they are very expensive and not yet proven from a reliability standpoint. The importance of reliability when one operates at the cutting edge of a technology is clearly appreciated by a quick reference to Fig. 11.

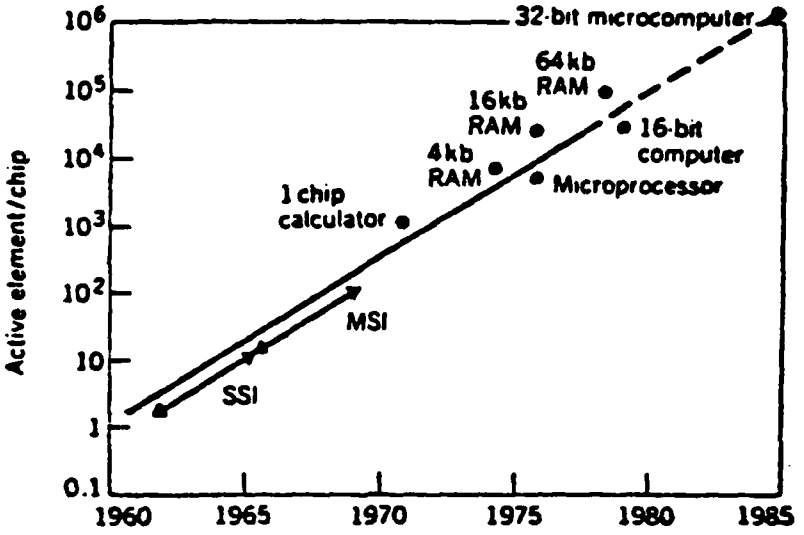


Fig. 5 — By 1985, ICs with complexities of one million devices per chip will be possible. Microcomputers handling 32-bit operations are one manifestation.

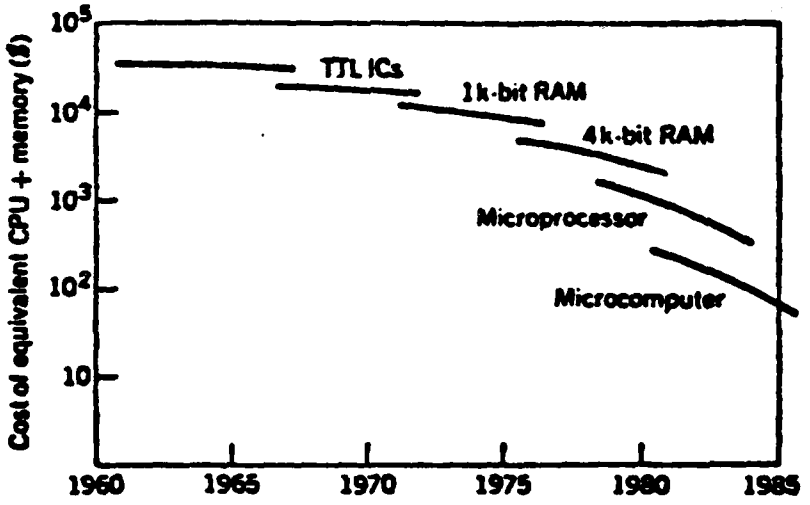


Fig. 6 — The cost of computing power (hardware) is dropping so drastically that by 1984 the capabilities of a much larger IBM 1800 computer will be available in a $100 IC chip [61]

Parameter	1976	1979	1985
Die size (mil^2)	160 x 160	250 x 250	450 x 450
(production level, mm^2)	4.0 x 4.0	6.35 x 6.35	11.4 x 11.4
Resolution (μm) (production level)	6	3	1
Device per die (nonmemory)	10000	80000	1 000 000
Wafer size (inches)	3	4	5 (ribbon technology)

Fig. 7 — Comparative IC processing data [61, p. 40]

Parameter	1976 (NMOS process)	1980 (HMOS II process)	1985 (SBMOS/ DIMOS processes)*
Speed, ns (internal gate)	6	2	1
Power dissipation, mW (per gate)	3	0.5	0.25
Speed-power product, pJ	18	1.0	0.25
Power dissipation perpackage, watts	1	1.5	5

*Schottky barrier MOS/dielectric-isolation MOS

Fig. 8 — Comparative IC performance data [61, p. 40]

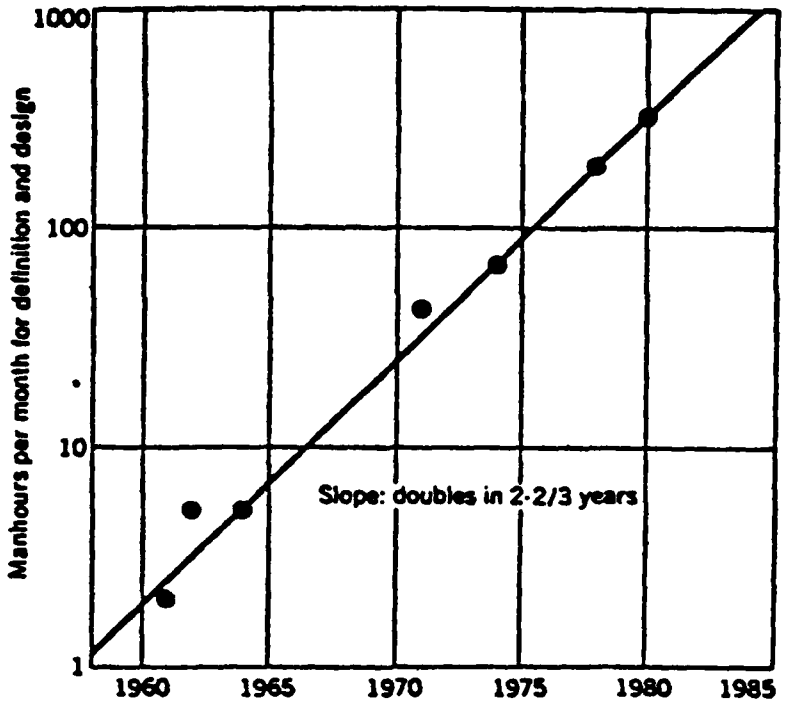


Figure 9

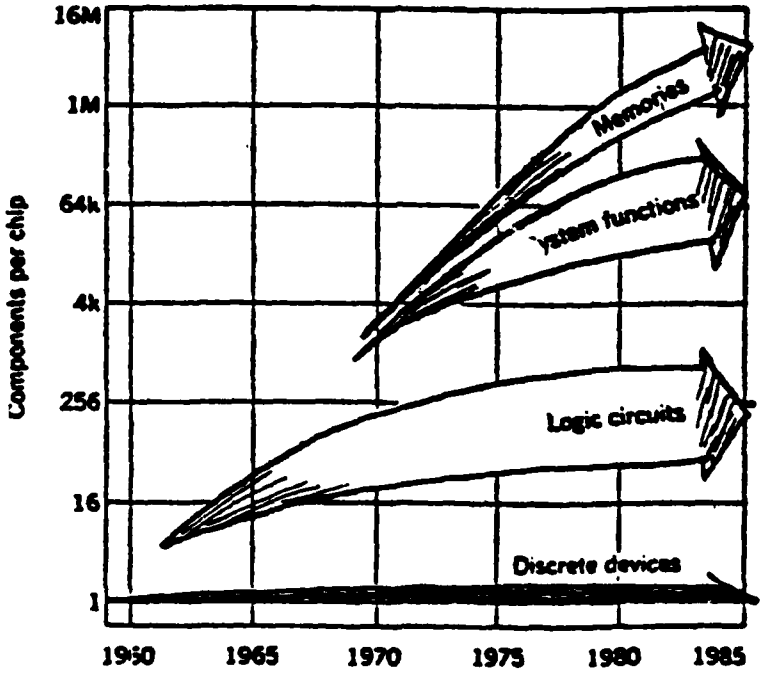


Figure 10

Year	Failure rate (percent/1000 hours)	MTBF, hours (years)
1974	1.27	78 000 (9)
1975	0.5	200 000 (23)
1976	0.12	833 000 (95)
1977	0.08	1 700 000 (194)
1978	0.013	7 700 000 (877)
1979	0.006	16 666 666 (1901)

Fig. 11 — Failure rates and mean time between failure (MTBF) for Motorola MC6800 microprocessor (ceramic package, 70°C ambient tempuerature) [61, p. 41]

DIGITAL IFM RECEIVER CHARACTERISTICS

Model No.	R 4011 L Band	R 5011 S-Band	R 6011 C-Band	R 7111 X-Band	R 8011 Ku-Band
Frequency range (GHz)	1-2	2-4	4-8	8-12	12-18
Unambiguous bandwidth (MHz)	1060	2120	4240	4240	6360
Sensitivity (Threshold) (dBm)	-65	-65	-65	-65	-60
Dynamic range (dB)	70	70	70	70	65
Input impedance (nom.) (Ω)	50	50	50	50	50
VSWR (max.)	2:1	2:1	2:1	2:1	2:1
Capture ratio (at discriminator input) (dB)	10	10	10	10	10
Resolution (11 bits) (MHz)	.52	1.04	2.08	2.08	3.12
Accuracy (RMS) (MHz)	1.25	2.5	5.0	6.5	12
Throughput delay (ns)	185	150	135	135	130
Shadow time (ns)	70	50	50	50	50
Pulsewidth (min. for full accuracy) (ns)	95	60	45	45	40

Fig. 12 — [19]

The state-of-the-art in 60 MHz signal processors is the so-called Advanced Digital Signal Processor (ADSP) now being developed by MIT's Lincoln Laboratory for the Ballistic Missile Defense Advanced Technology Center (BMDATC). [63] This rather sophisticated signal processor utilizes emmiter-coupled-logic (ECL) clocked at 30 MHz and arranged in the "two-transform" architecture which permits matched filtering in the frequency domain. It uses an FFT pipeline to convert input time samples to the frequency domain; multiplies each frequency sample by the appropriate reference function value, and then reconfigures the FFT pipeline to convert the information back to the time domain. The reason for converting to and from the frequency domain is that matched filtering by multiplication is easier than the convolution (integration) operation required in the time domain. Furthermore, the processor can be matched to a new waveform by simply changing the reference function stored in digital memory. The reference function can be modified as desired to compensate for equipment errors or adapt to non-uniform interference. The ADSP uses 10-bit 60 MHz, A/D converters developed by Hughes Aircraft to sample I and Q channels, thus handling 60 MHz bandwidth. This processor will require a large 192 K work input buffer, developed by Burroughs, which uses series-to-parallel converters to multiplex the input data into 1K ECL memory chips. It should be noted that the buffer can be loaded at an impressive 160 MHz rate. The radix four, 16,000-point FFT pipeline built by GE takes four time samples out of the input buffer each clock cycle and outputs four frequency samples, thus completing a transform in about 135 μsec.

The main disadvantage of the two-transform architecture is its inability to provide multiple simultaneous doppler channels. Each desired doppler channel requires a separate spectrum multiplication and inverse transform operation. This is, of course, the trade-off one must make in order to achieve almost complete flexibility in handling a broad class of signal waveforms, and in adapting the receive transfer function so as to compensate for radar equipment errors or to minimize the effects of clutter and jamming. It should be noted that the two-transform technique is a "batch" process which applies the same transfer function to all the samples in the range window. Thus, for clutter which is non-uniformly distributed in range, the optimal transfer function varies with range and is better handled by tapped-delay-line architecture in which the tap weights can be varied rapidly in correspondence with the range. The ADSP is provided with a GE developed completely programmable waveform generator which is required in this case for full waveform processing flexibility.

In the 250 MHz region, a 250 MHz 7-bit A/D converter was recently completed by Hughes Aircraft for BMDATC, and an 8-bit version of it in a full synchronous detector format is nearing completion. Sequentially loaded 250 MHz input buffers should not prove a major technical risk since series-to-parallel converters can time multiplex the data into existing ECL memory chips. MIT's Lincoln Laboratory has performed similar multiplexing at 1 GHz. It is, however, safe to say that full scale 250 MHz buffer units have not been built and tested to date. There has been no development as of now of a programmable, 250 MHz waveform generator, but its two major components, namely, the 250 MHz buffer and a suitable A/D converter are feasible, and therefore one can expect a development effort to produce a 250 MHz programmable waveform generator in the near future. The 250 MHz signal processor is absolutely essential for characterizing radar and other RF emis-

sions and for target recognition and classification and its development in the near future is assured.

A parallel development with advances in VLSI, VHSIC and LPLSI is the implementation of whole systems on a chip or very few chips. IFM receivers designed by TRW, and whose characteristics are given in Fig. 12, are illustrations of such systems. [19]

3.3 GaAs Technologies

Increases in speed and reduction in power requirements of better than one order of magnitude, respectively, with GaAs, compared to Si, are reachable goals in the next five years. In A/D converters at 60 MHz and 250 MHz clock rates, GaAs has already made its contribution in terms of making possible the implementation of important circuits such as the GaAs FET output hold-amplifiers. [13, 43]

It can be said that as monolithic GaAs power amplifiers, low-noise receivers, and A/D converters become commonplace, the analog and digital worlds will merge on GaAs wafers. Presently, research here proceeds along three fronts: analog low-noise devices; analog high-power devices; and digital circuits.

Rockwell International and TRW have evolved as leaders in developing receiver front ends on a chip using GaAs. On the other hand, Raytheon, Westinghouse and TI seem to lead in monolithic power amplifier design. Phased arrays at X-band and above will be also benefitted by these developments. Powers of 1 watt across the 12-to-18 GHz band, and 10-watts at X-band along with multistage gain of 30 dB and 1 dB bandwidth across 12-to-18 GHz region with output power of 1-watt are being designed by Westinghouse under contract to DARPA. Westinghouse is also building a monolithic 3-bit phase shifter. A wideband amplifier (1-to-10 GHz) with a 7-dB gain has been built by Rockwell and its designers are presently shooting for a 3-dB noise figure.

With respect to digital circuits, TRW has achieved data rates of 10 Gb/sec using monolithic GaAs circuits. Hughes, however, is probably the place with the broadest base of capabilities in this technology; Hughes is presently developing a high-speed 50-gate circuit for the Army at 1-to-2 GHz, and also experimenting with a 2 Gb/sec modulator/demodulator. A major objective of Hughes (El Segundo) is the development of high-speed satellite data links that use on-board signal processing.

TRW, on the other hand, is building a five-bit 5-Gb/sec A/D converter using transfer-electron devices (TED) but signal processing at Gb (gigabit) data rates will not become economically feasible without large-scale-integration. One thing is certain in the evolution of GaAs ICs: MSI circuits have been proven and various laboratories are scrambling to expand circuit complexity. HP is presently working on a 500-transistor chip using depletion mode FETs. Most of the MSI circuits to be initially produced by HP are for internal use in limiters, attenuators and other circuits using GaAs ICs. Systems to be affected by GaAs, LSI and VLSI circuits are those requiring low power and very high speed, and systems in which there is an advantage to have the analog and digital portion of the system on the same

chip, such as in a receiver or transmitter. The 1980s will most certainly bring about these developments based on current predictions concerning advances in GaAs technologies. Fig. 13 represents our best estimate of monolithic GaAs IC developments over the next 20 years.

Pre-1985		Post-1985	
DC to 4 GHz	4 to 20 GHz	20 to 40 GHz	above 40 GHz
Linear & digital GaAs ICs Common source, gate, drain circuits. Active loads, little circuit matching.	Lumped element monolithic GaAs ICs. Broadband amplifiers. Complete front-ends to complement DC-4-GHz ICs. Consumer products (direct satellite TV reception).	Lumped/ distributed GaAs ICs. Linear only.	Monolithic mixers and other components to complement 4-to-40 GaAs ICs. Distributed circuits.

Fig. 13 — Monolithic GaAs IC development in the next 20 years [1]

3.4 SAW Technologies

Perhaps one of the most important applications of surface acoustic waves is the so-called SAW-chirp transformation which is an analog signal processing technique for producing Fourier transforms in real time without resorting to A/D or D/A conversions.

A range of SAW filters are available and capable of yielding exceedingly large time-bandwidth products (i.e., TB > 10,000) with bandwidths of several hundred MHz. A linear-FM reflective-array-compressor (RAC) filter recently completed by Hughes has 180 MHz bandwidth and 90μsec propagation length for a TB=16,200. This accomplishment represents a mature state-of-the-art, and, in the opinion of experts, very close to the limit of what can be achieved by straightforward design of SAW structures on lithium niobate. A very similar RAC design can be used for burst waveforms. A 60 MHz, 80 μsec, 16-pulse burst processor has been built by MIT/Lincoln Laboratory on a single crystal of lithium niobate. Performance is comparable to the L-FM filters, i.e., sidelobe levels 35-40 dB. Here, a separate processor must be provided for each doppler channel which is desired simultaneously.

It is now possible to consider SAW techniques with semiconductors to achieve the kind of flexibility/programmability heretofore reserved for digital processors. Examples of such combinations are the:

a/ MIT/Lincoln Lab memory correlator

b/ MIT/Lincoln Lab integrating burst filter

c/ Hughes' chirp Z-transform processor, and

d/ MIT/Lincoln Lab SAW/CCD fast-in/slow-out buffer.

In the 1980's, SAW components will appear in hybrid systems especially as a means of performing real-time Fourier transform computations.

3.5 CCD Technologies

The sampled analog nature of the CCD coupled with the ability to tap the samples and to control the motion of the samples with digital clocking waveforms make charge-coupled-devices capable of performing a wide variety of signal processing functions. Clocking frequencies up to 200 MHz have been demonstrated with 900 MHz appearing to be a feasible goal when using Si.

Tapped CCD delay lines are excellent sampled analog filters and can be externally programmed to change filter characteristics, scan a frequency spectrum or provide correlation of weak signals in a strong noisy background.

Similarly, a digital CCD signal processing technology is being developed which combines the high-accuracy capability of digital systems with the low-power high functional density of CCD to form a unique LSI technology. Therefore, some complex digital systems that were thought to be impractical are now viewed as feasible. Digital CCD logic provides very cost-effective signal processing capability in terms of matched filters, correlation, convolution, and fast transforms (i.e., Fourier, Hadamard, Hilvert, etc.). Pipelined implementations are most suitable within the CCD technology. Present use of CCD's is limited because of the limitations encountered in the associated input/output circuitry in terms of speed and complexity. With the improvements anticipated in the 1980's in VLSI and VHSIC, these deficiencies will be removed and CCDs should be able to perform at their limit of about 1 GHz clock rates.

3.6 SAW/CCD Technologies

SAW and CCD technologies are combined to perform sophisticated signal processing functions. One such combination of obvious importance to signal processing is the use of a CCD delay-line time-compressor/expander with a SAW Chirp-Z-transformer. Fourier transforms with 1000 points can be achieved in a few tens of μsecs using the SAW Chirp Z-transform algorithm. This real-time performance is beyond the speed of the current digital FFT. The SAW implementation is also more attractive than the CCD Chirp X-transform for many applications, particularly when high speed and high time-bandwidth product are required. Even when CCDs get to be competitive with SAWs in terms of speed and time-bandwidth performance, the SAW signal processors will offer hardware simplicity since they are IF rather than base-band processors. The single SAW Chirp filter would have to be replaced by four filters in a base-band system, sine and cosine filters for the I and Q channels.

For the SAW/CCD combinations to be most effective, development of high speed CCDs must be continued. For instance, a 500-point SAW Chirp Z-transform requires a dispersive filter time-bandwidth of at least 4x500= 2000. Since 100 μsec is the maximum reasonable dispersive time delay, the minimum reasonable filter bandwidth is 20 MHz which yields a minimum signal bandwidth of 10 MHz. Since, also, CCDs are base-band samplers, they must load samples into the SAW at a 20 MHz rate. This is about right for currently

available CCDs, but in order to take maximum advantage of the high speed of SAW devices much faster CCDs should be developed. Advances in Si LSI and VLSI technologies will assure the higher speeds needed.

3.7 Acousto-optical Technologies

There are three fundamental types of signal processing using acousto-optic interactions:

a/ Real-time correlation and convolution

b/ Continuous and discrete Fourier transformation, and

c/ Programmable memory correlation.

To-date, real-time convolvers have been developed which have a time-bandwidth product greater than 10,000. A Fourier transform device, designed with chirp transform architecture, has been constructed; this device incorporates the acousto-optic convolver and dynamic ranges in excess of 60 dB with 80 MHz bandwidth have been achieved. Analog signal storage (i.e., memory) has been achieved by the use of acousto-photorefractive effect, and "live" signals have been correlated with signals that had been stored for up to two months. Harry Diamond Laboratories have contributed heavily to these developments.

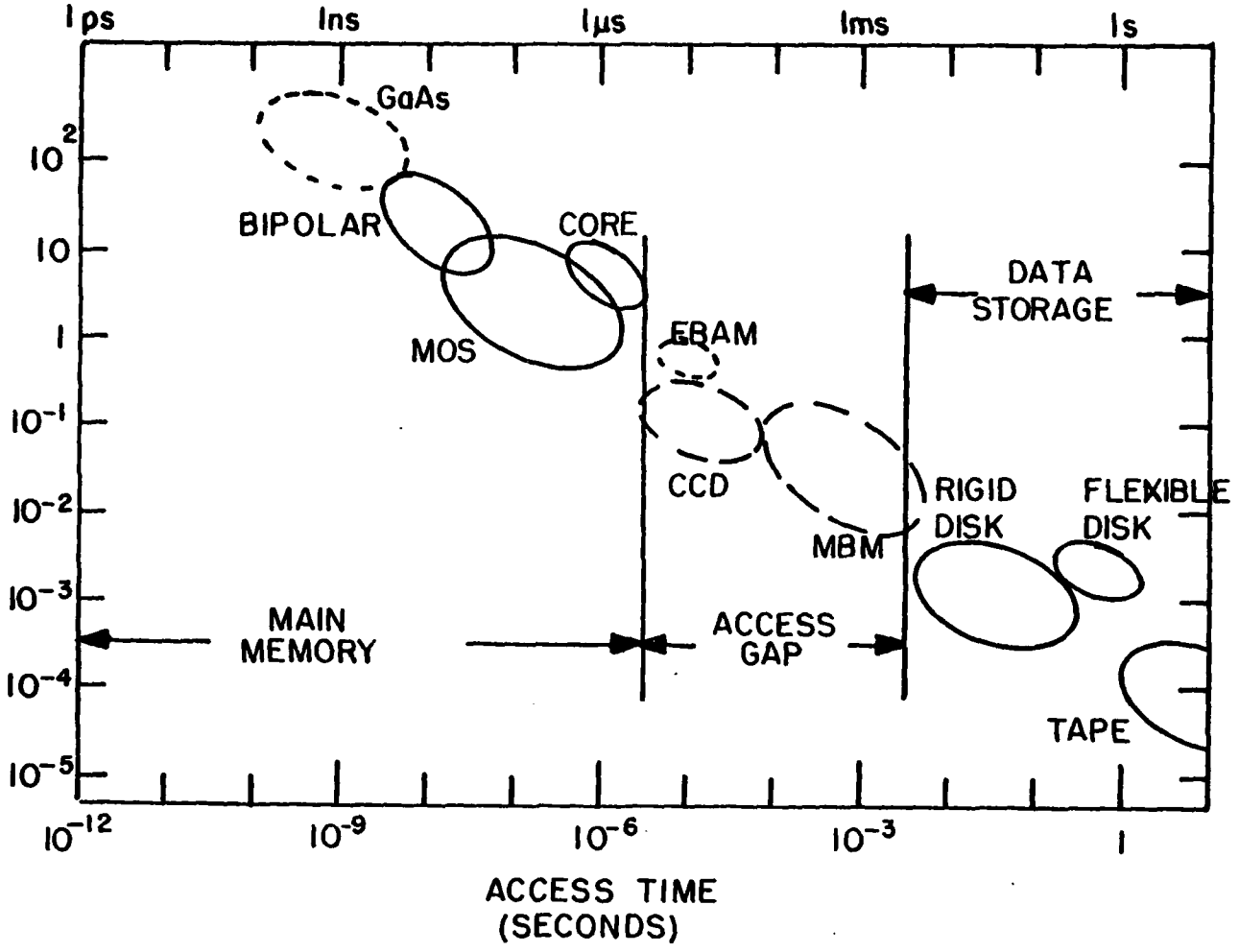
Signal processors based on acousto-optic devices are certainly feasible, but their use is limited to cases in which TB > 10,000 arise naturally and size/weight requirements are not very stringent. Since acousto-optic devices are also used in conjunction with CCDs and SAW devices, any advances in the latter two technologies will translate into corresponding improvements in acousto-optical signal processing.

Itek Corporation announced the availability of an analog acousto-optic signal processing element based on the Bragg cell and having a center frequency of 1000 MHz, bandwidth of 500 MHz and signal processing aperture time of 2.0 μsec.

It should be mentioned, also, that NOSC, San Diego, is developing an electro-optical A/D converter which has the potential for 6-to-8 bit resolution, and conversion rates approaching 1 GHz. The advantages of this approach lie in the fact that the optical device offers a substantial improvement over conventional A/D's because of the reduction in prime power required to drive comparators. The overall reduction in power in such a system, over a conventional one, is by a factor of 10.

3.8 Josephson Junction (JJ) Technology

This technology is still in the laboratory phase although it was pointed out recently that Aerospace Corporation is working on a JJ A/D converter for a broadband totally digital receiver with absolutely no analog components whatsoever. The elctro-magnetic signal is captured through a superconduction loop that uses a JJ. The superconducting loop will let the EM fields through one magnetic quantum unit at a time, thus quantizing the level of the EM field strength one fluxoid at a time. This is what has


1ps
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CORE
MOS
EBAM
CCD
MBM
RIGID DISK
FLEXIBLE DISK
TAPE
DATA STORAGE
MAIN MEMORY
ACCESS GAP
10^{2}
10
1
10^{-1}
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10^{-3}
10^{-4}
10^{-5}
10^{-12}
10^{-9}
10^{-6}
10^{-3}
1
ACCESS TIME (SECONDS)
DEVELOPMENTAL
NEW
MATURE

Fig. 14 — [18]

been referred to as the "superconduction quantum interference device (SQUID)" Such a system will cover the frequencies from ELF to at least X-band.

The National Bureau of Standards has demonstrated the first working JJ A/D converter at 200 MHz and 4-bit resolution. NBS predicts that JJs will reach their practical limit at 30 GHz.

If the JJ technology is sufficiently developed, its primary utilization will be in the ELECTRONIC INTELLIGENCE (ELINT) area.

3.9 Magnetic Bubble Memory (MBM) Technology

Magnetic Bubble Memory may soon make the all-solid state computer a reality. This is particularly important from the standpoint of signal processing because it means that bulk storage requirements can be met through MBMs, and the need for mechanical disk drives is eliminated. As indicated in Fig. 14, MBMs will also improve access, and overall system reliability improvements should result by eliminating mechanical disk drives. The advantages of MBMs are outlined in Figs. 15, 16, 17 and 18. Texas Instruments, Rockwell, Bell Labs and IBM have serious research and development programs in MBMs and maturity of their approaches leading to production for commercial and military use is assured in the very near future.

MBM vs. FLOPPY DISK	
Advantages	Disadvantages
Higher reliability Not mechanical Smaller physical volume Faster access Simpler interface Media integrity	Storage media not readily changed
MBM vs. RAM	
Advantages	Disadvantages
Not volatile More bits/device Reduced board space	Slower access Slower transfer rate
MBS vs. ROM or PROM	
Advantages	Disadvantages
Programmability More bits/device Reduced board space	Slower access Slower transfer rate

Fig. 15 — Advantages and disadvantages of using MBMs over other systems [18]

	One MBM	Four MBMs operated in parallel	Eight MBMs operated in parallel	Eight MBMs multiplexed one at a time
Capacity (bytes)	128K	512K	1M	1M
Average data rate (KHz)	78	312	625	78
Average access time (ms)	40	40	40	40
Power dissipation (100% duty factor) (W)	6	20	40	11
Standby power (W)	1.3	3.7	7.0	7.0
Board area (sq. in.)	16	45	90	90

Fig. 16 — Bubble memory system performance [18]

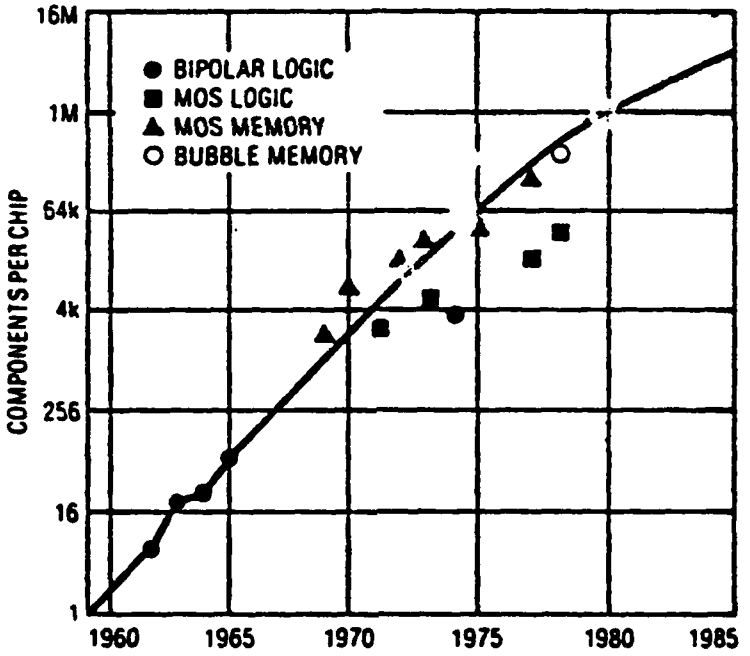

Fig. 17 — Semiconductor chip complexity

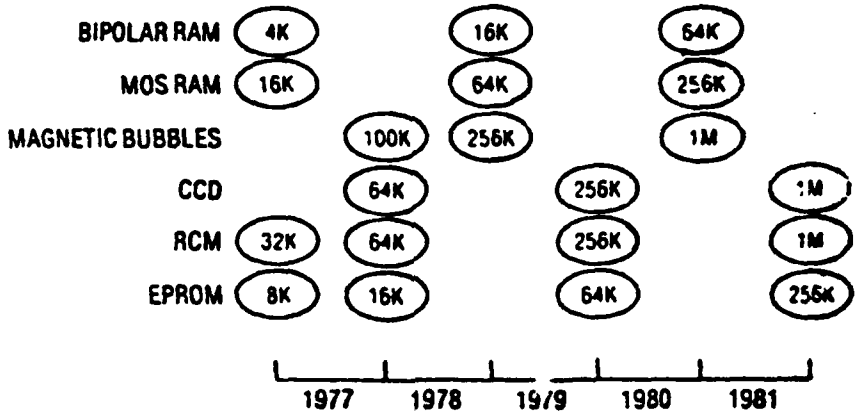

Fig. 18 — Solid-state memory technology trends. Chip capacity quadruples every two or three years for any given technology. During the early 1980's million-bit ROMs, CCDs, and MBMs should emerge.

ACKNOWLEDGMENTS

In a study such as this, a multiplicity of sources had to be consulted in order to determine the state-of-the-art and project with reasonable accuracy into the future those technological advancements which are most likely to impact (radar) signal processing in significant ways. Most of those sources are included in the bibliography which follows. There are, however, several important contributions made by individuals I had the pleasure of communicating with personally, and their valuable input to this study is gratefully acknowledged. Of great assistance were: Dr. Bernard Vatz and Mr. Warren D. Dickenson of the Ballistic Missile Defense/Advanced Technology Center, Huntsville, Ala.; Dr. Don Burlage of the U.S. Army Missile Research and Development Command, Redstone Arsenal, Ala., and Dr. Denis C. Webb of NRL, Electronics Technology Division.

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