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SIX CHANNEL DIGITAL DELAY GENERATOR

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A six channel digital delay generator is described which can provide delays of .5 μsec to 10,000 μsec. Delays are digitally generated and are designed to operate in high RFI areas such as those encountered in ballistic measurements.

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I. INTRODUCTION

In ballistic measurements, considerable use is made of delay units having time period ranges spanning .5 μsec to 100 μsec or more. Historically, delays were generated by R-C networks that fired thyratrons to provide the required output pulses. Because of severe electrical interference, very high input level (30-200 volts) signals were required to prevent false triggering. With the widespread use of digital techniques, time delays with reproducibilities better than .1 μsec are now available. Besides reproducibility, digital techniques require far less set up time and reduce chances of error. Therefore, since reproducibility and efficiency were prime concerns, digital delay techniques were chosen as the most desirable for our program.

II. CONCEPT

The basic concept of a digital delay system is quite simple. Figure 1 shows a simplified block diagram. A digital counter, upon command from the start control, counts the clock pulses until a predetermined number of pulses that has been set by the delay switches has been counted. At this time, an output pulse is generated that signifies the end of the delay period. This pulse can then be shaped to match the requirement of the peripheral equipment. The clock frequency can then be selected to provide the maximum time delay that might be selected by the switches. A chief advantage of this system is its inherent low sensitivity to interference from RFI generated by explosive firing units with spark gap initiators. A single pulse from an external noise source will only shorten the time delay by one clock pulse if this pulse occurs between two clock pulses. It was decided to use existing event counters manufactured by Tektronix as the delay generators. This unit was chosen because of the elaborate input discrimination and pulse shaping networks and because six units could be contained in one 483 mm rack width. Figure 2 shows a picture of the Tektronix DD501 events counter. The front panel delay switches allow up to a 100,000 clock pulse delay before providing an output pulse. All clock pulse and input trigger levels can be permanently set by screw driver adjustments or overridden by manual front panel controls. The input parameters of 1 meg ohm/20 pf allow the use of make and break screens for remote starting of the delay. For more detailed specifications, see the DD501 instruction manual.

The system clock was an M. F. electronics model 5401-1 in a printed circuit mounting package. This particular model has a 10 MHz temperature compensated crystal oscillator with a screwdriver adjustment for frequency correction.

The output circuits were designed and constructed in-house to provide the high voltages required to trip flash x-ray systems and thyratron controlled firing units. Details of this circuit are described in the next section.

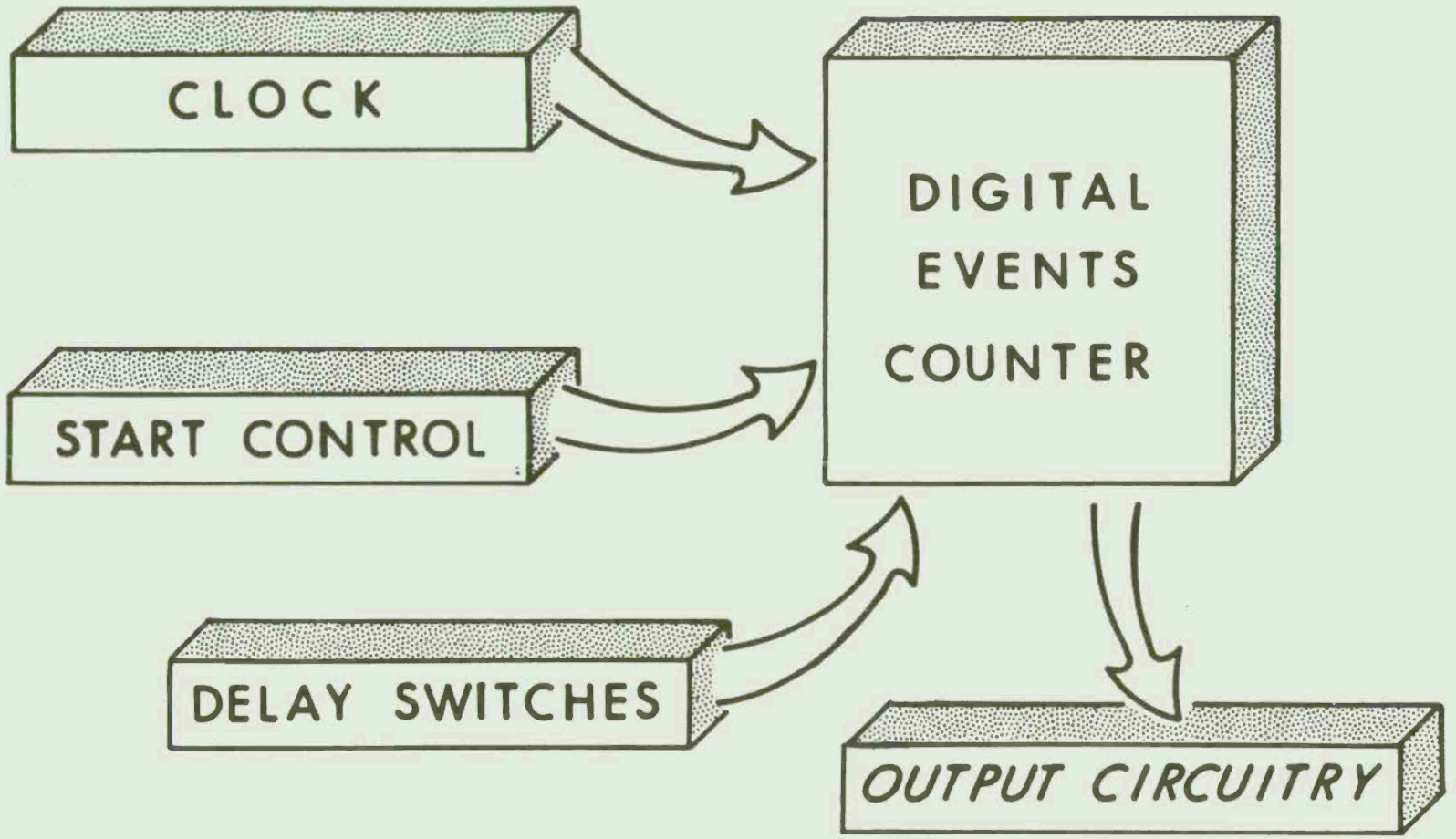

Figure 1. Block Diagram of a Digital Delay Generator

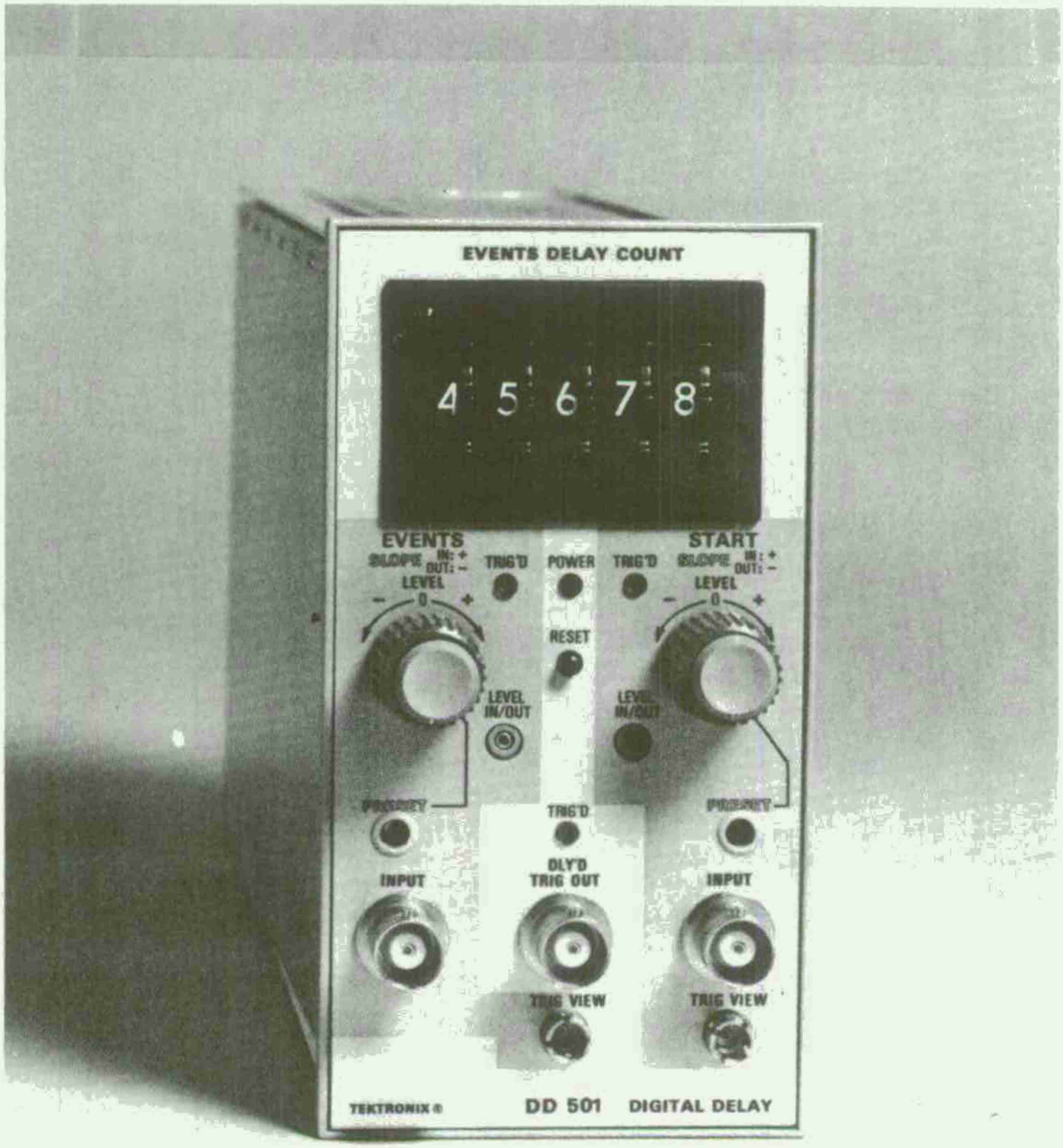

Figure 2. Tektronix DD501 Events Counter

III. DESIGN AND CONSTRUCTION

The circuit diagrams for the crystal clock oscillator, cable driver, and their required power supplies are shown in Figure 3. The 5 volt supply for the clock is obtained from a monolithic regulator, RG1. SCR1 is used as a clamp to short the 5 volt line to ground in case of regulator failure. The clock output is TTL compatible and not capable of driving six 50 ohm lines to the events inputs of the DD501's. The switching transistors Q_1 and Q_2 supply the proper impedance transformation to drive the 50 ohm cables. The disc capacitors on the 5 and ± 15 volt lines are required to reduce internal ringing problems related to the fast TTL pulses. After considerable experimentation, the output resistances consisting of six 51 ohm and one 100 ohm resistors were found to provide the optimum signal at the other end of the 50 ohm cable that was terminated only by the 1 meg/20 pf of the events input. The events input compensation capacitor can be set if required to reduce any remaining ring observed at the events input jack. The ± 15 volts supplies are of a straight forward design. The only unusual portion is the addition of two 10 μfarad capacitors after the 150Ω resistors. These are mounted on the clock board and are required to decouple the clock board itself from the TM506 mainframe.

Figure 4(a) and 4(b) show the physical layout of the clock circuit card. The layout of the power supplies was not critical except for the two 150Ω/5 watt resistors that are mounted on the TM506 interface board. However, the layout of the line driver, Figure 4(b), was important in order to reduce ringing. Figure 4(b) shows the layout of the circuitry around Q_1 and Q_2. Wiring lengths are kept to a minimum by mounting the two transistors and their components right over the output pin of the oscillator. The heat sink fins of the transistors are bent up and bolted with nylon bolts and insulating washers to a 3.18 mm thick aluminum heat sink which is placed over the entire back of the printed circuit (P.C.) card (see Figure 4(a)). The card is then placed in a P.C. board socket mounted behind plug-in locations one and two. All cabling to the plug-ins is soldered to this P.C. board socket. The requirement that the delayed trigger pulse be capable of directly firing a thyratron made the addition of an SCR trigger output necessary. The circuit diagram in Figure 5 shows the finalized design of the pulse shaper and SCR pulse generator. The incoming signal from pins P315-3 and P315-4 of the DD501 is applied to the base of transistor Q_5. Transistors Q_5 and Q_6 make up a modified Schmidt trigger that is used to generate a large amplitude and stretched pulse The output of Q_6 is applied to the base of Q_7 connected in a Darlington type circuit to the gate of SCR2. The SCR2 discharges the .05 Mfd disc capacitor into the 50 ohm resistor on the cathode of the SCR2. This is then the desired output pulse. The overall delay of this circuit adds .4 to .5 μsec to the delay set in by the delay switches on the DD501. SCR2 is selected in order to provide these short delay times. The 60/120 volts D.C. supply required for the SCR2 is generated by a voltage doubler, as shown in Figure 5. Two isolated unused 25 volt A.C. windings are available for each plug-in compartment in the TM506 interface. They are brought out to DD501

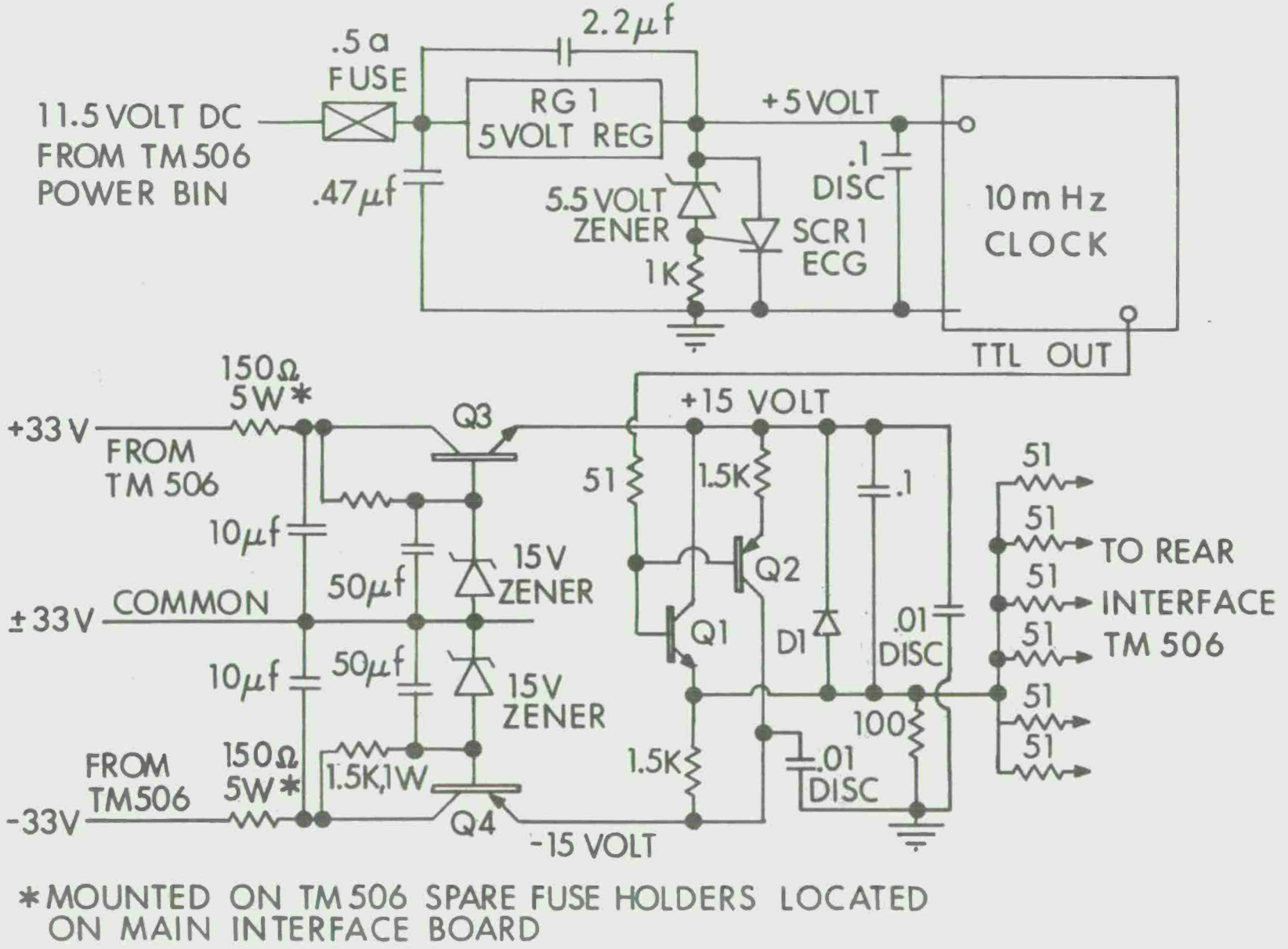

Figure 3. Schematic Diagram of Clock Circuit and Cable Driver

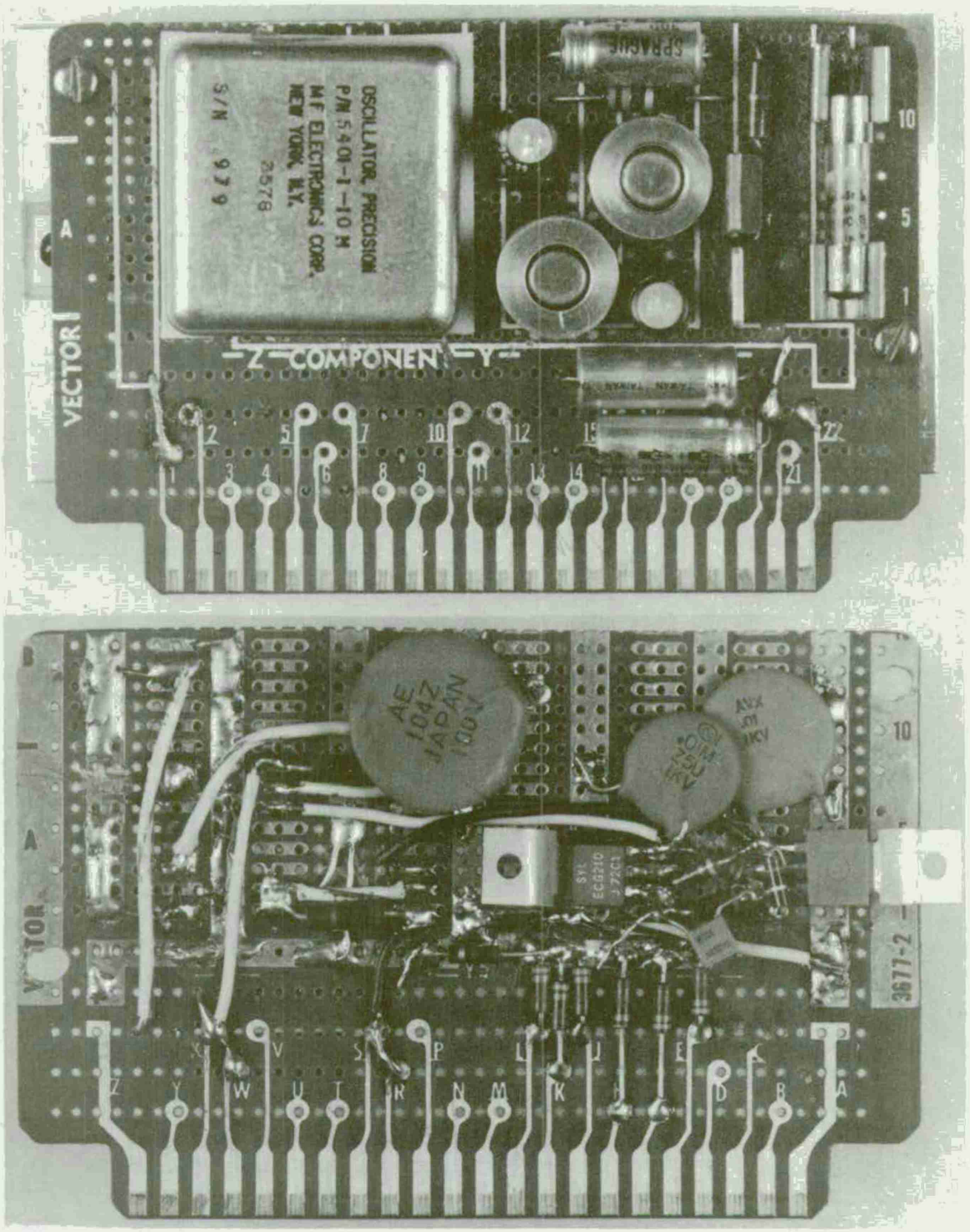

Figure 4. Oscillator Circuit Board
(A) Component Side
(B) Circuit Side

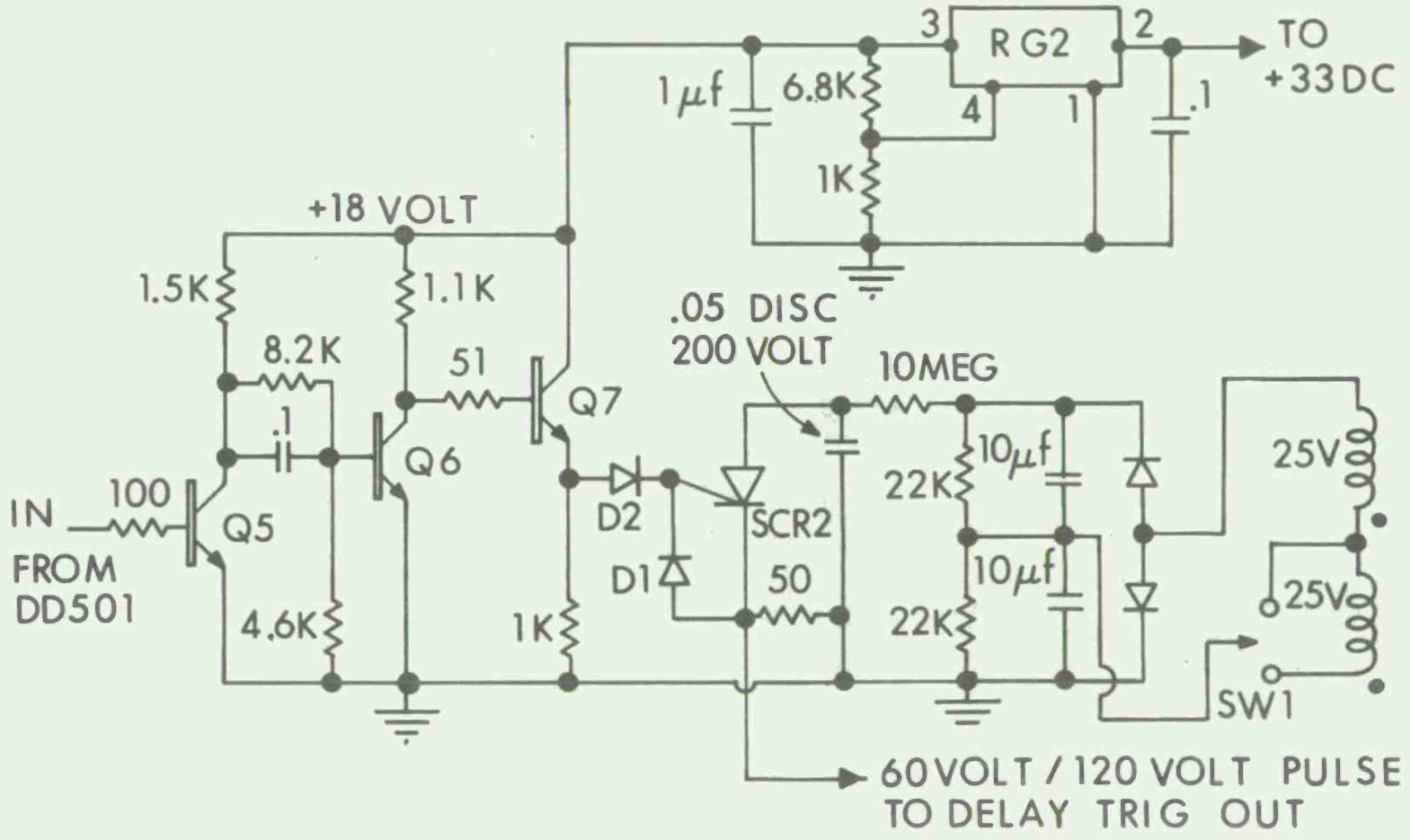

Figure 5. Schematic Diagram of Pulse Shaper and Output Driver

user pins and selected by SW1 for either a 60 or 120 volt D.C. output pulse. The physical size of components mounted on the trigger board was kept to a minimum by the use of 1/4 watt resistors and miniature low voltage capacitors. Figure 6 shows the layout of the P.C. board before installation into the DD501. The original connector to pins P315-3 and P315-4 of the DD501 is used to couple to the input of the board. This connector is also used as one of the mounts and standoff for the board. Figure 7 shows the complete installation of the board in the DD501. The board is mounted by a 25 mm standoff and bolt and the above mentioned connector. The wiring to the back interface and front panel is dressed along the bottom of the DD501. Neatness is an absolute necessity since the voltages involved can do extensive damage to the DD501 in case of an accidental short.

The completed six channel system is shown in Figure 8. The entire system occupies only 134 mm of rack space and is completely self-contained. The final specifications from actual measurements are shown in Table I.

Figure 8. Photograph of Completed Six Channel Delay System

TABLE I

Input	-1 to +1 volts, greater than 5ns wide; 1 meg, 20 pF impedance
Output	60 or 120 volts, .1 µsec risetime adjustable exponential decay
Time Delay Range	5 µsec to 10,000 µsec (easily selectable)
Repeatability	.05 µsec or less after 10 sec

In all tests to date, the units have not only been shown to be reliable but have exhibited an R.F. imunity far better than anticipated. In fact, no R.F. interference from x-ray pulsers or spark cap firing units have been noticed, even using twisted-pair firing lines.

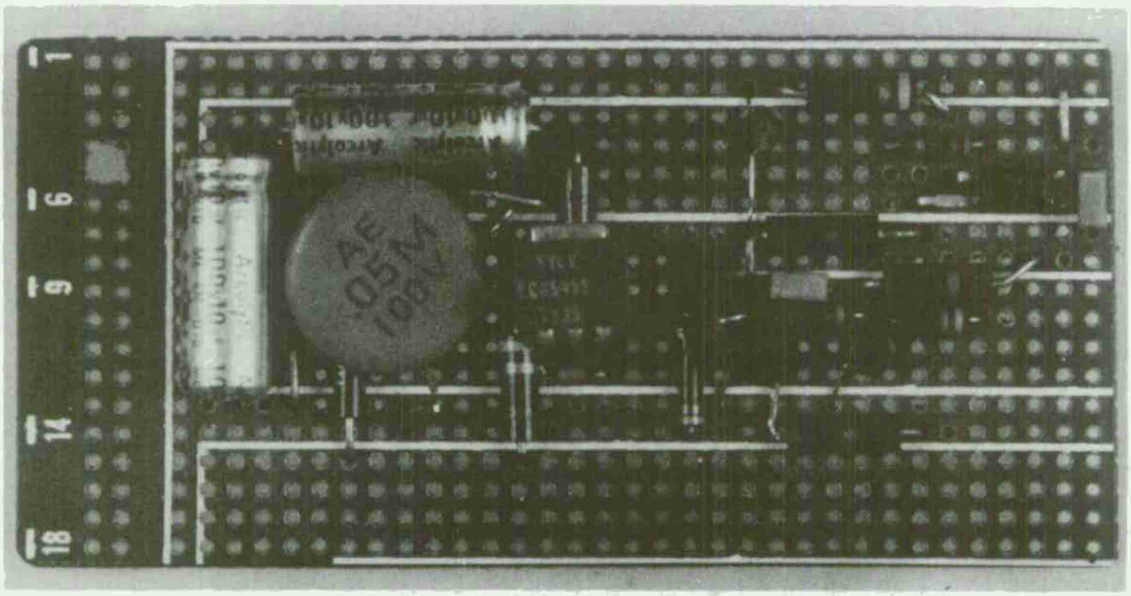

Figure 6. Pulse Shaper and Output Driver Ciruit Board

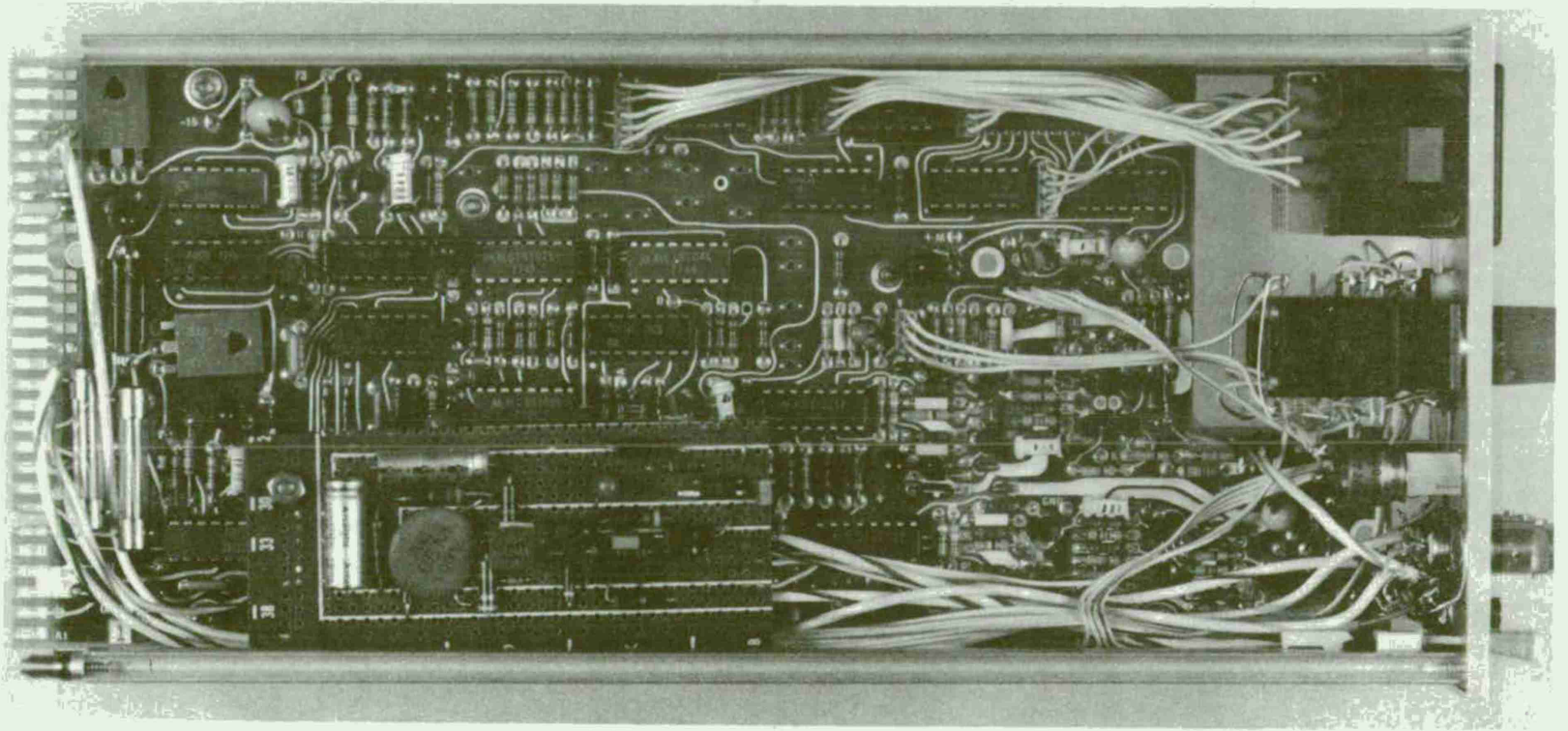

Figure 7. DD501 Events Counter with Pulse Shaper and Output Driver Board Installed

ACKOWLEDGEMENT

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