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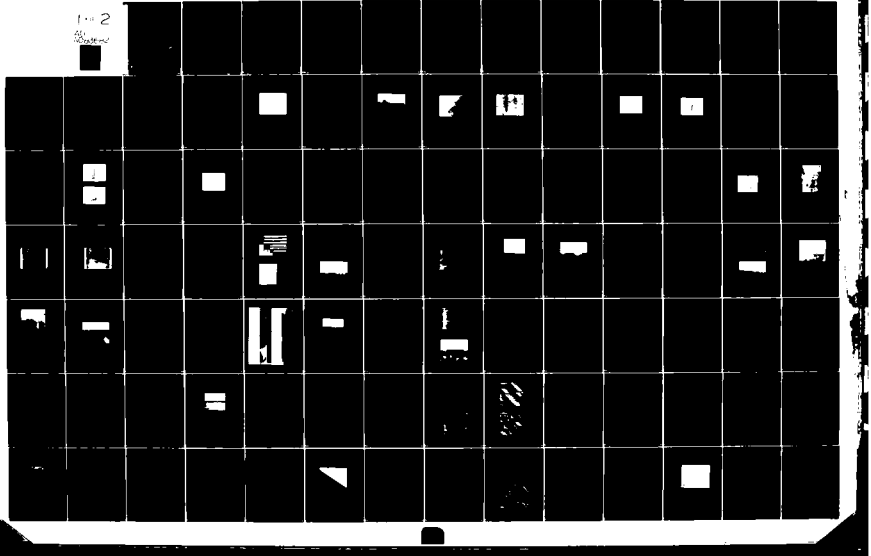

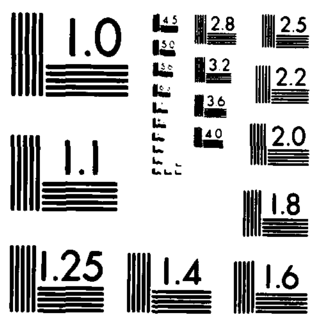

FINAL REPORT

NONCOPLANAR HIGH POWER FET

December 1974 - November 1978

Prepared by:

S.G. Bandy, D. M. Collins, D. R. Decker, J. H. Dully,
R. D. Fairman, S. B. Hyder, C. K. Nishimoto and R. Sankaran

Varian Associates, Inc.
Solid State Laboratory
611 Hansen Way
Palo Alto, CA 94303

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Using a p^+ substrate as the gate and employing low-doped V-grooves under the source and drain to reduce parasitic capacitances, a noncoplanar power FET was designed and fabricated which achieved submicron gate lengths with photolithography masks employing a resolution limit of several microns. Device performance was limited by low values of pinch-off voltage and gate breakdown voltage. Ion implantation or diffusion should enable the break-

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down voltage to be raised by virtue of separating the p-n junction from the growth interface.

FOREWARD

The work reported here was supported by the Office of Naval Research, Washington, D.C., under contract N00014-75-C-0303, and managed by Mr. Max Yoder. The program was aimed at developing a noncoplanar power FET structure in GaAs to realize the benefits of reduced common-lead resistance and inductance.

The work was carried out in the Varian Corporate Research Solid State Laboratory. In addition to the authors, contributions to this work were made by T. O. Yep, R. T. Fulks, and R. L. Bell.

ABSTRACT

Using a $p^{(+)}$ substrate as the gate and employing low-doped V-grooves under the source and drain to reduce parasitic capacitances, a noncoplanar power FET was designed and fabricated which achieved submicron gate lengths with photolithography masks employing a resolution limit of several microns. Device performance was limited by low values of pinch-off voltage and gate breakdown voltage. Ion implantation or diffusion should enable the breakdown voltage to be raised by virtue of separating the p-n junction from the growth interface.

SUMMARY

The objective of this program was to develop designs, techniques, and technology for fabrication of nocoplanar GaAs FETs for operation at X-band and higher frequencies with reduced noise and increased power output. The initial effort was directed toward the development of a noncoplanar structure using the substrate as the source. Problems with shunt SCL currents and nonuniform material growth in the tubs led to a change in design to one employing the substrate as the gate. This second design continued to use the buried-insulating layer technology developed for the first design and in this sense was an extension of it.

After solving a multitude of materials problems by advancing the technology in such areas of high-resistivity growth on p^+ substrates, controlled V-etch and growth, and the growth of continuous layers on unetched surfaces, operational devices were fabricated using the second design. Device performance was limited because of the low values of pinch-off voltage (only 2 V due to the thin MBE active layer) and gate breakdown voltage (presumably because of coincidence of the p-n junction with the growth interface and/or the edge of the p-n junction being defined by damaged material). For a device width of 1.5 mm, 134 mW of 1-dB compressed power was obtained with 2 dB of gain at 5 GHz.

In terms of future development, the best junction characteristics will probably be obtained with ion-implantation of the active layer, but this will be possible only when laser or electron-beam annealing of GaAs is developed. Until then, it appears that increasing the MBE active layer thickness and

improving the junction characteristics by either etching a trough around the mesa to separate the p-n junction from the proton-damaged field region and/or using diffusion to separate the p-n junction from the growth interface should yield a considerable improvement in device performance.

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1. INTRODUCTION

To obtain high power output at high frequency from a field-effect transistor, several factors need be considered. High power output is naturally obtained by increasing I_{dss} (the saturated drain current of zero gate bias) by paralleling several elemental FETs on the same chip. The chip power-handling capability in terms of thermal dissipation must be considered as power input to the chip is increased. Finally, the paralleling or increase of effective gate width must be accomplished with minimal degradation of the frequency performance, i.e. without increase or introduction of extrinsic parasitic elements.

One severe limitation of present low-noise FET designs is the fact that the three electrodes--source, drain, and gate--are all coplanar and lie on the top surface of the wafer as shown in Fig. 1. This structure largely defies paralleling to any great extent due to the welter of bonding wires that would be required for interconnection of isolated elements. However, at the same time, the use of an insulating substrate in present FET structures is a great advantage in terms of reducing electrical parasitics so that high frequency operation can be achieved. Therefore the problem is how to retain the advantages of the insulated substrate structure whilst overcoming the disadvantages of the coplanar electrode structure. A simple modification that solves many problems simultaneously is to make the electrode configuration of source, drain, and gate noncoplanar so as to remove the constraints implicit in the coplanar geometry. Since microwave FETs are normally operated common source, it is then possible to attach the source to the electrical ground

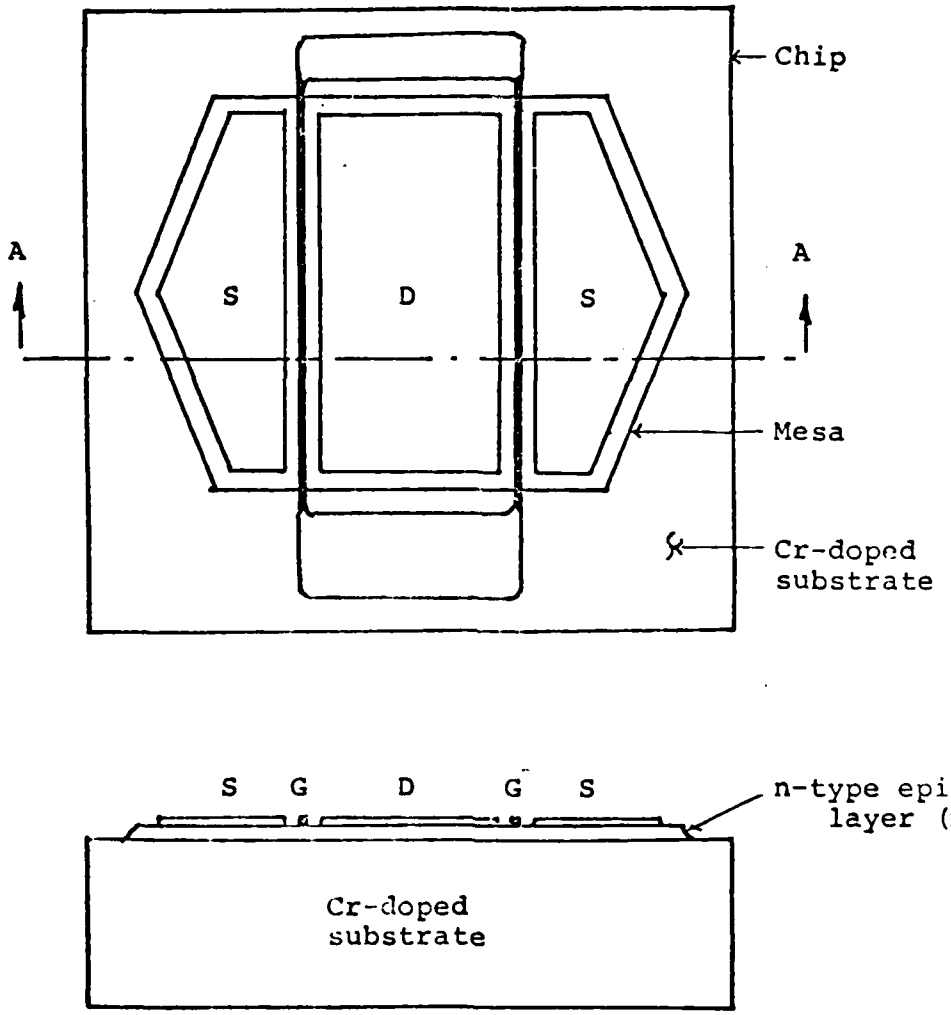


Figure 1. **Traditional coplanar FET geometry (schematic).**

plane with minimal parasitic inductance. One major advantage of this approach is the ability to parallel elemental FETs on a single chip with no degradation of extrinsic parasitics. This is accomplished by connecting the drains and gates to common bonding pads through top surface metallization with interconnection of the isolated sources completed at the ground plane.

The potential advantages of a noncoplanar FET depend in detail on the electrode configuration chosen but in general result in a greater degree of design flexibility and capability of paralleling to obtain high power capability. In particular, if it is chosen to locate the source and gate on opposite sides of the active layer, it is possible to align the gate so as to partially overlay the source without shorting, resulting in a substantial decrease in source series resistance, R_s. If, additionally it is chosen to locate the drain and gate on opposite sides of the active layer, it is possible to eliminate limitations due to surface breakdown between drain and gate. Finally, if the gate is on the opposite side of the active layer from the source and drain, then the source and drain are both on the same side and the source-to-drain spacing can be reduced to a dimension as small as technology and drain breakdown voltage considerations permit, to obtain significantly higher frequency capability.

The objective of this program has been to develop designs, techniques, and technology for fabrication of noncoplanar GaAs field-effect transistors for operation at X-band and higher frequencies with reduced noise and increased power output. Benefits with respect to reduced values of source resistance and common-lead inductance, a possible

increase in the drain breakdown voltage, reduced parasitic capacitances (fewer bonding pads), reduced thermal resistance (fewer bonding pads permits a reduction in area and hence thickness of the die), and shorter channel lengths should be realized.

Two fundamentally different designs to the fabrication of noncoplanar FETs have been investigated under this contract. The initial effort was directed toward the development of a noncoplanar structure using the substrate as the source. Problems with the fabrication of this structure led to a change in design to one employing the substrate as the gate. The second design continued to use the buried-insulating-layer technology developed for the first design and hence was an extension of the initial work, but with changes in design to eliminate problems with SCL currents and nonuniform material growth in the tubs. In terms of time and expense, approximately one-fourth was spent on the first design and three-fourths on the second design.

2. COMMON-SOURCE BURIED-INSULATING-LAYER NONCOPLANAR POWER FET

The formation of buried insulating regions within the surface of an n^+ GaAs substrate permits fabrication of noncoplanar FETs with the substrate acting as common source electrode and with gate and drain lying opposite the source on the upper epitaxial surface as shown in Fig. 2. This fabrication approach is based on the technology of etching basins in the GaAs surface using an SiO_2 mask and regrowth of semi-insulating GaAs into these regions using the SiO_2 to provide selective epitaxial growth into the holes. This approach has the advantage of using reasonably well-understood materials technology to obtain the noncoplanar geometry as well as yielding an n^+-n contact which should substantially reduce the source resistance R_s. Disadvantages of this approach are that the drain and gate are still coplanar, good control over etching geometry must be achieved and maintained, and both insulating and moderately doped material must be grown in the presence of heavily doped n^+ GaAs. Nevertheless, the straightforwardness of this approach is appealing, and the initial effort was devoted to developing the technology to fabricate the common-source buried-insulating-layer noncoplanar FET.

2.1 Material and Device Technology Developed for the Common-Source Buried-Insulating-Layer Noncoplanar FET

The processing procedure developed for the common-source buried-insulating-layer noncoplanar FET involves various etching, polishing, and growth procedures which will be discussed here in some detail.

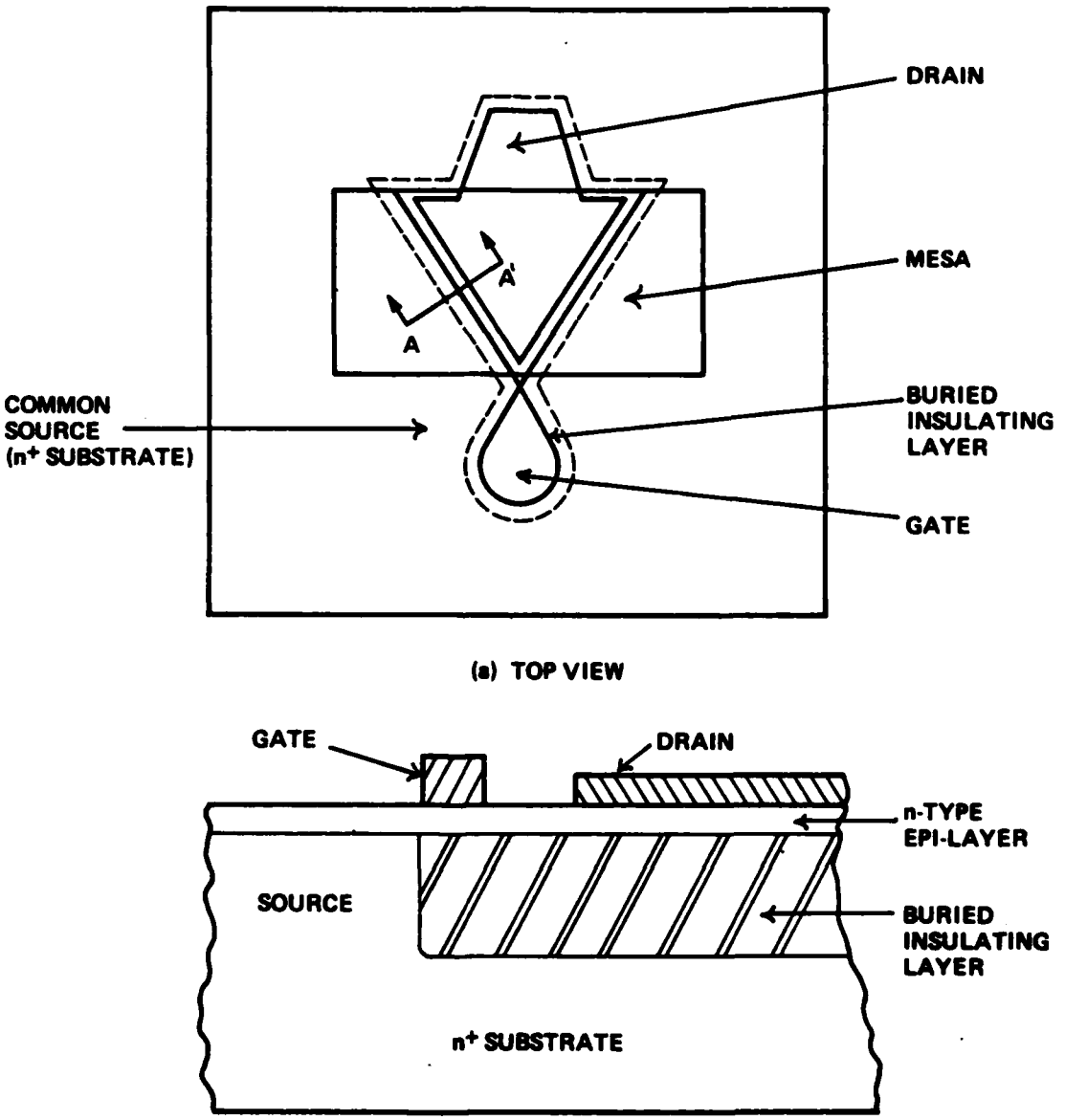


Fig. 2. Buried-insulating-layer noncoplanar FET.

The substrates were Te doped (2-3 x $10^{18}/cm^3$) GaAs misoriented by 1-3° from (100) toward (110). Wafers 0.02-inch thick were lapped with 3200-grit slurry and polished with 3-micron diamond paste to bring the top surface parallel to the back surface within about 5 microns. The final damaged layer was removed by chem-mechanical polishing on a pad with 1:25 by volume of 5% sodium-hypochlorite:water. The wafers were then degreased and etched with 4 H_2SO_4:H_2O_2:H_2O for 1 minute. This was followed by a 4000-5000 Å thick SiO_2 deposition.

Windows were formed in the SiO_2 films by masking with photoresist and etching away the unmasked areas. Then holes were formed in the substrate at the areas exposed by the windows. Of the different etchants tried for this purpose, a solution of $K_3Fe(CN)_6$:KOH:H_2O (8:12:100 by weight) was found to be the best, especially since the etching was fairly isotropic. Holes formed by NH_4OH:H_2O_2:H_2O (20:7:500 by volume) have many desirable qualities, such as extremely smooth surfaces and sharp corners, but the etch rates for (111)A and B faces were quite different so that on one of the (110) cleavage faces the holes were dove-tailed. The etching time was adjusted to give holes about 16 microns deep as shown in Fig. 3.

The holes were back-filled with oxygen-doped GaAs. In the presence of other impurities, probably Si or Zn, oxygen doping has been found to give high resistivity n-GaAs,[1] although the exact compensation mechanism was unclear. The protective SiO_2 layer facilitated selective epitaxial deposition of GaAs in the holes.[2,3] The deposition process utilized a vapor phase reaction of Ga and GaAs with H_2 and

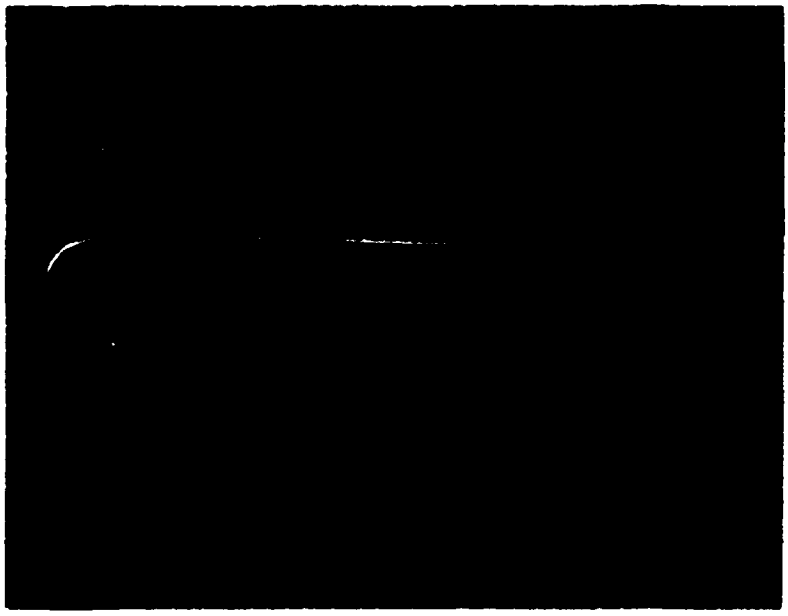


Fig. 3. Etched hole, 16 microns deep on n^+-GaAs in (100) orientation. (Mag. 500x)

$AsCl_3$ in an open flow system.[4,5] The different parameters affecting the growth of GaAs in this system have been analyzed elsewhere.[6] An excess amount of semi-insulating GaAs was deposited in the hole so that the top surface of the deposit was above the surface of the n^+ substrate, Fig. 4.

The wafers were then mounted on quartz plugs and the excess semi-insulating GaAs was repolished using 3-micron diamond paste. The polishing was stopped just when the diamond paste started removing the SiO_2 layer on the n^+ substrate. The SiO_2 layer was then stripped using dilute HF. The mechanical damage was removed by chem-mechanical polishing with dilute sodium-hypochloride solution. Figure 5 shows such a repolished wafer etched with 10 H_2O:H_2O_2:HF to delineate the insulating regions.

After repolishing, the wafers were boiled in 5% KCN for 1 hour, rinsed in DI water, and cleaned in isopropyl alcohol. Sub-micron thick n-type GaAs was deposited on these wafers in a vapor phase epitaxial reactor using the $Ga/AsCl_3/H_2$ system. The Ga source contained Sn as the dopant. The use of such a system for uniform sub-micron epitaxial films has been demonstrated before.[7] The layers were typically about 0.3-micron thick doped to $10^{17}/cm^3$. A light 10 H_2O:HF:H_2O_2 etch prior to the deposition of this layer revealed the pattern even after the deposition of this layer (Fig. 6). This was necessary to aid alignment of the wafer during subsequent processing.

After active layer growth, processing to form FETs was begun. Mesas were etched across the insulating regions. Ohmic drain contacts were deposited and delineated by metal

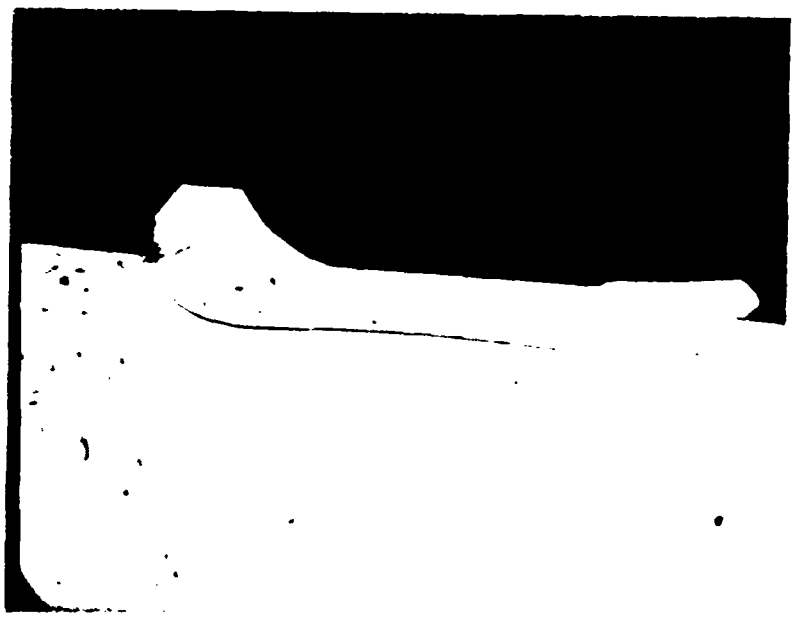


Fig. 4. Epitaxial n^- GaAs deposit in a hole etched in to an n^+ GaAs in (100) orientation. (Mag. 650x)

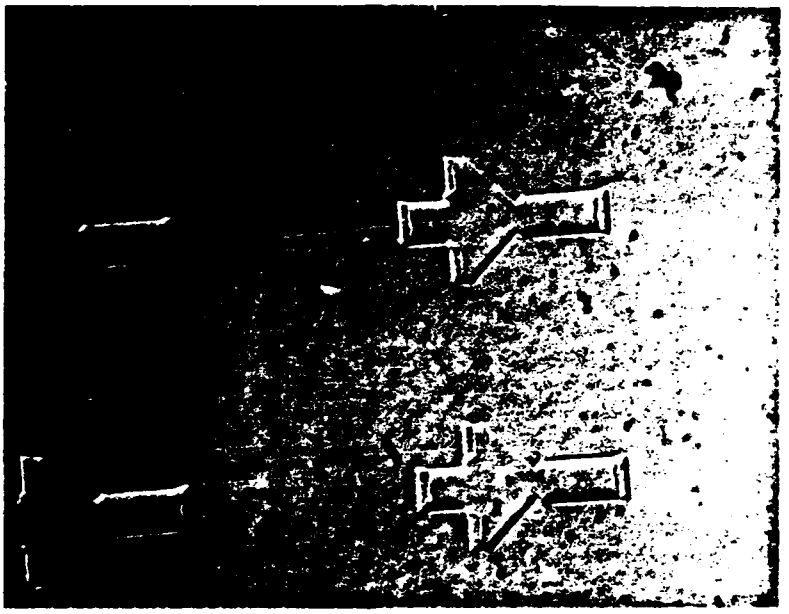


Fig. 5. Epitaxial n^- GaAs deposits in holes etched into an n^+ GaAs in (100) orientation, after the excess n^- deposits have been removed. The boundary has been revealed by a 10 H_2O: HF:H_2O_2 etch. (Mag. 80x)

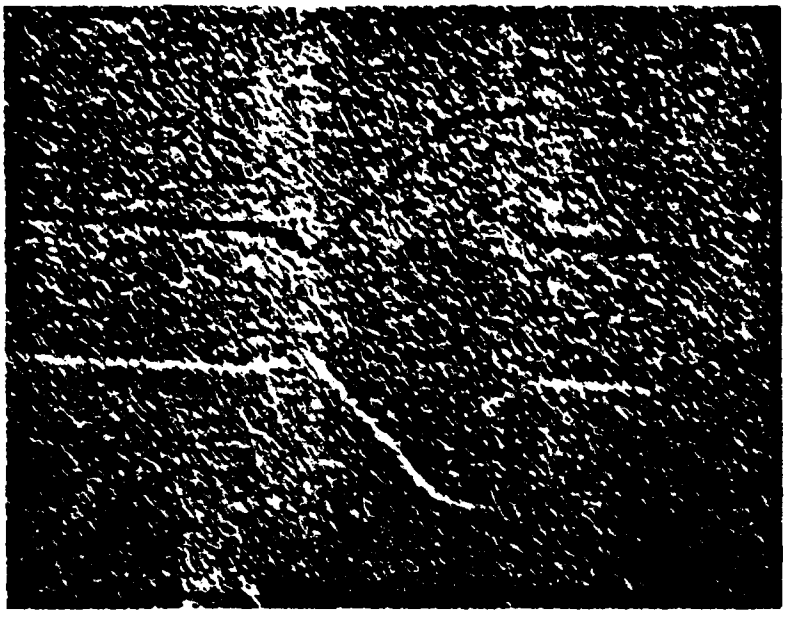


Fig. 6. After the deposition of n-GaAs on the repolished wafer of Fig. 5. (Mag. 250x)

lifting techniques. The drain edge was aligned with the visible (by delineation) edge of the n^+ source beneath the active layer. The drain contacts were alloyed and the drain current was measured. If required, the epitaxial layer was thinned slightly at this stage to provide the appropriate drain current. Schottky-barrier gate metallization was deposited and delineated by lifting. A gold contact overlay completed the device processing to produce a finished noncoplanar FET as shown in the photograph in Fig. 7.

2.2 Characterization and Evaluation of Common-Source Buried-Insulating-Layer Noncoplanar FETs

A total of five wafers of common-source buried-insulating-layer noncoplanar FETs have been fabricated using the technology developed and described in the preceding section. The first wafer completed, NCT-1, exhibited devices with a field-effect transistor characteristic for the substrate biased positive and the drain electrode biased negative. This is, of course, the reverse bias polarity to that desired in order to operate with the substrate as common source. For a positive drain bias relative to the substrate, excessive drain current (breakdown) was obtained for drain bias in the range of 2-3 V as shown in Fig. 8. Since drain breakdown occurred below the saturation point, these devices did not perform well as microwave amplifiers. This same type of behavior has been observed on all noncoplanar FETs made with the oxygen-doped buried-insulating-layer technology.

The salient features of transistors assembled from wafer NCT-1 are typified by the data shown in Table I.

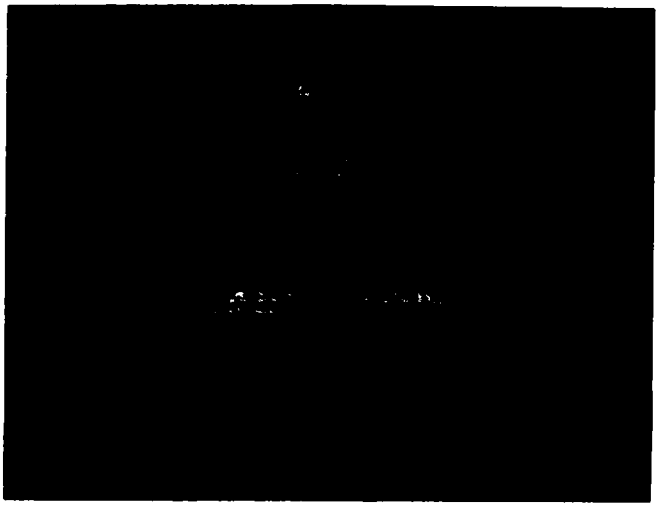


Fig. 7. Noncoplanar FET.

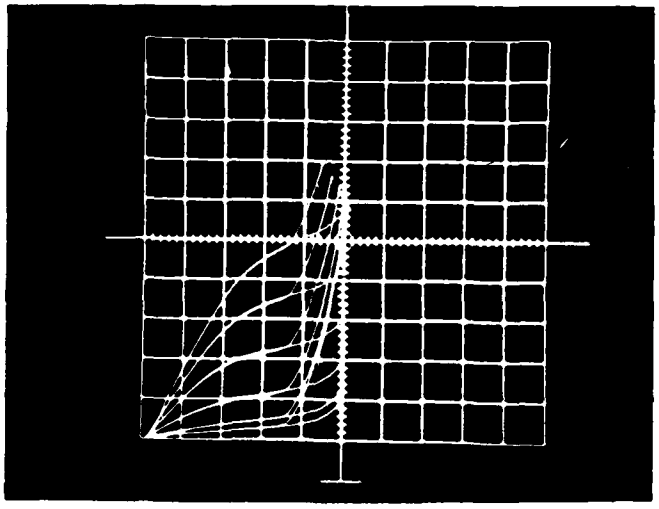


Fig. 8. Drain I-V characteristic of wafer NCT1-11 showing drain breakdown. Horizontal: 0.5 V/div; vertical: 10 mA/div; gate voltage steps 1 V.

TABLE I: NCT-1 Characteristics

(a) Curve Trace

Unit	I_{dss} (mA)	V_{dss} (V)	g_m (mmho)
1	50	2	13
2	58	2	15
6*	60	1.4	15 (@ V_{ds} = +2 V)
7	56	2	14
8	54	1.8	15
9	66	1.7	15
10	60	1.5	15

* bonded in forward direction (drain bias positive)

(b) Amplifier test @ 7 GHz

Unit	Gain (dB)
1	4.8
2	5.0
6	1.5
7	4.0
8	4.7
9	3.2
10	5.2

With the exception of Unit 6, these devices were mounted in a 4-terminal package in order to operate with the drain grounded and the source (substrate) biased positively and acting as a drain. This package has large parasitic capacitances and is no longer used for conventional transistors, but was convenient for this application since it enabled operation with the substrate ungrounded. Since Unit 6 could not be biased in saturation, the amplifier data were probably not indicative of the performance capability of these devices. Transistor NCT 3-1 was measured for source resistance, R_s, which was about 2.5 ohms. Microwave network analysis on NCT 3-1 yielded a transconductance g_m = 1.7 mmho and an output conductance g_{ds} = 1.6 mmho at 2 GHz. The input capacitance was about 0.57 pF. The calculated f_{max} was about 2 GHz and no attempt was made to test this device in an amplifier.

Wafer NCT-4 produced visually good transistors with an I_{dss} of about 50-70 mA. However, the gate characteristic was soft and leaky, breaking down at about 4 V. The drain current could only be modulated by about 4 mA with a maximum gate bias of -4 V. This problem is believed to be caused by difficulties of growth of the active layer over the insulating region and associated interface problems.

Wafer NCT-5 was also fabricated using oxygen doping to obtain semi-insulating material for the buried-insulating-layer. After alloying of the drain contact, the current was about 140 mA so the wafer was lightly etched in 10 methanol: $2H_3PO_4$:$1H_2O_2$ which reduced the current to the range of 80-120 mA. After gate formation, however, the measured saturation current I_{dss} was in the range of 2-10 mA. This large decrease

of current occurring at the gate deposition stage is not ordinarily observed. One possible explanation is that the higher current measured before gate deposition was carried in a heavily-doped layer near the surface and that the slight amount of thinning that occurs normally during gate fabrication due to cleaning, sputter etching, etc., thus greatly reduced the current. In spite of the reduced saturation, wafer NCT-5 exhibited drain breakdown voltage in the range of 3 to 6 V for positive drain bias as shown in Fig. 9. Several transistors were assembled from this wafer and tested with the results shown in Table II. Curve trace characteristics of transistors from NCT-5 are shown in Figs. 9 and 10.

The calculated f_{max} from the measured admittance data was 7 GHz for Unit 1 and 8 GHz for Unit 3. The poor performance of transistors from NCT-5 can be attributed to low transconductance, high input capacitance, and high output conductance. In fact, input conductance (Re y_{11}) and the imaginary part of y_{21} are also significantly higher for these transistors compared to equivalent-width coplanar GaAs transistors. These differences can all be traced to the properties of the buried-insulating-layer. In particular, the apparent increase of g_{ds} with frequency is not observed in devices fabricated on Cr-doped semi-insulating GaAs substrates and is indicative of shunting the output with a high capacitance RC-series branch.

The parasitic capacitance of the gate bonding pad over the buried insulating layer was calculated to be about 0.04 to 0.06 pF for a 10-micron deep insulating region. However, measurement of input capacitance for transistors from NCT-1,

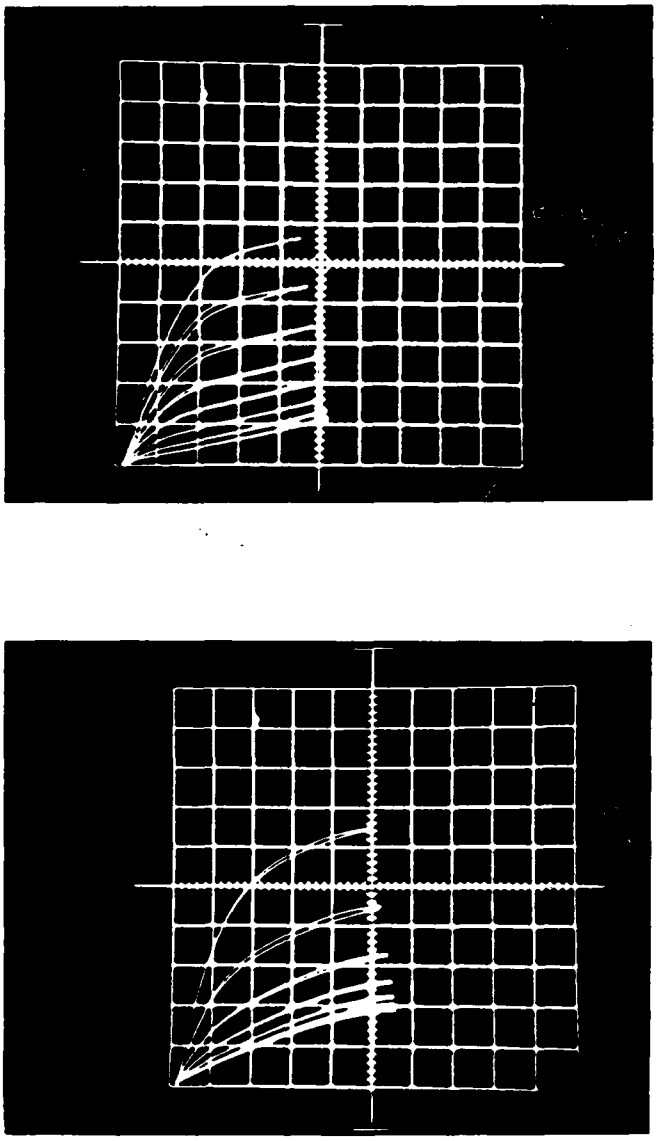


Fig. 9. Drain I-V characteristics from wafer NCT-5 units 1 and 3. Horizontal: 1 V/div, vertical: 2 mA/div (upper) and 1 mA/div (lower). Gate voltage steps 0.5 V.

TABLE II: NCT-5 Characteristics

1. Curve trace, R_s, and C_{gs} (1 MHz).

Unit	I_{dss}(mA)	V_{dss}(V)	g_m(mmho)	V_p(V)	R_s(Ω)	C_{gs}(pF)
1	9.6	1.6	4.4	4*	40.	0.39
2	2.4	1.2	1.5	2*	58.	0.40
3	4.8	1.4	4.0	3*	4.8	0.66
5	10.0	1.6	3.0	3*	16.	0.42

2. Microwave Network Analyzer (admittance in mmho).

	Im $y_{11} \approx \omega C_{in}$		Re $y_{21} \approx g_m$		Re $y_{22} \approx g_{ds}$	
f(GHz)	1	3	1	3	1	3
2	5.2	6.0	4.5	5.9	0.65	0.52
3	6.7	8.2	4.4	5.6	0.81	0.70
4	9.3	11.5	4.4	5.6	0.99	0.89
5	12.2	15.3	4.9	6.4	1.69	1.69
6	14.0	18.0	4.9	6.3	2.05	2.16
7	18.1	23.2	5.1	6.4	2.67	3.29
8	21.8	28.3	6.4	8.1	4.27	5.10
9	25.6	32.9	6.4	7.8	7.67	9.81
10	28.7	37.0	7.6	8.7	15.22	22.14

3. Amplifier data:	1	3
G(dB) at 4 GHz	3.	5.

*Does not pinch off completely.

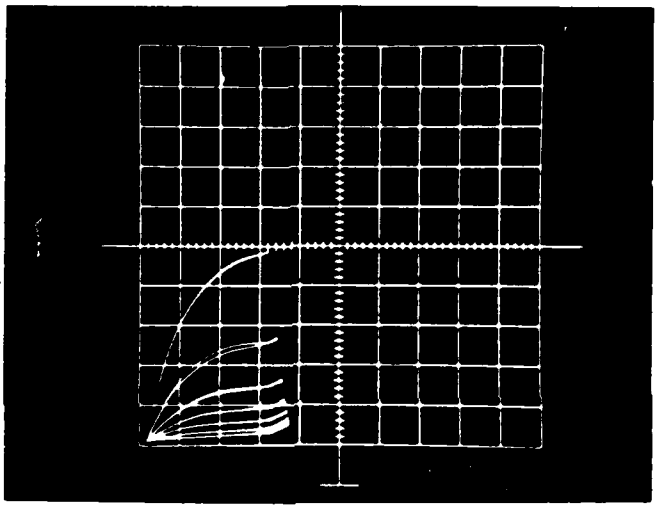


Fig. 10. Drain I-V characteristic of wafer NCT5-2. Horizontal 1 V/div, vertical 0.5 mA/div, gate voltage steps 0.5 V.

3, and 5 indicates a range from 0.4 to 0.6 pF. The gate capacitance over the active layer is about 0.2 pF for n-layer doping of 1 x $10^{17}cm^{-3}$. Therefore, the excess capacitance ranges between 0.2 and 0.4 pF or a factor of 3 to 10 higher than estimated. Three effects may be contributing to the increase of parasitic capacitance as follows:

(1) uneven polishing of the wafer surface after buried-insulating-layer growth;

(2) excessive vapor etching prior to active layer growth;

(3) out-diffusion of donor impurities from the n^+ substrate into the buried insulating layer during active layer growth.

The most straightforward solution to the excessive parasitic capacitance is to use deeper insulating regions under the gate and drain-bonding pads, minimize the bonding-pad size through improved wire-bonding techniques, and minimize high-temperature processing during active layer growth.

Drain breakdown also was a major problem for the non-coplanar FETs fabricated. This problem reflects on the breakdown characteristics of the oxygen-doped semi-insulating layer. Breakdown in semi-insulating GaAs has been studied by Haisty et al.[8] Undoped semi-insulating GaAs was shown to break down at the trap-filled-limit (TFL) as predicted by Lampert.[9] Only Cr-doped semi-insulating GaAs was shown to exhibit high breakdown under conditions of electron injection. More recently, the compensation mechanism of semi-insulating GaAs has been studied by Eisen et al.[10] Their conclusion is that both Cr and O doping are required to

produce semi-insulating GaAs for which the Fermi level remains pinned at mid gap under injection of either holes or electrons. These studies appear to be relevant to the present work. The circumstances of drain breakdown under positive bias are quite analogous to the TFL breakdown observed in undoped semi-insulating GaAs.[8] The n^+ substrate would be injecting electrons into the oxygen-doped material under this bias condition. Under negative drain bias, the active layer would be attempting to inject electrons into the insulating material but the effect would be weaker due to lighter doping of the active layer compared to the substrate. Therefore, the TFL breakdown for negative drain bias would be substantially higher than for positive drain bias as observed. Since oxygen is a deep donor in GaAs[11] and since it must be weakly ionized (there are very few free electrons in the insulating layer), there are few electron traps (ionized oxygen donors) available in the insulating region. Therefore, the TFL is reached for a small electron injection under appropriate bias conditions and the device breaks down. The solution, of course, is to dope the insulating layer with Cr to provide a deep acceptor to trap the injected electrons or alternately to dope with O plus a shallow acceptor at sufficient density to raise the TFL voltage. It is interesting that oxygen doping will produce insulating GaAs which is not, however, very useful for FET fabrication due to low breakdown voltage.

The other major problem observed in fabrication of buried-insulating-layer, noncoplanar FETs appeared to be associated with the interface properties between the insulating region and the active epitaxial layer (NCT-4). Various interface problems are notorious in the growth of

FET material, even onto Cr-doped GaAs substrates. However, growth of uniformly-doped active layers with high quality (abrupt) interfaces with the insulating regions in the noncoplanar geometry presents unique problems due to the presence of adjacent heavily n^+-doped substrate material. The magnitude of this problem is not apparent since only one of the 5 wafers exhibited a serious modulation problem. Various modifications of VPE growth procedures or the possibility of LPE growth of the final layer offer alternative approaches to minimizing the autodoping from the n^+ material and obtaining high quality interfaces.

Summarizing, the problem areas encountered with the design of Fig. 2 were low drain breakdown voltage for positive drain bias, excess parasitic capacitance and conductance on the input and output of the transistor, and non-zero pinchoff currents.

3. BASIC MATERIALS DEVELOPMENT FOR THE COMMON-GATE BURIED-INSULATING-LAYER NONCOPLANAR POWER FET

Figure 11 shows the proposed noncoplanar power FET structure investigated next. This structure will not have the space-charge-limited current shunt around the gate that the common-source buried-insulating-layer FET had problems with. Neither will it need the mechanical polishing step to level off the regrown tubs, which in turn uncontrollably thinned these regions and resulted in large parasitic capacitances. Although the structure in Fig. 11 has regrown tubs, no intimate photolithography contact is needed to form small gate lengths after their formation, and anyway their small size would result in little, if any, overgrowth above the surface. The use of ion-implantation to form the insulating tubs is not feasible because of sideways channeling which would increase the gate resistance and maybe pinch it off.

Figure 11 also offers the following advantages in addition to those accorded to a noncoplanar structure:

(1) Drain swing out to V_B (drain-to-gate breakdown voltage) rather than $V_B - V_{pinch\text{-}off}$.

(2) Reliability of a p-n junction gate (e.g., no metal migration, etc.).

(3) Possibility of increased doping away from the gate for better linearity without compromising source contact resistance.

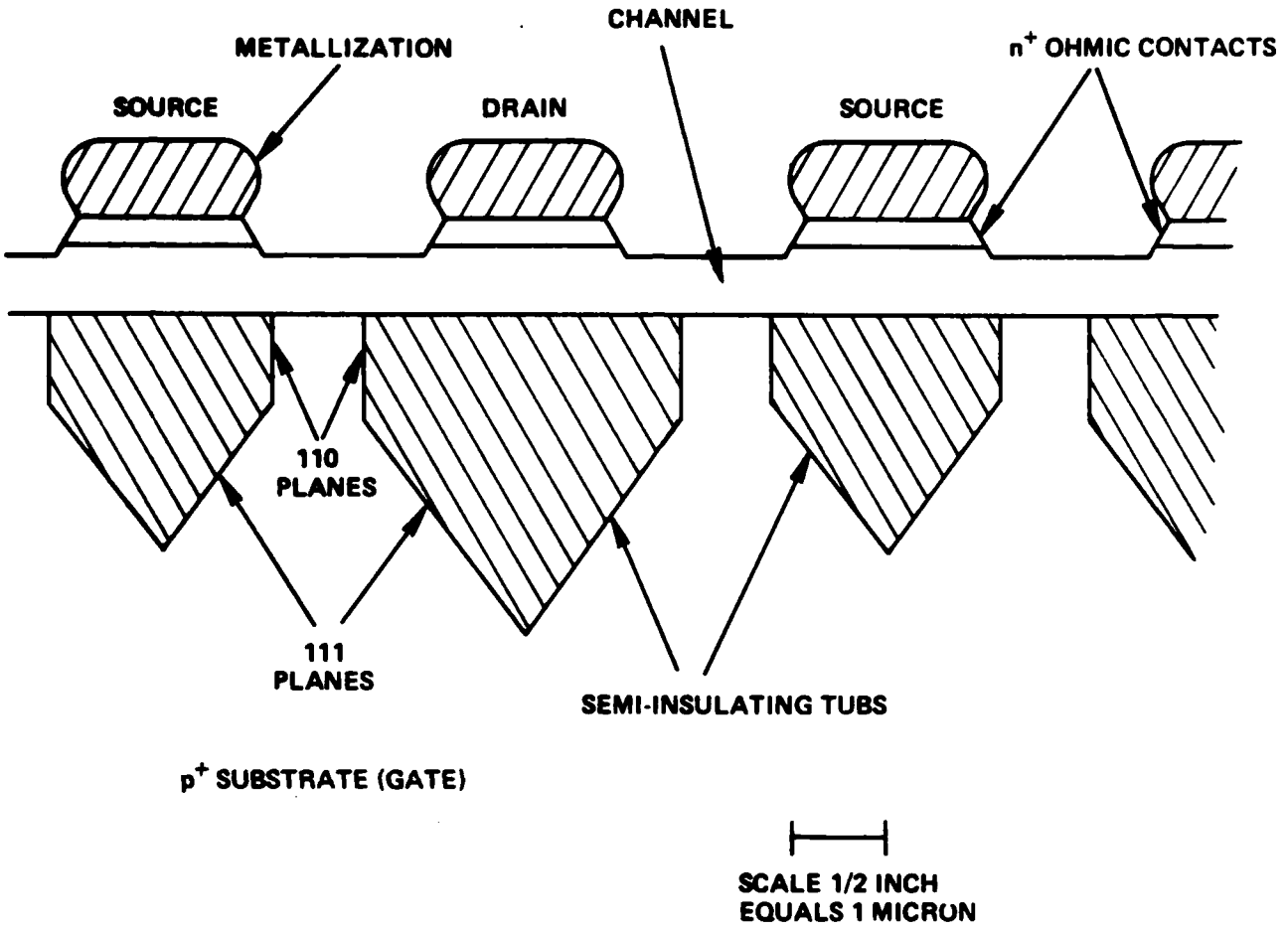


Fig. 11 Back-Gated Junction FET.

(4) Gate lengths less than the resolution limit of the photolithography masks employed.

(5) Small die size which means thinner substrates and better heat sinking.

(6) Ability to thin the channel after the gate formation (processing advantage).

(7) No signal propagation phase delays as encountered with long metal gate stripes.

While retaining the tub growth technology developed during the first phase of this contract, the new structure incorporates features that should render it a more reliable and higher power device.

3.1 Gate Trough Etch and Growth

As shown in Fig. 11, those portions of the substrate under the source and drain contacts are to be etched away and refilled with insulating or low-doped material. This will not only reduce the parasitic capacitance of the source and drain to the gate, but will determine the gate length provided the spacing of these regions is less than the source-to-drain spacing. Since the best growth will occur if the etching is also done in situ in the vapor-epi reactor, this approach was investigated initially.

This study was initially carried out using n^+ Te-doped substrates as the p^+ Cd-doped substrates to be used were still on order.

3.1.1 Gate Trough Orientation Determination Using Vapor Etch

The fabrication of the gate trough involved a detailed study of the etching behavior of various GaAs planes by HCl vapor in an $AsCl_3$ vapor-epi reactor, using different temperatures and flow rates.

The $Ga/AsCl_3/H_2$ system employed a high purity Spectrosil quartz reactor tube mounted horizontally with the $AsCl_3/H_2$ line entering at the closed end to saturate the Ga source. An etch line connected to the $AsCl_3/H_2$ line with a set of valves bypassed the source and entered the reactor ahead of the substrate. For an $AsCl_3$ bubbler temperature of 20°C, the background doping of the system was $10^{15} cm^{-3}$.

On planar etching with the wafers partially covered with an SiO_2 layer, the etching rates at 750°C were found to be in decreasing order:

$$(110) > (100) > (111)A > (111)B$$

and in the ratio of 2.5 : 1.32 : 1 : 0.66 with typical $AsCl_3$ mole fractions. All wafers were chemically polished damage-free before SiO_2 deposition, and the A and B faces were distinguished by their reactions to a Br-methanol etch. The order found agrees with crystallographic intuition since the (111) plane is the most densely packed with lowest surface energy and (110) is the least densely packed with the largest surface energy. The etch rate of the (111)A plane is larger than the (111)B plane as the As-rich face has a lower surface energy due to the larger size of the As atom.

To simulate the gate trough, line etches on different planes were studied using 2- to 3-micron lines photolithographically etched in SiO_2. After polishing and an H_2SO_4:H_2O_2:H_2O (4:1:1) etch, a 1500-Å thick SiO_2 layer was grown on the substrate and the pattern was etched in the SiO_2 photolithographically. The etching order derived from the observation of these etches can be deceptive as interface effects and gas flow kinetics tend to interfere with ideal etching relationships and slow and fast etching planes can co-exist in the early stages of etching.

For a mask about 3-microns wide, aligned along the <100> direction on the (001) wafer plane of GaAs, there was a considerable amount of under-etch below the SiO_2 mask and the (110) planes predominated as is seen in the scanning electron microscope photo in Fig. 12. Figure 13 is an optical picture of two 2.8-micron-wide mutually perpendicular lines aligned along the <110> and the <1$\bar{1}$0> directions on the (001) plane and Figs. 14 and 15 are scanning electron microscope pictures of the two lines. The etched groove in one case has vertical walls of (110) planes, together with (111)A planes terminating in a (100) plane as shown in the SEM picture in Fig. 15 and by the sketch in Fig. 16. The etched groove is the type depicted in Fig. 11, but Fig. 15 shows an undercut of about a micron on both sides of the SiO_2 mask of 2.8-micron width when etched 5-microns deep. The other etch line in the <110> direction does not show any significant undercut, although the (111)B planes terminate this etch in a V-groove as seen in the SEM picture in Fig. 14.

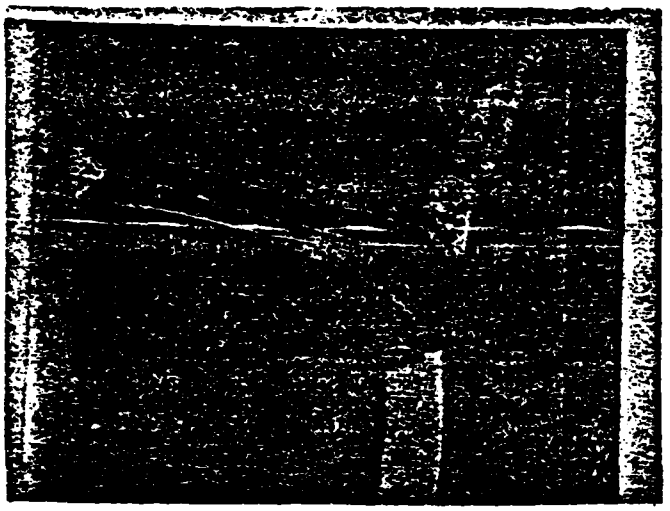


Fig. 12 SEM picture of etch along (100) direction on (001) plane. (1040x)

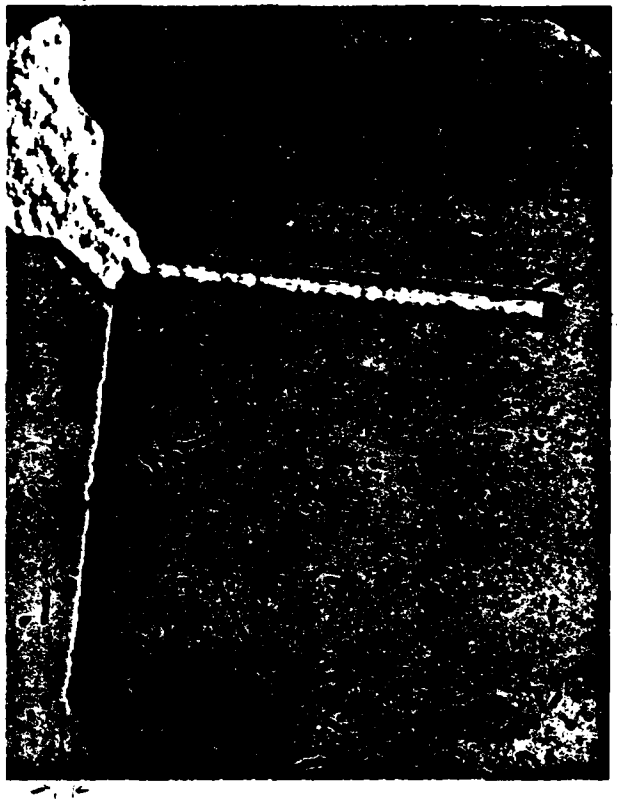


Fig. 13 Optical picture of etch on (001) plane along the <110> and <1$\bar{1}$0> directions. (~400x)

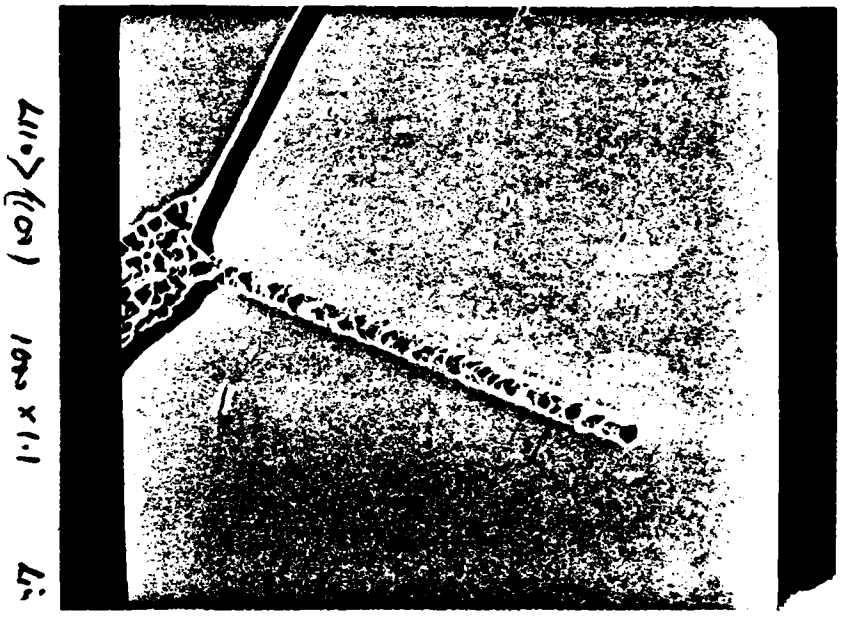


Fig.14 SEM picture of etch on (001) wafer along the $\langle 1\bar{1}0 \rangle$ direction. Etch depth 5 microns. (1040x)

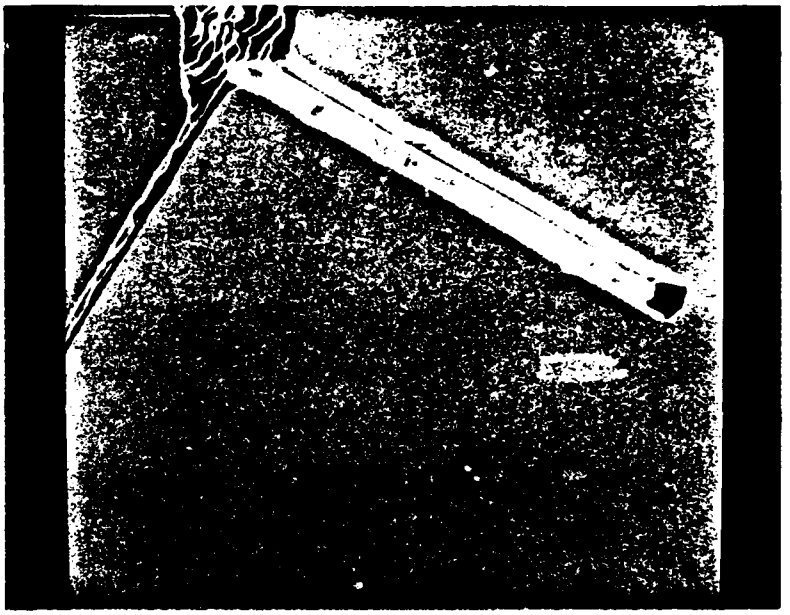


Fig. 15 SEM picture of etch on (001) wafer along the ⟨110⟩ direction. Etch depth 5 microns. (1040x)

To simulate the effect of adjacent gate troughs, a "Photronic Labs" resolution mask with the smallest pair of lines about 3-microns wide and about 1.5-microns apart was then used to achieve the pattern on 1500 Å thick SiO_2. The wafer could now be etched in-situ, in an $AsCl_3/H_2$ flow divided between the etch line and the source with the substrate at 750°C, anywhere between 5 to 9 min and still get the complete V-shaped groove. Using a 9-1/2 min etch time the undercut below the SiO_2 mask could be made such that the grooves are as little as 0.2 micron apart. Figure 17 shows the etched lines along the $<1\bar{1}0>$ and the <110> directions, and Fig. 18 shows the cleaved section of the wafer showing the etched grooves along the $<1\bar{1}0>$ direction. Although the etch was about 8-microns deep in the larger grooves, the smaller pair of lines only etched about 2-microns, as seen from Fig. 18. Figures 19 and 20 show the control that can be attained in etching these grooves. Figure 20 is the cleaved section of the surface shown in Fig. 19. The two small pairs of grooves are about 0.2-microns apart.

Etching the $(1\bar{1}0)$ plane surface of GaAs with groove directions along <110>, <001>, <112>, and $<11\bar{1}>$ did not show any direction with the desirable groove shape, and undercut was always excessive. Wafers with (111) surfaces are unsuitable because of the asymmetric etching rates on either side of the trough. The (001) plane of GaAs was therefore chosen with the groove direction along $<1\bar{1}0>$ as giving the most suitably-shaped V-groove, whose etch was easily controlled and reproducible. For the same gate length, the V-shaped sides will mean a lower gate resistance as compared with the vertical sides shown in Fig. 11. Also, less field crowding at the corners should increase the breakdown voltage.

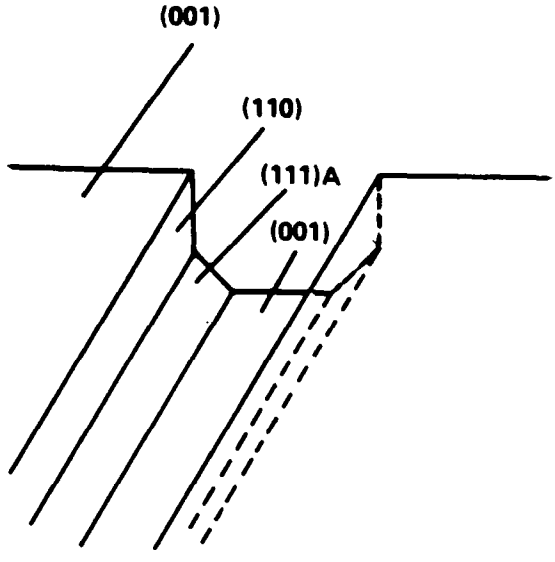


Fig. 16 Planes participating in etch along the <110> direction.

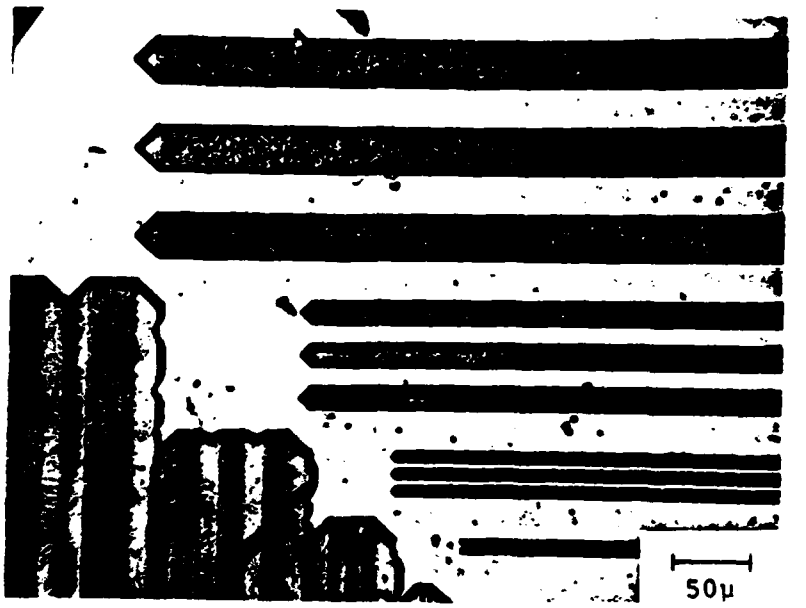


Fig. 17 Etched lines along the <1$\bar{1}$0> and the <110> direction.

Fig. 18 Etched grooves along the <1$\bar{1}$0> direction.

Fig. 19 Magnified portion of Fig. 17.

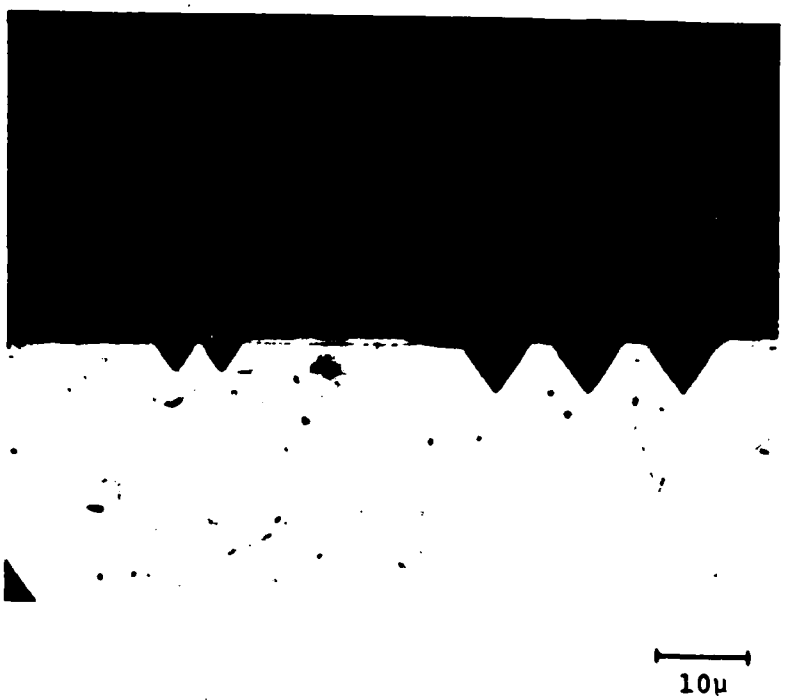


Fig. 20 Cleaved section of Fig. 19.

3.1.2 Gate Trough Growth

Figure 21 shows the etch and growth on the (001) plane for mutually perpendicular mask lines. The controlled undercut of the $<1\bar{1}0>$ direction is again readily apparent.

Etch and growth of CVD GaAs on the (001) surface was then attempted for adjacent V-grooves along the $<1\bar{1}0>$ direction. Figure 22 shows the smallest pair of grooves on the resolution mask etched for 7 minutes with a vapor growth of 3-1/2 minutes. The final surface is seen to be (100). Figure 23 shows the larger lines etched and filled in the same run as shown in Fig. 22. The growth plane in this figure is the intermediate plane in the growth series and is (311)B.

Growth rate of vapor phase GaAs on GaAs substrates is in decreasing order on planes {111}A > {211}B > {311}B ≈ {311}A > {100}. The growth rate on {111}B planes is negligibly small as compared to other planes. Hence in the long groove terminating in the 111 B planes when aligned along the $<1\bar{1}0>$ direction on the (001) plane, growth essentially starts at the {211} B planes and continues next to form {311} B planes and on to form the higher index planes, ultimately ending in the {100} plane. Figure 24 shows a sketch of the successive growth of the planes.

In order to simulate more closely the V-groove center-to-center spacing of 4-microns and also facilitate the study of variations over the wafer surface, a mask was

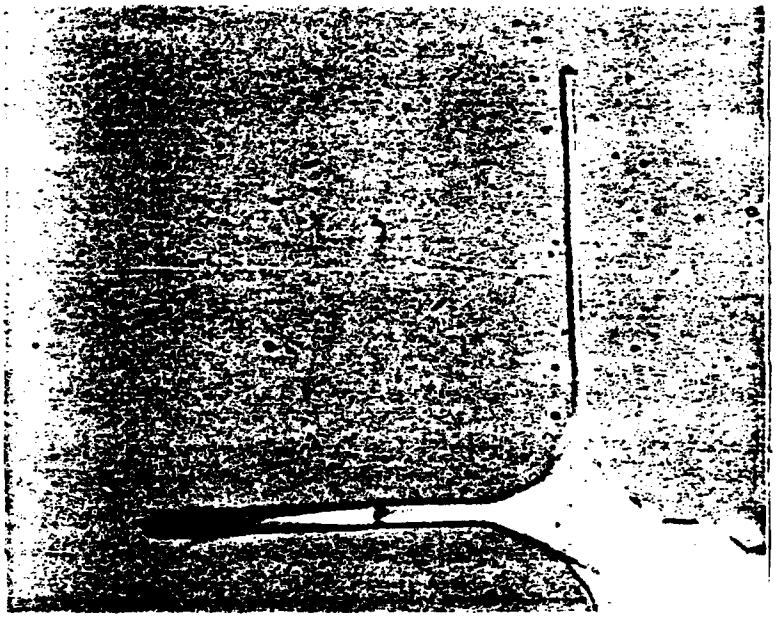


Fig. 21 Etch and growth on (001) plane along the (110) and ($1\bar{1}0$) directions. (544x)

Fig. 22 Etching and regrowth in V-grooves.

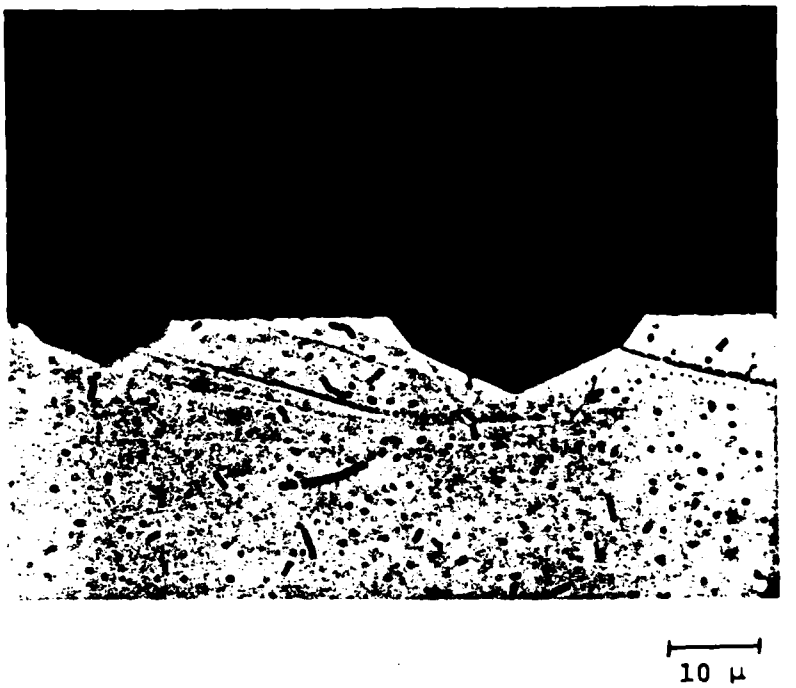


Fig. 23 Intermediate growth in the grooves illustrating the kinetics of growth.

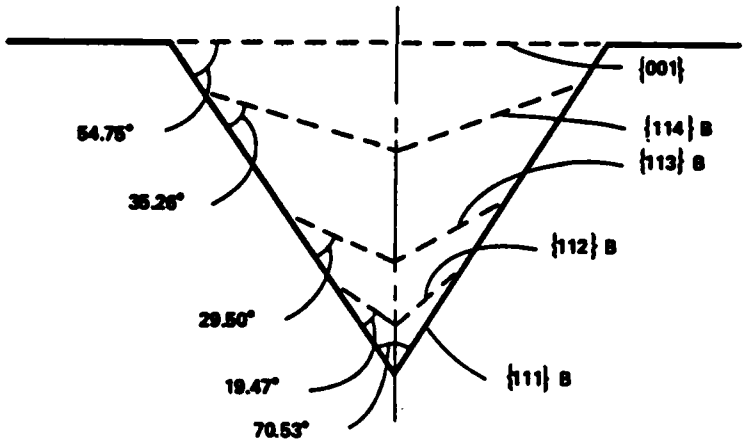


Figure 24 Growth of GaAs planes in the $[1\bar{1}0]$ directional groove bounded by {111}B planes.

made with 2-micron gaps and spaces extending the full width of the mask. The starting wafer of (001) GaAs was provided with 1500 Å thick SiO_2 stripes 1.3-microns wide produced by the usual photolithographic technique. These were 4-microns apart and along the proper [110] direction as shown in Fig. 25. The vapor etching was done by bubbling H_2 through the $AsCl_3$ bubbler at 20°C and directing half the flow through the Ga source at 825°C and the other half through the etch line. The substrate was at 760°C. Figure 26 shows the cleaved section perpendicular to the grooves vapor-etched at a total flow rate of 420 cc/min for 10 min. A few of the grooves in this wafer were large as shown in this figure. Such large grooves are due to coalescence of adjacent grooves and can form due to (1) over-etching, (2) variation in the widths of the SiO_2 stripes or (3) when a few of the SiO_2 stripes come loose from the substrate due to poor adhesion. The size of the groove was also larger at the upstream end than at the downstream end suggesting depletion of HCl from the gas stream as it passed over the wafer. Figure 27 shows the refilled grooves with a 4-min etch and a 2-min growth at a flow rate of 420 cc/min. After refilling the grooves, the SiO_2 layer was removed and a 10^{17} Sn-doped GaAs layer 2500 Å thick was deposited. The cleaved section of such a wafer is shown in Fig. 28. The top surface of the wafer is shown in Fig. 29. The contrast is due to the small difference between the surface of the refilled region and the original wafer surface and allows alignment of the gates. Figure 30 shows a thick Sn-doped GaAs layer (1.2 microns) and demonstrates that such a layer can be grown on the "vees" with a minimum amount of vapor-etch prior to deposition.

Summarizing, the etching can be stopped just at the moment when the adjacent edges of the "vees" meet and the

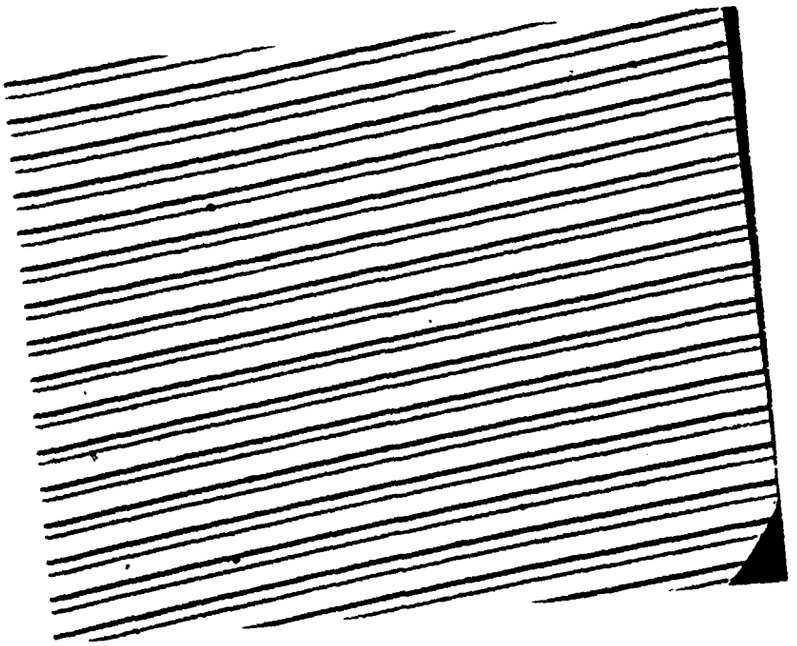


Fig. 25 SiO_2 mask pattern having a 4 micron period for purposes of studying vee etch uniformity (1400x).

Fig. 26 Vapor etched grooves using the mask pattern of Fig. 25 (1400x).

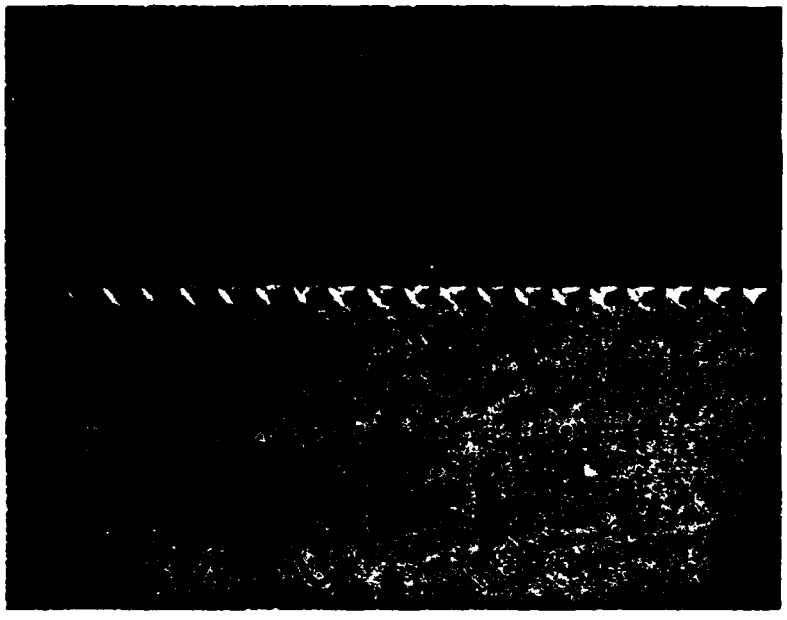


Fig. 27 Refilled grooves (1400x).

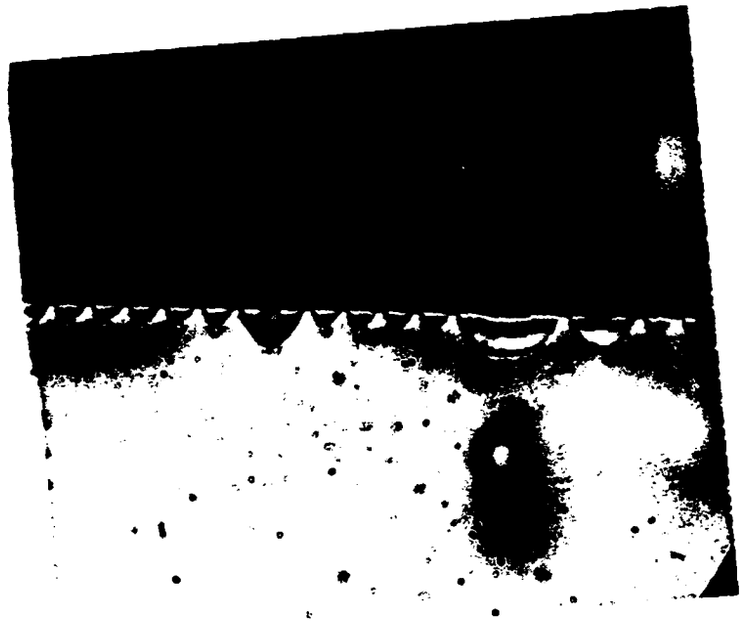


Fig. 28 Active layer growth over the refilled grooves (1400x).

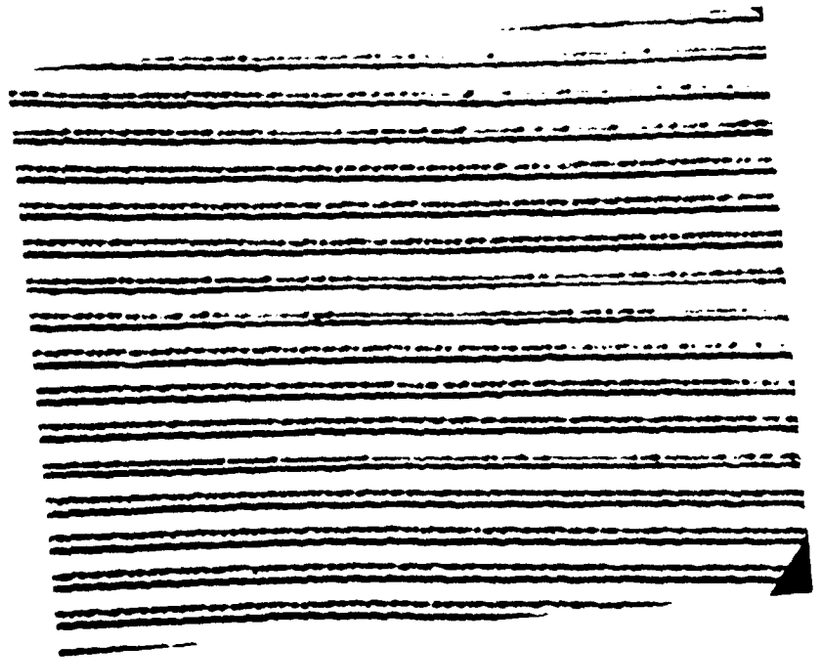


Fig. 29 Top surface of Fig. 28 (1400x).

Fig. 30 Thick active layer growth (3766x).

"vees" can be refilled to be flush with the initial surface of the wafer. It has also been shown that after removing the SiO_2 layer from this wafer, a thin layer of GaAs, Sn-doped to $10^{17}/cm^3$, could be deposited on the wafer with a minimum of etching prior to growth. Further work showed that this technique was fairly reproducible although quite sensitive to a number of variables such as source size, amount of deposits in the deposition zone of the reactor, the width of the SiO_2 windows and the quality of adhesion of the SiO_2 lines to the substrate surface. Although the optimum conditions of etch and growth appear to be different every time the Ga source is changed, these could be determined in about 4-6 experiments. To control the width of the SiO_2 windows, a new wafer polishing technique using dilute sodium hypochlorite was instituted. This produces a much flatter wafer surface compared to that obtained using the Br-methanol polishing technique and allows the mask to make contact over a larger area during the photolithographic process.

3.1.3 Gate Trough Etch and Growth Using Cd-doped GaAs

Cd-doped substrates were received from Metal Specialties having a (100) surface and a doping range of 3-9 x $10^{17}cm^{-3}$. The processes developed using the n^+ Te-doped substrates were repeated on the Cd-doped substrates to ensure their viability, and showed that the etching behavior of Cd-GaAs is quite different from Te-GaAs in two respects:

(1) The Cd-GaAs etches faster than Te-GaAs. To produce the right size vees, the etching time was found to be five times smaller for Cd-GaAs than for Te-GaAs. This

was confirmed by placing Cd-GaAs and Te-GaAs side by side in the reactor. When the latter etched to produce perfect vees, the former was very much overetched. Gannon and Nuese[12] observed that the etch rate is dependent on the dopant in the substrate as well as the doping level with a solution etch. Contrary to VPE etching, however, they found that with $NH_4OH:H_2O_2$ that n-type GaAs etched faster than p-type GaAs.

(2) After the adjacent vees have joined and the SiO_2 stripes have fallen off, the protrusions in Cd-GaAs etched only slowly. This resulted in the vees gradually flattening out to produce a planar surface instead of coalescing as in Te-GaAs. This is shown in Fig. 31. This behavior suggests a difference in the ratio of the etching rates for (001) and (111)B planes. This ratio may be quite small for Cd-GaAs compared to Te-GaAs so that the protrusions get etched away fast in Te-GaAs.

After the vees are etched by the right amount, they may be refilled with GaAs just as in the case of Te-GaAs. Figure 32 shows a wafer with the vees refilled with undoped GaAs.

The different etching characteristics for the "vees" on the p^+ material prompted redoing the etch and growth experiment for the areas under the source and drain bonding pads. A quick etch experiment revealed that, as for the n^+ material, the <100> directions are the next slowest, and pattern edges aligned along the <100> directions gave only about 2 microns of oxide undercut for an etch depth of 5.5 microns. The device edges were thus chosen to lie along the <110> and <100> directions.

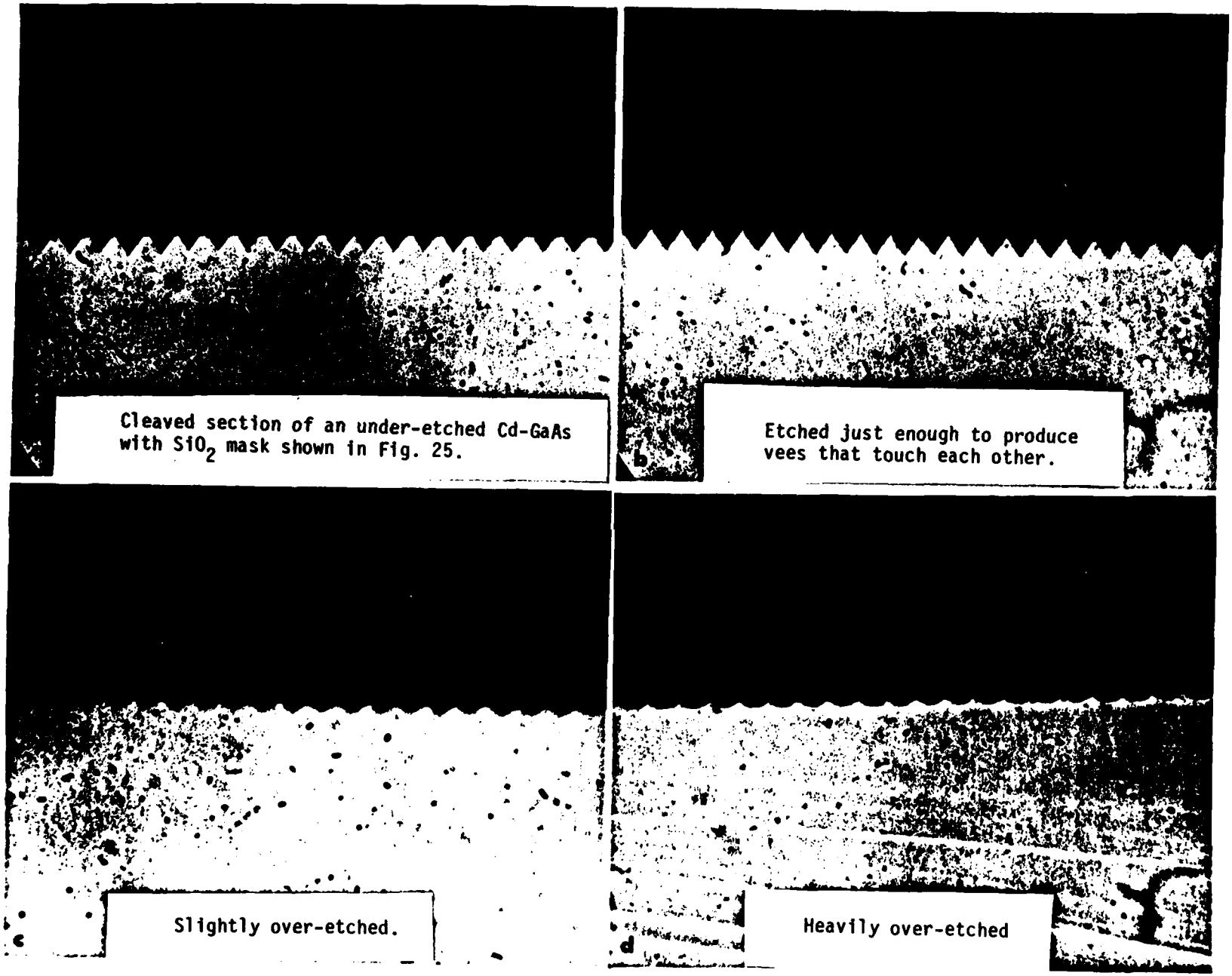

Cleaved section of an under-etched Cd-GaAs with SiO_2 mask shown in Fig. 25.
Etched just enough to produce vees that touch each other.
Slightly over-etched.
Heavily over-etched

Figure 31

Fig. 32 Cleaved section of Cd-GaAs etched and refilled with undoped GaAs.

3.2 Mesa Definition and Field Growth

Besides the insulating "vees" under the active source and drain electrodes, insulating regions must be provided under the source and drain pads and the connecting metallization. This is analogous to the mesa etch used for devices fabricated on a semi-insulating substrate, and must not only insulate but also provide low capacitance to the underlying p^+ substrate. However, edges along the <110> direction perpendicular to the "vee"-direction undercut the oxide mask around 20 microns while etching down only 7 microns, and hence are not desirable edges for device fabrication. However, edges at 45° to the <110> directions were found to undercut only around 2 to 4 microns while etching to a depth of around 10 microns. Accordingly, the source and drain pads and interconnection lines were chosen to have their edges aligned at 45° to the <110> directions. These will have to be filled with GaAs in a separate run, however, since the time to fill these is quite different from the time to fill the "vees".

In the time needed to fill the "vees," the deposits in the pad area are only about 2 microns thick. Therefore these will have to be filled with semi-insulating GaAs in a separate run. The conditions of etching and refilling of the pad areas were established using a GaAs wafer containing pad areas and lines as in Fig. 33. The cleaved section of a vapor-etched and grown pad is shown in Fig. 34. The surface of the refilled pad is always a little above the wafer surface because of the way in which the pad area is filled. The height of the mesa is a function of the width of the SiO_2

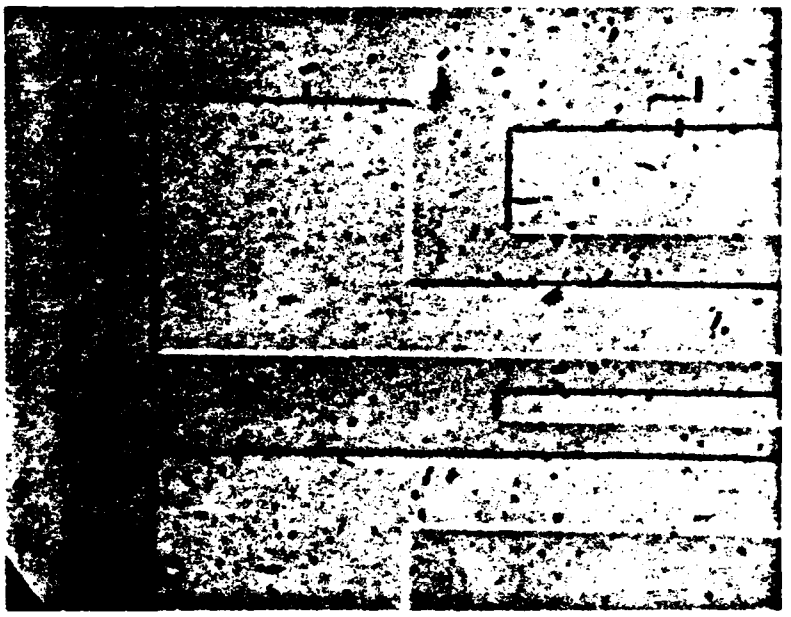


Fig. 33 Pattern used to study field growth. (290x)

Fig. 34 Field etch and growth profile using pattern of Fig. 33 (1400x).

opening and should be quite small (of the order of a micron) in the actual device.

Although the "vees" need only be low-doped to perform well, it is imperative that the field growth be insulating lest there be parasitic conduction between the source and drain contacts. Consequently, Cr-doping must be employed in the field growth.

3.3 Substrate Autodoping Problems

3.3.1 High Background Doping of Cd-doped Substrates

Having corrected the temperature profile along the Ga source and with new CrO_2Cl_2 in the bubbler, the reactor background doping was about 3-4 x $10^{14}/cm^3$ and the undoped layers on Cr-doped substrates had mobilities of 8400 and 60,600 cm^2/V-sec at 300 and 77°K. Since a background doping of about $10^{15}/cm^3$ is sufficient to produce good quality Cr-doped material (resistivity 10^7 - 10^8 ohm-cm) in the vapor phase epitaxial system, getting high resistivity material on Cr- or Te-doped GaAs test substrates was easily accomplished. However, there was no success at getting lightly-doped or semi-insulating GaAs on Cd-doped substrates. The layers (undoped as well as Cr-doped) on these substrates were relatively heavily doped (approximately in the $10^{16}/cm^3$ range) and p-type; even the layers on Cr-doped GaAs substrates inserted next to the Cd-GaAs during the VPE process turned out heavily p-type.

The impurity making the layer p-type has been verified to be Cd. There are a number of ways in which Cd can get into the epilayer:

(a) Solid state diffusion from the substrate into the epilayer during growth;

(b) release of Cd into the gas stream during vapor etching and subsequent contamination of the grown layer due to incomplete removal by the H_2 gas flow; and

(c) evaporation of Cd from the substrate surface due to its high vapor pressure.

The second and third mechanisms can dope the epilayers on the adjacent Cr-doped GaAs substrates also.

To reduce contamination due to the second mechanism, the vapor etching step was eliminated and a previously-saturated Ga source was used. A typical run under these conditions consisted of a thermal equilibration period (15 min) followed by the epitaxial growth to produce an epilayer about 8 microns thick. But this did not reduce the background doping by any significant amount.

To prevent the release of Cd from the back side of the wafer and from its edges, a thick layer of silicon nitride (about 6000 Å) was deposited. The undoped GaAs layer deposited on such a wafer was still heavily p-type, indicating that:

(a) 6000 Å thick Si_3N_4 does not prevent the loss of Cd from the surface of GaAs, and/or

(b) the Cd lost from the front surface during thermal equilibration and during the early stages of

deposition of the VPE layer "poison" the liner and the substrate holder and dope the epilayer continuously.

An attempt was made to solve the second problem by using a more elaborate growth procedure involving (1) growing about 4 microns of undoped GaAs, (2) removing the substrate holder-push rod assembly from the reactor, (3) placing the wafer in a clean assembly, and (4) depositing a second 4-micron thick layer. The top layer on the Cd-GaAs substrate (with Si_3N_4 on the back and edges) was still highly doped in this case, although the corresponding layer on the neighboring Cr-GaAs was extremely lightly doped. With the addition of Cr to the system during the second stage of growth, only the layer on the Cr-doped GaAs was semi-insulating. From these experiments, it appears that layers grown on Cd-doped substrates cannot be made semi-insulating. Although the diffusivity of Cd in GaAs is nominally very low,[13] anomalously high doping of the epilayer results even for epilayer thicknesses of about 10 microns.

3.3.2 Background Doping Investigations Using Ge-Doped Substrates

Experiments using substrates of Ge-doped (p^+) GaAs grown by the liquid phase epitaxy technique on Cr-doped GaAs indicated that very good quality undoped (as low as $10^{14}/cm^3$) and Cr-doped layers could be obtained on Ge-doped GaAs. The main drawback of Ge doping is that bulk crystals grown by the Czochralski technique are n-type. The requirement that Ge-doped GaAs be grown by the LPE technique on some other p-type GaAs substrate, however, has the advantage

that the quality of the material on which the device will be fabricated will be higher than Czochralski-grown substrates.

Further experiments were performed on VPE deposition of lightly doped n-type GaAs on Ge-doped (p^+) GaAs, the latter being grown by the liquid phase epitaxial technique on Zn-doped (p^+) GaAs. While some of the epilayers were lightly doped ($N_D - N_A \approx 1 \times 10^{15}$/cc), there was difficulty reproducing these results. More often the epilayers were p-type doped to low 10^{16}/cc. The epilayer dopant making it p-type must be Zn since Ge-doped layers in the VPE system are n-type. The high diffusion coefficient of Zn in GaAs should not be a serious problem since the Ge-doped GaAs layer was quite thick (about 10 microns). Coating the back side and the edges of the wafer with thick Si_3N_4 to prevent outward diffusion of Zn improved the situation somewhat; but still the epilayers were sometimes p-type and sometimes n-type, doped to mid-10^{15}/cc. These values were unsatisfactory, since the epilayer must be about $1 \times 10^{15} cm^{-3}$ or lower and n-type for Cr doping. The Zn-doped GaAs used for these experiments was doped to $10^{19} cm^{-3}$. Since the device does not need such a highly doped substrate, it was decided to lower the doping level of the substrate to see if the quality of the epilayer improved. Even if lower Zn-doped substrates were not able to solve the problem, two options remained:

(1) Use thick (50 microns or so) Ge-doped p-type GaAs grown by LPE on Cr-doped GaAs as the substrate. High purity material may be grown on this, as per the preliminary experiments. After the device is fabricated, the Cr-doped GaAs substrate can be removed by preferential dissolution (a technique commonly employed in our lab for making photocathodes).

(2) Use a bypass reactor to reduce the doping of the epilayer grown on the Ge-doped GaAs/Zn-doped GaAs substrates (or even on Cd-doped GaAs substrates). In this technique extra H_2+$AsCl_3$ is admitted into the VPE reactor at a point after the Ga source and before the substrate. The extra HCl in the deposition zone reduces the incorporation of impurities into the epilayer while at the same time lowering the growth rate somewhat. Nozaki et al,[14] who first described this technique, observed that the doping can be lowered from $10^{16}/cm^{-3}$ to $10^{12}/cm^{-3}$. It seems fair to assume that the technique will work for p- as well as n-type dopants. Initial experiments using Cd-doped GaAs substrates show that by using this technique the 7-micron thick epilayer was n-type doped to 1 x $10^{15}cm^{-3}$, which contrasts with the p-type epilayers doped to above $10^{16}cm^{-2}$ on Cd-GaAs using the ordinary VPE system.

Using the new batch of substrates, Ge-GaAs layers 30 microns thick were grown by LPE. Pieces cut from these were coated with Si_3N_4 on the back and the edges. Undoped epilayers grown on these pieces were clearly shown to be n-type doped to $10^{15}cm^{-3}$. Attempts to Cr-dope the epilayers were unsuccessful initially. The problem was later traced to a faulty mass flow controller supplying H_2 to the CrO_2Cl_2 bubbler. After repairing this, the epilayers on Ge-GaAs/Zn-GaAs were successfully Cr-doped. When the epilayer thickness was about 6 microns (corresponding to the tub depth), Cr-doping produced a net doping of less than $10^{13}cm^{-3}$ since the zero-voltage-capacitance on a 20-mil Au dot was less than 4 pF.

Realizing that the "vees" are only about 2 microns deep and that these will also have to be filled with high resistivity material, attempts were then made to grow Cr-doped layers 2 microns thick. In these cases, it was observed that although most of the top layer was lightly doped, the n-type doping appeared to increase upwards to at least $10^{17}cm^{-3}$ as the p^+ substrate was approached as indicated from the doping profile plots derived from the capacitance. Such a high n-doping right at the p^+ interface would lower the p-n junction breakdown voltage and increase the parasitic capacitances (thereby negating the function of the vee grooves, no matter how low a doping was achieved away from the interface). Since Ge diffusing into the grown region will produce p-type doping, any n^+ interface layer must be due to Ge contamination coming from the vapor phase (in which case it acts as an n-type dopant).

In order to be sure that the n^+ layer at the interface was not an artifact of the profiler (i.e. an anomally due to punch-through and excessive leakage stemming from the profiling depletion region edge metting with the depletion region of the underlying p-n junction), an n^+ layer was grown on top to facilitate ohmic contact and to prevent punch-through, and mesas were etched down to the p^+ substrate. This enabled the Cr-doped layer to be profiled from the p^+ substrate towards the surface. The low capacitance of the p^+/epilayer junction implied that the low doping at the surface continued all the way to the p^+ substrate. However, the diode dc characteristics were so unusual and uninterpretable (even to the point of showing SCR-type negative

resistance) that there was a little uncertainty in arriving at this conclusion. The negative resistance SCR characteristics appeared to be due to trapping effects in the Cr-doped layer and not due to some unintentially grown multilayer structure. (Negative resistance was also observed by Hasegawa, et al.[15] when they grew p-type Fe-doped GaAs by the LPE process on n^+ Si-doped substrates and concluded that this was related to the presence of a high density of iron hole traps). The low capacitance from the p-n junction side would suggest no n^+ layer adjacent to the p^+ substrate, but if this were true it seems difficult to explain why punch-through did not occur when profiled from the Schottky-barrier side.

The identical procedure of profiling with a Schottky-barrier and then etching mesas and profiling from the p^+ substrate side was carried out for an undoped buffer layer growth on the p^+ Ge-doped substrate (for this growth the doping was lowered by an $AsCl_3$ bypass around the source[14] rather than by Cr-doping). While at zero bias the layer was fully depleted with 12 pF of capacitance for the Schottky-barrier, but when profiled from the substrate side the zero-bias capacitance increased to around 30-40 pF. This implies an n^+ layer adjacent to the substrate, but not of such a magnitude as to seriously degrade device performance. It may be that the n^+ layer was completely compensated when the layer was Cr-doped, explaining why it was not seen previously.

3.3.3 Formation of Vees on Ge-doped Substrates

Since the surfaces of the LPE layers of Ge-doped GaAs were somewhat rough showing the typical terrace pattern, they were repolished with diamond paste and then

with Br-methanol. The entire polishing procedure removed about 10 microns, leaving about 20 microns of the layer. Using Si_3N_4, the mask for etching the vees was put on the repolished surfaces. Vapor etching in the reactor using techniques established previously (using Cd and Te-doped substrates) showed, however, that the etching proceeded sideways very fast to give shallow trapezoids rather than vees. This does not appear to be due to surface damage left during repolishing as indicated by experiments done on as-grown LPE surfaces. This was also found to be the case with SiO_2 as the masking material. Identical experiments using Te-doped GaAs produced the required grooves, leading to the conclusion that this behavior was peculiar to the Ge doping. Whether or not this is due to the interaction of Ge with SiO_2 or Si_3N_4 to produce GeO_2 or Ge_3N_4 (or more complex Ge-Si compounds with O_2 or N_2) is not known.

Experiments with $NH_4OH:H_2O_2:H_2O$ (20:7:1000 by volume) were successful in producing good vees with the mask aligned along the [110] direction perpendicular to that for the V-etch in the VPE system. The obvious advantage of this weak solution etch is that the etch rate can be controlled quite precisely to adjust the gate length (the separation between the adjacent vees), being more difficult to do with the vapor etch. Using the solution etch to produce the vees and the VPE system for the subsequent refilling, semi-insulating vees were obtained. With the grooves aligned in the perpendicular direction, growth proceeded from each end of the groove towards the middle rather than from the sides of the vees as it had previously. Incomplete growth thus manifested itself by completely empty vees in the middle portion of the grooves.

3.4 Active Layer Growth

The next step in the device fabrication is the VPE deposition of the n-type ($10^{17}cm^{-3}$) active layer on the Ge-doped substrates after removal of the SiO_2 or Si_3N_4 used as the mask for the vee etch and growth. This process is made more difficult compared with conventional device fabrication techniques owing to the requirement that the active layer must be grown with very little vapor etch of the substrate. Appreciable vapor etch to clean the substrate surface can lead to removal of the vees.

As an initial effort towards growing the active layer, "vee" patterns were etched and grown over the whole wafer using the mask pattern shown in Fig. 25 . A $10^{17}cm^{-3}$ Sn-doped active layer was then grown over the whole wafer after the oxide mask was stripped. No vapor etch was used for the active layer growth lest the "vees" be eliminated. During the source saturation a highly doped Sn layer grew until the source was saturated, after which the layer was allowed to be etched. At just the point the layer was etched off, the active layer was grown to the desired thickness. Figure 35 shows the resulting growth over the "vees".

This procedure of controlling the source saturation time so that a highly doped layer is grown and then just etched off was found to be too exacting to be practical. The alternative was to use a previously saturated source or to use a slider boat to cover the wafer during the source saturation.

Fig. 35 Active-layer growth over the refilled grooves.

Difficulties were experienced in growing a continuous active layer over the V-grooves by vapor phase techniques. Various surface cleaning procedures were tried along with a small amount of vapor etch, but the growth remained discontinuous independent of whether the source was previously saturated or a slider boat was used. It may be that a residue is left on the surface during the removal of either the SiO_2 or the Si_3N_4 mask (both were used). Such discontinuities provide shorting paths for the FET ohmic contacts directly to the substrate gate below, and also made it impossible to characterize the active layer for doping and thickness (a discontinuous active layer on an insulating substrate as used for coplanar devices would not have these problems).

When the surface of the wafer was Augered in the MBE system, carbon was seen on the surface. This could very well be the cause for the discontinuous growth. There is evidence that when the surface is lightly etched, the C is not removed but simply re-deposits, explaining why the various surface cleanings were ineffective. Evidently the severe vapor etch typically done before vapor growth for conventional FETs is able to remove this C. The C was sputtered off in the MBE system and an active layer was grown by MBE that was deemed acceptable for device processing. Schottky-barrier leakage, although much less than for the vapor-grown layers, still prevented evaluation of the active layer, so it may be that the layer still has discontinuities in it. Nevertheless, the decision was made to employ MBE active layers for the initial effort at actual device fabrication.

4. DEVICE FABRICATION DEVELOPMENT FOR THE COMMON-GATE BURIED-INSULATING-LAYER NONCOPLANAR POWER FET

4.1 Device Design

Figure 36 gives the fabrication sequence for the noncoplanar power FET and Fig. 37 the mask set design corresponding to this sequence. The design consists of 1.5, 3, and 6 mm gate width devices along with many test structures and alignment marks. The source and drain figures are interdigitated with the gate repetition period being only 6 microns. The 1.5-mm device, for example, only occupies an area of approximately 100 x 100 microns. Not shown is the integral heat sink mask which will enable the substrates to be thinned to 1 to 2 mils and then plated up with gold to a thickness commensurate with handling and die attachment. The small die size enables the die to be thinned to a smaller thickness than can the larger die size used in coplanar design, thus reducing the thermal resistance and compensating to a degree the higher average power dissipation per unit area that comes as a result of the compact device structure. Appendix A gives the computation of the thermal resistance and Appendix B the computation of the parasitic capacitance expected for this structure.

4.2 Source and Drain Ohmic Contacts

In order to minimize the power losses in the 4-micron wide source and drain fingers, the finger metallization should be at least around 0.5 micron high. In the past such thicknesses were achieved by first depositing the traditional thickness to achieve good ohmic contacts, then alloying the contacts, and finally putting down an Au over-

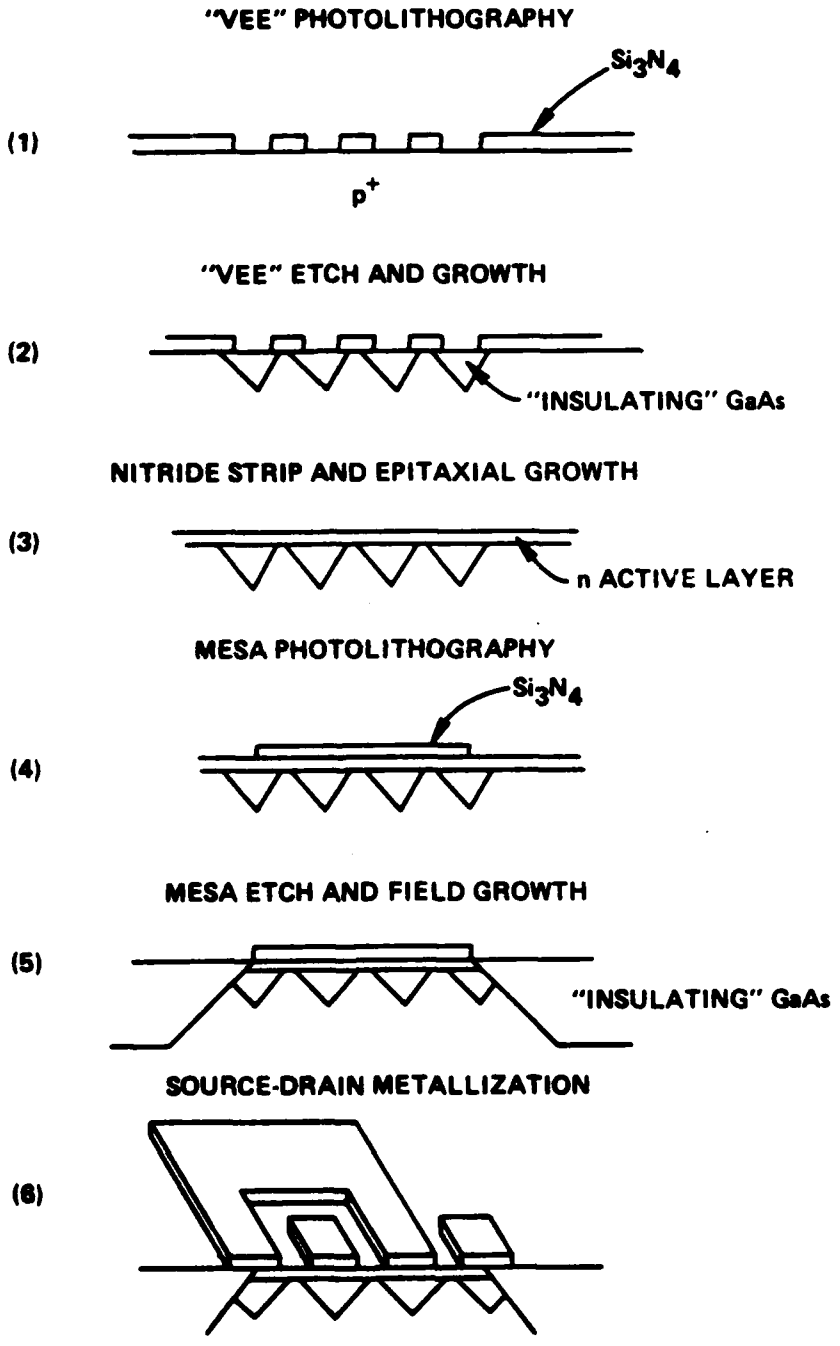


Fig. 36 Noncoplanar power FET fabrication sequence.

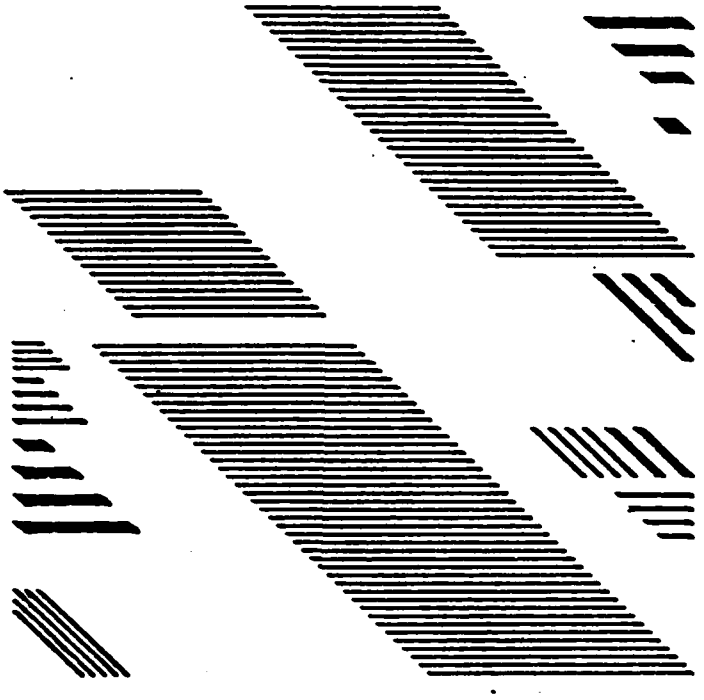


Figure 37 (a). Vee etch and growth mask.

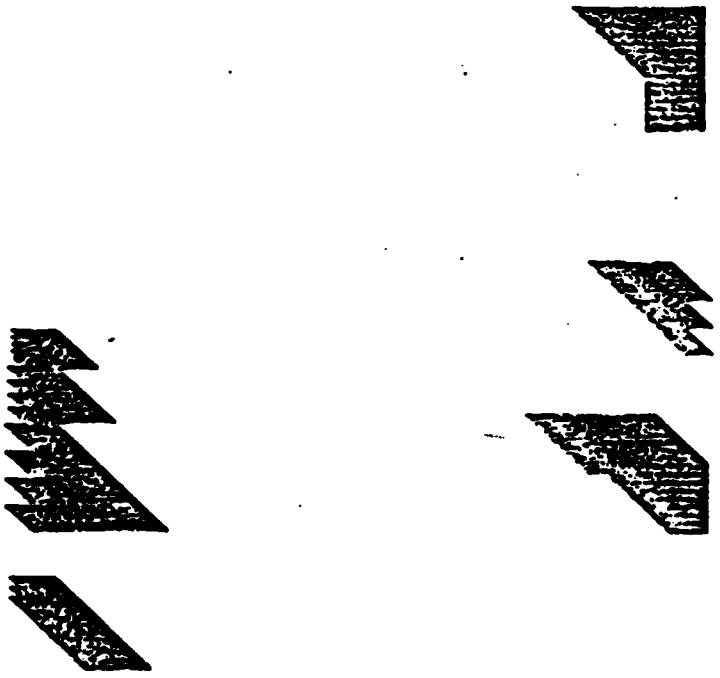


Figure 37(b). Nitride strip mask (protects alignment marks).

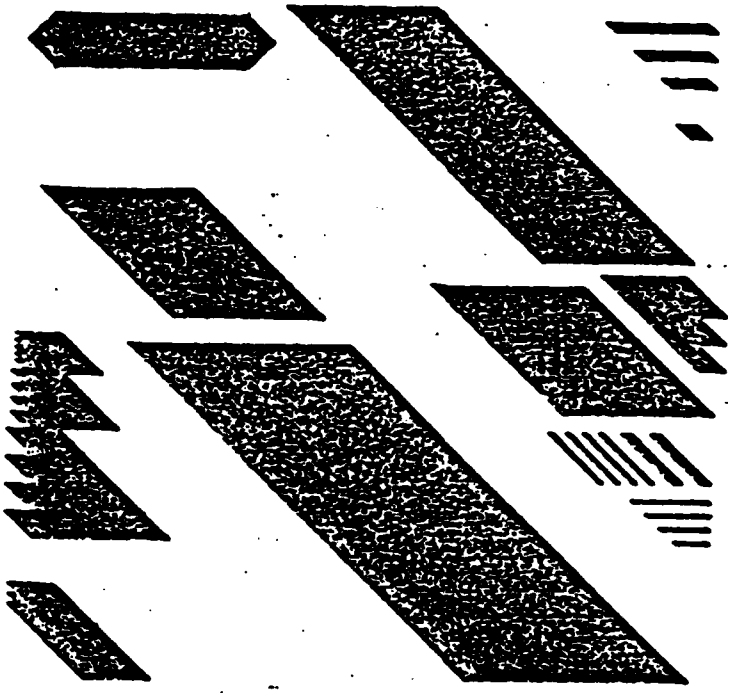


Figure 37(c). Mesa etch mask.

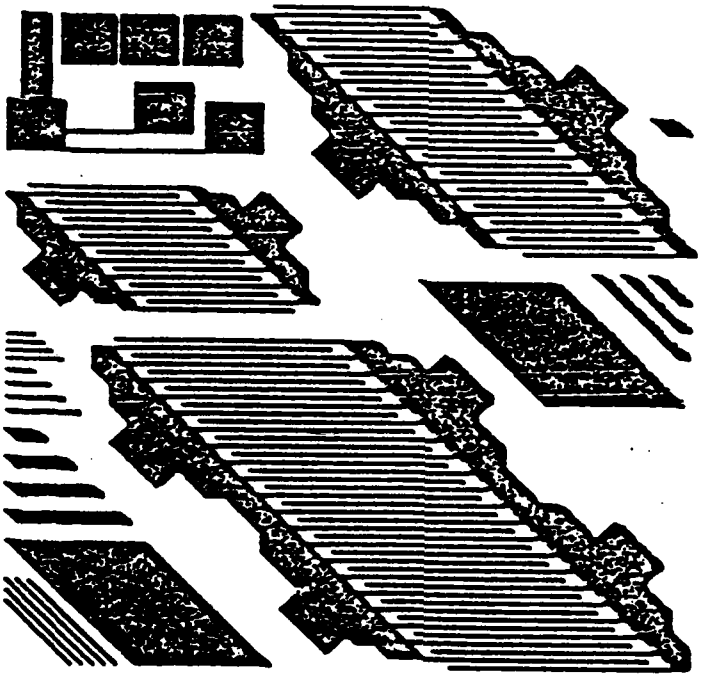


Figure 37(d). Source-drain metallization mask.

lay to achieve the desired total thickness. The overlay, of course, requires a second alignment in the photo-resist process. With the noncoplanar design such a realignment of the fingers would not be desirable, since there is only a 2-micron gap between the fingers to fit the gate into, and a misalignment of only 1-micron would halve this gap and perhaps result in the gate ending up under the finger rather than between the fingers as it should. It would be preferable to deposit the total metallization thickness all at once and lift it off, if this could be done without degrading the contact resistance. The standard thickness is 1000 Å of Au over 500 Å of Au-Ge/Ni, and it is desired to increase the Au thickness to around 5000 Å.

To determine the effect of increasing the thickness of the Au over the Au-Ge/Ni layers before the alloy, three different depositions were made: 1000 Å (standard), 2500 Å, and 5000 Å of Au over 500 Å of Au-Ge/Ni. After alloying, the contact resistance was determined by extrapolating a plot of resistance vs contact spacing back to zero spacing. The results were 4×10^{-6} ohm-cm^2 for the 1000 Å slice, 10^{-6} ohm-cm^2 for the 2500 Å slice, and 4×10^{-5} ohm-cm^2 for the 5000 Å slice (all of the slices were pieces from the same epitaxial wafer). In addition to a higher contact resistance, the data for the 5000 Å slice were much more scattered than for the other two thicknesses.

This result was reconfirmed by repeating the experiment. A specific contact resistance of 1.6×10^{-6} ohm-cm^2 was obtained for 1240 Å of Au-Ge/Ni/Au, 6.4×10^{-6} ohm-cm^2 for 4680 Å, and 1.54×10^{-5} ohm-cm^2 for 9000 Å. To see if Ge or Ni depletion by the thicker Au is the problem, a double

thickness of Au-Ge (900 Å) was sputtered, followed by a double Ni thickness (150 Å) and a 4000 Å overlay. The contact resistance remained high. However, when the Au-Ge was evaporated (vs being sputtered as in all the previous trials) using double the thickness of Au-Ge/Ni and a 4000 Å Au overlay, a specific contact resistance of around 10^{-6} ohm-cm^2 was obtained. Evidently the sputtering is responsible for the degradation in the specific contact resistance with increasing Au overlay thickness. Thus it may be that sputtering is an acceptable process for thin Au overlays but not for thick Au overlays when alloying occurs after the overlay deposition.

Using Auger electron spectroscopy, Robinson[16] has found for the Au-Ge/Ni alloy that at and above 352°C a significant amount of Ga outdiffuses and accumulates on the surface without any outdiffusion of As. Since Ge is known to act as a donor in GaAs when excess As exists, it is probably this outdiffusion of Ga that is responsible for the contacts being ohmic. Simple diffusion of Ga in Au would not seem to account for this phenomenon, especially for the large Ga concentration at the surface. If it can be believed that the 352°C nominal sintering temperature did not in fact exceed 356°C, then the Au-Ge eutectic cannot be responsible for the large Ga removal. However, since the Au-Ga eutectic is at 341°C, then quite possibly the Ga concentration at the surface can be explained by the eutectic removal of the Ga and re-precipitation at the surface upon cooling. If so, then the amount of Ga removed should be proportional to the thickness of the Au in the contact. Initially, the more Ga removed, the better the ohmic contact since this aids the Ge

in acting as a donor. However, it seems obvious that as more and more Ga is removed, an As layer is formed which effectively acts as an insulating layer, thus degrading the contact resistance. This might explain the contact resistance first improving and then degrading as the Au overlay thickness is increased, although this minimum might also be caused by the higher sheet resistance of the metallization as the Au overlay decreases (which was not taken into account in computing the specific contact resistance). Although the mechanism by which the Ga separates from the As and goes into solution with the Au is not understood, it may be that the sputter cleaning and deposition damages the surface to such an extent that this interaction is enhanced and, together with the thick Au overlay, results in an increased specific contact resistance when alloyed.

By measuring the resistance of long narrow stripes of metallization, the conductivity of the metal could easily be determined. For the evaporated 1000 Å Au-Ge/Ni, 4000 Å Au overlay configuration previously determined as suitable for a low specific contact resistance, the as-deposited overlay Au resistivity was determined to be around 3.9×10^{-6} ohm-cm. After alloying, it rose to 18×10^{-6} ohm-cm, which is about 7.4 times that of the 2.44×10^{-6} ohm-cm published bulk value for Au. With just the 4000 Å of Au overlay directly on GaAs, the resistivity rose to 6.5×10^{-6} ohm-cm after alloy. It thus appears that the Au-Ge/Ni interaction with the Au overlay is responsible for most of the degradation, but still there is a factor of 1.6 in degradation even without it, perhaps as the result of Ga coming out of the substrate.

Along with the resistivity measurements, specific contact resistance measurements were also made and revealed that the value was not always as low as that obtained the first time (a value as high as 10^{-5} ohm-cm^2 was measured). It appears that the only sure and reliable way to eliminate interaction between the ohmic contact layer and the overlay layer is to insert a barrier metal such as W or Mo between them.

A run was made with the following contact structure: 1600 Å evaporated Au-Ge/Ni/Au, 1200 Å sputtered W-Ti, and an evaporated 3800 Å overlay. After alloy, the Au overlay resistivity was 2.3×10^{-6} ohm-cm (the alloy thus anneals the evaporated Au to the published value) and the specific contact resistance was around 6×10^{-7} ohm-cm^2, which indeed is a very low value. The same Au-Ge/Ni/Au contacts without the W-Ti or Au overlay gave a high specific contact resistance for some reason (the contact was "puddled" in appearance). Thus it appears that the W barrier not only can prevent the degradation caused by the thick overlay, but can, at least in some cases, improve the specific contact resistance of nonoverlaid contacts.

4.3 Device Fabrication on Ge-doped Substrates

With the V-grooves filled and the MBE active layer deposited over them as discussed in Section 3.4, the mesas were next formed by etching the field to a depth of around 5 microns and regrowing semi-insulating GaAs back flush with the surface to provide low-capacitance areas for the source and drain pads to sit on. The field growth occurs sideways out from the mesas and at the same time grows slowly upward

above the mesa surface. To avoid an excessive height of the field above the mesa surface and subsequent overlay of the growth over the oxide mask especially at the corners, the growth was continued only out far enough to provide a base for the source and drain pads.

Figure 38 shows the completed device structure. The edge of the field growth can clearly be seen. For this run, the field growth did not continue uniformly out from the mesa edges as it had for the dummy runs used to calibrate the process. Device characteristics were not obtained from this run for several reasons. First of all, it appeared that the source and drain fingers were broken in crossing the step between the mesa and the field (this is probably more a fault of the ohmic contact metallization than of the step since the contacts showed a tendency to puddle when alloyed -- a W-Ti barrier and overlay Au were not used in order to shorten the feedback loop for materials evaluation). Secondly, the field growth was not insulating as evidenced by a test structure included with the device structures, causing a leaky connection between the gate and the source and drain pads. Thirdly, another test structure revealed that the p-n junction between the MBE layer and the substrate was quite leaky.

The excessive leakage of the p-n junction grown by MBE on Ge-doped substrates for the completed power FET run points to a potential problem of fundamental importance, as to whether coincidence of the electrical junction with the growth interface will result in unacceptable leakage characteristics. Secondly, the bad surface morphology for the

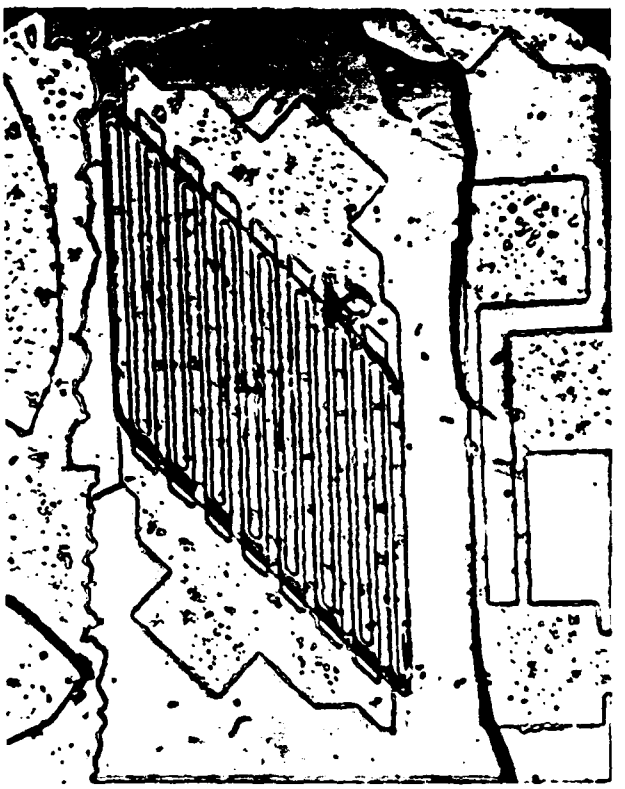


Fig. 38 Completed noncoplanar device structure.

"vees" and the field growth on the Ge-doped material is of some concern. This may possibly be minimized by better control of the growth time and better cleaning after the solution etch. Such problems were not encountered with the Cd-doped substrates where the vees were vapor-etched (rather than solution-etched) and were oriented in the perpendicular direction. The Cd-doped substrates give good surface morphology but have so far given rise to p-doped vees, while the Ge-doped material gives insulating vees but poor surface morphology. The problem of the field growth not being insulating was traced to depletion of the Ga source, which was easily remedied by changing the Ga source.

A one-micron MBE growth on an unmasked Cd substrate resulted in a surface p-doping of only $2 \times 10^{14} cm^{-3}$, i.e. much lower than the unacceptably high $10^{16} cm^{-3}$ values obtained by VPE growth, possibly a result of the lower temperature growth (550°C vs 760°C). Consequently, since vee growth by VPE on the Ge-doped substrates has proven to be more difficult to control than on the Cd-doped substrates (resulting in vees that are commonly either under- or over-filled), an attempt was made to fill the vees in a Cd-doped substrate by MBE. The substrate was installed in the MBE system immediately after solution etching the vees, with the oxide mask still in place. The substrate was heat-cleaned, then sputter-cleaned and annealed, in situ, prior to the MBE growth. The resulting MBE vee growth was unsatisfactory in that cleaved cross-sections showed very little filling of the vees and the material which had grown in the vees did not appear to have grown epitaxially (i.e. it appeared to be

polycrystalline). The poor growth presumably results because of the shadowing effect of the oxide overhang. Even with no oxide present, it appears that poor MBE growth in the vees may still result because of the shadowing effect of the walls of the vees.

Concerning the problem of junction leakage, an experiment was performed by MBE to examine whether or not a good gate junction could be fabricated at the interface between the p-type substrate and the n-type active layer. This was investigated by growing n-type MBE layers ($n \approx 10^{17} cm^{-3}$; ~6000 Å thick) on both Cd-doped and Ge-doped substrates (without vees). The substrates were heat-cleaned, then sputter-cleaned and annealed prior to the MBE growth. P-N junction diodes were fabricated by evaporating 10-mil ohmic contact dots and etching mesas. The diodes on the first Cd substrate run gave low leakage current (<1 μA) out to a sharp breakdown voltage of 18 V. On the other hand, the diodes on the Ge-doped material were quite leaky immediately upon application of bias, and beyond 4 V they would invariably become shorted. The results of a run with the Cd and Ge substrates side by side were the same as previously for the Ge material, while diodes on the Cd-doped substrate had low leakage out to about 5 V and 10 nA of leakage at around 12 V. The results on the Cd substrate were probably not as good as the first time because the substrate was not solution-etched prior to insertion into the MBE system, and unlike the first run the surface contamination (mainly oxygen) would not disappear by heat treatment and came off only after the sputter cleaning.

The high (18 V) breakdown of the Cd substrate diodes was explained by running a doping profile, using the p-n junction. The profile showed that the Cd had diffused (or autodoped) significantly into the n-type MBE growth, causing the junction interface to be removed from the growth interface. Since Ge would not be expected to diffuse significantly this probably explains why the Cd substrate diodes have superior leakage characteristics. Only about 100-200 Å of material can be removed in a reasonable length of time (~1 hr) by the sputter ion gun.

4.4 Switch to Zn-doped Substrates

4.4.1 Materials Development on Zn-doped Substrates

Work in our laboratory involving liquid phase epitaxy had shown that oxygen doping could compensate Zn doping and produce high resistivity layers. In light of the poor surface morphology and high leakage junctions obtained with Ge-doped substrates, an effort was made to see if O_2 could be used to compensate the p-dopant (Zn or maybe even Cd) in the VPE filling of V-grooves and the field regions.

Accordingly, O_2 was used as a donor impurity to compensate p-type impurities in the epilayers grown on both Zn-doped and Cd-doped GaAs substrates by VPE (doping of the substrate being about $1 \times 10^{18} cm^{-3}$). To simulate the vee growth, 2-3 micron thick epilayers were grown first. When the amount of O_2 introduced into the $Ga/AsCl_3/H_2$ reactor system was low, the layers were p-type, obviously

due to uncompensated Zn or Cd. At high O_2 concentrations, the layers were n-type on the Zn substrates, but were still p-type on the Cd substrates. The higher vapor pressure for Cd evidently precludes its compensation by O_2 at least for layers as thin as 2-3 microns thick required for vee growth. Consequently, all further efforts were directed towards using the Zn substrates.

By optimizing the O_2 input, very lightly doped ($<10^{14}cm^{-3}$) n- or p-type layers were obtained. This doping was sufficiently low to fully deplete the vees in an FET structure. Gold Schottky barriers of 20-mil diameter, applied to these layers to determine the doping profile, depleted the epilayer right up to the interface at zero bias. By using this technique, 4-micron spaced vees were etched and refilled in the VPE system to evaluate the quality of the material in the vees. Microscopic examination of these wafers show that the morphological problems with Ge-doped GaAs (solution etched to form vees and refilled in the VPE reactor) were not present in the case of Zn-doped GaAs substrates. The etching and refilling of the vees were very good as shown in Fig. 39. Electrical characterization of the material in the vees has not yet been done owing to instrumentation problems.

For the field region, 6-8 micron thick semi-insulating material must be grown on the Zn-doped GaAs. The bonding pads that sit on this field growth must have low capacitance and low leakage to the substrate. If the same O_2 concentration as that employed for the 2-3 micron layer discussed above is used, the 6-8 micron thick layers would be n-type since the Zn doping of the epilayer decreases away from the interface. The O_2 required to compensate the Zn should

Fig. 39 Cleaved section of wafer #CR-67-26 at a magnification of 1400x. Substrate is Zn-doped GaAs and the vees are filled with undoped GaAs.

therefore also decrease. Since the 6-8 micron thick epilayers were doped in the $10^{14}cm^{-3}$ range, attempts were made to compensate these impurities by introducing Cr along with O_2. The resulting layers were quite p-type (10^{15}-$10^{16}cm^{-3}$), suggesting that Cr was nullifying the effect of O_2. The next set of experiments conducted did not use any Cr. Since Zn incorporation into the epilayer was expected to decrease as the epilayer grows, the O_2 concentration was programmed to decline continuously from the optimum value deduced for thin layers to very small values at the outer surface. The resulting epilayers were very lightly doped, n-type or p-type, depending on the rate of decrease of O_2. For a 20-mil Au dot, the zero bias capacitance was about 2 pF and the depletion depth was about 7 microns. Beyond that, the doping profile was essentially that for the epilayer-substrate interface. These were considered to be very encouraging results.

In the experiments discussed above, the back side of the Zn-doped GaAs substrates was coated with a thick SiO_2 film to reduce the efflux of Zn from this surface. In the absence of such a protective layer, the undoped epilayers will have more Zn and the O_2 concentration needed to compensate the Zn will be higher.

With the switch to Zn-doped substrates, and in light of the success with the vee growth, MBE active layers were grown on the Zn-doped substrates in the same way as on the Cd-doped and Ge-doped substrates described previously. The substrates were heat-cleaned, then sputter-cleaned and annealed prior to the MBE growth. P-N junction diodes were

fabricated by evaporating 10-mil ohmic contact dots and etching mesas. Three runs were done with target values of 6000 Å thickness and Sn doping of $10^{17}cm^{-3}$. The first run was sputter-cleaned around 200 Å (moving the ion gun closer to the substrate did not increase the sputtering rate), the second was sputter-cleaned 400 Å, and the third was sputter-cleaned 400 Å with a longer Sn predeposition in an effort to achieve a steeper transition to $10^{17}cm^{-3}$. The first and second runs were essentially identical, with a breakdown voltage of around 7.5 V, while the third run had a breakdown voltage of around 7 V (making the transition from p to n more abrupt would be expected to lower the breakdown voltage). For all three runs, the leakage current at breakdown ranged from 20 to 100 μA. For $10^{17}cm^{-3}$ doping, a breakdown voltage of around 15 V would be expected. If breakdown were due to mesa edge effects or due to a bad growth interface, it would seem that the breakdown voltages would be more scattered than they were (± 0.3 V). The measured breakdown voltage corresponds to a doping of around $4 \times 10^{17}cm^{-3}$, but back-side profiling using the p-n junction seemed to indicate that the doping was indeed the intended $10^{17}cm^{-3}$ value.

4.4.2 Device Fabrication on Zn-doped Substrates

Four wafers using Zn-doped substrates and having had active layers grown in the MBE system and the vees and tubs etched and refilled with oxygen-doped GaAs in the Ga-$AsCl_3$-H_2 VPE system were started simultaneously for device fabrication. All had identical processing steps.

Figure 40 shows the noncoplanar structure with the materials growth portion of the process completed.

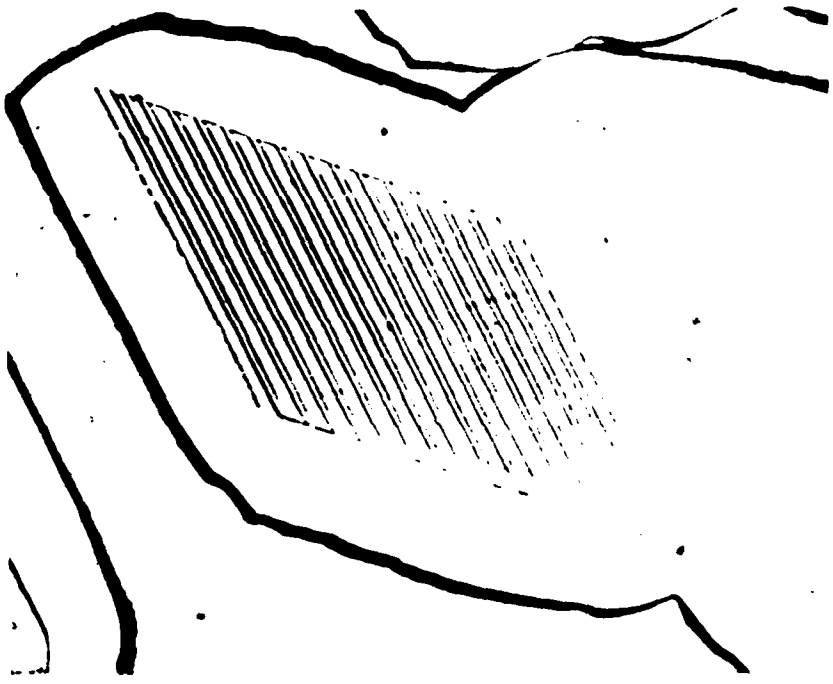


Fig. 40 Present noncoplanar surface.

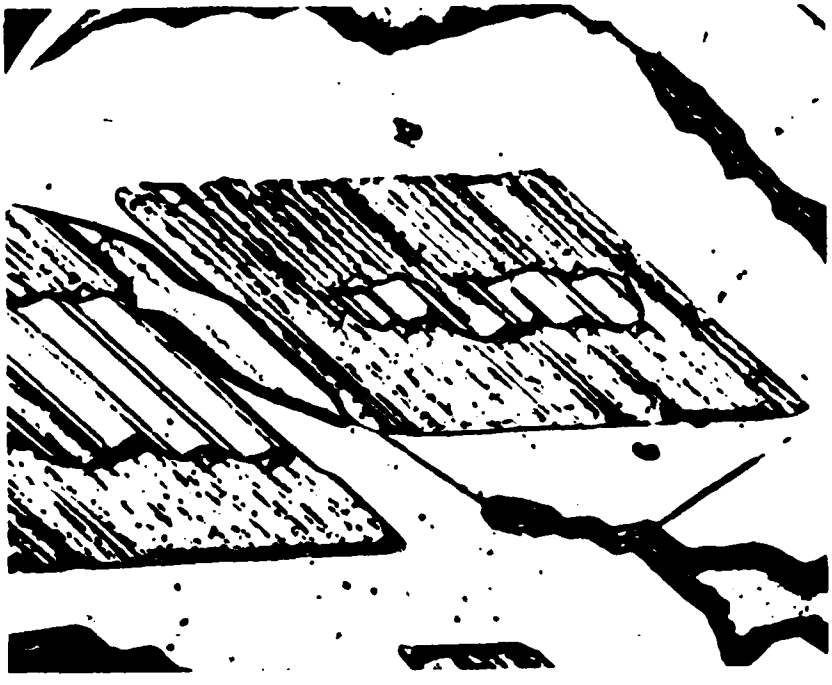


Fig. 41 Dec. '77 noncoplanar surface morphology.

The 1.5-mm wide device and a portion of the 3-mm wide device are shown. To be noticed is the smooth surface morphology which contrasts with that obtained using Ge-doped substrates which typically looked as shown in Fig. 41. Figure 41 shows the vee and field over and under growths and the sharp step between the field and the device which resulted in broken fingers. Figure 41 was typical of the device wafer whose processing was described in Section 4.3, although in a few small areas better (but not perfect) patterns were seen. On the other hand, Fig. 40 was typical of the four wafers processed and represents the processing development at that time. The vees are uniformly filled flush with the surface as is also the field growth. The irregular borders in the field are simply where the field growth has not been completed as shown in Fig. 42 to avoid overgrowth and webbing at the device corners as shown in Fig. 43. The incomplete field growth poses no problem since nothing is out there anyway.

The wafers were taken clear through to completion. After the deposition of an SiO_2 layer in the field to prevent conduction from the metallization to the substrate, the source and drain ohmic contacts were deposited. To get the Au-Ge/Ni to stick to the oxide, 200 Å of Cr was initially deposited.

Initial testing of the wafers indicated devices characterized by low currents, poor saturation, and inability to be pinched off (Fig. 44). Whereas 0.5 A and higher were expected for the drain currents, only around 30 mA was measured, and was the same for the 1.5, 3, and 6 mm wide

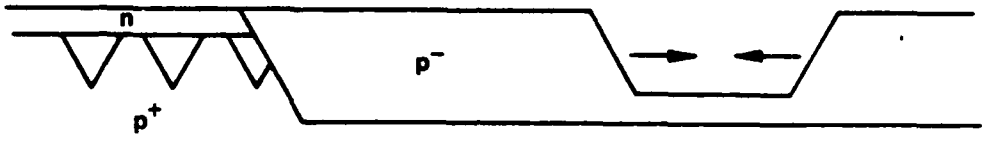


Fig. 42 Field growth kinetics.

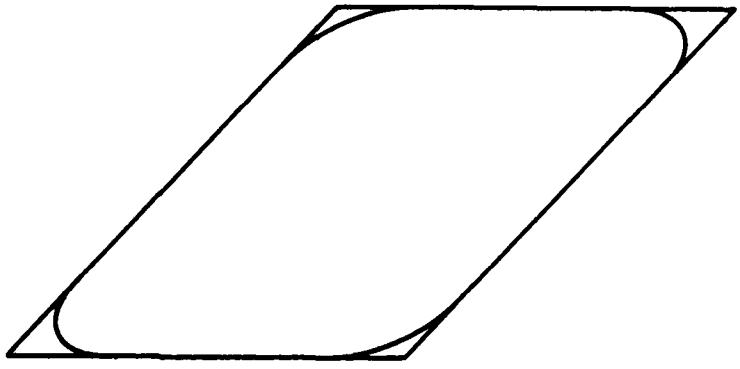


Fig. 43 Field overgrowth problems.

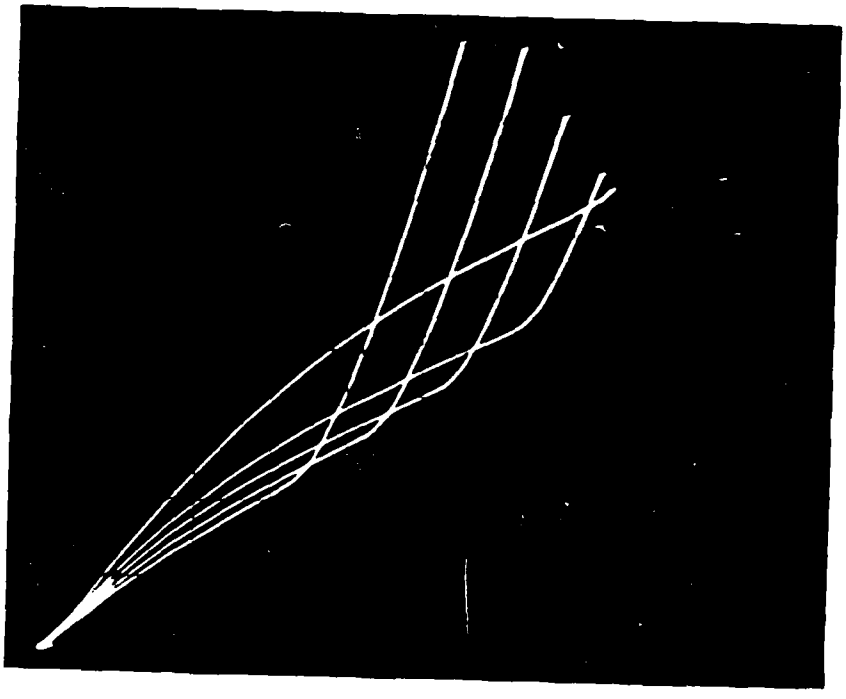
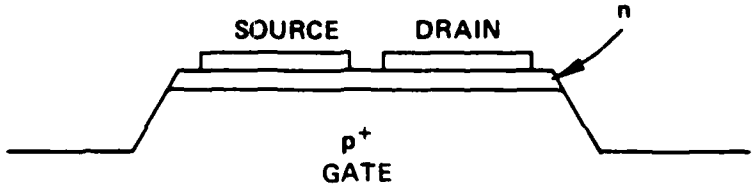


Fig. 44 Noncoplanar FET characteristics (5 mA/div vertically, 1 V/cm horizontally, 1 V/step).

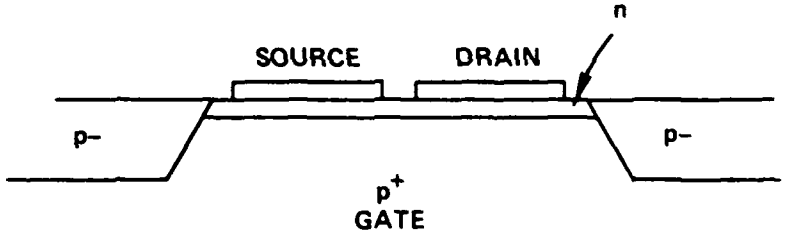
devices. The g_m's were only 5 mmho or less, and the devices would only pinch off one-fourth to one-half of the way. SEM inspection of the source and drain fingers as they crossed the field oxide indicated a possible break in the metallization, but redoing the metallization with evaporation at an angle did not change the results. Probing of the ohmic contact test patterns indicated rectifying contacts. This would seem to indicate that either the MBE layer was very low doped (it was not profiled since the MBE layers are difficult to profile because of leakage current), or the Zn diffused up into the MBE layer during the field growth, or possibly (but not likely) the 200 Å Cr layer was producing rectifying contacts.

In order to understand what the problems might be with the overall structure, the simpler structure shown in Fig. 45 was used to progressively study the electrical properties of the fabrication sequence. Figure 45a uses a mesa etch (the source and drain pads are big enough to probe so no pads over the field are needed) to evaluate the pinch-off characteristics of the active layer. The field etch and growth by VPE (Fig. 45b) would then be done on another portion of the wafer to determine its effect on the device characteristics (will Zn diffuse up to eliminate the active layer?). If deemed necessary, vees could be put down as shown in Fig. 45c to determine their effect.

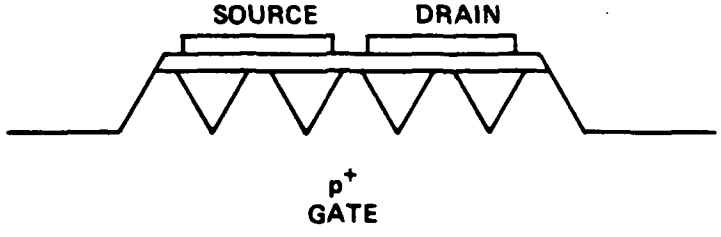
The structure of Fig. 45a was fabricated to evaluate the quality of the active layers and the interface between these layers and the p^+ substrates when the active layers were grown by MBE and VPE techniques. By the latter technique,



(a) MESA ETCH



(b) VPE ETCH AND GROWTH OF FIELD



(c) VEE PROCESS INCLUDED

Fig. 45 Test structures for electrical evaluation.

AD-A083 682 VARIAN ASSOCIATES INC PALO ALTO CA SOLID STATE LAB F/G 9/1
NONCOPLANAR HIGH POWER FET.(U)
DEC 79 S G BANDY, D M COLLINS, D R DECKER N00014-76-C-0303
UNCLASSIFIED NL

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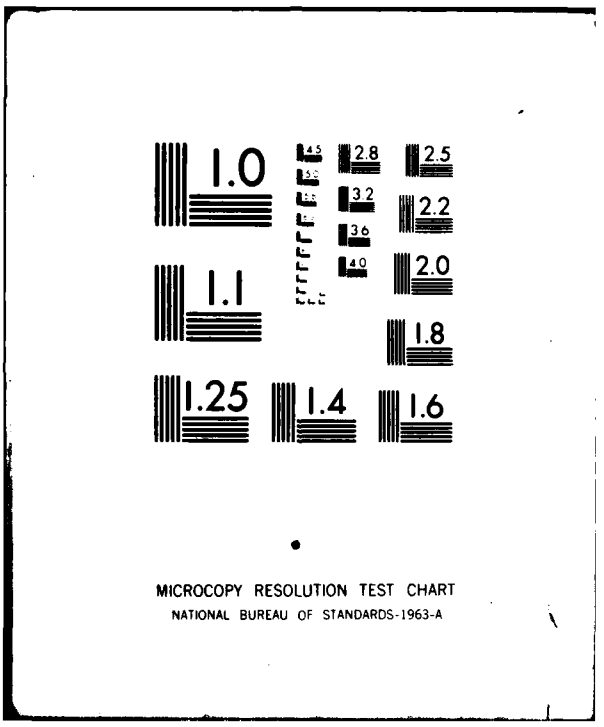
1.0
1.1
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1.4
1.6
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2.0
2.2
2.5
2.8
3.2
3.6
4.0
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

n-type epilayers (doped to 1 x $10^{17}cm^{-3}$) were grown in the conventional manner after heavy vapor etch of the substrate surface just before growth as well as without any vapor etch before growth. Previously in Section 3.4 it was stated that it was difficult to get continuous good quality FET layers by VPE without using any vapor etch. This was found to be due to turbulent flow patterns around the substrate holder used to keep the substrate surface covered during saturation of the Ga source. By modifying the holder, good quality layers were able to be obtained. The growth technique using this holder consisted of keeping the substrate surface covered during saturation of the Ga source and opening the slider of the holder to uncover the substrate surface and initiate growth. Figures 46 and 47 give the respective doping profiles for the active layers grown with and without vapor etch.

The two VPE wafers of Figs. 46 and 47 were scribed into three pieces each. Two of the pieces from each of the wafers were fabricated with the structure of Fig. 45a, one with Au-Ge/Ni contacts and the other with Cr/Au-Ge/Ni contacts. The other pieces were given the Fig. 45b process. No significant difference was seen between the two metallization schemes, indicating that the addition of Cr to the ohmic contacts produces no significant difference. Figures 48 and 49 give the drain characteristics of the devices fabricated on the vapor-etched and nonvapor-etched wafers, respectively. The device width is 250 microns. The devices pinched off nicely with reasonable drain currents and g_m's and showed good saturation. The devices were not tested extensively, but it appears that the nonvapor-etched wafer may have had slightly leakier p-n junctions.

RUN NO. 8P11-18 DIODE NO. _____ AREA 20 mils BARRIER Au. DATE 6-8-78

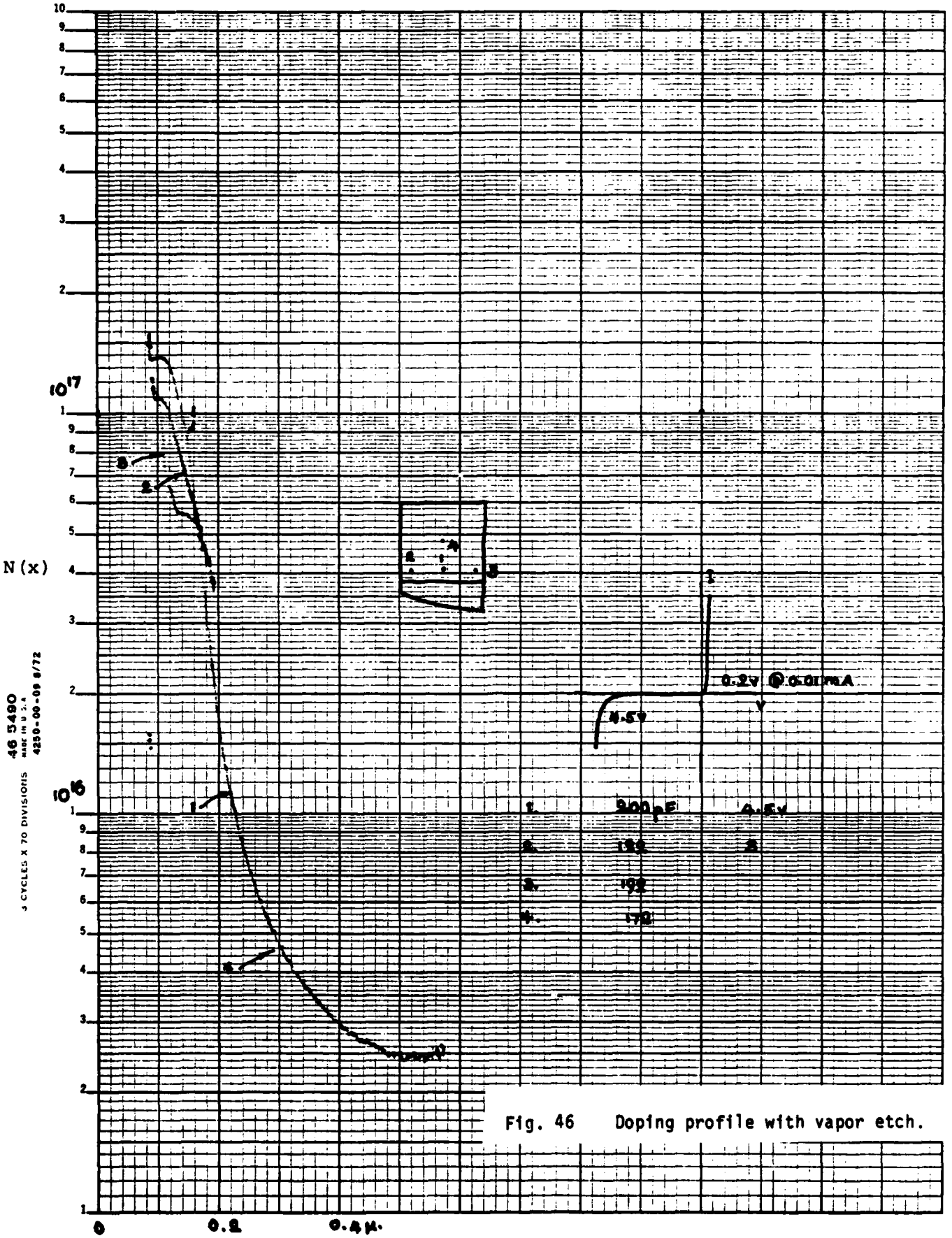


Fig. 46 Doping profile with vapor etch.

RUN NO. 80n-15 DIODE NO. _____ AREA 20 mils² BARRIER Au DATE 6-12-78

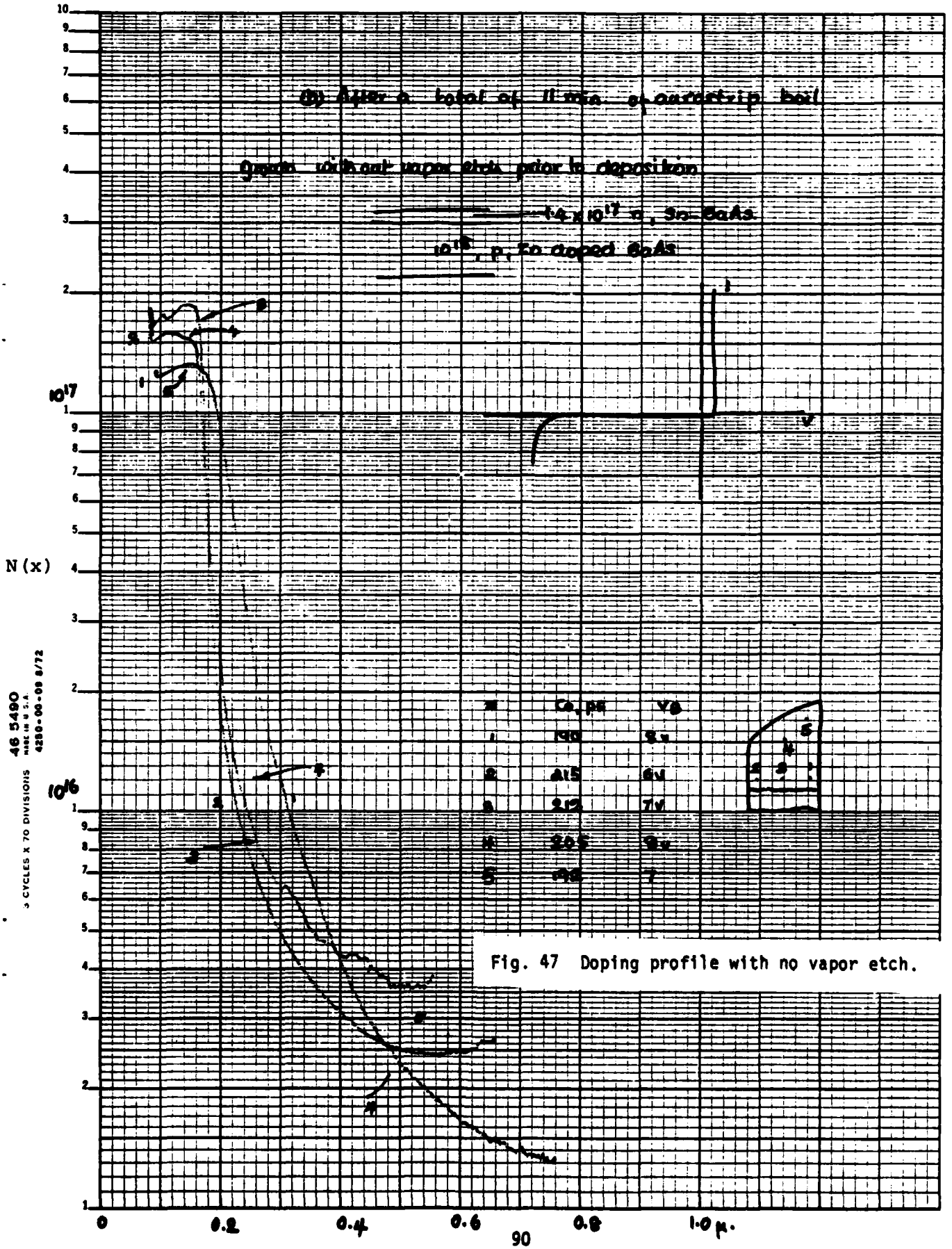


Fig. 47 Doping profile with no vapor etch.

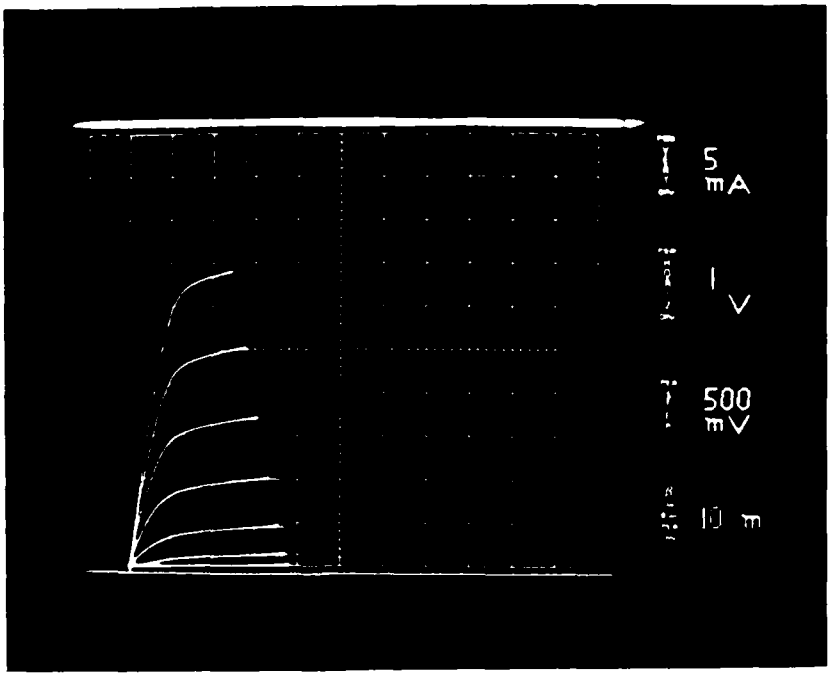


Fig. 48 Drain characteristics for vapor etch material.

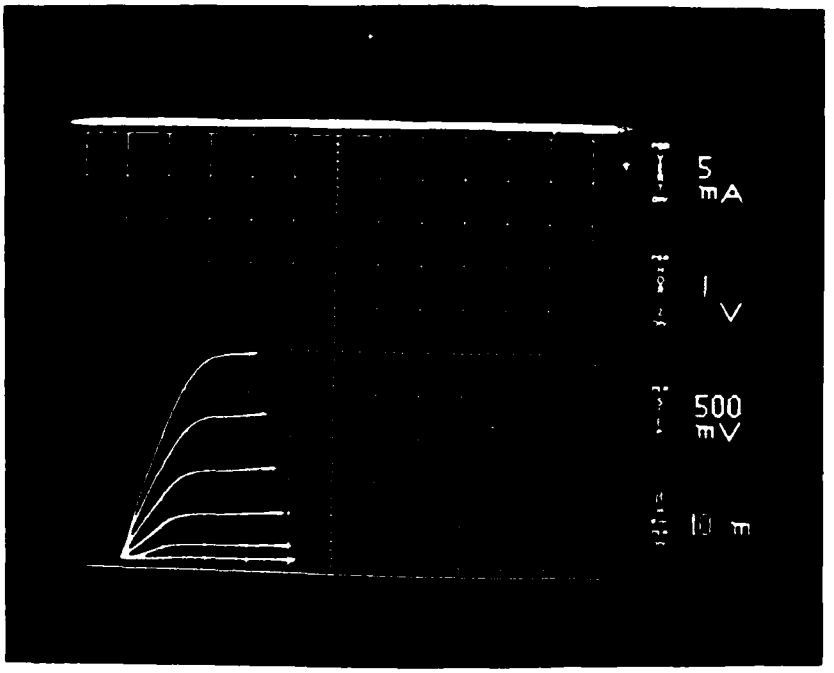


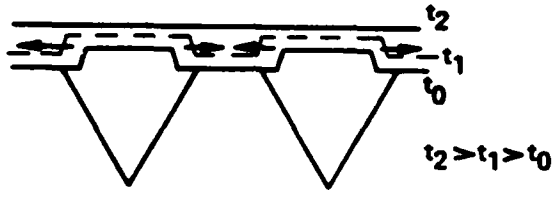
Fig. 49 Drain characteristics for no vapor etch.

When the process was continued on the VPE wafers to form the Fig. 45b structure, no significant difference was seen in the drain characteristics from those using the Fig. 45a structure. This would mean that Zn diffusion from the substrate into the active layer during the high temperature vapor etch and growth of the field regions was not significant and was not responsible for the lack of good FET characteristics for the completed noncoplanar structures. This result was duplicated twice for the VPE active layers. On the other hand, when the Fig. 45 structure was made with MBE-grown active layers, no channel current was seen with either the Fig. 45a or the Fig. 45b structure. In addition, very low current FET characteristics could be obtained by shining light on the channel. This strongly suggests the MBE layers are undoped as grown, and no need was seen for pursuing the Fig. 45c structure.

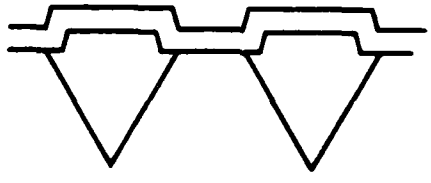
While it seemed clear that the MBE active layers were much too lightly doped, the reason for this was not obvious. Because of Schottky-barrier leakage, the MBE layers over the vees were unable to be profiled for doping when grown. FET active layers grown under similar conditions on Cr-doped substrates have been found to have reasonably predictable and reproducible doping profiles. It is possible that Zn autodoping (or some related phenomena) is occurring during the active layer growth, resulting in a lower doped active layer than that predicted. But more likely, the problem is related to the finite time needed for the Sn to build up before it is incorporated into the active layer.[17] Since a buffer layer is grown when a Cr-doped substrate is used, this problem of instant doping as soon as MBE growth starts is not as critical.

4.5 VPE Active Layer Growth Using a Slider Boat

The success of the VPE growth without vapor etch on the simple structures of Fig. 45 coupled with the doping problems encountered with the MBE active layers prompted its use on the noncoplanar structure. It seemed that the elimination of the black wax to protect the backside SiO_2 and the new slider boat design had solved the problems of discontinuous growth seen previously (when the black wax was eliminated, no carbon was seen on the surface by Auger prior to the MBE growth, so no sputter cleaning was needed). After recalibrating the growth rate on the vees (it appears that the growth rate is slower on the vees), a number of VPE growths were tried over vees grown on a Zn-doped substrate with the same result -- the surface was smooth and almost featureless except for a faint trace of the vee patterns. This was too faint to be used in the photolithographic alignment needed for the subsequent processing. Evidently the sideways growth that occurs with VPE smooths out the surface while for MBE the deposition is more uniform (Fig. 50). To preserve the alignment marks, a resist mask was used to preserve a portion of the SiO_2 over the alignment marks when stripping the SiO_2 after the vee growth just before the active layer growth. The resulting active layer growth was discontinuous because of contamination by the resist process. Another try at protecting the SiO_2 only on the corners of the wafer with black wax still resulted in discontinuous growth because of contamination from the wax. Slightly underfilling the vees did not solve the problem of the featureless surface, but at least the active layer would be thicker under the source and drain rather than thinner as in Fig. 50, thereby lowering the source resistance and perhaps raising the drain burnout voltage, as seen for recessed gates on coplanar power FETs.[18]



(a) VPE ACTIVE LAYER



(b) MBE ACTIVE LAYER

Fig. 50 VPE and MBE growth differences.

Unlike black wax, however, red wax on the corners was found to leave the surface contamination-free enough to grow a continuous active layer. With the "vee" patterns intact in the corners for alignment purposes, attention was directed more closely to the active layer growth. Using Nomarski interferometry, it was found that the active layer over the "vees" was thicker than that over the field by an amount varying from 3000 Å upwards to around one micron or more over the same wafer and from run to run. This effect is shown in Fig. 51. Also, the doping profile appeared to be independent of the growth time, which is doubtlessly related to the effect shown in Fig. 51. No effort was expended towards solving the uncontrolled growth over the "vee" regions, and wafers having the least active layer growth over the "vees" were processed into devices (Section 4.7.1) after some effort was put into developing an ion-implantation process.

4.6 Ion-Implantation of the Active Layer

Although the problem with the MBE active layer growth is not considered fundamental in nature and perhaps with more work the VPE active layer growth problem of too smooth a surface could be solved or circumvented, both techniques suffer from having the p-n junction coincide with the growth interface. To circumvent these problems, it was deemed desirable to try to implant the active layer.

Figure 52 gives the process envisioned for an ion-implanted noncoplanar structure. Not only is the vee pattern preserved on the surface, but the p-n junction no longer coincides with the growth interface. Furthermore, the

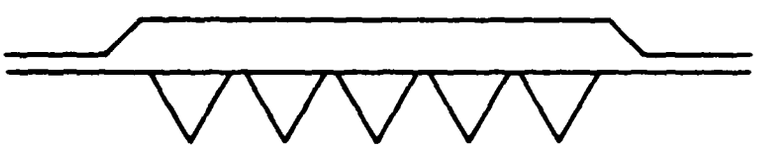
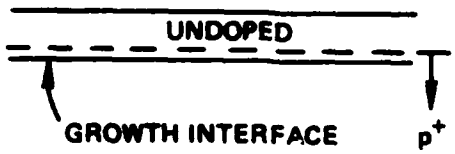


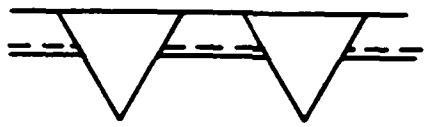
Fig. 51 Uncontrolled VPE growth over the vees.

growth interface has had an extensive vapor etch, and anyway during the growth of the undoped retion the initial part of the growth is p^+ because of autodoping and diffusion. Annealing of the ion-implanted layer will cause further p diffusion, and the implanted layer need not extend down to the p^+-doped region as shown in Fig. 51c. This will provide the retrograde doping profile needed for linearizing the drain characteristic[19] while maintaining the high doping needed for the ohmic contacts, a feature unique to this particular noncoplanar design.

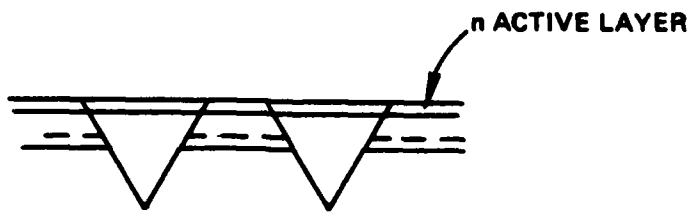
Si implants at 140 KeV and a dose of $2 \times 10^{12} cm^{-2}$ were made into 0.7-micron thick buffer layers grown by VPE on Zn-doped substrates. These exhibited very low effective doping when annealed at 800°C for 30 minutes. Plasma-grown silicon nitride with an index of refraction of around 2.05 was used as the anneal cap. Cr-doped substrate test samples implanted along with the Zn-doped substrates show the expected dose, indicating that Zn diffuses up during the anneal and compensates the Si implant. This was confirmed by running a non-implanted buffer layer through the anneal cycle. The buffer layer doping went from a very low n- or p-type doping to a very high p-type doping during the anneal. This amount of diffusion greatly exceeds what would be expected using the diffusion constants found in the literature and however, the anneal of the non-implanted layer indicates that enhanced diffusion due to ion-implantation damage is not responsible. The same results were obtained using Cd-doped substrates. When a buffer layer on a Ge-doped LPE layer atop a Zn-doped substrate was annealed, it appeared from photoluminescence data that the Zn diffused through the



(a) UNDOPED LAYER GROWTH



(b) VEE GROWTH



(c) ACTIVE LAYER IMPLANTATION

Fig. 52 Ion-implanted active layer process.

Ge-doped layer to dope the buffer layer p^+ (the Ge-doped layer was about 6 microns thick). Either the Ge-doped layer must be grown thicker or grown on a Cr-doped substrate which would be removed prior to die bonding. Laser annealing[20] or electron-beam annealing[21] should prevent the substrate diffusion problems. Appendix C summarizes the progress made at Varian on developing a capability in laser annealing and it appears that pulsed laser annealing will not do the job. Electron-beam annealing is presently being investigated.

4.7 Device Runs Using Proton Bombardment Isolation with Zn-doped Substrates

To avoid the long high-temperature step used for the VPE field growth in order to minimize substrate diffusion into the active layer, and also to avoid the possibility of problems with overetching and under- and over-growths, proton bombardment isolation of the field was investigated. It does not appear that any of the device runs made up to this point have had as their main source of failure any problem related to the field growth, but with ion-implantation now as an option, it made sense to investigate proton bombardment as a more reliable technique to provide field isolation.

Using $2 \times 10^{18} cm^{-3}$ Zn-doped substrates, proton doses of 10^{13}, 10^{14}, 3×10^{14}, 10^{15}, and $3 \times 10^{15} cm^{-2}$ were implanted at 170 KeV. Subsequent evaporation of Au dots on these wafers revealed that the $10^{15} cm^{-2}$ dose gave the lowest leakage and capacitance with the effective depletion depth at zero bias being 0.83 micron.

4.7.1 Device Run with VPE Active Layer

A device run was completed on one of the wafers having a VPE active layer. As mentioned in Sec. 4.5 and shown in Fig. 51, uncontrolled growth occurred over the vee regions. This rendered the wafers less than desirable for continued processing at that time, but the failure of ion-implantation to become a viable process because of substrate diffusion was cause for renewal of interest in these wafers. The wafer with the minimum overgrowth was chosen. Because the gate is on the bottom side of the channel, the possibility exists that the channel can be thinned after device fabrication until the desired pinch-off voltage is obtained.

Mesa definition was done by proton bombardment of the field at 100 KeV with a dose of $10^{15}cm^{-2}$. Only 100 KeV was used as a conservative measure against proton penetration of the approximately one-micron thick electroplated Au mask over the device area. After a 1400 Å SiO_2 deposition over the field to prevent conduction through the field region, 50 Å of Cr (to promote adhesion to the SiO_2) followed by 4500 Å of Au-Ge/Au (angled to surmount the SiO_2 step) was deposited and alloyed to form the ohmic contacts.

Figure 53 shows a photo of the 1.5-mm wide device. Upon alloying, the ohmic contact metallization pulled away from the oxide step, resulting in a break in the metallization as shown in Fig. 54. The W-Ti process was not used to avoid the long time delay to implement it. In places where continuity remained, the metallization was so than at the

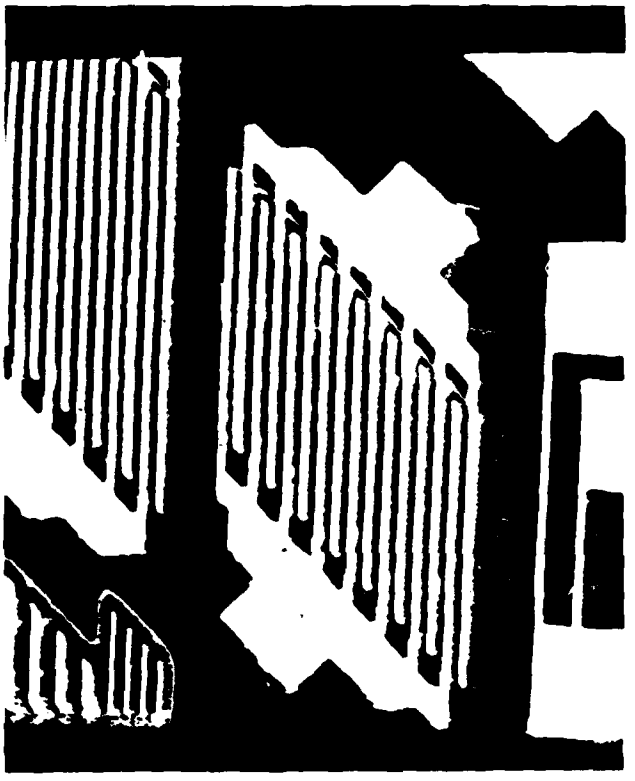


Fig. 53 1.5-mm wide device.

Fig. 54 Finger breakage crossing oxide step.

step that when the drain characteristics were observed the high drain current would usually melt the metallization at the step and open it up.

For those devices that did not open up completely, the following results were obtained. Typically, the active layer was too thick to pinch off without breaking down the gate. The gate p-n junction characteristic ranged from being quite leaky (symmetrical with respect to forward bias) on one part of the wafer to 100 μA at a 13-V reverse bias on another part of the wafer. It may be that terminating the gate p-n junction laterally by a proton damaged region is responsible for the gate leakage. This could be remedied by an etched trough around the device. The coincidence of the p-n junction with the growth interface could also contribute to the leakage, and a slight amount of diffusion might alleviate this problem.

Figure 55 shows the drain characteristic of an 0.4-A device (Z = 1.5 mm), and shows that the active layer is too thick to pinch off (further application of gate bias results in gate breakdown). It is quite certain that not all the fingers are connected, so effectively Z is something less than 1.5 mm. In other areas of the wafer the active layer is thinner and can be pinched off, and Fig. 56 shows one of these devices (0.12 A, again with not all of the fingers connected). Because of finger breaks and gate leakage, no devices were found that had both high current and good pinch-off characteristics. Figures 55 and 56 do reveal, however, good saturation characteristics and that this co-planar design is potentially capable of producing high power devices.

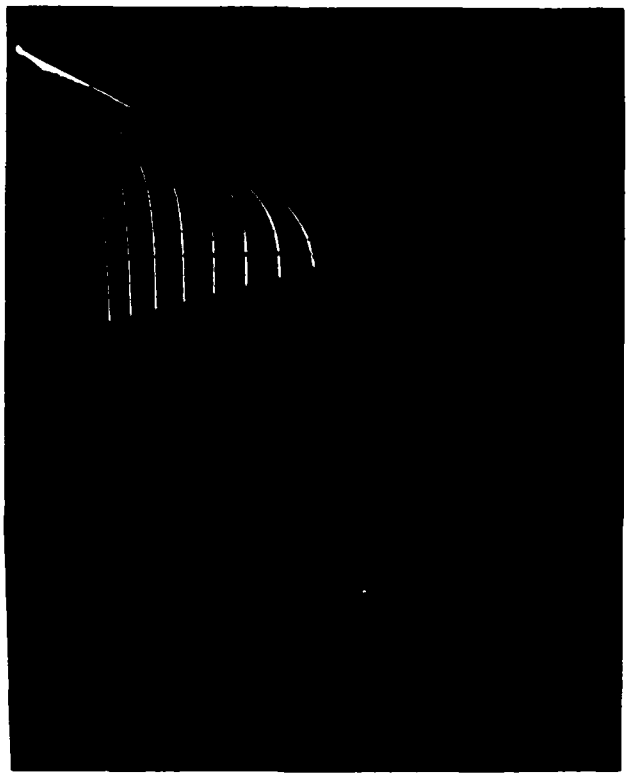


Fig. 55 0.4 A device (0.1 A/div, 1 V/div, -1 V/step).

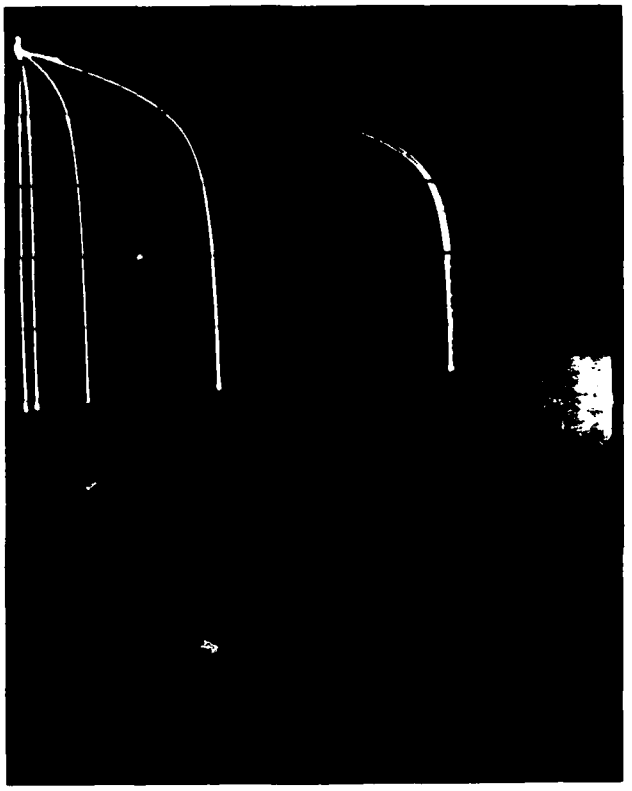


Fig. 56 0.12 A device (20 mA/div, 1 V/div, -1 V/step).

One interesting observation about this run was that in all cases the junction leakage was always better for the device than for the accompanying test structure (a mesa with an ohmic contact on top the size of the Z = 1.5 mm wide device) which in every case showed a dead short ohmic behavior. The area reduction in the p-n junction that the vees afford should in no way account for the vast difference -- a good p-n junction for a Z = 1.5 mm device might go out to 10 V with only 100 μA of leakage while the accompanying test structure gave ohmic behavior. At least the vees improve the leakage.

In probing from pad to pad of adjacent devices on the same die area to check for how well the proton bombardment isolated the active regions, any leakage measured was that attributable to leaky p-n junction gates. This indicates that no conduction occurred sideways between devices via the active layer and hence that the proton bombardment was successful at isolating the devices.

At this point two options existed. Either the metallization could be redone using the W-Ti process in an effort to get complete finger connection and rf evaluation, or an effort could be made to etch enough of the field away to prevent contact between the p-n junction edge and the proton bombarded region in hopes of improving the leakage (if indeed this mechanism is responsible for the bulk of the leakage). The latter option was chosen, but without success at either lowering the leakage or even determining if termination of the p-n junction by a proton-damaged region had an adverse effect on the leakage. Because of the thick active layer growth over the vees, it was uncertain that the p-n

junction could be exposed without complete removal of the proton-bombarded region out in the field and destroying the devices. In addition, the GaAs etch severely attacked the areas once covered by the Au-Ge/Ni metallization, etching to a depth of around 2 microns in those areas while etching only 1000 Å elsewhere. This would seem to suggest that some effect of the Au-Ge/Ni contact extends down to a depth of around 2 microns. At any rate, in those areas where this severe attack occurred adjacent to the resist the (device area is resist protected), the etch severely undercut the resist and damaged the active area of the devices.

4.7.2 Device Run with MBE Active Layer Using SnTe

MBE growth of the active layer was again tried, this time with the newly developed SnTe process.[17] This process was developed at Varian during the time period of the previous device run described in Section 4.7.1. Previously, with Sn as the source, the active layers were undoped presumably because of the need for Sn buildup on the surface before it is incorporated. It has been found that with SnTe as the source the incorporation of Sn as the dopant begins immediately.

Three Zn-doped substrates had vee grooves etched and grown in the bypass VPE reactor (all previous vee processing had been done in the CR reactor). These wafers were numbered BP #15-30, BP #15-32, and BP #15-33, and MBE active layers #161, #175, and #177 were deposited on these wafers, respec-

tively, using the new SnTe process. These wafers had progressively less and less carbon contamination each time when entering the MBE system as more effort was made to speed up the transition time from the bypass reactor to the MBE system. Wafer BP #15-30 sat around long enough before the MBE growth that the carbon contamination on the surface could not be completely removed by the sputter ion gun in the MBE system. As usual, Au dots on the MBE layers were quite leaky, but by taking C-V data and using software it appeared that the doping was somewhere around $10^{17}cm^{-3}$.

The three MBE wafers along with another of the VPE wafers of Section 4.5 with the least amount of overgrowth were all given a mesa definition by proton bombardment of the field at 100 KeV with a dose of $10^{15}cm^{-2}$. One micron thick electroplated Au was used as the mask for this operation. After an SiO_2 deposition over the field, the source and drain metallization was done using the W-Ti process of Section 4.2 (only 2000 Å of Au was put down over the W-Ti to avoid lift-off problems). After alloying the ohmic contacts, the wafers were thinned to 4 mils thick and ohmic contacts were put on the back side.

The wafers having MBE active layers #161 and #177 were found to have very leaky gates. MBE #161 had ohmic gates which is probably a result of the carbon on the surface which could not be completely removed by sputter-ion etching. MBE #177 had gate characteristics which were symmetrical in the forward and reverse directions. Although MBE #177 supposedly had the least carbon contamination, a small unexplainable void spot in each vee growth perhaps shorted

the gate to the ohmic contacts. The VPE active layer wafer had large drain currents, but the g_m's were very low (application of volts on the gate caused only a small percentage change in the drain current) and the drain characteristic was very shaky. Nothing more was done with the devices on these three wafers.

The devices on MBE active layer #175 had leaky gates, but not so bad as to prevent device testing. The devices showed good drain characteristics with I_{dss} being around 0.2 A for the 1.5-mm wide device. Figure 57 shows the drain characteristic for a 1.5-mm wide device and reveals that the pinch-off voltage is only around 2 V, being less than the value typically used for low-noise FETs. Evidently the MBE layer was grown thinner than intended.

The drain voltage could be taken out to 8 or 9 V without any indication of breakdown on the curve tracer, at which point the devices would open up on the drain end due to melting of the drain contact. This melting occurred around the oxide step crossover of the drain fingers, and extended over nearly half the total pad area, suggesting that device heating rather than the metallization current was responsible. The source metallization never melted in spite of the fact that it carried the same current. Interchange of the source and drain still led to the melting of the terminal used as the drain, indicating that some asymmetry in the metallization was not responsible for only the drain contact melting. Evidently gate breakdown is responsible. This problem limited the output power that could be obtained by increasing the drain bias. When biased at half of I_{dss} the drain

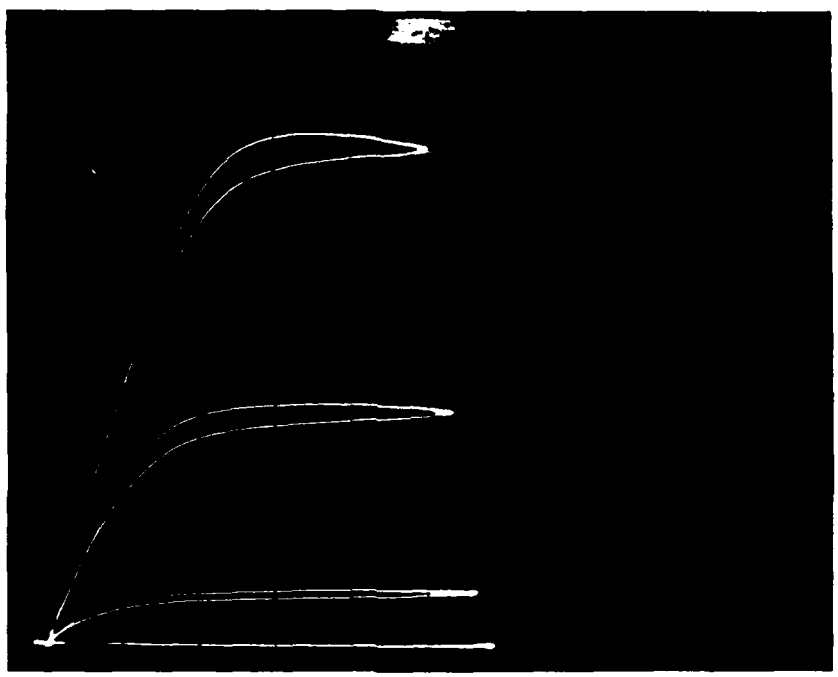


Fig. 57 Drain characteristic for 1.5 mm device.

voltage could be taken out a little further before the drain opened up.

Because of source and drain lead inductances, gain could not be obtained above 5 GHz. As shown in Fig. 58, the large die size in comparison to the device size prevented bonding into an rf fixture commensurate with the device size, resulting in large lead inductances. Table III gives the performance obtained from the 1.5-mm wide devices bonded in the common-gate configuration.

TABLE III

1.5-mm Device Performance at 5 GHz

Device	Bias $I_d(1/2\ I_{dss})$	V_d	Output Power at 1 dB compression	Gain
NCP 1-1	35 mA	10 V	53.7 mW	2.1 dB
NCP 1-2	100 mA	8 V	134 mW	2.0 dB

As previously mentioned, the low bias current is the result of the thin MBE layers grown, and the drain bias is limited by melting of the drain contact. The output power is about a factor of two lower than expected theoretically. However,

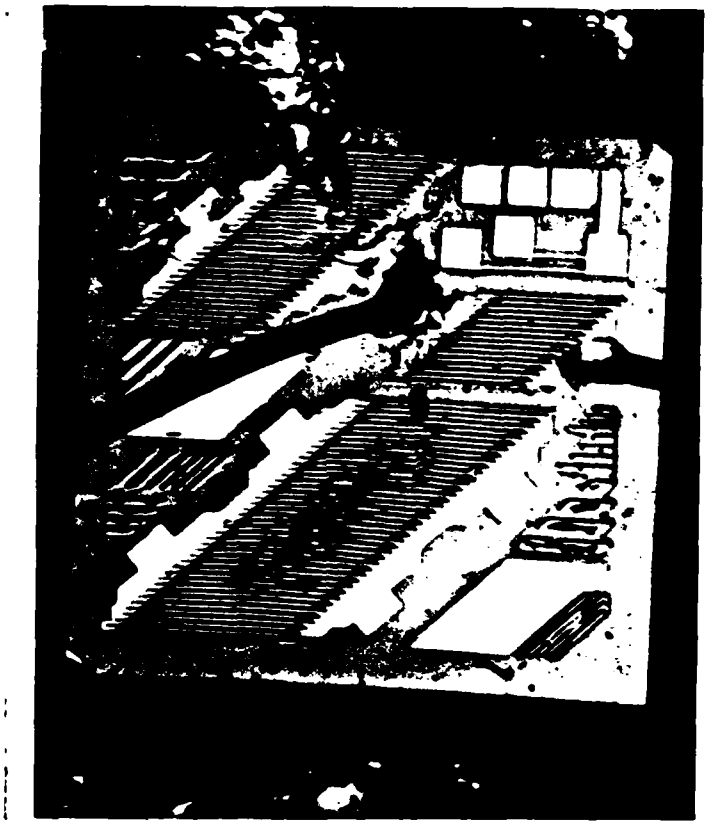


Fig. 58 Illustration of how large die size results in large lead inductance.

the saturated power appeared to be slightly above the theoretical value, suggesting class AB operation. The gains for the 3-mm wide devices appeared to be about 1 dB lower than for the 1.5-mm wide devices. Appendix D gives the s-parameters for two 1.5-mm wide devices, one bonded in the common-gate configuration and the other in the common-source configuration.

What remains for this device run is to determine the circuit model for the 1.5-mm devices from the s-parameters and deduce the actual reduction in parasitic capacitance that the vees accomplish. The causes for the drain terminal melting and the low value of 1 dB compressed power also should be investigated further. Perhaps an effort could be made to reduce the die size someway so that the lead inductances could be reduced.

5. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

5.1 Conclusions

The initial effort to develop a noncoplanar power FET using the substrate as the source encountered problems of uneven growth and excessive conduction with the buried-insulating layer. To circumvent these problems and yet retain the advantages of using a buried-insulating layer, the effort was switched to a design using the substrate as the gate. Although the previous problems were eliminated, a new set of problems was encountered which required a great deal of technology to be developed.

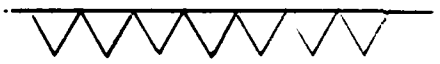
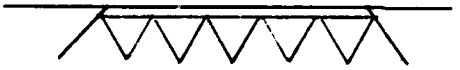
Although the straightforward noncoplanar junction FET first described by the French[22] was easily reproduced, the concept of reducing stray capacitance and defining submicron gate lengths by etching and refilling grooves under the source and drain has required the advancement of so many areas of technology that achievement of a working device in the advanced form was rather slow. This program has therefore contributed significantly to the advancement of general device-related 3-5 compound materials technologies. In the MBE area, for example, the unexpectedly severe segregation of Sn as a dopant, which had caused the failure of two sets of device runs, was cured by the adoption of SnTe as a dopant source.

Table IV lists some of the prime candidates for the fabrication methods at each stage of construction of the common-gate noncoplanar power FET, comprising some 54 different possible combinations and involving two or three

techniques at the cutting edge of technology as well as an array of advanced growth and device fabrication techniques.

TABLE V

Fabrication Options for the Noncoplanar Power FET

Fabrication Steps	Options
(1) Choice of substrate	(a) Cd-doped
	(b) Ge-doped LPE layer on Zn-doped
	(c) Zn-doped
(2) Formation of insulating tubs under source and drain 	(d) VPE etch and growth
	(e) Solution etch and VPE growth
	(f) Solution etch and MBE growth
(3) Active layer growth 	(g) VPE growth
	(h) MBE growth
	(i) Ion-implantation
(4) Mesa isolation 	(j) VPE etch and growth
	(k) Proton bombardment
(5) Metallization	(l) Thick source and drain fingers

Chronologically, the following combinations of options have been tried with the results as stated.

Combination	Merits Anticipated or Realized	Problem Areas Leading to Abandonment
adgjl	Realized good morphological vee and field growth.	High background levels of Cd in the vees and the field growth prevented their functioning towards reduction of parasitic capacitance.
begjl	Lower diffusion constant and vapor pressure of Ge enabled low background levels in the vee and field growth.	Unable to vapor etch vees. The vees had to be solution etched in a direction perpendicular to the one originally used, resulting in non-uniform growth morphology. Also the active layer was discontinuous apparently because of surface contamination and not being able to vapor etch.
behjl	With MBE, the surface can be sputter cleaned before the active layer deposition. Continuous MBE layers were grown.	Bad surface morphology with the vee and field growths. Leaky junctions, possibly due to lack of Ge diffusion to separate growth interface from p-n junction.
afhjl	Returned to Cd-doped substrates to see if MBE could solve the high Cd background problem by virtue of its lower temperature.	Although the Cd background was low, shadowing prevented MBE growth in the vees.
cdhjl	The Zn background was low enough to compensate with O_2. Good vee and field growth morphology was obtained.	The MBE active layers appeared undoped, probably because of Sn pre-dep problems.

cdgjl	By taking greater care in cleanliness and redesign of the slider boat, continuous active layers were grown by VPE.	The active layer growth thickness over the vee regions was uncontrollably thick.
cdikl	Using the well-established vee and etch growth along with ion-implantation should eliminate active layer morphological problems and enable the p-n junction to be away from any growth interface for higher breakdown voltages.	Both Zn and Cd were found to diffuse up and compensate the implated layer during the thermal anneal.

Thus, although an optimum technique was developed towards successfully achieving any one of the fabrication steps, no single technique was able to simultaneously satisfy the needs of all of the fabrication steps. The large number of permutations of the available options (3 x 3 x 3 x 2 = 54 since none of the options were known a priori to be mutually exclusive) has led to a considerable expenditure of time, And, of course, a decision had to be made at the juncture of the failure of each combination whether to try a new combination of to put more effort into making the combination work (e.g., the abandonment of combinations cdhjl and cdgjl was not because of any known fundamental problems and may have been made to work if more effort had been expended on them instead of switching to a new combination).

Working devices were finally obtained at the end of this contract using combination cdhkl with the newly-developed SnTe doping source for the MBE growth. Device performance was limited because of the low values of pinch-off voltage (due to the thin MBE active layer) and gate breakdown voltage

(perhaps because of coincidence of the p-n junction with the growth interface and/or the edge of the p-n junction being defined by damaged material). For the 1.5-mm wide devices, 134 mW of 1-dB compressed power was obtained with 2 dB of gain at 5 GHz.

Summarizing, working noncoplanar devices have been fabricated and tested, and the areas needed for improvement have been defined.

5.2 Recommendations for Future Work

The devices fabricated using the SnTe MBE active layer should be characterized with regards to parasitic capacitance reduction by the vees, and the causes for the drain terminal melting and the low value of 1-dB compressed power should be investigated further. An effort should be made to reduce the die size so that the lead inductances can be reduced.

In terms of future device runs, the best junction characteristics will probably be obtained with ion-implantation of the active layer, but this will be possible only when laser or electron-beam annealing of GaAs is developed. In the meantime, it appears that increasing the MBE active layer thickness and improving the junction characteristics by either etching a trough around the mesa to separate the p-n junction from the damaged field region and/or using diffusion to separate the p-n junction from the growth interface should yield a considerable improvement in device performance.

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APPENDIX A
POWER FET THERMAL RESISTANCE

For the structure shown in Figure A.1,

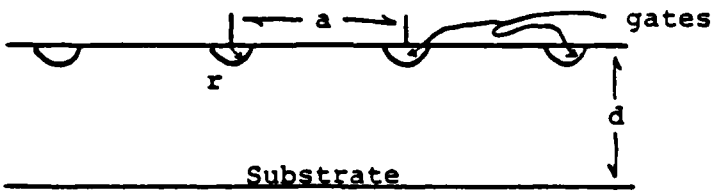

Figure A.1

if it is assumed that all the heat generated at the gate is carried away through the substrate (and none by the top contacts or through the air), then it is sufficient to solve for the capacitance from the gate cylinders to the substrate base, replace ε by the thermal conductivity k and take the reciprocal to obtain the thermal resistance. By eqs. (7.13), (7.14) of Spangenberg's Vacuum Tubes,

$$C = \frac{q_c}{V_g} = \frac{Z\varepsilon a}{d - \frac{a}{\pi}\ln\left(2\sin\frac{\pi r}{a}\right)}$$

where $q_g = -2q_c$, $d_{cg} = d_{gp}$ and $V_p = 0$. The thermal resistance per gate is thus

$$R_{th} = \frac{d - \frac{a}{\pi}\ln\left(2\sin\frac{\pi r}{a}\right)}{Z\,ka}$$

The equal temperature lines are circles around the gates and horizontal lines at the substrate base.

As an example, for the coplanar power FETs fabricated at Varian, d = 8 mils, r = 0.5 micron (one micron gates), a = 53 microns and Z = 3.5 mm, so using k = 0.4 W/cm$^{\circ}$K gives

$$R_{th} = 33.4^{\circ}\text{C/watt.}$$

For the noncoplanar structure of Figure 24, letting d = 1 mil (the smaller die size should enable the substrate to be thinned to this dimension), r = 0.5 micron, a = 6 micron and Z = 3.5 mm,

$$R_{th} = 31.1^{\circ}C/watt,$$

so the reduction in gate spacing will not result in a higher thermal resistance provided d is reduced accordingly. It should be easier to flip-clip the noncoplanar device because of the fewer bonds needed on the top surface.

APPENDIX B
NON-COPLANAR PARASITIC CAPACITANCE

For the "vee" structure shown in Figure B.1,

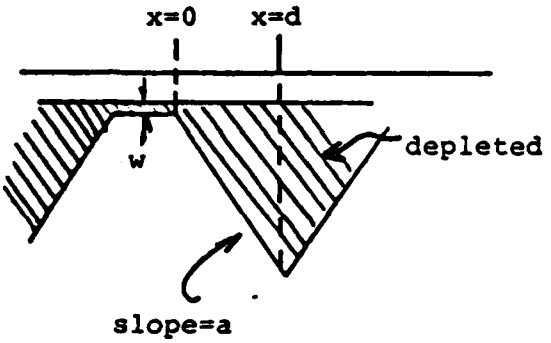

Figure B.1

if fully depleted, then for the "vee" portion only

$$C = \frac{\epsilon Z}{a} \ln \frac{w + ad}{w} .$$

With $w = 0.1$ micron for $10^{17} cm^{-3}$ material and zero gate bias, in the limit of zero gate width $d = 3$ microns and $a = \sqrt{2}$ for the design of Figure 24,

$$C = 2.67 \epsilon Z$$

while without the "vee,"

$$C = \frac{\epsilon Z d}{w} = 30 \epsilon Z,$$

giving around an order of magnitude reduction in the parasitic capacitance.

APPENDIX C
LASER ANNEALING

Using a Q-switched ruby laser with pulse lengths of 25-40 ns, no electrical activation of Si was seen in 100 keV Si-implanted Cr-doped GaAs with doses less than $1 \times 10^{14} cm^{-2}$. Table A-1 shows the electrical activation and mobility of uncapped GaAs with 100 keV Si implant doses of $1 \times 10^{14} cm^{-2}$.

TABLE A-1
SUMMARY OF GaAs LASER ANNEAL RESULTS

Laser Energy	Pulse Duration	Carrier Concentration	Mobility
1.1 J/cm^2	40 nsec	$8.1 \times 10^{12} cm^{-2}$	680 $cm^2/V\text{-}sec$
1.1	25	2.2×10^{13}	600
1.3	30	6.4×10^{13}	330
1.8	25	2.6×10^{13}	300
800°C thermal	30 min.	2.4×10^{13}	2330

This data indicates a reduction of mobility with increasing laser energy, with the maximum value being only 30% of the value obtained by thermal annealing. The data suggests that perhaps higher mobilities can be obtained by reducing the beam energy below 1.1 J/cm^2, but at the expense of reducing the carrier activation to even less than the 10% value of 1.1 J/cm^2. No improvement was seen using a nitride cap during the anneal and, in fact, the best mobilities were obtained without the nitride cap (most of the time the nitride cap

would blow off). The data in Table A-1 agrees with the results of others using Q-switched laser annealing as reported in the literature. The laser energy threshold for salient surface decomposition to occur was found to be 1.5 J/cm^2.

Using the laser in the free-running mode without the Pockel cell (0.2 ms pulses), no electrical activation of the Si-implanted GaAs was seen for energies all the way up to 2.8 J/cm^2.

APPENDIX D: 1.5 mm NONCOPLANAR POWER FET S-PARAMETERS

PAGE 4: ANA=A5209/DEPT 0810 4/30/79
VARIAN METROLOGY LAB/C. NISHIMOTO
NCP FET

.00 VOLTS, .00 MA (MEAS 1) NCP FET-1

FREQ (MHZ)	GA MAX DB	GU MAX DB	S21 DB	S12 DB	K - MAG	U MAG
2000.000	8.99	10.39	1.22	-26.08	1.63	.26
2500.000	7.67	8.52	.02	-27.98	2.25	.16
3000.000	7.22	7.66	-1.06	-32.58	3.61	.09
3500.000	6.62	6.91	-2.22	-39.38	7.81	.04
4000.000	7.62	7.75	-3.58	-45.85	10.28	.03
4500.000	2.72	2.66	-4.72	-46.43	32.58	.01
5000.000	2.49	2.33	-5.48	-38.23	12.25	.02
5500.000	2.91	2.64	-6.28	-35.76	7.66	.04
6000.000	3.08	2.66	-7.17	-33.07	4.98	.06
6500.000	.72	.45	-8.37	-32.25	6.66	.04
7000.000	-.49	-.72	-9.18	-31.06	6.98	.04
7500.000	2.13	1.60	-9.75	-29.64	3.11	.10
8000.000	3.02	2.26	-10.72	-29.26	2.23	.15
8500.000	-5.37	-5.41	-12.07	-29.96	13.58	.02
9000.000	-6.81	-6.82	-12.91	-29.32	16.81	.01
9500.000	-7.38	-7.29	-13.48	-29.45	16.91	.01
10000.00	-8.27	-8.24	-14.92	-30.08	19.09	.01
10500.00	-1.31	-.87	-13.09	-28.63	4.11	.10
11000.00	38.24		-12.21	-26.08	675.52	
11500.00	23.78		-13.63	-27.57	24.02	
12000.00	-15.85	-15.85	-19.10	-29.81	65.06	.00
12500.00	-6.57	-6.68	-16.67	-37.70	25.55	.01
13000.00	-2.08	-2.24	-16.34	-31.25	4.54	.08
13500.00	-1.92	-2.07	-16.33	-28.13	3.10	.12
14000.00	-4.56	-4.21	-16.28	-24.09	3.58	.11

REF PLANE EXT(CM): IN= 2.70, OUT= 2.70

Common gate V_{ds} = 4V

	y_{11}		y_{21}		y_{12}		y_{22}	
2.00	69.6665	-40.2220	-50.1309	64.1646	-3.0735	1.7031	3.7018	16.0642
2.50	73.7074	-35.9495	-49.2306	70.3086	-2.7895	2.0267	4.6614	21.9501
3.00	73.0893	-37.2408	-42.8801	80.6458	-1.4732	1.9551	4.8334	30.5166
3.50	65.9325	-47.9027	-24.3538	97.6777	-1.0634	.9244	7.6610	42.4477
4.00	57.5960	-51.8596	-7.8065	111.6384	-.8286	.9169	8.0395	65.4153
4.50	58.0590	-47.0153	26.1360	122.9600	.8140	-.6360	37.6885	77.2763
5.00	62.7858	-52.6835	69.1374	148.2636	1.4123	-3.4955	64.9596	100.0891
5.50	51.3240	-65.6917	171.6604	139.1698	-.2590	-7.4175	131.9895	127.4258
6.00	29.3961	-63.0401	253.5555	-129.1930	-12.9696	-6.3257	272.8843	-48.1169
6.50	29.7823	-50.7288	56.2949	-120.7247	-8.4102	1.3380	122.3618	-102.6[illegible]
7.00	22.1736	-50.8373	26.4624	-98.7592	-8.0366	1.3719	103.0500	-95.1[illegible]
7.50	27.0660	-50.9037	-25.6591	-77.4238	-6.1651	5.5511	50.4024	-118.[illegible]
8.00	22.0801	-49.5927	-26.9312	-35.7389	-2.8065	4.4313	16.6019	-85.4[illegible]
8.50	30.4602	-41.6249	-8.4211	-33.7750	-3.7254	2.4193	35.9175	-62.[illegible]
9.00	31.7404	-40.6259	-9.3369	-28.7362	-3.6978	2.2219	35.8104	-57.[illegible]
9.50	35.5069	-43.8474	-11.5851	-28.6741	-4.1229	2.6774	37.4221	-57.[illegible]
10.00	41.8140	-49.8320	-12.1677	-31.6979	-4.7774	3.6001	47.5160	-65.4[illegible]

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VARIAN METROLOGY LAB/C. NISHIMOTO
NCP FET

.00 VOLTS, .00 MA (MEAS 1) NCP FET-3 C.S.

FREQ (MHZ)	GA MAX DB	GU MAX DB	S21 DB	S12 DB	K MAG	U MAG
2000.000	2.52	1.59	-1.47	-12.90	1.28	.06
2500.000	1.12	.39	-2.68	-12.75	1.43	.06
3000.000	.31	-.37	-3.52	-12.48	1.58	.06
3500.000	-.20	-.89	-4.21	-12.24	1.53	.07
4000.000	-.54	-1.20	-4.87	-11.82	1.46	.08
4500.000	-1.58	-1.95	-5.23	-11.54	1.66	.07
5000.000	-1.38	-1.79	-5.38	-11.01	1.58	.09
5500.000	-1.01	-1.52	-5.34	-10.29	1.34	.11
6000.000	-.73	-1.35	-5.49	-9.68	1.22	.13
6500.000	-1.49	-1.85	-5.94	-9.12	1.26	.14
7000.000	-1.93	-2.09	-5.98	-8.38	1.27	.14
7500.000	-1.61	-1.87	-5.84	-7.70	1.18	.17
8000.000	-1.58	-1.69	-5.77	-7.34	1.14	.19
8500.000	-3.18	-3.18	-5.96	-7.09	1.48	.11
9000.000	-3.48	-3.33	-6.86	-6.88	1.48	.11
9500.000	-2.35	-2.41	-5.41	-6.26	1.21	.14
10000.00	-1.11	-1.39	-4.78	-5.67	1.07	.18
10500.00		3.37	-2.36	-3.94	.61	.73
11000.00			.49	-2.64	-.87	
11500.00	-9.48	-9.59	-10.95	-6.09	2.59	.03
12000.00	-3.78	-3.37	-4.85	-4.78	1.37	.07
12500.00	-1.15	-.38	-3.87	-3.28	1.04	.23
13000.00	-1.38	-.37	-3.28	-4.08	1.08	.23
13500.00	-1.22	.25	-3.57	-3.37	1.03	.38
14000.00	-.96	.19	-2.72	-2.49	1.02	.38

REF PLANE EXT(CM): IN= 2.78, OUT= 2.78

Common Source V_d = 4V

C.S.

	y_{11}		y_{21}		y_{12}		y_{22}	
2.00	65.0006	67.3101	28.9351	-107.9799	-12.6758	-27.1820	7.4222	29.7681
2.50	99.2250	66.9281	-11.1133	-127.0258	-22.9540	-32.7816	17.3434	40.6584
3.00	151.7273	32.2506	-91.4429	-125.8604	-46.0124	-31.0853	43.2840	53.4513
3.50	147.7839	-56.7289	-148.3981	-39.7631	-60.8295	-4.2536	78.2516	34.6[illegible]
4.00	94.0210	-100.8252	-124.2661	37.9919	-54.1058	21.8602	89.5644	1.56[illegible]
4.50	73.1160	-80.3520	-94.3354	36.1140	-45.3924	18.4205	79.6695	-5.5710
5.00	51.7469	-86.1213	-71.5207	57.3164	-39.9057	26.9168	77.1209	-22.1147
5.50	32.4687	-80.3627	-49.5497	63.4207	-33.8064	30.4394	71.7444	-31.9427
6.00	16.4567	-71.2820	-25.2020	62.3772	-24.3872	33.5661	59.9158	-43.5[illegible]
6.50	11.3888	-58.5904	-15.3826	50.3275	-19.3325	30.9335	50.0924	-45.1[illegible]
7.00	10.0978	-51.9487	-10.9520	43.9263	-16.6503	30.0379	42.4012	-45.4[illegible]
7.50	5.7378	-46.8938	-5.6241	40.0177	-11.6996	30.4736	35.2080	-46.[illegible]
8.00	3.5159	-40.1875	-1.7887	34.1302	-7.8681	27.4392	27.9161	-44.6[illegible]
8.50	9.9861	-40.0519	-7.7511	33.5739	-12.7894	27.4077	31.1439	-41.[illegible]
9.00	9.3641	-37.5572	-6.4908	30.5363	-10.7338	26.5657	27.2156	-39.[illegible]
9.50	6.0925	-38.4665	-5.1908	32.7735	-8.2705	28.8487	25.9592	-41.[illegible]
10.00	2.7280	-39.0117	-2.3840	34.1077	-6.8835	29.8157	23.5947	-42.[illegible]

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