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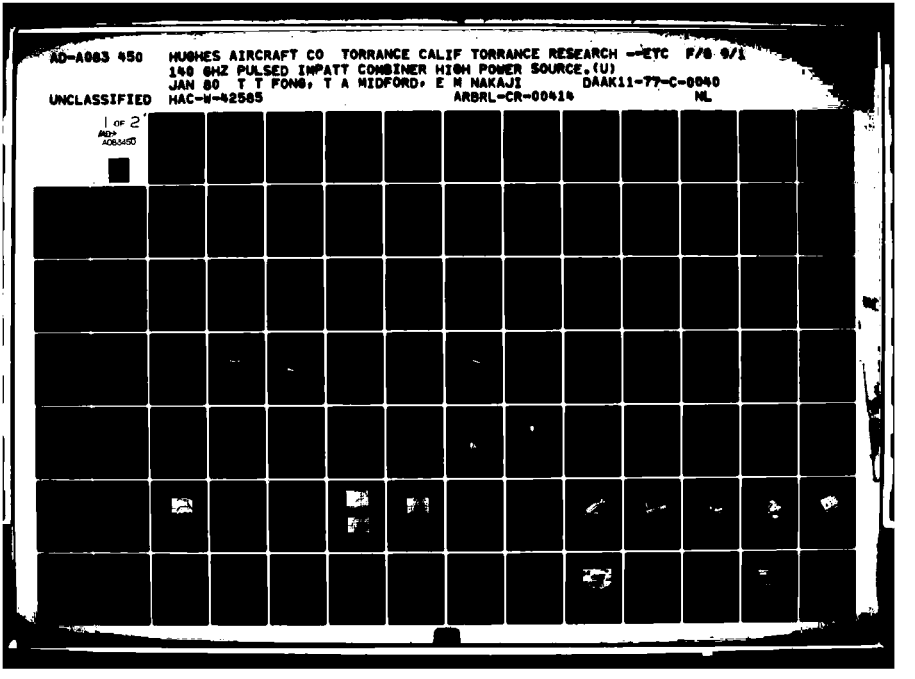

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# 140 GHz PULSED IMPATT COMBINER HIGH POWER SOURCE

Prepared by

Hughes Aircraft Company
Torrance Research Center
3100 W. Lomita Blvd.
Torrance, CA 90509



January 1980

US ARMY ARMAMENT RESEARCH AND DEVELOPMENT COMMAND
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Pulsed IMPATT Oscillators
IMPATT Diodes

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The objective of this program was to develop silicon IMPATT diode and power combiner circuit technology in order to demonstrate improved pulse power generating capability at 140 GHz. The program efforts have led to significant advances in the state-of-the-art for pulsed solid state power generation in D-band.

The diodes fabricated for this program were double drift IMPATTs with active regions formed by a combination of n-type epitaxial growth and multiple

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20. dose/energy p-type ion implants. Since the diodes were intended for operation under short pulse (∿ 100 ns) conditions, copper heat sinks were used.

Several diode package configurations were studied. The most successful was a double quartz standoff configuration.

Three types of power combining structures were investigated in detail during the program. These included:

1) A resonant rectangular waveguide structure with center-mounted diodes.

2) A variation of (1), employing the coplanar biasing configuration.

3) A rectangular waveguide combiner with sidewall-mounted diodes (Kurakowa circuit).

Of these three combiner circuits, the rectangular cavity with sidewall mounted diodes was by far the most successful. In this circuit, power from two pulsed diodes was combined with approximately 90% combining efficiency.

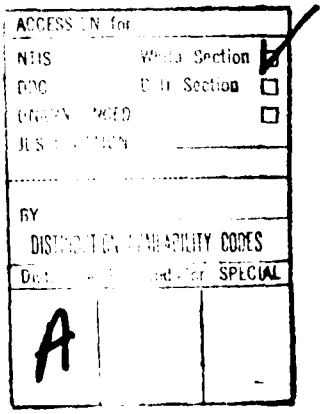
As a result of techniques developed during the program, high peak power output at 140 GHz was achieved for both single and multiple diode oscillators. As a result of improved diode design and fabrication, single diode peak power levels of 3.0 watts at 3% efficiency were obtained for a 100 ns pulse length and a 50 KHz pulse repetition frequency. This represents an approximate factor of four increase in single device power during the program. In addition, a two-diode power combiner based on an oversize version of Kurakowa circuit was constructed which produced 3.0 watts of peak output power.

At the conclusion of the technical effort, two high power pulsed sources complete with modulators were delivered to the Army. One of these sources is a single diode oscillator, the other a two diode power combiner oscillator. Both of these sources meet the program object of 3.0 watts of peak output power at pulse lengths of 50-100 ns.

## FOREWORD

This project (Contract No. DAAK11-77-C-0040) was initiated by the U.S. Army Ballistic Research Laboratories. The project monitor was Mr. Dick McGee (DRDAR-BLB). This report is a summation of the entire program effort conducted from 1 July 1977 through November 30, 1978. This report was submitted by the authors June 1979.

The work reported herein was carried out at the Hughes Aircraft Company Torrance Research Center, Torrance, California under the direction of K. P. Weller and T. A. Midford. Other principal contributors were C. Chao, T. T. Fong, E. M. Nakaji and Y. C. Ngan. Technical assistance was provided by F. C. Fischer, A. E. Martin, M. G. Padella, and G. Watanabe.



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# I. INTRODUCTION

The objective of the work described in this report was to develop a 140-GHz pulsed IMPATT diode power combiner high power source. Advanced diode, packaging and combiner circuit technologies were developed and implemented for this program which resulted in state-of-the-art results for pulsed IMPATT diodes operating at 140 GHz and the first demonstration of efficient pulsed power combining from more than one IMPATT diode at frequencies above 100 GHz. The performance goals for the power combiner are summarized in Table I.

TABLE 1

140 GHz PULSED POWER COMBINER GOALS

| | |
|---|---|
| Frequency | 140 GHz |
| Peak power output | 3 W |
| Pulse length | 100 n sec |

Additional technical goals of the program were: (1) to further develop and refine 140 GHz IMPATT diode technology to the end of achieving the reproducible fabrication of 1 watt peak power diodes, and (2) to demonstrate the feasibility of adding power from two or more IMPATT diodes at 140 GHz.

The development efforts on this program were carried out in three major areas: IMPATT diodes, diode packaging and power combiner circuits. The diodes fabricated for the program were double drift region (DDR)

silicon IMPATTs with active regions formed by epitaxial growth and ion implantation. Attempts were also made at fabricating diodes entirely by multiple epitaxy, the performance of these diodes; however, was inferior to that of the ion implanted structures. A semi-empirical design approach was adopted which consists of successive iterations of a combination of theoretical analysis and experimental results. At the end of the program, the best performing diode lots had measured doping profiles in good agreement with optimized design predictions. Because the devices used on this program were operated at short pulse lengths (~100 n sec) and low duty cycle, copper heat sinks were used.

Several variations of IMPATT diode package were investigated. These include single and double quartz standoff configurations as well as the direct - contacted (packageless) diode and a low inductance pedistal version of the standard Hughes quartz ring package. Of these, the double quartz standoff package was by far the most sucessful. All of the high power pulsed diodes developed during the program used this package.

The major millimeter wave power combiner circuits which were studied during the program include: (1) a rectangular resonant waveguide cavity employing center-mounted diodes, (2) an alternate version of (1), the so-called "coplanar biased" waveguide combiner circuit, and (3) a rectangular resonant waveguide combiner employing wall-mounted diodes. The latter is the Kurakowa circuit used sucessfully at X-band with up to 8 diodes. We have used a variation of the Kurakowa circuits to combine power from two pulsed IMPATT operating near 140 GHz with approximately 90% combining efficiency.

The work described in this report has led to the achievement of some very significant progress including a substantial advance in the state-of-the-art performance of pulsed IMPATT diodes operating at 140 GHz. Specifically we have achieved:

1. A peak output power of over 3.0 W from a single pulsed IMPATT diode operating at 140 GHz.

2. The first demonstration of highly efficient power combing at 140 GHz. Using two diodes in the Kurakowa type circuit, we have fabricated a pulsed power combiner which generates 3 watts of peak output power.

The performance objectives of this program have thus all been met or exceeded.

At the conclusion of the technical effort, two pulsed sources complete with modulator were delivered to the Army. Both of these sources met the program goal of 3.0 watts of output power. One source was a single diode pulsed oscillator operation at 140 GHz, the other a two diode pulsed power combiner/oscillator operating near 145 GHz.

In Section II of this report, the IMPATT diode design, fabrication and packaging procedures are described. Section III deals with power combiner circuit development. Section IV presents performance data for the pulsed diodes and power combiner circuits. Section V summarizes the performance of the delivered hardware. Finally, Section VI presents the conclusions and suggestions for future work. In Appendix A additional specifications and operating procedures for the delivered hardware is provided.

## II. IMPATT DIODE DEVELOPMENT

In this section, the technical approach used to develop pulsed IMPATT diodes at 140 GHz is described. The procedure for the IMPATT diode design is discussed in Section 2.1. The diode fabrication techniques are described in Section 2.2. Section 2.3 deals with diode package design and fabrication.

### 2.1 DIODE DESIGN

The key parameters involved in the design of IMPATT diodes are the doping profile, epitaxial-region thickness, diode area and the thermal resistance. A semi-empirical approach was used to determine the optimum values for these parameters. In some cases, theoretical device models were used to determine the initial design parameters. However, these models are limited due to the many physical approximation required to make practical calculation.[1,2] There are also basic limitations due to the unavailability of certain fundamental material parameters. Therefore, a design procedure based on an approximate theoretical analysis and experimental data was used. This semi-empirical approach has resulted in the achievement of state-of-the-art results for pulsed diodes at 140 GHz.

To achieve maximum peak power output at 140 GHz, we have concentrated on developing double drift IMPATT diodes with optimum doping profile and expitaxial layer thickness for pulsed operation. The double drift diode has been chosen as our approach because of its established high power and efficiency capabilities, as well as its high device impedance for easier circuit matching to achieve optimum performance. The pulsed diode, however, operates at much higher current densities than the CW diode, its design is quite different and must be considered separately. Another unique property of the pulsed IMPATT diode is that the operating

frequency chirps across the bias pulse because of the temperature variation during the pulse. This frequency chirp characteristic is often used in a radar system to improve the glint and clutter rejection, and is therefore an important property. In the following the pulsed diode design and thermal considerations are summarized. Based on these considerations, a summary set of device parameters is then presented for 140 GHz pulsed operation.

### 2.1.1 Doping Profile and Depletion Layer Thickness

For pulsed double drift IMPATT diodes, the primary design consideration is the impedance-frequency characteristic of the diode as a function of current density. Because IMPATT operation is strongly current dependent, the frequency for peak negative conductance is a function of the operating current. As current density increased, the optimum frequency increases and so does the diode output power. For CW diodes the maximum current density is limited thermally, but for pulsed diodes this limit is extended many times depending on the pulse width and duty factor. For extremely narrow pulse widths and low duty operation, the diode is no longer thermally limited. The current density can be further extended until space charge effects cause power saturation and efficiency reduction. In other words the ultimate diode output power is limited electronically.

To design a pulsed diode, it is necessary to predetermine the operating current density. However, the operating current density is also intimately dependent on several other factors, such as pulse width, duty factor, power output and device impedance. The choice of an optimum current density must therefore be derived from certain trade-offs and the optimization of as set of parameters simultaneously. Based on a detailed transient thermal analysis of a pulsed diode and a nominal 3 watt per diode power level, an optimum current density of approximately $10^5$ Amp/cm$^2$ is appropriate. This optimum current density is obtained

assuming a maximum junction temperature of 250°C. With a given operating current density and junction temperature, the diode doping profile can then be designed.

The profile design is based on a symmetrical double drift region structure as shown in Figure 1. The structure has equal doping densities in the n and p regions. It has been established both theoretically and empirically that the symmetrical DDR diodes are capable of nearly optimum performance in terms of output power and efficiency. The asymmetricaly design which compensates the unequal ionization rates of electrons and holes results in very minor improvement in the device performance. On the other hand, an optimum asymmetrical design requires a full knowledge of the large signal behavior of the DDR diode which is strongly circuit dependent. It is therefore difficult to ascertain the optimum device parameters. More importantly, the minor improvement that can be gained from an asymmetrical design, can be easily lost through complication in epi growth or uncertainties in the design parameters, such as field and temperature dependence of the electron and hole ionization rates. We therefore have followed the proven approach and designed the DDR diodes around a symmetrical doping profile for which $N_A = N_D$.

For a given optimum current density and a maximum operating junction temperature, the small signal device admittance can be calculated for a given doping concentration. Strictly speaking, optimum diode design requires knowledge of the large signal characteristics of the device, which in turn is strongly dependent on the circuit parameters. Since an exact analysis and accurate prediction of the circuit response is nearly impossible at D-band (110-170 GHz) frequencies, we base the diode design on the small signal characteristics, modifying the design appropriately to take account of large signal effects. An example of this design approach follows.

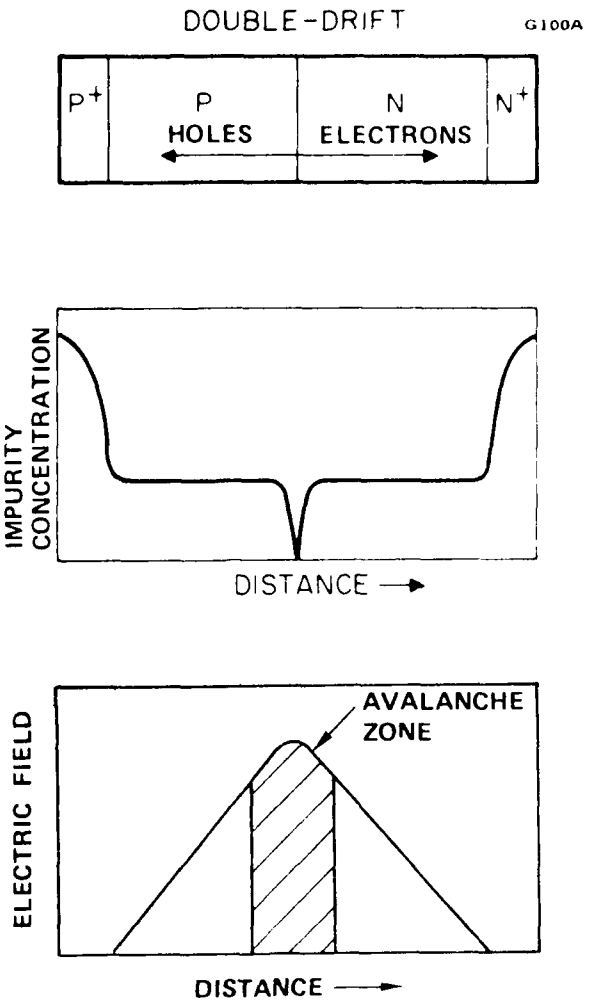


Figure 1 Double drift IMPATT structure.

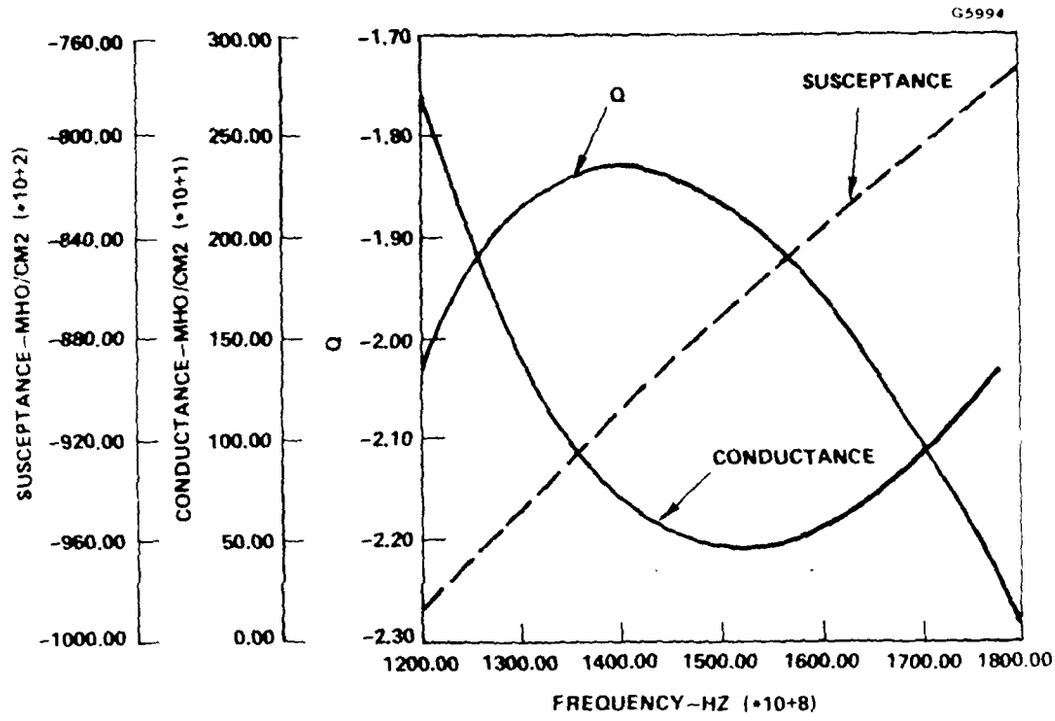


Figure 2 Calculated small-signal conductance, susceptance and device Q as functions of frequency for 140 GHz pulsed double drift IMPATT diode.

Figure 2 presents the calculated small signal device admittance as a function of frequency for $J = 1.2 \times 10^5$ Amp/cm$^2$ and $T_j = 250^oC$. The doping concentration is selected to be $N_A = N_D = 4.5 \times 10^{17}$ atoms/cm$^3$. The device admittance is obtained from a computer simulation based on the analysis of Misawa.[3,4] The ionization rates of Grant[2] and the drift velocities given by Canali et. al.[1] were used in the calculation.

It is seen from Figure 2 that the peak negative conductance occurs at 150 GHz. However, when operating in the large signal condition for optimum power and efficiency, the IMPATT negative conductance decreases in magnitude to approximately half of its small signal value, the device susceptance increases which causes a downward shift in operating frequency. Taking into consideration large signal effects, and to some degree based on experience, we select $N_A = N_D = 4.5 \times 10^{17}$ atoms/cm$^3$ as a reasonable doping concentration for the 140 GHz pulsed diode. At this doping concentration, the diode has a reverse breakdown voltage at room temperature of about 9.5 volts. At a current density of $1.2 \times 10^5$ Amp/cm$^2$ and 250$^o$C junction temperature, the operating bias voltage is 14.0 volts. The higher bias voltage is a result of temperature rise at the junction and space charge resistance.

To complete the diode design, it is required to determine the depletion region widths of the n and p layers. For the symmetrical structure under consideration, the widths of the two regions are equal, it therefore suffices to consider one region only. The total depletion width is simply twice the single layer width.

For optimum diode performance the epitaxial layer thickness must be precisely controlled such that the active epi thickness is equal to the total depletion width at the optimum operating current density and maximum junction temperature. Under this condition the electric field is barely punched through (punch through factor = 1). Further increase in the punch through factor causes widening in the avalanche zone width

which degrades the IMPATT efficiency and output power. On the other hand epi that is too thick results in an unswept region which degrades power and efficiency because of increased series resistance. To achieve optimum performance, it is, therefore, important to determine the diode depletion width at the operating current density and temperature. Since the depletion width for a particular doping concentration at breakdown and room temperature can be determined readily, it is necessary to consider the depletion width widening caused by space charge and temperature effects.

Space charge causes variation of the electric field in the depletion region. This effect gives rise to a voltage increase for an abrupt p-n junction. It can be shown this voltage rise is

$$\Delta V_B = J \frac{(W_D - X_A)^2}{2\epsilon V_s} \tag{2-1}$$

where $W_D$ is the depletion width of a p-n junction diode with a breakdown voltage of $V_B$. $X_A$ is the avalanche region width (in which most of the carriers are generated). Here $\epsilon$ is the dielectric constant of silicon and $V_s$ is the scattering limited electron (or hole) velocity in silicon. J is the current density. Assuming an n doping concentration of $N_D$, the diode breakdown voltage is governed by Poisson's equation, and

$$V_B = \frac{W_D^2}{2qN_D\epsilon} \tag{2-2}$$

where q is the electronic charge. Therefore,

$$\frac{\Delta V_B}{V_B} = \frac{J}{2qN_D V_S}\left(1 - \frac{X_A}{W_D}\right)^2 \tag{2-3}$$

The incremental depletion width, $W_D$, caused by the space charge can now be obtained from

$$\frac{\Delta W_D}{W_D} = \frac{\Delta V_B}{V_B} = \frac{J}{2qN_D V_S}\left(1 - \frac{X_A}{W_D}\right)^2 \qquad (2\text{-}4)$$

For $N_D = 4.5 \times 10^{17}$ cm$^{-3}$, $X_A \simeq 0.30\ W_D$ for double drift diodes; and letting $J = 1.2 \times 10^5$ Amp/cm$^2$ and $V_s = 8 \times 10^6$ cm/sec, we have

$$\frac{\Delta W_D}{W_D} = 0.10 \text{ due to space charge}$$

Thus, the depletion width is increased by about 10% due to space charge effects.

The ionization rates of electrons and holes decrease with increasing temperature. For an IMPATT diode with a given doping concentration the depletion width (or breakdown voltage) will increase with increasing temperature. The incremental depletion width caused by temperature can be obtained by calculating the diode breakdown voltage at room temperature and the operating temperature. For a junction temperature of 250°C and a doping concentration of $N_D = 4.5 \times 10^{17}$ cm$^{-3}$, the voltage rise in relation to $V_B$ at room temperature has been calculated using a computer model and the rise is approximately 20%, or

$$\frac{\Delta W_D}{W_D} = \frac{\Delta V_B}{V_B} = 0.20 \text{ due to temperature rise}$$

The total widening of the depletion region width is therefore 30%. For $N_D = 4.5 \times 10^{17}$ cm$^{-3}$ the total depletion width at breakdown and

room temperature is 0.29 μm. At an operating temperature of 250°C and bias current density of $1.2 \times 10^5$ Amp/cm$^2$, the total depletion width is

$$W_T = 1.30\ W_D = 0.38\ \mu m$$

For a 140 GHz pulsed double drift diode, the electron and hole regions should therefore have a total depletion layer thickness of 0.38 μm.

In summary, the pulsed double drift IMPATT diode requires a lower doping concentration as compared to the CW diode to compensate the much higher operating current density. For 140 GHz operation we have determined that the doping density should be approximately $4.5 \times 10^{17}$ cm$^{-3}$. The high current density and elevated junction temperature also cause considerable widening of the depletion layer. The increase in depletion width is considerably larger in pulsed diodes; it therefore requires a thicker epi layer than a CW diode. For 140 GHz operation, a total active layer width of 0.38 μm is required.

### 2.1.2 Thermal Design

The proper thermal design of pulsed IMPATT diode to achieve both high peak power and low junction temperature lies in the accurate prediction of transient thermal properties of the diode, as it goes through periodic heating and cooling cycles caused by the bias pulses. Once the transient thermal resistance is known, the maximum allowable bias input power to maintain a safe operating junction temperature can be calculated. The required RF power in conjunction with the maximum input power then determines the device junction area and the operating current density. Thus, as a first step, the transient thermal resistance of a diode must be determined.

Consider now the case of a uniform heat source with radius R on a semi-infinite heat sink of thermal conductivity K and thermal diffusivity $\alpha$ as shown in Figure 3. It can be shown that the transient thermal resistance related to the maximum temperature at the center of the diode and at the end of a heating cycle is given by[5]

$$\theta = \frac{2}{\pi RK} + \frac{d^{1/2}(\alpha t_1)^{1/2}}{\pi R^2 K} \left\{ \frac{2}{(\pi d)^{1/2}} \left[ 1 - e^{-R^2/4\alpha t_1} \right] - \frac{R}{(\alpha t_2)^{1/2}} + I + \frac{R}{d^{1/2}(\alpha t_1)^{1/2}} \operatorname{erfc} \left[ \frac{R}{2(\alpha t_1)^{1/2}} \right] \right\} \qquad (2\text{-}5)$$

where

$$I = \frac{2}{\pi d} \int_0^\infty \frac{e^{-dx^2} \left\{ e^{-(1-d)x^2} - e^{-x^2} \right\} \left\{ 1 - \cos \frac{RX}{(\alpha t_2)^{1/2}} \right\} dx}{x^2 \left( 1 - e^{-x^2} \right)}$$

and $d = t_1/t_2$ is the duty factor (Figure 3). The first term is a dc term proportional to the CW thermal resistance; the remainder of the terms consist of a dc contribution as well as an ac contribution following the heat pulse.

For copper K = 3.96 W/cm$^{o}$C and $\alpha$ =1.14 cm$^2$/s. Using these values, the transient spreading thermal resistance for a copper heat sink can

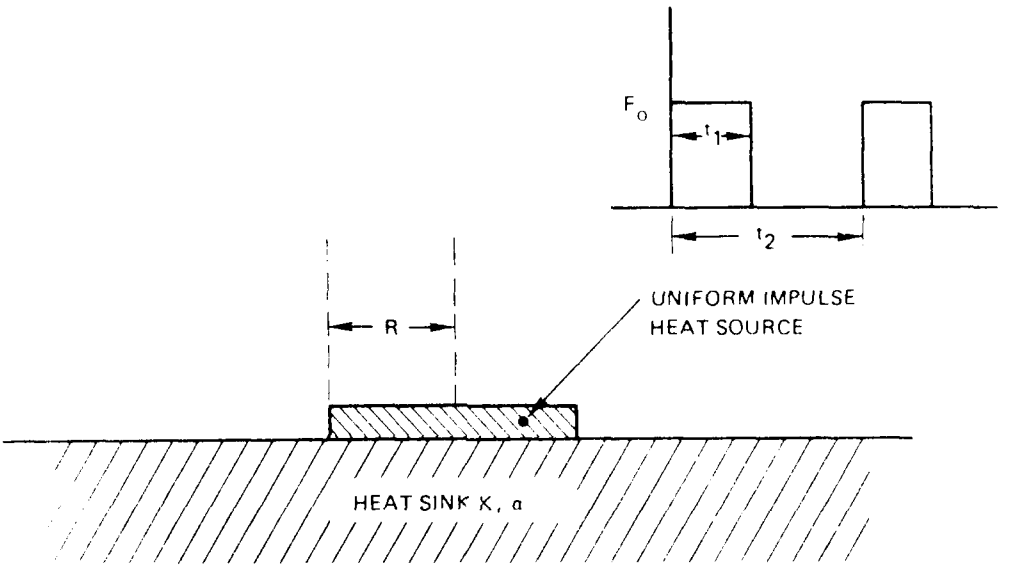


Figure 3 Semi-infinite solid heated by periodic impulse heat source over a circular area.

be calculated using a computer. Figure 4 presents the calculated thermal resistances of copper at 0.5 percent duty factor as a function of pulse width for four diode radii.

In an actual diode, the heat generation is mostly confined to the active layer close to the diode junction. Since the junction for the double drift diode is located at a distance from the heat sink, the silicon layer also contributes to the resistance of heat flow. For typical 140 GHz diodes this layer is approximately 0.2 μm thick with a diameter of approximately 63 μm, its thermal mass is small and so is the thermal time constant. For all practical purposes, at the pulse widths of interest, the thermal resistance contribution from this layer approaches its CW value. We can therefore approximate the thermal resistance of the silicon layer by

$$\theta_{Si} = \frac{t}{\pi R^2 K_{Si}} \qquad (2\text{-}6)$$

where t is the thickness of the silicon layer and $K_{Si}$ is the thermal conductivity of silicon.

For most homing and terminal guidance radar applications at 140 GHz, narrow pulse width is generally required to improve the close-in range and target information. The normal pulse width requirement is typically less than 100 ns with a repetition rate less than 100 KHz. Subsequent thermal design is therefore based a 100 ns pulse width and 100 KHz repetition rate.

The total thermal resistance of an IMPATT diode including the transient thermal spreading resistance and the silicon layer contribution can be calculated using Equations (2.5) and (2.6). Given the input bias power, this thermal resistance defines the maximum junction temperature

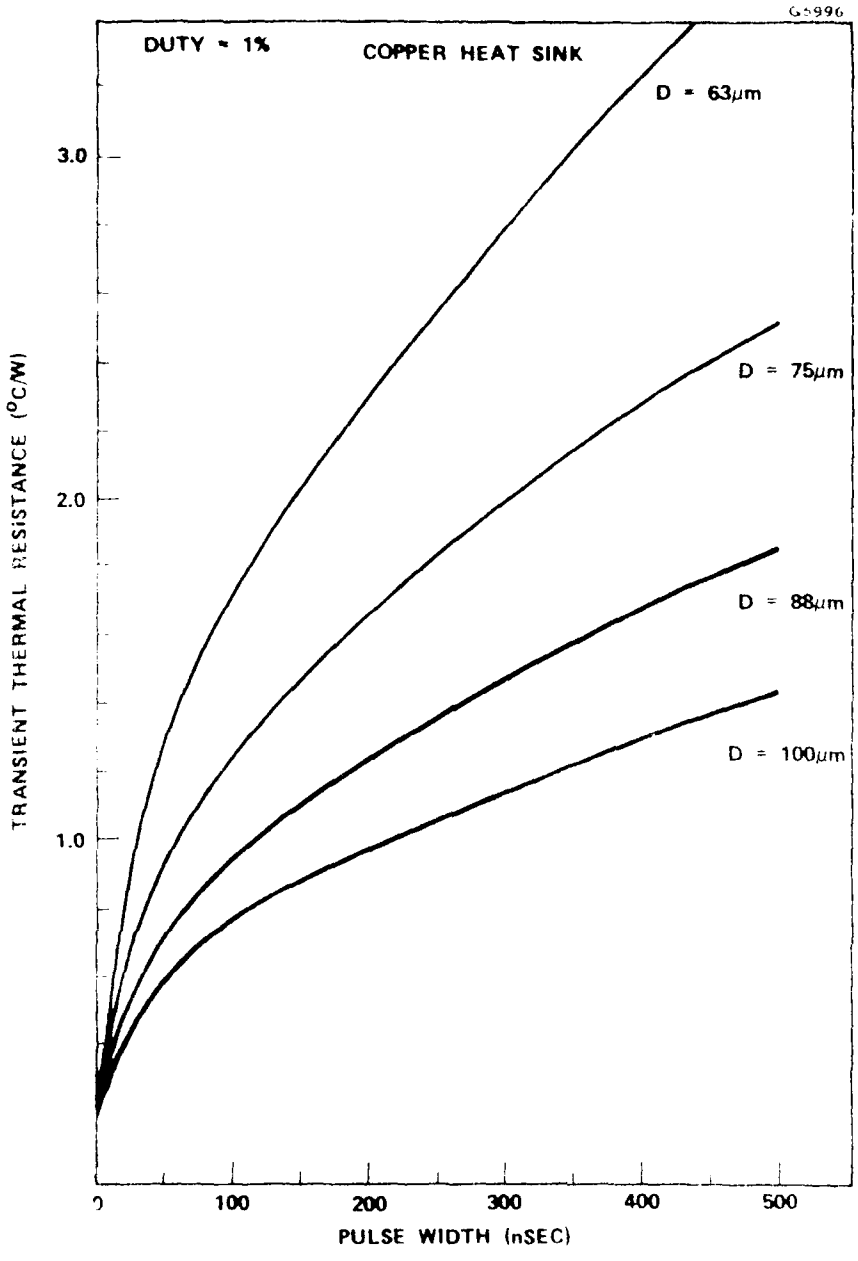


Figure 4. Transient thermal resistance of a pulsed IMPATT diode on a copper heat sink.

rise at the end of a heating cycle. Figure 5 shows the total thermal resistance of a 140 GHz double drift IMPATT diode plotted as a function of junction diameter for a copper heat sink. A fixed 100 ns pulse width and a 1% duty factor are used in this calculation.

For a given input bias power, it is evident from Figure 5 that the junction temperature decreases with increasing junction diameter. Therefore, from thermal considerations alone one would choose a large junction diameter for the diode design. However, the device impedance is inversely proportional to the diode area. In order to match to the circuit impedance for efficient IMPATT operation, the diode diameter cannot be increased arbitrarily. The optimum diode diameter must therefore be chosen in conjunction with the circuit properties. It has been shown that for a typical reduced height waveguide 140 GHz oscillator, a minimum negative resistance of approximately one ohm is required. Using the device admittance as presented in Figure 2, it can be shown that the one ohm negative resistance corresponds to a junction diameter of approximately 75 μm. As shown in Figure 5, for a 75 μm junction diameter, 80 W input power will raise the junction temperature by 225°C for a copper heat sink at 100 ns and 1.0% duty.

Finally, assuming a nominal operating diode efficiency of 4% (reasonable based on experience at 140 GHz and other millimeter wave frequencies, such as 94 GHz), the operating current density may be determined. At an operating junction temperature of 250°C, the diode operating voltage is 14 volts. Thus a pulsed bias current of 5.36 amperes is required, corresponding to a current density of about $1.1 \times 10^5$ Amp/cm$^2$.

### 2.1.3 Design Summary

Factors that influence pulsed double drift IMPATT diode design have been discussed. Diode parameters, such as doping densities, depletion

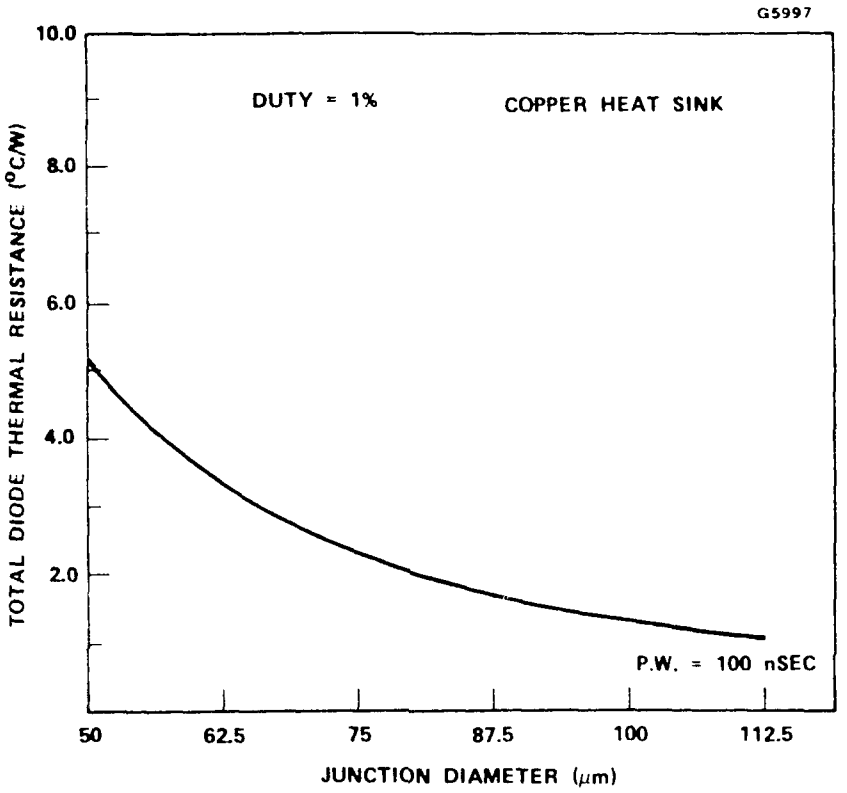


Figure 5 Total pulsed IMPATT diode thermal resistance on a copper heat sink.

layer thickness, [illegible]
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pulsed results achieved on this [illegible]
cated using these design parameters [illegible]
3.0 watts at an operating efficiency [illegible] reasonable to assume that further refinements in diode fabrication and circuit design will result in further improved performance. Table 2 is a summary of pertinent design parameters for the 140 GHz pulsed double drift diode.

During this program, diode lots were fabricated with design parameters varying around the values shown in Table 2-1. At the conclusion of this program, and based on the results achieved, we believe this design to be near optimum for high power pulsed 140 GHz diodes.

TABLE 2

140 GHz PULSED DDR IMPATT PARAMETERS

| | |
|---|---|
| Doping Concentration | $N_D = N_A = 4.5 \times 10^{17}$ cm$^{-3}$ |
| Epi Thickness | $W_D = W_A = 0.19$ µm |
| Breakdown Voltage | 9.4 volts |
| Junction Diameter | 75 µm |
| Current Density | $1.2 \times 10^5$ Amp/cm$^2$ |
| Bias Voltage | 14.0 Volts |
| Bias Current | 5.36 Amps |
| Efficiency | 4% |
| Peak Power Output | 3 Watts |
| Heat Sink | Copper for p.w. $\leq$ 100 ns |

## 2.2 DEVICE FABRICATION TECHNOLOGY

In this section, the standard IMPATT diode fabrication process established in our laboratory is first outlined. The critical steps in the 140 GHz IMPATT diode fabrication are then described in detail including material growth and evaluation, junction formation and substrate thinning.

Throughout this program, the principal approach to device profile fabrication has been the use of multiple dose and energy ion implantation to form the "p" portion of the $p^+$-p-n-$n^+$ device profile. Alternatively, this layer may be formed by p-type epitaxy. In general, the performance of devices fabricated using the multiple epitaxy approach was substantially inferior to the ion implanted diodes and during the latter portion of the program, the former approach was dropped. In general, the reason for the lack of success of the epitaxial diodes is believed to be lack of precision in layer thickness and doping density control. Note that high power 94 GHz pulsed diodes are routinely fabricated using multiple epitaxy.

### 2.2.1 Standard Fabrication Procedure

The following is an outline of the standard diode fabrication procedure used for making double-drift region diodes. The process steps are subsequently discussed in detail in Sections 2.2.1a to 2.21f.

| Step | Procedure |
|---|---|
| 1. | An n-type epitaxial layer is grown on an $n^+$ silicon substrate wafer. |
| 2. | The p-n junction and the p-type drift region are formed by ion implantation of boron. |

3. A $p^+$ contact region is diffused into the front (p-type) side of the wafer.

4. The front side is metallized with evaporated chromium, platinum, and gold in that order. Plating is then used to increase the thickness of the gold.

5. The substrate is thinned by chemical etching to between 8 and 10 μm.

6. Chromium and gold metallization is evaporated on the back (substrate) side of the wafer followed by gold plating.

7. Photolithography is used, first to isolate 5 mil diameter silicon mesas by etching through the silicon down to the front metallization and then to define metal islands concentrically on the back of the mesas to use for contact pads. The center-to-center separation at the mesas is 25 mils.

8. The diodes are separated by ultrasonic vibration.

9. The diodes are thermocompression bonded onto gold-plated copper heat sinks.

Early in the program, some lots of diodes were fabricated on integral plated silver heat sinks. In processing these devices, silver is plated on the front (junction side) of the wafer to a thickness of 5 to 8 mils following step 5. Steps 6 and 7 are then carried out. The diode center-to-center spacing for the plated heat sink diodes is increased to 75 mils. Following mesa isolation, diode-heat sink assemblies are mechanically punched out of the silver heatsink wafer. A major consequence of the plated heat sink process is a reduction in yield (roughly 10:1) because of the increased center-to-center diode spacing. During the latter

portion of the program, nearly all diodes were processed using the "pill" process, and consequently diodes were individually thermocompression bonded to copper heat sinks. In most respects, this is the preferred process because of: (1) improved yields, (2) shorter process turn around and (3) greater packaging flexibility.

2.2.1a Epitaxial Silicon Material

The growth of silicon epitaxy for IMPATT diodes is accomplished using the pyrolysis of silane through the following simplified reaction:

$$SiH_4 \longrightarrow Si + 2H_2$$

The reaction is complete at temperatures above 800°C. The growth temperature used is 1000°C. This temperature is optimum for obtaining good thickness control and reproducibility while limiting outdiffusion of the dopant from the substrate. The growth rate is normally 0.5 μm/min and is relatively constant over a wide temperature range when using a silane concentration in hydrogen of 0.14 percent and a flow rate of 75 liters/min. The corresponding gas velocity is 20 cm/sec, a relatively high velocity. This provides good thickness uniformity over the length of the susceptor. However, for 140 GHz IMPATTs, a slower growth rate of 0.2 m/min has to be used to achieve proper control of the epitaxial thickness.

A horizontal 35 kW Radyne reactor was used exclusively for growing silicon IMPATT diode wafers for this program. The reactor tubes are water cooled so as to minimize deposition on the tube and also to effect a faster cool down which minimizes outdiffusion. The silicon substrate is gas etched at a temperature of 1200°C using HCl for about 10 minutes so that all surface damage and impurities are etched off. The temperature is then reduced to 1000°C to initiate growth. A typical epi-layer grown using silane pyrolysis normally has a dip in the concentration

profile near the substrate-epi interface. This is due to the fact that the dopant does not sufficiently mix with the silane gas when introduced into the system. One obvious solution is to allow the gases to come to an equilibrium state in some form of a mixing box before being introduced into the reactor chamber. For this purpose we have built an epitaxial reactor which provides the premixing capability to avoid the thin, high resistivity layer at the $n^+$-n interface. It also has the capability for multi-layer growth with various doping combinations.

This is essential in the development of multi-epitaxial double-drift diodes. A schematic of the reactor is shown in Figure 6. The reactor has both p and n type doping with all the necessary refinements for best gas flow patterns and mixing. Details of the gas handling system designed to accomplish this are shown in Figure 7.

After the growth cycle ends, the reactor is cooled down to 850°C immediately. All residual silane gas is flushed out and then the tube is cooled down to room temperature at a slow rate. This procedure minimizes outdiffusion and at the same time avoids crystal damage due to thermal stress.

2.2.1b Evaluation of Epitaxial Material

A key step in high frequency IMPATT fabrication is evaluation of the deposited epitaxial silicon. The epi layer must not only have the proper thickness and resistivity necessary to obtain the desired frequency characteristics, but the impurity concentration as a function of distance through the layer must be uniform with no concentration irregularities or variations in excess of about ±10 percent. Also, back diffusion into the epi layer from the highly doped substrate must be minimized during epi deposition and p-n junction formation. To monitor the quality of the epi material, a representative impurity doping profile is obtained

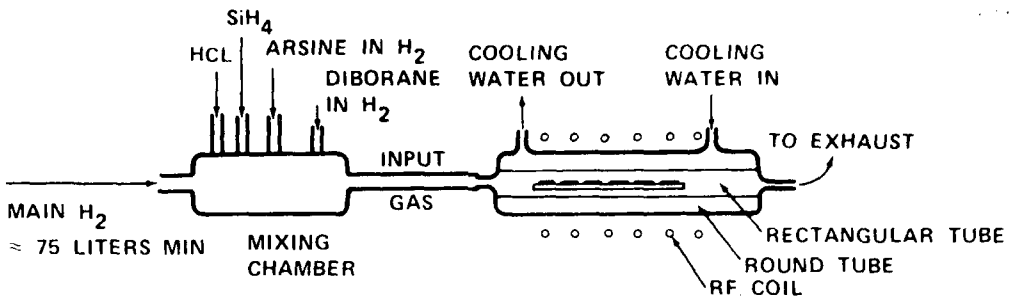



Figure 6 Schematic diagram of silicon epitaxial reactor.

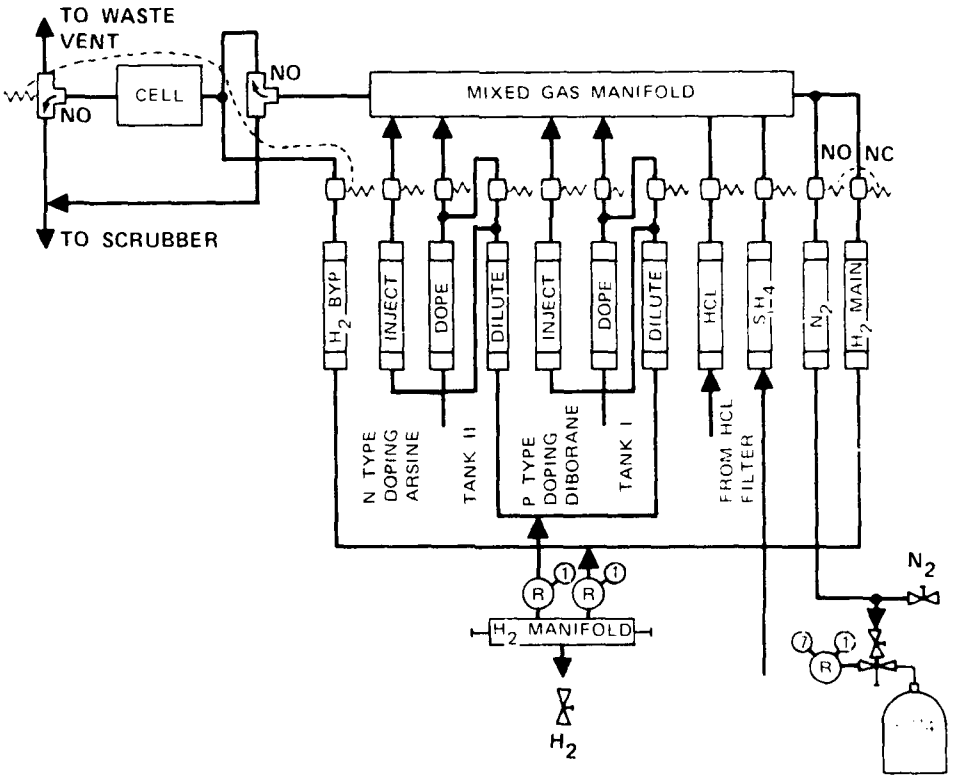



Figure 7 Details of gas flow controls for the epitaxial reactor.

for all epi runs utilizing capacitance versus voltage measurements made on selectively located p-n junction regions.

Capacitance per unit area at zero bias is a function of the background impurity concentration. As the reverse voltage is increased, the junction depletion layer width increases while the capacitance decreases. The doping concentration at various levels below the epi surface can be obtained from the capacitance at various depletion layer widths. An automatic doping profiler which gives a direct plot of doping vs. depth on a log-log scale is used for this purpose. If the epi thickness is greater than the depletion depth below the surface at breakdown, such as in epi material for double-drift IMPATT diodes, then part of the epi material must be removed before forming a sample p-n junction so that the depletion region of the sample junction will approach and enter the substrate. To do this the silicon surface must be etched in the form of steps with accurately known step heights. For the 140 GHz double-drift IMPATT diodes, a total active layer thickness of 0.38 μm is required. However, breakdown will limit capacitance measurements to depletion widths of approximately 0.1 μm. Thus junctions made on a wafer with four to five steps with 0.08 μm step-height will ensure that the depletion width will enter the substrate on the 3rd and 4th step. By adjusting for the etched steps, the impurity profiles can be plotted from the junction depth below the 1st step (original epi surface) through the entire layer and into the leading edge of the substrate. The accurate doping density profile characterization is essential, particularly for double-drift IMPATT diode fabrication.

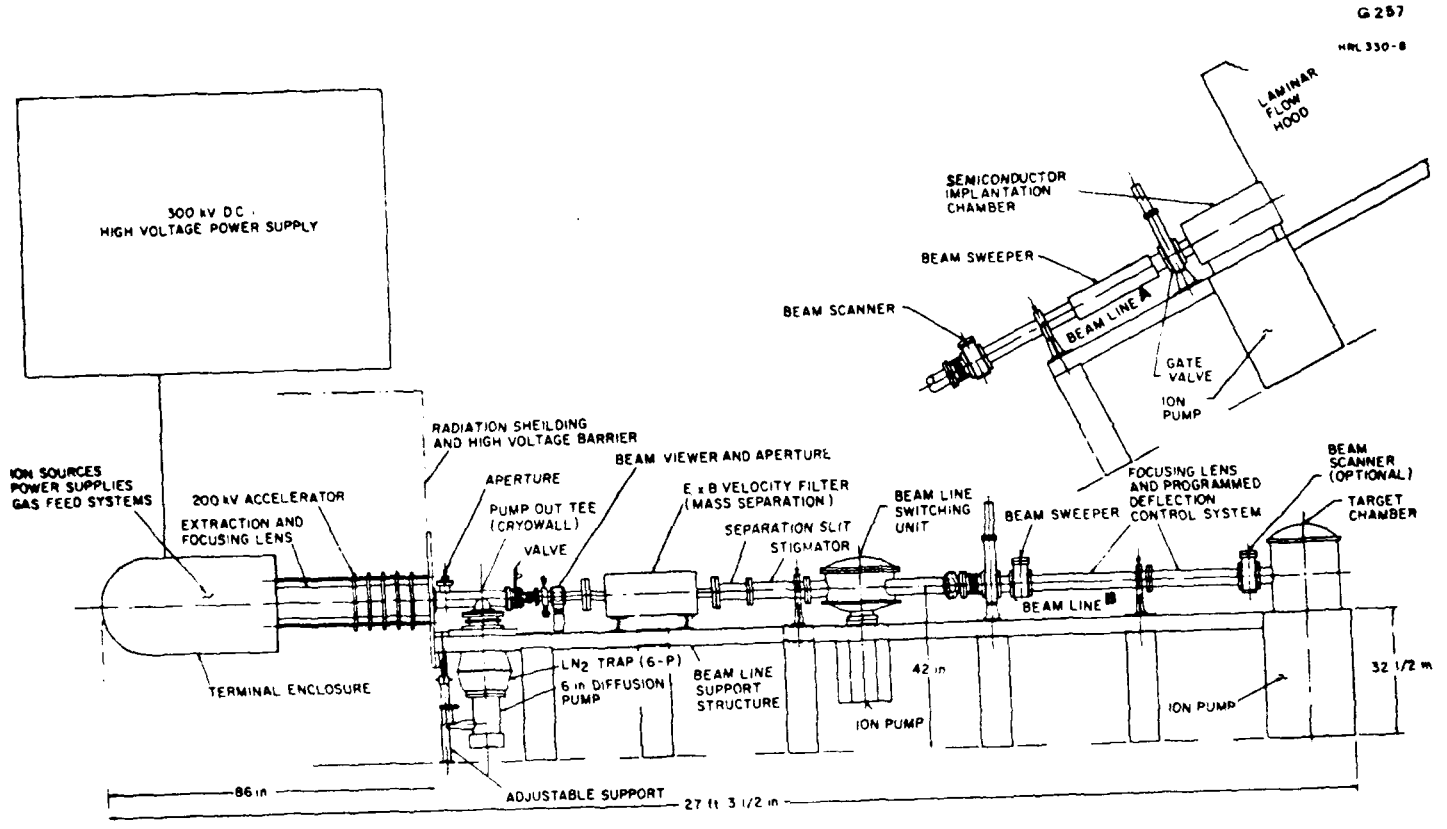
A p-type sample wafer is also included in each epitaxial run. A sheet resistivity measurement and an angle lap and stain thickness measurement are made on this sample wafer immediately after the run. This control step provides prompt first order information on any major discrepancies in the growth parameters so that necessary corrective action can be taken immediately.

2.2.1c Ion Implantation

A 300kV ion implantation machine at Hughes Research Laboratories in Malibu has time dedicated to double-drift IMPATT diode development. A schematic drawing of the machine is contained in Figure 8.

To make double-drift IMPATT diodes, boron ions are implanted into an epitaxial silicon wafer of the proper doping and thickness. The implant schedule is determined according to the frequency of operation and is modified to accommodate slight variations of the epitaxial silicon material parameters from the design values.

In order to properly establish the p-type drift-region in the double-drift $p^+pnn^+$ structure, the ion implation must have the following characteristics: (1) ion purity ($^{11}B^+$), (2) accelerating energy control, (3) dose control, and (4) uniformity across the wafer. In addition to these controls, the wafer must be oriented in a random direction (off crystalline axes) with respect to the incident beam to avoid unwanted axial or planar channeling effects. Accurate doping profile measurements on implanted layers play a key role in establishing the range-energy and activity-dose relations for the high energy implant machine used for the double-drift diode development. The ion distribution in the epitaxial layer is approximately Gaussian in shape. The Gaussian distribution is characterized by a mean range ($R_p$) and a mean variance or straggling ($\Delta R_p$) about the mean range. Since the expression for the composite profile is given by a summation of exponential terms, the functional dependence of $R_p$ and $\Delta R_p$ on energy has been established for boron and other ions in silicon. From the doping profile design of the double-drift diodes, these data are used in computer programs to establish the dose-energy schedule for the implatation. As an example, the doping profile design of a 140 GHz double-drift IMPATT diode implanted with boron is shown in Figure 9. Note that the $p^+$ diffusion ($\sim$1.5 μm in depth) is not shown.




System Characteristics

Ion species: all
Ion voltage range: 10 to 300 kV
Beam current: 0.01 to 100 μA
Mass separation: 60-cm EXB filter
Pumping: trapped diffusion pumps (2) and ion pumps (3)
Special: three beam lines with electrostatic switching

Figure 8 Schematic of 300 kV ion implantation machine.

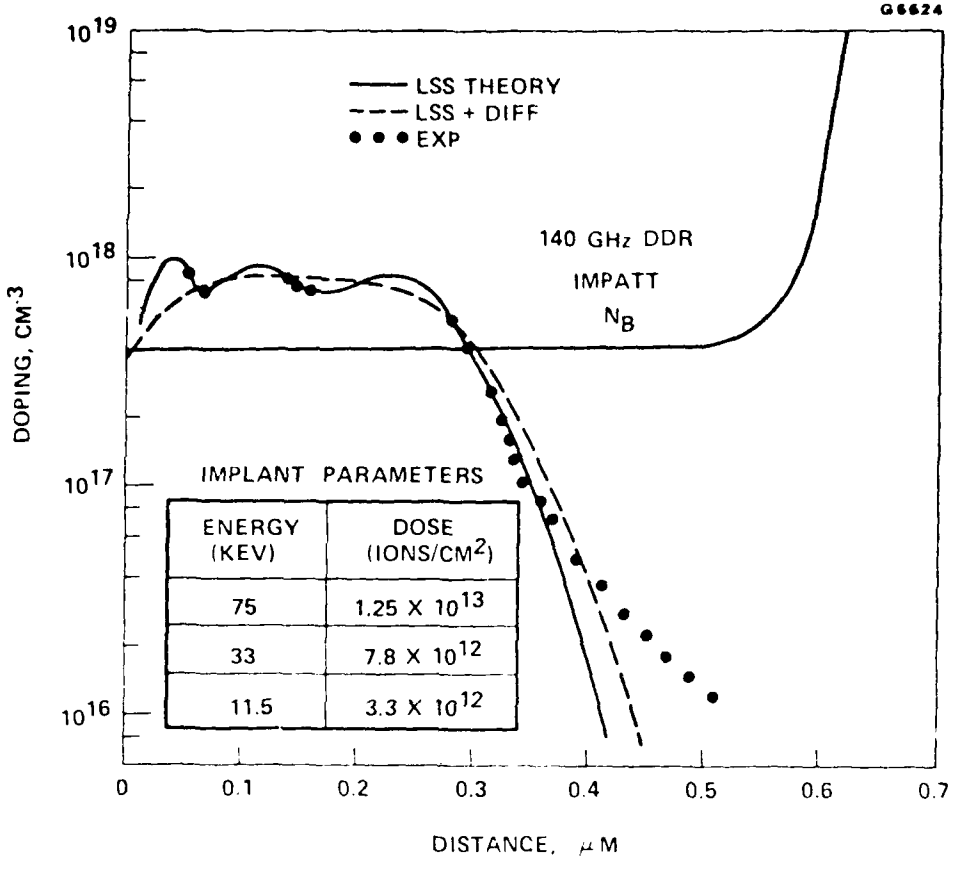



Figure 9 140 GHz Double Drift IMPATT Profile

### 2.2.1d Low Temperature Diffusion

The double-drift IMPATT diodes fabricated for this program require a shallow $p^+n$ diffusion. To ensure that the p dopant (boron) diffusion does not degrade the epitaxial N-type doping profile, the diffusion temperature must be kept low ($\leq 1000^{\circ}C$). At this temperature the boron diffusion is relatively slow, as is the outdiffusion of arsenic from the substrate. Because of the difference in diffusion coefficients, diffusion from the surface from a high concentration boron source is typically over five times faster than outdiffusion from the substrate. Thus for a 0.15 μm diffusion depth, the outdiffusion from the substrate is less than 0.03 μm which is acceptable for high performance IMPATT devices.

Diffusion at lower temperatures has similar behavior. The $1000^{\circ}C$ temperature is chosen primarily because of ease of depth control. For higher temperatures the control is more difficult because the total time for a shallow diffusion is less (on the order of one to two minutes). The time required for the temperature to stabilize is longer than this, resulting in unwanted outdiffusion from the substrate.

In the present diffusion furnaces, as shown schematically in Figure 10, the doping is done by bubbling nitrogen (Ns) through a liquid source (trimethyl borate). The doping gas thus formed is flowing at a high rate so as to create a high surface concentration. The gas handling system for our diffusion tubes is also shown in Figure 10. The wafers are loaded onto a quartz boat and pushed into the furnace tube at a temperature rate of $100^{\circ}C$/minute until the boat is situated in the $1000^{\circ}C$ flat zone. A stabilization time of three minutes is allowed before the source is turned on. Nitrogen ($N_B$) is the carrier gas flowing at a rate of about 2 liters/minute. Before going into the tube, the nitrogen is mixed with doping gas and oxygen gas ($O_B$). The oxygen is present to slightly oxidize the silicon surface to prevent a compound containing

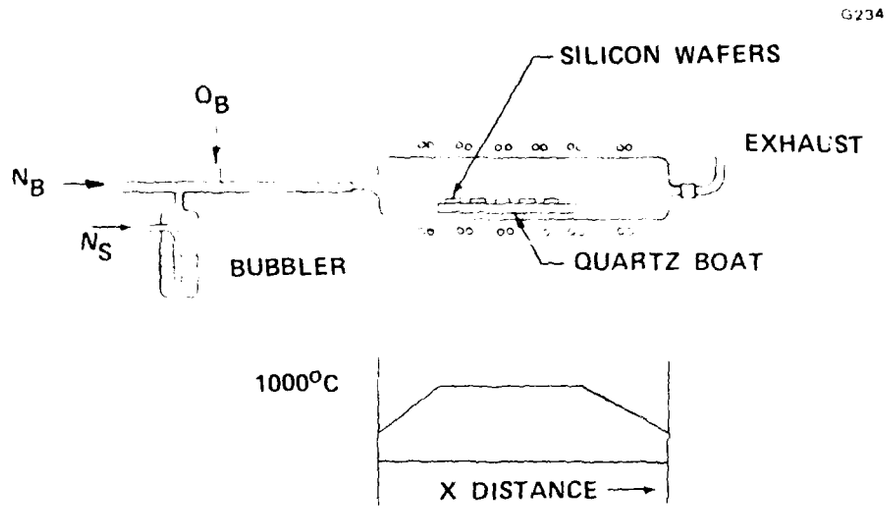



Figure 10 Schematic of diffusion furnace.

boron and silicon, which is insoluble in most acids, from forming. Diffusion time for a junction depth of 0.15 μm is 4 minutes. The depth is measured on a sample wafer by angle lapping and staining to bring out both the epitaxial thickness and diffusion depth. If the total epitaxial thickness is known, the junction depth can be most easily measured as a fraction of total thickness. V/I measurements are made on the sample wafer after diffusion for evaluating the surface doping concentration.

### 2.2.1e Substrate Thinning

Reducing the substrate thickness is critical for millimeter wave IMPATT diodes because of parasitic series resistance effects. Standard substrate thinning techniques were applied for the DDR diodes made for this program.

The wafer substrates are first pre-etched to 75-100 μm in thickness. They are then mounted on a sapphire disk with black wax, and chemically etched to 8-10 μm. The etchant is a 3:5:3 mixture of $HF:HNO_4:HAC$, with a small content of $Br^+$ ions. This etchant is used for critical substrate thinning because it yields reproducible etch rates and a good surface morphology. The use of this procedure has generally yielded excellent results for this high frequency program, except for some difficulty with wafer non uniformity (see Section 2.2.2).

### 2.2.1f Metallization

From past experience in life testing, a system of metallization employing evaporated chromium (700 A), platinum (2000 A) gold (1500 A) and plated gold (6000 A) on the front ($p^+$) side of the wafer has given consistently reliable results. This metallization scheme was used for both the single and double-drift diode lots fabricated for this program.

The evaporated layers are produced in on a cyro-sublimation ion-pumped vacuum system with an electron beam-heated source. The wafers are heated to approximately 100°C prior to the evaporation of the metal layers. The metallization on the back or substrate side of the wafer consists of evaporated chromium (700 A) and gold (1500 A) and plated gold (6000 A).

### 2.2.2 Modified Grid-Etch Thinning Process

It has been mentioned previously that reducing the substrate (i.e., the $n^+$ region) thickness is critical. The standard thinning procedure sometimes results in non-uniformly thinned wafers. In order to develop thinner and more uniform diodes, a modified grid etch technique was investigated, under other program funding, for the DDR wafers.

For this technique, the $p^+$ contact region was formed by boron diffusion, and photolithography was used to define a pattern of 8.0 mil diameter dots on the front ($p^+$) side of the wafer. The dot center-to-center spacing was 75 mils. Next, the silicon material between the dot pattern was etched to a depth of approximately 4 μm with a Sirtl etch solution. The front side of the wafer was metallized with Cr-Pt-Au and then plated with silver. The back $n^+$ substrate) side of the wafer was then thinned using a wet chemical etchant. As soon as the front side metallization was observed to penetrate the substrate, the etching was stopped and the required diode thickness ($\sim$4 μm) was then obtained. If the original wafer thickness was non-uniform, the parts of the wafer where the metallization first appeared were protected with wax. Thinning then continued on the remainder of the wafer. After thinning, the back side of the wafer was metallized with Cr-Au and diodes were formed out of the 8 mil diameter mesas using photolithography. Finally, the silver layer was etched away and the individual diode pills separated.

Figure 11 shows one of the diode pills before separation. The larger circular area surrounding the pill represents one of the 8 mil dots originally used as a mask during the initial wafer etch. Scanning electron microscope (SEM) photographs of the finished diodes have shown this technique to be successful in reducing the diode thickness to 6-8 μm.

## 2.3 PACKAGE DESIGN AND FABRICATION

For pulsed IMPATT diode oscillators above 100 GHz, particular attention must be paid to package design and the reduction of parasitics. This section describes the approach to these problems and the development of the final package.

### 2.3.1 Package Design

For this program, several low parasitic package configurations were investigated. The best performance was obtained from the double standoff package shown in Figure 12. This package was used on all of the combiner hardware supplied at the conclusion of the program. Comments on the double standoff configuration and other packages investigated during course of the program are given in the remainder of this section.

#### 2.3.1a Single Standoff Package

For minimum parasitics combined with a reasonably rugged mechanical configuration, the open quartz standoff type package is the most widely used and in general the most successful diode package configuration for use above 100 GHz. The simplest version of this package is the single standoff version shown in Figure 13. Many versions of this package have been assembled and tested at Hughes over the past several years. In general for millimeter wave high power pulsed IMPATT diodes, we have found it highly desirable to minimize the parasitic series inductance

E2215

Figure 11. Diode pillformed or modified grid electrochemique. Magnification = X.

E2311

Figure 1. Double standoff high power 140 GHz diode. (210X)

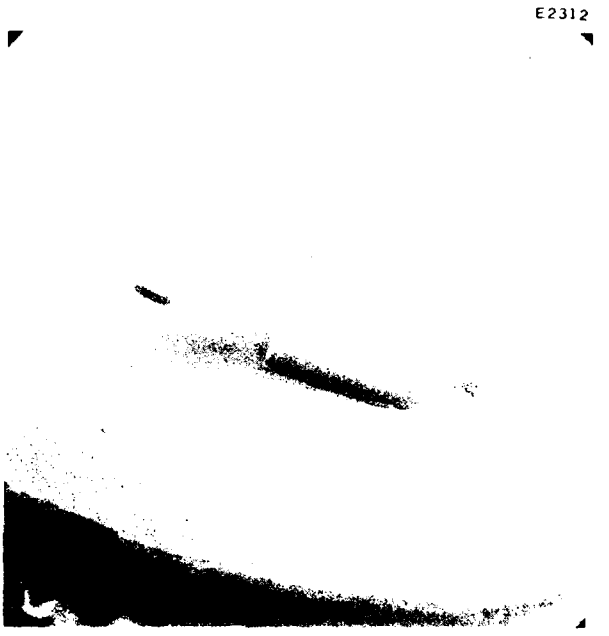



Figure 13 Single quartz stand-off packaged diode for 140 GHz pulsed source (200X).

associated with the ribbon or preform connecting the diode to the standoff. This has given rise to several minimal inductance package configurations which are discussed below.

### 2.3.1b Double Standoff Package

The double standoff diode package shown in Figure 12 has a lower series inductance than the single standoff for 140 GHz high power pulsed IMPATT diodes. This package was used throughout the latter stages of the program and, as noted above, was supplied on all deliverable hardware. Figure 14 shows the double standoff package schematically with the circuit contact pin. Note that the total parasitic shunt capacitance seen by the diode includes the contribution from the quartz blocks as well as the fringing capacitance from the post. As a result, the addition of a second standoff results in only a nominal increase in total shunt capacitance, but a significant decrease in series inductance.

### 2.3.1c Directly Contacted Diode

The directly contacted diode which has minimal parasitics, and is in reality, packageless is shown in Figure 15. This configuration employs a 2 mil gold ball bonded on the top of a diode chip. Contact to the diode is made with the bias post or other circuit element directly onto the gold ball. This package suffers from mechanical instability, particularly during temperature cycling, but was used with some success during the early part of the program, particularly in conjunction with the coplanar biased circuit development.

### 2.3.1d Quartz Ring Pedestal Package.

During this program, a low parasitic version of the standard Hughes quartz ring millimeter wave package was investigated for use in pulsed operation at 140 GHz. This package is shown schematically in Figure 16.

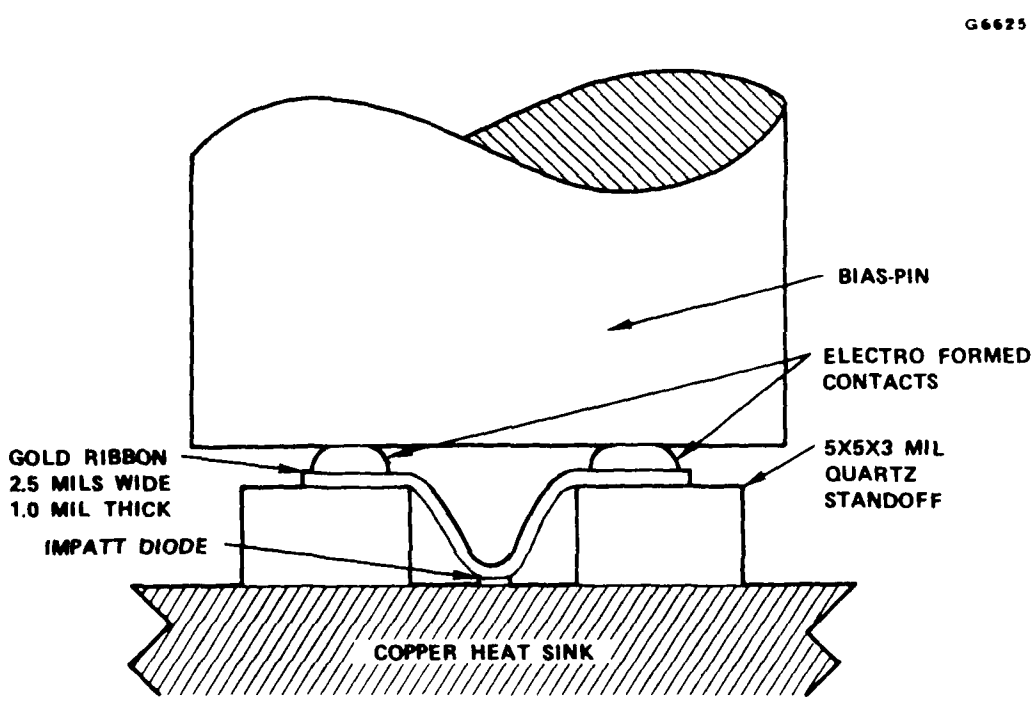



Figure 14 Double standoff package with bias pin shown in normal operating position.


Figure 15 Directly contacted diode with void ball.

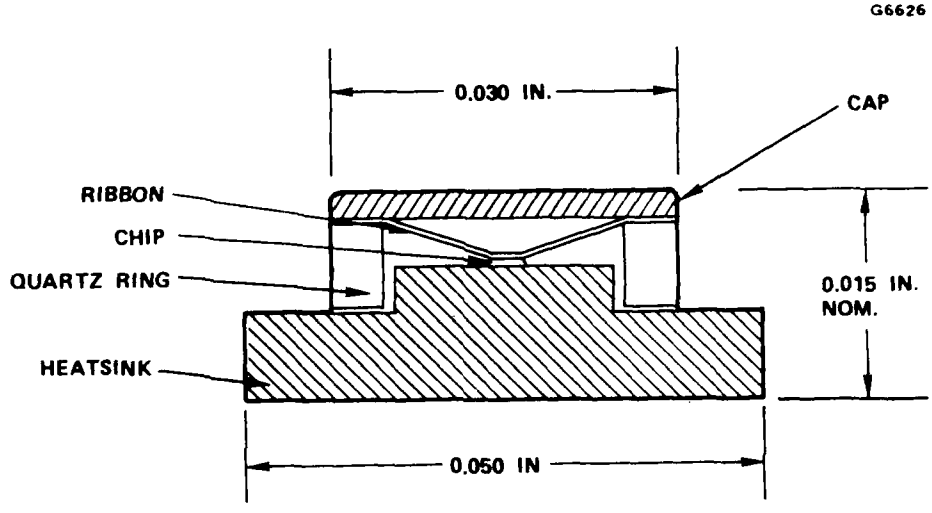



Figure 16 Low parasitic quartz ring pedestal package for pulsed 140 GHz operation.

In this package, the IMPATT diode is mounted on a pedestal so that the parasitic inductance of the connecting ribbon is less than in the absence of the pedestal, i.e., the normal production quartz ring package. The pedestal package is hermetically sealable and very rugged. During this program, significant difficulties were encountered in fabricating parts for the pedestal package, and in general, its rf performance was inferior to that of the double standoff packages. For these reasons, and because of the success of the double standoff package, the development of the pedestal package was curtailed during the latter months of the program.

## III. COMBINER CIRCUIT DEVELOPMENT

During the course of this program, several circuit approaches were investigated for IMPATT diode power combining at 140 GHz. These included: (1) a millimeter wave integrated circuit (MMIC) configuration coupling power from two or more devices into a resonant waveguide cavity: (2) the so called "coplanar based" waveguide power combiner, (3) a rectangular resonant waveguide combiner employing center mounted diodes, and (4) a rectangular resonant waveguide combiner employing wall mounted diodes. Only a limited amount of effort was devoted to the MMIC circuit development task and this only during the first two months of the program. The work during this period consisted largely of scaled circuit model measurements made at S- and X-band using a network analyser. This work was subsequently continued as part of a 60 GHz IMPATT diode combiner program.[6] No circuit measurments were made at 140 Ghz. This MMIC work is not described further in this report, for further details reference (6) may be consulted. In the remainder of this section, the two versions of the rectangular waveguide cavity resonator and the coplanar biased circuit are discussed in detail.

Currently, the waveguide resonator combiner is the most well established approach to millimeter wave power combining. In general, this type of combiner may be implemented in different configurations of which the two principal forms are where:

1. IMPATT diodes are mounted in coaxial modules in the waveguide walls of the resonant cavity.

2. IMPATT diodes are mounted in the center of the waveguide resonator.

Two versions of the center mounted configurations were studied on this program. These were: (1) a reduced height waveguide resonator with bias to the individual diodes supplied by coaxial bias elements, extending through the broad waveguide wall (Figure 20), and (2) the "coplanar biased configuration which employs a disc resonator with a bias line extending through the narrow waveguide sidewall (Figure 21).

## 3.1 RECTANGULAR WAVEGUIDE RESONATOR WITH WALL MOUNTED DIODES

This type of resonator combiner was first developed by Kurokawa[7] in X-band frequencies; using twelve one-watt IMPATT diodes, over ten watts output power was achieved. The basic configuration is shown in Figure 17. Harp[8] later modified the Kurokawa combiner into a cylindrical resonator configuration and combined up to sixteen IMPATT diodes with 90% combining efficiency in X- and Ka-bands. Presently, the cylindrical resonator combiner has been widely accepted as a standard technique for combining power at frequencies from X- through Ka-band. However, it is less desirable as a power combiner at higher frequencies. This is because of moding problems and difficulties with coupling from the cylindrical cavity resonator to a waveguide output circuit.

The Kurokawa combiner using a rectangular waveguide resonator is better suited for power combining at 140 GHz. The reason is that in a rectangular cavity, there are three independent eigenvalues related to the three independent coordinates x, y, and z. A high degree of freedom in controlling the number of modes in the resonator can thus be achieved. In general, the mode density must be kept small to avoid moding problems. In order to keep the mode density small, ideally a fundamental mode resonator should be used. However, a fundamental mode resonator is too small at 140 GHz for combining a sufficient number of diodes to achieve high power. A compromise is therefore required in the resonator design to minimize the number of modes near the operating frequency and to maximize certain physical dimensions for optimum diode placement.

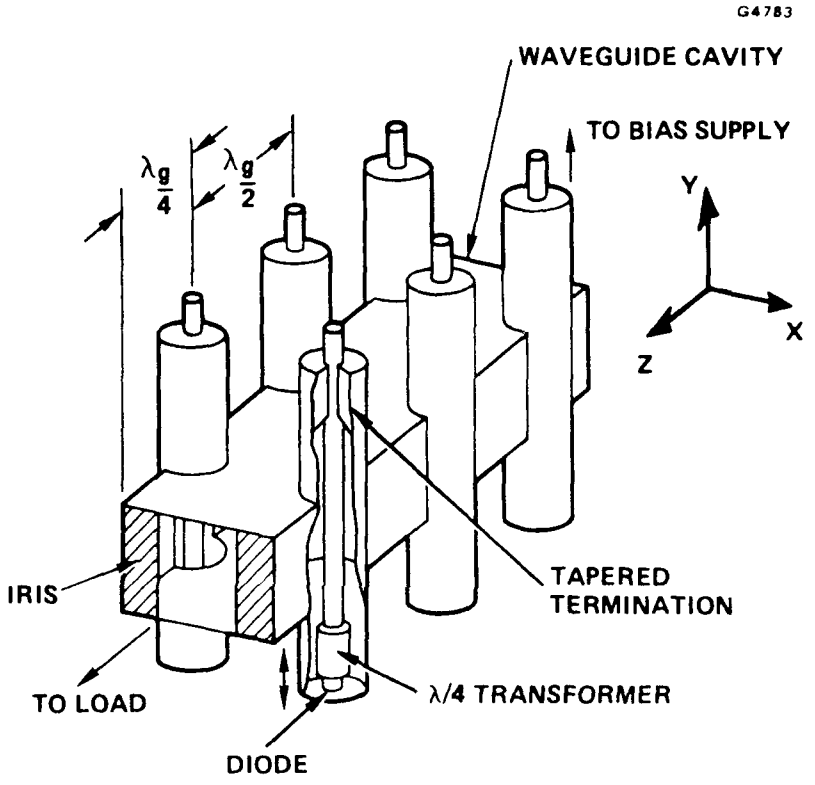



Figure 17 Power combiner using coaxial modules in a waveguide resonator.

The general approach is to place pairs of diodes in the resonator cavity either $\lambda g/2$ or $\lambda g$ apart, where $\lambda g$ is the guide waveguide. At 140 GHz, it becomes exceedingly inconvenient to space the two pairs of modules $\lambda g/2$ apart as in most lower frequency combiners. For this reason, combiners employing more than a single pair of diodes typically employ the $\lambda g$ spacing rather than the $\lambda g/2$ value.

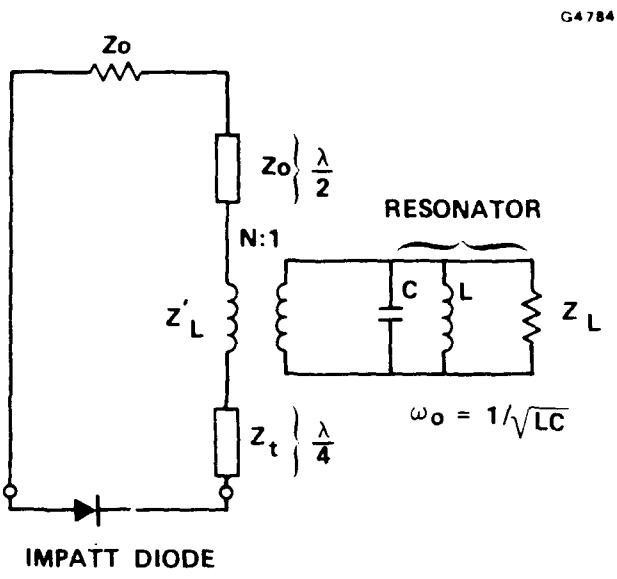
The equivalent circuit for a coaxial module cross-coupled to a waveguide resonator is shown in Figure 18. The resonator is simply represented by a tank LRC circuit and the coupling to the coaxial module by an N:1 transformer.

At resonance, the cavity conductance is low because the Q is high. Therefore a high load resistance $Z_L'$ is placed in series with the coaxial termination $Z_o$ by virtue of the coupling transformer. By properly selecting the quarter-wave transformer impedance $Z_t$, the low device negative resistance $Z_D$ ($\simeq 1 - 2$ ohms) is transformed to a higher value so as to exceed $Z_o + R_e(Z_L')$, a necessary condition for oscillation. The fraction of power being coupled to the resonator, or the coupling efficiency $\eta$, is given by

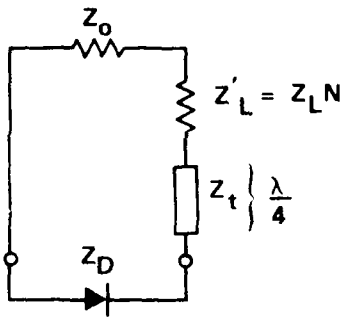
$$\eta = \frac{R_e\left(Z_L'\right)}{R_e\left(Z_L'\right) + Z_o} \qquad (3\text{-}1)$$

If the transformation ration N is high so that $R_e(Z_L') >> Z_o$, high coupling efficiency can be achieved.

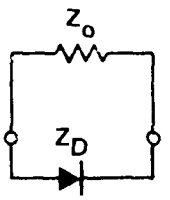
Off resonance, the cavity resistance is low and represents a short circuit. The equivalent circuit for this case is shown in Figure 18c. The quarter-wave transformer is no longer $\lambda/4$ so that the device impedance is no longer transformed to a higher impedance, and $Z_o >> Z_D$. Power from oscillations off resonance are now dissipated in the coaxial termination.




(A) GENERAL CIRCUIT




(B) AT RESONANCE




(C) OFF RESONANCE

Figure 18 Equivalent circuit for coaxially-coupled resonant power combiner.

This has the important effect of stabilizing all spurious oscillations to provide the single frequency characteristic which is essential for combiner operation.

It should be noted that the coupling between the coaxial module and the waveguide is predominantly through the magnetic field. The magnetic field is maximum just inside the waveguide side walls, and the direction is consistent with that of the magnetic field inside the coaxial modules. Because the diameter of the coaxial module is much smaller than the width of the waveguide* the module only intercepts a small fraction of the total magnetic field line inside the resonant cavity. This implies that each module is only weakly coupled to the resonator, and that the interaction between modules is negligible.

In this program, the sidewall configuration was successfully developed at 140 GHz for a single diode pair and this type of combiner circuit was delivered at the completion of the program.

At 140 GHz, because of the relatively small waveguide dimensions, the two diode sidewall combiner is difficult to realize mechanically. The cavity width was therefore enlarged from the standard 0.065" to 0.100" while the cavity height was maintained at 0.0325". The cavity output opening was directly connected to a standard WR-7 waveguide (0.065" x 0.0325") without the use of any tapered waveguide transition. The WR-7 waveguide opening serves as a natural inductive iris for the resonant cavity.

*The validity of this statement is somewhat limited at 140 GHz. In reality, the module diameter is about 1.2 mm while the waveguide width is only 1.65 mm. Therefore the coaxial module does intercept a significant portion of the total magnetic field line of the resonator. Nevertheless, because of our success with the Kurokawa combiner at 140 GHz, the approximate theory developed for lower frequencies does seem to be valid up to 140 GHz.

The two IMPATT diodes were located slightly away from the waveguide side walls. Tuning was achieved by a movable back short. Figure 19 is a schematic diagram of the resonant circuit configuration.

## 3.2 RECTANGULAR WAVEGUIDE POWER COMBINER - CENTER-MOUNTED DIODES

A different version of the rectangular waveguide power combiner is one in which the coaxial modules are located in the center of the waveguide cavity. Figure 20 shows this configuration. In this arrangement, the electric field of the resonator is maximum at the diode locations while the magnetic field is negligible. Thus, the coupling between the resonator and the coaxial modules is primarily achieved through the electric field.

As in all power combining schemes, the placement of an IMPATT diode in a strong field region of the resonator results in optimum power transfer. However, if the coaxial module is centrally located, the bias post, by virtue of geometry, intercepts an entire electric field line that starts from the bottom and ends at the top of the waveguide cavity. This means that the coupling between the resonator and each diode module is strong. As a consequence, the interaction among modules is strong and results in little isolation between devices.

During this program, we have investigated several versions of this circuit with generally dissappointing results. Experiments were carried out by combining two IMPATT diodes (Figure 20). In all cases, it was found that the diode closer to the load causes significant rf degradation to the diode near the back short, and in general coherent oscillation was difficult to achieve. This can be explained on the basis of lack of isolation between diodes. This unfavorable aspect is probably the major reason why this type of combiner has performed with such limited success. During the last few months of the program, an effort on this circuit was terminated in favor of the side-mounted diode version (Section 3.1).

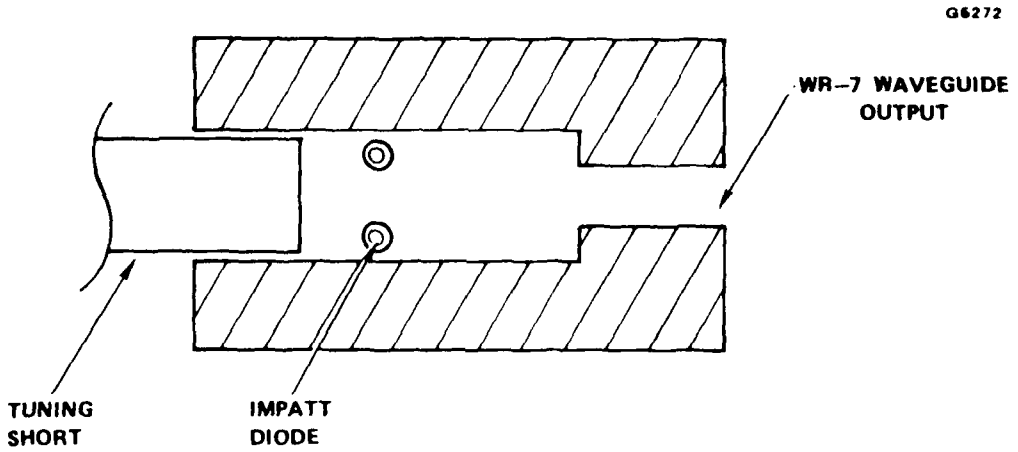



Figure 19 Resonant circuit configuration.

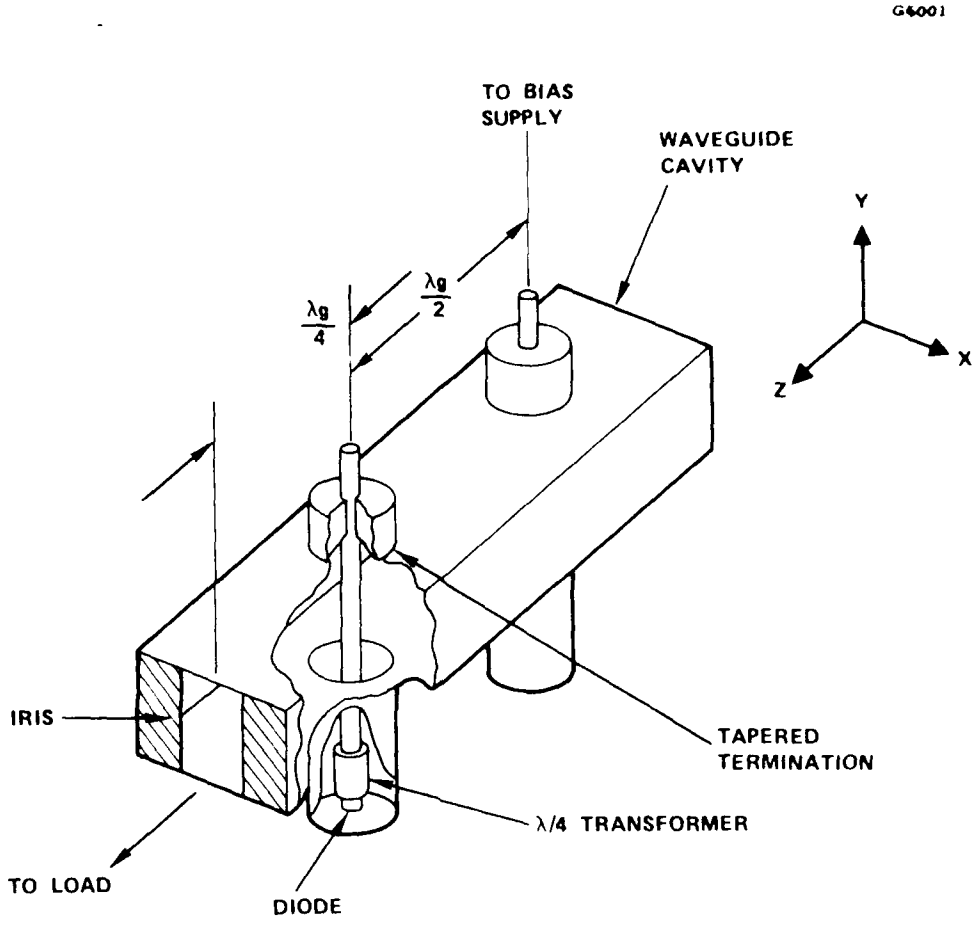



Figure 20 Power combining using coaxial modules mounted in the center of a waveguide.

## 3.3 COPLANAR BIASED WAVEGUIDE POWER COMBINER - CENTER-MOUNTED DIODES

Early in this program we investigated another configuration to combine IMPATT diodes in a rectangular waveguide cavity. This is the so-called coplanar biased scheme shown in Figure 21 for a single diode. This diode is mounted in a slot of a block of metal and is contacted by a wire extending into the slot from the side wall of the slot. The wire is coated with a very thin layer of insulator. In order to provide the transformation required to match the relatively high circuit impedance to the relatively low device impedance, a resonant cap is soldered to the end of the wire above the diode. The other end of the wire is then soldered to a bias circuit board. A second metal block is used to cover the slot of the block thus forming the waveguide. Several diodes can be mounted this way in the same block. Figure 22 is a photograph of a four-diode coplanar biased circuit, and Figure 23 is a scanning electron micrograph of the bias wire-resonart cap arrangment. The diodes are spaced 1.40 mm apart ($\lambda_{g/2}$) for optimum rf power output at 140 GHz. Figure 24 shows the four-diode combiner circuit assembled with an output isolator.

Initially, single diodes were evaluated for rf performance in this circuit. A peak power of 815 mW with a frequency chirp of 129.4-131.9 GHz was achieved. When two diodes having similar zero-biased junction capacitances (1.6 pf and 1.7 pf, respectively) were tested in the same circuit, a peak power of only 847 mW with a frequency chirp of 128.8-130.2 GHz was achieved. When operated individually over the same frequency range, the 1.7 pf diode had an ouput power of 525 mW and the 1.6 pf diode had an output power of 350 mW. Finally, when four diodes were tested in this cavity, a peak output power of 1086 mW with a frequency chirp of 127.8-130.0 GHz over an RF pulse of 80 nanoseconds was achieved when only two of the four diodes are turned on. The output frequency chirp of the other two diodes was quite different in nature and was not contributing to the output power when all four diodes were turned on.

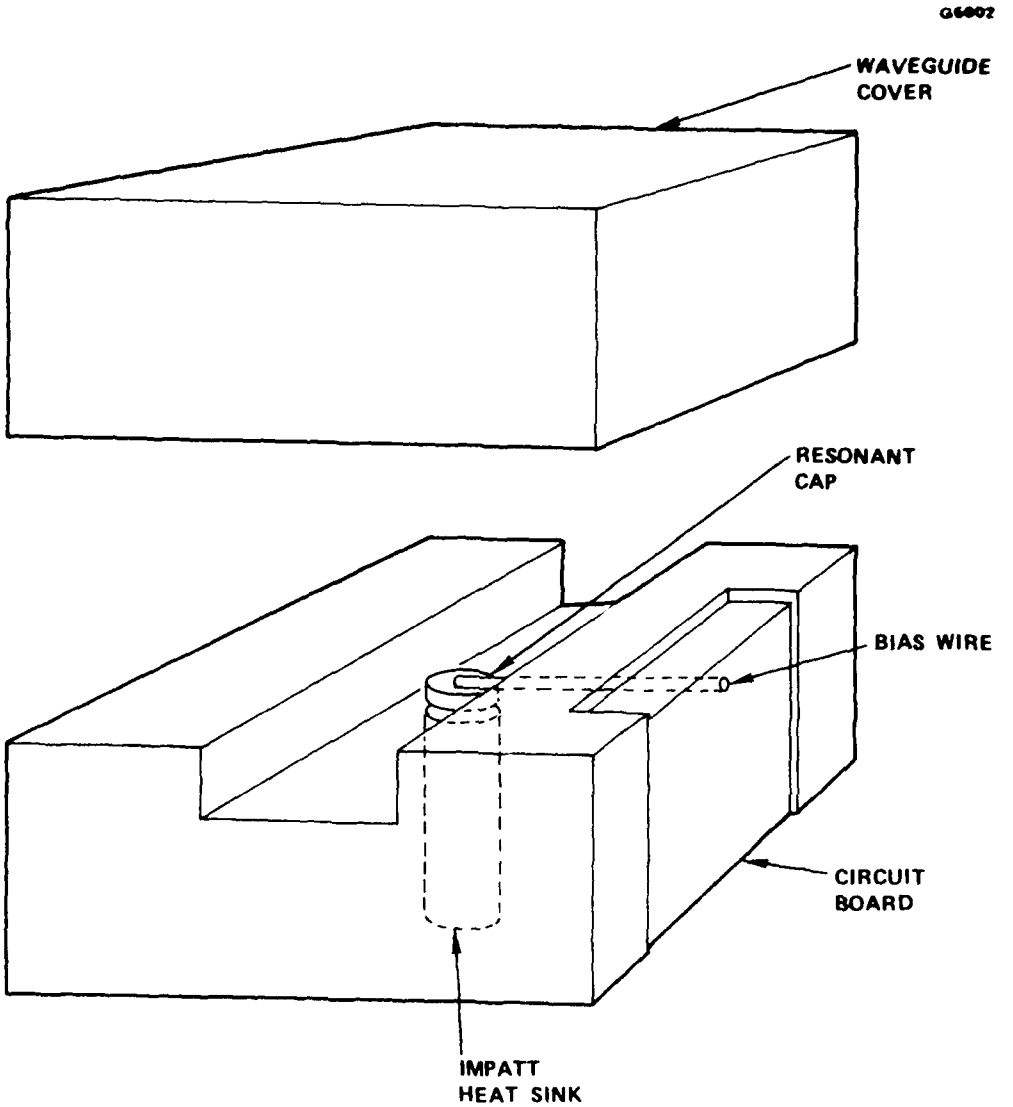



Figure 21 Coplanar biased circuit design.

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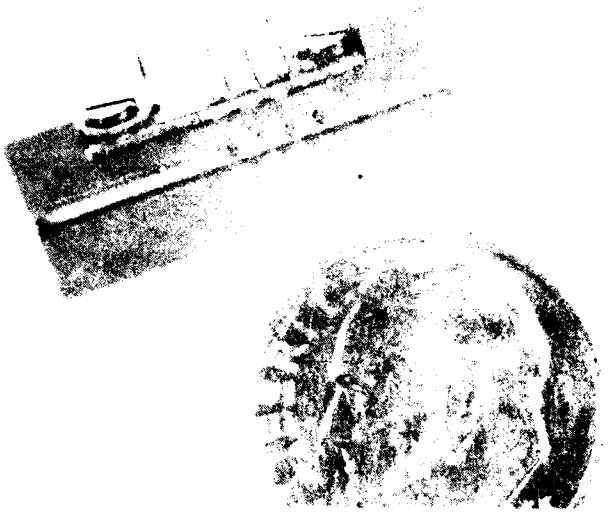

Figure 22 Four-diode combiner circuit using coplanar biased scheme designed for 140 GHz operation.

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Figure 23 Scanning electron micrograph of the four-diode combiner showing the bias wires and resonant caps.

E2087

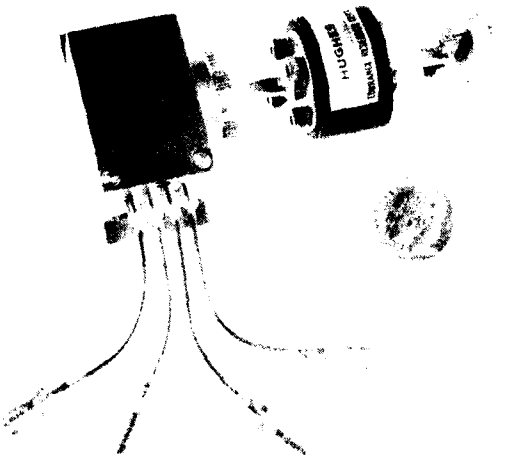


Figure 24 140 GHz four-diode combiner circuit assembled with an output isolator.

One of the difficulties with this scheme is the absence of a damping mechanism for spurious oscillations. Unlike a coaxial module, the diodes are contacted by a cap via an insulated wire which passes through the metal side wall. The bias wire is simply a low-pass filter with a predominantly reactive component. This means that any spurious oscillations outside of resonance (assuming that the resonant cavity has a set of well-defined resonance frequencies) will not be totally suppressed but will be reflected back, resulting in low combining efficiency. Furthermore, because the bias wires and resonant caps (Figure 21) mechanically occupy a sizable volume of the cavity, the resonance characteristics of the cavity is not well-defined and the loaded Q may be quite low. This means that the line widths will be broad and some modes will overlap. This will again result in a reduction of combining efficiency. In reality, the resonant cap structure is a more well-defined resonator than the cavity itself. Thus, in the absence of a well-defined common resonator, any coherent oscillation between two or more diodes is probably more of an injection-locking nature rather than power combining. This is probability why test results with this current have not been more successful. Effort on this circuit, like the other center-mounted configurations was suspended in favor of the combiner employing side-mounted diodes.

# IV PULSED DIODE AND COMBINER CHARACTERIZATION AND PERFORMANCE

Characterization of devices operated in the pulsed mode is complicated by the fact that the electrical and thermal parameters of interest vary with time over the applied pulse width. Most testing during the program was carried out at pulse widths between 50 and 150 nsec. The pulse repetition frequency (PRF) was normally set at 50 kHz. In general, moderate (20%) excursions from this value had little effect on the parameters measured during the pulse application. This result is consistent with the negligible effect of PRF changes in this range on the transient thermal resistance as calculated in Section 2.1.2.

## 4.1 THERMAL CHARACTERIZATION

Steady-state thermal resistance was measured on pulsed diodes as a means of evaluation. However, a more meaningful parameter for pulsed applications is the transient thermal resistance $\theta_T$ defined in Section 2.1.2 which is related to the junction temperature rise $\Delta T_j$ at the end of the applied bias pulse. An estimate of $\Delta T_j$ can be obtained by observing the voltage rise across the pulse. Since the bias current is not strictly constant over the applied pulse, the voltage change is not entirely due to heating. However, it can at least be used to give an indication of the temperature rise. As an example, diodes from a particular lot of diodes were measured to have a voltage coefficient of reverse breakdown voltage of 0.0123 V/$^{o}$C. Thus if the voltage rise across a "flat" current pulse is say 3 V, the temperature rise across the pulse is estimated to be

$$T = \frac{3.0}{0.0123} = 244^{o}C \quad .$$

## 4.2 SINGLE DIODE RF CHARACTERIZATION

A discussion of pulsed oscillator RF characteristics including output power, efficiency, frequency and frequency chirp is given in this section.

### 4.2.1 Measurement Setup

Power measurements were made using a dry calorimeter (Hitachi model E39C4) which, in spite of its slow response time, is much less frequency sensitive than a thermistor mount. The calorimeter sensitivity was found to be 60.9 V/mW at 60 GHz. Since the calorimeter has a relatively flat frequency response, this sensitivity was assumed to be valid at 140 GHz. This assumption constitutes a conservative measurement in power because it is likely that the sensitivity may decrease at high frequencies.

Frequency detection and measurement were made by a point contact detector and frequency meter respectively. An oscilloscope display of the detected output pulse in conjunction with the wavemeter was used to determine the frequency chirp characteristics across the pulse. A low loss isolator was used with the IMPATT oscillator to provide 20 dB of isolation. Further isolation was obtained by an attenuator which was placed between the isolator and the frequency meter.

### 4.2.2 Diode Lot Evaluation

A total of 38 diode lots were fabricated during the program. Of these, many had incorrect doping profiles, based on the design values presented in Section 2.1. RF results from some of these lots are presented in Tables 3 through 5. Table 3 shows comparative data for the three best lots fabricated. Of these, lots DD21 and DD54 were the best and individual diodes from both of these lots were able to produce more than

TABLE 3

PULSED 140 GHz DIODE EVALUATION RESULTS

| Lot No. | Zero Bias Capacitance (pF) | Breakdown Voltage (V) | $f_o$ (GHz) | $f_1$ (GHz) | Peak Power (W) | Pulse Length (nsec) |
|---|---|---|---|---|---|---|
| DDD 23 | 2.13 | 9.8V | 130 | 126 | 0.772 | 50 |
| DDD 21 | 1.7 | 10.2 | 128 | 131 | 1.90 | 100 |
| DDD 21 | 2.8 | 10.1 | 128 | 131 | 2.2 | 100 |
| DDD 54 | 2.15 | 9.6 | 136.2 | 143.0 | 3.08 | 60 |

TABLE 4

RF TEST RESULTS FOR DIODES FROM LOT DDD 21

| Capacitance Range (pf) | Number of Devices Tested | Best Peak Power Results (Watts) | Frequency (GHz) |
|---|---|---|---|
| 1.6 - 1.7 | 4 | 1.9 from 1 device | 128 - 131 |
| 2.5 - 3.0 | 4 | 2.2 from 2 different devices | same |

All tests performed at 100 nsec pulse length and 50 KHz pulse reputation frequency.

TABLE 5

RF TEST RESULTS FOR DIODES FROM LOT DDV 54

| Diode | Capacitance, pf | Peak current, A | Peak output power, W | Pulse width, ns | Frequency, GHz |
|---|---|---|---|---|---|
| # 4 | 2.12 | 6.0 | 2.73 | 70 | 136.1 - 142.7 |
| # 5 | 2.29 | 7.0 | 2.60 | 60 | 135.7 - 142.8 |
| #12 | 2.15 | 7.0 | 3.08 | 60 | 136.2 - 143.0 |

2.0 watts of peak power over pulse lengths of up to 100 nsec. Table 4 shows test data from 8 diodes from lot DDD21 and also indicates the effects of varying diode area. Table 5 illustrates the performance from the diodes from lot DDD-54. In this case, note the almost identical rf performance from the 3 diodes tested.

Note that the best performing lots had doping densities ($N_D = N_A = 3\text{-}4 \times 10^{17}$ $cm^{-3}$) and breakdown voltages ($V_b$ = 9-10 V) in good agreement with the design values of Section 2.1.

All diodes were individually tested for output power and frequency response in a standard single diode waveguide cavity circuit. This circuit is shown schematically in Figure 25.

The test circuit consists of a 0.010 reduced height waveguide cavity with a tapered waveguide height transition to the WR-7 waveguide output. Tuning was achieved by a sliding back short. A relatively large bias pin with diameter between 0.027" and 0.035" was used in the cavity. A bias pin of this size inside a 0.100" wide reduced height waveguide can no longer be regarded as a thin inductive post, but rather a close approximation to a step transformer whose lower face provides additional impedance transformation between the IMPATT diode and the reduced height waveguide load.

For the single diode characterization, all rf measurements were made using a pulse repetition frequency of 50 KHz. The width of the input current pulse was adjustable between 80 ns and 130 ns. Many diodes with different junction capacitances were tested, and the optimum capacitance which yielded the highest output power and the best rf tuning characteristics was found to be between 2.0 pf and 2.5 pf. Figure 26 shows a typical input current pulse (top trace) and the corresponding rf video pulse (bottom trace) for one of the high power diodes. The peak power was 3.0W and the rf pulse width was 100 ns. The frequency

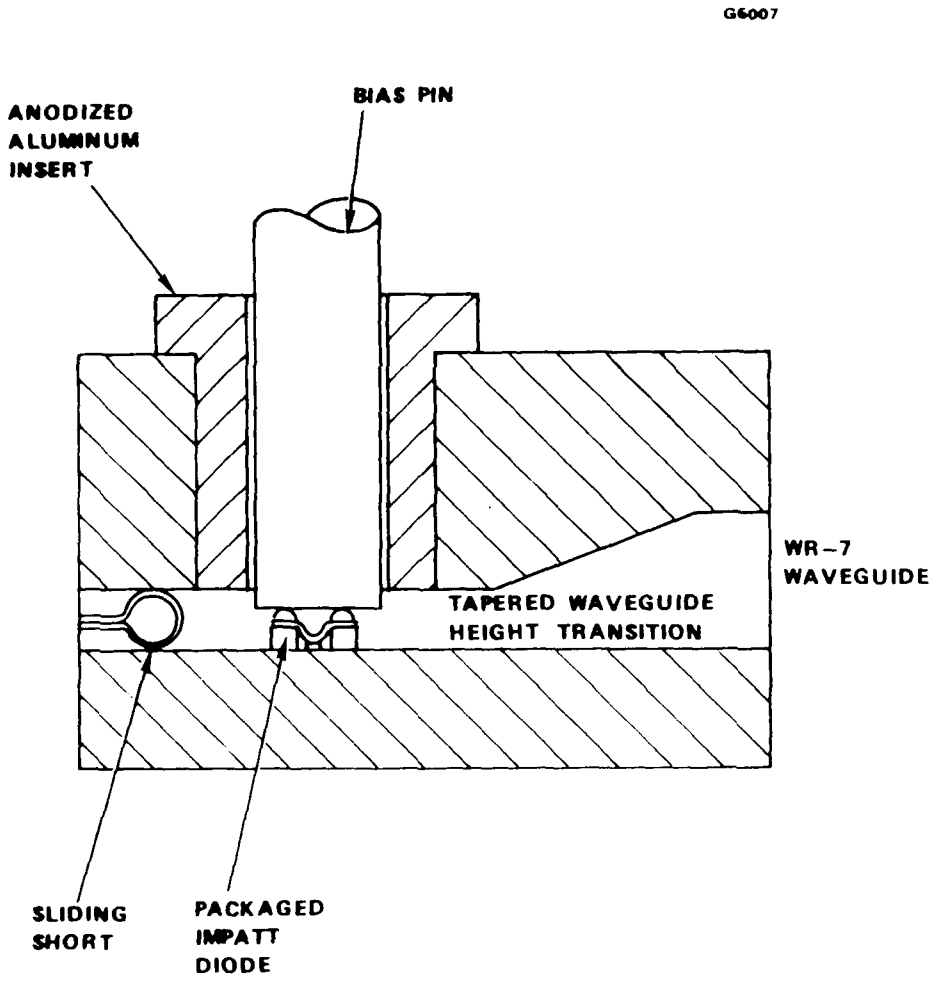


Figure 25 Bias-pin transformer waveguide circuit configuration.

E-2314

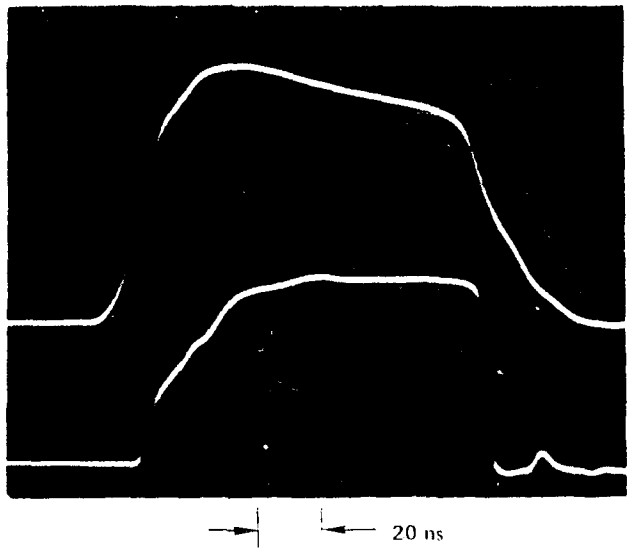


Figure [illegible] A typical input current pulse (top trace) and video output pulse (bottom trace) for a high power 1.0 GHz pulsed oscillator.

chirp caused by transient thermal heating of the diode was from 139.0 GHz to 142.0 GHz. The conversion efficiency was 2.8%. Figure 27 summarizes the performance of a high power 140 GHz diode from lot DDD54. Shown are output power, frequency and efficiency as a function of pulse bias current.

Based on these results, nearly all of the combiner development work carried out during the latter months of the program, and including the deliverable hardware, made use of diodes from Lot DDD 54. All of these diodes were packaged in the double standoff configuration described in Section 2.3.

## 4.3 TWO DIODE COMBINER CHARACTERIZATION

As discussed in Section 3.1, the basis for the final two diode combiner was the enlarged Kurakawa circuit with the diodes mounted near the sidewalls. This configuration is shown in Figure 19.

Prior to testing in the combiner, the diodes were individually tested for output power and frequency response in the standard single diode circuit (Figure 25). Following is data for the diodes (Lot DDD 54) which were delivered with the combiner circuit. Diode C-3 produced 1.0 watt of peak power with a frequency chirp due to transient thermal heating of 143 to 144.5 GHz. Diode B-8 generated 2.5 watts of peak power with a frequency chirp from 145.0 to 146.0 GHz. They were then mounted inside the resonator cavity and each was driven by a separate pulse modulator. When both diodes were turned on at the same time and tuned for maximum output power, a combined output of 3.0 watts peak power was obtained. This implies that the combining efficiency was approximately to 90%. Figure 28(a) and 28(b) show the video rf output pulses (bottom traces) for diodes DDD54C-3 and DDD54B-8, respectively, together with their corresponding input current pulses (top traces). Figure 28(c) shows the combined rf output (bottom trace) when both diodes were turned

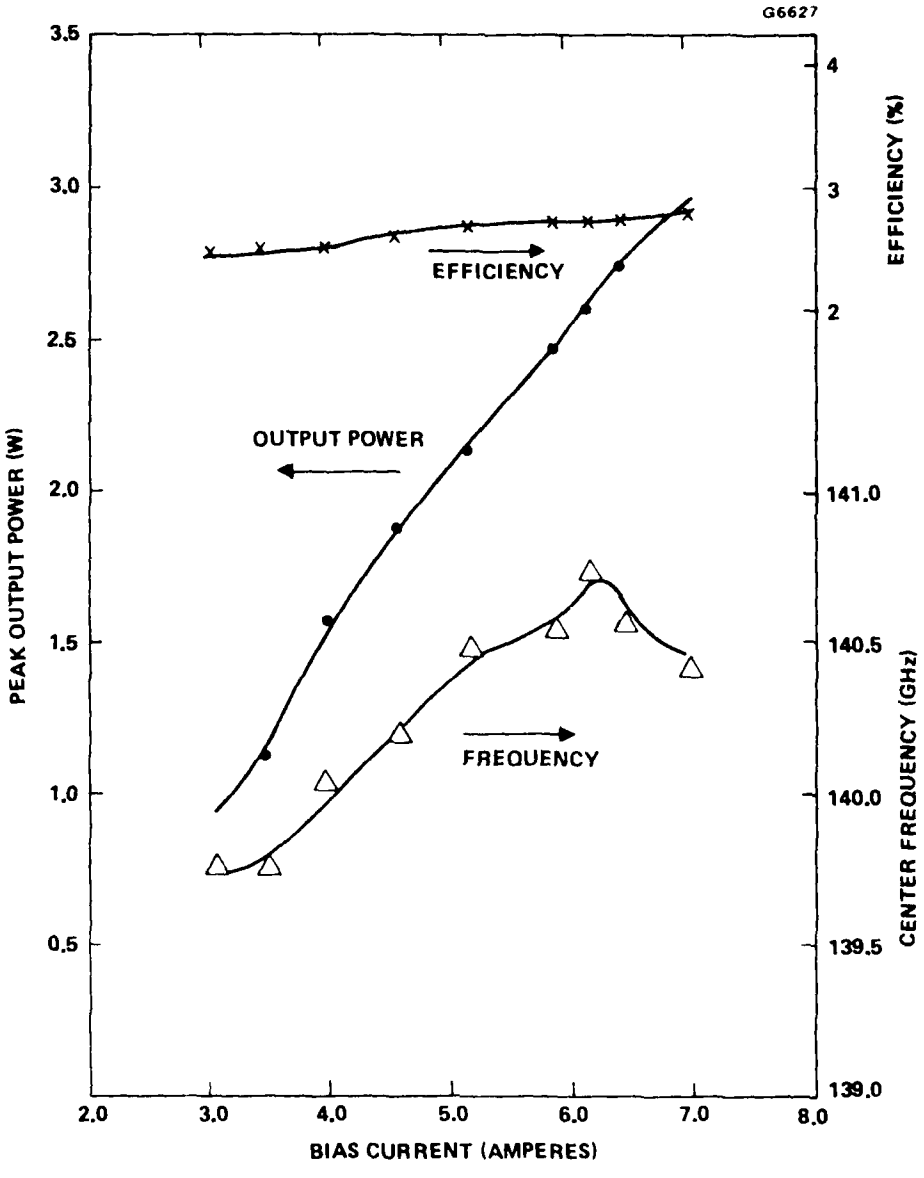


Figure 27 Operating characteristics of a high power pulsed diode from lot DDD54.

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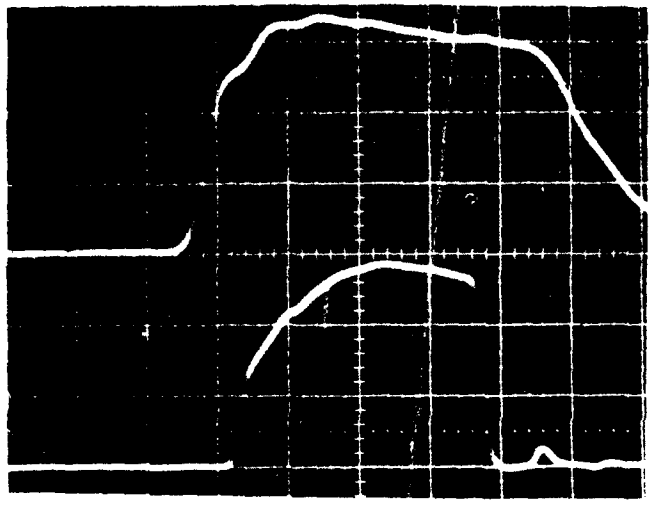

Figure 28(a) Video outputs of input current pulse (top) and rf output pulse (bottom) for diode DDD54C-3.

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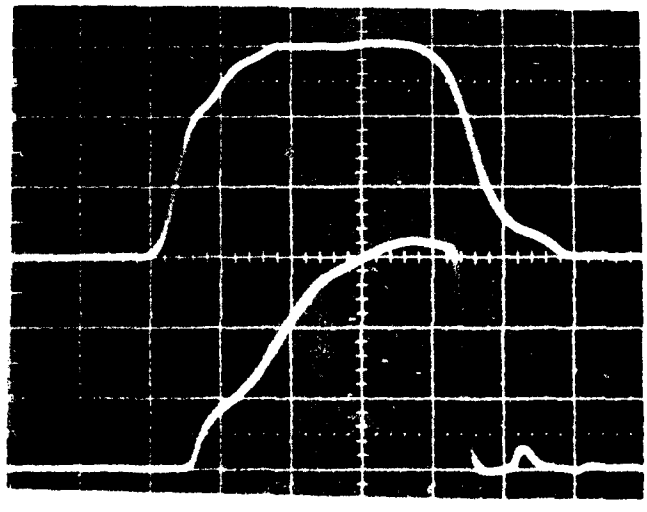

Figure 28(b) Video outputs of input current pulse (top) and rf output pulse (bottom) for diode [illegible].

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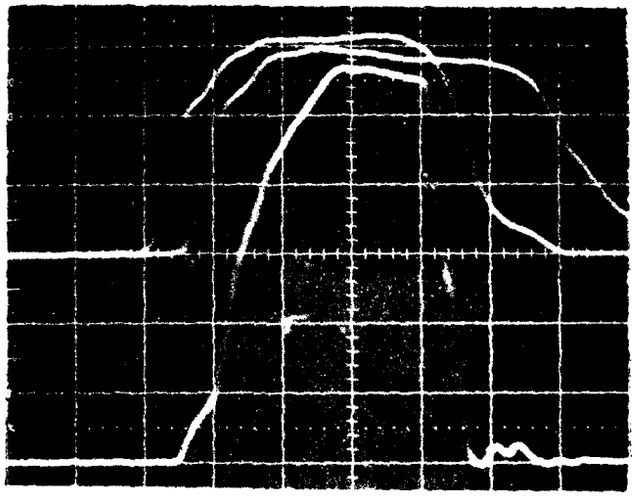

Figure 28(c) Video outputs of input current pulses (top two traces) and rf output pulse (bottom) when both diodes DDD54C-3 and DDD54B-8 were turned on.

on. The current pulses (top two traces) for both diodes are also displayed for comparison. The frequency response of the combined r pulse extended from 144.5 to 145.5 GHz and was clean and sharp throughout 90% of the pulse width, indicating true power combining.

A second circuit identical to the first one was constructed and two more diodes were tested. In this case the center frequency was reduced to 141.0 HHz, but the combined power was only 2.7 watts.

## V PERFORMANCE OF DELIVERED UNITS

At the conclusion of the technical effort, and upon mutual agreement with the Army, the following items were delivered:

1. One single-diode 3.0 watt IMPATT diode oscillator operating at 140 GHz (Figure 29).

2. One single-diode pulse modulator* with bias box and bias cable (Figures 30 and 31).

3. One two-diode 3.0 watt IMPATT oscillator (Figure 32).

4. One two-diode pulse modulator* with bias boxes and bias cables (Figures 33 and 34).

5. One D-Band isolator TRG model D112.

The detailed performance data for the single diode oscillator is summarized in Figures 26 and 27.

The specifications for the single diode oscillator are given below:

| | |
|---|---|
| Peak power out of intermediate waveguide | 2.9 W |
| Peak power out of isolator | 2.2 W |
| Center frequency | 140.0 GHz |
| Frequency chirp | 139.1-141.0 GHz |
| Pulse width | 85 ns |
| Flatness within pulse | 1 dB |

*The modulators are very similar to standard Hughes commercial units. Modulator development was not a part of this program.

E2318

Figure 29 Pulsed 3.0 watt 140 GHz IMPATT oscillator with isolator.

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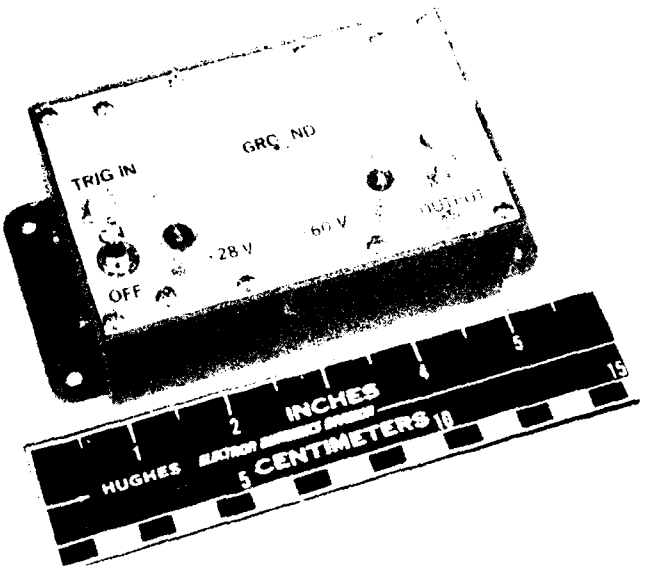


Figure 30 Single-diode pulse modulator.

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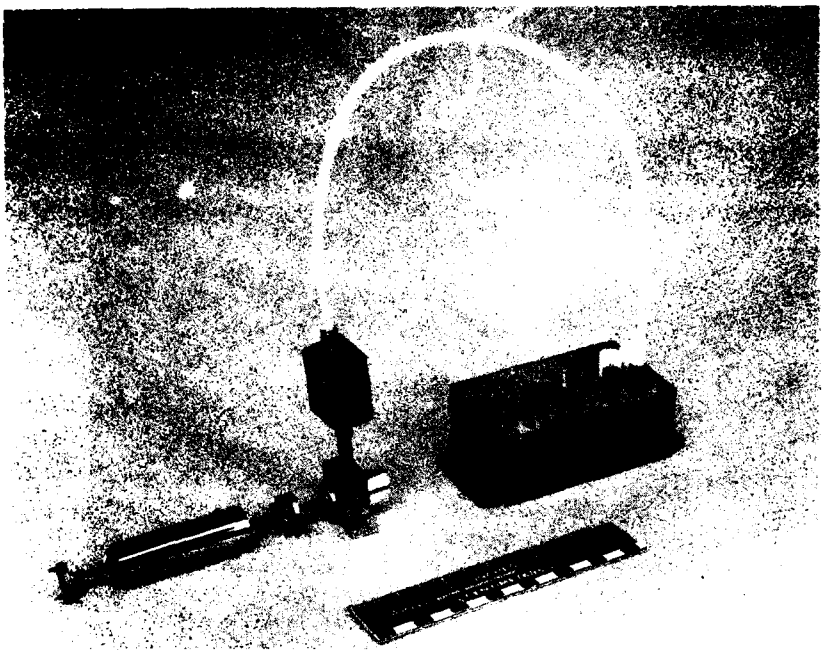

Figure 31 Single diode oscillator and pulse modulator.

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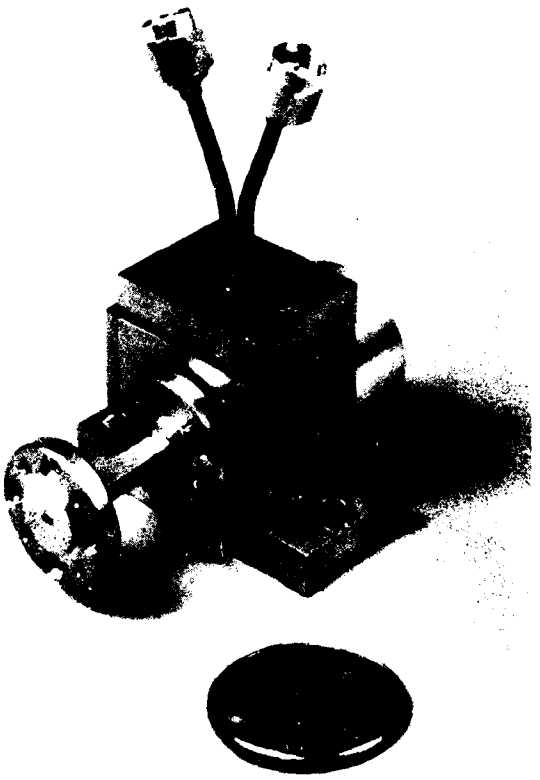

Figure 32 145 GHz Two-diode combiner.

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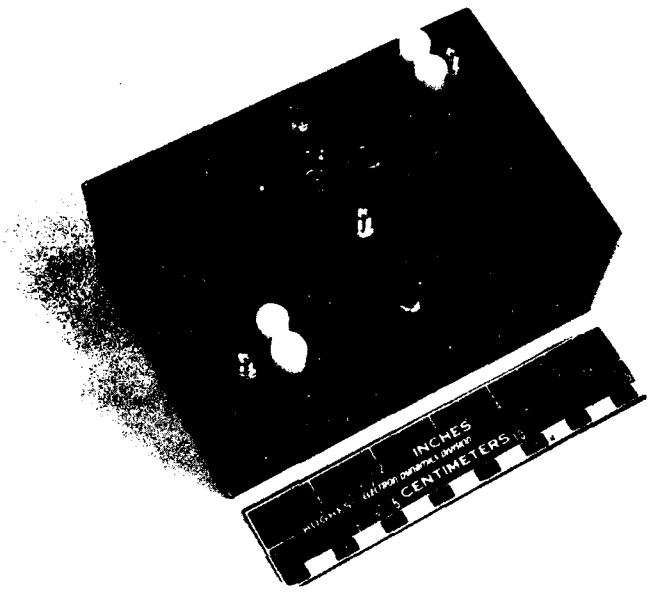


Figure 33 Two-diode pulse modulator.

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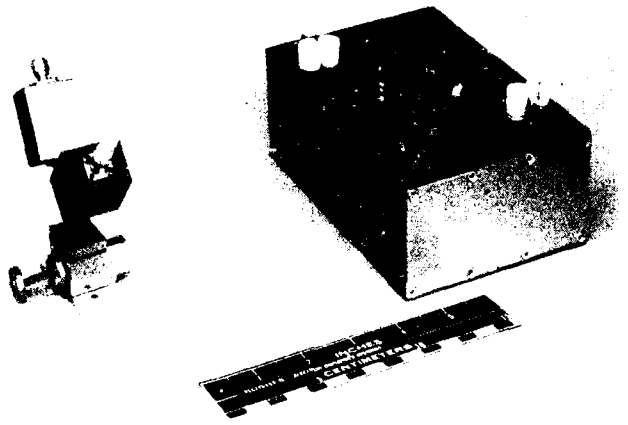

Figure 5. [illegible] developed [illegible] operation.

The operating characteristics of the two diode oscillator/combiner are described in Section 4.3. The specifications for this unit are as follows:

| | |
|---|---|
| Peak output power | 2.8W |
| Center frequency | 145.5 GHz |
| Frequency chirp | 145.0 - 146.0 GHz |
| Pulse width | 80 ns |

Complete operating instructions for the single and two-diode oscillators are provided in Appendix A.

## VI. CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

Significant advances in the state-of-the-art for pulsed millimeter wave diodes and oscillators operating near 140 GHz have been achieved as a result of the work described in this report. Specific accomplishments include:

1. The design and fabrication of silicon double drift IMPATT diodes capable of peak output powers of over 3 watts at 140 GHz. The best single device result prior to this program was about 800 mW of peak power.

2. The first time demonstration of efficient power combining from two pulsed IMPATT diodes at 140 Ghz.

3. The establishment of a basic resonant waveguide circuit configuration suitable for power combining from millimeter wave IMPATT diodes.

4. The employment of a nonhermetic, but rugged double quartz standoff package with appropriate parasitics for matching power from high power pulsed diodes to variety of waveguide circuits.

5. The delivery to the Army of two high power pulsed IMPATT oscillators. Both of these oscillators meet the program objective of 3.0 watts of output power, one from a single diode, the other from a two-diode power combiner.

It seems probable that additional work on the diode, package and oscillator circuit will lead to relatively modest improvements in single diode oscillator performance. With this program, the groundwork has been laid for further power combiner development work at 140 GHz. The

oversize Kurokowa circuit should provide the basis for combining power from additional pairs of side-wall mounted diodes, for example 4 or 6 diodes. More recent experience with this circuit at lower frequencies specifically at 60 and 94 GHz suggest that further progress with this circuit is probably limited these numbers of diodes. The requirement for additional power would then require higher level circuit combining of two or more Kurakowa modules perhaps with hybrid couplers.

This situation suggests that fundamentally new approaches to millimeter wave diode power combining are required, particularly at frequencies above 100 GHz. A very promising approach is to employ quasi optical techniques in conjunction with an open resonator combiner. This approach is currently being pursued at Hughes under U.S. Army Electronics Research and Development Command sponsorship. Another possibility which has not yet received any significant attention at 140 GHz is chip level combining. Work at lower frequencies (60 and 94 GHz) with series and parallel connections of diode chips however suggest this will be a difficult technology to implement at 140 GHz.

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# APPENDIX A

# OPERATION INSTRUCTIONS FOR THE 140 GHz SINGLE-DIODE IMPATT OSCILLATOR AND TWO-DIODE IMPATT COMBINER

WARNING

BEFORE ATTEMPTING TO OPERATE ANY ITEMS, PLEASE READ THE ATTACHED INSTRUCTIONS VERY CAREFULLY. FAILURE TO DO SO MAY RESULT IN UNNECESSARY OR IRREPARABLE DAMAGE TO THE IMPATT OSCILLATORS AND PULSE MODULATORS.

## LIST OF DELIVERED ITEMS

One single-diode IMPATT oscillator (Figure 29).

One single-diode pulse modulator with bias box and bias cable (Figures 30 aand 31).

One two-diode IMPATT oscillator (Figure 32).

One two-diode pulse modulator with bias boxes and bias cables, Hughes model (Figures 33 and 34).

One D-Band isolator, TRG model D112.

OPERATION INSTRUCTIONS FOR THE SINGLE-DIODE IMPATT OSCILLATOR

## 1. GENERAL DESCRIPTION

The single-diode IMPATT oscillator (Figure 29) consists of three sections: the oscillator cavity, the intermediate waveguide, and the isolator. Because of certain critical tuning elements, the oscillator cavity and the intermediate waveguide should always remain together as one unit. Under no circumstances should the two be separated.

The oscillator can be used with or without the isolator. Using the isolator will ensure that the proper r.f. output is obtained. If the isolator were not used, there is always the risk of having the oscillator being detuned by the external load.

The single-diode pulse modulator (Figure 30) has been tuned to give the IMPATT the best r.f. performance. No additional tuning is necessary. Figure A-1 shows a typical test setup for the single diode oscillator.

## 2. TO OPERATE THE IMPATT OSCILLATOR

1. Put the pulse modulator switch to OFF position.

2. Using a pulse generator with a 50 KHz PRF, a pulse width of approximately 0.2 μs, and a pulse height of approximately 2V, supply a continuous train of square pulses into TRIG IN.

3. Supply +60V and +28V as indicated making sure the GROUND is properly connected to all power supplies. The +28V terminal should draw about 70 mA.

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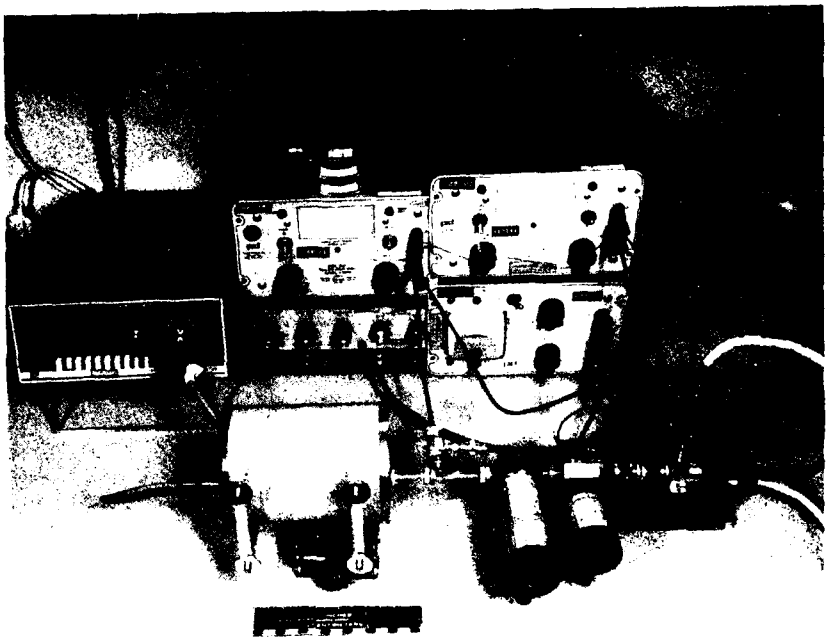

Figure A-1 Single diode oscillator test setup.

4. Connect the OUTPUT terminal to the IMPATT oscillator using the blue bias box marked with a letter "S" and any one of the three white bias cables. See Figure 31 for detail. Do not use the bias boxes marked "A" or "B".

5. To turn IMPATT on, simply put the pulse modulator switch to ON position. The +60V terminal should be drawing about 80 mA. Fig-ure 26 shows the current pulse and r.f. video output.

6. To turn IMPATT off, simply turn the pulse modulator switch to the OFF position.

CAUTION:

BEFORE DISCONNECTING IMPATT FROM THE PULSE MODULATOR, ALWAYS

a. Have pulse modulator switch in OFF position.
b. Turn off all power supplies.
c. Turn off pulse generator.

---

Specifications:

| | |
|---|---|
| Peak power out of intermediate waveguide | 2.9 W |
| Peak power out of isolator | 2.2 W |
| Center frequency | 140.0 GHz |
| Frequency chirp | 139.1-141.0 GHz |
| Pulse width of chirp | 85 ns |
| Flatness within chirp | < 1 dB |

OPERATION INSTRUCTIONS FOR THE TWO-DIODE IMPATT OSCILLATOR

## 1. GENERAL DESCRIPTION

The two-diode IMPATT oscillator (Figure 32) consists of the oscillator cavity and the output waveguide. The two should always remain as one unit. Furthermore, do not subject the oscillator to shock or vibration.

The oscillator is tuned to a center frequency of 145.5 GHz; as such it may not be usable in a 140 GHz system. However, since it is a power combiner, it may be used as a demonstration unit. To do so would only require a D-Band detector, frequency meter and attenuator.

The two-diode pulse modulator (Figure 33) has been tuned for maximum IMPATT performance. No further adjustments are necessary. Figure A-2 shows the two diode oscillator in a typical test setup.

## 2. TO OPERATE THE TWO-DIODE IMPATT OSCILLATOR

1. Put both pulse modulator switches to OFF position.

2. Using a pulse generator with a 50 KHz PRF, a pulse width of approximately 0.2 μs, and a pulse width of approximately 2V, supply a continuous train of square pulses into TRIG IN.

3. Supply +70V and +28V as indicated, making sure that the GROUND terminal is properly connected to all power supplies.

4. Using the blue bias box marked "A" and a white bias cable, connect output terminal A OUT to the IMPATT input terminal "A". Likewise, using the blue bias box marked "B" and another white bias cable, connect output terminal B OUT to the IMPATT input terminal "B". See Figure 34 for details.

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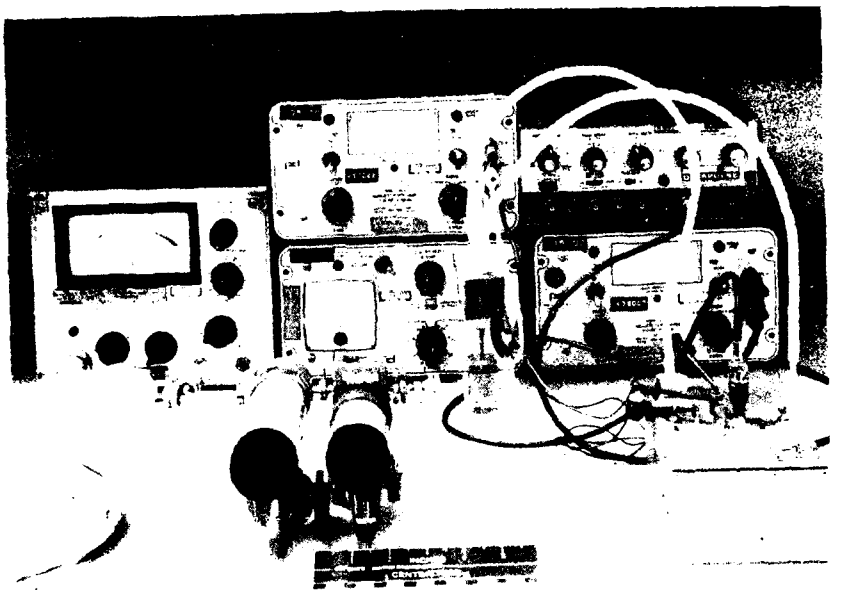

Fig. A-1. Test fixture oscillator test setup.

5. To turn on diode A (B), simply put pulse modulator switch A (B) to ON position. To turn on both diodes, simply put both switches to ON position. Use detector to observe the r.f. video output. Figures 28 a, b and c show the current pulses and r.f. video outputs for diode A, B and A + B, respectively.

   NOTE: If diode A is turned on alone, its optimum r.f. video output may not be observable because it occurs at a slightly different tuning short position.

6. To turn off diode(s), put the appropriate switches to the OFF position.

CAUTION:

BEFORE CONNECTING IMPATT FROM THE PULSE MODULATOR, ALWAYS

a. Have pulse modulator swithces in OFF position.
b. Turn off all power supplies.
c. Turn off pulse generator.

---

Specifications:

| | |
|---|---|
| Peak output pow | 2.8W |
| Center frequency | 145.5 GHz |
| Frequency chirp | 145.0 - 146.0 GHz |
| Pulse width | 80 ns |

AD-A083 450 HUGHES AIRCRAFT CO TORRANCE CALIF TORRANCE RESEARCH --ETC F/G 9/1
140 GHZ PULSED INPATT COMBINER HIGH POWER SOURCE.(U)
JAN 80 T T FONG, T A MIDFORD, E M NAKAJI DAAK11-77-C-0040
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