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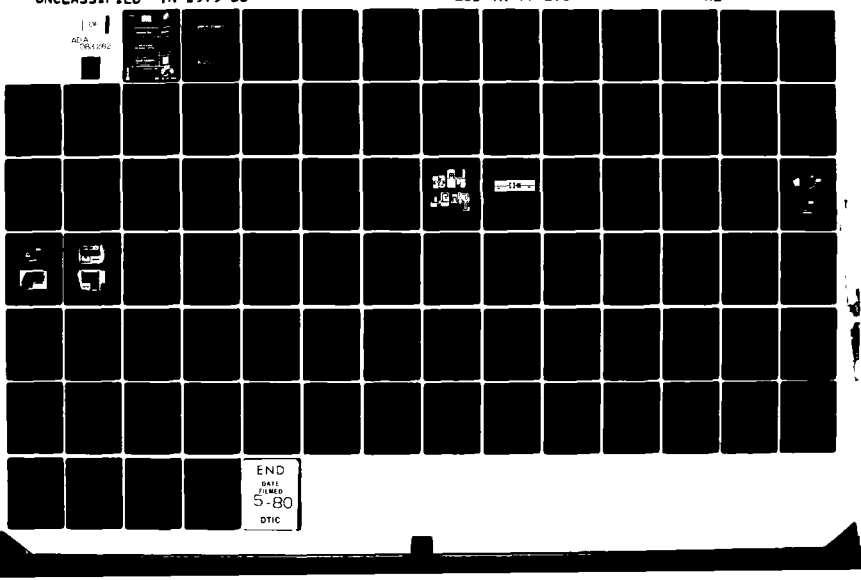

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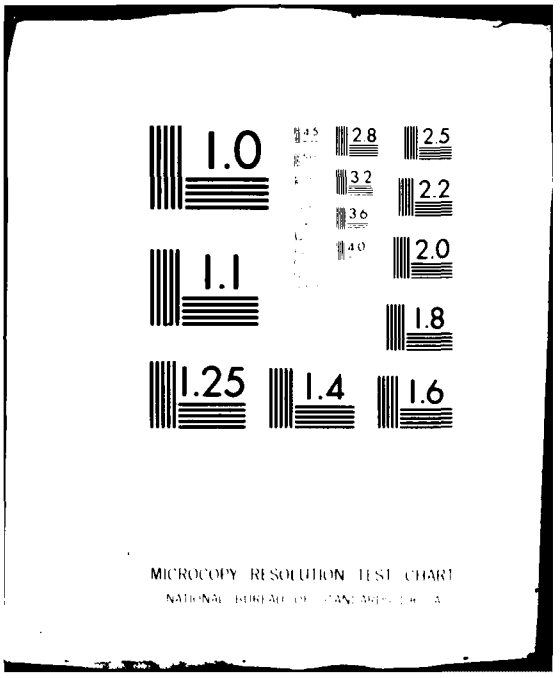
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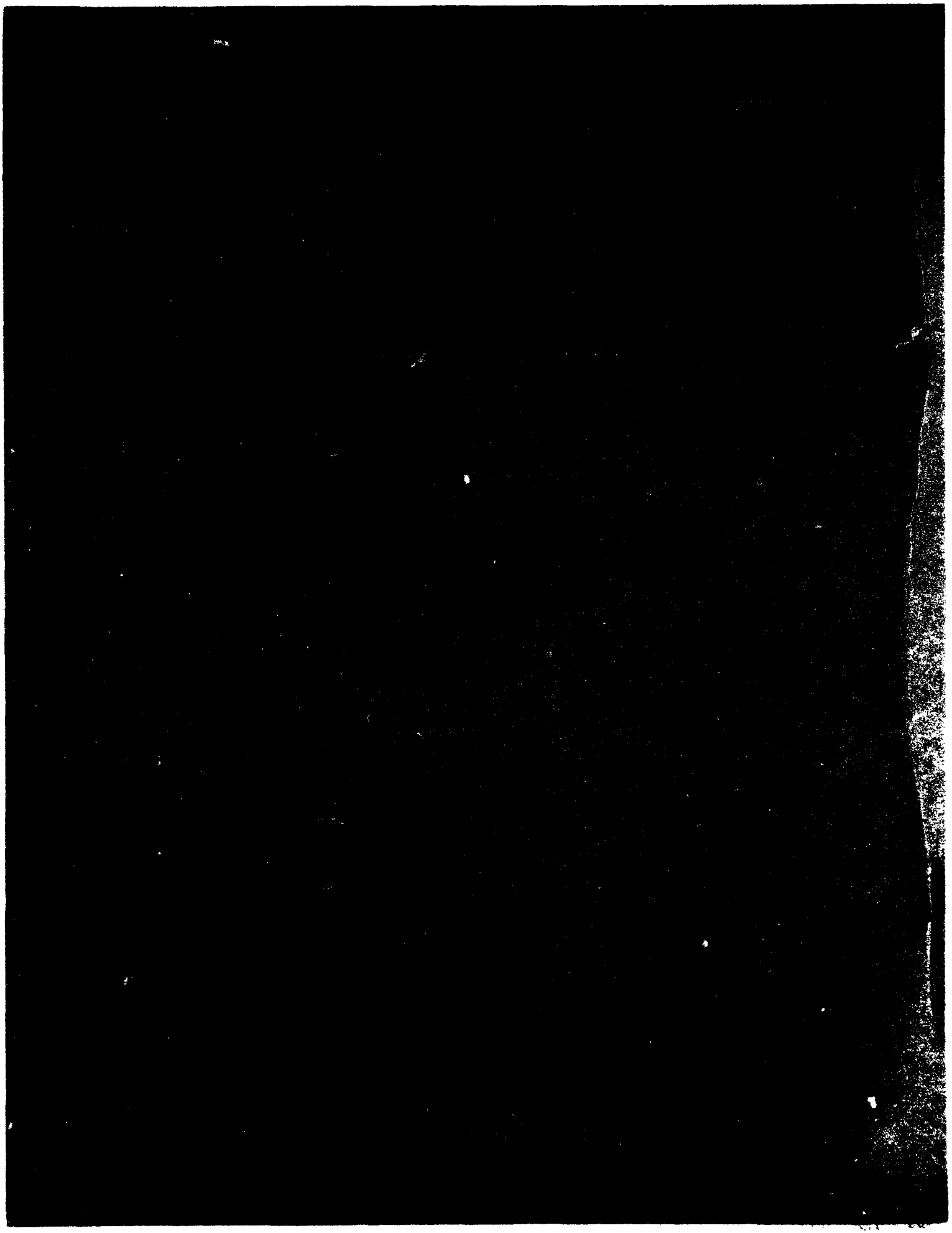


MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LINCOLN LABORATORY

A HIGH PERFORMANCE UHF SATELLITE TRANSMITTER

M. L. STEVENS

Group 63

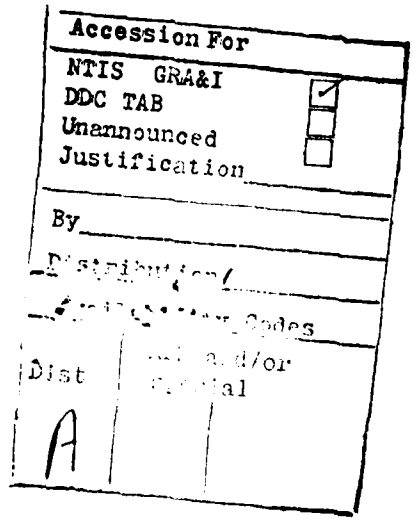
TECHNICAL NOTE 1979-68

28 NOVEMBER 1979

LEXINGTON MASSACHUSETTS

ABSTRACT

This note describes the design, construction, and performance of a 50 W UHF satellite transmitter which was built to demonstrate design and construction techniques that lead to easy replication of circuits in a manufacturing environment, without sacrifice in performance. High-efficiency performance is demonstrated over a 20 MHz band, centered at 260 MHz, with a fixed-tuned, single-ended design.



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I. PROGRAM GOALS

The goal of the UHF transmitter development program was to develop the design and construction techniques for high-power, high-efficiency amplifiers suitable for use in satellite transmitters operating in the military UHF satellite-communications band. The particular developments addressed in this study are:

1. Design and construction techniques that lead to easy replication of circuits in a manufacturing environment without sacrifice in performance, and

2. High-efficiency performance over the entire military UHF communication-satellite down-link band with a fixed-tuned single-ended design.

An earlier paper (Ref. 1) describes the techniques for designing high-power UHF amplifiers with collector efficiencies consistently over 78% at single frequencies. The purpose of this study is to extend this performance over a 20-MHz band centered at 260 MHz.

This note describes the design and construction of a UHF transmitter which was built to demonstrate the techniques which were developed in the course of this study.

The specifications for the UHF transmitter are:

Operational bandwidth:	250-270 MHz
Minimum output power:	50 W
Minimum collector efficiency of final amplifier $\frac{P_{out}}{\text{DC power to final}}$:	78%
Maximum RF drive required:	1 mW
Minimum overall efficiency $\frac{P_{OUT}}{\text{TOTAL } P_{in}, \text{ DC + RF}}$:	60%

Second harmonic output:	- 50 dBc*
Third harmonic output:	- 50 dBc*
Spurious output other than harmonic:	none

* dB referenced to the carrier at the rated power output

II. TRANSISTOR MEASUREMENTS

Before the transistors were chosen for this design, a sample quantity of many different types was tested as part of an initial screening.

The DC characteristics of each transistor are measured on a curve tracer and the data is kept on file. The curves for each transistor of a particular type are compared to see the device-to-device variations in DC performance. Small variations in DC performance have been found to be an indicator of good control in the device fabrication processes.

Device ruggedness is indicated by the ability of devices to withstand a measurement of the collector-base-junction reverse breakdown voltage at the reverse collector current specified by the manufacturer. Transistors which have a high failure rate in the reverse-breakdown test also exhibit high sensitivity to load mismatches and tend to have poor reliability.

Next, the collector-base-junction capacitance is measured as a function of voltage. This test is also an indicator of the manufacturer's control of the device fabrication.

The measurements just described indicate something about the device fabrication and reliability, but they indicate nothing about the RF performance. To determine the RF performance, the devices must be measured under actual operating conditions with RF drive applied. This is especially true for high-efficiency, non-linear operation.

The most useful RF measurement is the load-pull test. The fundamental details of the load-pull measurement are described in Ref. 1 and will not be repeated here. A block diagram of the test set-up is shown in Fig. 1. The load-pull measurement is performed at 250, 260, and 270 MHz and the load impedance needed for maximum efficiency is determined at each frequency.

The last test which is performed on the individual transistors is a high-power S-parameter measurement using the technique of Mazumder and Puije (Ref. 2). A block diagram of the test set-up is shown in Fig. 2. The high-power S-parameter measurement yields all four S-parameters of a non-linear 2-port.

The S-parameters are used to determine the regions of instability on the source and load impedance planes. The relative stability of various transistor types can then be compared to each other and the transistor type exhibiting the greatest margin of stability can be chosen for the design. The load and source impedances can then be chosen such that they do not fall into the regions of instability.

III. DEVICE SELECTION

The transistor selected for the final amplifier is the 2N6439, (C2M60-28) a 60-W device manufactured by Communications Transistor Corporation. The 2N6439 was chosen because it provides a considerable margin-of-safety when operated at 50 W and the load-pull measurements indicate good efficiency over the band of interest. In addition, there are other manufacturers producing the 2N6439 (Motorola), which alleviates the problem of having a sole source for a high-reliability device procurement.

The optimum drive for the 2N6439 was found to be 8 W. The driver was therefore sized to produce 8 W into a 50-Ω load over the 250-to-270 MHz band. Two transistors were found to have good efficiency at the 8-W level, the C12-28, a 12-W device, and the CD2088, a 10-W device. Both transistors

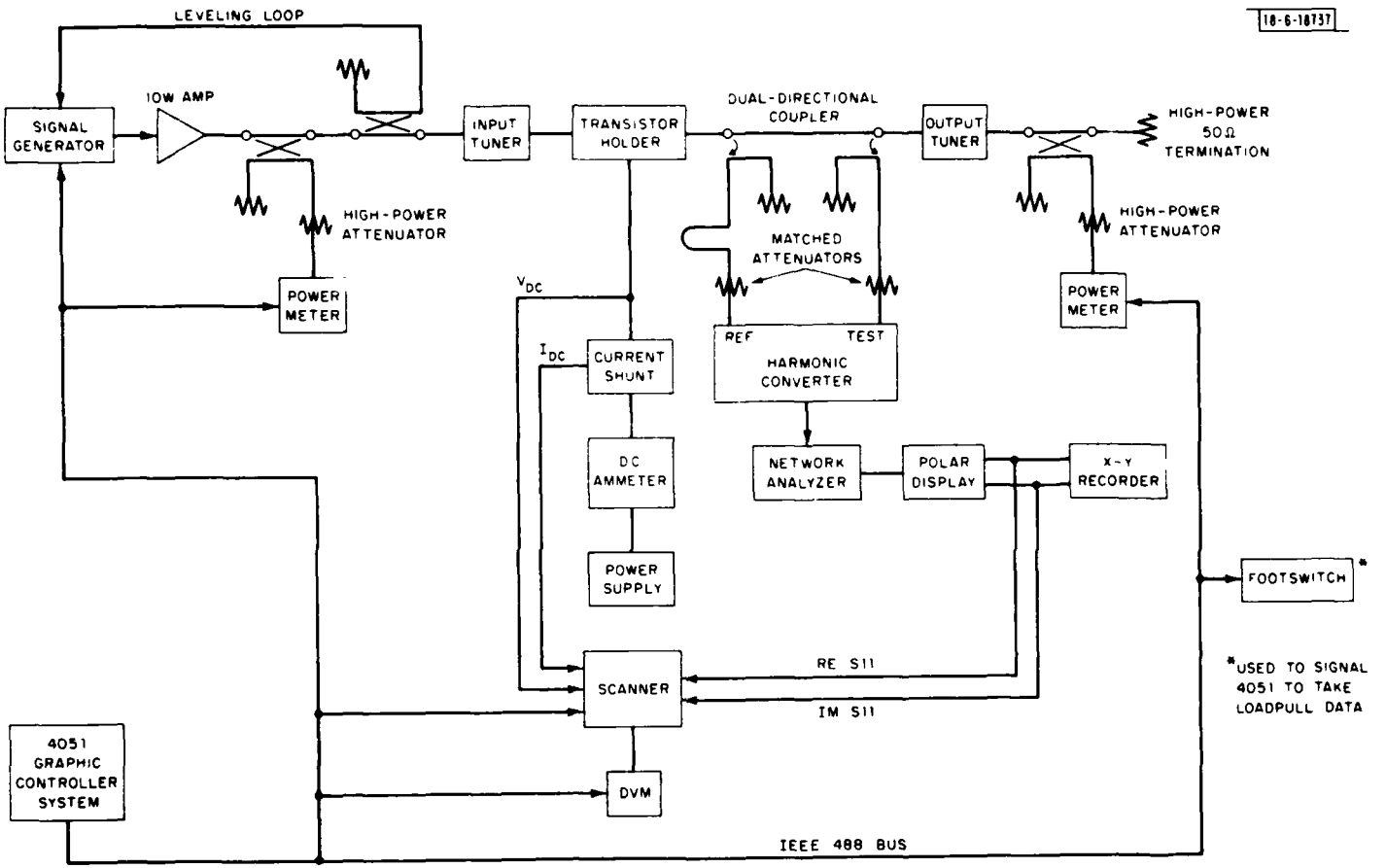

Fig. 1. Block diagram of load-pull test set-up.

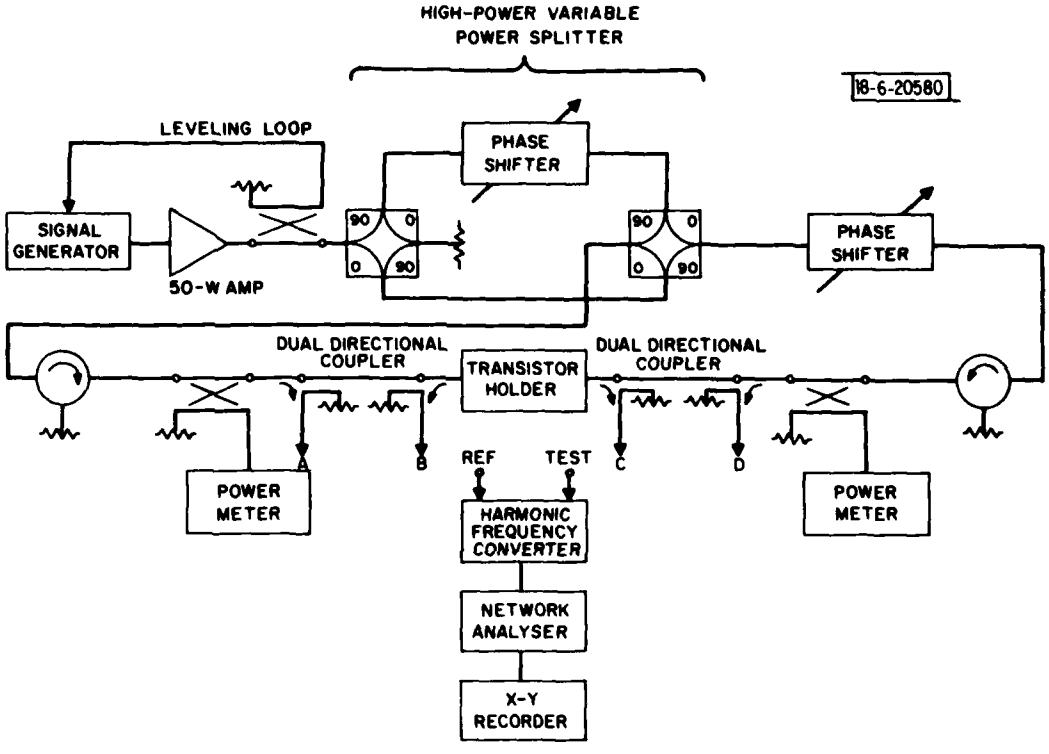

Fig. 2. Block diagram of high-power S-parameter test set-up.

have adequate margin for high-reliability at the 8-W level. The CD2088 was found to have $\tilde{\sim}$ 3 dB more gain at the maximum-efficiency point than the C12-28, but the C12-28 was selected for the driver because it demonstrated superior stability.

The optimum input for the driver stage using the C12-28 was found to be 0.8 W, but the pre-driver was specified to produce 1 W of output to provide a slight gain margin. Several transistor types were examined for the 1-W stage. The CD2035 was selected initially because it exhibited high efficiency and gain at the 1-W level. Instability problems in the 1-W stage forced a re-evaluation however, and the CD2087 was chosen for greater stability. At the same time, the loading on the 1-W stage was altered to provide a greater margin of amplifier stability over all frequencies where the amplifier exhibited gain. Some efficiency was sacrificed to provide the extra margin of stability.

Since the DC power into the 1-W stage represents a small percentage of the total DC power requirement of the transmitter, a small decrease in efficiency of the 1-W stage does not significantly affect the overall efficiency of the transmitter.

The required drive for the 1-W stage is 100 mW. It was determined that this could be supplied by a 2-stage preamp using Class A, feedback amplifiers. The Class A, feedback design was chosen to provide the 1-W stage with a reasonable 50-Ω source impedance over a wide frequency range. This would help to keep the 1-W and succeeding Class C stages stable at frequencies out of the band of interest. Also, the feedback design results in very stable performance over widely varying temperatures and supply voltages.

The disadvantages of using the Class A feedback design are:

1. The maximum efficiency using resistive feedback is 25%.

2. The open-loop gain of the transistors must be at least 10 dB (and preferably 20 dB) greater than the desired closed-loop gain, over the frequencies of interest, for consistent, predictable performance.

The transistors in the last preamp stage must be capable of reliable operation with a power dissipation of $\approx$ 0.5 W. Since the input signal level to the preamp is 1 mW, the gain of the preamp must be at least 20 dB, so each stage of the preamp must provide at least 10 dB of gain. Both preamp stages were designed to provide 13 dB of gain with a saturated power output of 100 mW from the second stage. This provides an additional 6 dB of gain margin in the transmitter, such that the output power of the transmitter will not be affected by as much as 6-dB loss in input signal. The open-loop gain of the transistors used in the preamp must be at least 23 dB. This implies an f_T of 4 to 5 GHz for the transistors.

The Hewlett Packard 35812E was chosen for both stages of the preamp since it meets the requirements of both preamp stages, and it is available in a rugged, hermetically sealed, stud-mounted package. The stud-mounting provides a reliable mechanical and thermal attachment of the transistor to a heat sink.

A summary of the design specifications for the individual stages are given in Table 1.

TABLE 1

SUMMARY OF SPECIFICATIONS

STAGE	P_{OUT}	P_{IN}	GAIN	CLASS OF OPERATION	DEVICE MANUFACTURER
FINAL AMPLIFIER	50 W	8 W	8 dB	Class C	2N6439 CTC
10-W DRIVER	8 W	1 W	9 dB	Class C	C12-28 CTC
1-W PRE-DRIVER	1 W	100 mW	10 dB	Class C	CD2087 CTC
100 mW PREAMP	100 mW	10 mW	13 dB	Class A FEEDBACK	35812E H-P
10 mW PREAMP	10 mW	1 mW	13 dB	Class A FEEDBACK	35812E H-P

IV. CIRCUIT DESIGN

A. Class C Stages

The load-pull measurements were performed on a sample quantity of each transistor type. The measurements indicate that the 1-W and 10-W devices are enough alike so that small variations between devices may be neglected, and that a single output circuit design will be adequate for all devices of a particular type.

This is not the case, however, for the transistor used in the final amplifier. Each transistor used in a final-amplifier stage requires an individual circuit design tailored specifically for that transistor. The reason for this is because of the high VSWR of the load impedance which must be provided for the final stage. Figures 3-5 show the actual load-pull data taken on the 2N6439, the C12-28, and the CD2087. As shown in Figs. 3-5, as the power level increases, so does the VSWR of the load. To maintain good performance, the desired impedances must be realized within a tolerance of ± 10%. For the CD2087 (which requires a real load impedance of $\overset{\sim}{\sim}$ 100 Ω), the tolerance is ± 10 Ω, which is easy to measure, and easy to

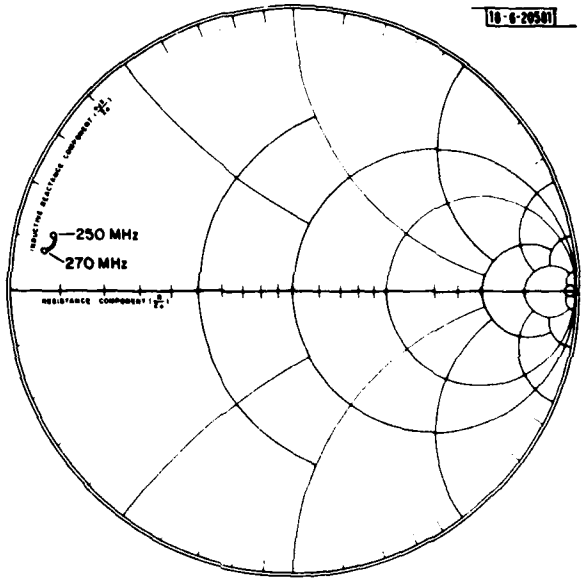

Fig. 3. Load impedance for the 2N6439 transistor at 50 W.

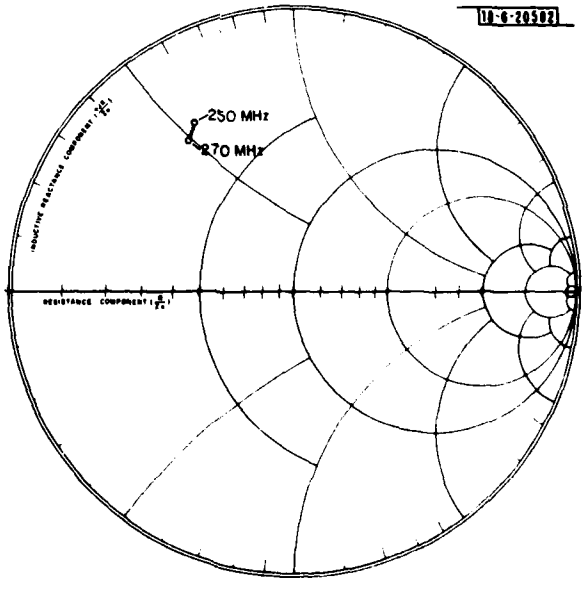

Fig. 4. Load impedance for the C12-28 transistor at 8 W.

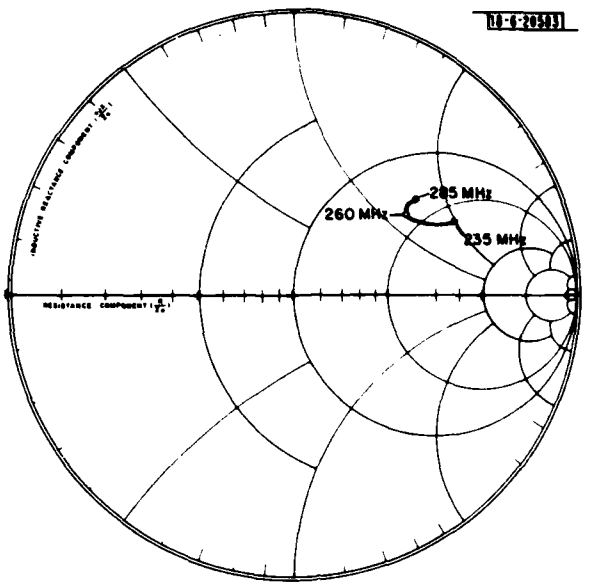

Fig. 5. Load impedance for the CD2087 transistor at 1 W.

realize. For the 2N6439 (which requires a real load impedance of $\approx$ 2.5 Ω), the tolerance is now $\pm$ 0.25 Ω, which is neither easy to measure nor to realize. Measurements have shown that the required load impedance for most low-power devices lies well within the necessary 10% tolerance. However, the required load impedance for several 2N6439 transistors was found to vary more than 17%. Therefore, the device-to-device variations are larger than the acceptable tolerance for the higher-power transistors.

The output circuit for the final amplifier was designed first. The initial design was done graphically on Smith-chart coordinates. The circuit elements used in the initial design are 50-Ω microstrip transmission lines and lumped capacitors. The microstrip transmission lines are used because they can be easily mass-produced on copper-clad teflon-fiberglass board. The lumped capacitors are necessary to provide the small capacitive reactance values called for in the circuit design. Distributed capacitors would require prohibitively large areas of printed-circuit board.

After the initial design was completed, the circuit-element values were optimized by a computer optimization program, COMPACT*
During the optimization, the microstrip transmission lines were constrained to remain 50-Ω lines with only the length as a variable. The lumped-capacitor values were also allowed to vary. The computer optimization attempted to determine the element values resulting in the smallest mean square error between the desired reflection coefficient, and the actual reflection coefficient presented to the transistor. Great care was taken to insure that the optimization did not end on a local minimum. When optimization was finally reached, resulting in the desired load for one particular transistor, then the resulting element values were used as the starting points for the optimizations for all other transistors of the same type. One additional constraint was added to the optimization process for all subsequent transistors; the individual lengths of the two microstrip transmission lines were allowed to vary, but the overall length was held constant. In other words, the variables which were used in subsequent optimizations were the values of the shunt capacitors, and their positions along a microstrip transmission line of fixed length.

The results of this procedure created an individual circuit design for each 2N6439 transistor. However, all of these designs could be built on the same printed-circuit-board layout, with only small changes in shunt-capacitor values, and/or capacitor locations along the microstrip transmission line.

During the final stages of the optimization procedure, the parasitic lead inductances of the capacitors were included as fixed element values, and all capacitors over 50 pF were broken down into parallel combinations of smaller capacitors. The importance of the parasitic lead inductance can be seen by computing the inductance needed to resonate with the larger

*Compact Engineering, Inc., Los Altos, California, (January 1977).

capacitor values used in the filter design. A typical capacitor value is four 36-pF capacitors in parallel, or 144-pF. The operating frequency is 260 MHz. The resonating inductance is given by:

$$L = \frac{1}{(2\pi f)^2 C} \qquad (1)$$

For the example given, the value of L is 2.6 nH. The lead inductance of a typical ATC 100 or ATC 175 capacitor, in the B case size, with microstrip ribbon leads, is 0.5 to 1.5 nH, depending on the length of the ground path. It is seen that the parasitic lead inductance, therefore, is a significant portion of the resonant inductance and can have a dramatic effect on circuit performance. Paralleling small capacitors to achieve large capacitance values helps in two ways. First, the effective lead inductance is divided by the number of capacitors in parallel since the lead inductances are effectively in parallel when capacitors of equal value are used. Second, the effective series resistance of several capacitors in parallel is generally much less than the effective series resistance of a single component having the same total capacitance. The published performance curves for American Technical Ceramics, ATC 100 capacitors (Ref. 3) indicate that the equivalent series resistance varies approximately, inversely as the square root of the capacitance. Because of this, a single 144-pF capacitor will have twice the equivalent series resistance of four 36-pF capacitors connected in parallel. Maintaining a low equivalent series resistance is a major factor in keeping the losses in the matching filters to a minimum.

The design of the output matching network for the final amplifier is shown in Fig. 6. The element values are tabulated in Table 2 for a sample of 2N6439 transistors.

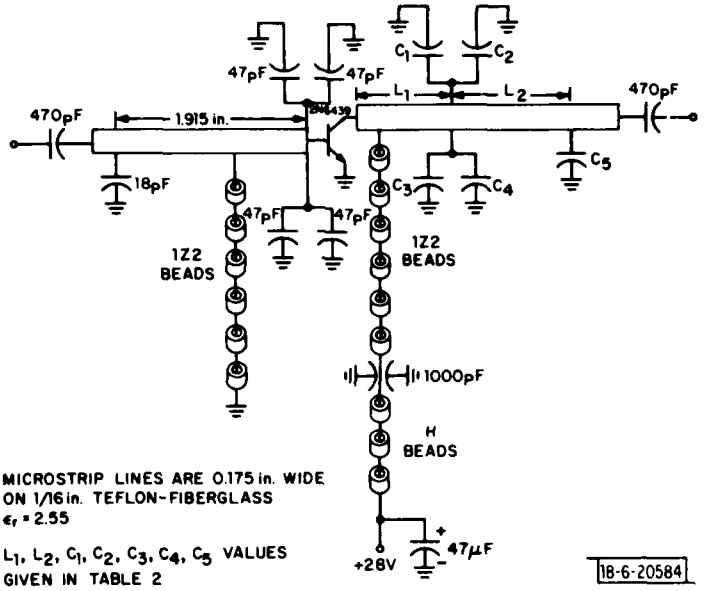

Fig. 6. 50-W final amplifier.

TABLE 2

50 W AMPLIFIER COMPONENT VALUES

DEVICE #	L_1	L_2	C_1, C_2, C_3, C_4	C_5
1	0.822"	2.050"	33 pF	30 pF
2	0.751"	1.907"	36 pF	33 pF
3	0.903"	2.065	33 pF	33 pF
4	0.764"	1.896"	36 pF	33 pF
5	0.750"	1.803"	39 pF	36 pF

The design of the input matching filter for the final amplifier was accomplished by matching the input impedance values given in the manufacturer's specifications to 50 Ω using a Chebychev impedance-transforming network (Ref. 4). The final value and placement of the 18-pF capacitor in the input matching filter was determined during initial turn-ON.

The 10-W driver circuit is shown in Fig. 7. The output circuit was designed graphically using Smith-chart coordinates and the input circuit was determined experimentally at initial turn-ON. The output circuit for the driver stage is a high-pass structure which does not result in the highest possible efficiencies because of the high harmonic content of the output signal. However, a low-pass structure which provides the same match requires either very long microstrip transmission lines or lumped inductors. The high-pass structure was chosen because of its compactness and simplicity, and because the harmonic content of the driver output signal would not be passed through the final amplifier.

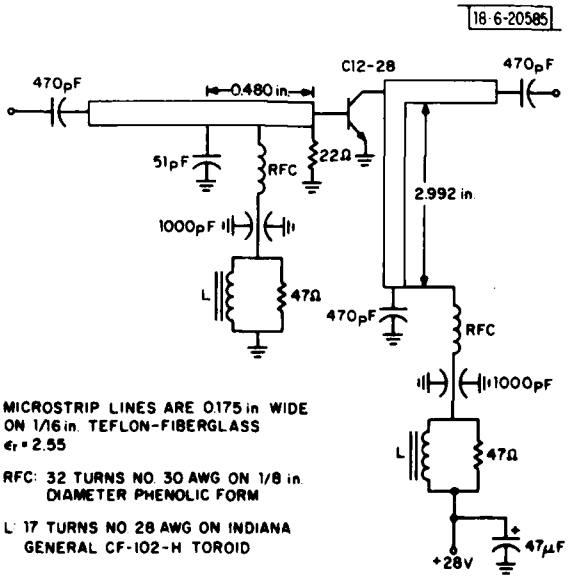

Fig. 7. 10-W driver.

The 1-W pre-driver circuit is shown in Fig. 8. This circuit was initially derived using graphical techniques on Smith-chart coordinates. The output circuit was then optimized for the desired values using COMPACT The load was not optimized for efficiency in this case. As mentioned in the previous section, the stability margin of the 1-W amplifier was increased by loading the transistor away from the point of maximum efficiency. Load-pull measurements for the CD2087 indicate a maximum efficiency of 60% with 1 W of RF output power and 80 mW of RF input power. The increased stability margin was achieved by operating the transistor at 45% collector efficiency with the same input and output power levels. The impedance transformation which was required in the output circuit did not lend itself to a microstrip transmission line realization, because the length of the series and shunt-stub lines would have required too much circuit-board area. The values of equivalent lumped inductors were easily realizable, however; so the circuit was designed using both lumped capacitors and lumped inductors.

The input circuit was realized in microstrip and the final input tuning was done during initial turn-ON.

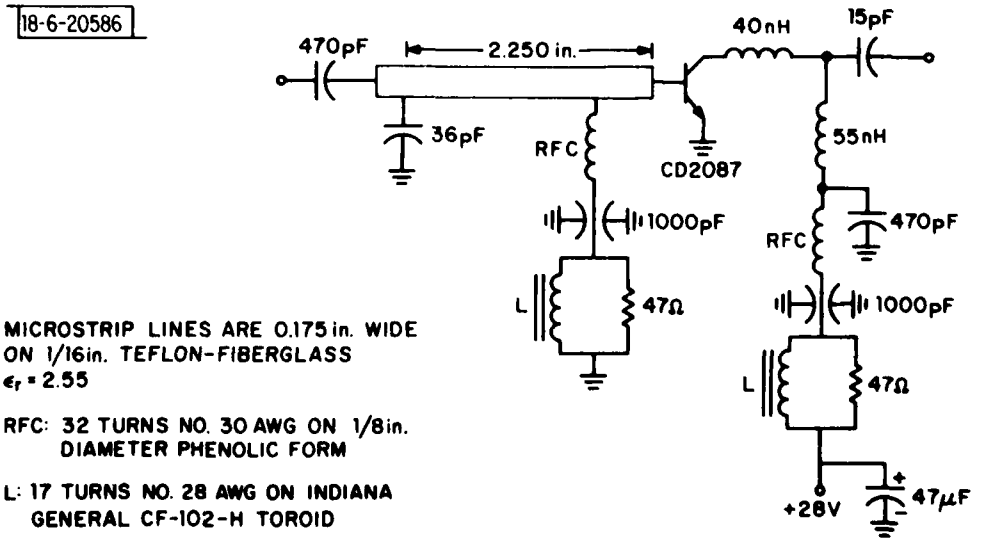

Fig. 8. 1-W pre-driver.

B. Preamp Stages

The preamp circuit was modeled as shown in Fig. 9.

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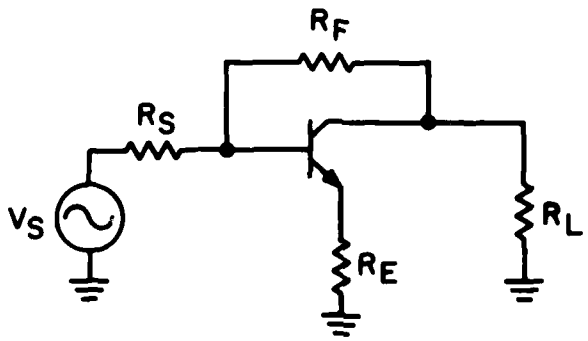


Fig. 9(a). Class A feedback amplifier.

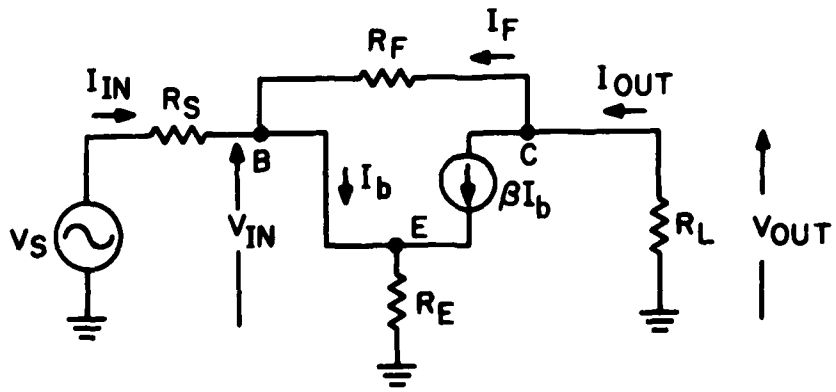


Fig. 9(b). Feedback amplifier model.

The following equations may be written for the circuit shown in Fig. 9b (See Appendix B)

$$Z_{in} \approx \frac{R_E(R_F + R_L)}{R_E + R_L} \tag{2}$$

$$G_V \approx \left(\frac{R_E - R_F}{R_F + R_L}\right) \cdot \left(\frac{R_L}{R_E}\right) \tag{3}$$

$$Z_{OUT} \approx \frac{R_E(R_F + R_S)}{R_S + R_E} \tag{4}$$

where, Z_{IN} is the input impedance of the amplifier stage,
G_V is the voltage gain of the amplifier stage,
and Z_{OUT} is the output impedance of the amplifier stage.

A computer program was written to solve the three non-linear equations simultaneously given the following criterion:

The input impedance Z_{IN}
The load resistance R_L
And, the voltage gain in dB $(20\log_{10}|G_V|)$

The computer would then solve for the two feedback resistors R_E and R_F, and the necessary source resistance R_S which would give the specified Z_{IN} and G_V, and match Z_{OUT} to R_L.

For the special case where $Z_{IN} = Z_{OUT}$, the equations may be solved directly yielding the following results:

$$R_S = R_L \tag{5}$$

$$R_E = \frac{R_S}{1 - G_V} \tag{6}$$

$$R_F = \frac{R_S^2}{R_E} \tag{7}$$

Equations 5-7 were solved for the special case where $R_S = 50\ \Omega$, $R_L = 50\ \Omega$, and $Z_{IN} = Z_{OUT} = 50\ \Omega$. The gain was specified at 13 dB or $G_V = -4.47$. (G_V is negative because the common-emitter stage is an inverting amplifier.) Solving for R_E and R_F:

$$R_E = 9.1\ \Omega$$

$$R_F = 273.5\ \Omega$$

Included in R_E is the r_e' of the transistor which is given by (Ref. 6):

$$r_e' = \frac{25}{I_E\text{(mA)}} \tag{8}$$

I_E must be determined by the power-output capabilities of the stage. Since the feedback amplifier has an output impedance of 50 Ω and the load is 50 Ω, half of the available power from the transistor is dissipated in the amplifier feedback circuitry. Therefore, the transistor must be biased to produce twice the necessary output power. Furthermore, the transistor sees a total load of 25 Ω since the amplifier source impedance and the load impedance are, effectively, in parallel.

The second preamp stage must supply 100 mW into a 50-Ω load, so the transistor must be biased to supply 200 mW into 25 Ω. The minimum collector voltage is given by

$$V_{CC} = \sqrt{2P_oR_L} \tag{9}$$

$V_{CC} = 3.16$ V, $P_o = 0.2$ W, $R_L = 25\ \Omega$

The quiescent bias current can now be determined from the equation

$$I_Q = \frac{2P_o}{V_{CC}} \tag{10}$$

I_Q = 127 mA for P_o = 0.2 W and V_{CC} = 3.16 V.

This current exceeds the maximum current rating of the 35812E transistor. It was determined that the amplifier would have adequate output power with a quiescent operating point of 90.0 mA and 4.46 V. Under these conditions, the amplifier produced 80 mW of saturated output power.

The same circuit was used for the 10-mW stage; however, the bias point was set at 28 mA. An active bias network was used with the second stage to keep the total current requirements of the preamp stage to a minimum. The bias circuit is shown in Fig. 10. The circuit uses a balanced differential amplifier to maintain a constant DC current through R_E2. The voltage across R_E2 is compared to the voltage across the voltage divider R1 and R2. If the voltage across R_E2 drops, the differential amplifier becomes unbalanced with less current being drawn through R4. This causes the voltage on the base of the 35812E to rise; thereby supplying more current to the base of the 35812E. For immunity to power-supply variations, R2 could be replaced with a zener-reference diode.

Since high-beta transistors can be used in the differential pair, the normal current through R1 and R2 can be insignificant compared to the quiescent current of the 35812E. The current through the differential pair must be only slightly greater than the maximum required bias current for the 35812E under worst-case conditions. Under high radiation conditions the DC beta of the 35812E may degrade to as low as 20. Using this as the worst-case bias condition, the resistor values can then be determined. For a power supply voltage of 7 V and $R_E2 \approx 20\ \Omega$, the complete preamp circuit is shown in Fig. 11. The feedback resistor values were changed slightly to

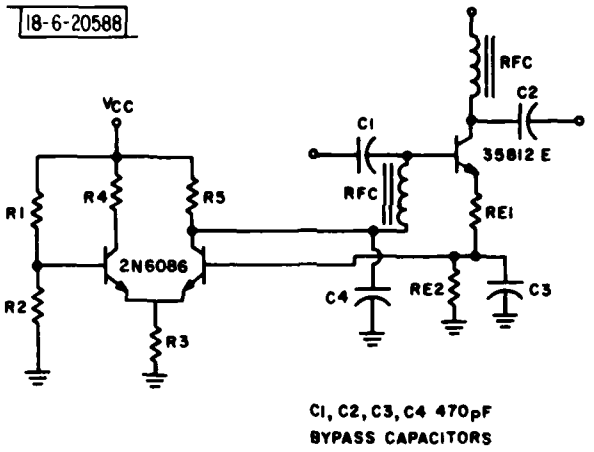
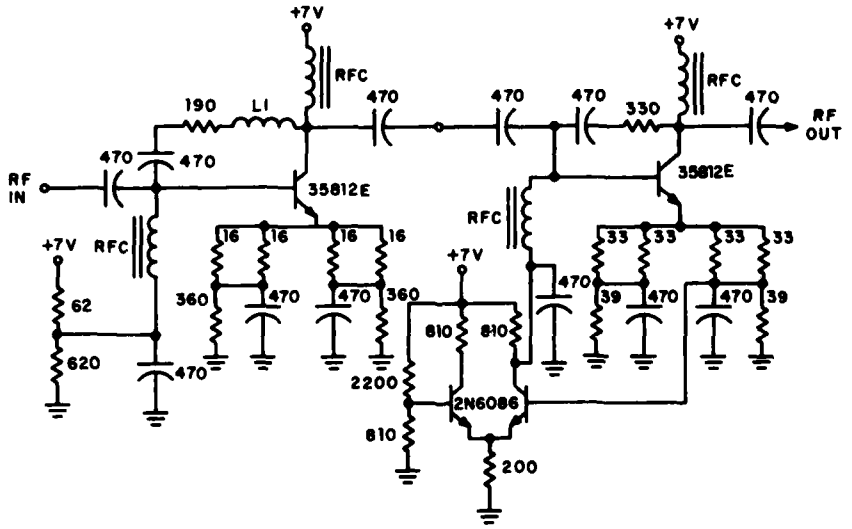


Fig. 10. Active bias network.



RFC: 5 TURNS NO. 30 AWG NYLESE ON FERROXCUBE 3B FERRITE BEAD

L1: 9 TURNS NO. 30 AWG NYLESE ON 6,32 NYLON SCREW

18-6-20589

ALL CAPACITORS ARE pF UNLESS OTHERWISE SPECIFIED

RESISTORS ARE IN OHMS

Fig. 11. Two-stage preamp circuit.

optimize the gain and VSWR over the 250-to-270-MHz band. An inductor, L1, was added to the feedback circuit of the first stage, to compensate for gain roll-off at the higher frequencies. Multiple, paralleled, emitter resistors were used to balance the current flow through the two emitter leads, and to reduce the series inductance in the emitter circuit as much as possible.

V. CONSTRUCTION TECHNIQUES

A. Printed-Circuit-Board Layout

The entire transmitter was constructed on $\frac{1}{16}$" teflon-fiberglass printed-circuit boards. The actual printed-circuit board layouts are shown in Fig. 12.

The breadboard version of the final amplifier was originally laid out on a 3" x 3" board to save space, and it was necessary to fold the microstrip transmission lines to fit the circuit on the board. The final-stage amplifiers constructed in this fashion required some minor re-tuning after construction because the coupling between adjacent lengths of folded line was not considered in the original design. Since the final-amplifier circuit is extremely critical to the operation of the transmitter, and because one of the original goals was to construct high-power amplifiers which require no tuning after assembly, the final amplifier was redesigned using co-linear transmission lines. Although this resulted in a much longer package, the width was reduced such that the board area remained essentially the same. The co-linear circuit layout resulted in excellent agreement between predicted and measured performance, and required no tuning after assembly.

B. Grounding

Another major difficulty encountered during the construction of breadboard circuits was how to ground components on the top side of the printed-circuit board to the ground plane underneath, in a way that resulted

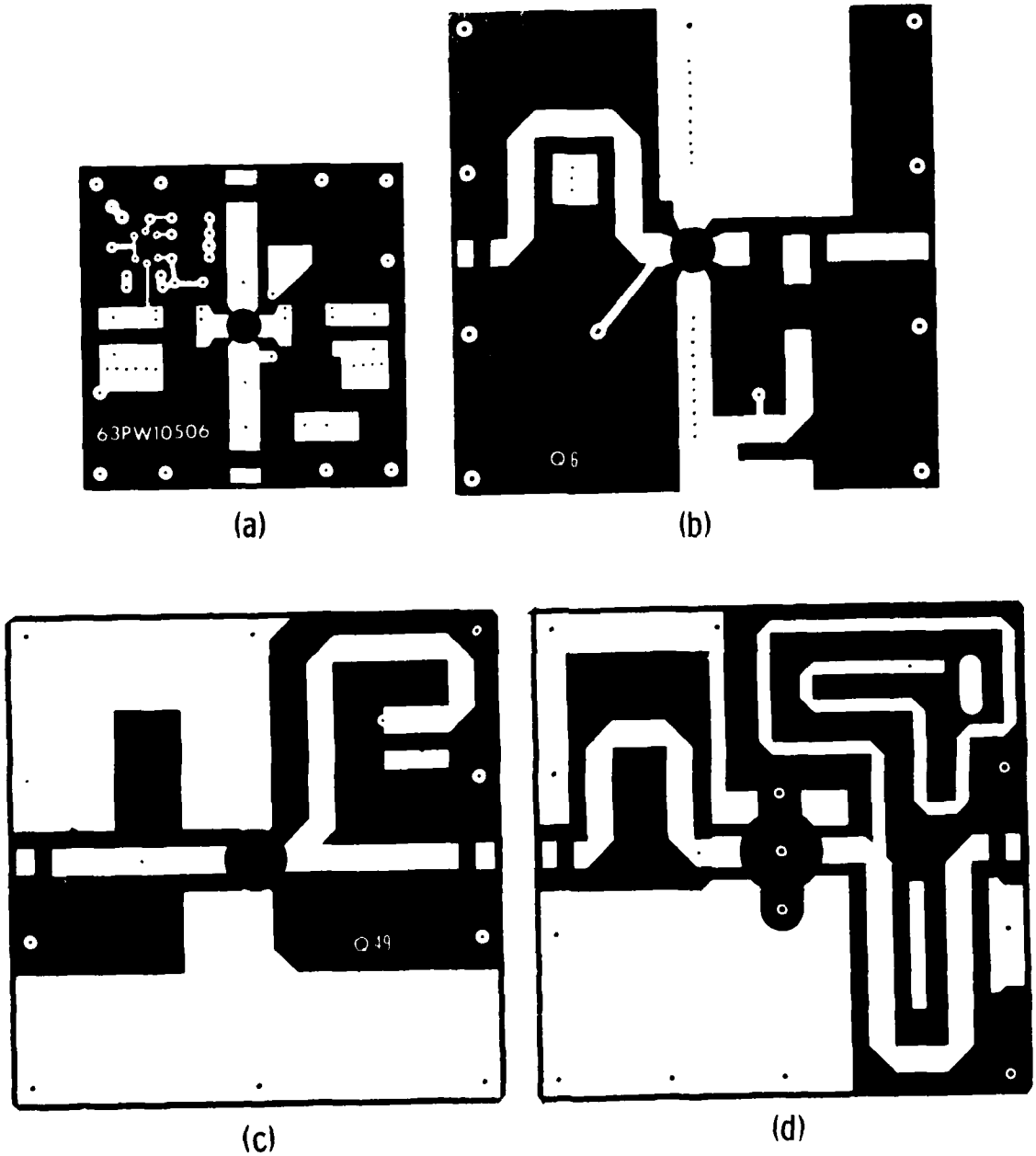


Fig. 12(a-e). Printed-circuit-board layouts: (a) Preamp stages (b) 1-W stage (c) 10-W stage (d) 50-W stage.

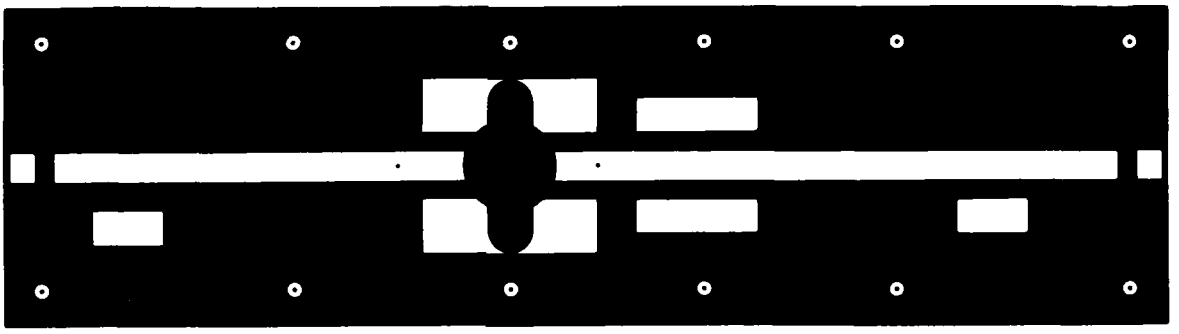


Fig. 12(a-e). Printed-circuit-board layouts: (e) 50-W prototype stage.

in minimum parasitic induc ance. The breadboard circuits were constructed with small ground-pad areas on the top side of the board, which were grounded to the bottom side with #24 or #26 AWG tinned-copper-wire strands spaced $\approx \frac{1}{16}$" apart. This technique was found to present several problems. First, the grounding was not consistent from board to board. The lacings were found to introduce a noticeable parasitic inductance into the ground path of the critical components, and the value of the parasitic inductance was found to be overly sensitive to location, wire size, and number-of-lacings. Second, the lacing wire had to be soldered to both sides of the teflon-fiberglass board with no service loop, to provide the minimum parasitic inductance. Because of the large coefficient of thermal expansion of teflon-fiberglass board, this technique results in intermittent ground connections and cracked solder joints.

A better method of grounding components was achieved by placing the ground pads at the edge of the board wherever possible and soldering a wide strip of copper foil to the top and bottom metalizations, folding the strip around the edge of the board. In places where the ground pads could not be placed at the edge of the board, narrow slots were milled through the teflon-fiberglass board adjacent to the ground-pads so that a foil strip could be passed through the board. After all of the foil grounding strips were placed on the board, and before any components were mounted, the printed-circuit boards were lead-tin solder-plated to protect the copper foil from oxidation.

The foil-grounding technique resulted in very low parasitic inductances. The procedure was very repeatable and well-suited to a manufacturing environment. Another benefit resulting from the foil-grounding technique is that there is no solder build-up on the ground-plane side of the board such as there is when lacing is used. This allows the printed-circuit boards to lie flat on the bottom of the enclosures, which simplifies box construction and provides better mechanical and thermal contact between the printed-circuit board and the enclosure. The thin copper foil has superior

thermal-cycling characteristics over lacing, plated-thru holes, or edge plating, because the thin foil "gives" when subjected to thermal stresses rather than cracking and causing an intermittent connection.

C. DC Bias Considerations

There are three important requirements for the DC bias networks in any RF circuit:

1. The bias network must cause minimal loading of the circuit at the frequencies of interest. If the DC bias network is part of the RF circuit, then high-Q elements must be used in the RF portion of the network to minimize losses at the frequencies of interest. All of the care that has gone into producing a very-high-efficiency amplifier may be lost if the DC bias network adds only a few tenths of a dB additional loss in the output network.
2. The bias network must terminate the active device in such a way that stability is maintained from DC to f_{max}. The RF circuit provides the necessary termination for the active device at the operating frequency, but the bias network must properly terminate the transistor at all other frequencies where the active device has gain.
3. The bias network must have low loss at DC. This consideration is important for high-efficiency performance.

The collector bias network used on the breadboard final-stage amplifier was a $\lambda/4$ 100-Ω microstrip transmission line shorted at the end with a 470-pF RF-bypass capacitor. DC was fed in near the bypass capacitor through four ferrite beads of Indiana General "H" material, and a shunt 47-μF tantalum capacitor. The base bias network used on the breadboard final-stage consisted of a self-resonant RF choke in series with three "H" beads from the base to ground. The RF choke is 32 turns of #30 AWG close-wound on a $\frac{1}{8}$" diameter x $\frac{1}{2}$" phenolic, axial-leaded coil form. This bias

configuration gives excellent performance over the entire 250-to-270-MHz band. However, at ≈ 240 MHz a low-frequency oscillation (below 1 MHz) was excited in the breadboard final amplifier.

A different bias configuration is used in the prototype final amplifier. It has the advantages of being more compact, having lower loss, and providing greater stability at low frequencies. The new collector bias circuit consists of six Ferroxcube "1Z2" ferrite beads placed over a #22 AWG tinned copper wire. The wire is attached to the collector on one end and to a 1000-pF feed-through capacitor on the other end. The feed-through capacitor is mounted on a partition separating the RF circuitry and the DC circuitry. In the DC compartment the feed-through capacitor is connected to a shunt 47-μF tantalum capacitor and the DC connector. Over the wire connecting the feed-through to the tantalum capacitor are three "H" beads. The base bias network for the prototype final-amplifier consists of six "1Z2" beads over a tinned copper wire connected between the base and ground. The prototype bias configuration is shown in Fig. 6.

A different bias network was used on the 10-W and 1-W stages. The bias network is shown in Fig. 13.

The RF choke is a self-resonant coil at the operating frequency of 260 MHz and causes negligible loading of the RF circuitry. The feed-through capacitor bypasses any residual RF currents to ground and isolates the DC circuitry from RF. A coil wound on a ferrite toroid in parallel with a 47-Ω resistor provides a series resistance of ≈ 47 Ω down to ≈ 100 KHz. The 47-Ω resistor lowers the Q of the bias network, particularly the RF choke, at frequencies where the transistor has very high gain. This reduces the tendency of the amplifier to oscillate at frequencies below the operating band.

An additional 22-Ω resistor was placed between the base and ground of the C12-28 transistor in the 10-W driver to increase the damping on the base bias network. The 22-Ω resistor caused only slight loading of the RF circuit because of the low input impedance of the transistor.

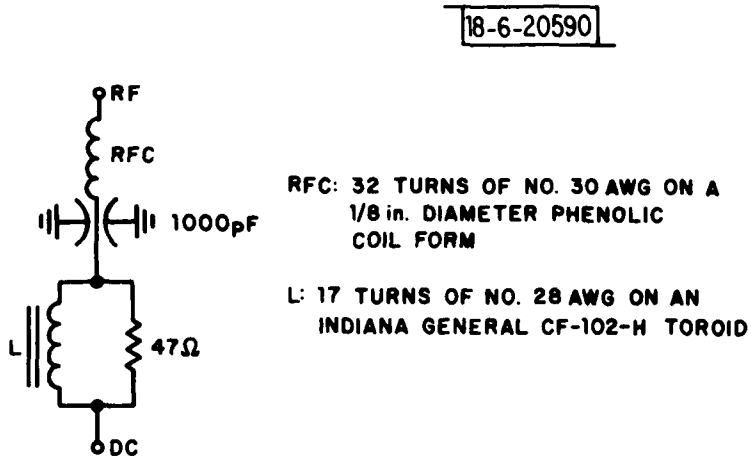


Fig. 13. Bias network for 1-W and 10-W stages.

VI. BREADBOARD TRANSMITTER

A block diagram of the breadboard transmitter is shown in Fig. 14. Directional couplers were placed on the input and output of the transmitter for *RF measurements*. Circulators were placed at the output of the 1-W pre-driver stage and at the final-amplifier output for protection against high-VSWR loads.

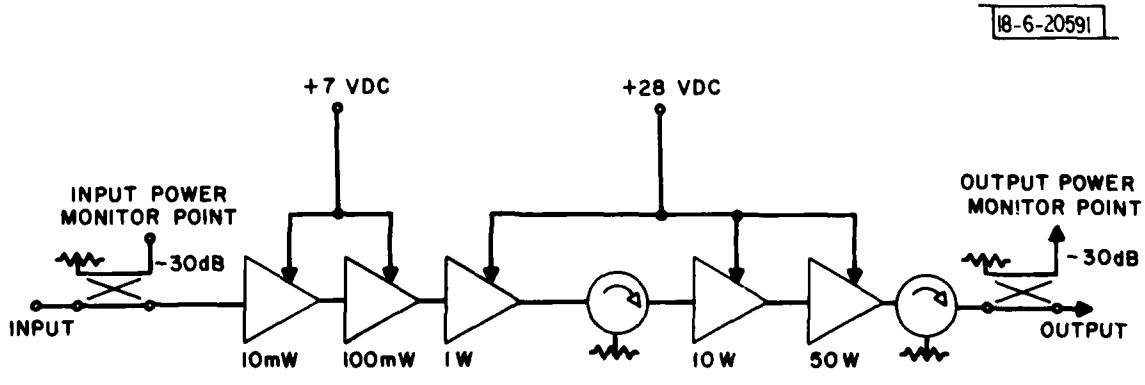
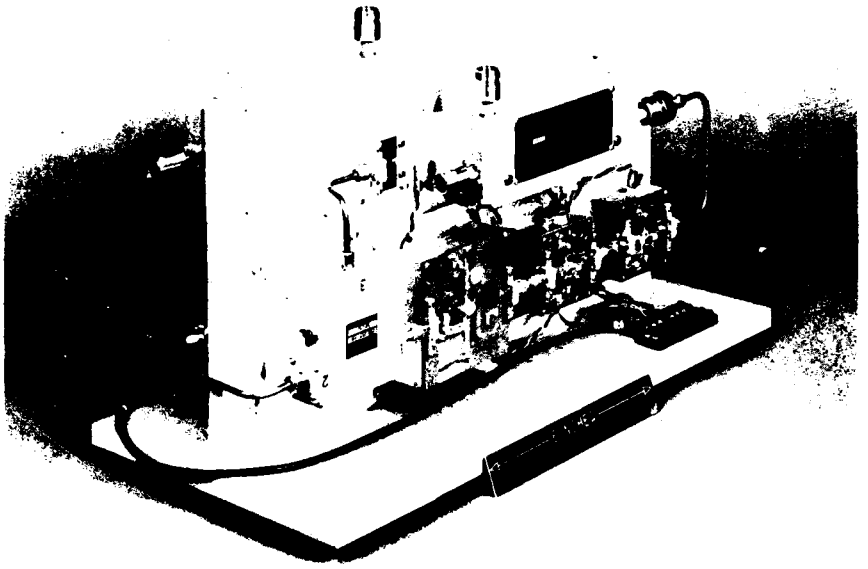


Fig. 14. Block diagram of the breadboard transmitter.

The breadboard transmitter is shown in Fig.15 as it was mounted for testing.

P202-9331



P202-9332

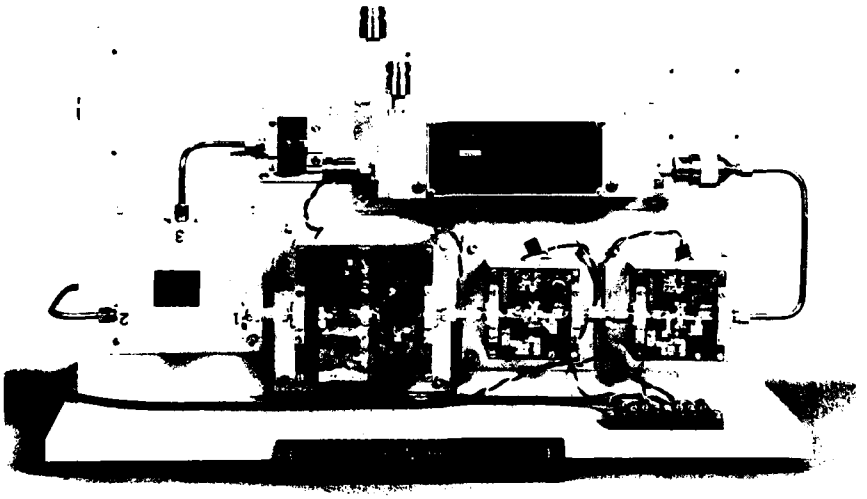


Fig. 15(a-b). (a) Breadboard transmitter (b) Breadboard transmitter low-power stages.

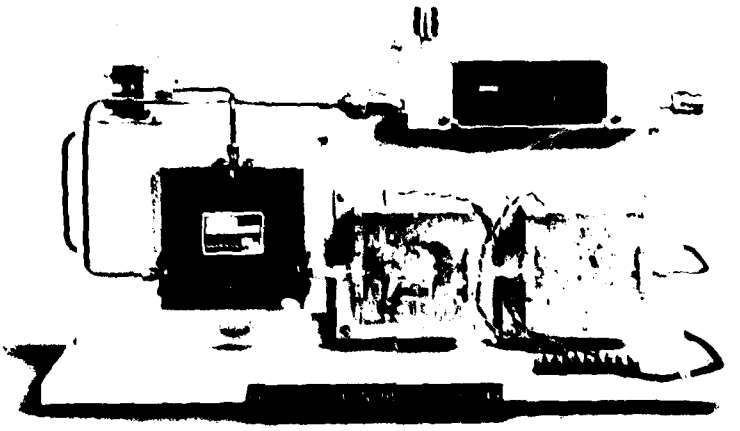


Fig. 15(c). Breadboard transmitter high-power stages.

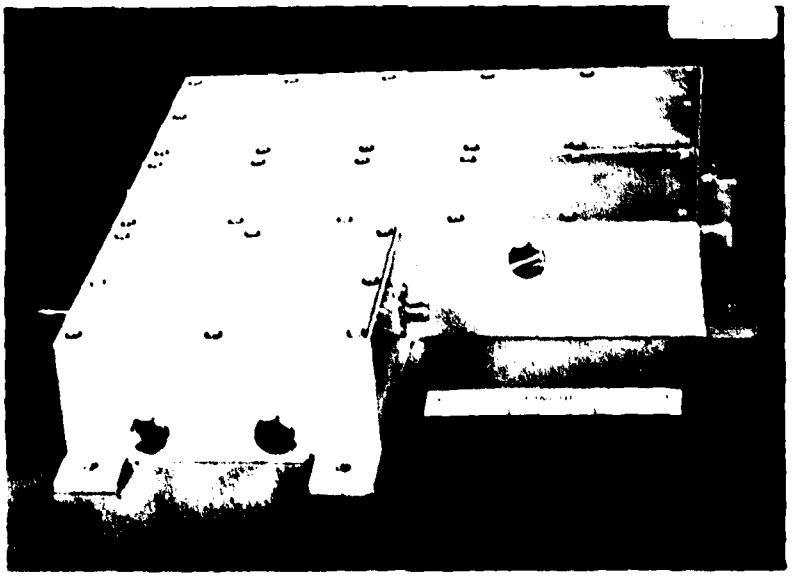


Fig. 16(a-c). Prototype transmitter driver and final amplifier: (a) Fully assembled.

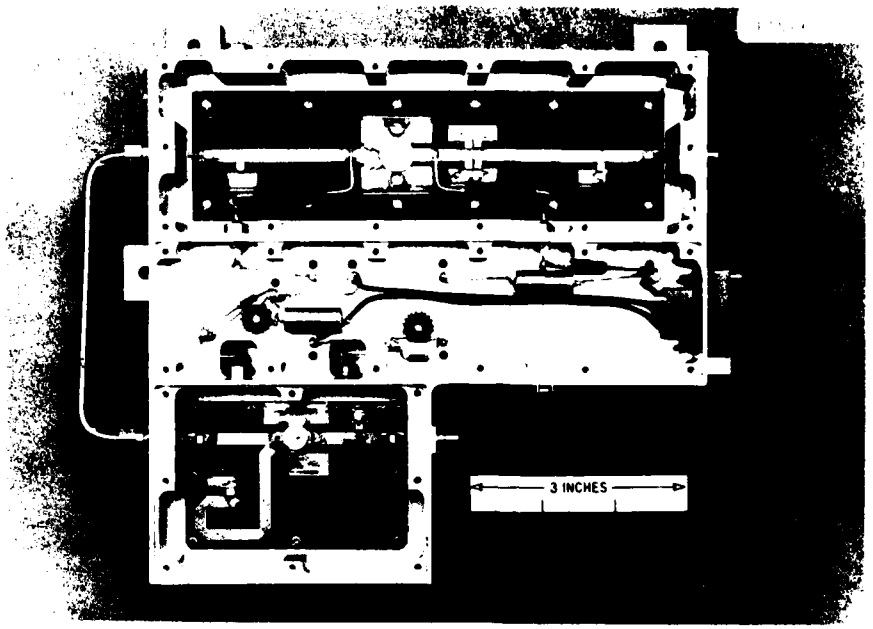


Fig. 16(a-c). Prototype transmitter driver and final amplifier: (b) Top view with covers removed.

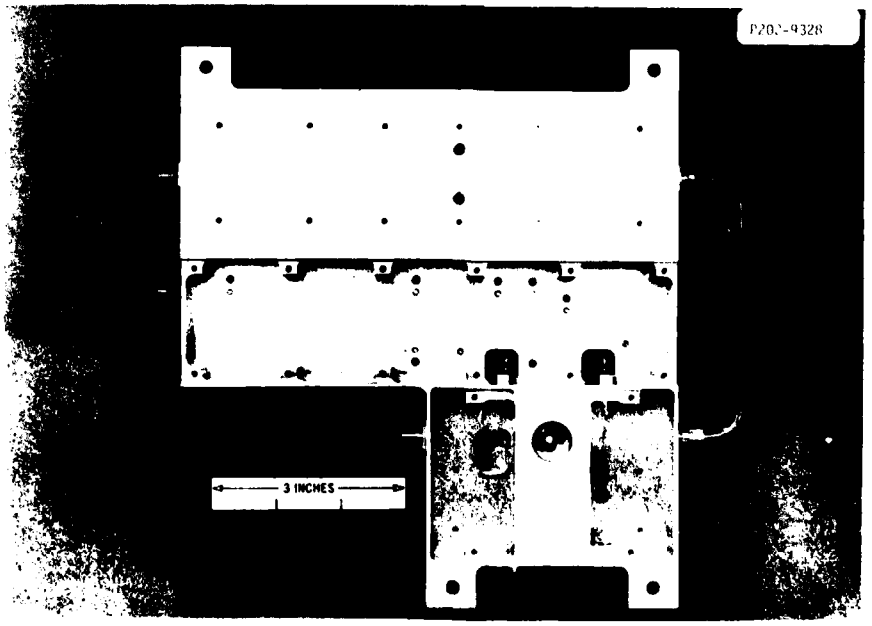


Fig. 16(a-c). Prototype transmitter driver and final amplifier: (c) Bottom view with covers removed.

VII. PROTOTYPE DRIVER AND FINAL AMPLIFIER

A flight-like prototype consisting of the final-amplifier and driver stages was constructed, to demonstrate packaging techniques suitable for a space environment. The major considerations in the design of the flight-like enclosure were:

1. The transfer of heat away from the high-power stages into the spacecraft structure.
2. The ruggedness to withstand the rigors of launch.
3. Low mass.

The transfer of heat is accomplished through the bottom surface of the module where large areas of metal have been left for this purpose. The high-power transistors make intimate contact with the inside bottom surface of the enclosure resulting in the shortest possible heat path from the transistors to the spacecraft structure.

The enclosure was milled from a solid block of aluminum to provide rigidity, and maximum electrical and thermal conduction throughout all parts of the box. All components have a low profile to minimize the chance of vibration-induced movement and flexing, and lie on a solid surface where they can be bonded with a flight-approved epoxy. The printed-circuit boards are mounted flat on the inside bottom surface of the enclosure for maximum mechanical support and heat-sinking.

The measured mass of the flight-like prototype driver and final amplifier as shown in Fig. 16 is 1.1612 kg. This mass could be reduced considerably by more extensive machining processes, but this was not felt to be necessary for the purposes of this study.

VIII. RF PERFORMANCE

Detailed RF performance measurements were made on the breadboard transmitter. With the aid of computer-automated instrumentation, the RF performance was measured over variations in frequency, input-power level, power-supply voltages, and temperature. Complete performance data is included in Appendix A, and a summary is given in Table 3.

TABLE 3

TRANSMITTER PERFORMANCE SUMMARY

250-270 MHz

TEMPERATURE	+25°C	+60°C	-40°C
POWER OUTPUT	55-59 W	54-56 W	46.5-54 W
MINIMUM COLLECTOR EFFICIENCY	66%	64%	62%
MINIMUM OVERALL EFFICIENCY	57%	55%	53%
MAXIMUM RF DRIVE REQUIRED FOR 50 W OUTPUT	-1.8 dBmW (0.66 mW)	-.3 dBmW (0.933 mW)	+2. dBmW* (1.6 mW)
HARMONIC OUTPUT**	< - 50 dBc	< - 50 dBc	< - 50 dBc
SPURIOUS OUTPUT	NONE	NONE	LOW-FREQUENCY, LOW-LEVEL OSCILLATION WHEN DRIVEN AT 240 MHz
MAXIMUM DC POWER REQUIRED	105 W	103 W	98 W

*Maximum RF Drive required for 45 W output

**dBc = dB referenced to carrier at full output power

Table 3 shows a degradation in performance at -40°C. This was caused by a loss in gain in the preamplifier stages. A modification in the bias level of the Class A stages should restore the gain at -40°C.

The overall efficiency of the transmitter was slightly below the goal of 60% minimum across the band of interest. This is mainly due to the low collector efficiency of the final amplifier, which occurred after several circuit changes were made to increase the stability at low frequencies. When new final amplifier and driver circuit boards were built and tested which incorporated all of the changes into a new design, the collector efficiency of the final amplifier was between 76% and 78%, and the overall efficiency of the final and driver together was over 64% across the band.

The calculated overall efficiency of the entire transmitter using the new driver and final amplifier is 62% at 250 MHz and +25°C.

IX. DISCUSSION

There are several performance deficiencies which showed up during the temperature testing of the breadboard transmitter. The loss in gain at -40°C has already been discussed. Another problem which appeared at low temperature was a spurious low-frequency oscillation in the final amplifier. The oscillation would occur when the transmitter was being tested at $\approx$ 240 MHz, outside the band of interest. The oscillation is indicative of a marginally adequate bias network in the final amplifier. Modifications to the bias circuitry were made on the prototype final amplifier, which helped to clear up this problem.

A subharmonic spurious output occurs in the 1-W stage when the power-supply voltage drops to 4-10 V from the nominal 28 V DC, while the stage is being driven at full input power from the preamp. The occurrence of this mode of operation is shown by an abrupt rise in current to the 1-W stage. (See Appendix A, Figs. 6i, 7i, and 8i). If the R.F. drive is reduced or removed, the instability no longer occurs. One possible solution is to

redesign the Class A preamplifier stages to operate from the same 28-V supply so that when the supply voltage drops, the drive to the 1-W stage is reduced also.

Another basic deficiency in the preamp is a small gain margin. Originally the preamp was designed such that the output from the 1-W stage would not change with as much as 6-dB loss in RF-drive to the preamp. When the 1-W stage was redesigned for greater stability, the new stage no longer had the same saturation characteristics and the 6-dB gain margin was lost. A new preamp design would restore an adequate gain margin to the system.

X. CONCLUSION

It has been shown that the measurement, design, and construction techniques developed in this study are sufficient to produce flight-qualified, UHF transmitter hardware in a manufacturing environment without sacrifice in performance. It has been shown that an overall transmitter efficiency of greater than 60%, over a 20-MHz bandwidth, is achievable with a fix-tuned design. Furthermore, the most critical part of the transmitter, the output-matching circuitry, requires no tuning after assembly. The selection and placement of capacitors in the input circuitry was found to be necessary only for the first units which were constructed, and the process could be completed in a matter of minutes by manufacturing personnel.

The measurements which were performed on the breadboard transmitter indicate that a redesign of the Class A preamp stages may be necessary. Because of the low power consumption of the preamp, it is not expected that any redesign in this area will affect the overall efficiency significantly.

One other area which requires further investigation is the design of bias networks for high-power Class C stages, to result in stable performance at frequencies both in and out of the band-of-interest. A general solution to this problem which could be applied to all stages regardless of power level or RF circuit design, was never found.

One final note is that a microprocessor-controlled, motor-driven, slotted-line tuner has been constructed which allows the necessary load-pull measurements to be performed quickly and accurately by unskilled personnel. The slotted-line tuner will be the subject of a forthcoming paper.

ACKNOWLEDGMENTS

The author would like to express his appreciation to Richard E. Dolbec for the design of special test apparatus and his helpful comments and suggestions during the course of this study. The author would also like to thank Richard Maggliocco, Anthony Shaw, and Charles Almeida for technical assistance, and Melvin Holmes for the design of the flight-like enclosure for the prototype driver and final amplifier.

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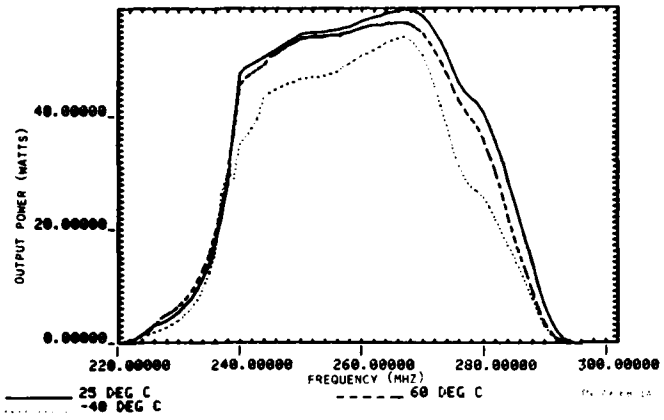
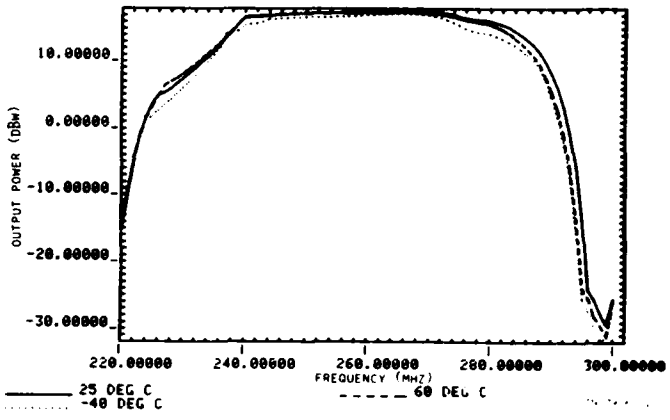
5. Pettit and McWhorter, Electronic Amplifier Circuits, (McGraw Hill, New York 1961) p. 14.

APPENDIX A

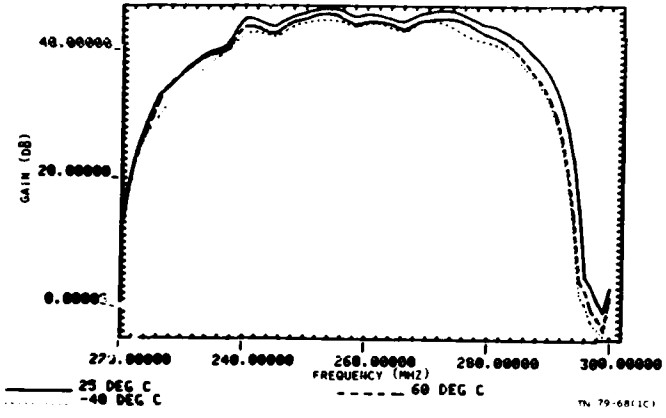
TRANSMITTER PERFORMANCE DATA



(a) Output power (watts)

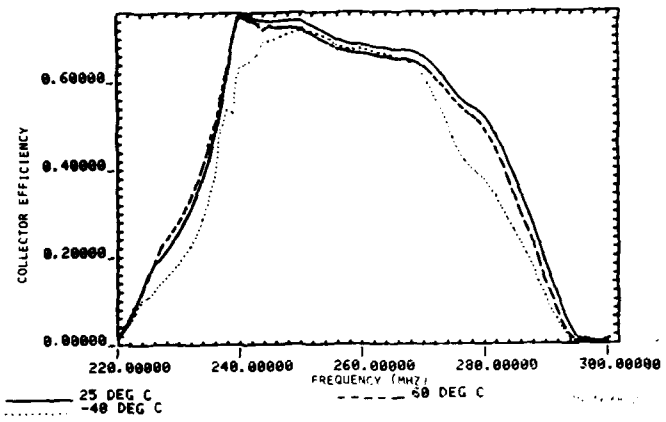


(b) Output power (dBW)

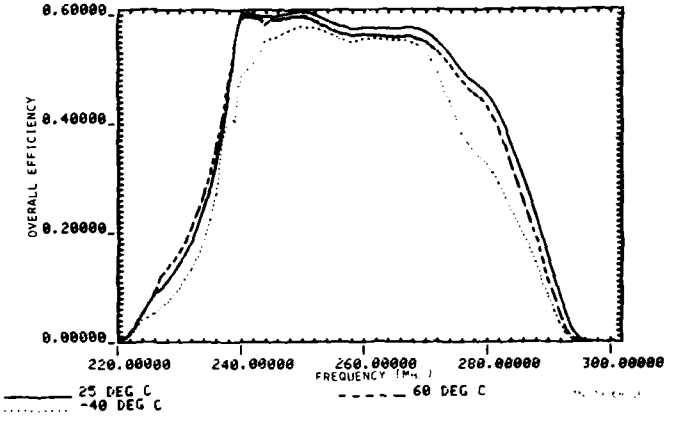


(c) Gain (dB).

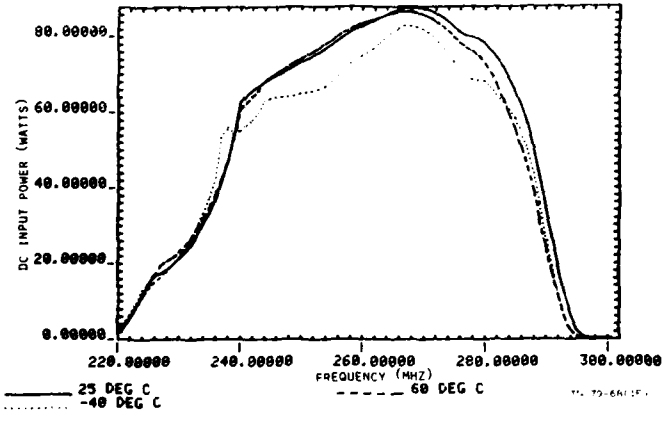
Fig. 1(a-c). Transmitter performance vs frequency and temperature.



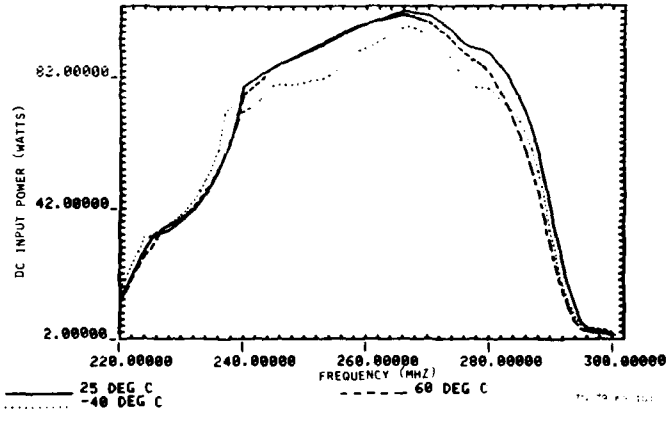
(d) Collector efficiency



(e) Overall efficiency

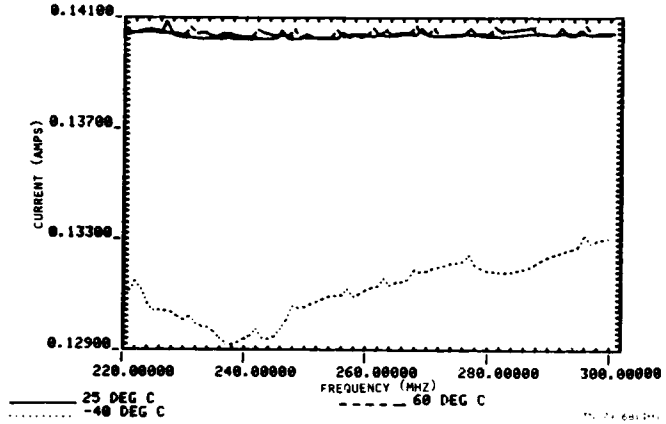


(f) DC input power to final amplifier

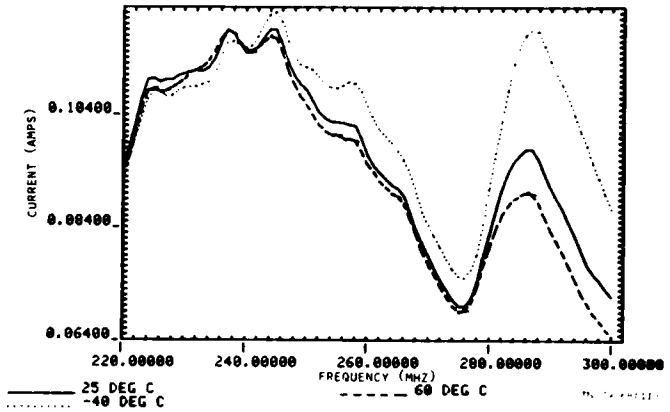


(g) DC input power to transmitter.

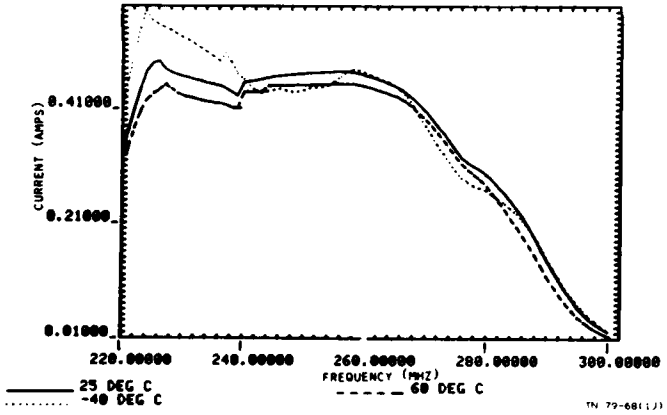
Fig. 1(d-g). Transmitter performance vs frequency and temperature.



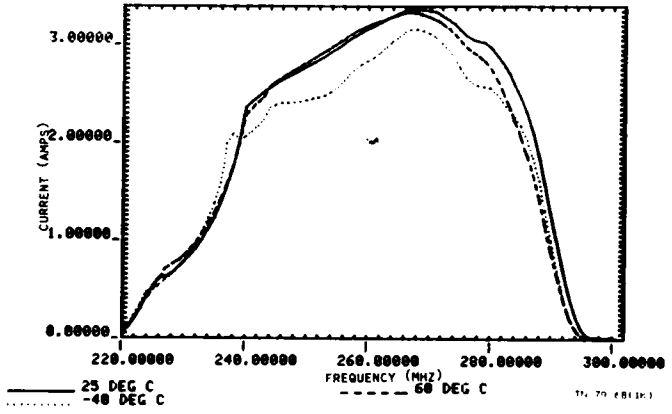
(h) DC current to preamp



(i) DC current to 1-watt stage

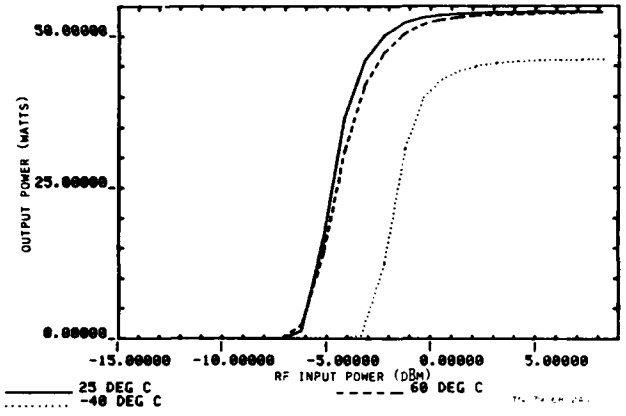


(j) DC current to 10-watt stage

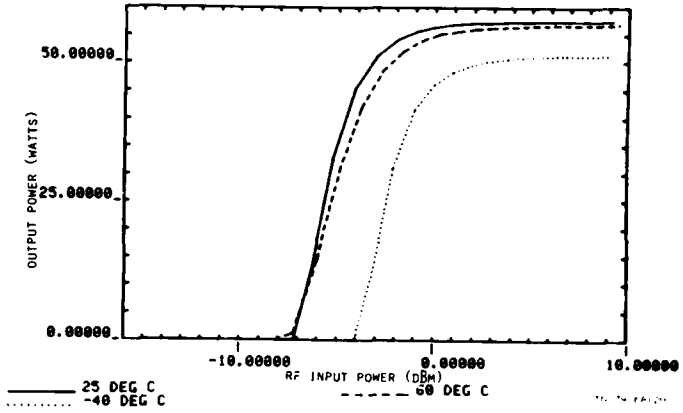


(k) DC current to final amplifier.

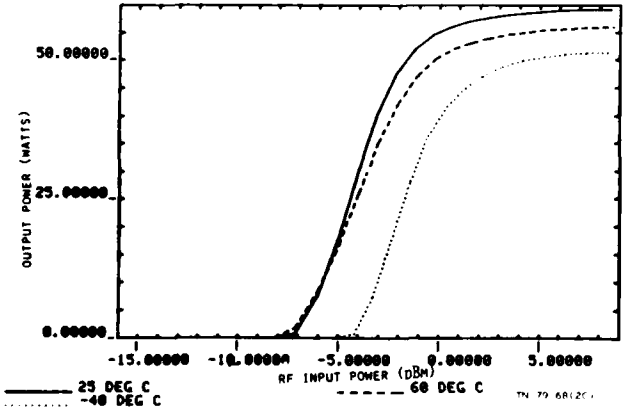
Fig. 1(h-k). Transmitter performance vs frequency and temperature.



(a) 250 MHz

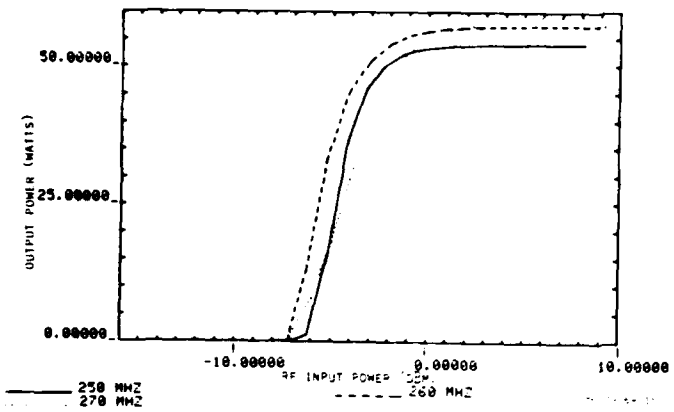


(b) 260 MHz

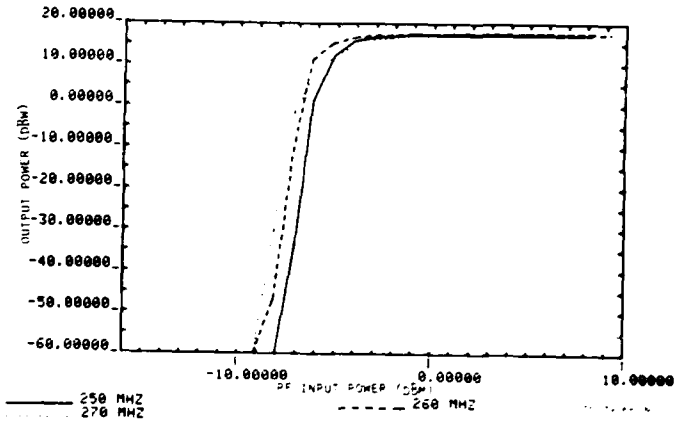


(c) 270 MHz

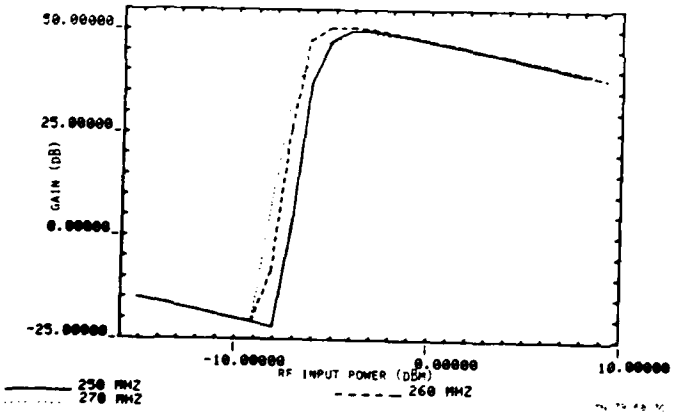
Fig. 2(a-c). Transmitter output power vs r.f. input level and temperature.



(a) Output power (watts)

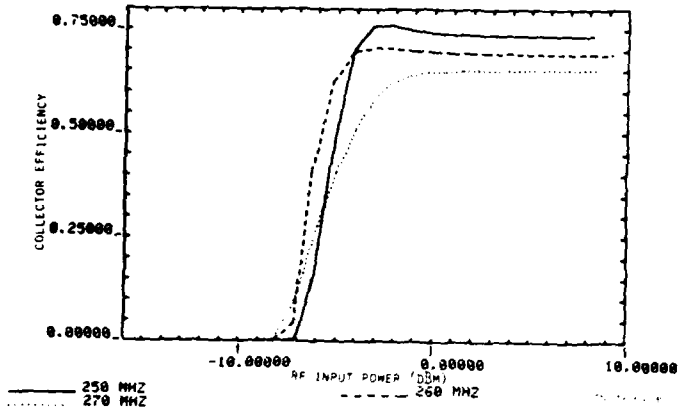


(b) Output power (dBW)

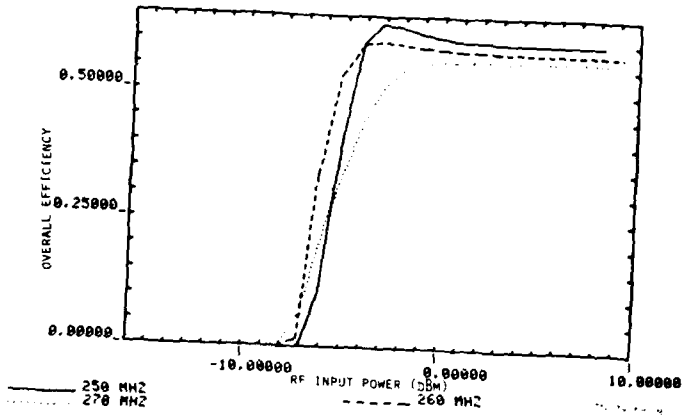


(c) Gain (dB)

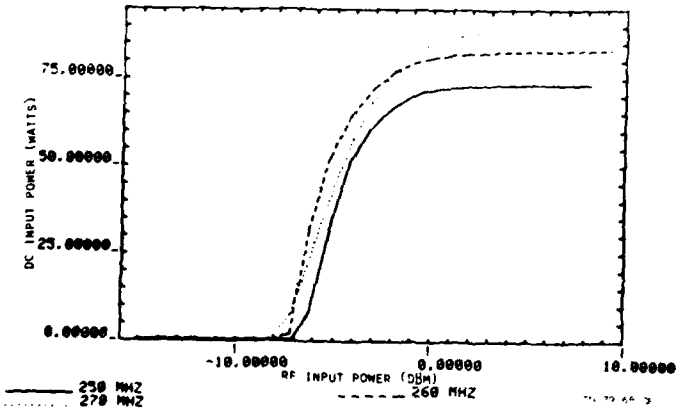
Fig. 3(a-c). Transmitter performance vs r.f. input level and frequency at 25 DEG C.



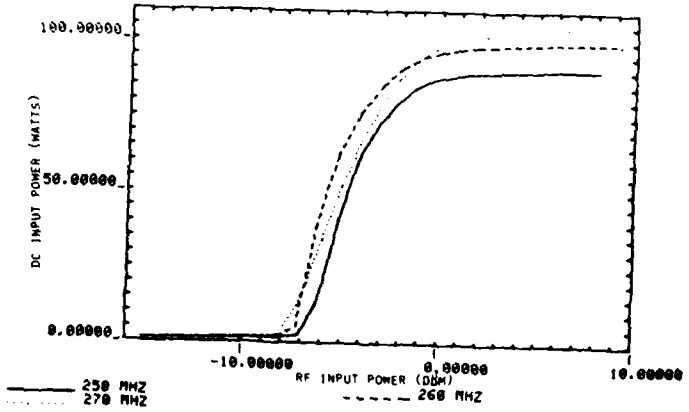
(d) Collector efficiency



(e) Overall efficiency

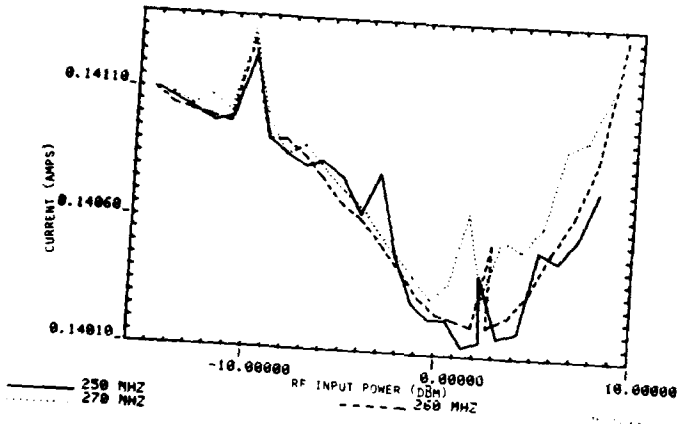


(f) DC input power to final amplifier

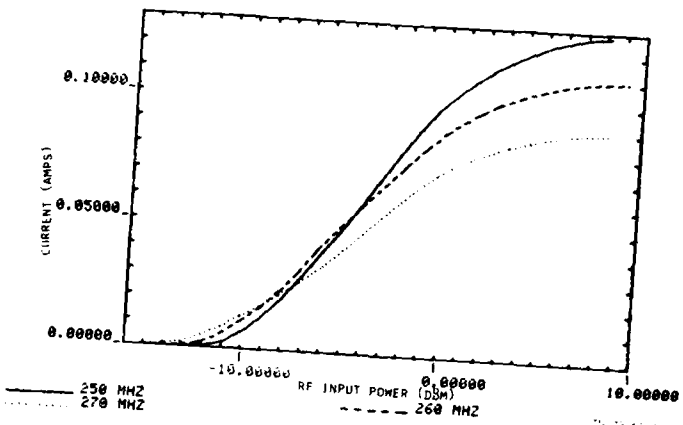


(g) DC input power to transmitter

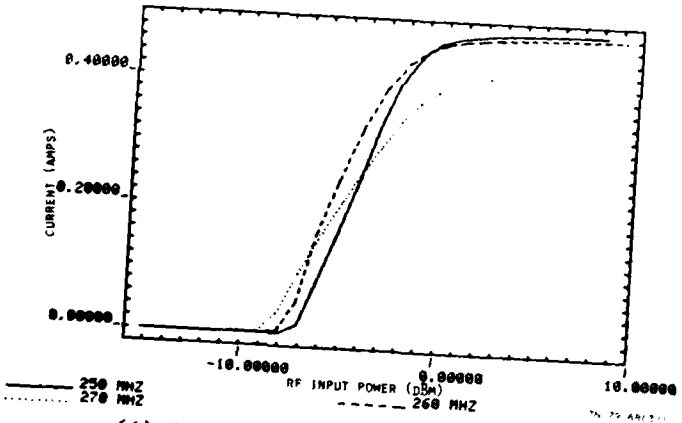
Fig. 3(d-g). Transmitter performance vs r.f. input level and frequency at 25 DEG C.



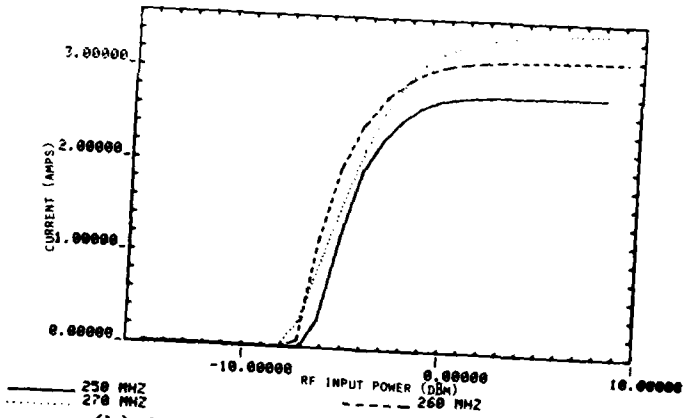
(h) DC current to preamp



(i) DC current to 1-watt stage

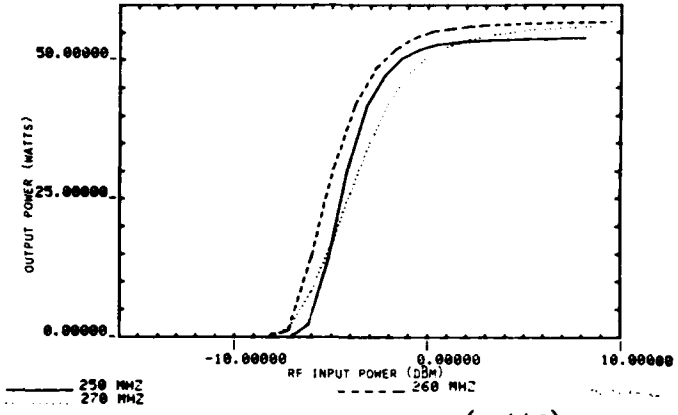


(j) DC current to 10-watt stage

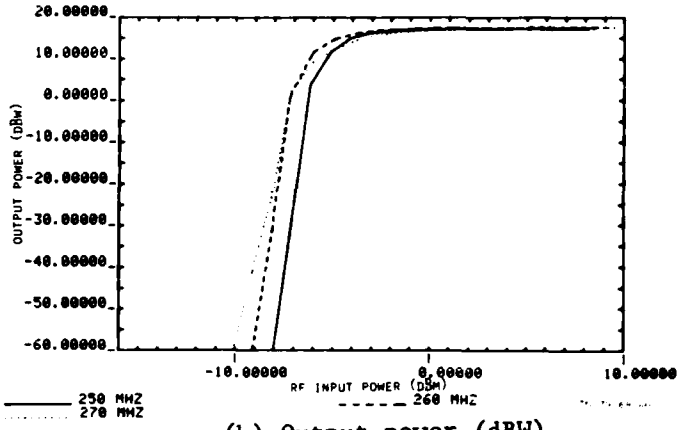


(k) DC current to final amplifier

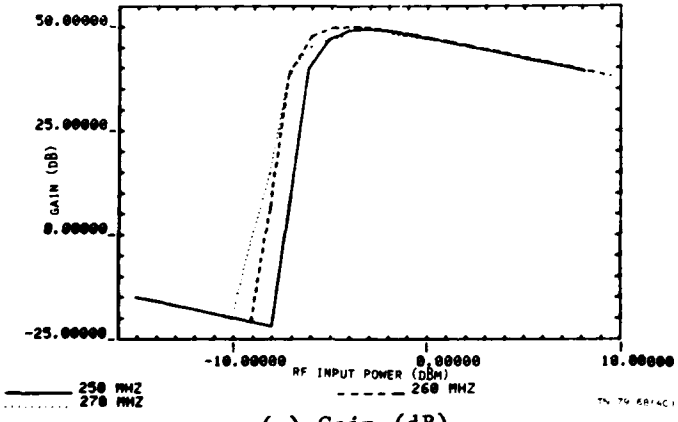
Fig. 3(h-k). Transmitter performance vs r.f. input level and frequency at 25 DEG C.



(a) Output power (watts)

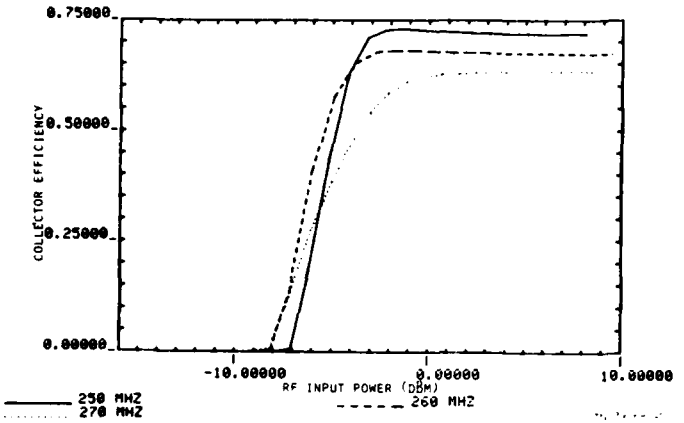


(b) Output power (dBW)

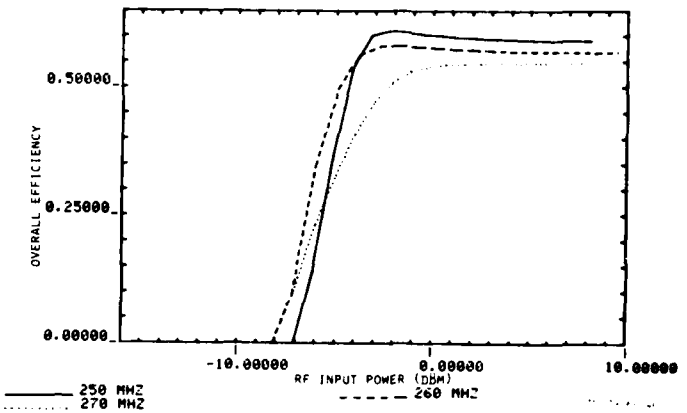


(c) Gain (dB)

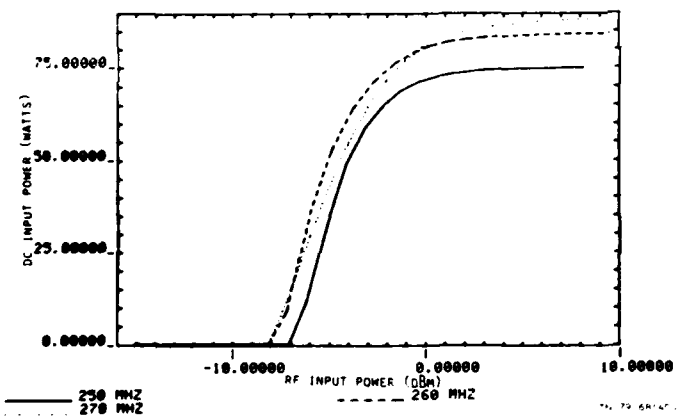
Fig. 4(a-c). Transmitter performance vs r.f. input level and frequency at 60 DEG C.



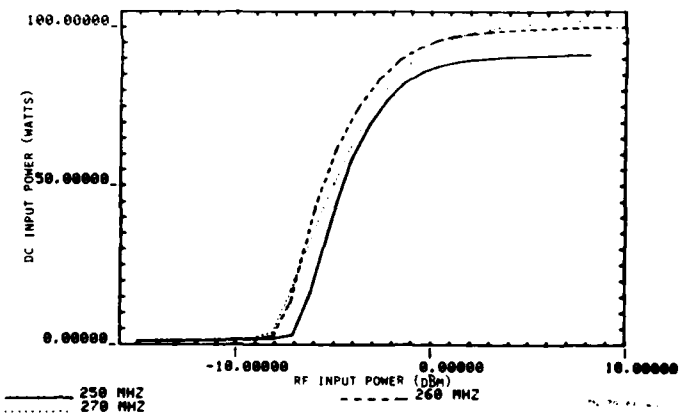
(d) Collector efficiency



(e) Overall efficiency

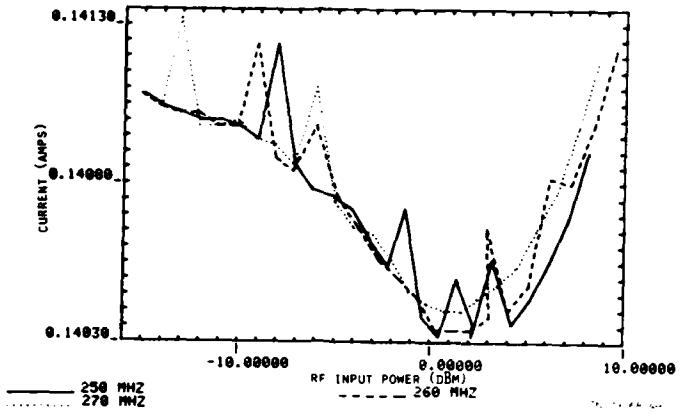


(f) DC input power to final amplifier

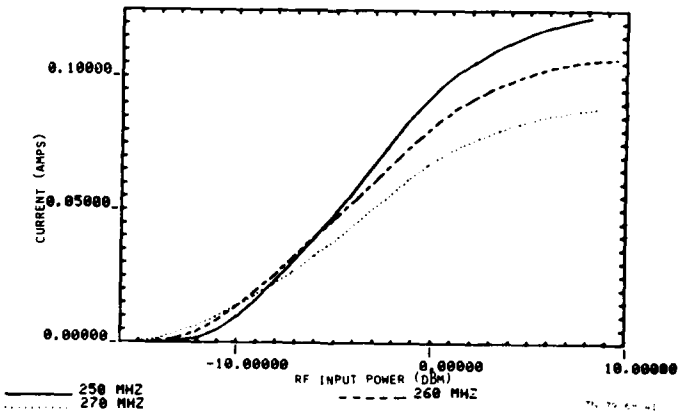


(g) DC input power to transmitter

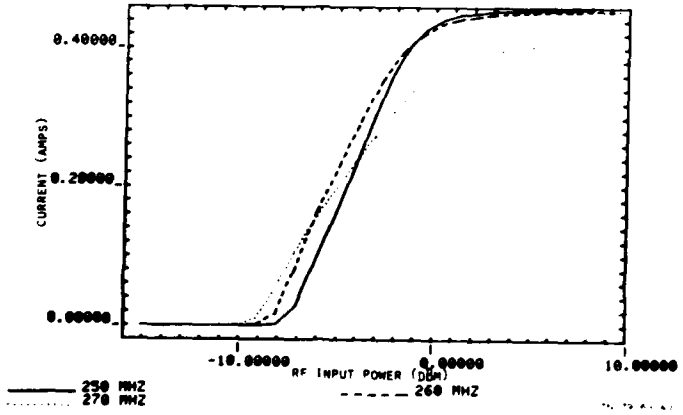
Fig. 4(d-g). Transmitter performance vs r.f. input level and frequency at 60 DEG C.



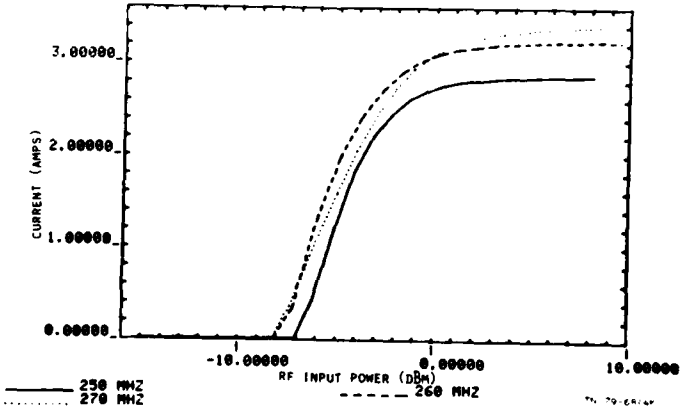
(h) DC current to preamp



(i) DC current to 1-watt stage

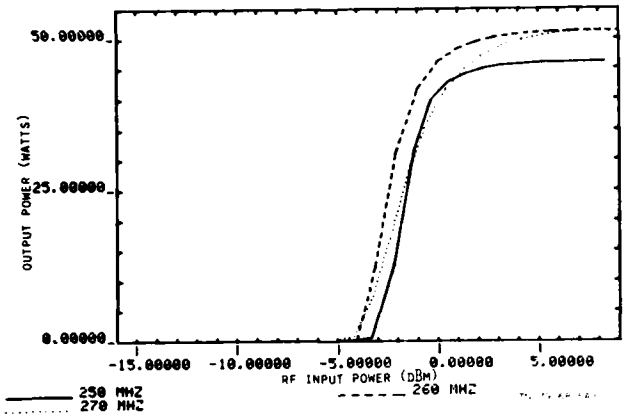


(j) DC current to 10-watt stage

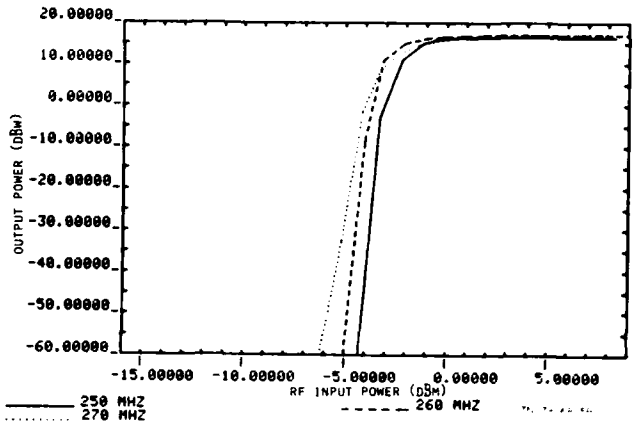


(k) DC current to final amplifier

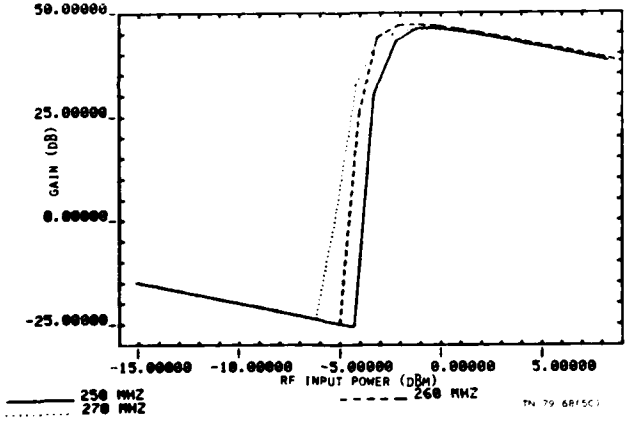
Fig. 4(h-k). Transmitter performance vs r.f. input level and frequency at 60 DEG C.



(a) Output power (watts)

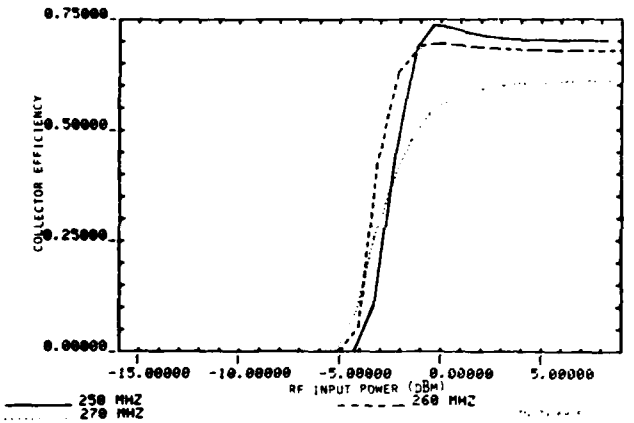


(b) Output power (dBW)

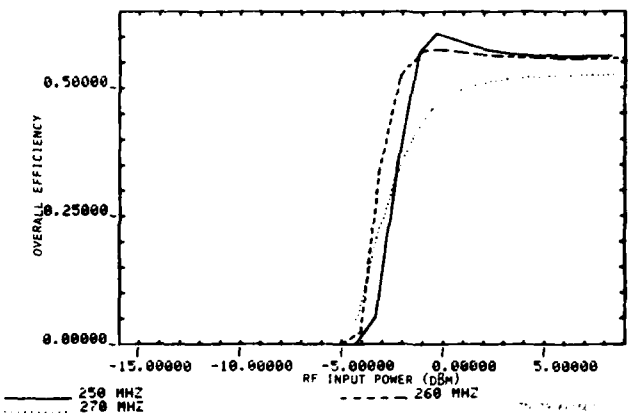


(c) Gain (dB)

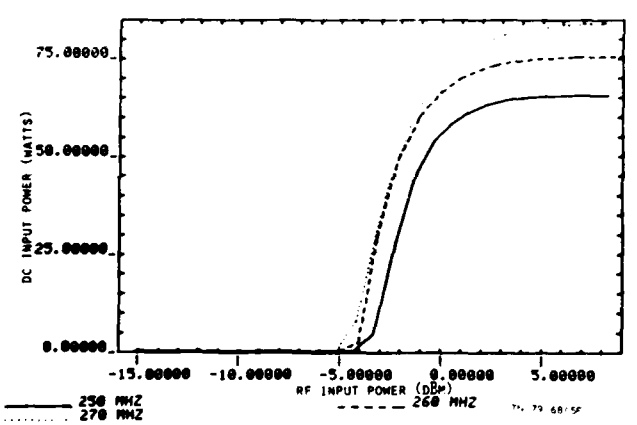
Fig. 5(a-c). Transmitter performance vs r.f. input level and frequency at -40 DEG C.



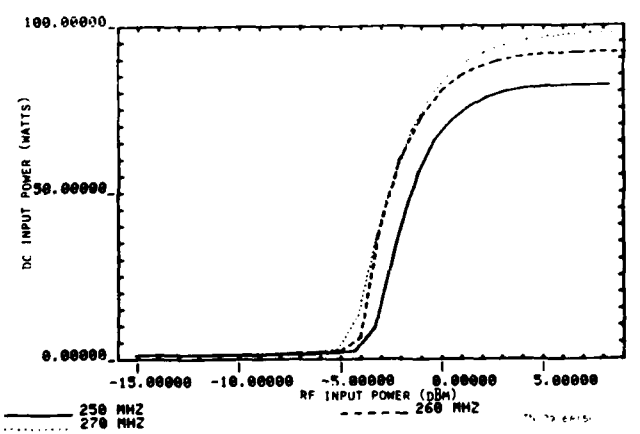
(d) Collector efficiency



(e) Overall efficiency

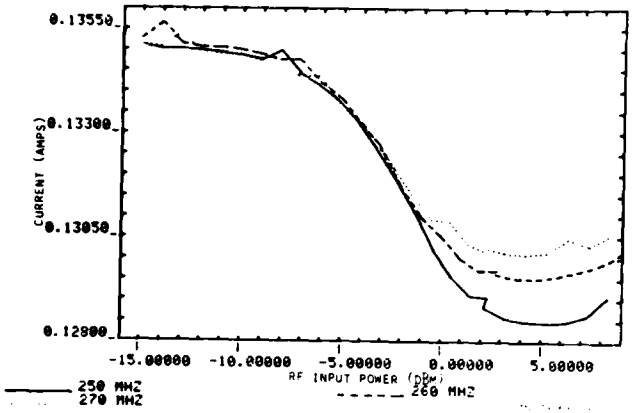


(f) DC input power to final amplifier

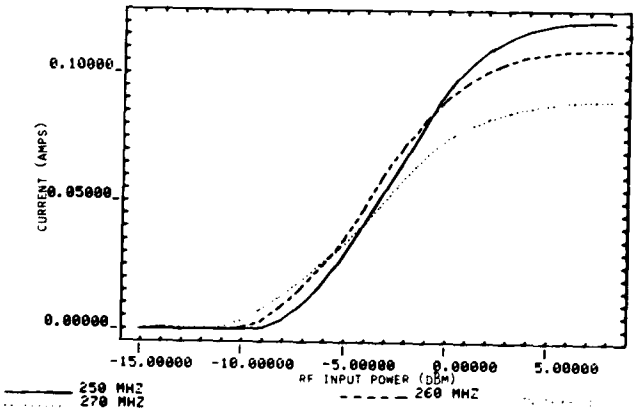


(g) DC input power to transmitter

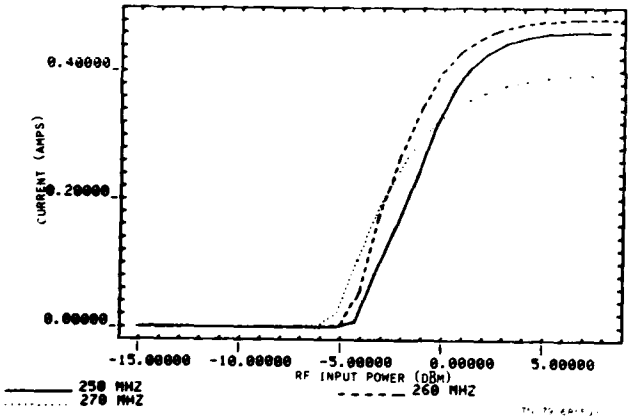
Fig. 5(d-g). Transmitter performance vs r.f. input level and frequency at -40 DEG C.



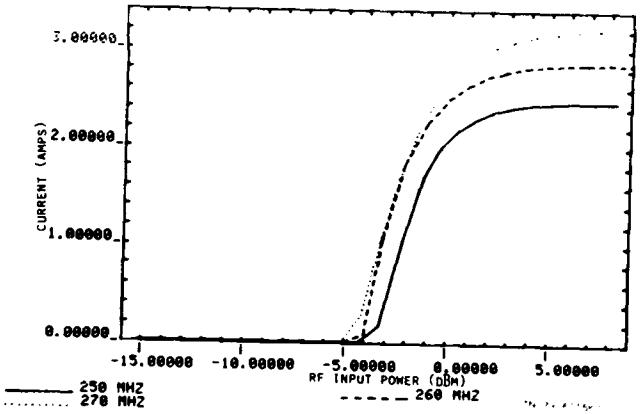
(h) DC current to preamp



(i) DC current to 1-watt stage

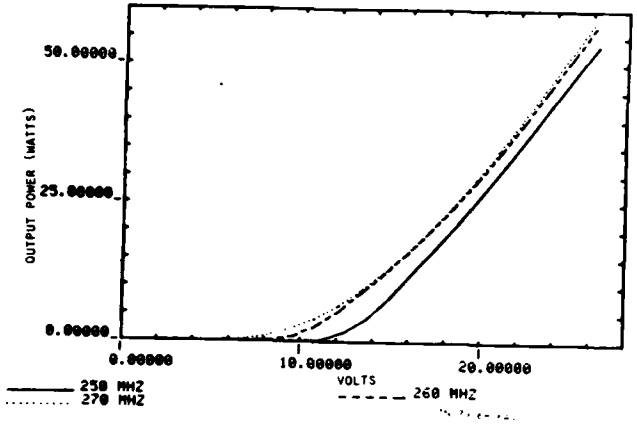


(j) DC current to 10-watt stage

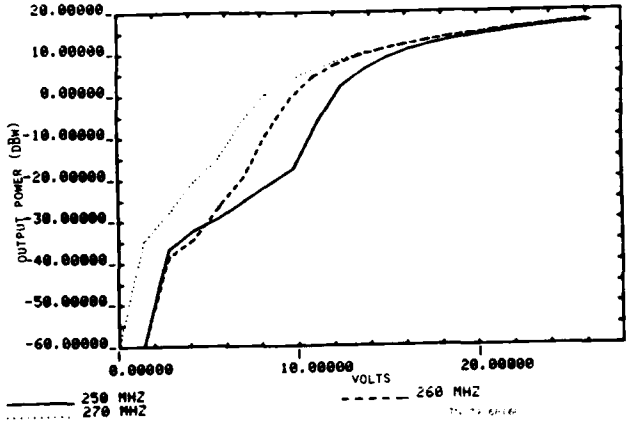


(k) DC current to final amplifier

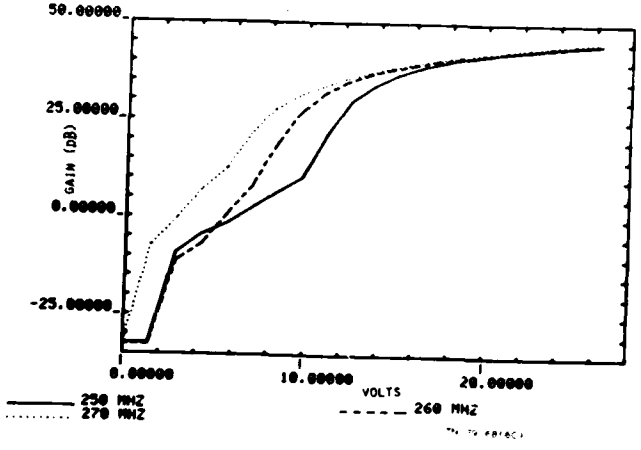
Fig. 5(h-k). Transmitter performance vs r.f. input level and frequency at -40 DEG C.



(a) Output power (watts)

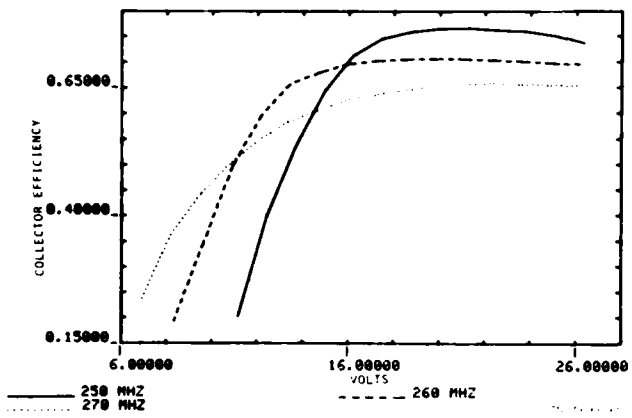


(b) Output power (dBW)

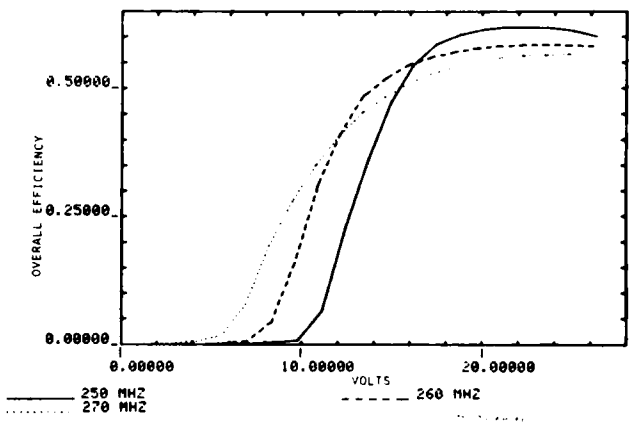


(c) Gain (dB)

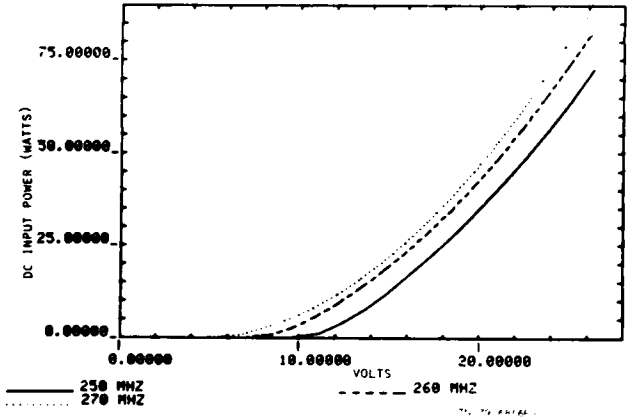
Fig. 6(a-c). Transmitter performance vs 28-volt supply voltage and frequency at 25 DEG C.



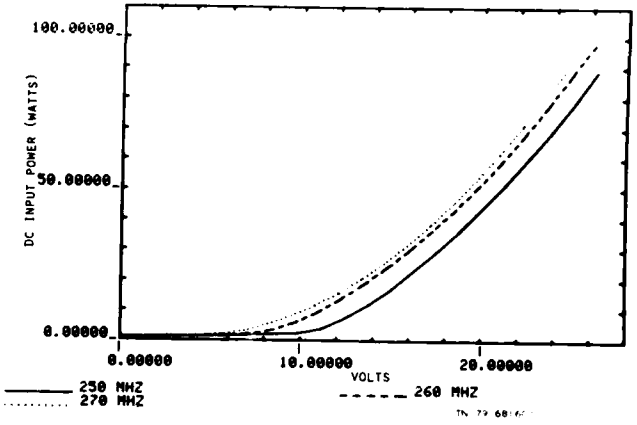
(d) Collector efficiency



(e) Overall efficiency

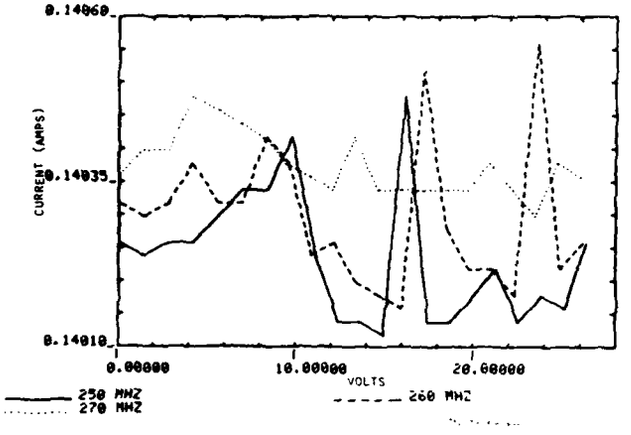


(f) DC input power to final amplifier

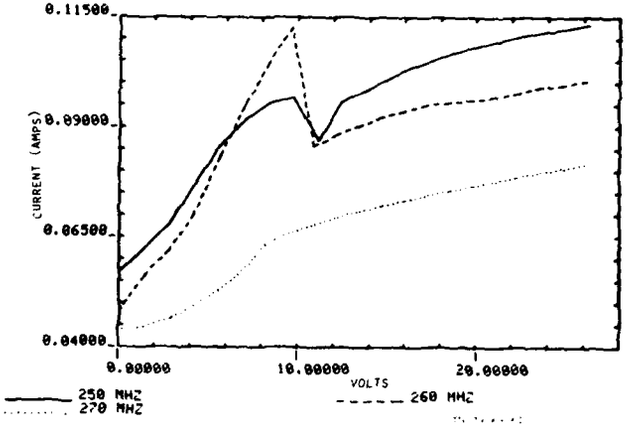


(g) DC input power to transmitter

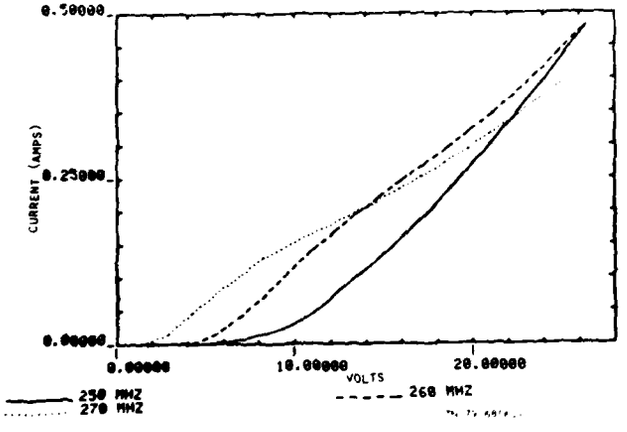
Fig. 6(d-g). Transmitter performance vs 28-volt supply voltage and frequency at 25 DEG C.



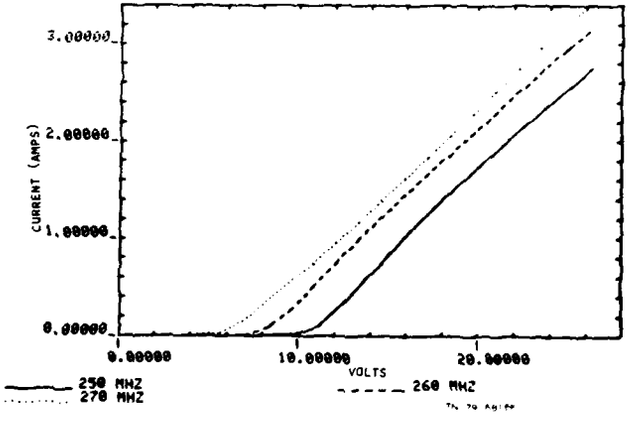
(h) DC current to preamp



(i) DC current to 1-watt stage

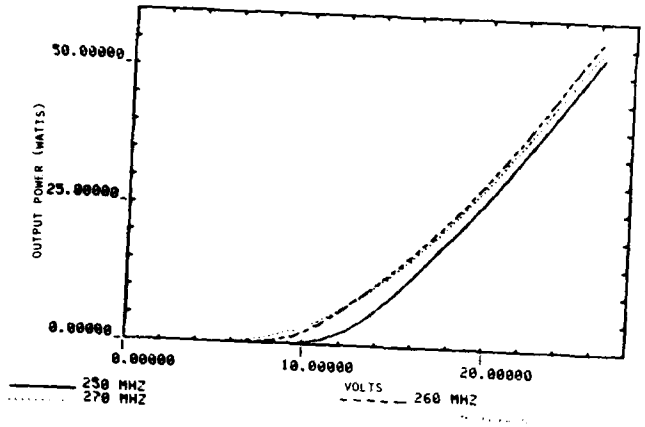


(j) DC current to 10-watt stage

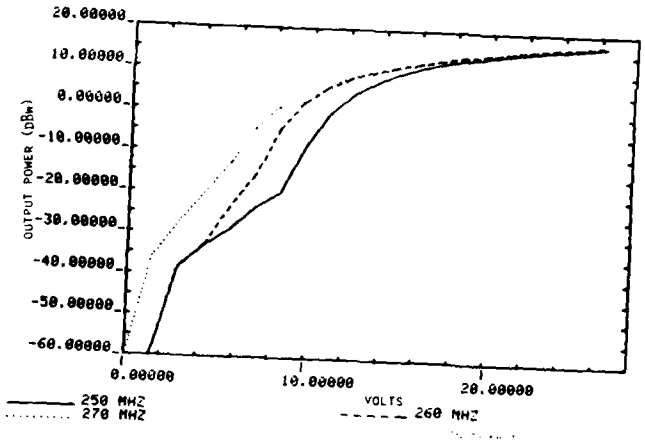


(k) DC current to final amplifier

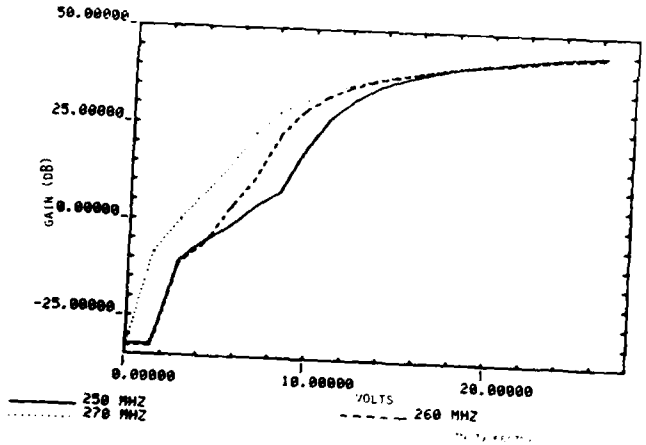
Fig. 6(h-j). Transmitter performance vs 28-volt supply voltage and frequency at 25 DEG C.



(a) Output power (watts)

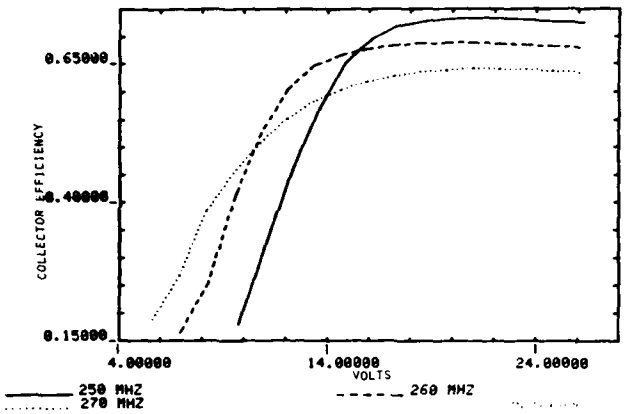


(b) Output power (dBW)

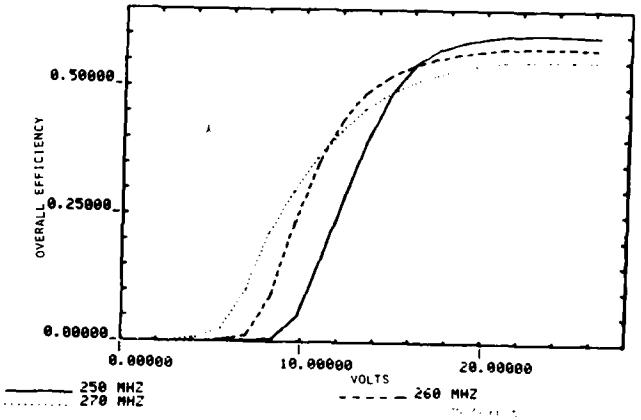


(c) Gain (dB)

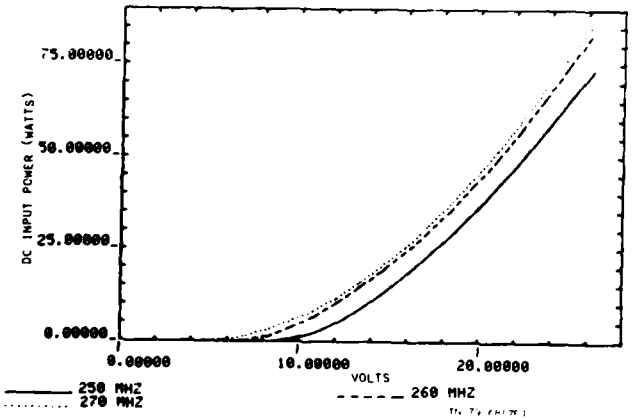
Fig. 7(a-c). Transmitter performance vs 28-volt supply voltage and frequency at 60 DEG C.



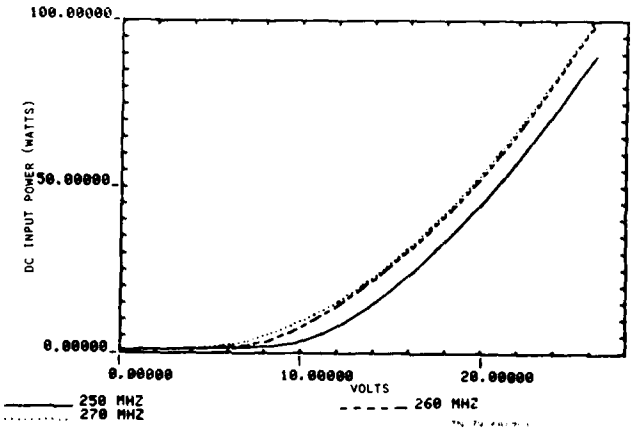
(d) Collector efficiency



(e) Overall efficiency

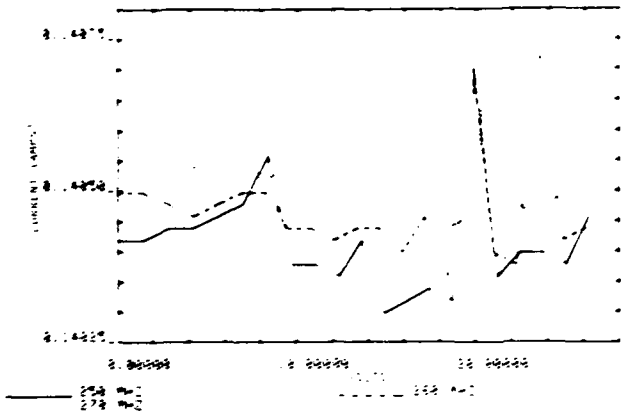


(f) DC input power to final amplifier

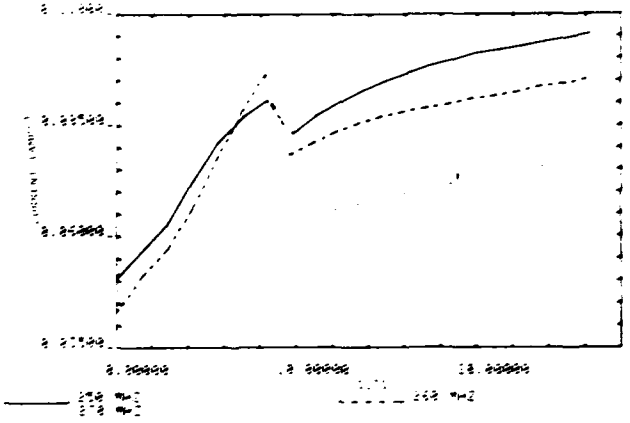


(g) DC input power to transmitter

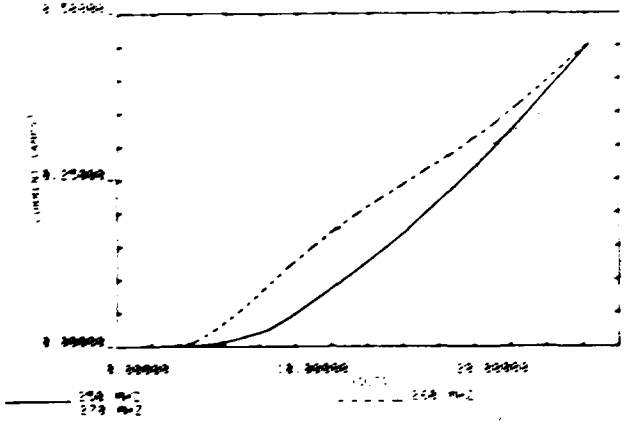
Fig. 7(d-g). Transmitter performance vs 28-volt supply voltage and frequency at 60 DEG C.



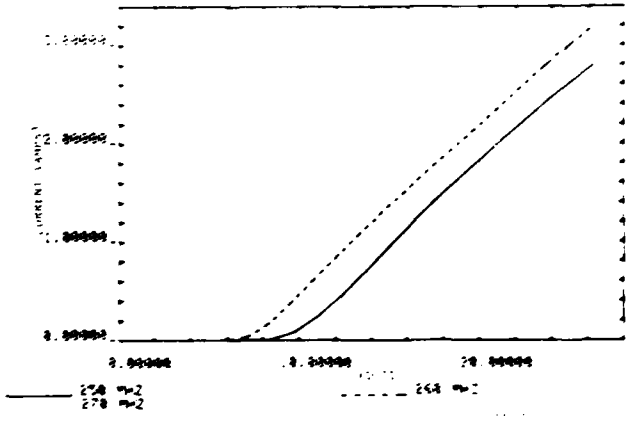
(h) DC current to preamp



(i) DC current to 1-watt stage

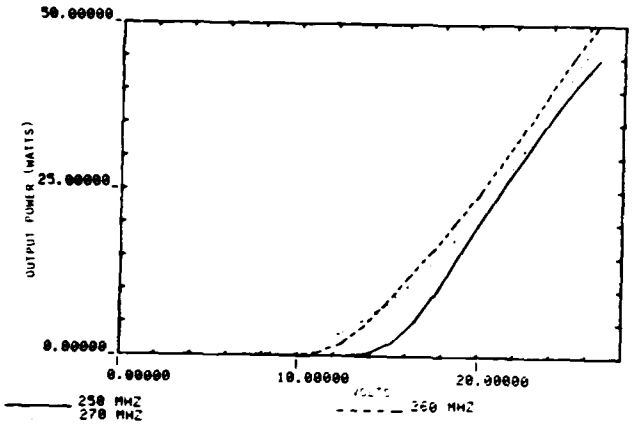


(j) DC current to 10-watt stage

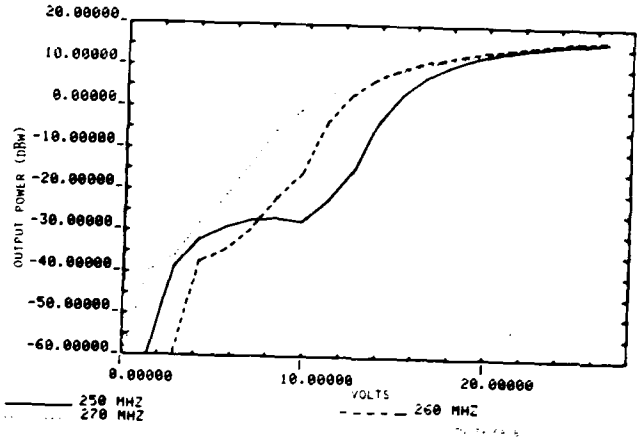


(k) DC current to final amplifier

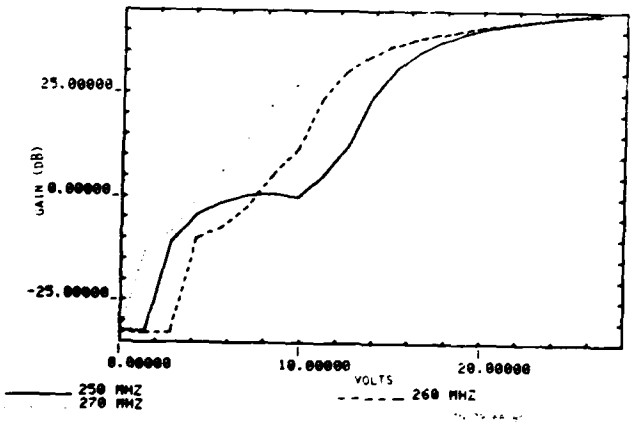
Fig. 7(h-k). Transmitter performance vs 28-volt supply voltage and frequency at 60 DEG C.



(a) Output power (watts)

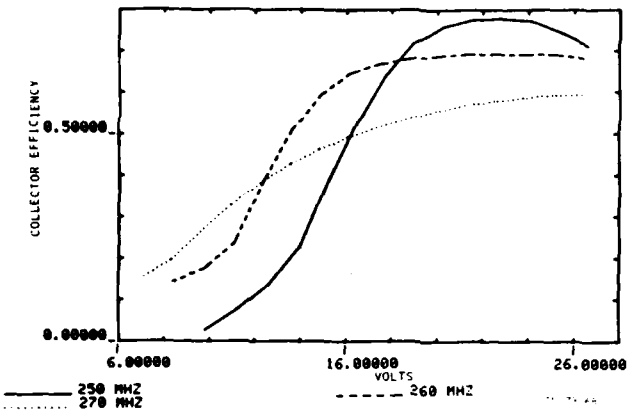


(b) Output power (dBW)

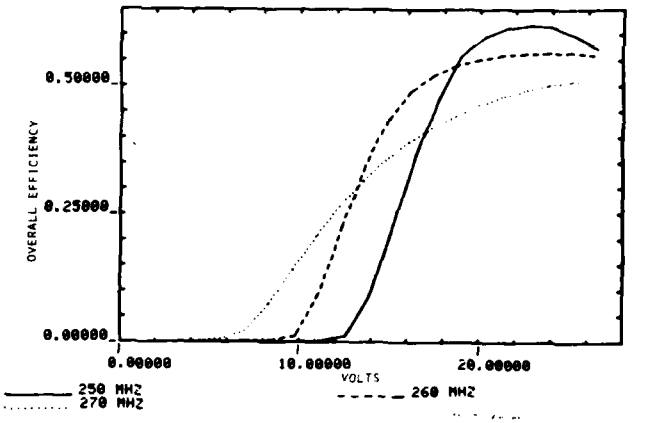


(c) Gain (dB)

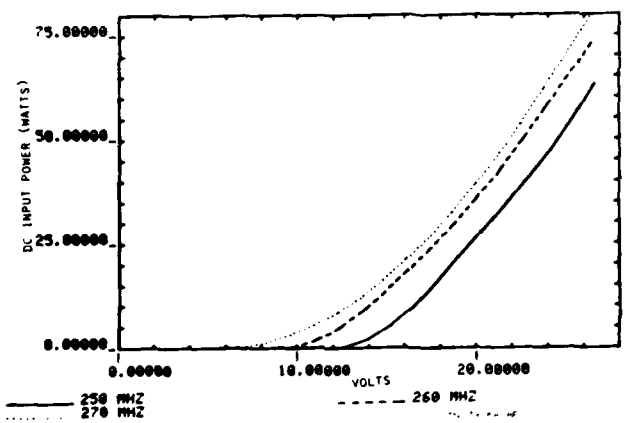
Fig. 8(a-c). Transmitter performance vs 28-volt supply voltage and frequency at -40 DEG C.



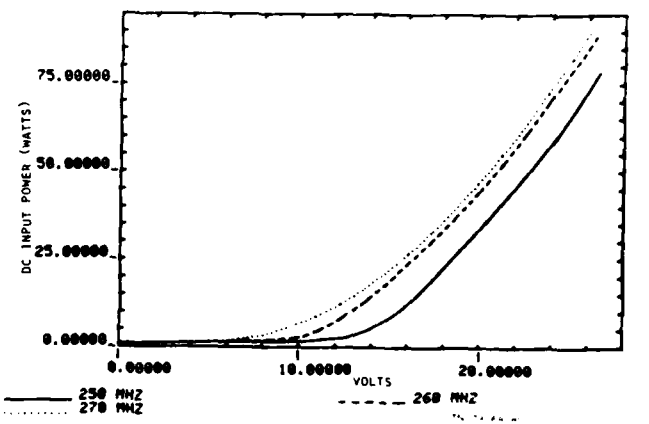
(d) Collector efficiency



(e) Overall efficiency

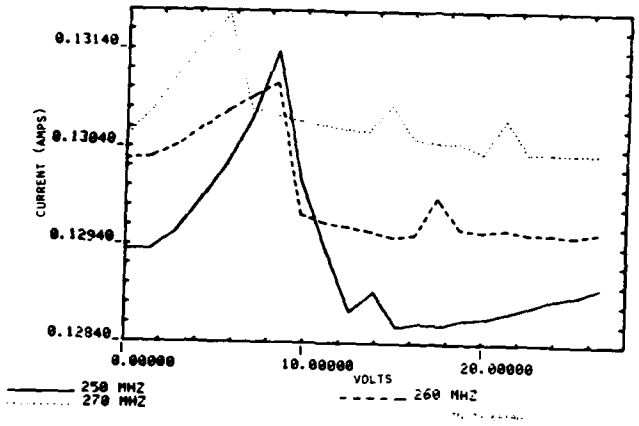


(f) DC input power to final amplifier

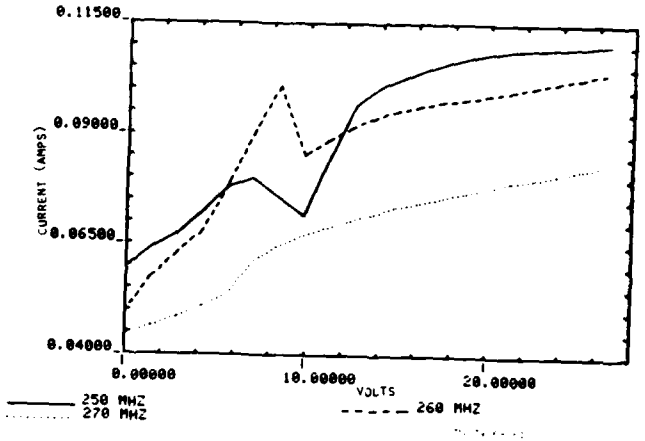


(g) DC input power to transmitter

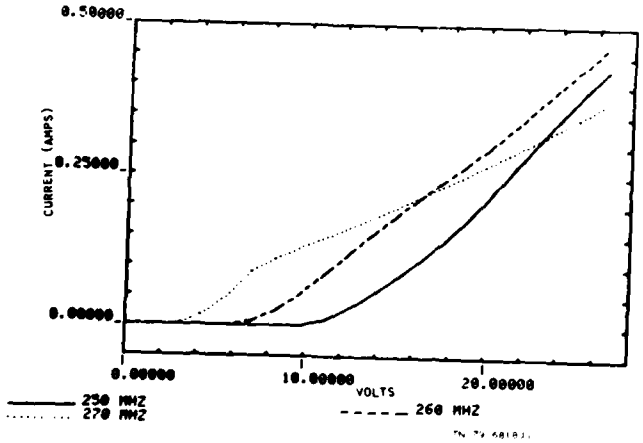
Fig. 8(d-g). Transmitter performance vs 28-volt supply voltage and frequency at -40 DEG C.



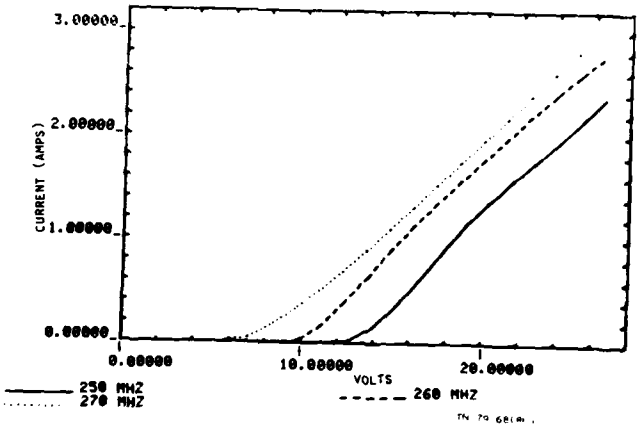
(h) DC current to preamp



(i) DC current to 1-watt stage

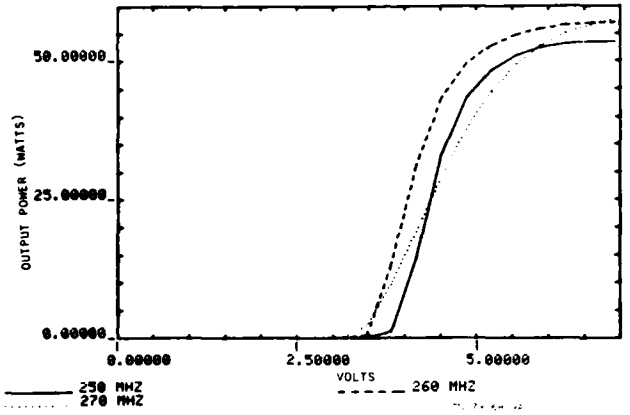


(j) DC current to 10-watt stage

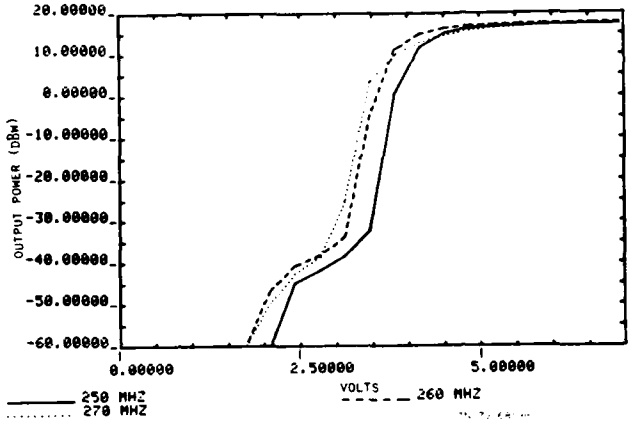


(k) DC current to final amplifier

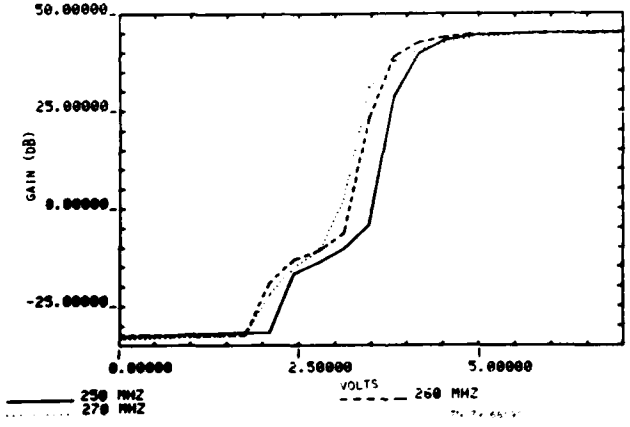
Fig. 8(h-k). Transmitter performance vs 28-volt supply voltage and frequency at -40 DEG C.



(a) Output power (watts)

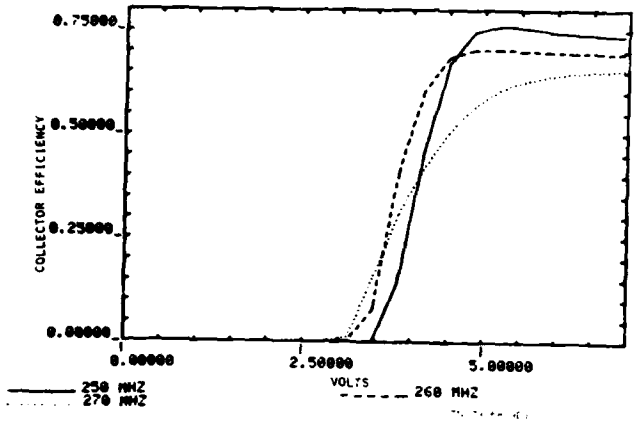


(b) Output power (dBW)

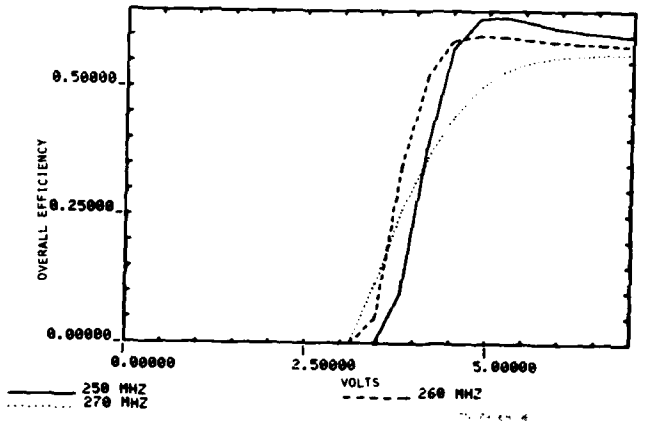


(c) Gain (dB)

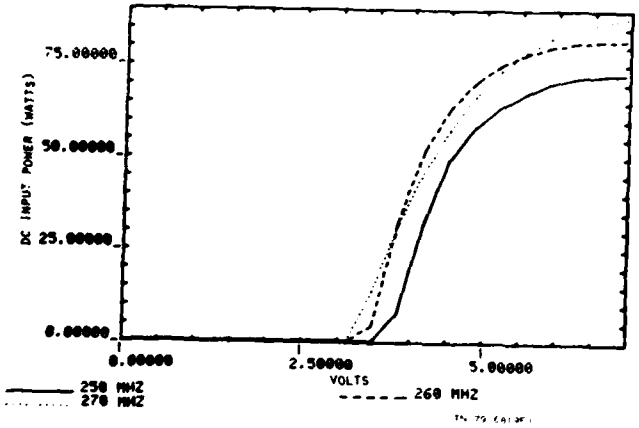
Fig. 9(a-c). Transmitter performance vs 7-volt supply voltage and frequency at 25 DEG C.



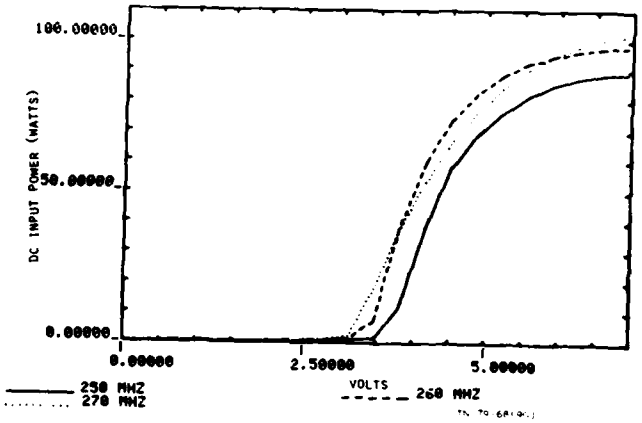
(d) Collector efficiency



(e) Overall efficiency

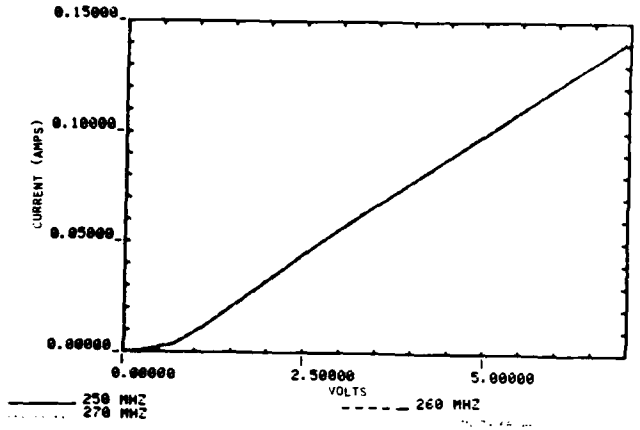


(f) DC input power to final amplifier

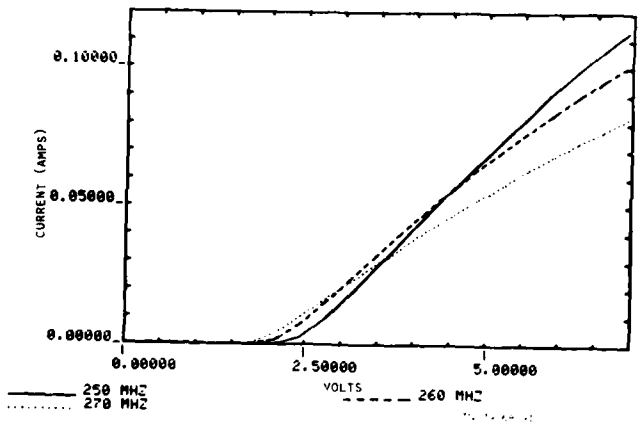


(g) DC input power to transmitter

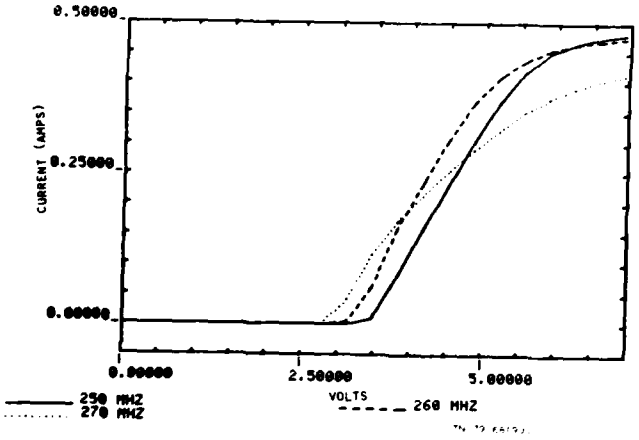
Fig. 9(d-g). Transmitter performance vs 7-volt supply voltage and frequency at 25 DEG C.



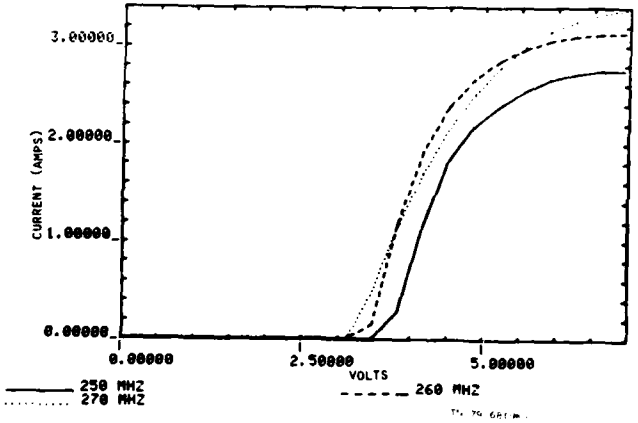
(h) DC current to preamp



(i) DC current to 1-watt stage

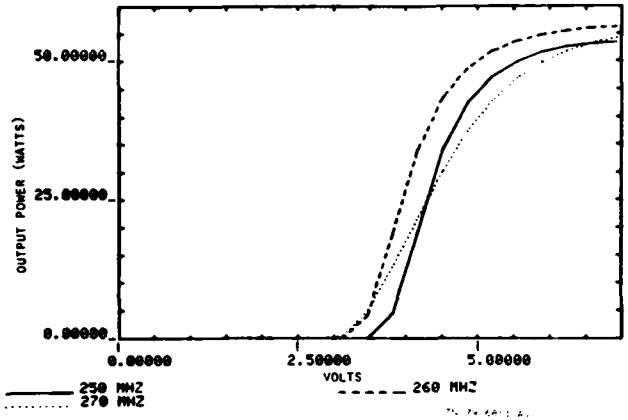


(j) DC current to 10-watt stage

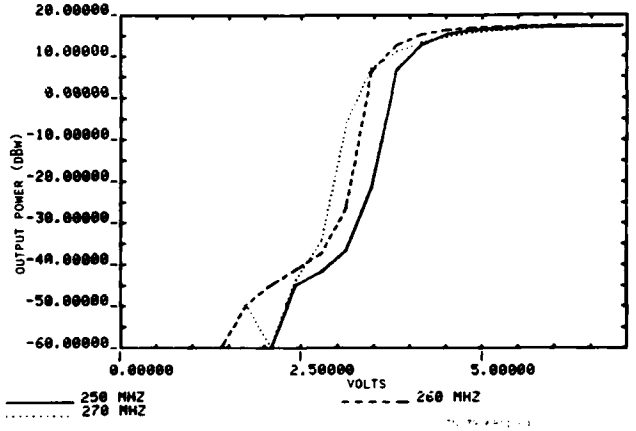


(k) DC current to final amplifier

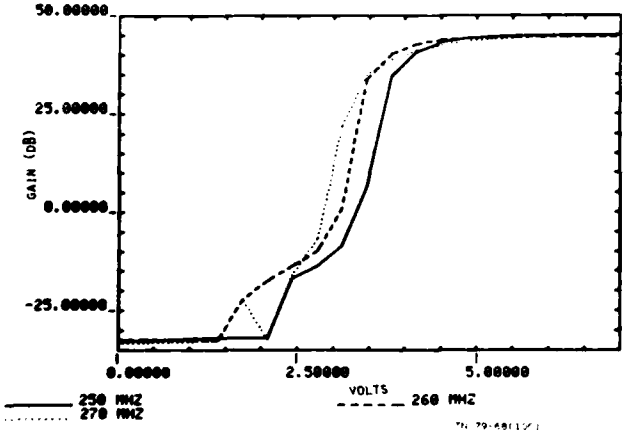
Fig. 9(h-k). Transmitter performance vs 7-volt supply voltage and frequency at 25 DEG C.



(a) Output power (watts)

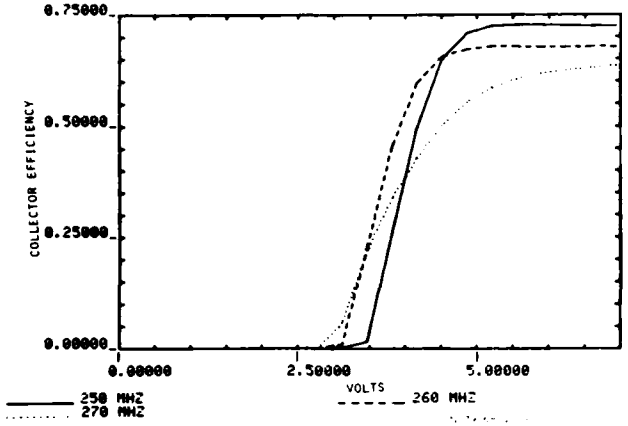


(b) Output power (dBW)

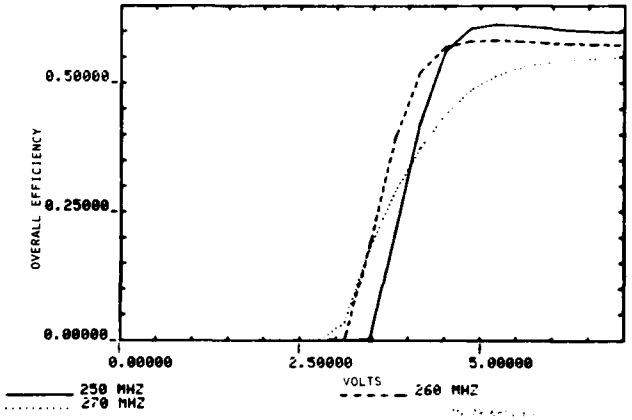


(c) Gain (dB)

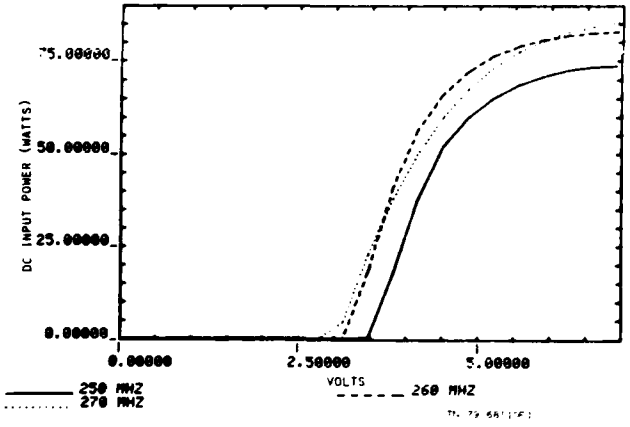
Fig. 10(a-c). Transmitter performance vs 7-volt supply voltage and frequency at 60 DEG C.



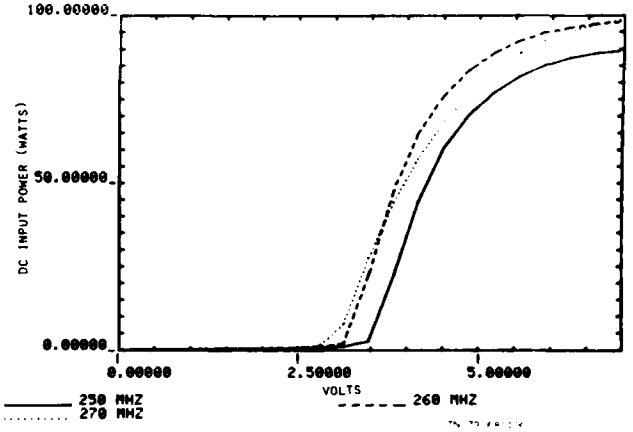
(d) Collector efficiency



(e) Overall efficiency

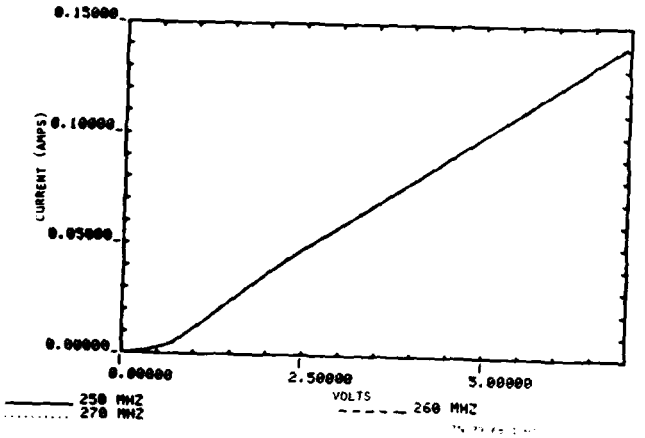


(f) DC input power to final amplifier

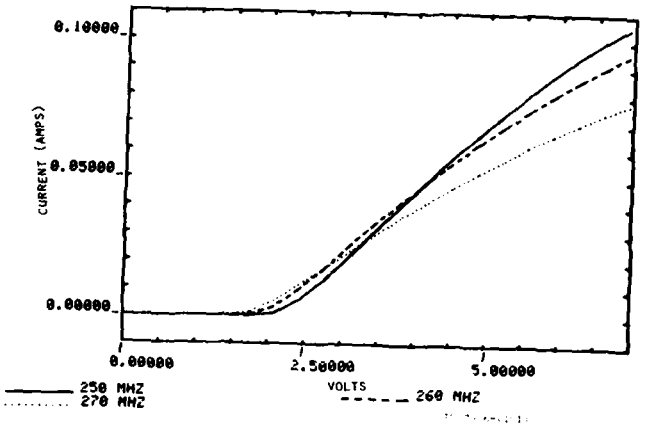


(g) DC input power to transmitter

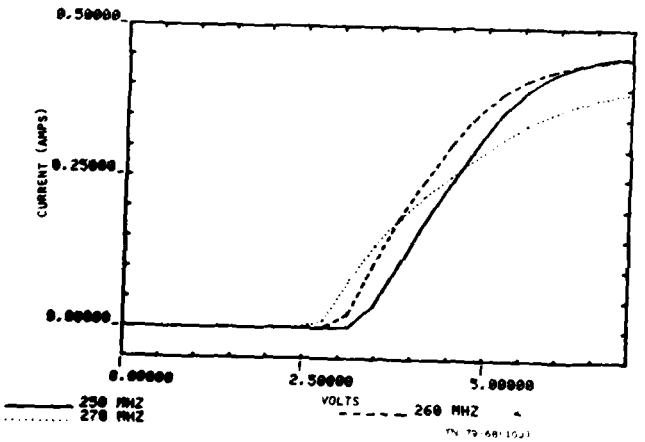
Fig. 10(d-g). Transmitter performance vs 7-volt supply voltage and frequency at 60 DEG C.



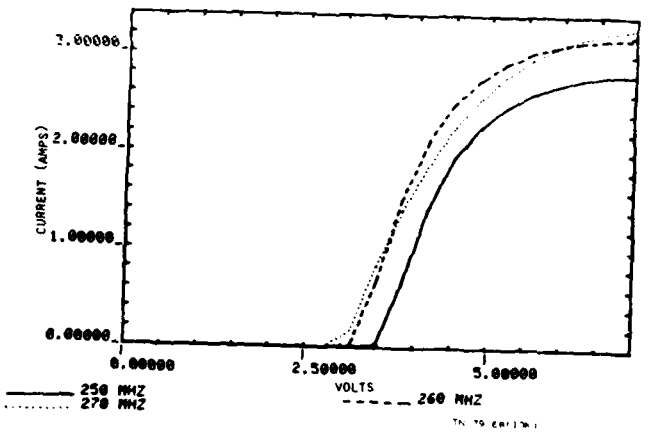
(h) DC current to preamp



(i) DC current to 1-watt stage

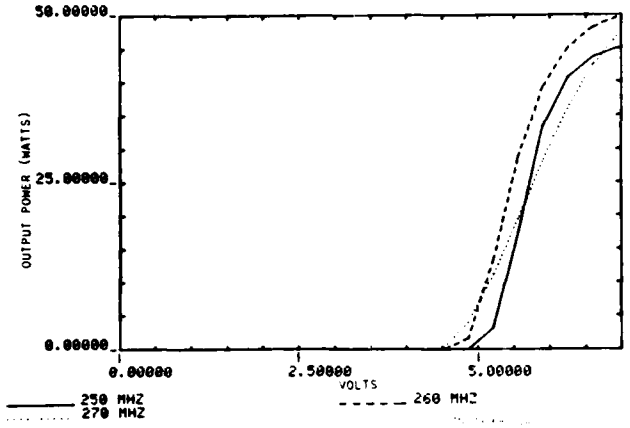


(j) DC current to 10-watt stage

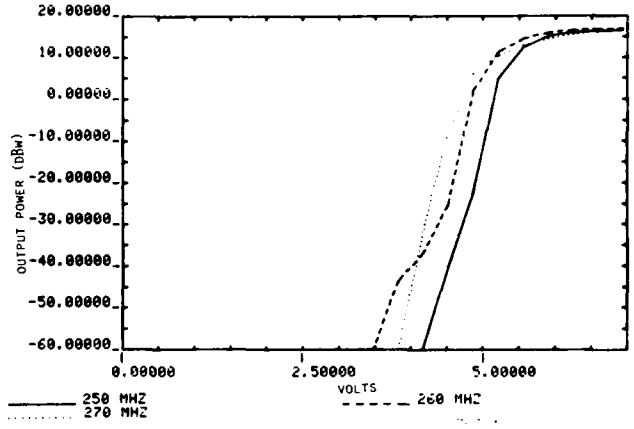


(k) DC current to final amplifier

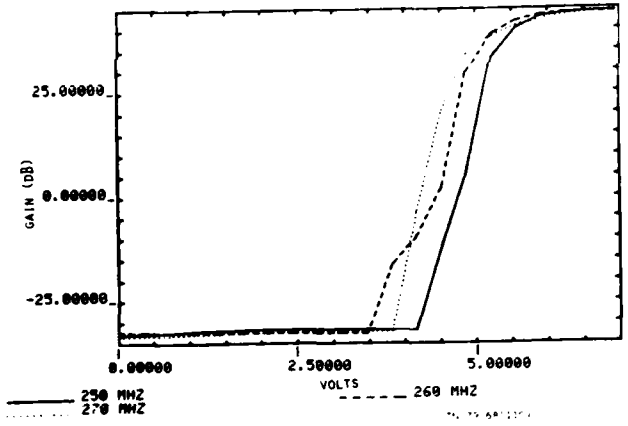
Fig. 10(h-k). Transmitter performance vs 7-volt supply voltage and frequency at 60 DEG C.



(a) Output power (watts)

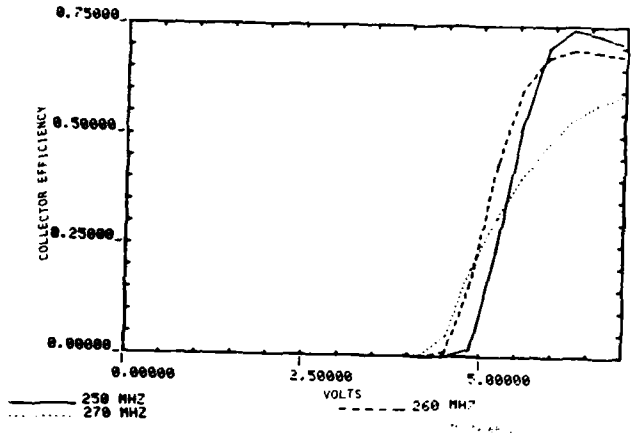


(b) Output power (dBW)

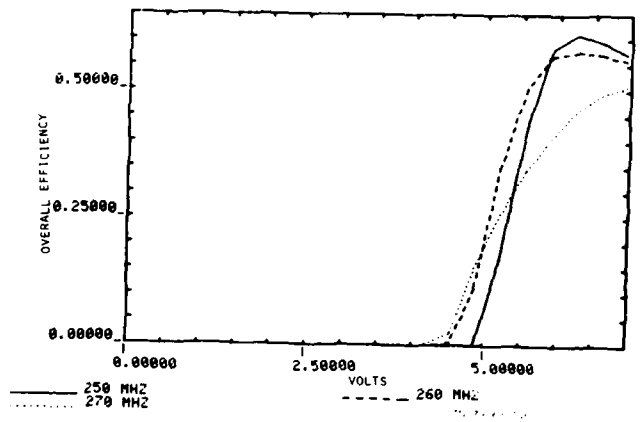


(c) Gain (dB)

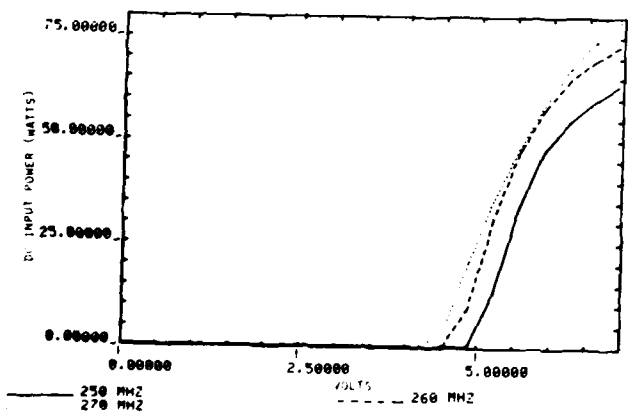
Fig. 11(a-c). Transmitter performance vs 7-volt supply voltage and frequency at -40 DEG C.



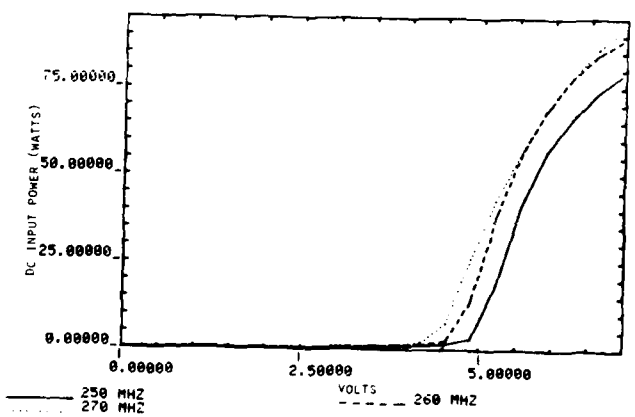
(d) Collector efficiency



(e) Overall efficiency

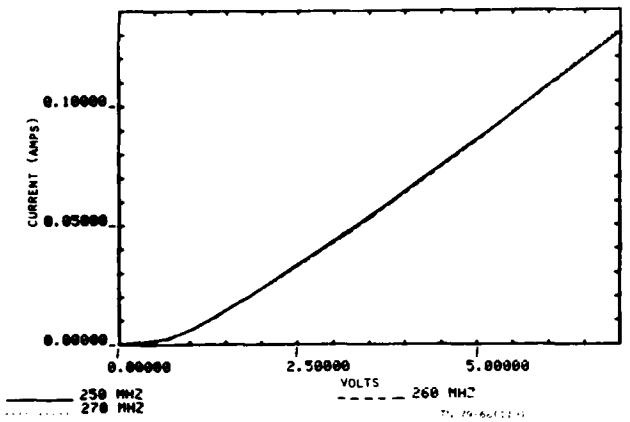


(f) DC input power to final amplifier

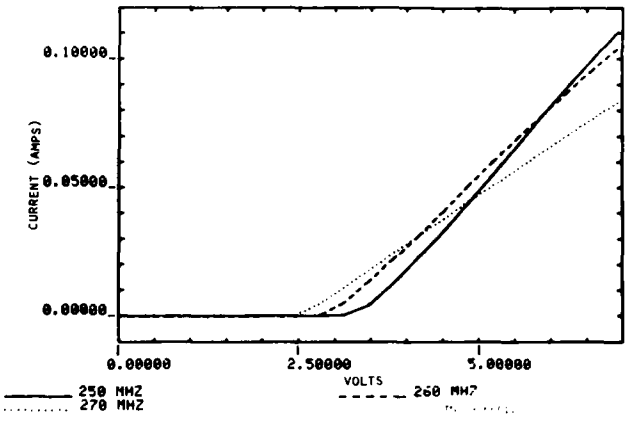


(g) DC input power to transmitter

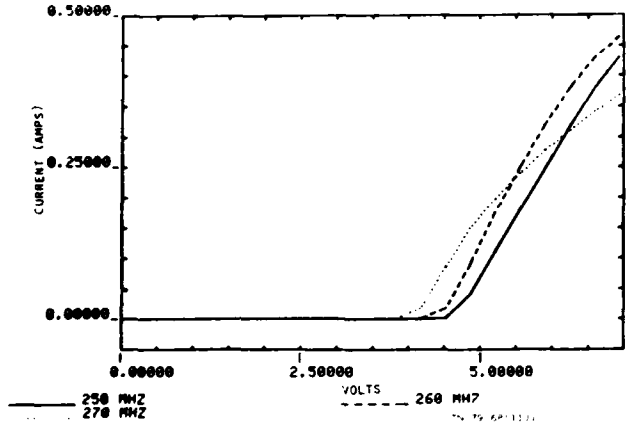
Fig. 11(d-g). Transmitter performance vs 7-volt supply voltage and frequency at -40 DEG C.



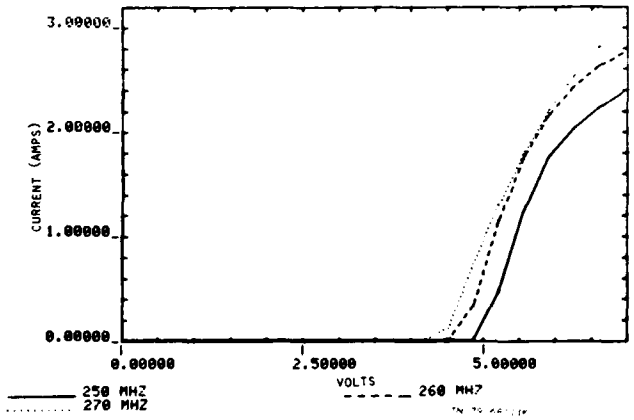
(h) DC current to preamp



(i) DC current to 1-watt stage



(j) DC current to 10-watt stage



(k) DC current to final amplifier

Fig. 11(h-k). Transmitter performance vs 7-volt supply voltage and frequency at -40 DEG C.

APPENDIX B

DERIVATION OF FEEDBACK-AMPLIFIER DESIGN EQUATIONS

The following equations can be written from the model shown in Fig. 9b. The gain, defined as $\frac{V_{OUT}}{V_{IN}}$, is derived as follows:

$$V_{IN} = (1 + \beta)\ I_b R_E \tag{B-1}$$

$$V_{OUT} = -I_{OUT} \cdot R_L \tag{B-2}$$

from Eq. B-1

$$I_b = \frac{V_{IN}}{(1 + \beta)R_E} \tag{B-3}$$

from Eq. B-2

$$I_{OUT} = -\frac{V_{OUT}}{R_L} \tag{B-4}$$

$$I_F = \frac{V_{OUT} - V_{IN}}{R_F} \tag{B-5}$$

$$I_F = I_{OUT} - \beta Ib \tag{B-6}$$

Combining Eqs. B-3, B-4, B-5, and B-6

$$\frac{V_{OUT} - V_{IN}}{R_F} = -\frac{V_{OUT}}{R_L} - \frac{\beta\ V_{IN}}{(1+\beta)R_E} \tag{B-7}$$

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{R_E - \alpha R_F}{R_L + R_F}\right) \cdot \left(\frac{R_L}{R_E}\right) \qquad \text{(B-8)}$$

where $\alpha = \frac{\beta}{1 + \beta}$

The input impedance is defined as:

$$Z_{IN} = \frac{V_{IN}}{I_{IN}} \qquad \text{(B-9)}$$

From Fig. 9b,

$$I_{IN} = I_b - I_F \qquad \text{(B-10)}$$

from Eqs. B-3 and B-5

$$I_{IN} = \frac{V_{IN}}{(I + \beta)R_E} - \frac{V_{OUT} - V_{IN}}{R_F} \qquad \text{(B-11)}$$

$$I_{IN} = V_{IN}\left(\frac{1}{(1 + \beta)R_E} + \frac{1}{R_F}\right) - \frac{V_{OUT}}{R_F} \qquad \text{(B-12)}$$

rewriting Eq. B-8

$$V_{OUT} = V_{IN}\left(\frac{R_E - \alpha R_F}{R_L + R_F}\right) \cdot \frac{R_L}{R_E}$$

substituting this value of V_{OUT} into Eq. B-12

$$I_{IN} = V_{IN}\left(\frac{1}{(1 + \beta)R_E} + \frac{1}{R_F}\left(1 - \frac{R_E - \alpha R_F}{R_L + R_F} \cdot \frac{R_L}{R_E}\right)\right) \qquad \text{(B-13)}$$

$$Z_{IN} = \frac{(1 + \beta)\ R_E\ (R_L + R_F)}{(1 + \beta)(R_L + R_E) + R_F} \qquad \text{(B-14)}$$

The output impedance is defined as:

$$Z_{OUT} = \frac{V_{OUT}}{I_{OUT}} \qquad \text{(B-15)}$$

Z_{OUT} is determined by replacing R_L in Fig. 9b with a voltage source, V_{OUT}, and setting $V_S = 0$.

$$I_{OUT} = I_F + \beta I_b \qquad \text{(B-16)}$$

$$V_{IN} = (I_F - I_b)R_S \qquad \text{(B-17)}$$

Substituting Eq. B-17 into Eq. B-5

$$I_F = \frac{V_{OUT}}{R_F} - (I_F - I_b)\frac{R_S}{R_F} \qquad \text{(B-18)}$$

$$I_F = \frac{V_{OUT}}{R_F + R_S} + \frac{I_b R_S}{R_F + R_S} \qquad \text{(B-19)}$$

From Eqs. B-3 and B-17

$$I_b = \frac{R_S}{(1 + \beta)R_E + R_S}\ I_F \qquad \text{(B-20)}$$

substituting Eq. B-20 in Eq. B-19 and solving for I_F:

$$I_F = V_{OUT} \cdot \frac{(1 + \beta)R_E + R_S}{(1 + \beta)R_E R_F + ((1 + \beta)R_E + R_F)R_S} \qquad \text{(B-21)}$$

substituting Eq. B-20 into Eq. B-16

$$I_{OUT} = \left(1 + \frac{\beta R_S}{(1 + \beta)R_E + R_S}\right) I_F \qquad \text{(B-22)}$$

substituting Eq. B-21 into Eq. B-22:

$$Z_{OUT} = \frac{(1 + \beta)R_E(R_F + R_S) + R_F R_S}{(1 + \beta)(R_E + R_S)} \qquad \text{(B-23)}$$

if $\beta \to \infty$, Eqs. B-8, B-14, and B-23 reduce to:

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{R_E - R_F}{R_L + R_F}\right) \cdot \left(\frac{R_L}{R_E}\right) \qquad \text{(B-24)}$$

$$Z_{IN} = \frac{R_E(R_L + R_F)}{R_L + R_E} \qquad \text{(B-25)}$$

$$Z_{OUT} = \frac{R_E(R_S + R_F)}{R_E + R_S} \qquad \text{(B-26)}$$

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amplifier

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This note describes the design, construction, and performance of a 50 W UHF satellite transmitter which was built to demonstrate design and construction techniques that lead to easy replication of circuits in a manufacturing environment, without sacrifice in performance. High-efficiency performance is demonstrated over a 20 MHz band, centered at 260 MHz, with a fixed-tuned, single-ended design.

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