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MONOLITHIC INTEGRATION OF MICROWAVE GAAS POWER FETS.(U)
NOV 79 V SOKOLOV, R E WILLIAMS N00014-77-C-0657

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MONOLITHIC INTEGRATION OF MICROWAVE GaAs POWER FETs

Texas Instruments Incorporated
Central Research Laboratories
13500 North Central Expressway
Dallas, Texas 75265

November 1979

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20. ABSTRACT (*Continue on reverse side if necessary and identify by block number*)

Efforts during the second year of this contract have included investigations of monolithic integration of GaAs power field effect transistors (FETs) at X-band microwave frequencies and incorporation of on-chip matching using lumped elements and coplanar ground metallization for monolithic FET circuit design. Two monolithic circuits have been investigated - a push-pull two-stage amplifier on a 2.0 x 2.0 mm chip, and a three-transistor paraphase amplifier on a 2.0 x 2.4 mm chip. Results for the two-stage push-pull amplifier include

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1.4 W with 12.4 dB gain at 9.0 GHz. To provide the necessary 180° out-of-phase signals for the push-pull devices, 180° hybrid rings fabricated on alumina substrates are used. Fabrication of the paraphase amplifier, which is intended to replace the input 180° hybrid ring, and preliminary evaluation of these chips have also been done.

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SECTION I
INTRODUCTION

This report covers the progress made during the second year (Phase II) of a continuing research program for the monolithic integration of microwave GaAs power field effect transistors (FETs) under Contract No. N00014-77-C-0657. The objective of this program is to demonstrate the feasibility of monolithic GaAs microwave integrated amplifier circuits utilizing power FETs in X-band.

During the first year of this program, a two-stage push-pull FET power amplifier was designed that incorporated four transistors on a single 2.0 mm x 2.0 mm x 0.1 mm GaAs chip. This chip was designed so that it could be cleaved in half and only the first stage tested. At the end of the first year the first stage (consisting of a pair of 600 μm FETs) yielded a small signal gain of 8 dB and a power output of 760 mW with an associated gain of 4.7 dB at 9.5 GHz. This was the first reported monolithic, power FET amplifier at X-band. Much of the Phase I work was also concerned with laying the groundwork for monolithic fabrication, assembly, and testing.

The objectives for Phase II were to (1) complete testing and optimization of the monolithic single-stage and two-stage push-pull amplifier, (2) continue improving and evaluating monolithic component and fabrication techniques, and (3) develop and perform a preliminary evaluation of a monolithic paraphase amplifier, or "active balun," that would interface with the input of the two-stage push-pull chip. The paraphase amplifier has a single 50 Ω unbalanced transmission line input and a 100 Ω balanced line output; it incorporates three monolithically fabricated FETs.

In addition to Phase II, work was also initiated on developing a fully integrated monolithic push-pull FET device as part of a program expansion effort. The objective of this work is to take advantage of the push-pull mode of operation in reducing the effective source lead inductance between push-pull transistor cells and thereby increase the power and gain capability of the FET over that of a conventionally operated device having the same total gate width.

Among the accomplishments made during the second phase are the following:

- Monolithic two-stage push-pull amplifiers were evaluated from several slices and yielded output powers between 1 W and 1.3 W with at least 10 dB gain in the 8 to 9.5 GHz frequency range. Operated with short duration, low duty cycle pulses, such an amplifier yielded 1.5 W with 12 dB gain at 9.0 GHz.

- Fabrication improvements included: (1) The introduction of plated "air-bridge" source interconnects on all the FETs incorporated on the monolithic chips. (2) Improved fabrication of monolithic overlay type capacitors used for rf tuning and rf bypass, which has resulted in higher yield and reproducibility of these components. Capacitors with values between 1 pF and 8 pF have been fabricated. Typical Q values of 30 have been measured at 5 GHz. (3) Improved chip mounting techniques have increased the yield of devices for rf evaluation and have virtually eliminated the cracking of the GaAs chips due to soldering-induced stresses.

- A monolithic FET paraphase amplifier was designed and fabricated. This chip is also 2.0 mm x 2.0 mm and incorporates three power FETs. Preliminary evaluation of this monolithic chip from the first processed slice has shown balun action at 9.5 GHz with 3 dB gain under small signal conditions.

- A third mask set, which incorporates fully integrated push-pull FET devices (up to a total gate width of 4.8 mm), has been designed and submitted for mask fabrication.

The rest of this report is organized according to the key accomplishments listed above. Section II discusses the fabrication improvements and evaluation of monolithic components. Sections III and IV discuss the results obtained on the push-pull and paraphase amplifier chips, respectively. Section V describes the design of the fully integrated push-pull devices. Finally, Section VI presents the plans for future work.

SECTION II
FABRICATION AND PROCESSING

Fabrication of monolithic devices largely parallels that of discrete devices. Specific exceptions, such as capacitor formation, are discussed below. All monolithic devices were fabricated on vapor phase epitaxy (VPE) material consisting of an active layer and an undoped buffer layer grown on semi-insulating substrates. Device isolation is achieved by etching mesas. Then the source-drain is defined by lift-off and is alloyed. Part of the source-drain pattern consists of alignment marks to be used by the e-beam machine when defining the gate stripes. These are defined next and are typically between 0.5 and 0.8 μm long. The gates are recessed, and TiPtAu is used for gate metallization. To speed e-beam exposure, only the gate stripes and very small "mini-pads" are defined at this stage. Although this technique is also used on several of our discrete devices, it is particularly useful on monolithic devices where gate "pads" often continue into extensive metallization. The next metallization is TiAu and serves several purposes. Metallization over the source-drain areas acts as a current-spreading layer. Other TiAu metallization overlaps the gate fingers and acts as "gate pad" areas. The monolithic inductors are also defined at this step. The inductors are on a second mask to facilitate changes. Hence, a double exposure, using two masks, is necessary to define this layer. The resist is soaked in Xylene prior to development.[1] This produces an undercut resist profile that facilitates lift-off. This has been found to be especially useful in forming the nearly closed circles of the inductor loops. Next, Si_3N_4 is plasma-deposited over the entire slice. Top capacitor plates are formed on top of this nitride layer at appropriate locations (see subsequent discussion).

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[1] B. J. Canavello, M. Hatzakis, and J. M. Shaw, "Process for Obtaining Undercutting of Photoresist to Facilitate Lift-off," IBM Tech. Disclosure Bull. 19, 4048 (1977)

- Air-Bridge Source Interconnects

Various plating steps follow, which have been formulated to allow fabrication of air-bridge source interconnects. These eliminated the need to stitch-bond the four groups of source pads present on each device. This greatly facilitates the testing and probing required to determine if all transistors on a given device are operable. The plating proceeds as follows: A photoresist pattern in defined with openings over the source pads and all other areas that are to be plated. The exposed nitride is etched away, and the remaining nitride/photoresist forms the plating mask. The exposed areas are plated up to approximately the level of the resist. The resist is left on the slice, and a very thin layer of sputtered gold is applied in a hummer, a process that requires only about five minutes and does not require an evaporator. More resist is applied over the sputtered gold. The bridge pattern is defined over the source pads, exposing the sputtered gold, and this area is plated. All the resist is then dissolved, which lifts off the excess sputtered gold. The dissolving of the first layer of resist produces the air gaps between the slice surface and the bridge. SEM photographs of an air bridge amplifier and close-up views of the bridge are contained in Figures 1 through 3. Finally, the slices are lapped to a thickness of 4 μm, metallized on the back, and scribed.

- Monolithic Capacitors

The capacitors used on the monolithic devices continue to be fabricated using the geometry developed in the first year of the program; which consists esentially of two capacitors in series (Figure 4). Although this technique requires twice the area of a "single" capacitor, it results in an element having a very high yield. This is essentially due to the fact that nitride grows from all surfaces and thus the top plate has no sharp edge to cross over. The only problem that has been encountered with these capacitors occurred on one run when the top plate metallization was mistakenly made very thin. In all other cases, yield has been extremely high.

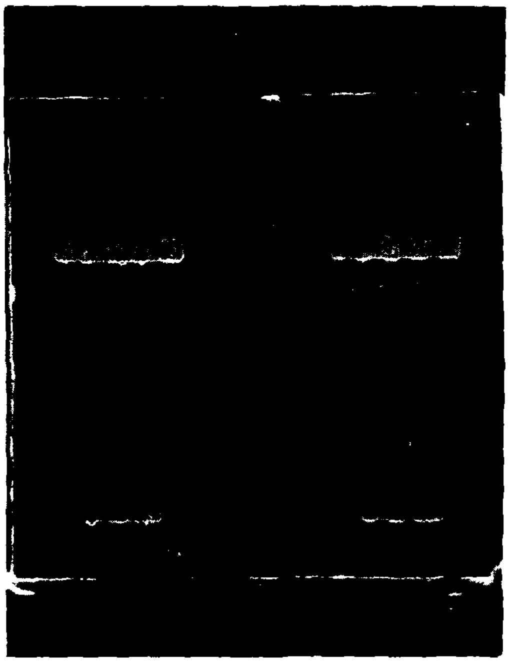


Figure 1 SEM Photograph of a Completed Two-Stage Monolithic Amplifier

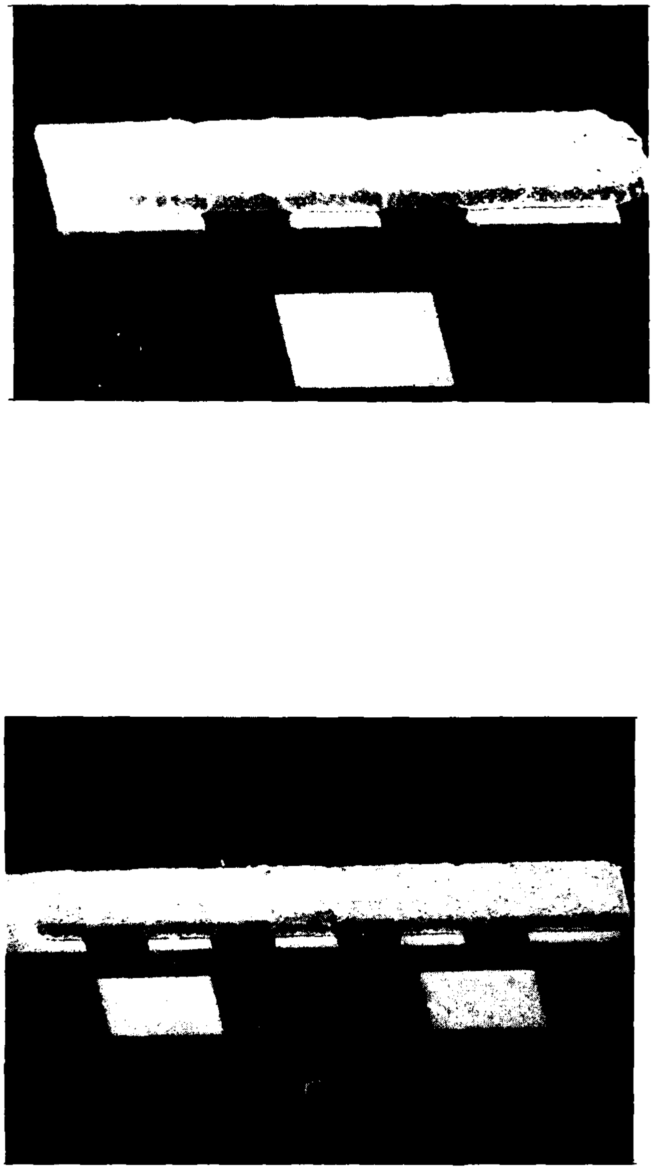


Figure 2 SEM Photograph of the Plated Air Bridges on the First- and Second-Stage Transistors

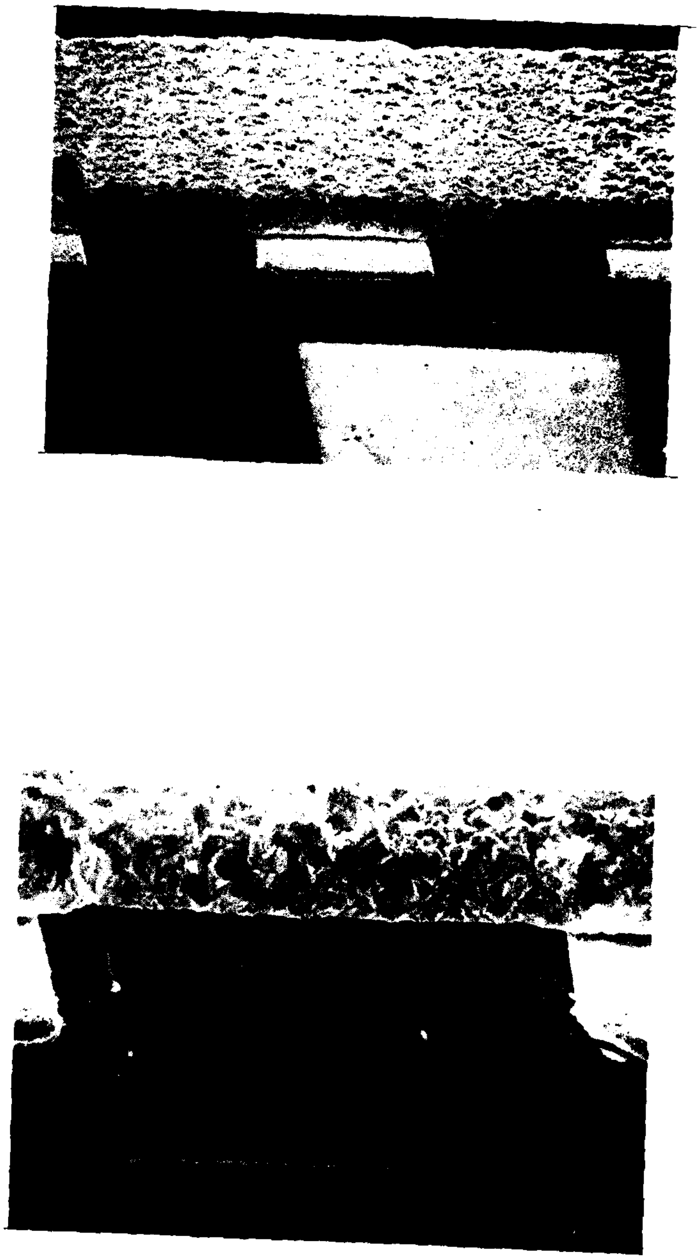


Figure 3 SEM Photographs Showing Regions Where the Gate Stripes Go Under the Air Bridges

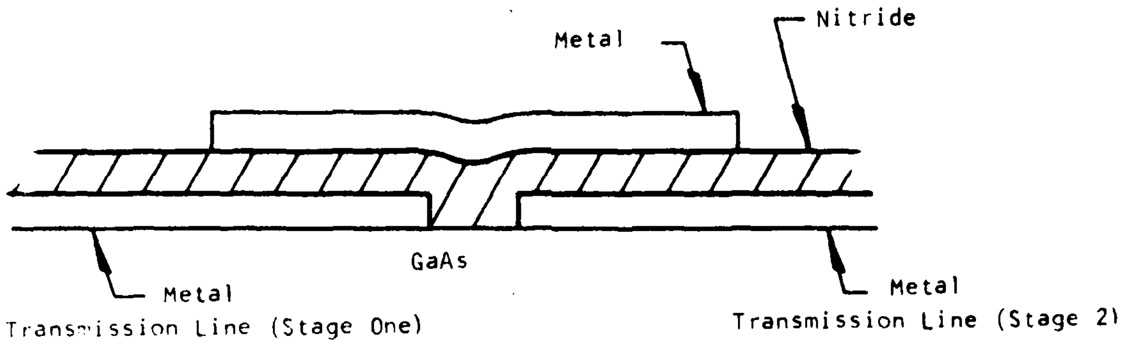


Figure 4 Interstage Monolithic Capacitor (Essentially Two Capacitors in Series)

Aluminum was used initially as the top plate metal, but there appeared to be some adhesion problems. These were not severe enough to prevent the capacitors from being functional, but the definition of the plate was not as crisp and clean as desired. Consequently, all recent slices have used TiAu as the capacitor top plate metallization, and adhesion has been excellent.

The Q's of several capacitors were measured by scribing the capacitors from a chip, bonding them in a standard varactor package, and inserting the package in a section of reduced height waveguide. Bond wire inductance series-resonates the capacitance at microwave frequencies. Knowledge of the transmission loss, the resonant frequency, and the 3 dB bandwidth of resonance determines the microwave series resistance and the Q of the resonant circuit.[2] Q's of approximately 30 at 6 GHz with approximately 1 Ω series resistance were obtained for the capacitors on GaAs. Approximately, Q = 40 was obtained for identical capacitors fabricated on alumina.

- Mounting

Several problems were encountered in properly mounting monolithic devices. These are related to the fact that the chip must be thin for power dissipation (100 μm for these devices), yet the size of the chip is much larger than conventional discrete FETs. The chips are soldered to gold-plated copper pedestals having a surface area approximately the same as the device. (This allows access to all four sides of the chip from the test fixture.) However, virtually all large monolithic devices developed "spontaneous" cracks after mounting. That is, cracks might appear at any time from hours to days after bonding. This severely limited our ability to test such devices. The problem was thought to be caused by thermal stresses developed during cooling

[2] Bernard C. DeLoach "A New Microwave Measurement Technique to Characterize Diodes and an 800-Gc Cutoff Frequency Varactor at Zero Volts Bias," IEEE Trans. Microwave Theory Tech. MTT-12, 15 (1964).

after the large, thin GaAs chip was soldered to the metal block. In fact, several devices were cross-sectioned shortly after having been mounted and revealed cracks that began at the chip/solder interface, but had not yet reached the surface.

In an attempt to correct the problem of chip fracture, a lower melting point solder, 96% Sn/4% Ag (M.P. 217°C), was substituted for the 80% Au/20% Sn (M.P. 280 °C) solder. Used with a small amount of flux, the Sn/Ag alloy wets the chip's back side and the gold-plated mounting block quite well, so that a good solder joint is established with minimum "scrubbing" or pressure applied to the chip. All the devices are now being mounted using the Sn/Ag solder, and no obvious fractures due to soldering-related stresses have been observed.

Experiments have also begun in which solder is evaporated on the back of the slice before scribing, and also onto the mounting blocks. Several solders are being investigated. This technique should improve the uniformity of the joint in thickness and solder coverage, as well as reducing the need for pressure on the thin chip during mounting.

- <u>Yield</u>

The yield-determining elements for the monolithic chips are the FETs. The passive elements, capacitors and inductors, have yields significantly higher than the FETs. Hence, the yield for a given chip varies approximately as the total gate width. If catastrophic failures (which eliminate entire slices) are eliminated, the dc yield of the two-stage, four-transistor amplifier has been 30% or greater.

- <u>Integrated Push-Pull Device (See Section V)</u>

Mask fabrication is currently under way for the integrated push-pull FET device. Figure 5 is a plot of the source-drain geometry. (This computer-generated plot contains some extraneous lines related to the mask fabrication procedure.) Each field will contain a 1200 μm, a 2400 μm, and a

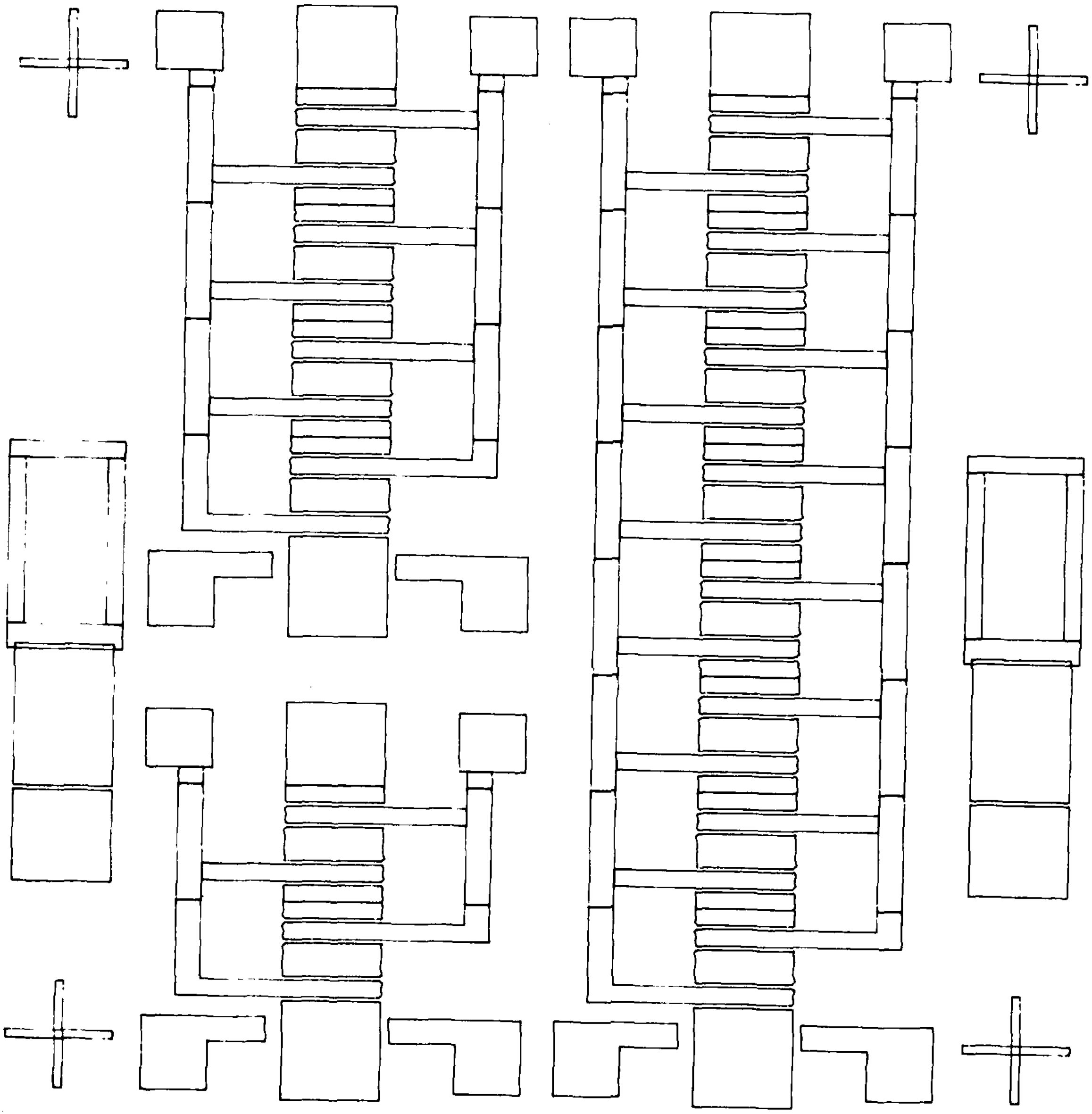


Figure 5 Source-Drain Geometry of the Integrated Push-Pull FET. (This is a computer-generated plot and contains extraneous lines that are a result of the mask fabrication procedure. Hence, the actual mask will differ slightly.)

4800 μm devices. It also contains alignment marks for e-beam exposure and test areas for C-V profiling and gate recess. The masks are expected to be available by December; hence, fabrication is expected to begin early in the next phase of the contract.

SECTION III
EVALUATION OF MONOLITHIC PUSH-PULL AMPLIFIERS

Testing of both single-stage and two-stage push-pull monolithic chips from several slices was performed. The objective of this testing was to document the performance of the push-pull amplifiers and gain experience in fabrication and handling of the monolithic chips. As a result, the yield of good devices available for rf testing has increased steadily throughout Phase II.

A. Single-Stage Evaluation

Further evaluation of the single-stage (two 600 μm devices) monolithic push-pull amplifier described in the first annual report was performed.

Figure 6 shows the large signal gain versus frequency characteristic at an input level of 24 dBm. At 9.5 GHz a gain of 4.5 dB and a 1 dB bandwidth of 1.4 GHz is obtained (refer to gain compression characteristic shown in the first annual report).

AM to PM conversion and third order intermodulation distortion measurements were also made. Figure 7 shows the results for the AM to PM conversion measurement at 9.5 GHz. The worst-case AM to PM conversion is 2.5°/dB and occurs at an output power of 0.6 W (P_{in} = 22 dBm). For output powers of up to 0.5 W the AM to PM conversion is no worse than 0.6°/dB.

Third order intermodulation results were compared directly to an equivalent 1.2 mm discrete device. This conventional amplifier yields 6.5 dB small signal gain and a 1 dB gain compression point of 630 mW. Generally, the two amplifiers yielded similar characteristics. The third order products were down 20 dB from two tones at an output level (for each tone) of 23.3 dB for the push-pull and 23.8 dB for the conventional amplifier. Figure 8 shows the results for the push-pull amplifier.

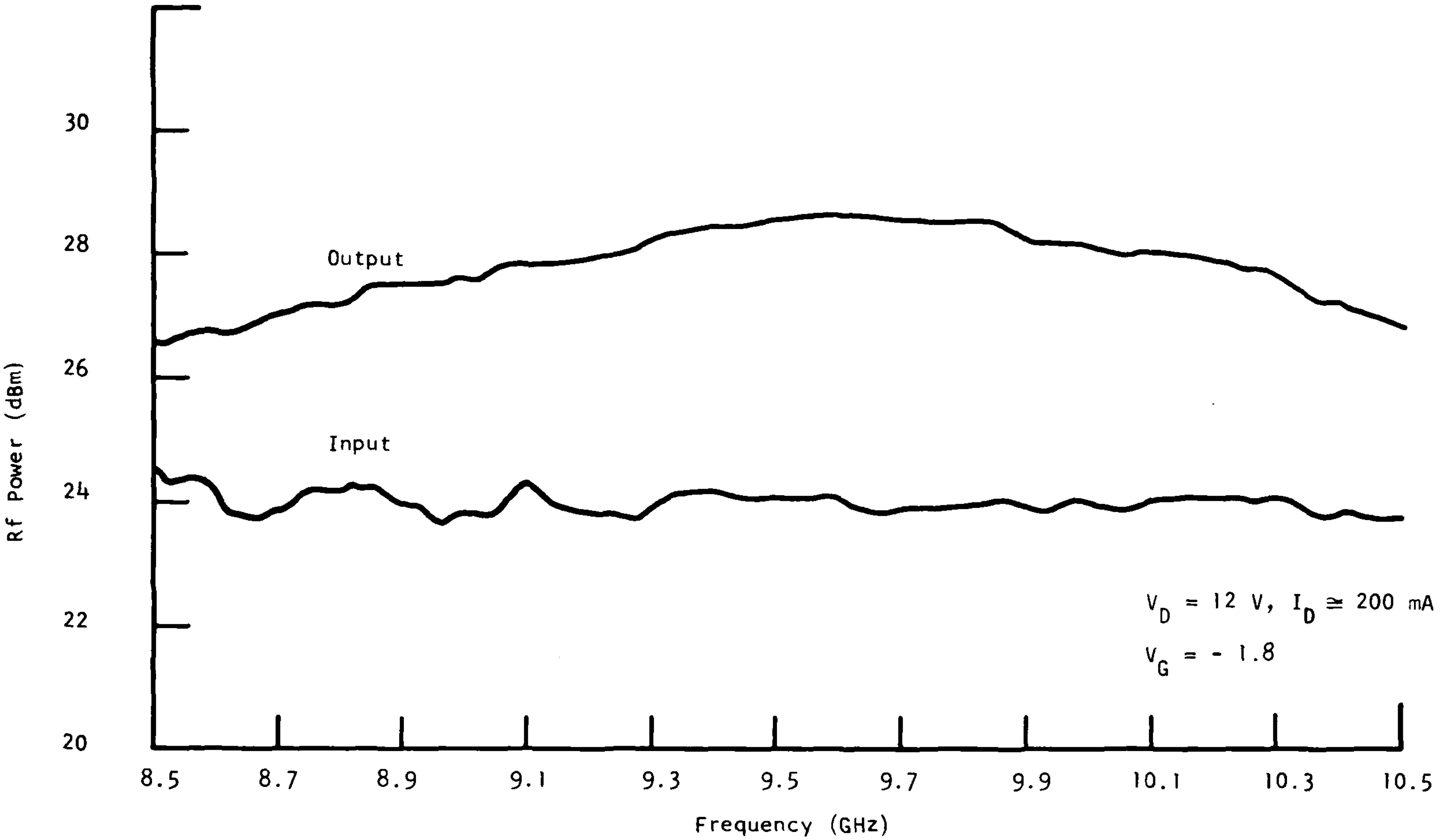


Figure 6 Large Signal Gain vs Frequency Characteristic

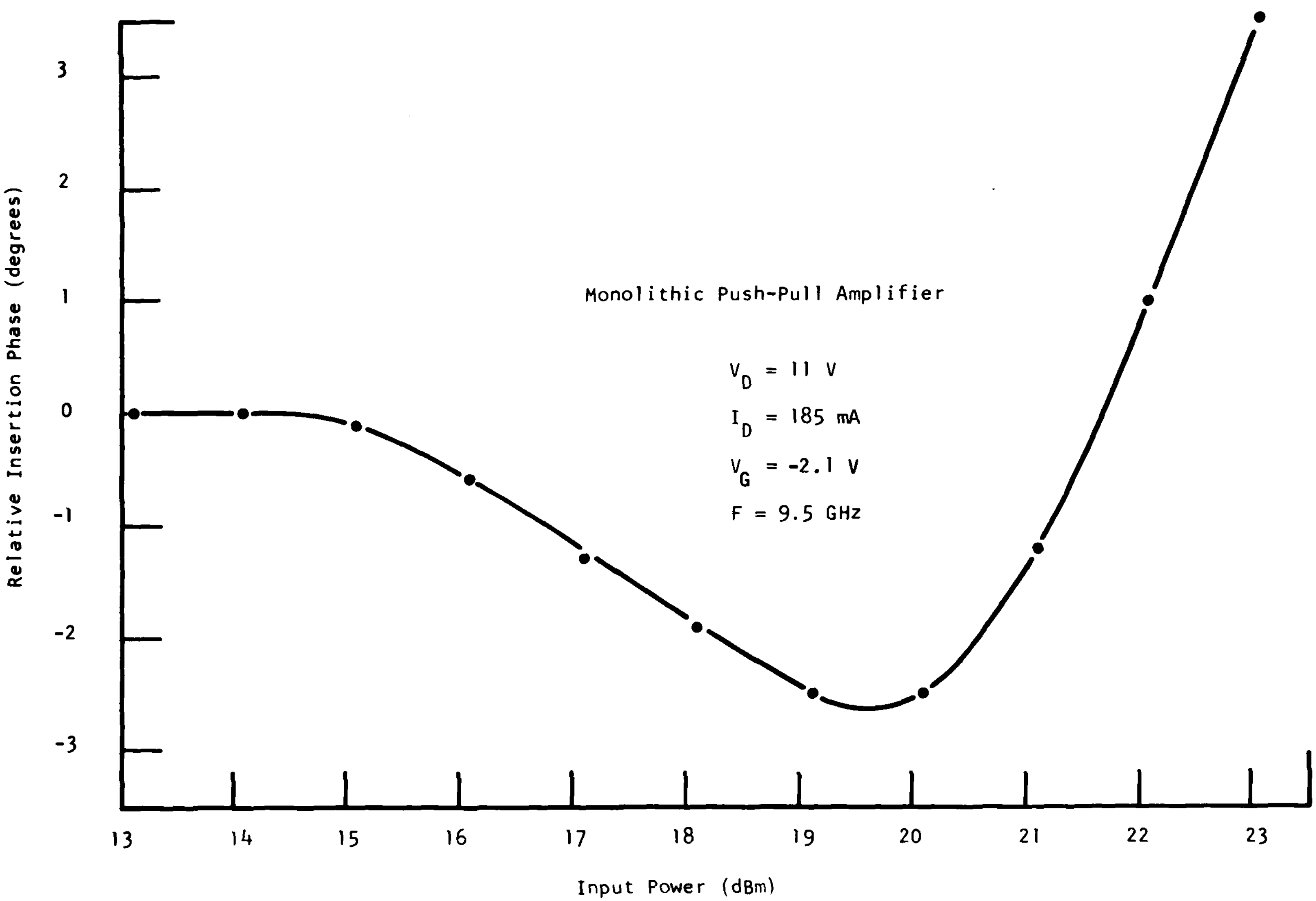


Figure 7 AM to PM Conversion for Single-Stage Monolithic Amplifier

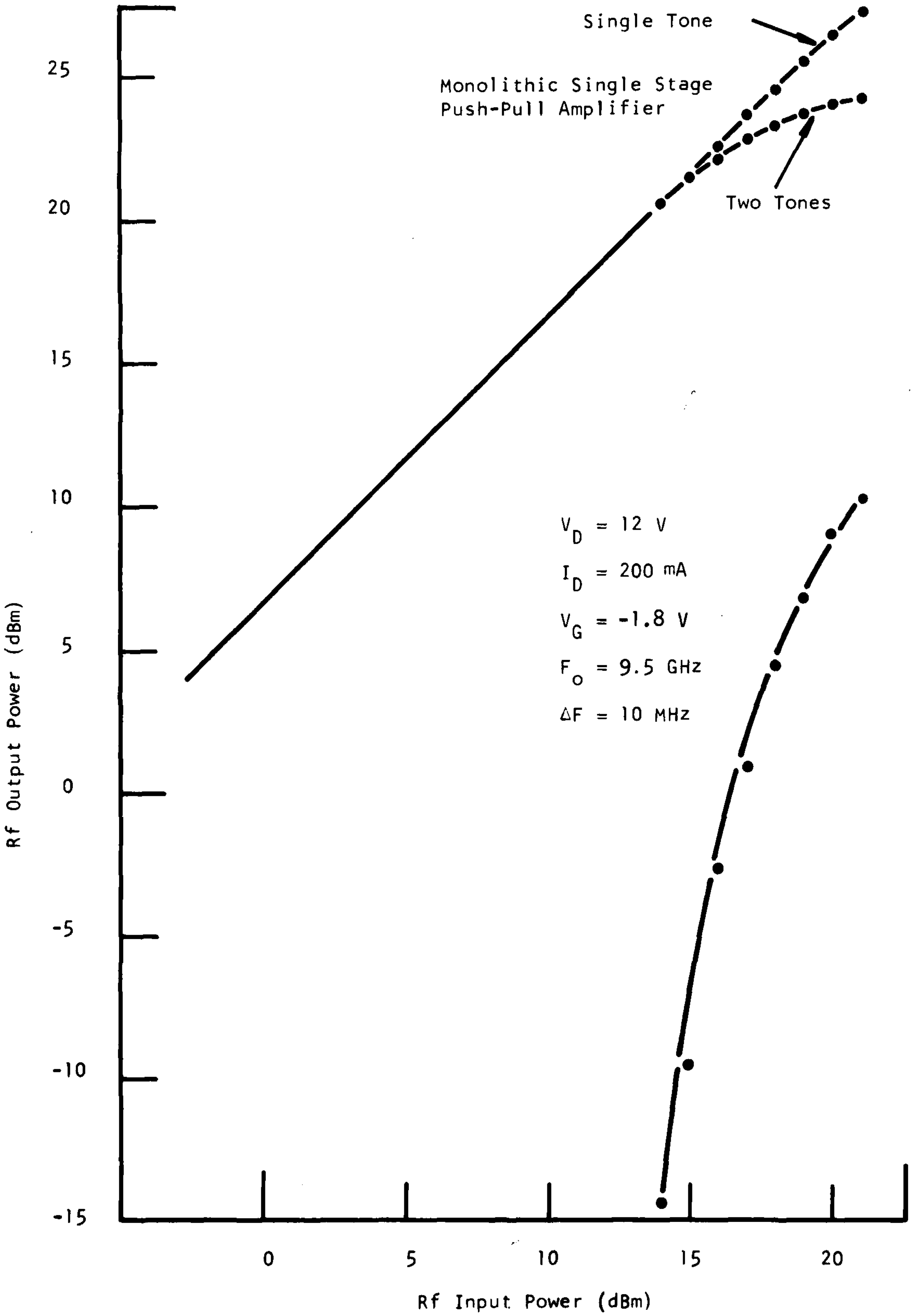
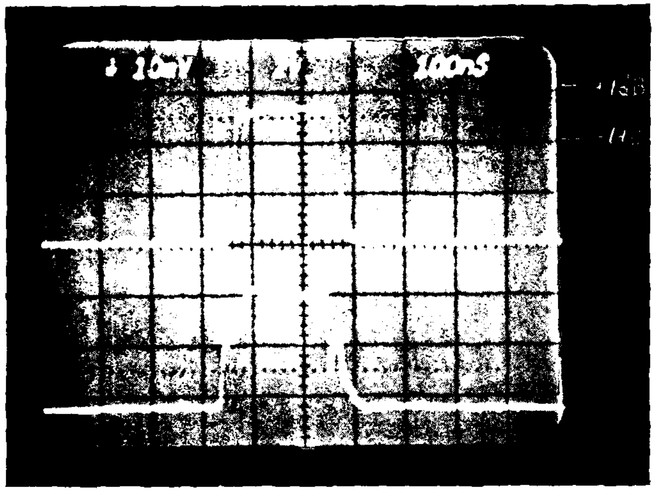


Figure 8 Third-Order Intermodulation Distortion Measurements

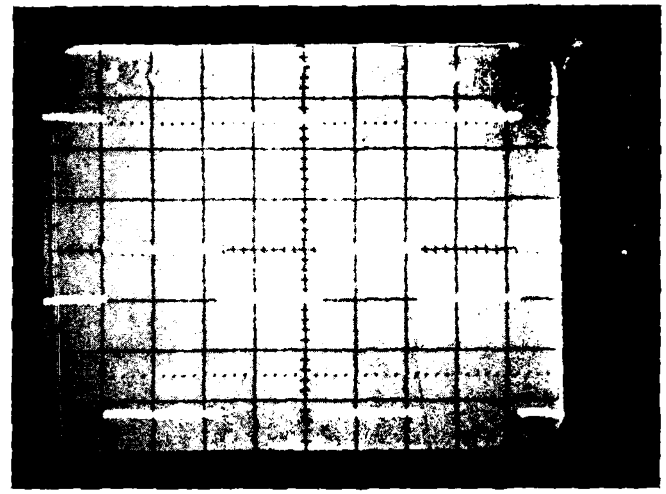
Finally, pulse characteristics were also measured. For short pulse lengths (approximately 200 ns) and low duty cycle ($\leq 1\%$) operation, about 0.4 dB increase in the output power is observed as compared to the cw case. For 20 μs pulses at 50% duty cycle, amplitude droop is about 0.2 dB. Similar results are typically observed for discrete devices. Figure 9(a) shows the short pulse case, while Figure 9(b) shows the 50% duty cycle pulse results for the monolithic amplifier. In both photos the upper trace is the detected rf output power while the lower trace is the pulsed gate voltage applied to the amplifier. The rf input power is kept constant at 23 dBm, while the gate bias is pulsed alternately from the pinch-off voltage (-6.5 V) to the nominal value of maximum rf output power (-2.0 V). Under cw conditions an output power of 28.4 dBm is observed, and this value is used as a cw datum which corresponds to the upper dotted graticule line in the photos of Figure 9. Calibration of the video detector about the cw reference is indicated by the 1 dB marks in the photos. During pinch-off the rf output power is about 13 dBm (10 dB loss through amplifier).

B. <u>Two-Stage Evaluation</u>

Figures 10(a) and 10(b) show the first successful two-stage push-pull amplifier assembled and tested in our laboratory. As seen in the photo, stitch-bonding is used to interconnect the source pads in these earlier devices. A pair of 600 μm gate width FETs and a pair of 1.2 mm gate width FETs are used in the first and second stages, respectively. These stages are capacitively coupled by means of a 1 pF silicon nitride capacitor fabricated monolithically on the chips. The same input and output microstrip circuitry on alumina is used as before. The chip dimensions are 2.0 mm x 2.0 mm x approximately 0.1 mm. The two extra bias chokes are used to supply bias to the interstage drain and gate electrodes. The first devices fabricated yielded a small signal gain of 15 to 17 dB at 9.0 GHz. Figure 11 shows the gain compression characteristic for one of the chips retuned for large signal operation (shunt inductors made longer on drains). The small signal gain is 13 dB at 9.5 GHz, and the 1 dB gain compression point occurs at a power output of 1.1 W. At 10 dB gain, 1.26 W is obtained.



(a)



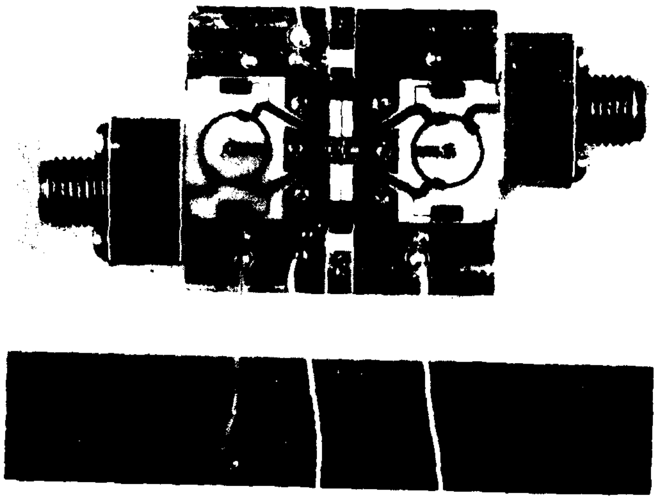
(b)

Vertical: Upper Trace (Output Power): 2dB/div between ± 1 dB marks; cw reference is upper dotted graticule line.

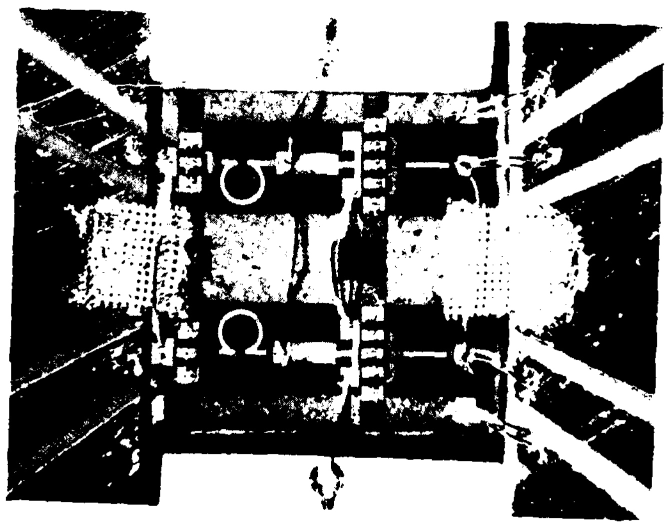
Lower Trace (Gate Voltage): 2 V/div
Zero Reference - Center graticule line, both traces

Horizontal: (a) 100 ns/div
(b) 10 μs/div

Figure 9 Pulse Characteristics for Monolithic Amplifier
(a) Duty Cycle: 1%
(b) Duty Cycle: 50%



(a)



(b)

Figure 10 A Two-Stage Push-Pull Amplifier
(a) Overall Amplifier
(b) Details of Two-Stage Monolithic Chip and Alumina Circuit Interface

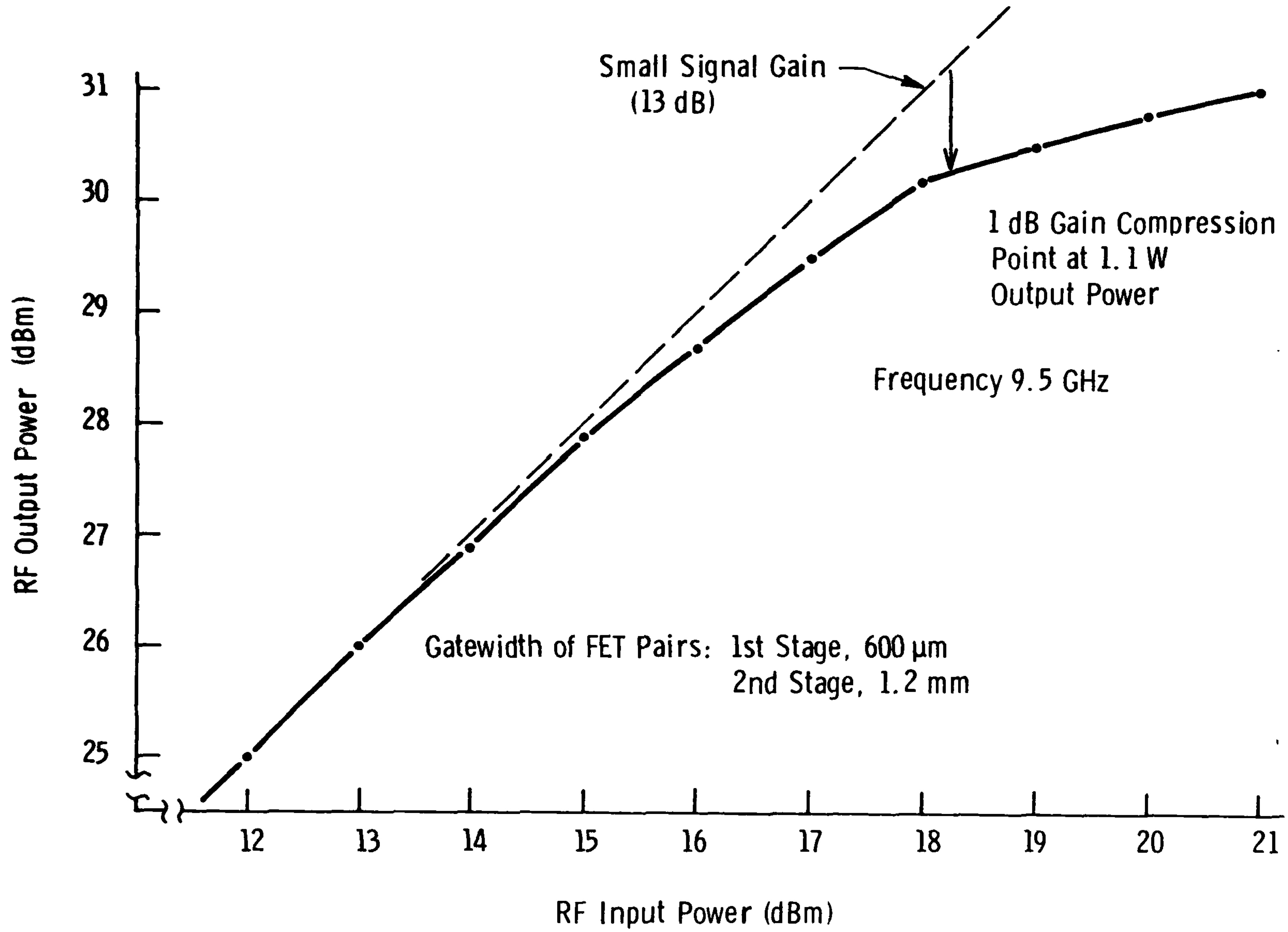
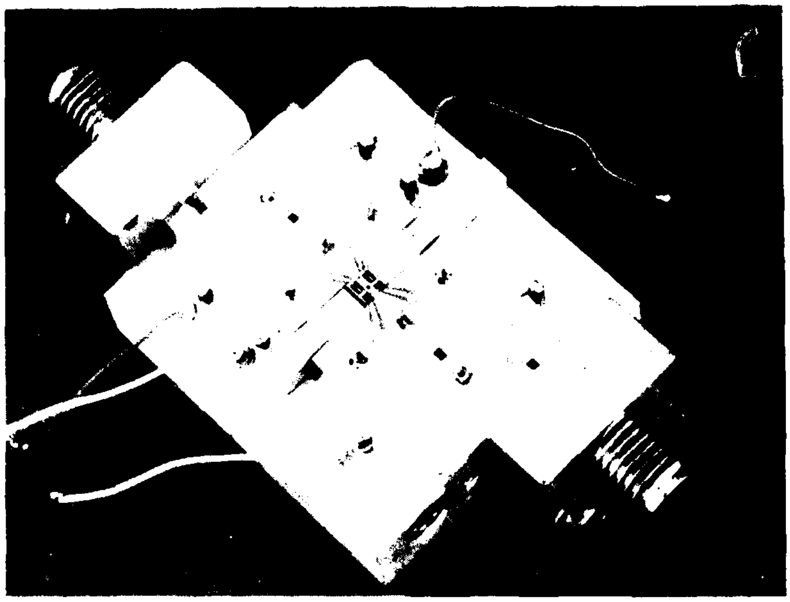


Figure 11 Gain Compression Characteristic for Two-Stage Monolithic Push-Pull Amplifier

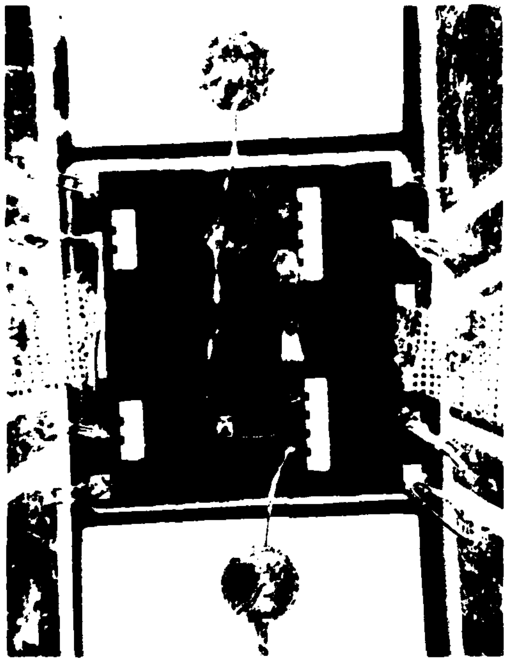
Several slices of push-pull, two-stage devices were processed and evaluated since the first such amplifier was tested. In general, the peformance has been comparable to the first results shown above. All of these later monolithic chips incorporate plated air-bridge source interconnections that eliminate the need for stitch-bonding of the source pads. Figure 12 shows one of these later devices mounted in the test fixture. Note the air-bridge source interconnects and the interstage 1 pF coupling capacitors in Figure 12. The top plate of the capacitor is Ti/Au (instead of Al, as used on earlier devices). Bias is supplied externally through bias chokes, two of which are located in close proximity to the chip, while the other two are integral with the 180° hybrid rings [see Figure 12(a)].

Figure 13 shows typical small signal and large signal gain characteristics as a function of frequency from 8.5 to 11.5 GHz for one such amplifier. The 1 dB gain compression point at 9.5 GHz is 0.9 W, and the saturated output power is 1 W with 10 dB gain. In the figure the small signal gain was obtained by reducing the first and second stage drain bias to 5.0 V and 8.0 V, respectively, while the corresponding voltages for larger signal operation were 6.7 V and 12.5 V. No other retuning was done.

The gain compression characteristic for still another monolithic amplifer with air bridge source interconnects is shown in Figure 14. For this amplifier the small signal gain is 14 dB, and the 1 dB gain compression point occurs at 1.1 W of output power at 9.0 GHz. The saturated output power is 1.2 W with 11 dB gain. Although this performance is good, the power-added efficiency is low at 16%. To check the quality of the chip mounting, insofar as thermal impedance is concerned, this amplifier was pulsed by biasing the gate with short duration, low duty cycle gate pulses. The gates of both the first and second stages were driven from the pinch-off voltage to the optimum voltage for maximum output power. A common voltage was used for both sets of gates. Figure 15 shows the superimposed oscilloscope traces of both cw and pulsed operation with 100 mW of input power applied to the amplifier. It is interesting to note that the difference in output power is about 1 dB between



(a)



(b)

Figure 12 Two-Stage Push-Pull Amplifier (a) Test Fixture (b) Mounted Device

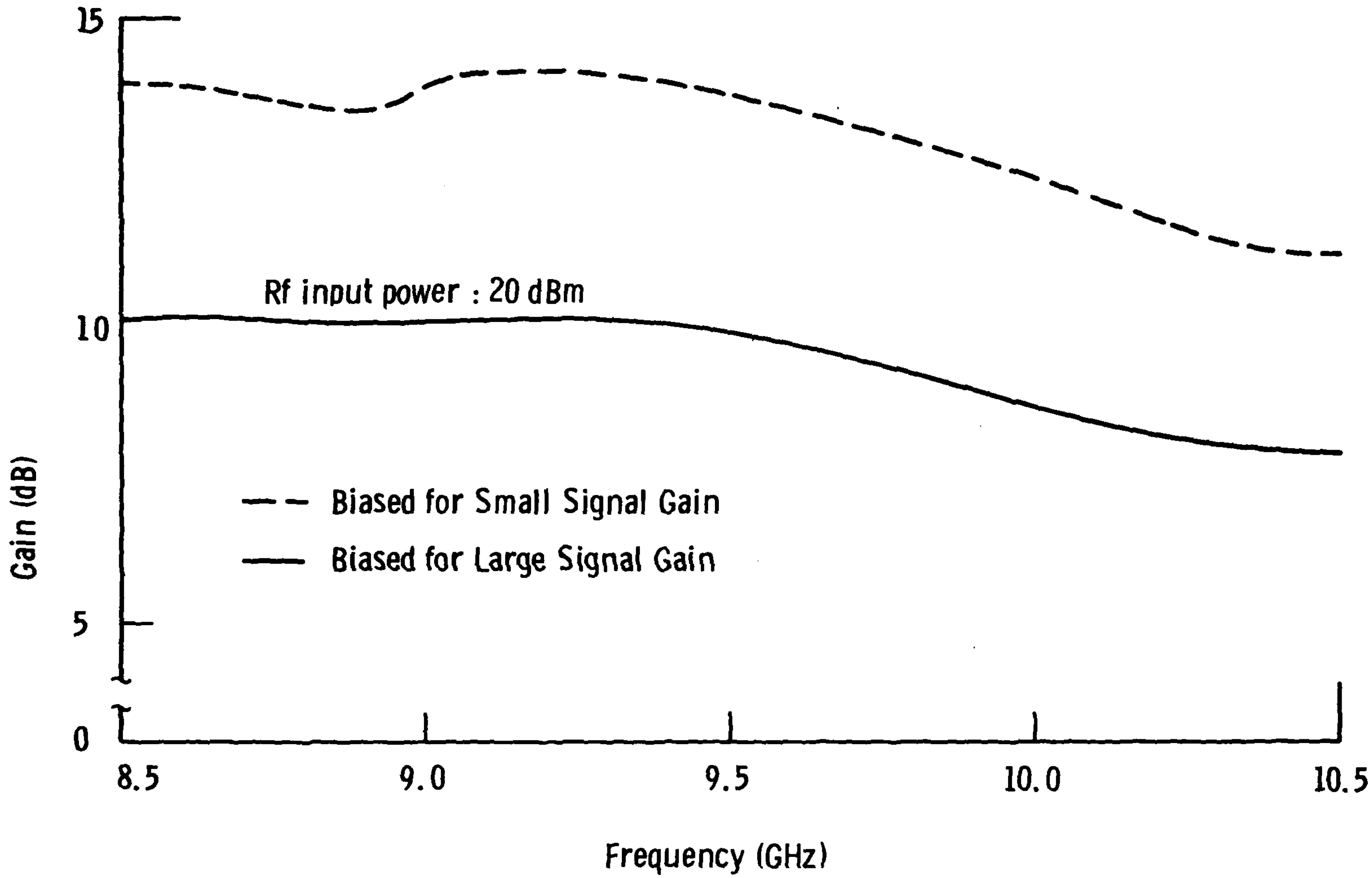


Figure 13 Small and Large Signal Gain vs Frequency Characteristic for Two-Stage Push-Pull Amplifier (Performance Shown in Figures 14 and 15)

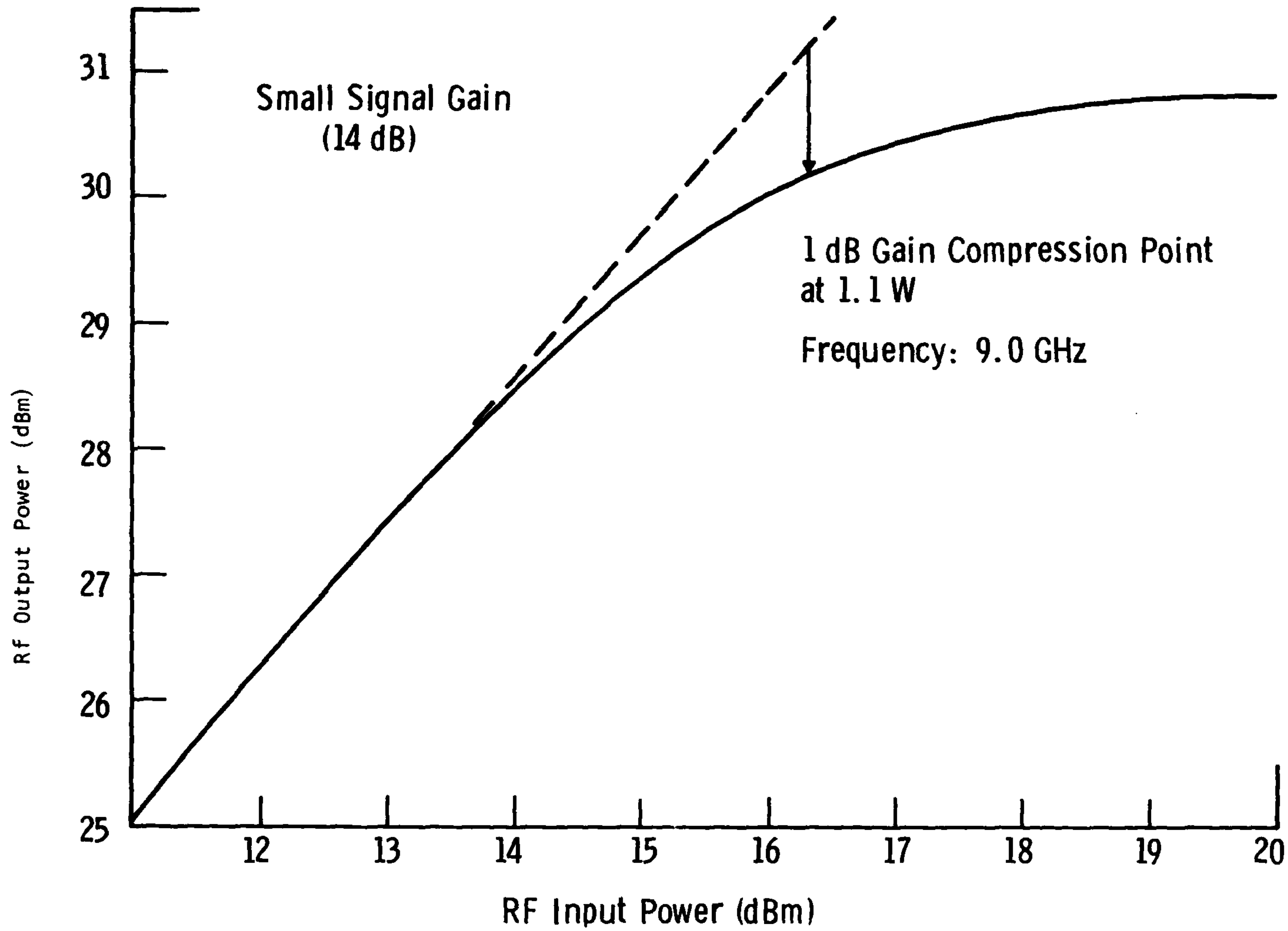
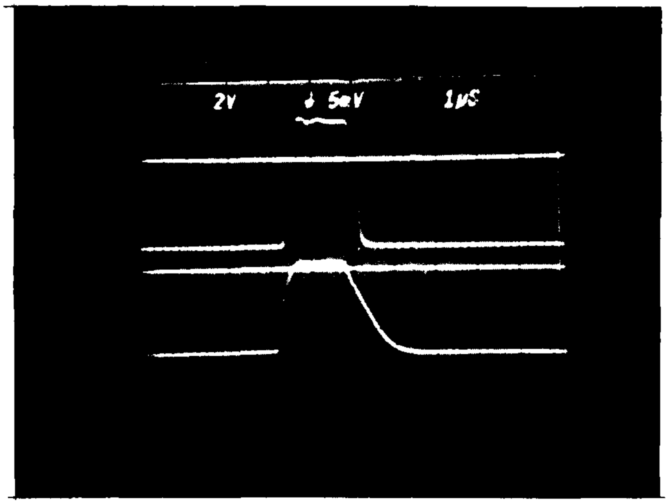


Figure 14 Gain Compression Curve for Two-Stage Push-Pull Amplifier (Slice 121-IIn)



Vertical: Upper traces (output power)
~ 1 dB/div between first and second graticule lines from the top.

Cw reference is second graticule line from the top.

Lower Traces (Gate Voltage): 2 V/div.

Zero reference is center graticule line, all traces

Horizontal: 1 μs/div

Figure 15 Pulse Characteristics of Two-Stage Monolithic Push-Pull Amplifier for Short Pulse, Low Duty Cycle Operation cw and pulsed operation. This is more than is usually observed with well heat-sunk discrete devices, and more than was observed with a single-stage push-pull amplifier utilizing the first stage only. Under pulsed operation the output power is 31.8 dBm, or 1.5 W with 12 dB gain. The power-added efficiency during the pulse is 20%.

The above results seemed to indicate a possible thermal resistance problem. Indeed, after a cross section sample was prepared of the above chip and its copper block carrier, it was apparent that voids in the solder joint resulted in inadequate heat sinking of the power devices, causing the observed power output degradation during cw operation. In fact, one of the voids was directly beneath one of the 1.2 mm FETs of the second stage, as shown in Figure 16. These results emphasize the importance of good heat-sinking requirements for power monolithic devices.

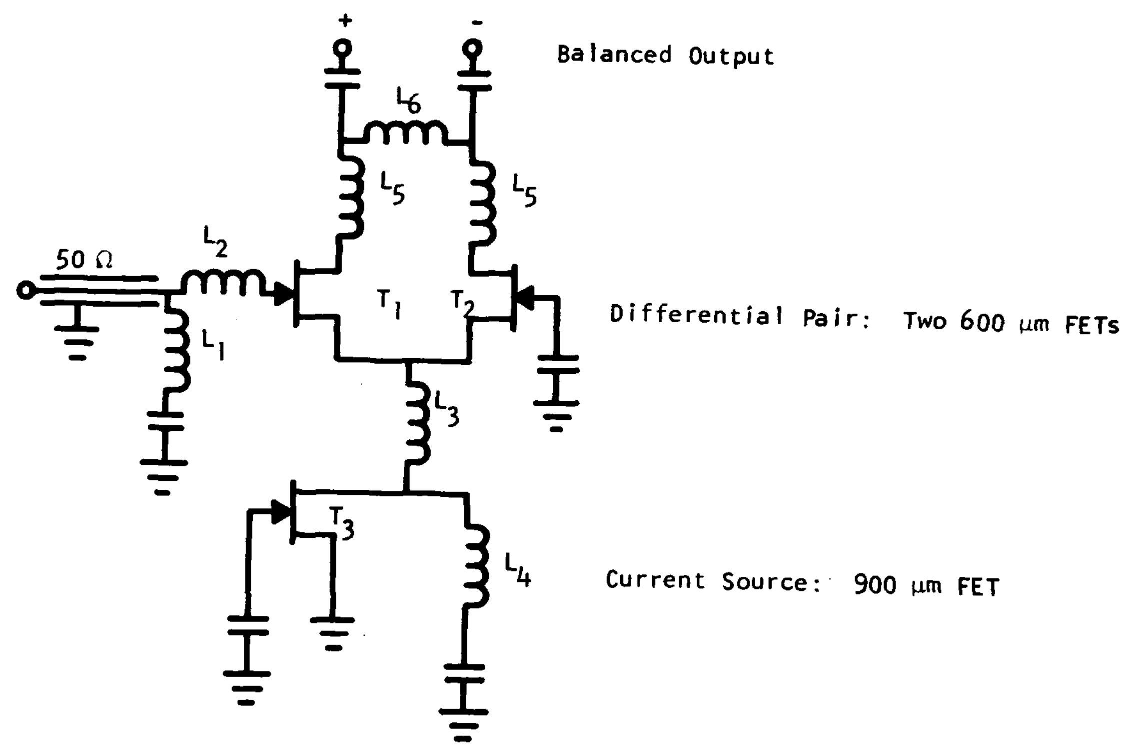
Figure 16 Cross Section of Two-Stage Push-Pull Amplifier Showing Poor Solder Joint Which Accounts for the Degradation in cw Output Power

*Note the cross section of the plated air-bridge source interconnect.

SECTION IV
PARAPHASE AMPLIFIER DEVELOPMENT

Figure 17 shows a schematic diagram of the three-FET paraphase amplifier. Two 600 μm gate width devices are used for the differential pair. The unbalanced input is applied to one of the gates while the other gate is rf shorted to ground. The balanced output of the paraphase amplifier is taken from the differential pair. The output tuning is identical to that used in the first stage of the push-pull amplifier, which also makes use of a pair of 600 μm devices. As explained below, the input impedance to the paraphase amplifier is twice the input impedance of a 600 μm FET, due to the grounded condition of the second gate. Consequently, the inductors L_1 and L_2 are used to impedance match the 50Ω input line to an FET having an equivalent input impedance of a 300 μm gate width device. The current source transistor is realized by somewhat larger device, having a total gate width of 900 μm. To provide a high impedance at the common source connection to the differential pair, the gate of the current source transistor is rf shorted to ground, and a shunt inductor, L_4, is used at the drain to parallel resonate the drain to source capacitance of the current source transistor.

Figure 18(a) shows a simplified schematic of the ideal paraphase amplifier. The input is shown driven by an ideal voltage source of magnitude, V. Figure 18(b) shows the same circuit driven by an equivalent set of generators, an even pair and an odd pair, driving both gate inputs of the differential pair. Because of the constant current source, no common mode current flows, since any common voltage change applied to the differential gates is accompanied by an equal change in voltage at the common source node of the differential pair. Consequently, the only current that flows is that due to the pair of antiphase generators of magnitude 0.5 V. The antiphase current into each gate is just the applied voltage divided by the input impedance of a 600 μm device (as in the push-pull case), i.e., $I = V/2 \div Z|_{600\,\mu m}$. Therefore, the input impedance to the single-ended gate as shown in Figure 18(a) is just



All capacitors are dc blocking type ≈ 10 pF

$L_1 \cong 0.8$ nH
$L_2 \cong 0.3$ nH
$L_3 \cong 0.2$ nH
$L_4 \cong 1$ nH
$L_5 \cong 0.8$ nH
$L_6 \cong 1.5$ nH

$\left.\begin{array}{l} T_1 = 600\ \mu m \text{ FET} \\ T_2 = 600\ \mu m \text{ FET} \end{array}\right\}$ Differential Pair
$T_3 = 900\ \mu m$ FET Current Source

Figure 17 Three-FET Paraphase Amplifier For 9.5 GHz Operation

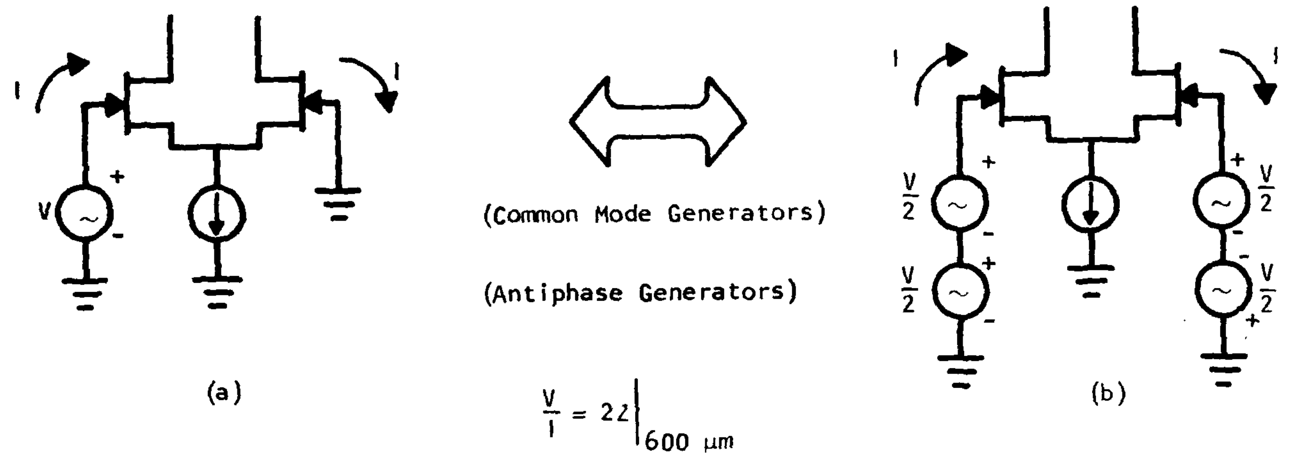
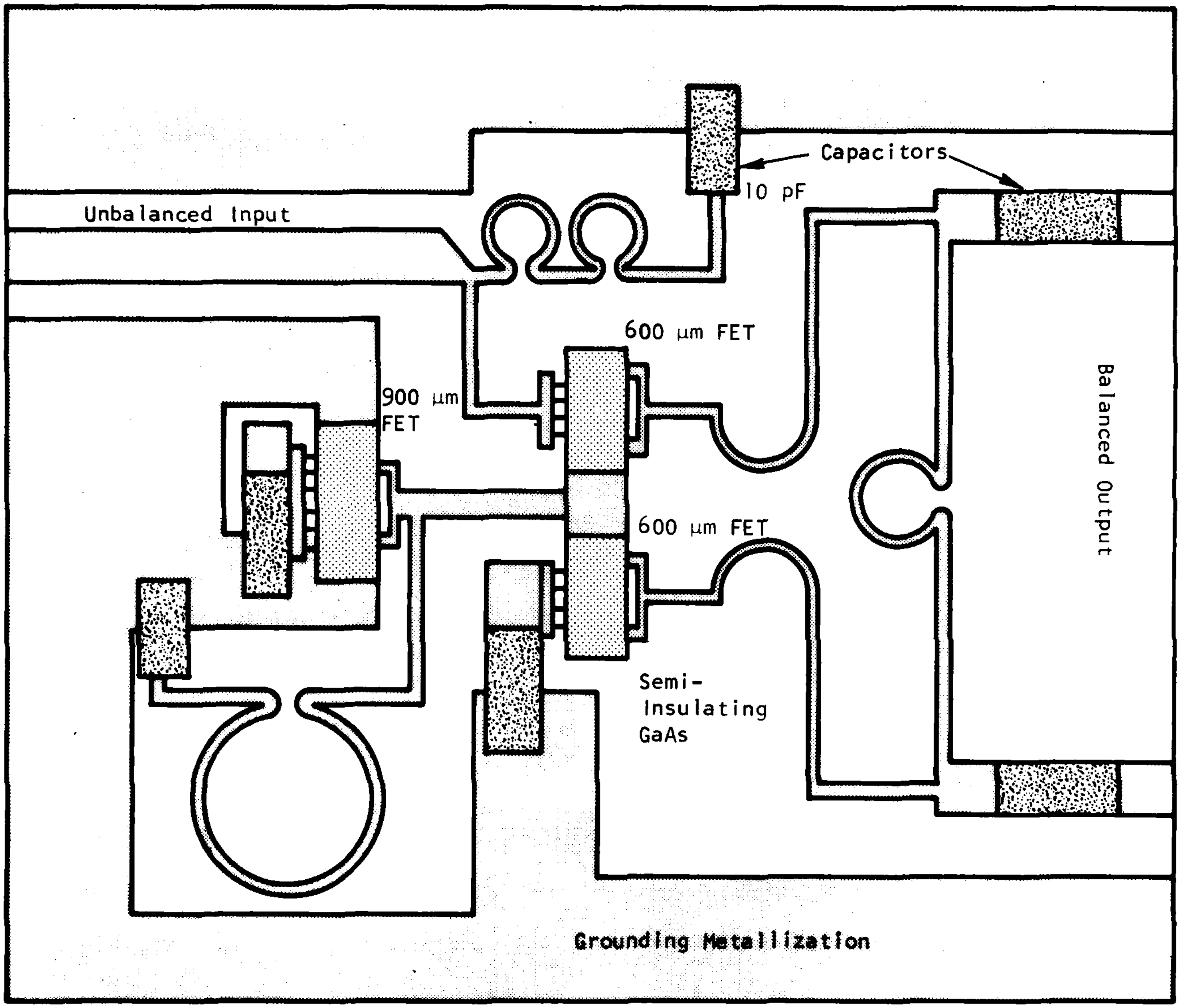


Figure 18 Idealized Schematic of Paraphase Amplifier
(a) Single input generator to paraphase amplifier
(b) Equivalent set of in-phase and antiphase input generators to differential amplifier

$$Z = \frac{V}{I} = \frac{V}{(V/2) + Z\Big|_{600\ \mu m}} = 2Z\Big|_{600\ \mu m}$$

Finally, Figure 19 shows the chip layout for the paraphase amplifier. The chip size is 2 mm x 2.4 mm. All capacitors are monolithically fabricated, are of the metal/silicon nitride/metal overlay type, and are used for dc blocking purposes only. Their value is 8 pF or more. All inductors are monolithically fabricated over semi-insulating GaAs. The chip is designed so that it can be interfaced at the output with another balanced transmission line or push-pull chip in that it incorporates two series chip capacitors for dc-blocking. For evaluation of the paraphase amplifier alone, the chip is cut to a 2 mm x 2 mm dimension and interfaced with an output balun (or the two signals can be tested separately) to check the antiphase characteristic. Two positive voltages, one on the drains of the differential pair and another on the gates of the differential pair, plus a negative bias applied to the gate of the current source FET, operate the amplifier. The current source FET is a 900 μm device to accommodate the dc currents of the differential pair which consists of two 600 μm devices. The input is a 50Ω transmission line fabricated on the GaAs substrate. To evaluate the effectiveness of the current source alone, the chip may also be cut to a 1 mm x 2 mm dimension so that the output impedance may be measured and maximized.

Figure 20 shows a microphotograph of a processed paraphase amplifier chip. The dark bars are the plated air-bridge source interconnects over the current source and the differential pair transistors. The lighter rectangular areas are the 8 pF overlay capacitors. In Figure 20 the entire chip is shown, including the output coupling capacitor provision for connecting to the push-pull amplifier. (The pair of output capacitors does not have the top plate for these first processed devices in which the chip is cleaved to a 2.0 mm x 2.0 mm dimension to test the paraphase amplifier only.)



Chip Dimensions 2 mm x 2.4 mm

Figure 19 Chip Layout for Paraphase Amplifier

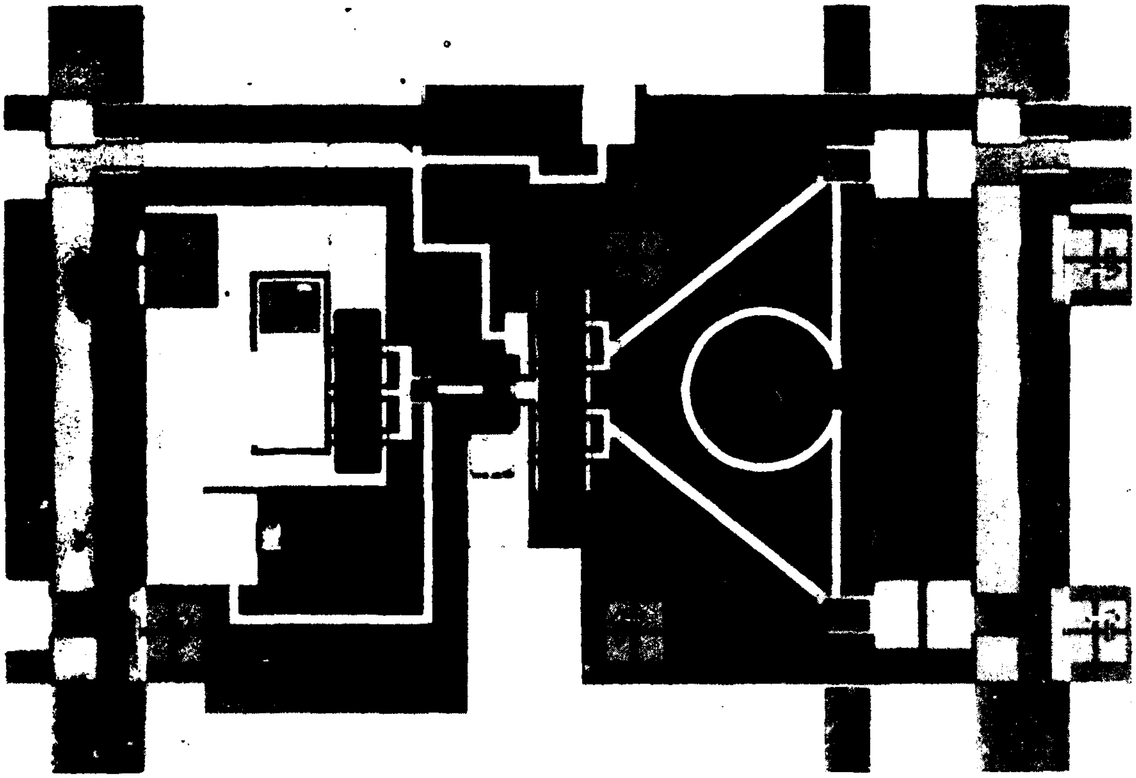


Figure 20 Microphotograph of Paraphase Amplifier Chip

Figure 21 shows the paraphase chip mounted in the test fixture. The input circuit consists of a 50 Ω microstrip to coplanar microstrip transition, while the output circuit makes use of the 180° hybrid ring to power-combine the two antiphase output signals of the paraphase amplifier and provide a single unbalanced 50 Ω line output.

Figure 22 shows the gain vs frequency results obtained from the first slice. At 9.0 GHz a small signal gain of 3 dB is obtained for the amplifier configuration as shown in Figure 21. For these tests, however, it was difficult to maintain a "good ground" on the chip's ground metallization. Some evidence of a standing wave was noted on the ground metallization of the alumina circuits as well. Since the balun action depends on the second gate of the differential pair being rf shorted to ground, it is believed that some of the anomalous response shown in Figure 22 is due to this problem. The test fixture is presently being improved to ensure a better connection between the top and bottom grounding metallization. Furthermore, upon examination of the resistivity of the buffer/substrate material used for this first paraphase amplifier slice, it was observed that an abnormally high conductance (and reactance) was measured. Consequently, it is believed that the small gain and somewhat anomalous results obtained on these first chips are partially due to the abnormal resistivity of the substrate as well as to the inadequate grounding of the chip's ground metallization. Further processing of better slices is now under way.

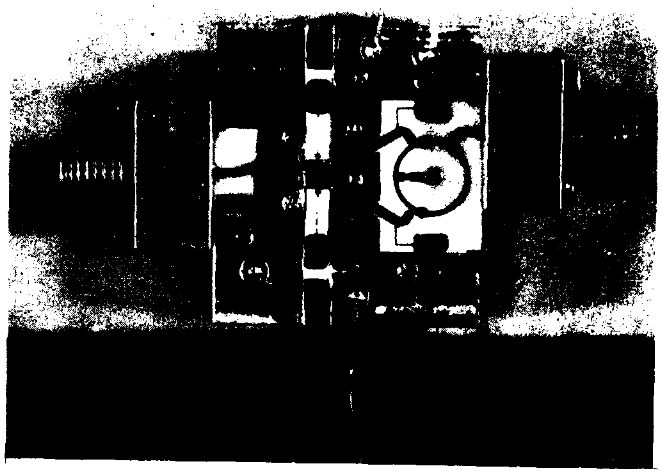
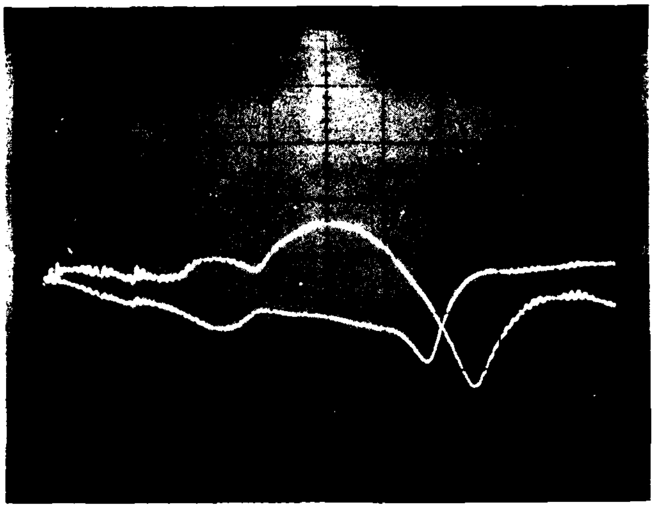


Figure 21 Paraphase Amplifier Chip in Test Fixture



Vertical:	Top trace (Gain): 5 dB/div Lower trace (Return Loss) 10 dB/div
Horizontal:	400 MHz/div Range 7 to 11 GHz.
Reference:	Center graticule line, both traces

Figure 22 Small Signal Gain vs Frequency for Paraphase Amplifier

SECTION V
FULLY INTEGRATED FET PUSH-PULL DEVICE

The monolithic push-pull configuration offers several circuit-related advantages that are especially significant for power amplifier application at microwave frequencies. Some of these advantages, as related to impedance matching, for example, have already been demonstrated with the monolithic devices fabricated for this program.

One particular feature, however, that is unique to the monolithic push-pull FET configuration employing coplanar grounding metallization has not been fully exploited or studied. This feature is that fundamental frequency source currents are confined primarily to the chip's grounded surface. These currents flow between the source of each transistor and the source of its push-pull counterpart via the coplanar ground metallization. If each transistor pair is closely matched (which it is by virtue of being fabricated monolithically), then only a small fraction of the total rf source current needs to flow to true chassis ground. Consequently, connection of the transistor source pads to the chassis or carrier plate is not as crucial as it is in the case of a conventional discrete FET. Furthermore, if the source connecting path between each pair of push-pull FETs is minimized, then source lead inductance and resistance are minimized also. This is especially significant in light of fairly strong evidence based on experience with discrete power devices that source lead inductance is large enough to cause gain and output power degradation even at X-band frequencies. Reduction of source lead inductance by confining ground currents to flow between transistor pairs operating in push-pull can, therefore, be a method for improving intrinsic device performance, especially in the case of power devices with large total gate widths.

With the above concept as the primary motivation, we have expanded the scope of the present monolithic program to include the investigation of reduced source lead inductance in X-band power FETs by the methods outlined above. Plans to carry out this investigation are discussed below.

The program expansion begins with the design and fabrication of a GaAs power FET with a total gate width of 1200 μm operating in a fully integrated push-pull mode. As shown in Figure 23, the push-pull transistor pairs are incorporated into a single device composed of four 300 μm push-pull transistor cells. Both input and output ports consist of a pair of terminals that support a balanced signal with respect to ground. Coplanar ground metallization is used in the same manner as in the previously developed monolithic push-pull amplifier chips. Balun circuits such as the 180° hybrid rings designed previously for the program will be used to interface the chip with standard unbalanced microstrip lines. To achieve the configuration shown in Figure 23, three crossover structures or "air-bridges" are required for the separation of input and output electrodes. Another air bridge is required to interconnect the source pads for dc grounding. This air bridge technology is being implemented in the latest monolithic chips for connecting the individual source pads.

Following fabrication, the new devices will be characterized to assess the peformance of the integrated push-pull configuration. The main goal will be to document the influence of the new configuration on the effective source lead inductance and to establish whether it is significant in improving overall device performance. Small signal S-parameters, together with power output performance at X-band frequencies, will be compared directly with the previous 600 μm pair, single-stage, push-pull amplifiers and with conventional 1200 μm single-stage amplifiers.

To date, mask designs have been submitted for fabrication which include the 1200 μm devices as well as larger gate width devies up to a total of 4.8 mm (see Section II).

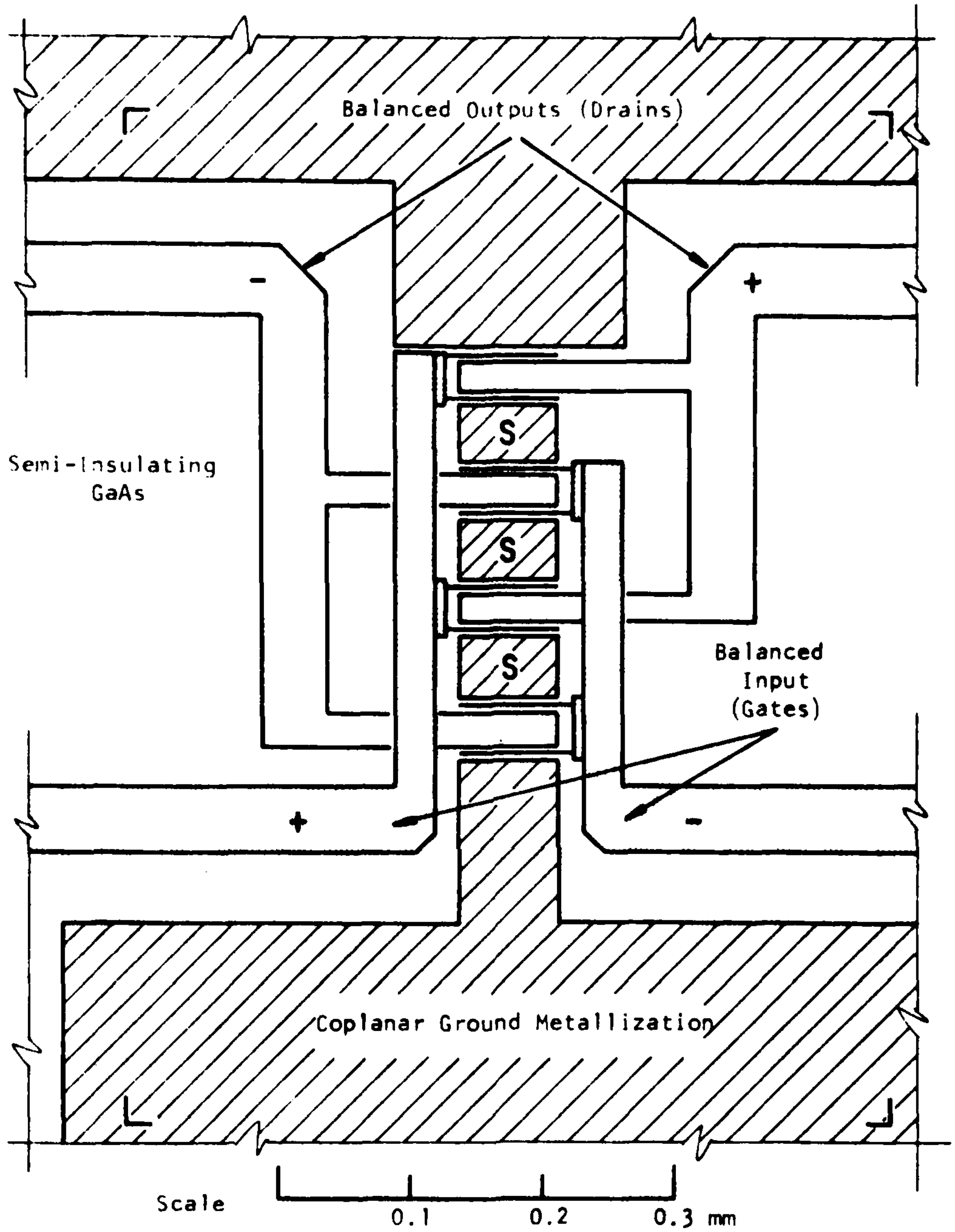


Figure 23 A Fully Integrated Push-Pull Power FET Device for X-Band Operation

SECTION VI
PLANS FOR FUTURE WORK

Plans for the future include continued work in improving monolithic fabrication and assembly techniques, including component evaluation, and further testing and optimization of the paraphase amplifier chip. Work will also commence on fabrication and evaluation of the fully integrated push-pull (FIPP) chips.

First, we plan to complete the evaluation and optimization of the paraphase amplifier chip. Initial measurements have shown balun action, but under small signal conditions and with insufficient gain. However, indications are that the slice had an abnormally high loss in the substrate material and that rf grounding from the fixture to the chip was not adequate. Further slice processing together with modifications in the grounding interface between chip and test fixture are necessary to make a fair evaluation of the paraphase amplifier performance. Power output, gain, and bandwidth performance, as well as the tracking of the 180° characteristic over frequency, will be measured. Once optimized, the paraphase amplifier will be connected to the two-stage push-pull amplifier chip. This two-chip device should realize a 16 to 18 dB power amplifier with 1.2 W output power having a push-pull output and a conventional single-ended, unbalanced input.

Second, work will begin on fabrication of the FIPP FETs. Initial evaluation will be made on the 1.2 mm devices. Characterization of these devices (using balun circuits to interface the chips with standard unbalanced transmission lines) should yield information on the design of appropriate matching circuits. It is anticipated that these matching circuits will be incorporated on the same chip in future designs of the FIPP devices. Analogous work is planned for the 2.4 and 4.8 mm devices.

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