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INDIUM PHOSPHIDE FOR HIGH FREQUENCY POWER TRANSISTORS.(U)
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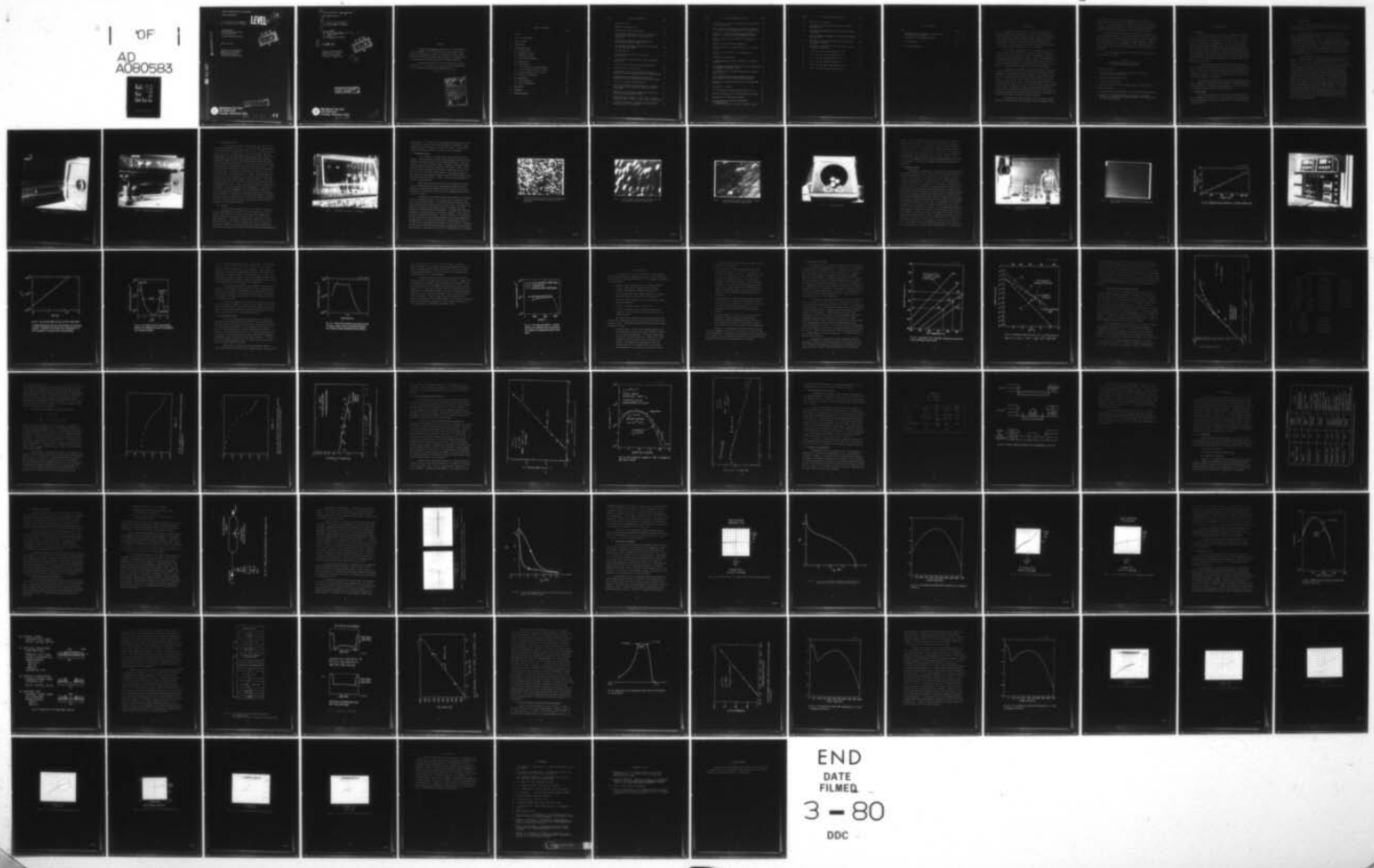

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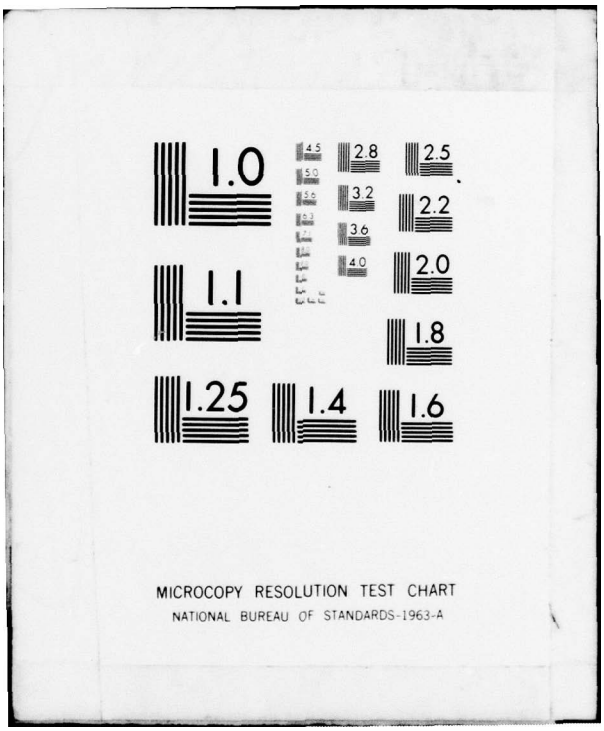
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INDIUM PHOSPHIDE FOR HIGH FREQUENCY POWER TRANSISTORS

LEVEL II 12

V. L. Wrick, G. W. Eldridge,
R. C. Clarke and M. C. Driver

Interim Report
For Period 21 March 1978
to 21 March 1979

Contract N00014-78-C-0254

Sept. 28, 1979

Office of Naval Research
Department of the Navy
800 N. Quincy Street
Arlington, Virginia 22217

Westinghouse R&D Center
1310 Beulah Road
Pittsburgh, Pennsylvania 15235

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ABSTRACT

Technology development is presented for the development of an InP power ~~FET.~~ FIELD EFFECT TRANSISTOR Both ion implantation and vapor phase epitaxy results are presented as a means for providing an active channel. Processing technology (etching, ohmic contacts) is reviewed as well as a description of various approaches for gating n-type InP.

Conclusions and plans for the last phase of the program are discussed. As a result of the first part of the program, work is to be concentrated on developing ~~JFET~~ JUNCTION FIELD EFFECT TRANSISTOR technology.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

Figure LIST OF ILLUSTRATIONS (Cont'd) Page

LIST OF TABLES

1. INTRODUCTION

The overall objective of this program is to provide some empirical evidence as to the utility of InP for the production of a power microwave field effect transistor (FET). Prior to the beginning of this study, small signal InP FETs had been produced as well as theoretical discussions of the relative merits of InP and GaAs for microwave FETs. These studies all provide useful input toward answering the power question; however, they are not complete.

InP remains a question mark for both theoretical and technological reasons. The philosophy of the present study is to begin by evaluating the technology and to conclude by RF modeling the device to investigate the larger theoretical issues. Table 1 is a compendium of the technological and theoretical problems associated with the use of InP for microwave power FETs. The remainder of this interim report will discuss our progress toward solving the technological problems.

At this point, it should be noted that the most critical technological problem in InP is the low Schottky barrier height. Various approaches to this problem have been discussed in the literature; however, any solution must be consistent with the intended role for the device. A power FET must first be able to carry large currents and reasonably large gate voltages. A typical design would include a device with a pinchoff voltage no less than 5 volts and probably ranging between 6 and 7 volts. In addition, to optimize power and efficiency, it is useful to allow the gate to be driven slightly positive with respect to the source to utilize full channel current capability. These power constraints render some InP barrier "solutions" unusable.

Our experience to date has shown that the so-called "oxide assisted" Schottky barriers can sometimes produce low leakage junction

characteristics, however, they are inappropriate for power FETs. A junction FET (JFET) can provide the ruggedness and pinchoff voltages necessary for power application. The gate technology section enumerates the various experiments undertaken to realize both oxide assisted and junction gates, and describes the direction of intensified work.

Materials problems associated with both vapor phase epitaxy (VPE) and Ion Implantation (I.I.) have been addressed in Phase I and are under good control. A device fabrication scheme has been successfully developed and is useable for a variety of design approaches. Emphasis has now been placed on the development of a JFET. New masks are in process and new device runs will be underway in the next six months of the program.

The conclusions and plans for future work are detailed in the final section of the report.

Table I

Technological and Theoretical Issues for
InP Microwave Power Transistors

Technological Problems

A. Provide Reproducible, High Mobility VPE and Ion Implanted Material for Device Fabrication

B. Develop Low Leakage Schottky Gate

C. Develop P-N Junction Gate

D. Develop Low Specific Resistance Ohmic Contacts to P&N Type InP

Theoretical Problems

A. Determine the Nature and Behavior of Gate-Drain Feedback Capacitance

B. Determine Device Design Parameters (gate length, gate-drain, spacing, etc.) which Differ from GaAs Technology in Affecting Power and Frequency Performance

2. VAPOR PHASE EPITAXY

2.1 Introduction

The $PCl_3/In/H_2$ process for the growth of indium phosphide epitaxial layers has been in general use for many years.[1-3] A carefully controlled concentration of phosphorus trichloride vapor in hydrogen is passed over indium at high temperatures, 700 - 750°C, and the products, indium monochloride and phosphorus vapor, pass over a polished seed wafer at 650°C. Epitaxy of indium phosphide subsequently takes place on the seed wafer with a growth rate and impurity content dependent on the raw materials used, but more importantly on the conditions employed. The mole fraction of phosphorus trichloride,[4] the vapor phase stoichiometry[5] and the source and seed temperature are the most significant variables in the process.

The early Westinghouse reactor demonstrated that it could achieve acceptable slice morphology and produce pure indium phosphide layers. However, the non-obvious aspects of reactor design necessitated changes in the reactor to allow the reproducible growth of multilayer structures. Therefore, after initial growth with the old system, work on a revised design was instigated.

The following sections detail the design criteria which ultimately resulted in an automated reactor capable of growing complex epitaxial structures. Discussion is also provided on the critical aspects of the growth sequence which provides FET material.

2.2 Reactor Design

The main system features are the reactor tube, gas manifold and feed lines, and the furnace. The following sections discuss these topics individually to give better insight into the overall epitaxial growth apparatus.

(A) Reactor Tube

Figure 1 shows the original reactor tube design. Provision was made for two source growth techniques, PH_3 additions, vapor dopant and liquid dopant additions.

In the design of reactor tubes, a tradeoff must be made between conflicting growth parameters. Since a mole fraction of phosphorus-trichloride greater than 10^{-2} is required to produce pure indium phosphide buffer layers, it is an advantage to keep the hydrogen diluent flow as low as possible. Also, unswept lines present a problem in that gas gradually diffuses out of them during reactor use. While the reactor shown in Figure 1 has a high degree of system flexibility, it is undesirable because of the large volumes of hydrogen required to keep the lines flushed out.

The old system had a simple catch tube to deal with by-product removal. Indium chlorides and yellow phosphorus form each time the reactor is used and these condense outside the furnace. The removal and introduction of wafers allows the air to see these by-products producing airborne vapors of hydrolyzed by-products consisting mainly of P_2O_5. These contaminate both outgoing layers and incoming clean substrates. A simplified design of the reaction chamber with short multi-purpose feed lines and a reverse flow catch tube has been exchanged with the original reactor tube as shown in Figure 2. This allows the minimum of flushing gas yielding relatively high mole fractions in the reaction chamber. The diameter of the growth chamber (40 mm) permits the use of 300 gm indium charges permitting long growth sequences. The reverse flow catch tube captures nearly all of the by-products. In excess of 150, growth sequences have been performed without resorting to acid washing the reactor tube. Long-term sequential growth without disturbing the apparatus is the key to the optimization of device structures, stability and reproducibility.

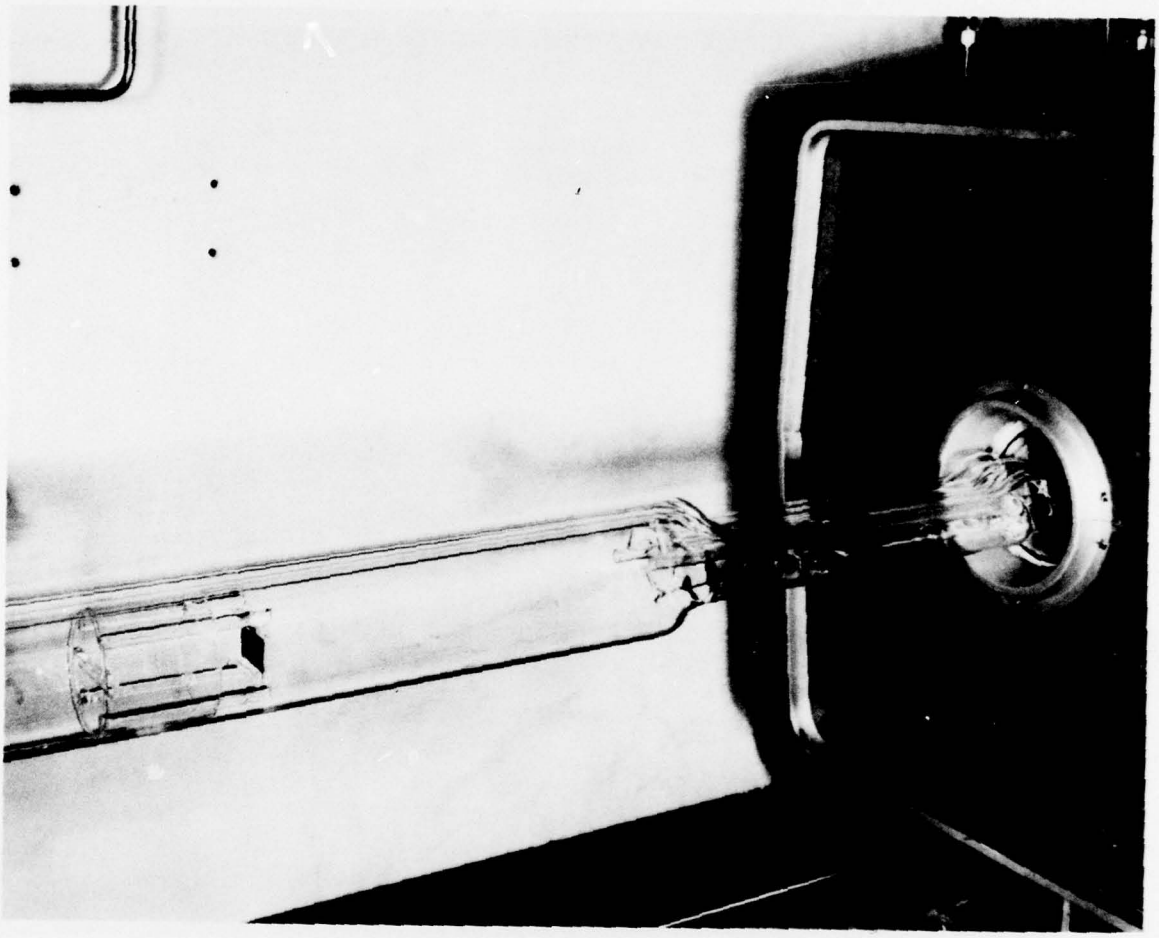

Figure 1 Old Reactor Tube

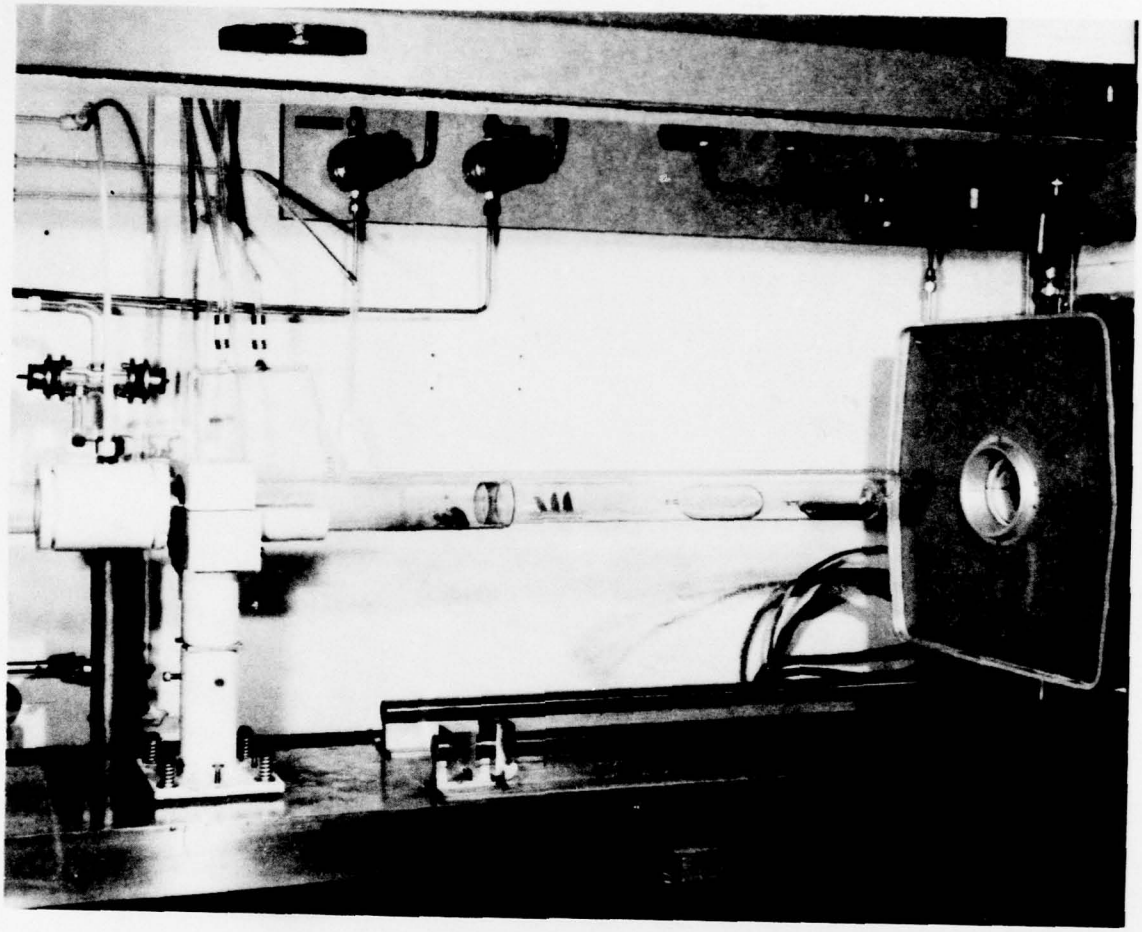

Fig. 2 Modified InP Reactor Tube

(B) Reactor Feed Lines

It is essential to system reproducibility that all feed lines be flushed during reactor operation. The rolling furnace design necessitates long delivery tubes on the order of 8 feet. A simple calculation of the sweep time of a dopant gas or a reactant gas using 6 mm bore tubing gives an 8 - 10 minute response time at 100 cc/min. Reactor tube simplification did away with liquid dope and double source circuits, reducing the number of lines. Those remaining were growth PCl_3, etch PCl_3, H_2S doping and PH_3 addition. The PH_3 and H_2S and etch flows used the second entry to the reactor that passes only over the seed. A tight fitting baffle was provided to prevent these functions from affecting the source ingot. In addition to minimizing the number of lines, the sweep time of each line was reduced to a minimum. Capillary lines were used in all circuits (2 mm bore) and the dopant injection values were adjacent to the main reaction chamber as shown in Figure 3. The effect of these response times on device structures can be predicted from the known growth rate curves. Error in the pinchoff voltage of final devices is reduced to $\sim$3% as the response times are minimized. A further complication in the rapid changing of gas concentrations is dead space, i.e., any region of a gas circuit (lines and valves) that is not swept by the carrier gas. Attention to the detailed construction of electronic injection valves and their position in the gas flow circuit is necessary to provide for sharp cutoffs in dopant concentration that give sharp structures in the epitaxial material.

(C) Furnace

A highly uniform temperature profile is necessary to get high priority high resistivity epitaxy.[4] This is achieved in a 'roll-on' furnace construction using a sodium-filled heat pipe. However, the furnace needs special attention in use in order to preserve the seed wafer properties. In steady state operation the source zone is set at 700°C and the seed zone at 650°C. When the hot furnace is rolled onto the reaction chamber the cold source metal ingot takes an appreciable time to heat up because of its thermal inertia, whereas the seed temperature

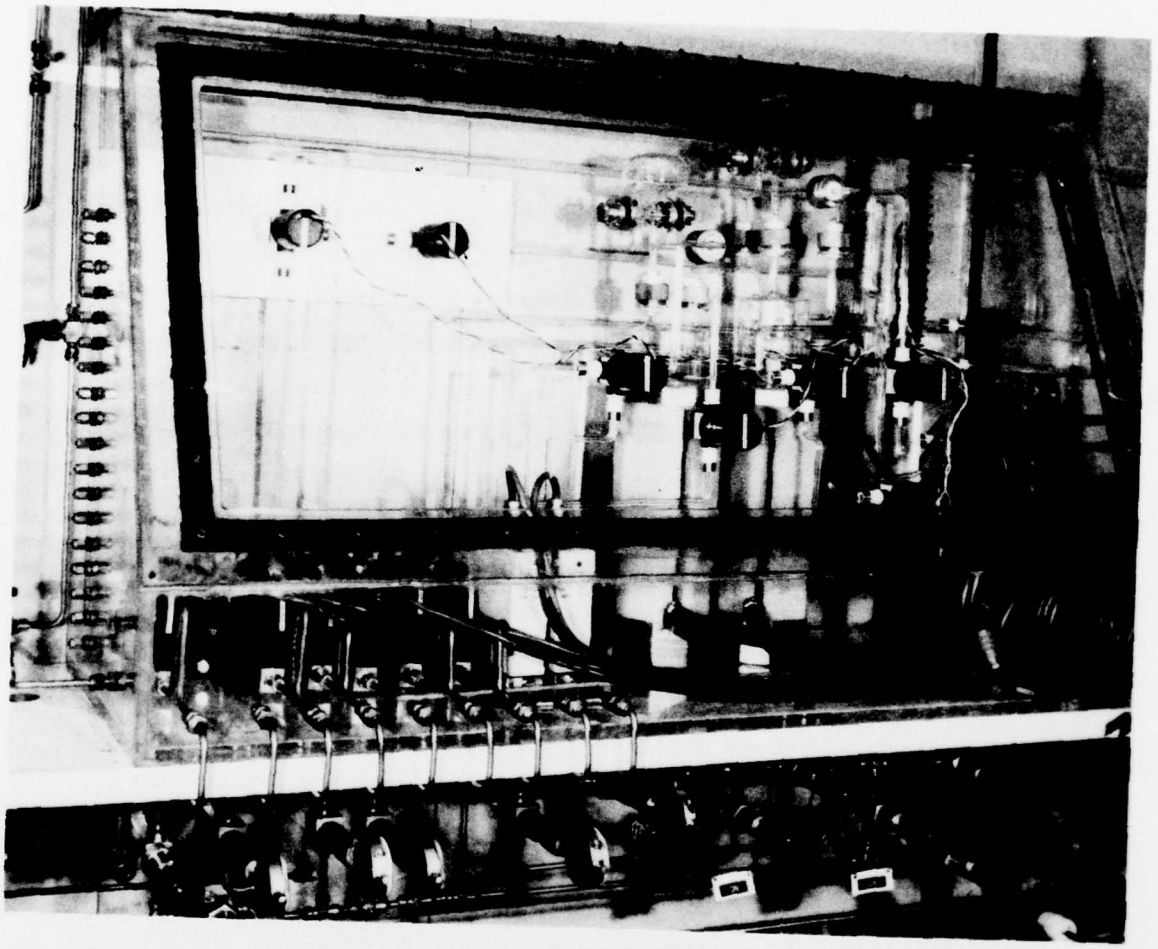

Fig. 3 Modified InP Reactor Gas Manifold

rises rapidly. If the wafer's surface temperature exceeds that of the source ingot, the wafer is unstable and begins to dissociate by the release of phosphorus leaving an indium-rich surface. Care is taken during the startup procedure to prevent this from happening.

2.3 Morphology Control

It is essential to maintain good surface flatness during epitaxy. Morphology control permits photolithography and other surface treatments for device layout to be performed effectively. The slices should be flat, shiny and defect-free. A number of sources of system introduced defects have been identified in this work. Figure 4 shows the poor epitaxy produced on an indium-rich surface owing to the dissociation of the seed wafer before growth. A well known feature of III-V epitaxy is that growth on exactly oriented surfaces produce facets and many pyramid type defects. Figure 5 shows the defects produced on an exactly oriented wafer.

Vapor etching, which was used to try and remedy the effects of slice overheating, can also provide anomalous surface structures. Phosphorus trichloride was passed directly into the seed zone to etch the surface of the crystal; however, the surface became rough and matte as shown in Figure 6.

In addition to the growth process induced defects, the preparation of the wafers for growth is a critical step in achieving an epilayer free of surface defects. The procedure used to polish and clean the iron-doped indium phosphide slices is given below. The samples are waxed to a large glass block using a mixture of beeswax and resin. Excess wax is removed using trichloroethane. The samples are chemically polished on a rotating Pellon pad as shown in Figure 7, using a mixture of 50:50:2 methanol:water:bromine. The water is added to the mixture to prevent the Pellon pad from becoming detached from the underlying glass polishing plate. One hundred micrometers is removed from the face of the wafer and a final high polish is given in a 1/4% solution. The slice is kept wet with cold methanol and the block transferred to boiling isopropyl alcohol. The slice floats off and is transferred wet to a Soxhlet

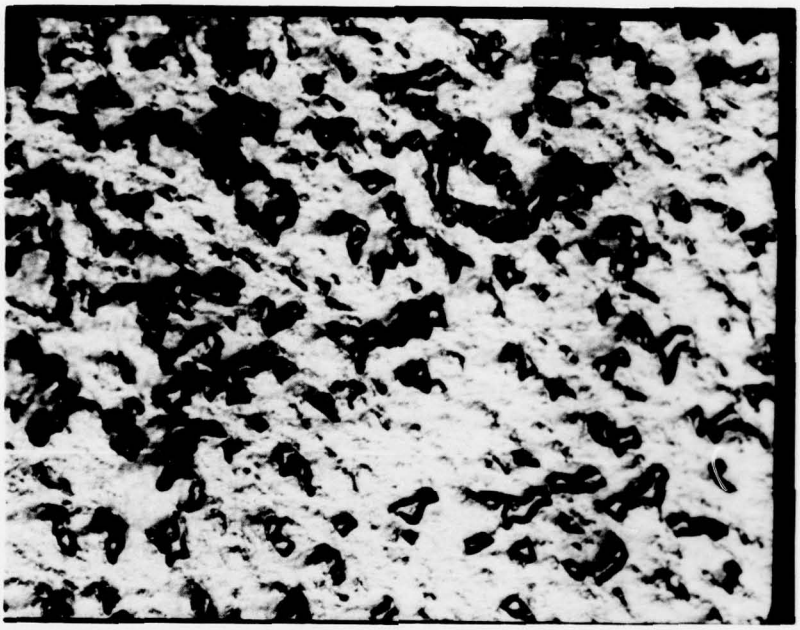

Fig. 4 InP VPE Sample Showing the Effects of Phosphorous Dissociation During Reactor Heating Prior to Deposition

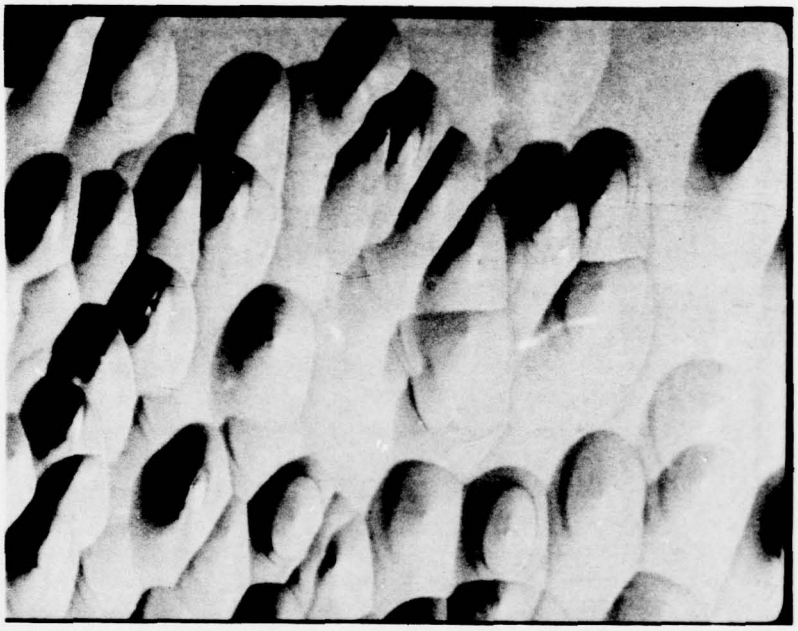

Fig. 5 InP VPE Sample Exhibiting Growth Hillocks from On Orientation Substrate (Mag. 100X)

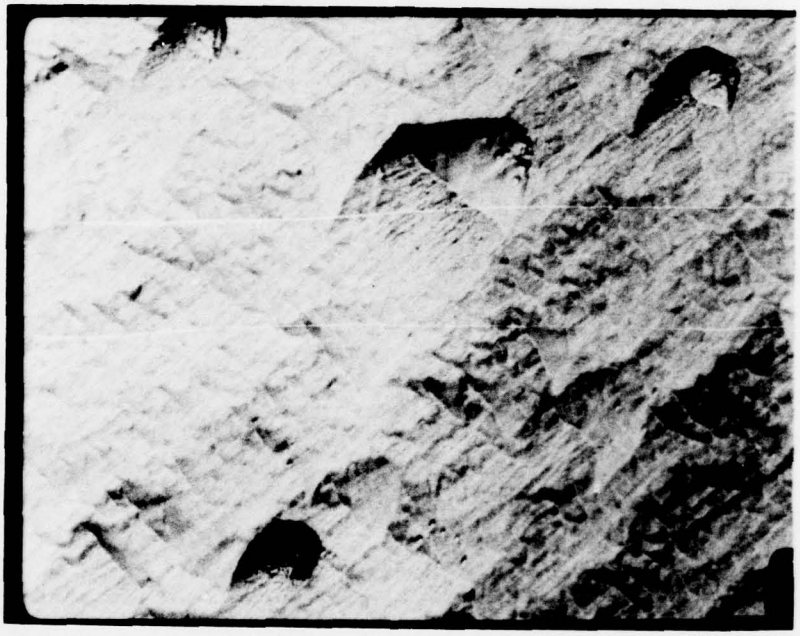

Fig. 6 InP VPE Sample Showing the Effects of Over-etching the Substrate (Mag. 100X)

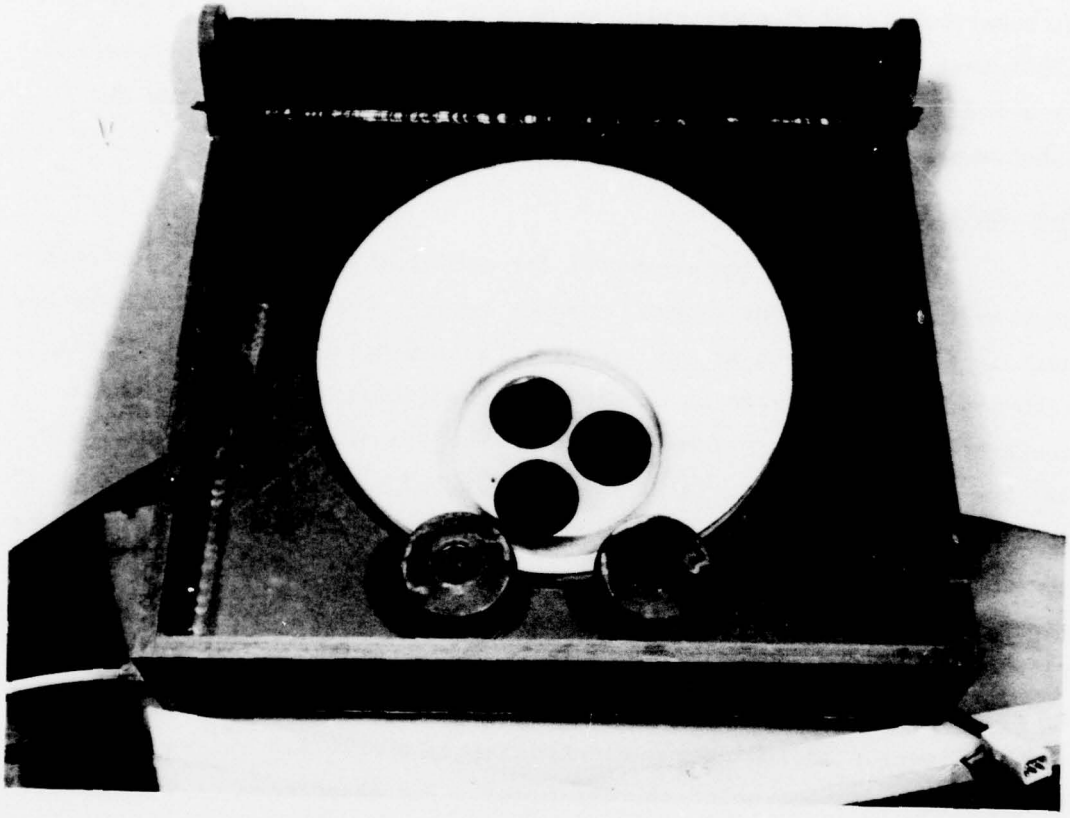

Fig. 7 Polishing Machine

cleaner. Figure 8 shows the Soxhlet cleaner filled with electronic grade isopropyl alcohol. After washing several times, the samples are removed. They instantly dry and show no drying or blowing marks and are perfectly clean. The wafers are then waxed, polished side down to the glass block, and the same procedure is carried out. The wafers are loaded directly from the Soxhlet into the reactor. Figure 9 shows the micromorphology of the epitaxial surface of a wafer oriented 2% off (100) that has undergone the previously outlined procedures for preparation and growth. The surface is specular and exactly replicates the substrate.

2.4 Multilayer Growth

Multilayers are essential for optimization of device performance. High resistivity buffer layers, channel layers, buried channel layers and surface contact layers are all required on a routine basis. The first priority is to determine an accurately reproducible growth rate and a characterized doping system. Figure 10 shows a plot of the growth rate vs time for the reactor. A growth rate of 1500 Å/min is achieved over the total of seven runs. The influence of unpredictable saturation times for the indium source was prevented by observing saturation through a gold plated mirror in the blind end of the roll-on furnace. Knowing the growth rate, it is possible to produce multilayers within the epitaxial layer by switching and timing the gas flows. Figure 11 shows the control panel for the reactor including the electronically controlled valves and timers for accurate sequencing of the gas flows. The dependence of the carrier concentration on the pressure of hydrogen sulfide in the reactor seed chamber is shown in Figure 12. Because of a well established growth rate and dependence of carrier concentration on the hydrogen sulfide pressure, it is possible to switch the dopants and phosphorus trichloride flows to produce multilayered crystals. Figure 13 shows the capacitance voltage profile of a structure 0.5μ thick at $\sim 5 \times 10^{16}$ cm^{-3} on a 3 buffer layer. The channel depleted out, but the buffer at $<10^{14}$ cm^{-3} can be clearly seen. A phenomenon which is identified as an interface rise occurred at the interface between the buffer layer and the substrate. The interface

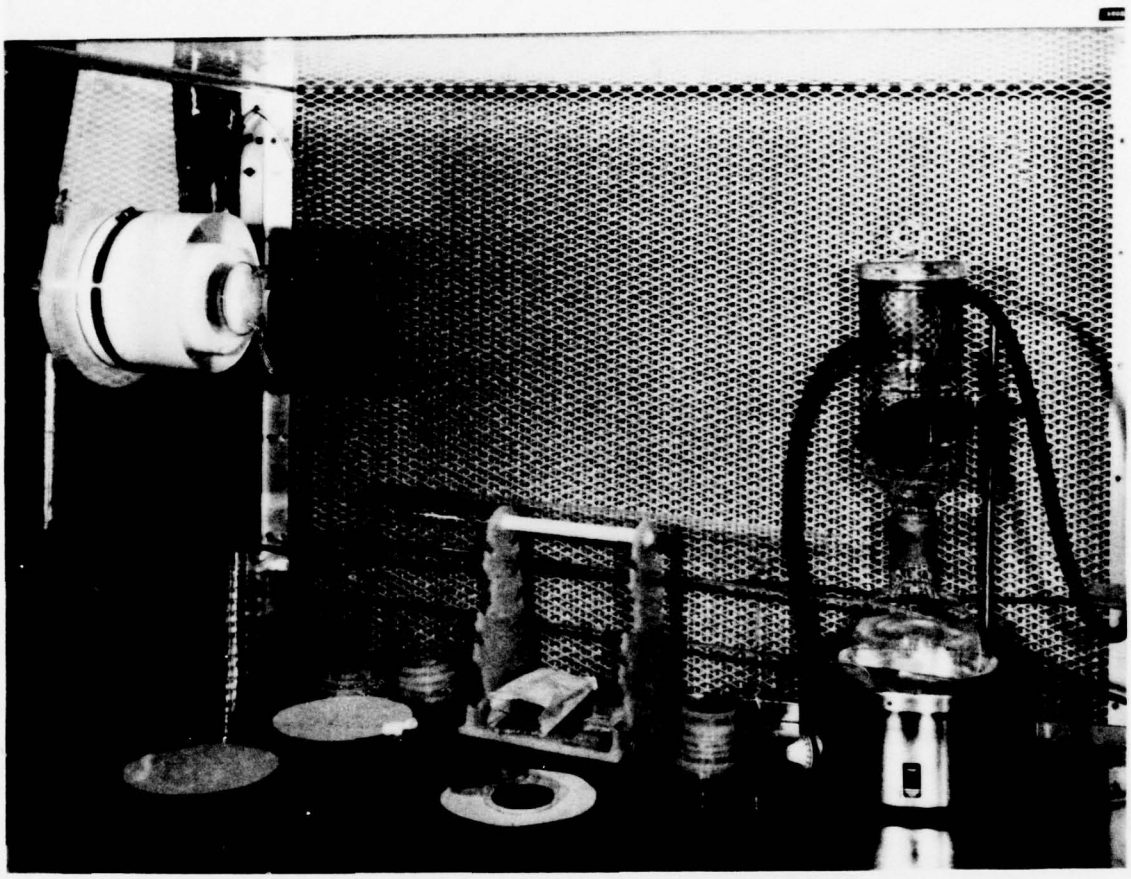

Fig. 8 Vapor Degreasing Soxhlet for Pre-cleaning InP Substrates

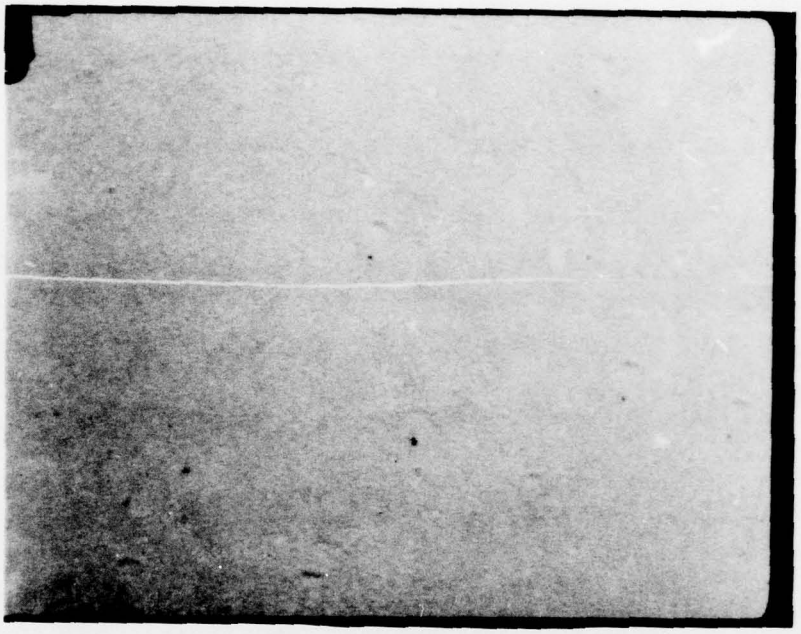

Fig. 9 InP VPE Sample Exhibiting Device Quality Morphology (Mag. 100X)

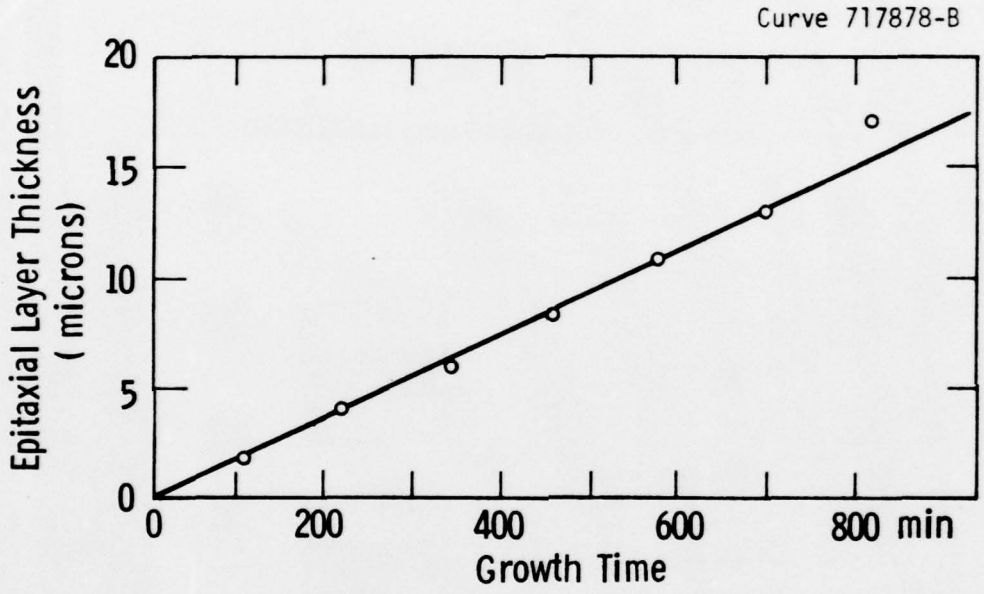

Fig. 10 – Epitaxial layer thickness vs. reactor growth time

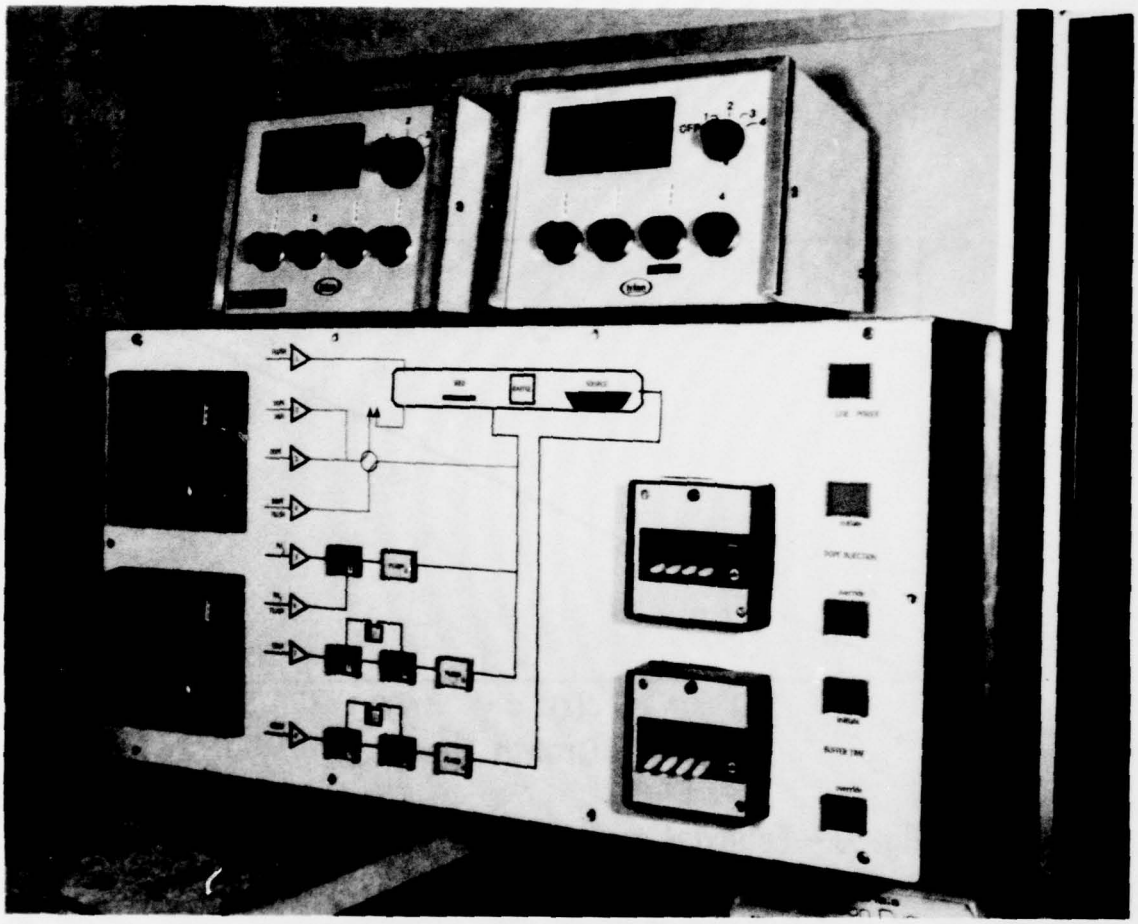

Fig. 11 Automated Reactor Control Panel

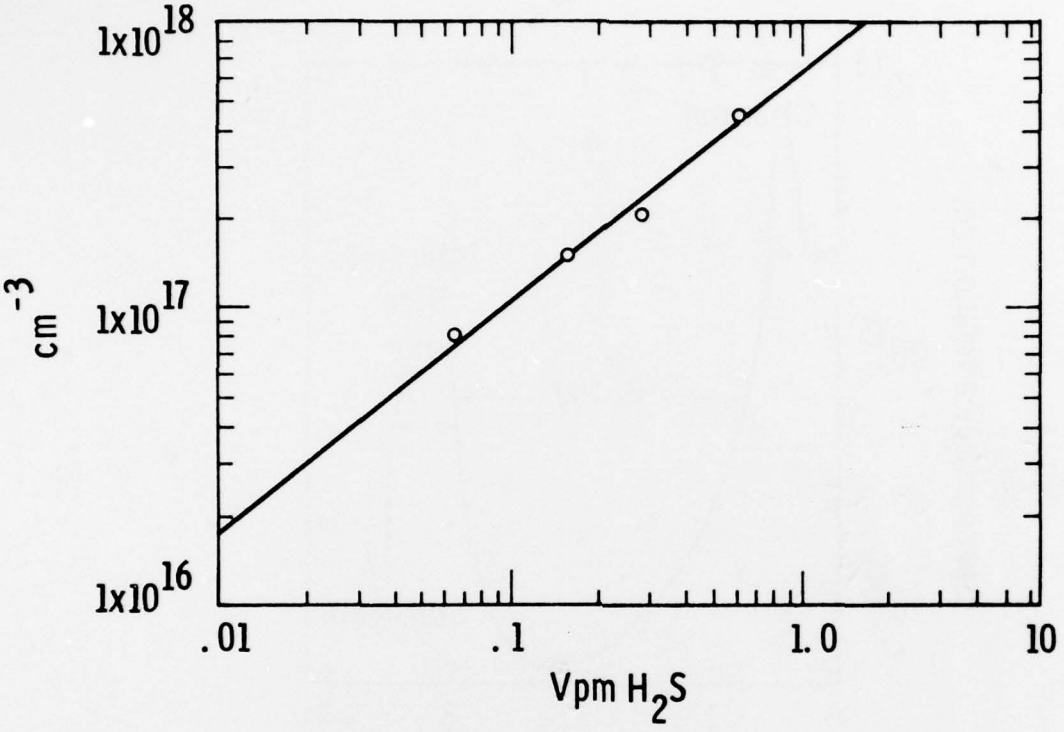

Fig.12 – The concentration of H_2S over the seed wafers is plotted against the carrier concentration in the grown crystals. Conditions for growth were maintained as in Fig.10 except for a varying sulfur concentration

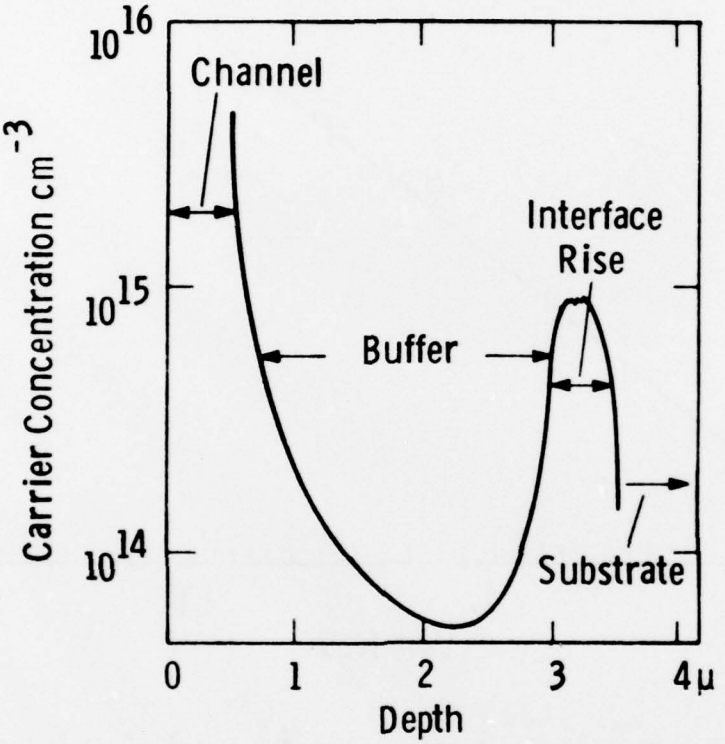

Fig. 13— The depth-carrier concentration profile of an epitaxial structure illustrating the interface problem

rise is an unintentionally high carrier concentration at the substrate epilayer interface. The interface rise is n-type and has electron mobility of ~1000 cm^2/volt sec at room temperature. Table I gives the Hall data for consecutively grown epitaxial layers. The thicker the buffer layer the less the impact of the interface rise is felt. It is impossible to grow device quality buffer layer-channel structures until the interface problem is solved. Likewise, the anomalous rise in doping prevents growing the channel directly on the substrate.

The Fe-doped InP substrates do not exhibit the surface conversion due to heat treatment that is observed in GaAs Cr-doped material. Therefore, it is believed that problems may be associated with the epitaxial starting transient or the gas phase stoichiometry. Experiments are underway to determine the appropriate reactor conditions necessary to eliminate this problem.

Sulfur-doped channels were made by injecting H_2S into the seed zone with automatic sequencers. Figure 14 shows a buried channel structure that could enhance the gate properties and linearity of the final device. A cleaned and stained cross section of the same layer is also shown. The stain used was a ferricyanide-KOH mixture.

2.5 Wafer Characterization

One of the most significant characterization techniques for FET wafers is the capacitance voltage profile. From it one may determine the thickness of the channel, the carrier concentration, the pinch-off voltage and the uniformity. The low Schottky barrier height of metals to indium phosphide has hindered conventional C-V analysis of FET material. The breakdown voltage of 10^{17} cm^{-3} indium phosphide was only a few volts, even with native oxide-assisted structures.[6] Marginal improvements using electrolytes have also been published.[7] Work with Silox-coated indium phosphide layers has enabled the profiling of FET layers of indium phosphide routinely.

Nondestructive carrier profiling was performed using two closely spaced mercury contacts[8] with a coaxial mercury vacuum probe[9]

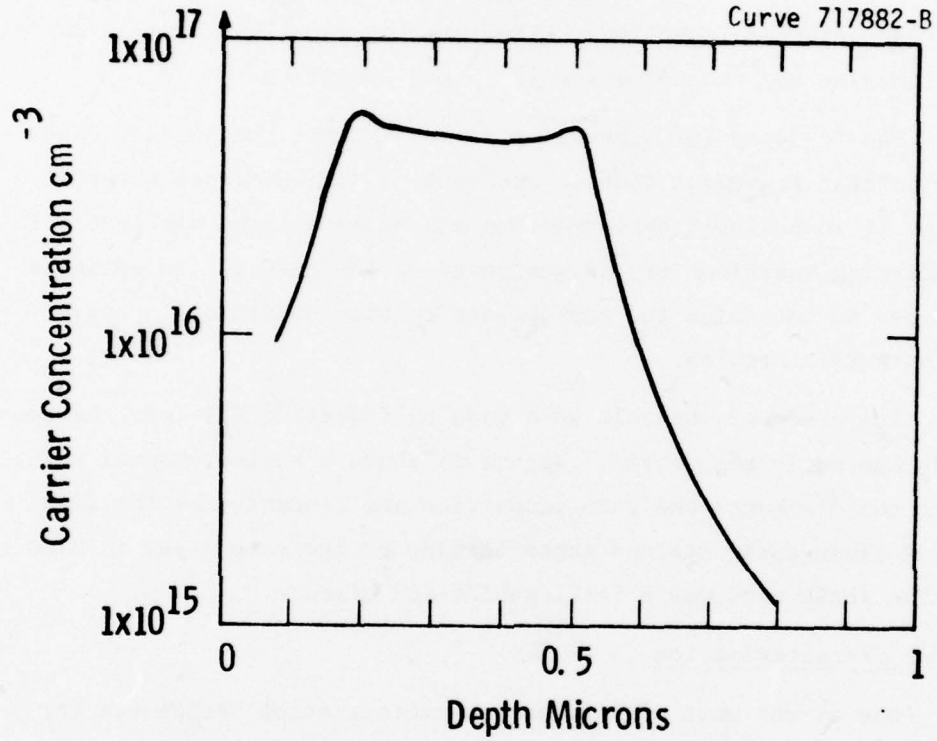

Fig. 14 — This is the profile of a buried channel structure. Both rising and falling interfaces are limited by debye spreading of the carriers

and a Miller profiler.[10] The two Schottky barrier approaches require no ohmic contact and the coaxial probe minimizes series resistance, a problem with FET channel profiling.[11] The outer coaxial contact was much larger in area than the central test diode and contributed little error to the measurement.

Epitaxial wafers were rinsed in HF and high purity water to remove any reactor by-products and then 'Silox' treated. "Silox" (SiO_2) was deposited on the wafers using a travelling plate system,[12] where the samples experienced an atmosphere of nitrogen and silane and some oxygen (2 - 3%). Deposition occurred at 60Å per 30-second pass at 420°C. Improvement in the breakdown voltage of the mercury oxide semiconductor diodes as the oxide was added was dramatic, as was the depletion depth in the FET channel. Figure 15 shows how the FET channel could be depleted into pinchoff as the oxide thickness in the diodes was increased. Routine characterization measurements of the carrier concentration and voltage breakdown were performed using 200Å of oxide.

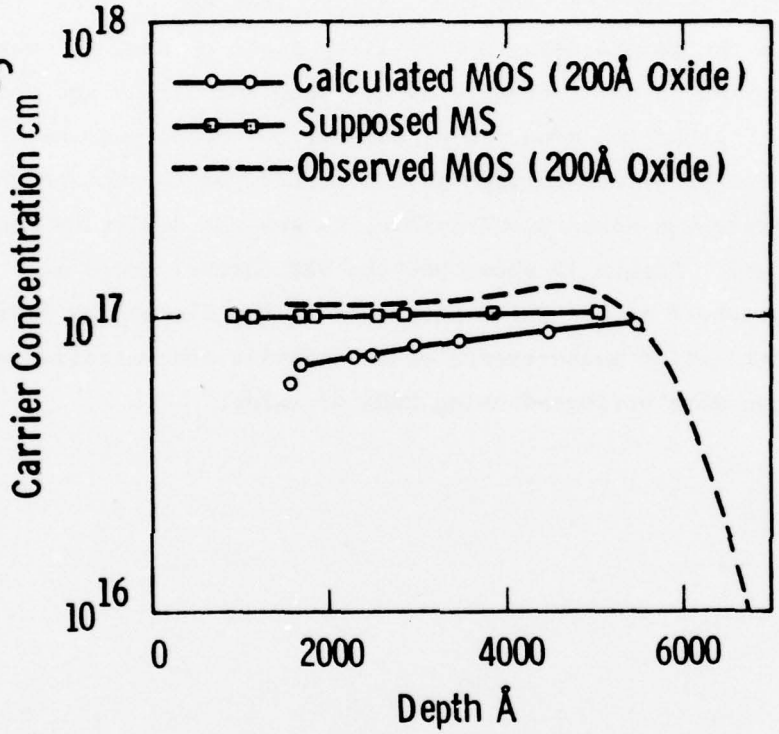

Fig. 15 — The observed (Miller) carrier profile of an epitaxial layer compared to calculated and supposed versions of the same

3. ION IMPLANTATION

Ion implantation (I^2) is a semiconductor doping technique that can be used either to complement VPE growth or can stand alone for the fabrication of InP power FET structures. For example, ion implantation can be used to:

1. Produce n^+ source and drain pads for simplified ohmic contact formation with reduced contact resistance parasitics and improved breakdown characteristics.
2. Provide large area, active channel wafers with accurately controlled depth and concentration characteristics.
3. Tailor the active channel profile for more nearly constant FET transconductance.
4. Provide p^+ selective doping for JFET gates.
5. Provide a completely selective doping technology that eliminates the need for mesa isolation, and results in a planar structure.

InP implantation technology has borrowed heavily from the existing GaAs technology; the InP learning curve has been much more rapid as a result. Westinghouse has shown InP offers several distinct advantages over GaAs:

1. InP(Fe)provides a suitable semi-insulating substrate for ion implantation that does not exhibit anomolous compensation or conversion phenomena. As a result, ingot qualification and activation efficiency calibration is largely avoided and selective implants can be performed with impunity. Westinghouse ion implantation work with similarly grown LEC GaAs suggests that the uniformity and reproducibility of activation efficiency in InP may

be associated with the growth technique rather than being inherent to the compound.

2. Sulfur implants of InP(Fe) yield constant activation efficiency for doses of 2×10^{12} to $2 \times 10^{15}/cm^2$. At the upper dose limit this yields 30 /square layers with free electron concentrations of $5 \times 10^{19}/cm^2$, at the surface. The implanted profile is not appreciably broadened by the activation anneal. This concentration exceeds the GaAs limit through routine processing by a factor of ten. Ohmic contact to $5 \times 10^{19}/cm^8$ material should not require alloying if native oxide removal is complete; a single metal FET fabrication process is a possibility.

3. Silicon implants of InP(Fe) yield respectable activation efficiencies at FET channel doses with Hall mobilities that are 90% of the calculated drift mobility. Electrical activity profiling again demonstrates that the ion implantation profile integrity is retained through annealing.

4. Beryllium implants of InP(Fe) yield p layers with high activation efficiency and good profile integrity. Preliminary results on magnesium implants, which are more attractive for shallow p^+ gate implants, suggest that similar results can be achieved with Mg implantation.

Absence of a straightforward, reliable Schottky barrier contact to implanted InP has been an obstacle to accumulating data on InP implantation. Some advances have been made on this problem under this program, and an ion implantation approach to a JFET will be more vigorously pursued during the conclusion of the program.

3.1 Encapsulation Technology

An encapsulant for ion implanted InP must prevent vaporization of the phosphorous and simultaneously not absorb indium. The temperature for annealing can be estimated a-priori by comparison with the data on GaAs and scaling by the ratio of the melting points; this is shown in Figure 16. Actual annealing temperature requirements are somewhat lower than these estimates. Si implants require 700°C-715°C to achieve theoretical mobility; higher annealing temperatures may yield higher activation as has been reported elsewhere, but there is no reason to do so. S implant activation does not improve in the 600°C-700°C range and the mobility may in fact decrease. Be activation is complete at 650°C. In short, a selective channel device with selective n^+ source and drain and a selective p gate can be annealed at 700°C. This requires an encapsulant effective to this temperature.

The congruent evaporation temperature of InP is approximately 350°C as is shown in Figure 17, compared to the 550°C value for GaAs. This compounds the encapsulation problem since, ideally, the encapsulant should be deposited at or well below this temperature to avoid creating a surface nonstoichiometry. Westinghouse has investigated a number of possible, low temperature (< 150°C) sputtered dielectric layer encapsulants. None of these layers survive mechanically beyond 650°C. Overlaying these sputtered layers with a better quality, higher temperature dielectric leads to failure at essentially the same temperature. Westinghouse has also investigated plasma enhanced Si_3N_4 encapsulants deposited at 340°C. Si rich plasma Si_3N_4 is an encapsulant that is effective to at least 750°C. However, annealing at 750°C leads to a thin (< 500Å) n^+ conversion layer on the InP surface which may be due to indiffusion of Si from the Si_3N_4 layer. Si deficient Si_3N_4 is mechanically ineffective.

Westinghouse has found that "Silox" phosphosilicate glass deposited at 380°C is an effective encapsulant for InP that meets the 700°C annealing requirement. Silox deposition is essentially a close spaced "pyrolytic" system[13] with gas distribution jets and sample

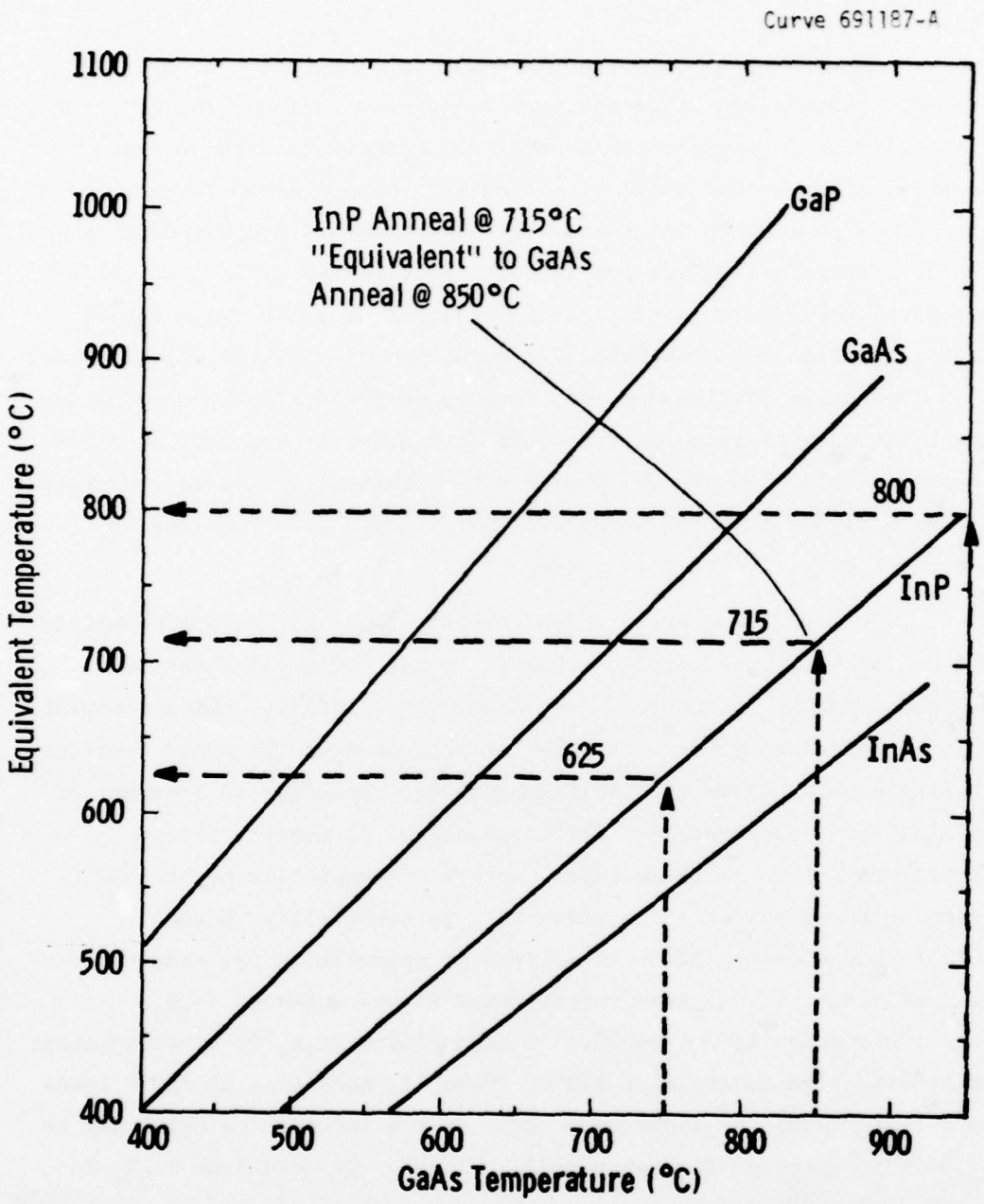

Fig. 16 – "Equivalent" III-V activation temperatures scaled from crystal melting point data to GaAs

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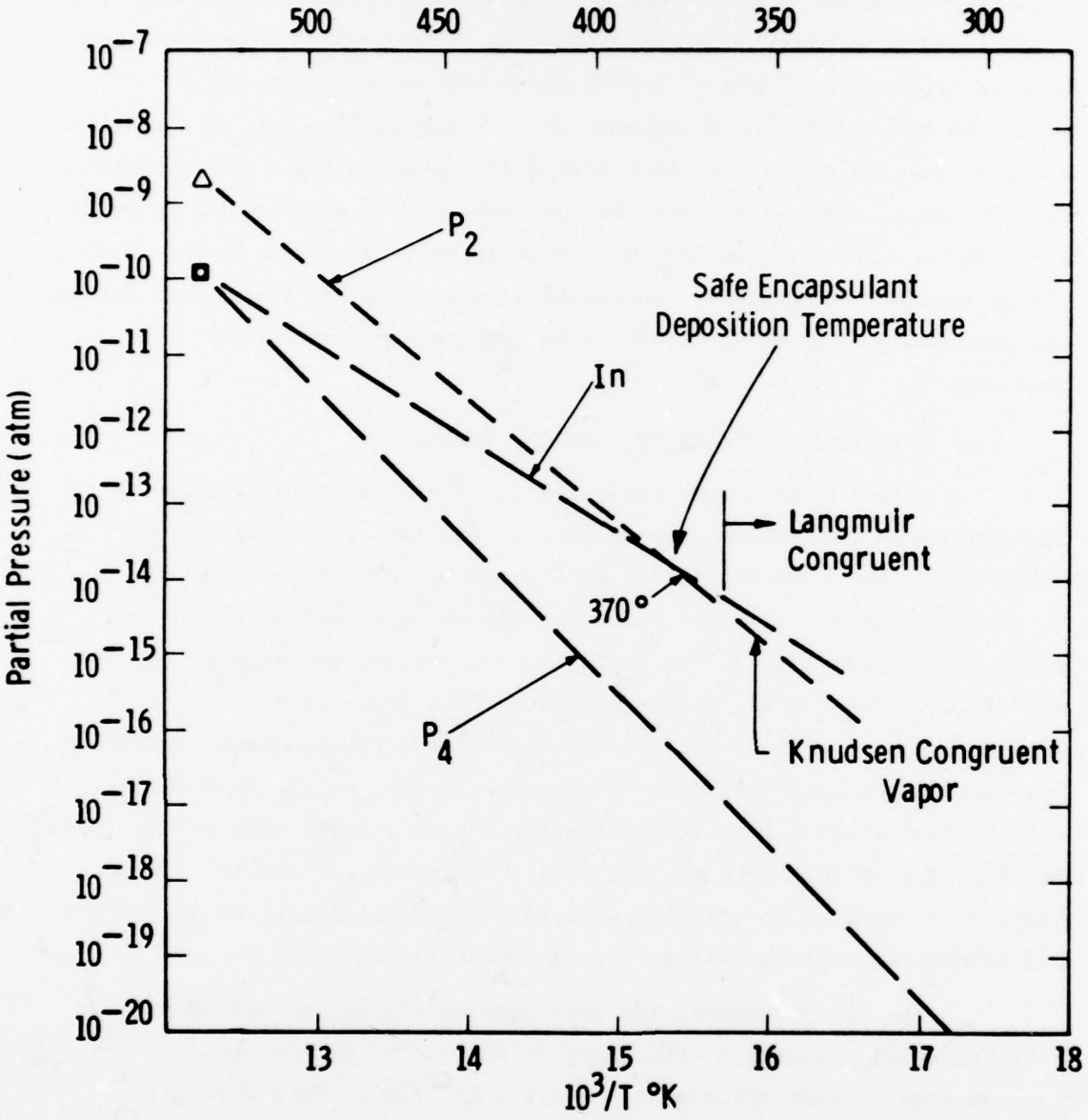

Fig. 17 – Equilibrium vapor pressure on In, P_2, and P_4 over InP (after R. F. C. Farrow, J. Phys. D, Appi. Phys. 7, 2436 (1974)

traverse mechanism to allow very fast deposition with good uniformity. 500Å of 7A% phosphosilicate glass (PSG) is first laid down at 380°C and this is followed by 2000Å of 11A% P doped PSG deposited at 380°C. P doping of the glass retards absorption of P and In from the InP; plastic flows of the 11% glass minimizes stress during annealing. Conventional CVD PSG can be used to achieve the same result. It does appear, however, that native oxides on the InP lay a role in protecting the surface during the encapsulant deposition. This native oxide tends to break down during the long heatup and stabilization time required in conventional CVD reactors.

3.2 Silicon Activation and Channel Implants

Figure 18 shows the activated donor concentration versus implanted dose for ambient temperature Si implants into InP(Fe) with 700°C annealing. The activation data is extracted from van der Pauw Hall measurements. The data spans a range of experimental conditions which are listed in detail in Table II. In particular, samples #3, #9 and #13 were $A\ell_2O_3$ grid polished followed by a 3000Å free etch in bromine methanol while the remainder were bromine methanol etch polished followed by the same free etch. Reduced activity for the grid polished samples demonstrates that this polishing damage extends well behond 3000Å. Samples #9 through 13 are in fact full 2" diameter InP slices. These samples, as well as the remainder, exhibit good uniformity of activation and remarkable reproducibility for an infant technology.

The well-prepared, low dose samples #'s 10, 11 and 12 exhibit a differential activation efficiency of 65% and an extrapolated compensation concentration of $0.4 - 0.6 \times 10^{12}/cm^2$. This value is consistent with the surface depletion expected from 0.6 eV surface barrier. Since this depleted charge is not measured using the Hall technique, this compensation concentration is probably not a bulk effect.

The 150 kV Si implants exhibit saturation of the active concentration at a value of $1 \times 10^{13}/cm^2$. Theoretical calculations of the Si profile imply, in turn, saturation at the $5 \times 10^{17}/cm^3$ level.

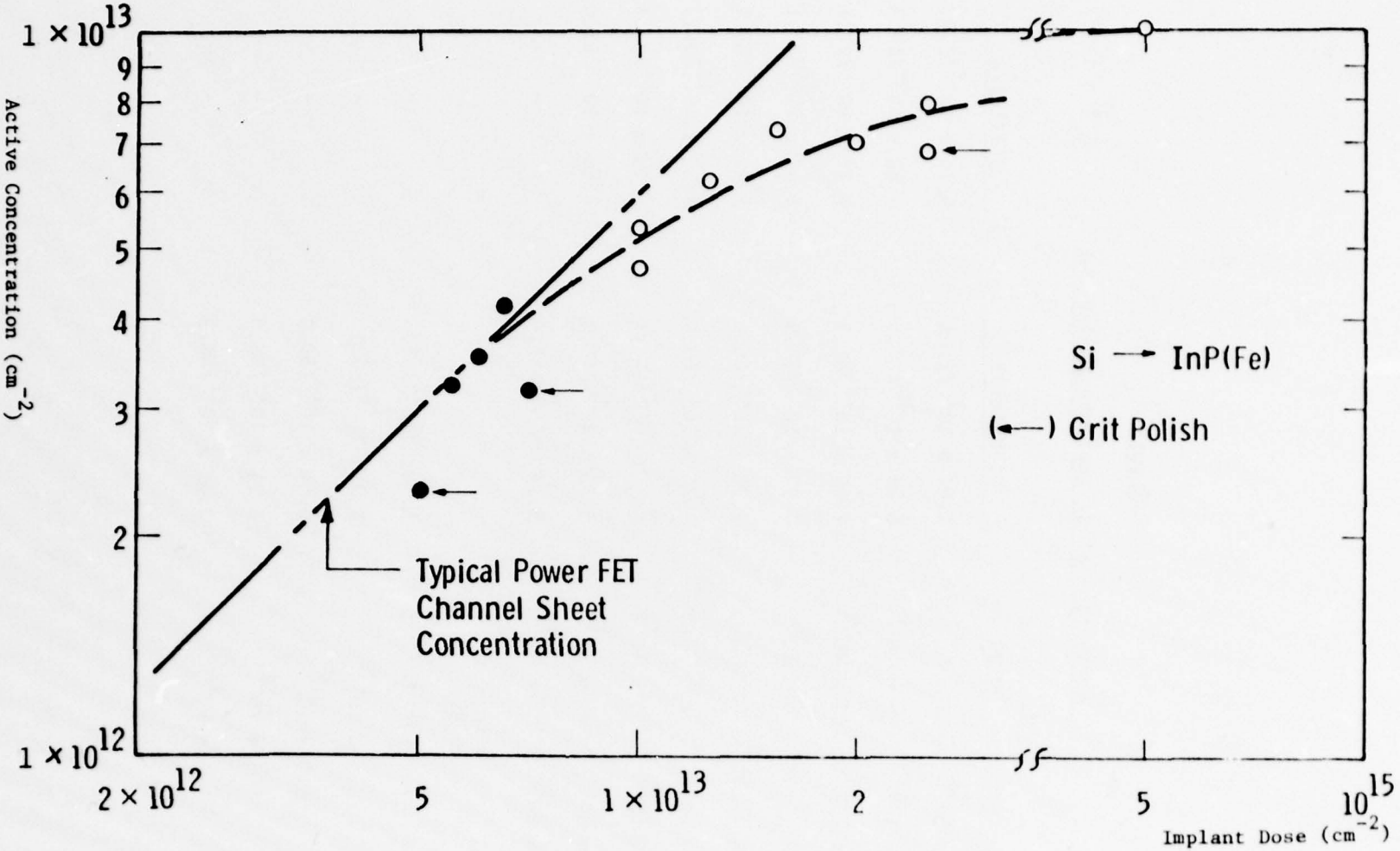

Fig. 18 Si Carrier Activation VS Implant Dose Demonstrating Saturation Limit of $\sim 9 \times 10^{12}/cm^2$

TABLE II

Activation of Si Implants in InP(Fe)

	Q in 150 KV	Q in 50 KV	Q(300°K)/%	Q(77°K)/%
1.	5×10^{14}	0	1.02×10^{13}/2.04	9.16×10^{12}/1.83
2.	2×10^{13}	5×10^{12}	6.88×10^{12}/27.5	4.82×10^{12}/19.3
3.	2×10^{13}	5×10^{12}	7.89×10^{12}/31.5	6.77×10^{12}/27.1
4.	1.6×10^{13}	4×10^{12}	7.07×10^{12}/35.3	5.42×10^{12}/27.1
5.	1.6×10^{13}	-	7.38×10^{12}/46.1	5.72×10^{12}/35.7
6.	1×10^{13}	2.5×10^{12}	6.20×10^{12}/49.6	4.52×10^{12}/36.2
7.	8×10^{12}	2×10^{12}	4.7×10^{12}/47.1	3.76×10^{12}/37.6
8a.	8×10^{12}	2×10^{12}	5.33×10^{12}/53.3	4.10×10^{12}/41.0
8b.	8×10^{12}	2×10^{12}	5.14×10^{12}/51.4	-
	Q in 400 KV			
9.	7×10^{12}		3.18×10^{12}/45.5	-
10.	6.5×10^{12}		4.2×10^{12}/64.5	-
11.	6.0×10^{12}		3.54×10^{12}/59.0	-
12.	5.5×10^{12}		3.24×10^{12}/59.0	-
13.	5.0×10^{12}		2.31×10^{12}/46.3	-

This calculation assumes that the Si profile follows LSS theory and that it does not spread on annealing; these assumptions are shown to be valid below. Higher concentrations can be achieved by hot implants and/or higher temperature anneals but this is not necessary for channel implants. These hot implants ($\approx$ 200°C) are awkward due to both the limitations of production ion implantation machines regarding heating and the inability to use photoresist for selective implants. Thick phosphosilicate encapsulant layers can be employed for selective implants if the apertures are prepared by ion milling.

Hall profiling experiments determine the quantities

$$\Sigma(z) = \int_z^\infty G(z')\, dz'$$

$$M(z) = \int^\infty \mu(z')\, G(z')\, dz/\Sigma(z)$$

where z' is the depth variable and its lower limit is determined by etching plus surface depletion; $\Sigma(z)$ is the remaining conductance and $M(z)$ is the indicated mobility average. This measurement was performed on sample #16 and the $\Sigma(z)$ and $M(z)$ data is shown in Figures 19and20, respectively. Computer assisted analysis would be required to extract $n(z)$ and $\mu(z)$. Variations in $M(z)$ are negligible to first order so it is possible to make preliminary estimates of $n(z)$. This estimate indicates good agreement with the predicted, joined half guassian profiles (R_{max} = 3500Å, $G_{shallow}$ = 1500Å, and G_{deep} = 900Å); there is no anomaly in the surface activity.

Figure21 shows the Hall mobility [M(o)] of the samples listed in Table II as a function of active donor concentration. The theoretical mobility curve (μ vs. $N_D(cm^{-3})$ is included assuming a 1500Å conducting layer thickness; this width is appropriate for the 150 kV implants only and the 400 kV data is highlighted with arrows. With the exception of grit polished samples and samples with peak concentrations below $1 \times 10^{17}/cm^3$, the mobility exceeds 85% of the theoretical limit. The data imply that an implant with an active channel dose yielding

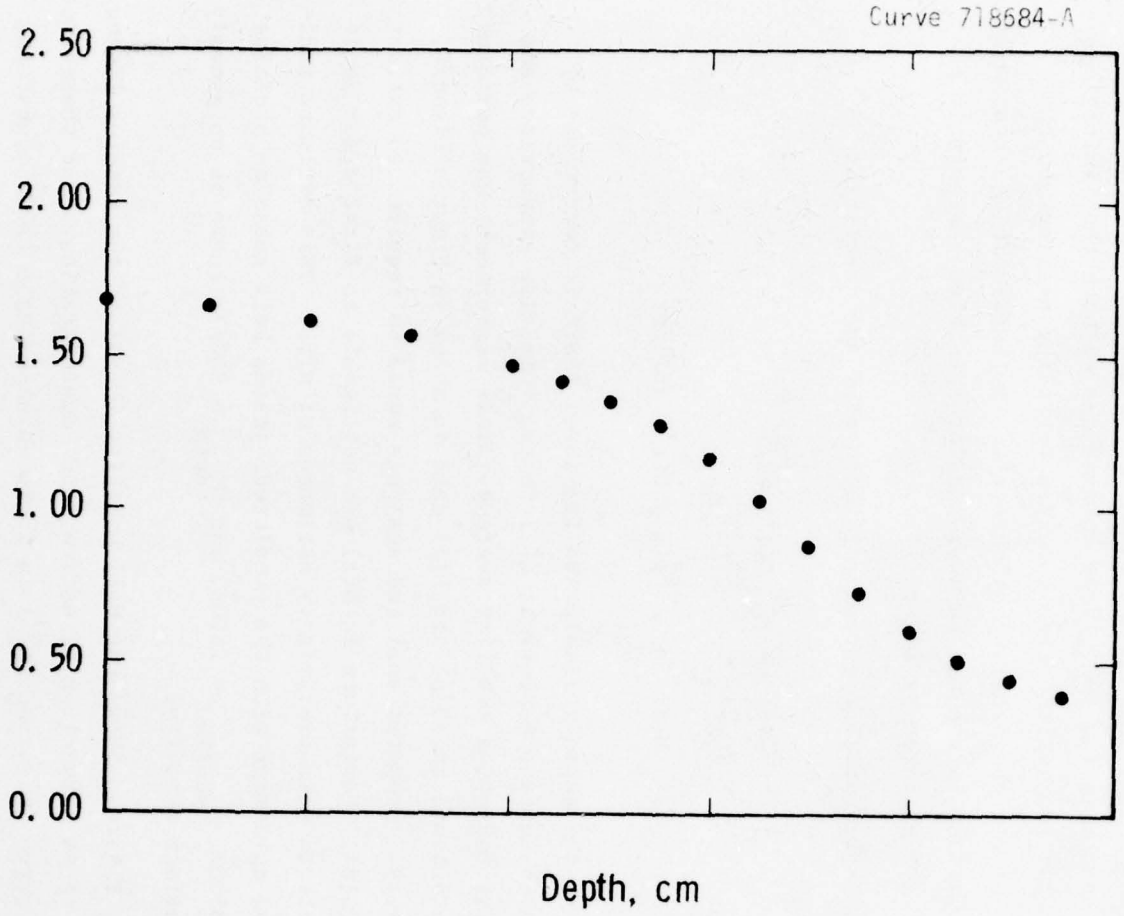

Fig. 19 – Conductivity vs. depth for differential hall measurement on ion implanted InP

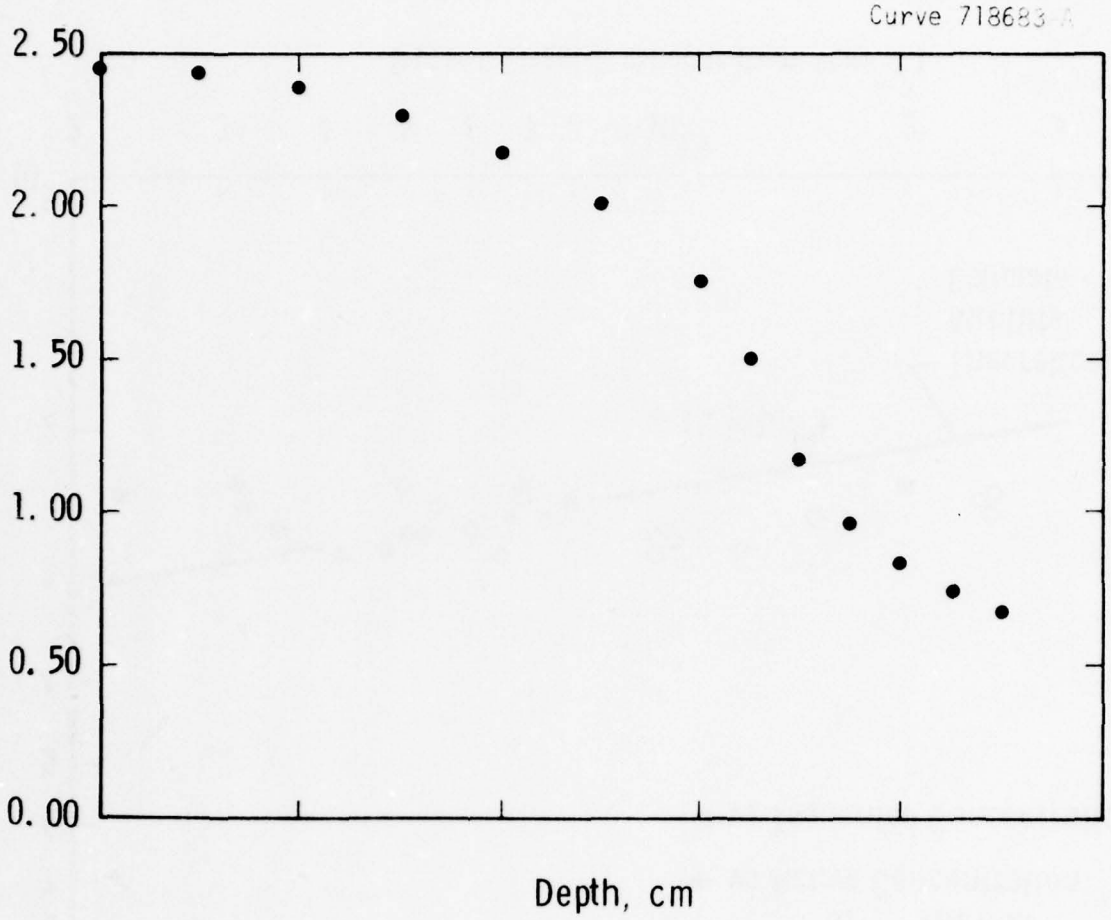

Fig. 20 – Hall coefficient multiplied by conductivity squared for differential Hall measurement on ion implanted InP

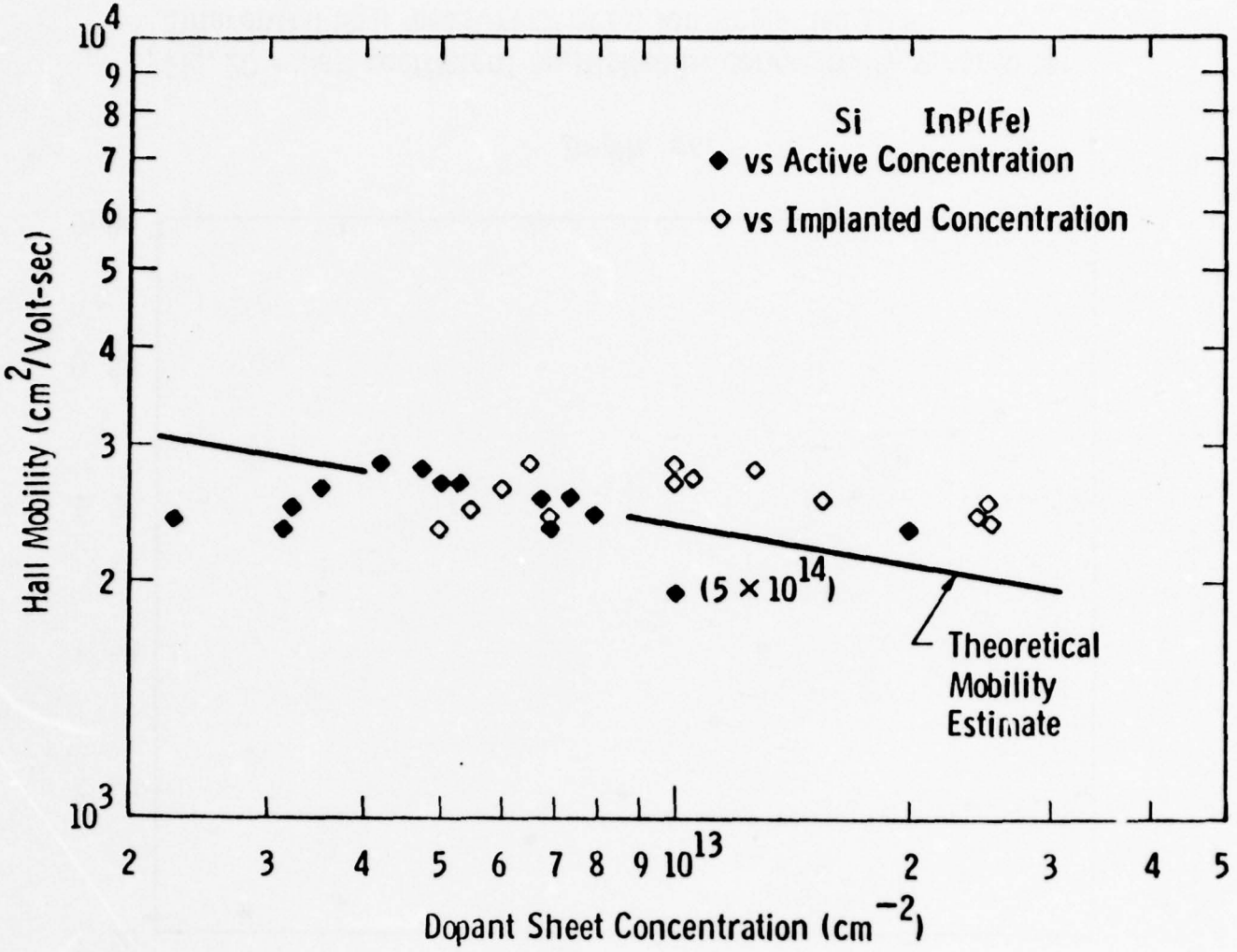

Figure 21 Mobility vs Sheet Concentration Demonstrating Near Theoretical Transport for Si Implantation in InP

4-4.5 x $10^{12}/cm^2$ donors yields a mobility of 2750 cm^2/volt sec with confidence. This concentration includes a 1-2 x $10^{12}/cm^2$ concentration that is later removed either in forming a gate recess or in forming a p^+ gate.

3.3 Sulfur Implantation and n^+ Contacts

Sulfur substitutes on the phosphorus sublattice as opposed to silicon which substitutes on the indium sublattice; hence, distinctions in their activation characteristics might be expected. Figure 22 shows the active concentration as a function of dose for $^{32}S^+$ implants. For 700°C anneals, the activation efficiency remains constant at 30% throughout the usable dose range. Despite the low activation efficiency, the highest close datum corresponds to a 30 Ω/□ layer which is quite adequate for ohmic contact source and drain pads.

The profile of high dose implants has been measured to determine if the integrity of the sulfur profile is adequate for selective n^+ contacts. Figure 23 shows the chemical profile after 650°C annealing; the solid line shows the chemical profile before annealing. The latter is in good agreement with LSS theory while the former shows simple Fickian diffusion with a diffusion coefficient of 3 x 10^{15} cm^2/sec. The data points near the surface suggest outdiffusion but are, in fact, an artifact due to matrix effects. Profiling through the encapsulant demonstrates that outdiffusion does not occur. Hall profiling demonstrates that the surface S activation is equivalent to the average value. Surface concentrations of 5 x $10^{19}/cm^3$ are achieved by ambient temperature S implants to 2 x $10^{15}/cm^2$. At these concentrations the Schottky barrier width of a deposited metal is 50-100Å. Since this width allows low voltage tunneling, an InP FET with single level metallization and no contact forming becomes a real possibility.

Figure 24 shows the electron mobility of S implanted layers as a function of dose. The range of mobility for Si implants is indicated by the cross-hatched zone. Clearly S implants are not appropriate for active channels. A significant improvement in the S implants are not

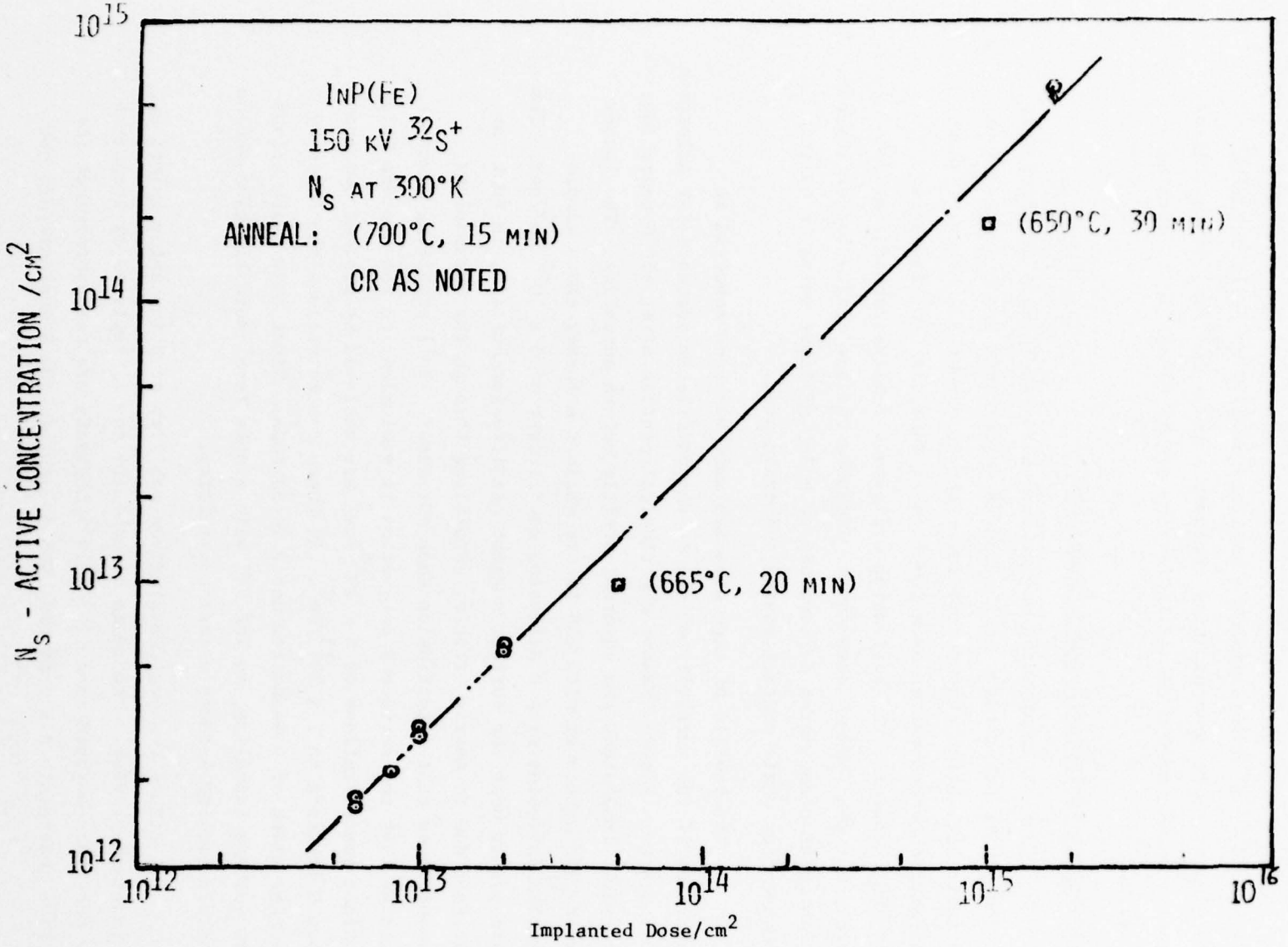

Figure 22 Active Concentration vs Dose for $^{32}S^+$ Implants in InP(Fe)

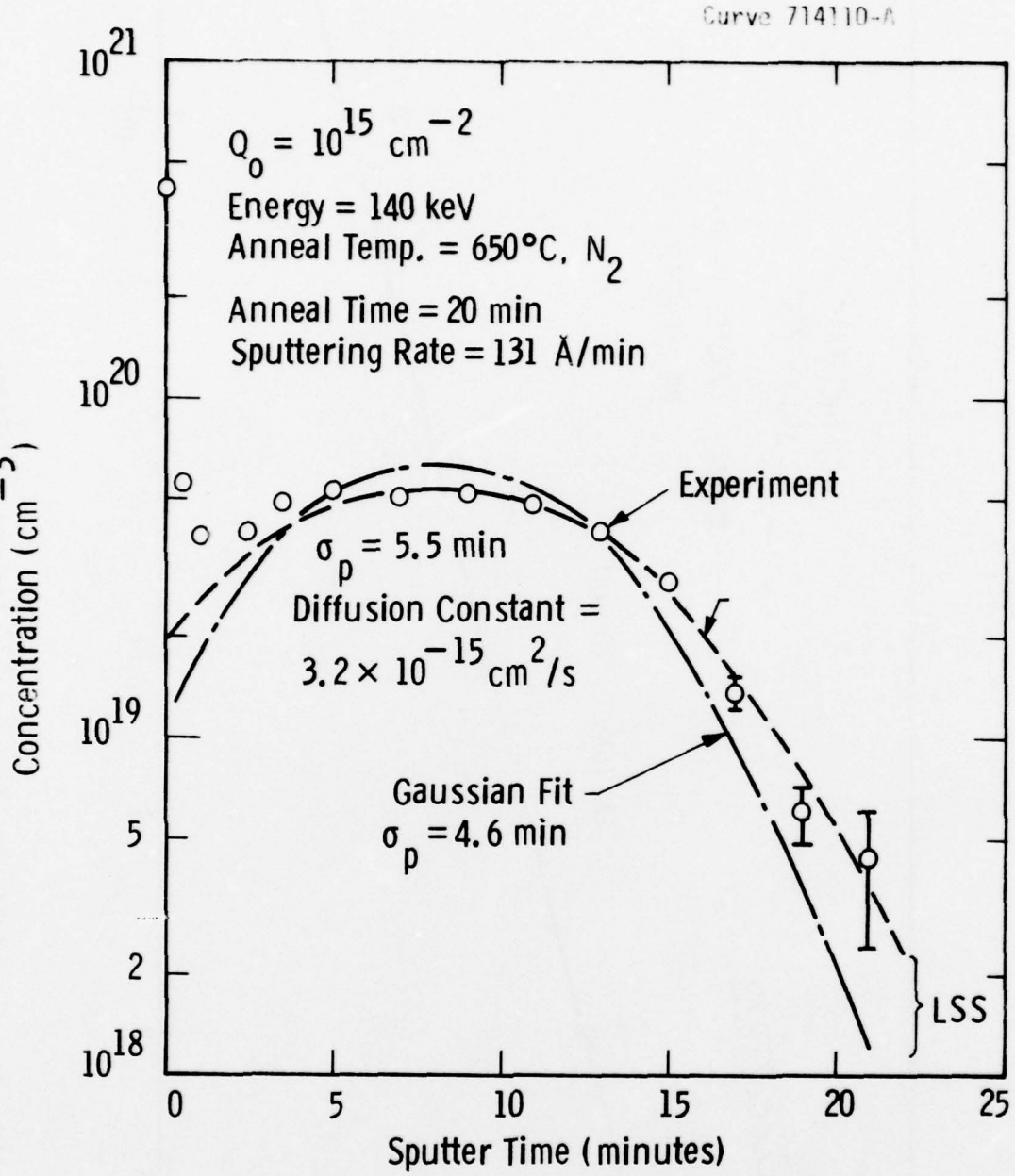

Fig. 49 – AES profile of S implant in <100> Cr-doped InP after 650°C anneal

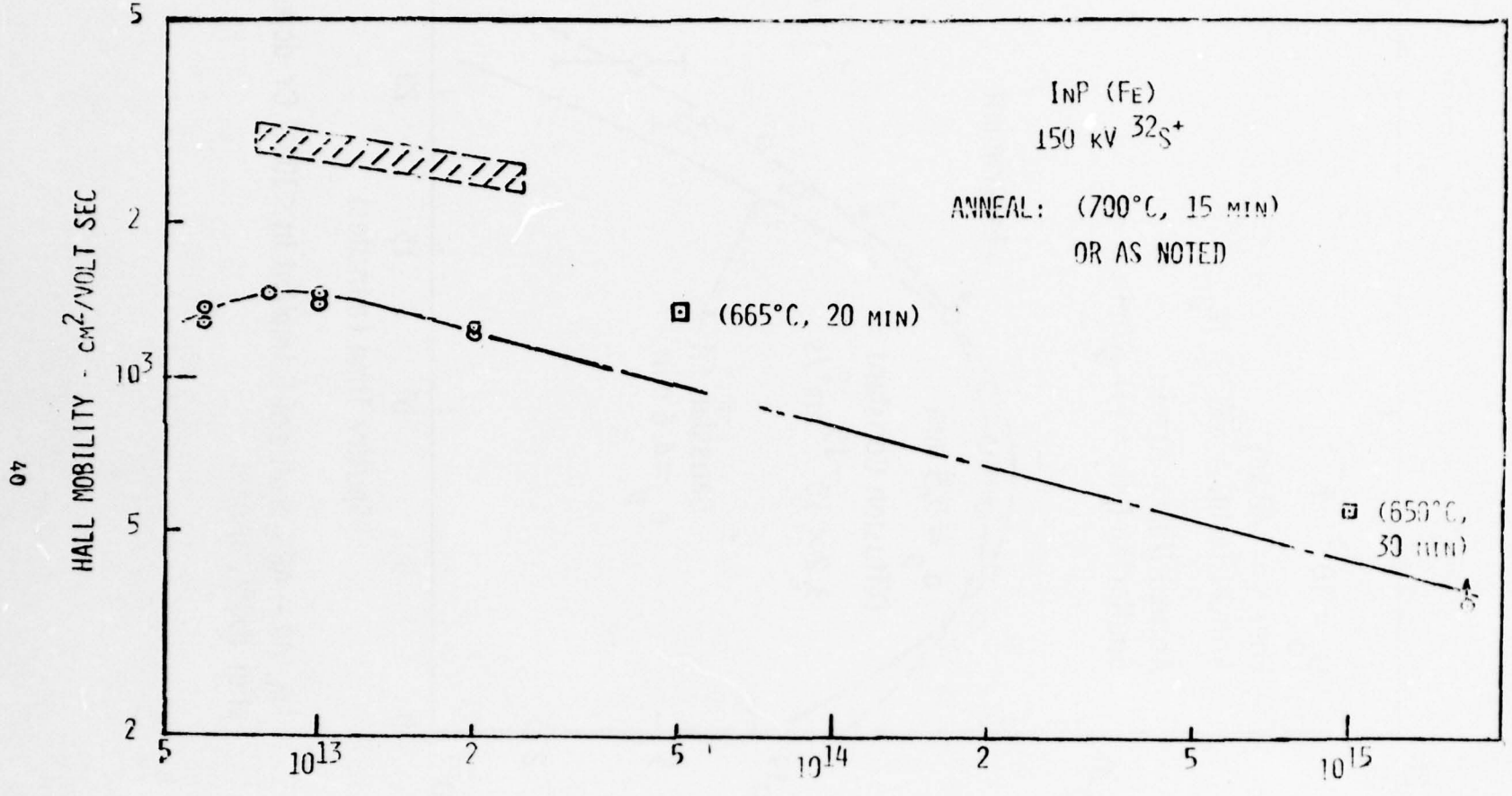

Figure 24 Electron Mobility vs. Dose for $^{32}S^+$ Implants in InP(Fe)

appropriate for active channels. A significant improvement in the S implanted mobility could be achieved through hot implants.

3.4 Be and Mg Implants for p^+ Gates

Westinghouse has achieved p layer formation using beryllium and magnesium implants. Implants of the heavier group II species (zinc and cadmium) were not successful initially and were not pursued further since they are not expected to retain the shallow, sharp profile required for a p^+ gate.

Table III summarizes the Hall data for Be test implants. Activation efficiency is excellent and the mobility is consistent with bulk results. Be, however, is not a good choice for shallow p^+ implants. The acceptor concentration required is $> 9 \times 10^{17}/cm^3$ for good transconductance ($\lambda_A < \lambda_D/10$) and this places the metallurgical junction at $R_p + 2\sigma_p$ for a $1 \times 10^{17}/cm^3$ channel. At the lowest convenient implant energy of 50 keV, the metallurgical junction is 3000Å. This is incon--istent with reasonable implanted channel depths. Magnesium implants at 50 kV to the same concentration should yield metallurgical junctions at 1000-1200Å which is equal to the desired value. Work in implantation is now concentrating on Mg implants. Thus far, activation has been inconsistent, perhaps due to the high activity between Mg and O_2. We expect to conclude the Mg study during the second half of the program which will determine its role in the JFET. If Mg does not work, we can use Be in conjunction with thicker epi channel structures.

3.5 Selective Ion Implantation

Westinghouse has used a composite of its InP encapsulant and photoresist for selective ion implantation of InP. The procedure is outlined in Figure 25. The active area is first defined by developing the resist and chemically etching to the InP surface. Care is required to obtain good photoresist on PSG and to avoid severe undercutting during etching. Active layer implants do not result in resist removal problems; since the resist is not in contact with InP, there is no carbonized ring of resist on the InP surface after implant.

TABLE III

Be^{+} I290378-4a

$3.5 \times 10^{13}/cm^2$

	300°K	Est. Acc.	77°K	Est. Act.
ρ_s Ω/	3572	± 4%	6770	± 6%
σ_s Ω^{-1}	2.80×10^{-4}	± 4%	1.48×10^{-4}	± 6%
N_A cm^{-2}	3.01×10^{13}	+ 10% - 25%	2.94×10^{12}	± 20%
μ_p cm^2/Volt-sec	52.75	+ 25% - 10%	313.65	± 20%
Act. Eff.	86%		8.4%	

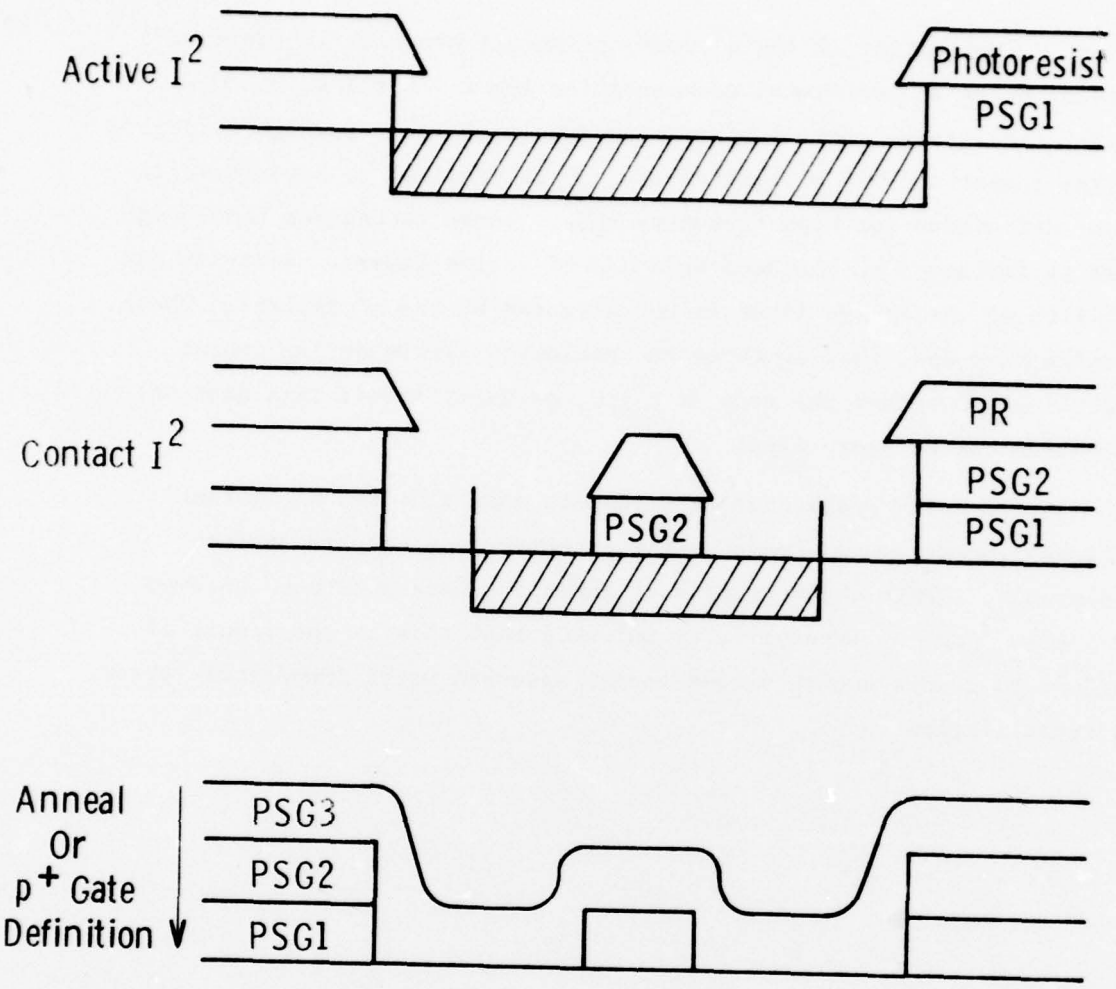

Fig. 25 – Process steps for selective ion implantation in InP (Fe)

Definition of the n^+ contact implant proceeds in the same fashion using an additional encapsulation layer. A thick, 2.5 micron resist facilitates removal after high dose implants. Surface hardening of the resist and ion milling of the PSG is required to achieve sufficient definition for high frequency FETs. These techniques have been used to implant S n^+ contacts on S and Si active layers. Activity and mobility of the active layer is not affected by the n^+ implant. These samples have one, two, or three encapsulation layers during anneal depending on whether the area is n^+, n, or unimplanted; this does not affect annealing properties.

Contact resistance measurements show that the n^+ implant activates normally and leads to the expected reduction in contact resistance. Ohmic contacts without annealing have not been achieved on $5 \times 10^{19}/cm^3$ n^+ layers; it is believed that this is the result of failure to remove native oxides and/or adsorbed water immediately prior to metallization.

4. FET FABRICATION

The fabrication of an InP Schottky barrier FET is virtually identical to that of a GaAs FET in terms of operations sequence, however, there are significant differences in the process steps. These include different etches, different ohmic contact procedures, as well as the need for a special approach to the gate. A significant fraction of the first part of this program was devoted to developing viable gate processes. Initially, it was felt that an "oxide-assisted" Schottky barrier would provide a suitable gate. The process sequence developed to date reflects such an approach; however, the fabrication sequence is sufficiently flexible to allow for modification as better gate processes are developed. As mentioned in the Introduction, it is now believed that a JFET is the best approach to meeting the requirements imposed by a power FET. Preliminary p-n junction work has been encouraging and work is now concentrated in this area.

4.1 Gate Technology

Since the low metal barrier height on n-type InP is a well known problem, it was felt that any ensemble of experiments aimed at a true Schottky barrier would most likely fail. Hence, work has to date centered around three approaches to obtaining gating action. They are:

(A) Alloyed p-n junction

(B) Dielectric-assisted Schottky barrier

(C) Implanted p-n junction.

Table IV is a compendium of the experimental results gathered to date. Clearly, the oxide-assisted barriers displayed the lowest leakage properties; however, they suffered from other problems. The following sections will detail the experiments involved in developing a gate technology and conclude with a direction for the program.

TABLE IV — InP GATE EXPERIMENTS

Gate	Vr	Leakage* Current	Comments
Plated 0.2% Zn/Au	−5.0	0.75A/cm^2 (7.5 μA)	As Plated Results Best, Alloy Degrades Barrier
Plated Zn	−3.0	0.40A/cm^2 (4 μA)	Alloy 1 min. @ 300°C In Ar/H_2
Thin Oxide - Au	−8.0	0.0197 A/cm^2 (0.197 μA)	Treat InP In HNO_3 for 5 min. @ 80°C - Difficult for Device Processing
Thin Oxide - Au	−8.0	0.02A/cm^2 (0.197 μA)	G-HNO_3 Process Sample Held @ 80°C - Compatible With Photoresist
Thin Oxide - Cr/Au	−10.0	5.5A/cm^2 (55 μA)	Plasma O_z Exposure @ 40°C
Thin Oxide - Cr/Au	−15.0	0.001A/cm^2 (0.01 μA)	420°C CVD SiO_z, C-V Hysteresis Present
Thin Nitride - Cr/Au	−15.0	0.001A/cm^2 (0.01 μA)	40°C Si_3N_4 Deposition, C-V Hysteresis Present
P^+ Implant - Au	−10.0	90.0A/cm^2 (0.9 mA)	50 KEV Mg I^2 @ 1×10^{13} 700°C Alloy for 15 min W PSG, 1200 Å Junction Depth

* Current Values in Parentheses Are Scaled for a 1 μ Gate and 1 mm Periphery

(A) Alloyed p-n Junctions

The alloyed p-n junction relies on driving a Group II element into the surface of the InP to convert it to p-type material. Magnesium is extremely reactive with oxygen and is therefore readily corroded. Beryllium is extremely toxic and requires extreme safety precaution; hence the only choices left for deposition on a sample are zinc and cadmium. Since both these elements have high vapor pressures and contaminate evaporation systems, we initially resorted to plating techniques.

Pure zinc was plated onto an indium phosphide sample using zinc fluoborate solution with a pH between 3.0 and 4.0. The as-plated Zn contact exhibited "ohmic-like" behavior; however, annealing improved the barrier slightly. A 1-min alloy at 300°C in Ar/H_2 produced rectifying contacts with a barrier of 0.66 volts as determined by C-V measurements. Leakage is high at -3.0 volts. After a sequence of time-temperature cycles, it was felt that Zn was not driving in, and in all probability was evaporating from the sample.

An alternative approach was a 2% Zn/Au plated contact followed by an anneal. The as-plated contacts displayed leaky rectifying behavior with a barrier of 0.64 volts. An alloy cycle similar to the Zn contact alloy destroyed the rectifying properties. Gold appears to diffuse more rapidly into InP than Zn, causing a poor p-n junction and rendering this metal system inappropriate.[13] New combinations of Zn and other metals are being investigated together with different alloy cycles. Results of these studies along with Auger profiles to determine relative diffusivities will be concluded during the remainder of the investigation.

(B) Dielectric-Assisted Schottky Barrier

The dielectric-assisted Schottky barrier relies on the ability to interpose a thin insulator between the surface of InP and the Schottky metal. Assuming that the deposited dielectric is an ideal insulator with no trapped charge or interface states, the apparent barrier height would be increased, causing the reduction of reverse leakage current.[14] The problem is reduced to providing the following dielectric film properties:

1) Reproducible growth of a thin insulator;

2) Elimination of states associated with the insulator/semiconductor interface;

3) Growth of a dense insulator such that leakage is significantly reduced.

If the insulator fails to meet all of the above criteria, the result is either an MIS device (thick dielectric which causes transconductance decrease) or a leaky or bias unstable junction. The three available choices were to form a native oxide, or deposit SiO_2 or Si_xN_y.

Native oxides obtained through anodization have been observed to be unreliable vis-a-vis interface state formation. An alternative is an oxidation step involving wet chemical treatment. A sample of InP was treated in HNO_3 at 80°C [15] followed by evaporation of Au. Diodes were formed photolithographically and leakage of $\sim.02$ A/cm^2 was observed at -8 volts bias. This process was only considered to be a test of the HNO_3 oxide properties because the 80°C HNO_3 treatment is incompatible with the photoresist used in the processing sequence.

An alternative approach was to react HNO_3 carried by gas with the sample. This process is referred to as G-HNO_3. Figure 26 shows a schematic of an apparatus which was constructed to provide G-HNO_3 treatment that is photoresist compatible. InP samples were provided with a diode array pattern defined using AZ-1350-J photoresist. The sample is placed in the reaction tube and brought to 100°C. HNO_3 is held at $\sim$80°C through which nitrogen is bubbled over the sample. This reaction is allowed to continue for 10 minutes; the gas flow is then stopped and the sample is cooled prior to removal. Gold is evaporated over the sample and diodes are formed by liftoff of the positive resist using acetone. Samples exhibited leakage $\sim.02$ A/cm^2 and a C-V measured barrier height of 0.58 volts. The devices showed little ruggedness to forward current; however, C-V measurements were well behaved with no observable hysteresis.

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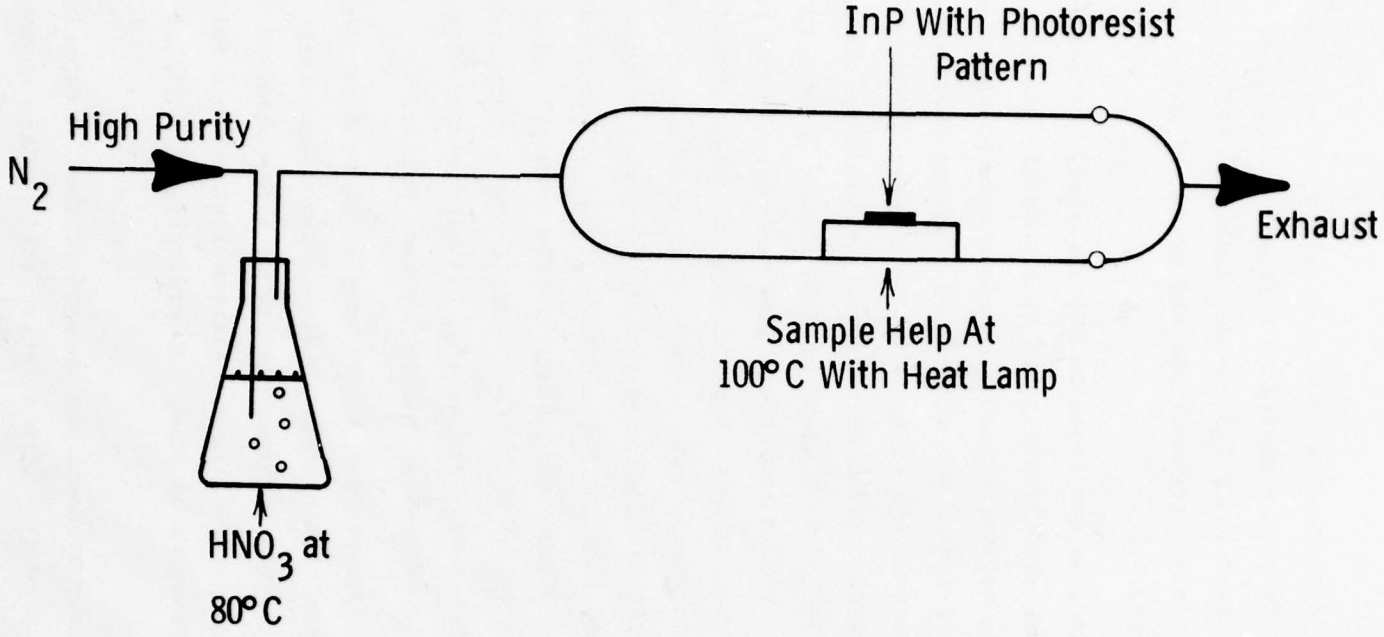


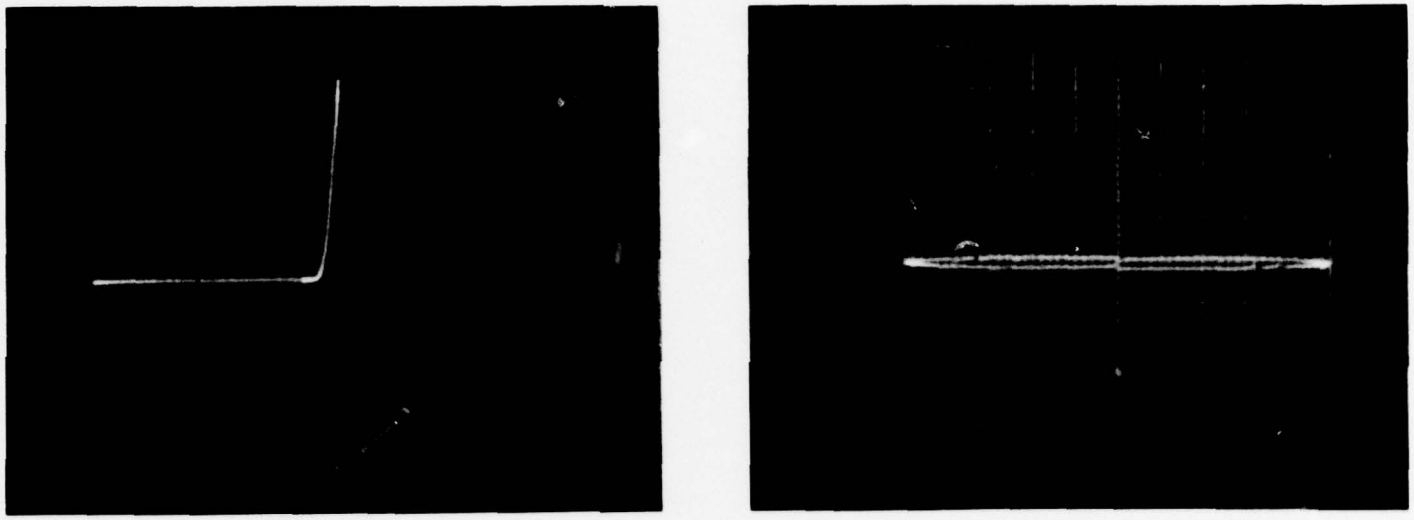
Fig. 26 – G-HNO_3 system for providing thin native oxides on InP

Ellipsometric measurements of a similarly prepared sample showed no measurable oxide when compared to a freshly etched reference sample. It is believed that while this G-HNO_3 technique did give encouraging results, it is not reproducible and produces contacts which fail readily under forward bias.

SiO_2 deposition, as described in the materials characterization section for VPE, was also investigated as a possible gate assist insulator. Samples with varying oxide thicknesses were prepared and evaporated metal contacts formed via liftoff of positive photoresist. Depending on the thickness of the oxide, the devices had MOS characteristics or showed forward current as previously discussed. Figure 27 shows I-V characteristics for both examples, and Figure 28 is a representative example of a C-V measurement of these devices. It can readily be seen that there are unacceptable traps which would cause bias instability in the FET. Measurements made using mercury dots showed a very small hysteresis; hence, it was concluded that the deposition sequence or the metal selected was inducing the additional states. Evaporated aluminum, chrome/gold, platinum, palladium and gold were all tried in an effort to utilize the Silox. Despite the differing temperatures of evaporation and reactivities of these metals, all attempts resulted in samples with unacceptable hysteresis for device fabrication.

Si_xN_y was plasma deposited on InP samples at room temperature using an LFE PND-301 deposition system. Devices formed with this material showed C-V hysteresis problems similar to those observed for the Silox MOS devices. Additionally, the minimum reproducible thickness of Si_xN_y with the LFE apparatus is 200Å. Accordingly, Si_xN_y films were not pursued any further.

The plasma system approach was pursued further by exposing an InP sample to an oxygen plasma to form a native oxide. This approach had already been reported in the literature[16] to be successful in producing good electrical properties at the oxide/InP interface. InP samples with AZ-1350-J defined patterns in place were subjected to an oxygen plasma for 5 minutes at 40°C. Care was taken to ensure that



a. 10 μA/cm - ver
2V/cm - hor.

b. 10 μA/cm - ver
10V/cm - hor.

Fig. 27 I-V Characteristics for Silox "Assisted" Aℓ Schottky Contacts - a. demonstrates thin (∼100Å) oxide, b. shows thick (>200Å) oxide with no forward current

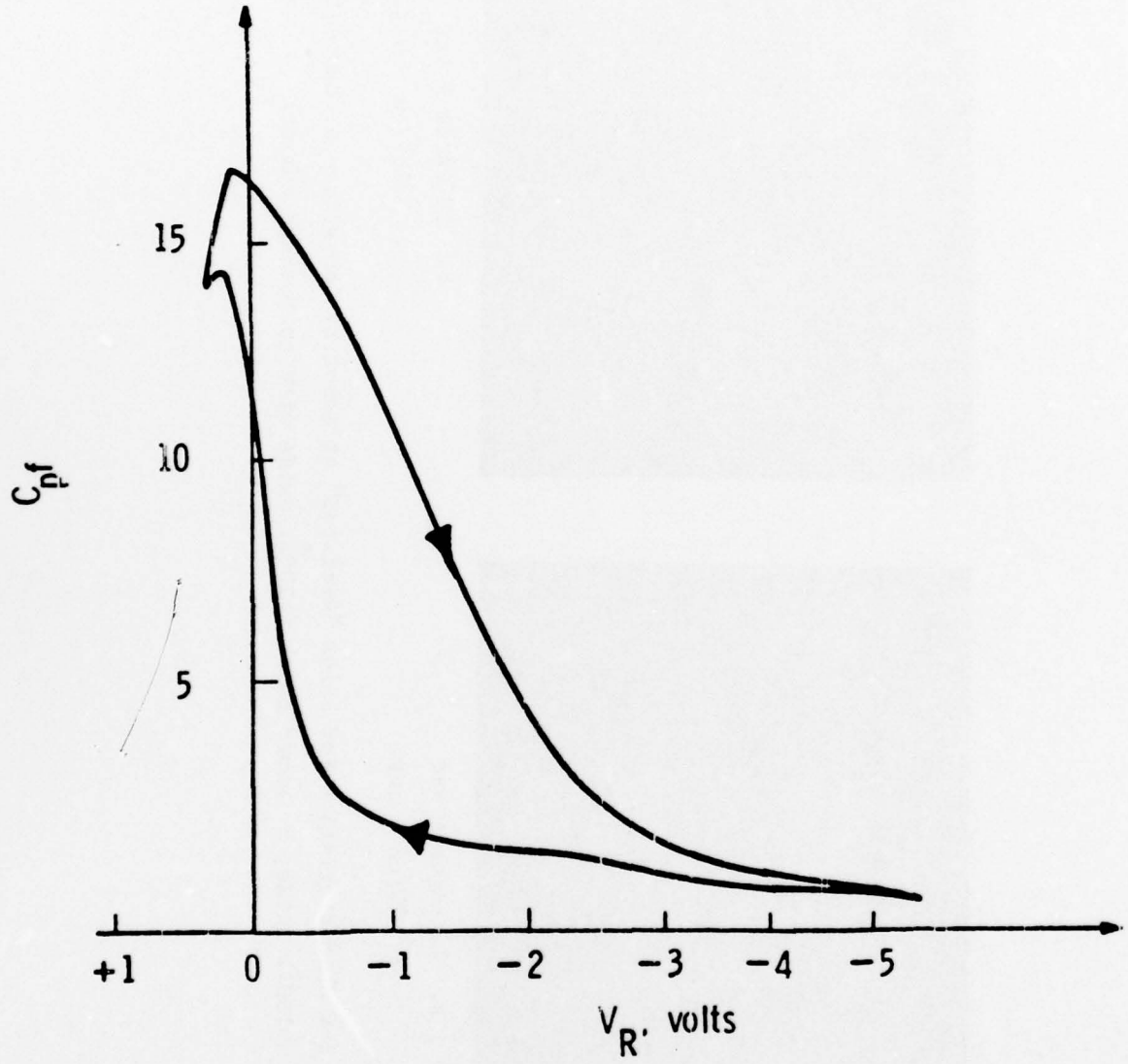


Fig. 28 C-V for High Temperature CVD SiO_2 InP w Cr/Au Indicating the Presence of Interface Traps.

enough photoresist was left after the plasma exposure to permit liftoff of the metal deposited on the device. 500Å of chromium was evaporated, followed by 3000Å of gold, and the combined metallization was then defined by rejection using acetone. Figure 29 shows a representative I-V characteristic of these devices and Figure 30 is a C-V curve for the same diode. These devices showed the best I-V and C-V characteristics of all the insulator-assisted barriers. Additionally, the FET fabrication sequence easily accommodates this oxide, hence it was selected as the technique to be applied to the FET fabrication.

Unfortunately, the plasma oxide suffers from catastrophic failure with relatively minor reverse avalanche or forward bias currents. Thus it was concluded that in the long term, alternative gate systems would have to be developed for the program.

(C) Implanted p-n Junctions

As indicated in the discussion of magnesium and beryllium ion implantation, beryllium is not a good choice for a degenerate, shallow, p^+-n junction. Magnesium, a better choice for the application, was implanted with fluences ranging from 2.5×10^{12} to 2.0×10^{13} at 50 keV into iron-doped InP substrates for activation evaluation. Additionally, a 1.0×10^{13} dose at the same energy was implanted into a sample previously implanted with silicon and whose LSS profile determined by Van der Pauw measurements is represented in Figure 31. Van der Pauw Hall samples were fabricated from the Mg-implanted samples to determine mobility and activation levels. Mobilities in the samples were low, and coupled to the difficulty of making ohmic contacts to p-type InP, it was impossible to get reliable data on the Mg activation.

The Mg implant into the Si-implanted sample was processed for diode evaluation using a liftoff of aluminum. The aluminum acts as a poor Schottky barrier to the InP as shown in Figure 32; hence the I-V behavior of the implanted p-n junction should be the dominant rectifying mechanism. Figure 33 shows the reverse-biased characteristic of the Mg/Si-implanted p-n junction. Clearly, by comparison with Figure 32,

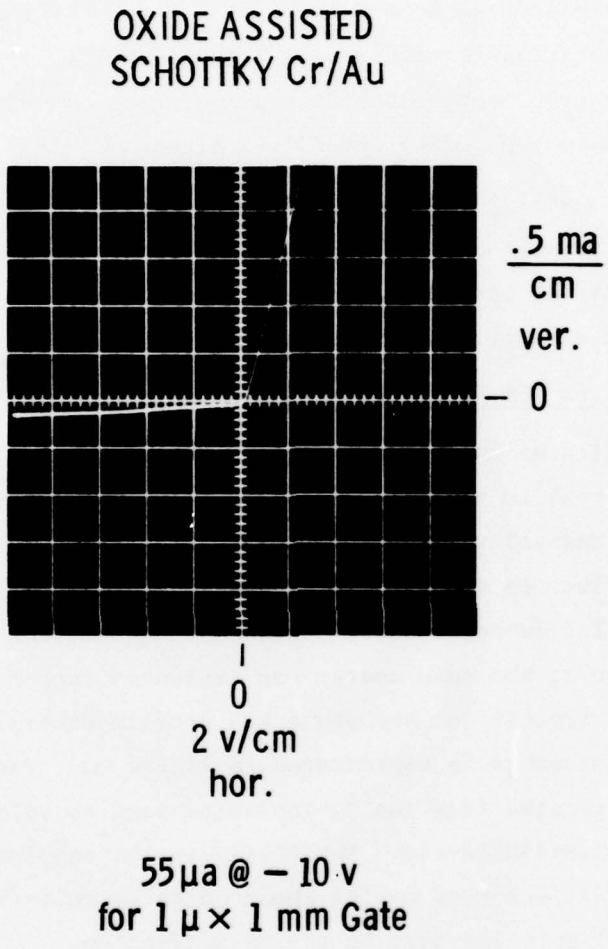


Fig. 29 I-V characteristic for plasma oxide assisted Schottky diode InP

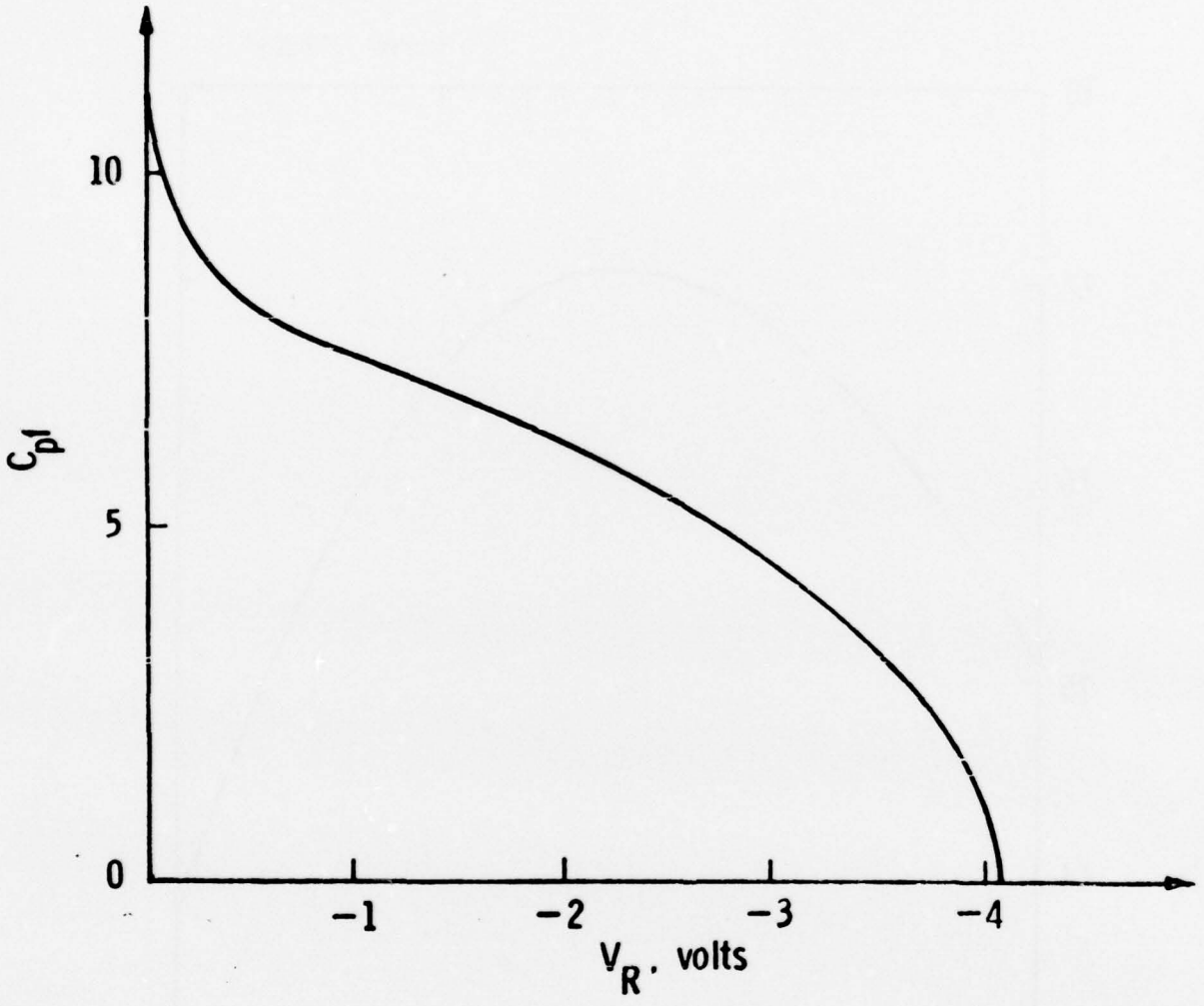


Fig. 30 C-V for Low Temperature Plasma Oxidized InP w Cr/Au Demonstrating a Lack of Oxide Induced Hysteresis

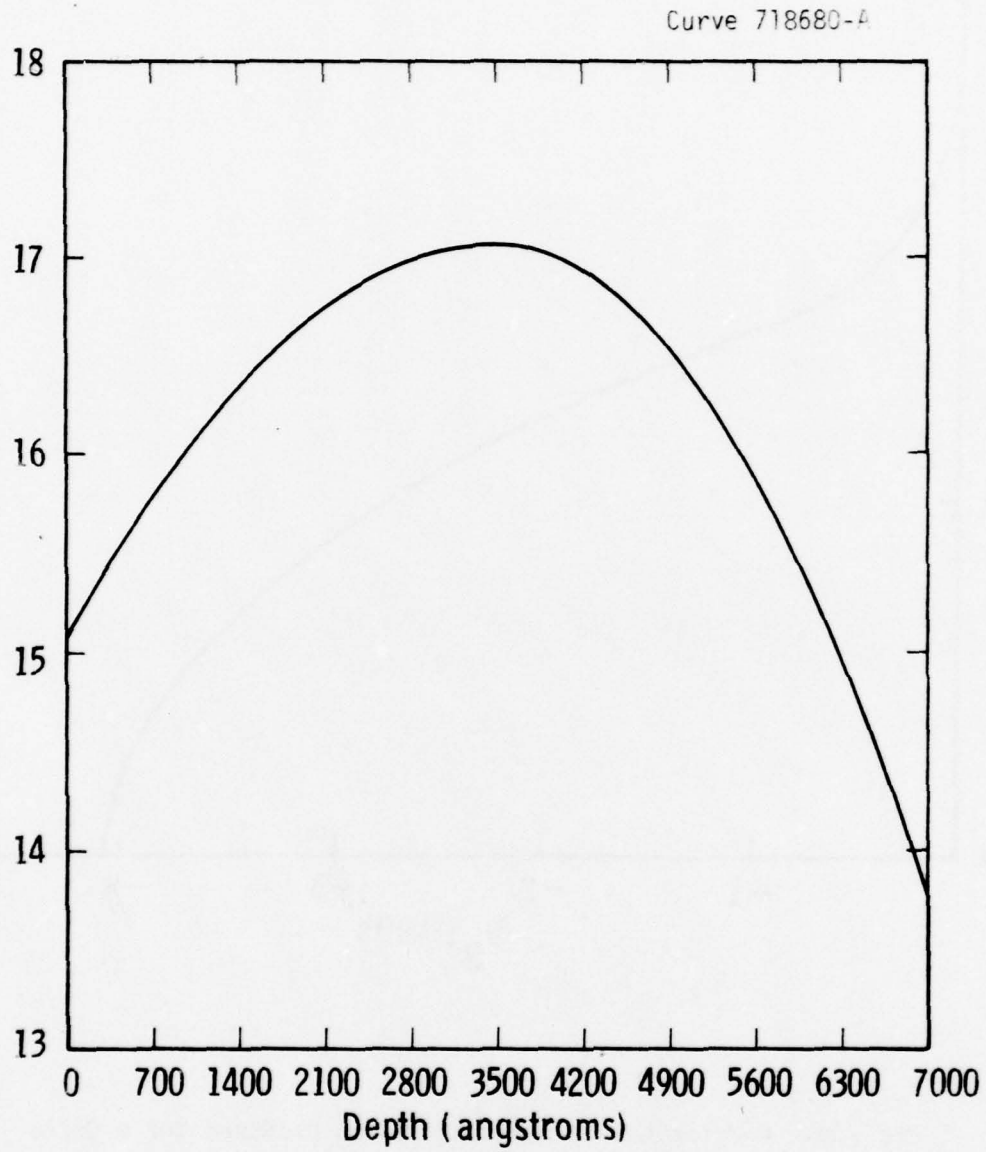
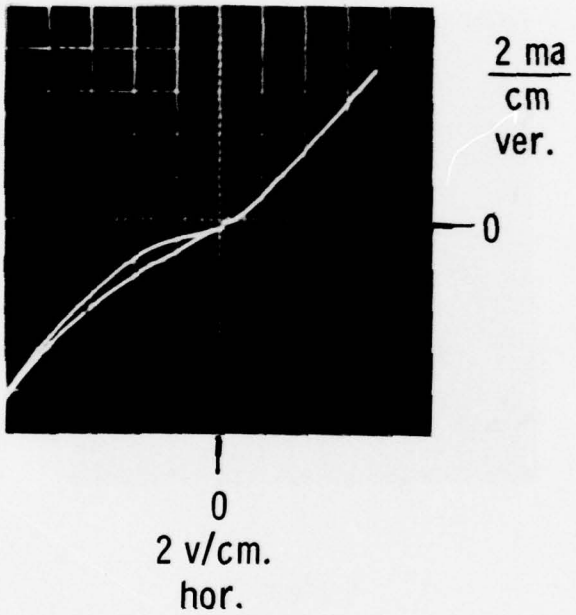


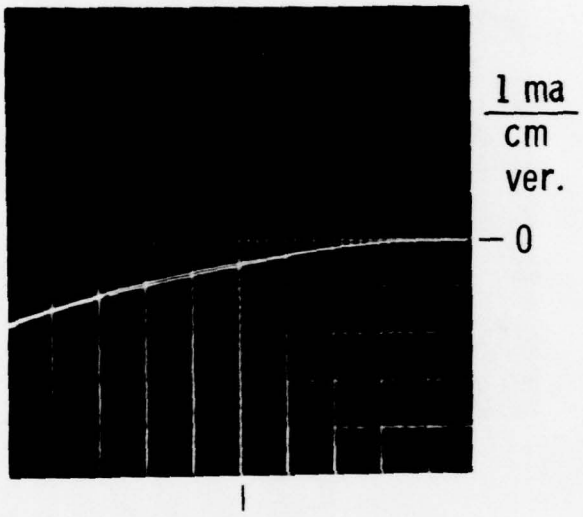
Fig. 31 — LSS profile correlated with hall data for Si implanted InP (Fe)



12.73 ma @ − 10 v
for 1μ × 1 mm Gate

Fig. 32 I vs. V for Al Schottky barrier on InP

Mg/Si IMPLANTED
PN JUNCTION



1 v/cm
hor.

.9 ma @ − 10 v
for 1 μ × 1 mm Gate

Fig. 33 I-V characteristic of MG/Si implanted Pn junction

the junction action is present; however, its leakage behavior was disappointing. To determine if there was some anomalous doping redistribution in the Mg implant causing the problem, the sample was subjected to SIMS analysis for "chemical" profiling. Figure 34 compares the SIMS determined MG profile to the LSS profile calculated for the known implant conditions. Some redistribution of the Mg took place during the anneal cycle (15 minutes at 700°C); however, it does not explain the leakage. A reasonable conclusion is that there may have been traps causing leakage current.

With the inconsistent results afforded by magnesium, the concluding phase of the program will pay special attention to p-type implantation to look more closely at shallow p^+-n junctions. It is felt that this technology has not yet reached its full potential.

In summary, the various gate experiments outlined led us to rely initially on a plasma oxide-assisted gate structure. Further experiments on p-n junction formation are planned based on experience with processed FETs.

4.2 Device Fabrication

Figure 35 outlines the fabrication scheme which has been employed for an "oxide-assisted" InP FET. The basic features are similar to the GaAs device technology used at Westinghouse. This section will review the fabrication with attention to the etch and ohmic contact technology used to date.

As discussed in the VPE materials section, a problem still exists with an anomalously high donor concentration at the interface between the active and buffer layers. However, ion implanted material was available, and so devices were fabricated using Si directly implanted into Fe-doped substrates. Ideally, fabrication on either ion implanted or VPE material should be identical. Thus far we have been able to a routinely profile ion implanted samples using Silox as was done for the VPE material (See Sec. 3.3.1). Because of experience with differential Hall characterized Si implants, we have relied to the first order on LSS calculations to determine the profiles. After an implanted and annealed

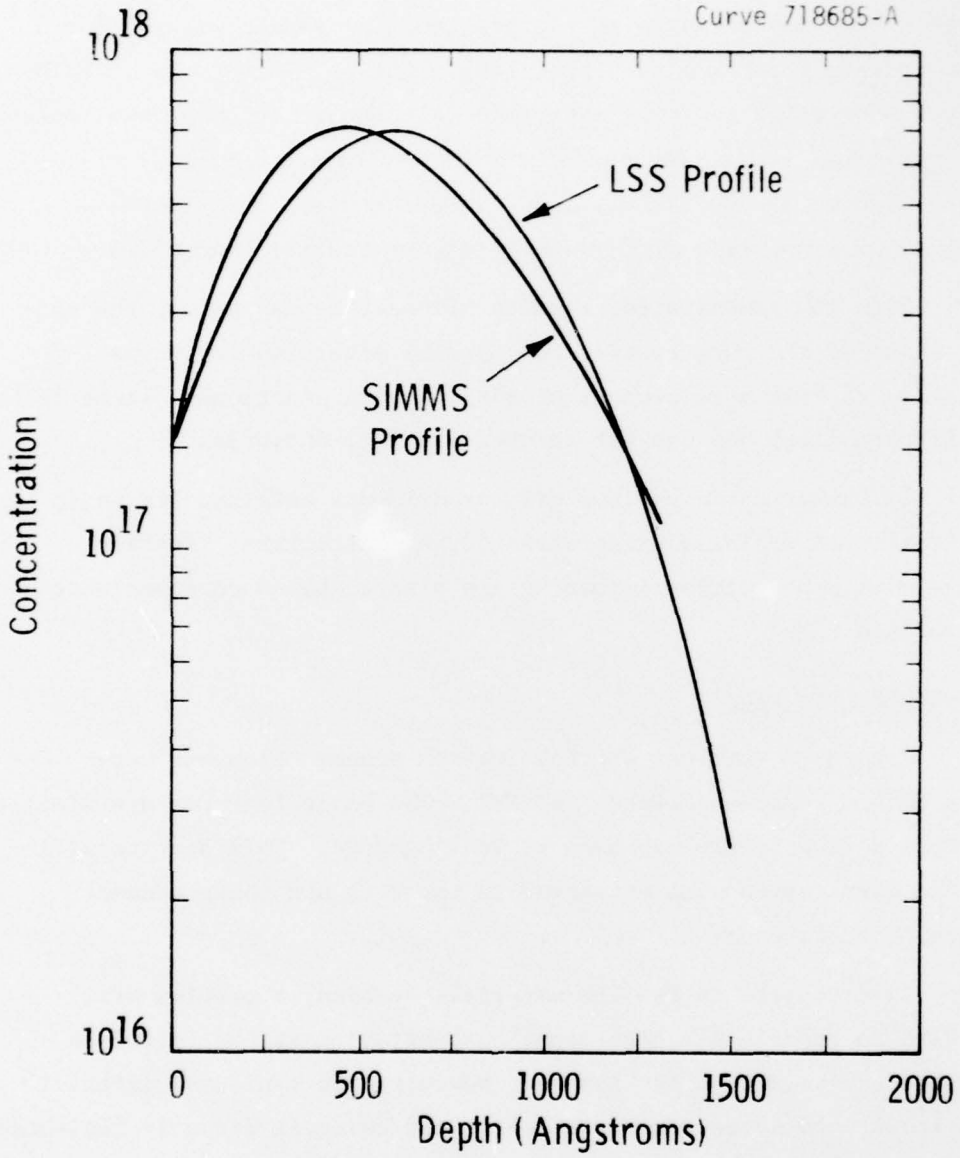
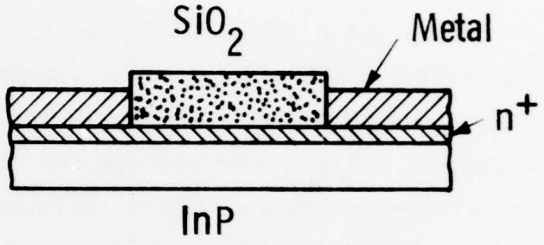


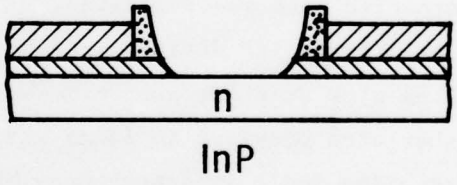
Fig. 34 — SIMMS and LSS profiles of 50 KEV MG implant in InP (Fe)

- First Mask - Isolation
  Photoresist - AZ111 - Expose
  Etch InP - 1gm HIO_3 : 19cc H_2O

- Second Mask - Ohmic Contacts
  Sputter 5000 Å SiO_2
  Photoresist - AZ111 - Expose
  Ion Mill + Chemical Etch SiO_2
  Metallize and Reject
  600 Å Au Ge
  600 Å Pd
  3500 Å Au
  Alloy 460°C for 15 sec



- Third Mask - Channel Thinning
  Photoresist - AZ1350J - Expose
  Chemical Etch SiO_2
  Etch InP - 1gm HIO_3 : 19cc H_2O



- Fourth Mask - Gate
  Photoresist - AZ1350J - Expose
  Low T Plasma Oxide
  Metallize and Reject
  600 Å Cr
  3500 Å Au

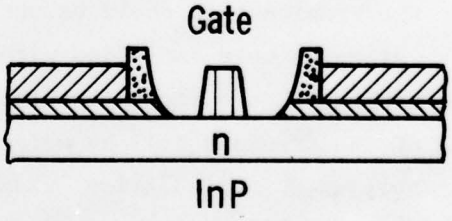


Fig. 35 — Realigned InP FET fabrication sequence

wafer is received from ion implantation, a Van der Pauw Hall sample is fabricated and the sheet concentration and mobility are determined for the wafer. This sheet concentration, along with the LSS parameters for the implant energy used, are used as input to a computer program which determines the "first order" profile of the material. Figure 36 is a flow sequence for the program. The computer first calculates n(x) using the LSS skewed Gaussian. It then integrates n(x) to give sheet concentration and a pinchoff voltage for this material. A function is provided which simulates the removal of Δx amount of material from the surface. Using the previously determined profile, the new sheet concentration and pinchoff voltage for the "etched" wafer are determined. By correlating our theoretical calculation with actual etching of the wafer and Hall sample, the fabrication sequence on ion implanted material is started with a trim etch. At this point the sample is ready for the masking sequences outlined in Figure 35.

Previous work on InP has relied on bromine-based etches.[17,18] Our experience with bromine is that it is among the worst of chemicals for photoresist processing. The possible use of iodic acid as an alternative etch was suggested,[19] hence an investigation was made of its utility to InP device processing. Figure 37 shows a Talystep of both an etch step for a bromine-based etch and an iodic acid etch. Neither etch provides an ideal step for bringing thin gate stripes over mesas. The iodic acid etch does provide a uniform etch without the severe edge effects observed with the bromine-based etch. It is possible that the bromine etch could be optimized to prevent this behavior; however, since we were satisfied with the iodic acid performance, it has become the standard etch solution. Figure 38 shows the etch rate properties of the standard 1:19 by weight aqueous HIO_3 solution. It is routinely used for isolation, channel thinning, and gate recess. It should be noted that the etch appears to attack heavily doped InP more slowly than lightly doped material. Further work is necessary to carefully calibrate the etch rate as a function of doping.

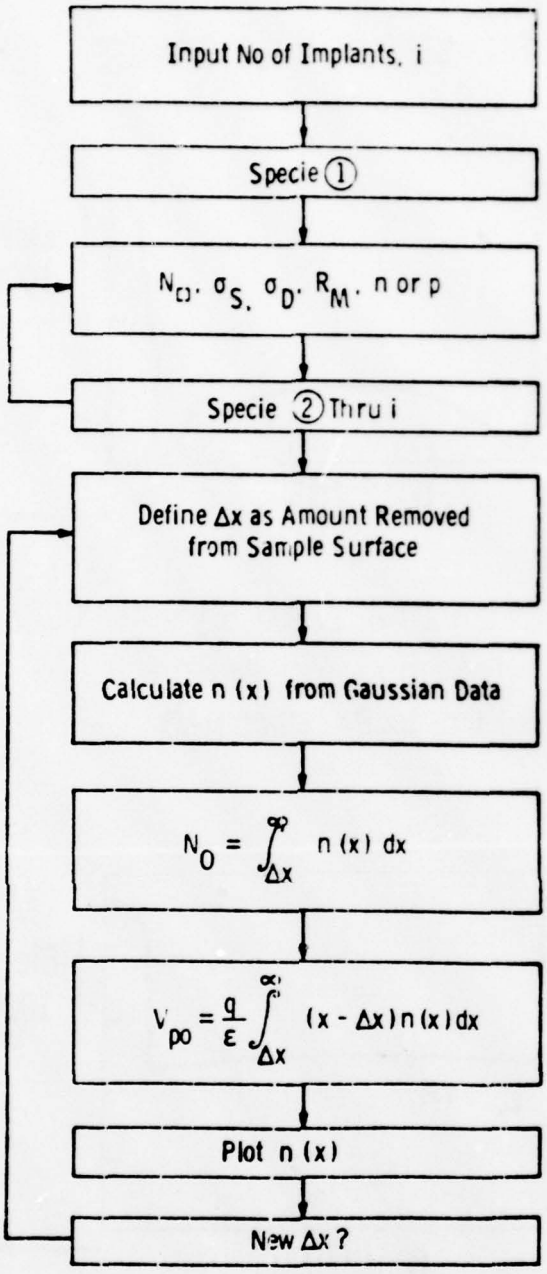
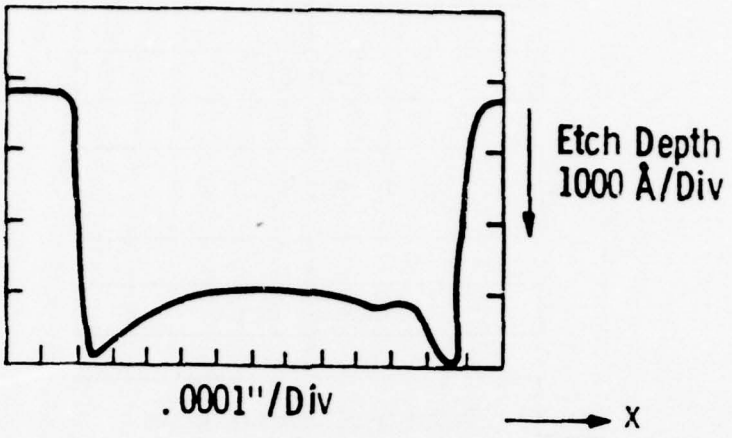


Fig. 36 LSS calculation for multiple implantations
(a) doping profile
(b) pinchoff voltage as a function of surface etching

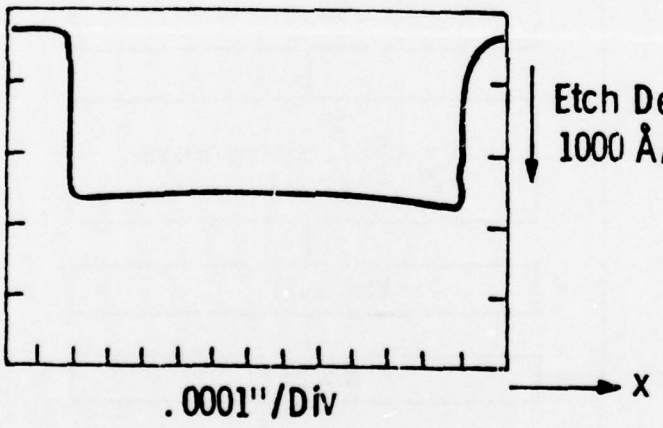
TALYSTEP OF InP ETCHANTS

I.



8 Min Etch In 8:1:200, By Vol., Of
HBr:Br-A: H_2O, Where Br-A Is
10gms KBr: 1ccBr: 20 cc H_2O

II.



13 Min Etch In Dilute Iodic Acid,
2gms HIO_3: 38 cc H_2O

Fig. 37 Talystep of InP etchants

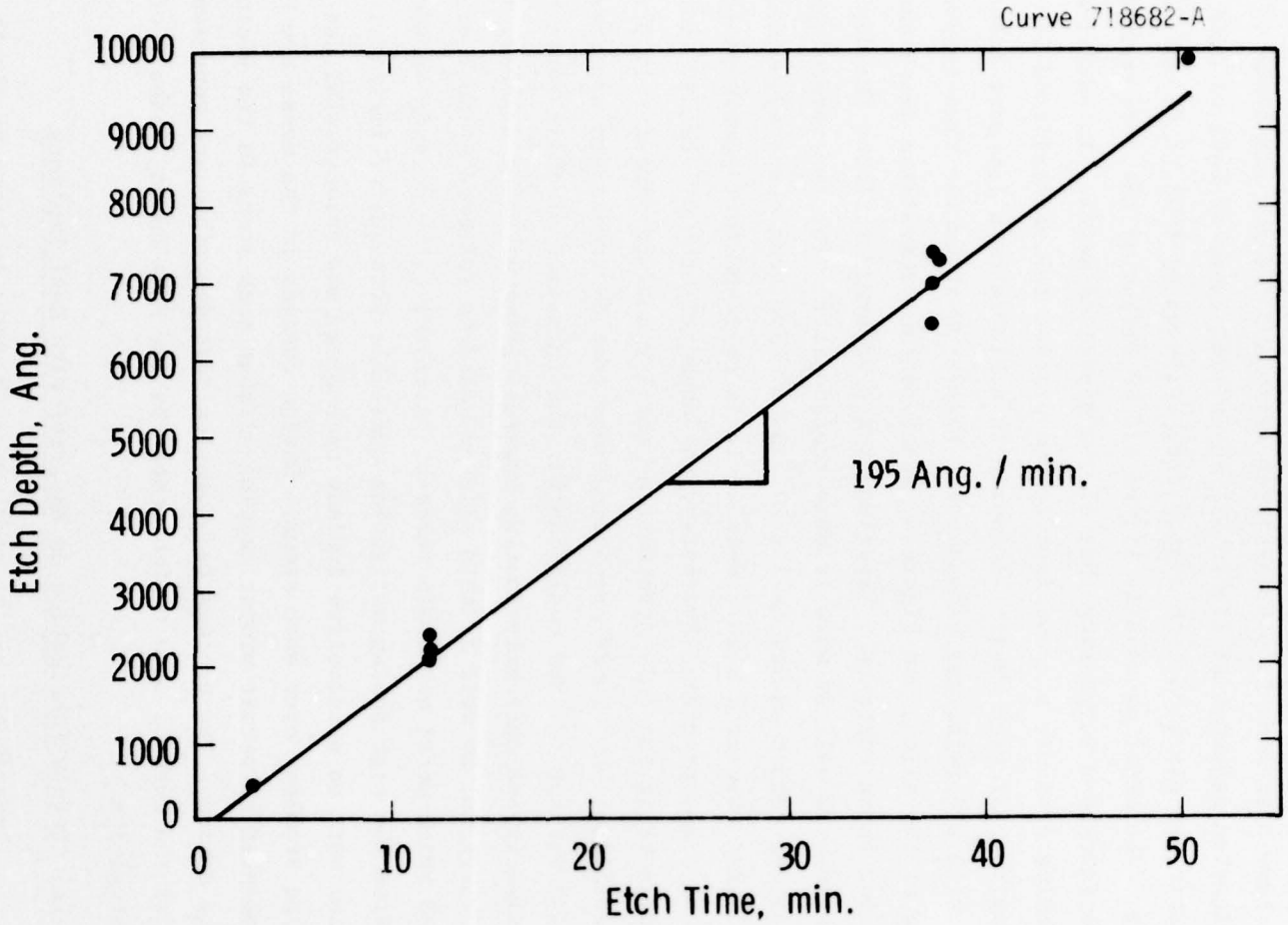


Fig. 38 — Etch depth vs. time for 1:19 HIO_3 : H_2O, by weight, on N type InP

Ohmic contacts and interconnects for device processing to date have been made in one mask step using AuGe/Pd/Au. As shown in the fabrication sequence of Figure 35, an initial layer of 600Å of AuGe eutectic was electron beam evaporated, followed by 600Å of Pd and 3500Å of Au. The metal was easily lifted off by virtue of the surrounding oxide thickness surpassing that of the deposited metal. In addition, the oxide provides a convenient cap to protect the unmetallized InP during the alloying cycle. Alloying is achieved on a low mass carbon boat with a forming gas atmosphere. Figure 39 shows the time-temperature cycle of the alloy, and Figure 40 shows contact resistance measurement data for these contacts. Experiments are underway to lower the contact resistance as well as make it more reproducible. For the technology described, values as low as 7×10^{-6} Ω-cm^2 have been observed, as well as a worst case of 2×10^{-4} Ω-cm^2. It is believed that sample preparation is a key problem. Presently, the chemical etch of the SiO_2 with buffered HF is the only treatment of the InP surface immediately prior to metallization. There are indications that HF treatments may damage the InP surface[20] and could inhibit the formation of ohmic contacts. Experiments are currently looking towards different metal schemes, i.e., AuGe/Ti/Pt/Au, as well as thin alloyed contacts followed by another mask to add thick metal and drain busses. Ultimately, the devices should benefit from the high doping activation available with sulfur implants. Initial work on a selective implant technology was unsuccessful due to capping problems over etch steps. Design changes in the masks are being implemented to permit proper capping without etch steps in the vicinity of the device. The process technologies just described are representative of the methods used to fabricate the InP FETs during Phase I of the investigation.

(A) Device Fabrication on Material with Dual Implants

Because of initial problems with ohmic contacts to single implanted structures, dual implants were employed. Samples I-6 and I-7 were implanted with Si at 50 keV, 1×10^{13} and 400 keV, 6.5×10^{12}. In addition, monitor samples were run with single implants at each of the

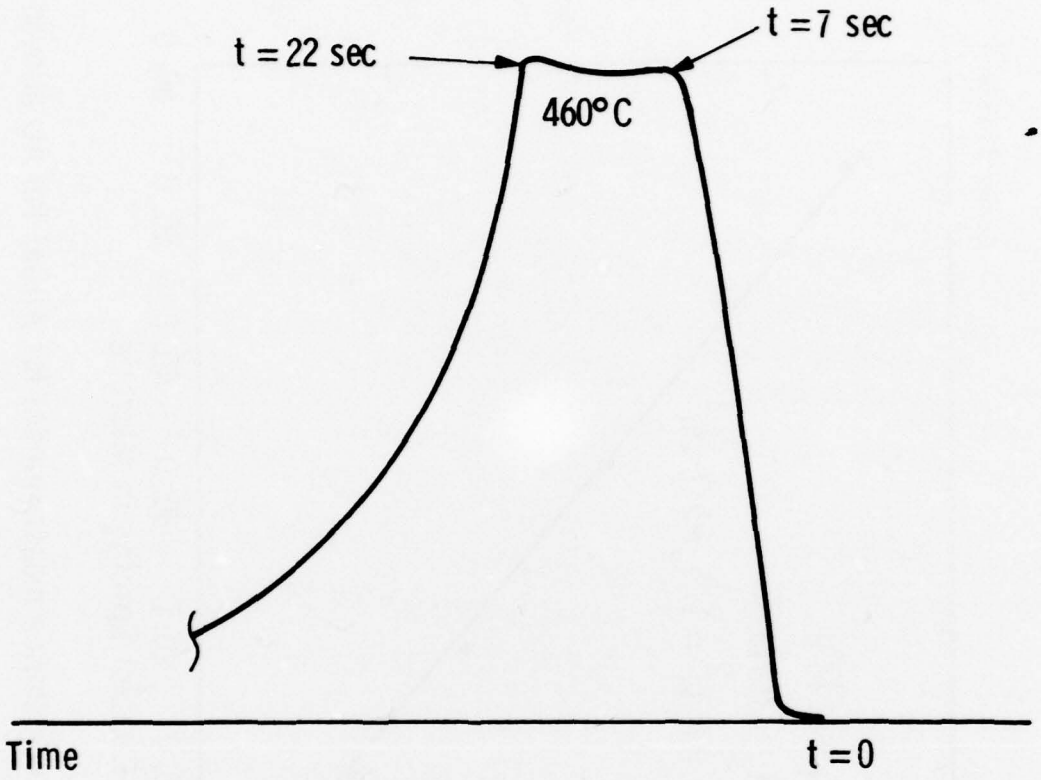


Fig. 39 — Measured time-temperature alloy cycle for InP devices w. AuGe/ Pd/ Au

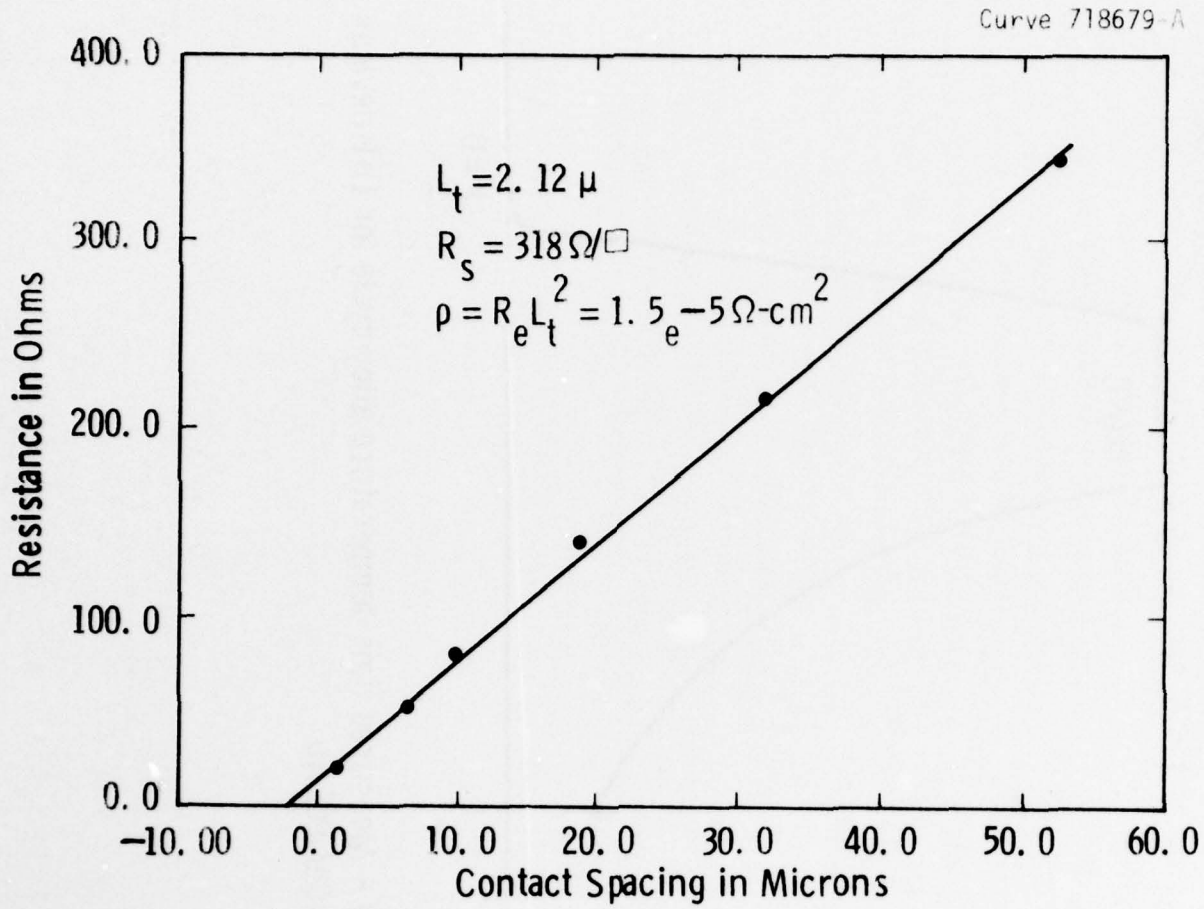


Fig. 40 — Contact resistance measurement for AuGe/ Pd/ Au alloyed on N-type InP

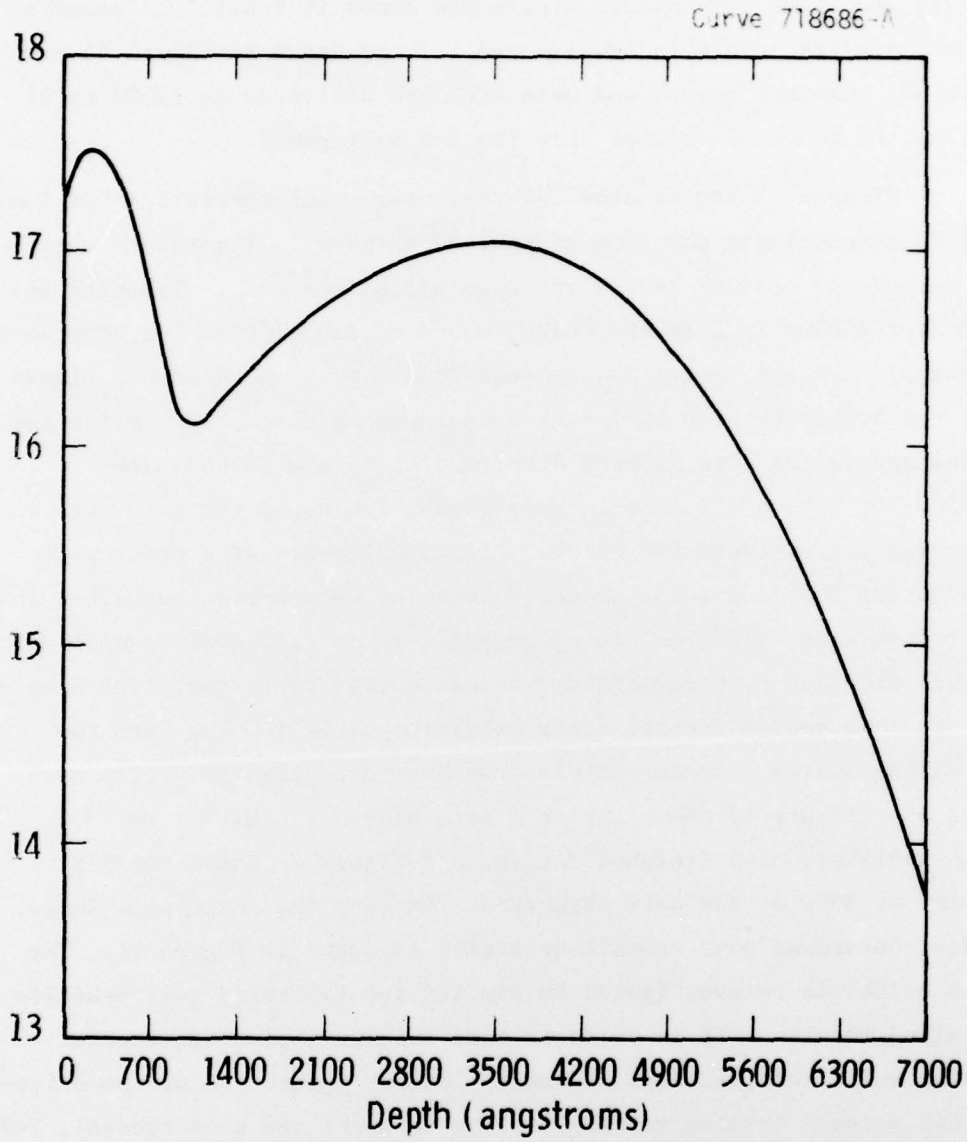


Fig. 41 — LSS profile correlated with Hall data for I-6, dual Si implant in InP (Fe)

above conditions. Phosphorus doped SiO_2 was deposited at 380°C, and the samples were annealed for 15 minutes at 690°C in forming gas. Mobility and sheet concentration data are shown in Table IV. Based on computer scaling, profiles for I-6 and I-7 are shown in Figure 41 and Figure 42. Channel recess and gate etch are projected at 1700Å total to bring the pinchoff voltage into the 5-6 volt range.

Figures 43 and 44 show I-V test probe characteristics for I-6 and I-7, respectively for 300μ of source periphery. The wafers were next masked and channel recess was done using 1:19 HIO_3. Thinning was aimed at reducing I_{DSS} to the neighborhood of 120 - 140 mA for 300μ source periphery. I-6 was overetched as seen from Figure 45; however, Figure 46 shows the appropriate channel recess achieved on slice I-7. Slice I-6 was damaged in the gate masking step, while I-7 was masked with AZ-1350J for gate application. Very light etching of the gate area was done using the standard HIO_3 etch. Plasma oxide-assisted gates were intended for these devices; hence, no probing was carried out after the gate recess etch. I-7 was placed immediately in the plasma system after the gate etch and room temperature oxidation was performed. The sample was held in a vacuum carrier after oxidation until loading into the evaporation system. Cr-Au was electron beam deposited as outlined in Figure 35. Figure 47 shows the zero gate bias I-V behavior for 300μ source periphery of a finished device, and Figure 48 shows the I-V behavior of 300μ of the gate structure. Because the gates were leaky, the devices showed poor transistor action as shown in Figure 49. The plasma oxide was reinvestigated on similar ion implanted test vehicles with mixed results. It is believed that the ion implanted material contains sufficient residual damage to inhibit the action of the oxide-assisted gates. Despite surface etching (channel and gate recess), I-7 had poor gating as did the new test samples.

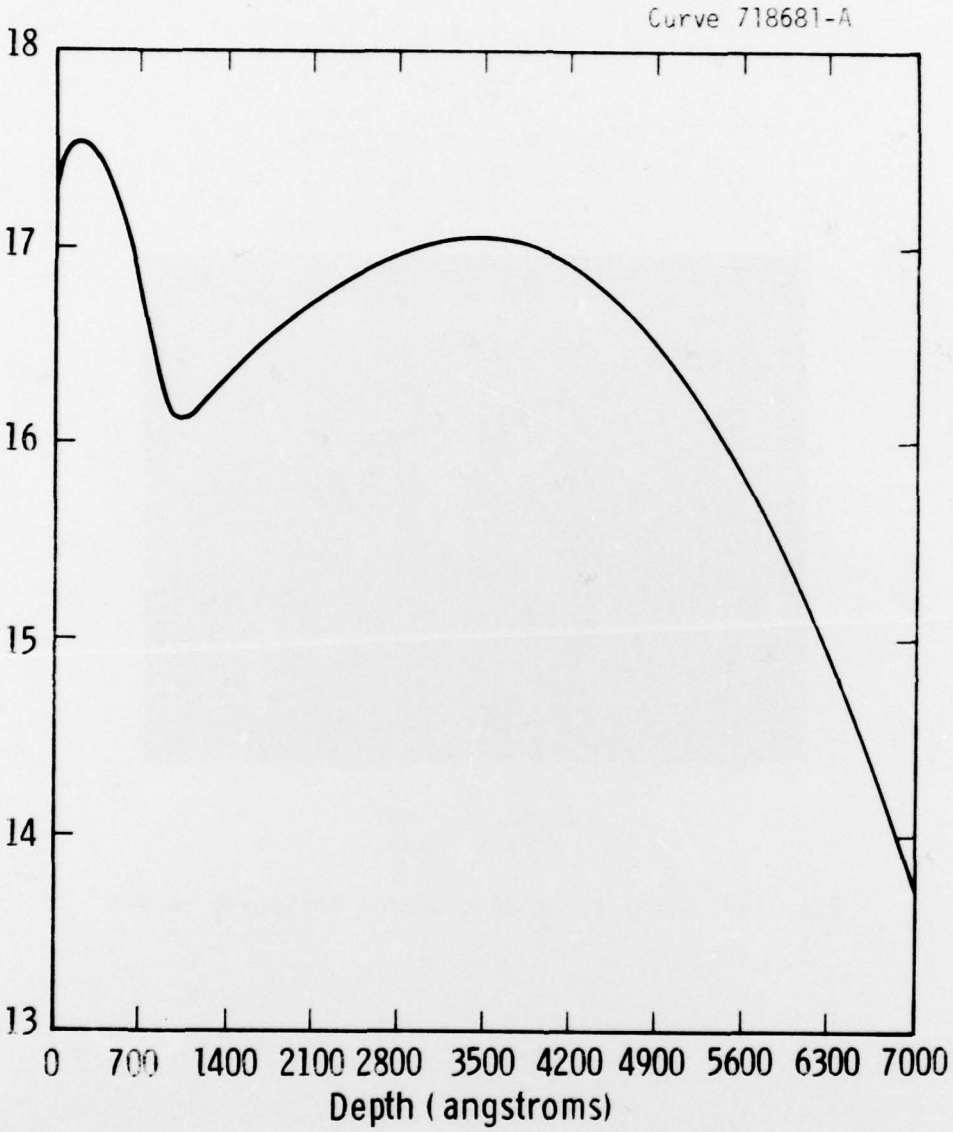
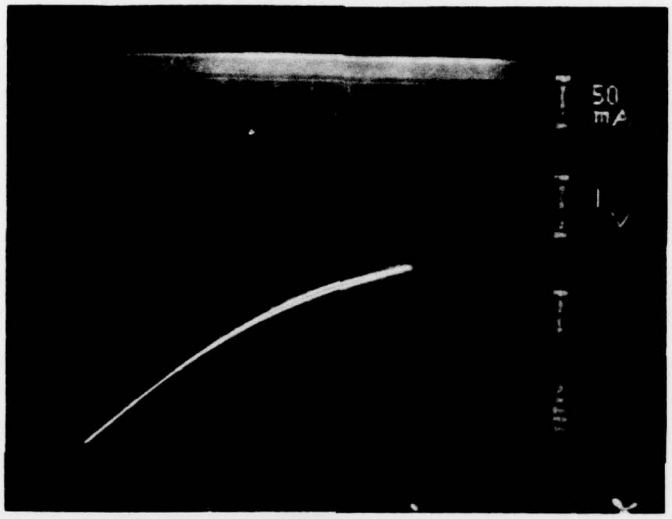
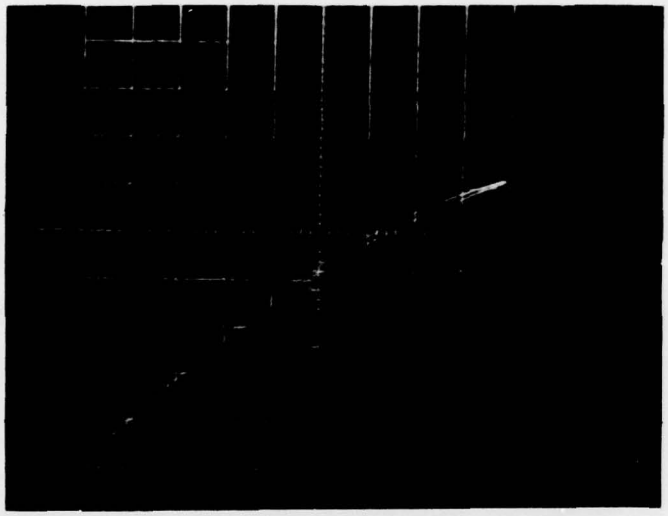


Fig. 42 — LSS profile correlated with Hall data for I-7, dual Si implant in InP (Fe)



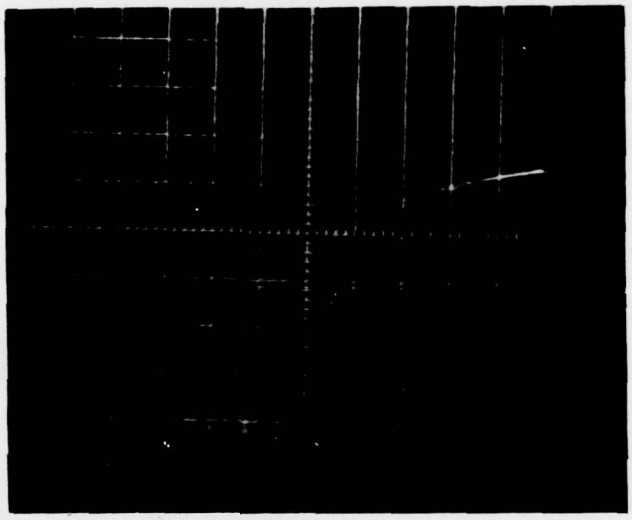
50 ma/cm - ver
1 v/cm - hor.

Fig. 43 I vs. V for 300μ source periphery on I-6



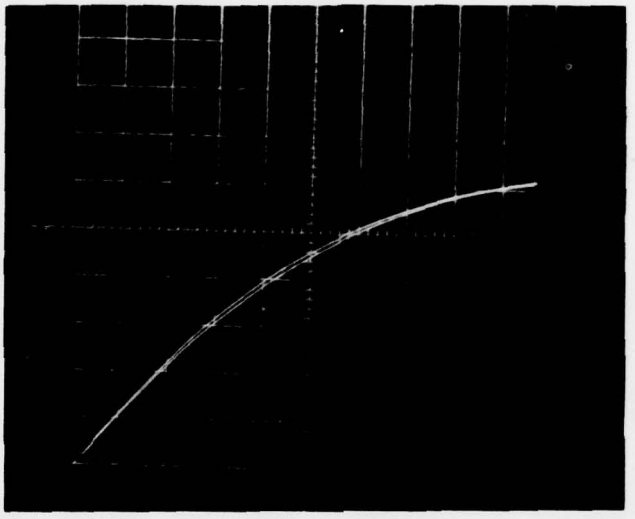
50 ma/cm - ver
1 v/cm - hor.

Fig. 44 I vs. V for 300μ source periphery on I-7



10 ma/cm - ver
1 v/cm - hor.

Fig. 45 I vs. V for 300μ thinned channel on I-6



20 ma/cm - ver
1 v/cm - hor.

Fig. 46 I vs. V for 300μ thinned channel on I-7

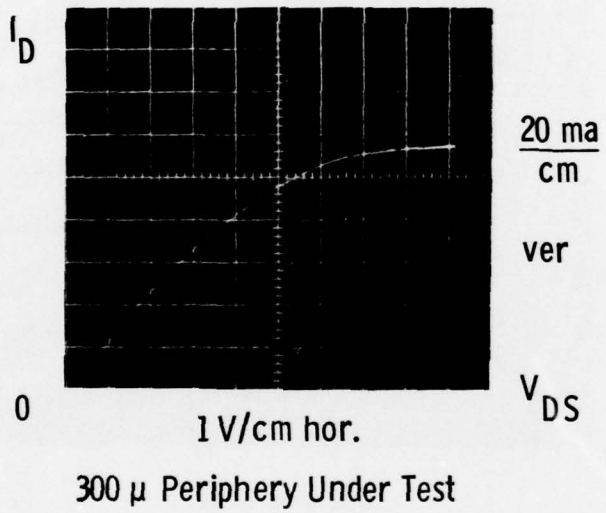
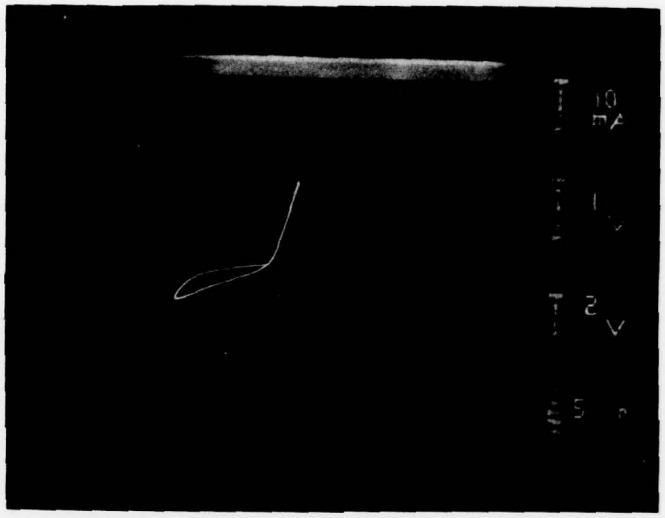
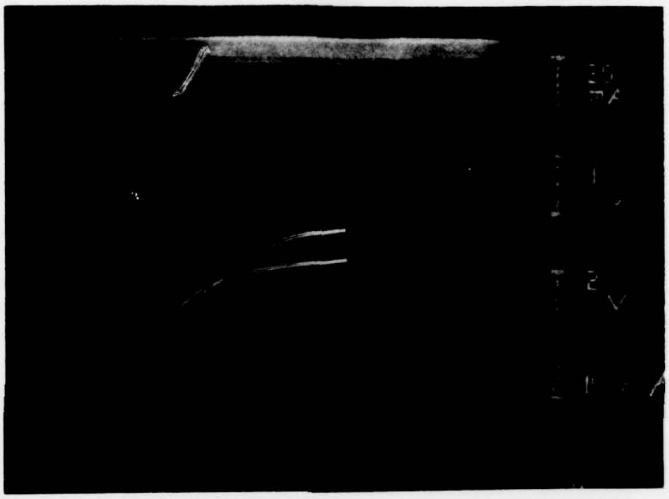


Fig. 47 Zero bias I vs. V for finished device on I-7



10 ma/cm ver
1 v/cm - hor.

Fig. 48 I vs. V for 300μ gate-source junction on I-7



20 ma/cm - ver
1 v/cm - hor.
2v/cm - step

Fig. 49 I vs. V for 300μ FET with gate-bias on I-7

5. CONCLUSIONS

While the plasma oxide technique appears to be compatible with VPE material, the overall conclusion from experiments performed to date is that dielectric-assisted gates are nonreproducible and will not ultimately satisfy performance criteria consistent with the goals of a power FET. Phase I of this program established a viable materials and device processing capability for InP with the exception of the gate. As discussed in the gate technology section of this report, work is now directed squarely at p-n junction formation. The remainder of the program effort is aimed at an ion implanted junction and a re-examination of diffused gates. The success of either of these two approaches can be integrated with the technology developed in Phase I to provide the test device necessary for examining the larger question of the role of InP FETs for high frequency microwave power generation.

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