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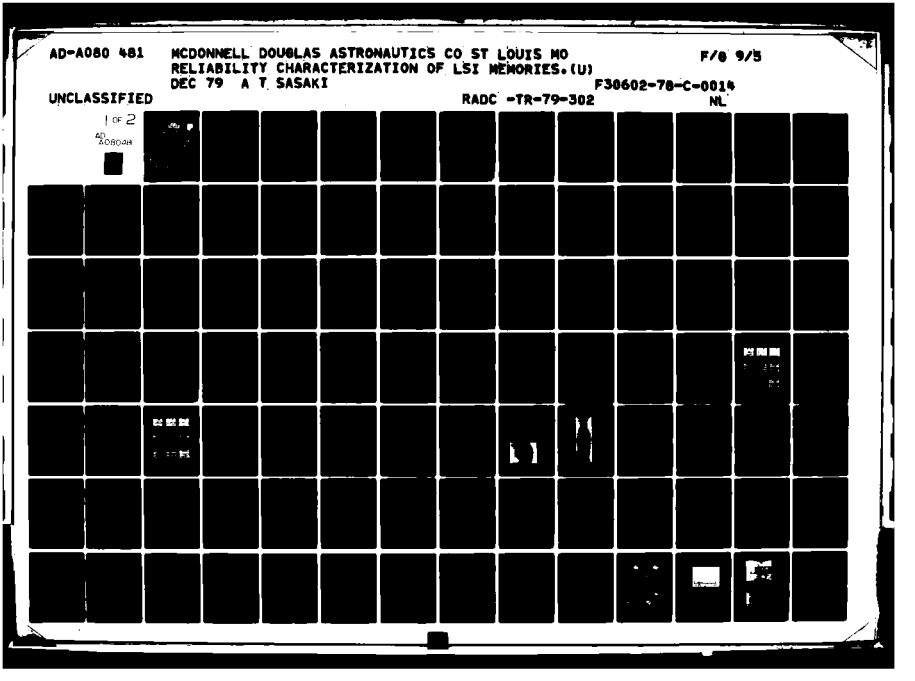

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The primary objective of this effort was to evaluate and characterize the reliability and failure modes of 4K Large Scale Integration (LSI) memories procured to the specification requirements of MIL-M-38510/237. Secondary objectives were to evaluate the screening effectiveness of the detail specifications and to compare the relative effectiveness of high temperature accelerated life tests performed with both static and dynamic excitation. The program objectives were achieved by subjecting the test devices to a matrix of temperature cycling tests, high temperature non-operating life tests, and high tempera-

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ture operating life tests with static and dynamic excitation.

The part types under evaluation include a 1K x 4 bit NMOS static RAM (AM9130) and a 4K x 1 bit NMOS static RAM (AM9140).

The test results indicated that the AM9130 and AM9140 devices have a high reliability potential. However, there was an insufficient number of life test failures to estimate the device failure rates based on the Arrhenius Reaction Rate Model. A total of eighteen devices of 240 total tested were failed at the completion of testing and all but two failures were attributed to a surface related mechanism(s). Seven of the eighteen device failures were due to marginal I_{CC} values at the start of life testing and a single failure was attributed to a degraded input caused by static discharge or an electrical transient. All failures occurred in the static and dynamic life test cells with a total of 120 parts. It is believed that high reliability military systems can be designed with devices procured to the MIL-M-38510/237 specification.

Based on the limited cell size and small number of failures, the test results are not conclusive as to the relative effectiveness of static versus dynamic excitation during accelerated life testing. It is recommended that more extensive evaluations be performed to determine whether static excitation or dynamic excitation is more effective for LSI memories. These evaluations should include larger test cell sizes and multiple wafer lots.

PREFACE

The work described in this report was performed by the Parts Evaluation Laboratory section of the McDonnell Douglas Astronautics Company - St. Louis Engineering Reliability Department during the period between December 1977 and May 1979. Electrical testing was performed by the Advanced Test and Design Group of the McDonnell Douglas Electronics Company. The work was performed for the USAF Rome Air Development Center under contract number F30602-78-C-0014. Mr. Carmine Salvo of the RADC Reliability Physics Section provided technical direction. In addition to the many McDonnell Douglas personnel who contributed to the program, special thanks are extended to Messrs. Van Weissflug, Michael Roberts, Thomas Faltus, Edward Sisul, Will Eastes and finally to Ron Mackin and Gordon Johnson for providing engineering management of the test program.

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EVALUATION

This study in support of TPO5, C^3 System Availability, is one of the first in a series of reliability assurance efforts designed to evaluate the reliability, failure modes and mechanisms, of the latest LSI NMOS technologies which are being used in Air Force electronics.

Memory devices have been selected as test vehicles because, typically, introduction of new semiconductor design fabrication techniques occurs first in memory devices. Thus, memory reliability studies allow the earliest assessment of design, process and materials associated with the reliability of the emerging technology.

The devices selected for this study were commercial AM9130 and AM9140, 4K n-channel silicon gate MOS RAMs purchased to MIL-M-38510/237 Class B requirements. This effort employed high stress test cells including 4000 hour operating life tests at Vcc = 6.5 volts and temperatures of 175°C and 200°C. Despite extreme conditions, only 18 devices of 120 stressed in these operating life test cells failed, and of those, one was not considered life test induced, and seven were marginal Icc failures on parts which were close to the specification limit on that parameter prior to life test. There were no temperature cycling or high temperature non-operating life test cell failures.

This study establishes a baseline for LSI NMOS silicon gate reliability of these relatively mature, early generation 4K devices. The results will be used in improving MIL-M-38510 specifications and MIL-STD-883 test methods and procedures. The data is already being applied to innovative studies of more advanced technology memories using microprocessors to detect and record transient or soft

errors which occur during the life test between the electrical test measurement times. With so few hard failures occurring in a 4,000 hour accelerated life test, such an approach is expected to yield a great deal of additional useful reliability information.

The AM29140 is already in use in F-16 and F-18 systems and the AN/TPX-42A IFF equipment. This study should provide assurance that parts procured to the requirements of MIL-M-38510/237, Class B will perform reliably in these and other systems.

CARMINE J. SALVO
Project Engineer

1.0 INTRODUCTION

Air Force systems are currently being designed with 4096-bit static NMOS Random Access Memories (RAMs). New, more complex, higher density devices are expected in the near future with this technology. A reliability characterization program is an essential step in assessing the reliability of the 4K-bit NMOS RAM technology. Particular attention was given to determining the suitability of high temperature operating life tests with static excitation and to compare the relative effectiveness of static versus dynamic excitation accelerated life tests.

The primary objective of this program was to evaluate and characterize the reliability and failure modes of 4096-bit LSI Memories procured to the specification requirements of MIL-M-38510/237. The secondary objective was to evaluate the screening effectiveness of the detail specifications and to make recommendations for improving the screening effectiveness as a result of life testing.

This report provides a general description of the overall program and presents the results of all tests and evaluations conducted throughout the program. The results of failure analysis and data analysis are also included in this report.

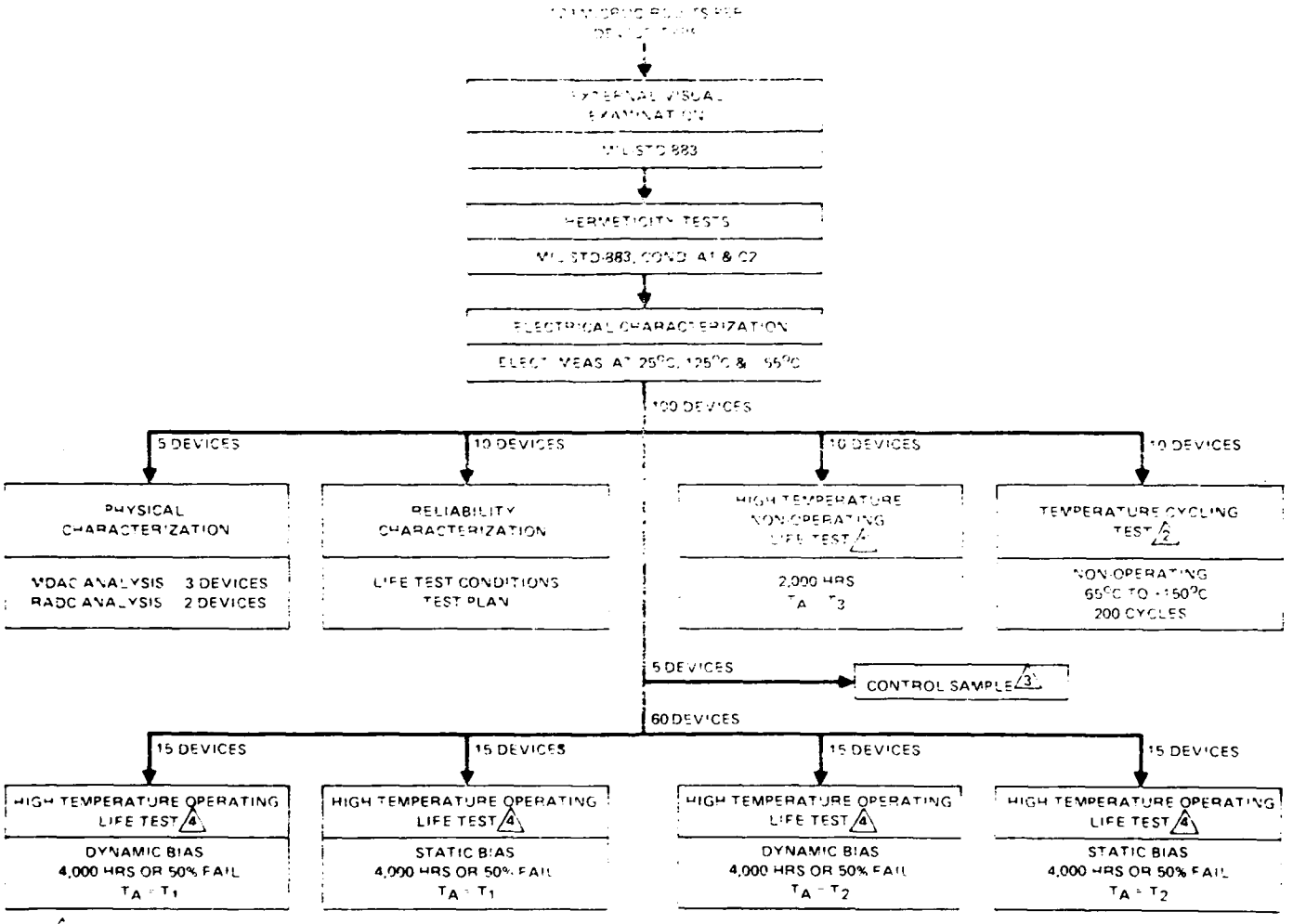
2.0 PROGRAM DESCRIPTION

2.1 TEST PROGRAM

The program for characterizing the failure modes of 4096-bit LSI memories is illustrated in Figure 2-1. The work flow of the test program was subdivided into three phases which included: (a) initial inspections and hermeticity testing, (b) electrical, physical and reliability characterizations, and (c) a matrix of temperature cycling and high temperature operating and nonoperating life tests. Upon receipt of devices at MDAC-St. Louis, the test devices were subjected to visual inspection and hermeticity tests. All devices that passed the Phase I inspections and tests were electrically tested to the appropriate MIL-M-38510 slash sheet. The electrical characterizations were performed on a 100% basis to the Group A dc and functional tests of the appropriate MIL-M-38510 slash sheet. Following the initial examinations and electrical tests, acceptable devices were allocated by serial number to individual test groups. The device allocation for each part type is shown in Figure 2-1.

Physical characterizations were performed by both MDAC-St. Louis and RADC on a sample of five devices of each memory type. Destructive physical analyses were used to determine construction methods, manufacturing process techniques, detail device schematics, and internal gas ambient. These results were used to predict potential reliability problems, to identify any physical limitations which may influence the selection of life test temperatures and to provide a baseline for failure analyses activities.

Reliability characterizations were performed on a sample of ten devices of each memory type as prerequisites to determining the accelerated life test conditions. These studies included the evaluation of both static and dynamic excitation bias circuits and thermal resistance measurements for computing the device junction temperatures at the anticipated life test temperatures. Prior to selecting the static excitation bias circuits, considerations were given to the devices' operational modes, address input selection and output load. For the dynamic excitation bias circuits, the considerations included the devices' operational modes, data patterns, operating frequency, and output load.



1. 25°C ELECTRICAL MEASUREMENTS AT 168, 504, 1000, 1500 & 2000 HOURS. 125°C & -55°C ELECTRICAL MEASUREMENTS AT 2000 HOURS.
2. 25°C ELECTRICAL MEASUREMENTS AT 10, 50, 100, 150 & 200 CYCLES. 125°C & -55°C ELECTRICAL MEASUREMENTS AT 200 CYCLES.
3. TESTED PRIOR TO HIGH TEMPERATURE LIFE & TEMPERATURE CYCLING TESTS ELECTRICAL MEASUREMENTS.
4. 25°C ELECTRICAL MEASUREMENTS AT 168, 504, 1000, 1500, 1900 & 2000 HOURS. 125°C & -55°C ELECTRICAL MEASUREMENTS ADDED AT 504, 1000 & 2000 HOURS.

FIGURE 2-1. PROGRAM WORK FLOW

The results of the Phase II characterizations were used to select the operating life test conditions for Phase III evaluations. In addition to the operating life tests, high temperature storage tests and temperature cycling tests were included in the evaluations. The high temperature storage tests were performed with ten devices of each part type for 2000 hours at an ambient temperature of 275°C. The temperature cycling tests consisted of ten devices of each part type subjected to -65°C to 150°C temperature extremes for 200 cycles. The accelerated life tests were performed with 60 devices of each part type and consisted of: (a) two cells of 15 devices each with static excitation and (b) two cells of 15 devices each with dynamic excitation. The duration of the life tests was 4000 hours with ambient temperatures of the test cells at 200°C and 175°C. Interim electrical performance measurements were performed on test devices after cool down to room ambient temperature with bias applied. The schedule of electrical measurements for the memory stress tests is shown in Tables 2-1 through 2-3. The subgroups 1, 2, and 3 are the dc tests at 25°C, 125°C, and -55°C and subgroups 9, 10, and 11 are the functional tests at 25°C, 125°C, and -55°C of the detail specification and are defined in Appendix B. All devices that failed an interim test at 25°C were removed from the life test and subjected to failure analysis. In addition, shmoo plots were initially generated for access time as a function of supply voltage for 25°C, 125°C and -55°C with two devices of each part type. One device of each type was assigned to the 200°C dynamic excitation test cell and shmoo plots were generated at the 4000 hour measurement point.

A control sample of five devices of each memory type was subjected to electrical performance measurements prior to the start of each interim test measurement period. The purpose of the control sample was to verify the long term stability of the automated test equipment.

TABLE 2-1. HIGH TEMPERATURE OPERATING LIFE TEST INTERIM ELECTRICAL MEASUREMENT SCHEDULE

CUMULATIVE HOURS	M38510/237, TABLE III		SMM00
	SUBGROUPS 1 & 9	SUBGROUPS 2, 3, 10 & 11	
0	X	X	X
168	X		
504	X	X	
1000	X	X	
1500	X		
2000	X	X	
4000	X	X	X

TABLE 2-2. HIGH TEMPERATURE NON-OPERATING LIFE TEST INTERIM ELECTRICAL MEASUREMENT SCHEDULE

CUMULATIVE HOURS	M38510/237, TABLE III	
	SUBGROUPS 1 & 9	SUBGROUPS 2, 3, 10 & 11
0	X	X
168	X	
504	X	
1000	X	
1500	X	
2000	X	X

TABLE 2-3. TEMPERATURE CYCLING INTERIM ELECTRICAL MEASUREMENT SCHEDULE

CUMULATIVE CYCLES	M38510/237, TABLE III	
	SUBGROUPS 1 & 9	SUBGROUPS 2, 3, 10 & 11
0	X	X
10	X	
50	X	
100	X	
150	X	
200	X	X

2.2 MEMORY TYPES

Two different LSI memory types were selected for reliability and life characterizations. These included a 1024 x 4 bit static RAM (AM9130) and a 4096 x 1 bit static RAM (AM9140), both implemented with NMOS technology and procured to the initial draft of the MIL-M-38510/237 specification requirements. A total of 120 memories of each part type was procured to MIL-STD-883, Class B equivalent processing requirements with the exception that a 168 hour, 125°C static burn-in was performed. Initially, it was hoped that the memories could be procured from multiple sources. However, the devices were only available from a single source. The manufacturer, part numbers, part description, and military specification references of the selected memories are shown in Table 2-4.

TABLE 2-4. MEMORY TYPES

MIL-M-38510 REFERENCE	PART TYPE	MANUFACTURER	MANUFACTURER PART NUMBER
/23704BWC	1024 x 4 BIT NMOS STATIC RAM 22 PIN CERAMIC DIP	ADVANCED MICRO DEVICES	AM9130ADM-B
/23712BWC	4096 x 1 BIT NMOS STATIC RAM 22 PIN CERAMIC DIP	ADVANCED MICRO DEVICES	AM9140ADM-B

NOTES:
1. ALL MEMORIES SCREENED TO MIL-STD-883, CLASS B WITH 168 HOUR, 125°C STATIC BURN-IN.
2. NOT QPL-38510 DEVICES.

3.0 RESULTS OF PHASE I INSPECTIONS AND TESTS

3.1 EXTERNAL VISUAL EXAMINATIONS AND HERMETICITY TESTS

All devices were shipped from the manufacturer in anti-static tube/rail type carriers and were examined for conformance to the purchase order requirements for device type, package style, lead finish and marking. Each device was examined at 10X magnification for evidence of damage to package, package seals, and leads per MIL-STD-883, Method 2009.1. Nine AM9130 and seven AM9140 devices exhibited chipped corners which appeared to be cosmetic defects. Subsequent hermeticity testing and electrical characterizations showed that the chipped corners were only cosmetic defects and all 16 devices were acceptable for the test program.

Following the external visual examinations, all devices were subjected to hermeticity testing to MIL-STD-883, Method 1014.1, Conditions A1 and C2. A single AM9140 device failed both fine and gross leak tests and was returned to the manufacturer for replacement. The replacement device was received from Advanced Micro Devices (AMD) shipped in a plastic bag (not anti-static material) and is shown in Figure 3-1. A summary of the visual inspections and hermeticity tests is presented in Table 3-1.

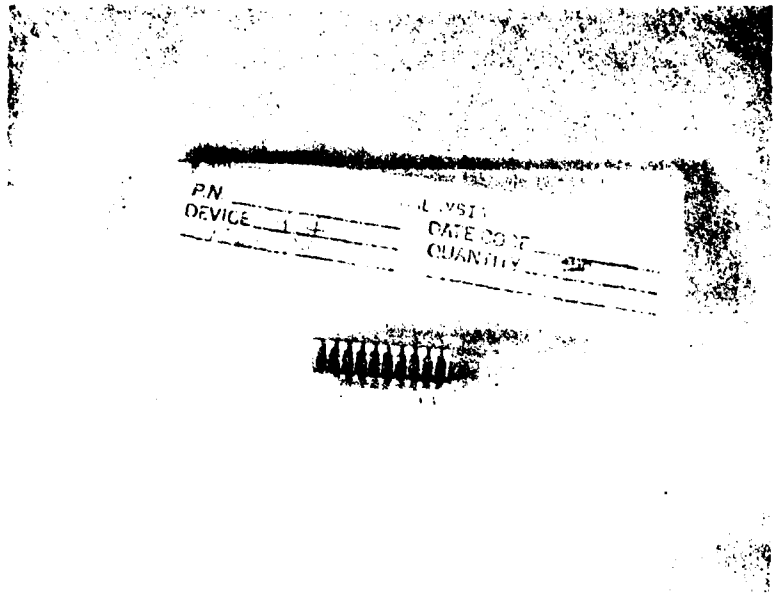


FIGURE 3-1. REPLACEMENT AM9140 DEVICE IN NON ANTI-STATIC MATERIAL

TABLE 3-1. INITIAL INSPECTION AND HERMETICITY TEST RESULTS

PART NUMBER	TOTAL TESTED	VISUAL INSPECTION		HERMETICITY TESTS				TOTAL FAILED ⚠2
		PASSED ⚠1	FAILED	FINE LEAK		GROSS LEAK		
				PASSED	FAILED	PASSED	FAILED	
AM9130	120	120	0	120	0	120	0	0
AM9140	120	120	0	119	1	119	1	1

NOTES:

⚠1 COSMETIC DEFECTS NOTED BUT DID NOT AFFECT SUBSEQUENT TESTS.

⚠2 SAME DEVICE FAILED BOTH FINE AND GROSS LEAK TESTS BUT DID NOT HAVE CHIPPED CORNERS.

4.0 RESULTS OF PHASE II CHARACTERIZATIONS

4.1 ELECTRICAL CHARACTERIZATIONS

Phase II activities were initiated with electrical characterizations of 120 devices of each part type. This characterization consisted of performing on a 100% basis all of the initial draft MIL-M-38510/237 specification electrical performance tests at 25°C, 125°C and -55°C. In addition, for a sample of two devices of each part type, shmoo plots were generated for chip enable access time as a function of supply voltage and temperature.

The electrical test conditions, test limits, waveforms, algorithms and tests for both part types are included in Appendix B. All electrical tests were in accordance with the initial draft of MIL-M-38510/237 with the following exceptions: a) output high voltage (V_{OH}) and output low voltage (V_{OL}) dc tests measurements and b) chip enable access time ($t_{a(CE)}$) measurements. To facilitate automated test measurements of V_{OH} and V_{OL}, both tests were performed by forcing the required output current and measuring the output voltage. The slash sheet requirements specify an output current measurement after forcing the output pin to a specified voltage. To assure that both the chip enable access time and output enable on delay (t_{CO}) parameters are within specification limits, the device output buffer must be turned off for a minimum of 280 nS. However, by changing the timing of the output enable buffer to be coincident with the chip enable pulse, a more accurate $t_{a(CE)}$ was measured. The t_{CO} parameter cannot be guaranteed with this measurement technique but it was decided based on previous experience that the chip enable access time would be the better indicator of device aging.

The earlier RADC funded, Reliability Evaluation and Electrical Characterization of Memories Program (Contract F30602-77-C-0003), included the AM9140 device for comprehensive electrical characterizations. The results of this program indicated that there was no observed pattern sensitivity for the AM9140 devices. The AM9130 device uses the identical oxide and diffusion masks as the AM9140 and differs only in the final metallization step. In-house studies at [illegible] tests indicated that there was also no pattern sensitivity for the AM9130 devices. The patterns for the earlier electrical characterization program included:

GALPAT, GALWRT, WALKING, ROWPAT, MARCH, ADDCOMP and SHIFTING DIAGONAL. A description of these algorithms is provided in Appendix B. The initial draft of the MIL-M-38510/237 specification (AM9130 and AM9140) required functional testing with the GALDIA, MARCH, CHECKERBOARD and CHECKERBOARD NOT patterns. Based on the results of the Reliability Evaluation and Electrical Characterization of Memories Program, it was decided to complete the 100% electrical tests with only the specified slash sheet test patterns.

A summary of the initial electrical characterization results are shown in Table 4-1. Nine (7.5%) AM9130 and five (4.2%) AM9140 failed to meet the requirements of the slash sheets. AMD replaced all the failed devices and the replacements passed all subsequent electrical tests. The devices that failed initial electrical tests were not subjected to failure analysis. However, a review of the failure data showed various V_{OH}, V_{OL}, I_{IH}, I_{CC} and functional test failures. It is not known how these devices passed the manufacturer's final electrical test prior to shipment, and AMD could/would not provide an explanation of the reject rate of the screened devices. However, it is believed that the 5.8% combined reject rate is excessive for devices screened to a MIL-M-38510 equivalent specification.

4.1.1 AM9130 Electrical Characterization Results

4.1.1.1 DC Tests - The test data for both part types are summarized for the test cells, i.e., devices allocated for temperature cycling tests, etc. These data summaries include both parameter mean and standard deviation values.

The results of the AM9130 electrical characterization dc tests for a typical test cell, i.e., non-operating life with ten devices, are shown in Table 4-2. The input/output leakage currents measured on the automated test system default to ± 50 nAdc as a minimum value. Therefore, for those parameters whose actual values lie between ± 50 nAdc, the computed mean ($\bar{x}$ ± 50 nAdc) and sigma (± 0) shown in the tables are not representative of the actual mean and sigma. The measured parameter values are well within the limits contained in the initial draft of MIL-M-38510/237.

TABLE 4-1. INITIAL ELECTRICAL PERFORMANCE MEASUREMENT RESULTS

PART NUMBER	TYPE OF TEST	T_A = 25°C		T_A = 125°C		T_A = -55°C		TOTAL FAILED (2)
		TESTED	FAILED	TESTED (1)	FAILED	TESTED (1)	FAILED	
AM9130	DC	120	6	111	0	111	0	6
	AC	120	9	111	0	111	0	9
	SHMOO	2	0	2	0	2	0	0
	TOTAL	120	9	111	0	111	0	9
AM9140	DC	120	3	115	0	115	0	3
	AC	120	3	115	0	115	0	3
	SHMOO	2	0	2	0	2	0	0
	TOTAL	120	5	115	0	115	0	5

NOTES:

(1) ONLY DEVICES THAT PASSED 25°C ELECTRICALS TESTED AT 125°C AND -55°C.

(2) AMD REPLACED ALL FAILED DEVICES. REPLACEMENTS PASSED ALL SUBSEQUENT ELECTRICAL TESTS.

TABLE 4-2. AM9130 INITIAL ELECTRICAL CHARACTERIZATIONS - DC TESTS

PARAMETER	MIL-M-38510/23704 TEST LIMITS MIN	MAX	T_A = 25°C MEAN	SIGMA	T_A = 125°C MEAN	SIGMA	T_A = -55°C MEAN	SIGMA	UNITS
I_{IH}		10	0.048	0.022	0.049	0.015	0.051	0.011	µA
I_{OH219}		↑	0.050	0.000	0.050	0.000	0.050	0.013	↑
I_{OH220}			0.050	0.000	0.050	0.000	0.048	0.025	
I_{OH221}			0.050	0.000	0.050	0.000	0.050	0.000	
I_{OH226}			0.050	0.000	0.050	0.000	0.051	0.009	
I_{OH222}			0.050	0.000	-0.195	0.072	0.046	0.024	
I_{OH223}			0.050	0.000	-0.195	0.068	0.050	0.000	
I_{OH224}		↓	0.050	0.000	-0.195	0.074	0.046	0.024	↓
I_{OH225}		10	0.050	0.000	-0.225	0.093	0.046	0.024	µAdc
I_{CC27}		125	85.600	4.603	64.400	3.180	102.000	6.518	mAdc
I_{CC28}		125	80.100	4.271	60.200	3.000	95.800	6.029	↑
I_{CC29}		89	60.500	3.232	45.300	2.132	72.200	4.429	↓
I_{CC30}		64	46.600	2.686	36.600	1.807	54.200	3.668	mAdc
V_{OH31}	2.2		4.070	0.059	3.990	0.058	3.950	0.050	Vdc
V_{OH32}	2.2		3.010	0.055	3.040	0.054	2.990	0.055	↑
V_{OL33}		0.4	0.139	0.014	0.183	0.016	0.116	0.013	↓
V_{OL34}		0.4	0.160	0.014	0.213	0.016	0.132	0.013	Vdc

NOTE
DATA FOR NON OPERATING LIFE TEST CELL WITH 10 DEVICES.

TABLE 4-3. AM9130 INITIAL ELECTRICAL CHARACTERIZATIONS - FUNCTIONAL TESTS

PARAMETER	MIL-M-38510/23704 TEST LIMITS MIN	MAX	T_A = 25°C MEAN	SIGMA	T_A = 125°C MEAN	SIGMA	T_A = -55°C MEAN	SIGMA	UNITS
READ/WRITE									
$t_{A(CE)}$; V_{CC} = 4.5 V									
MARCH		500	143.000	9.769	182.000	8.798	127.000	9.193	ns
MEMORY STATUS		500	161.000	8.012	186.000	9.376	150.000	7.896	ns
$t_{A(CE)}$; V_{CC} = 5.5 V									
MARCH		500	138.000	4.629	175.000	5.637	122.000	4.631	ns
READ/MODIFY/WRITE									
$t_{A(CE)}$; V_{CC} = 4.5 V									
MARCH		500	166.000	7.851	191.000	8.699	155.000	7.851	ns
$t_{A(CE)}$; V_{CC} = 5.5 V									
MARCH		500	146.000	6.455	171.000	6.511	135.000	5.843	ns

NOTE
DATA FOR NON OPERATING LIFE TEST CELL WITH 10 DEVICES.

4.1.1.2 Functional Tests - The results of AM9130 chip enable access time measurements performed while running functional tests for a typical test cell, i.e., non-operating life with ten devices, are shown in Table 4-3. Examination of the mean values of access time obtained for the MARCH, CHECKERBOARD, and CHECKERBOARD NOT patterns showed no pattern related variations and corroborated the results of the previous Reliability Evaluation and Electrical Characterization of Memories Program. GALDIA and MARCH pattern tests with a sample of two devices showed less than 5 nS difference in access time measurements. Therefore, the access time measurements for the GALDIA pattern were performed as a GO/NO-GO test to minimize the test times.

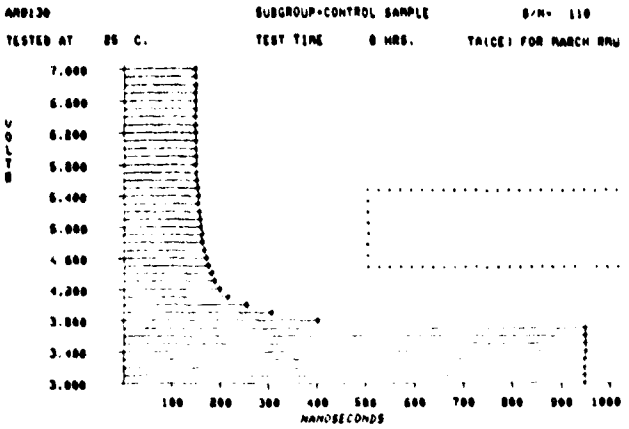
4.1.1.3 Shmoo Plots - The AM9130 shmoo plots of chip enable access time were generated as a function of the device supply voltage, V_{CC}. The access time shmoo plots for the MARCH pattern at 25°C, 125°C, and -55°C are illustrated in Figure 4-1. Additional shmoo plots generated at 125°C for various test patterns are included in Figure 4-2 and showed no pattern related variations. A review of the shmoo plots indicated there would be no device operating restrictions at the maximum rated supply voltage and maximum specified temperature.

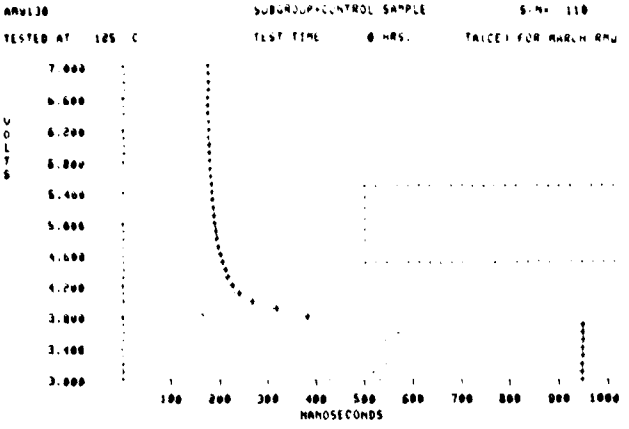
4.1.2 AM9140 Electrical Characterization Results

4.1.2.1 DC Tests - The results of the AM9140 electrical characterization dc tests for a typical test cell, i.e., non-operating life with ten devices, are shown in Table 4-4. The interpretation of the computed mean and sigma values for input/output leakage current are identical to the AM9130. These results are similar to the AM9130 and indicate parameter values are well within limits for the military specification requirements and the limits for the supply current (I_{CC27}) test parameter could be tightened.

4.1.2.2 Functional Tests - The results of the AM9140 chip enable access time measurements performed while running functional tests for a typical test cell, i.e., non-operating life with ten devices, are shown in Table 4-5. These results are similar to the AM9130 and indicate no pattern related variations.

4.1.2.3 Shmoo Plots - The AM9140 shmoo plots of chip enable access time were generated as a function of the device supply voltage, V_{CC}. Figure 4-3 illustrates the access time shmoo plots for the MARCH pattern at 25°C, 125°C, and -55°C.





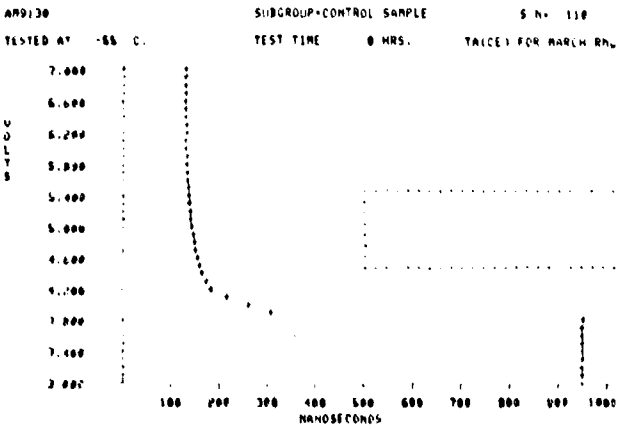
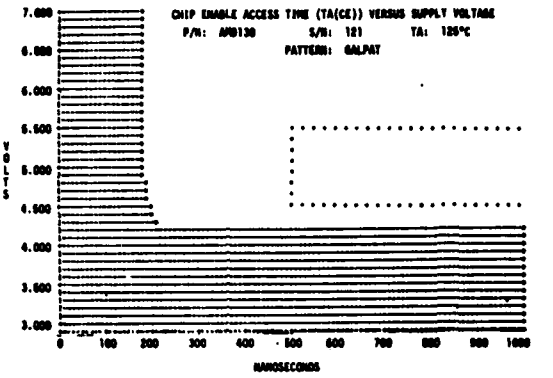
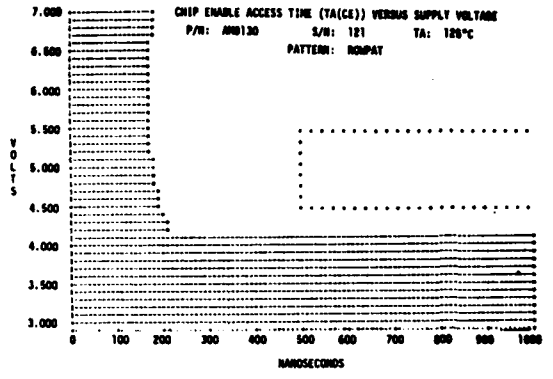


FIGURE 4-1 AM9130 TYPICAL SUB500 PLOTS FOR CHIP ERASE ACCESS TIME





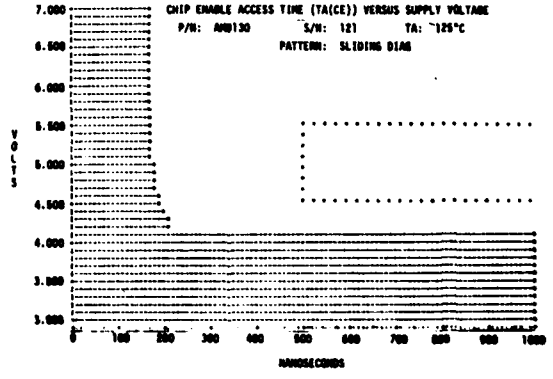


FIGURE 4-2. AM9130 SHMOO PLOTS FOR CHIP ENABLE ACCESS TIME - VARIOUS PATTERNS

TABLE 4-4. AM9140 INITIAL ELECTRICAL CHARACTERIZATIONS - DC TESTS

PARAMETER	MIL-M-38510/23712 TEST LIMITS		T_A = 25°C		T_A = 125°C		T_A = -55°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}		10	0.051	0.010	0.051	0.008	0.050	0.000	µAdc
I_{OHZ19}		↕	0.050	0.000	0.050	0.000	0.090	0.097	↕
I_{OHZ20}			0.050	0.000	0.050	0.000	0.090	0.097	
I_{OHZ21}			0.050	0.000	0.050	0.000	0.095	0.097	
I_{OHZ26}			0.050	0.000	0.050	0.000	0.085	0.094	
I_{OLZ22}			0.050	0.016	0.075	0.026	0.055	0.016	
I_{OLZ23}			0.050	0.000	0.060	0.021	0.055	0.016	
I_{OLZ24}		↕	0.050	0.000	0.075	0.026	0.060	0.021	↕
I_{OLZ25}		10	0.050	0.000	0.080	0.026	0.055	0.016	µAdc
I_{CC27}		125	79.200	6.889	63.900	4.110	86.300	7.048	mAdc
I_{CC28}		125	74.100	6.841	59.600	4.074	80.600	6.995	↕
I_{CC29}		89	55.800	4.878	44.900	2.892	61.000	4.941	↕
I_{CC30}		64	42.200	4.021	36.100	2.598	46.200	4.436	mAdc
V_{OH31}	2.2		4.160	0.145	4.100	0.138	4.160	0.149	Vdc
V_{OH32}	2.2		2.950	0.127	2.970	0.125	2.930	0.119	↕
V_{OL33}		0.4	0.125	0.006	0.160	0.014	0.113	0.007	↕
V_{OL34}		0.4	0.147	0.009	0.189	0.019	0.132	0.009	Vdc

NOTE:
DATA FOR NON-OPERATING LIFE TEST CELL WITH 10 DEVICES.

TABLE 4-5. AM9140 INITIAL ELECTRICAL CHARACTERIZATIONS - FUNCTIONAL TESTS

PARAMETER	MIL-M-38510/23712 TEST LIMITS		T_A = 25°C		T_A = 125°C		T_A = -55°C		UNITS
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
READ/WRITE									
$t_{A(CE)}$, V_{CC} = 4.5 V									
MARCH		500	167.000	17.420	189.000	17.870	155.000	15.840	nS
CHECKERBOARD		↕	166.000	17.320	188.000	17.580	154.000	15.710	↕
CHECKERBOARD NOT		↕	166.000	17.320	188.000	17.690	154.000	16.160	↕
MEMORY STATUS		500	177.000	17.970	200.000	20.020	162.000	17.160	nS
$t_{A(CE)}$, V_{CC} = 5.5 V									
MARCH		500	155.000	13.960	177.000	15.210	143.000	13.530	nS
CHECKERBOARD		↕	154.000	14.820	176.000	15.210	142.000	12.380	↕
CHECKERBOARD NOT		↕	154.000	14.820	176.000	15.210	142.000	12.790	↕
MEMORY STATUS		500	166.000	16.480	190.000	18.730	154.000	15.100	nS
READ/MODIFY/WRITE									
$t_{A(CE)}$, V_{CC} = 4.5 V									
MARCH		500	165.000	16.470	186.000	17.680	152.000	13.290	nS
$t_{A(CE)}$, V_{CC} = 5.5 V									
MARCH		500	154.000	14.360	174.000	15.540	141.000	13.000	nS

NOTE
DATA FOR NON OPERATING LIFE TEST CELL WITH 10 DEVICES.

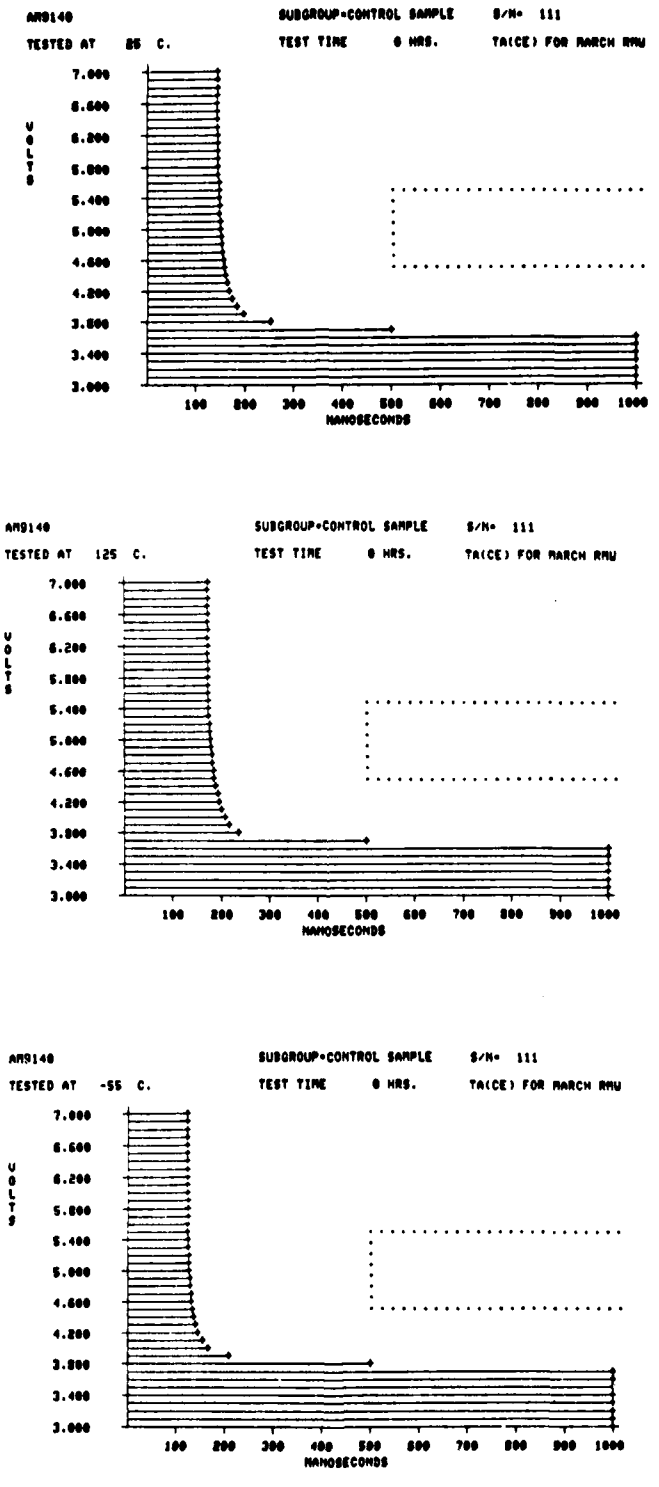


FIGURE 4-3. AM9140 TYPICAL SHMOO PLOTS FOR CHIP ENABLE ACCESS TIME

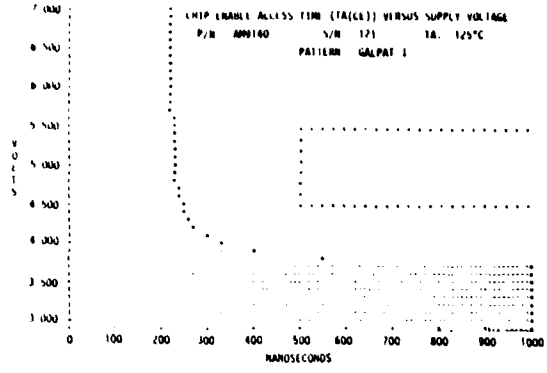
Additional shmoo plots for various test patterns generated at 125°C are included in Figure 4-4 and showed no pattern related variations. The AM9140 can be operated at the maximum rated supply voltage and maximum specified temperature.

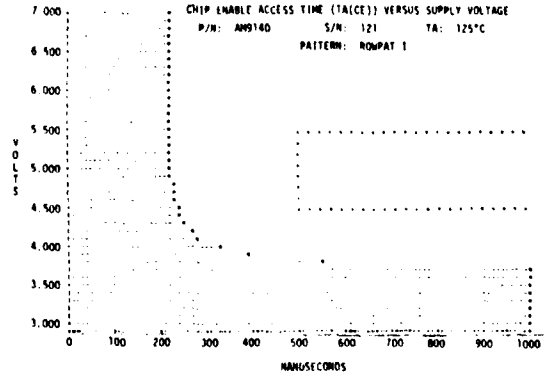
4.1.3 Analysis of Electrical Characterization Results - Electrical characterization test results were used to compute the maximum power dissipation for both part types. Discussion of the dc and functional test results are also included in subsequent paragraphs.

4.1.3.1 Power Dissipation - The results of power dissipation calculations for all test cells for 25°C, 125°C and -55°C are shown in Table 4-6. The average values of the maximum power dissipation at each temperature were obtained from the products of average values of device supply current and the maximum value of device supply voltage. The worst case values shown in Table 4-6 were calculated as the product of the average plus three sigma (3σ) values of the device supply current and maximum supply voltage (V_{CC}=5.5 Vdc). The worst case power dissipation values are shown for each ambient temperature for the quiescent state. The maximum power dissipation values are within the limits (P_D=1.25 W) specified by the manufacturer. The results of these calculations indicate homogeneous test cells.

4.1.3.2 DC Tests - The test results indicated that the distributions of all parameters were within the manufacturer's limits and tightened limits for the supply current (I_{CC2}) could be incorporated in the released version of the MIL-M-38510/237 specifications.

4.1.3.3 Functional Tests - The MARCH pattern was the most effective (100) pattern in detecting all the initial functional test failures. The GALDIA and CHECKERBOARD patterns detected 56 to 67 of the functional failures. These results are in agreement with a previously conducted electrical characterization program [1]. The MARCH pattern was the only common pattern for both test programs. However, both test programs showed no N^2 or N pattern related variations and an N^2 pattern for these 4K RAMs is probably unnecessary. In addition, AMD does not include the GALDIA pattern for functional test of its commercial devices.





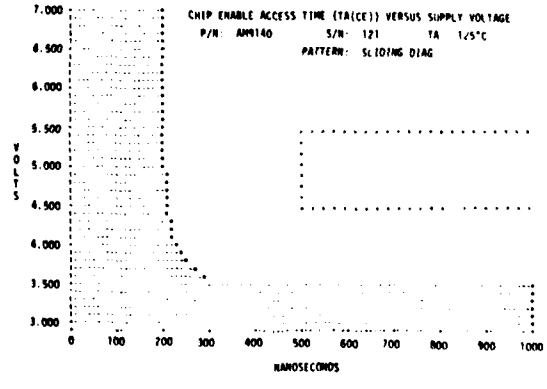


FIGURE 4-4. AM9140 SHMOO PLOTS FOR CHIP ENABLE ACCESS TIME - VARIOUS PATTERNS

TABLE 4-6. DEVICE POWER DISSIPATION

PART TYPE	TEST CELL	CELL TEMP °C	MAXIMUM POWER DISSIPATION - AVERAGE T_A = 25°C	T_A = 125°C	T_A = -55°C,	MAXIMUM POWER DISSIPATION WORST CASE	UNITS
AM9130	STATIC	200	492	368	594	736	mW
	STATIC	175	474	351	572	673	▲
	DYNAMIC	200	483	373	594	753	|
	DYNAMIC	175	468	354	572	695	|
	STORAGE	275	471	354	561	669	▼
	TEMPERATURE CYCLING	-65 150	496	374	594	710	mW
AM9140	STATIC	200	430	332	496	617	mW
	STATIC	175	430	345	473	559	▲
	DYNAMIC	200	428	348	480	570	|
	DYNAMIC	175	437	369	474	522	|
	STORAGE	275	436	351	476	593	▼
	TEMPERATURE CYCLING	-65 150	394	314	438	594	mW

NOTE:
POWER DISSIPATION COMPUTED FOR EACH TEST CELL PRIOR TO LIFE TESTS.

Plots of the worst case values of chip enable access time for a typical test cell as a function of temperature, as shown in Figures 4-5 and 4-6, illustrated the temperature dependence of this parameter.

4.2 PHYSICAL CHARACTERIZATIONS

Physical characterizations of two devices of each part type were performed to determine the construction methods, manufacturing process techniques, materials and detail device schematics. The devices were subjected to detailed optical, SEM and radiographic examinations, energy dispersive x-ray analysis, angle sectioning and bond pull testing. A summary of the major construction features for the AM9130 and AM9140 are shown in Table 4-7. The detailed results of these analyses are provided in Appendix A.

The results of physical characterizations showed the following: a) an uneven eutectic coverage beneath the die of all the devices examined, b) identical diffusion/oxide masks for both the AM9130 and AM9140 with only different metallization masks to achieve the required memory organization, c) no material used in the manufacturing process that would limit life test temperatures, d) the observed test probe marks do not compromise the device's bond strength, and e) the detail circuit schematics are in agreement with the initial draft of the MIL-M-38510/237 logic diagrams.

The coverage in the eutectic for one AM9130 was approximately eighty-five percent (85%) but within the specified requirement of fifty percent (50%) die attach coverage per MIL-STD-883, Method 2010.3. The uneven eutectic coverage will impede heat conduction from the die to package and result in some devices operating with higher junction temperature than others. A sample of devices that passed the stress tests as well as all devices that failed the stress tests were examined radiographically. These results showed no relationship between uneven eutectic coverage and the occurrence of failures during the life tests.

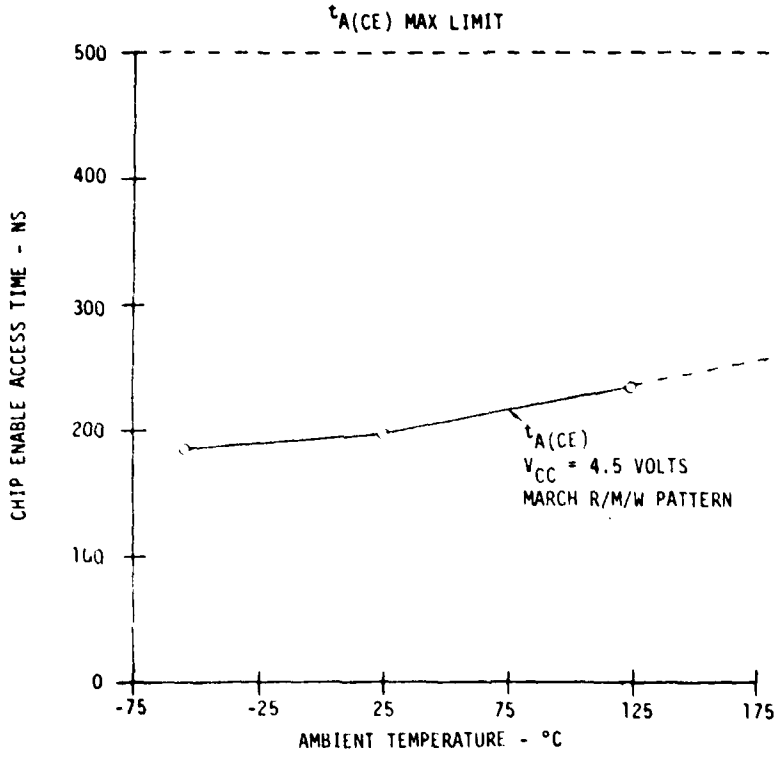


FIGURE 4-5. AM9130 WORST CASE CHIP ENABLE ACCESS TIME VERSUS AMBIENT TEMPERATURE FOR A TYPICAL TEST CELL

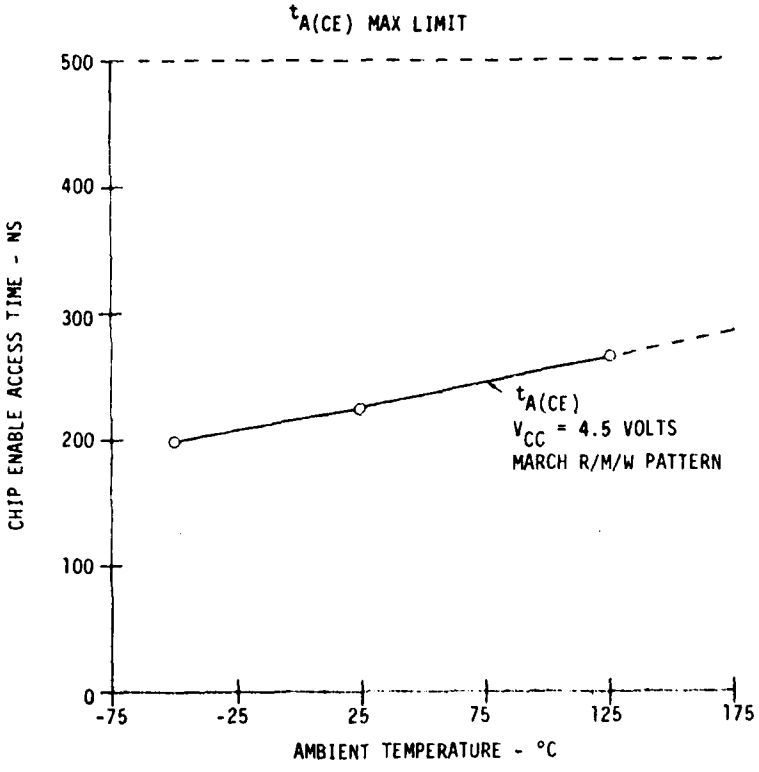


FIGURE 4-6. AM9140 WORST CASE CHIP ENABLE ACCESS TIME VERSUS AMBIENT TEMPERATURE FOR A TYPICAL TEST CELL

TABLE 4-7. MAJOR CONSTRUCTION DETAILS

PART NUMBER	AM9130 MIL-M-38510/23704	AM9140 MIL-M-38510/23712
DESCRIPTION	1Kx4 NMOS STATIC RAM	4Kx1 NMOS STATIC RAM
MANUFACTURER	ADVANCED MICRO DEVICES	ADVANCED MICRO DEVICES
PACKAGE TYPE	22 PIN CERAMIC DIP	22 PIN CERAMIC DIP
LID SEAL	SOLDER	SOLDER
LEAD MATERIALS		
EXTERNAL FRAME	GOLD PLATED KOVAR REFRACTORY METAL/ NICKEL PLATED	GOLD PLATED KOVAR REFRACTORY METAL/ NICKEL PLATED
DIE		
ATTACH METALLIZATION SCRIBE	GOLD/SILICON EUTECTIC ALUMINUM MECHANICAL	GOLD SILICON EUTECTIC ALUMINUM MECHANICAL
WIRE BONDS		
MATERIAL CHIP FRAME	ALUMINUM ULTRASONIC ULTRASONIC	ALUMINUM ULTRASONIC ULTRASONIC
MEMORY CELL	6 TRANSISTOR CELL	6 TRANSISTOR CELL

Probe marks were noted on several bond pads and AMD related that all pads are probed during die level testing with the exception of the Memory Status pad. A bond pull test was performed to determine if bonding over probe mark sites would result in inadequate bond strength. All bonds passed the MIL-STD-883, Method 2011.2 bond pull requirement of 1.7 grams for a 1.1 mil aluminum wire. No bond wire lifted from the bond pad.

RADC performed Gas Mass Spectometer (GMS) analysis of four devices to determine the package atmosphere. The percentage of all constituents identified in GMS analysis are presented in Appendix A, Table A4.

4.3 RELIABILITY CHARACTERIZATIONS

Reliability characterizations of each device type were performed to establish the electrical and environmental conditions to be used in subsequent stress tests. The selected test conditions must provide adequate stressing of anticipated failure mechanisms without inducing failure modes that are not typical under normal operating conditions. For this study both static and dynamic excitations were used to stress the memory devices. The failure mechanisms for the AM9130 and AM9140 were expected to be similar to other NMOS LSI devices such as surface instability and dielectric breakdown. Therefore, the charge migration mechanisms would be accelerated by the static excitation bias circuits and mechanical mechanisms such as dielectric breakdown in the memory cell matrix would be accelerated by the dynamic excitation bias circuits. Since all type of failure mechanisms were expected, the requirements for the test program included both static and dynamic excitations.

4.3.1 Selection of Static Excitation Test Conditions - The effectiveness of the reliability characterization is based primarily upon the choice of accelerating stresses. A major part of this program was devoted to the selection of suitable combinations of electrical and thermal stresses for the accelerated life testing. The major considerations in defining the static excitation bias

circuits were: a) device operational modes, b) input address selection, and c) output load conditions. In addition, the candidate static bias circuits were required to meet the following criteria:

a) maintain maximum rated voltage across the device to provide maximum acceleration of surface effect failure mechanisms,

b) maintain the device current at a controlled low level to minimize failures due to thermal runaway and electromigration, and

c) maintain a consistent set of output voltage conditions over the temperature range.

To establish a consistent set of internal memory stress conditions, it is necessary to clock the data and control signals into the test device. However, this approach would not provide a valid comparison of static and dynamic excitations. Therefore, "fully static" configurations were used for this program and random data was stored in the device memory each time power was initially applied to the device.

A study of the device logic diagrams and schematics provided the possible operational modes available. These included the: a) read mode, b) write mode, c) high output impedance mode, and d) precharge mode. The truth tables for the AM9130 and AM9140 to place the DUT into each of these operational modes are shown in Tables 4-8 and 4-9, respectively. The read, write and high output impedance modes were the only operational modes included for static excitation bias circuits. The precharge mode was not considered because the outputs were in an indeterminite state, i.e., the previous state of the data output or the high impedance state.

The device address inputs may be selected from one of 1024 combinations for the AM9130 and one of 4096 combinations for the AM9140. Since the data stored into the DUT memory is random and unpredictable, input addresses with both positive and zero volts applied to the gate are acceptable. It is expected that the positive voltage across the gate oxides would accelerate the N-channel transistor failures due to cation contamination in the gate oxide.

TABLE 4-8. AM9130 TRUTH TABLE

Operation	Inputs R/W	$\overline{CS}$	A_{DD}	CE	OE	OD	Outputs I/O1 - I/O4
1. Chip Not Selected	X	H	X	H	X	X	HIZ
2. Write "L" in Cell A_{XY}	L	L	A_{XY}	H (or	L X	X H)	L (externally driven)
3. Write "H" in Cell A_{XY}	L	L	A_{XY}	H (or	L X	X H)	H (externally driven)
4. Read Data in Cell A_{XY}	H	L	A_{XY}	H	H	L	Data in Cell A_{XY}
5. CE Low-Chip Precharge	X	X	X	L	X	X	Previous DO if OE = H and OD = L or else HIZ

NOTES:
1. Data-out is the same as the original data-in.
2. CE is a clocking pulse and the "H" represents the first part of the cycle (UP level) and "L" represents the second part (DOWN level).
3. X's are "Don't Cares".
4. A_{XY} denotes proper address logic to address cell A_{XY}.

TABLE 4-9. AM9140 TRUTH TABLE

Operation	Inputs R/$\overline{W}$	DI	$\overline{CS}$	A_{DD}	CE	OE	OD	Outputs DO
1. Chip Not Selected	X	X	H	X	H	X	X	HIZ
2. Write "L" in Cell A_{XY}	L	L	L	A_{XY}	H	X	X	L
3. Write "H" in Cell A_{XY}	L	H	L	A_{XY}	H	X	X	H
4. Read Data in Cell A_{XY}	H	X	L	A_{XY}	H	H	L	Data in Cell A_{XY}
5. CE Low-Chip Precharge (NOTE: 4)	X	X	X	X	L	X	X	Previous DO if OE = H and OD = L or else HIZ

NOTES:
1. Data-out is the same as the original data-in.
2. CE is a clocking pulse and the "H" represents the first part of its cycle (UP level) and "L" represents the second part (DOWN level).
3. X's are "Don't Cares".
4. When CE = L, the DO is in an active state unless OE = L or OD = H.

The zero volts on the gate would bias the transistor off and accelerate failures due to contamination in/on the passivation. Previous preliminary static bias evaluations were performed for the AM9140 device during the Reliability Evaluation and Electrical Characterization of Memories Program. These results showed that there was negligible difference in the device operating current for the various address inputs selected. The input address conditions included: a) all addresses high, b) all addresses low and c) half the addresses high and half the addresses low. Based upon these results it was decided to bias half the addresses high and half the addresses low during static bias evaluations.

The output load conditions are dependent upon the DUT output state. Since the output states are random and unpredictable, the output load should include both pull up and pull down resistors. However, the output load current will not significantly increase the junction temperature of the output transistors. The rated output load current (I_{OL}) is 3.2 mAdc with a 0.4 Vdc maximum output low (V_{OL}) voltage. The maximum power dissipated in the device output transistor is 1.28 mW. Consideration was also given to the use of an output load to accelerate electron injection. However, the accelerating conditions for electron injection are low temperature, high voltage and high channel current [2]. In addition, the AM9130 uses a single Input/Output (I/O) pin for writing and reading data. During a static excitation write mode, the I/O acts as an input pin. When the AM9130 device is in the high output impedance or "OFF" state, the output resistor load has negligible effect on the DUT output circuitry. Similar output conditions exist for the AM9140 device. Therefore, all static excitation bias circuits included no output load.

4.3.2 Static Excitation Circuit Evaluations - Using the major considerations identified in Section 4.3.1, three static excitation bias circuits were evaluated. Figure 4-7 illustrates the three static bias configurations for the AM9130. The AM9130 device was biased in the read, write and high output impedance modes with half the addresses high and half the addresses low and no output load. The results of evaluating the AM9130 device in these circuits over the etmperature range from 125°C through 250°C indicated no appreciable

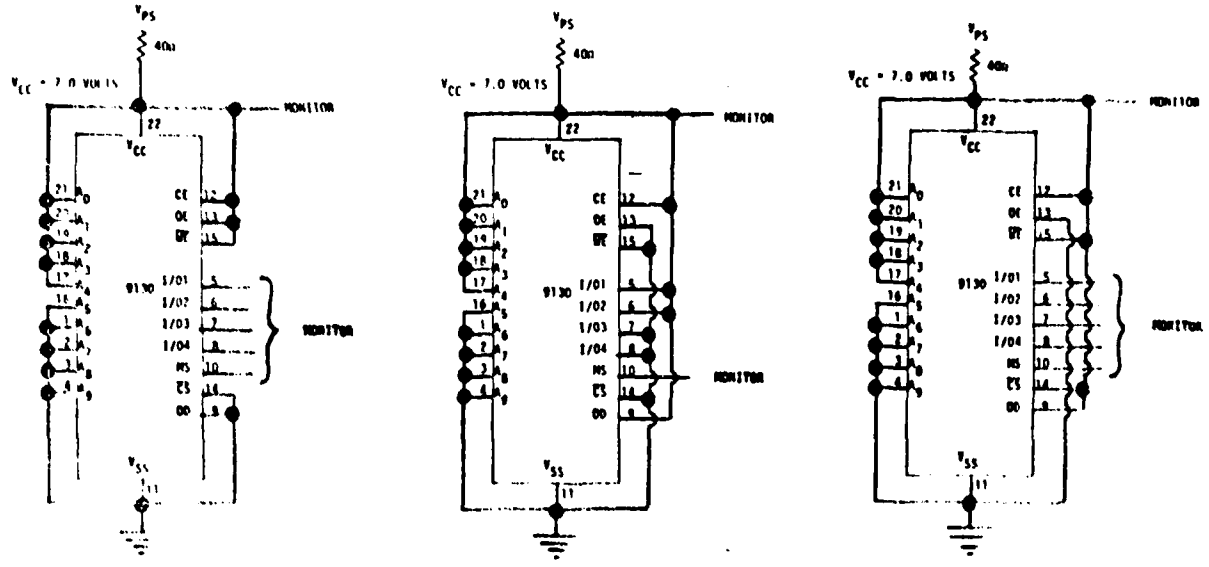


FIGURE 4-7. AM9130 CANDIDATE STATIC EXCITATION BIAS CIRCUITS

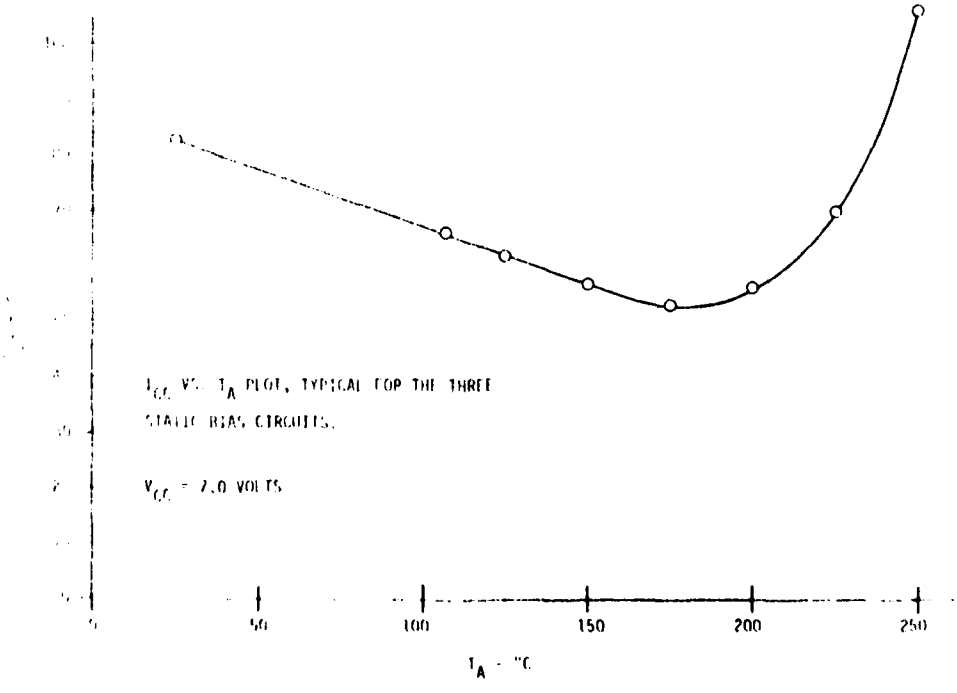


FIGURE 4-8. TYPICAL AM9130 STATIC EXCITATION BIAS CIRCUIT EVALUATION

difference among the three configurations. The device V_{CC} voltage during these tests was maintained at 7.0 Vdc. A typical plot of device I_{CC} current as a function of ambient temperature for the read mode is shown in Figure 4-8. For all three circuit configurations there was less than 2 mAdc difference between the I_{CC} values in each circuit over the evaluation temperature range. The write mode static circuit currents were approximately 2 mAdc higher, but this difference is not considered important.

The bias evaluation results showed that at 225°C, the outputs that were monitored either had changed state or were on the verge of changing state. At 250°C, all outputs had switched to a complementary state. Therefore, the maximum temperature at which the device could be properly operated for all configurations was 200°C. The read mode circuit was selected for further step-stress testing because with the devices outputs enabled, it permits monitoring of the output pins for changes in internal operating states.

The AM9140 device static excitation bias circuits are shown in Figure 4-9. These circuits are similar to the AM9130 configurations which included read, write and high output impedance modes with half the addresses high and half the addresses low with no output load. The results showed no appreciable difference for the three configurations. The operating temperature range was from 125°C through 250°C with the device V_{CC} voltage maintained at 7.0 Vdc. Figure 4-10 shows a typical plot of device current as a function of ambient temperature for the read mode. The three circuit configurations showed less than 3 mAdc difference between the I_{CC} values in each circuit over the evaluation temperature range. This minimal difference was not considered important in the selection of the step-stress circuit. For all configurations the monitored outputs had changed states or were on the verge of changing states at 225°C. At 250°C, the output had switched to a complementary state. Therefore, the test device could be properly operated at a maximum temperature of 200°C. The read circuit was selected for step-stress testing. The advantage of this circuit is that with the output enabled the device can be monitored for changes in internal operating states.

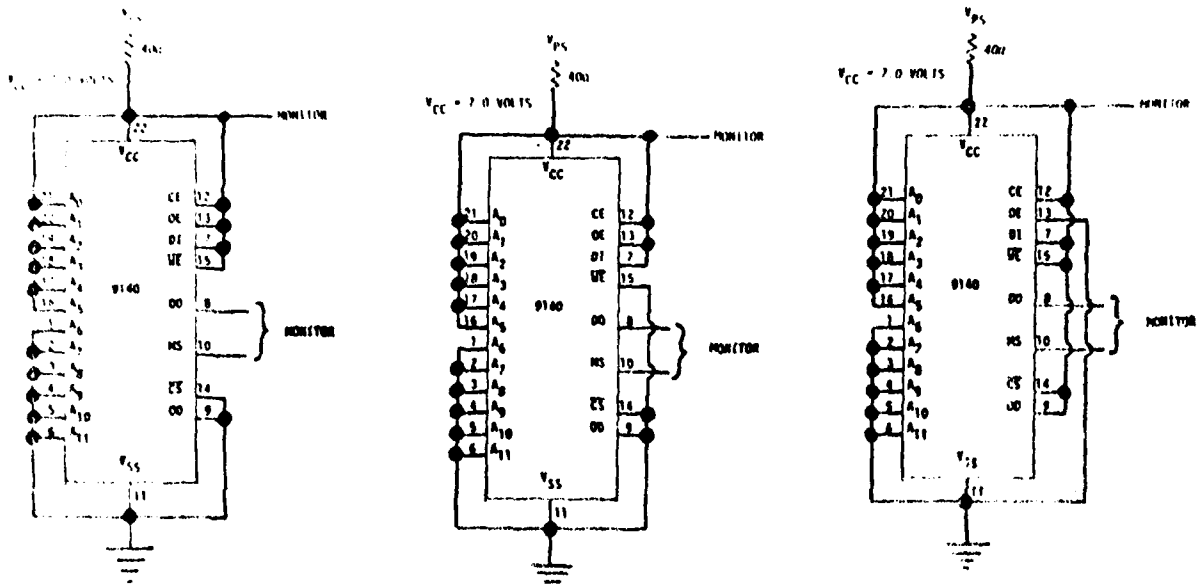


FIGURE 4-9. AM9140 CANDIDATE STATIC EXCITATION BIAS CIRCUITS

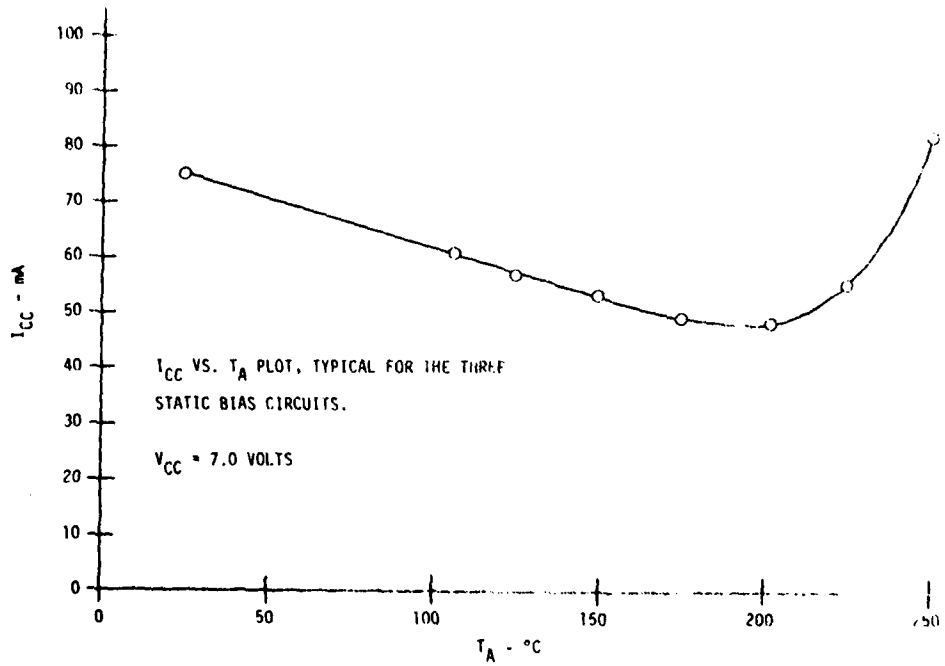


FIGURE 4-10. TYPICAL AM9140 STATIC EXCITATION BIAS CIRCUIT EVALUATION

The manufacturer's static burn-in circuits for both device types are shown in Figure 4-11. Static bias circuit evaluations of these circuits at V_{CC} of 7.0 Vdc for the AM9130 and AM9140 indicated similar results to the circuits of Figure 4-7 and 4-9. Device output switching occurred at 225°C with device currents within 3 mAdc of the MDAC-St. Louis configurations. However, these configurations were not selected because the address inputs selected did not include zero volts on the gate to accelerate failures due to contamination in/on the passivation.

4.3.3 Selection of Dynamic Excitation Test Conditions - The dynamic excitation bias evaluations provide electrical stress conditions that are similar to the device usage conditions. This is the main criteria in designing dynamic life test circuits. Other major considerations in establishing the dynamic excitation bias circuits were: a) device operational modes, b) data pattern selection, c) output load conditions, and d) operating frequency. In addition, the candidate static bias circuits were required to meet the following criteria:

a) maintain maximum rated voltage across the device to provide maximum acceleration of surface effect failure mechanisms,

b) maintain the device current at a controlled low level to minimize failures due to thermal runaway and electromigration, and

c) maintain a consistent set of internal memory stress conditions over the temperature range.

The three different dynamic operating modes are the read, write and read/modify/write (R/M/W) modes. The device timing diagrams for these modes are included in Appendix B. The possible modes for dynamic evaluations are the read/write, continuous read, continuous write, and read/modify/write modes. Combinations of the read cycle followed by a succession of write cycles and vice versa were not considered. Since the data retrieval and storage for a read/write cycle operates at a slower frequency, the read/modify/write cycle (read and write during the same cycle) was selected. In addition, the effects of continuous read cycles and continuous write cycles were also

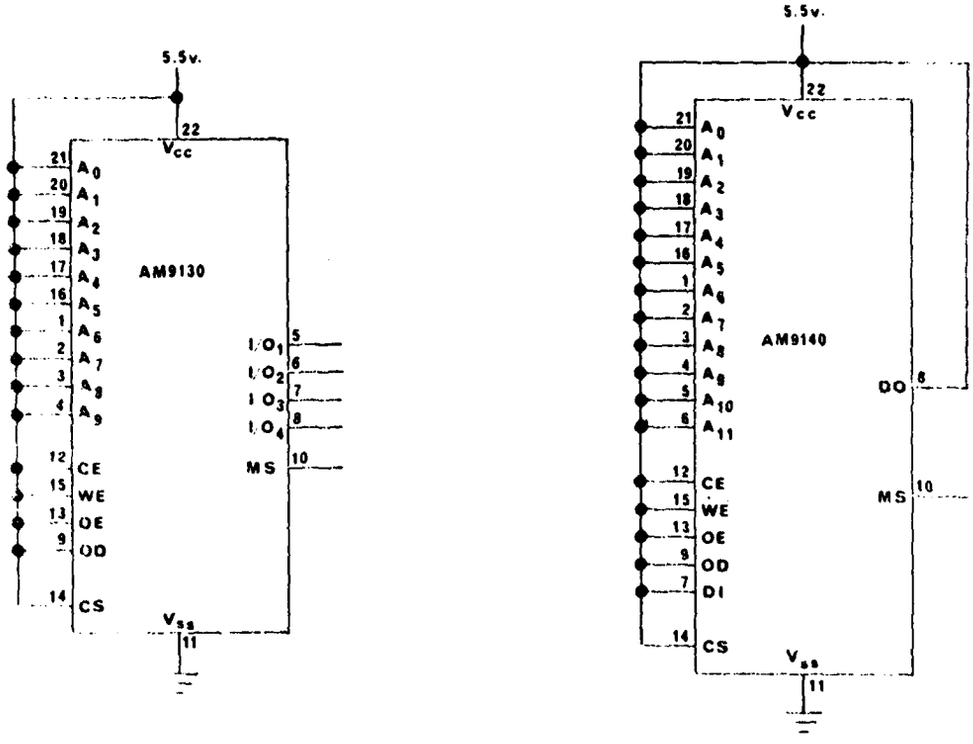


FIGURE 4-11. MANUFACTURER'S BURN-IN CIRCUITS

evaluated. Prior to performing continuous read cycles, the selected data pattern was written into all memory cells. This operating cycle was intended to stress the sense amplifier circuitry. During the continuous write cycles, it was intended to stress the write amplifier circuitry and observe the effects.

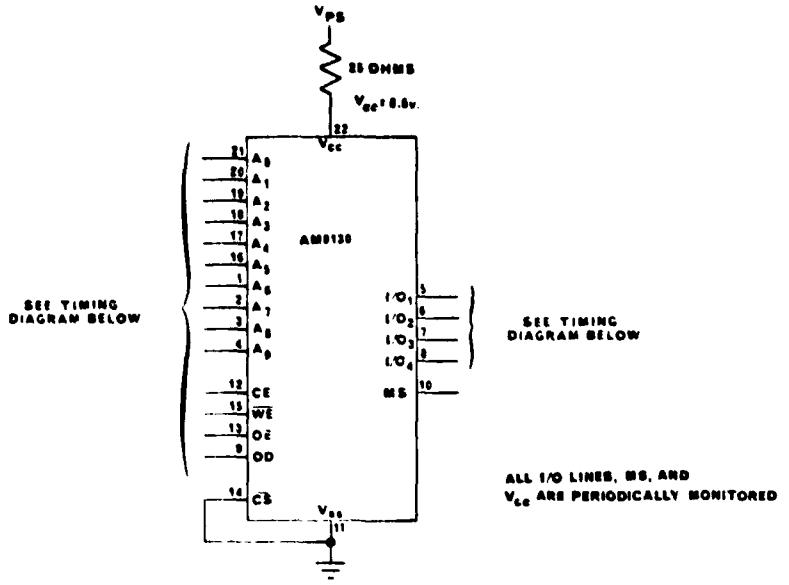
N^2, $N^{3/2}$ and N type data patterns were considered for high temperature device operations. Proper pattern selection is necessary in establishing the worst case stress on the test device. However, to accelerate the random defect failures it was necessary for the data pattern to write the same data in each memory location. With this approach the identical stress levels are placed on each active element every time data is written/read from the DUT memory. If these stresses cause the charges on a particular transistor to move toward the $Si\text{-}SiO_2$ interface, subsequent cycles reinforce this effect. Hence, using this groundrule both N^2 and $N^{3/2}$ patterns were not implemented. Many N type patterns met this criteria but the patterns were limited to: a) all "1's" in the entire memory, b) all "0's" in the entire memory and c) an field of alternating "1's" and "0's" (CHECKERBOARD). Other data patterns with both "1's" and "0's" combinations are available but the checkerboard pattern is the only pattern that provided the effects of complementary data in adjacent cell locations. It is also essential that "topogicaly pure" patterns based on the correct bit map and proper address sequence be used for dynamic bias evaluations.

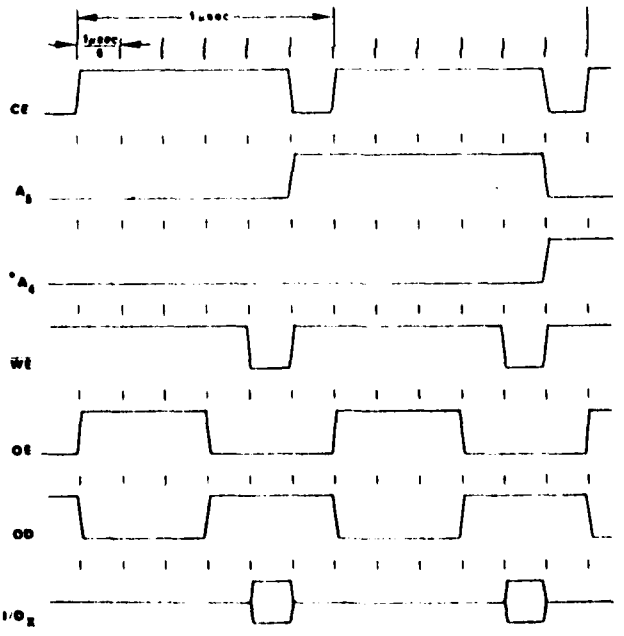
For dynamic excitation test conditions a suitable output device load is necessary to simulate part usage in system applications. Typical applications show the data outputs of a memory device driving the data bus of a microprocessor. Since the output load of the AM9130 and AM9140 is MOS, a capacitive load is satisfactory for characterizations and stress testing. The output load used for dynamic bias evaluations was a 30 pF load.

The final consideration for the dynamic bias circuits was the device operating frequency. A literature search produced no information concerning the effects of the device frequency in conducting an accelerated life test. The MDAC-St. Louis designed dynamic driver circuit operated both part types at near the maximum operating frequency.

4.3.4 Dynamic Excitation Circuit Evaluations

Three dynamic excitation bias circuits (continuous read, continuous write and read/modify/write modes) were evaluated using the considerations and criteria of Section 4.3.3. The AM9130 circuit and timing diagrams for the read/modify/write mode are shown in Figure 4-12. For the continuous read mode, the Write Enable ($\overline{WE}$) signal is switched to a high state for the total cycle time after the power up sequence with the proper pattern written into the memory. For the continuous write mode, the $\overline{WE}$ signal is switched to a low state for the total cycle time immediately after the power up sequence. The three dynamic bias circuits were operated in the temperature range of 125°C to 230°C with a CHECKERBOARD pattern. Initially, the device supply voltage was 5.5 Vdc, but between 212°C and 230°C, the supply voltage was varied between 5.5 Vdc and 7.0 Vdc. This was done to observe changes in device operation at the same voltage as the static bias evaluations. The AM9130 device showed no appreciable difference in device currents among the three dynamic configurations. Figure 4-13 shows a typical plot of device I_{CC} current as a function of ambient temperature. There was less than 1 mAdc difference in I_{CC} current among the three configurations. The difference in device current between the static and dynamic excitations bias evaluation was also negligible (<1 mAdc). The AM9130 device was functional at 211°C but nonfunctional at 225°C and was not affected by the supply voltage changes. This was similar to AM9130 static bias evaluations which switched in the same range of ambient temperatures. The AM9130 device performed suitably in all three modes and all the circuits were acceptable for step-stress testing. The AM9130 timing waveforms at 25°C, 200°C and 230°C for the R/M/W, continuous read and continuous write modes, are shown in Figure 4-14. The waveforms show that the I/O signals are stable at 200°C for all modes, but were unstable and nonfunctional at 230°C. Based on preliminary evaluations all dynamic bias





*THE FREQUENCIES OF THE SUBSEQUENT ADDRESS LINE SIGNALS ARE HALF THE FREQUENCY OF THE PRECEDING ADDRESS LINE SIGNAL.

**THE WAVEFORM ONLY ILLUSTRATES THE SIGNAL ON THE I/O LINE RESULTING FROM THE DYNAMIC BIAS CIRCUIT DRIVER.

ROW ADDRESS: LSB = A_0, MSB = A_8

COLUMN ADDRESS: LSB = A_9, MSB = A_{17}

FIGURE 4-12. AM9130 CANDIDATE DYNAMIC EXCITATION BIAS CIRCUIT

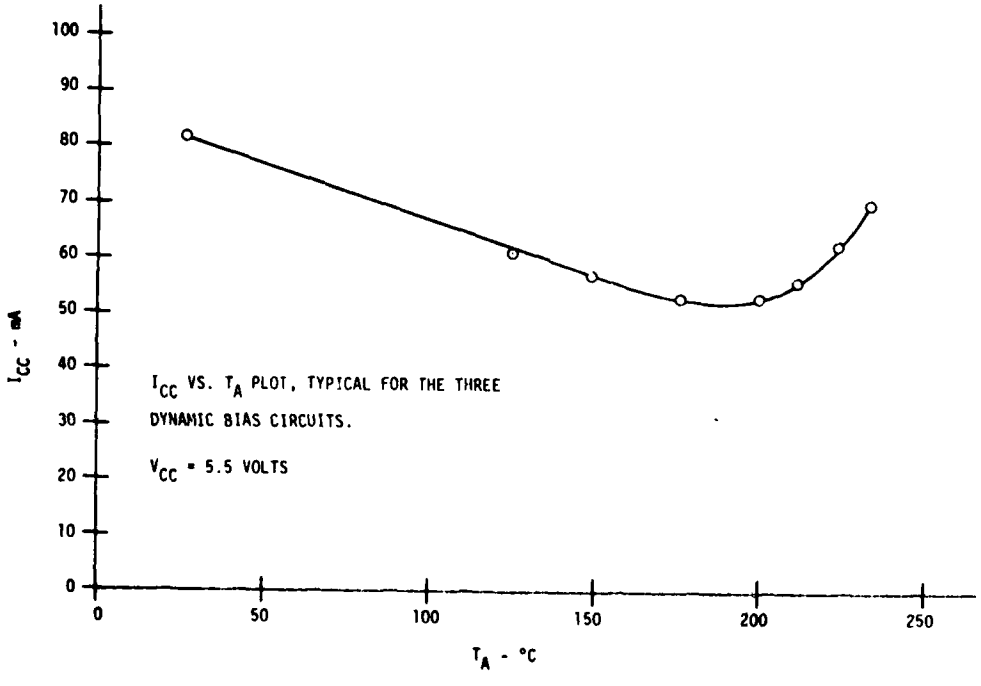


FIGURE 4-13. TYPICAL AM9130 DYNAMIC EXCITATION BIAS CIRCUIT EVALUATION

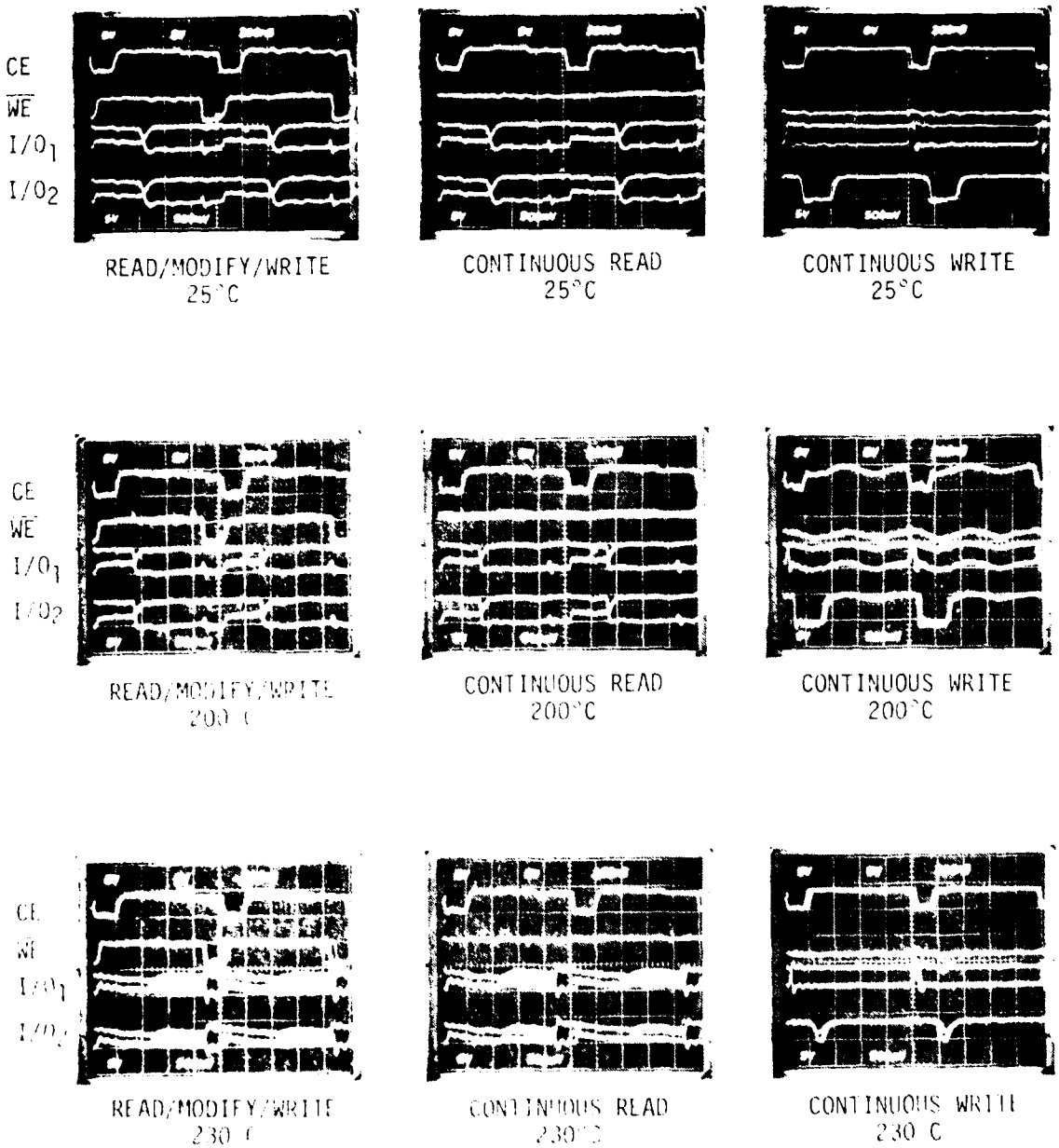
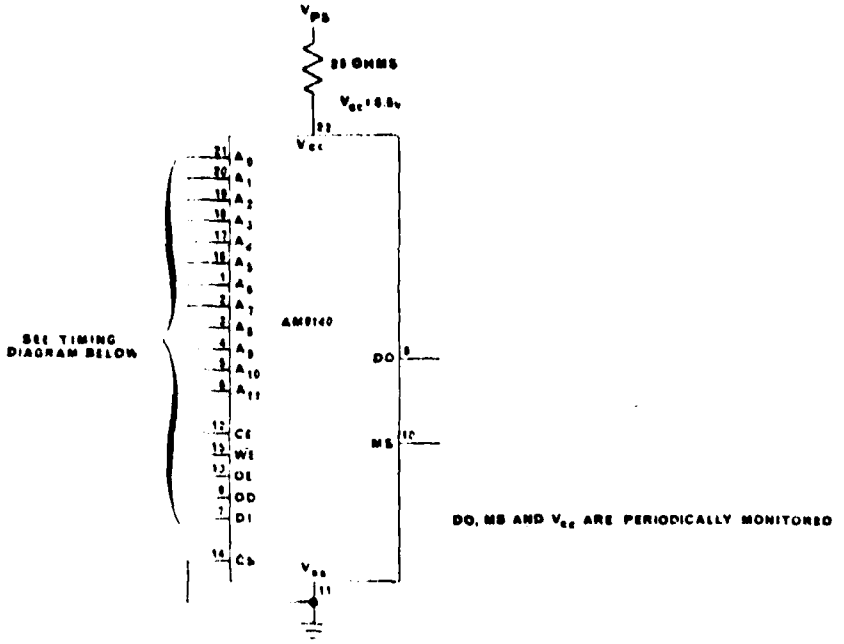


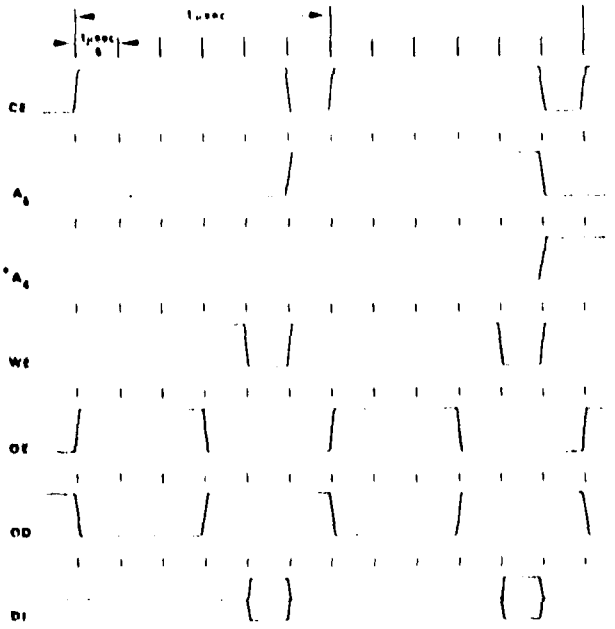
FIGURE 3-13. AMPLIFIED DYNAMIC EXCITATION WAVEFORMS

circuits performed satisfactorily. The R/M/W configuration was selected for step stress testing because it exercises all functions of the devices and best simulates device usage in system applications.

The AM9140 circuit and timing diagrams for the read/modify/write cycle are shown in Figure 4-15. The timing is similar to the AM9130. The two other dynamic modes included the continuous read and continuous write modes and are controlled by the $\overline{WE}$ signal. The AM9140 dynamic bias circuits were operated from 125°C to 230°C with a checkerboard pattern. The device supply voltage bias was varied from 5.5 Vdc to 7.0 Vdc. Figure 4-16 shows a typical plot of the I_{CC} current as a function of ambient temperature. The change in device current for the three bias configurations was negligible and the results were also comparable to the static bias evaluations. The AM9140 timing waveforms at elevated temperature for the R/M/W, continuous read and continuous write modes are shown in Figure 4-17. The Data Out signals were unstable at 225°C and the device was non functional at 230°C. All three dynamic bias circuits were acceptable for step-stress testing, however, the R/M/W mode bias circuit was selected because the device exercises all functions and best simulates usage conditions.

4.3.5 Step-Stress Tests - Step-stress tests were performed to validate the results of static and dynamic bias evaluations of the selected circuits and to obtain device failure data for determination of life test conditions. For each part type, step-stress testing was conducted on four devices with static excitation and four devices with dynamic excitation. The test devices were operated in the static and dynamic bias configurations at 125°C for 16 hours. During step-stress testing, the device current and output voltage were monitored prior to the start and end of each step. Following cool down with bias, the devices were electrically tested and surviving devices were returned to test. The test temperature was then increased by 25°C and the sequence was repeated. The maximum temperature for both step-stress tests was determined by the criteria established in Sections 4.3.1 and 4.3.3. The AM9130 and AM9140 were operated to a maximum temperature of 225°C. Summaries of the AM9130 and AM9140 static and dynamic step-stress tests are presented in Tables 4-10 and 4-11, respectively. The static step-stress tests showed that all device





*THE FREQUENCIES OF THE SUBSEQUENT ADDRESS LINE SIGNALS ARE HALF THE FREQUENCY OF THE PRECEDING ADDRESS LINE SIGNAL

ROW ADDRESS LSB = A_0; MSB = A_5

COLUMN ADDRESS LSB = A_6; MSB = A_{11}

FIGURE 4-15. AM9140 CANDIDATE DYNAMIC EXCITATION BIAS CIRCUIT

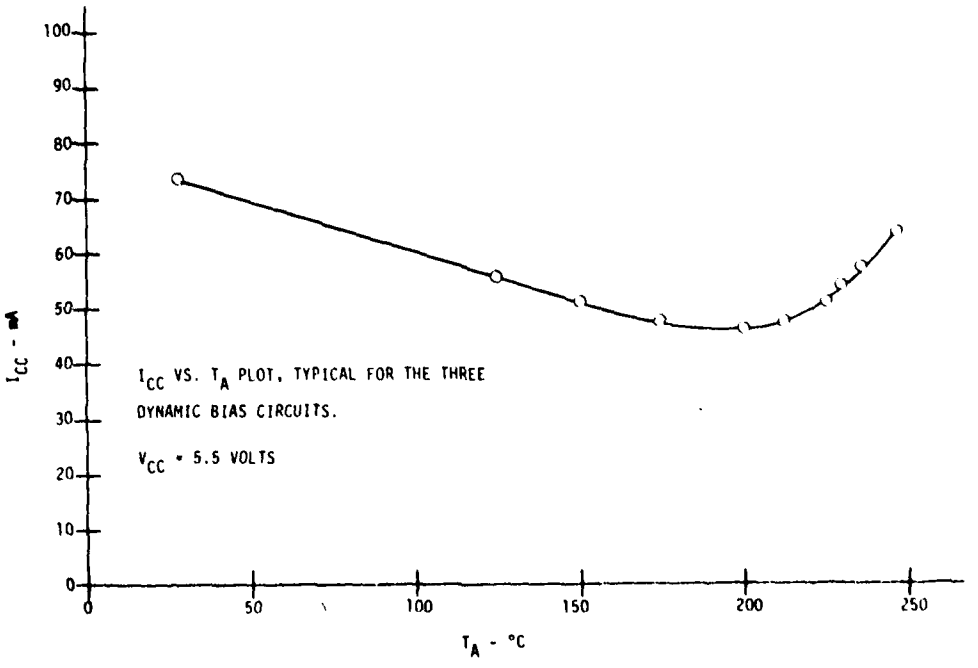
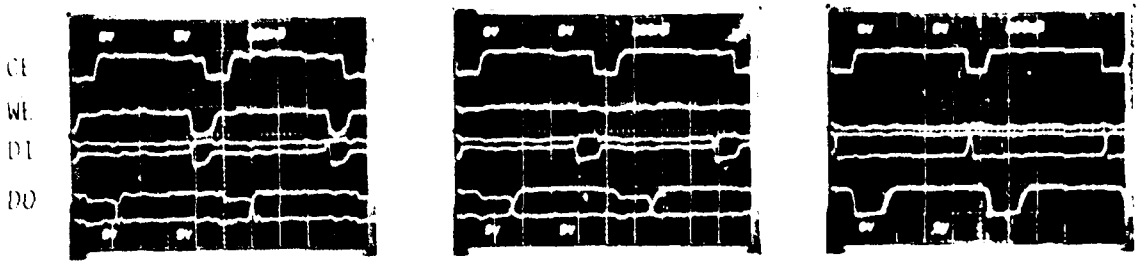


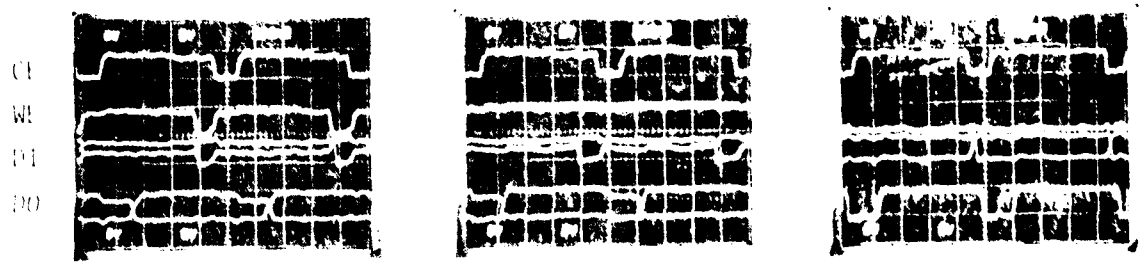
FIGURE 4-16. TYPICAL AM9140 DYNAMIC EXCITATION BIAS CIRCUIT EVALUATION



READ/MODIFY/WRITE
25°C

CONTINUOUS READ
25°C

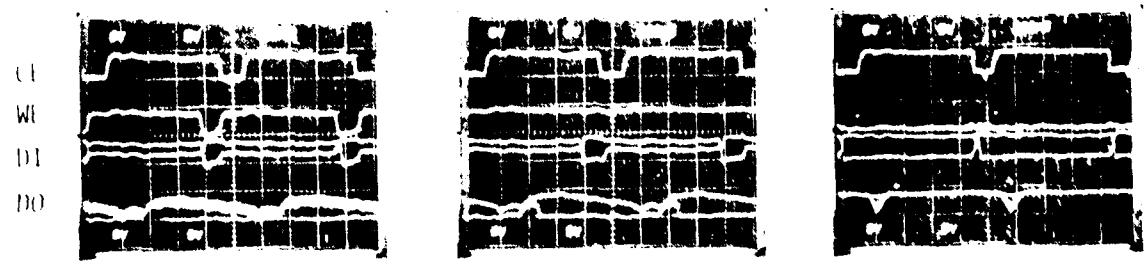
CONTINUOUS WRITE
25°C



READ/MODIFY/WRITE
200°C

CONTINUOUS READ
200°C

CONTINUOUS WRITE
200°C



READ/MODIFY/WRITE
230°C

CONTINUOUS READ
230°C

CONTINUOUS WRITE
230°C

FIGURE 3-3. APPLIED DYNAMIC EXCITATION WAVEFORMS

TABLE 4-10. STATIC EXCITATION STEP-STRESS TEST RESULTS

DEVICE TYPE	QTY	CUMULATIVE NUMBER OF FAILURES (STEP STRESS TEMPERATURE/HOURS OF STRESS)				
		125°C/16 HRS.	150°C/16 HRS.	175°C/16 HRS.	200°C/16 HRS.	[illegible]
AM9130	4	0	0	0	0	
AM9140	4	0	0	0	0	

TABLE 4-11. DYNAMIC EXCITATION STEP-STRESS TEST RESULTS

DEVICE TYPE	QTY	CUMULATIVE NUMBER OF FAILURES (STEP STRESS TEMPERATURE/HOURS OF STRESS)			
		125°C/16 HRS.	150°C/16 HRS.	175°C/16 HRS.	200°C/16 HRS.
AM9130	4	0	0	0	0
AM9140	4	0	0	0	0

outputs switched or were on the verge of switching at 225°C. The dynamic step-stress tests indicated that the devices were nonfunctional or unstable at 225°C. There were no step-stress test failures. A review of the dc and functional test data for both part types indicated negligible parameter degradation. The dc parameters which were expected to degrade were the supply currents and output voltages. The ac parameter used to observe device degradation was the chip enable access times.

4.3.6 Junction Temperature Determinations - After completion of the bias circuit evaluations and step-stress tests, the maximum junction temperatures during life testing were determined for both part types. The temperature dependence of a substrate diode forward voltage was used to determine the device junction temperatures. A MDAC-St. Louis thermal resistance tester was used to make the substrate diode forward voltage measurements. The tester is designed to establish the DUT life test conditions for 99.9% of the time and forward biases the substrate diode for 1 msec. The largest difference between the junction and ambient temperatures for both part types was 1.2°C.

4.3.7 Device Current Density - Current density determinations were required to assure that device currents were not excessive for life test conditions. At the maximum bias evaluation temperature the calculated current densities were 3.2×10^4 A/cm^2 for the AM9130 and 2.3×10^4 A/cm^2 for the AM9140. At room temperature, the device current density was 3.6×10^4 A/cm^2. Based on Black's data [3], no metal migration failures were expected in 4000 hours of life testing at 200°C for the AM9130 and AM9140.

4.3.8 Rationale for Life Test Conditions - The three static bias circuits for both device types evaluated were equally suitable for static bias life testing based on their performance at elevated temperatures. The read mode bias circuits, shown in Figures 4-7 and 4-9, with the outputs enabled, permit monitoring of the output pins for changes in internal device operating states and were selected for the life tests. The other two circuits do not permit monitoring of the output data for the address selected. Similarly, the three dynamic bias circuits for both device types were suitable for life testing.

The read/modify/write mode was selected for life testing because it exercises all functions of the devices and simulates usage conditions. A checkerboard data pattern was selected because it would stress half the cells in the high state and half in the low state with adjacent cells in complementary states. The same state is always stored in a given memory cell.

The temperatures selected for the operating life tests were 200°C and 175°C. During the static bias circuit evaluations and step-stress tests, the outputs of both device types were in a high state and stable at ambient temperatures up to 200°C. However, at 225°C the outputs were either switched or on the verge of switching to a low state. The supply currents were also increasing with temperature in this temperature range (200°C to 225°C) but were not excessive. Similarly, both device types remained functional in the dynamic bias evaluations and step-stress tests at 200°C but were unstable and erratic at 225°C. Therefore, the maximum life test temperature of 200°C was established for both static and dynamic excitations.

The supply voltage selected for both the static and dynamic life tests was 6.5 Vdc. During bias circuit evaluations both device types were operated at 7.0 Vdc in both the static and dynamic configurations at 200°C. During the subsequent life tests, with the individual DUT V_{CC} voltage variations, an average of 6.5 Vdc on the devices ensured that no devices would exceed 7.0 Vdc, the absolute maximum device rating.

5.0 RESULTS OF PHASE III STRESS TESTS

The Phase III stress tests included a matrix of temperature cycling, high temperature operating (static and dynamic excitation) and high temperature non-operating storage life tests. The interim electrical measurement schedules are shown in the previous Tables 2-1 through 2-3.

5.1 TEMPERATURE CYCLING TEST RESULTS

The temperature cycling tests were performed to the requirements of MIL-STD-883, Method 1010.7, Condition C (-65°C to +150°C) for 200 cycles. The temperature cycling tests for both device types were performed in a non-operating mode to reveal potential package and bond weakness as well as corrosion mechanisms due to moisture in the device package. A summary of the temperature cycling test results are presented in Table 5-1. There were no temperature cycling test failures for the AM9130 and the AM9140. Following temperature cycling tests all devices were subjected to an external visual examination and hermeticity tests. The results of these inspections and tests are summarized in Table 5-2. A dark stain was observed on the inside of the leads at the braze material as shown in Figure 5-1. SEM examination of the stain site disclosed that the gold plating had been nicked by a sharp edge as shown in Figure 5-2. Energy dispersive x-ray analysis of the dark material surrounding the nick disclosed that it was composed of a) copper, silver, and molybdenum (lead braze), b) nickel and cobalt (lead base metals), c) gold (plating), d) aluminum (background), and e) chlorine (a contaminant) as shown in Figure 5-3. This indicated that the material was scrapings or debris from the nick. The source of the chlorine is unknown, but probably came from a contaminant chemical residue. Since chlorine is corrosive it probably caused the scrapings to decompose giving it the blackened appearance. Since the chlorine could corrode the lead base metal exposed by the nicks a potential problem exists. However, no deterioration of the leads occurred during the temperature cycling tests.

TABLE 5-1. SUMMARY OF TEMPERATURE CYCLING TEST RESULTS

PART TYPE	QTY	CUMULATIVE NUMBER OF FAILURES AT CYCLES OF TEST					
		0	10	50	100	150	200
AM9130	10	0	0	0	0	0	0
AM9140	10	0	0	0	0	0	0

TABLE 5-2. POST TEMPERATURE CYCLING INSPECTION AND TESTS

PART TYPE	QTY	EXTERNAL VISUAL				HERMETICITY TESTS			
		Marking		Case Lead Seals [1]		FINE LEAK		GROSS LEAK	
		Pass	Fail	Pass	Fail	Pass	Fail	Pass	Fail
AM9130	10	10	0	10	0	10	0	10	0
AM9140	10	10	0	10	0	10	0	10	0

NOTE:

[1] BLACK COMPOUND AT BRAZE OF PACKAGE LEADS.

40X

FIGURE 5-1. OPTICAL PHOTOGRAPH OF THE STAIN ON A PACKAGE LEAD

100X

FIGURE 5-2. SEM PHOTOGRAPH OF THE PACKAGE LEAD SHOWING THE NICK (ARROW)

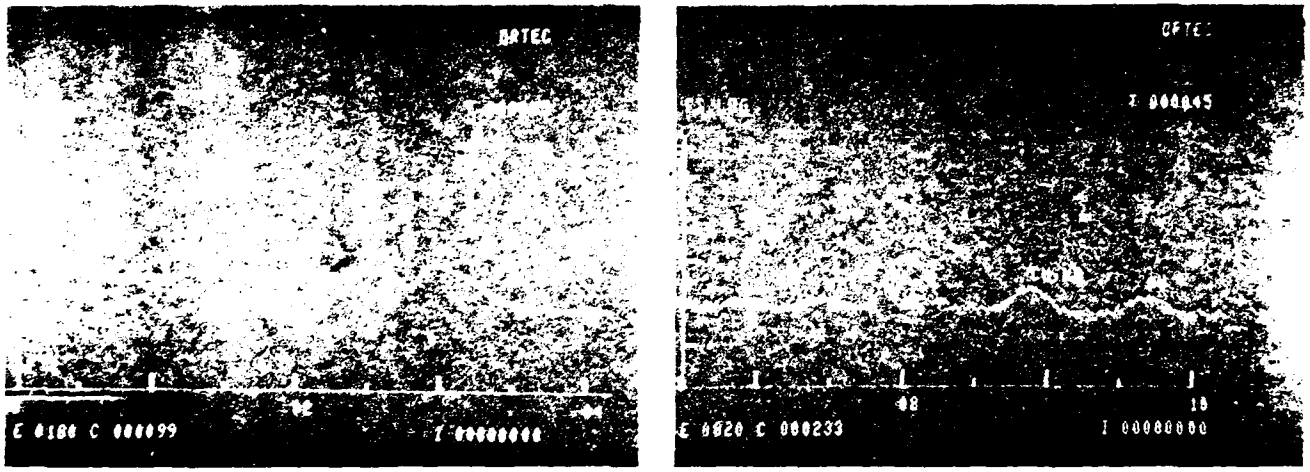


FIGURE 5-3. ENERGY EMISSION ANALYSIS OF THE MATERIAL AROUND THE NICK

5.2 OPERATING AND NON-OPERATING LIFE TEST RESULTS

The operating life tests were performed with both static and dynamic excitation to compare their relative effectiveness for accelerating LSI memories failures. The AM9130 and AM9140 life tests with both static and dynamic excitations were conducted with 15 devices in each test cell at: a) 200°C for 4000 hours, and b) 175°C for 4000 hours. A summary of the test devices' life test conditions is presented in Table 5-3.

The AM9130 life test results for cumulative 25°C failures are shown in Table 5-4. Table 5-5 presents the number of -55°C/125°C failures at the electrical measurement points. The total percentage of AM9130 life test (operating and non-operating) failures for all three temperatures was approximately 11%. Table 5-6 shows the AM9140 life test results with cumulative failures at 25°C. Table 5-7 shows the number of AM9140 -55°C/125°C failures at each measurement point. The total percentage of life test (operating and non-operating) failures for all three temperatures was approximately 14 .

The non-operating or storage life tests were performed to evaluate the test devices' long term process stability and mechanical reliability. Although a 200°C storage life test would permit a direct comparison between the non-operating storage and operating life tests, it was anticipated based on previous test experience that few failures would occur in this environment. Since the maximum acceleration will occur at the maximum temperature permissible, the non-operating life tests were conducted at 275°C. Tables 5-4 and 5-6 present a summary of the AM9130 and AM9140 life test results. There were no storage life test failures.

TABLE 5-3. SUMMARY OF LIFE TEST CONDITIONS

PART TYPE	TEST CELL	AMBIENT TEMPERATURE T_A (°C)	DEVICE VOLTAGE V_{CC} (Vdc)	DEVICE CURRENT I_{CC} (mAdc)	POWER DISSIPATION P_D (mW)	JUNCTION TEMPERATURE T_J (°C)
AM9130	STATIC	200	6.48	58.00	375.84	211
	STATIC	175	6.56	55.00	360.80	186
	DYNAMIC	200	6.51	59.68	388.52	212
	DYNAMIC	175	6.51	59.60	388.00	187
AM9140	STATIC	200	6.49	49.50	321.26	210
	STATIC	175	6.50	51.00	331.50	185
	DYNAMIC	200	6.49	57.16	370.97	211
	DYNAMIC	175	6.51	56.48	367.68	186

TABLE 5-4. SUMMARY OF AM9130 LIFE TEST RESULTS FOR 25°C FAILURES

PART TYPE	TEST EXCITATION	TEMP °C	QTY	CUMULATIVE NUMBER OF FAILURES AT HOURS OF TEST [1]						
				0	168	504	1000	1500	2000	4000
AM9130	STATIC	200	15	0	0	0	0	0	0	0
	STATIC	175	15	0	0	0	0	0	0	0
	DYNAMIC	200	15	0	0	0	0	0	1	1
	DYNAMIC	175	15	0	0	0	0	0	0	0
	STORAGE	275	10	0	0	0	0	0	0	-

[1] ALL FAILED DEVICES REMOVED FROM TEST FOR FAILURE ANALYSIS.

TABLE 5-5. SUMMARY OF AM9130 LIFE TEST RESULTS FOR -55°C/125°C FAILURES

PART TYPE	TEST EXCITATION	TEMP °C	QTY	NUMBER OF FAILURES AT HOURS OF TEST (1)						
				0	168	504	1000	1500	2000	4000
AM9130	STATIC	200	15	0	-	6	1 (2)	-	0	0
	STATIC	175	15	0	-	1	0	-	0	0
	DYNAMIC	200	15	0	-	0	0	-	1 (3)	0
	DYNAMIC	175	15	0	-	0	0	-	0	0
	STORAGE	275	10	0	-	-	-	-	0	-

(1) FAILED DEVICES LEFT ON LIFE TEST.

(2) DEVICE ALSO FAILED AT PREVIOUS MEASUREMENT TIME.

(3) DEVICE ALSO FAILED 25°C ELECTRICAL MEASUREMENTS AND WAS REMOVED FROM LIFE TEST.

TABLE 5-6. SUMMARY OF AM9140 LIFE TEST RESULTS FOR 25°C FAILURES

PART TYPE	TEST EXCITATION	TEMP °C	QTY	CUMULATIVE NUMBER OF FAILURES AT HOURS OF TEST						
				0	168	504	1000	1500	2000	4000
AM9140	STATIC	200	15	0	1	1	1	1	1	2
	STATIC	175	15	0	0	1	1	1	1	1
	DYNAMIC	200	15	0	0	0	0	0	0	1
	DYNAMIC	175	15	0	0	0	0	0	0	0
	STORAGE	275	10	0	0	0	0	0	0	-

⚠ ALL FAILED DEVICES REMOVED FROM TEST FOR FAILURE ANALYSIS.

TABLE 5-7. SUMMARY OF AM9140 LIFE TEST RESULTS FOR -55°C/125°C FAILURES

PART TYPE	TEST EXCITATION	TEMP °C	QTY	NUMBER OF FAILURES AT HOURS OF TEST (1)						
				0	168	504	1000	1500	2000	4000
AM9140	STATIC	200	15	0	-	1	1 (2)	-	0	3 (2) (3)
	STATIC	175	15	0	-	1 (3)	0	-	0	3
	DYNAMIC	200	15	0	-	0	0	-	0	2 (3)
	DYNAMIC	175	15	0	-	0	0	-	0	0
	STORAGE	275	10	0	-	-	-	-	0	-

(1) FAILED DEVICES LEFT ON LIFE TEST.

(2) DEVICE ALSO FAILED AT PREVIOUS MEASUREMENT TIME.

(3) DEVICE ALSO FAILED 25°C ELECTRICAL MEASUREMENTS AND WAS REMOVED FROM LIFE TEST.

6.0 FAILURE ANALYSIS

All devices that failed high temperature stress (operating) tests were subjected to failure analysis. The failed devices were analyzed to determine failure mode, failure mechanism and probable cause of failure. Table 6-1 presents a summary of the failure analysis results for the AM9130 and AM9140 for 25°C, 125°C and -55°C electrical measurement failures. Detailed discussions of the failure analysis results are contained in Appendix D.

TABLE 6-1. AM9130 AND AM9140 FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS B. ANALYSIS FINDINGS	QUANTITY OF FAILURES AND TIME OF FAILURE						DEVICE DESIGNATOR
	AM9130			AM9140			
	STATIC LIFE		DYNAMIC LIFE	STATIC LIFE		DYNAMIC LIFE	
	200°C	175°C	200°C	200°C	175°C	200°C	
A. I_{IH} AT PINS 3 AND 9 B. DEGRADED INPUT PROTECTION NETWORK DUE TO SURFACE INSTABILITY CAUSED BY STATIC DISCHARGE				1@504 HRS			D2.1
A. V_{OH}[32], V_{OL}[34], $t_{a(CE)}$ B. SURFACE INSTABILITY			1@2000 HRS				D2.2
A. $t_{a(CE)}$ B. SURFACE INSTABILITY				1 @168 HRS 1[4]/@504 HRS 1[7]/@4000 HRS 1[4]/@4000 HRS	1[3]/@4000 HRS 2[4]/@4000 HRS	1[3]/@4000 HRS	D2.3
A. $t_{a(CE)}$ B. NOT DETERMINED						1[2]/@4000 HRS	D2.4
A. I_{CC}[30] B. NOT ANALYZED (I_{CC} MARGINAL AT START OF LIFE TEST)	6[5]/@504 HRS	1[5]/@504 HRS					
TOTAL NUMBER OF FAILED PARTS	6	1	1	4	4	2	

NOTES:

1. [illegible]
2. [illegible]
3. [illegible]
4. [illegible]
5. [illegible]

7.0 DATA EVALUATIONS AND CORRELATIONS

7.1 AM9130 DATA ANALYSIS

There were insufficient test failures to allow failure distribution analysis. Table 5-4 and Table 5-5 show that there were eight device failures. Seven failures were attributed to marginal I_{CC30} currents prior to the start of life tests. These devices failed I_{CC30} measurements at -55°C. Since the failure data is inadequate for failure distribution analysis, the dc and functional data was investigated for trends that would allow extrapolation of times to failure. The stress test data summaries which included parameter mean and standard deviations tabulations for 0 hour and 4000 hour data at 25°C and 125°C are contained in Appendix C. This includes test data for input/output leakages, supply current, output voltages and access times. With the exception of the supply current, I_{CC}, all device parameters have worst case values at the maximum measurement temperature (125°C). The worst case supply current occurs at -55°C. The input/output leakages and supply current worst case values are at maximum V_{CC} voltage (5.5 Vdc) but worst case output voltage and access times occur at the minimum V_{CC} voltage (4.5 Vdc). All test data was reviewed and the device parameters exhibited excellent stabilities during the 4000 hour life test. No trend was observed and an increase of 6 mAdc for supply current was noted at the 504 hour electrical measurement point. This was attributed to a recalibration of the automatic test system and was verified by an identical shift in data for the control sample. The shift in dc parametric data for all AM9130 4000 hour life tests was negligible. It was expected that the chip enable access time would be the indicator of device aging. Therefore, the chip enable access times for the 200°C and 175°C life test cells were plotted as a function of the electrical measurement time and are shown in Figures 7-1 and 7-2. This worst case values of access time were the computed mean plus 3 sigma values for a MARCH R/M/W pattern at V_{CC} = 4.5 Vdc and 125°C. The graphs indicated negligible access time degradation. With no data trend the interpolated time to failure ($t_{a(CE)}$ > 500 nS) could not be estimated. In addition, the static and dynamic excitations and life test temperature and overvoltage stress conditions had a negligible effect on device operation. The data did not allow extrapolation of times to failures for any AM9130 static and

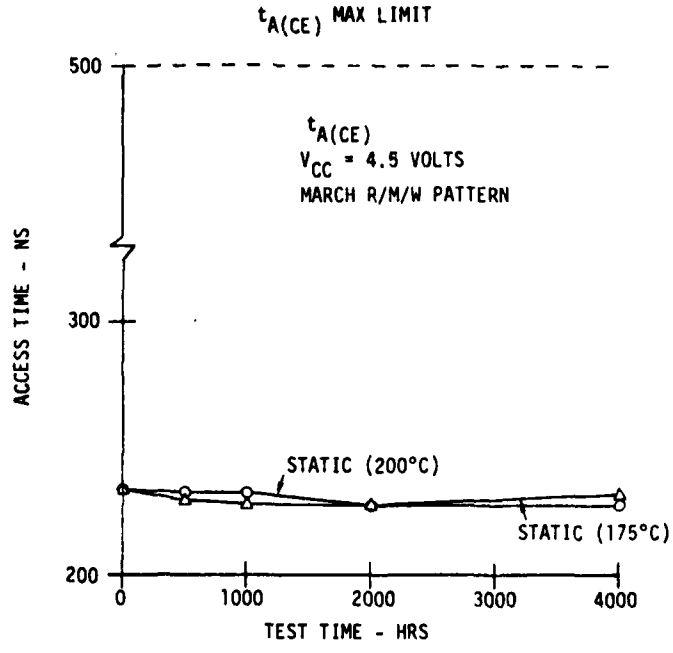


FIGURE 7-1. AM9130 WORST CASE CHIP ENABLE ACCESS TIME VERSUS TEST TIME FOR STATIC EXCITATION TEST CELL

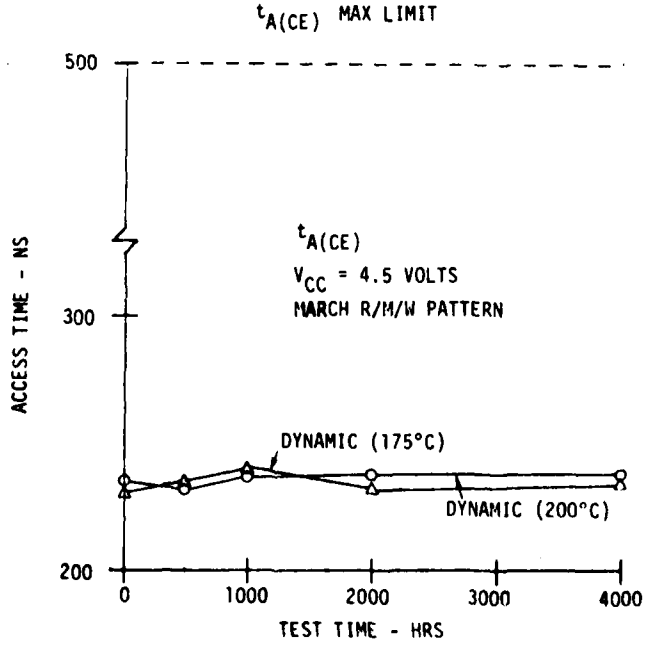


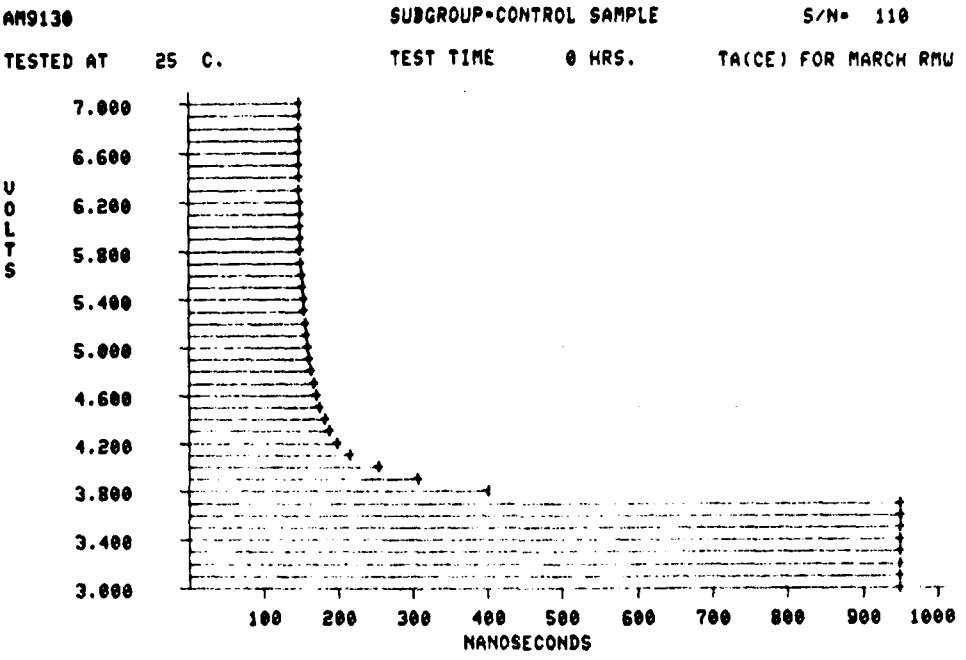
FIGURE 7-2. AM9130 WORST CASE CHIP ENABLE ACCESS TIME VERSUS TEST TIME FOR DYNAMIC EXCITATION TEST CELL

dynamic test cells. In order to investigate device access time degradation as a function of V_{CC} voltage, one of the devices for which an initial shmoo was generated was placed on dynamic life test for 4000 hours. Shmoo plots, as shown in Figure 7-3, for both 0 hours and 4000 hours at 25°C indicated minimal degradation as a function of V_{CC} voltage. Considering the severity of the stress test conditions the lack of test induced failures or parameter degradation trends indicates the device should have a high reliability potential.

The AM9130 life test data for functional tests was analyzed to determine the relative effectiveness of the GALDIA (N^2), MARCH (N), and CHECKERBOARD (N) patterns. The criteria used to judge pattern effectiveness was the ability of the pattern to detect life test failures. A summary of the percentage of pre-stress test and life test functional failures detected by each pattern is shown in Table 7-1. The N pattern was equally effective in detecting life test failures as the N^2 pattern. However, with only one life test timing related failure these results are not considered conclusive. During initial electrical testing, the MARCH pattern was most effective in detecting failed devices.

7.2 AM9140 DATA ANALYSIS

There were also insufficient test failures to allow failure distribution analysis of the AM9140. There were eight static excitation and two dynamic excitation life test failures. One static excitation life test failure was due to a degraded input caused by static discharge or an electrical transient. The life test data was then analyzed to determine whether trends existed that would allow extrapolation of times to failure. Appendix C includes the stress tests data summaries of parameter mean and standard deviation tabulations for 0 hour and 4000 hour data. A review of all the test data showed that the AM9140 exhibited excellent parameter stabilities during the 4000 hour life test. The I_{CC} anomaly of the AM9130 due to an automated test system recalibration was also noted with the AM9140. In addition, the AM9140 dc tests showed negligible parameter shifts with no discernible trends. The functional test data was reviewed and the chip enable access times were plotted as a function of the electrical measurement time. Figures 7-4 and 7-5 show the worst case test cells.



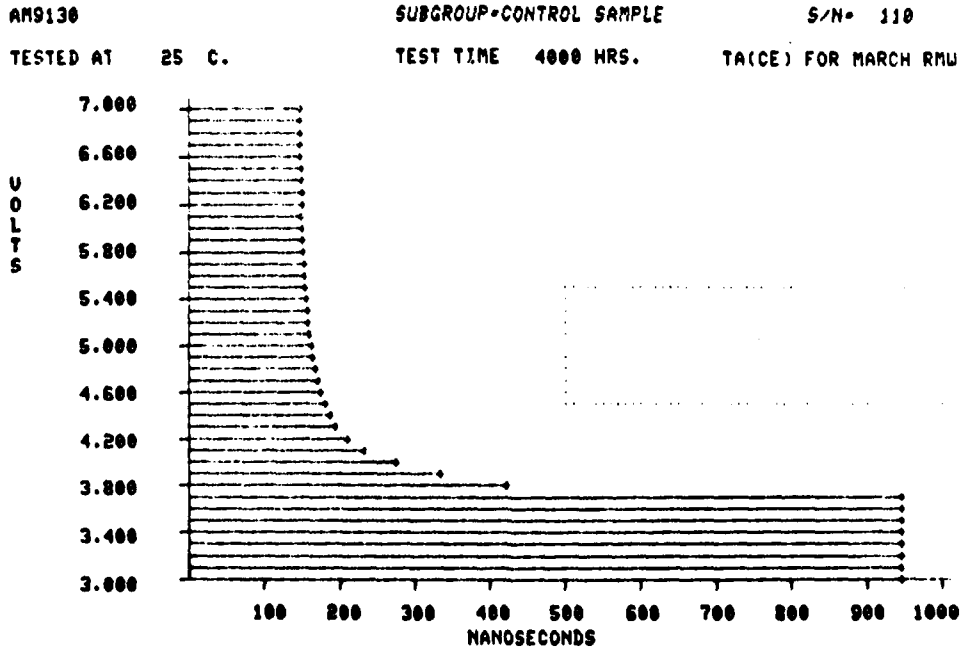


FIGURE 7-3. AM9130 CHIP ENABLE ACCESS TIME SHMOO PLOTS - 0 HOUR AND 4000 HOUR DYNAMIC EXCITATION LIFE TEST AT 200°C

TABLE 7-1. PATTERN EFFECTIVENESS SUMMARY

PRE-STRESS TEST FAILURES

PART TYPE	TOTAL NUMBER OF FAILED DEVICES	PERCENT OF FAILED DEVICES DETECTED BY PATTERN			
		N^2	N		
		GALDIA	MARCH	CHECKERBOARD STOP	CHECKERBOARD POWERDOWN
AM9130	9	56	100	67	67
AM9140	3	67	100	67	67

LIFE TEST FAILURES

PART TYPE	TOTAL NUMBER OF FAILED DEVICES	PERCENT OF FAILED DEVICES DETECTED BY PATTERN			
		N^2	N		
		GALDIA	MARCH	CHECKERBOARD STOP	CHECKERBOARD POWERDOWN
AM9130	1	100	100	100	100
AM9140	10	90	90	10	60

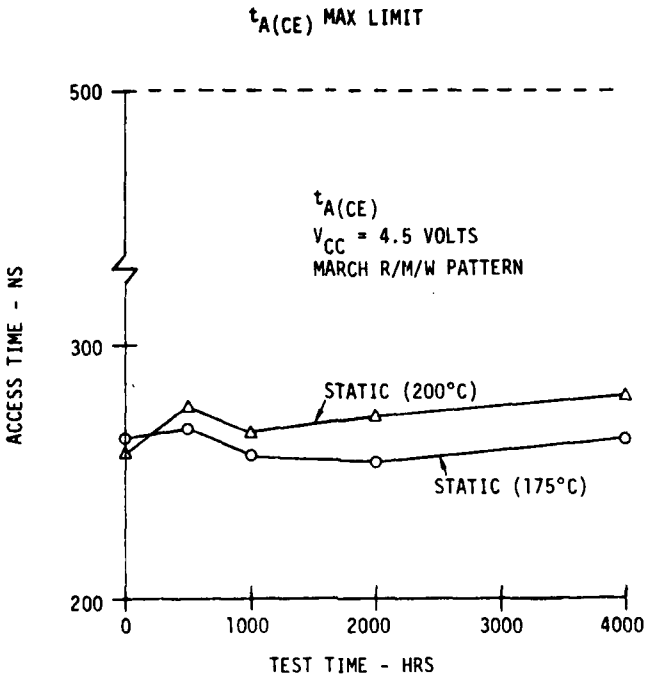


FIGURE 7-4. AM9140 WORST CASE CHIP ENABLE ACCESS TIME VERSUS TEST TIME FOR STATIC EXCITATION TEST CELL

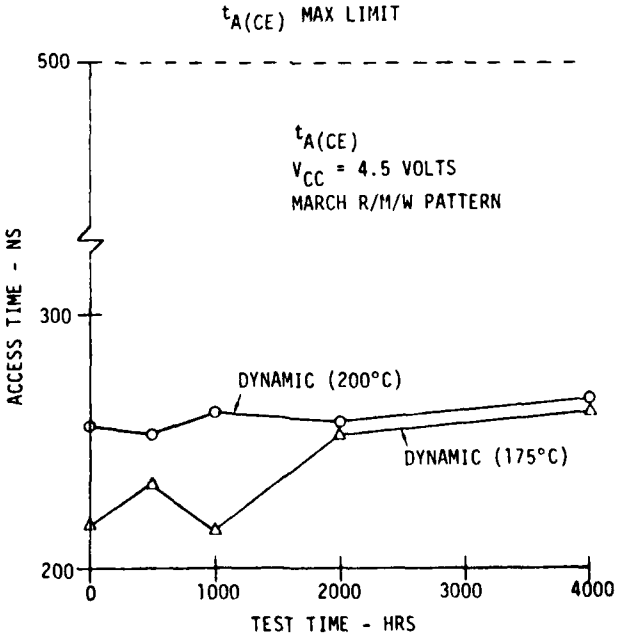
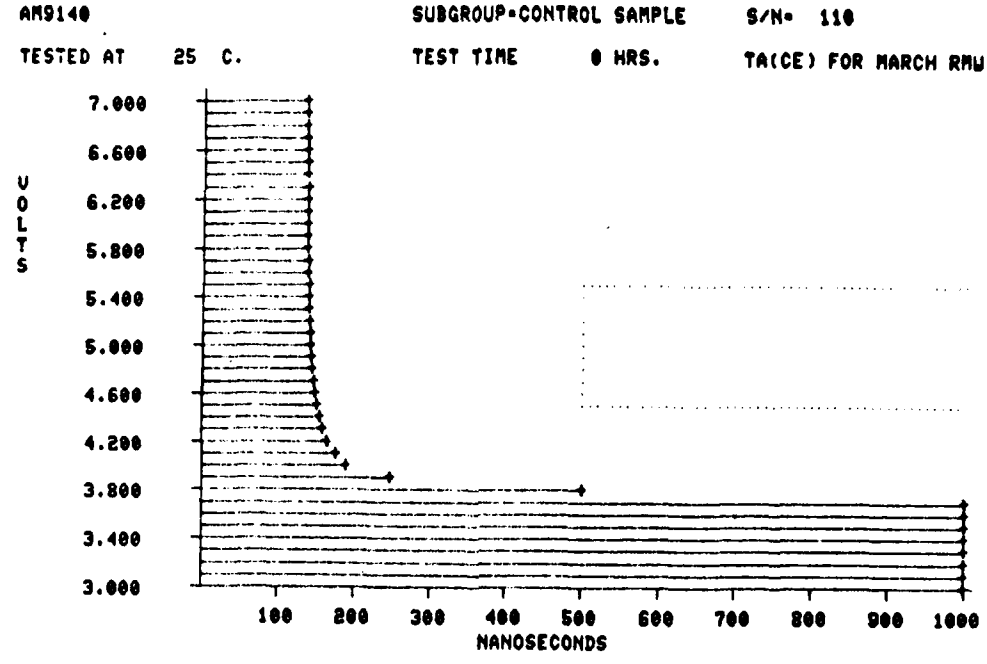


FIGURE 7-5. AM9140 WORST CASE CHIP ENABLE ACCESS TIME VERSUS TEST TIME FOR DYNAMIC EXCITATION TEST CELL

The worst case values are the computed mean plus 3 sigma values for a MARCH R/M/W pattern at V_{CC} = 4.5 Vdc and 125°C. The static test cell data showed limited access time change with an interpolated time to failure ($t_{a(CE)}$ 500 nS) of approximately 42,000 hours at 200°C for the 200°C test cell and 57,000 hours at 175°C for the 175°C test cell based on the 2000 hour and 4000 hour measurement points. In addition, a single device which was initially shmoo plotted was placed on dynamic life test for 4000 hours. Shmoo plots, as shown in Figure 7-6, for both 0 hour and 4000 hours at 25°C indicated minimal degradation as a function of V_{CC} voltage. Considering the severity of the stress test conditions the lack of test induced failures indicates a high reliability potential.

Table 7-1 presents a summary of the percentage of pre-stress test and life test functional failures detected by the GALDIA (N^2), MARCH (N), and CHECKERBOARD (N) patterns. The MARCH pattern was as effective in detecting functional life test failures as the GALDIA pattern. Although no pattern detected 100 of the life test failures, these results are misleading since the power down test was not performed with the GALDIA and MARCH patterns. The results of this test program and the Reliability Evaluation and Electrical Characterization of Memories program both indicate that the N^2 pattern is not necessary in the MIL-M-38510/237 Group A electrical tests. As was the case with the AM9130 devices, the MARCH pattern was most effective in detecting failures during initial electrical testing.



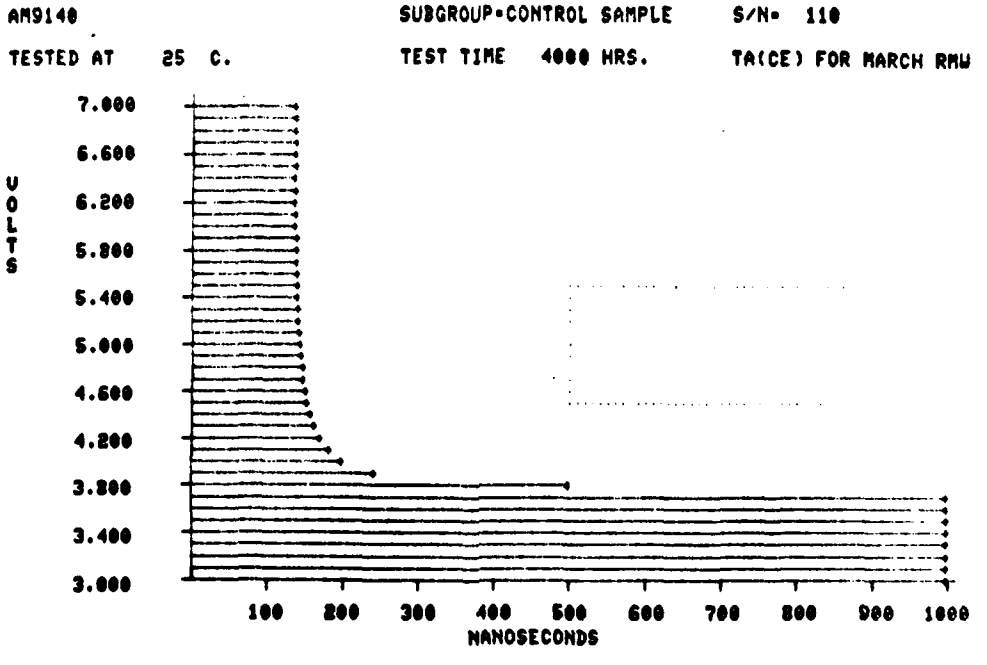


FIGURE 7-6. AM9140 CHIP ENABLE ACCESS TIME SHMOO PLOTS - 0 HOUR AND 4000 HRS. DYNAMIC EXCITATION LIFE TEST AT 200°C

8.0 CONCLUSIONS AND RECOMMENDATIONS

This reliability program to evaluate the 4K static RAMs procured to the MIL-M-38510/237 specification included both electrical and environmental stresses. These devices were evaluated as a function of voltage, temperature and static and dynamic excitations. Although the AM9130 and AM9140 indicated a high reliability potential, there were insufficient life test failures (18 failures out of 120 devices on operating life tests) to estimate device failure rates based on the Arrhenius Reaction Rate Model. Previous LSI memories life tests (1K NMOS static RAMs) conducted at MDAC-St. Louis were operated at higher temperatures ($\geq$ 250°C) and accelerated a larger number of failures. The small number of AM9130 and AM9140 failures may be due to the reduced life test maximum temperature of 200°C and improved manufacturing process since the 1K NMOS static RAMs were introduced. In addition, the elimination of pattern related design deficiencies may have contributed to the increased reliability of these 4K static RAMs. It is believed that high reliability military systems can be designed with devices procurred to the MIL-M-38510/237 specification.

Static excitation bias circuits were expected to be more effective than dynamic circuits in accelerating charge migration failure mechanisms, while dynamic excitation bias circuits were expected to be more effective in accelerating mechanical mechanisms such as dielectric breakdown in the memory cell matrix. The failure analysis results show predominantly surface instability (bake recoverable) failures for both the static and dynamic test cells. Based on the limited test cell size and small number of failures, these results are not conclusive. The controversy whether a static or dynamic excitation circuit is more effective for burn-in/life conditions remains unresolved. Therefore, it is recommended that more extensive evaluations be performed for static excitation versus dynamic excitation of LSI memories. These should include larger test cell sizes and multiple wafer lots.

The MIL-M-38510/237 specification requires a dynamic burn-in/life circuit that operates the test devices in a write only configuration at less than rated cycle times. During reliability characterizations a similar circuit (continuous write circuit at rated cycle time and maximum rated voltage)

produced satisfactory results. However, it is believed that a dynamic bias circuit for burn-in/life tests should operate at rated cycle times in a configuration that approximates device usage in system applications, e.g., read/modify/write cycle.

The supply current (I_{CC27}) and chip enable access time ($t_{a(CE)}$) test limits could be tightened based on the electrical characterization and life test parameters degradation results. In addition, the GALDIA (N^2) pattern may be deleted from the military specification without compromising device reliability. Both changes were previously recommended by MDAC-St. Louis for the Reliability Evaluation and Electrical Characterization of Memories Program.

9.0 REFERENCES

[1] A. T. Sasaki, "Reliability Evaluation and Electrical Characterization of Memories," Final Technical Report, RADC Contract F30602-77-C-0003, October 1978.

[2] B. Euzent, "Hot Electron Injection Efficiency in IGFET Structures," 15th Annual Proceedings, Reliability Physics Symposium, April 1977.

[3] J. R Black, "Electromigration - A Brief Summary and Some Recent Results," IEEE Transactions on Electron Device, April 1969.

9.1 REFERENCED MILITARY DOCUMENTS

MIL-M-38510, Military Specification; Microcircuits, General Specification for.

MIL-M-38510/237, Military Specification; Microcircuits, Digital, MOS, 4096 Bit Static Random Access Memory (RAM), Monolithic, Silicon.

MIL-STD-883, Military Standard; Test Methods and Procedures for Microelectronics.

APPENDIX A

PHYSICAL CHARACTERIZATIONS

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1.0 INTRODUCTION

The physical characteristics evaluation was performed to document the physical and electrical structures of 4K static RAMs procured to the initial draft of the MIL-M-38510/237 specification.

The test devices selected for examination were 4K static RAMs manufactured by Advanced Micro Devices in 1K x 4 and 4K x 1 organizations. Two samples of each organization, procured to MIL-M-38510/23704 and 23712 with the manufacturer equivalent MIL-STD-883 Class B screening and designated as AM9130 ADMB and AM9140 ADMB, were used in this study. The devices examined in the study are presented in Table A1.

TABLE A1. TEST DEVICES EXAMINED

MIL-M-38510 REFERENCE	MANUFACTURER & PART NUMBER	PART DESCRIPTION	DATE CODE	ASSIGNED SERIAL NUMBER
/23704 BWC	ADVANCED MICRO DEVICES AM9130 ADM-B	1024 X 1 STATIC R/W RAM	7803 GP	6 7
/23712 BWC	ADVANCED MICRO DEVICES AM9140 ADM-B	4096 X 1 STATIC R/W RAM	7803 HP	6 7

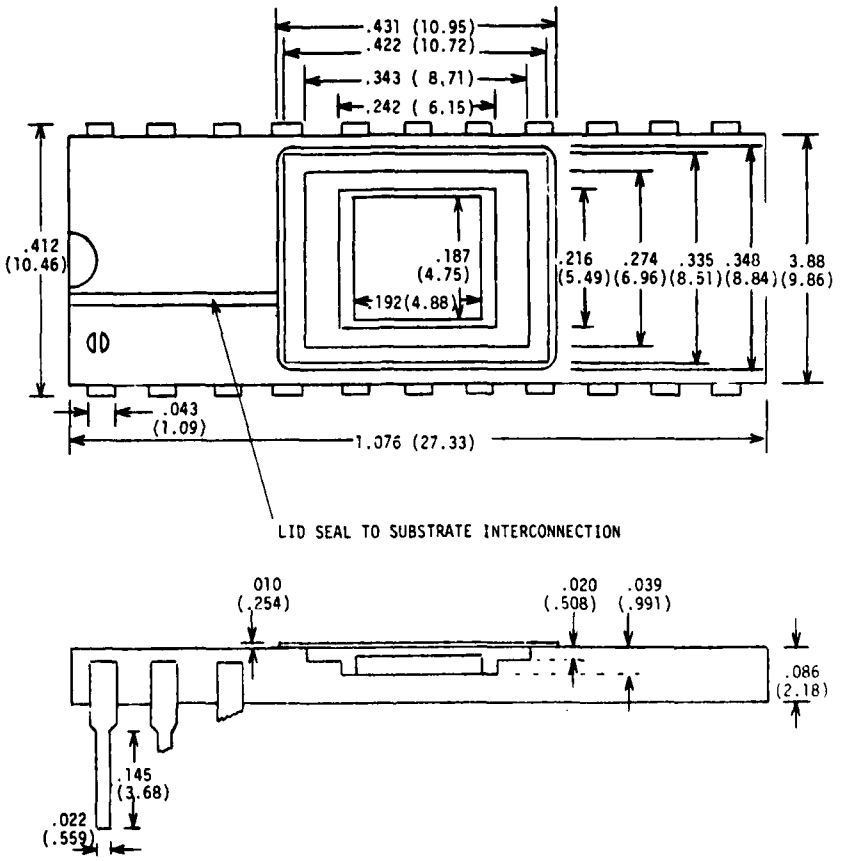
2.0 PHYSICAL CHARACTERIZATION

2.1 PACKAGE ANALYSIS

Both part types were constructed in identical 22-pin side brazed packages. This package with its dimensions is illustrated in Figure A1. The packages were constructed of three layers of black cofired ceramic having a minimum of ninety percent (90%) alumina content. Several superficial chips were noted on all four packages, particularly at the corners. The chips probably resulted from improper handling techniques during processing. Figure A2 presents package photographs of the parts examined. The external leads were gold plate over nickel and the lead frame gold plate only, both on Kovar type metal. The package lid was gold plate on Kovar type metal sealed with solder of eighty percent (80%) gold and twenty percent (20%) tin. The information on the material composition of the package, leads and lid seal was provided by the manufacturer. The lid seal appeared uniform and hermeticity tests confirmed the integrity of the seal. The average mass of the four parts examined was 2.437 grams.

2.2 DIE ANALYSIS

Both the AM9130 and AM9140 utilized the same diffusion/oxide masks. Different metallization masks were used to achieve the 1K x 4 and 4K x 1 memory organizations. The die of both part types was mechanically scribed using a diamond saw technique. The die size from scribe line to scribe line measured 187 x 192 mils (4.75 x 4.88 mm), and the die was bonded in a cavity with approximate volume of .00212 cu in (34.72 cu mm). The attachment of the die to the package is through a ninety-eight percent (98%) gold and two percent (2%) silicon eutectic. This was confirmed by an energy dispersive x-ray analysis of the eutectic region. The energy emission analysis, shown in Figure A3, indicates the presence of silicon and gold in the eutectic and aluminum due to background scatter from the leads. Radiographic examinations disclosed an uneven eutectic coverage beneath the die of all the devices examined as illustrated in Figure A4. This uneven coverage was more pronounced in the AM9130 with an approximate coverage of eighty-five percent (85%), as shown in Figure A5.

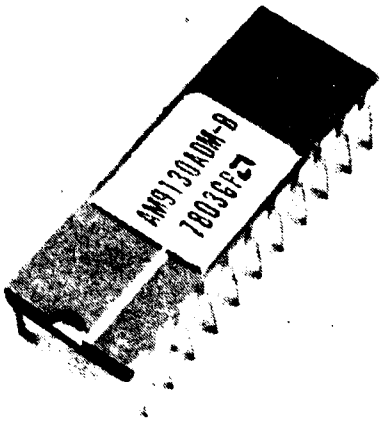


NOTES:

1. ALL DIMENSIONS ARE SPECIFIED IN INCHES (MILLIMETERS).
2. ALL MEASUREMENTS ± .004 (.102).

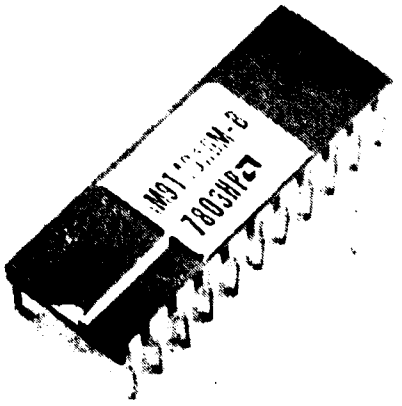
FIGURE A1. 22 PIN SIDE BRAZED PACKAGE

AM9130 S/N 6



AM9130 S/N 7

AM9140 S/N 6



AM9140 S/N 7

FIGURE A2. PACKAGE PHOTOGRAPHS

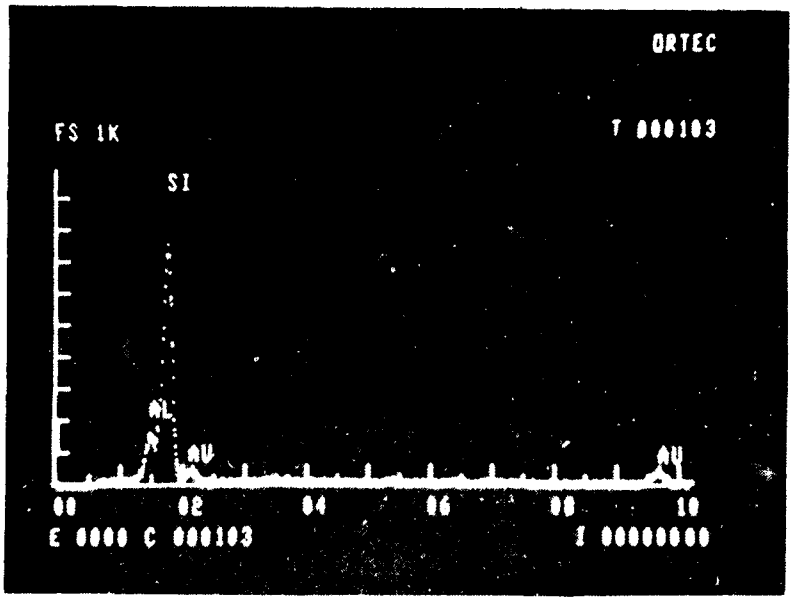


FIGURE A3. ENERGY EMISSION ANALYSIS OF DIE BOND MATERIAL

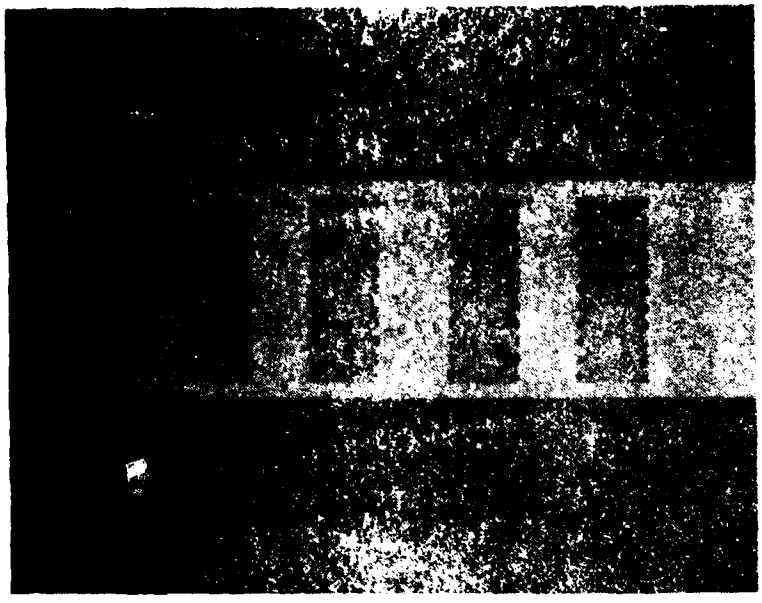


FIGURE A4. X-RAY PHOTOGRAPH OF DEVICES EXAMINED

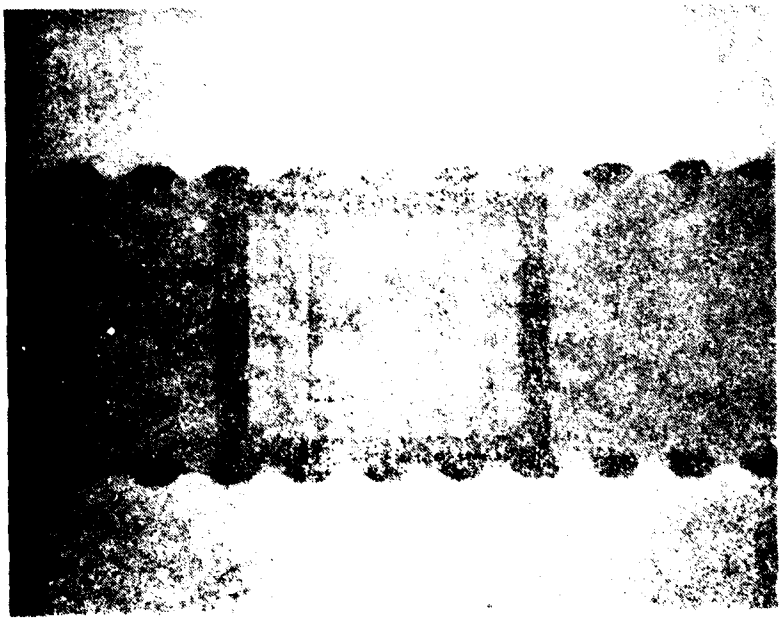


FIGURE A5. X-RAY PHOTOGRAPH OF [illegible] VOIDS [illegible]

2.3 WIRE INTERCONNECTS

Aluminum wires of 1.1 mil (.128 mm) diameter were ultrasonically bonded at the bond pads on the die and the lead frame. Figures A6 and A7 present SEM photographs of an aluminum-aluminum bond at a pad and an aluminum-gold bond at the lead frame, respectively. Probe marks were noted on some pads, as presented in Figures A8 and A9. The manufacturer related that these probe marks should be present on all pads with the exception of the Memory Status pad. The probe marks occured during wafer level die testing. Since probe marks were not visible in most cases, the wire bonds were probably made at the probe sites. To determine if bonding over probe mark sites resulted in inadequate bond strength, a bond pull test was performed on one device of each type. Table A2 presents a summary of this test. No bond failed due to the lifting of a lead from the pad, thus, verifying the integrity of the bonds. In addition, all bonds passed the MIL-STD-883B, Method 2011.2 bond pull requirement (1.7 gm) for a 1.1 mil aluminum wire. The placement of the bonds on the die pads satisfied the requirements of MIL-STD-883B in all cases. However, several bonds were located near or over the pad edge, as shown in Figure A10.

2.4 SUMMARY

A summary of the physical characteristics of the devices studied is presented in Table A3. Presented in Table A4 are the results of a gas mass spectrometer (GMS) analysis performed by RADC.

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RELIABILITY CHARACTERIZATION OF LSI MEMORIES.(U)
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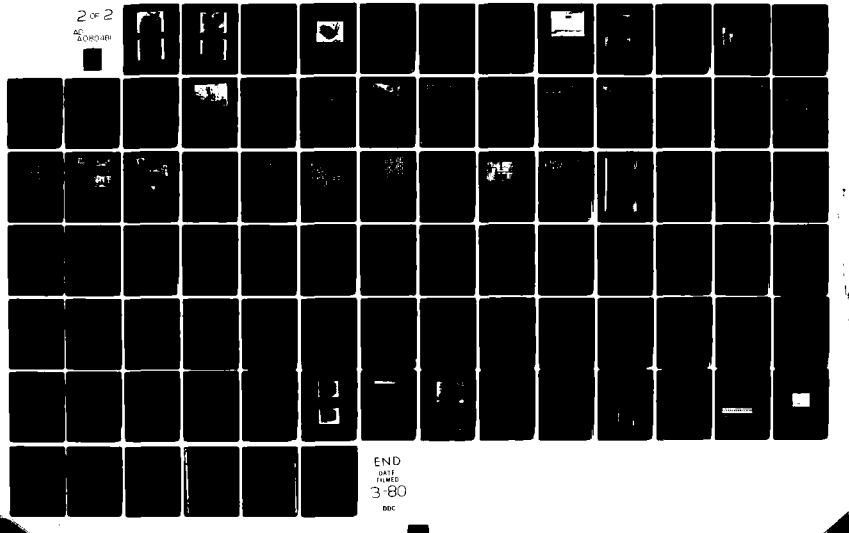

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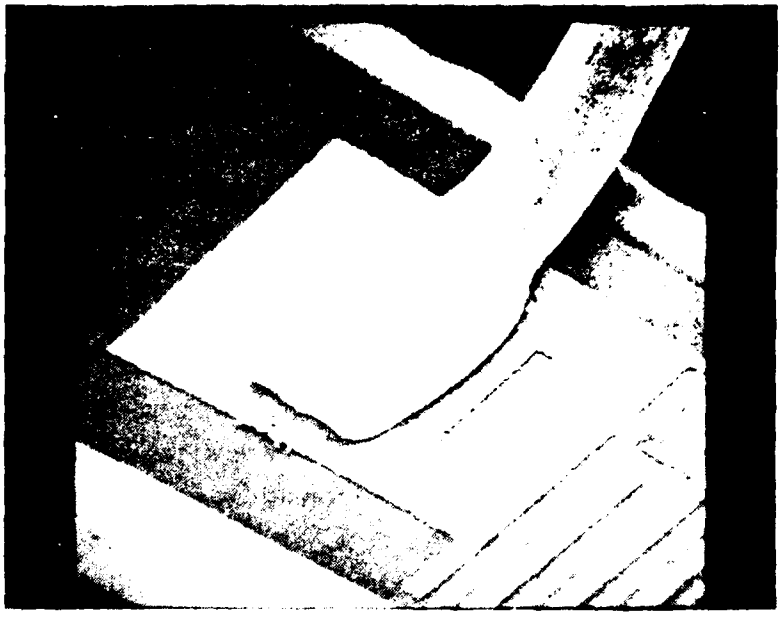

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FIGURE A6. SEM PHOTOGRAPH OF AN Al-Al BOND AT A DIE PAD

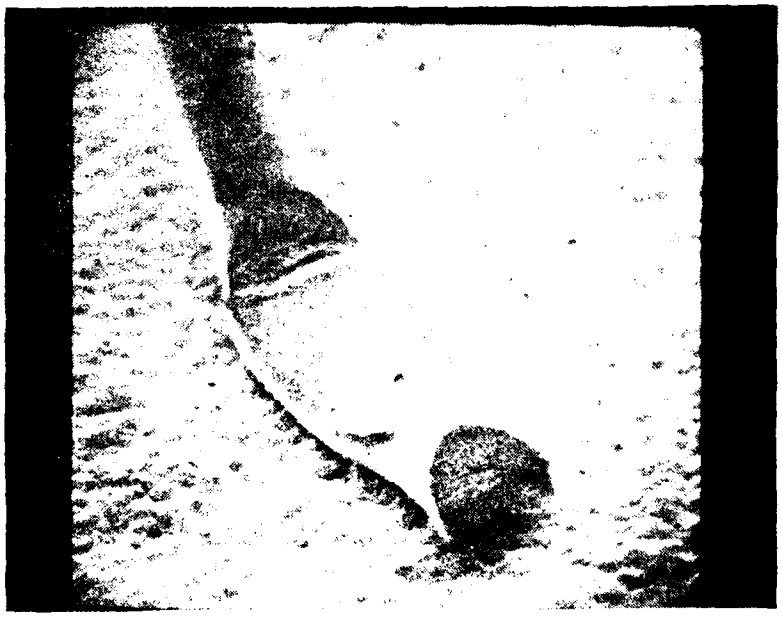

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FIGURE A7. SEM PHOTOGRAPH OF AN Al-Au BOND AT THE LEAD FRAME

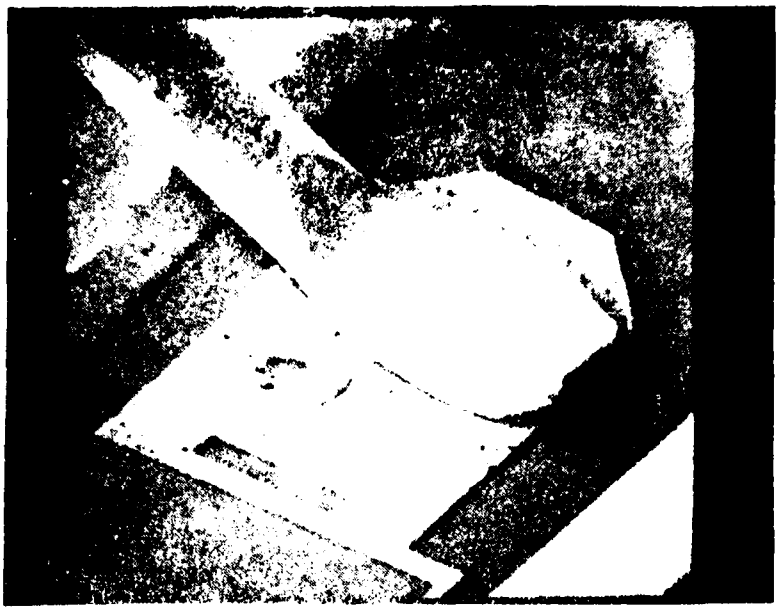

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FIGURE A8. SEM PHOTOGRAPH OF A TEST PROBE MARK - PAD 1 AM9130 S/N 6

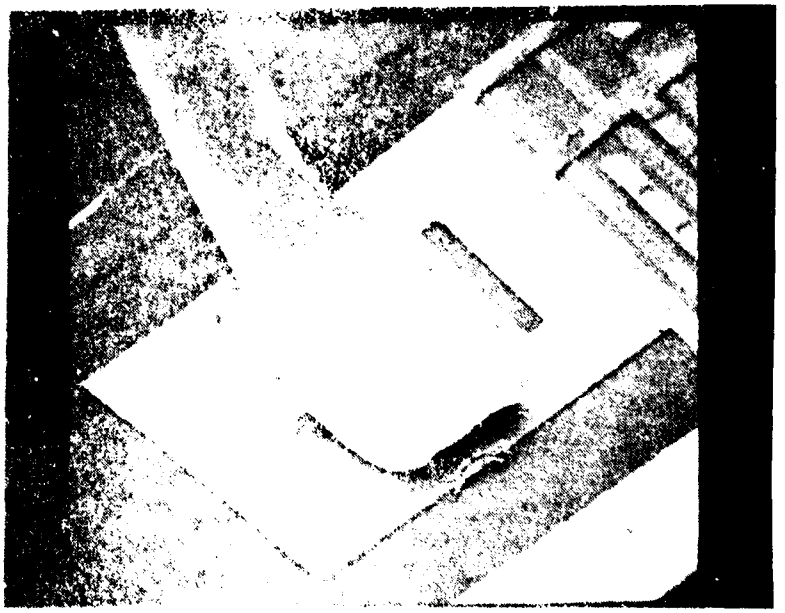

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FIGURE A9. SEM PHOTOGRAPH OF A TEST PROBE MARK - PAD 1 AM9130 S/N 6

TABLE A2. BOND PULL TEST SUMMARY

PART TYPE	SERIAL NO. 2/	FORCE REQUIRED TO BREAK BOND 1/				MIL-STD-883 METHOD 2011.2 REQUIREMENT GRAMS
		MIN GRAMS	MEAN- GRAMS	SIGMA	MAX GRAMS	
AM9130	6	4.0	5.0	0.8	6.5	1.7
AM9140	6	4.3	5.8	0.7	6.6	1.7

NOTES:

1/ NO BOND SEPARATION AT BOND PAD.

2/ TWENTY-FOUR (24) BOND WIRES OF EACH PART TYPE PULLED. BOTH TWENTY-TWO (22) PIN DEVICE TYPES HAVE TWO (2) V_{CC} AND TWO (2) V_{SS} BOND WIRES TO THE DIE.

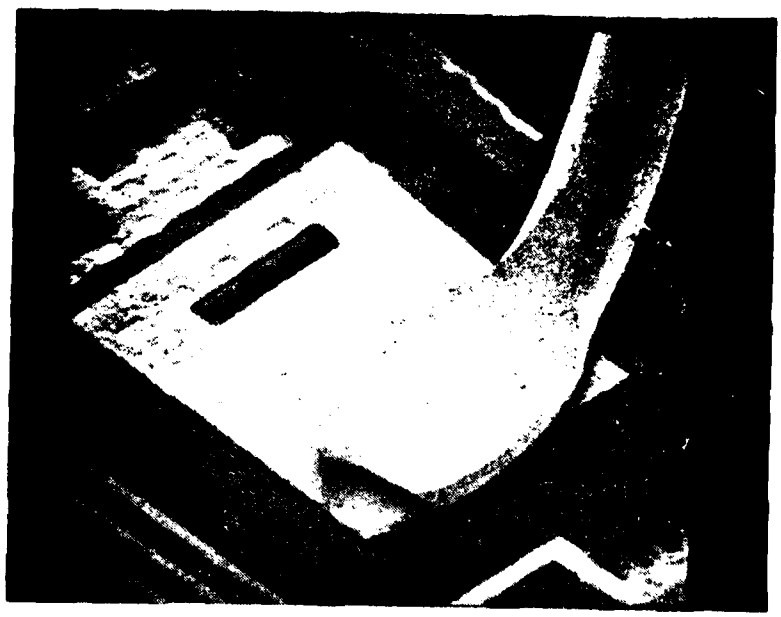

FIGURE A10. SEM PHOTOGRAPH OF LEAD DISPLACEMENT – PAD 4 AM9130 S/N 6

TABLE A3. SUMMARY OF PHYSICAL CHARACTERISTICS

PACKAGE	
Type	22-pin side brazed, cofired ceramic
Size	1.076 x .412 in (27.33 x 10.46 mm)
Mass	2.437 gm
Die Cavity	.00212 cu in (34.72 cu mm)
DIE	
Size - scribe line to scribe line	187 x 192 mils (4.75 x 4.88 mm)
Area	35904 sq mils (23.18 sq mm)
Scribe Method	Mechanical - Diamond saw
Attachment	Gold/Silicon Eutectic
BOND PAD	
Area of smallest pad	18.9 sq mils (.012 sq mm)
WIRE	
Material	Aluminum
Size (diameter)	1.1 mil (.028 mm)
Average measured bond pull strength	5.4 gm of force
Bonding Method	Ultrasonic
INTERCONNECTS	
Aluminum	
Narrowest stripe measured	.139 mils (.0035 mm)
Closest line spacing	.305 mils (.00775 mm)
Nominal Thickness	6000 Å
V_{CC} Stripe Cross Sectional Area	3.4×10^{-7} sq in (2.2×10^{-6} sq cm)
Polysilicon	
Narrowest stripe measured	.194 mils (.0049 mm)
Closest line spacing	.417 mils (.0106 mm)

TABLE A4. SUMMARY OF GAS MASS SPECTROMETER ANALYSIS RESULTS

PART TYPE	SERIAL NUMBER	CONCENTRATION (% V/V)				
		N_2	H_2	O_2	CO_2	H_2O
AM9130	8	98.8	0.8	-	0.2	0.2
	9	98.7	1.0	-	0.2	0.2
AM9140	8	98.8	0.5	0.5	0.2	-
	9	99.3	0.5	-	0.2	-

NOTE:
GMS ANALYSIS PERFORMED BY RADC (RBRM).

3.0 DEVICE TECHNOLOGY

Both the AM9130 and AM9140 memories were implemented with N-channel depletion and enhancement mode polysilicon gate MOS transistors. The enhancement and depletion mode transistors used with these devices have nominal thresholds set at 0.8V and -3.5V, respectively. Depletion mode transistors that were used as loads were formed by using ion implantation coupled with a buried contact between the polysilicon gate and source diffusion layer, as shown in Figure A11. The interconnects used throughout the devices were metallization, polysilicon and diffused conductors.

An angle section was performed on both device types to study tne internal structure of the memory cell transistors. A close-up photograph of the memory cell area is presented in Figure A12. The corresponding section and transistor structure is presented in Figure A13.

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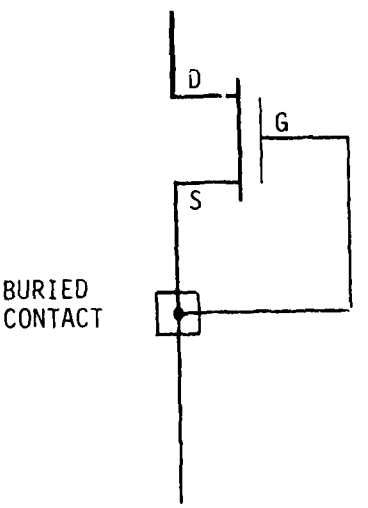
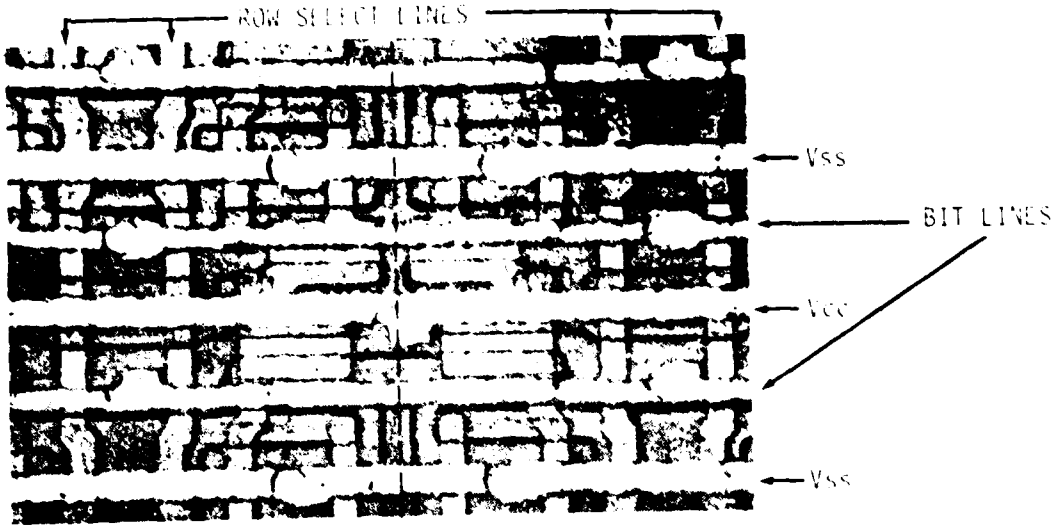
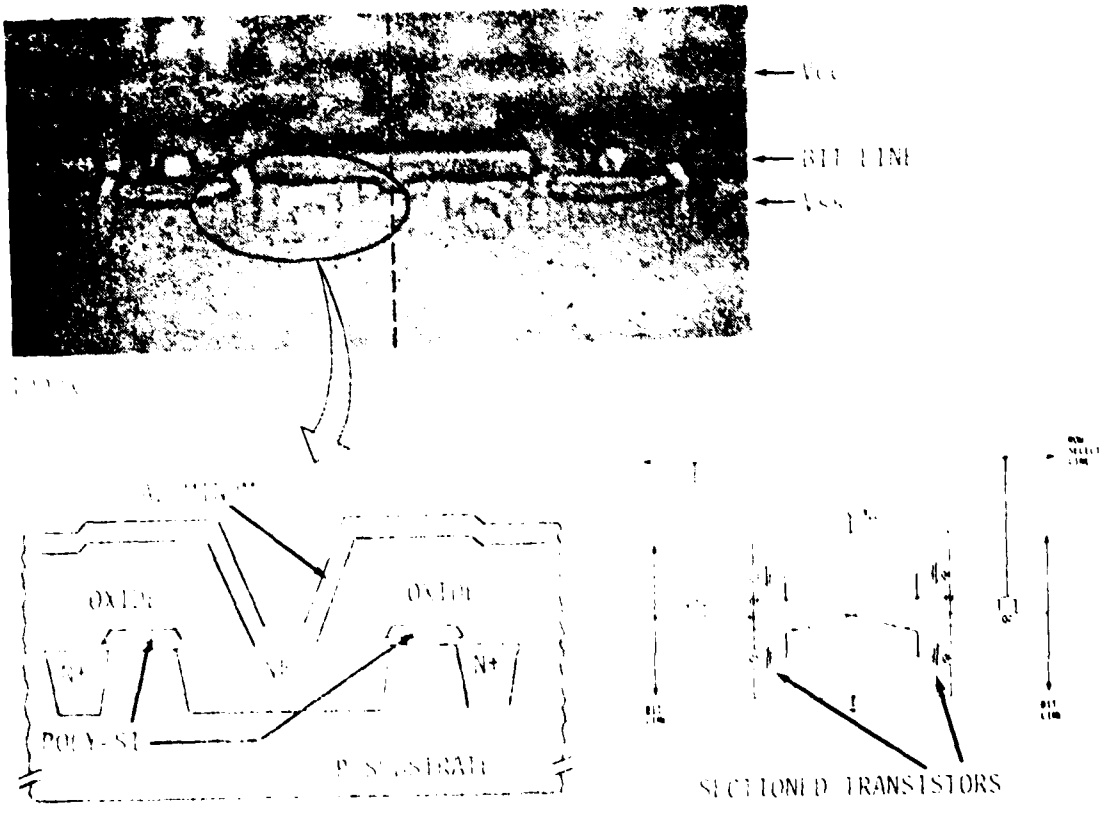


FIGURE A11. BURIED CONTACT



[illegible]

[illegible] MEMORY CELL CLOSE-UP



[illegible] MEMORY CELL TRANSISTOR STRUCTURE

4.0 ELECTRICAL CHARACTERIZATION

Die photographs indicating the functional blocks for the AM9130 and AM9140 are presented in Figures A14 and A15, respectively. The pinouts of the corresponding devices are presented in Figures A16 and A17 with associated bit maps in Figures A18 and A19. The bit maps were verified and correspond to those illustrated in the initial draft of the MIL-M-38510/237.

4.1 DEVICE ORGANIZATION

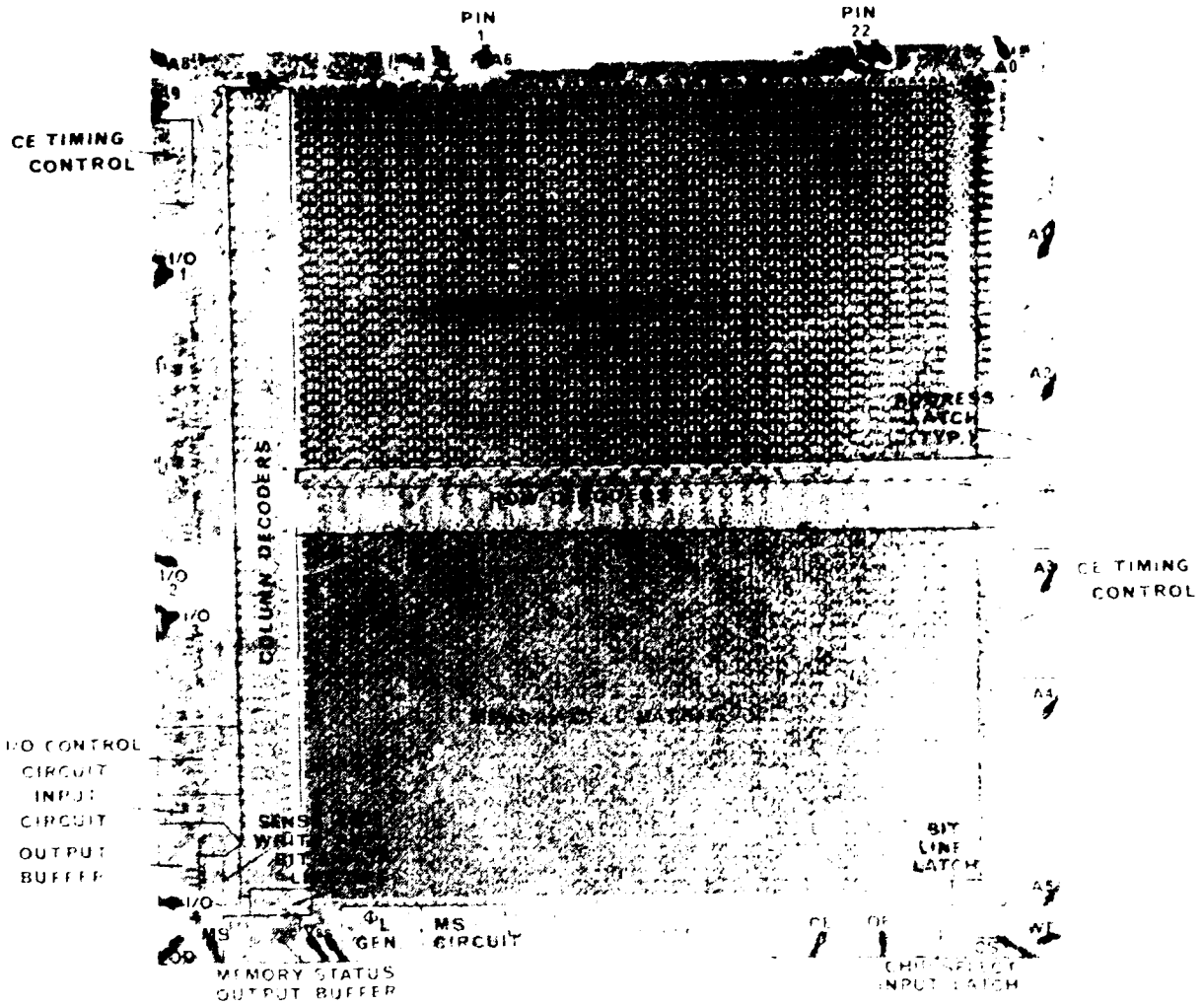
The AM9130 is organized as 1024 words with four bits per word. A single four bit word is accessed through ten address lines (A0 through A9). Addresses A0 through A5 select one of 64 rows of memory through the row decoders. Similarly, addresses A6 through A9 select four of 64 columns, one column from each bit section, through the column decoders. Data is written into or read out from the cells through four input/output (I/O) pads. Bits 1, 2, 3 and 4 correspond to I/O 1, 2, 3 and 4, respectively.

The AM9140 is organized as 4096 words with one bit per word. A one bit word is accessed through twelve (12) address lines (A0 through A11). As in the AM9130, addresses A0 through A5 select one of 64 rows through the row decoders. Addresses A6 through A11 select one of 64 columns through the column decoders. Data is written into the accessed cell through the Data In (DI) pad and read out through the Data Out (DO) pad.

4.2 CIRCUIT DESCRIPTION

All the inputs of the AM9130 and AM9140 devices are designed with static charge protection circuits, as presented in Figure A20. These circuits utilize an RC network coupled with field turn-on transistors with threshold voltages in the 10-20 V range. The circuits are designed to protect against both positive and negative transients in the 200 volt range.

The address input registers of both memory types are implemented using a latching network which operates as an address register. This latching register allows the memory to ignore the address lines until the next Chip Enable (CE)


PIN 1
PIN 22
CE TIMING CONTROL
I/O 1
I/O 2
I/O 3
I/O 4
COLUMN DECODERS
ADDRESS LATCH (TYP.)
CE TIMING CONTROL
I/O CONTROL
CIRCUIT
INPUT
CIRCUIT
OUTPUT
BUFFER
BIT LINE LATCH
MS CIRCUIT
MEMORY STATUS OUTPUT BUFFER

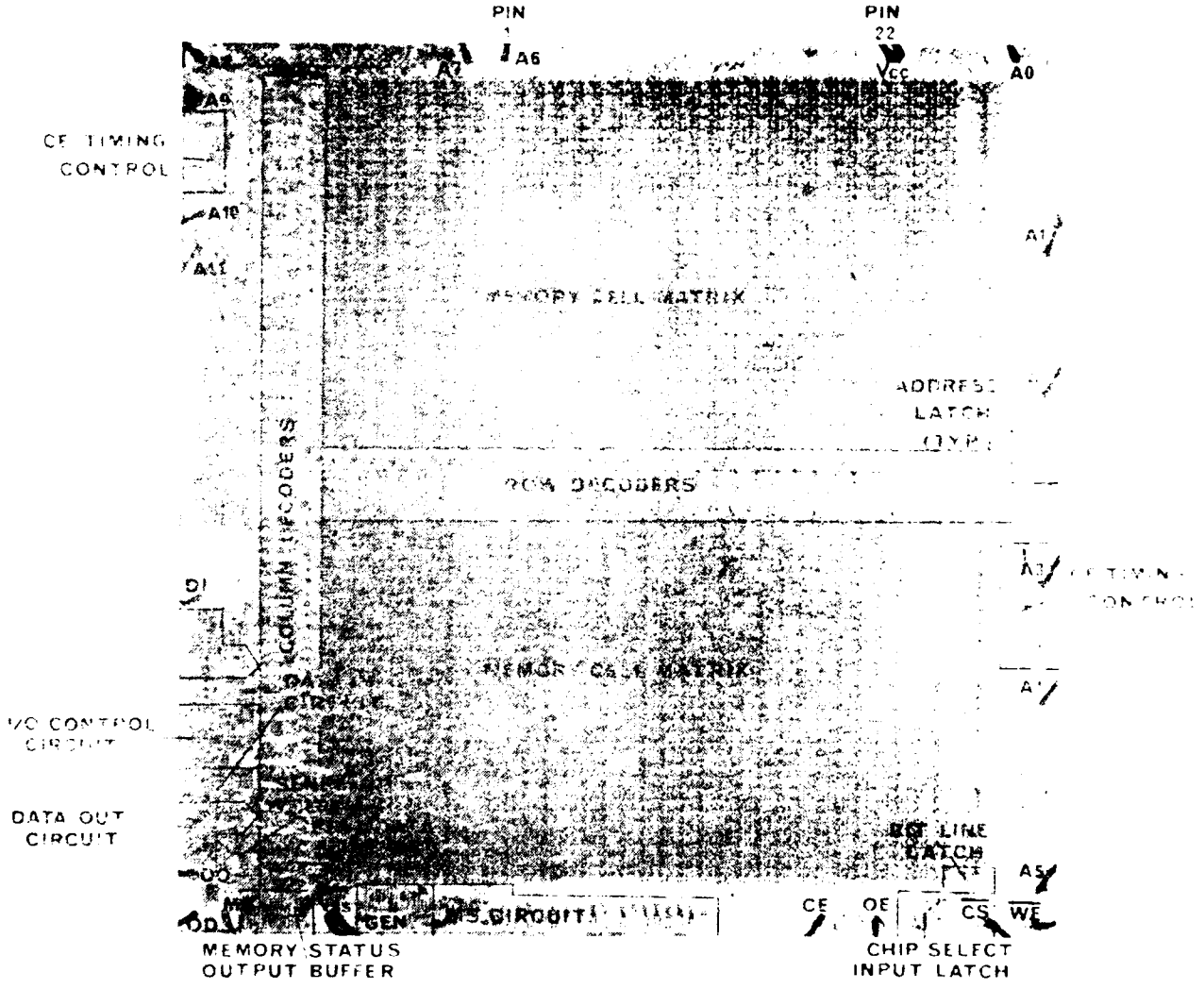


FIGURE A15. DIE PHOTOGRAPH INDICATING THE FUNCTIONAL BLOCKS OF THE AM9140

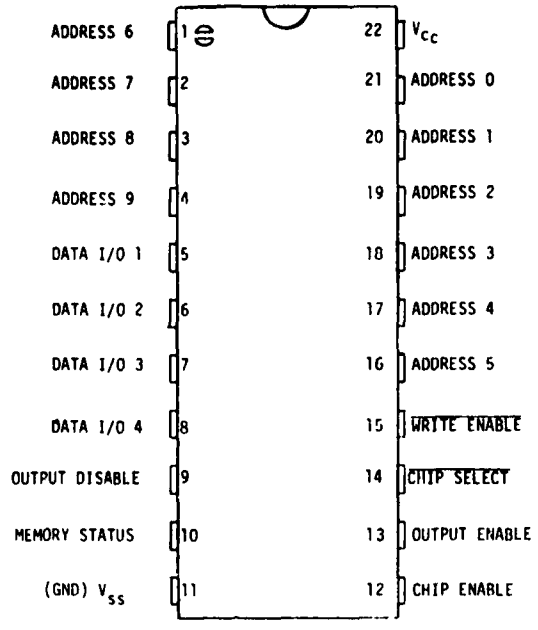


FIGURE A16. PINOUT FOR THE AM9130

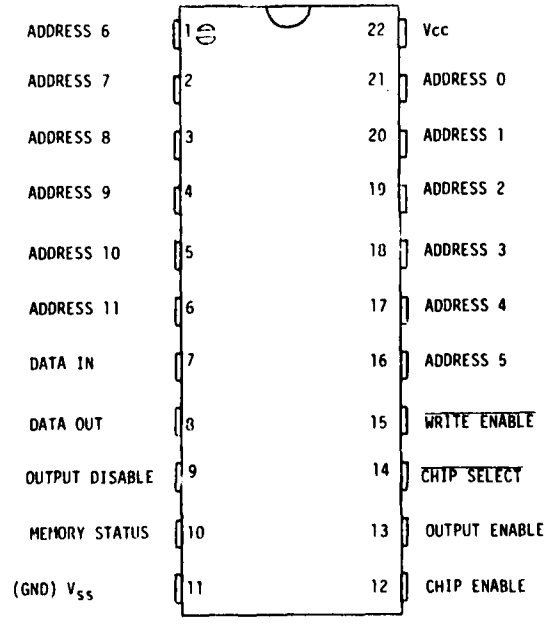


FIGURE A17. PINOUT FOR THE AM9140

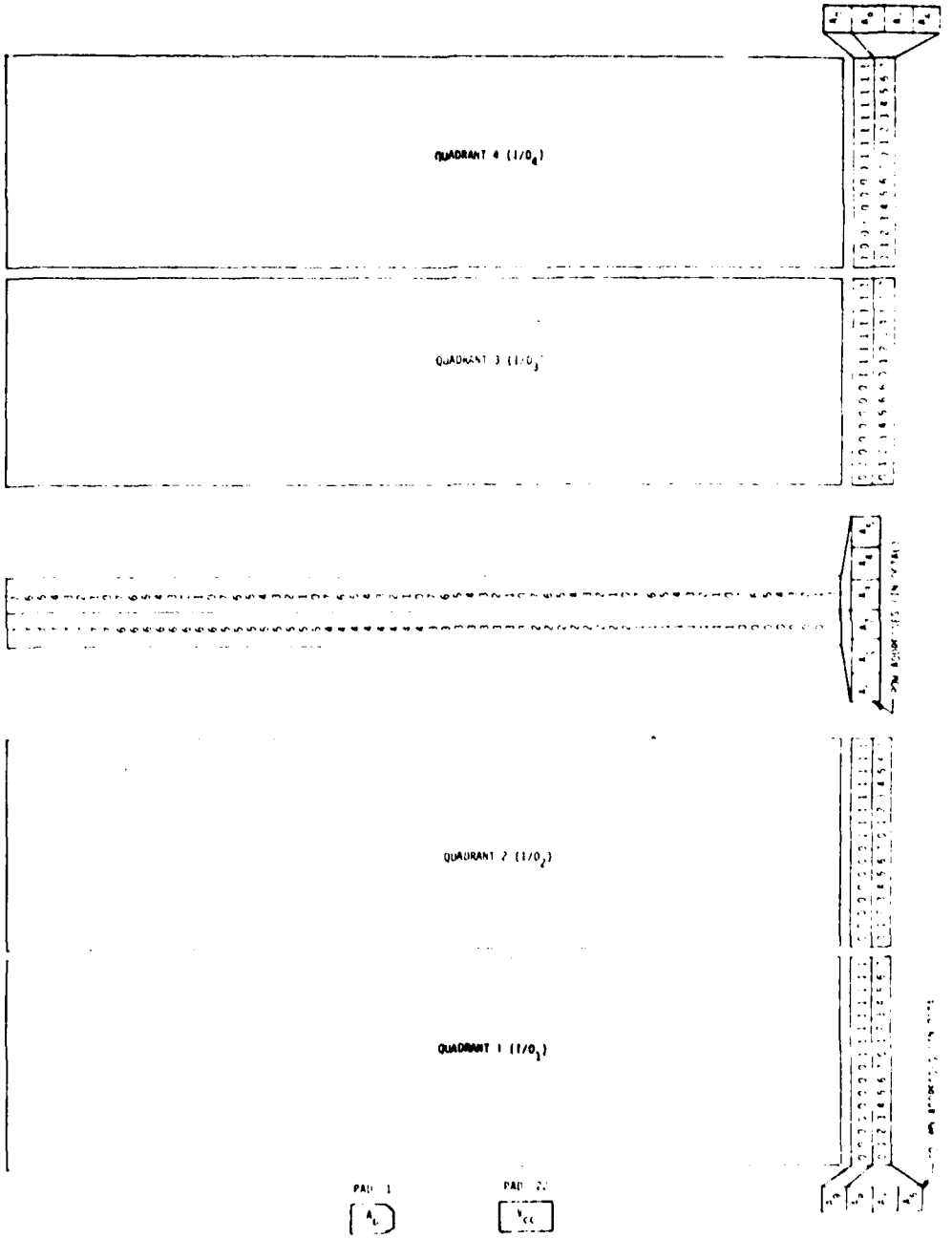


FIGURE A18. BIT MAP FOR THE AM9130

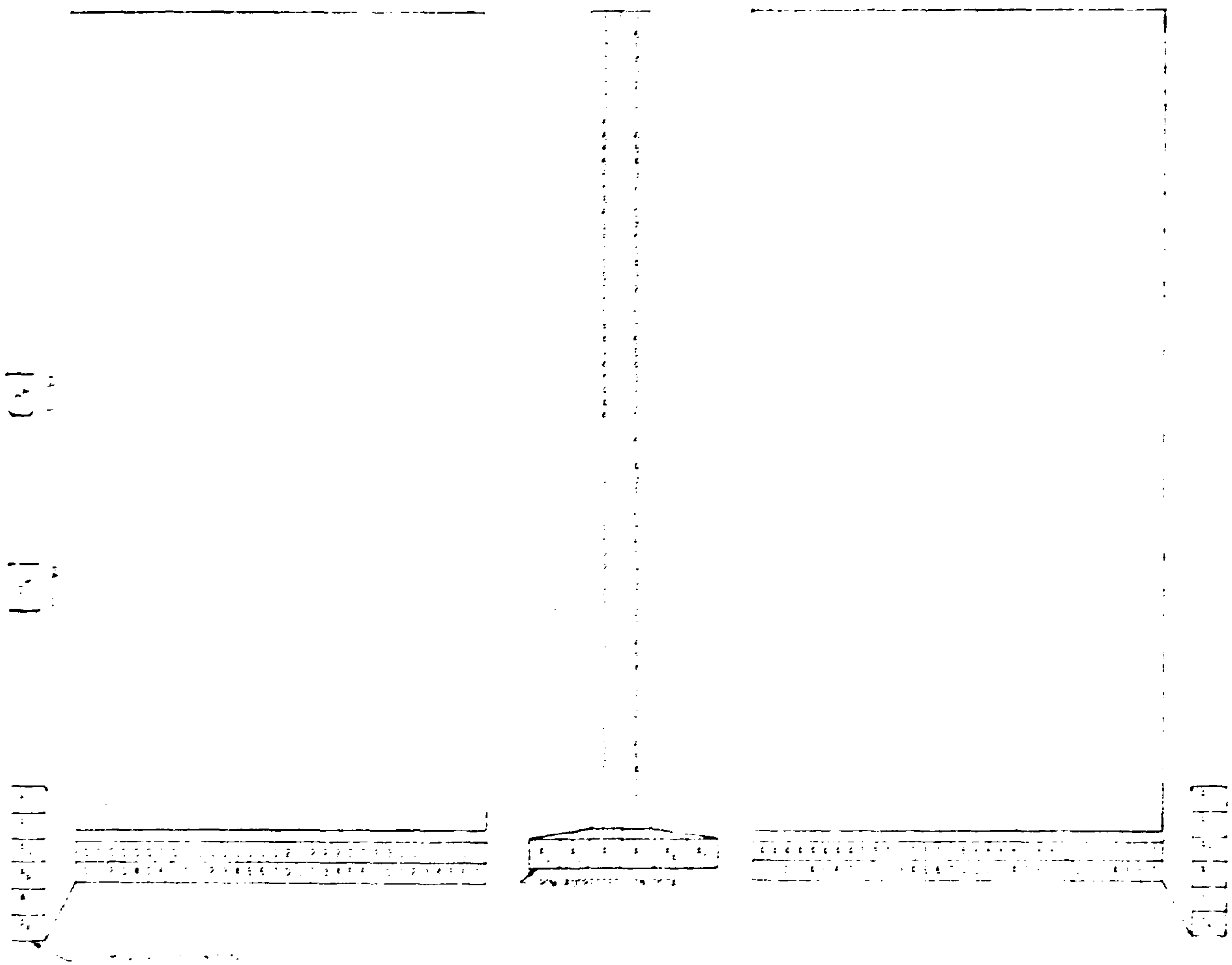
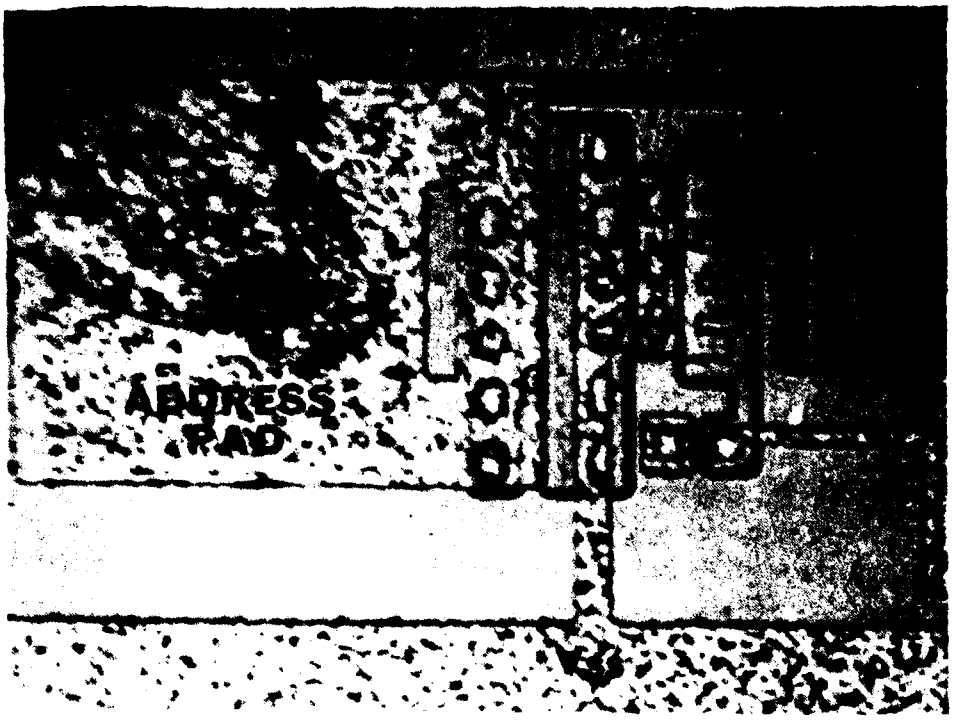


FIGURE A.9. BIT MAP FOR THE [illegible]



610X

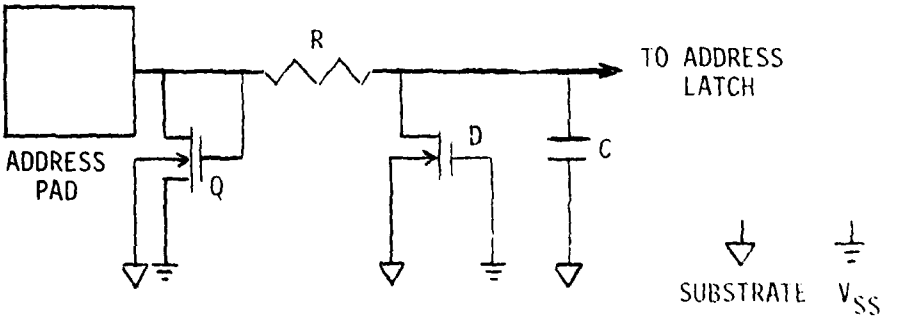


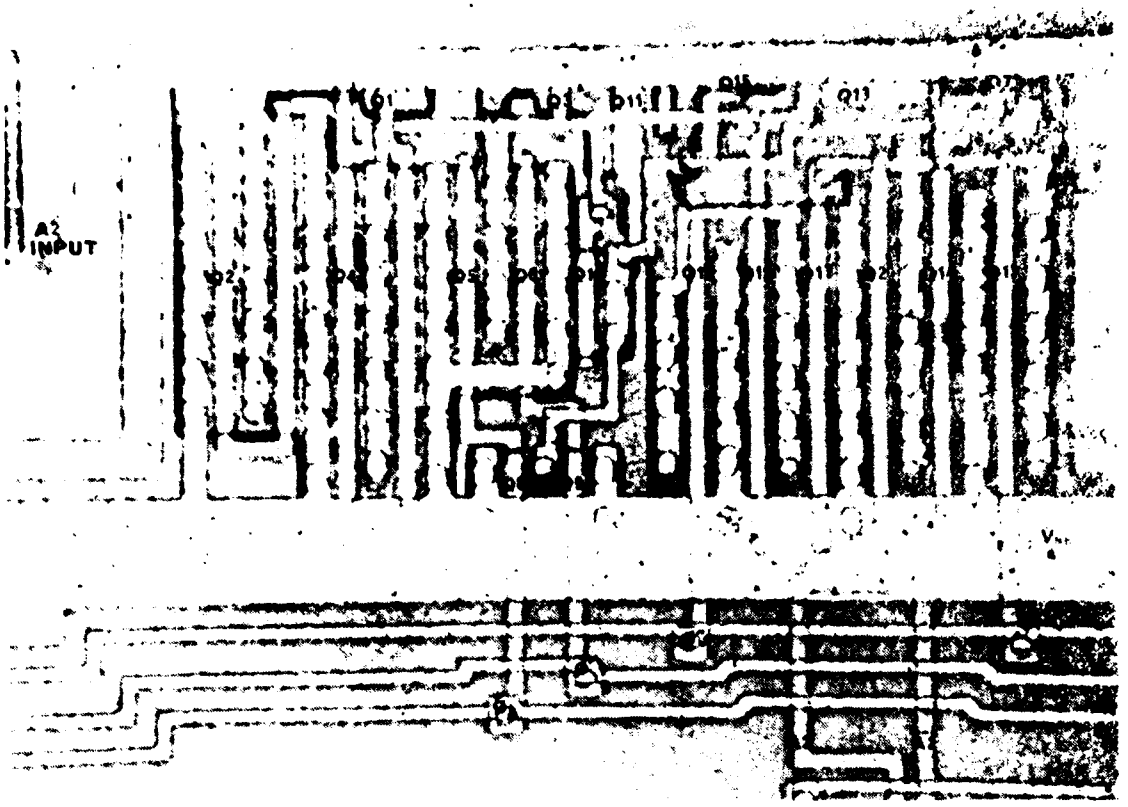
FIGURE A20. STATIC CHARGE PROTECTION CIRCUIT

cycle is initiated. The latch is set in response to the Chip Enable input and the outputs of the slowest row address bit position through the Φ_A signal. The address input register is presented in Figure A21 and the Φ_A signal generator in Figure A22. The $\overline{\text{Chip Select}}$ ($\overline{CS}$) input performs the function of a high order address, used when multiple devices are stacked to handle word capacities larger than that of an individual device. The $\overline{\text{Chip Select}}$ input register is presented in Figure A23. The Row decoders are identical for both device types and a typical example is presented in Figure A24. The Column decoders for the two device types differ for addresses A10 and A11. Although both addresses A10 and A11 are present, they are inaccessible to the user on the AM9130 device. The gates of decoder transistors Q2 and Q3 are connected to ground for the AM9130, as shown in Figure A25.

All of the AM9130 and AM9140 functions operate from an internal timing control network, which outputs several clocked signals in response to the Chip Enable signal. This network is presented in Figures A26, A27 and A28. These Chip Enable controlled signals, with the Output Enable (OE), Output Disable (OD) and $\overline{\text{Write Enable}}$ ($\overline{WE}$) are used in the input-output control circuits which are presented in Figure A29.

In the AM9130, the Input circuit and Output Buffer circuit are accessed through a common pad for each word bit. The AM9130 Input circuit and Output Buffer circuit are presented in Figure A30 and Figure A31 respectively.

The AM9140 Input circuit is accessed through the Data In pad and the Output Buffer circuit is accessed through the Data Out pad. The Input circuits and Output Buffer circuits of word bits 1 and 2 of the AM9130 exist on the AM9140 but are inaccessible. The I/O 3 pad of the AM9130 serves as the Data In pad of the AM9140 and the I/O 4 pad of the AM9130 serves as the Data Out pad of the AM9140. The I/O 2 pad of the AM9130 is not used on the AM9140. The I/O 1 pad of the AM9130 serves as the A11 pad of the AM9140. Conversely, the A10 pad of the AM9140 is not used on the AM9130. Presented in Figure A32 is the I/O 1 pad and unused static charge protection circuits of addresses A10 and A11 of the AM9130. Figure A33 illustrates how addresses A10 and A11 are implemented on the AM9140.



450X

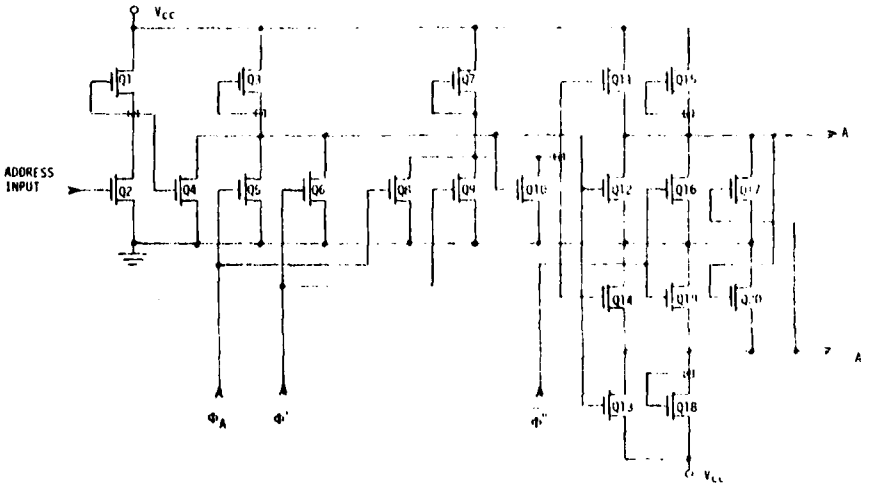
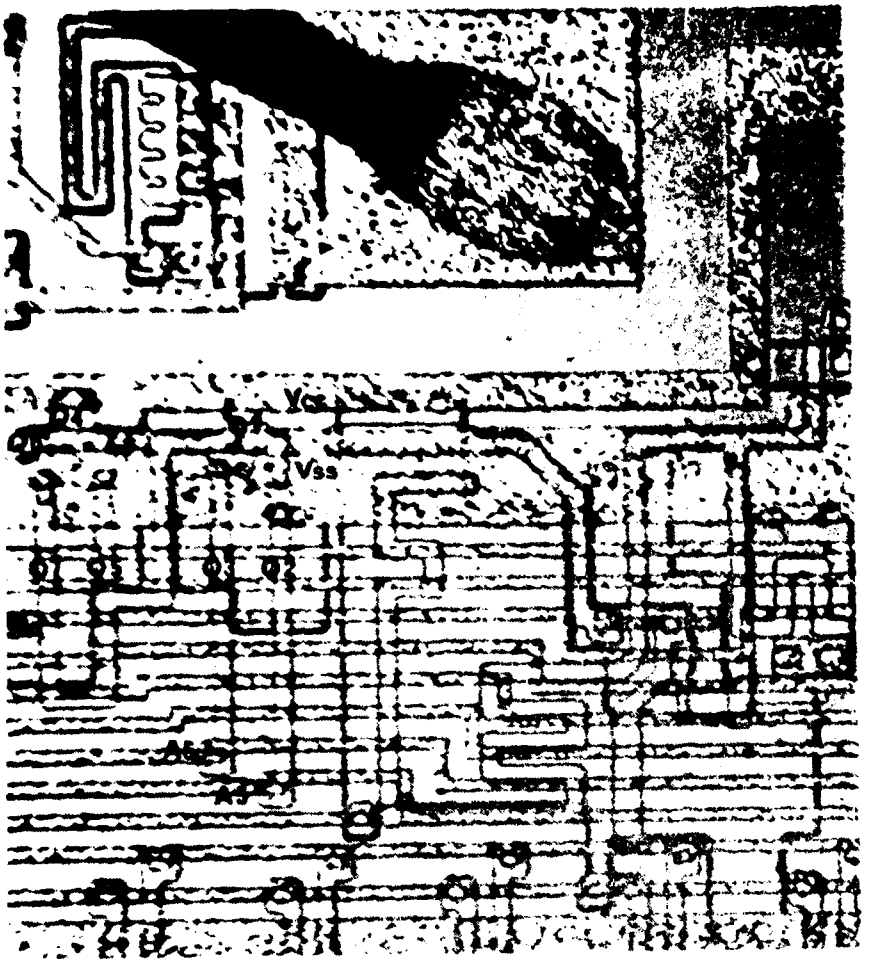


FIGURE A21. ADDRESS INPUT LATCH



410X

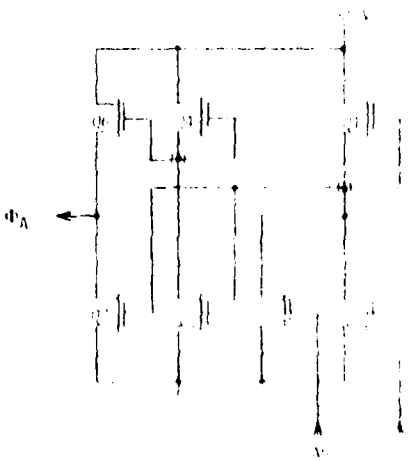
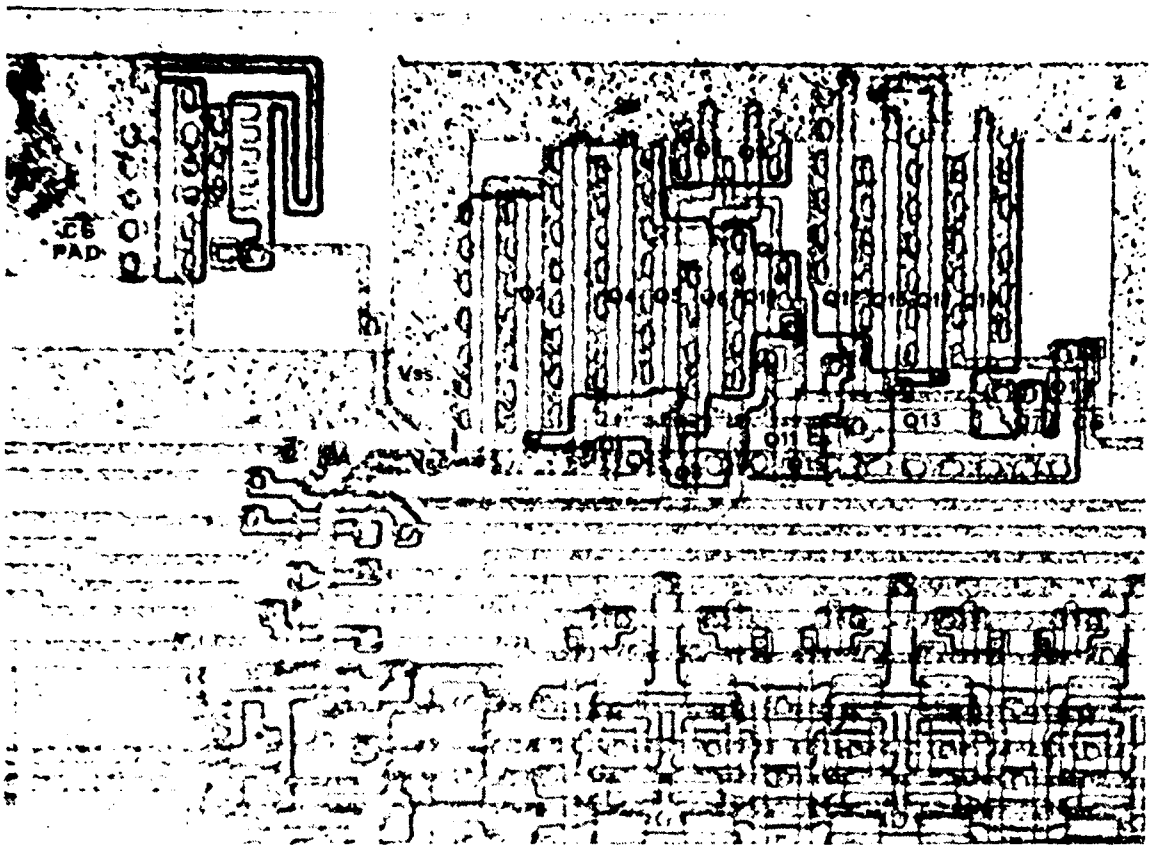


FIGURE A-7. Φ_A SIGNAL GENERATOR



330X

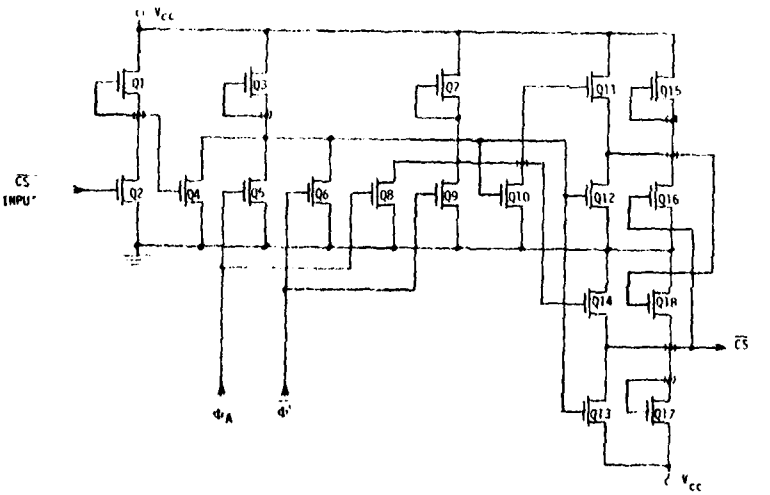
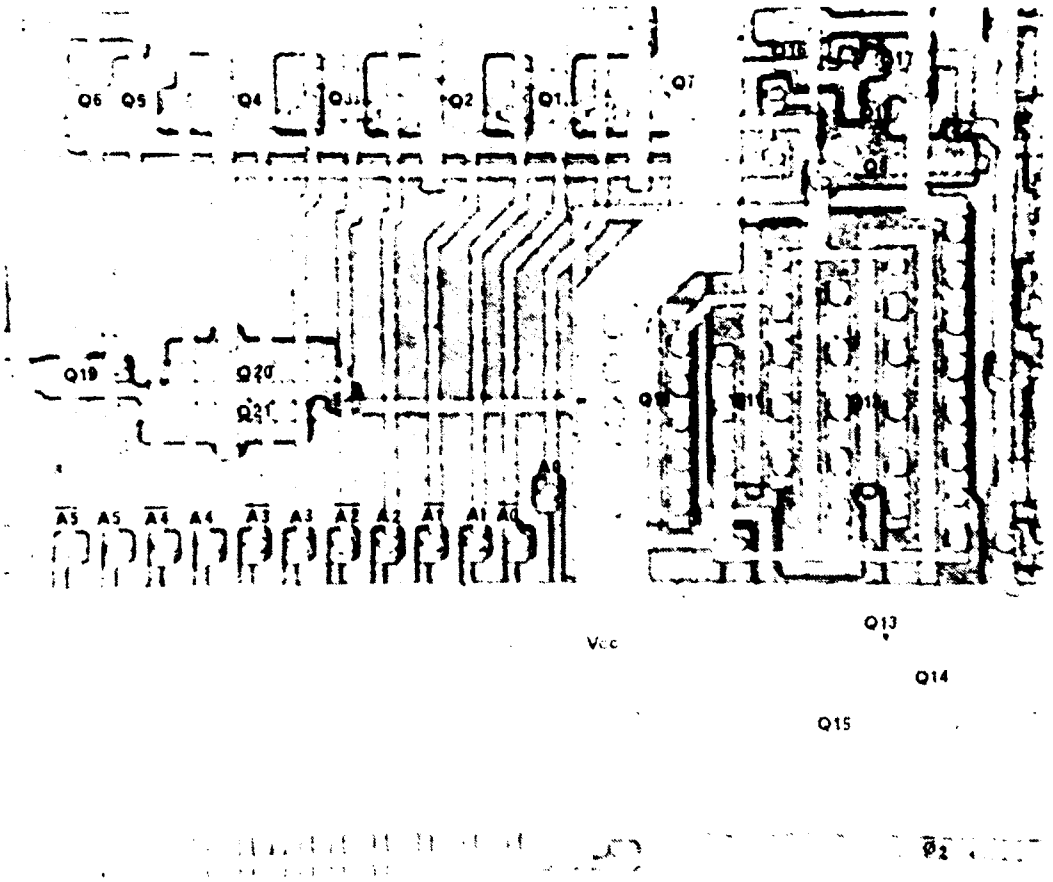


FIGURE A23. CHIP SELECT INPUT LATCH



420X

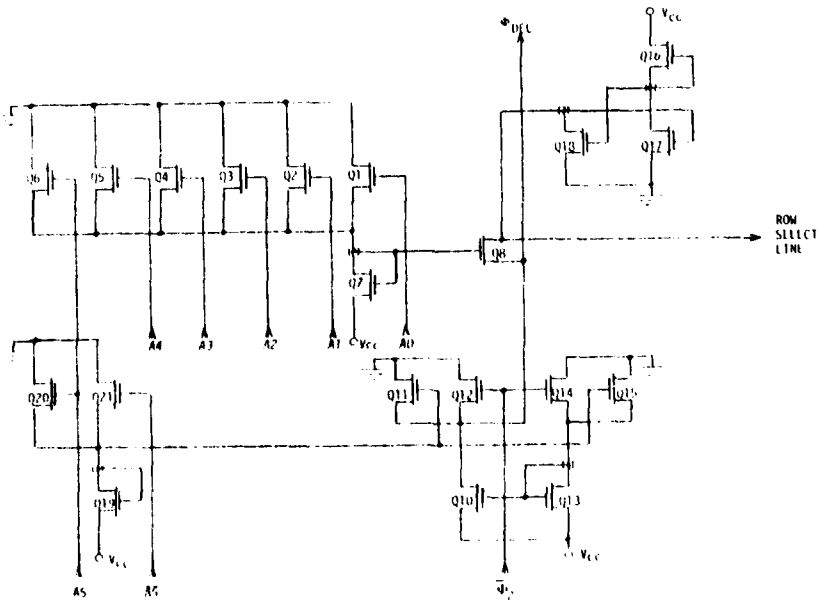
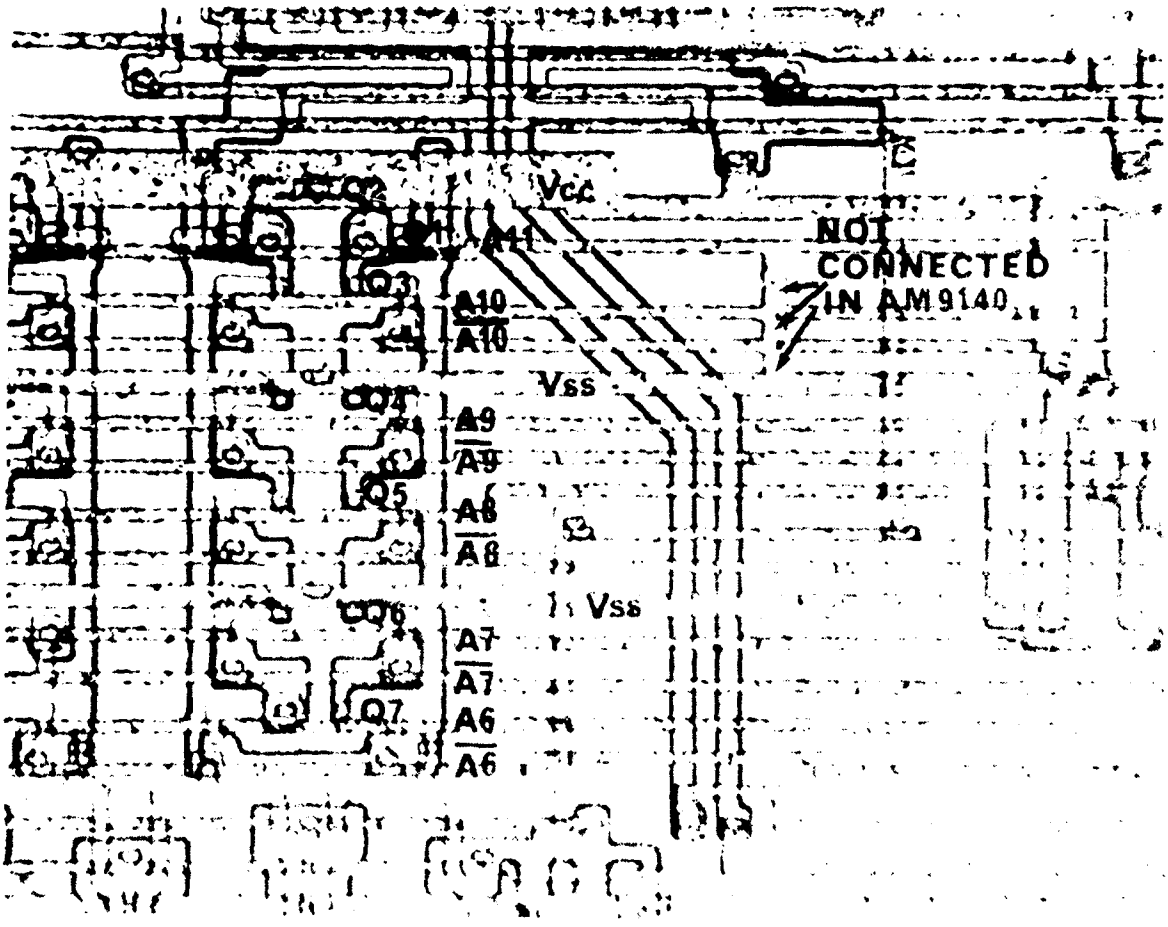


FIGURE A24. ROW DECODER



490X

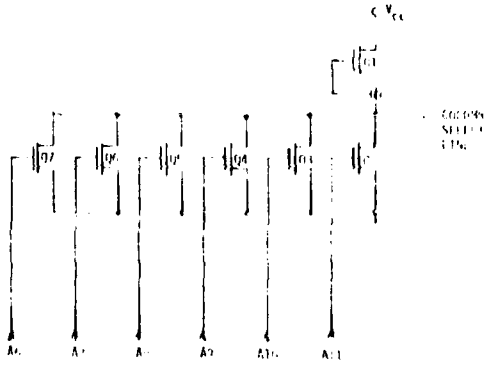
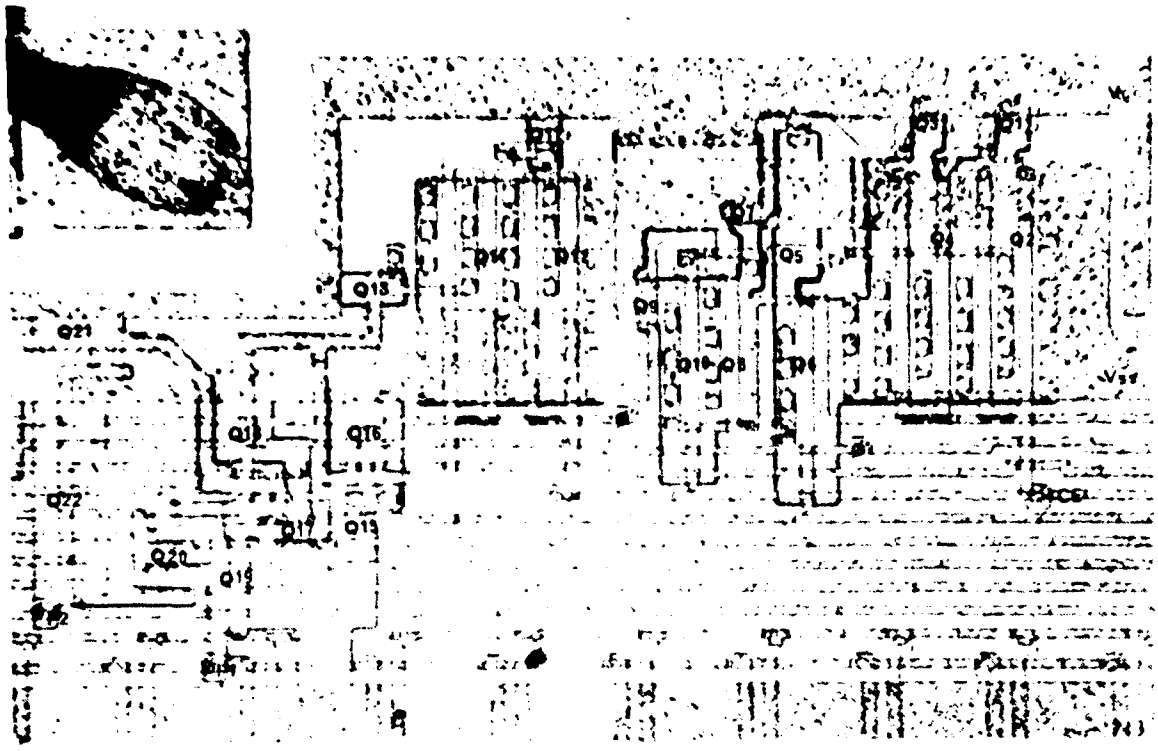


FIGURE A25. COLUMN DECODER - AM9130



300X

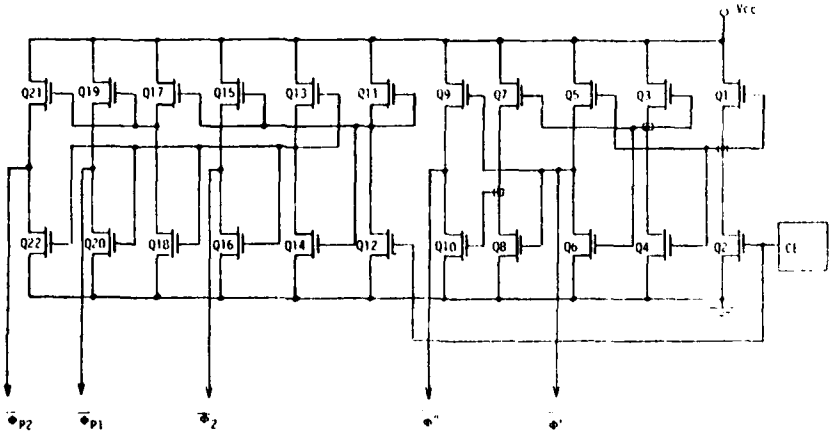
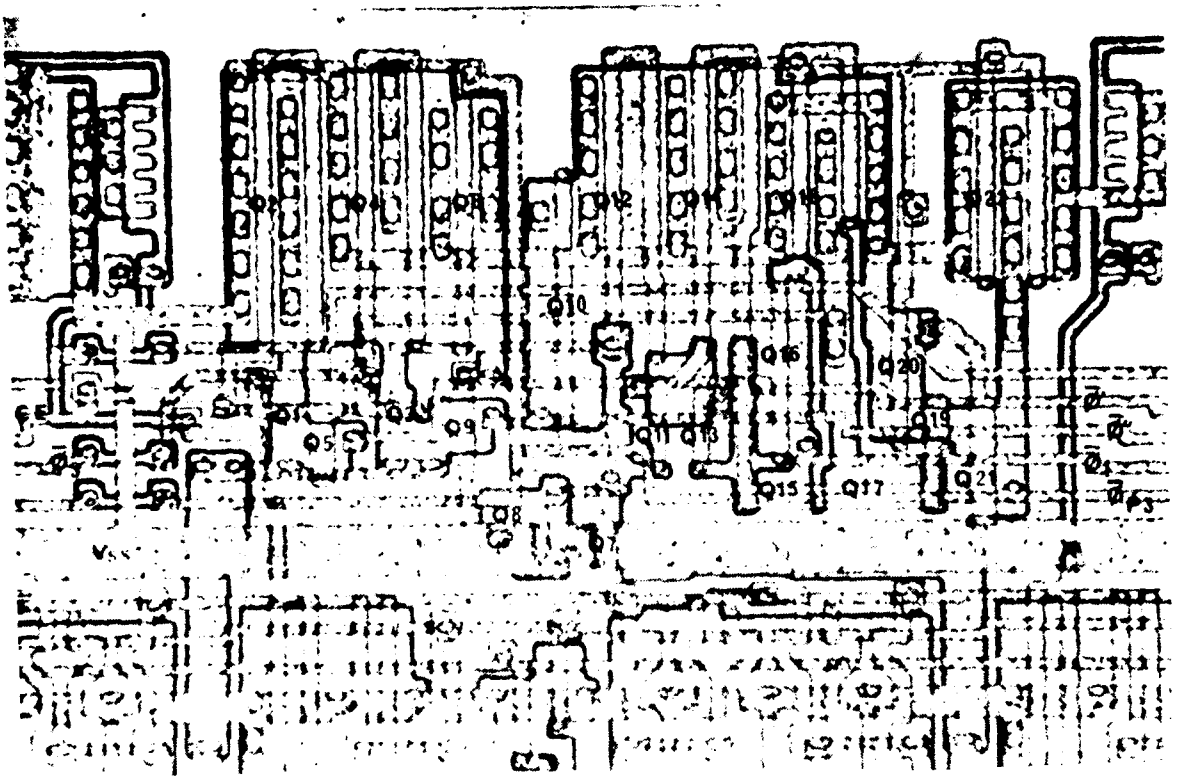


FIGURE A26. CHIP ENABLE TIMING CONTROL



360X

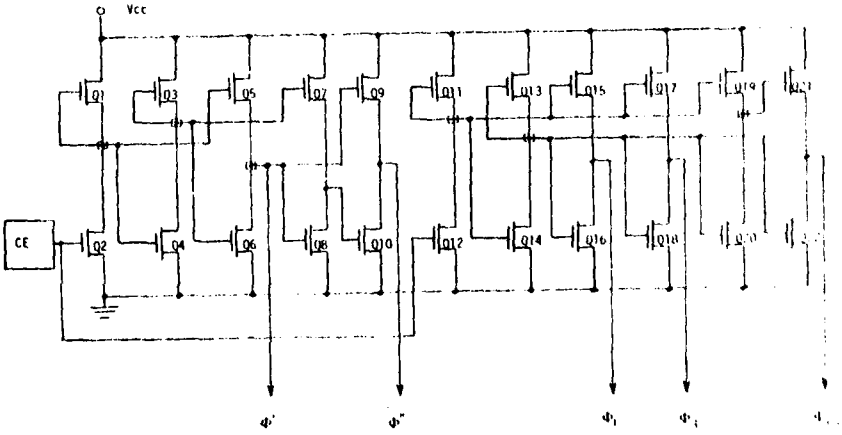
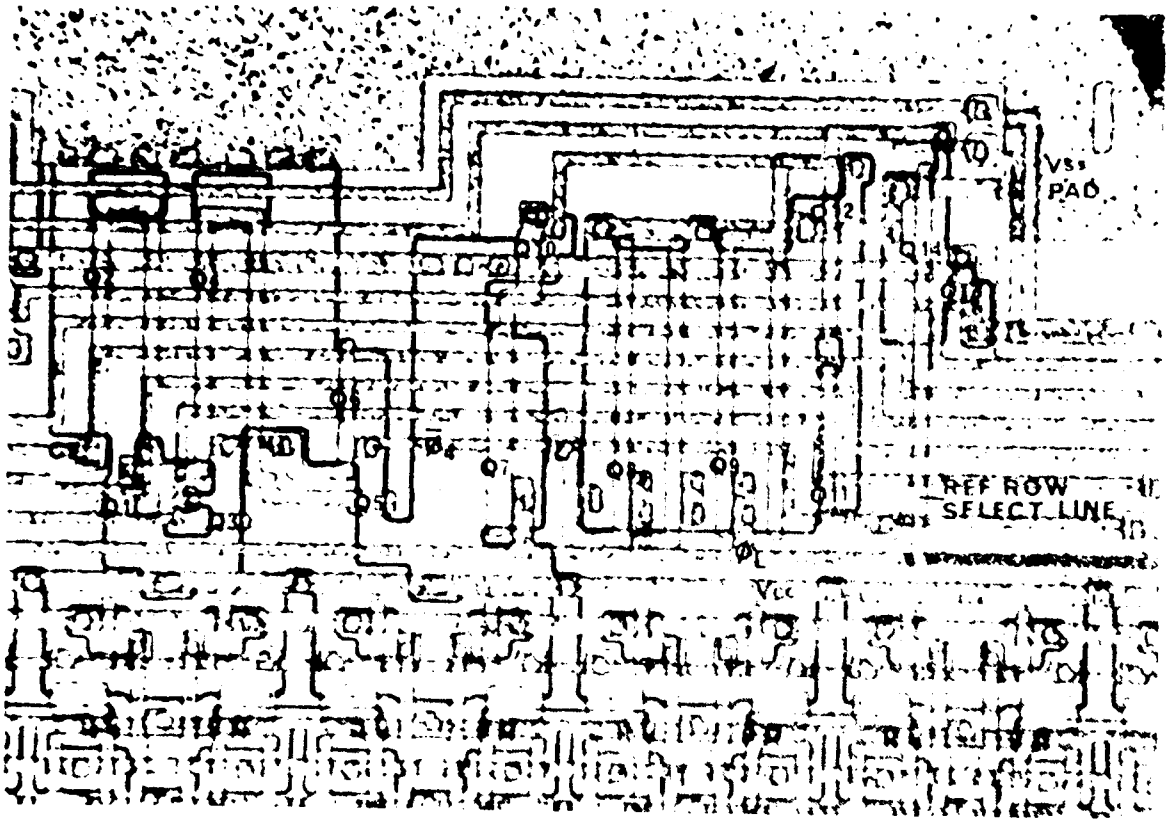


FIGURE A27. CHIP ENABLE TIMING CONTROL



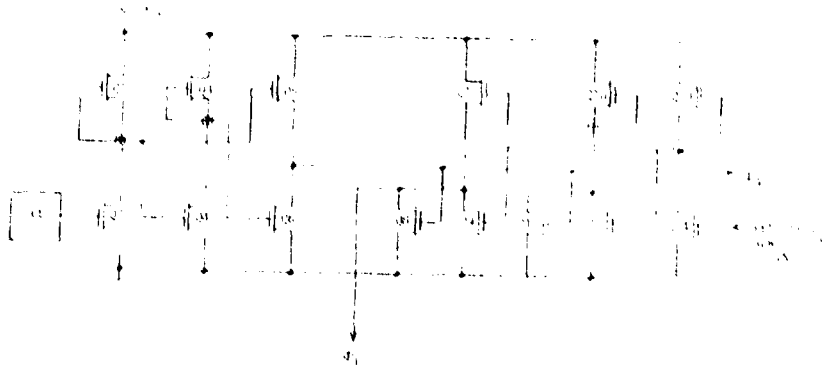


FIGURE A.28. CHIP ENABLE TIMING CONTROL (Φ_1 GENERATOR)

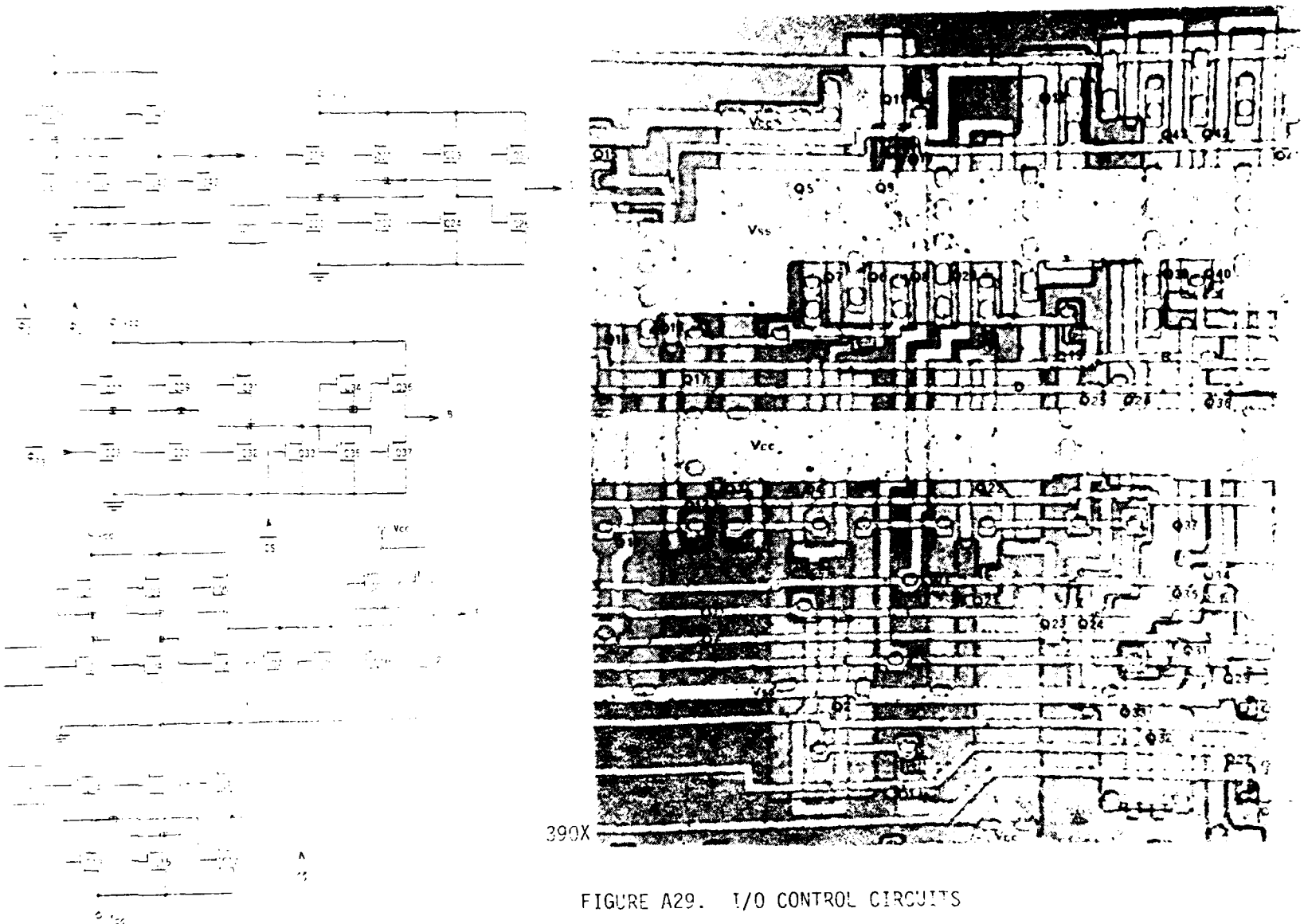


FIGURE A29. I/O CONTROL CIRCUITS

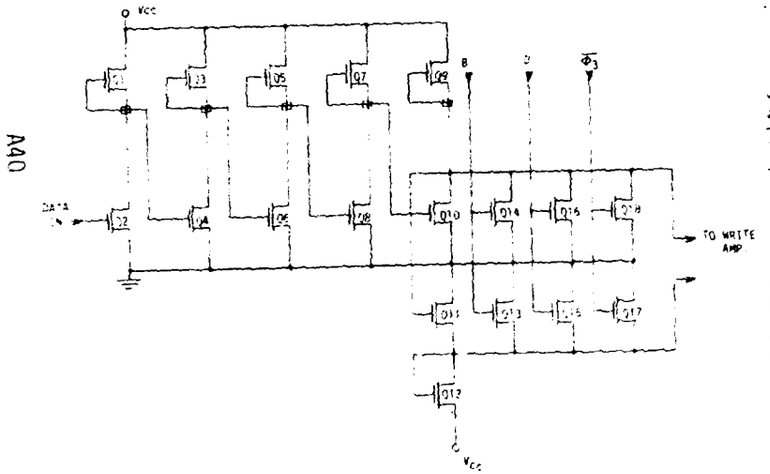
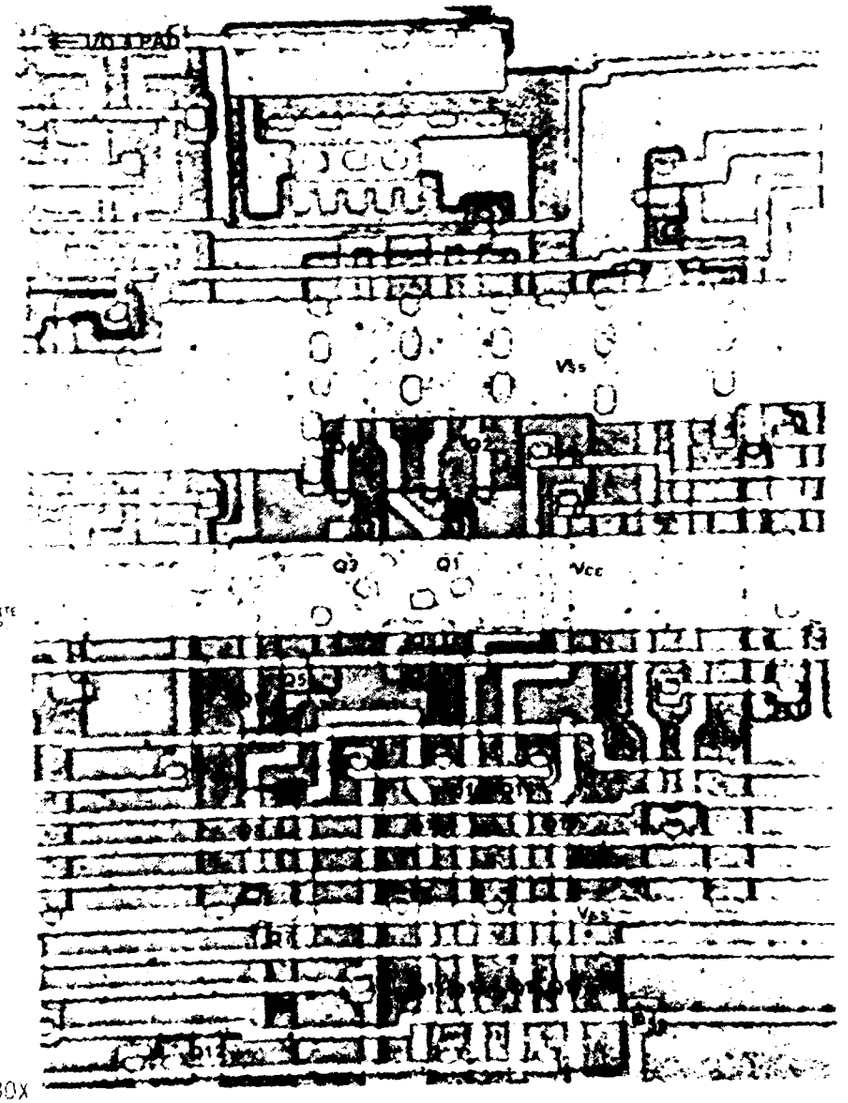
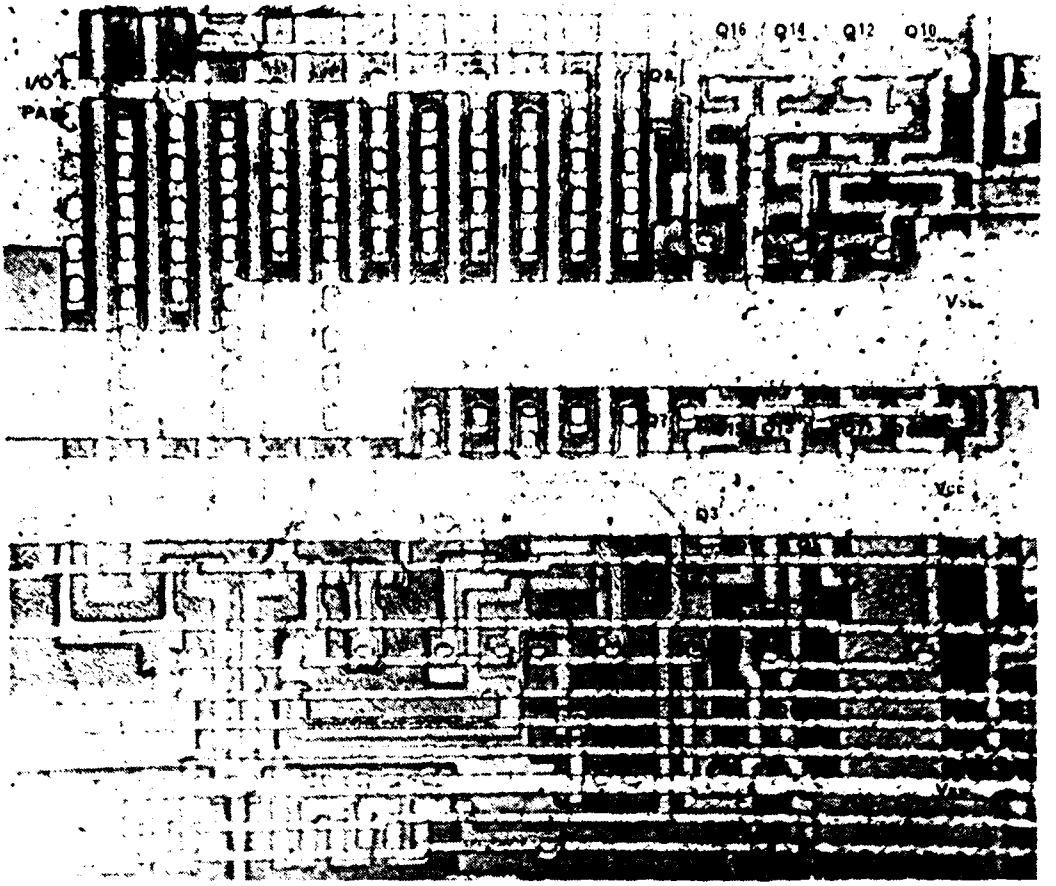


FIGURE A30. INPUT CIRCUIT – AM9130



430X



520X

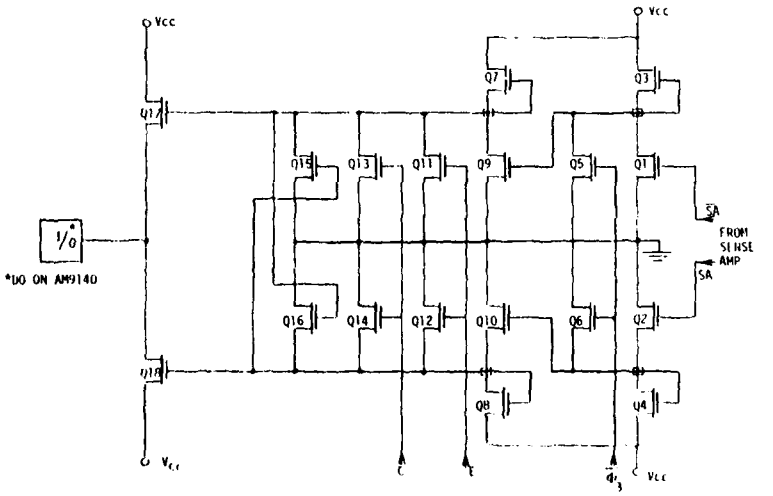


FIGURE A31. OUTPUT BUFFER - AM9130

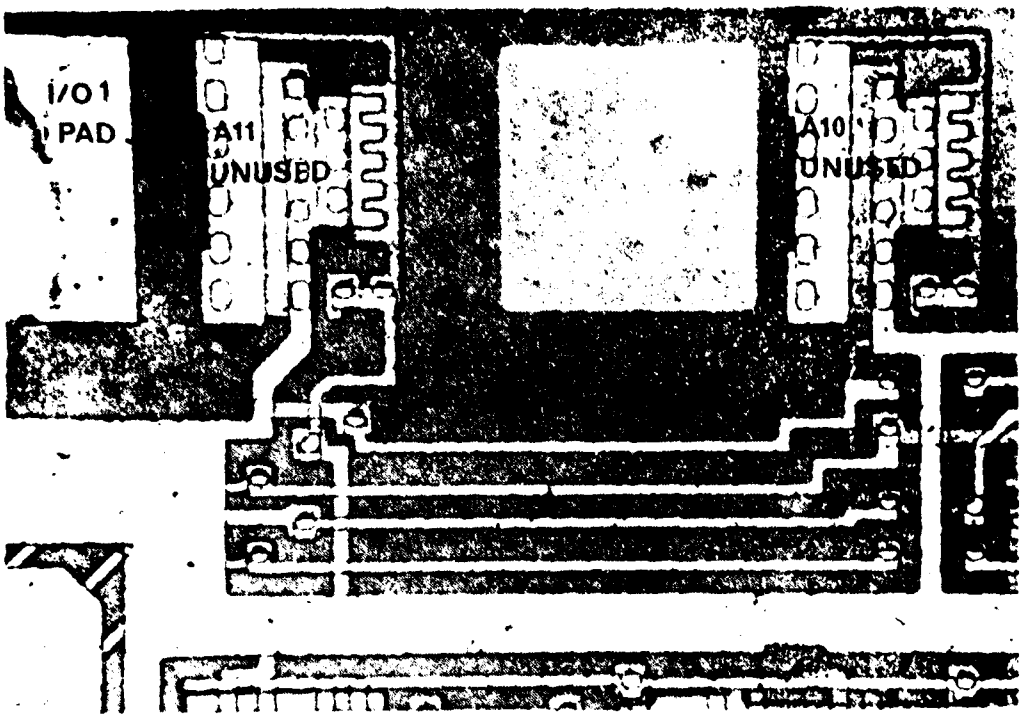


FIGURE A32. I/O 1 PAD AND UNUSED STATIC CHARGE PROTECTION CIRCUITS ON THE AM9130

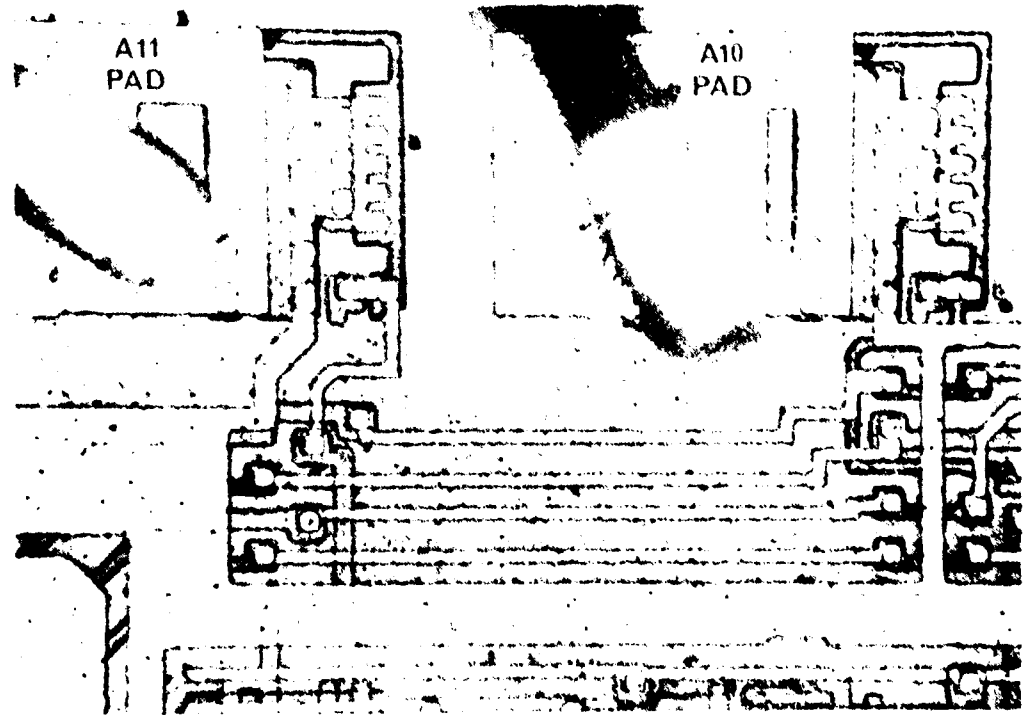
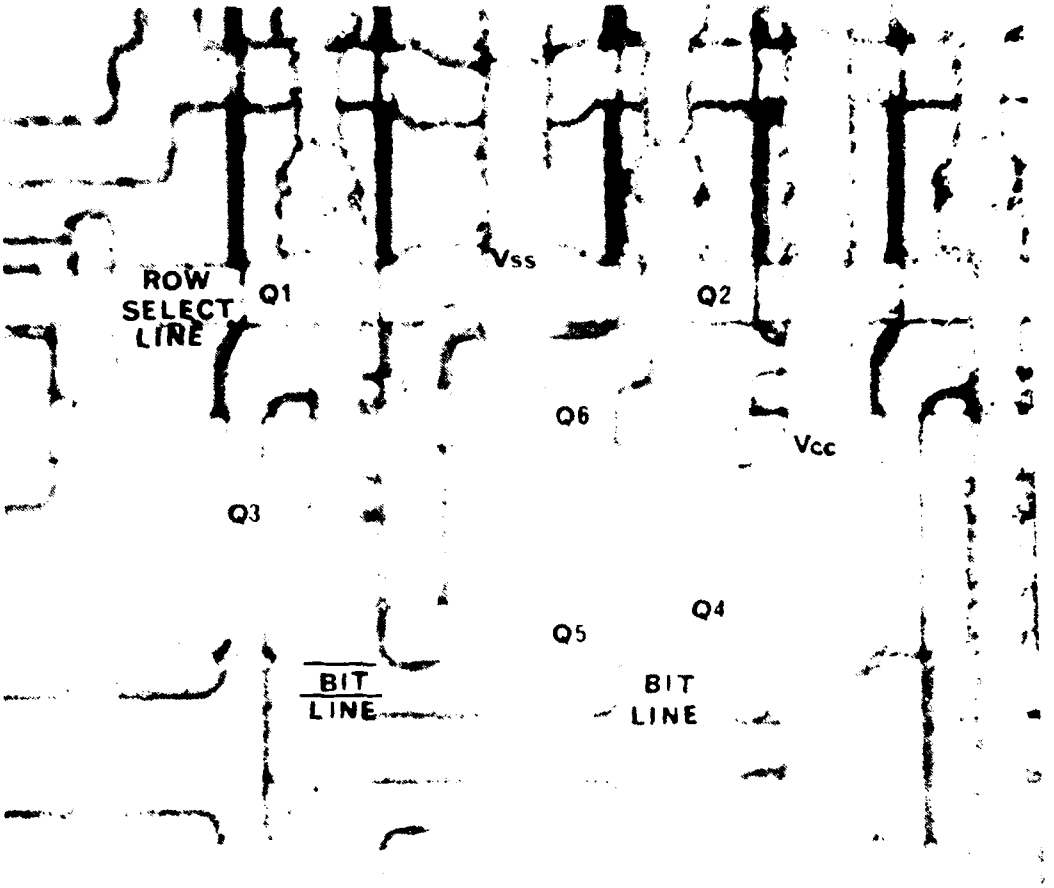


FIGURE A33. A10 AND A11 ADDRESS PADS ON THE AM9140

The Memory Cell consists of a bistable latch for the static storing of data. The cell is accessed through the row select line and data flow is along the bit lines. Figure A34 presents a typical memory cell. The bit and data line organization is presented in Figure A35. The Bit Line Latch, presented in Figure A36, aids the accessed cell in discharging the high capacitance load developed on the data and bit lines. Data flows along the data lines through the Sense Amplifier to the Output Buffer during a read cycle and through the Write Amplifier from the Input during a write cycle. The Sense and Write Amplifiers are presented in Figure A37. Both devices provide a Memory Status (MS) circuit which parallels the data flow circuits to supply accurate timing information of the device's operation. The Memory Status circuit is presented in Figure A38 with its Output Buffer in Figure A39. The capacitor network presented in Figure A40 is used by the Memory Status circuit to simulate the line capacitance of the bit lines. The area of this network for the AM9130 is twenty-five percent (25%) of that used by the AM9140, since each output of the AM9130 accesses 1/4 of the bit line capacitance of the AM9140.



2000X

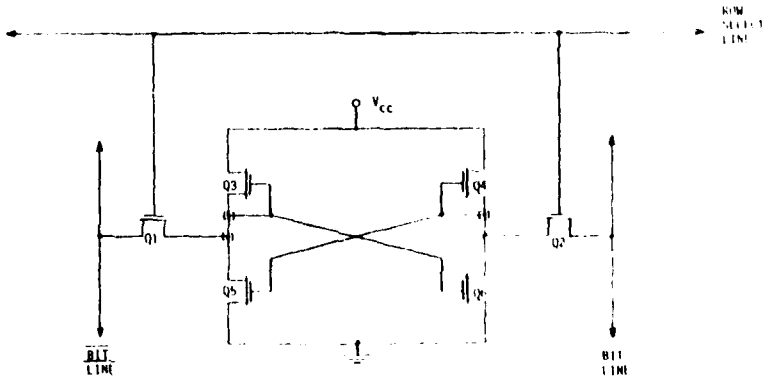
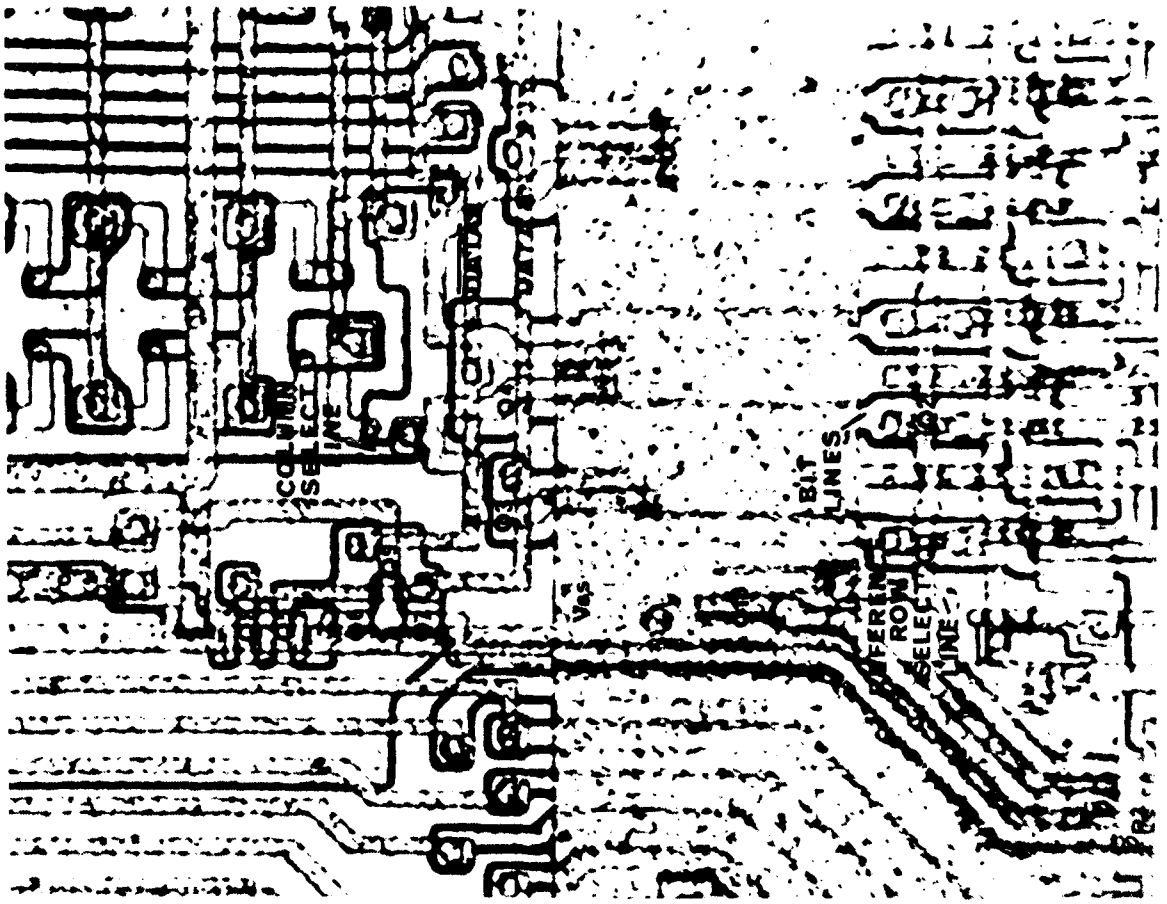


FIGURE A34. MEMORY CELL



510X

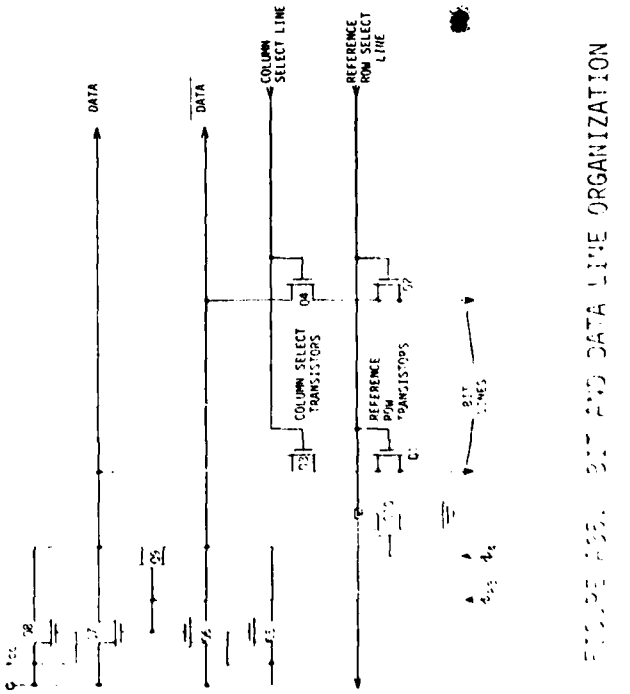


FIGURE A15. BIT AND DATA LINE ORGANIZATION

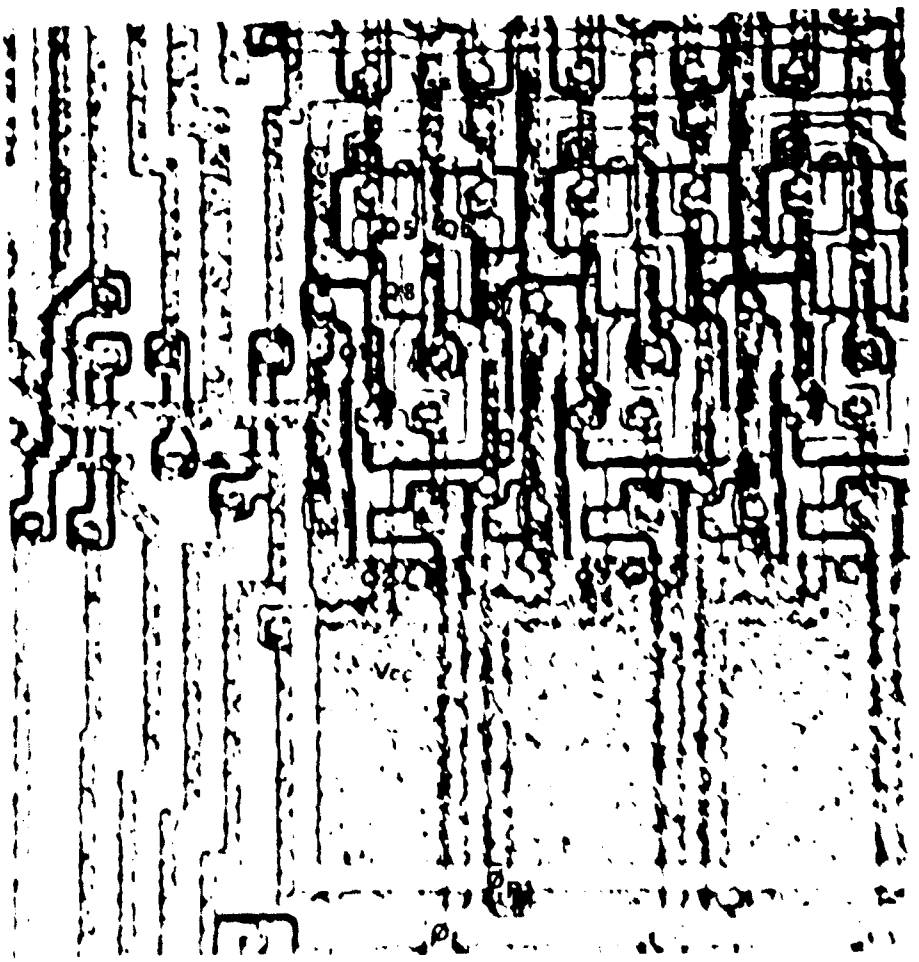
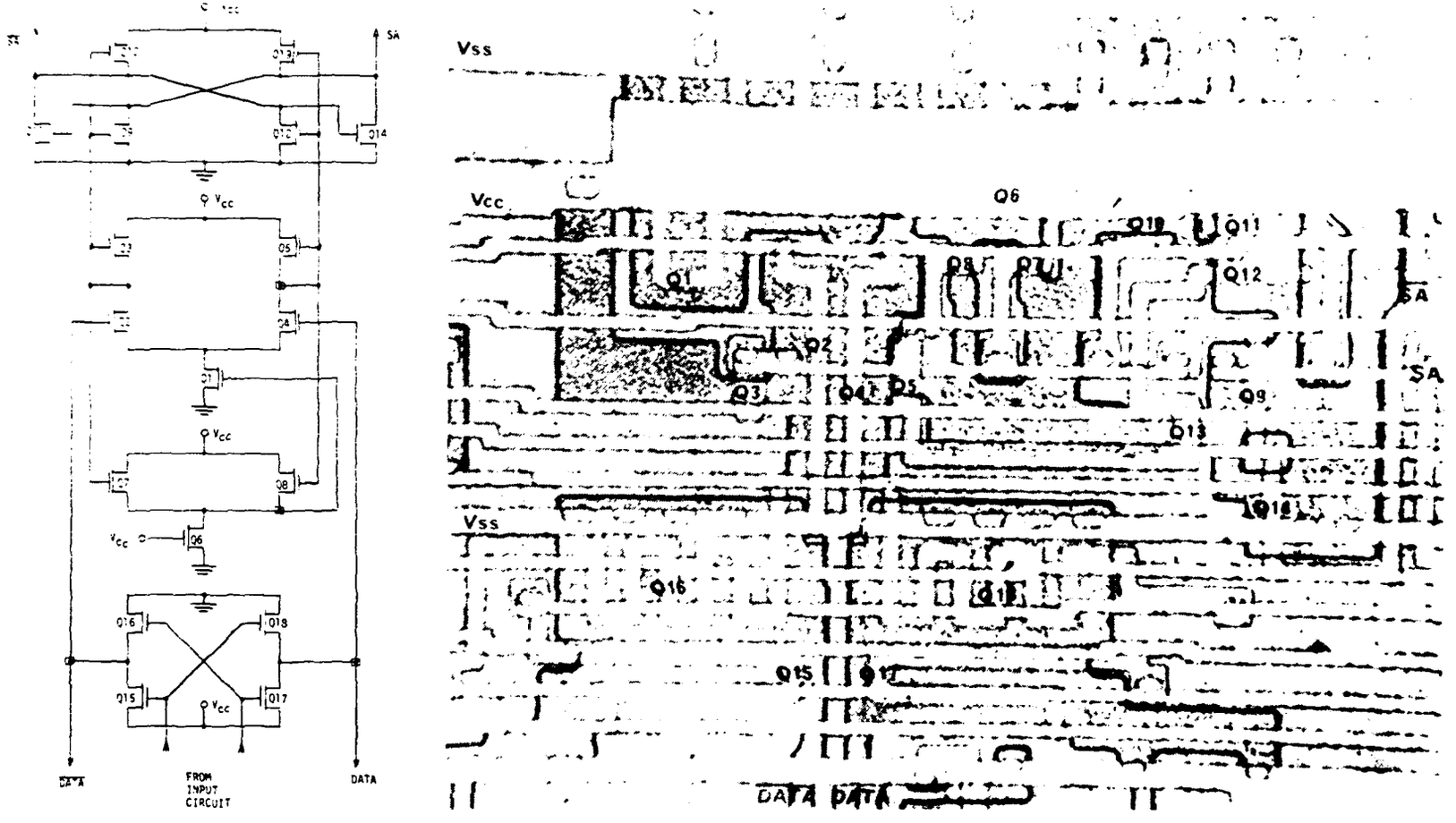
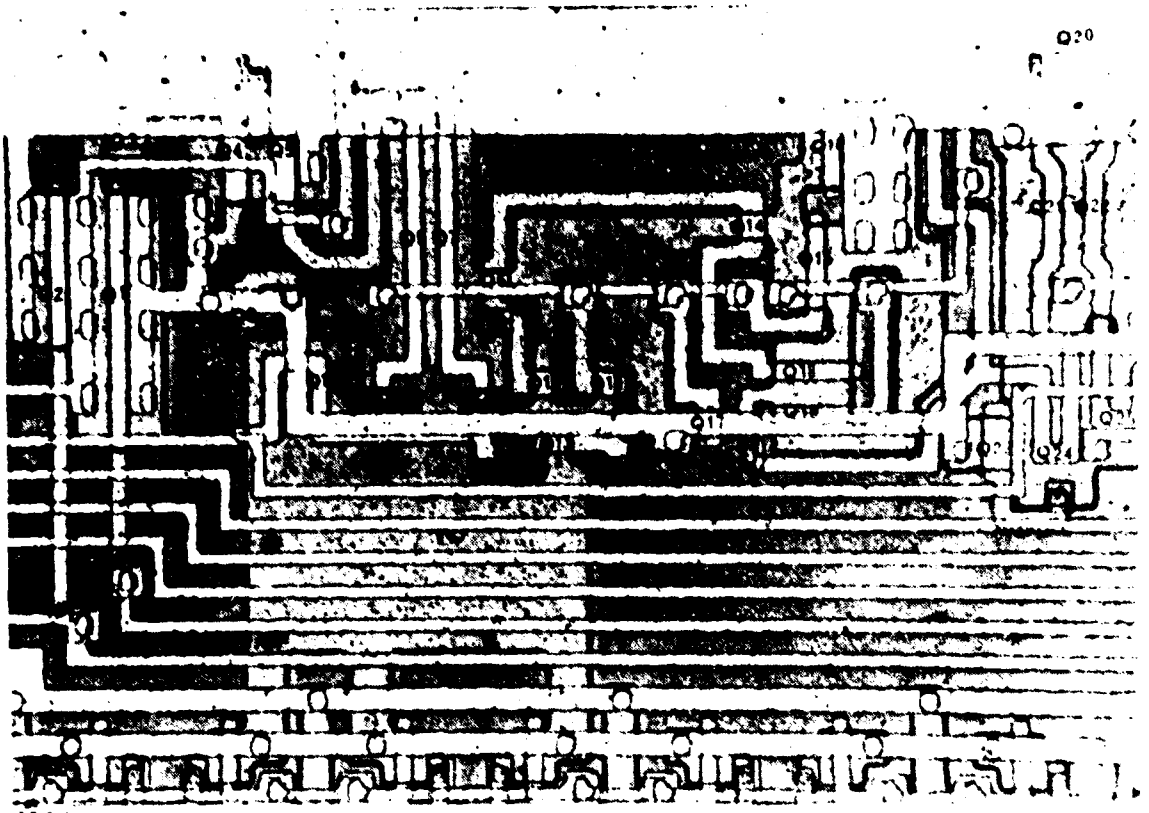


FIGURE A36. BIT LINE LATCH



540X

FIGURE A37. SENSE AND WRITE AMPLIFIERS



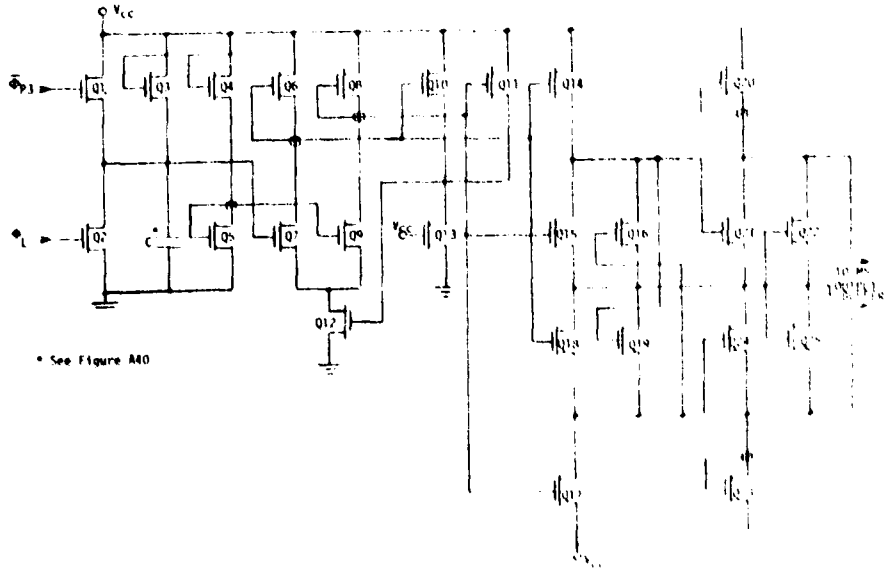
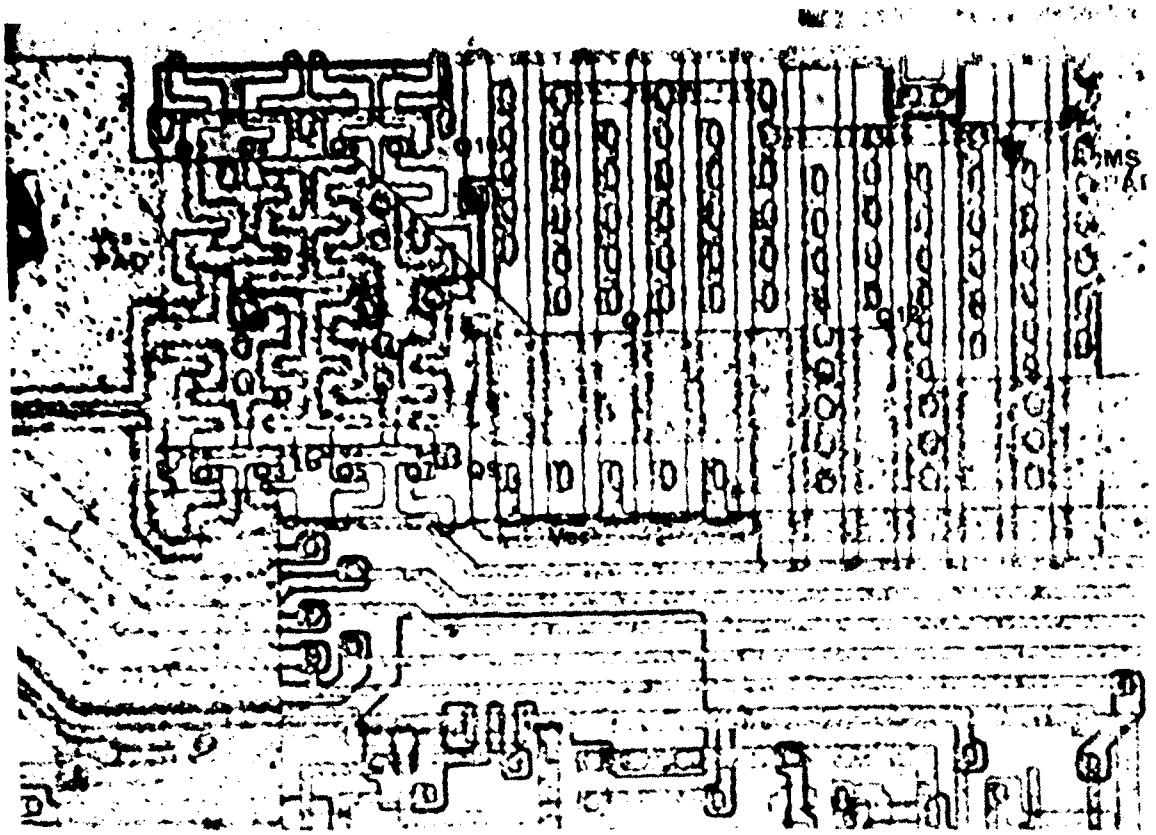


FIGURE A38. MEMORY STATUS CIRCUIT



380X

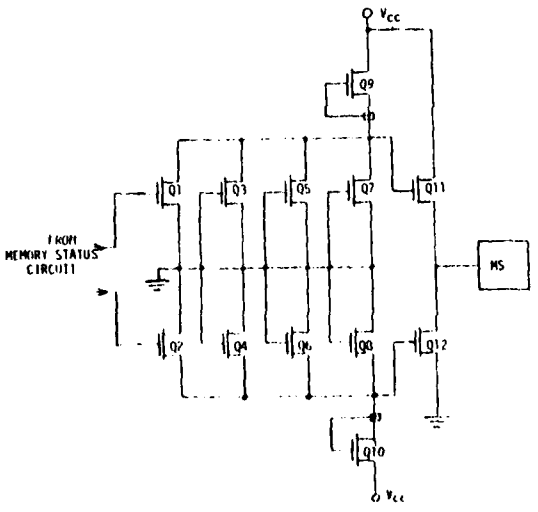
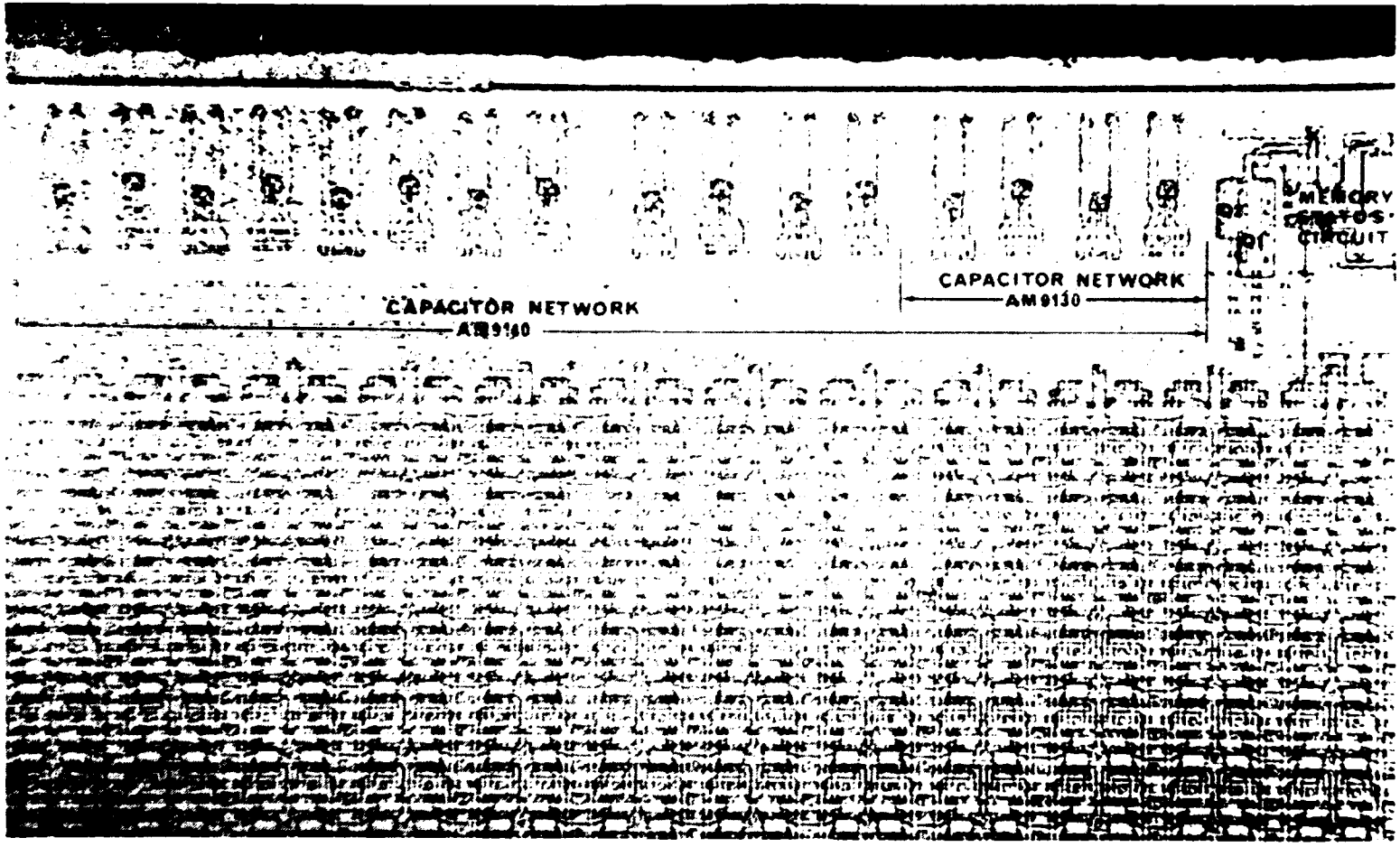


FIGURE A39. MEMORY STATUS OUTPUT BUFFER



180X

FIGURE A40. MEMORY STATUS CAPACITOR NETWORK

5.0 CONCLUSIONS

Internal visual examination of the devices studied revealed no feature that may limit life test temperatures. The uneven eutectic coverage discovered through x-ray examination, though in compliance with MIL-STD-883B, will impede heat conduction from die to package, and result in some devices operating with higher junction temperatures than others.

The test probe marks on the lead pads did not compromise the devices' bond strength. Bond integrity was confirmed through a bond pull test per MIL-STD-883B, Method 2011.2. In several cases the bond was displaced near the pad edge but away from where metal exited the pad. The alignment window in each pad isolated the bond from the active input protection circuitry near the bond pad.

The circuit schematics of the AM9130 and AM9140 are in agreement with the MIL-M-38510 logic diagrams. For the internal timing control network, several clock signals are simulataneously generated in response to the Chip Enable signal. These signals (Φ', Φ'', etc.) are not all identified in the initial draft of the MIL-M-38510/237 logic diagrams for both part types.

APPENDIX B

ELECTRICAL TEST CONDITIONS

APPENDIX B

This appendix is included to supply various details for the electrical test conditions of the AM9130 and AM9140 devices. Presented in Figures B1, B2 and B3 are the timing requirements of the AM9130 for the read, write and read/modify/write cycles, respectively. Similarly, presented in Figures B4, B5 and B6 are the timing requirements of the AM9140 for the read, write and read/modify/write cycles. Switching time test circuits for the AM9130 and AM9140 are presented in Figures B7 and B8. Tables B1 and B2 show the Group A inspection electrical tests for the AM9130 and AM9140 devices per the initial draft of MIL-M-38510/237. Table B3 provides a list of the symbols and their definitions that are applicable for these devices. Table B4 lists the functional algorithms provided by the manufacturer for the initial draft of MIL-M-38510/237. Table B5 lists the functional algorithms used in the Reliability Evaluation and Electrical Characterization of Memories Program for the AM9140 device. The functional algorithm of an additional pattern used during failure analysis is presented in Table B6.

Read cycle test conditions over operating range (notes 7, 8, and 9).

Parameter	Description	Min	Max	Unit
$t_{C(rd)}$	Read Cycle Time (Note 5)	770		ns
$t_{a(CE)}$	Access Time (Note 3) (CE to Output Valid Delay)		500	ns
$t_{W(CEH)}$	Chip Enable HIGH Time (Note 14)	500		ns
$t_{W(CEL)}$	Chip Enable LOW Time (Note 14)	250		ns
$t_{h(\overline{CS})}$	Chip Enable to Chip Select Hold Time	250		ns
$t_{h(ad)}$	Chip Enable to Address Hold Time	220		ns
$t_{SU(\overline{CS})}$	Chip Select to CE Set-up Time (Note 4)	-5		ns
$t_{SU(ad)}$	Address to Chip Enable Set-Up Time	0		ns
$t_{SU(rd)}$	Read to Chip Enable Set-Up Time	0		ns
$t_{h(rd)}$	Chip Enable to Read Hold Time	0		ns
t_{OH}	Chip Enable to Output OFF Delay (Note 3)	0		ns
t_{CF}	OE or OD to Output OFF Delay (Note 11)		200	ns
t_{CO}	OE or OD to Output ON Delay (Note 11)		220	ns
$t_{SU(OE)}$	Output Enable to CE LOW Set-Up Time (Note 12)	90		ns
t_{DM}	Data Out to Memory Status Delay	0		ns
t_P	Internal Preset Interval (Note 14)		$t_{W(CEL)}$	ns

Read cycle timing definitions.

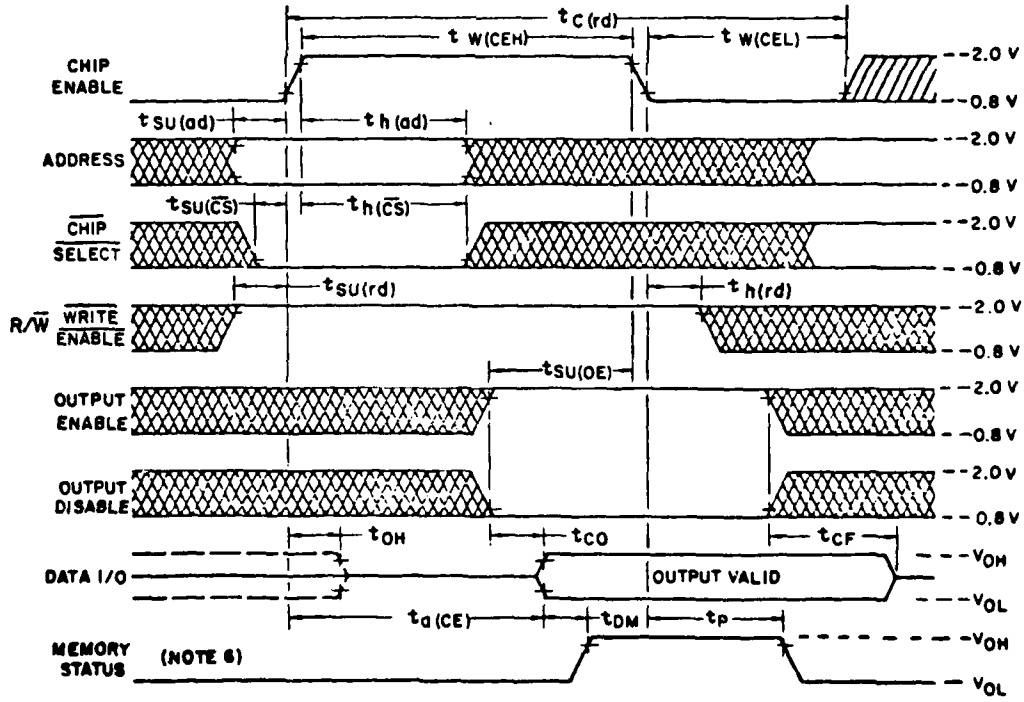


FIGURE B1. READ CYCLE WAVEFORMS AND TEST CONDITIONS FOR AM9130

Write cycle test conditions over operating range (notes 7, 8, and 9).

Parameter	Description	Min	Max	Unit
$t_{C(wr)}$	Write Cycle Time (Note 5)	770		ns
$t_{a(CE)}$	Access Time (CE to Output [+] Delay)		500	ns
$t_{W(CEH)}$	Chip Enable HIGH Time (Notes 14, 15)	550		ns
$t_{W(CEL)}$	Chip Enable LOW Time (Notes 14, 15)	250		ns
$t_{SU(ad)}$	Address to Chip Enable Set-Up Time	0		ns
$t_{h(ad)}$	Chip Enable to Address Hold Time	200		ns
$t_{SU(\overline{CS})}$	Chip Select to CE Set-Up Time (Note 4)	-5		ns
$t_{h(\overline{CS})}$	Chip Enable to Chip Select Hold Time	200		ns
$t_{W(wr)}$	Write Pulse Width (Note 10)	200		ns
$t_{SU(da)}$	Data Input Set-Up Time (Note 10)	220		ns
$t_{h(da)}$	Data Input Hold Time (Note 10)	0		ns
t_{DM}	Data Out to Memory Status Delay	0		ns
t_p	Internal Preset Interval		$t_{a(CE)}$	ns

Write cycle timing (definitions)

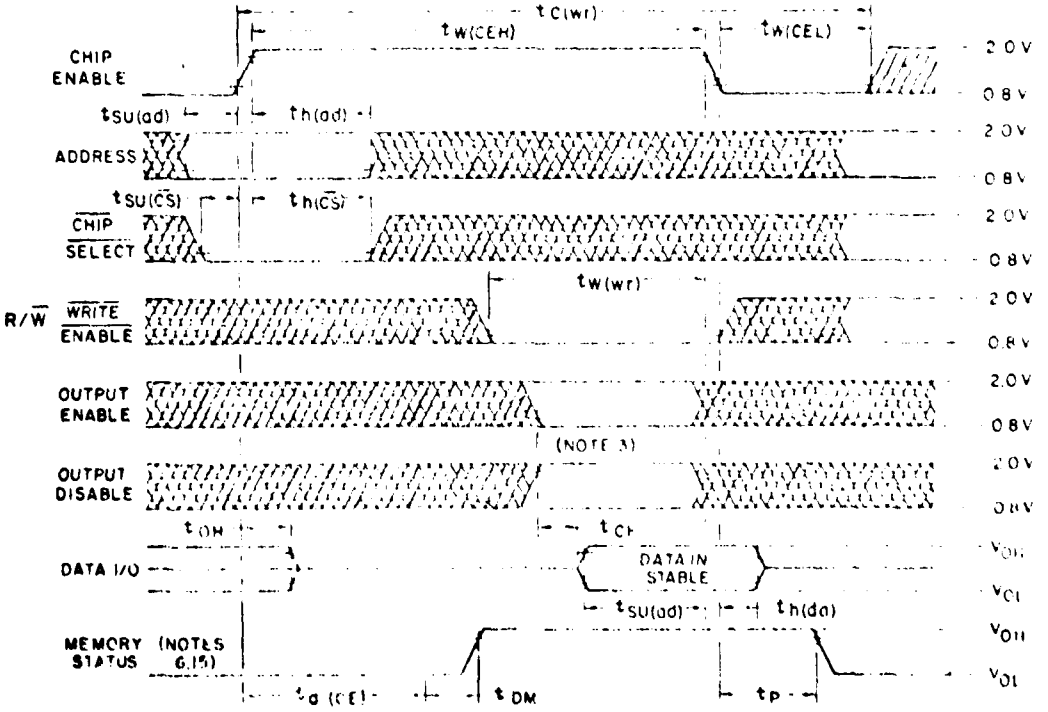


FIGURE 12. WRITE CYCLE WAVEFORMS AND TEST CONDITIONS FOR AM9130

Read/modify/write cycle test conditions over operating range (notes 7, 8, and 9).

Parameter	Description	Min	Max	Unit
$t_{C(RMW)}$	R/M/W Cycle Time (Notes 5, 16)	1,170		ns
$t_{a(CE)}$	Access Time (CE to Output Valid Delay)		500	ns
$t_{W(CEH)}$	Chip Enable HIGH Time (Notes 14, 15)	900		ns
$t_{W(CEL)}$	Chip Enable LOW Time (Notes 14, 15)	250		ns
$t_{h(\overline{CS})}$	Chip Enable to Chip Select Hold Time	200		ns
$t_{h(ad)}$	Chip Enable to Address Hold Time	200		ns
$t_{SU(\overline{CS})}$	Chip Select to CE Set-Up Time (Note 4)	-5		ns
$t_{SU(ad)}$	Address to Chip Enable Set-Up Time	0		ns
$t_{SU(rd)}$	Read to Chip Enable Set-Up Time	0		ns
t_{OH}	Chip Enable to Output OFF Delay	0		ns
$t_{h(da)}$	Data Input Hold Time (Note 10)	0		ns
$t_{SU(da)}$	Data Input Set-Up Time (Note 10)	200		ns
$t_{W(wr)}$	Write Pulse Width (Note 10)	200		ns
t_{CF}	OE or OD to Output OFF Delay (Note 11)		200	ns
t_{CO}	OE or OD to Output ON Delay (Note 11)		220	ns
t_{DV}	Data Valid after Write Delay	10		ns
$t_{h(rd)}$	Read Mode Hold Time	tA		ns
t_{DM}	Data Out to Memory Status	0		ns
t_P	Internal Preset Interval		$t_{W(CEL)}$	ns

Read/modify/write cycle timing definitions.

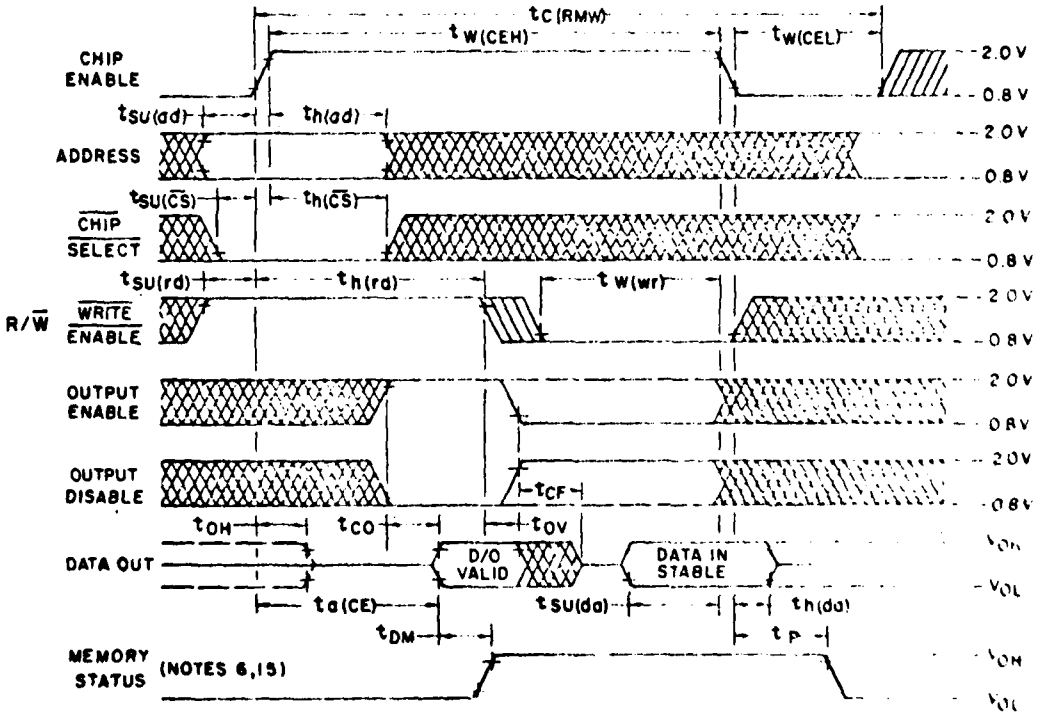


FIGURE B3. READ/MODIFY/WRITE CYCLE WAVEFORMS AND TEST CONDITIONS FOR AM9130

Read cycle test conditions over operating range (notes 7, 8, and 9).

Parameter	Description	Min	Max	Unit
$t_{C(rd)}$	Read Cycle Time (Note 5)	770		ns
$t_{a(CE)}$	Access Time (Note 3) (CE to Output Valid Delay)		500	ns
$t_{W(CEH)}$	Chip Enable HIGH Time (Note 14)	500		ns
$t_{W(CEL)}$	Chip Enable LOW Time (Note 14)	250		ns
$t_{h(\overline{CS})}$	Chip Enable to Chip Select Hold Time	200		ns
$t_{h(ad)}$	Chip Enable to Address Hold Time	200		ns
$t_{SU(\overline{CS})}$	Chip Select to CE Set-Up Time (Note 4)	-5		ns
$t_{SU(ad)}$	Address to Chip Enable Set-Up Time	0		ns
$t_{SU(rd)}$	Read to Chip Enable Set-Up Time	0		ns
$t_{h(rd)}$	Chip Enable to Read Hold Time	0		ns
t_{OD}	Chip Enable to Output OFF Delay (Note 3)	0		ns
t_{CF}	OE or OD to Output OFF Delay (Note 11)		200	ns
t_{CO}	OE or OD to Output ON Delay (Note 11)		220	ns
$t_{SU(OE)}$	Output Enable to CE LOW Set-Up Time (Note 12)	90		ns
t_{DM}	Data Out to Memory Status Delay	0		ns
t_p	Internal Preset Interval (Note 14)		$t_{W(CEL)}$	ns

Read cycle timing definitions

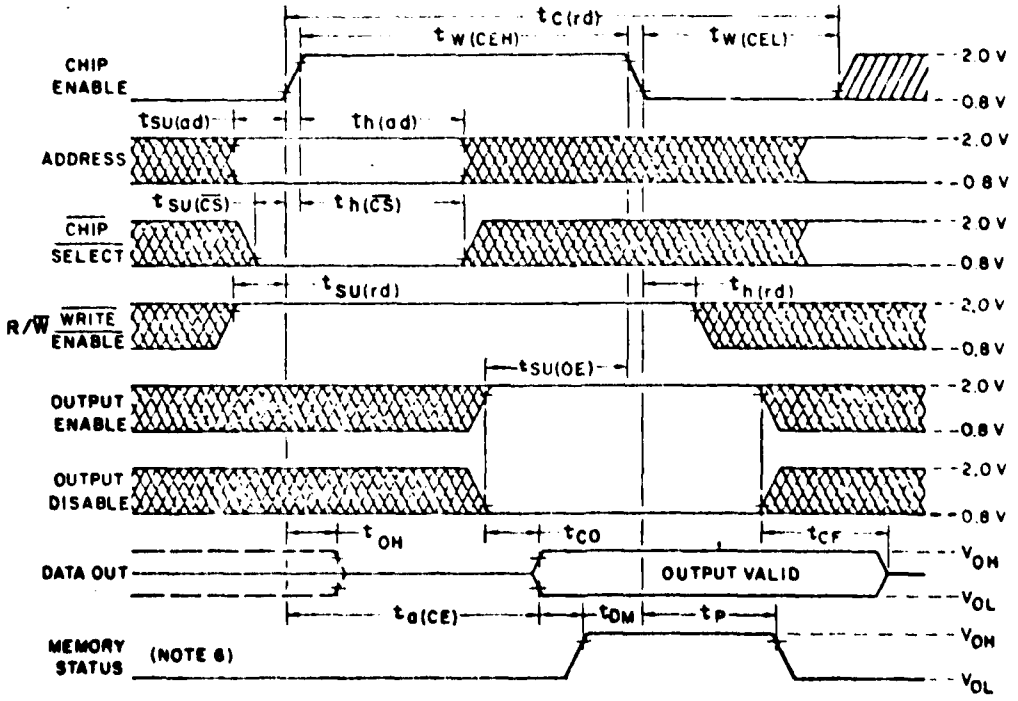


FIGURE B4. READ CYCLE WAVEFORMS AND TEST CONDITIONS FOR AM9140

Write cycle test conditions over operating range (notes 7, 8, and 9).

Parameter	Description	Min	Max	Unit
$t_{C(wr)}$	Write Cycle Time (Note 5)	770		ns
$t_{a(CE)}$	Access Time ($\overline{CE}$ to Output ON Delay)		500	ns
$t_{W(CEH)}$	Chip Enable HIGH Time (Notes 14, 15)	500		ns
$t_{W(CEL)}$	Chip Enable LOW Time (Notes 14, 15)	250		ns
$t_{SU(ad)}$	Address to Chip Enable Set-Up Time	0		ns
$t_{h(ad)}$	Chip Enable to Address Hold Time	200		ns
$t_{SU(\overline{CS})}$	Chip Select to $\overline{CE}$ Set-Up Time (Note 4)	-5		ns
$t_{h(\overline{CS})}$	Chip Enable to Chip Select Hold Time	200		ns
$t_{W(wr)}$	Write Pulse Width (Note 10)	200		ns
$t_{SU(da)}$	Data Input Set-Up Time (Note 10)	200		ns
$t_{h(da)}$	Data Input Hold Time (Note 10)	0		ns
t_{DM}	Data Out to Memory Status Delay	0		ns
t_P	Internal Preset Interval		$t_{W(CEL)}$	ns

Write cycle timing definitions.

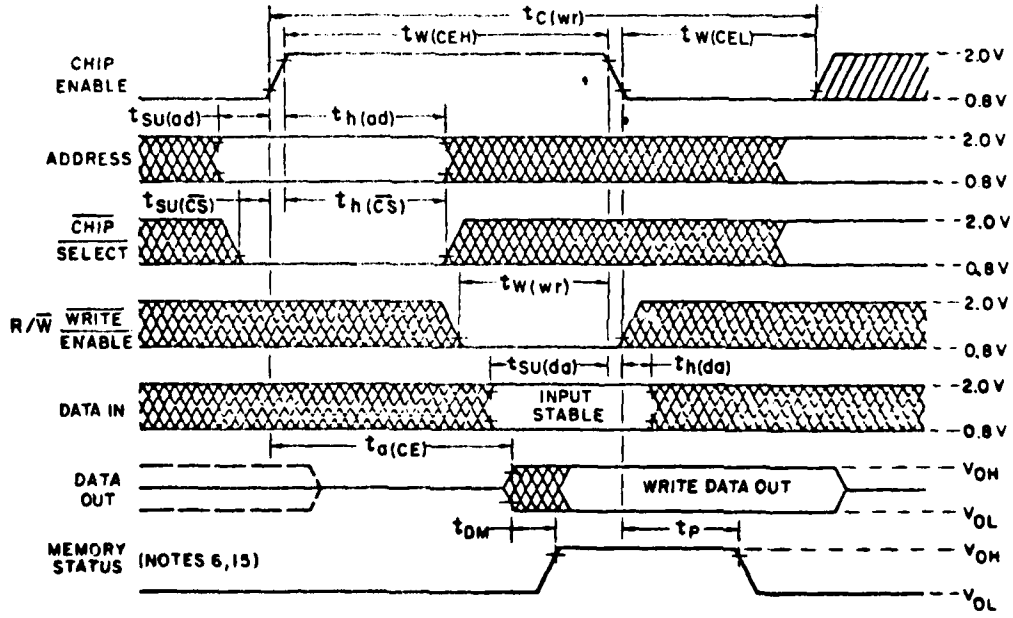


FIGURE B5. WRITE CYCLE WAVEFORMS AND TEST CONDITIONS FOR AM9140

Read/modify/write cycle test conditions over operating range (notes 7, 8, and 9)

Parameter	Description	Min	Max	Unit
$t_{C(RMW)}$	R/M/W Cycle Time (Notes 5, 16)	970		ns
$t_{a(CE)}$	Access Time (CE to Output Valid Delay)		550	ns
$t_{W(CEH)}$	Chip Enable HIGH Time (Notes 14, 15)	700		ns
$t_{W(CEL)}$	Chip Enable LOW Time (Notes 14, 15)	250		ns
$t_{h(\overline{CS})}$	Chip Enable to Chip Select Hold Time	200		ns
$t_{h(ad)}$	Chip Enable to Address Hold Time	200		ns
$t_{SU(\overline{CS})}$	Chip Select to CE Set-Up Time (Note 4)	-5		ns
$t_{SU(ad)}$	Address to Chip Enable Set-Up Time	0		ns
$t_{SU(rd)}$	Read to Chip Enable Set-up Time	0		ns
t_{OH}	Chip Enable to Output OFF Delay	0		ns
$t_{h(da)}$	Data Input Hold Time (Note 13)			ns
$t_{SU(da)}$	Data Input Set-Up Time (Note 10)	200		ns
$t_{W(wr)}$	Write Pulse Width (Note 10)	200		ns
t_{CF}	OE or $\overline{OD}$ to Output OFF Delay (Note 11)		200	ns
t_{CO}	OE or $\overline{OD}$ to Output ON Delay (Note 11)		200	ns
t_{DV}	Data Valid after Write Delay	10		ns
$t_{h(rd)}$	Read Mode Hold Time	10		ns
t_{DM}	Data Out to Memory Status	0		ns
t_p	Internal Preset Interval		$t_{W(CEL)}$	ns

Read/modify/write cycle timing definitions.

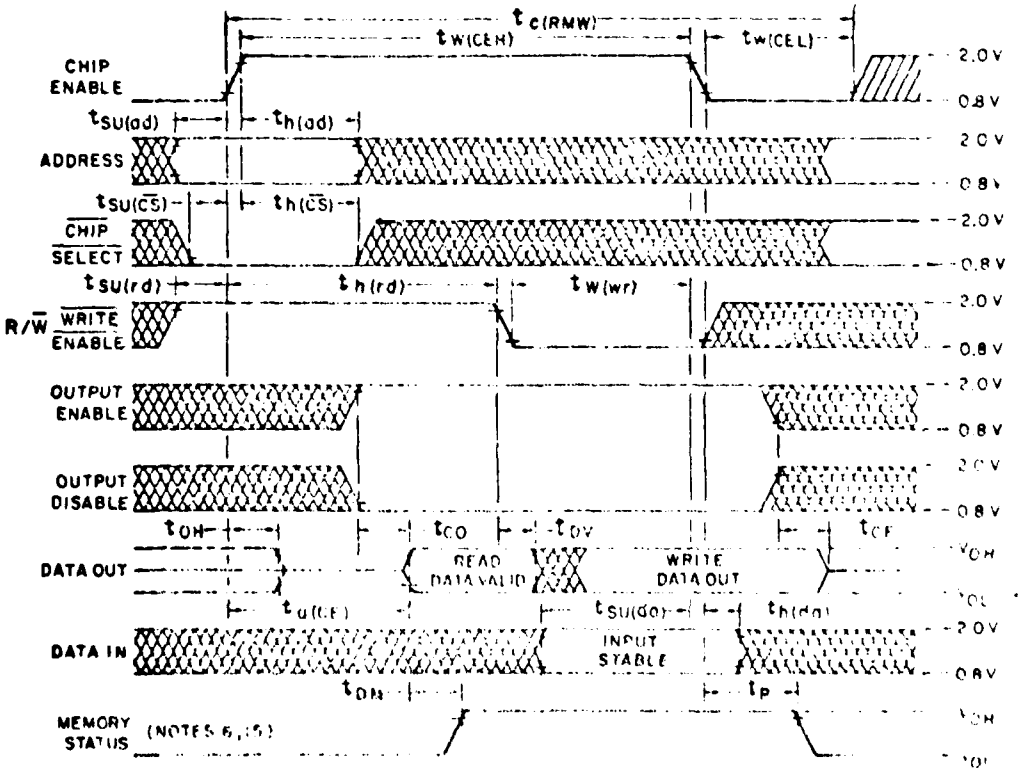


FIGURE B6. READ/MODIFY/WRITE CYCLE WAVEFORMS AND TEST CONDITIONS FOR A

NOTES FOR FIGURES B1 THROUGH B6

1. Typical operating supply current values are specified for nominal processing parameters, nominal supply voltage and the specific ambient temperature shown.

2. Typical power-down supply current values are specified for nominal processing parameters, the specific supply voltage shown and the specific ambient temperature shown.

3. At any operating temperature the minimum access time, $t_{a(CE)}$(min.), will be greater than the maximum CE to output OFF delay t_{OH}(max.).

4. The negative value shown indicates that the Chip Select input may become valid as late as 5.0 ns following the start of the Chip Enable rising edge.

5. The worst-case cycle times are the sum of CE rise time, $t_{w(CEH)}$, CE fall time and $t_{w(CEL)}$. The cycle time values shown include the worst-case $t_{w(CEH)}$ and $t_{w(CEL)}$ requirements and assume CE transition times of 10 ns.

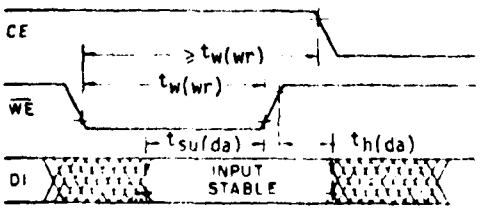
6. The Memory Status signal is a two-state output and is not affected by the Output Disable or Output Enable signals. If the output data buffers are turned off, Memory Status will continue to reflect the internal status of the memory.

7. Output loading is assumed to be one standard TTL gate plus 50 pF of capacitance. See load at lower right.

8. Timing reference levels for both input and output signals are 0.8V and 2.0V.

9. CE and $\overline{WE}$ transition times are assumed to be $\leq$ 10 ns.

10. The internal write time of the memory is defined by the overlap of CE high and $\overline{WE}$ low. Both signals must be present on a selected chip to initiate a write. Either signal can terminate a write. The $t_{w(wr)}$, $t_{su(da)}$ and $t_{h(da)}$ specifications should all be referenced to the end of the write time. The Write Cycle timing diagram shows termination by the falling edge of CE. If termination is defined by bringing $\overline{WE}$ high while CE is high, the following timing applies:

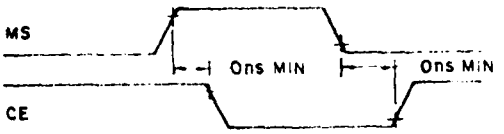


11. The output data buffer can be ON and output data valid only when Output Enable is high and Output Disable is low. OE and $\overline{OE}$ perform the same function with opposite control polarity.

12. The output data buffer should be enabled before the falling edge of CE in order to read output information. When the output is disabled and CE is low, the output data register is cleared.

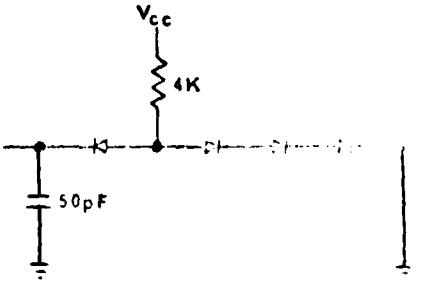
13. Input and output data are the same polarity.

14. The Chip Enable waveform requirements may be defined by the Memory Status output waveform. For a read cycle, the basic CE requirement is that $t_{w(CEH)} \geq t_{a(CE)}$ and $t_{w(CEL)} \geq t_p$:

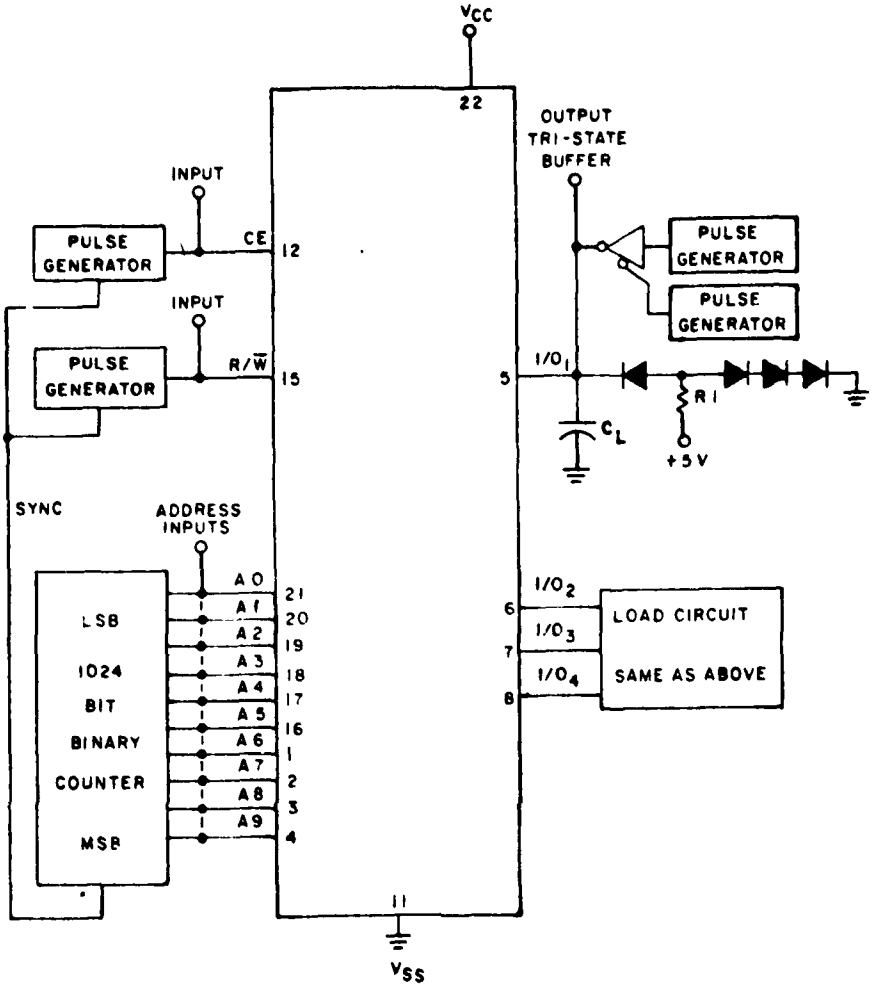


15. The Memory Status output functions as if all operations are read cycles. If a write cycle begins with $\overline{WE}$ low and Data In is stable at the time CE goes high, the rising edge of MS may be used as an indication that the write is complete and CE may be brought low. In a cycle where $\overline{WE}$ goes low at some point within the CE High time, the rising edge of MS should be ignored as an indication of write status. The falling edge of MS is always valid independent of the type of operation being performed.

16. For the R/M/W cycle $t_{w(CEH)}$(min.) is defined as $t_{h(rd)}$(min.) + $t_{w(wr)}$. Note 5 defines $t_{c(RMW)}$ but it may also be viewed as $t_{c(rd)}$ + $t_{w(wr)}$. Modify times are assumed to be zero. For systems with Data In and Data Out tied together R/M/W timing should make allowance for t_{CF} time so that no bus conflict occurs.

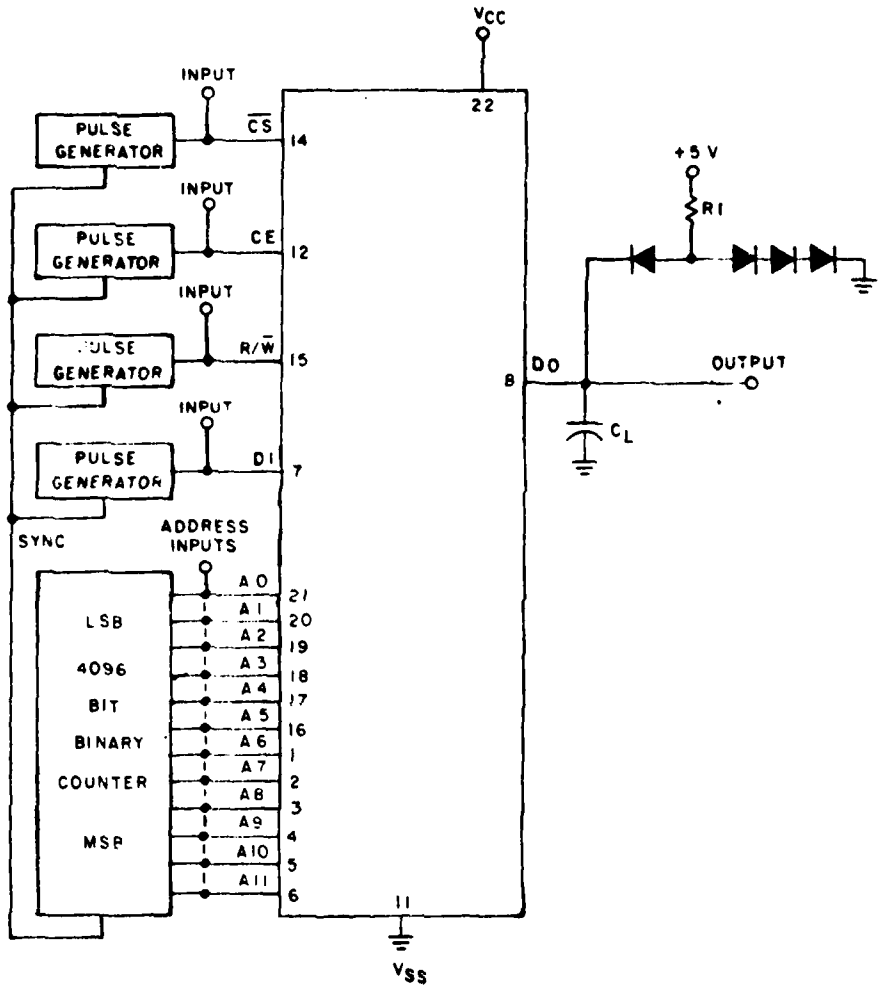


OUTPUT LOAD



NOTES:
A. C_L = 50 pF minimum, including probe and jig capacitance.
B. R_1 = 4 KΩ.
C. Address waveforms must be coherent to within ±5 ns of CE.
D. All t_{TLH} and $t_{THL} \leq 20$ ns.
E. All generator output impedance = 50Ω.
F. All diodes are 1N914 or equivalent.

FIGURE B7. SWITCHING TIME TEST CIRCUIT FOR AM9130



NOTES:

A. C_L = 50 pF minimum, including probe and jig capacitance.

B. R_1 = 4 KΩ.

C. Address waveforms must be coherent to within ±5 ns of CE.

D. All t_{TLH} and $t_{THL} \leq 20$ ns.

E. All generators output impedance = 50Ω.

F. All diodes are 1N914 or equivalent.

FIGURE B8. SWITCHING TIME TEST CIRCUIT FOR AM9140

TABLE B1. GROUP A INSPECTION FOR AM9130

TERMINAL CONDITIONS PINS NOT DESIGNATED MAY BE HIGH ≥2.0V OR LOW ≤0.8V OR OPEN.

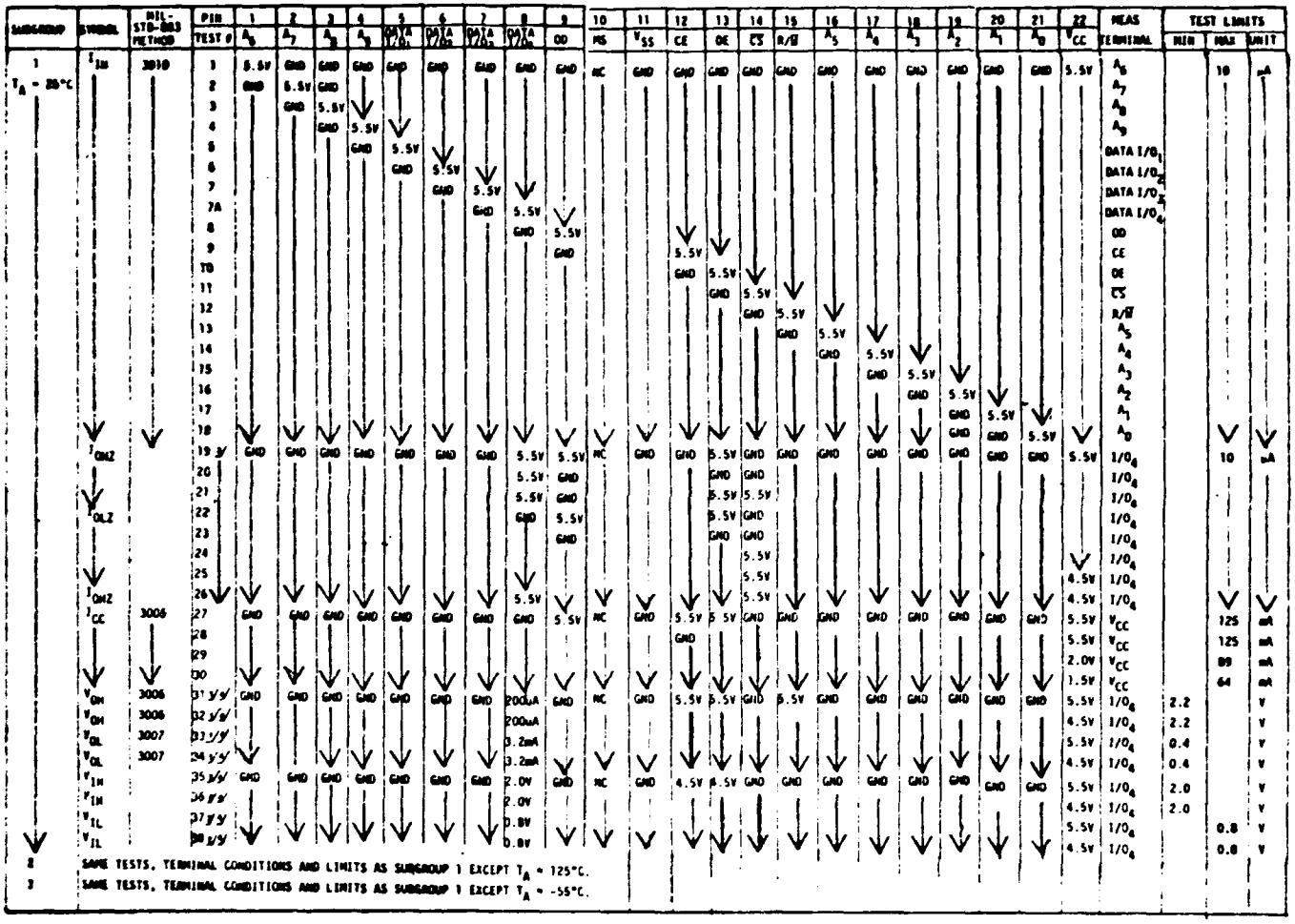


TABLE B1 (CONTINUED). GROUP A INSPECTION FOR AM9130

TERMINAL CONDITIONS PINS NOT DESIGNATED MAY BE HIGH ≥ 2.0V OR LOW ≤ 0.8V OR OPEN.

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	PIN TEST #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	ALGORITHMS 8/	MEAS TERMINAL	TEST LIMITS MIN	MAX	UNIT
				A_6	A_7	A_8	A_9	$DATA\ I/O_1$	$DATA\ I/O_2$	$DATA\ I/O_3$	$DATA\ I/O_4$	OD	MS	V_{SS}	CE	OE	$\overline{CS}$	R/$\overline{W}$	A_5	A_4	A_3	A_2	A_1	A_0	V_{CC}					
9	t_a (CE)		39	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	GND	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	4.5V	MARCH	I/O		500	ns
T_A = 25°C			40																						4.5V	GALDIA				
			41																						5.5V	MARCH				
			42																						5.5V	GALDIA				
			43																						4.5V	MARCH RMW				
			44																						5.5V	MARCH RMW				
		6/	45																						4.5V	CB STOP				
		6/	46																						4.5V	$\overline{CB}$ STOP	↓			
			47																						4.5V	SCAN 1	MS			
			48																						5.5V	SCAN 1	MS			
		7/	49																						1.5V	PWR DOWN CB	I/O			
↓	↓	7/	50	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	1.5V	PWR DOWN $\overline{CB}$	I/O		↓	↓
10	SAME TESTS, TERMINAL CONDITIONS AND LIMITS AS SUBGROUP 9 EXCEPT T_A = 125°C.																													
11	SAME TESTS, TERMINAL CONDITIONS AND LIMITS AS SUBGROUP 9 EXCEPT T_A = -55°C.																													

NOTES:

1. A "1" AND A "0" RESPECTIVELY ARE WRITTEN IN AND THEN READ BACK TO PERFORM THE V_{OH} AND V_{OL} MEASUREMENTS.
2. THESE PARAMETERS ARE LISTED HERE BUT ARE CHECKED FUNCTIONALLY IN THE DYNAMIC GO - NO/GO TEST.
3. THE I_{OHZ} AND I_{OLZ} TESTS ARE REPEATED FOR DATA I/O PINS 1 THROUGH 3 SEQUENTIALLY BY EXPOSING THE PINS TO BE TESTED TO THE IDENTICAL PARAMETERS SHOWN ON I/O_4.
4. IDENTICAL CONDITIONS ARE REPEATED FOR I/O 1 THROUGH 3, SEQUENTIALLY, AS I/O_4.
5. SEE ATTACHED TIMING DIAGRAM, FIGURES B1 , B2 AND B3 FOR WAVEFORMS AND AC PARAMETERS TESTED.
6. THE STOP TEST IS PERFORMED BY LOADING THE MEMORY WITH A CB OR $\overline{CB}$ PATTERN, WAITING 1 SECOND, AND READING THE DATA.
7. POWER DOWN IS DONE BY LOADING THE DEVICE @ 5.5V WITH A CB OR $\overline{CB}$ PATTERN, LOWERING V_{CC} TO 1.5V, RETURNING V_{CC} TO 5.5V AND VERIFYING CORRECT DATA.
8. SEE TABLE B3 FOR DESCRIPTIONS OF ALGORITHMS.

TABLE B2. GROUP A INSPECTION FOR AM9140

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	PIN TEST #	1 A_6	2 A_7	3 A_8	4 A_9	5 A_{10}	6 A_{11}	7 DI	8 DO	9 OD	10 MS	11 V_{SS}	12 CE	13 OE	14 $\overline{CS}$	15 R/$\overline{W}$	16 A_5	17 A_4	18 A_3	19 A_2	20 A_1	21 A_0	22 V_{CC}	MEAS TERMINAL	TEST LIMITS MIN	MAX	UNIT
1	I_{IH}	3010	1	5.5V	GND	GND	GND	GND	GND	GND	NC	GND	NC	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	5.5V	A_6		10	uA
T_A = 25°C			2	GND	5.5V	GND																				A_7			
			3		GND	5.5V																				A_8			
			4			GND	5.5V																			A_9			
			5				GND	5.5V																		A_{10}			
			6					GND	5.5V																	A_{11}			
			7						GND	5.5V																DI			
			8							GND		5.5V			5.5V											OD			
			9									GND			GND	5.5V										CE			
			10													GND	5.5V									OE			
			11														GND	5.5V								$\overline{CS}$			
			12															GND	5.5V							R/$\overline{W}$			
			13																GND	5.5V						A_5			
			14																	GND	5.5V					A_4			
			15																		GND	5.5V				A_3			
			16																			GND	5.5V			A_2			
			17																				GND	5.5V		A_1			
			18																					GND	5.5V	A_0		10	uA
	I_{OHZ}		19	GND	GND	GND	GND	GND	GND	GND	5.5V	5.5V	NC	GND	GND	5.5V	GND	GND	GND	GND	GND	GND	GND	GND	5.5V	DO			
			20								5.5V	GND				GND													
	I_{OLZ}		21								5.5V	GND				5.5V													
			22								GND	5.5V				5.5V													
	I_{OHZ}		23								GND	GND				GND													
			24								GND														4.5V				
			25								GND														4.5V				
			26								5.5V														4.5V				
	I_{CC}	3005	27	GND	GND	GND	GND	GND	GND	NC	GND	5.5V	NC	GND	5.5V	5.5V	GND	GND	GND	GND	GND	GND	GND	GND	5.5V	V_{CC}		125	mA
			28												GND										5.5V			125	
			29																						2.0V			89	
			30																						1.5V			64	
	V_{OH}	3006	31 1/							5.5V	-200uA	GND	NC	GND	5.5V	5.5V	GND	5.5V							5.5V	DO	2.2		V
	V_{OH}	3006	32 1/							5.5V	-200uA														4.5V		2.2		
	V_{OL}	3007	33 1/							GND	3.2mA														5.5V		0.4		
	V_{OL}	3007	34 1/							GND	3.2mA														4.5V		0.4		
	V_{IH}		35 2/							2.0V	5.5V				4.5V	4.5V		GND							5.5V	DI	2.0		
	V_{IH}		36 2/							2.0V															4.5V		2.0		
	V_{IL}		37 2/							0.8V															5.5V			0.8	
	V_{IL}		38 2/							0.8V															4.5V			0.8	
2	SAME TESTS, TERMINAL CONDITIONS AND LIMITS AS SUBGROUP 1, EXCEPT T_A = 125°C.																												
3	SAME TESTS, TERMINAL CONDITIONS AND LIMITS AS SUBGROUP 1, EXCEPT T_A = -55°C.																												

TABLE B2 (CONTINUED). GROUP A INSPECTION FOR AM9140

TERMINAL CONDITIONS PINS NOT DESIGNATED MAY BE HIGH ≥2.0V OR LOW ≤0.8V OR OPEN.

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	PIN TEST #	1 A_6	2 A_7	3 A_8	4 A_9	5 A_{10}	6 A_{11}	7 DI	8 DO	9 OD	10 MS	11 V_{SS}	12 CE	13 OE	14 $\overline{CS}$	15 R/$\overline{W}$	16 A_5	17 A_4	18 A_3	19 A_2	20 A_1	21 A_0	22 V_{CC}	ALGORITHMS 6/	MEAS TERMINAL	TEST LIMITS MIN	MAX	UNIT
9	t_a(CE)		39	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	GND	3/	3/	3/	3/	3/	3/	3/	3/	3/	3/	4.5V	MARCH	DO		500	ns
T_A = 25°C	↓	↓	40	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	4.5V	GALDIA RMW	↓	↓	↓	↓
↓			41																						5.5V	MARCH				
			42																						5.5V	GALDIA RMW				
			43																						4.5V	MARCH RMW				
			44																						5.5V	MARCH RMW				
		4/	45																						4.5V	CB STOP				
		4/	46																						4.5V	$\overline{CB}$ STOP	↓			
			47																						4.5V	SCAN 1	MS			
			48																						5.5V	SCAN 1 1	MS			
		5/	49																						1.5V	PWR DN CB	DO			
↓	↓	5/	50	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	1.5V	PWR DN $\overline{CB}$	DO			
10	SAME TESTS, TERMINAL CONDITIONS AND LIMITS AS SUBGROUP 9, EXCEPT T_A = 125°C.																													
11	SAME TESTS, TERMINAL CONDITIONS AND LIMITS AS SUBGROUP 9, EXCEPT T_A = -55°C.																													

NOTES:

1. A "1" AND "0" RESPECTIVELY ARE WRITTEN IN AND THEN READ BACK TO PERFORM THE V_{OH} AND V_{OL} MEASUREMENTS.
2. THESE PARAMETERS ARE LISTED HERE BUT ARE CHECKED FUNCTIONALLY IN THE DYNAMIC GO-NO/GO TEST.
3. SEE ATTACHED TIMING DIAGRAM, FIGURES B4, B5 AND B6 FOR WAVEFORMS AND AC PARAMETERS TESTED.
4. THE STOP TEST IS PERFORMED BY LOADING THE MEMORY WITH A CB OR $\overline{CB}$ PATTERN, WAITING 1 SECOND, AND READING THE DATA.
5. POWER DOWN IS DONE BY LOADING THE DEVICE AT 5.5V WITH A CB OR $\overline{CB}$ PATTERN, LOWERING V_{CC} TO 1.5V, RETURNING V_{CC} TO 5.5V AND VERIFYING CORRECT DATA.
6. SEE TABLE B3 FOR DESCRIPTIONS OF ALGORITHMS.

TABLE B3. SYMBOLS AND DEFINITIONS

SYMBOL	DEFINITION
V_{CC}	Supply voltage
V_{SS}	Common or reference voltage mode
OE	Output enable, input
OD	Output disable, input
CE	Chip-enable, input
CS	Chip-select, input
DI	Data input
DO	Data output
A_0 thru A_{11}	Address input
R/W	Read or write input
I/O1 - I/O4	Data input output
I_{OHZ}	High-impedance-state output current
I_{OLZ}	High-impedance-state output current
I_{CC}	Supply current from V supply
V_{OH}	High level output voltage
V_{OL}	Low level output voltage
V_{IH}	High level input voltage
V_{IL}	Low level input voltage
MS	Memory status output
$t_{c(rd)}$	Read cycle time
t_w	Pulse width
t_{su}	Setup time
t_h	Hold time
t_a	Access time
wr	Write
CEH	Chip enable high
CEL	Chip enable low
ad	Address
da	Data
rd	Read
su	Setup
$t_{c(RMW)}$	Read modify write cycle time
$t_{su(ad)}$	Address to chip enable setup time
$t_{h(ad)}$	Chip enable to address hold time
$t_{su(CS)}$	Chip select to chip enable setup time
$t_{h(CS)}$	Chip enable to chip select hold time
$t_{su(rd)}$	Read to chip enable setup time
$t_{h(rd)}$	Chip enable to read hold time
t_{OH}	Chip enable to output OFF delay
$t_{su(da)}$	Data input setup time
$t_{h(da)}$	Data input hold time
$t_{w(wr)}$	Write pulse width
t_{CF}	OE or OD to output OFF delay
t_{CO}	OE or OD to output ON delay
t_p	Internal Preset Interval
$t_{w(CEH)}$	Chip enable HIGH time
$t_{w(CEL)}$	Chip enable LOW time
$t_{a(CE)}$	Access time (CE to output valid delay)
$t_{su(OE)}$	Output enable to CE low setup time
t_{DM}	Data out to Memory Status delay
$t_{c(wr)}$	Write cycle time
t_{DV}	Data valid after write delay

TABLE B4. MIL-M-38510/237 FUNCTIONAL ALGORITHMS

Functional algorithms are test patterns which define the exact sequence of test used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device.

ALGORITHM	DESCRIPTION
	AM9130
GALDIA (N^2)	A. Write "0" into all of the memory. B. Starting at location 0 write 1 to that location (1). C. Read 0 at the background location 1 +31 and then read 1 at the test word location 1. D. Repeat Step C diagonally (incrementing the background location by 31 every time). E. Write 0 to the test word location 1 and read 0 to check it. F. Repeat Steps B-E through all locations. GALDIA "1" is the same as GALDIA "0" with opposite data.
MARCH (N)	A. Write a background pattern of "0s" throughout memory. B. Incrementing from address 0 to address 1023, read a "0" and write a "1" into each cell. C. Incrementing from address 1023 to address 0, read a "1" and write a "0" into each cell. D. Repeat Steps B and C with a background pattern of "1s" throughout memory.
CB (N)	A. Write 0 and 1 alternately in the first or even row. B. Write 1 and 0 alternately in the second or odd row. C. Repeat Steps A and B through all rows. D. Read 0 and 1 alternately in the first or even row. E. Read 1 and 0 alternately in the second or odd row. F. Repeat Steps D and E through all rows. G. Repeat Steps A through F with complement data.
SCAN 1 (N)	A. Write a background of "1s" throughout memory. B. Read a "1" from each location in the memory starting at address 0 to address 1023.
	AM9140
GALDIA (N^2)	A. Write "0" into all of the memory. B. Starting at location 0 write 1 to that location (1). C. Read 0 at the background location 1 +63 and then read 1 at the test word location 1. D. Repeat Step C diagonally (incrementing the background location by 63 every time). E. Write 0 to the test word location 1 and read 0 to check it. F. Repeat Steps B-E through all locations. GALDIA "1" is the same as GALDIA "0" with opposite data.
MARCH (N)	A. Write a background pattern of "0s" throughout memory. B. Incrementing from address 0 to address 4095, read a "0" and write a "1" into each cell. C. Incrementing from address 4095 to address 0, read a "1" and write a "0" into each cell. D. Repeat Steps B and C with a background pattern of "1s" throughout memory.
CB (N)	A. Write 0 and 1 alternately in the first or even row. B. Write 1 and 0 alternately in the second or odd row. C. Repeat Steps A and B through all rows. D. Read 0 and 1 alternately in the first or even row. E. Read 1 and 0 alternately in the second or odd row. F. Repeat Steps D and E through all rows. G. Repeat Steps A through F with complement data.
SCAN 1 (N)	A. Write a background of "1s" throughout memory. B. Read a "1" from each location in the memory starting at address 0 to address 4095.

TABLE B5. FUNCTIONAL ALGORITHMS FOR THE RELIABILITY EVALUATION AND ELECTRICAL CHARACTERIZATION OF MEMORIES PROGRAM

ALGORITHM	DESCRIPTION
	AM9148
GALPAT (N^2)	A. Write a background pattern of "0s" throughout memory. B. Write a "1" (test bit) at the first location. C. Read location in sequence - read location 2, read test bit, read location 3, read test bit. Read in sequence until every location is read with test bit location. D. Move the test bit to second location and repeat the sequence in step C. E. Repeat the sequence until each cell is used as test bit location.
GALWRT (N^2)	A. Write a background pattern of "0s" throughout memory. B. Write a "1" into the background cell and read a "1" from the test bit cell. C. Repeat the sequence with the same test bit cell but the next background cell. Continue until entire memory is sequence. D. Move test bit to next location and start sequence again. E. Repeat sequence until each cell is used as test bit location.
WALKING (N^2)	A. Write a background pattern of "0s" throughout memory. B. Write a "1" at the first cell (test bit). C. Read the entire memory. D. Complement the "1" at the first cell and write a "1" into cell 2 (new test bit). E. Read the entire memory. F. Repeat the sequence until each cell is used as test bit location. G. Repeat steps B through F with a background pattern of "1s" throughout memory.
ROWPAT ($N^{3/2}$)	A. Write a background pattern of "0s" for the first row. B. Write a "1" at the first location (test bit). C. Read location in sequence - read location 2, read test bit, read location 3, read test bit. Read until all 64 locations in row is checked with the test bit. D. Move the test bit to second location and repeat the sequence in step C. E. Repeat the sequence until each cell in the first row is used as test bit location. F. Increment until all rows are completed. G. Repeat steps B through F with a background pattern of "1s" throughout memory.
MARCH (N)	A. Write a background pattern of "0s" throughout memory. B. Incrementing from address 0 to address 4095, read a "0" and write a "1" into each cell. C. Incrementing from address 4095 to address 0, read an "1" and write an "0" into each cell. D. Repeat steps B and C with a background pattern of "1s" throughout memory.
SHIFTING DIAGONAL (N)	A. Write a background of "0s" with a diagonal stripe of "1s". B. Read the pattern incrementing the address by one each time. C. Shift the stripe right one time. D. Read out the pattern incrementing the address by one each time. E. Repeat steps B through D until the stripe has been shifted 64 times and the pattern read out each time. F. Repeat steps B through E with a background of "1s" with a diagonal stripe of "0s".
ADDCOMP (N)	A. Write an alternate pattern of "0s" and "1s" throughout memory. B. Verify each location by the address sequence - address, address complement, address, address + 1, etc. C. Read out data pattern from memory.

TABLE B6. FUNCTIONAL ALGORITHM USED DURING FAILURE ANALYSIS

COLWRT ($N^{3/2}$)

A. Write a background pattern of "0s" throughout the memory.
B. Set the address to zero. This becomes the first test bit.
C. Write a "1" into the test bit.
D. Read a "1" from the test bit.
E. Write a "0" into the background cells of the test bit's column alternating the writes with a read of a "1" from the test bit.
F. Increment the row address by one. This bit becomes the new test bit in the column.
G. Repeat steps C through F until all the cells in the column have been the test bit.
H. Increment the column address by one and repeat steps C through G.

APPENDIX C

PARAMETER CHARACTERIZATIONS

APPENDIX C
PARAMETER CHARACTERIZATIONS

Electrical parameter measurements were performed on all devices prior to the start of stress tests, during stress tests and at the conclusion of each stress test. The initial and final data at 25°C and 125°C was summarized in groups of devices defined by the various stress tests. These summaries are provided in Tables C1 through C12. The input/output leakage currents measured on the automated test system default to $\pm$ 50 nAdc as a minimum value. Therefore, for those parameters whose actual values lie between $\pm$ 50 nAdc, the computed mean ($\bar{x} \leq 50$ µAdc) and sigma ($\sigma = 0$) shown in the tables are not representative of the actual mean and sigma. No important parametric shifts indicating parameter degradation were observed from the initial data to the final data.

TABLE C1. AM9130 STATIC LIFE TEST PARAMETER CHARACTERIZATIONS AT 25°C

PARAMETER	MIL-M-38510/23704 TEST LIMITS		175°C STATIC LIFE				200°C STATIC LIFE				UNITS
			0 HR		4000 HR		0 HR		4000 HR		
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}		10	0.050	0.009	0.048	0.021	0.047	0.025	0.049	0.013	µAdc
I_{OHZ19}		10	0.048	0.019	0.050	0.000	0.050	0.000	0.050	0.000	µAdc
I_{OHZ21}		10	0.050	0.000	0.050	0.000	0.050	0.000	0.048	0.019	µAdc
I_{CC27}		125	87.800	7.882	88.000	8.112	89.500	7.029	89.500	7.053	mAdc
V_{OH32}	2.2		2.990	0.059	2.980	0.059	3.020	0.065	3.010	0.065	Vdc
V_{OL34}		0.4	0.162	0.014	0.160	0.014	0.162	0.015	0.160	0.015	Vdc
V_{CC} = 4.5 Vdc READ/WRITE t_{MS}, SCAN 1		500	161.000	8.858	165.000	8.535	159.000	11.450	162.000	11.326	nS
READ/MODIFY/WRITE $t_{A(CE)}$, MARCH		500	166.000	9.417	169.000	9.509	164.000	11.780	166.000	11.659	nS

TABLE C2. AM9130 STATIC LIFE TEST PARAMETER CHARACTERIZATIONS AT 125°C

PARAMETER	MIL-M-38510/23704 TEST LIMITS		175°C STATIC LIFE				200°C STATIC LIFE				UNITS
			0 HR		4000 HR		0 HR		4000 HR		
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}		10	0.050	0.000	0.050	0.009	0.049	0.013	0.049	0.012	µAdc
I_{OHZ19}		10	0.048	0.019	0.050	0.000	0.050	0.000	0.050	0.000	µAdc
I_{OHZ21}		10	0.050	0.000	0.050	0.000	0.050	0.000	0.050	0.000	µAdc
I_{CC27}		125	67.800	9.496	65.400	5.814	66.900	5.044	67.400	4.715	mAdc
V_{OH32}	2.2		3.010	0.056	3.010	0.059	3.050	0.065	3.040	0.065	Vdc
V_{OL34}		0.4	0.211	0.020	0.215	0.016	0.215	0.018	0.211	0.017	Vdc
V_{CC} = 4.5 Vdc READ/WRITE t_{MS}, SCAN 1		500	185.000	14.170	191.000	10.294	184.000	14.070	186.000	13.399	nS
READ/MODIFY/WRITE $t_{A(CE)}$, MARCH		500	190.000	14.800	194.000	10.960	189.000	15.000	191.000	13.798	nS

TABLE C3. AM9130 DYNAMIC LIFE TEST PARAMETER CHARACTERIZATIONS AT 25°C

PARAMETER	MIL-M-38510/23704 TEST LIMITS		175°C DYNAMIC LIFE				200°C DYNAMIC LIFE				UNITS
			0 HR		4000 HR		0 HR		4000 HR		
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}		10	0.050	0.000	0.050	0.000	0.047	0.027	0.049	0.012	µAdc
I_{OHZ19}		10	0.047	0.026	0.050	0.000	0.045	0.039	0.050	0.000	µAdc
I_{OHZ21}		10	0.050	0.000	0.050	0.000	0.047	0.026	0.050	0.000	µAdc
I_{CC27}		125	85.100	5.577	85.100	5.672	86.100	4.362	85.200	4.331	mAdc
V_{OH32}	2.2		3.010	0.069	3.010	0.069	3.020	0.072	3.020	0.074	Vdc
V_{OL34}		0.4	0.160	0.014	0.158	0.014	0.159	0.015	0.158	0.014	Vdc
V_{CC} = 4.5 Vdc READ/WRITE t_{MS}, SCAN 1		500	162.000	11.710	165.000	11.329	160.000	11.220	163.000	11.700	nS
READ/MODIFY/WRITE $t_{A(CE)}$, MARCH		500	166.000	12.590	168.000	12.674	165.000	12.060	168.000	12.611	nS

TABLE C4. AM9130 DYNAMIC LIFE TEST PARAMETER CHARACTERIZATIONS AT 125°C

PARAMETER	MIL-M-38510/23704 TEST LIMITS		175°C DYNAMIC LIFE				200°C DYNAMIC LIFE				UNITS
			0 HR		4000 HR		0 HR		4000 HR		
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}		10	0.051	0.018	0.051	0.018	0.050	0.000	0.049	0.009	µAdc
I_{OHZ19}		10	0.055	0.039	0.054	0.032	0.050	0.000	0.050	0.000	µAdc
I_{OHZ21}		10	0.056	0.045	0.055	0.039	0.050	0.000	0.050	0.000	µAdc
I_{CC27}		125	64.400	4.599	64.300	4.608	63.900	3.270	64.500	4.975	mAdc
V_{OH32}	2.2		3.040	0.070	3.030	0.070	3.050	0.072	3.040	0.075	Vdc
V_{OL34}		0.4	0.212	0.016	0.209	0.017	0.215	0.016	0.209	0.017	Vdc
V_{CC} = 4.5 Vdc READ/WRITE t_{MS}, SCAN 1		500	187.000	13.560	190.000	14.033	186.000	12.390	189.000	13.421	nS
READ/MODIFY/WRITE $t_{A(CE)}$, MARCH		500	191.000	14.500	193.000	14.880	191.000	12.870	193.000	14.050	nS

TABLE C5. AM9130 STORAGE LIFE TEST AND TEMPERATURE CYCLING PARAMETER CHARACTERIZATIONS AT 25°C

PARAMETER	MIL-M-38510/23704 TEST LIMITS		275°C STORAGE LIFE				-65/150°C TEMPERATURE CYCLING				UNITS
			0 HR		2000 HR		0 CYC		200 CYC		
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}		10	0.048	0.022	0.050	0.000	0.049	0.015	0.050	0.000	uAdc
I_{OHZ19}		10	0.050	0.000	0.050	0.000	0.050	0.013	0.056	0.034	uAdc
I_{OHZ21}		10	0.050	0.000	0.050	0.000	0.046	0.024	0.061	0.021	uAdc
I_{CC27}		125	85.600	4.603	90.600	4.636	90.100	6.955	89.900	6.927	mAdc
V_{OH32}	2.2		3.010	0.055	3.020	0.055	3.010	0.063	3.008	0.063	Vdc
V_{OL34}		0.4	0.160	0.014	0.166	0.016	0.164	0.014	0.164	0.014	Vdc
V_{CC} = 4.5 Vdc READ/WRITE											
t_{HS}, SCAN 1		500	161.000	8.012	161.000	7.828	160.000	9.273	161.000	9.904	nS
READ/MODIFY/WRITE											
$t_{A(CE)}$, MARCH		500	166.000	7.851	167.000	8.092	165.000	10.360	166.000	10.550	nS

TABLE C6. AM9130 STORAGE LIFE TEST AND TEMPERATURE CYCLING PARAMETER CHARACTERIZATIONS AT 125°C

PARAMETER	MIL-M-38510/23704 TEST LIMITS		275°C STORAGE LIFE				-65/150°C TEMPERATURE CYCLING				UNITS
			0 HR		2000 HR		0 CYC		200 CYC		
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}		10	0.049	0.015	0.050	0.000	0.047	0.021	0.050	0.000	uAdc
I_{OHZ19}		10	0.050	0.000	0.050	0.000	0.050	0.000	0.058	0.033	uAdc
I_{OHZ21}		10	0.050	0.000	0.045	0.032	0.050	0.000	0.061	0.021	uAdc
I_{CC27}		125	64.400	3.180	70.200	4.692	68.000	4.910	67.600	4.960	mAdc
V_{OH32}	2.2		3.040	0.054	3.043	0.054	3.040	0.062	3.008	0.063	Vdc
V_{OL34}		0.4	0.213	0.016	0.217	0.016	0.217	0.016	0.164	0.014	Vdc
V_{CC} = 4.5 Vdc READ/WRITE											
t_{HS}, SCAN 1		500	186.000	9.376	186.000	10.257	184.000	11.520	185.000	11.308	nS
READ/MODIFY/WRITE											
$t_{A(CE)}$, MARCH		500	191.000	8.699	193.000	10.549	189.000	12.380	190.000	12.437	nS

TABLE C7. AM9140 STATIC LIFE TEST PARAMETER CHARACTERIZATIONS AT 25°C

PARAMETER	MIL-M-38510/23712 TEST LIMITS		175°C STATIC LIFE				200°C STATIC LIFE				UNITS
			0 HR		4000 HR		0 HR		4000 HR		
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}		10	0.051	0.005	0.050	0.000	0.051	0.007	0.050	0.000	µAdc
I_{OHZ19}		10	0.050	0.000	0.050	0.000	0.070	0.056	0.050	0.000	µAdc
I_{OHZ21}		10	0.050	0.000	0.050	0.000	0.050	0.000	0.050	0.000	µAdc
I_{CC27}		125	77.800	4.589	76.929	4.420	78.200	5.628	76.321	5.079	mAdc
V_{OH32}	2.2		2.950	0.004	2.954	0.000	2.950	0.101	2.904	0.095	Vdc
V_{OL34}		0.4	0.153	0.008	0.149	0.009	0.144	0.013	0.146	0.013	Vdc
V_{CC} = 4.5 Vdc											
READ/WRITE											
t_{WS}, SCAN 1		500	191.000	22.110	188.000	22.449	183.000	21.110	186.000	18.768	nS
READ/MODIFY/WRITE											
$t_{A(CE)}$, MARCH		500	176.000	20.430	172.000	20.690	168.000	18.860	170.000	18.945	nS

TABLE C8. AM9140 STATIC LIFE TEST PARAMETER CHARACTERIZATIONS AT 125°C

PARAMETER	MIL-M-38510/23712 TEST LIMITS		175°C STATIC LIFE				200°C STATIC LIFE				UNITS
			0 HR		4000 HR		0 HR		4000 HR		
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}		10	0.051	0.013	0.050	0.000	0.051	0.013	0.050	0.000	µAdc
I_{OHZ19}		10	0.050	0.000	0.050	0.000	0.050	0.000	0.050	0.000	µAdc
I_{OHZ21}		10	0.050	0.000	0.050	0.000	0.050	0.000	0.050	0.000	µAdc
I_{CC27}		125	63.300	3.664	61.964	4.026	60.400	4.032	61.357	3.855	mAdc
V_{OH32}	2.2		2.970	0.006	2.983	0.002	2.970	0.103	2.906	0.096	Vdc
V_{OL34}		0.4	0.194	0.012	0.194	0.014	0.196	0.017	0.188	0.017	Vdc
V_{CC} = 4.5 Vdc											
READ/WRITE											
t_{WS}, SCAN 1		500	206.000	24.210	220.000	26.769	213.000	23.860	220.000	20.784	nS
READ/MODIFY/WRITE											
$t_{A(CE)}$, MARCH		500	189.000	22.270	203.000	25.578	197.000	23.390	202.000	20.847	nS

TABLE C9. AM9140 DYNAMIC LIFE TEST PARAMETER CHARACTERIZATIONS AT 25°C

PARAMETER	MIL-M-38510/23712 TEST LIMITS		175°C DYNAMIC LIFE				200°C DYNAMIC LIFE				UNITS
			0 HR		4000 HR		0 HR		4000 HR		
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{1H}		10	0.051	0.009	0.050	0.000	0.051	0.007	0.050	0.000	µAdc
I_{OHZ19}		10	0.050	0.000	0.050	0.000	0.050	0.000	0.050	0.000	µAdc
I_{OHZ21}		10	0.050	0.000	0.050	0.000	0.050	0.000	0.050	0.000	µAdc
I_{CC27}		125	79.400	4.730	76.833	4.639	78.100	4.833	74.800	3.881	mAdc
V_{OH32}	2.2		2.960	0.075	2.962	0.076	2.960	0.166	2.943	0.168	Vdc
V_{OL34}		0.4	0.147	0.010	0.160	0.009	0.146	0.016	0.134	0.015	Vdc
V_{CC} = 4.5 Vdc											
READ/WRITE											
t_{HS}, SCAN 1		500	180.000	17.370	184.000	17.393	187.000	21.030	191.000	20.822	nS
READ/MODIFY/WRITE											
$t_{A(CE)}$, MARCH		500	166.000	15.300	171.000	14.932	173.000	18.070	178.000	18.389	nS

TABLE C10. AM9140 DYNAMIC LIFE TEST PARAMETER CHARACTERIZATIONS AT 125°C

PARAMETER	MIL-M-38510/23712 TEST LIMITS		175°C DYNAMIC LIFE				200°C DYNAMIC LIFE				UNITS
			0 HR		4000 HR		0 HR		4000 HR		
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{1H}		10	0.050	0.006	0.060	0.022	0.050	0.003	0.050	0.000	µAdc
I_{OHZ19}		10	0.050	0.000	0.060	0.015	0.050	0.000	0.050	0.000	µAdc
I_{OHZ21}		10	0.050	0.000	0.053	0.013	0.050	0.000	0.050	0.000	µAdc
I_{CC27}		125	67.000	5.609	60.700	3.741	62.800	3.750	60.333	3.358	mAdc
V_{OH32}	2.2		2.980	0.075	2.982	0.076	2.980	0.165	2.975	0.163	Vdc
V_{OL34}		0.4	0.182	0.017	0.199	0.013	0.187	0.022	0.193	0.023	Vdc
V_{CC} = 4.5 Vdc											
READ/WRITE											
t_{HS}, SCAN 1		500	183.000	17.890	221.000	21.774	207.000	24.030	223.000	22.089	nS
READ/MODIFY/WRITE											
$t_{A(CE)}$, MARCH		500	170.000	15.570	204.000	19.302	193.000	21.020	208.000	20.236	nS

TABLE C11. AM9140 STORAGE LIFE TEST AND TEMPERATURE CYCLING PARAMETER CHARACTERIZATIONS AT 25°C

PARAMETER	MIL-M-38510/23712 TEST LIMITS		275°C STORAGE LIFE				-65/150°C TEMPERATURE CYCLING				UNITS
			0 HR		2000 HR		0 CYC		200 CYC		
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}		10	0.051	0.010	0.050	0.000	0.051	0.007	0.050	0.000	µAdc
I_{OHZ19}		10	0.050	0.000	0.050	0.000	0.050	0.000	0.050	0.000	µAdc
I_{OHZ21}		10	0.050	0.000	0.050	0.000	0.050	0.000	0.050	0.000	µAdc
I_{CC27}		125	79.200	6.889	83.400	6.646	71.600	8.883	71.050	8.905	mAdc
V_{OH32}	2.2		2.950	0.127	2.960	0.127	2.930	0.143	2.936	0.143	Vdc
V_{OL34}		0.4	0.147	0.009	0.153	0.010	0.152	0.019	0.152	0.017	Vdc
V_{CC} = 4.5 Vdc READ/WRITE t_{HS}, SCAN 1		500	177.000	17.970	177.000	18.330	201.000	27.750	199.000	27.098	nS
READ/MODIFY/WRITE $t_{A(CE)}$, MARCH		500	165.000	16.470	166.000	16.800	184.000	24.770	184.000	23.640	nS

TABLE C12. AM9140 STORAGE LIFE TEST AND TEMPERATURE CYCLING PARAMETER CHARACTERIZATIONS AT 125°C

PARAMETER	MIL-M-38510/23712 TEST LIMITS		275°C STORAGE LIFE				-65/150°C TEMPERATURE CYCLING				UNITS
			0 HR		2000 HR		0 CYC		200 CYC		
	MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	MEAN	SIGMA	
I_{IH}		10	0.051	0.008	0.050	0.000	0.051	0.015	0.050	0.000	µAdc
I_{OHZ19}		10	0.050	0.000	0.050	0.000	0.050	0.000	0.050	0.000	µAdc
I_{OHZ21}		10	0.050	0.000	0.050	0.000	0.050	0.000	0.050	0.000	µAdc
I_{CC27}		125	63.900	4.110	71.150	6.570	57.100	7.081	55.400	6.445	mAdc
V_{OH32}	2.2		2.970	0.125	2.980	0.080	2.960	0.143	2.959	0.144	Vdc
V_{OL34}		0.4	0.189	0.019	0.194	0.014	0.199	0.024	0.205	0.025	Vdc
V_{CC} = 4.5 Vdc READ/WRITE t_{HS}, SCAN 1		500	200.000	20.020	193.000	19.699	223.000	31.260	227.000	31.028	nS
READ/MODIFY/WRITE $t_{A(CE)}$, MARCH		500	186.000	17.680	180.000	18.283	204.000	27.060	209.000	28.159	nS

APPENDIX D

FAILURE ANALYSIS

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FAILURE ANALYSIS

1.0 PROCEDURE

All parts that failed an electrical test during the program were analyzed to determine their failure mode, failure mechanism, and probable cause of failure. The general analysis procedure was as follows:

a) Each failure was confirmed via a separate bench test set-ups, a curve tracer test, or a retest on the automated test system.

b) Each failed part was examined using suitable diagnostic equipment such as a curve tracer to isolate the degradation to a specific element or junction to the extent possible via external measurements. If it was possible to isolate the degradation externally, the part was leak tested, delidded and the degraded component investigated to determine its failure mode and mechanism. If the degradation could not be isolated externally, the part was subjected to an unpowered bake and retested. Any part that recovered after baking was classified as a surface related failure and was leak tested, delidded, and examined, but no further attempt was made to identify the exact failure mode or mechanism. If the part did not recover after baking, it was leak tested, then delidded for trouble-shooting to isolate the failed component(s) for analysis.

2.0 SUMMARY

A summary of the analysis findings is presented in Table D1. The table contains a description of the failure symptoms and the analysis findings for each type of failure. In addition, it lists the quantity of failures, failure times, test conditions for each type of failure and a paragraph number reference to the related analysis report.

TABLE D1. AM9130 AND AM9140 FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS B. ANALYSIS FINDINGS	QUANTITY OF FAILURES AND TIME OF FAILURE				REPORT PARA. NO. APP. D
	AM9130	AM9140			
	DYNAMIC LIFE	STATIC LIFE		DYNAMIC LIFE	
	200°C	200°C	175°C	200°C	
A. I_{IL} AT PINS 3 AND 9 B. DEGRADED INPUT PROTECTION NETWORK DUE TO JUNCTION INSTABILITY CAUSED BY STATIC DISCHARGE			1@504 HRS		D2.1
A. V_{OH}[32], V_{OL}[34], $t_{a(CE)}$ B. SURFACE INSTABILITY	1@2000 HRS				D2.2
A. $t_{a(CE)}$ B. SURFACE INSTABILITY		1 @168 HRS 1[4]/@504 HRS 1[5]/@4000 HRS 1[4]/@4000 HRS	1[3]/@4000 HRS 2[4]/@4000 HRS	1[3]/@4000 HRS	D2.3
A. $t_{a(CE)}$ B. NOT DETERMINED				1[2]/@4000 HRS	D2.4
TOTAL NUMBER OF FAILED PARTS	1	4	4	2	

NOTES:

1/ ALSO FAILED AT -55°C AND +125°C
2/ ALSO FAILED AT -55°C
3/ FAILED ONLY AT -55°C AND +125°C
4/ FAILED ONLY AT +125°C
5/ FAILED AT -55°C ONLY

2.1 AM9140 I_{IH} FAILURE

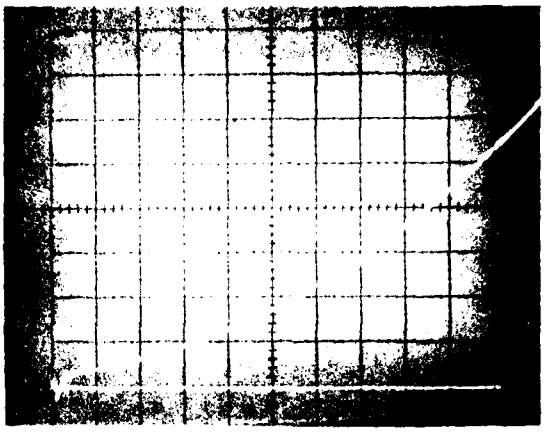
An AM9140, S/N 79, failed I_{IH} at pin 3 (ADDRESS 8) and at pin 9 (OUTPUT DISABLE) after 504 hours of static excitation life tests at 175°C. The part passed the 504 hour, 25°C parametric tests, failed I_{IH} at +125°C and -55°C, and then failed I_{IH} when retested at 25°C as shown in Table D2.

A curve tracer bench test of S/N 79 disclosed that I_{IH} at pin 3 was 31μA at the specified V_{INH} of 5.5 volts. The complete I_{IH} characteristic is shown in Figure D1. I_{IH} at pin 9 was 2200 μA at 5.5 volts and the complete I_{IH} characteristic is shown in Figure D2. The part was delidded for failure analysis. A photograph of the pin 9 input network is shown in Figure D3 and its electrical schematic is shown in Figure D4. For further clarification, a photograph of the pin 9 network of a sample part, after removal of the aluminum metallization to expose the diffused components, is presented in Figure D5. The aluminum interconnect between R2 and the input transistor of the output disable stage was severed open and I_{IH} of pin 9 was remeasured. I_{IH} (9) was unchanged indicating that the leakage was located in the protection network. No further isolation was possible because of the structure of the protection network, but the leakage was probably caused by degradation of the junction between the substrate and the n-type diffusion (N1) that composes R1, R2, the drain of Q1, and the drain of D1. The input network of pin 3, shown in Figure D6, was the same as that of pin 9 except that the pin 3 network contained a polysilicon gate capacitor (C1) between pin 3 and V_{SS} and that R2 was connected to the input transistor of the address stage via a polysilicon interconnect rather than an aluminum interconnect. Because the R2 diffusion was butted directly to the polysilicon interconnect, the address stage was not severed from the input protection network. C1 could be disconnected and was, but this did not change the leakage. Although it could not be definitely established, the failure mode of pin 3 was probably the same as that of pin 9.

S/N 79 was baked for 16 hours at 200°C and exposed to ultraviolet (U.V.) light for 15 minutes after which I_{IH} at pins 3 and 9 had completely recovered

TABLE D2. I_{IH} MEASUREMENTS AT 504 HOUR MEASUREMENT POINT

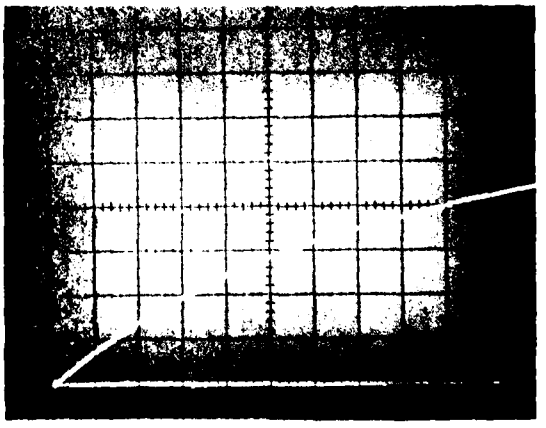
PARAMETER	TEST TEMPERATURE	MEASURED VALUE PIN 3	MEASURED VALUE PIN 9	SPECIFICATION LIMIT
I_{IH}	+25°C	<50 nA	<50 nA	10 µA
I_{IH}	+125°C	42 µA	>102 µA	10 µA
I_{IH}	-55°C	23 µA	>102 µA	10 µA
I_{IH}	+25°C RETEST	42 µA	>102 µA	10 µA



I_{IH} = 5 μA/DIV.

V_{IH} = 0.5 VOLT/DIV.

FIGURE D1. I_{IH} CHARACTERISTIC OF PIN 3 (A8) OF S/N 79



I_{IH} = 500 μA/DIV.

V_{IH} = 0.5 VOLT/DIV.

FIGURE D2. I_{IH} CHARACTERISTIC OF PIN 9 (OUTPUT DISABLE) OF S/N 79

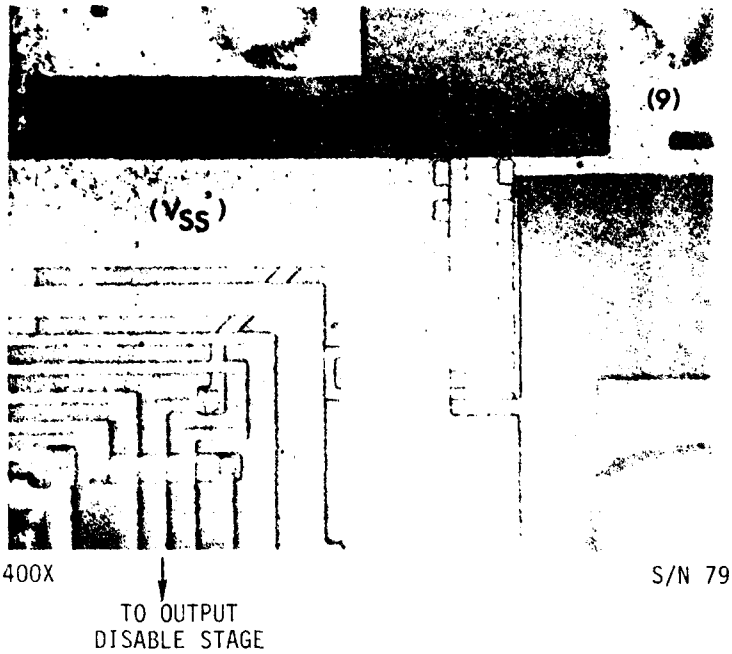


FIGURE D3. PIN 9 INPUT PROTECTION NETWORK

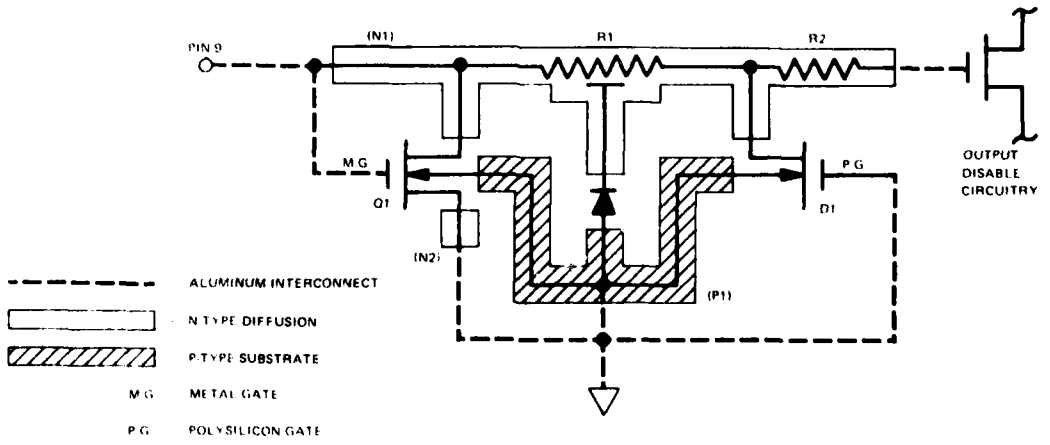
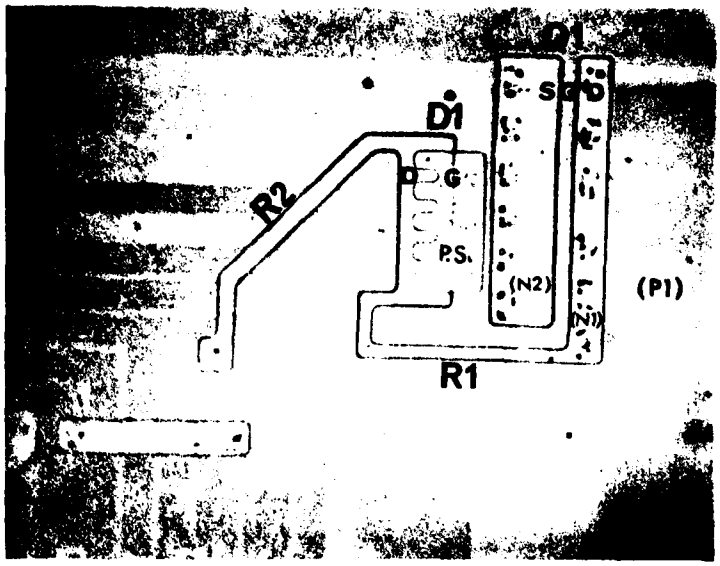
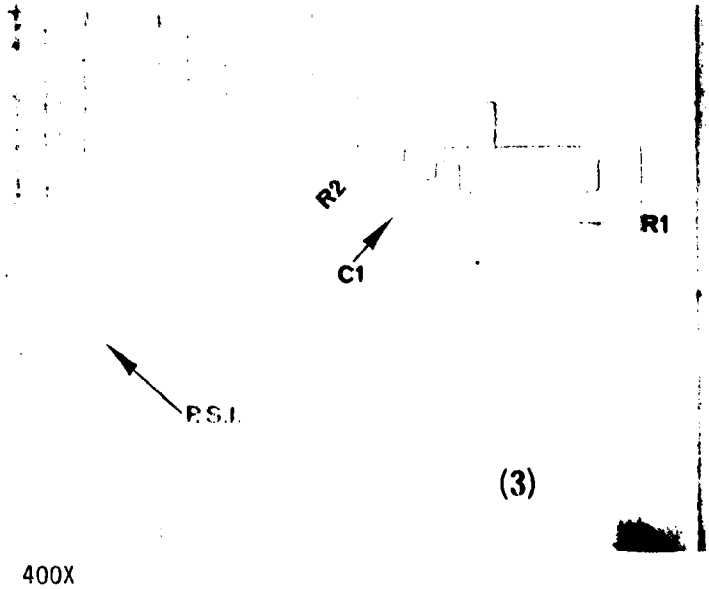


FIGURE D4. ELECTRICAL SCHEMATIC/LAYOUT DIAGRAM OF THE PIN 9 INPUT NETWORK



500X

FIGURE D5. PIN 9 INPUT PROTECTION NETWORK OF SAMPLE PART AFTER ALUMINUM REMOVAL



400X

FIGURE D6. PIN 3 INPUT PROTECTION NETWORK OF AM9140 S/N 79
(P.S.I. = POLYSILICON INTERCONNECT)

(< 50 nA). This indicated that the degradation was the result of a surface instability mechanism. During life test, pins 3 and 6 had been connected to V_{SS}. Thus, no bias had been applied across the input protection networks of pin 3 and pin 6. This plus the fact that I_{IH} was nominal at 25°C when first tested after 504 hours indicated that the instability was not induced by the life test. Apparently, the pin 3 and pin 9 input networks were degraded either by static charge generated during handling of the part between the first 25°C test and the +125°C test or by an electrical transient generated during the parametric tests. For reasons unknown the damage was not permanent and could be reversed.

2.2 AM9130 V_{OL}, V_{OH}, $t_{a(CE)}$ FAILURE

One AM9130, S/N 62, failed V_{OH32} at pin 5(output 1) and at pin 6 (output 2) and V_{OL34} at pin 6 at 25°C after 2000 hours of 200°C dynamic life test. The part also failed $t_{a(CE)}$ during all of the various MARCH, GALDIA, and CHECKERBOARD pattern tests at supply voltages of 4.5V and 5.5V. Also, the part failed all 16 V_{OL} and V_{OH} tests and all $t_{a(CE)}$ pattern tests at +125°C.

A curve tracer bench test verified the V_{OL} failure at pin 6 and the V_{OH} failure at pin 5. The output of pin 5 was low ("0") when it should have been high ("1") and the output of pin 6 was high ("1") when it should have been low ("0"). The output at pin 5 could be made to go high and the output at pin 6 could be made to go low by selecting an appropriate address other than that used for the V_{OL} and V_{OH} tests. This indicated that the problem was the result of improper logic delivered to the output stage rather than any degradation in the output transistors. The V_{OH} failure at pin 6 could not be confirmed and this indicated that the part had recovered partially.

A bench tester for the AM9130 and AM9140 devices was constructed in order to investigate voltage and pattern sensitivities and to create failed-bit maps. The bench tester utilizes a 6800 microprocessor-based computer to input signals and data to the device under test. Control signals also drive an address sequencer capable of automatic, external, or manual triggering. Test programs are stored via magnetic tape and all output, control, and address signals are monitored via both a logic analyzer and an oscilloscope. This test setup is shown in a block diagram in Figure D7.

Using a Read/Modify/Write pattern of alternating columns of "1's" and "0's", each address was analyzed and a failed-bit map created for the four outputs at the nominal supply voltage of 5.0 volts. This disclosed failures occurring at numerous addresses. For example, Figure D8 shows the four outputs at address 1700_8 during a sequence of output enable pulses. Note that after writing a "0" to output 2, a "1" incorrectly appears at output 2 and that after writing a "1" to output 4, a "0" incorrectly appears at

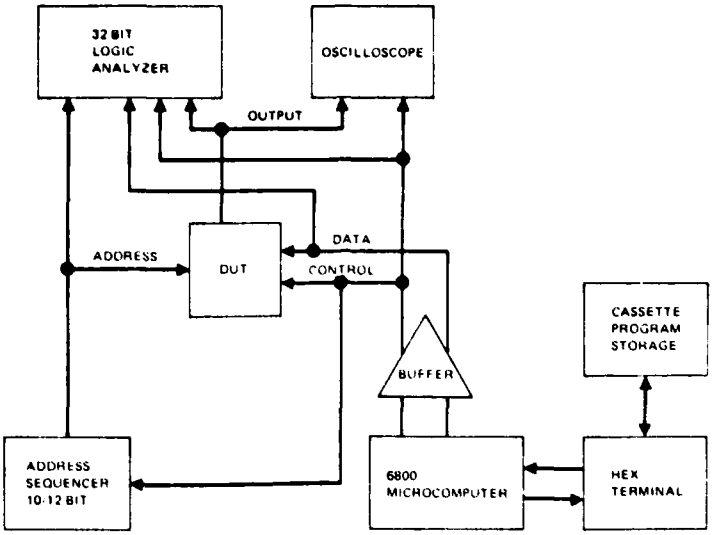


FIGURE D7. MEMORY EXERCISER AND OUTPUT DISPLAY

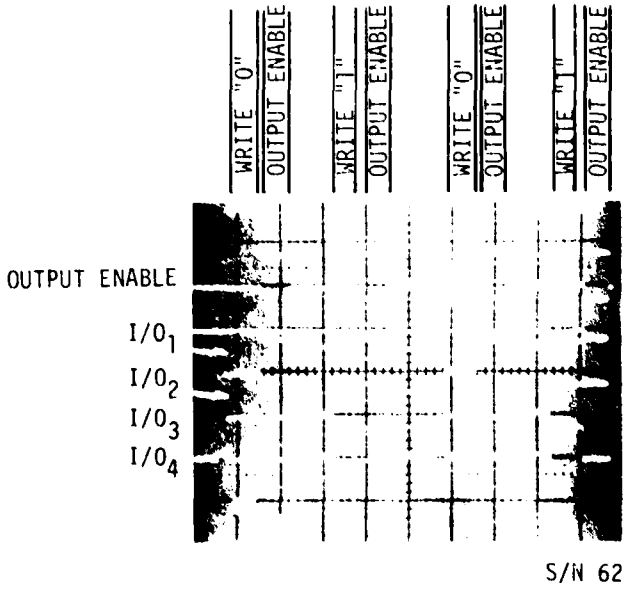


FIGURE D8. MEASURED WAVEFORMS OF ADDRESS 1700_8 AT V_{CC} = 5.00 VOLTS

output 4. A complete bit map showing the physical location (die location) of all the failed bits at 5.0 volts is presented in Figure D9. The part exhibited a critical supply voltage (V_{CRIT}) above which the part functioned properly and below which the part exhibited an increasing number of failed bits (the lower the supply voltage, the greater the number of failed bits). The critical voltage is illustrated in Figure D10. Figure D10 is a composite oscilloscope trace showing output 2 (address 1777_8 operating properly at 4.66 volts and failing at 4.65 volts. The critical voltage was pattern or address sensitive as illustrated in Figure D11 through D14 which are shmoo plots generated on the automated test system. The critical voltage also varied (drifted) with time of applied power. For example, at one point during the bench testing, at address 1777_8, V_{CRIT} was 5.70 volts. After 15 minutes of testing V_{CRIT} increased to 6.38 volts. The part was then turned off for 30 minutes and when retested V_{CRIT} was 5.83 volts. Critical voltages as high as 6.72 volts (after 20 minutes of operation) and as low as 5.40 volts (after one week of storage) were observed for this part. The drift phenomenon was observed at most of the failed bits and may be the reason for the pattern sensitivity indicated by the shmoo plots.

After curve tracer pin-pin tests disclosed no sign of degradation at any input or output component, the part was baked for 16 hours at 200°C. A retest of the part on the automated test system after baking disclosed that it had completely recovered. Thus, the failure of this part was the result of a surface related mechanism probably caused by ionic contamination in or on a passivation layer.

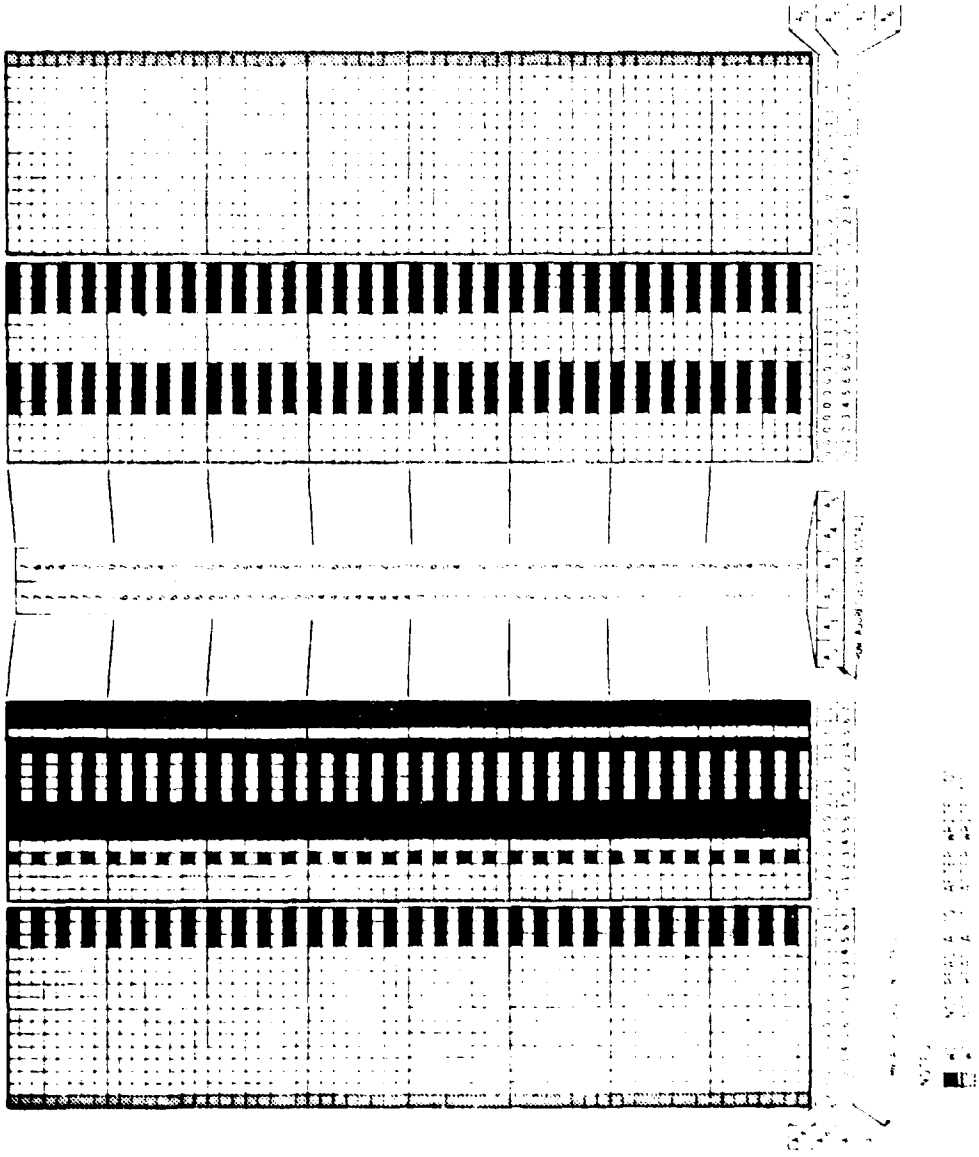


FIGURE D9. BIT MAP OF AM9130 S/N 62 AT V_{CC} = 5.00 VOLTS

I/O_2 @ V_{DD} = 4.66V

OUTPUT ENABLE

I/O_2 @ V_{DD} = 4.65V

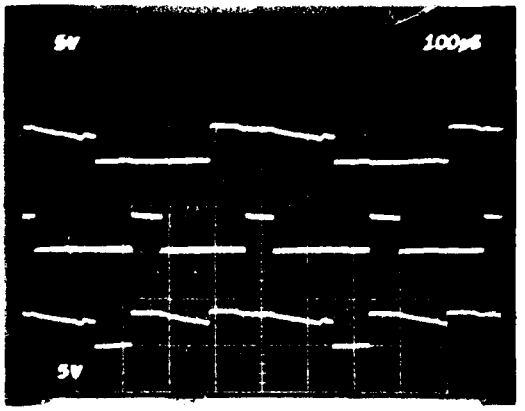


FIGURE D10. ILLUSTRATION OF CRITICAL SUPPLY VOLTAGE FOR AM9130 S/N 62

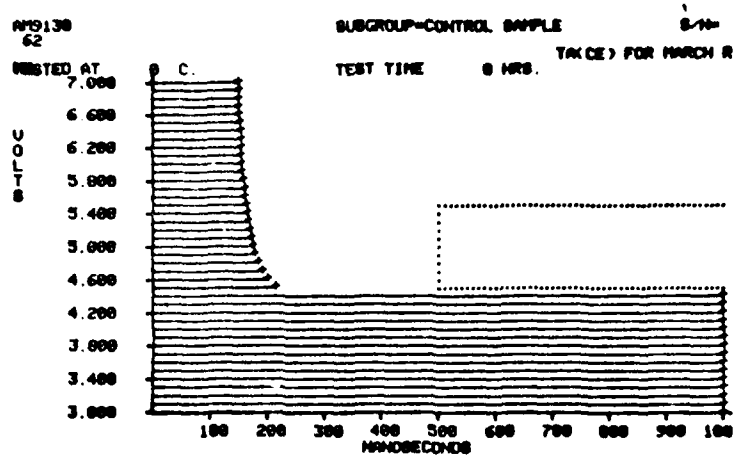


FIGURE D11. CHIP ENABLE ACCESS TIME SHMOO PLOT OF AM9130 S/N 62 - MARCH R/M/W

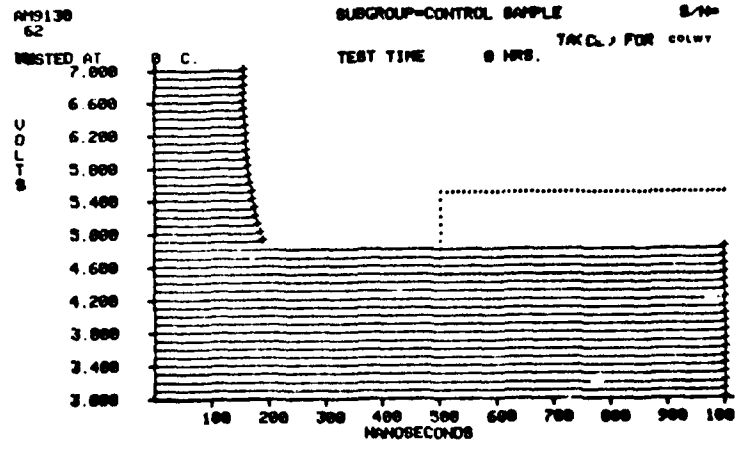


FIGURE D12. CHIP ENABLE ACCESS TIME SHMOO PLOT OF AM9130 S/N 62 - COLWRT

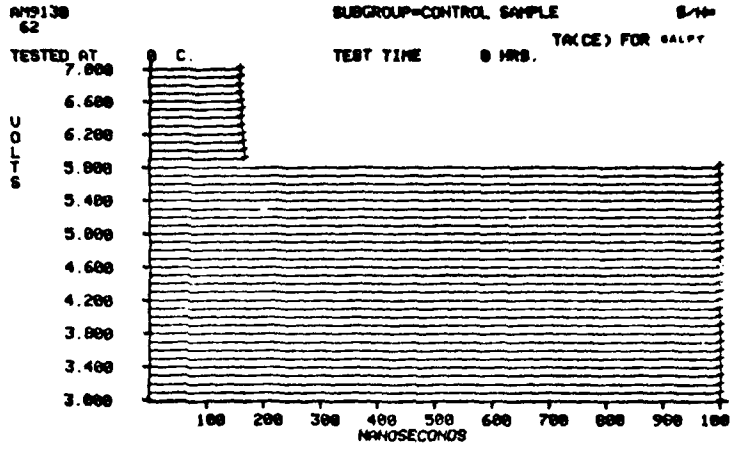


FIGURE D13. CHIP ENABLE ACCESS TIME SHMOO PLOT OF AM9130 S/N 62 - GALPAT

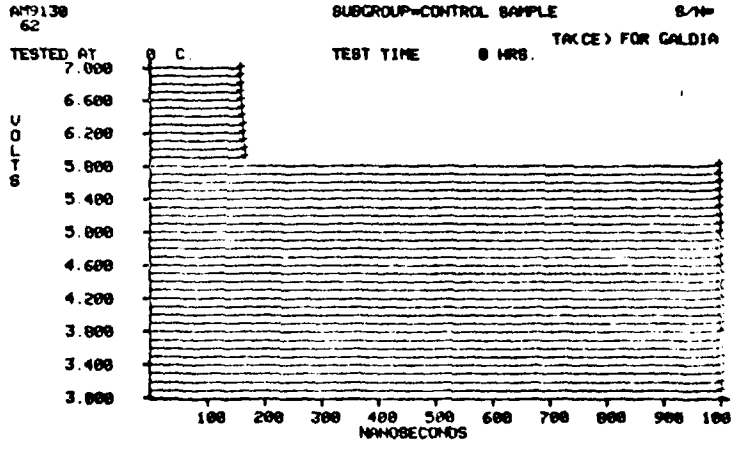


FIGURE D14. CHIP ENABLE ACCESS TIME SHMOO PLOT OF AM9130 S/N 62 - GALDIA R/M/W

2.3 AM9140 $t_{a(CE)}$ FAILURES

Eight AM9140 devices failed $t_{a(CE)}$ during various MARCH, GALLOP and CHECKERBOARD tests at one or both of the supply voltage test conditions. Six parts only failed at -55°C and/or +125°C. Two parts, S/Ns 88 and 92, failed at 25°C (S/N 92 also failed at -55°C and +125°C). In each case the failed value of $t_{a(CE)}$ was greater than 950 nanoseconds, the upper limit setting of the measurement system (the specified maximum limit is 500nS).

The two parts that exhibited 25°C failures were bench tested using the microprocessor controlled test set-up described in paragraph 2.2. S/N 88 had failed $t_{a(CE)}$ during MARCH, MARCH RMW, GALDIA RMW, MS, CB POWER DOWN, and CBN POWER DOWN, all at V_{CC}=5.5 volts, during the parametric tests. S/N 92 had failed $t_{a(CE)}$ MARCH, MARCH RMW, GALDIA RMW, and MS, all at both 4.5V and 5.5V, during the parametric tests. However, during the bench test no anomalous patterns or failed conditions were detected over the supply voltage range of 3.0 to 7.0 volts. Therefore, shmoo plots of MARCH RMW and GALDIA RMW of both parts were generated on the automated test system. S/N 92 passed both shmoo tests, therefore a complete parametric retest was performed. S/N 92 passed all tests indicating that it had completely recovered while awaiting analysis. S/N 88 failed the MARCH RMW shmoo test as shown in Figure D15, but passed the GALDIA RMW as shown in Figure D16. Since the shmoo test results indicated that $t_{a(CE)}$ during GALDIA RMW had recovered, a complete parametric retest of S/N 88 was performed. S/N 88 passed the GALDIA RMW test, but still failed the other five tests that it had originally failed. These findings indicated that the failure had partially recovered and therefore S/N 88 possibly was a surface related failure. After curve tracer pin-pin checks disclosed no sign of degradation at any input or output component, S/N 88 was baked for 16 hours at 200°C. A retest of the part after baking disclosed that it had completely recovered.

In view of the results of the investigation of the 25°C failures, the six parts that failed only at high or low temperature were baked prior to any bench testing. After a 72 hour, 200°C bake, all six parts completely recovered. Thus, the failure of all eight AM9140 devices which exhibited excessive $t_{a(CE)}$ was attributed to a surface related mechanism probably caused by ionic contamination in or on a passivation layer.

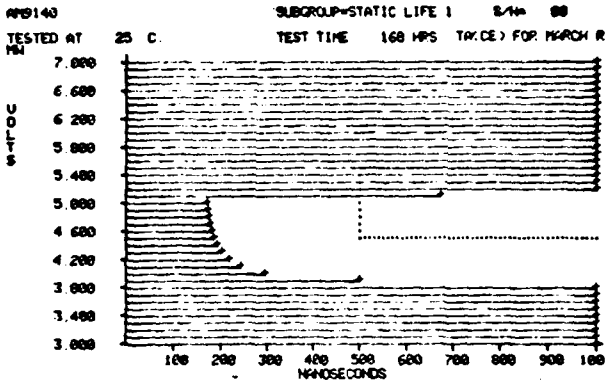


FIGURE D15. CHIP ENABLE ACCESS TIME SHMOO PLOT OF AM9140 S/N 88 - MARCH R/M/W

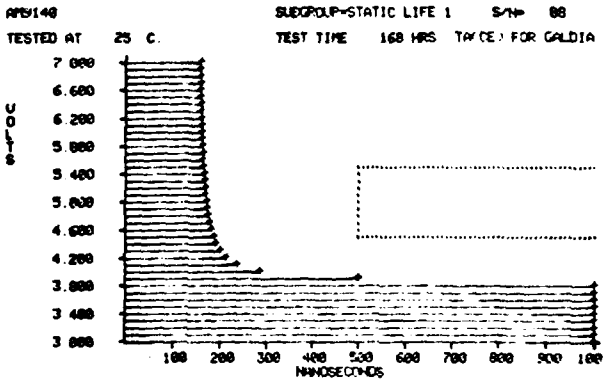


FIGURE D16. CHIP ENABLE ACCESS TIME SHMOO PLOT OF AM9140 S/N 88 - GALDIA R/M/W

2.4 AM9140 $t_{a(CE)}$ CB AND CBN POWER DOWN FAILURE

One AM9140, S/N 63, failed the 25°C and the -55°C $t_{a(CE)}$ CHECKERBOARD (CB) and CHECKERBOARD NOT (CBN) POWER DOWN tests after 4000 hours of 200°C dynamic life test. The power down test consists of writing a CB or CBN pattern into the memory at V_{CC} = 5.5 volts, reducing V_{CC} to 1.5 volts for one second, raising V_{CC} back to 5.5 volts and then performing a CB or CBN read and compare test.

The microprocessor controlled bench test set described in paragraph 2.2 was not equipped to perform the powerdown checkerboard patterns, and time did not permit reprogramming it to do so because the part failed so late in the program. Therefore, S/N 63 was retested on the automated test system. The part still failed the CBN test but now passed the CB test indicating that it had partially recovered. After curve tracer pin-pin tests disclosed no sign of degradation at any input or output component, the part was delidded, baked, and exposed to U.V. light. When retested the part was again failing both the CB and the CBN tests. Additional diagnostic testing of the part on the automated test system established that the failures occuring during the checkerboard tests were located at four adjacent memory cells: 3136_8, 3137_8, 3236_8, and 3237_8. Optical examination of these four cells revealed no obvious anomaly, consequently the glassivation layer was removed chemically for re-examination and further analysis. Examination of the four cells again revealed no anomaly. A retest of the part on the automated test system at this point prior to any further analysis, disclosed that it now was failing all functional tests. The failures were permanent and could not be reversed by baking. Apparently, the part had been damaged irreversibly by the glassivation removal, but the nature of the damage could not be established. As a result, no further analysis of the original CB/CNB failures could be performed and the failure mode and mechanism of this part could not be established.

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