

AD-A076 118

YUCCA INTERNATIONAL INC SCOTTSCALE AZ
SOFTWARE DEVELOPMENT, ITEM 0005 OF MICROPROCESSOR-BASFD POWER C--ETC (I
FEB 79

F/G 9/3
DAAK70-78-C-0117
NL

UNCLASSIFIED

| OF |
AD
A076 118



END
DATE
FILMED
12-79
DDC

LEVEL II



AD A 076118

⑥

SOFTWARE DEVELOPMENT,

ITEM ~~0005~~

OF

MICROPROCESSOR-BASED POWER

CONDITIONER CONTROLLER.

SC

CONTRACT NO. DAAK78-78-C-0117

⑬

⑪ Feb 79

⑫ 51

DDC FILE COPY

PREPARED FOR

U. S. ARMY MERADCOM

FORT BELVOIR, VIRGINIA 22060

PREPARED BY

YUCCA INTERNATIONAL INCORPORATED

14415 N. SCOTTSDALE ROAD

SUITE 700

SCOTTSDALE, ARIZONA 85260

THIS DOCUMENT IS BEST QUALITY PRACTICABLE.
 THE COPY FURNISHED TO DDC CONTAINED A
 SIGNIFICANT NUMBER OF PAGES WHICH DO NOT
 REPRODUCE LEGIBLY.

DISTRIBUTION STATEMENT A
 Approved for public release;
 Distribution Unlimited

DDC
 REPRODUCED
 OCT 29 1979
 D

FEBRUARY 1979

79 08 28 042

392729

JP

TABLE OF CONTENTS

	<u>PAGE</u>
1.0.0 SUMMARY	1
2.0.0 PREFACE	1
3.0.0 COPYRIGHT PERMISSION.	1
4.0.0 INTRODUCTION.	2
5.0.0 INVESTIGATION	2
5.1.0 VOLTAGE REGULATION CONSIDERATIONS	2
5.2.0 VOLTAGE REGULATION ROUTINES	2
5.2.1 SMALL ERROR ROUTINE	3
5.2.2 LARGE ERROR ROUTINE	4
6.0.0 DISCUSSION.	5
7.0.0 CONCLUSIONS	6
8.0.0 RECOMMENDATION.	6

LIST OF APPENDICES

APPENDIX A -- FLOW CHARTS	7
APPENDIX B -- SOFTWARE LISTING	16

79 08 28 042

1.0.0 SUMMARY

This report describes the efforts performed under Task 5 of U. S. Army contract no. DAAK70-78-C-0117 to develop a microprocessor-based controller for the Delco 15KW power conditioner.

Continuing from the hardware development, the previous task, the software necessary to perform voltage regulation of the converter section was developed using the Motorola Exorcisor development system and the MC6809 Assembler.

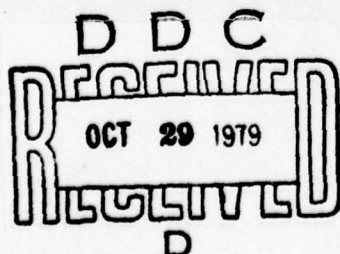
The assembled program was executed and debugged using the simulation capability provided by the Motorola MC6809 Simulator and Motorola Exorcisor.

2.0.0 PREFACE

Work described in this report was performed by Yucca International, Inc. under the direction of the U. S. Army Mobility Equipment Research & Development Command. This completes the fifth task of the first phase of the U. S. Army contract no. DAAK70-78-C-0117. The Contracting Officer's Representative is Dr. David Lee of the U. S. Army MERADCOM Headquarters at Fort Belvoir, Virginia.

3.0.0 COPYRIGHT PERMISSION

No copyright permission is required.



Accession For	
NTIS GRA&I	<input checked="" type="checkbox"/>
DDC TAB	<input type="checkbox"/>
Unannounced Justification	<input type="checkbox"/>
By <u>Per Htr. on file</u>	
Distribution/	
Availability Codes	
Dist.	Avail and/or special
<u>A</u>	

4.0.0 INTRODUCTION

This is a report of the fifth of six tasks of the U. S. Army contract no. DAAK70-78-C-0117.

Performed during the previous tasks was the design and development of the controller hardware. The objective of this task was to generate the necessary software to perform voltage regulation of the converter section of the Delco 15 KW power conditioner.

This report details the voltage regulation routines. Contained in the report are flow charts and an assembled listing of the software.

5.0.0 INVESTIGATION

5.1.0 VOLTAGE REGULATION CONSIDERATIONS

The software generated during this task is intended to operate the controller hardware to perform voltage regulation of the AC to DC section in the power conditioner.

The power conditioner is designed to operate from a poor quality AC source, thus the AC input is allowed to fluctuate +19% and -15% from 120/208 VRMS.

The fluctuating AC input voltage, the converter operating frequency, and the load on the converter output determines the converter output voltage.

To regulate the converter output voltage at a steady DC level the controller varies the converter operating frequency.

5.2.0 VOLTAGE REGULATION ROUTINES

Two different converter output voltage error correction routines were employed in the controller software.

One corrects for small errors, the other corrects for large errors. Currently, a large error is defined as a measured voltage that differs greater than 10% from the reference value.

5.2.1 SMALL ERROR ROUTINE

The small error correctior is based on a percentage of the error that was detected. The reference value and the measured value will both be an 8 bit binary value. A one bit difference between the two values corresponds approximately to a 0.5% error. The correction to the converter oscillator DAC value (which represents operating frequency) is calculated by shifting the 11 bit binary value (10 bits + 1 overload offset bit) right the appropriate number of bit positions.

For instance, to correct a 0.5% error (1 bit error), a 0.1% correction is applied to the converter oscillator DAC value. This correction is found by dividing the DAC value by 1024, to produce a value that is approximately 0.1% of the DAC value. The division is performed by shifting right 10 places. Although it may take several times through the small error routine to correct the error to zero, a correction much less than the actual error avoids possible overcorrection. The overcorrection would be due to non-linearity of the converter output power versus operating frequency characteristics.

Table 2 in the listing shows the percent that the converter oscillator frequency will be adjusted given a particular converter output voltage error.

Table 2 can be expanded to correct for larger errors but it is expected that regulator would be slower compared to the large error correction routine described below.

5.2.2 LARGE ERROR ROUTINE

For large converter output voltage errors it may be inefficient to use the small error correction method.

An alternate method was devised to correct for large changes in converter output voltage due to application and removal of full loads.

This method utilizes a table which correlates a calculated value of converter output power with a corresponding converter operating frequency.

The frequency value obtained from the table assumes a converter input voltage of 300 volts DC and is subject to a correction factor when the input voltage deviates from 300 volts DC.

The converter output power requirements can be calculated by measuring the converter output voltage (V_{measured}) and inverter input current (I_{measured}) and using the equation derived below:

$$1) \quad V_{\text{Measured}}/I_{\text{Measured}} = \text{Resistance of converter load} = V_{\text{Reference}}/I_{\text{Desired}}$$

$$2) \quad I_{\text{Desired}} = (V_{\text{Reference}}/V_{\text{Measured}}) (I_{\text{Measured}})$$

$$3) \quad \text{Power} = (I_{\text{Desired}}) (V_{\text{Reference}}) = (I_{\text{Desired}}) (\text{Ratio})$$

To simplify equation 3, the $V_{\text{Reference}}$ term was replaced with Ratio. When the front panel voltage select switches are set to 120 VRMS out, the Ratio will be 1.00, otherwise it will be a normalized value relative to 120 VRMS.

The final equation actually used in the software is

$$\text{Power} = (V \text{ Nominal}/V \text{ Measured}) (I \text{ Measured}) (\text{Ratio})$$

This routine is intended to use the load vs. frequency table to correct a large converter output voltage error to an error within the range of the small error correction routine. If necessary, the range of the small error correction routine can be extended from 10% to 20% or greater to accommodate for inaccuracies of the load vs. frequency table.

6.0.0 DISCUSSION

The controller software was developed with the intent of making it a framework that will accommodate additional required tasks as development progresses. In addition to the routines that will regulate converter output voltage, there is programming intended for future required tasks.

The two regulation routines used in the controller software, each have their disadvantages when used for large error correction.

If the small error correction routine was expanded to correct for large errors also, the controller would be less vulnerable to changes in converter characteristics. The small error routine does not use a load vs. frequency table and will be relatively insensitive to converter design changes or parts replacement. It will also use less program memory because the involved calculation routines will not be needed. Since only the converter output voltage sense signal is required for regulation, the reliability is increased. Regulation is expected to be much slower. Regulation speed can become critical when removal of full loads or overloads occur, thus, if regulation is not fast, then transient overvoltage will result.

The large error correction routine will be utilized by the controller because it is expected to offer the best regulation performance. Should this be proven untrue as development progresses, then the large error routine will be discarded in favor of the expanded small error correction routine.

The controller software has been developed to the point that after system debug it can be tested with the converter section to perform voltage regulation under normal load conditions. No time-overload profile capability has been implemented in the software yet and the overload portion of the load vs. frequency table (Table 3 in the listing) has not been developed.

During periods of converter SCR commutation failure, the converter will be deactivated for a Delco recommended period of 22ms. The software necessary to regulate the converter with one phase disabled will be developed at a later date.

Mirror modifications to the hardware have been implemented in an effort to simplify the software. These and any other modifications will be listed in the next report.

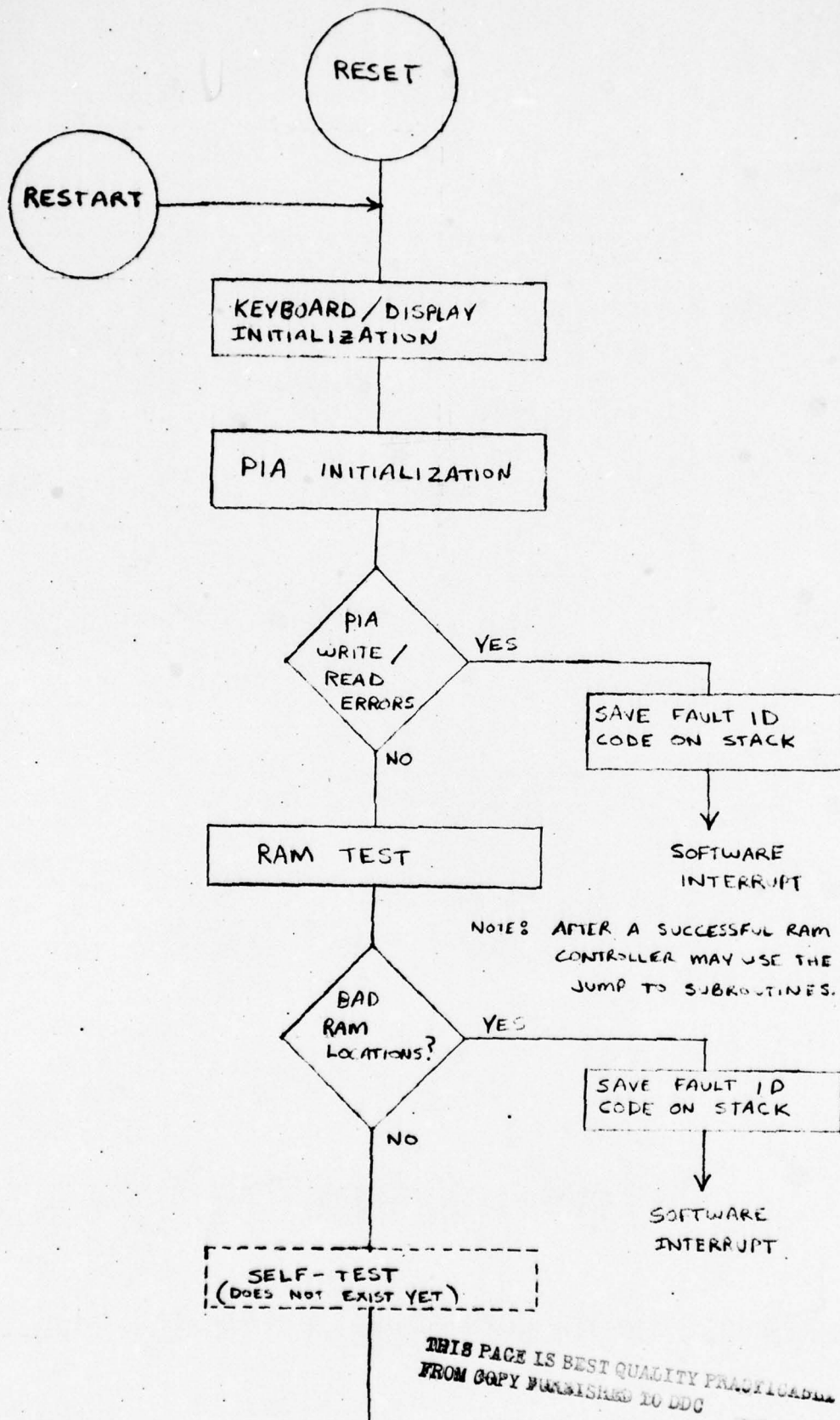
7.C.0 CONCLUSIONS

The software has been developed and is ready to be combined with the controller hardware for checkout and debug of the system.

8.C.0 RECOMMENDATIONS

It is recommended that Yucca International, Inc. proceed immediately with the next task, System Debug.

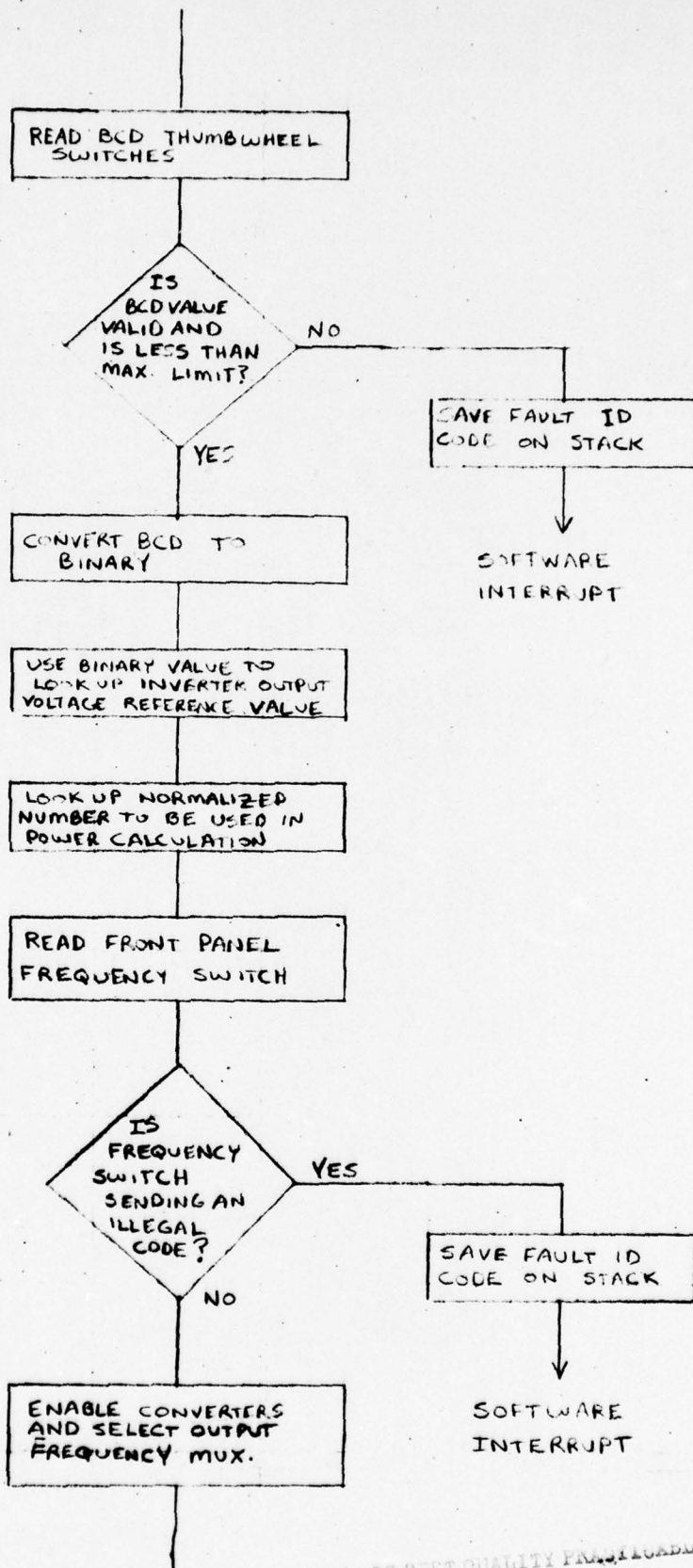
APPENDIX A -- FLOW CHARTS



APPENDIX A FLOW CHARTS

PART 1 OF 7

THIS PAGE IS BEST QUALITY PRACTICABLE FROM COPY FURNISHED TO DDC



APPENDIX A
PART 2 OF 7

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

SELECT MUX2 TO
CONVERTER OUTPUT
VOLTAGE

LOAD CONVERTER OSCILLATOR
DAC WITH A VALUE THAT
WILL PRODUCE APPROXIMATELY
100V RMS AT NO LOAD.

CLEAR ANY COMM FAIL
INTERRUPT THAT WAS
PENDING

WAIT FOR NEXT
CONVERTER OPERATING
CYCLE INTERRUPT

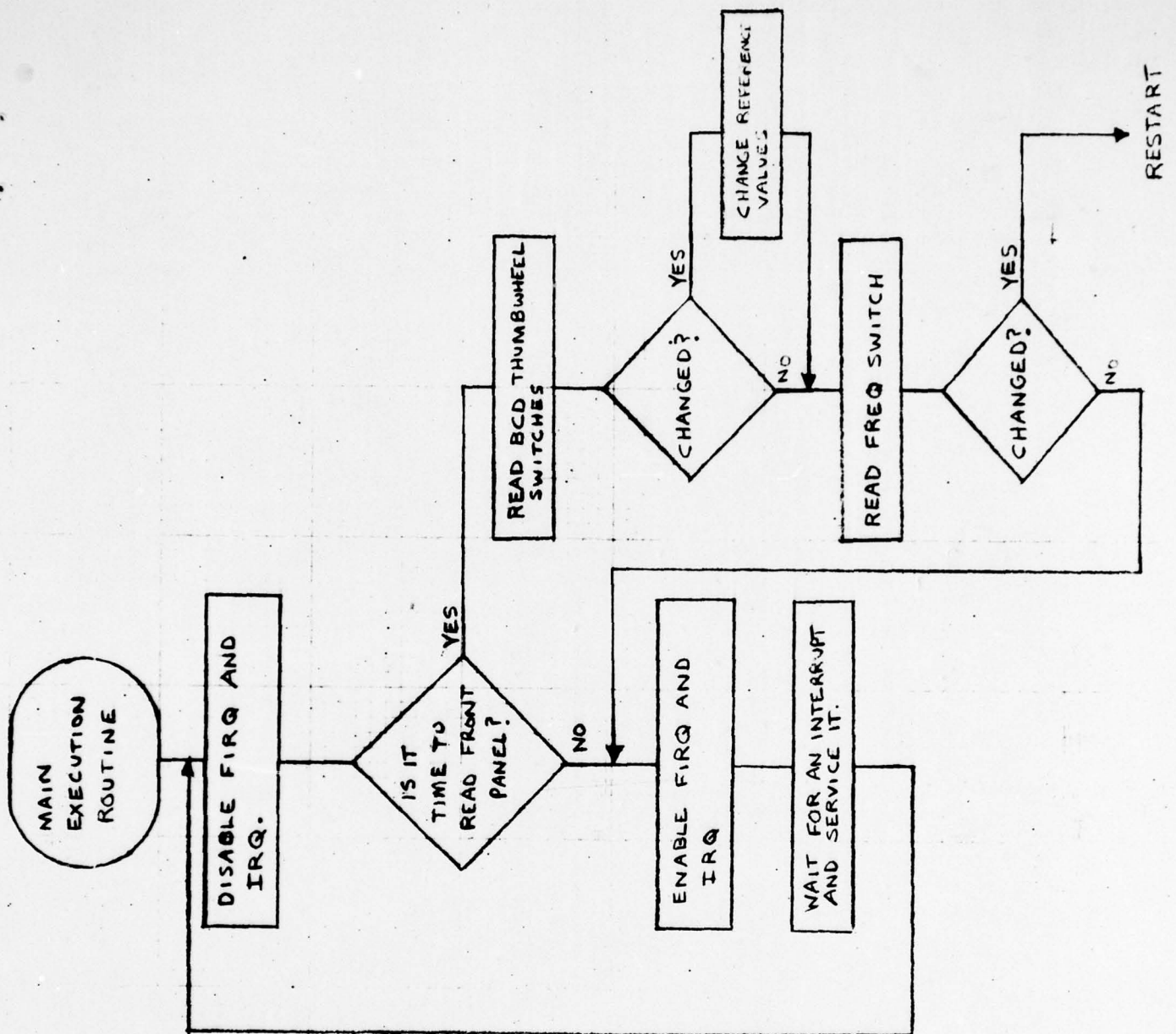
* INTERRUPT WILL NOT BE SERVICED
BECAUSE INTERRUPTS ARE DISABLED.

ALLOW AN ADDITIONAL
WAITING PERIOD FOR
CONVERTER OPERATING FREQ
TO TAKE EFFECT.

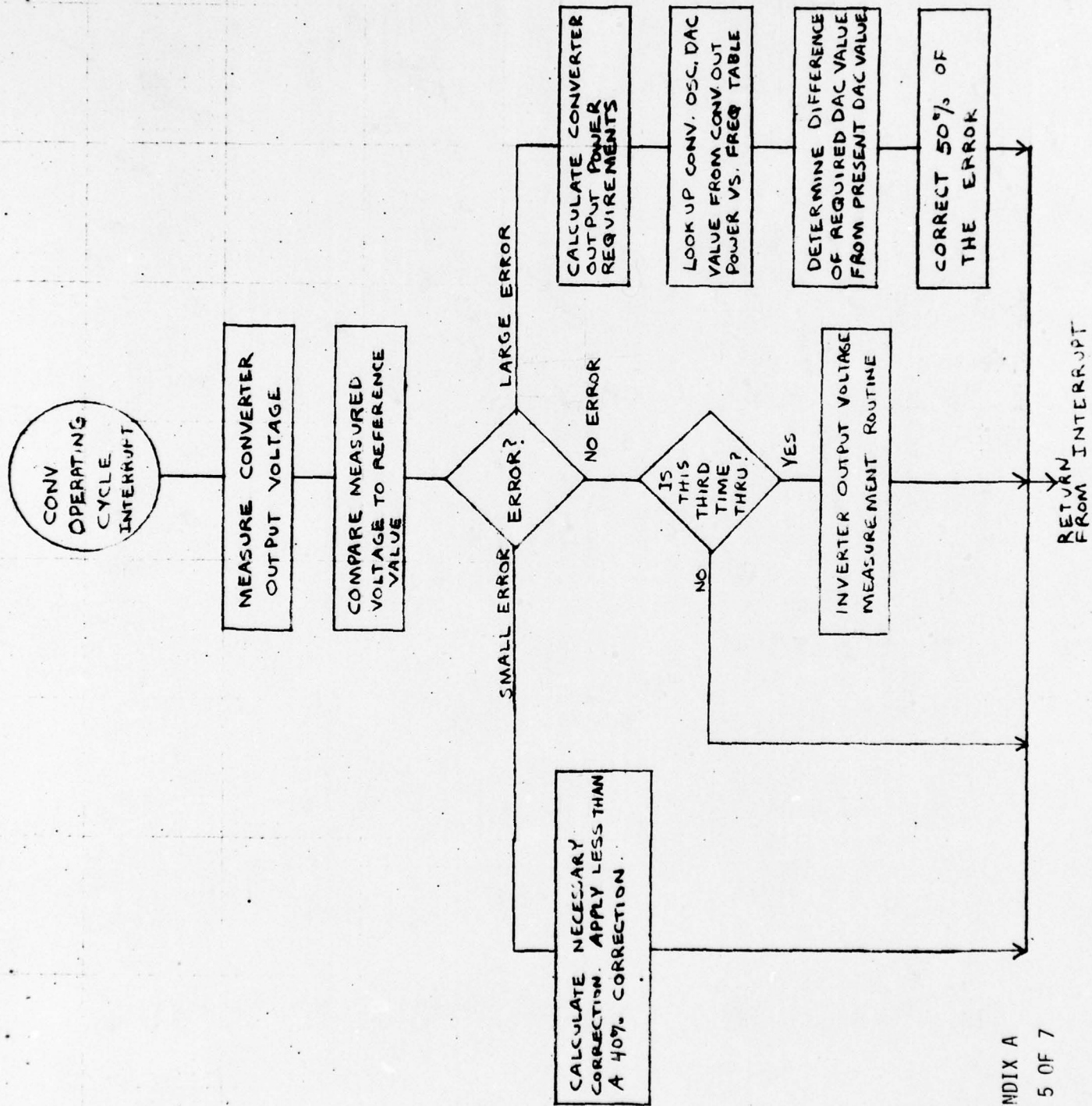
↓
MAIN
EXECUTION
ROUTINE

THIS PAGE IS BEST QUALITY PRACTICABLE
FROM COPY FURNISHED TO DDC

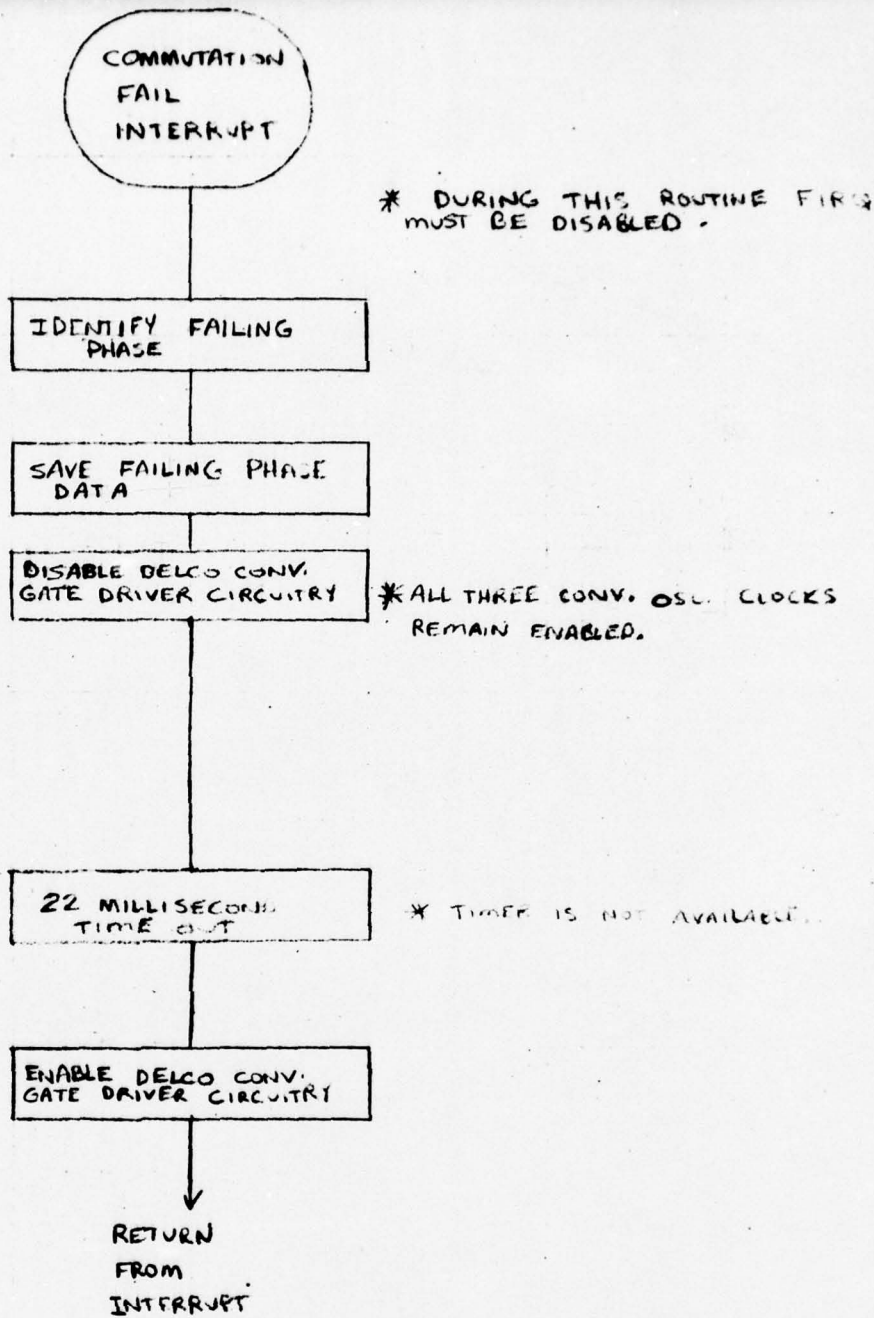
APPENDIX A
PART 3 OF 7



APPENDIX A
PART 4 OF 7

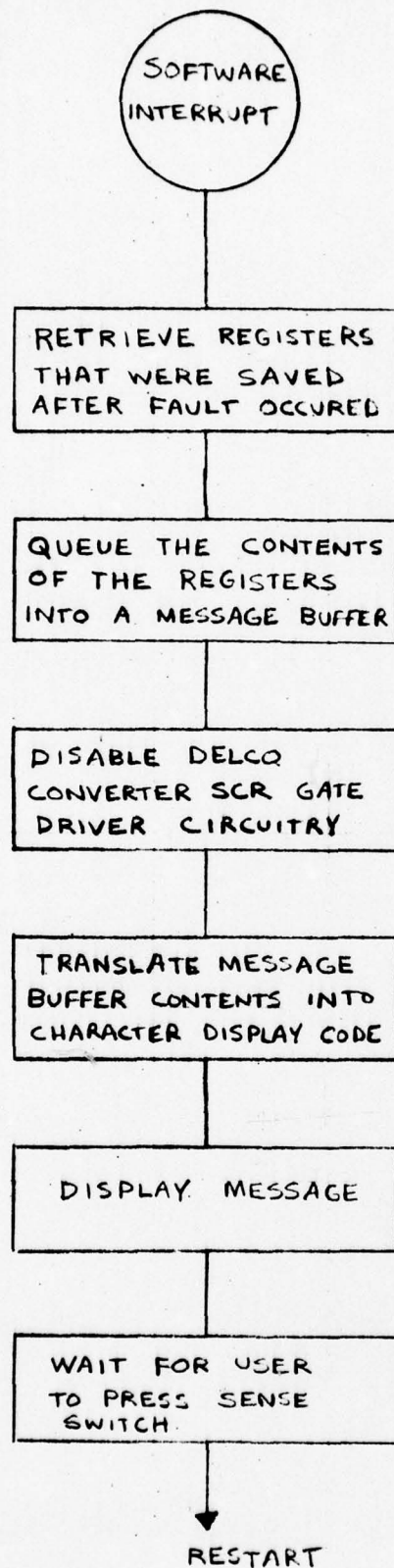


APPENDIX A
PART 5 OF 7



THIS PAGE IS BEST QUALITY PRACTICABLE
 FROM COPY FURNISHED TO DDG

APPENDIX A
 PART 6 OF 7



APPENDIX A
PART 7 OF 7

APPENDIX B -- SOFTWARE LISTING

APPENDIX B

PAGE 001 CNTR4 .SA:1 CNTRLR

	NAM	CNTRLR.0
00001		
00002	DPT	CRE
00003	*****	
00004	♦	
00005	♦	
00006	*****	
00007	♦	15 KW POWER CONDITIONER CONTROLLER SOFTWARE
00008	*****	
00009	♦	
00010	♦	
00011	♦	DEVELOPED BY YUCCA INTERNATIONAL , INC.
00012	♦	
00013	♦	REVISION 1 FEB. 16, 1979 R. KRAWL
00014	♦	
00015	♦	DEVELOPED FOR U.S. ARMY MERADCOM
00016	♦	CONTRACT NO. DAAG70-78-C-0117
00017	♦	C.O.R. DAVID LEE
00018	♦	
00019	♦	
00020	*****	

```

00023      *
00024      *
00025      *
00026      *
00027      *****
00028      *
00029      *          PROGRAM EQUATES
00030      *****
00031      *
00032      * WRITE ENABLE SIGNALS
00033      *-----*
00033      8000      A WE0      EQU      $8000      ; DAC HI BYTE (BITS 1-0)
00034      8001      A WE1      EQU      $8001      ; DAC LO BYTE
00035      8002      A WE2      EQU      $8002      ; SPARE
00036      8003      A WE3      EQU      $8003      ; SPARE
00037      8004      A WE4      EQU      $8004      ; LOAD DAC STROBE
00038      8005      A WE5      EQU      $8005      ; CLEAR COMM. FAIL INT.
00039      8006      A WE6      EQU      $8006      ; SPARE
00040      8007      A WE7      EQU      $8007      ; SPARE
00041      *
00042      *
00043      * READ ENABLE SIGNALS
00044      *-----*
00045      8000      A RE0      EQU      $8000      ; SPARE
00046      8008      A RE1      EQU      $8008      ; A/D#2 BYTE
00047      8010      A RE2      EQU      $8010      ; A/D#1 LO BYTE
00048      8018      A RE3      EQU      $8018      ; A/D#1 HI BYTE
00049      8020      A RE4      EQU      $8020      ; 1/4 DEG. CNTR LO BYTE
00050      8028      A RE5      EQU      $8028      ; 1/4 DEG. CNTR HI BYTE
00051      8030      A RE6      EQU      $8030      ; UNASSIGNED
00052      8038      A RE7      EQU      $8038      ; BCD SW (DIG 2 AND 3)
00053      8040      A RE8      EQU      $8040      ; FREQ. SWITCH
00054      8048      A RE9      EQU      $8048      ; WAVEFORM EPROM
00055      8050      A RE10     EQU      $8050      ; SPARE
00056      8058      A RE11     EQU      $8058      ; SPARE
00057      8060      A RE12     EQU      $8060      ; SPARE
00058      8068      A RE13     EQU      $8068      ; SPARE
00059      8070      A RE14     EQU      $8070      ; SPARE
00060      8078      A RE15     EQU      $8078      ; SPARE
00061      *
00062      *
00063      * OTHER EQUATES
00064      *-----*
00065      4000      A DSPLYD EQU      $4000      ; WRITE DATA TO DISPLAY
00066      4001      A DSPLYC EQU      $4001      ; WRITE COMMAND TO DISP
00067      0000      A DMODE  EQU      $00        ; 8 CHARACTER, LEFT ENTRY
00068      0090      A WDISPL EQU      $90        ; LOC. 0, AUTO-INC.
00069      00DF      A CLRDIS EQU      $DF        ; CLEAR DISPLAY RAM
00070      00FF      A STAK   EQU      $00FF     ; STACK
00071      *
00072      *
00073      *
00074      0039      A HILIM  EQU      $39        ; BCD THUMB SW MAX LIM
00075      0055      A TRUE   EQU      $55        ; TRUE
00076      00AA      A NTRUE  EQU      $AA        ; NOT TRUE

```

```

00078      *
00079      *****
00080      *
00081      *                   PIA EQUATES
00082      *****
00082      40A1  A CNTRLA EQU   $40A1   ; CONTROL REG. A
00083      40A0  A PORTA  EQU   $40A0   ; PERIF REG. A( OR DDR
00084      *
00085      00FF  A DREXN  EQU   $FF     ; MAKE PA0-PA7  OUTPUTS
00086      *
00087      * PERIPHERAL PORT A OUTPUT LINES
00088      *-----*
00089      0003  A PROMSL EQU   $03     ; PA1, PA0 = EPROM RD SL
00090      001C  A MUX1SL EQU   $1C     ; PA4, PA3, PA2
00091      00E0  A MUX2SL EQU   $E0     ; PA7, PA6, PA5
00092      *
00093      *
00094      40A3  A CNTRLB EQU   $40A3   ; CONTROL REG. B
00095      40A2  A PORTB  EQU   $40A2   ; PERIF REG. B( OR DDR
00096      *
00097      00FF  A DREXNB EQU   $FF     ; MAKE PB0-PB7  OUTPUTS
00098      *
00099      * PERIPHERAL PORT B OUTPUT LINES
00100      00FC  A FREQSL EQU   $FC     ; PB1-PB0 = OUTPUT FREQ
00101      00FC  A ENABLA EQU   $FC     ; PHASE A CONV (PB2=0)
00102      0008  A ENABLB EQU   $08     ; PHASE B CONV (PB3=0)
00103      0010  A ENABLC EQU   $10     ; PHASE C CONV (PB4=0)
00104      001C  A ENALL  EQU   $1C     ; PHASE A, B, C CONV EN
00105      0020  A .33KHZ EQU   $20     ; CONV OSC. OFFSET EN
00106      0040  A ENBLCV EQU   $40     ; CONV ENABLE (PB6=0)
00107      0080  A CNVRT2 EQU   $80     ; A/D#2 CONVERT (PB7=0)
00108      *
00109      *
00110      40C1  A CNTRLC EQU   $40C1   ; CONTROL REG. C
00111      40C0  A PORTC  EQU   $40C0   ; PERIF REG. C( OR DDR
00112      *
00113      0003  A DREXNC EQU   $03     ; MAKE PC0-PC1 OUTPUTS
00114      *           $           AND PC2-PC7 INPUTS
00115      *
00116      * PERIPHERAL PORT C OUTPUT LINES
00117      *-----*
00118      0001  A CNVRT1 EQU   $01     ; A/D#1 CONVRT (PC0=0)
00119      0002  A NORMAL EQU   $02     ; NORMAL(PC1=0)
00120      *                   10 DEG. (PC1=1)
00121      *
00122      * PERIPHERAL PORT C INPUT LINES
00123      *-----*
00124      0008  A CMPLT1 EQU   $08     ; A/D#1 CMPLT (PC3=0)
00125      0010  A CMPLT2 EQU   $10     ; A/D#2 CMPLT (PC4=0)
00126      00E0  A COMFAL EQU   $E0     ; CNVRTR COMMUT. FAIL
00127      *                   PHASE C FAIL (PC5 =0)
00128      *                   PHASE B FAIL (PC6 =0)
00129      *                   PHASE A FAIL (PC7 =0)

```

```

00131      *
00132      *
00133      *****
00134      *          MULTIPLEXER SELECT EQUATES
00135      *****
00136      * MUX#1 SELECT ; PA4, PA3, PA2
00137      *-----*
00138      0000      A IVCURC EQU      $00      ; INV OUT CURR C
00139      0004      A IVCURB EQU      $04      ; INV OUT CURR B
00140      0008      A IVCURA EQU     $08      ; INV OUT CURR A
00141      000C      A IVVOLC EQU     $0C      ; INV OUT VOLT C
00142      0010      A IVVOLB EQU     $10      ; INV OUT VOLT B
00143      0014      A IVVOLA EQU     $14      ; INV OUT VOLT A
00144      0018      A IVNPT EQU     $18      ; INV INP CURR
00145      001C      A SPARE1 EQU     $1C      ; SPARE CHANNEL
00146      *
00147      *
00148      * MUX#2 SELECT ; PA7, PA6, PA5
00149      *-----*
00150      0000      A CVCURC EQU     $00      ; CONV OUT CURR C
00151      0020      A CVCURB EQU     $20      ; CONV OUT CURR B
00152      0040      A CVCURA EQU    $40      ; CONV OUT CURR A
00153      0060      A NPTVLC EQU     $60      ; INPUT VOLT C
00154      0080      A NPTVLB EQU     $80      ; INPUT VOLT B
00155      00A0      A NPTVLA EQU     $A0      ; INPUT VOLT A
00156      00C0      A CVOUT EQU      $C0      ; CONV OUT VOLT
00157      00E0      A SPARE2 EQU     $E0      ; SPARE CHANNEL
00158      *
00159      *
00160      * OUTPUT FREQUENCY MUX SELECT ; PB1, PBO
00161      *-----*
00162      0000      A .50HZ EQU       $00      ; PB1=0, PBO=0
00163      0001      A .60HZ EQU       $01      ; PB1=0, PBO=1
00164      0002      A .400HZ EQU     $02      ; PB1=1, PBO=0
00165      0003      A EXTERN EQU     $03      ; EXTERNAL
00166      *

```

```

00168
00169
00170
00171P 0000      0001  A DVISOR RMB      1
00172P 0001      0001  A VMEASR RMB      1      ; CONVERTER OUTPUT VOLT
00173            *                               ; MEASURED VALUE.
00174P 0002      0001  A DVIDND RMB      1
00175P 0003      0001  A VNOMNL RMB      1      ; NOMINAL CONVERTER OUT
00176            *                               ; VOLTAGE REFERENCE VAL
00177P 0004      0001  A PLARTY RMB      1      ; POLARITY OF CONVERTER
00178            *                               ; OUTPUT VOLTAGE ERROR.
00179P 0005      0001  A BCDVAL RMB      1      ; BCD VALUE READ FROM
00180            *                               ; THUMBWHEEL SWITCHES.
00181P 0006      0001  A STABLE RMB      1      ; COUNTS INTERVALS THAT
00182            *                               ; OUTPUT VOLTAGE HAS MAI
00183            *                               ; TAINED A STEADY LEVEL.
00184P 0007      0001  A LOKOUT RMB      1      ; DON'T EXECUTE INV OUT
00185            *                               ; MEASUREMENT ROUTINE.
00186P 0008      0001  A FQMODE RMB      1      ; OUTPUT FREQ. MODE
00187            *                               ; 04H=400HZ, 02H=60HZ, 01H=50H
00188P 0009      0002  A DACVAL RMB      2      ; CONVERTER OSCILLATOR
00189            *                               ; DAC VALUE.
00190            *                               ; 000H - 3FFH = NORMAL
00191            *                               ; 400H - 7FFH = OVRLD
00192P 000B      0002  A SAVE1  RMB      2      ; TEMPORARY STORAGE
00193P 000D      0001  A COUNT1 RMB      1      ; TEMPORARY STORAGE
00194P 000E      0002  A IMEASR RMB      2      ; INVERTER INPUT CURREN
00195            *                               ; MEASURED VALUE.
00196P 0010      0001  A OVRDLD RMB      1      ; OVERLOAD FLAG
00197            *                               ; 55H=OVRDLD AAH=NO OVRDLD
00198P 0011      0002  A MLTCAN RMB      2      ; NUMBER TO BE MULTIPLI
00199P 0013      0001  A QUOTNT RMB      1      ; WHOLE UNITS TO BE MUL
00200P 0014      0001  A REMNDR RMB      1      ; FRACTIONAL NUMBER TO
00201            *                               ; BE MULTIPLIED.
00202P 0015      0002  A RESULT RMB      2      ; RESULT OF MULTIPLICAT
00203P 0017      0002  A REFRNC RMB      2      ; INV OUT VOLT REF VALU
00204P 0019      0002  A RATIO  RMB      2      ; NORMALIZED VALUE
00205P 001B      0001  A FAILST RMB      1      ; CONV COMM. FAIL STAT.
00206            *                               ; IF BIT 7 = 1 THEN PHS
00207            *                               ; IF BIT 6 = 1 THEN PHS
00208            *                               ; IF BIT 5 = 1 THEN PHS
00209P 001C      0001  A SERVIC RMB      1      ; FRNT PNL SERVICE CNT
00210P 001D      0004  A MESSBF RMB      4      ; MESSAGE BUFFER
00211P 0021      0008  A DSPBUF RMB      8      ; DISPLAY BUFFER
00212
00213
00214
00215A CFF2
00216
00217A CFF2      0000  A      FDB      $0000  ; UNUSED
00218A CFF4      0000  A      FDB      $0000  ; UNUSED
00219A CFF6      C11F  A      FDB      FIRQ   ; FAST INTERRUPT REQ.
00220            *                               ; ( CONV. OPER. CYC. INT
00221A CFF8      C387  A      FDB      IRQ    ; INTERRUPT REQUEST.
00222            *                               ; ( CONV. COMM. FAIL INT
00223A CFFA      C3C9  A      FDB      SWINT  ; SOFTWARE INTRUPT VECT
00224A CFFC      C3C1  A      FDB      NM     ; NON-MASK INTRPT VECTR
00225A CFFE      C000  A      FDB      RESTRT ; RESTART VECTOR

```

```

00227 *****
00228 * BEGINNING OF PROGRAM
00229 * -----
00230A C000 ORG $C000 ; BEGINNING ADDRESS
00231 *
00232A C000 1A 50 A RESTRT ORCC ##50 ; DISABLE FIRQ AND IRQ
00233A C002 10CE 00FF A LDS #STAK ; INITIALIZE STACK PTR.
00234 *
00235 * KEYBOARD/DISPLAY INITIALIZATION
00236 * -----
00237A C006 86 00 A KEYDIS LDA #DMODE
00238A C008 B7 4001 A STA DSPLYC ; INIT. KYBD/DSPLY MODE
00239A C00B 86 2A A LDA ##2A
00240A C00D B7 4001 A STA DSPLYC ; PROG. 8279 INT. CLK
00241 * TO 100KHZ.
00242A C010 86 90 A LDA #WDISPL
00243A C012 B7 4001 A STA DSPLYC ; COUNTER INIT LOC. 0
00244A C015 86 DF A LDA #CLRDIS
00245A C017 B7 4001 A STA DSPLYC ; CLR DSPLY RAM TO "1'S
00246 *
00247 *
00248 * PERIPHERAL INTERFACE ADAPTER ( PIA ) INIT.
00249 * -----
00250A C01A 86 04 A LDA ##04
00251A C01C B7 40A1 A STA CNTRLA ; ENABLE PORT A
00252A C01F C6 FF A LDB ##FF
00253A C021 F7 40A0 A STB PORTA ; ALL PORT A LINES HIGH
00254A C024 7F 40A1 A CLR CNTRLA ; ENABLE DATA DIR A
00255A C027 F7 40A0 A STB PORTA ; ALL PORT A LINES ARE
00256 * OUTPUT LINES.
00257A C02A B7 40A1 A STA CNTRLA ; ENABLE PORT A
00258A C02D F1 40A0 A CMPB PORTA ; READ BACK PORT A
00259A C030 27 06 C038 BEQ OK3
00260A C032 34 07 A FAULT3 PSHS B, A, CC ; PORT A RD/WR ERROR
00261A C034 CC 5503 A LDD ##5503 ;
00262A C037 3F SWI
00263 *
00264A C038 B7 40A3 A OK3 STA CNTRLB ; ENABLE PORT B
00265A C03B F7 40A2 A STB PORTB ; ALL PORT B LINES HIGH
00266A C03E 7F 40A3 A CLR CNTRLB ; ENABLE DATA DIR B
00267A C041 F7 40A2 A STB PORTB ; ALL ARE OUTPUT LINES
00268A C044 B7 40A3 A STA CNTRLB ; ENABLE PORT B
00269A C047 F1 40A2 A CMPB PORTB ; READ BACK PORT B
00270A C04A 27 06 C052 BEQ OK4
00271A C04C 34 07 A FAULT4 PSHS B, A, CC ; PORT B RD/WR ERROR
00272A C04E CC 5504 A LDD ##5504 ;
00273A C051 3F SWI
00274 *
00275A C052 B7 40C1 A OK4 STA CNTRLC ; ENABLE PORT C
00276A C055 F7 40C0 A STB PORTC ; ALL PORT C LINES HIGH
00277A C058 7F 40C1 A CLR CNTRLC ; ENABLE DATA DIR C
00278A C05B C6 03 A LDB #DREXNC ; PC1, PC0 ARE OUTPUTS
00279A C05D F7 40C0 A STB PORTC
00280A C060 B7 40C1 A STA CNTRLC ; ENABLE PORT B
00281A C063 B6 40C0 A LDA PORTC ; READ BACK PORT C
00282A C066 84 03 A ANDA #DREXNC ; MASK OUTPUT LINES
00283A C068 81 03 A CMPA #DREXNC ; IS DATA CORRECT?
00284A C06A 27 06 C072 BEQ RAMTST ; YES, THEN BRANCH.

```



```

00285A C06C 34 07 A FAULT5 PSHS B, A, CC ;PORT C RD/WR ERROR
00286A C06E CC 5505 A LDD ##5505 ;
00287A C071 3F SWI
00288 *
00289 *
00290 * RAM TEST
00291 * -----
00292 * EACH RAM LOCATION IS TESTED WITH AN AAH,
00293 * 55H DATA PATTERN. RAM IS THEN CLEARED.
00294A C072 C6 AA A RAMTST LDB #NTTRUE
00295A C074 108E 0080 A LDY ##0080
00296A C078 86 FF A AGAIN2 LDA ##FF
00297A C07A E7 A6 A AGAIN1 STB A, Y
00298A C07C E1 A6 A CMPB A, Y
00299A C07E 27 06 C086 BEQ OK6
00300 *
00301A C080 34 07 A FAULT6 PSHS B, A, CC ;BAD RAM LOCATION.
00302A C082 CC 5506 A LDD ##5506
00303A C085 3F SWI
00304A C086 4A OK6 DECA
00305A C087 26 F1 C07A BNE AGAIN1
00306A C089 C1 55 A CMPB #TRUE
00307A C08B 27 04 C091 BEQ CLRRAM ;RAM IS OK! CLEAR RAM.
00308A C08D C6 55 A LDB #TRUE
00309A C08F 20 E7 C078 BRA AGAIN2
00310 *
00311A C091 86 FF A CLRRAM LDA ##FF
00312A C093 108E 0080 A LDY ##0080
00313A C097 6F A6 A AGAIN8 CLR A, Y
00314A C099 4A DECA
00315A C09A 26 FB C097 BNE AGAIN8
00316 *
00317 * SELF-TEST
00318 * -----
00319 * JSR SELFTS
00320 *
00321 *

```

```

00323      *
00324      * INITIALIZE RAM
00325      * -----
00326A C09C C6   AA   A       LDB   #NTTRUE
00327A C09E F7   0010 P       STB   OVERLD
00328A C0A1 C6   B5   A       LDB   #$B5
00329A C0A3 F7   0003 P       STB   VNMNLI
00330      *
00331      * INITIALIZE CONVERTER OSC. DAC
00332      * -----
00333      *
00334A C0A6 CC   0000 A       LDD   #$0000
00335A C0A9 BD   C253 A       JSR   DACDRV   ; SEND 000H TO DAC.
00336      *
00337      *
00338      * READ BCD THUMBWHEEL SWITCHES
00339      * -----
00340A C0AC BD   C33C A       JSR   THUMB   ; READ BCD THUMB SWITCH
00341A C0AF B7   0005 P       STA   BCDVAL   ; SAVE IT
00342A C0B2 BD   C34A A       JSR   VALID   ; VERIFY BCD VALUE IS V
00343      *                               AND CONVERT IT TO BINARY.
00344      *                               ALSO LOOKUP INV. OUT VOLT
00345      *                               REF VALUE AND NORMALIZED
00346      *                               NUMBER FOR POWER CALCULAT.
00347      *
00348      *
00349      *
00350      *
00351      * READ FREQUENCY SWITCH
00352      * -----
00353A C0B5 C6   FF   A       LDB   #$FF   ; PREPARE TO SEND DATA
00354      *                               TO PORT B.
00355A C0B7 C4   FC   A       ANDB  #FREQL   ; CLEAR FREQ SELECT BIT
00356A C0B9 B6   8040 A       LDA   RE8     ; READ FREQ SWITCH
00357A C0BC 84   07   A       ANDA  #$07   ; MASK FREQ BITS
00358A C0BE B7   0008 P       STA   FQMODE  ; SAVE FREQ MODE
00359A C0C1 81   04   A       CMPA  #$04   ; IS IT 400HZ?
00360A C0C3 27   0E   COD3 BEQ   SET400  ; YES, THEN BRANCH.
00361A C0C5 81   02   A       CMPA  #$02   ; IS IT 60 HZ ?
00362A C0C7 27   0E   COD7 BEQ   SET60   ; YES, THEN BRANCH.
00363A C0C9 81   01   A       CMPA  #$01   ; IS IT 50 HZ ?
00364A C0CB 27   0E   CODB BEQ   SET50   ; YES, THEN BRANCH.
00365A C0CD 34   07   A FAULT7 PSHS  B, A, CC  ; BAD FREQ SWITCH
00366A C0CF CC   5507 A       LDD   #$5507 ;
00367A C0D2 3F                   SWI
00368      *
00369      *

```

```

00371          * OUTPUT FREQUENCY MODE SELECTION
00372          *-----*
00373A COD3 CA 02      A SET400 ORB      # 400HZ
00374A COD5 20 06      CODD          BRA      AHEAD1
00375A COD7 CA 01      A SET60  ORB      # 60HZ      ; OR BITS TO SLCT 60 HZ
00376A COD9 20 02      CODD          BRA      AHEAD1
00377A CODB CA 00      A SET50  ORB      # 50HZ      ; OR BITS TO SLCT 50 HZ
00378          *
00379A CODD C8 1C      A AHEAD1 EORB     #ENALL     ; EN CONV. OSC. CLOCKS
00380A CODF C8 40      A          EORB     #ENBLCV    ; EN DELCO CONVERTER SCR
00381          *                                     GATE DRIVER CIRCUITR
00382A COE1 F7 40A2    A          STB      PORTB     ; SEND ENABLE AND
00383          *                                     SELECT DATA.
00384          *
00385A COE4 C6 DC      A          LDB      ##DC
00386A COE6 F7 40A0    A          STB      PORTA     ; SELECT MUX2 TO CONVER
00387          *                                     OUTPUT VOLTAGE.
00388          *
00389          *
00390          * INCREASE CONVERTER OSC FREQ. TO PRODUCE
00391          * APPROX 100 VRMS AT INVERTER OUT AT NO LOAD.
00392          *-----*
00393A COE9 CC 0070    A          LDD      ##0070
00394A COEC BD C253    A          JSR      DACDRV
00395          *
00396          * ALLOW TIME FOR CONV. TO RESPOND TO NEW
00397          * OPERATING FREQUENCY.
00398          *-----*
00399A COEF B7 8005    A          STA      WE5       ; CLEAR COMM. FAIL INT.
00400A COF2 13          SYNC          ; WAIT FOR FIRQ, BUT
00401          *                                     DON'T SERVICE IT.
00402A COF3 C6 0A      A          LDB      ##0A
00403A COF5 BD C381    A          JSR      DELAY     ; DELAY AT LEAST 25 US.
00404          *                                     TO ALLOW INTRPT TO CLEAR.
00405          *
00406          *

```

```

00408 *****
00409 * MAIN EXECUTION ROUTINE
00410 *****
00411 *
00412 *
00413A COF8 1A 50 A MAIN ORCC ##50 ;DISABLE FIRQ AND IRQ
00414A COFA 7A 001C P DEC SERVIC ;IS IT TIME TO READ
00415 * THE FRONT PANEL?
00416A COFD 26 1B C11A BNE MAIN1 ;NO, THEN BRANCH.
00417A COFF BD C33C A JSR THUMB ;READ THUMB SWITCHES.
00418A C102 B1 0005 P CMPA BCDVAL ;DISTURBED?
00419A C105 27 03 C10A BEQ NOCHNG ;NO, THEN BRANCH.
00420A C107 BD C34A A JSR VALID ;VERIFY BCD AND CHANGE
00421 * REFERENCES.
00422 *
00423A C10A B6 8040 A NOCHNG LDA RE8 ;READ FREQ SWITCH.
00424A C10D 84 07 A ANDA ##07 ;MASK FREQ BITS.
00425A C10F B1 0008 P CMPA FQMODE ;CHANGED?
00426A C112 27 06 C11A BEQ MAIN1 ;NO, THEN BRANCH.
00427A C114 34 07 A FAULTD PSHS B, A, CC ;FREQ SWITCH CHANGED.
00428A C116 CC 550D A LDD ##550D ;
00429A C119 3F SWI
00430A C11A 1C AF A MAIN1 ANDCC ##AF ;ENABLE FIRQ AND IRQ.
00431A C11C 13 SYNC
00432A C11D 20 D9 COF8 BRA MAIN
00433 *
00434 * DATA PROCESSING ROUTINE AND CONV. OUT
00435 * CURRENT CHECK AND CONV
00436 * INPUT VOLTAGE CHECK WILL BE INSERTED.
00437 * LATER.

```

```

00439 *****
00440 * CONVERTER OPERATING CYCLE INTERRUPT ( FIRQ
00441 *****
00442 * THIS ROUTINE MEASURES THE CONVERTER
00443 * OUTPUT VOLTAGE AND DETERMINES THE
00444 * MAGNITUDE OF ERROR ( IF ANY ) FROM A
00445 * REFERENCE VALUE. THE REFERENCE VALUE
00446 * "VNOMNL" IS MAINTAINED AND
00447 * MODIFIED ONLY BY THE INVERTER OUTPUT
00448 * VOLTAGE MEASUREMENT ROUTINE.
00449 *
00450 * LARGE ERRORS ( >10% ) FROM NOMINAL WILL
00451 * BE CORRECTED BY CALCULATING CONV. OUT
00452 * POWER REQUIREMENTS.
00453 *
00454 *
00455 * SMALL ERROR CORRECTION
00456 * METHODS INVOLVE FEW CALCULATIONS.
00457 *
00458 * TO MINIMIZE POSSIBLE OVERTHOOT AND
00459 * UNDERSHOOT OF CONV OUT VOLTAGE, A 100%
00460 * CORRECTION IS NOT APPLIED IMMEDIATELY.
00461 * GENERALLY, LESS THAN 50% OF THE NECESSARY
00462 * CORRECTION IS MADE. THEREFORE, THIS ROUT-
00463 * INE WILL EXECUTE FIVE OR MORE TIMES
00464 * BEFORE THE ERROR BECOMES ZERO.
00465 *
00466 * DURING PERIODS OF CONVERTER OUTPUT VOLT-
00467 * AGE STABILITY ( ERRORS < 2 BITS ) THE
00468 * INVERTER OUT VOLT MEAS ROUTINE WILL BE
00469 * ALLOWED TO EXECUTE. AN INV OUT VOLT
00470 * ERROR WILL BE CORRECTED BY ADJUSTING
00471 * THE CONV OUT VOLT REFERENCE "VNOMNL".
00472 *
00473 * MEASURE CONVERTER OUTPUT VOLTAGE
00474 *-----*
00475 * MUX#2 IS SELECTED TO CONV OUT VOLT
00476 * AT ALL TIMES WHEN INTERRUPTS
00477 * ARE ENABLED.
00478 *
00479A C11F B6 40A2 A FIRQ LDA PORTB ;READ PORT B
00480A C122 88 80 A EORA #CNVRT2 ;CLR B7 ( CONVERT A/D#
00481A C124 B7 40A2 A STA PORTB ;HOLD ANALOG VALUE IN
00482 * *
00483 * *
00484A C127 F6 40C0 A WAIT1 LDB PORTC ;READ PORT C
00485A C12A C4 10 A ANDB #CMPLT2 ;HAS A/D#2 FINISHED?
00486A C12C 26 F9 C127 BNE WAIT1 ;NO, THEN WAIT.
00487 *
00488A C12E F6 8008 A LDB RE1 ;READ A/D#2
00489A C131 8A 80 A DRA #CNVRT2 ;RETURN CONVERT A/D#2
00490A C133 B7 40A2 A STA PORTB ;BLANK A/D#2 OUTPUTS A
00491 * *
00492A C136 F7 0001 P STB VMEASR ;SAVE CONV. OUT VOLT
00493 * *

```

```

00495      *DETERMINE MAGNITUDE AND POLARITY OF CONV
00496      * OUTPUT VOLTAGE ERROR.
00497      *
00498A C139 F0 0003 P SUBB VNONML ; DOES MEAS= NOMINAL?
00499A C13C 27 17 C155 BEQ NOAJST ; YES, THEN DON'T ADJUST
00500A C13E 2D 05 C145 BLT TOOLOW ; BRANCH IF LOW.
00501      *
00502A C140 7F 0004 P TOOHI CLR PLARTY ; INDICATE CONV VOLT HI
00503A C143 20 06 C14B BRA DTERM
00504      *
00505A C145 50 TOOLOW NEGB ; 2'S CMLPMNT NEG VAL
00506A C146 86 FF A LDA #FF
00507A C148 B7 0004 P STA PLARTY ; INDICATE CONV VOLT LO
00508      *
00509      *
00510      * DETERMINE IF ERROR IS LARGE OR SMALL
00511      *
00512A C14B C1 14 A DTERM CMPB #14 ; IS ERROR > 20 BITS? (
00513A C14D 2A 7D C1CC BPL LRGERR ; YES, ADJ FOR LRG ERR.
00514      *
00515A C14F 58 SMLERR LSLB ; MLTPLY ERR BITS BY 2
00516A C150 8E C46F A LDX #TABLE2
00517A C153 6E 95 A JMP [B,X] ; JMP TO ADDR OF AJST
00518      * ROUTINE.
00519      *
00520      *
00521      * NO ADJUSTMENT TO CONVERTER OPERATING FREQ.
00522      *
00523A C155 B6 0006 P NOAJST LDA STABLE ; LOOK AT COUNT.
00524A C158 81 03 A CMPA #03 ; HAS CONV OUT VOLT ERR
00525      * REMAINED SMALL FOR 3
00526      * CONSEC OPERATING CYC.
00527A C15A 102C 0259 C3B7 LBGE INVOUT ; YES, THEN BRANCH.
00528A C15E 7C 0006 P INC STABLE
00529A C161 16 00EE C252 LBRA EXIT
00530      *
00531      *
00532      * ADJUST ROUTINES
00533      *
00534      *
00535      * CORRECT FOR .5% ( 1 BIT ) ERROR ;
00536      *
00537      * THE CORRECTION IS MADE BY ADJUSTING
00538      * THE CONVERTER OSCILLATOR
00539      * FREQUENCY BY .1%. 1/1024 = .1% APPROX.
00540A C164 F6 0009 P E. 1PC LDB DACVAL ; LOAD MS BYTE .
00541A C167 54 LSRB ; MOVE BIT 8 TO CARRY.
00542      * IS IT SET?
00543A C168 24 34 C19E BCC ADJUST ; NO, THEN BRANCH.
00544A C16A 5C INCB ; ROUND OFF.
00545A C16B 20 31 C19E BRA ADJUST ; THE RESULT OF THE DIV /
00546      * BY 1024 IS IN ACC. B
00547      *
00548      *
00549      * CORRECT FOR 1% ( 2 BIT ) ERROR.
00550      *
00551A C16D F6 0009 P E. 2PC LDB DACVAL ; LOAD MS BYTE OF DACVA
00552A C170 7D 000A P TST DACVAL+1 ; IS B7 OF LS BYTE SET?

```

```

00553A C173 2A 29 C19E BPL ADJUST ; NO, THEN BRANCH.
00554A C175 5C INCB ; YES, ROUND OFF.
00555A C176 20 26 C19E BRA ADJUST ; RESULT OF DIV BY 512
00556 * IS IN ACCUMULATOR B.
00557 *
00558 *
00559A C178 86 01 A E. 4PC LDA ##01 ; PREPARE TO DIV BY 256
00560A C17A 20 0C C188 BRA AHEADB
00561 *
00562 *
00563A C17C 86 02 A E. 8PC LDA ##02 ; PREPARE TO DIV BY 128
00564A C17E 20 08 C188 BRA AHEADB
00565 *
00566 *
00567A C180 86 03 A E1. 5PC LDA ##03 ; PREPARE TO DIV BY 64.
00568A C182 20 04 C188 BRA AHEADB
00569 *
00570 *
00571A C184 86 04 A E3. 1PC LDA ##04 ; PREPARE TO DIV BY 32.
00572A C186 20 00 C188 BRA AHEADB
00573 *
00574 *
00575A C188 7F 0006 P AHEADB CLR STABLE ; ERROR IS SIGNIFICANT
00576 * VOLTAGE CAN NOT BE
00577 * CONSIDERED STABLE.
00578A C18B B7 000D P STA COUNT1
00579 *
00580 * SHIFT
00581 *-----
00582 * COUNT1 SPECIFIES THE NUMBER OF PLACES TO
00583 * SHIFT THE ACC. D TO THE LEFT.
00584 * THE VALUE IN ACC. A BECOMES THE
00585 * CORRECTION TO BE APPLIED TO DAC.
00586A C18E FC 0009 P SHIFT LDD DACVAL
00587A C191 58 AGAIN3 LSLB
00588A C192 49 ROLA
00589A C193 7A 000D P DEC COUNT1
00590A C196 26 F9 C191 BNE AGAIN3
00591A C198 1E 89 A EXG A, B
00592A C19A 4D TSTA ; IS BIT 7 SET?
00593A C19B 2A 01 C19E BPL ADJUST ; NO, THEN BRANCH.
00594A C19D 5C INCB ; ROUND OFF.

```

```

00596      *
00597      * ADJUST ;
00598      *-----
00599      * ACCUM B CONTAINS THE CORRECTION TO BE
00600      * APPLIED TO THE PRESENT DAC VALUE.
00601      *
00602A C19E 4F      ADJUST CLRA
00603A C19F FD      000B   P   STD   SAVE1   ; SAVE CALCULATED CORRE
00604A C1A2 27      16   C1BA  BEQ   ZERO   ; BRA IF CORRECTION =0
00605A C1A4 FC      0009   P   LDD   DACVAL
00606A C1A7 7D      0004   P   TST   PLARTY  ; IS DAC VALUE TOO HIGH
00607      *                               TOO LOW?
00608A C1AA 27      05   C1B1  BEQ   REDUCE  ; BRANCH IF TOO HIGH.
00609      *
00610A C1AC F3      000B   P   INCRS ADDD   SAVE1   ; ADD CORRECTION.
00611A C1AF 20      03   C1B4  BRA   LOADAC
00612      *
00613A C1B1 B3      000B   P   REDUCE SUBD   SAVE1   ; SUBTRACT CORRECTION.
00614      *
00615A C1B4 BD      C253   A   LOADAC JSR   DACDRV  ; SEND NEW VAL TO DAC
00616A C1B7 16      0098 C252  LBRA  EXIT
00617      *
00618      *
00619      * ZERO
00620      * -----
00621      * CALCULATED CORRECTION IS LESS THAN 1 BIT.
00622      * ADD OR SUBTRACT A BIT ANYWAY.
00623A C1BA FC      0009   P   ZERO   LDD   DACVAL
00624A C1BD 7D      0004   P   TST   PLARTY
00625A C1C0 27      05   C1C7  BEQ   SUBTR1
00626      *
00627      *
00628A C1C2 C3      0001   A   ADD1   ADDD   #$0001
00629A C1C5 20      ED   C1B4  BRA   LOADAC
00630      *
00631      *
00632A C1C7 83      0001   A   SUBTR1 SUBD   #$0001
00633A C1CA 20      E8   C1B4  BRA   LOADAC
00634      *
00635      *

```



```

00637      *
00638      *
00639      *
00640      *****
00641      * LARGE ERROR ;
00642      *-----*
00643      *
00644      *   THIS ROUTINE DETERMINES A NEW CONV. OSC.
00645      *   DAC VALUE BASED ON POWER REQUIREMENTS.
00646      *
00647      *
00648A C1CC 7F 0006 P LRGERR CLR STABLE ; DUE TO UNSTABLE LOAD
00649      * ; CLEAR STABLE.
00650A C1CF BD C2F5 A JSR MEASR1 ; MEASURE INV INP CURR
00651      * ; CONV OUT VOLTAGE.
00652A C1D2 F6 0003 P LDB VNMNL ; GET CONV VOLT REF
00653A C1D5 F0 0001 P SUBB VMEASR ; DETERMINE DIFFERENCE
00654      * ; FROM MEASURED VALUE.
00655A C1D8 2C 0C C1E6 BGE LOW ; BRA IF CONV VOLT LOW
00656A C1DA 50 NEGB ; CONV VOLT IS HIGH
00657A C1DB 7D 0004 P TST PLARTY ; DOES POLARITY AGREE
00658      * ; WITH PREVIOUS MEASUREMENT
00659A C1DE 27 0D C1ED BEQ AHEAD4 ; YES, THEN BRANCH.
00660A C1E0 34 07 A FAULT9 PSHS B, A, CC ; POLARITY OF CONV OUT
00661      * ; VOLTAGE ERROR CHANGED
00662A C1E2 CC 5509 A LDD ##5509 ;
00663A C1E5 3F SWI
00664      *
00665      *
00666A C1E6 7D 0004 P LOW TST PLARTY ; DOES POLARITY AGREE
00667      * ; WITH PREVIOUS MEASURE
00668A C1E9 26 02 C1ED BNE AHEAD4 ; YES, THEN BRANCH.
00669A C1EB 20 F3 C1E0 BRA FAULT9
00670      *
00671      *
00672      *
00673A C1ED C0 10 A AHEAD4 SUBB ##10 ; ERR > 15 BITS? (7.5%)
00674A C1EF 2E 06 C1F7 BGT CALCUL ; YES, CALCULATE POWER
00675      * ; REQUIREMENTS.
00676      *
00677A C1F1 34 07 A FAULTA PSHS B, A, CC ; ERR HAS DECREASED BY
00678      * ; MORE THAN 5 BITS FROM
00679      * ; PREVIOUS MEASUREMENT.
00680      * ; THIS INDICATES NON-R
00681      * ; ABILITY OF MEASUREMENT
00682A C1F3 CC 550A A LDD ##550A ;
00683A C1F6 3F SWI
00684      *
00685      *

```

```

00687 *
00688 *
00689 *****
00690 * CALCULATE POWER REQUIREMENTS
00691 * -----
00692 *
00693 *
00694 * PREQ = ( VNOM / VMEAS ) X (IMEAS)X(RATIO )
00695 * PREQ = CONV OUT POWER REQUIRED
00696 * VNOM = CONV OUT VOLT NOMINAL
00697 * IMEAS = INV INPUT CURR MEASURED
00698 * VMEAS = CONV OUT VOLT MEASURED
00699 * RATIO = NORMALIZED VALUE. IF DESIRED
00700 *         INV OUT VOLT IS 120VRMS THEN
00701 *         RATIO = 1.00
00702 *
00703A C1F7 7F 0002 P CALCUL CLR DVIDND
00704A C1FA 7F 0000 P CLR DVISOR
00705A C1FD 8E 0000 P LDX #DVISOR ;POINT TO CONV OUT VOL
00706 * MEASURED VALUE.
00707A C200 108E 0002 P LDY #DVIDND ;POINT TO CONV OUT VOL
00708 * REFERENCE VALUE.
00709A C204 BD C2C7 A JSR DIVIDE ;VNOMNL DIV BY VMEASR
00710 * PRODUCES 8 BIT QUOTIEN
00711 * AND 8 BIT REMAINDER.
00712A C207 FC 000E P LDD IMEASR
00713A C20A BD C292 A JSR MLTPLY ;IMEASR X QUOTIENT
00714 * AND REMAINDER.
00715 *
00716 *
00717A C20D FC 0019 P LDD RATIO
00718A C210 B7 0013 P STA QUOTNT
00719A C213 F7 0014 P STB REMNDR
00720A C216 FC 0015 P LDD RESULT
00721A C219 BD C292 A JSR MLTPLY
00722A C21C 1E 89 A EXG A, B
00723A C21E 49 ROLA
00724A C21F 59 ROLB
00725A C220 49 ROLA
00726A C221 84 01 A ANDA #$01
00727A C223 8E CC00 A GETVAL LDX #TABLE3
00728A C226 31 8B A LEAY D, X
00729A C228 E6 A4 A LDB ,Y ;LOAD LOWER 8 BITS OF
00730 * 11 BIT DAC VALUE.
00731A C22A 4F CLRA ;CLEAR UPPER BITS.
00732A C22B 8E CD05 A LDX #TABLE5 ;PREPARE TO DETERMINE
00733 * UPPER 3 BITS.
00734 *
00735A C22E 10AC 81 A TRYAGN CMPY ,X++
00736A C231 2D 03 C236 BLT AHED1
00737A C233 4C INCA
00738A C234 20 F8 C22E BRA TRYAGN
00739 *
00740 *
00741 *INSERT ROUTINE TO APPLY
00742 *A CORRECTION FACTOR IF CONV INPUT VOLT ABNOR
00743 *
00744A C236 108E 0009 P AHED1 LDY #DACVAL ;POINT TO OLD DAC VALU

```

```

00745A C23A 10A3 A4 A CMPD ,Y ;VAL < OR > OLD VAL?
00746A C23D 2E 0A C249 BGT AHEAD5 ;BRA IF GREATER THAN.
00747A C23F FD 000B P STD SAVE1
00748A C242 108E 000B P LDY #SAVE1
00749A C246 FC 0009 P LDD DACVAL
00750 *
00751 *
00752A C249 A3 A4 A AHEAD5 SUBD ,Y ; DIFFERENCE BETWEEN VA
00753 * ; AND OLD DAC VALUE.
00754A C24B 44 LSRA
00755A C24C 56 RORB ; DIV DIFFERENCE BY 2.
00756A C24D E3 A4 A ADDD ,Y ; APPLY 50% CORRECTION
00757A C24F BD C253 A JSR DACDRV ; SEND ACC. D TO DAC.
00758 *
00759 *
00760 *
00761 *****
00762 * EXIT
00763 * ----
00764 *
00765A C252 3B EXIT RTI
00766 *
00767 *
00768 *
00769 *
00770 *
00771 *
00772 *****
00773 * DAC DRIVER
00774 * -----
00775 *
00776 *
00777A C253 FD 0009 P DACDRV STD DACVAL ; SAVE CORRECTED DAC
00778 * ; VALUE.
00779A C256 81 04 A CMPA ##04 ; DACVAL EXCEED 3FFH?
00780A C258 2C 1B C275 BGE ACTVAT ; YES, ACTVAT 33KHZ OFSE
00781A C25A B6 0010 P LDA OVERLD ; NO, EXAMINE OVERLD FLG
00782A C25D 81 55 A CMPA #TRUE ; IS OVERLOAD MODE SET?
00783A C25F 27 25 C286 BEQ REMOVE ; YES, REMOVE 33KHZ OFST
00784 * ; AND IGNORE TIMER.
00785A C261 81 AA A CMPA #NTRUE ; IS OVERLD NOT SET?
00786A C263 27 06 C26B BEQ SENDIT ; YES, THEN BRANCH.
00787A C265 34 07 A FAULTB PSHS B, A, CC ; OVERLD MEM LOC. OR
00788 * ; DATA BUS IS BAD.
00789A C267 CC 550B A LDD ##550B ;
00790A C26A 3F SWI
00791 *
00792 *
00793A C26B FC 0009 P SENDIT LDD DACVAL
00794A C26E FD 8000 A STD WE0 ; LOAD DAC BUFFER.
00795A C271 B7 8004 A STA WE4 ; XFER DAC BUFF TO DAC.
00796A C274 39 RTS
00797 *
00798 *
00799A C275 BD C26B A ACTVAT JSR SENDIT ; SEND DAC VALUE FIRST
00800 * ; BEFORE APPLYING 33KHZ OFFSET.
00801A C278 B6 40A2 A LDA PORTB ; READ PORT B
00802A C27B 84 DF A ANDA ##DF ; CLEAR PB5

```

```

00803A C27D B7 40A2 A STA PORTB ;ACTIVATE 33KHZ OFFSET
00804A C280 86 55 A LDA #TRUE ;SET OVERLD FLAG.
00805A C282 B7 0010 P STA OVERLD ;SET OVERLD FLAG.
00806 *
00807 *
00808 * INSERT ROUTINE TO START OR MAINTAIN TIME
00809 *
00810A C285 39 RTS
00811 *
00812 *
00813A C286 B6 40A2 A REMOVE LDA PORTB ;READ PORT B
00814A C289 8A 20 A ORA #33KHZ ;SET PB5
00815A C28B B7 40A2 A STA PORTB ;DEACTIVATE 33KHZ OFFS
00816A C28E BD C26B A JSR SENDIT ;SEND DAC VALUE TO DAC
00817 *
00818 * INSERT ROUTINE TO STOP TIMER SINCE OVERLOA
00819 * DEACTIVATED.
00820 *
00821A C291 39 RTS
00822 *
00823 *
00824 *
00825 *****
00826 * MULTIPLY
00827 * -----
00828 * THIS SUBROUTINE WILL MULTIPLY THE VALUE IN
00829 * ACC. D BY "QUOTNT" AND "REMNR".
00830 *
00831A C292 FD 0011 P MLTPLY STD MLTCAN
00832A C295 7D 0013 P TST QUOTNT ;IS QUOTIENT ZERO?
00833A C298 27 0A C2A4 BEQ AHEAD6 ;YES, THEN BRANCH.
00834 *
00835A C29A 7A 0013 P AGAIN4 DEC QUOTNT
00836A C29D 27 0D C2AC BEQ AGAIN5
00837A C29F F3 0011 P ADDD MLTCAN
00838A C2A2 20 F6 C29A BRA AGAIN4
00839 *
00840A C2A4 FD 0015 P AHEAD6 STD RESULT
00841A C2A7 CC 0000 A LDD #$0000
00842A C2AA 20 03 C2AF BRA AHEAD7
00843 *
00844A C2AC FD 0015 P AGAIN5 STD RESULT
00845 *
00846A C2AF 74 0015 P AHEAD7 LSR RESULT
00847A C2B2 76 0016 P ROR RESULT+1
00848A C2B5 78 0014 P LSL REMNR
00849A C2B8 25 04 C2BE BCS AHEAD8
00850A C2BA 27 07 C2C3 BEQ FINISH
00851A C2BC 20 F1 C2AF BRA AHEAD7
00852 *
00853 *
00854A C2BE F3 0015 P AHEAD8 ADDD RESULT
00855A C2C1 20 EC C2AF BRA AHEAD7
00856 *
00857A C2C3 FD 0015 P FINISH STD RESULT
00858A C2C6 39 RTS
00859 *
00860 *

```

```

00861      *
00862      *****
00863      * DIVIDE
00864      * -----
00865      * THE X REG POINTS TO 2 BYTE DIVISOR
00866      * THE Y REG POINTS TO 2 BYTE DIVIDEND
00867      * THE RESULT OF DIVISION WILL BE STORED
00868      * IN TWO LOCATIONS. "QUOTNT"= WHOLE UNITS
00869      * "REMNRD"= FRACTION
00870      *
00871A C2C7 7F 0014 P DIVIDE CLR REMNRD
00872A C2CA 7F 0013 P CLR QUOTNT ;
00873A C2CD 86 08 A LDA #$08 ;
00874A C2CF B7 000D P STA COUNT1 ;
00875A C2D2 EC A4 A LDD ,Y ;LOAD DIVIDEND
00876A C2D4 10A3 84 A DIVID1 CMPD ,X ;COMPARE DIVISOR
00877A C2D7 2B 11 C2EA BMI NOINCR ;BRA IF DIVIDND<DIVISOR
00878A C2D9 A3 84 A SUBD ,X ;SUBTRACT DIVISOR
00879A C2DB 7C 0013 P INC QUOTNT ;
00880A C2DE 20 F4 C2D4 BRA DIVID1 ;
00881      *
00882A C2E0 10A3 84 A DIVID2 CMPD ,X ;COMPARE DIVISOR
00883A C2E3 2B 05 C2EA BMI NOINCR ;
00884A C2E5 A3 84 A SUBD ,X ;
00885A C2E7 7C 0014 P INC REMNRD ;
00886      *
00887A C2EA 78 0014 P NOINCR LSL REMNRD ;MULT REMNRD BY 2
00888A C2ED 58 LSLB
00889A C2EE 49 ROLA ;MULT DIVIDND BY 2
00890A C2EF 7A 000D P DEC COUNT1 ;
00891A C2F2 26 EC C2E0 BNE DIVID2 ;
00892A C2F4 39 RTS
00893      *
00894      *
00895      *
00896      *
00897      *
00898      *
00899      *****
00900      * MEASURE1
00901      *
00902      * THIS SUBROUTINE MEASURES INV INPUT CURR AND
00903      * CONVERTER OUTPUT VOLTAGE, SIMULTANEOUSLY.
00904      *
00905A C2F5 86 D8 A MEASR1 LDA #$D8
00906A C2F7 B7 40A0 A STA PORTA
00907A C2FA 86 01 A LDA #$01
00908A C2FC B7 40C0 A STA PORTC
00909A C2FF B6 40A2 A LDA PORTB
00910A C302 88 80 A EDRA #CNVRT2
00911A C304 C6 07 A LDB #$07
00912A C306 BD C381 A JSR DELAY
00913A C309 7F 40C0 A CLR PORTC
00914A C30C B7 40A2 A STA PORTB
00915      *
00916A C30F F6 40C0 A AGAIN7 LDB PORTC
00917A C312 C4 18 A ANDB #$18
00918A C314 26 F9 C30F BNE AGAIN7

```

```

00919A C316 86 06 A LDA #06
00920A C318 B7 000D P STA COUNT1
00921A C31B F6 8010 A LDB RE2 ; A/D#1 LO BYTE
00922A C31E B6 8018 A LDA RE3 ; A/D#1 HI BYTE
00923 *
00924 *
00925A C321 C4 C0 A ANDB #C0
00926A C323 58 LSLB
00927A C324 49 ROLA
00928A C325 FD 000E P STD IMEASR
00929A C328 F6 8008 A LDB RE1
00930A C32B F7 0001 P STB VMEASR
00931A C32E B6 40A2 A LDA PORTB
00932A C331 8A 80 A ORA #CNVRT2
00933A C333 B7 40A2 A STA PORTB ; BLANK A/D#2 OUTPUTS, S
00934A C336 86 03 A LDA #03
00935A C338 B7 40C0 A STA PORTC ; BLANK A/D#1 OUTPUTS, S
00936 * 10 DEGREE MODE.
00937A C33B 39 RTS
00938 *
00939 *
00940 *
00941 *
00942 *
00943 *****
00944 * READ BCD THUMBWHEEL SWITCHES
00945 * -----
00946A C33C B6 8038 A THUMB LDA RE7 ; READ 2ND AND 3RD DIGI
00947A C33F 81 39 A CMPA #HILIM ; DOES SETTING EXCEED M
00948A C341 2E 01 C344 BGT FAULT1 ; YES, THEN BRANCH.
00949A C343 39 RTS
00950 *
00951A C344 34 07 A FAULT1 PSHS B, A, CC ; SWITCH EXCEEDS MAX LI
00952A C346 CC 5501 A LDD #5501 ; ERROR 1
00953A C349 3F SWI
00954 *
00955 * VERIFY BCD VALUE IS VALID
00956 * -----
00957A C34A 1F 89 A VALID TFR A, B
00958A C34C 84 0F A ANDA #0F ; MASK 3RD DIGIT.
00959A C34E 81 0A A CMPA #0A ; IS IT WITHIN THE DECI
00960A C350 2D 06 C358 BLT BINARY ; YES, THEN BRANCH.
00961 *
00962A C352 34 07 A FAULT2 PSHS B, A, CC ; BCD SWITCH SENT AN IN
00963A C354 CC 5502 A LDD #5502 ; ERROR 2
00964A C357 3F SWI
00965 *
00966 * CONVERT BCD TO BINARY
00967 * -----
00968A C358 C4 F0 A BINARY ANDB #F0
00969A C35A 27 06 C362 BACK1 BEQ LOOKUP
00970A C35C 8B 0A A ADDA #0A ; ADD 10 BITS TO 3RD DI
00971 * EACH
00972A C35E C0 10 A SUBB #10
00973A C360 20 F8 C35A BRA BACK1
00974 *
00975 *
00976 * LOOKUP INV. OUTPUT VOLT REF VALUE

```

```

00977
00978A C362 B7 000B P LOOKUP STA SAVE1 ;SAVE BCD SWITCH BINAR
00979A C365 8E 0447 A LDX #TABLE1 ;BEGINNING ADDR OF TAB
00980A C368 E6 86 A LDB A,X ;FIND INV OUT VOLT REF
00981A C36A 86 01 A LDA ##01
00982A C36C FD 0017 P STD REFRNC
00983
00984 * LOOKUP NORMALIZED NUMBER FOR POWER CALCULAT
00985
00986A C36F 8E 0499 A LDX #TABLE4
00987A C372 B6 000B P LDA SAVE1 ;RETRIEVE BCD SWITCH B
00988A C375 E6 86 A LDB A,X ;FIND NORMALIZED RATIO
00989A C377 4F CLRA
00990A C378 C1 50 A CMPB ##50
00991A C37A 2E 01 C37D BGT AHEADC
00992A C37C 4C INCA
00993A C37D FD 0019 P AHEADC STD RATIO ;SAVE IT.
00994A C380 39 RTS
00995
00996
00997
00998 *****
00999 * DELAY
01000 * -----
01001
01002A C381 12 DELAY NOP
01003A C382 12 NOP
01004A C383 5A DECB
01005A C384 26 FB C381 BNE DELAY
01006A C386 39 RTS
01007
01008
01009 *****
01010 * COMMUTATION FAIL INTERRUPT SERVICE ROUTINE
01011
01012A C387 B6 40C0 A IRQ LDA PORTC ;READ PORT C
01013A C38A 84 E0 A ANDA #COMFAL ;MASK FAIL BITS.
01014A C38C 88 E0 A EORA #COMFAL ;IDENTIFY FAILING PHAS
01015A C38E B7 001B P STA FAILST ;SAVE FAIL STATUS
01016A C391 B6 40A2 A LDA PORTB
01017A C394 9A 40 A ORA ENBLCV
01018A C396 B7 40A2 A STA PORTB DISABLE CONVERTER
01019 *****
01020
01021 * THE FOLLOWING IS A 22 MILLISECOND DELAY
01022 * ROUTINE BEFORE RE-ENABLING THE
01023 * CONVERTER AFTER A COMMUTATION FAILURE.
01024
01025 *****
01026A C399 86 65 A LDA ##65 LOAD TIMER VARIABLE
01027A C39B 5F CLRB CLEAR NMBR TMS REG.
01028A C39C 8E 001B A CYCLE LDX ##001B LOAD TIMING CONSTANT
01029A C39F 30 1F A AGN LEAX -1,X DEC X REG
01030A C3A1 26 FC C39F BNE AGN CYCLE COMPLETED?
01031A C3A3 5C INCB
01032A C3A4 34 04 A PSHS B
01033A C3A6 A1 E0 A CMPA ,S+
01034A C3A8 26 F2 C39C BNE CYCLE NO TIME OUT?

```

```

01035
01036A C3AA 96 40 A LDA ENBLCV
01037A C3AC 43 COMA
01038A C3AD B4 40A2 A ANDA PORTB
01039A C3B0 B7 40A2 A STA PORTB ENABLE CONVERTER
01040A C3B3 B7 8005 A STA WES ; CLEAR COMM FAIL INTRP
01041A C3B6 3B RTI
01042 *
01043 *
01044 *
01045 *****
01046 * INVERTER OUTPUT VOLTAGE MEASUREMENT ROUTINE
01047 *
01048 *
01049A C3B7 7D 0007 P INVOUT TST LOKOUT
01050A C3BA 1026 FE94 C252 LBNE EXIT
01051 *
01052 *
01053 *
01054 * REST OF ROUTINE GOES HERE.
01055 *
01056A C3BE 16 FE91 C252 LBRA EXIT
01057 *
01058 *
01059A C3C1 CC 550F A NMI LDD #$550F ; NMI WARNING
01060 *
01061 * POWER SUPPLY FAILURE INT ROUT WILL
01062 * REPLACE THIS ERROR ROUTINE.
01063 *
01064A C3C4 3F SWI
01065 *
01066 *
01067 *
01068A C3C5 CC 550E A FAULTE LDD #$550E ; ILLEGAL SM ERR JMP
01069A C3C8 3F SWI
    
```



```

01071 *
01072 *****
01073 * SOFTWARE INTERRUPT ROUTINE
01074 *
01075 * THIS ROUT WILL SERVICE AN INTRPT GENERATED
01076 * DUE TO A FAULT CONDITION. THE VAL IN ACC B
01077 * IDENTIFIES THE FAULT. THE CC, A AND B REG
01078 * WERE SAVED ON THE STACK. THE ABOVE REG WILL
01079 * BE FORMATTED AND DISPLAYED.
01080 *
01081 *          REGISTER      [ FAULT ][ CC ][ A ][ B ]
01082 *          -----
01083 *          ! ! ! ! ! ! ! !
01084 *          -----
01085 *          POSITION      1 2 3 4 5 6 7 8
01086 *
01087 *
01088 * THE DISPLAY WILL NOT BE CLEARED AND NORMAL
01089 * EXECUTION WILL NOT RESUME UNTIL THE USER HAS
01090 * DEPRESSED THE SENSE SWITCH.
01091 *
01092 *
01093 *
01094 * FAULT1= BCD SWITCH SETTING EXCEEDS MAX LIM
01095 * FAULT2= BCD SWITCH SENT ILLEGAL CODE
01096 * FAULT3= PORT A READ/WRITE ERR
01097 * FAULT4= PORT B READ/WRITE ERROR
01098 * FAULT5= PORT C READ/WRITE ERROR
01099 * FAULT6= BAD RAM LOCATION
01100 * FAULT7= BAD FREQ SWITCH
01101 * FAULT8= NOT USED
01102 * FAULT9= NON-REPEATABILITY OF MEASUREMENT
01103 * FAULTA= NON-REPEATABILITY OF MEASUREMENT
01104 * FAULTB= DATA BUS OR OVRLO MEM LOC BAD
01105 * FAULTC= NOT USED
01106 * FAULTD= FREQ SWITCH CHANGED
01107 * FAULTE= ILLEGAL SM ERR JMP
01108 * FAULTF= NMI INTERRUPT
01109 *
01110 *
01111A C3C9 30 6C A SWINT LEAX $OC, S ; ADDRESS OF 12TH BYTE
01112 * ; INTO STACK.
01113A C3CB 108E 001D P LDY #MESSBF
01114A C3CF E7 A0 A STB ,Y+ ; STORE FAULT CODE IN
01115 * ; MESSAGE BUFFER.
01116A C3D1 E6 80 A LDB ,X+
01117A C3D3 E7 A0 A STB ,Y+ ; PUT PRE-INT COND CODE
01118 * ; INTO MESSAGE BUFFER.
01119A C3D5 EC 84 A LDD ,X
01120A C3D7 ED A4 A STD ,Y ; PUT ACC. A AND ACC. B
01121 *
01122A C3D9 B6 40A2 A LDA PORTB ;
01123A C3DC 9A 40 A ORA ENBLOC ; SET CONV ENBL BIT
01124A C3DE B7 40A2 A STA PORTB ; DISABLE CONV
01125 *
01126A C3E1 BD C3ED A JSR SETUP ; TRANSLATE MESSAGE
01127A C3E4 BD C412 A JSR PRINT ; DISPLAY ALL CHARCTRS
01128A C3E7 BD C420 A JSR SENSE ; WAIT FOR SENSE SWITCH

```

```

01129A C3EA 7E 0000 A JMP RESTRT
01130 *
01131 *
01132 *
01133 * SETUP
01134 * -----
01135 * TRANSLATE MESSAGE INTO CHARACTER CODE
01136 *
01137A C3ED 86 04 A SETUP LDA #$04 COUNT1
01138A C3EF 8E 001D P LDX #MESSBF
01139A C3F2 CE C42D A LDU #DSPTBL
01140A C3F5 108E 0021 P LDY #DSPBUF
01141A C3F9 B7 000D P STA COUNT1
01142 *
01143A C3FC E6 80 A LOOP4 LDB ,X+
01144A C3FE 1F 98 A TFR B,A
01145A C400 44 LSRA
01146A C401 44 LSRA
01147A C402 44 LSRA
01148A C403 44 LSRA
01149A C404 C4 0F A ANDB #$0F
01150A C406 A6 C6 A LDA A,U
01151A C408 E6 C5 A LDB B,U
01152A C40A ED A1 A STD ,Y++
01153A C40C 7A 000D P DEC COUNT1
01154A C40F 26 EB C3FC BNE LOOP4
01155A C411 39 RTS
01156 *
01157A C412 8E 0021 P PRINT LDX #DSPBUF
01158A C415 C6 08 A LDB #$08
01159A C417 A6 80 A PRINT8 LDA ,X+
01160A C419 B7 4000 A STA DSPLYD
01161A C41C 5A DECB
01162A C41D 26 F8 C417 BNE PRINT8
01163A C41F 39 RTS
01164 *
01165A C420 B6 8040 A SENSE LDA RES
01166A C423 84 08 A ANDA #$08 ; IS SENSE SWITCH DEPRES
01167A C425 27 F9 C420 BEQ SENSE ; NO, THEN WAIT.
01168A C427 86 DF A LDA #CLRDIS
01169A C429 B7 4001 A STA DSPLYC ; CLEAR DISPLAY
01170A C42C 39 RTS
01171 *****
01172 * THIS INDICATES SEGMENT VS. BIT POSITION
01173 * IN LABEL "DSPLYD".
01174
01175 * "DSPLYD" MSB, -, -, -, -, -, -, LSB
01176 * SEGMENT D C, B, A, , G, F, E
01177
01178 * NOTE: A ZERO IN A BIT
01179 * POSITION TURNS ON THE
01180 * CORRESPONDING LED SEGMENT.
01181 * B3 POSITION IS DEC. POINT.
01182 *
01183 *
01184 *
01185 *
01186 *

```

01187		* DISPLAY CHARACTER TABLE			
01188		*			
01189A	C42D	0C	A DSPTBL	FCB	\$0C ; 0
01190A	C42E	9F	A ONE	FCB	\$9F ;
01191A	C42F	4A	A TWO	FCB	\$4A ;
01192A	C430	0B	A THREE	FCB	\$0B ; 3
01193A	C431	99	A FOUR	FCB	\$99 ; 4
01194A	C432	29	A FIVE	FCB	\$29 ; 5
01195A	C433	28	A SIX	FCB	\$28 ; 6
01196A	C434	8F	A SEVEN	FCB	\$8F ; 7
01197A	C435	08	A EIGHT	FCB	\$08 ; 8
01198A	C436	89	A NINE	FCB	\$89 ; 9
01199A	C437	88	A LETTERA	FCB	\$88 ; A
01200A	C438	38	A LETTRB	FCB	\$38 ; B (LOWER CASE)
01201A	C439	6C	A LETTRC	FCB	\$6C ; C
01202A	C43A	1A	A LETTRD	FCB	\$1A ; D (LOWER CASE)
01203A	C43B	68	A LETTRE	FCB	\$68 ; E
01204A	C43C	E8	A LETTRF	FCB	\$E8 ; F
01205A	C43D	98	A LETTRH	FCB	\$98 ; H
01206A	C43E	1A	A LETTRJ	FCB	\$1A ; J
01207A	C43F	7C	A LETTRL	FCB	\$7C ; L
01208A	C440	08	A LETTRP	FCB	\$08 ; P
01209A	C441	9F	A LETTRI	FCB	\$9F ; I
01210A	C442	BA	A LETTRN	FCB	\$BA ; N (LOWER CASE)
01211A	C443	FA	A LETTRR	FCB	\$FA ; R (LOWER CASE)
01212A	C444	1C	A LETTRU	FCB	\$1C ; U
01213A	C445	FF	A BLANK	FCB	\$FF ; BLANK
01214A	C446	F7	A POINT	FCB	\$F7 ; DECIMAL POINT
01215			*		
01216			*		
01217			*		

01219
 01220
 01221
 01222
 01223
 01224

```

*
*****
* TABLE 1 ; INVERTER OUTPUT VOLTAGE REF TABLE
* ALL VALUES ARE PRECEDED BY A "1".
* 1FFH = 210 VOLTS PEAK
*
    
```

01225A	C447	58	A	TABLE1	FCB	\$58	; 100VRMS, 141.42 V PK
01226A	C448	5C	A		FCB	\$5C	
01227A	C449	5F	A		FCB	\$5F	
01228A	C44A	62	A		FCB	\$62	
01229A	C44B	66	A		FCB	\$66	
01230A	C44C	69	A		FCB	\$69	
01231A	C44D	6D	A		FCB	\$6D	
01232A	C44E	70	A		FCB	\$70	
01233A	C44F	74	A		FCB	\$74	
01234A	C450	77	A		FCB	\$77	
01235A	C451	7B	A		FCB	\$7B	; 110VRMS, 155.6 V PK
01236A	C452	7E	A		FCB	\$7E	
01237A	C453	81	A		FCB	\$81	
01238A	C454	85	A		FCB	\$85	
01239A	C455	88	A		FCB	\$88	
01240A	C456	8C	A		FCB	\$8C	
01241A	C457	8F	A		FCB	\$8F	
01242A	C458	93	A		FCB	\$93	
01243A	C459	96	A		FCB	\$96	
01244A	C45A	9A	A		FCB	\$9A	
01245A	C45B	9D	A		FCB	\$9D	; 120VRMS, 169.7 V PK
01246A	C45C	A0	A		FCB	\$A0	
01247A	C45D	A3	A		FCB	\$A3	
01248A	C45E	A7	A		FCB	\$A7	
01249A	C45F	AB	A		FCB	\$AB	
01250A	C460	AE	A		FCB	\$AE	
01251A	C461	B1	A		FCB	\$B1	
01252A	C462	B5	A		FCB	\$B5	
01253A	C463	B8	A		FCB	\$B8	
01254A	C464	BC	A		FCB	\$BC	
01255A	C465	BF	A		FCB	\$BF	; 130VRMS, 183.85 V PK
01256A	C466	C3	A		FCB	\$C3	
01257A	C467	C6	A		FCB	\$C6	
01258A	C468	CA	A		FCB	\$CA	
01259A	C469	CD	A		FCB	\$CD	
01260A	C46A	D0	A		FCB	\$D0	
01261A	C46B	D4	A		FCB	\$D4	
01262A	C46C	D7	A		FCB	\$D7	
01263A	C46D	DB	A		FCB	\$DB	
01264A	C46E	DE	A		FCB	\$DE	; 139V, 196.6 V PK
01265							

*

```

01267 *
01268 *
01269 *****
01270 * TABLE 2 ; SMALL ERROR CORRECTION JMP TABLE
01271 * -----
01272 * A SMALL ERROR OF 15 BITS WILL CAUSE
01273 * THE E3.1PC ROUTINE TO BE EXECUTED.
01274 * THIS ROUTINE WILL ADJUST THE CONV
01275 * OSC FREQ 3.1% TO PARTIALLY CORRECT
01276 * THE CONV OUT VOLT ERROR.
01277 *
01278A C46F C3C5 A TABLE2 FDB FAULTE ; ILLEGAL ADDRESS
01279A C471 C164 A FDB E.1PC ; 1 BIT ERROR .52%
01280A C473 C16D A FDB E.2PC ; 2 BIT ERROR 1.04%
01281A C475 C178 A FDB E.4PC ; 3 BIT ERROR 1.56%
01282A C477 C17C A FDB E.8PC ; 4 BIT ERROR 2.08%
01283A C479 C17C A FDB E.8PC ; 5 BIT ERROR 2.60%
01284A C47B C17C A FDB E.8PC ; 6 BIT ERROR 3.12%
01285A C47D C180 A FDB E1.5PC ; 7 BIT ERROR 3.64%
01286A C47F C180 A FDB E1.5PC ; 8 BIT ERROR 4.16%
01287A C481 C180 A FDB E1.5PC ; 9 BIT ERROR 4.68%
01288A C483 C180 A FDB E1.5PC ; 10 BIT ERROR 5.20%
01289A C485 C180 A FDB E1.5PC ; 11 BIT ERROR 5.72%
01290A C487 C180 A FDB E1.5PC ; 12 BIT ERROR 6.24%
01291A C489 C180 A FDB E1.5PC ; 13 BIT ERROR 6.76%
01292A C48B C184 A FDB E3.1PC ; 14 BIT ERROR 7.28%
01293A C48D C184 A FDB E3.1PC ; 15 BIT ERROR 7.80%
01294A C48F C184 A FDB E3.1PC ; 16 BIT ERROR 8.32%
01295A C491 C184 A FDB E3.1PC ; 17 BIT ERROR 8.84%
01296A C493 C184 A FDB E3.1PC ; 18 BIT ERROR 9.36%
01297A C495 C184 A FDB E3.1PC ; 19 BIT ERROR 9.88%
01298A C497 C184 A FDB E3.1PC ; 20 BIT ERROR 10.40%
01299 *
01300 *
01301 *
01302 *****
01303 * TABLE 4
01304 * -----
01305 *
01306 * ALL VALUES IN TABLE ARE NORMALIZED
01307 * TO 120V RMS. THE TABLE BEGINS WITH
01308 * 0D5H AND ENDS WITH 128H .
01309 * THESE VALUES BECOME A MULTIPLIER IN
01310 * CONV OUT POWER CALCULATIONS.
01311 * VALUES D5H AND FEH REPRESENT 0. D5H AND 0. FE
01312 * VALUES 00H AND 28H REPRESENT 1. 00H AND 1. 28
01313 *
01314A C499 D5 A TABLE4 FCB $D5 ; 100 VRMS
01315A C49A D7 A FCB $D7
01316A C49B DA A FCB $DA
01317A C49C DC A FCB $DC
01318A C49D DE A FCB $DE
01319A C49E E0 A FCB $E0
01320A C49F E2 A FCB $E2
01321A C4A0 E4 A FCB $E4
01322A C4A1 E6 A FCB $E6
01323A C4A2 E9 A FCB $E9
01324A C4A3 EB A FCB $EB ; 110 VRMS

```

01325A	C4A4	ED	A	FCB	\$ED	
01326A	C4A5	EF	A	FCB	\$EF	
01327A	C4A6	F1	A	FCB	\$F1	
01328A	C4A7	F3	A	FCB	\$F3	
01329A	C4A8	F5	A	FCB	\$F5	
01330A	C4A9	F7	A	FCB	\$F7	
01331A	C4AA	FA	A	FCB	\$FA	
01332A	C4AB	FC	A	FCB	\$FC	
01333A	C4AC	FE	A	FCB	\$FE	
01334A	C4AD	00	A	FCB	\$00	
01335A	C4AE	02	A	FCB	\$02	; 120 VRMS
01336A	C4AF	04	A	FCB	\$04	
01337A	C4B0	06	A	FCB	\$06	
01338A	C4B1	08	A	FCB	\$08	
01339A	C4B2	0B	A	FCB	\$0B	
01340A	C4B3	0D	A	FCB	\$0D	
01341A	C4B4	0F	A	FCB	\$0F	
01342A	C4B5	11	A	FCB	\$11	
01343A	C4B6	13	A	FCB	\$13	
01344A	C4B7	15	A	FCB	\$15	; 130 VRMS
01345A	C4B8	18	A	FCB	\$18	
01346A	C4B9	1A	A	FCB	\$1A	
01347A	C4BA	1C	A	FCB	\$1C	
01348A	C4BB	1E	A	FCB	\$1E	
01349A	C4BC	20	A	FCB	\$20	
01350A	C4BD	22	A	FCB	\$22	
01351A	C4BE	24	A	FCB	\$24	
01352A	C4BF	26	A	FCB	\$26	
01353A	C4C0	28	A	FCB	\$28	; 139 VRMS

01354

01355

01356

01357

01358

01359

01360

01361

01362

01363

01364

01365

01366

01367

01368

01369

01370

01371

01372A CC00

01373A CC00

01374A CC08

01375A CC10

01376A CC18

01377A CC20

01378A CC28

01379A CC30

01380A CC38

01381A CC40

01382A CC48

*

*

*

* TABLE 3 ; CONV OUT POWER VS. CONV OSC FREQ.

*

* CONV OUTPUT POWER IS REPRESENTED

* BY A 9 BIT HEX VALUE.

* POWER CAN RANGE FROM 000H TO 1FFH.

* THIS RANGE WILL CORRESPOND TO A CONV OUT

* POWER OF 0KW TO 36KW.

* THE 512 VALUES IN THE TABLE CAN

* RANGE FROM 000H TO 7FFH. THIS WILL RESULT

* CONVERTER OPERATING FREQ RANGE OF APPROX.

* 5HZ TO 10.4KHZ.

* THE UPPER 3 BITS OF FREQ ARE

* SUPPRESSED IN THE TABLE. THESE ARE

* RECONSTRUCTED IN THE PROGRAM.

ORG \$CC00

01372A	CC00		A	TABLE3	FCB	\$03, \$07, \$0B, \$0F, \$13, \$17, \$1B, \$1F
01373A	CC00	03	A		FCB	\$23, \$27, \$2B, \$2F, \$33, \$37, \$3B, \$3F
01374A	CC08	23	A		FCB	\$43, \$47, \$4B, \$4F, \$53, \$57, \$5B, \$5F
01375A	CC10	43	A		FCB	\$63, \$67, \$6B, \$6F, \$73, \$77, \$7B, \$7F
01376A	CC18	63	A		FCB	\$83, \$87, \$8B, \$8F, \$93, \$97, \$9B, \$9F
01377A	CC20	83	A		FCB	\$A3, \$A7, \$AB, \$AF, \$B3, \$B7, \$BB, \$BF
01378A	CC28	A3	A		FCB	\$C3, \$C7, \$CB, \$CF, \$D3, \$D7, \$DB, \$DF
01379A	CC30	C3	A		FCB	\$E3, \$E7, \$EB, \$EF, \$F3, \$F7, \$FB, \$FF
01380A	CC38	E3	A		FCB	\$03, \$07, \$0B, \$0F, \$13, \$17, \$1B, \$1F
01381A	CC40	03	A	MSB1XX	FCB	\$23, \$27, \$2B, \$2F, \$33, \$37, \$3B, \$3F
01382A	CC48	23	A		FCB	

01383A	CC50	43	A	FCB	\$43, \$47, \$4B, \$4F, \$53, \$57, \$5B, \$5F
01384A	CC58	63	A	FCB	\$63, \$67, \$6B, \$6F, \$73, \$77, \$7B, \$7F
01385A	CC60	83	A	FCB	\$83, \$87, \$8B, \$8F, \$93, \$97, \$9B, \$9F
01386A	CC68	A3	A	FCB	\$A3, \$A7, \$AB, \$AF, \$B3, \$B7, \$BB, \$BF
01387A	CC70	C3	A	FCB	\$C3, \$C7, \$CB, \$CF, \$D3, \$D7, \$DB, \$DF
01388A	CC78	E3	A	FCB	\$E3, \$E7, \$EB, \$EF, \$F3, \$F7, \$FB, \$FF
01389A	CC80	03	A	MSB2XX	FCB \$03, \$07, \$0B, \$0F, \$13, \$17, \$1B, \$1F
01390A	CC88	23	A	FCB	\$23, \$27, \$2B, \$2F, \$33, \$37, \$3B, \$3F
01391A	CC90	43	A	FCB	\$43, \$47, \$4B, \$4F, \$53, \$57, \$5B, \$5F
01392A	CC98	63	A	FCB	\$63, \$67, \$6B, \$6F, \$73, \$77, \$7B, \$7F
01393A	CCA0	83	A	FCB	\$83, \$87, \$8B, \$8F, \$93, \$97, \$9B, \$9F
01394A	CCA8	A3	A	FCB	\$A3, \$A7, \$AB, \$AF, \$B3, \$B7, \$BB, \$BF
01395A	CCB0	C3	A	FCB	\$C3, \$C7, \$CB, \$CF, \$D3, \$D7, \$DB, \$DF
01396A	CCB8	E3	A	FCB	\$E3, \$E7, \$EB, \$EF, \$F3, \$F7, \$FB, \$FF
01397A	CCC0	03	A	MSB3XX	FCB \$03, \$07, \$0B, \$0F, \$13, \$17, \$1B, \$1F
01398A	CCC8	23	A	FCB	\$23, \$27, \$2B, \$2F, \$33, \$37, \$3B, \$3F
01399A	CCD0	43	A	FCB	\$43, \$47, \$4B, \$4F, \$53, \$57, \$5B, \$5F
01400A	CCD8	63	A	FCB	\$63, \$67, \$6B, \$6F, \$73, \$77, \$7B, \$7F
01401A	CCE0	83	A	FCB	\$83, \$87, \$8B, \$8F, \$93, \$97, \$9B, \$9F
01402A	CCE8	A3	A	FCB	\$A3, \$A7, \$AB, \$AF, \$B3, \$B7, \$BB, \$BF
01403A	CCF0	C3	A	FCB	\$C3, \$C7, \$CB, \$CF, \$D3, \$D7, \$DB, \$DF
01404A	CCF8	E3	A	FCB	\$E3, \$E7, \$EB, \$EF, \$F3, \$F7, \$FB, \$FF
01405A	CD00	00	A	MSB4XX	FCB \$00
01406A	CD01	00	A	MSB5XX	FCB \$00
01407A	CD02	00	A	MSB6XX	FCB \$00
01408A	CD03	00	A	MSB7XX	FCB \$00
01409A	CD04	00	A	MSB8XX	FCB \$00 ; ILLEGAL
01410			*		
01411			*		
01412			*		* THE VALUES IN THIS TABLE WILL BE
01413			*		* REPLACED WITH VALUES THAT WILL MORE
01414			*		* ACCURATELY REPRESENT THE NON-
01415			*		* LINEARITY OF THE CONVERTER.
01416			*		* THE VALUES WILL ALSO BE SUBJECT TO A
01417			*		* NORMALIZED MULTIPLICATION FACTOR
01418			*		* THAT WILL BE BASED ON CONV INPUT
01419			*		* VOLTAGE.
01420			*		* THE NON-LINEAR PORTION OF THE TABLE WILL
01421			*		* BE ADDED AT A LATER DATE.
01422			*		
01423			*		
01424			*		
01425			*		
01426			*		*****
01427			*		* TABLE 5
01428			*		* -----
01429A	CD05	CC40	A	TABLE5	FDB MSB1XX
01430A	CD07	CC80	A		FDB MSB2XX
01431A	CD09	CCC0	A		FDB MSB3XX
01432A	CD0B	CD00	A		FDB MSB4XX
01433A	CD0D	CD01	A		FDB MSB5XX
01434A	CD0F	CD02	A		FDB MSB6XX
01435A	CD11	CD03	A		FDB MSB7XX
01436A	CD13	CD04	A		FDB MSB8XX
01437			*		
01438			*		
01439			*		
01440					END

TOTAL ERRORS 00000--00000
 TOTAL WARNINGS 00000--00000

0020 . 33KHZ 00105*00814
 0002 . 400HZ 00164*00373
 0000 . 50HZ 00162*00377
 0001 . 60HZ 00163*00375
 C275 ACTVAT 00780 00799*
 C1C2 ADD1 00628*
 C19E ADJUST 00543 00545 00553 00555 00593 00602*
 C07A AGAIN1 00297*00305
 C078 AGAIN2 00296*00309
 C191 AGAIN3 00587*00590
 C29A AGAIN4 00835*00838
 C2AC AGAIN5 00836 00844*
 C30F AGAIN7 00916*00918
 C097 AGAIN8 00313*00315
 C39F AGN 01029*01030
 C0DD AHEAD1 00374 00376 00379*
 C1ED AHEAD4 00659 00668 00673*
 C249 AHEAD5 00746 00752*
 C2A4 AHEAD6 00833 00840*
 C2AF AHEAD7 00842 00846*00851 00855
 C2BE AHEAD8 00849 00854*
 C188 AHEADB 00560 00564 00568 00572 00575*
 C37D AHEADC 00991 00993*
 C236 AHED1 00736 00744*
 C35A BACK1 00969*00973
 P 0005 BCDVAL 00179*00341 00418
 C358 BINARY 00960 00968*
 C445 BLANK 01213*
 C1F7 CALCUL 00674 00703*
 00DF CLRDIS 00069*00244 01168
 C091 CLRRAM 00307 00311*
 0008 CMPLT1 00124*
 0010 CMPLT2 00125*00485
 40A1 CNTRLA 00082*00251 00254 00257
 40A3 CNTRLB 00094*00264 00266 00268
 40C1 CNTRLC 00110*00275 00277 00280
 0001 CNVRT1 00118*
 0080 CNVRT2 00107*00480 00489 00910 00932
 00E0 COMFAL 00126*01013 01014
 P 000D COUNT1 00193*00578 00589 00874 00890 00920 01141 01153
 0040 CVCURA 00152*
 0020 CVCURB 00151*
 0000 CVCURC 00150*
 00C0 CVOUT 00156*
 C39C CYCLE 01028*01034
 C253 DACDRV 00335 00394 00615 00757 00777*
 P 0009 DACVAL 00188*00540 00551 00552 00586 00605 00623 00744 00749
 00777 00793
 C381 DELAY 00403 00912 01002*01005
 C2D4 DIVID1 00876*00880
 C2E0 DIVID2 00882*00891
 C2C7 DIVIDE 00709 00871*
 0000 DMODE 00067*00237

00FF DREXN 00085*
 00FF DREXNB 00097*
 0003 DREXNC 00113*00278 00282 00283
 P 0021 DSPBUF 00211*01140 01157
 4001 DSPLYC 00066*00238 00240 00243 00245 01169
 4000 DSPLYD 00065*01160
 C42D DSPTBL 01139 01189*
 C14B DTERM 00503 00512*
 P 0002 DVIDND 00174*00703 00707
 P 0000 DVISOR 00171*00704 00705
 C164 E. 1PC 00540*01279
 C16D E. 2PC 00551*01280
 C178 E. 4PC 00559*01281
 C17C E. 8PC 00563*01282 01283 01284
 C180 E1. 5PC 00567*01285 01286 01287 01288 01289 01290 01291
 C184 E3. 1PC 00571*01292 01293 01294 01295 01296 01297 01298
 C435 EIGHT 01197*
 00FC ENABLA 00101*
 0008 ENABLB 00102*
 0010 ENABLC 00103*
 001C ENALL 00104*00379
 0040 ENBLCV 00106*00380 01017 01036 01123
 C252 EXIT 00529 00616 00765*01050 01056
 0003 EXTERN 00165*
 P 001B FAILST 00205*01015
 C344 FAULT1 00948 00951*
 C352 FAULT2 00962*
 C032 FAULT3 00260*
 C04C FAULT4 00271*
 C06C FAULT5 00285*
 C080 FAULT6 00301*
 C0CD FAULT7 00365*
 C1E0 FAULT9 00660*00669
 C1F1 FAULTA 00677*
 C265 FAULTB 00787*
 C114 FAULTD 00427*
 C3C5 FAULTE 01068*01278
 C2C3 FINISH 00850 00857*
 C11F FIRQ 00219 00479*
 C432 FIVE 01194*
 C431 FOUR 01193*
 P 0008 FQMODE 00186*00358 00425
 00FC FREQSL 00100*00355
 C223 GETVAL 00727*
 0039 HILIM 00074*00947
 P 000E IMEASR 00194*00712 00928
 C1AC INCRS 00610*
 C3B7 INVOUT 00527 01049*
 C387 IRQ 00221 01012*
 0008 IVCURA 00140*
 0004 IVCURB 00139*
 0000 IVCURC 00138*
 0018 IVNPT 00144*
 0014 IVVOLA 00143*
 0010 IVVOLB 00142*
 000C IVVOLC 00141*
 C006 KEYDIS 00237*
 C437 LETTRA 01199*

C438 LETTRB 01200*
 C439 LETTRC 01201*
 C43A LETTRD 01202*
 C43B LETTRE 01203*
 C43C LETTRF 01204*
 C43D LETTRH 01205*
 C441 LETTRI 01209*
 C43E LETTRJ 01206*
 C43F LETTRL 01207*
 C442 LETTRN 01210*
 C440 LETTRP 01208*
 C443 LETTRR 01211*
 C444 LETTRU 01212*
 C1B4 LOADAC 00611 00615*00629 00633
 P 0007 LOKOUT 00184*01049
 C362 LOOKUP 00969 00978*
 C3FC LOOP4 01143*01154
 C1E6 LOW 00655 00666*
 C1CC LRGERR 00513 00648*
 C0F8 MAIN 00413*00432
 C11A MAIN1 00416 00426 00430*
 C2F5 MEASR1 00650 00905*
 P 001D MESSBF 00210*01113 01138
 P 0011 MLTCAN 00198*00831 00837
 C292 MLTPLY 00713 00721 00831*
 CC40 MSB1XX 01381*01429
 CC80 MSB2XX 01389*01430
 CCC0 MSB3XX 01397*01431
 CD00 MSB4XX 01405*01432
 CD01 MSB5XX 01406*01433
 CD02 MSB6XX 01407*01434
 CD03 MSB7XX 01408*01435
 CD04 MSB8XX 01409*01436
 001C MUX1SL 00090*
 00E0 MUX2SL 00091*
 C436 NINE 01198*
 C3C1 NMI 00224 01059*
 C155 NOAJST 00499 00523*
 C10A NOCHNG 00419 00423*
 C2EA NOINCR 00877 00883 00887*
 0002 NORMAL 00119*
 00A0 NPTVLA 00155*
 0080 NPTVLB 00154*
 0060 NPTVLC 00153*
 00AA NTTRUE 00076*00294 00326 00785
 C038 OK3 00259 00264*
 C052 OK4 00270 00275*
 C086 OK6 00299 00304*
 C42E ONE 01190*
 P 0010 OVERLD 00196*00327 00781 00805
 P 0004 PLARTY 00177*00502 00507 00606 00624 00657 00666
 C446 POINT 01214*
 40A0 PORTA 00083*00253 00255 00258 00386 00906
 40A2 PORTB 00095*00265 00267 00269 00382 00479 00481 00490 00801
 00803 00813 00815 00909 00914 00931 00933 01016 01018
 01038 01039 01122 01124
 40C0 PORTC 00111*00276 00279 00281 00484 00908 00913 00916 00935
 01012

C412 PRINT 01127 01157*
C417 PRINT8 01159*01162
0003 PROMSL 00089*
P 0013 QUOTNT 00199*00718 00832 00835 00872 00879
C072 RAMTST 00284 00294*
P 0019 RATIO 00204*00717 00993
8000 RE0 00045*
8008 RE1 00046*00488 00929
8050 RE10 00055*
8058 RE11 00056*
8060 RE12 00057*
8068 RE13 00058*
8070 RE14 00059*
8078 RE15 00060*
8010 RE2 00047*00921
8018 RE3 00048*00922
8020 RE4 00049*
8028 RE5 00050*
8030 RE6 00051*
8038 RE7 00052*00946
8040 RE8 00053*00356 00423 01165
8048 RE9 00054*
C1B1 REDUCE 00608 00613*
P 0017 REFRNC 00203*00982
P 0014 REMNDR 00200*00719 00848 00871 00885 00887
C286 REMOVE 00783 00813*
C000 RESTRT 00225 00232*01129
P 0015 RESULT 00202*00720 00840 00844 00846 00847 00854 00857
P 0008 SAVE1 00192*00603 00610 00613 00747 00748 00978 00987
C268 SENDIT 00786 00793*00799 00816
C420 SENSE 01128 01165*01167
P 001C SERVIC 00209*00414
C0D3 SET400 00360 00373*
C0D8 SET50 00364 00377*
C0D7 SET60 00362 00375*
C3ED SETUP 01126 01137*
C434 SEVEN 01196*
C18E SHIFT 00586*
C433 SIX 01195*
C14F SMLERR 00515*
001C SPARE1 00145*
00E0 SPARE2 00157*
P 0006 STABLE 00181*00523 00528 00575 00648
00FF STAK 00070*00233
C1C7 SUBTR1 00625 00632*
C3C9 SWINT 00223 01111*
C447 TABLE1 00979 01225*
C46F TABLE2 00516 01278*
CC00 TABLE3 00727 01373*
C499 TABLE4 00986 01314*
CD05 TABLE5 00732 01429*
C430 THREE 01192*
C33C THUMB 00340 00417 00946*
C140 TOOHI 00502*
C145 TOOLOW 00500 00505*
0055 TRUE 00075*00306 00308 00782 00804
C22E TRYAGN 00735*00738
C42F TWO 01191*

C34A VALID 00342 00420 00957*
P 0001 VMEASR 00172*00492 00653 00930
P 0003 VNOMNL 00175*00329 00498 00652
C127 WAIT1 00484*00486
0090 WDISPL 00068*00242
8000 WE0 00033*00794
8001 WE1 00034*
8002 WE2 00035*
8003 WE3 00036*
8004 WE4 00037*00795
8005 WE5 00038*00399 01040
8006 WE6 00039*
8007 WE7 00040*
C1BA ZERO 00604 00623*