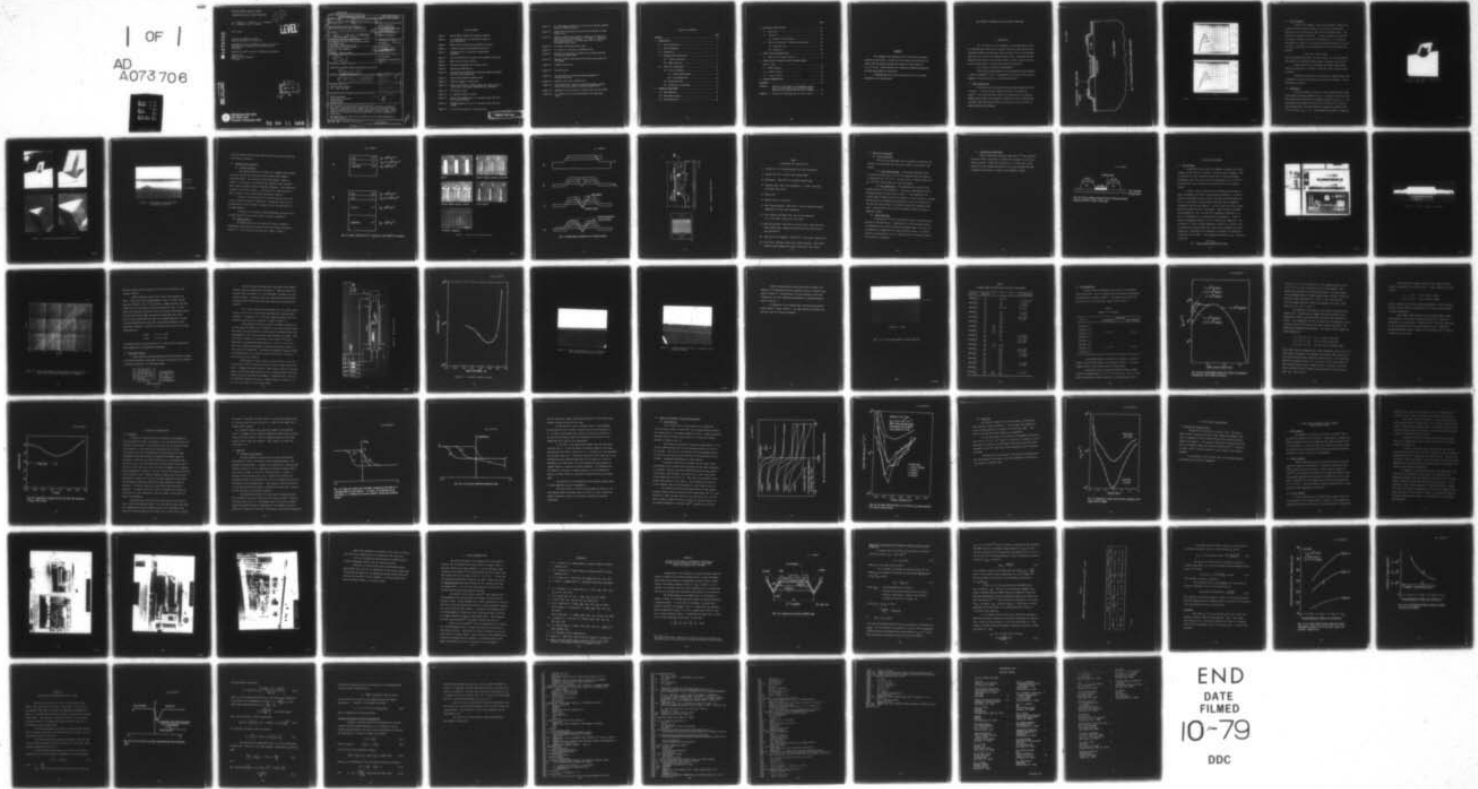


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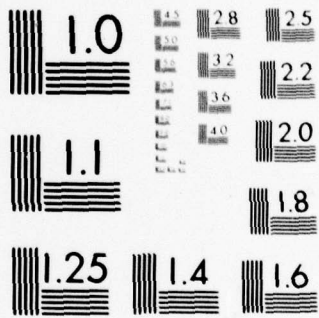
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GALLIUM ARSENIDE VERTICAL CHANNEL
INSULATED GATE FIELD EFFECT TRANSISTOR

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M. C. Driver, D. L. Barrett, G. W. Eldridge,
H. C. Nathanson, and V. L. Wruck

LEVEL II

Final Report

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ABSTRACT

The techniques for producing n^+ -p- n^+ structures in gallium arsenide are described. Evaluation of the surface state densities of anodic oxide on gallium arsenide show minima at about mid gap of 2×10^{11} eV cm^2 . These densities are affected by annealing conditions and their measurement by sweep time.

Recommendations for future work include the use of indium phosphide as the semiconductor.

GaAs VERTICAL INSULATED-GATE FIELD EFFECT TRANSISTOR

1. INTRODUCTION

(a) The objective of the program is to develop vertical channel insulated-gate field effect transistor devices in GaAs which will be ultimately capable of delivering 5 watts of power (Class A) with minimum power gain of 6 dB over the frequency range 4-8 GHz. Additional design goals for these devices are that they shall be linear in phase ($\pm 5^\circ$ deviation) and gain (IMD < -20 dB) over the range of operation.

(b) Review of Previous Accomplishments

The previous accomplishments of this program have been recorded in detail elsewhere,⁽¹⁾ but it is appropriate to review the main areas of progress in the fabrication of a vertical MOS GaAs FET.

1.1 Device Fabrication

Devices have been fabricated using the planar geometries shown in Figure 1. The devices have shown FET action as illustrated in Figure 2. The source and drain contacts for these devices is gold germanium with an anodic oxide insulator (1000Å thick) and an aluminum gate. The ohmic source and drain contacts are alloyed for 10secs at 450°C in argon containing 10% hydrogen.

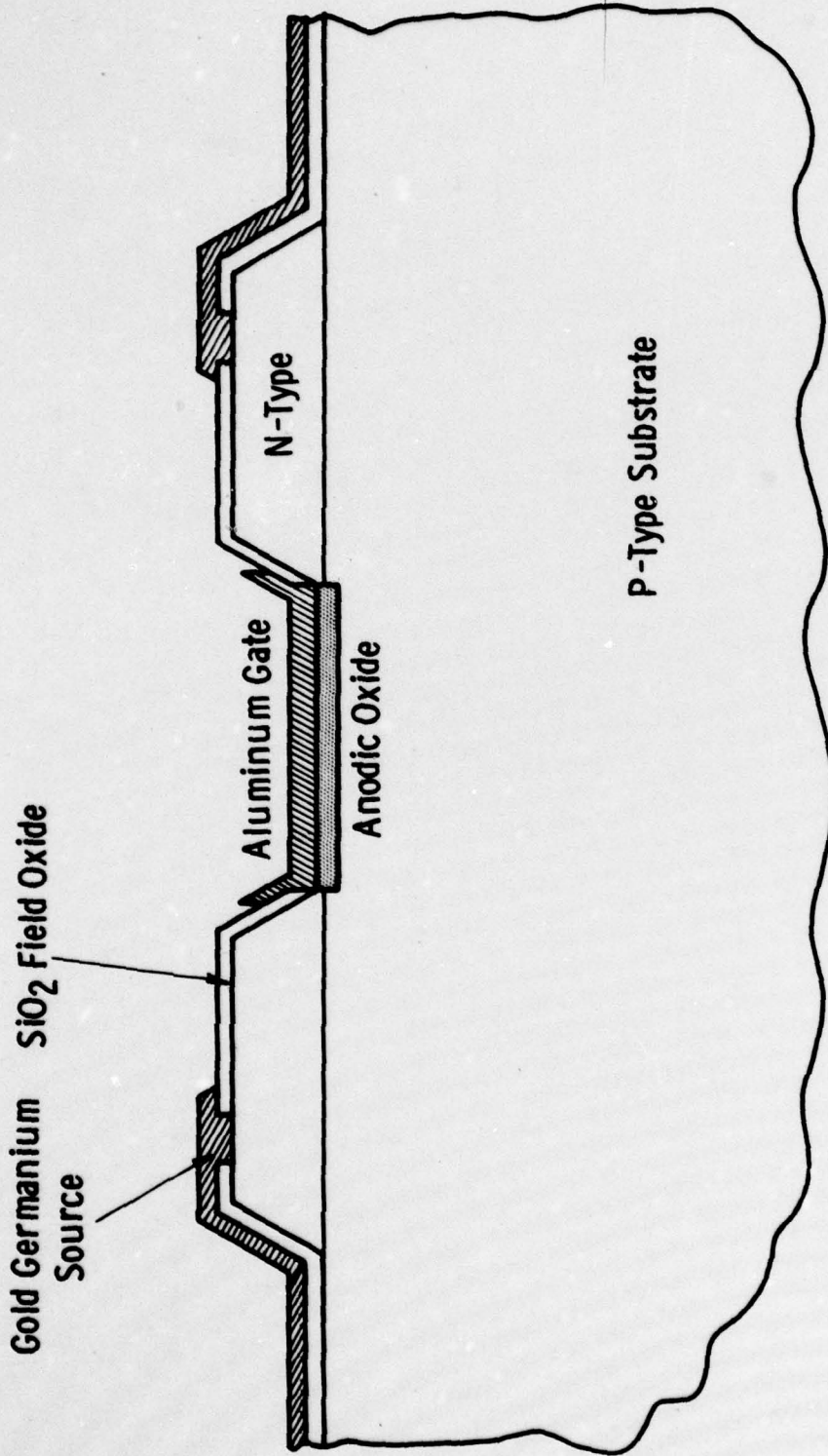
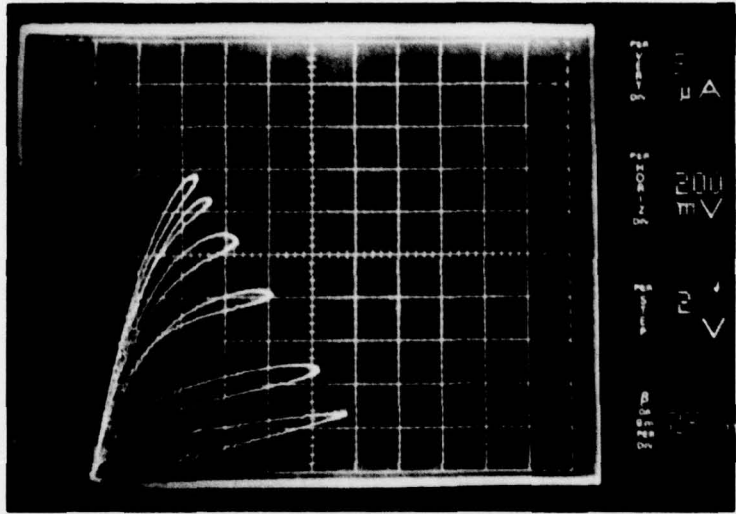
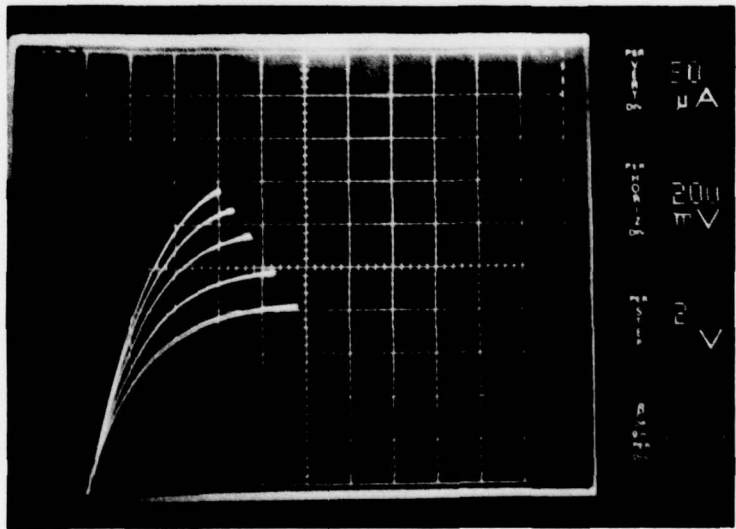


Fig. 1 -- Planar MISFET formed from epitaxial material



(a)



(b)

Figure 2 I-V characteristics of transistors formed on Slice CD3-R38-1B

1.2 Etch Development

As part of the program, etches were developed to produce the V-groove structure (shown in Figure 3) as part of the processing required for the V-groove device which will be discussed later. They consisted of mixtures of the form $X : H_2O_2 : H_2O$ where X can be HCl, HF or NaOH. The ratio (in mls) of the components $x : y : 100$ where x, the amount of X (from 2 to 6 mls) does not have much effect on the etch rate and y, the amount of H_2O_2 determines the etch rate from the relationship

$$\text{Etch rate} = 483.3y \text{ \AA}/\text{min}.$$

This relationship holds from 2 to 8 mls of H_2O_2 . At 10 mls and above the surface of the gallium arsenide begins to develop a matt finish.

The HF-based etch is anisotropic and causes rounded mesas, whereas the NaOH etch is isotropic, resulting in the structures shown in Figure 4.

Anodization etching has also been used to remove material and, in addition, is able to delineate the p-n junction structures. This is illustrated in Figure 5.

1.3 Anodization

The most favorable dielectric in this program has been anodic oxide formed on gallium arsenide using a 1 : 1 mixture of 3% citric acid and ethylene glycol buffered with ammonium hydroxide to a pH of 5.5. This solution had the minimum self-etching rate ($0.024 \text{ A}/\text{sec}^{(2)}$) and produced uniform films with good dielectric properties (breakdown field = $4.37 \times 10^6 \text{ V}/\text{cm}$, $\epsilon_s/\epsilon_0 = 7.2$). The anodization procedure is compatible

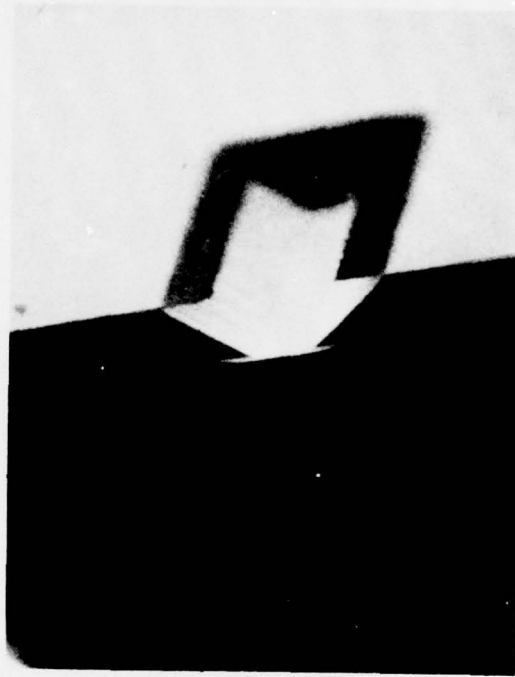
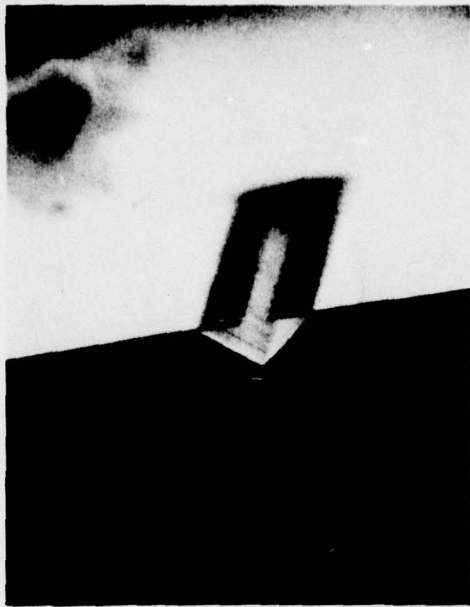
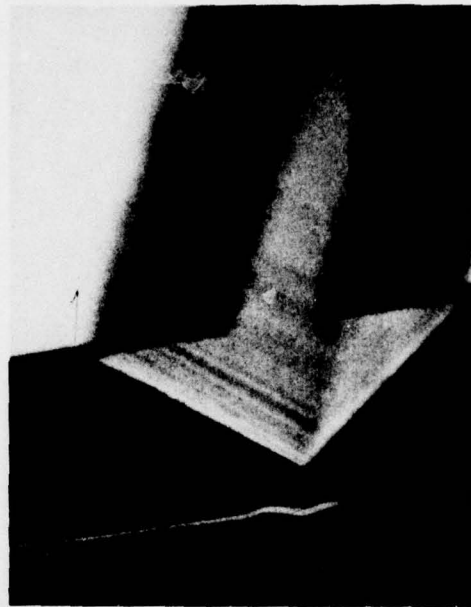


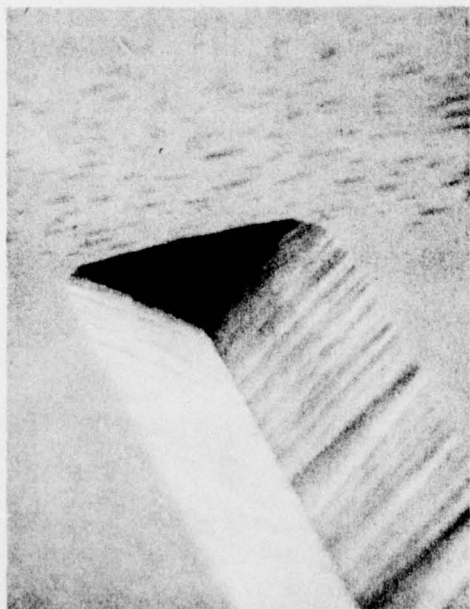
Figure 3 Wide V-groove obtained with
NaOH:H₂O₂:H₂O etch.



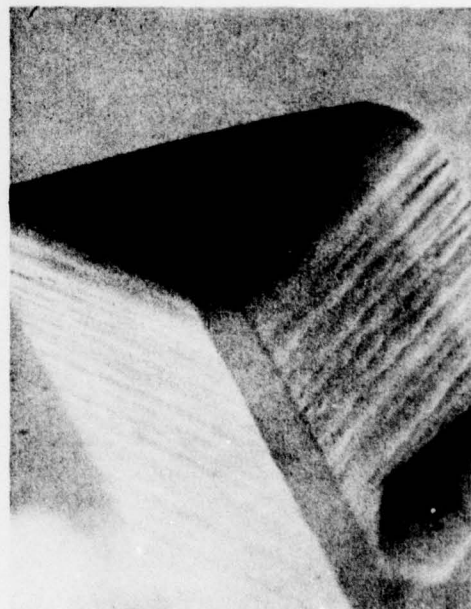
(a)



(b)

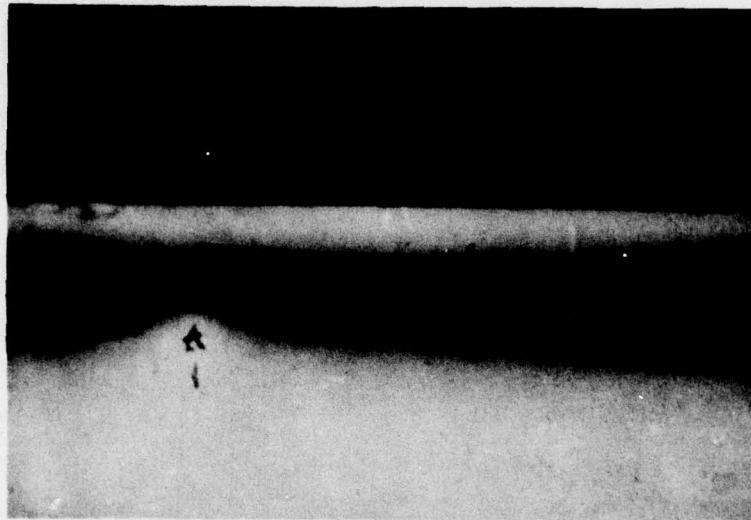


(c)



(d)

Figure 4 V-grooves obtained with NaOH:H₂O₂:H₂O etch



3.5 μm P

4.5 μm n⁻

SI substrate

Figure 5 - Delineation of p-n structures
using anodic oxidation.

with device fabrication and the anodizing solution does not attack any of the device structures.

1.4 Proposed Device Structure

(a) V-groove Structure

The V-groove structure is planned as a stepping stone between the planar devices and the final vertical channel VMIST geometry (described below). The reasons for using this geometry, shown in Figure 6, is the greater accessibility for inspection than the VMIST device and the somewhat simpler fabrication procedure. This fabrication procedure is outlined in Table 1. The mask set for these devices is shown in Figure 7 and the fabrication procedure in Figure 8.

Initially, the structure for the V-groove devices will be an n^+p-n^+ structure as shown in Figure 6(a). Ultimately, there will be an additional n^- layer as shown in Figure 6(b) for the realization of the VMIST geometry.

An analysis of the effect of photolithographic design rules on the power density of the V-groove device is given in Appendix A.

(b) VMIST Structure

The VMIST structure is the form of the device ultimately intended for this program and follows closely that already developed in silicon. ⁽³⁾ A cross-section of the device is shown in Figure 9.

a)

1 μm	N^+
1 μm	P
Substrate	N^+

$$N_d > 10^{18} \text{ cm}^{-3}$$

$$N_a = 5 \times 10^{16} \text{ cm}^{-3}$$

$$N_d > 10^{18} \text{ cm}^{-3}$$

b)

1 μm	N^+
1 μm	P
3-4 μm	n^-
Substrate	n^+

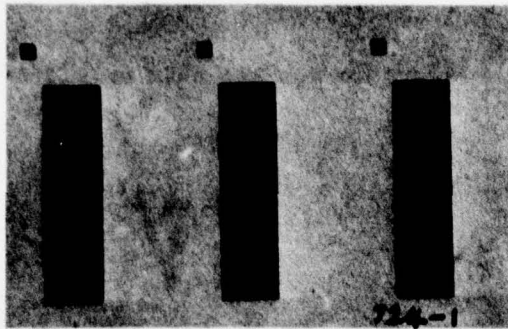
$$N_d > 10^{18} \text{ cm}^{-3}$$

$$N_a = 5 \times 10^{16} \text{ cm}^{-3}$$

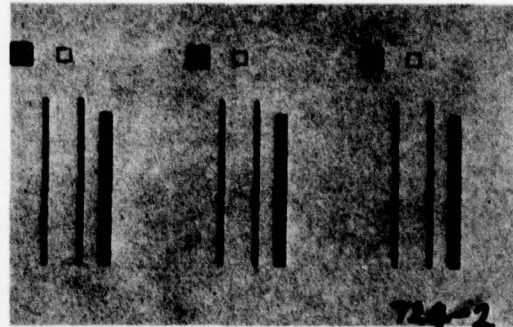
$$N_d < 10^{15} \text{ cm}^{-3}$$

$$N_d > 10^{18} \text{ cm}^{-3}$$

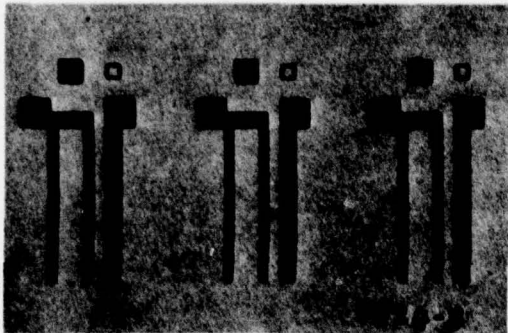
Fig. 6—Layer structures for V-groove (a) and VMIST (b) devices



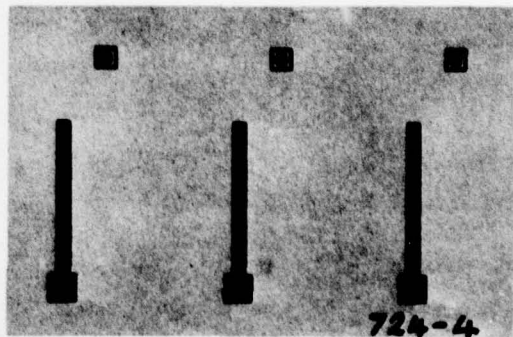
MESA



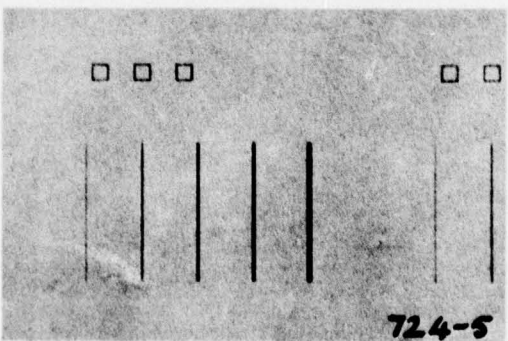
SOURCE-DRAIN CONTACT OPENINGS



SOURCE-DRAIN CONTACT METAL



GATE METAL



V-GROOVE OPENINGS

Figure 7 Mask set for V-groove devices

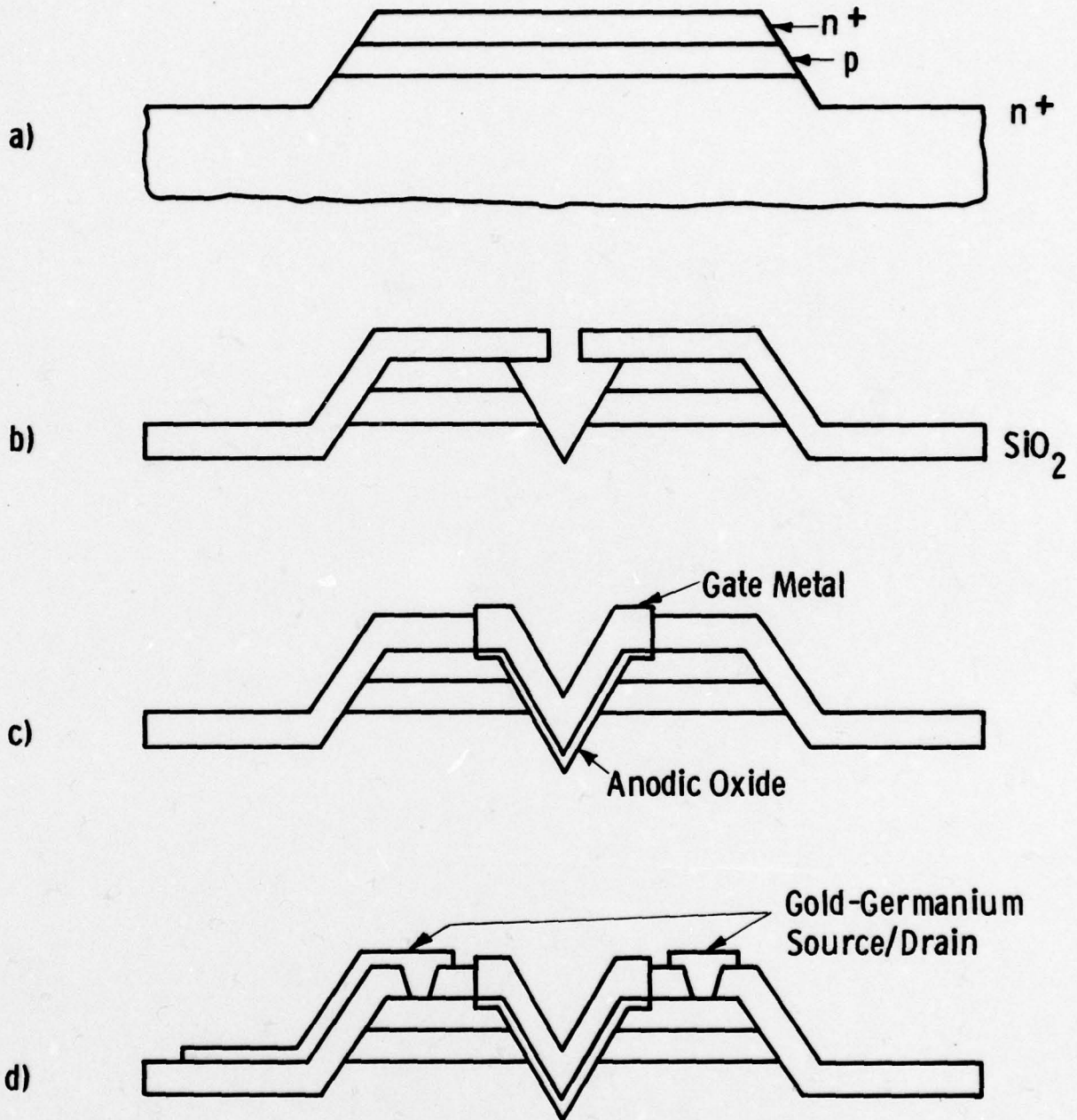


Fig. 8—Fabrication procedure for V groove device

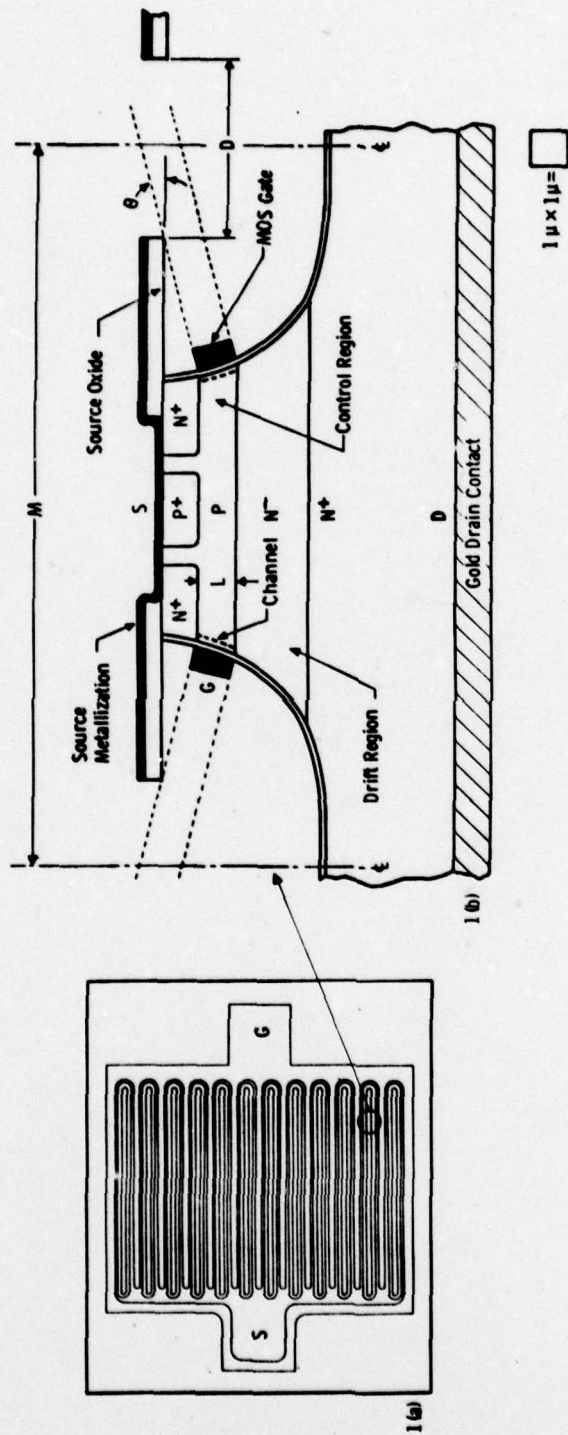


Figure 9 Topology of VMIST device

TABLE 1

Fabrication of V-groove Device

- 1) Evaluate n^+ - p - n^+ starting material for layer thicknesses.
- 2) Sputter SiO_2 (0.5 μm thick) onto surface wafer.
- 3) Photoresist - Mask #724-1 to delineate device mesas.
- 4) Using $\text{HF} : \text{H}_2\text{O}_2 : \text{H}_2\text{O}$ in the proportions 1 : 3 (30%) : 100 (mls) etch mesas [Fig. 8(a)].
- 5) Remove SiO_2 .
- 6) Sputter SiO_2 (0.5 μm thick).
- 7) Open V-groove opening - Mask #724-5 - with the required opening depending on the epi layer thicknesses.
- 8) Etch V-groove using $\text{NaOH} : \text{H}_2\text{O}_2 : \text{H}_2\text{O}$ in the proportions 1 gm : 3 mls (30%) : 100 mls [see Fig. 8(b)].
- 9) Open gate opening - Mask #724-4 [see Fig. 8(c)], etch oxide overhang, anodize GaAs, evaporate gold gate metal and reject excess with photoresist.
- 10) Open source drain openings - Mask #724-2 - etch oxide, remove resist.
- 11) Photoresist, delineate source-drain contact openings - Mask #724-3 - evaporate gold-germanium and reject excess metal [Fig. 8(d)].

1.5 Three Key Technologies

(a) n⁺-p-n⁺ Structure

Of the various approaches that are possible to fabricate the structure, the following were chosen for reasons of availability and control.

(i) Liquid Phase Epitaxy. Liquid phase epitaxial layers 2 μm thick of p-type ($N_A = 8 \times 10^{16} \text{ cm}^{-3}$) material have been grown on n⁺ substrates ($N_D = 10^{17} \text{ cm}^{-3}$). On top of this, a further n-layer with $N_D = 10^{17} \text{ cm}^{-3}$ and thickness 0.5 μm has been grown.

(ii) Ion Implantation. Ion implantation of silicon in VPE p-type layers on n-type substrates. The carrier concentrations of the VPE p-type layers are shown later in Table 2. The thickness of the p-layer shown in Figure 6(a) can be relaxed to a value as high as 5 microns during initial ion implantation experiments to allow for evaluation of the layer and some freedom in the implant energies and annealing conditions. Excess material can be readily removed by chemical etching or anodizing etching.

(b) Stable MOS Oxide

Previous work^(1,2) has indicated that anodic oxides held great promise for GaAs MOS devices. Anodization is a very convenient process to incorporate into a device fabrication procedure since it is very controllable and is compatible with other fabrication steps. Our results indicate that hysteresis is still a problem as far as long-term stability of the device is concerned.

(c) Inversion of p-type GaAs

Results obtained on previous planar devices⁽²⁾ have shown FET action but there is no positive evidence that inversion of the p-type surface occurred. Referring to Figure 10, it is likely that n-type material was left between the n-mesa on the p-type substrate and that accumulation of electrons occurred in the depleted n-region.

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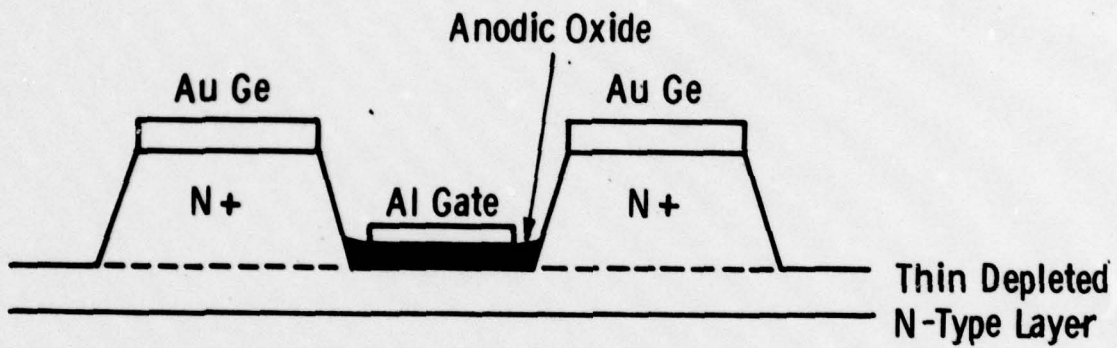


Fig. 10—Cross section of planar device showing possible presence of thin n-layer under gate

2. MATERIALS DEVELOPMENT

2.1 LPE Techniques

Liquid phase epitaxy (LPE) was employed to produce five layers suitable for the vertical transistor. One of the major strengths of LPE is the ability to quite precisely control both n- and p-type doping. Furthermore, since the p-type layer was constrained to be $5 \times 10^{16} \text{ cm}^{-3}$, this makes VPE a less attractive choice than LPE vis-a-vis p-doping control.

Figure 11 shows a picture of the LPE apparatus and Figure 12 shows the graphite boat used to grow multilayer structures. In order to achieve an LPE abrupt junction vertical structure with good doping control, it is necessary to choose dopants that have small segregation coefficients and are slow diffusers. For the n-type layer Sn was chosen and Ge was selected for the p-type dopant. Both are Group IV elements and are amphoteric; thus, the effective segregation coefficient (i.e., the n- or p-typeness) is a strong function of temperature. Figure 13 shows the segregation behavior of Sn as a function of temperature. For our particular device a growth temperature of 800°C was selected to aid in substrate-melt wetting which gives good surface morphology for device fabrication. Experiments were undertaken to determine the segregation coefficient of Ge at 800°C . The segregation coefficient, K_{Ge} , is defined as follows:

$$K_{\text{Ge}} = \frac{(N_A - N_D)_{\text{R.T.}}}{\text{Atomic Concentration of Ge in Melt}}$$

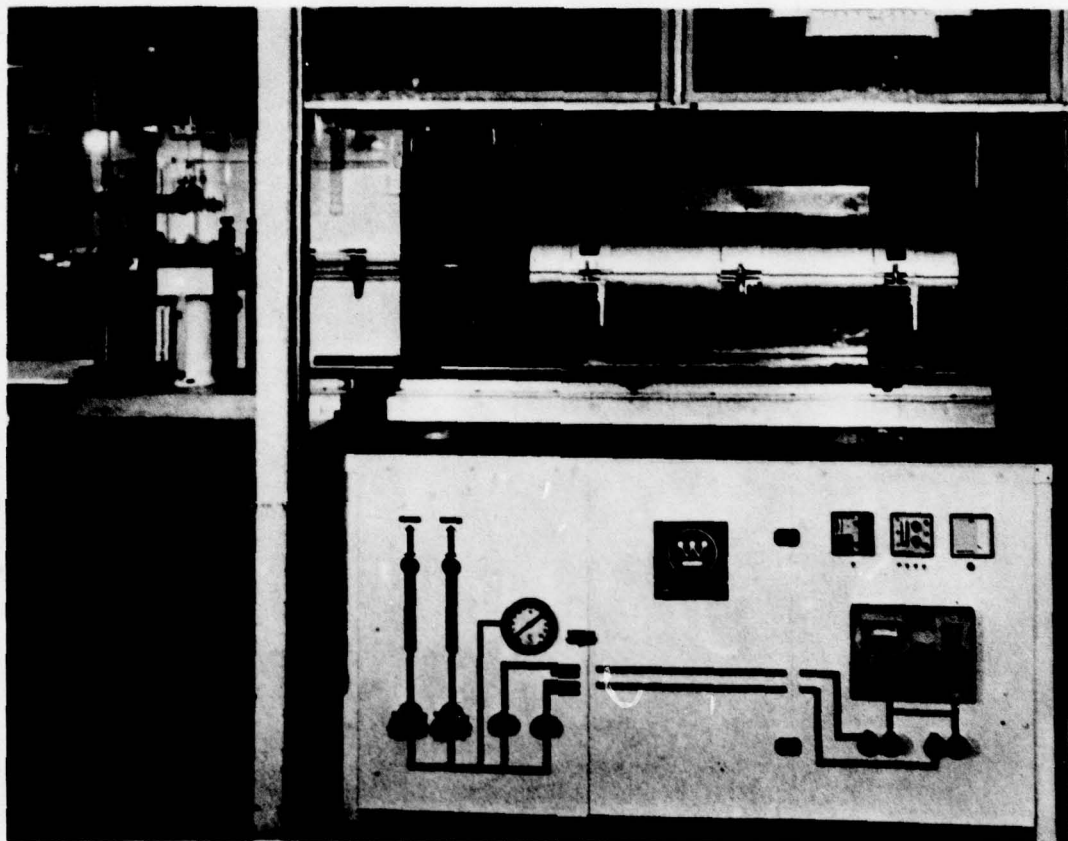


Figure 11 Liquid phase epitaxial growth system

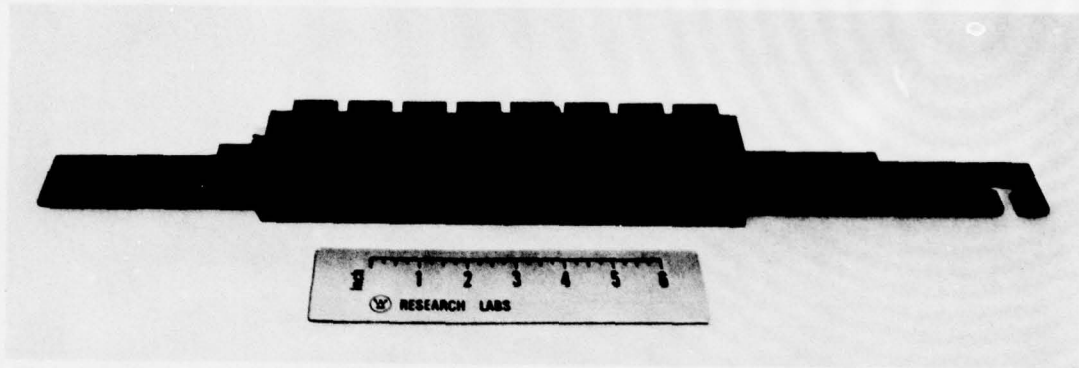


Figure 12 Eight-bin graphite sliding boat

Curve 685984-C

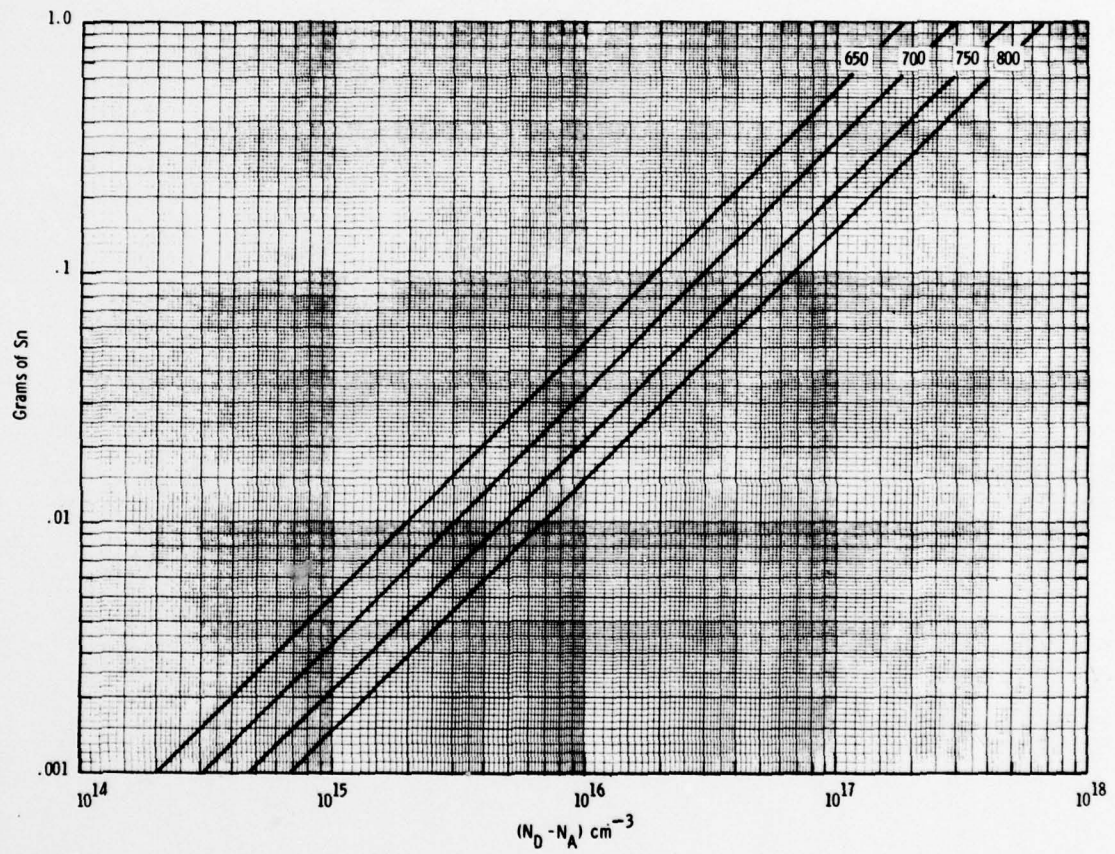


Figure 13 Grams of Sn needed to achieve particular doping level in 5 gm Ga melt with growth temperature as a parameter

Our data yields a value for K_{Ge} of 3.49×10^{-3} for LPE growth in the vicinity of 800°C .

Growth conditions were set for initial melt saturation of 800°C . After a melt bake of approximately 1 hour, a 12°C/hr cooling ramp was initiated. After 1°C of growth on a dummy substrate, the seed crystal was slid into place to grow the p-layer for 6 min. At this point, the slider was adjusted so that the seed was removed from contact with the melt and the dummy substrate was placed under the n-melt. After 5 min of growth from the n-melt on the dummy substrate, the seed was positioned under the n-type melt and growth proceeded for 3 min. Using this technique, we were able to provide layers with the following characteristics:

p-type	$2\mu @ 7.7 \times 10^{16}$
n-type	$1\mu @ 1.5 \times 10^{17}$

In addition, thick p-type layers with 7.7×10^{16} net hole concentration were supplied for ion implantation experiments.

2.2 Vapor Phase Epitaxy

Vapor epitaxial growth techniques have been developed to prepare all epitaxial multilayer GaAs VMIST structures and epitaxial ion implanted structures according to the following schemes:

$n^+ 1 \mu\text{m } 10^{18} \text{ cm}^{-3}$
$p 1 \mu\text{m mid } 10^{16} \text{ cm}^{-3}$
$n^- 3-4 \mu\text{m } < 10^{15} \text{ cm}^{-3}$
n^+ substrate

all epitaxial

ion implanted
$p 5 \mu\text{m}$
n^+ substrate

epi ion implanted

VMIST Structures

Epitaxial layers were deposited on polished silicon doped n^+ substrate wafers orientated with 100 surfaces. Substrate wafers were obtained from Laser Diodes, Inc. and subsequently polished in an acid-peroxide solution. Epitaxial layers were grown using the $\text{AsCl}_3/\text{Ga}/\text{H}_2$ technique within the multilayer epitaxial deposition system shown in Figure 14.

The n^- drift region was grown undoped with net carrier concentration in the 10^{13} cm^{-3} range using high AsCl_3 mole fraction growth conditions. An example of a $1.8 \mu\text{m}$ thick undoped epitaxial layer concentration profile on an n^+ substrate is shown in Figure 15.

P-type epitaxial layers were grown zinc-doped by addition of a dilute vapor of diethyl zinc in hydrogen to the reactor growth stream. The diethyl zinc was obtained in 5 nines purity from Alpha Products and thermostated at -20°C to give suitable vapor pressure for doping. Molar flow rates of diethyl zinc calculated to be in the $10^{-6} \text{ moles min}^{-1}$ range gave p-type epitaxial depositions of 6×10^{15} to $8 \times 10^{17} \text{ cm}^{-3}$. The actual concentration depended on growth rate and mole fraction of AsCl_3 used in the deposition. The optical micrograph of Figure 16 shows a cross-section of a $1.7 \mu\text{m}$ thick p surface layer and a $5 \mu\text{m}$ thick n^- drift layer on an n^+ substrate.

Sulfur doped n^+ surface layers of about 10^{18} cm^{-3} were grown by dilute H_2S in H_2 to the growth stream and from a heated solid sulfur source. Attempts were made to grow n^+ layers using a liquid tin chloride source, but the high vapor pressure over tin chloride proved difficult to control, and this technique was abandoned. A multilayer (n^+) - (p) - (n^-) - (n^+ substrate) epitaxial structure is shown in Figure 17 with a $2.8 \mu\text{m}$ n^+ , a $3.5 \mu\text{m}$ p, and a $2.8 \mu\text{m}$ n^- drift region.

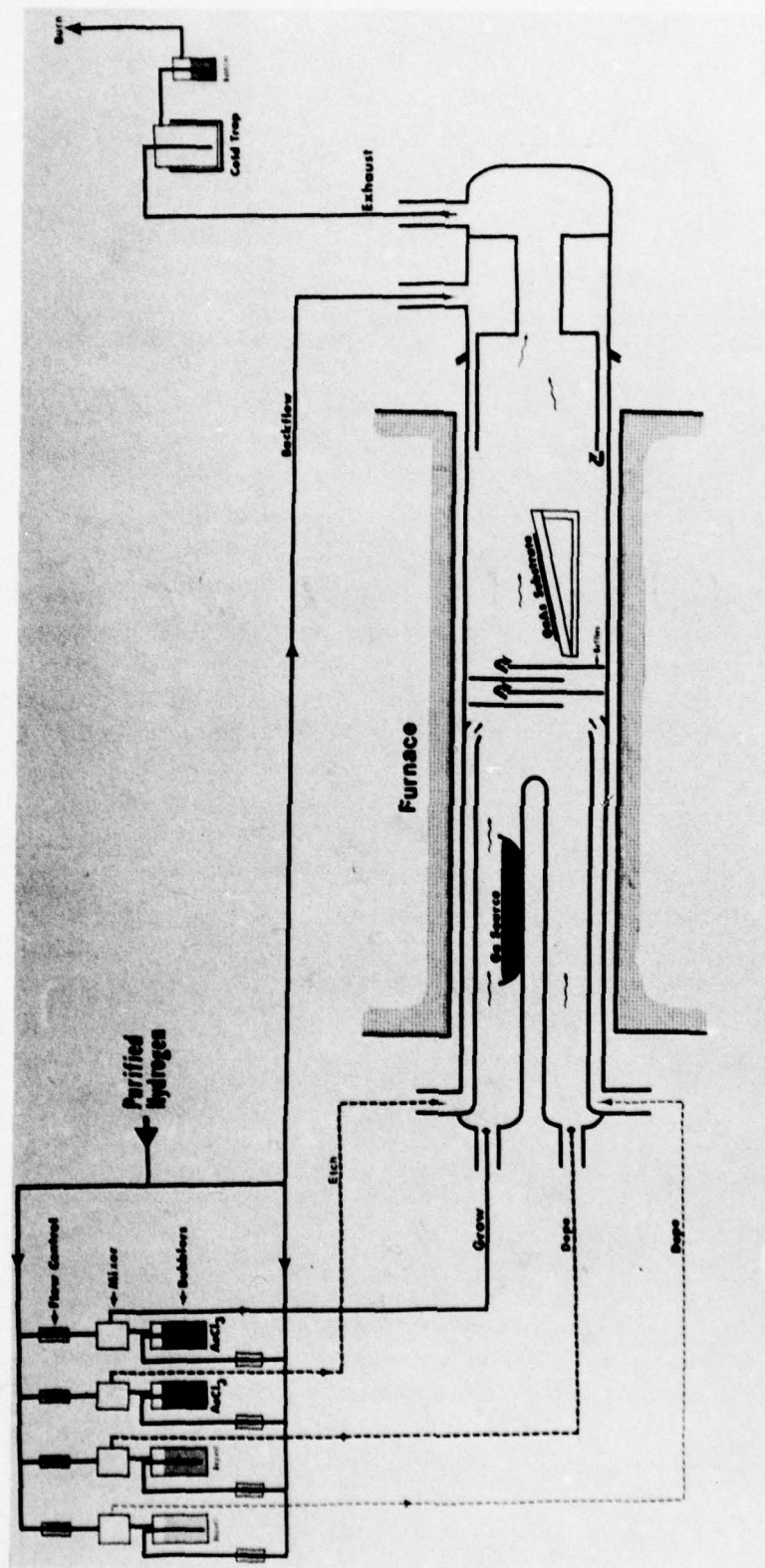


Figure 14 VPE reactor system

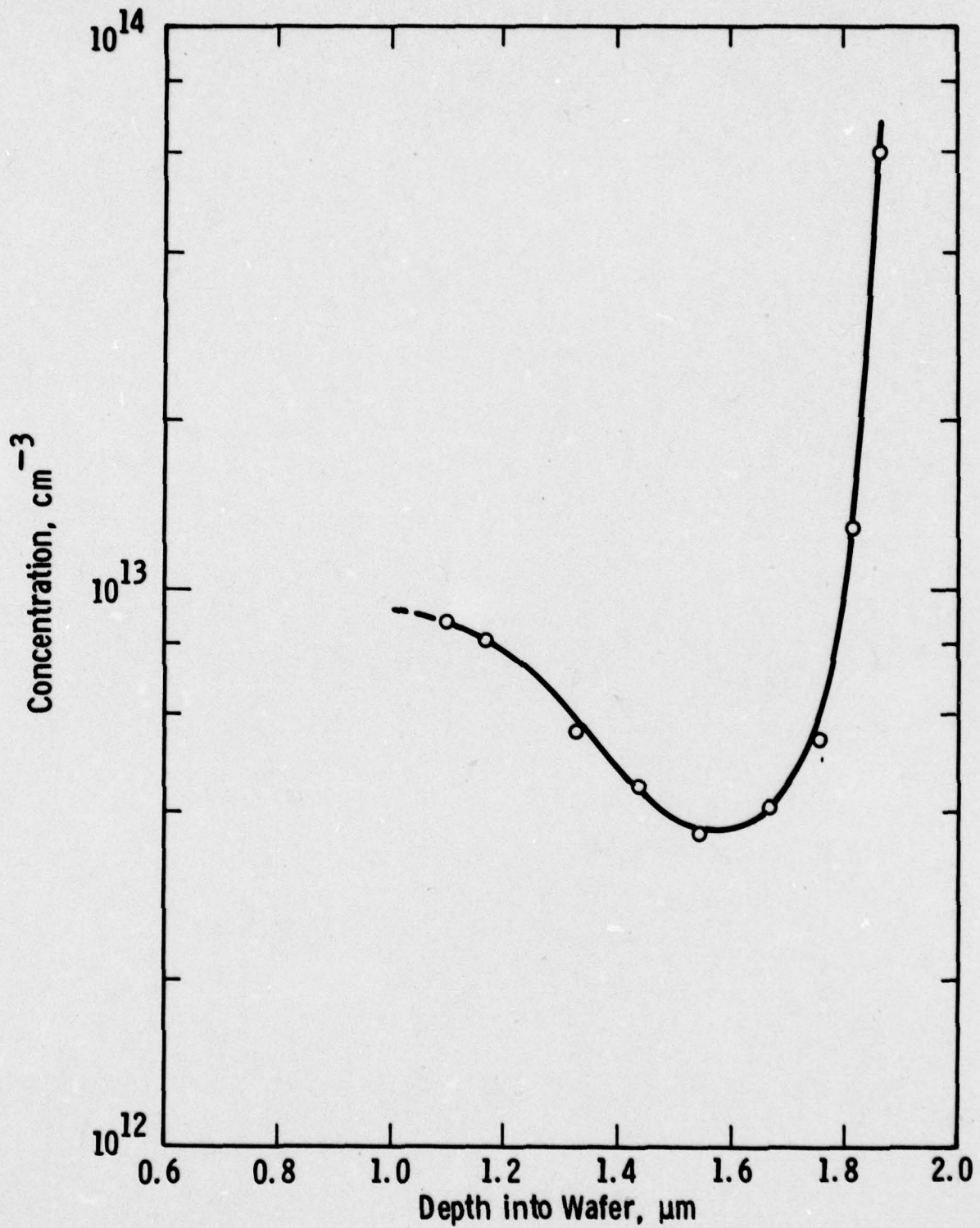


Figure 15 n⁻ epitaxial profile in GaAs

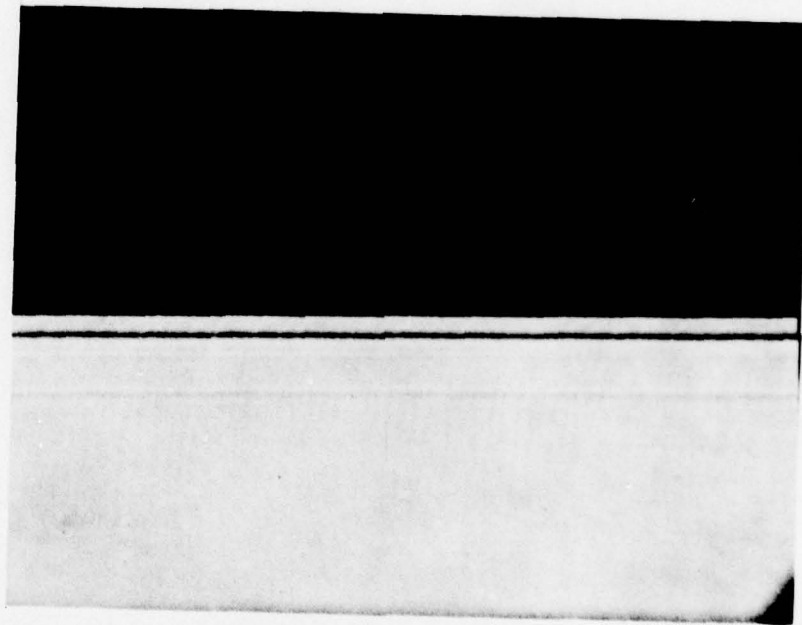


Figure 16 Optical micrograph of p-n⁻-n⁺ epitaxial wafer CD3-R43-2 cross-section (1700X)

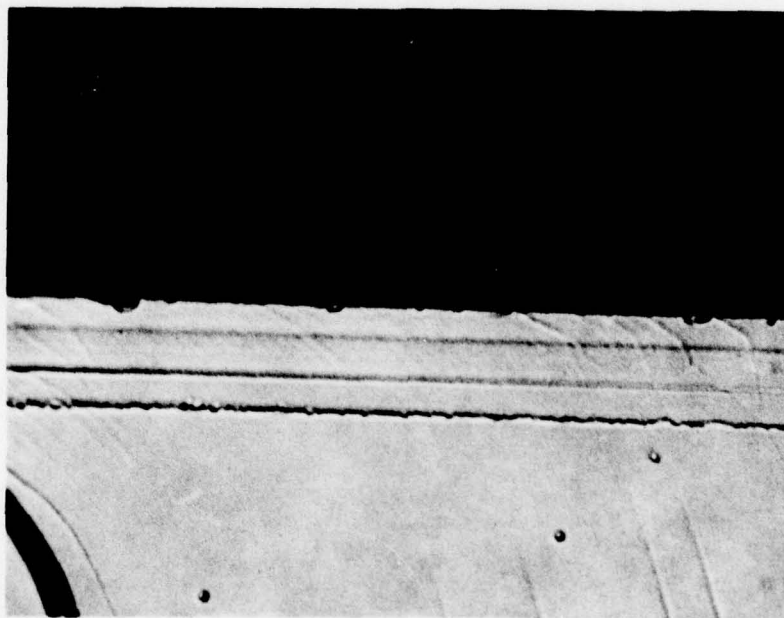
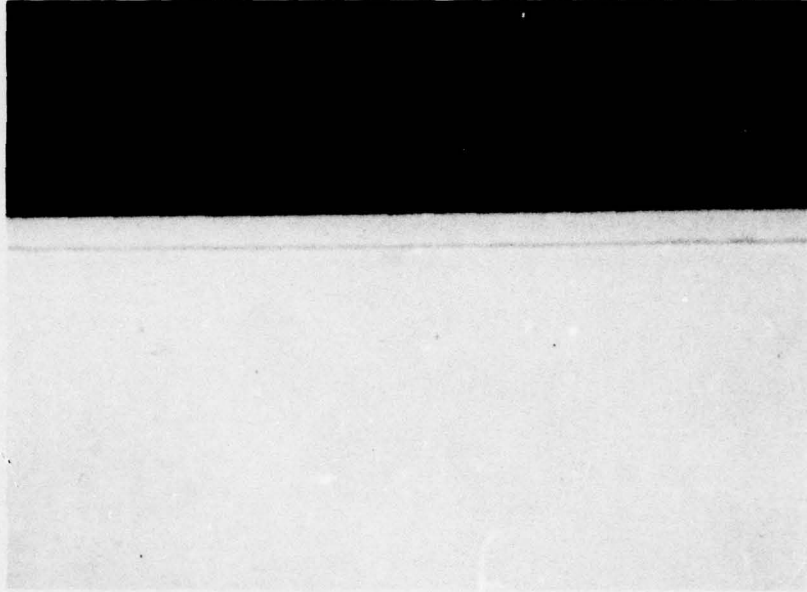


Figure 17 Photomicrograph of $n^+ - p - n^- - n^+$ epitaxial wafer
CD3-R38-1 (1700X)

Single p-type epitaxial layers were grown by diethyl zinc doping for ion implantation and are typified by the 6.3 μm thick layer shown in Figure 18. Concentrations of p-type epitaxial layers were evaluated by zero bias capacitance measurements on aluminum Schottky barrier contacts.

A compilation of zinc-doped single and multilayer epitaxial growth wafers is shown in Table 2. The semi-insulating substrate samples were used for evaluation purposes.



6.3 μm

CD4-R25-2 1700X

Fig. 18 - 6.3 μm p layer grown in n-type substrate.

TABLE 2

Zn-doped Single and Multilayer Epitaxial Growth Wafers

Wafer No.	Substrate	n ⁻	p	n ⁺	p Concentration
CD3-R40-1	n ⁺		4.2 μ m		
-2	n ⁺		2.1		6 x 10 ¹⁵ cm ⁻³
CD4-R32-1	n ⁺		7.0		9 x 10 ¹⁶
-2	n ⁺		2.5		6 x 10 ¹⁶
CD4-R33-1	n ⁺		2.6 - 3.5		1.3 x 10 ¹⁷
-2	n ⁺		-		-
CD4-R34-1	n ⁺		5.2		6 x 10 ¹⁷
-2	n ⁺		3.1		8 x 10 ¹⁷
CD4-R35-1	n ⁺		9.1		3.7 x 10 ¹⁷
-2	n ⁺		4.2		4.9 x 10 ¹⁷
CD4-R36-1	n ⁺		2.8		-
-2	n ⁺		2.8		-
CD3-R38-1	n ⁺	2.8	3.5		
-2	n ⁺	1.5	1.7		
CD3-R39-1	n ⁺	3.8	0.5		
-2	n ⁺	1.4	<0.5		
CD3-R41-1	SI		5.2		3.5 x 10 ¹⁶
-2	SI		2.1		1.4 x 10 ¹⁶
CD3-R42-1	SI		4.2		8.4 x 10 ¹⁷
-2	SI				8.5 x 10 ¹⁷
CD3-R43-1	SI	5.0	4.2		
-2	SI	6.0	2.0		
CD4-R22-1	SI		12.6		6.4 x 10 ¹⁷
-2	SI		9.6		4.4 x 10 ¹⁷
CD4-R23-1	SI		2.0		6 x 10 ¹⁶
-2	SI		0.5		7 x 10 ¹⁶
CD4-R24-1	SI		5.5		
-2	SI		6.0		
CD4-R25-1	SI		6.3		6 x 10 ¹⁶
-2	SI		2.8		5 x 10 ¹⁶
CD4-R28-1	SI		3.1		
-2	SI		1.4		
CD3-R36-1	SI	8.4	0.7		5 x 10 ¹⁷
-2	SI	5.0	0.5		

2.3 Ion Implantation

Silicon ions were implanted into several of the epitaxial layers shown above. The slice numbers and the required concentrations and thicknesses are shown in Table 3. The implants were made with a full dose of Si⁺ at 150 keV and a quarter dose at 50 keV.

TABLE 3
Samples to be Implanted

Slice No.	REQUIRED	
	Concentration	Layer Thickness
CD4-R32-2-1	6×10^{17}	0.2 μm
CD4-R33-1-A		
CD4-R35-1-1		
CD4-R35-2-A		
CD4-R32-2-2	1.2×10^{18}	0.2 μm
CD4-R33-1-B		
CD4-R35-1-2		
CD4-R35-2-B		

A calculated profile, according to LSS theory, is shown in Figure 19 for the first group of slices shown in Table 3. The lower energy provides a flat carrier profile to the surface.

Measurements using a four-point probe were made on Sample CD4-R33-1-A implanted with 1×10^{13} at 150 kV and 2.5×10^{12} at 50 kV. With no annealing the sheet conductivity σ_d ranged between 3.53 to

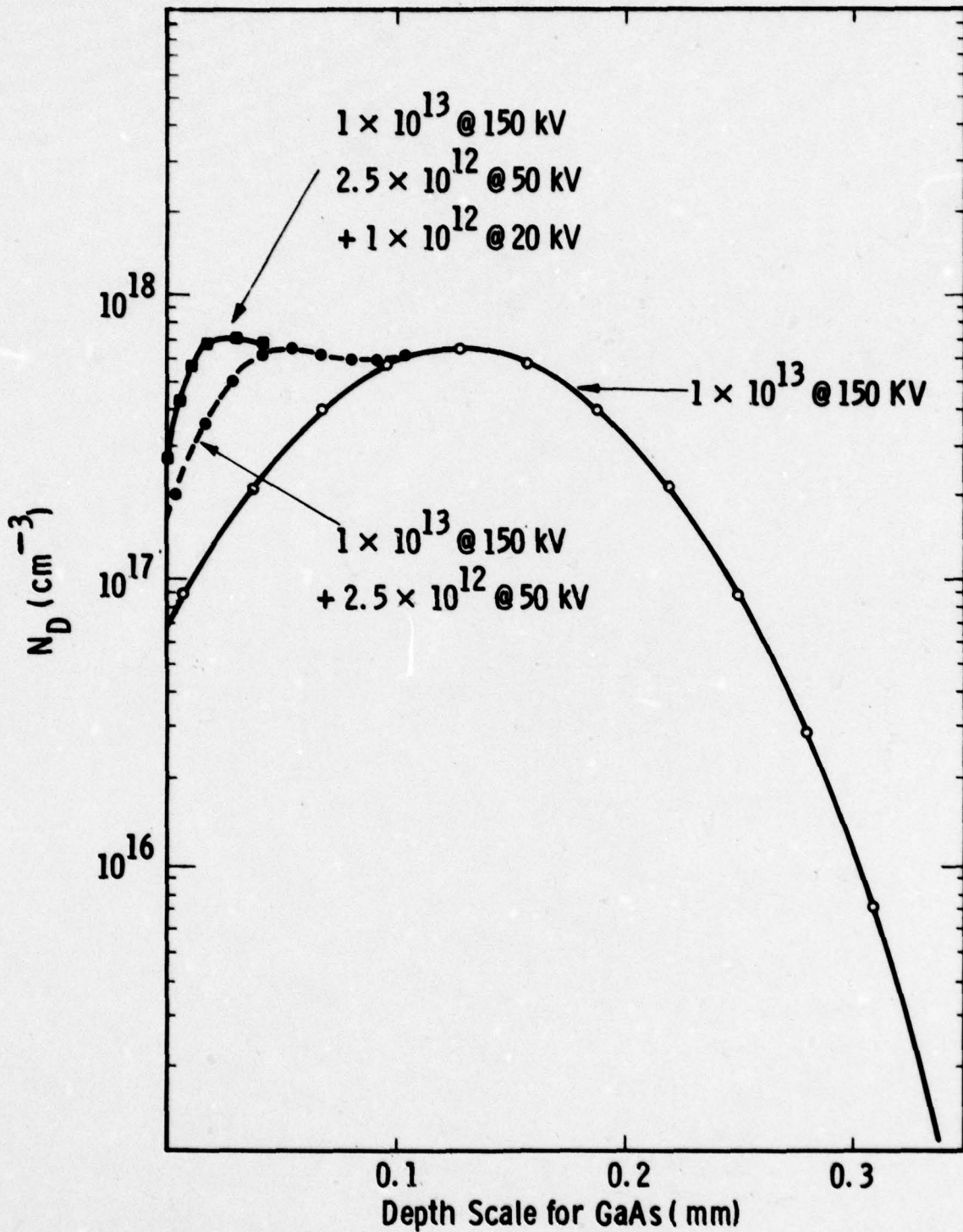


Fig. 19—Ion implantation profiles for silicon into gallium arsenide for use in VMIST structure

$5.02 \times 10^{-6} \Omega^{-1} \text{ cm}^{-1}$ in the dark at 1.5 volts applied and had a value of $3.1 \times 10^{-5} \Omega^{-1} \text{ cm}^{-1}$ in the dark with 22.5 volts applied. This implies that there may be some contact problems at the lower voltage. With the application of a bright tungsten light, the lower voltage conductivity values increased to $5.7 \times 10^{-6} \Omega^{-1} \text{ cm}^{-1}$; while for the 22.5 volt supply there was evidence of breakdown to the lower n-type layer ($\sigma_d = 6.7 \times 10^{-5} \Omega^{-1} \text{ cm}^{-1}$).

The sample was then cleaved in two, and the two halves designated a and b. CD4-R33-1-Aa was capped with 600Å of pyrolytic Si_3N_4 (deposited at 680°C) covered by 2000Å of pyrolytic SiO_2 (deposited at 420°C). A low temperature of 750°C was chosen for the annealing to avoid diffusion of the zinc from the p-type layer as much as possible. The annealing was performed in forming gas. The values of sheet conductivity after annealing are

- $3.67 \times 10^{-4} \Omega^{-1} \text{ cm}^{-1}$ (at 1.5 volts in the dark)
- $5.17 \times 10^{-4} \Omega^{-1} \text{ cm}^{-1}$ (at 22.5 volts in the dark)
- $5.45 \times 10^{-4} \Omega^{-1} \text{ cm}^{-1}$ (at 22.5 volts in tungsten light)

These values should be compared with a sheet conductivity of $6 \times 10^{-3} \Omega^{-1} \text{ cm}^{-1}$ which would be obtained if the implanted silicon were 100% activated and the resulting carriers had a mobility of 3000 $\text{cm}^2/\text{V-sec}$. This figure for mobility is pessimistic (for 1.25×10^{13} dose at 400 kV other workers⁽⁵⁾ have obtained figures closer to 4000 $\text{cm}^2/\text{V-sec}$). Obviously, the activation is not 100%, and if we assume the above mobility, the activation is quite low - more like 9%.

97
The second half of Sample CD4-R33-1-A was capped with pyro-
lytically deposited SiO₂ on the front only. A 650°C anneal for 1/2 hour
yielded

$$\sigma_d = 2 \times 10^{-4} \quad (\text{at } 22.5 \text{ volts in dark})$$

$$\sigma_d = 3-4 \times 10^{-4} \quad (\text{at } 22.5 \text{ volts in light})$$

which is somewhat worse than the standard encapsulant. 650°C was chosen
both for the zinc diffusion problem and the fact that gallium is known
to diffuse through SiO₂.

Both samples, when examined using the thermal probes, showed
p-type behavior (a) being more strongly p-type than (b). While this
measurement is not conclusive, it confirms the poor activation efficiency
of the silicon implant into the p-type epitaxial layer. Capacitance
voltage measurements (shown in Figure 20) also indicate that the surface,
at least, is still p-type.

Curve 697430-A

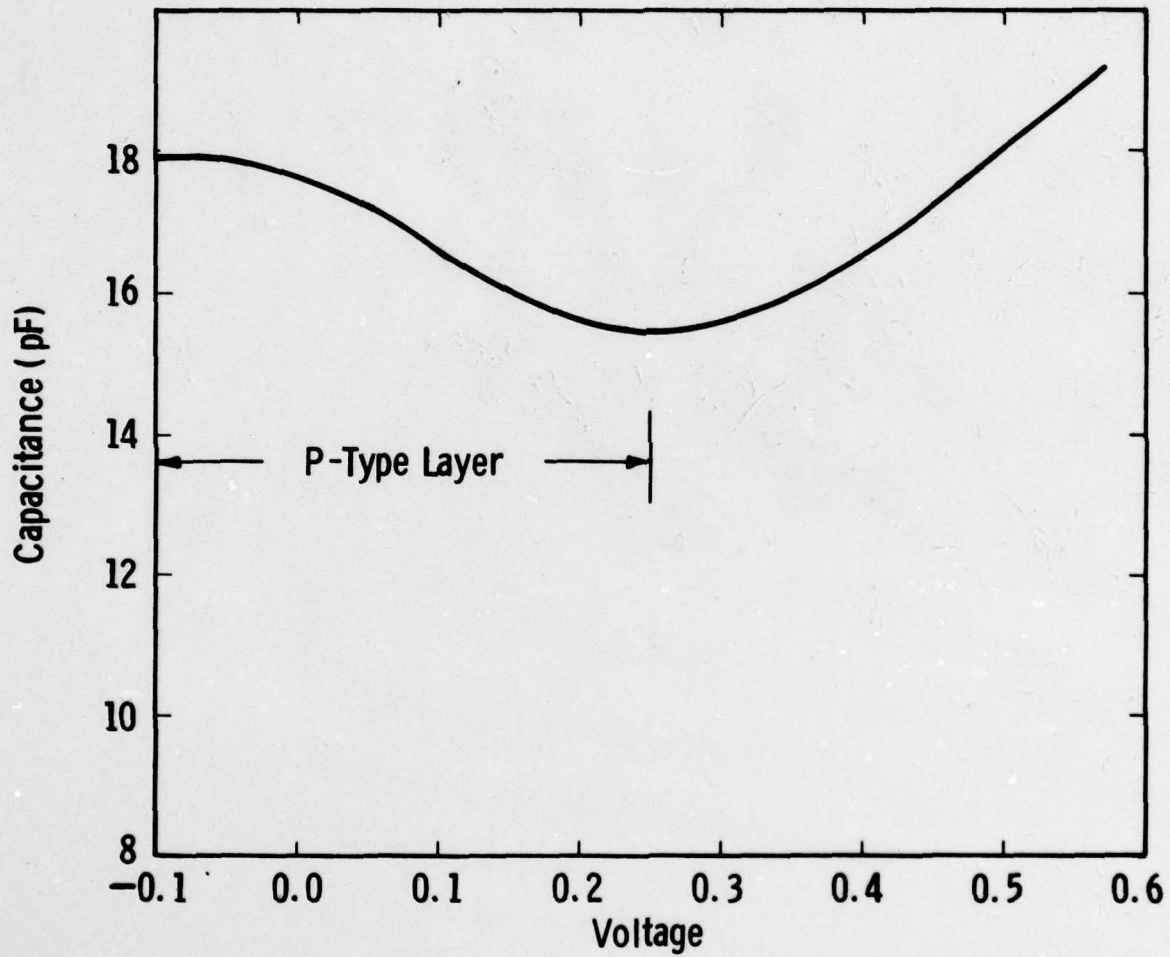


Fig. 20—Capacitance voltage plot for CD4-R33-1Ab showing a P-type surface layer.

3. DIELECTRIC INVESTIGATIONS

3.1 Discussion

The two most important factors that govern the performance of inversion mode field effect transistors are (a) the surface mobility and velocity of the carriers in the inversion layer (in this case electrons). If the mobility is not sufficiently higher than that of silicon ($200 \text{ cm}^2/\text{volt sec}$) then the advantage of gallium arsenide will have disappeared and the more difficult technology development cannot be justified. A factor of ten ($2000 \text{ cm}^2/\text{volt sec}$) is a reasonable target for which to aim. The saturated surface velocity should exceed that of silicon ($5 \times 10^6 \text{ cm/sec}$) by a factor of two (see Appendix A) if improved device performance is expected. (b) The electrical and chemical stability of the dielectric used. Chemical stability requires that the layer not deteriorate on contact with the air, be unduly hygroscopic and be able to withstand any subsequent fabrication steps, annealing or bonding operations. Electrical stability is more subtle than the chemical stability. It requires that the dielectric strength of the layers not deteriorate but, more importantly, that any surface states present be minimal and unchanging.

Experience with silicon indicates that there are two kinds of states which affect MOS performance: (a) Fast surface states (N_{ST}) which have communication with the conduction band of the semiconductor and which are filled and emptied as the Fermi level at the surface is raised

and lowered. The effect of these states is to distort the shape of the C-V curve as shown in curve B of Fig. 21. Curve A is the ideal curve without surface states;

(b) Insulator charges (Q_{SS}) which are trapped in the insulator itself. An example of such insulator charges are sodium ions in silicon dioxide on silicon devices. These are generally known as slow states because of their long time constants. Their effect is to shift the curve from B to C.

3.2 Stability

(a) Analysis of the Results

The major problem in evaluating the C-V data obtained from measurements at 1 MHz of the anodic oxide or gallium arsenide is the presence of the hysteresis. A typical curve obtained for p-type gallium arsenide is shown in Fig. 22. Beginning at a positive voltage (usually 15-20 volts) at point A, the bias is decreased until it reaches a negative voltage at point B ($V_A = 1V_B$). During this excursion, the semiconductor goes from "inversion" at point A to accumulation at point B following the curve through point C. The voltage is held at point B for a fixed time and then the voltage is returned at the same rate to point A but this time the curve proceeds via point D.

The theoretical curve for the same carrier concentration and oxide thickness but with no surface or oxide charges present is shown as the dotted line in Fig. 22. The measured curves are obviously shifted toward the negative voltages corresponding to the trapping of positive charge but in addition to the shift, the shapes of the curves are perturbed

Curve 697426-A

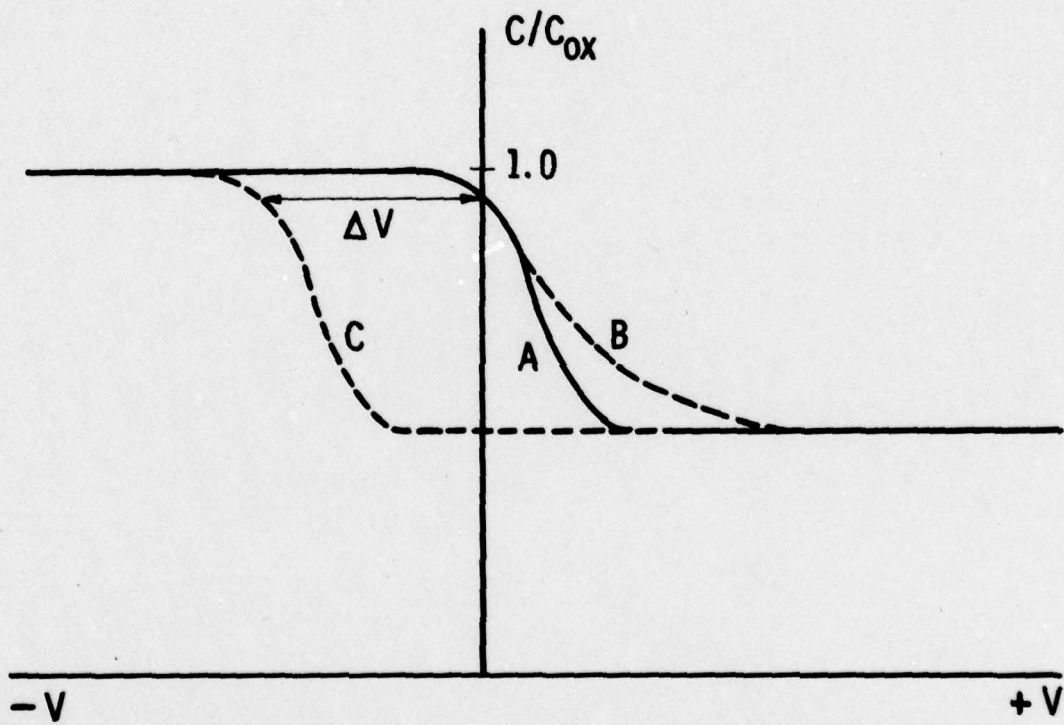


Fig. 21—Effect of surface and insulator changes on the ideal C-V characteristic for MIS devices. A = ideal; B = distorted due to fast states; C = shifted from A due to fixed or noncommunicating charge

Curve 697425-A

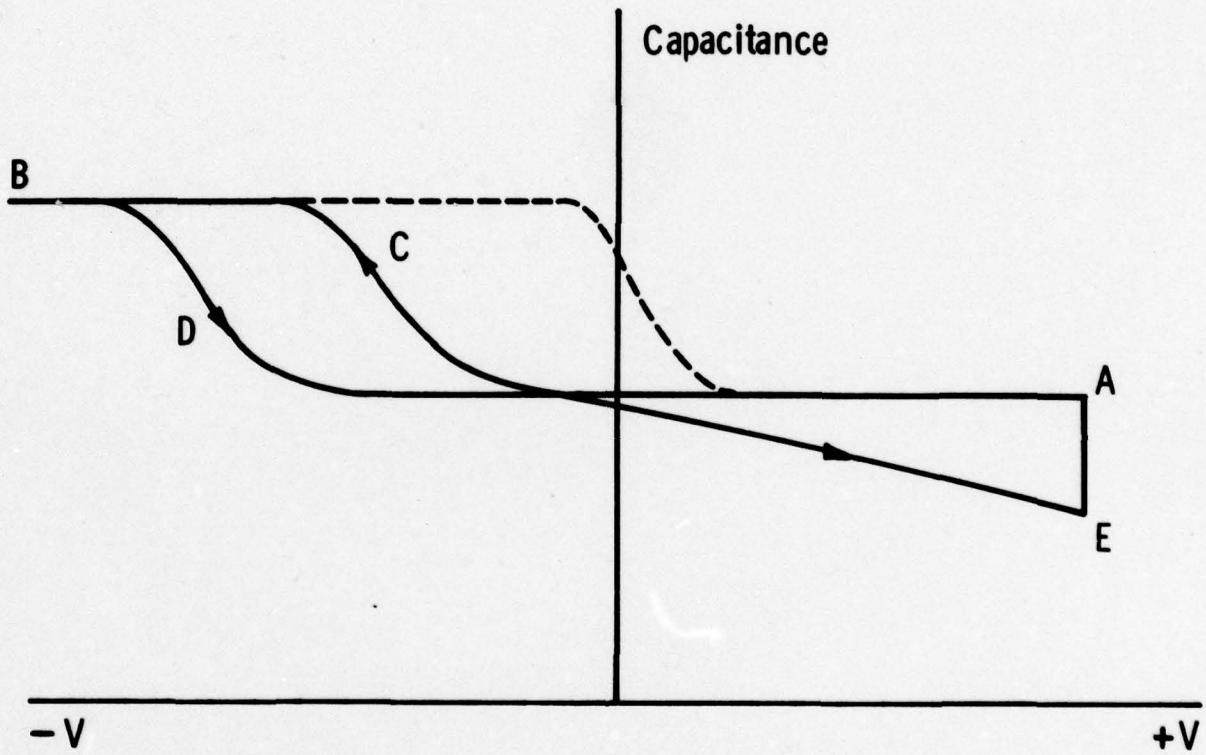


Fig. 22—C-V curves showing hysteresis loop

from the theoretical shapes indicating the presence of fast states whose occupancy changes during the bias sweep.

The hysteresis is due to trapping centers in the forbidden band filling up as the voltage is driven from A to B and then held at B. In order to investigate these centers, attention was centered on the curve ACB from whose shape the distribution of the states in the bandgap and their density can be determined.

If the shift of the capacitance voltage curve from the ideal, trap free case is ΔV then the amount of charge Q trapped in the system that produces this shift is given by $Q = C_0 \cdot \Delta V$ where C_0 is the capacitance of the anodic oxide layer. The surface potential of the oxide (ϕ_s) can be determined from the measured capacitance of the system (C) so that by measuring ΔV as a function of C , we can calculate the total amount of trapped charge as a function of surface potential. By differentiating the charge as a function of surface potential, we can determine the density of surface states as a function of their position in the energy bands.

The derivation of the equations and the computer program based on these equations is given in Appendix B.

The curve from D to E shows the deep depletion effects in the semiconductor when the voltage sweep is too fast to allow a sufficient number of minority carriers to be thermally generated to maintain equilibrium.

3.3 Effect of Treatment of Surface State Density

(a) Annealing Time

Fig. 23 shows the C-V curves obtained on a 1000Å thick (50 volt) anodic oxide on p-type (10^{17} cm⁻³) gallium arsenide annealed for various times in a nitrogen atmosphere at 360°C. Using the analysis described above the surface state density as a function of surface potential is shown in Fig. 24.

The minima of the curves are located at approximately -0.3 eV (on the conduction band side of the mid gap point which is 0.0 eV on this figure). The curves are not smooth in these measurements due to the fact that the data was taken from the C-V curves plotted on an XY recorder. Subsequent measurements are taken directly.

The obvious conclusion to be drawn from this data is that the minimum value of surface density decreases as the time of annealing is increased. However, the curve obtained from the four hour anneal, while having a lower minimum, lies above the 3, 2 and 1 hour curves in the region from -0.85 to 0.2 eV. Thus there is an increase in the surface state density in this region. This is borne out by the size of the hysteresis loop for the four hour C-V curve shown in Fig. 23.

The rapid rise of the surface state density as the surface potential departs from the position of the minimum means that it is very difficult to shift the Fermi level very far from this value. The fact that the barrier heights of Schottky contacts on gallium arsenide are not strongly dependent on the metal used⁽⁶⁾ confirms this situation.

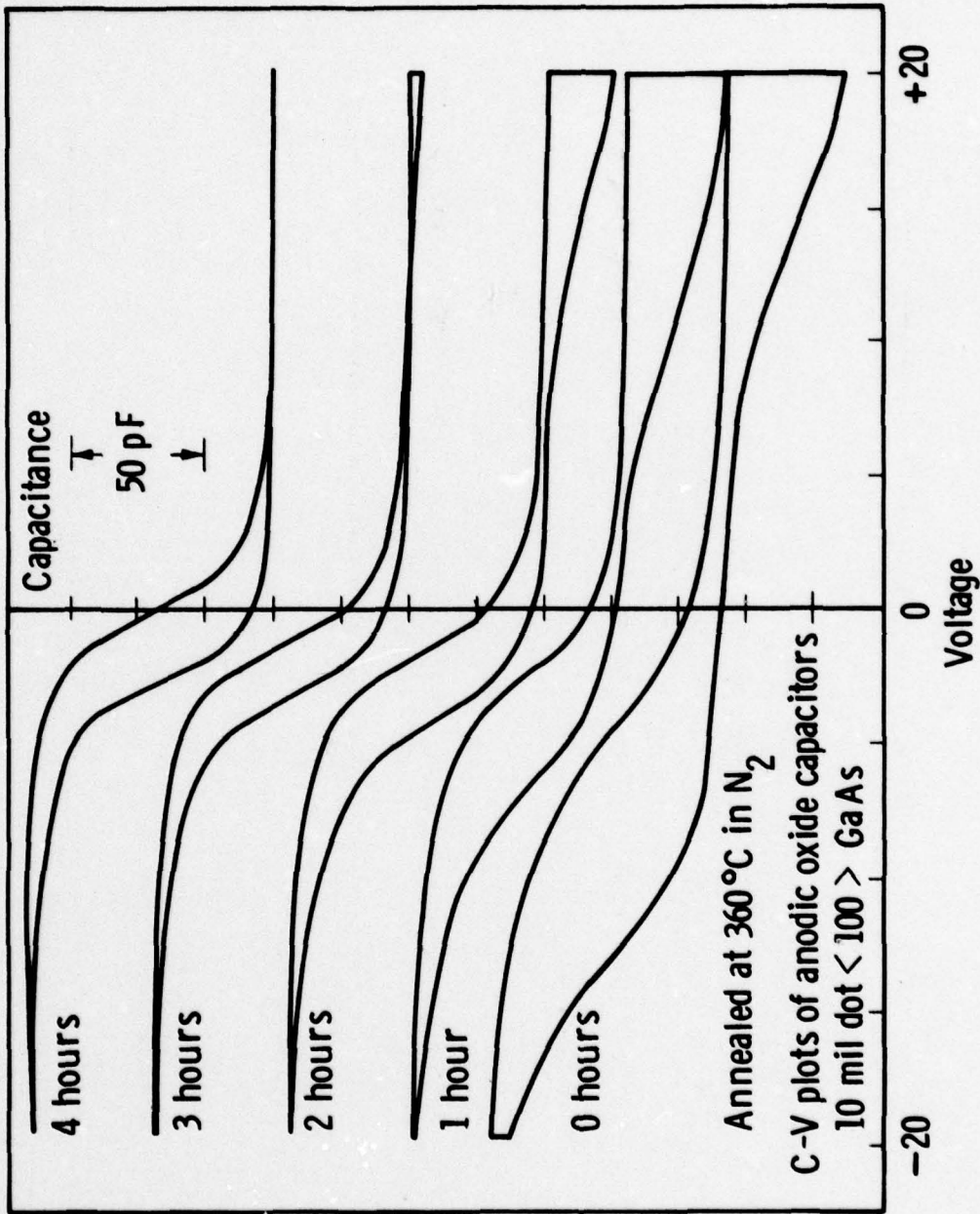


Fig. 23—C-V curves as a function of annealing time

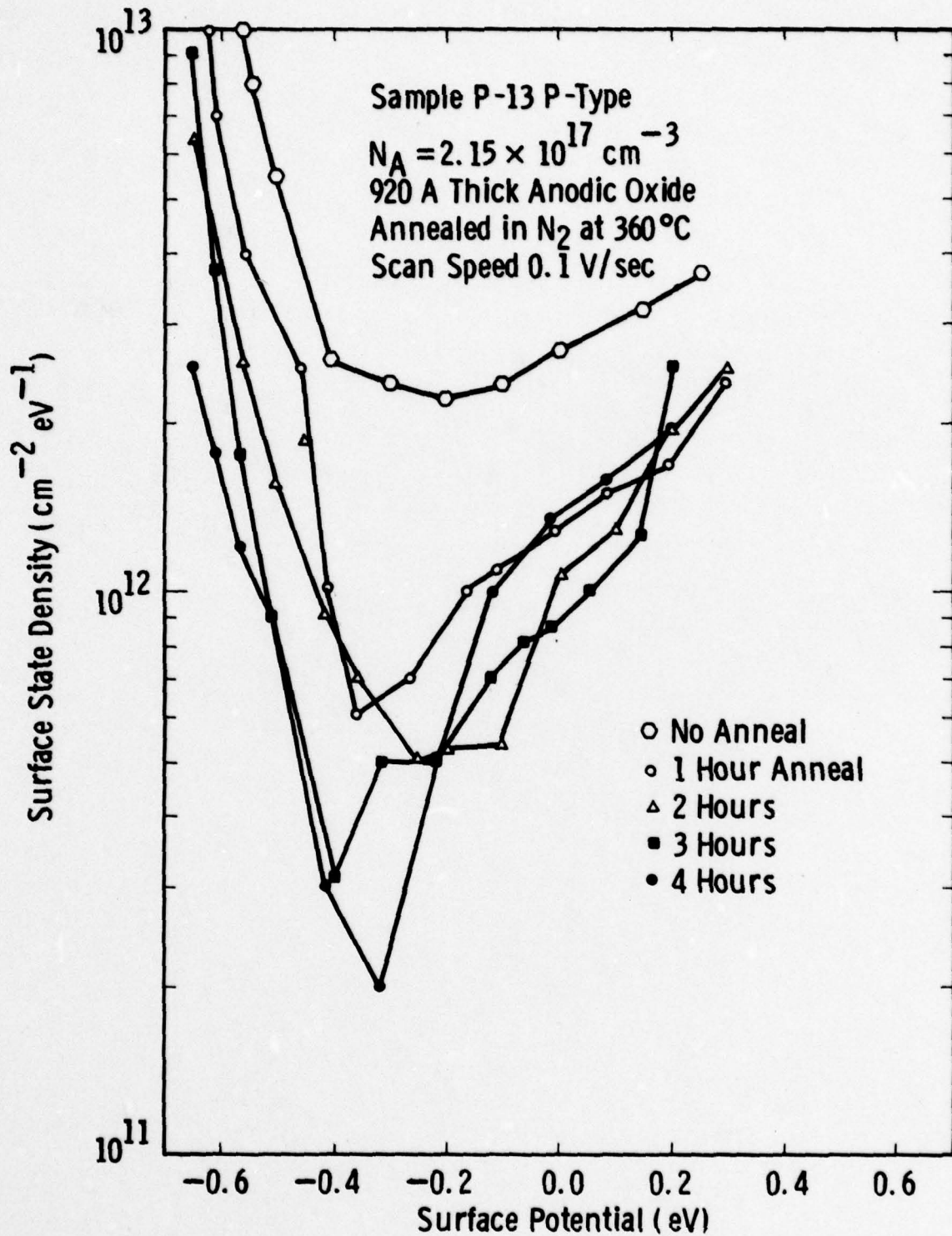


Fig. 24—Surface state density as a function of surface potential for various anneal times

(b) Sweep Time

The effect of sweep time on the measurement of the surface state density is shown in Figure 25. In this sample the minimum lies at near the mid gap point in contrast to the previous sample. This shift in the position of the minimum is not understood.

At slow scan speeds (0.01 volts/sec) the minimum of the curve lies at $5.5 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$, while at 1 volt/sec it is down to 1.1×10^{11} . This effect is related to the hysteresis loops seen on all the eV measurements in that the states have a finite charging up time associated with them.

The shape of the two curves is very similar, indicating that the time constant of the traps is the same irrespective of their position within the forbidden band.

Curve 697431-A

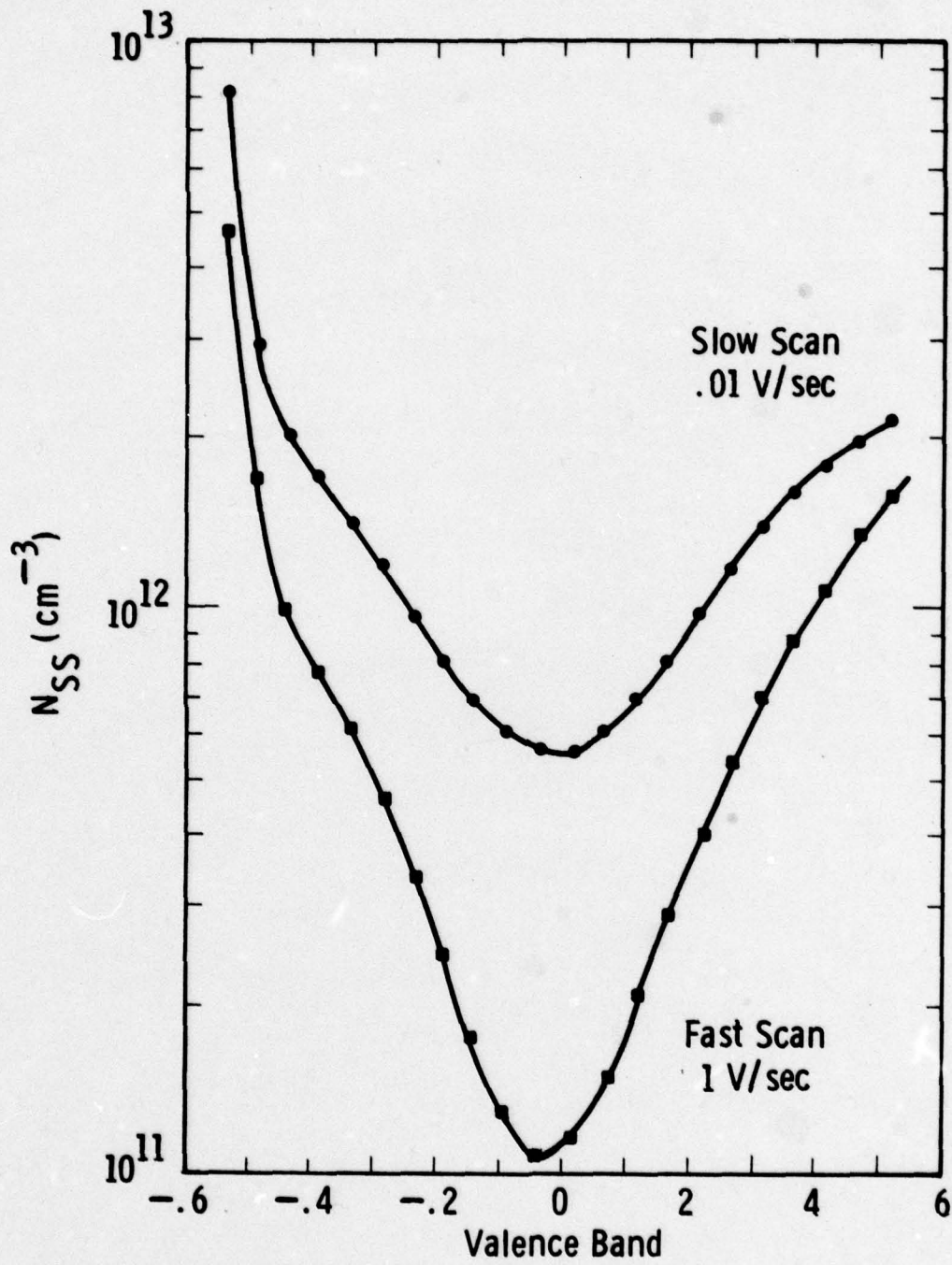


Fig. 25—Apparent surface state density variations with sweep rate of voltage

4. DEVICE DESIGN CONSIDERATIONS

4.1 Mask Set for V-groove Device

The mask set was discussed in Section 1.4(a). This device does not have an optimized design for high frequency performance since there is significant overlap between the gate and the source and drain regions (see Figure 8). The parasitic capacitances between the gate and drain is a feedback element that reduces the device gain.⁽⁷⁾ The device is useful in that it does not require critical control of the etching procedure.

The performance of the V-groove device with optimum parameters is discussed in more detail in Appendix A.

5. FUTURE PLANS IN PURSUING VERTICAL CHANNEL MOSFET DEVICE IN GaAs

5.1 VMIST Geometry

This geometry has already been proven in silicon⁽³⁾ and is the preferred geometry for this contract. Unfortunately, problems with material preparation have not allowed even the simpler V-groove device to be fabricated. In any future effort the control of the layer formation would have to be sufficient that the device fabrication procedure described in Section 1.4(a) could be implemented.

5.2 Stable Insulator

Anodic oxides have proved interesting but have not provided sufficient stability and freedom from hysteresis to make them a completely satisfactory gate insulator. Recent results by Chang and others⁽⁸⁾ have indicated that oxidation of the gallium arsenide surface using plasma oxidation and including a thin (100Å) layer of Al₂O₃ produces a dielectric with low leakage and a fixed (slow) charge density of $5 \times 10^{10} \text{ cm}^{-2}$. The film, however, does have hysteresis and no information was given regarding the fast states.

5.3 n⁺-p-n⁺ Profile

For the fabrication of the VMIST device, precise control of the thicknesses of the various layers is required. The optimum way of producing the material would seem to be the vapor phase or liquid phase

epitaxy of the n^- and p layers and rely on the ion implantation of silicon for the n^+ layer to form the source contact of the device.

The layers discussed in Section 2.2 were fabricated using the VPE reactor shown in Figure 26 which was designed to provide flexibility in doping of the epitaxial layers. The loping schemes used were dilute H_2S , solid sulfur, tin chloride, thin doped gallium source (all n-type) and liquid diethyl zinc (p-type).

Inadequate control of gas flow and gallium source kinetics have led to unreproducible layers so that a new VPE reactor has been designed (see Figure 27).

In order to accurately control the gas flow, mass flow controllers were installed, and to cut down on operator error or variations, switching of gases is accomplished with solenoid valves. The mass flow controllers, valves and thermally controlled bubbles for $AsCl_3$ and liquid dopants are all contained within a nitrogen enclosure (see Figure 28) to prevent possible oxygen contamination.

To improve the gallium source kinetics the temperature of the source has to be accurately controlled and, more importantly, the temperature gradient across the source must be close to zero (to avoid partial crusting of gallium arsenide on the gallium source). This is achieved by using a sodium heat pipe 24" long which controls a region 18" long to an accuracy of temperature of $\pm 0.5^\circ C$ and a temperature gradient less than $0.5^\circ C$ across the 18" length. The sodium heat pipe and the quartz deposition tube within it are designed for 2-inch diameter GaAs substrates.



Figure 26 - Original VPE reactor.

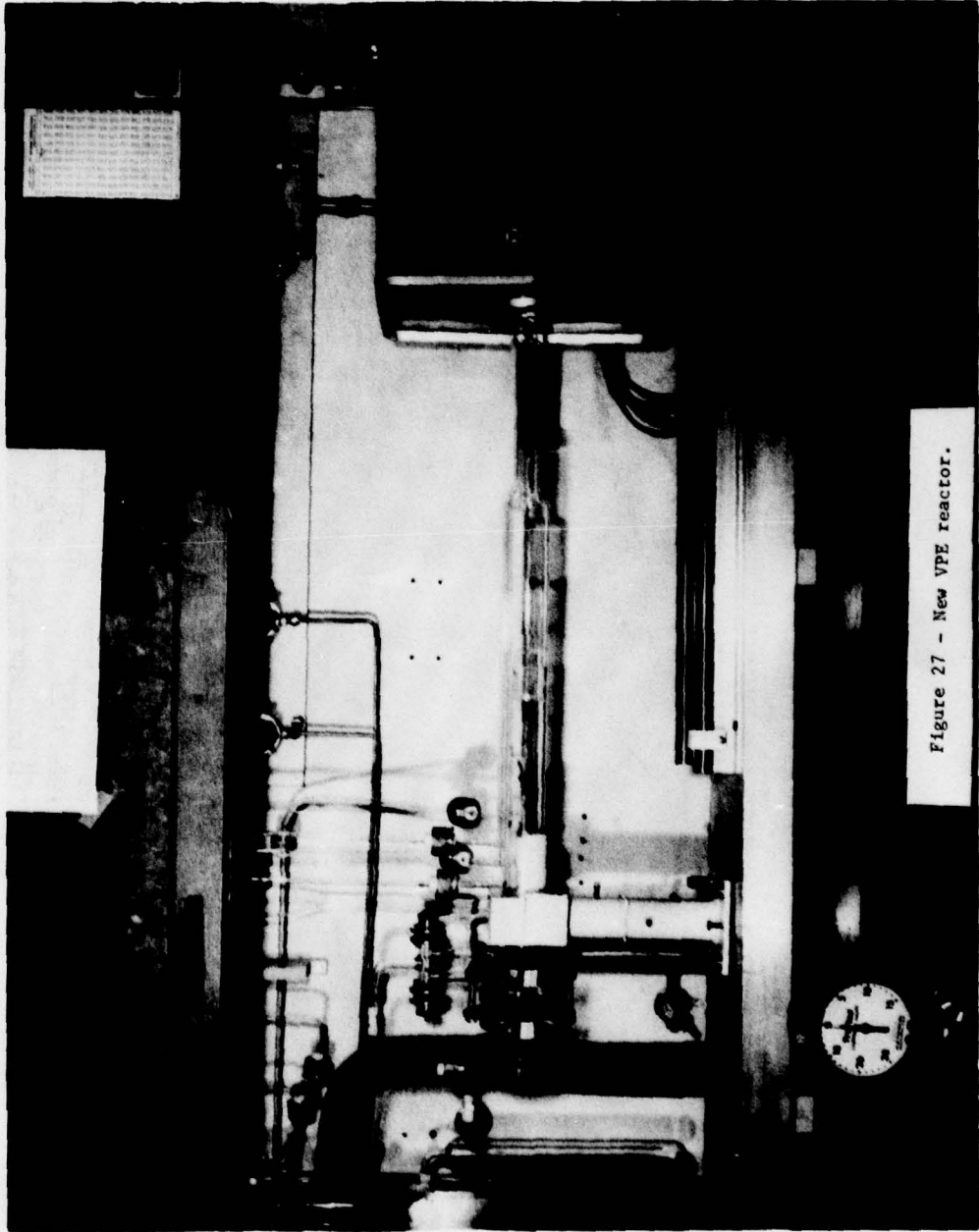


Figure 27 - New VPE reactor.

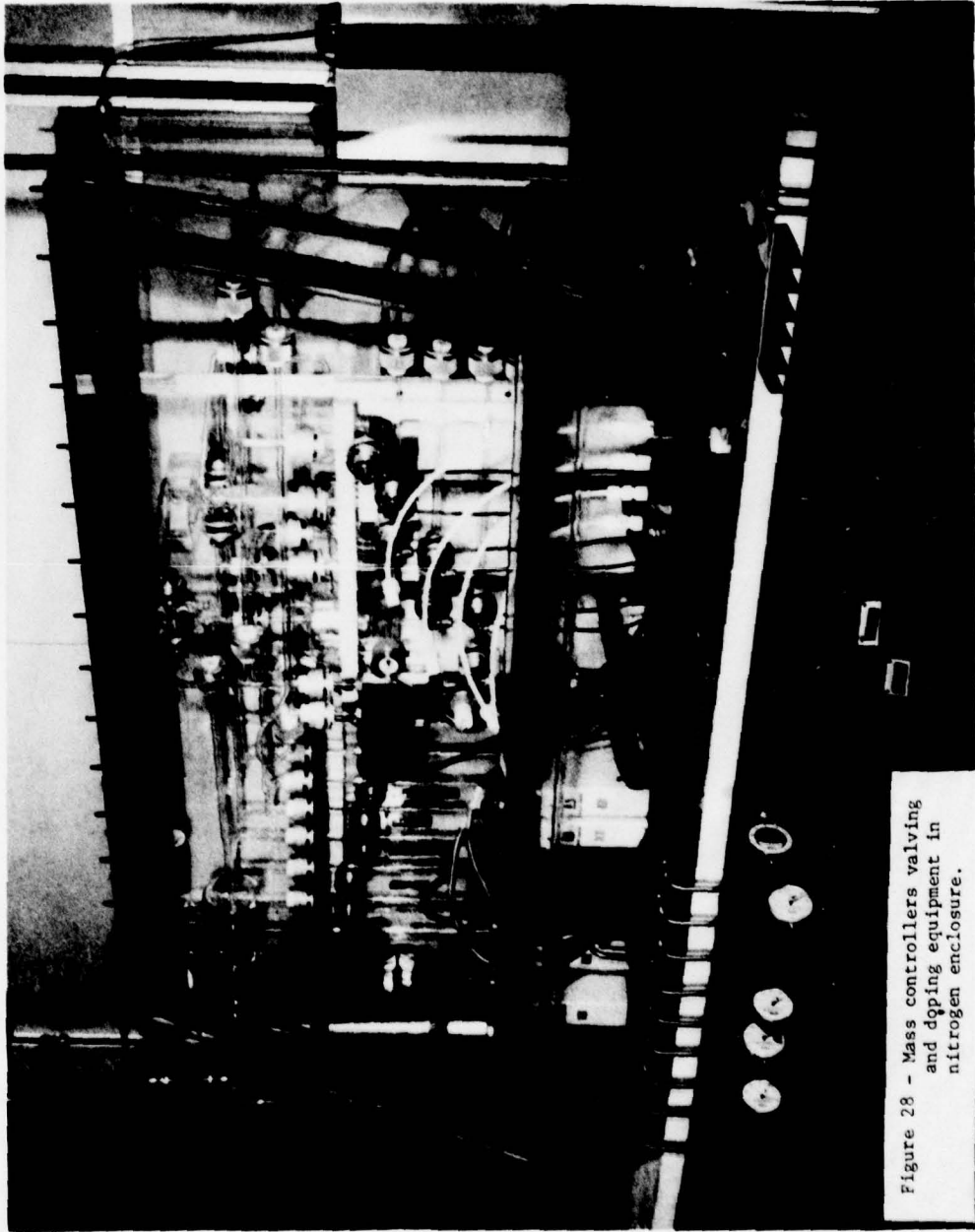


Figure 28 - Mass controllers valving
and doping equipment in
nitrogen enclosure.

Dual source capability is provided on this reactor so that we may switch from a doped source to an undoped one, and vice versa.

A six-zone conventional furnace provides a uniform and controllable temperature profile over the deposition region.

The reactor to date has been used to grow unintentionally doped buffer layers for the ion implantation of the active n-type layer. It has shown the capability of growing good surface finish layers with less than 10% variation in layer thickness. It has not been used to grow intentionally doped n or p layers to date.

6. FUTURE RECOMMENDATIONS

The results obtained in this program and by other workers indicate that the problem of the large density of surface states on gallium arsenide has not been conquered. A recent approach, plasma oxidation of the surface,⁽⁸⁾ has indicated that the fixed charge (flat band voltage shift) can be made as low as $5 \times 10^{10} \text{ cm}^{-2}$. Devices have been fabricated using anodic oxidation, but most of these are used in the depletion mode where surface states are not a problem since they are largely empty. It is not clear that efficient inversion of the gallium arsenide surface has ever been achieved.

In contrast to this, recent results⁽⁹⁾ have indicated that indium phosphide has been inverted at the surface using SiO_2 as the dielectric layer. Indium phosphide has a higher saturated drift velocity than that of gallium arsenide which leads to a higher frequency response for a device with the same geometry. In addition, the breakdown field of indium phosphide is higher than that of gallium arsenide, resulting in a higher operating voltage and hence higher power. These arguments have been made previously⁽¹⁰⁾ for Schottky barrier gate devices.

There is also evidence⁽¹¹⁾ that ion implantation of n^+ dopants into indium phosphide results in higher activation than similar ones into gallium arsenide. Fabrication of the device should be no more difficult than for gallium arsenide. Ohmic contacts of gold-germanium have already been developed and the problems of the Schottky barrier that plague the MESFET device will not be present in the InP MISFET.

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APPENDIX A

ANALYSIS OF THE EFFECT OF LITHOGRAPHIC DESIGN RULES ON POWER DENSITY FOR VERTICAL MIS GaAs TRANSISTORS HAVING ONE MICRON p AND n⁻ REGIONS

Assuming that we will fabricate a vertical MIS GaAs transistor having a p-region of one micron thickness and an n⁻ region of approximately one micron thickness (corresponding to device having an output transit time-limited frequency of about $f = \frac{1}{2\pi\tau} \sim 16$ GHz), it is of interest to investigate the role of the design rule of "a" microns such that for a given power level the device power density is not excessive.

The design geometry of the VMIST device is illustrated in Figure A-1 where it is assumed that two V-grooves 3 μ deep are fabricated a distance M apart. As can be seen by the figure, we assume that a groove 3 μ deep will cut through 1) the 1 μ n⁻ region with its negligibly thin ion implanted n⁺ contact,* 2) the 1 μ p-region and 3) about 1 μ into the n⁺⁺ source substrate contact. Assuming an etch angle of 60° (really 57.7° for the anisotropic etches used), we find that

$$M \sim \left[\left(2 \times \frac{1}{2} \times 3\mu \right) + 6a \right] \sim (3\mu + 6a)\mu.$$

*The figure illustrates a VMIST device with the source as top contact in contrast to Fig. 8, but this does not affect the validity of the treatment.

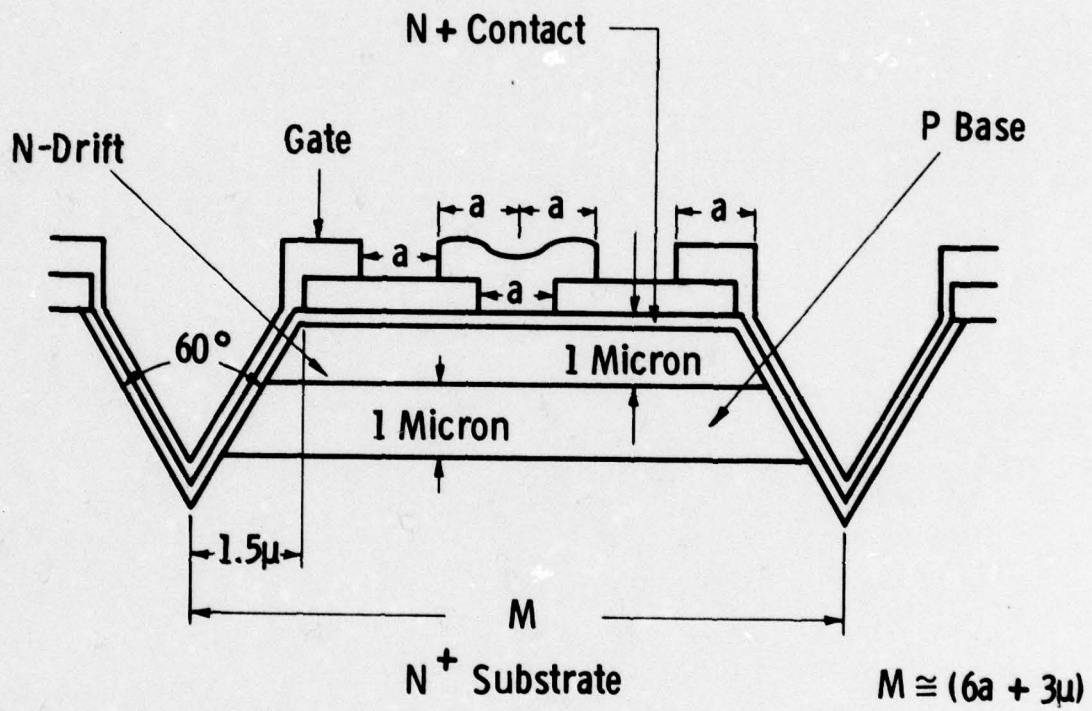


Fig. A-1 - Layout of unit cell of VMIST chip

Calculation of Chip Side "b" in Microns to Obtain a Given ac Power Output Pac

We assume that all carriers are moving with an effective saturation velocity v_{sat} . After Sigg⁽¹²⁾

$$g_m = \epsilon_{ox} v_{sat} / W_{ox}, \quad (A-1)$$

where W_{ox} is the VMIST oxide thickness.

Let us attempt to calculate the maximum current per unit length I_{max} by assuming the existence of same maximum effective gate voltage V_{max} given by

$$V_{max} = \beta E_{BD_{ox}} W_{ox}, \quad (A-2)$$

where $E_{BD_{ox}} =$ oxide breakdown field (volts/cm)

$\beta =$ reduction factor which accounts for lack of oxide integrity, edge effects, surface state reduction of effective field effect voltage, etc.

Letting $I_{max} = g_m V_{max}$, we have

$$= \frac{\epsilon_{ox} v_{sat}}{W_{ox}} \cdot \beta E_{BD_{max}} W_{ox}$$

or
$$I_{max} = \epsilon_{ox} v_{sat} E_{BD} \beta. \quad (A-3)$$

If we take the breakdown field for the gate insulator as (conservatively) $E_{BD_{max}} \sim 2 \times 10^6$ volts/cm; if we assume $\beta \sim 0.5$ and we take the effective saturation velocity anticipated for the GaAs VMIST as $v_{sat} \sim 10^7$ while we take the effective saturation velocity for the silicon VMOST as

$v_{sat} \sim 5 \times 10^6$ cm/sec⁽¹³⁾; and if, finally, we assume that both the VMIST and VMOST will have a breakdown voltage capability of $V_{BD} \sim 20$ volts, then we can generate the following table using Equations (A-1, A-2, A-3) and the fact that the maximum quiescent dc power dissipation for Class A operation, $P_{dc_{max}}$, is given by

$$P_{dc_{max}} \sim \frac{I_{max} V_{BD}}{4} . \quad (A-4)$$

Also included is the gate capacitance per unit length $C_{gate} = \frac{\epsilon_{ox} L}{W_{ox}}$, where L is the channel width, assumed equal to 1μ as in Figure A-1.

We also calculate the intrinsic cut-off frequency of each device

$$f_t = g_m / 2\pi C_{gate} .$$

In Table A-1 the values predicted for the VMOST device ($g_m = 16$ μ hos/ μ , $I_{max} = 160$ μ A/ μ) are in excellent agreement with results obtained during the VMOST Contract No. N00014-74-C-0012 with ONR, where Westinghouse typically obtained 18 μ hos/ μ and 180 mA/ μ for these two quantities.⁽¹³⁾ This gives partial credibility to the values of $g_m = 32$ μ hos/ μ , $I_{max} = 330$ mA/ μ , $P_{dc_{max}} = 1.5$ mW/ μ and $f_t \sim 16$ GHz predicted for the GaAs VMIST, if a surface saturation velocity of $\sim 10^7$ cm/sec can be obtained.

If we assume a chip size of $B \times B \mu^2$, then we can construct a VMIST device having N stripes of cross-section illustrated in Figure A-1. Thus, N would be given by B/M or $N = B/(3 + 6a)$ from Figure A-1. Each stripe is B microns long and dissipates a quiescent dc power of 1.5 mW/ μ from Table A-1. Thus,

$$\begin{aligned} P_{dc} &= \left\{ 2 \times 1.5 \text{ mW}/\mu \times B \right\} \times \#/\text{stripes} \\ &= \frac{2 \times 1.5 \text{ mW}/\mu \times B^2}{(3 + 6a)} . \end{aligned} \quad (A-5)$$

TABLE A-1
 COMPARISON OF MAXIMUM CAPABILITIES OF VMIST AND VMOST(2) DEVICES

	v_{satMOS}	g_m	$I_m = g_m V_{max}$	P_{dcmax}	C_{gate}^* (1000Å)	$g_m^*/2\pi C_{gate}$
VMOST (Si)	$5 \times 10^6 \frac{cm}{sec}$	$16 \frac{\mu mhos}{\mu}$	$160 \mu A/\mu$	$.75 \frac{mW}{\mu}$	$3.3 \times 10^{-4} pF/\mu$	8.3 GHz
VMIST (GaAs)	10^7	32	$350 \mu A/\mu$	$1.5 \frac{mW}{\mu}$	$3.3 \times 10^{-4} pF/\mu$	16.6 GHz

* $1 \mu gate$

If we assume that the output ac power P_{ac} is 50% of the dc quiescent dissipation, then for a given required P_{ac} (watts)

$$P_{ac} \cong 0.5 \text{ (dc quiescent power)} \cong \left(\frac{1.5 \times 10^{-3} B^2}{3 \times 6a} \right). \quad (\text{A-6})$$

Solving for the square chip size necessary to achieve a desired output power, P_{ac} , given an obtainable photolithographic design rule of "a" microns:

$$\text{Chip Side } B \cong 25 \sqrt{(3 + 6a)P_{ac}} \text{ microns} \quad (\text{A-7})$$

This equation is plotted in Figure A-2.

The dc quiescent device power density, PD, is given by the division of Equation (A-5) by B^2 the device area, or

$$\text{Power Density PD (watts/cm}^2\text{)} = \frac{3 \times 10^5}{(3 \times 6a)}. \quad (\text{A-8})$$

This equation is plotted in Figure A-3, where it can be seen that power densities approaching that of IMPATT diodes ($\sim 10^5$ W/cm²) can be achieved in the GaAs VMIST device with 1μ design rules.

Discussion

From Figure A-2 it can be seen (point A) that it would seem possible to design a VMIST chip approximately .008" x .008" square (excluding rads, etc.) having the capability of 4 watts rf at approximately 5-8 GHz (estimated) using only 2μ design rules - a rather loose constraint.

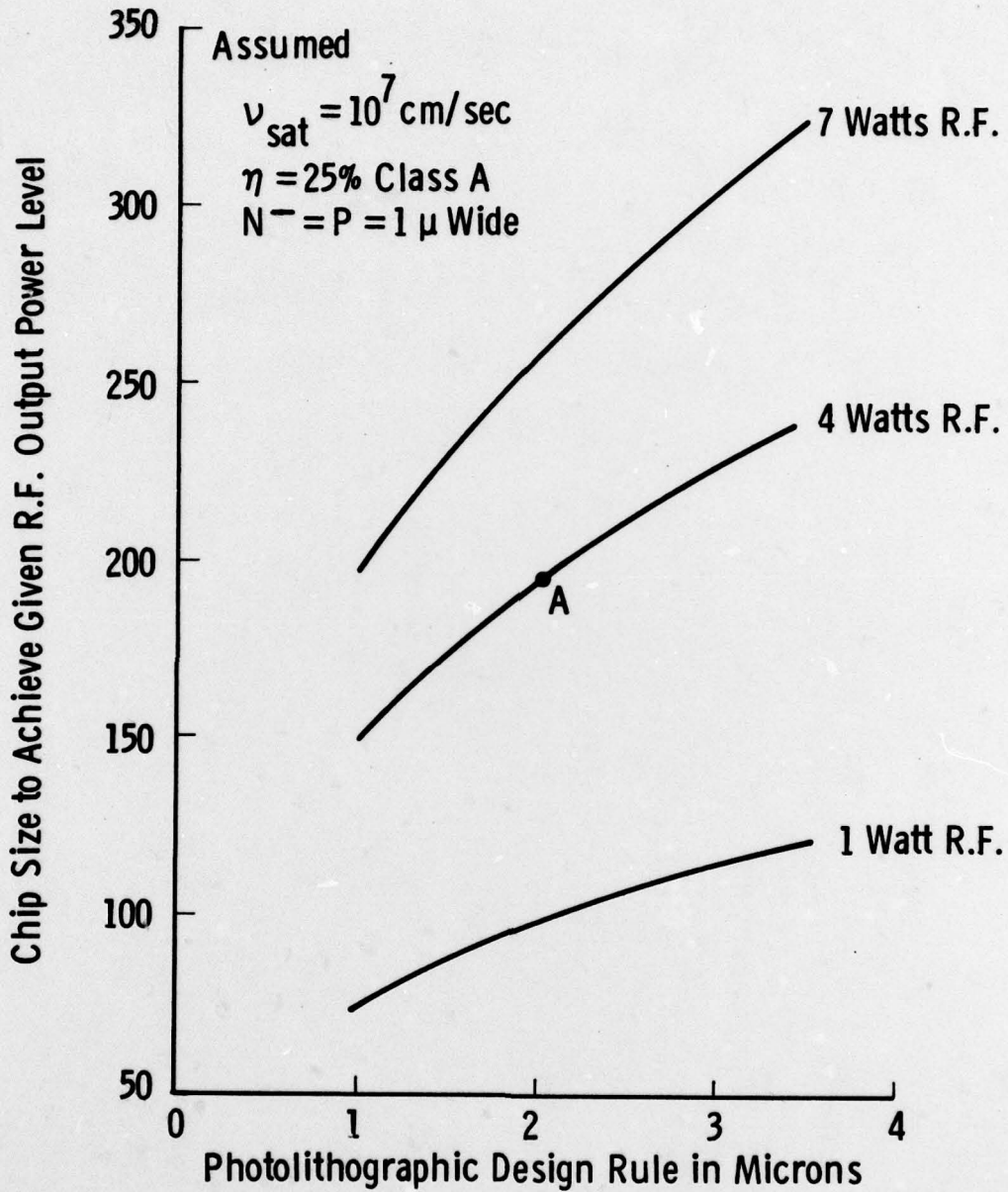


Fig. (A-2) —GaAs VMIST device analysis of photolithographic design rule on chip size, given a desired R.F. power level

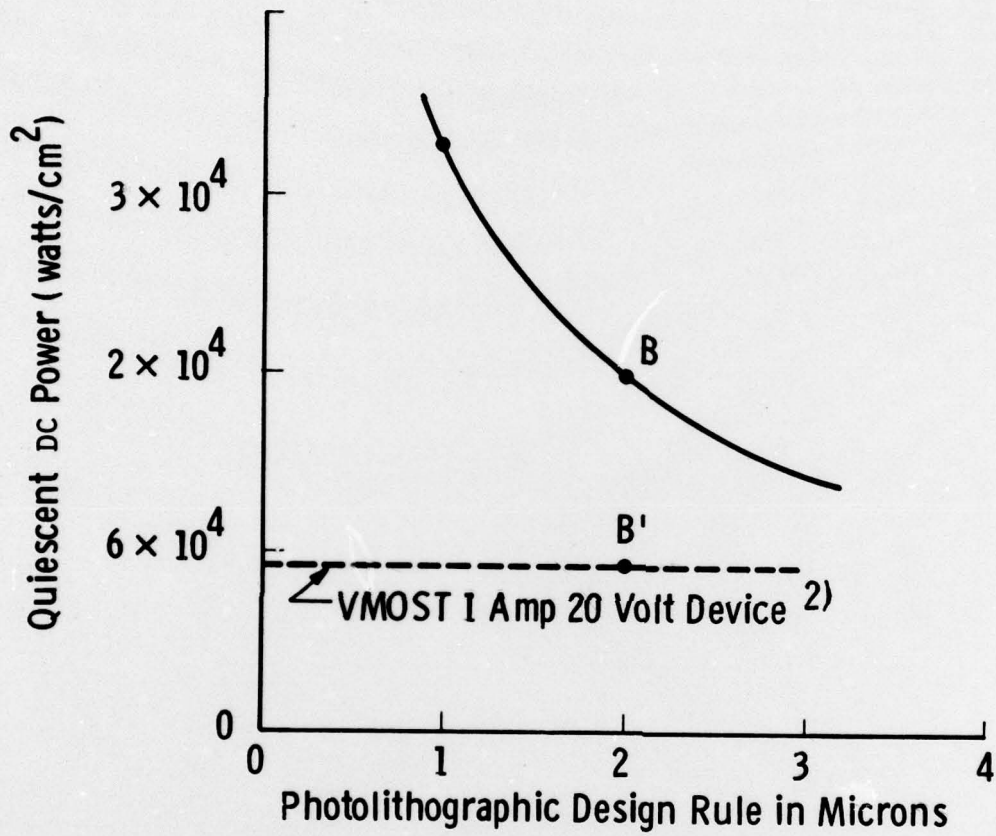


Fig. (A-3) — Quiescent dc power density vs design rules for GaAs VMIST

APPENDIX B

DEVIATION OF THE EQUATIONS FOR THE C-V CURVE

The various forms of the C-V curve in the absence of any surface states are shown in Figure B-1. Curve ABE is the so-called low frequency capacitance curve where the capacitance measurement frequency is low enough that the minority carriers in inversion can respond to the signal. This frequency is usually a few tens of Hz and below. At higher frequencies the capacitance follows the ABC curve, and if deep depletion occurs the ABD curve.

The oxide measurements are taken by illuminating the sample at point C to ensure equilibrium, and then sweeping the voltage so that the capacitance follows the curve CBA.

To derive the equations governing the shape of the curve ABC, the low frequency equations are used from point A to B and then a high frequency approximation from B to C.

The low frequency capacitance C_{LF} is related to the oxide capacitance C_o and the semiconductor capacitance via the relationship

$$C_{LF}/C_o = \frac{1}{1 + C_o/C_s}, \quad (B-1)$$

where $C_o = \frac{K_o \epsilon_o}{W_{ox}}$

$K_o \epsilon_o$ = the dielectric constant of the oxide of thickness W_{ox} .

Curve 697427-A

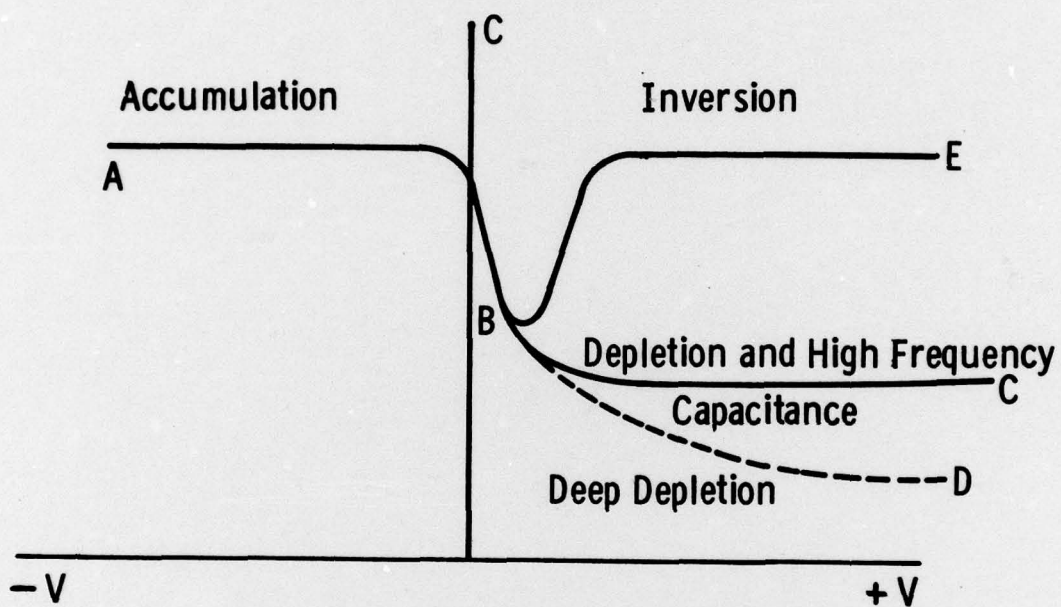


Fig. B1—C-V curves for a p-type semiconductor and insulating layer

The semiconductor capacitance

$$C_s = C_D (\text{sign of } u_s) \left[\frac{\sinh(u_s - u_F) + \sinh(u_F)}{F(u_s, u_F)} \right], \quad (\text{B-2})$$

where u_s is the surface potential and u_F is the Fermi level referenced to the center of the bandgap and is given by $u_F = \ln \left(\frac{N_a}{n_i} \right)$, C_D is the Debye length capacitance given by $C_D = \frac{K_s \epsilon_0}{L_D}$, and

$$L_D = \sqrt{\frac{K_s \epsilon_0}{2qn_i} \frac{kT}{q}} \quad \text{is the Debye length}$$

and n_i is the intrinsic carrier concentration.

$$F(u_s, u_F) = \left\{ 2 \left[\cosh(u_s - u_F) - \cosh(u_F) + u_s \sinh(u_F) \right] \right\}^{1/2}. \quad (\text{B-3})$$

The voltage on the metal contact is given by

$$V_G = \frac{kT}{q} \left[u_s + (\text{sign of } u_s) \frac{C_D}{C_0} F(u_s, u_F) \right]. \quad (\text{B-4})$$

These equations are appropriate from A to B on the capacitance-voltage curve. From B to C the 'high frequency' capacitance C_{HF} equations apply.

$$\frac{C_{HF}}{C_0} = \frac{1}{1 + C_0/C_s} \quad \text{where } C_s = \frac{K_s \epsilon_0}{W_{HF}} \quad (\text{B-5})$$

and

$$W_{HF} = L_D \exp(-u_F/2) \left[\left(8u_F - 12 + 4 \ln(u_F - 3) \right)^{1/2} - 2 \exp\left(u_F - \frac{u_s}{2}\right) + \frac{2 + \sqrt{2/e}}{\sqrt{u_F}} \right]. \quad (\text{B-6})$$

An additional equation used in the calculations is that governing the intrinsic carrier concentration n_i

$$n_i = \sqrt{N_c N_v} \exp(-E_g/kT) \quad \text{where } N_c \text{ and } N_v$$

are the densities of states in the conduction and valence bands, respectively. It appears in the program in the form

$$n_i = 4.05 \times 10^{14} \times T^{3/2} \times \exp(-E_g/2kT), \quad (\text{B-7})$$

which is appropriate for gallium arsenide.

Iterative Calculation of Carrier Concentration

In order to calculate the carrier concentration of the semiconductor from the minimum capacitance, it is necessary to use an iterative process based on the Taylor series since Equation (6-B) gives the capacitance as a function of Fermi level position.

$$\text{Let } C = f(u_F) \quad (\text{B-8})$$

$$\text{Define a function } F(u_F) = C - f(u_F) \quad (\text{B-9})$$

Now the Taylor series expansion of $F(u_F)$ is

$$F(u_F) = F(u_{Fn}) + (u_F - u_{Fn}) F'(u_{Fn}) + \text{higher terms}, \quad (\text{B-10})$$

where u_{Fn} is the n^{th} guess of the value which satisfies the equation.

$$\text{For } C = f(u_F) \quad F(u_F) = 0 \quad (\text{B-11})$$

$$\text{and } u_F = u_{Fn} - \frac{F(u_{Fn})}{F'(u_{Fn})} \quad \text{neglecting the higher terms.} \quad (\text{B-12})$$

Using the above formula we may guess a value u_{F_n} which satisfies the equation $C = f(u_F)$ and calculate from Equation (B-12) a new value of u_F which is a better fit. This new value can then be substituted for u_{F_n} to improve the fit still further, and so on. In line 720 of the program the fit is considered good enough if $u_F - u_{F_n} \leq 10^{-6}$.

Once the carrier concentration is known the theoretical trap-free curve can be calculated from Equations (B-1) to (B-7), knowing the oxide thickness. This theoretical curve is then compared with the experimental curve.

The curve fits are made using the IMSL program package. The program is shown below.

```

100     INTEGER Q1, Q2, P
110     REAL N1, N2, L1
120     DIMENSION V(40),CAP(40), VX(40),Q(40),XK(15),Y(15),
130     &C(14,3)
140     DIMENSION WK(630),DS(40),DSS(1),US(40),CX(40),WX(40)
150     DIMENSION UST(40),VT(40),CAPT(40),AB(40)
160     READ(11,4) N2,W0,T,N
170 C N2=INITIAL GUESS AT CARRIER CONC; W0=OXIDE THICKNESS;T=TEMP.
180 C N=NO. OF DATA POINTS;A1,A2,A3,A4 FIELD OF 24 CHARACTS FOR
190 C     SAMPLE NAME
200     READ(11,4) (VX(I),I=1,N)
210     READ(11,4) (CX(I),I=1,N)
220     READ(11,576) A1,A2,A3,A4
230 576     FORMAT(4A6)
240     BB = 1.0/(1.005*CX(N))
250     DO 26 I=1,N
260     AB(I)=CX(I)
270 C NORMALISE CAPACITANCE VALUES TO 1.005*MAX CAP VALUE
280 26     CX(I) = CX(I)*BB
290 4     FORMAT( )
300     PRINT 11
310 11     FORMAT(5X,'OFFSET VOLTAGE IS')
320     READ 4,VO
330     DO 27 I=1,N
340 27     VX(I)=VX(I)-VO
350     J=1
360     PRINT 55
370 C KX=NO OF KNOT POINTS FOR CURVE FIT
380     READ 4,KX
390 55     FORMAT(12X,'TYPE INTEGER >2 FOR NUMBER OF KNOTS')
400     P=0
410     C5=0
420 C V1=Q/KT
430     V1=0.02585*T/300
440 C NI=4.9E15(MDE*MDN/MO**2)**.75*EXP(-EG/2KT)
450     NI=4.05E14*SQRT(T**3)*EXP(-0.7172/V1)
460     PRINT 202
470 202     FORMAT(////,12X,'A PROGRAM THAT COMPARES C-V DATA TO THEORY')
480     PRINT 274
490 274     FORMAT(10X,'AND COMPUTES QSS FROM THE VOLTAGE DIFFERENCES'//)
500     PRINT 13, A1,A2,A3,A4
510 13     FORMAT(12X,'SAMPLE NUMBER ',4A6,/)
520 CO=K0*EPSO/WOX
530     CO=6.28E-9/W0
540 C LD=SQRT(KS*EPSO/2Q*NI*KT/Q)
550     L1=1.82E3*SQRT(V1/NI)
560 C CD=KS*EPSO/LD
570     C1=1.062E-12/L1
580 C FERMI LEVEL=U1
590     U1 = ALOG(N2/NI)
600 C CALCULATE SAMLE CARRIER CONC BY AN ITERATIVE PROCESS FROM
610 C     THE MAXIMUM AND MINIMUM CAP VALUES
620 C
630     B = 1.062E-12*(1.0/CX(1) - 1.0)/(CO*L1)
640 5     A = SQRT(8.*U1-12.+4.*ALOG(U1-3.))
650     E = B*EXP(U1/2)
660 C F IS F(X)
670     F = A + 2.52/SQRT(U1) - E
680 C FX IS F'(X)
690     FX = (4.*U1-10.)/((U1-3.)*A)-1.26/(U1*SQRT(U1))-0.5*E

```

```

700 C U2=U1-F(X)/F'(X)
710     U2 = U1 - F/FX
720     IF( ABS(U1-U2) - 1.0E-6*ABS(U1)) 20,20,10
730 10   U1 = U2
740     GO TO 5
750 20   N2 = N1*EXP(U1)
760     E = U1*V1
770 C
780     PRINT 203, T, W0, CO, N2, N1, E, U1
790 203   FORMAT(2X,'INPUT AND CALCULATED PARAMETERS ***',/,/,
800     &12X,'TEMPERATURE =',F6.1,' DEGREES K',/,12X,'OXIDE THICKNESS =
810     &F7.4,' MICRONS',/,12X,'OXIDE CAPACITANCE =',1P1E10.3,
820     &' F/SQ CM',/,12X,'DOPING LEVEL =',1P1E9.2,' PER CC',/,12X,
830     &'INTRINSIC LEVEL =',1P1E10.3,' PER CC',/,12X,'FERMI LEVEL =',
840     &OP1F7.4,' EV',/,12X,'NORMALIZED FERMI LEVEL =',F7.3,/)
850     PRINT 204, N
860 204   FORMAT(7X,'THE LIST OF NORMALIZED INPUT C-V DATA *',/,
870     &10X,'THE NUMBER OF POINTS IS',I3,/,12X,'I',7X,'C',8X,'CX',8X,
880     &/,11X,'****',5X,'*****',6X,'*****',6X,'*****')
890     DO 206 I = 1, N
900 206   PRINT 207, I,AB(I), CX(I), VX(I)
910 207   FORMAT(I13,F10.1,F10.3,F10.1)
920 C
930 C CALCULATE IDEAL TRAP FREE C-V CURVE
940 C
950 C U10 IS STARTING VALUE OF US
960     U10=-.2
970 44   DO 300 M=1,31
980     IF (ABS(U10).LT.0.001) U10=0.001
990     U=U10/V1
1000 C F(US,UF)=(2(COSH(US-UF)-COSH(UF)+US*SINH(UF)))*.5
1010     F=SQRT(EXP(U-U1)+EXP(U1-U)-EXP(U1)-EXP(-U1)+U*(EXP(U1)-EXP(-U
1020 C CS=CD*SIGN(US)*((SINH(US-UF)+SINH(UF))/F(US,UF))
1030     C2=C1*(U/SQRT(U**2))*(EXP(U-U1)-EXP(U1-U)+EXP(U1)-EXP(-U1))/(
1040     C3=1./(1+(CO/C2))
1050     V0=(U+(U/SQRT(U**2))*C1*F/CO)*V1
1060
1070 C PUT U AND V VALUES IN ARRAY
1080 400   UST(M)=U10
1090     VT(M)=V0
1100     IF(U10.EQ.0.001)U10=0.0
1110     U10=U10+0.05
1120 C PUT CAP VALUES IN ARRAY
1130     CAPT(M)=C3
1140     IF(P) 401,401,300
1150 C P SETS LIMIT ON THE MIN VALUE OF CAP. IT AVOIDS POINTS
1160 C ON THE INVERSION SIDE OF THE CV CURVE
1170 401   IF(CAPT(M).LE.CX(1)) P=M-1
1180     IF(CAPT(M).GT.CAPT(M-1)) P=M-1
1190 300   CONTINUE
1200 253   PRINT 6
1210 6     FORMAT(////,2X,'OUTPUT DATA - CUBIC SPLINE FIT ****')
1220     PRINT 7, P
1230 7     FORMAT(/,12X,
1240     &'NUMBER OF MATCHING THEORETICAL AND XPMTL POINTS IS',I3,/)
1250     DO 787 Q1=1,P

```

```

1260      Q2=P+1-Q1
1270      CAP(Q1)=CAPT(Q2)
1280      V(Q1)=VT(Q2)
1290 787   US(Q1)=UST(Q2)
1300      XK1 = KX - 1
1310      H = KX1
1320      XK(1) = 0.999*CX(1)
1330      XK(KX) = 1.0
1340      H = (XK(KX)-XK(1))/H
1350      DO 85 I=2,KX1
1360 85   XK(I) = XK(I-1) + H
1370 C
1380 C CURVE FIT TO EXPERIMENTAL RESULTS
1390 90   CALL ICSVKU(CX,VX,N,XK,KX,Y,C,14,ERROR,WK,IER)
1400     PRINT 92, ERROR
1410 92   FORMAT(//,12X,'ERROR IN FITTING THE DATA IS',1P1E8.2,/)
1420     PRINT 94, (XK(I),I=1,KX)
1430 94   FORMAT(12X,'THE KNOT POINTS ARE.....',/,(1P5E13.3))
1440     H = XK(KX)-XK(KX1)
1450     Y(KX) = ((C(KX1,3)*H+C(KX1,2))*H+C(KX1,1))*H +Y(KX1)
1460 C GENERATE VOLTAGE VALUES AT EXPERIMENTAL CAP POINTS
1470     CALL ICSEVU(XK,Y,KX,C,14,CAP,WX,P,IER)
1480     H = C0/1.6023E-19
1490     DO 555 I=1,P
1500       L2=P+1-I
1510 555   Q(L2) = (V(I) - WX(I))*H
1520       PRINT 1
1530 1     FORMAT(6X,'UST',12X,'DV',/)
1540       DO 2 J=1,P
1550         DV=Q(J)/H
1560 2     PRINT 254,UST(J),DV
1570 254   FORMAT(1P2E12.3)
1575 C CURVE FIT US VERSUS QS
1580     H=KX1
1590     XK(1)=1.01*UST(1)
1600     XK(KX)=1.05*UST(P)
1610     H=(XK(KX)-XK(1))/H
1620     DO 93 I=2,KX1
1630 93   XK(I)=XK(I-1)+H
1640     CALL ICSVKU(UST,Q,P,XK,KX,Y,C,14,ERROR,WK,IER)
1650     PRINT 92, ERROR
1655 C DIFFERENTIATE
1660     CALL DCSEVU(XK,Y,KX,C,14,UST,DS,P,DSS,P,IER)
1670     PRINT 100
1680 100   FORMAT(////,7X,'OUTPUT TABLE OF QSS VERSUS US',//,2X,
1690     &'I',4X,'US',5X,'INT QSS',4X,'QSS/EV',4X,'V(THEOR)',4X,'C',
1700     &6X,'VX',6X,'QC',/,1X,'***',2X,'****',4X,'*****',3X,'*****
1710     *',
1710     &63X,'*****',3X,'***',4X,'****',4X,'*****')
1720     DU = 0.025
1730     V(P) = 0.0
1740     DO 31 I = 2,P
1750       J = P + 1 - I
1760 31   V(J) = DU*(DS(J) + DS(J+1)) + V(J+1)
1770     DO 105 I=1,P
1775 C REFERENCE ENERGY VALUES TO MID GAP
1780     UST(I) = UST(I) - E
1790     L2 = P + 1 - I
1800     V(I) = V(I) + Q(I)
1810     CX(I) = CAP(L2)

```

```

1820      VX(I) = WX(L2)
1830 105  PRINT 110,I,UST(I),Q(I),DS(I),VT(I),CX(I),VX(I),V(I)
1840 110  FORMAT(I3,F7.3,1P2E11.3,OP1F11.3,OP1F7.3,F8.3,1P1E10.3)
1845 C CALCULATE CONSTANT PART OF QSS
1850      E = 0
1860      S = 0.0
1870      DO 37 I = 5,P
1880          J = P + 4 - I
1890          E = E + V(J)*V(J)
1900 37   S = S + V(J)
1910      EE = P - 5
1920      SS = P - 4
1930      S = S/SS
1940      E = SQRT((E-SS*S*S)/EE)
1950      PRINT 101,S,E
1960 101  FORMAT(//,12X,'AVERAGE CONST QSS =',1P1E11.3,' +/-',
1970      &E11.3,/)
1980      DV = 1.6023E-19*S/CO
1990      PRINT 102, DV
2000 102  FORMAT(12X,'THE AVERAGE OFFSET VOLTAGE IS THEN',F7.2,/)
2010 999  END
END OF FILE

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