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METAL-NITRIDE-OXIDE-SEMICONDUCTOR (MNOS) RADIATION CHARACTERIZA--ETC(U)
JUL 79 R W TALLON

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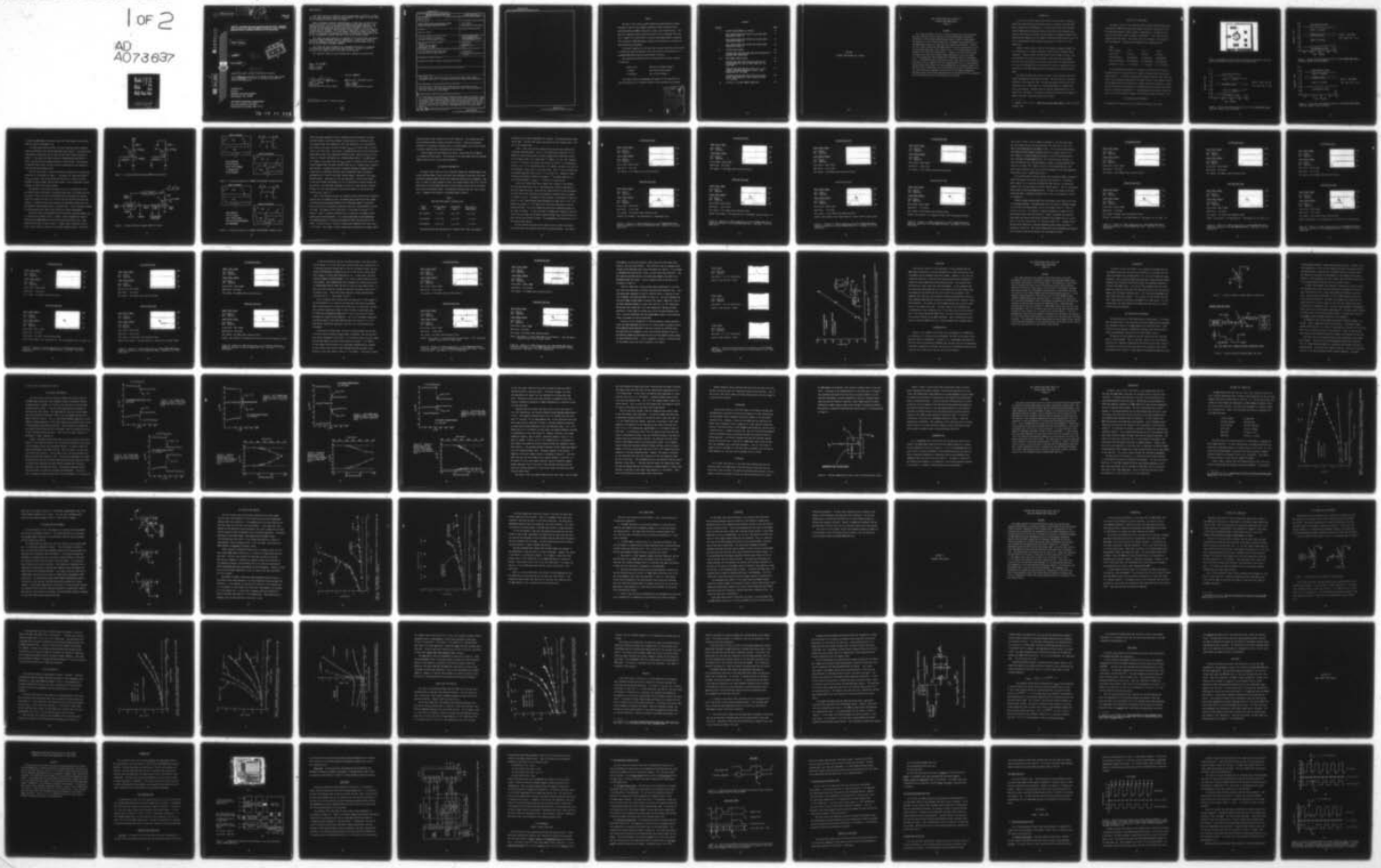

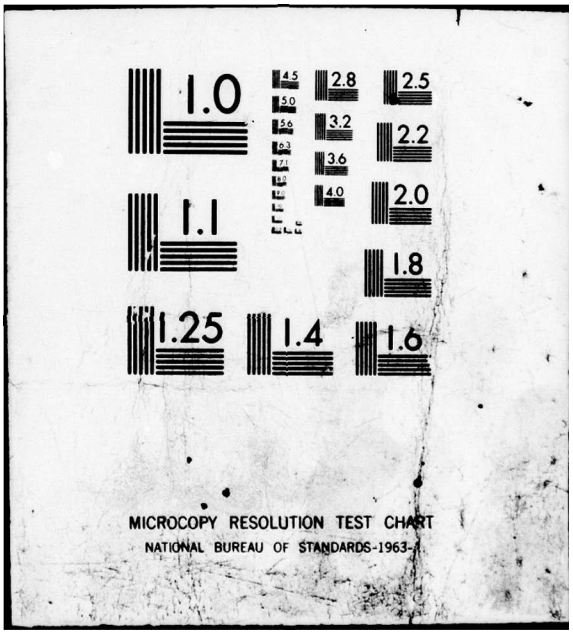
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(10) Roger W. Tallon

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Director
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Washington, DC 20305

AIR FORCE WEAPONS LABORATORY
Air Force Systems Command
Kirtland Air Force Base, NM 87117

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This final report was prepared by the Air Force Weapons Laboratory, Kirtland Air Force Base, New Mexico, under Job Order WDNE2207. Mr. Roger W. Tallon (ELP) was the Laboratory Project Officer-in-Charge.

This report has been reviewed by the Information Office and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nations.

This technical report has been reviewed and is approved for publication.

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19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

MNCS transistors, PMOS transistors, MNOS memories, integrated circuits, radiation effects, radiation hardening, radiation tests, ionizing radiation, dose rate, total dose, test methods.

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

This report describes the Radiation Characterization studies performed at the Air Force Weapons Laboratory (AFWL) on Metal-Nitride-Oxide-Semiconductor (MNOS) transistors, arrays, and related PMOS devices during the period of March 1972 to September 1978. The work presented shows the radiation test data, testing techniques, and radiation hardening ideas which assisted AFWL in the development of a radiation hard, monolithic, PMOS/MNOS RAM array (the Sperry Rand SR2256).

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PREFACE

The work in this report presents Radiation Characterization studies performed at the Air Force Weapons Laboratory (AFWL) on Metal-Nitride-Oxide-Semiconductor (MNOS) transistors, arrays, and related devices. This work was conducted during the period of March 1972 to September 1978, and was in support of an AFWL effort to develop (with Sperry Rand) a radiation hard, monolithic, MNOS RAM memory suitable for applications in nuclear and space radiation environments.

The overall objective of this work was to obtain data which would assist in optimizing radiation hardness levels and electrical characteristics of prototype MNOS memory devices and peripheral circuitry.

Key personnel who worked on this In-house effort and their responsibilities are:

Roger Tallon	Radiation & Engineer Support
Al Krause	Test Fixturization Support
Al Hoffland	Test Facility Support

The author wishes to acknowledge the support of Paul Marraffino of Sperry Gyroscope for his technical advice in the radiation test program.

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SECTION I

DISCRETE MNOS MEMORY CELL STUDIES

HIGH IONIZING DOSE RATE EFFECTS ON DISCRETE MNOS TRANSISTORS (PHASE 1)

ABSTRACT

This report describes the first of three ionizing dose rate evaluations performed on three types of radiation resistant MNOS memory transistors fabricated in 1971 by Sperry Rand Research Center, Sudbury, Massachusetts. The objective of this in-house effort was to determine the susceptibility of the MNOS memory devices to a high dose rate radiation environment. Results from this effort showed that the MNOS devices can survive and operate in such an environment [dose rate levels greater than 1×10^{12} Rad(Si)/sec] with no changes in the electrical specifications. However, the results also showed that there was a dose rate related disturb mechanism at dose rates above 1.4×10^{11} Rad(Si)/sec which degraded the information stored in the memory cells. This mechanism was not observed in other lower dose rate environments. Data from the tests suggested that this phenomenon was due to a high negative voltage being created across the high impedance gate to substrate junction of the test device, generating a false Write operation during the radiation burst. This false Write was suspected to be the cause of the memory degradations. The exact cause of this disturb mechanism was not determined in this evaluation. The clarification was left for another phase of testing.

INTRODUCTION

In 1971, while under contract with the Air Force Avionics Laboratory, Sperry Rand fabricated and tested three types of radiation resistant MNOS memory transistors (See Reference 1). Results from these tests indicated that the MNOS memory transistors (within the limits of the radiations employed), would survive, maintain a stored memory, and operate properly after absorbing Co-60 gammas up to 10^6 Rad(Si), absorbing 14 MeV neutrons up to 10^{15} n/cm^2, and absorbing LINAC electrons up to dose rate levels of 7×10^9 Rad(Si)/sec.

Because of these results, the Air Force Weapons Laboratory (AFWL) saw this technology as a possible competitor in the field of hardened memory components. However, before this possibility could become a reality, this new technology first had to be evaluated in high dose rate environments. Previous tests were limited to dose rate levels below 10^{10} Rad(Si)/second. As a result, AFWL embarked on an in-house test effort to determine the susceptibility of the MNOS memory device to high dose rate radiation environments.

This paper presents the first of a series of the high dose rate evaluations performed on these devices at AFWL. The first series of tests was conducted in the spring of 1972. The test environment used in this first evaluation was a 2 MeV E-beam (in a vacuum) generated by a Febetron 705 flash X-ray machine. The dose rates of interest ranged from 10^{11} to 10^{12} Rad(Si)/sec. and beyond. The devices evaluated were from the same group of memory transistors evaluated above by Sperry Rand.

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1. Wegener, H.A.R., et al. Radiation Resistant MNOS Memories, AFAL-TR-71-342, December 1972.

THE MNOS TEST TRANSISTORS

The devices tested in this evaluation were discrete Metal-Nitride-Oxide Semiconductor (MNOS) Non-stepped Gate Memory Transistors fabricated in 1971 at Sperry Rand Research Center, Sudbury, Massachusetts. The devices were from the same groups tested by Sperry in Reference 1. The transistors were grouped into three types. These types were "Fast Forward", "Slow Forward", and "Slow Reverse". Structures and properties are summarized below.

Type			
Write Voltage	$\pm$ 30 V	$\pm$ 30 V	$\pm$ 30 V
Write Time	100 μsec	100 msec	100 msec
Oxide Thickness	15 Angstroms	17 Angstroms	36 Angstroms
Nitride Thickness	622 Angstroms	661 Angstroms	826 Angstroms
Conductivity (Jn)	$3 \times 10^{-4} A/cm^2$	$2 \times 10^{-9} A/cm^2$	$5.3 \times 10^{-3} A/cm^2$

In the Forward Write transistor, a memory was written into the cell by the application of a large positive or negative voltage across the gate/substrate junction. A positive voltage wrote the device into the "High Conduction State", and a negative voltage wrote the device into the "Low Conduction State". For the Reverse device, the writing of a memory was just the opposite. A qualitative discussion of the physics of a Forward Write and a Reverse Write MNOS device is presented in Appendix "A". A photomicrograph and typical "Retention Plots" for the three types of memory cells tested are shown in Figures 1 to 4.

TEST OBJECTIVES AND APPROACH

The objectives of these tests were to determine the dose rate levels

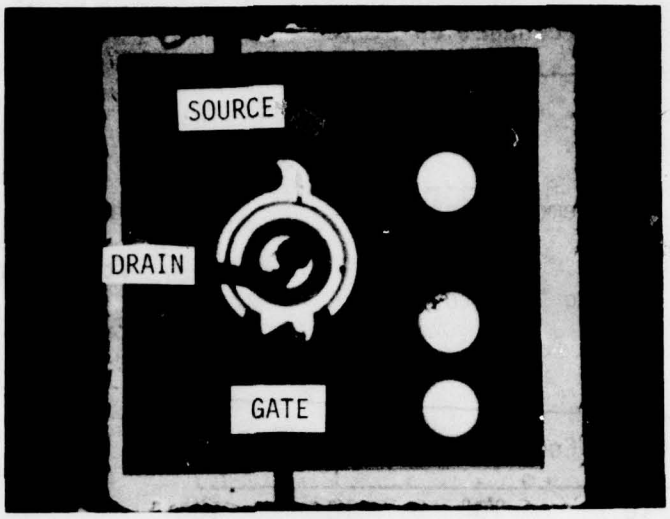


Figure 1. Photograph of the Typical Fast Forward, Slow Forward, and Slow Reverse MNOS Memory Transistor tested in this evaluation.

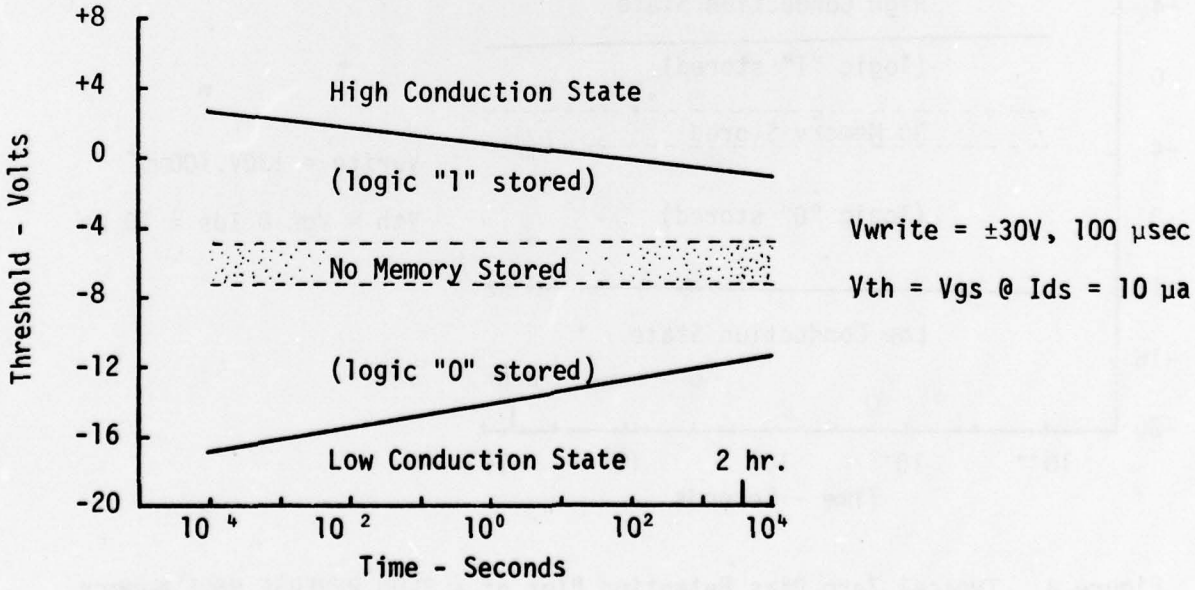


Figure 2. Typical Zero Bias Retention Plot of a FAST FORWARD MNOS Memory Transistor tested in this evaluation.

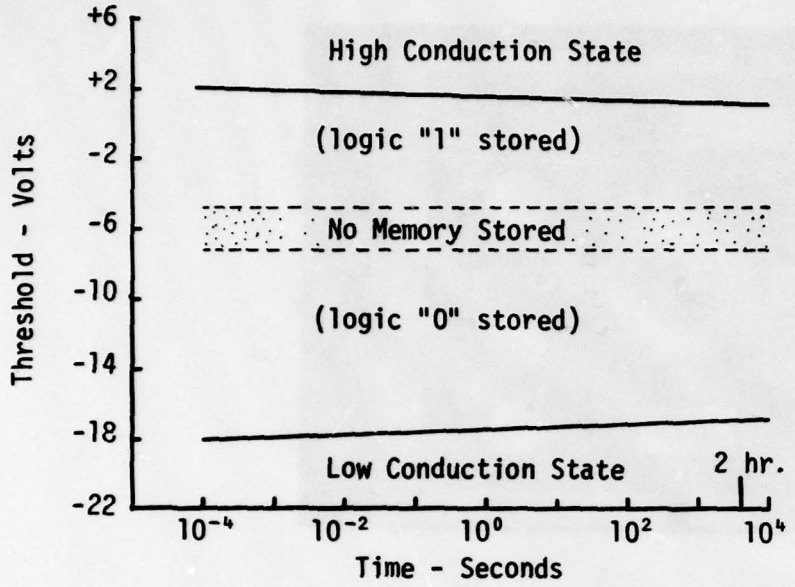


Figure 3. Typical Zero Bias Retention Plot of a SLOW FORWARD MNOS Memory Transistor tested in this evaluation.

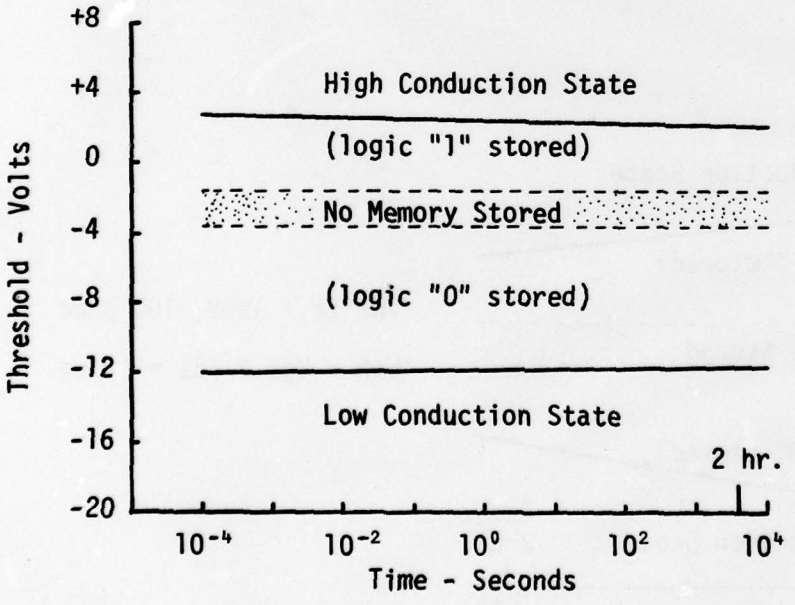


Figure 4. Typical Zero Bias Retention Plot of a SLOW REVERSE MNOS Memory Transistor tested in this evaluation.

at which the MNOS memory transistors could lose their memory, and to determine the cause of the memory loss.

To achieve these two objectives, the test transistors were evaluated under two different Drain Voltage conditions (See Figure 5). Both conditions represented as operating state in which the Gate had a high resistance to ground. In one case, the Drain Voltage was removed during the radiation burst, and the Drain was grounded through a 10 KΩ resistor. This was done to determine what effect (if any) the Drain Voltage had on the response of device during the radiation burst.

The test setup used to record the radiation responses for the above two conditions is illustrated in Figure 6. Included is an "Exerciser Control", a "V_{drain} Control", and three monitoring test points to record the Drain Voltage, the Gate Voltage, and the Gate Current. Also included were various triggers to control the timing sequence.

The function of the Exerciser Control was to: (1) provide the "Write" and "Read" pulses to the Gate of the device under test, (2) provide the trigger pulse to "fire" the flash x-ray machine, and (3) provide the required signal for turning "on" and "off" the Drain Voltage during the desired time interval. A double-current probe technique was employed to measure the sudden changes in Gate Current during a radiation burst. Such a procedure allowed for the substraction of cable noises during low current measurements.

Using this setup, the procedure devised to measure a possible memory loss is illustrated in Figures 7 and 8. Figure 7 shows a hypothetical case of a Forward Writing MNOS memory transistor that has been written with a large positive Write pulse to store a Logic "1" memory state, suffering a loss or shift in that state as a result of a transient radiation burst. Picture "A"

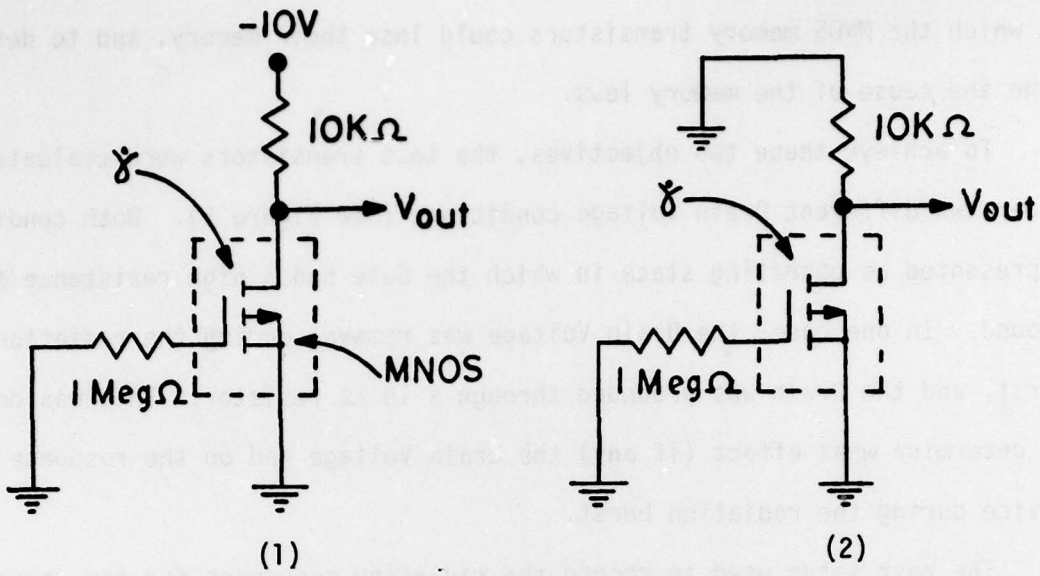


Figure 5. Transient Radiation Response MNOS Test Conditions.

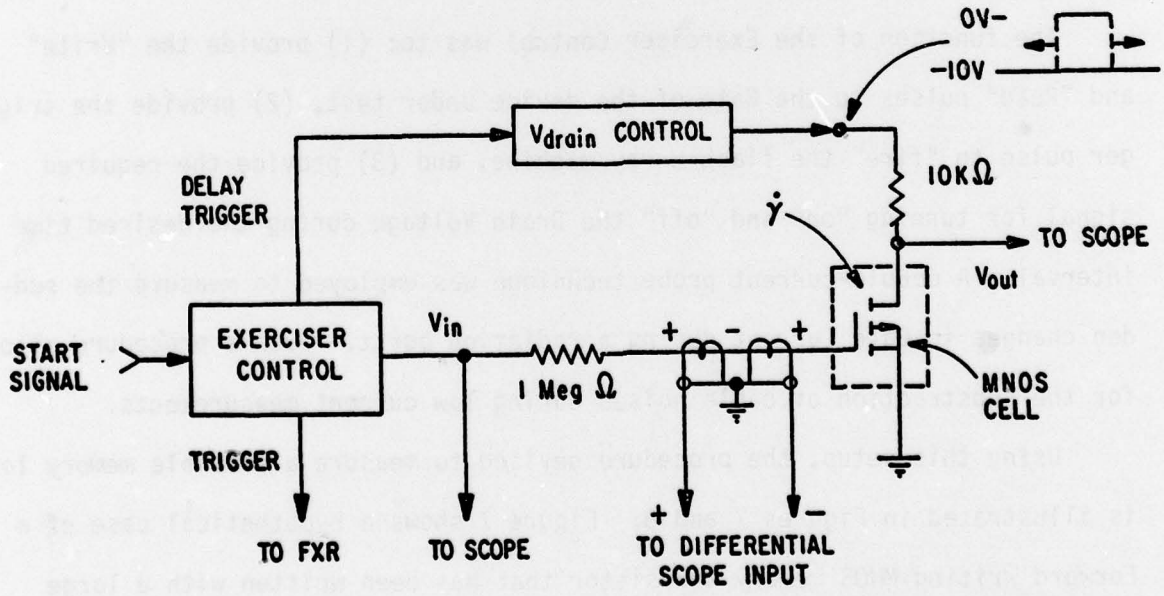


Figure 6. Transient Radiation Response MNOS Test Setup.

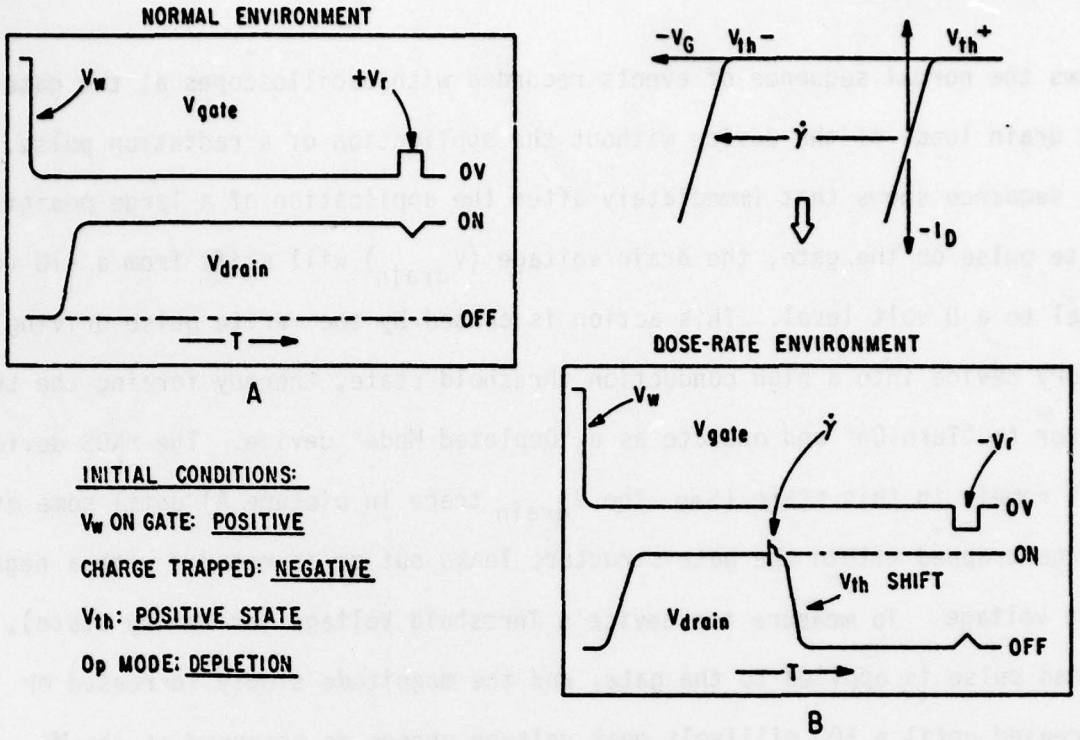


Figure 7. Illustrated Response of FORWARD SHIFTING MNOS P-Channel Device.

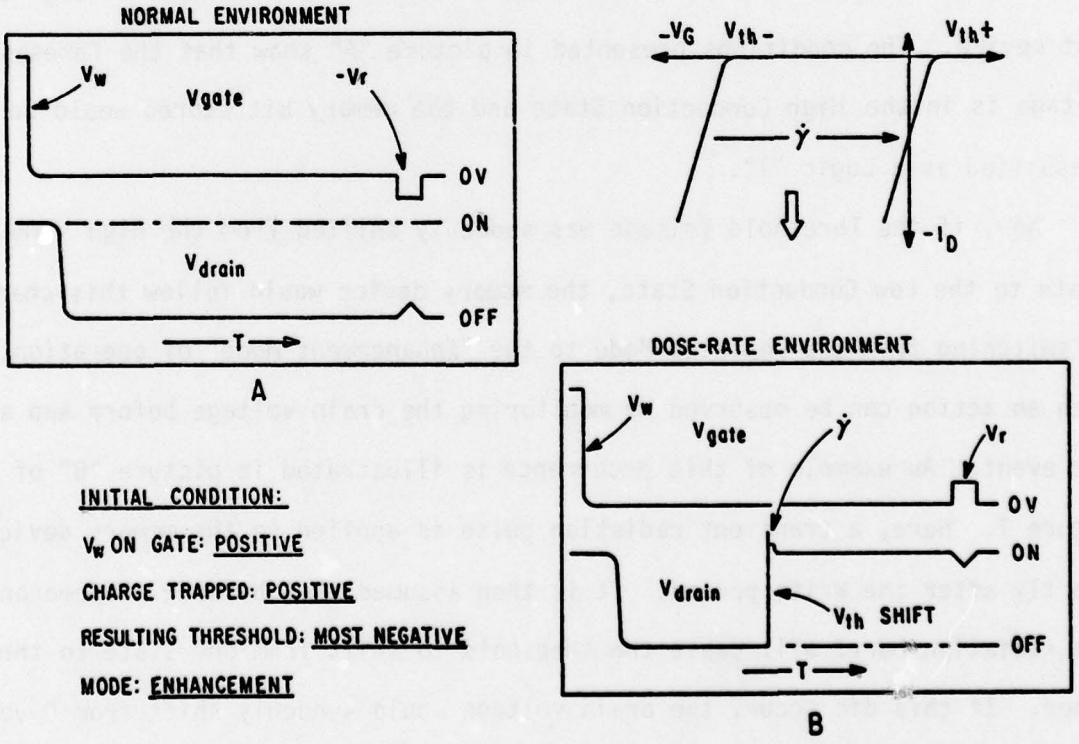


Figure 8. Illustrated Response of REVERSE SHIFTING MNOS P-Channel Device.

shows the normal sequence of events recorded with oscilloscopes at the gate and drain leads of the device without the application of a radiation pulse. The sequence shows that immediately after the application of a large positive Write pulse on the gate, the drain voltage (V_{drain}) will shift from a -10 volt level to a 0 volt level. This action is caused by the +Write pulse driving the memory device into a high conduction threshold state, thereby forcing the transistor to "Turn-On" and operate as a "Depleted Mode" device. The MNOS device will remain in this state (See the V_{drain} trace in picture A) until some of the charge trapped within the gate structure leaks out or is removed with a negative gate voltage. To measure the device's Threshold Voltage (or memory state), a Read pulse is applied to the gate, and the magnitude slowly increased or decreased until a 100 millivolt peak voltage change is observed at the V_{drain} measuring point. Note that for this test procedure, a 100 mV pulse change in the drain voltage corresponds to 10 μa of source-drain current through the test device. The conditions presented in picture "A" show that the Threshold Voltage is in the High Conduction State and the memory bit stored would be classified as a Logic "1".

Now, if the Threshold Voltage was suddenly shifted from the High Conduction State to the Low Conduction State, the memory device would follow this change by switching from the Depleted Mode to the "Enhancement Mode" of operation. Such an action can be observed by monitoring the drain voltage before and after the event. An example of this occurrence is illustrated in picture "B" of Figure 7. Here, a transient radiation pulse is applied to the memory device shortly after the Write period. It is then assumed that by some phenomenon the radiation burst will cause the threshold to shift from one state to the other. If this did occur, the drain voltage would suddenly shift from 0 volts to -10 volts. This change in drain voltage would be caused by the memory device

switching from an "ON" condition to an "OFF" condition. This sudden switching can be monitored before, during, and after the event. Using this measuring technique for the actual radiation tests, a possible memory loss or shift resulting from a high dose rate irradiation can be recorded.

Figure 8 shows the same sequences of events, except that now the memory is a Reverse Shifting device. The criterion is the same except that the recorded memory shifts will be in the reverse direction.

TEST RESULTS AND ANALYSIS

The overall test results of this evaluation showed that the MNOS memory transistors suffered memory losses and upsets when subjected to high dose rate radiation while operating under the two test conditions outlined in the Approach. However, in order for these changes to occur, the Forward devices had to be initially operating in the High Conduction State, and the Reverse devices had to be operating in the Low Conduction State. No upsets were recorded under the reverse situation. A summary of the results is presented below in Table 1.

TABLE 1.

HIGH DOSE RATE RESULTS IN RAD(Si)/SEC

Device Type	Partial Memory Loss	Total Memory Loss	Total Shift in Logic State
Fast Forward	1.4×10^{11}	5.0×10^{11}	9.0×10^{11}
Slow Forward	5.1×10^{11}	9.0×10^{11}	1.2×10^{12}
Slow Reverse	9.0×10^{11}	1.2×10^{12}	1.2×10^{12}

The above results were obtained with a Febetron 705 flash x-ray machine

operating in the 2 MeV E-beam Mode (in a vacuun). The radiation pulse width was 50 nsec. The dose rate levels used during the tests ranged from 1×10^{11} to 2×10^{12} Rad(Si)/sec.

Table 1 shows that the Fast Forward device was the most sensitive to transient radiation upsets. At 1.4×10^{11} Rad(Si)/sec, which was 7×10^{3} Rad(Si) of total dose per shot, the Fast Forward device suffered a partial loss of approx. 40% in its stored Logic "1" memory. At 5.0×10^{11} Rad(Si)/sec [2.5×10^{4} Rad(Si) per shot], the device loss 100% of its stored memory. Finally, at 9.0×10^{11} Rad(Si)/sec [4.5×10^{4} Rad(Si) per shot], the Fast Forward suffered a total shift in its logic state. That is, the pre-stored memory changed completely from a Logic "1" to a Logic "0". Samples of these finding are presented in Figures 9 through 11. The sample shown are for Test Condition Number 1 (V_{drain} = - 10 Volts during the burst).

It was also stated above that a memory loss or upset in the Forward Write devices would only occur if the devices were initially operating in the High Conduction State. Operating the Forward devices in the Low Conduction State during the radiation burst produced no recorded losses in memory or changes in state. An example of this discovery is presented in Figure 12. Shown is a Fast Forward memory being subjected to a dose rate of 1.24×10^{12} Rad(Si)/sec [approx. 6×10^{4} Rad(Si) per shot] while operating in the Low Conduction State. The result showed that there was no degrading effect on the Logic "0" memory. In fact, the Logic "0" memory was enhanced by the radiation burst [as shown by the Gate Threshold Voltage (V_{th}) being shifted further into the Low Conduction State]. This phenomenon was observed for all of the Forward Write devices.

The Slow Forward transistors were shown to have a greater resistance to the high dose rate radiation than the Fast Forward devices. This result

Pre-Radiation Data

Upper Trace: Vgate

Vert: 5V/div
Hor: 100μs/div

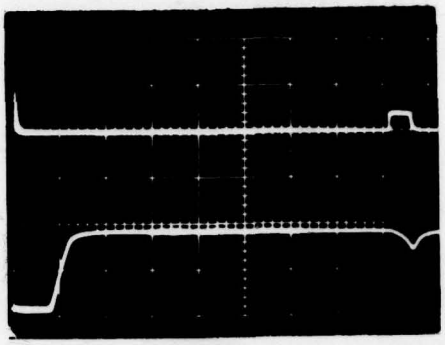
Lower Trace: Vdrain

Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100μs

Read Pulse: +2V @ 50μs

Vth: approx. +1.5V (860μs after the Write Pulse)



Radiation Shot Data

Upper Trace: Vgate

Vert: 5V/div
Hor: 100μs/div

Lower Trace: Vdrain

Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100μs

Read Pulse: -2.5V @ 50μs

Vth: approx. -2.5V (470μs after Radiation Shot)

Effects: Vth shifted ≃ -4V (equivalent to ≃ 40% memory loss)

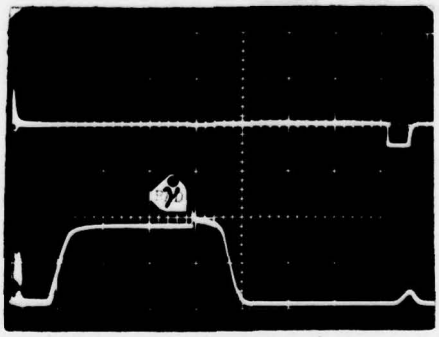


Figure 9. Effects of a 2MeV E-beam Pulse on a FAST FORWARD MNOS Memory Transistor operating in the HIGH CONDUCTION STATE. Dose Rate = 1.4×10^{11} Rad(Si)/sec.

Pre-Radiation Data

Upper Trace: Vgate

Vert: 5V/div
Hor: 100μs/div

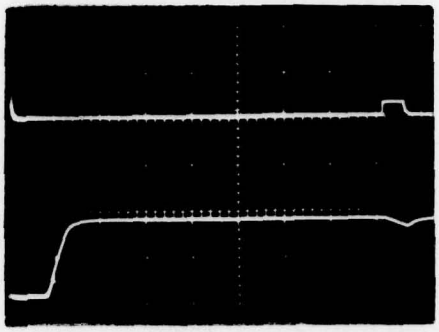
Lower Trace: Vdrain

Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100μs

Read Pulse: +3V @ 50μs

Vth: approx. +2.5V (820μs after the Write Pulse)



Radiation Shot Data

Upper Trace: Vgate

Vert: 5V/div
Hor: 100μs/div

Lower Trace: Vdrain

Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100μs

Read Pulse: -6.5V @ 50μs

Vth: approx. -6.5V (470μs after Radiation Shot)

Effect: Vth shifted ≃ -9V (equivalent to ≃ 100% memory loss for logic "1")

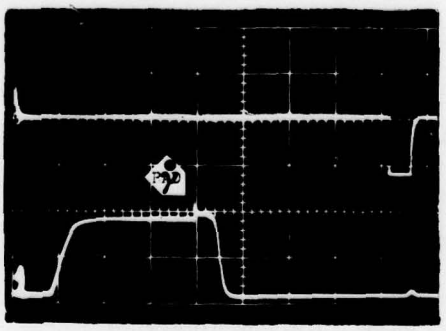
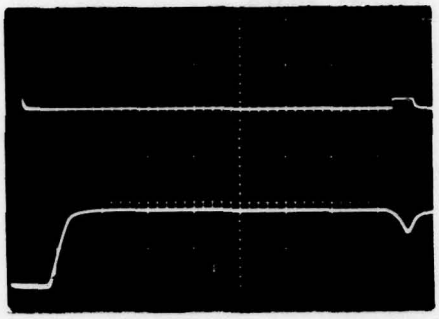


Figure 10. Effects of a 2MeV E-beam Pulse on a FAST FORWARD MNOS Memory Transistor operating in the HIGH CONDUCTION STATE. Dose Rate = 5.0×10^{11} Rad(Si)/sec.

Pre-Radiation Data



Upper Trace: Vgate

Vert: 10V/div
Hor: 100μs/div

Lower Trace: Vdrain

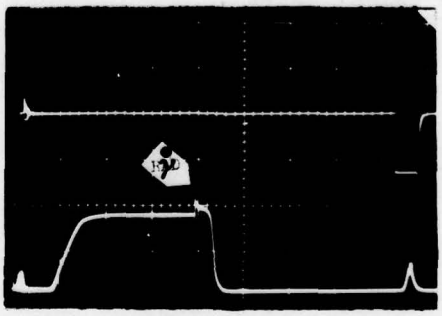
Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100μs

Read Pulse: +2.5V @ 50μs

Vth: approx. +2.0V (860μs after the Write Pulse)

Radiation Shot Data



Upper Trace: Vgate

Vert: 10V/div
Hor: 100μs/div

Lower Trace: Vdrain

Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100μs

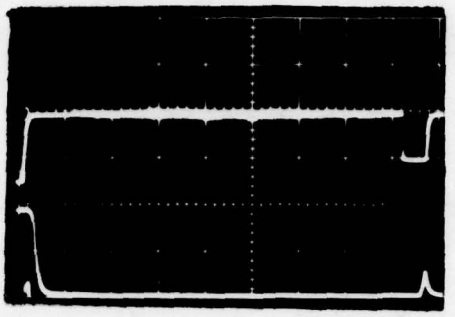
Read Pulse: -13V @ 50μs

Vth: approx. -12.5V (470μs after Radiation Shot)

Effects: Vth shifted ≃-14.5V (equivalent to a total shift in logic state).

Figure 11. Effects of a 2MeV E-beam Pulse on a FAST FORWARD MNOS Memory Transistor operating in the HIGH CONDUCTION STATE. Dose Rate = 9.0×10^{11} Rad(Si)/sec.

Pre-Radiation Data



Upper Trace: Vgate

Vert: 20V/div
Hor: 100μs/div

Lower Trace: Vdrain

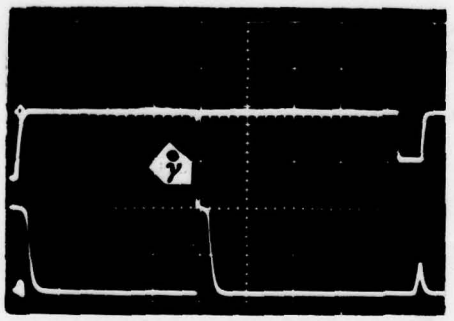
Vert: 5V/div
Hor: 100μs/div

Write Pulse: -30V @ 100μs

Read Pulse: -20V @ 50μs

Vth: approx. -19.5V (820μs after the Write Pulse)

Radiation Shot Data



Upper Trace: Vgate

Vert: 20V/div
Hor: 100μs/div

Lower Trace: Vdrain

Vert: 5V/div
Hor: 100μs/div

Write Pulse: -30V @ 100μs

Read Pulse: -21V @ 50μs

Vth: approx. -20.5V (470μs after Radiation Shot)

Effects: Vth shifted ≃ -1V (enhanced further into Low Conduction State).

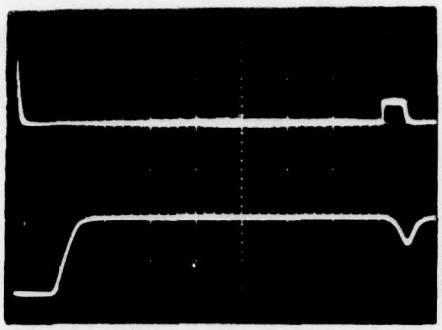
Figure 12. Effects of a 2MeV E-beam Pulse on a FAST FORWARD MNOS Memory Transistor operating in the LOW CONDUCTION STATE. Dose Rate = 1.24×10^{12} Rad(Si)/sec.

can be seen in Table 1 and in Figure 13 through 15. The data shows that the Slow Forward devices can withstand dose rate levels up to 5.0×10^{11} Rad(Si)/sec before any loss in memory occurs. This level was approxinately 18K Rad(Si) per shot higher than that required to produce losses in the Fast Forward. To totally wipe out a memory in the Slow Forward devices, a dose rate level of approximately 9.0×10^{11} Rad(Si)/sec was required. A dose rate level of 1.2×10^{12} was needed to produce a complete memory shift (logic "1" to logic "0"). Again, as with the Fast Forward devices, the Slow Forward transistors had to be initially operating in the High Conduction State before losses in memory would occur.

Of the three types of devices tested, the Slow Reverse Memory transistors showed the greatest resistance to high dose rate radiation. In addition, when a memory loss or upset was recorded for these devices, the operating condition was just the opposite from the Forward devices. That is, the Reverse devices were in the Low Conduction State. No upsets were noted in the High Conduction State. Highlights showing these results are presented in Figures 16 through 18.

Figure 16 shows the dose rate level where memory losses were first noted in the Reverse devices. The figure shows that the device's Threshold Voltage (V_{th}) shifted from approximately -10V to -6V (a delta shift of $\simeq$ +4V) as a result of the shot. This amount of change corresponds to a memory loss of approximately 50% to 60% (See Figure 4). Figure 17 presents the dose rate level where the Reverse type devices suffered a total memory loss or a total shift in its logic state (logic "0" shifting to logic "1"). A sample of the Reverse device operating in the High Conduction State during the burst is presented in Figure 18. The results showed that the stored memory was enhanced by the radiation and driven further into the conduction state.

Pre-Radiation Data



Upper Trace: Vgate

Vert: 5V/div
Hor: 100μs/div

Lower Trace: Vdrain

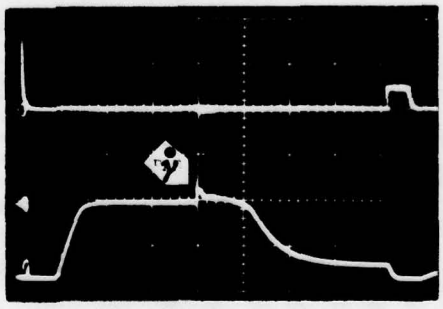
Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100ms

Read Pulse: +3V @ 50μs

Vth: approx. +2.5V (820μs after the Write Pulse)

Radiation Shot Data



Upper Trace: Vgate

Vert: 5V/div
Hor: 100μs/div

Lower Trace: Vdrain

Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100ms

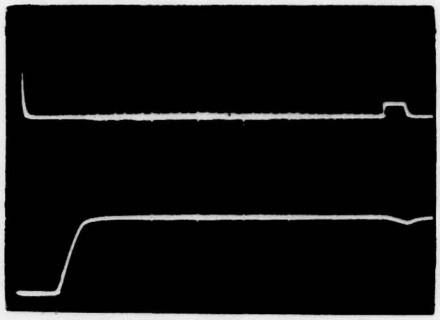
Read Pulse: +3V @ 50μs

Vth: approx. 0V(430μs after the Radiation Shot)

Effects: Vth shifted ≃ -2.5V (equivalent to ≃ 25% memory loss for logic "1")

Figure 13. Effects of a 2MeV E-beam Pulse on a SLOW FORWARD MNOS Memory Transistor operating in the HIGH CONDUCTION STATE. Dose Rate = 5.0×10^{11} Rad(Si)/sec.

Pre-Radiation Data



Upper Trace: Vgate

Vert: 5V/div
Hor: 100μs/div

Lower Trace: Vdrain

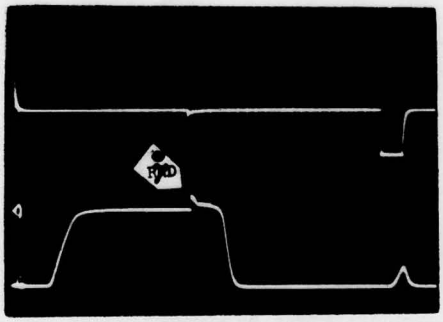
Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100ms

Read Pulse: +2V @ 50μs

Vth: approx. +2V (860μs after the Write Pulse)

Radiation Shot Data



Upper Trace: Vgate

Vert: 5V/div
Hor: 100μs/div

Lower Trace: Vdrain

Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100ms

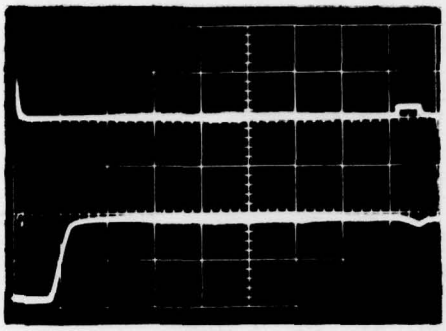
Read Pulse: -5V @ 50μs

Vth: approx. -5V (470μs after Radiation Shot)

Effect: Vth shifted ≃ -7V (equivalent to ≃ 100% memory loss for logic "1").

Figure 14. Effects of a 2MeV E-beam Pulse on a SLOW FORWARD MNOS Memory Transistor operating in the HIGH CONDUCTION STATE. Dose Rate = 9.0×10^{11} Rad(Si)/sec.

Pre-Radiation Data



Upper Trace: Vgate

Vert: 10V/div
Hor: 100μs/div

Lower Trace: Vdrain

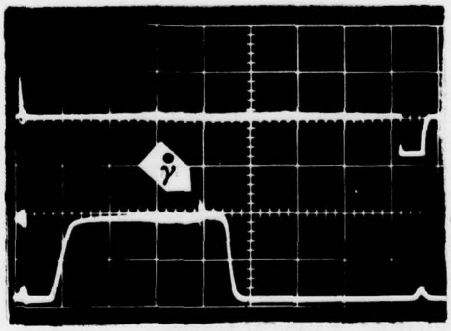
Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100ms

Read Pulse: +2.5V @ 50μs

Vth: approx. +2.5V (820μs after the Write Pulse)

Radiation Shot Data



Upper Trace: Vgate

Vert: 10V/div
Hor: 100μs/div

Lower Trace: Vdrain

Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100ms

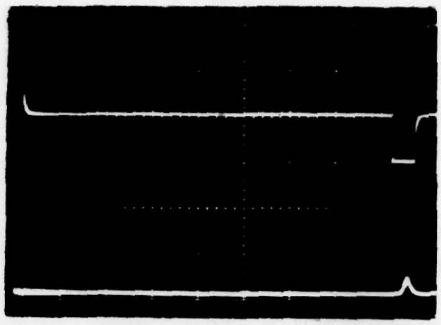
Read Pulse: -8.5V @ 50μs

Vth: approx. -8.5V (470μs after Radiation Shot)

Effect: Vth shifted ≃ -11V (equivalent to a total shift in logic state).

Figure 15. Effects of a 2MeV E-beam Pulse on a SLOW FORWARD MNOS Memory Transistor operating in the HIGH CONDUCTION STATE. Dose Rate = 1.2×10^{12} Rad(Si)/sec.

Pre-Radiation Data



Upper Trace: Vgate

Vert: 10V/div
Hor: 100μs/div

Lower Trace: Vdrain

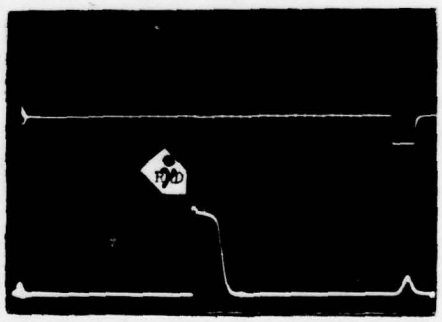
Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100ms

Read Pulse: -10V @ 50μs

Vth: approx. -10V (860μs after Write Pulse)

Radiation Shot Data



Upper Trace: Vgate

Vert: 10V/div
Hor: 100μs/div

Lower Trace: Vdrain

Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100ms

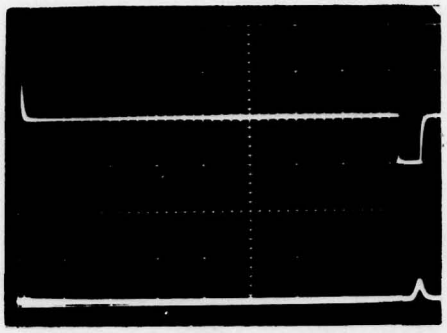
Read Pulse: -6V @ 50μs

Vth: approx. -6V (470μs after Radiation Shot)

Effect: Vth shifted ≃ +4V (equivalent to ≃ 50% to 60% memory loss for logic "0").

Figure 16. Effects of a 2MeV E-beam Pulse on a SLOW REVERSE MNOS Memory Transistor operating in the LOW CONDUCTION STATE. Dose Rate = 9.0×10^{11} Rad(Si)/sec.

Pre-Radiation Data



Upper Trace: Vgate

Vert: 10V/div
Hor: 100μs/div

Lower Trace: Vdrain

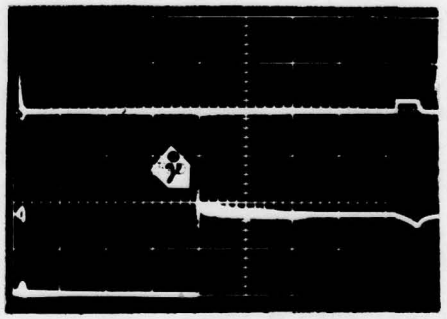
Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100ms

Read Pulse: -10V @ 50μs

Vth: approx. -10V (820μs after the Write Pulse)

Radiation Shot Data



Upper Trace: Vgate

Vert: 10V/div
Hor: 100μs/div

Lower Trace: Vdrain

Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100ms

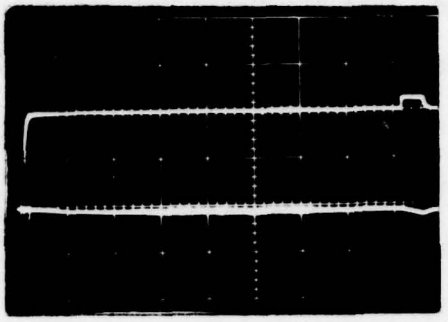
Read Pulse: +3.0V @ 50μs

Vth: approx. +3.0V (470μs after Radiation Shot)

Effect: Vth shifted ≃ +13V (equivalent to a total shift in logic state).

Figure 17. Effects of a 2MeV E-beam Pulse on a SLOW REVERSE MNOS Memory Transistor operating in the LOW CONDUCTION STATE. Dose Rate = 1.2×10^{12} Rad(Si)/sec.

Pre-Radiation Data



Upper Trace: Vgate

Vert: 10V/div
Hor: 100μs/div

Lower Trace: Vdrain

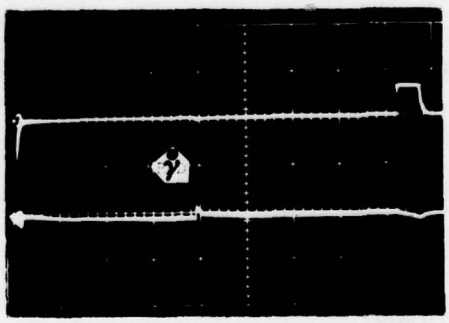
Vert: 5V/div
Hor: 100μs/div

Write Pulse: -30V @ 100ms

Read Pulse: +3V @ 50μs

Vth: approx. +3V (820μs after the Write Pulse)

Radiation Shot Data



Upper Trace: Vgate

Vert: 10V/div
Hor: 100μs/div

Lower Trace: Vdrain

Vert: 5V/div
Hor: 100μs/div

Write Pulse: -30V @ 100ms

Read Pulse @ +7V @ 50μs

Vth: approx. +7V (470μs after Radiation Shot)

Effect: Vth shifted ≃ +4V (enhanced further into the High Conduction State).

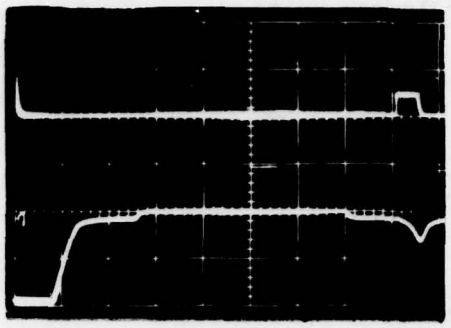
Figure 18. Effects of a 2MeV E-beam Pulse on a SLOW REVERSE MNOS Memory Transistor operating in the HIGH CONDUCTION STATE. Dose Rate = 1.2×10^{12} Rad(Si)/sec.

In the data presented thus far, the Drain Voltage on the device under test was equal to -10 volts during the radiation shot (Test Condition No. 1). To show that the Drain Voltage had no effect on the memory losses, two data samples are presented in Figures 19 and 20 to show the test results taken with a V_{drain} = 0 volts (Test Condition No. 2). In both cases, the Drain lead was clamped to ground through a 10 KΩ resistor shortly before the radiation period. This condition was held throughout the radiation period and for approximately 300 μs after the shot to allow for post stabilization. In both cases after the Drain Voltage was returned, the results show shifts in the memory states. These shifts were identical to those obtained under Test Condition No. 1. See Figures 15 and 17.

Other information worth noting from this phase was: (1) The changes in the stored memories as a result of the high dose rates were not permanent. With the application of a proper Write pulse after an irradiation, the memories could be electrically reset to their original pre-radiation state. (2) There was no permanent change noted in any of the electrical characteristics as a result of the radiation. (3) All of the memory transistors survived the tests. Even after absorbing dose rate levels of 1.2×10^{12} Rad(Si)/sec, the devices could still function as if they had never been irradiated.

In analyzing the above data, there was a paradox between the low dose rate Co-60 results obtained by Sperry Rand in Reference 1 and the high dose rate results presented in this report. In the Co-60 results, the data showed that the MNOS memory transistor could absorb well beyond 1×10^5 Rad(Si) of total gamma radiation before any noted memory degradation was recorded. In the high dose rate results, major degradations were recorded in the devices at total dose levels as low as 7×10^3 Rad(Si). Since both of these

Pre-Radiation Data



Upper Trace: Vgate

Vert: 5V/div
Hor: 100μs/div

Lower Trace: Vdrain

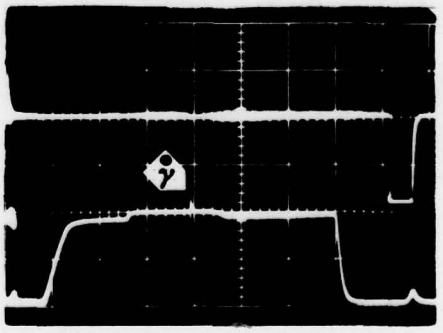
Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100ms

Read Pulse: +2.5V @ 50μs

Vth: approx. +2.5V (820μs after the Write Pulse)

Radiation Shot Data



Upper Trace: Vgate

Vert: 5V/div
Hor: 100μs/div

Lower Trace: Vdrain

Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100ms

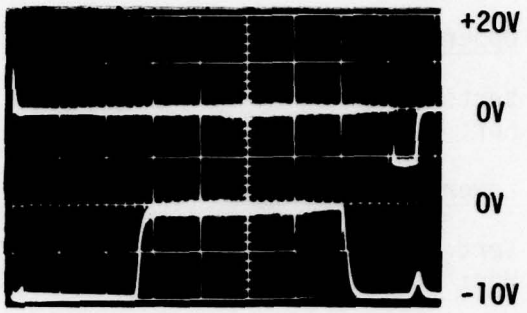
Read Pulse: -9.0V @ 50μs

Vth: approx. -9V (470μs after Radiation Shot)

Effect: Vth shifted ≃ 11.5V (same effect as with Vdrain = -10V, the device suffered a total shift in logic state).

Figure 19. Effects of a 2MeV E-beam Pulse on a SLOW FORWARD MNOS Memory Transistor operating in the HIGH CONDUCTION STATE and with Vdrain = 0 volts during the burst. Dose Rate = 1.2×10^{12} Rad(Si)/sec.

Pre-Radiation Data



Upper Trace: Vgate

Vert: 10V/div
Hor: 100μs/div

Lower Trace: Vdrain

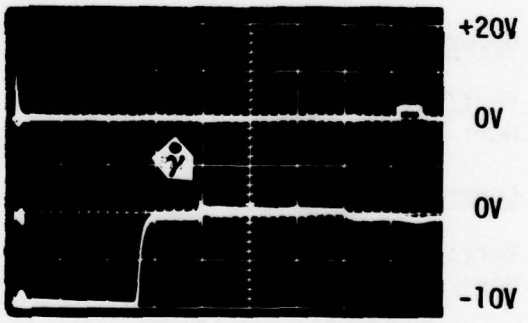
Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100ms

Read Pulse: -11.5V @ 50μs

Vth: approx. -11V (820μs after the Write Pulse)

Radiation Shot Data



Upper Trace: Vgate

Vert: 10V/div
Hor: 100μs/div

Lower Trace: Vdrain

Vert: 5V/div
Hor: 100μs/div

Write Pulse: +30V @ 100ms

Read Pulse: +3V @ 50μs

Vth: approx. +3V (470μs after Radiation Shot)

Effect: Vth shifted ≃ +14.5V (same effect as with Vdrain = -10V, the device suffered a total shift in logic state).

Figure 20. Effects of a 2MeV E-beam Pulse on a SLOW REVERSE MNOS Memory Transistor operating in the LOW CONDUCTION STATE and with Vdrain = 0V during the burst. Dose Rate = 1.2×10^{12} Rad(Si)/sec.

environments are ionizing radiation, there should have been some correlation in the total dose effects. Since there was none, an unknown effect related to the high dose rate E-beam environment was implied. In an attempt to determine the cause of this effect, current probes were installed in the Gate lead of each test device, and current measurements were made at predetermined dose rate levels. Typical responses taken on one device are presented in Figure 21.

Figure 21 shows that a large current pulse (proportional to the dose rate level) was generated in the Gate lead during the radiation shot. Plotting these peak responses in terms of electron flow as a function of dose rate produces the curve presented in Figure 22. The data presented show that up to 650μa of peak negative current (for approx. 100ns) will flow in the Gate lead when exposed to a dose rate level of 1.2×10^{12} Rad(Si)/sec. Noting that this current will also flow through the 1 MΩ Gate resistor, generating a large negative voltage pulse across the gate-substrate junction, a possible explanation for the sudden memory losses in the transient E-beam environment can now be formulated.

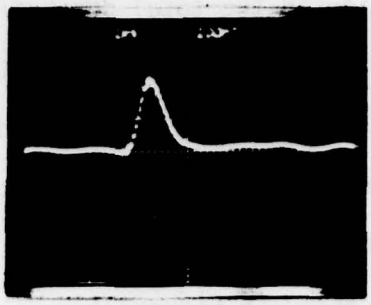
The basis of this explanation is that the negative voltage generated across the gate-substrate junction will be large enough to produce an equivalent negative Write operation on the device during the radiation burst. The result will be a tendency to shift the Threshold Voltage of the Forward devices toward the Low Conduction State and the Reverse devices toward the High Conduction State. If this assumption is correct, it would account for the memory losses and shifts recorded in this report.

Trace: Igate

Vert: 100μa/div
Hor: 100ns/div

Dose Rate = 1.3 x 10^{11} Rad(Si)/sec

Igate (+ Peak Current) = 220μa

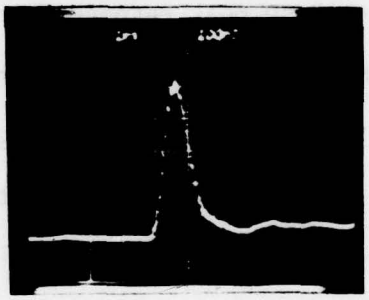


Trace: Igate

Vert: 100μa/div
Hor: 100ns/div

Dose Rate = 5.0 x 10^{11} Rad(Si)/sec

Igate (+ Peak Current) = 460μa



Trace: Igate

Vert: 100μa/div
Hor: 100na/div

Dose Rate = 1.3 x 10^{12} Rad(Si)/sec

Igate (+ Peak Current) = 680μa

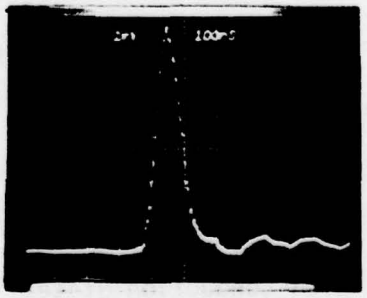


Figure 21. Transient Positive Gate Current Response on a FAST FORWARD MNOS Memory Transistor recorded during an Ionizing Radiation Burst (2MeV E-beam Mode).

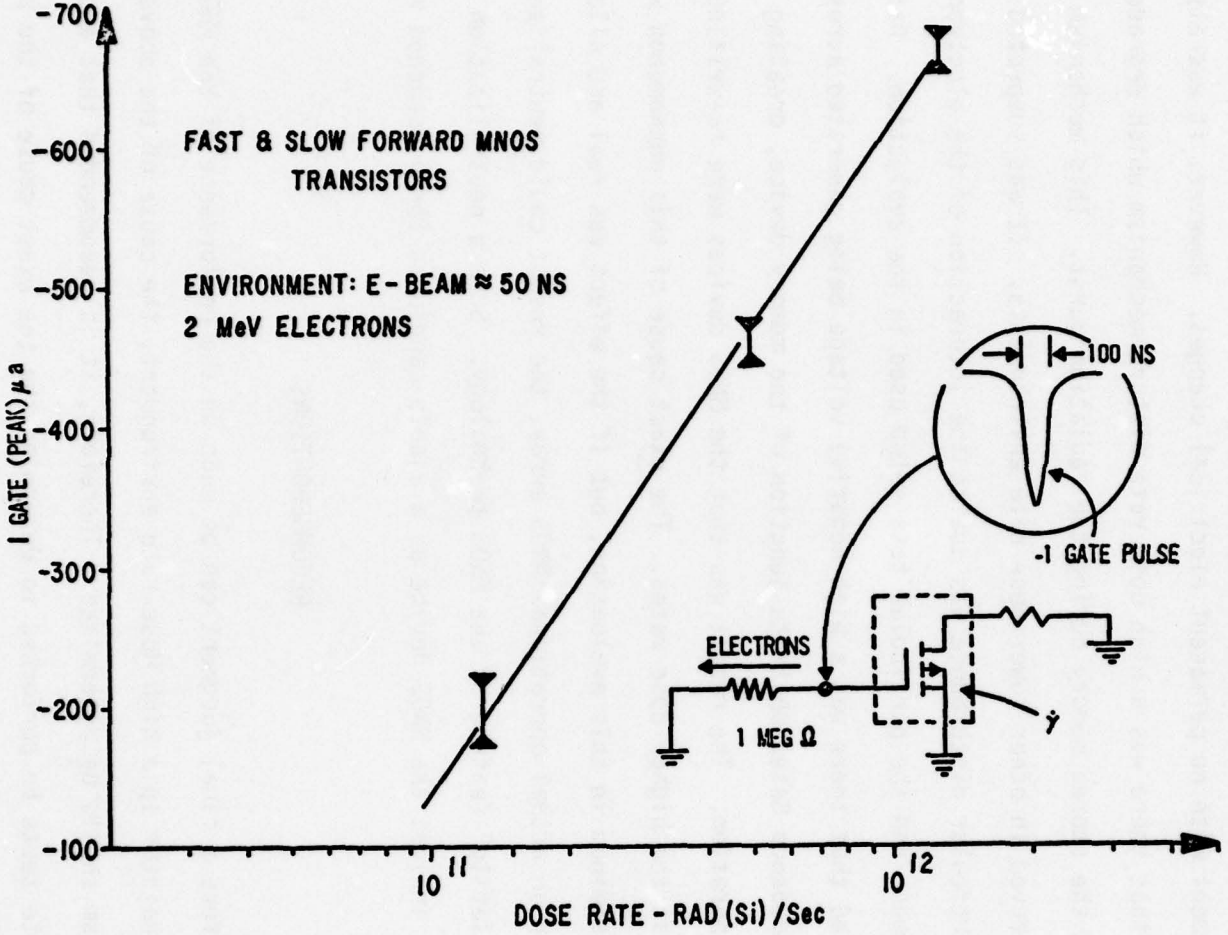


Figure 22. Transient Negative Peak Current Response in the Gate Circuit of the Forward and Reverse Write MNOS Memory Transistors as a function of a High Dose Rate 2 MeV Electron Environment.

DISCUSSION

From the test results in this evaluation, it was concluded that the MNOS memory transistor can survive and operate in a high ionizing dose rate environment with no permanent electrical changes. However, it was also concluded that there was a high dose rate disturb mechanism which degraded or changed the stored memory during the radiation burst. This mechanism was not observed in other lower dose rate environments. It was suspected that this particular disturbance was due to the interaction of the electron beam environment and the particular test setup used in the evaluation. Data suggested that there was a high negative voltage being generated across the high impedance Gate/Substrate junction of the memory device, creating a false Write operation. The result was that the MNOS devices were re-writing themselves at the higher dose rates. The exact cause of this phenomenon was not determined in this evaluation, but if the effect was real and allowed to occur in an actual operational MNOS array, the result could neutralize the "non-volatile" feature of the MNOS technology. Such a neutralization would greatly inhibit the MNOS device as a viable candidate for a hardened memory.

RECOMMENDATIONS

Before a final judgment can be made on the performance of the MNOS memory transistor in a high dose rate environment, the cause of the above disturb mechanism should be determined. Therefore, it is recommended that additional dose rate tests be performed to determine the the exact cause of the phenomenon, a possible circumvention technique, and the type of environments where the mechanism will most likely occur (See the next two test phases).

HIGH IONIZING DOSE RATE EFFECTS ON DISCRETE MNOS TRANSISTORS (PHASE 2)

ABSTRACT

This report describes the second of three ionizing dose rate tests performed on three types of radiation resistant (non-step gate) MNOS memory transistors fabricated in 1971 by Sperry Rand. The objectives of this effort were to determine the exact cause of the high dose rate disturb mechanism observed in the Phase 1 tests, and to find a possible circumvention technique which would prevent this disturbance from occurring in actual MNOS circuitry. The results of this effort showed that the disturb mechanism was due to a high negative voltage generating a false Write across the high impedance gate-substrate junction during the radiation burst. The results also showed that this false Write phenomenon could be eliminated by grounding the gate-substrate junctions of the test device during the radiation burst. Grounding these terminals during the burst resulted in a MNOS memory device that was only total dose dependent. That is, the memory losses due to the high dose radiation were the same as those measured in a low dose rate Co-60 environment. A possible compensation circuit that was devised to eliminate this false Write was composed of a PNP bidirectional diode operating in parallel with the memory gate resistance to ground. This technique, through photoconduction, would clamp the gate terminal to the same ground potential as the substrate during the radiation burst, thereby removing any possibility of a false Write charge buildup.

INTRODUCTION

In Phase 1 of this test effort, it was shown that the MNOS Non-step Gate Memory Transistor could survive and operate in a high dose rate radiation environment with no degradation in its electrical operating characteristics. But, it was also shown that there was a high dose rate disturb mechanism (not related to total dose effects) that degraded information stored in the memory cells. This initial data suggested that the disturbance was caused by a high dose rate induced Write pulse that re-wrote the memory cells during the radiation burst. This false Write phenomenon was never really verified in Phase 1. As a result, to help clarify the problem a second phase of testing was performed on the same devices. In this second phase, the same radiation environment was used, but with a different test setup and approach.

TEST OBJECTIVES AND APPROACH

The two objectives in this second phase of testing were: (1) to determine the exact cause of the high dose rate disturb mechanism which degraded the information stored in the MNOS memory cells during the Phase 1 tests, and (2) to find a possible circumvention technique which would prevent or reduce the phenomenon from occurring in furture MNOS circuitry.

To achieve the first objective, the test transistors were evaluated with all leads grounded. That is, the Gate, Source, Drain and Substrate leads were all clamped at ground during the radiation burst (Ref. Figure 1). The reason for using this setup was based on the assumption that the disturb mechanism was caused by a large negative voltage being generated across

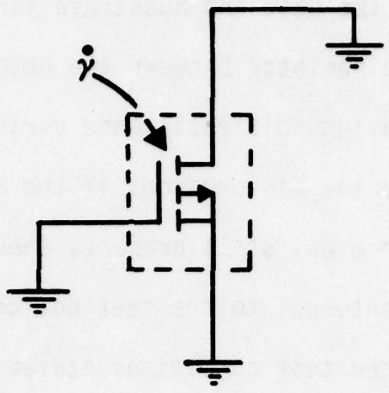
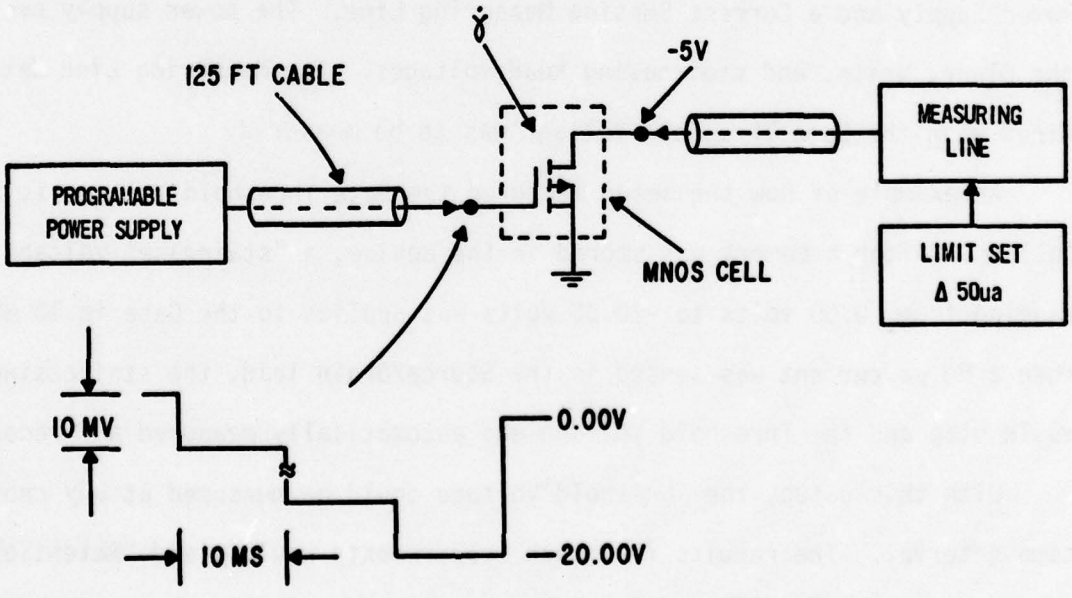


Figure 1. Transient Radiation Response MNOS Test Conditions.

FAIRCHILD 5000 TEST SETUP



NOTE: GATE, SOURCE, DRAIN, & SUBSTRATE ARE CLAMPED AT GROUND DURING $\dot{\gamma}$ BURST.

Figure 2. Transient Radiation Response MNOS Test Setup.

a high impedance between the Gate and Substrate junction. In Phase 1, this high impedance was a 1 MΩ resistor between the Gate of the device and the grounded Substrate. Removing this resistance during the radiation shot was expected to eliminate the disturbance, if the assumption was correct. However, if the disturbance was still present, then the effect would be due to an unknown mechanism internal to the test device itself.

To obtain the grounded test conditions stated above, and still perform the required Clear, Write, and Read functions on the memories (without removal from the test cell), a test setup different from Phase 1 had to be used. The new setup incorporated a Fairchild 5000C computerized control test system (See Figure 2). As shown, the automatic test system was connected directly to the test device (in the test cell) through 125 feet of "Kelvin-wired" transmission line. The basic system employed a Programmable Power Supply and a Current Sensing Measuring Line. The power supply provided the Clear, Write, and staircasing Read voltages. The Measuring Line determined <u>when</u> the Gate Threshold Voltage was to be measured.

An example of how the setup measured the Gate Threshold Voltage is as follows. After a memory was stored in the device, a "staircase" voltage ranging fromm 0.00 volts to -20.00 volts was applied to the Gate in 10 mV steps. When a 50 μa current was sensed in the Source/Drain lead, the staircasing would stop and the Threshold Voltage was automatically measured and recorded.

With this setup, the Threshold Voltage could be measured at any chosen time interval. The results from such measurements would yield "Retention Plot" of a Gate Threshold Window for a particular device before and after a radiation burst. From these plots, memory losses (as a result of a radiation) or shifts in the Gate Threshold Voltages could be measured. An example

of such a plot is presented in Figure 3.

TEST RESULTS AND ANALYSIS

The test results from this evaluation showed that when the leads of the MNOS memory transistors were clamped at ground, the devices suffered no memory losses or upsets as a result of the high dose rate disturb mechanism observed in Phase 1. The only losses measured were attributed to ionizing total dose effects. The importance of these two findings showed that the explanation formulated in Phase 1 for the sudden high dose rate memory losses was correct. That is, the disturb mechanism was due to a high negative voltage generating a false Write (during the radiation burst) across a high impedance gate-substrate junction. These findings also showed that the sudden charge buildup could be eliminated, simply by grounding the leads of the test device during the burst. Verification of these findings are presented in Figure 3 through 10.

Figures 3 through 6 present data taken on the Fast Forward transistors. Figures 7 and 8 show data taken on the Slow Forward transistors, and Figures 9 and 10 present data on the Slow Reverse devices. The data in these figures are presented in two types of plots. The first type is called a Retention Plot (See Figure 3). In this type of plot, two Gate Threshold Voltages are plotted with respect to time. The top curve represents the Threshold Voltage with the test transistor operating in the High Conduction State. The bottom curve represents the Gate Threshold Voltage with the device operating in the Low Conduction State. The voltage difference between these two curves is called the "Threshold Voltage Window". From such a plot, the memory storage characteristics can be determined for a test device.

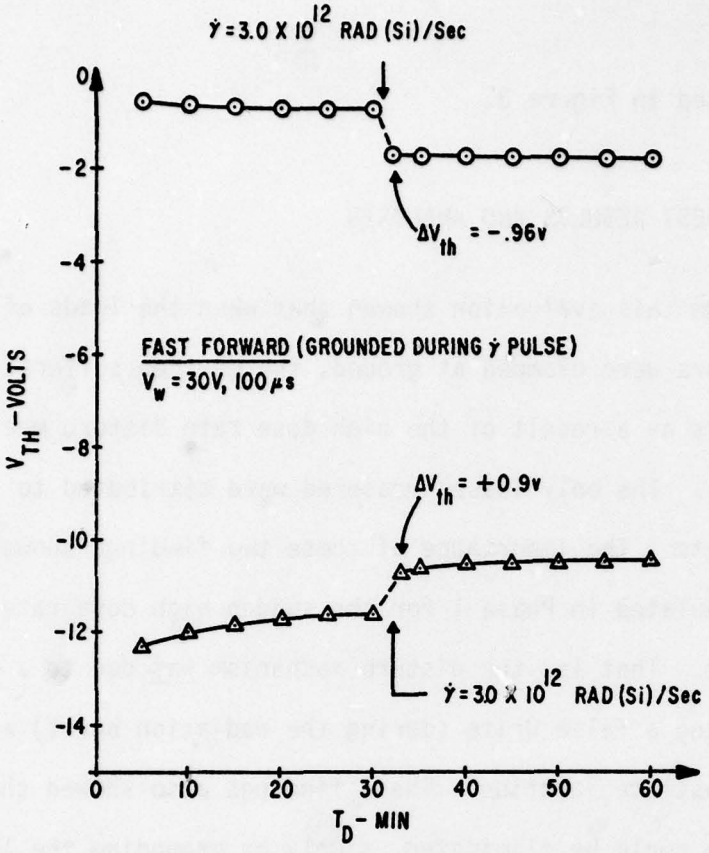


Figure 3. FAST FORWARD MNOS. Retention Plots of Vth Window BEFORE AND AFTER a Radiation Burst.

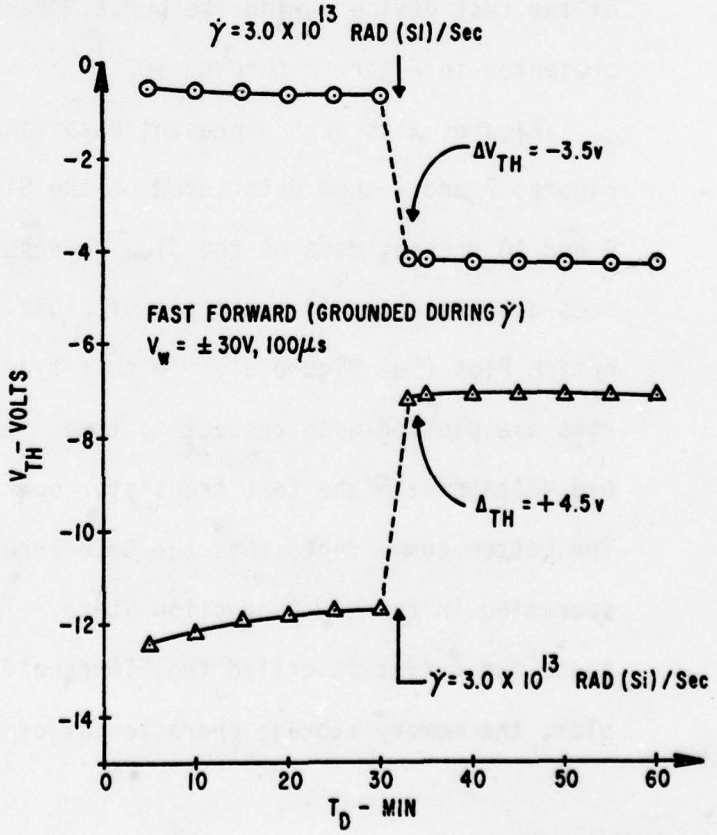


Figure 4. FAST FORWARD MNOS. Retention Plots of Vth Window BEFORE and AFTER a Radiation Burst.

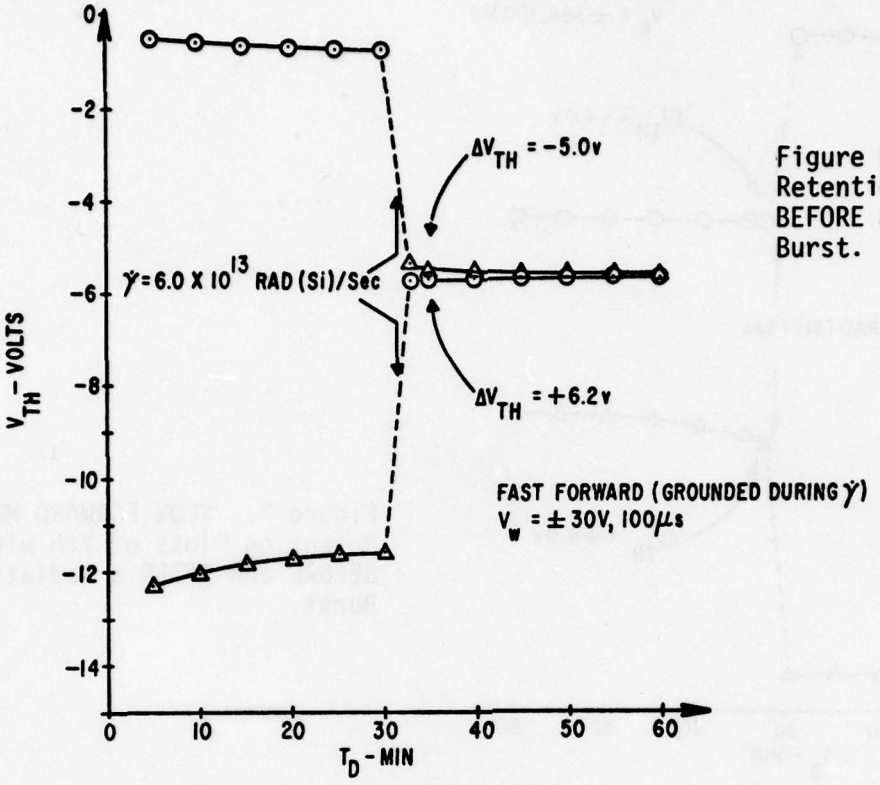


Figure 5. FAST FORWARD MNOS. Retention Plots of Vth Window BEFORE and AFTER a Radiation Burst.

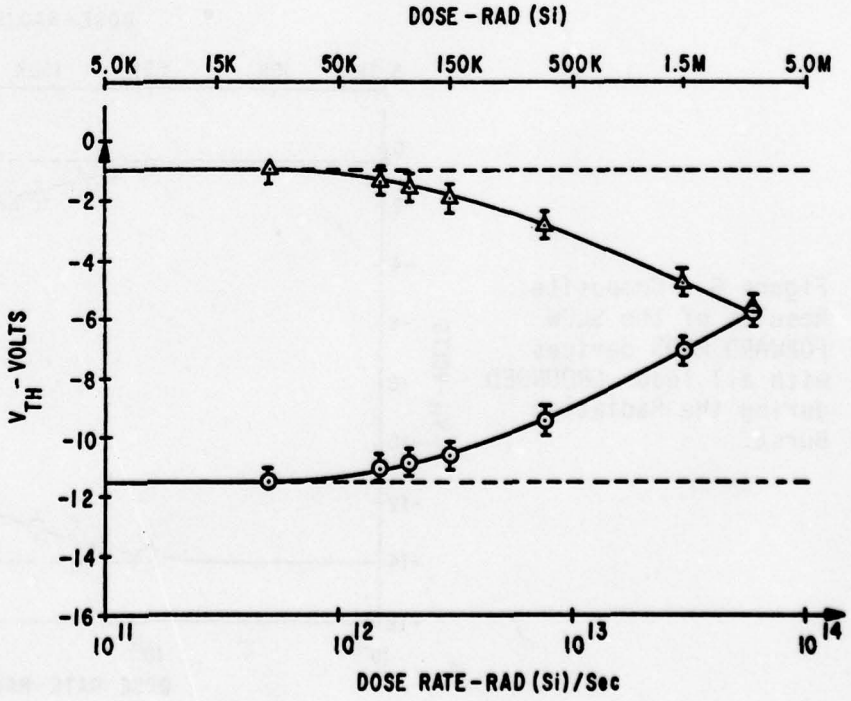


Figure 6. Composite Results of the FAST FORWARD MNOS devices with all leads GROUNDED during the Radiation Burst.

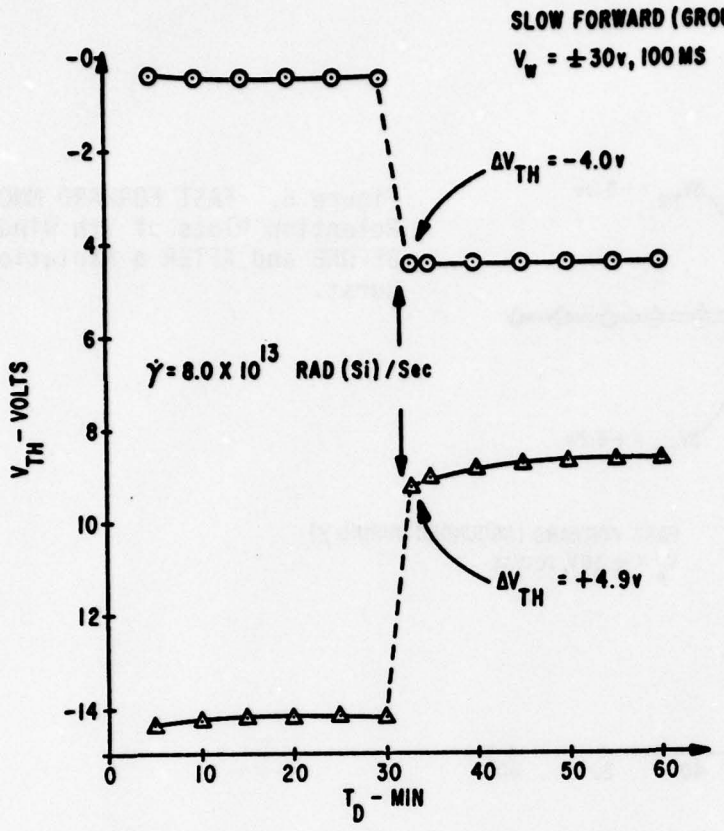


Figure 7. SLOW FORWARD MNOS. Retention Plots of Vth Window BEFORE and AFTER a Radiation Burst.

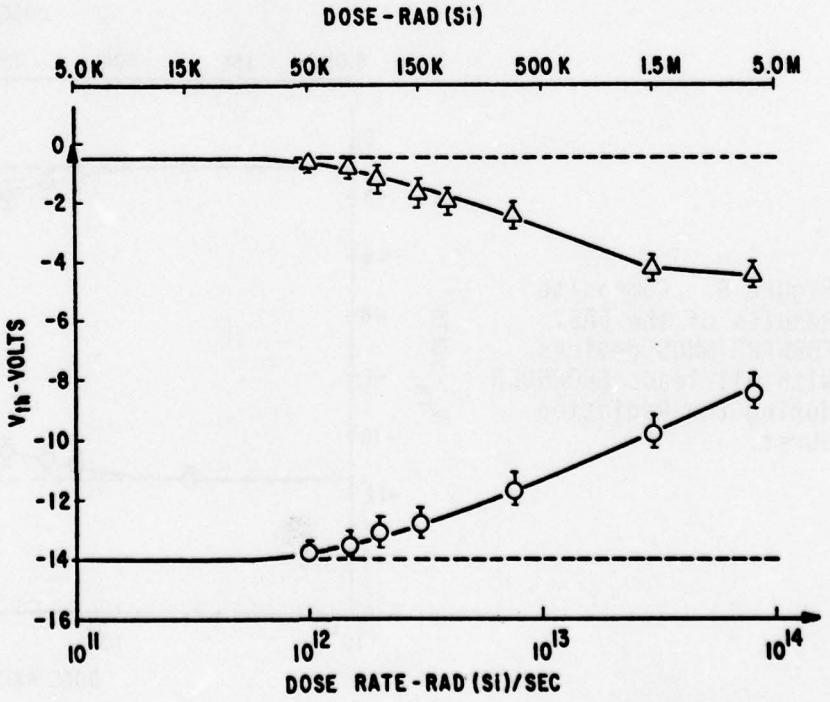


Figure 8. Composite Results of the SLOW FORWARD MNOS devices with all leads GROUNDED during the Radiation Burst.

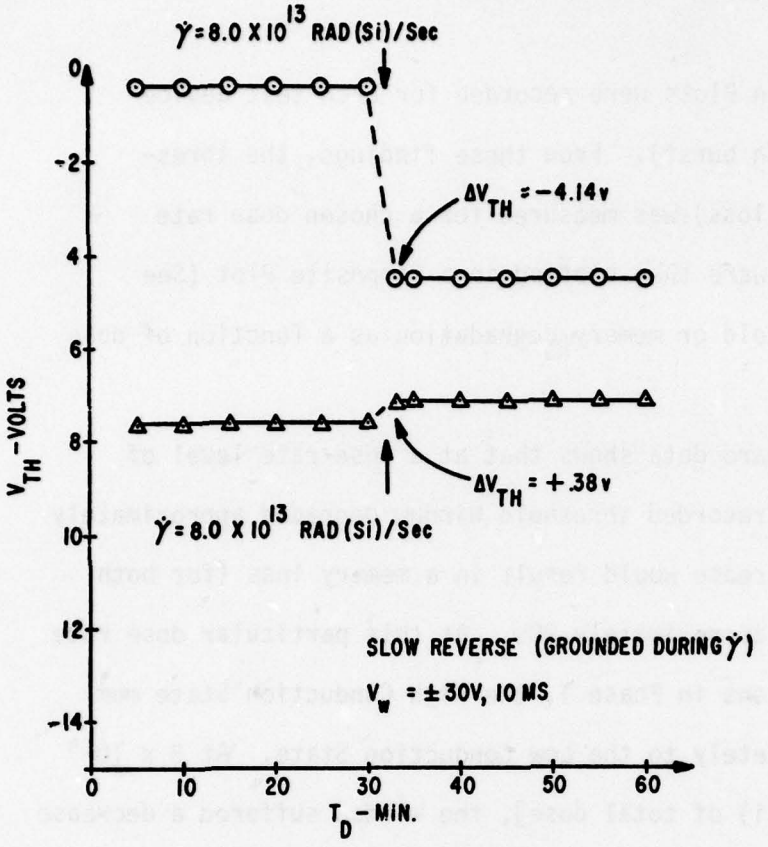


Figure 9. SLOW REVERSE MNOS. Retention Plots of Vth Window BEFORE and AFTER a Radiation Burst.

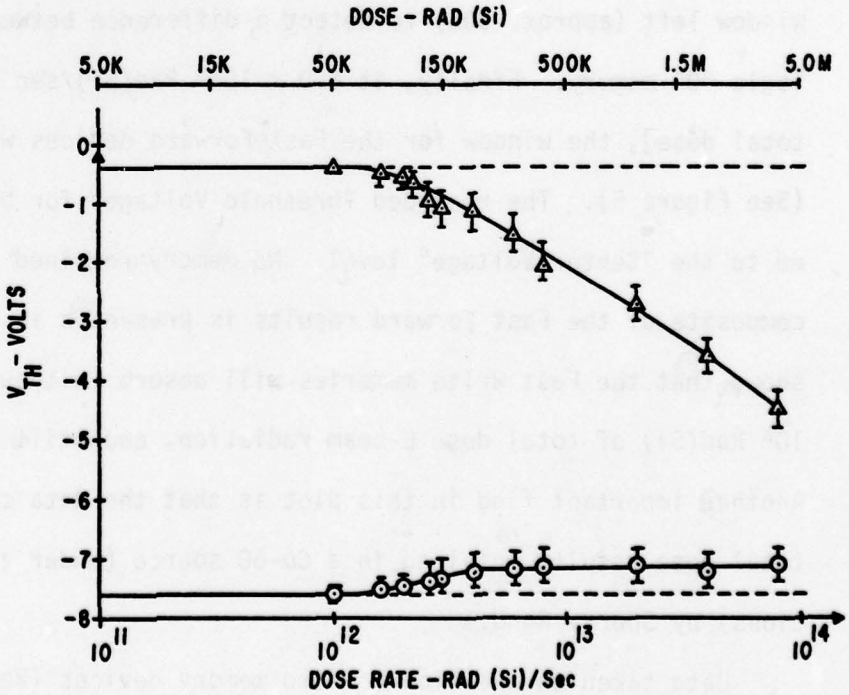


Figure 10. Composite Results of the SLOW REVERSE MNOS devices with all leads GROUNDED during the Radiation Burst.

In this test phase, Retention Plots were recorded for each test device (BEFORE and AFTER a radiation burst). Fron these findings, the threshold degradation (or memory loss) was measured for a chosen dose rate level. The overall results were then plotted in a Composite Plot (See Figure 6) showing the threshold or memory degradation as a function of dose rate and total dose.

Analyzing the Fast Forward data shows that at a dose rate level of 3.0×10^{12} Rad(Si)/sec, the recorded threshold Window degraded approximately 2 volts. This amount of decrease would result in a memory loss (for both logic "1" and logic "0") of approximately 20%. At this particular dose rate level under the test conditions in Phase 1, the High Conduction State memory would have shifted completely to the Low Conduction State. At 3×10^{13} Rad(Si)/sec [1.5×10^{6} Rad(Si) of total dose], the window suffered a decrease of approximately 8 volts (See Figure 4). However, there was still enough window left (approx. 30%) to detect a difference between a logic "1" or a logic "0" memory. Finally, at 6.0×10^{13} Rad(Si)/sec [3×10^{6} Rad(Si) of total dose], the window for the Fast Forward devices was completely closed (See Figure 5). The recorded Threshold Voltages for both states were degraded to the "Center Voltage" level. No memory remained in the devices. A composite of the Fast Forward results is presented in Figure 6. This plot shows that the Fast Write memories will absorb (without a re-write) 1.5×10^{6} Rad(Si) of total dose E-beam radiation, and still maintain a memory. Another important find in this plot is that the data correlate with the total dose results obtained in a Co-60 source (under zero gate bias conditions) by Sperry Rand.

Data taken on the Slow Forward memory devices (Ref Figure 7 and 8) showed

that the Threshold Voltage Window never closed during this phase of testing. The highest dose rate level that the test devices were subjected to was 8.0 x 10^{13} Rad(Si)/sec. At this level, the memories were subjected to a total dose per shot equal to 4 x 10^{6} Rad(Si). Threshold Window losses at this level were approximately 65%. This still left enough window to detect the correct memory. Also, as with the Fast Forward data, the composite results in Figure 8 correlated with the Sperry Rand Co-60 results.

The last two plots (Figures 9 and 10) showed the test results taken on the Slow Reverse type transistors. The results showed that there were no measurable degrading effects on the devices until a dose rate level of 1.2 x 10^{12} Rad(Si)/sec was reached. Note that in the Phase 1 tests, degradation of the memories in the same devices was noted at the dose rate level of 9.0 x 10^{11} Rad(Si)/sec, approximately 1.5 x 10^{3} Rad(Si) lower in total dose. An interesting result from this group of tests was that when losses in the Window did occur, only the Threshold Voltage in the High Conduction State was significantly effected. The high dose rate had little effect on the memory stored in the Low Conduction State. As an example, Figure 9 shows that the Gate Threshold Voltage suffered a shift of approximately -4.14 volts at the dose rate level of 8.0 x 10^{13} Rad(Si)/sec while operating in the High Conduction State. However, the change in Threshold at this same dose rate level while operating in the Low Conduction State was only +0.35 volts. This phenomenon was just the opposite from the results observed in Test Phase 1. The data from this phase also showed (See Figure 10) that the Reverse devices could maintain a readable memory in either state (without a re-write) at total dose levels beyond 1.5 x 10^{6} Rad(Si). These data also correlated with the Sperry Rand Co-60 results.

Another important result obtained from these tests was that all of the devices survived and were still operating properly after the tests. That is, the initial Clear, Write, Read and Storage Characteristics did not change as a result of the radiation.

CONCLUSIONS

From the test results in this test phase, it was again concluded that the MNOS memory transistor can survive and operate in a high ionizing dose rate environment with no permanent electrical changes in its operational characteristics. However, it was also concluded that the high dose rate memory losses observed in Phase 1 were due to a high negative voltage generating a false Write across a high impedance gate-substrate junction during a radiation burst. Another conclusion was that this false Write phenomenon could be eliminated simply by grounding the gate and substrate leads to a ground potential. And finally, grounding the gate and substrate together during the radiation burst resulted in a MNOS memory device that was not dose rate dependent (only total dose dependent). That is, the losses in memory stored in the MNOS in a high dose rate environment, were the same as those measured in a low dose rate environment (such as Co-60).

DISCUSSION

In the above test results, it was shown that grounding the gate and substrate leads of an MNOS memory transistor during a high dose rate radiation burst would eliminate the memory disturb mechanism observed in Phase 1. However, phyically grounding the gate and substrate junctions of an actual

LSI MNOS Memory array during a real transient radiation burst is not realistic. A solution to the problem would be to use some type of circumvention technique that would allow the array to operate normally in a non-radiation environment, and then automatically (during a radiation burst) clamp the gate and substract junctions to some common potential thereby preventing a sudden charge buildup across the gate to substrate terminals. One possible circumvention technique that could be used is illustrated below in Figure 11.

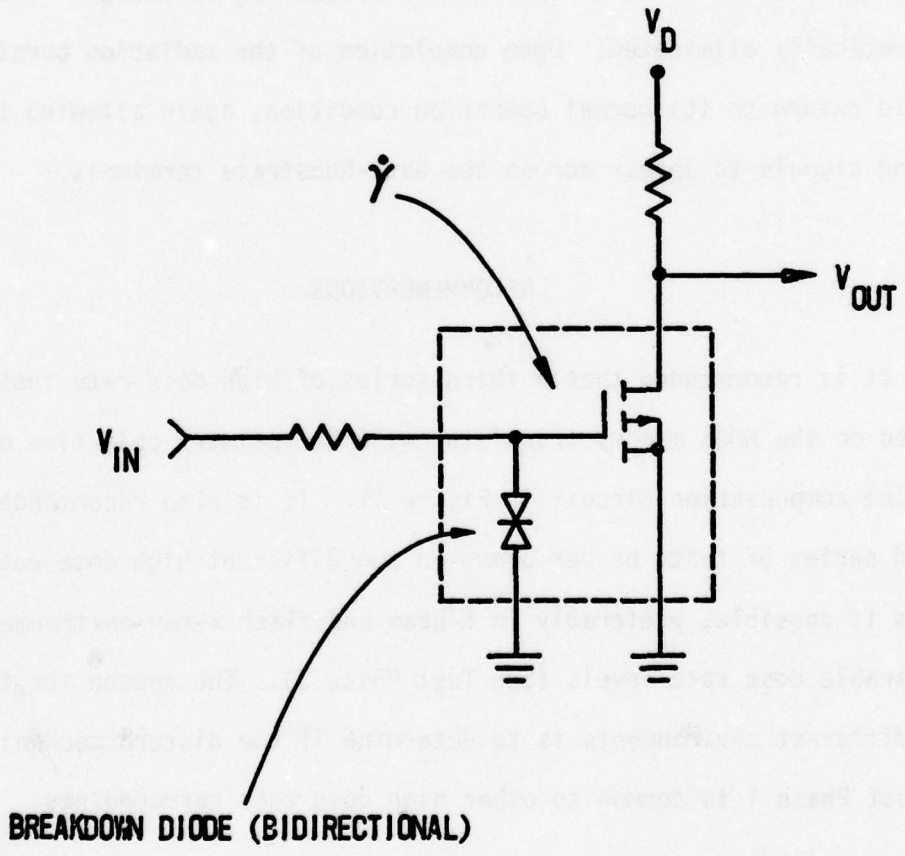


Figure 11. Possible Compensation Circuit using a PNP Bidirectional Diode.

Figure 11 shows a "back-to-back" PNP bidirectional diode in parallel with a high gate resistance to ground. During normal operation (no radiation), the bidirectional diode should act as a high impedance to ground thereby allowing the application of both positive and negative Clear-Write-Read pulses to the Gate terminal. During a transient radiation pulse, the diode (which will also be exposed to the radiation) should become photoconductive and clamp the Gate terminal to the same ground potential as the substrate. Therefore any charge buildup across the Gate-Substrate junction should be shunted to the common ground through the conducting diode. If this procedure works, the false Write phenomenon observed in Phase 1 should be automatically eliminated. Upon completion of the radiation burst, the diode should return to its normal operation condition, again allowing the proper gating signals to appear across the Gate-Substrate terminals.

RECOMMENDATIONS

It is recommended that a third series of high dose rate tests be performed on the MNOS memory transistor with the primary objective of evaluating the compensation circuit in Figure 11. It is also recommended that the third series of tests be performed in two different high dose rate environments if possible, preferably in E-beam and flash x-ray environments with comparable dose rate levels (See Test Phase 3). The reason for testing in two different environments is to determine if the disturb mechanism observed in Test Phase 1 is common to other high dose rate surroundings.

HIGH IONIZING DOSE RATE EFFECTS ON DISCRETE MNOS TRANSISTORS (PHASE 3)

ABSTRACT

This report describes the last of a series of high dose rate tests performed on radiation resistant MNOS memory transistors fabricated by Sperry Rand. The objectives of this particular effort were to determine the effectiveness of the diode compensation circuit (proposed in Phase 2) in eliminating the false Write phenomenon observed in Phase 1, and to evaluate this circuit along with the MNOS devices in two different high dose rate environments (E-beam and X-ray). The results of this evaluation showed that the diode compensation circuit was effective (in both environments) in eliminating the radiation induced Write pulse. Thus, the MNOS device was made only total dose dependent. Another conclusion was the false Write disturbance was found to be greater in the E-beam environment than in the flash x-ray environment. This was attributed to the number of "Secondary Electrons" present in each environment. It was believed that low energy secondary electrons being driven from the transistor can lids of the test devices and attaching themselves to the posts and fly-wires of the memory created the false Write effect. The effect was worse in the E-beam mode mainly because of the greater concentration of electrons. Finally, from these series of tests, it was concluded by the AFWL that the MNOS memory transistor was a viable candidate for use in a nuclear and space radiation environment. As a result, AFWL became actively involved in the design, testing, and fabrication of a fully decoded radiation hardened MNOS RAM array.

INTRODUCTION

In Phases 1 and 2 of this test series, it was demonstrated that the Non-step Gate MNOS Memory Transistor was inherently hard to high dose rate radiation, if the Gate and Substrate of the device were maintained at the same ground potential during the burst. Maintaining a ground potential on these two terminals resulted in an MNOS memory cell that was only affected by the total radiation dose absorbed. The rate of absorption had no effect. However, if the ground potential was not maintained during the burst, a possible memory loss could occur from a false Write pulse being created across the Gate/Substrate junction during the radiation. If this occurred, the MNOS device would also become dose rate dependent. Such a dependency would neutralize the non-volatility feature of this technology in high transient radiation. To eliminate this problem, a possible circumvention technique was proposed in Phase 2. This proposed technique was to use a bidirectional breakdown diode installed between the memory Gate and the grounded Substrate. The reason for using such a diode was that in a non-radiation environment, the diode would allow the memory transistor to operate normally. However, when the circuit was subjected to a high dose rate of radiation, the diode (through photoconduction) would automatically clamp the Gate terminal to the same ground as the substrate. This action should eliminate the false Write phenomenon.

The main thrust of this paper is to evaluate the above diode technique in two different high dose rate radiation environments. The two test environments are: (1) the AFWL Febetron 705 Flash X-ray machine operating in the 2 MeV E-beam Vacuum Mode, and (2) the AFWL PI-1590 Super Flash X-ray machine operating in the 10 MeV Gamma Mode. Levels of dose rate testing for both environments will range from 10^{11} to 2 x 10^{12} Rad(Si)/sec.

THE MNOS TEST TRANSISTOR

The MNOS memory transistor that was used in this evaluation was one of four different experimental gate structures built especially for the Air Force Weapons Laboratory by Sperry Rand in 1974 (ref. 1). The test device was classified as a Fast Forward, non step-gate, P-channel memory transistor, built on a bulk silicon substrate. Each device was packaged in a standard "KOVAR" TO-5 transistor can. Some of the structures and electrical characteristics are summarized below.

Oxide Thickness	20 Angstroms
Nitride Thickness	445 Angstroms
Write Voltage	24 Volts (Nominal)
Write Time	2 μSec or Greater
Read Time	250 nSec or Less
Retention	24 Hours or Greater

The above device was chosen because of its performance in neutron and total gamma radiation. In 1 MeV Pulse Neutrons, the memory transistors survived with no degrading effects at exposure levels to 10^{15} n/cm^2. In a low dose rate Co-60 environment, the devices were able to maintain a memory (without a Re-write) at exposure levels to 1×10^6 Rad(Si). See Figure 1. The survival level in Co-60 was well beyond 10^7 Rad(Si).

Figure 1 shows a typical Zero Bias Retention plot of one of the test devices recorded under non-radiation and Co-60 conditions. The Co-60 plot

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1. Marraffino, P, et al. Design and Fabrication of Radiation Hardened MNOS Memory Array, AFWL-TR-74-209.

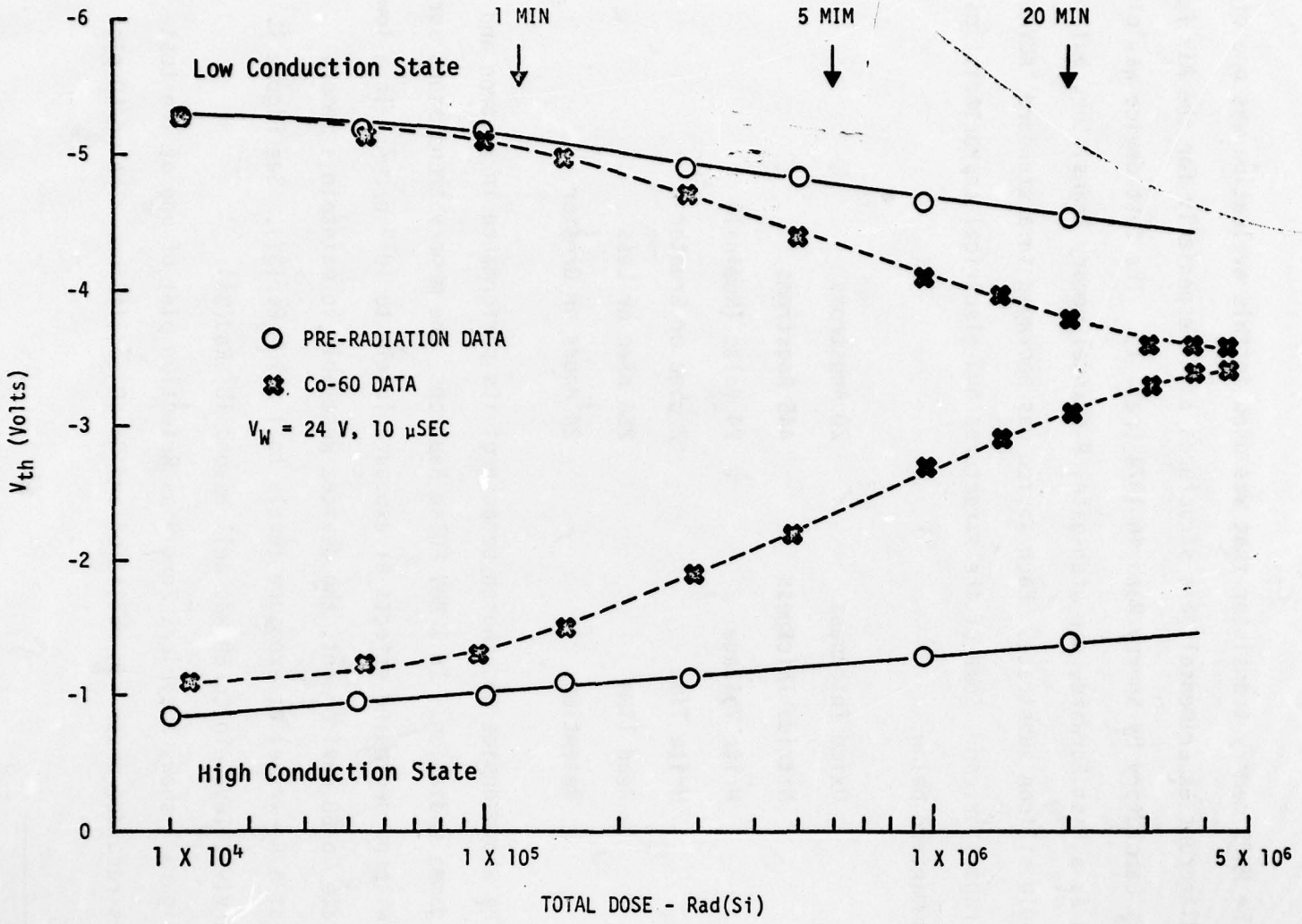

Figure 1. Typical Zero Bias Retentions Plots of the Threshold Voltage Window for a FAST FORWARD MNOS Memory Transistor BEFORE and DURING Co-60 Irradiation. Dose Rate ≈ 2 x 10^3 Rad(Si)/sec.

shows that at an exposure level of 1 x 10^6 Rad(Si), approximately 30% of the orginal memory window was still intact. This was still considered large enough to discriminate between a logic "1" and a logic "0" memory.

TEST OBJECTIVES AND APPROACH

The main objective in this test phase was to evaluate the Diode Compensation circuit presented in Phase 2. The second objective was to evaluate the new MNOS memory transistor in two different high dose rate environments and then compare the results.

To achieve these two objectives, the test transistor was evaluated under the test conditions presented in Figure 2. The first setup illustrates a worse case condition where large threshold voltage shifts were recorded after high dose rate irradiations (See Test Phase 1). The second configuration represents an optimum test condition where no charge buildup or false Write was allowed to occur across the leads of the test device. This setup was used in Phase 2 and in the Co-60 tests. Test condition 3 represents the circumvention technique where a bidirectional diode was installed between the memory gate and the grounded substrate. This setup allows the simulation of a MNOS memory transistor being driven by a Metal Oxide Semiconductor (MOS) type device. The bidirectional diode should become photoconducting during irradiation in the same way a PNP MOS source-drain junction would photoconduct. If the diode compensation circuit works, it should simulate (during the radiation burst) the test conditions presented in configuration number 2. Note that for this particular test phase, the bidirectional diode was composed of two single 1N914 diodes wired back-to-back.

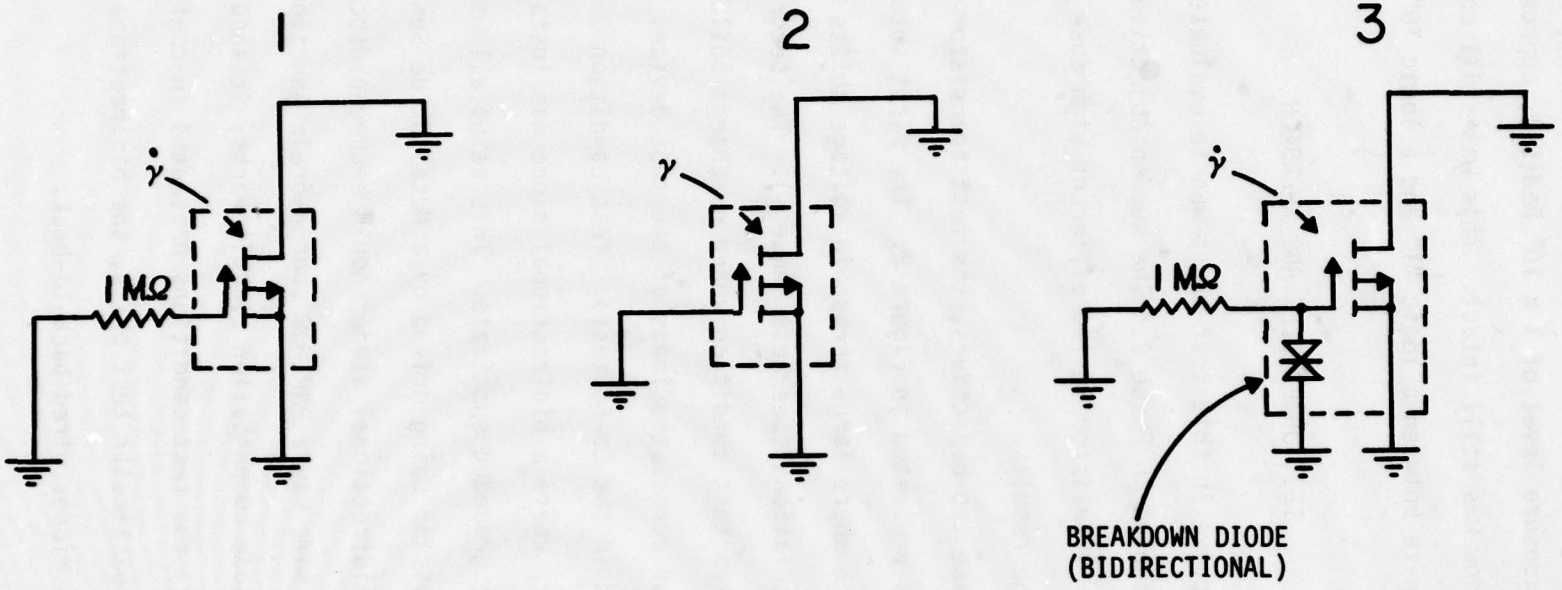

Figure 2. Transient Radiation Response MNOS Test Conditions.

TEST RESULTS AND ANALYSIS

The test results from this evaluation showed that the diode compensation circuit (Test Condition 3) did eliminate the false Write phenomenon observed under Test Condition 1. The compensation circuit was effective for both the E-beam and the Flash X-ray environments. In the comparison tests between the two high dose rate environments, the results showed that the same effects existed in both environments, but at different magnitudes. The effects were worse in the 2 MeV E-beam. Data showed that the memory losses (for the same dose rate levels) in the E-beam were greater by a factor of approximately 4 over the memory losses in the X-ray mode. Verification of these results is presented in Figures 3 and 4.

Figure 3 shows the Threshold Voltage shifts (or memory losses) of nine Fast Forward MNOS memory transistors as a function of E-beam total dose and dose rate. The main curve presents the data when the gates of the test devices were clamped at 1 MΩ above the substrate ground (Test Condition 1). For comparison purposes, the threshold shifts as a function of equivalent total accumulated dose were also plotted for Co-60 exposures. Finally, a third plot using the diode compensation circuit on three of the test transistors was also recorded.

The results in Figure 3 show that large threshold shifts did occur in the memory devices when operating in the High Conduction State and under Test Condition 1. As an example, at the dose rate level of 6×10^{11} Rad(Si)/sec [3×10^{5} Rad(Si) of total dose], the shifts were large enough to be considered a total memory loss. A total shift in memory state was considered to occur at the dose rate level of 1×10^{12} Rad(Si)/sec. These results are in agreement with the data obtained in the Phase 1 tests.

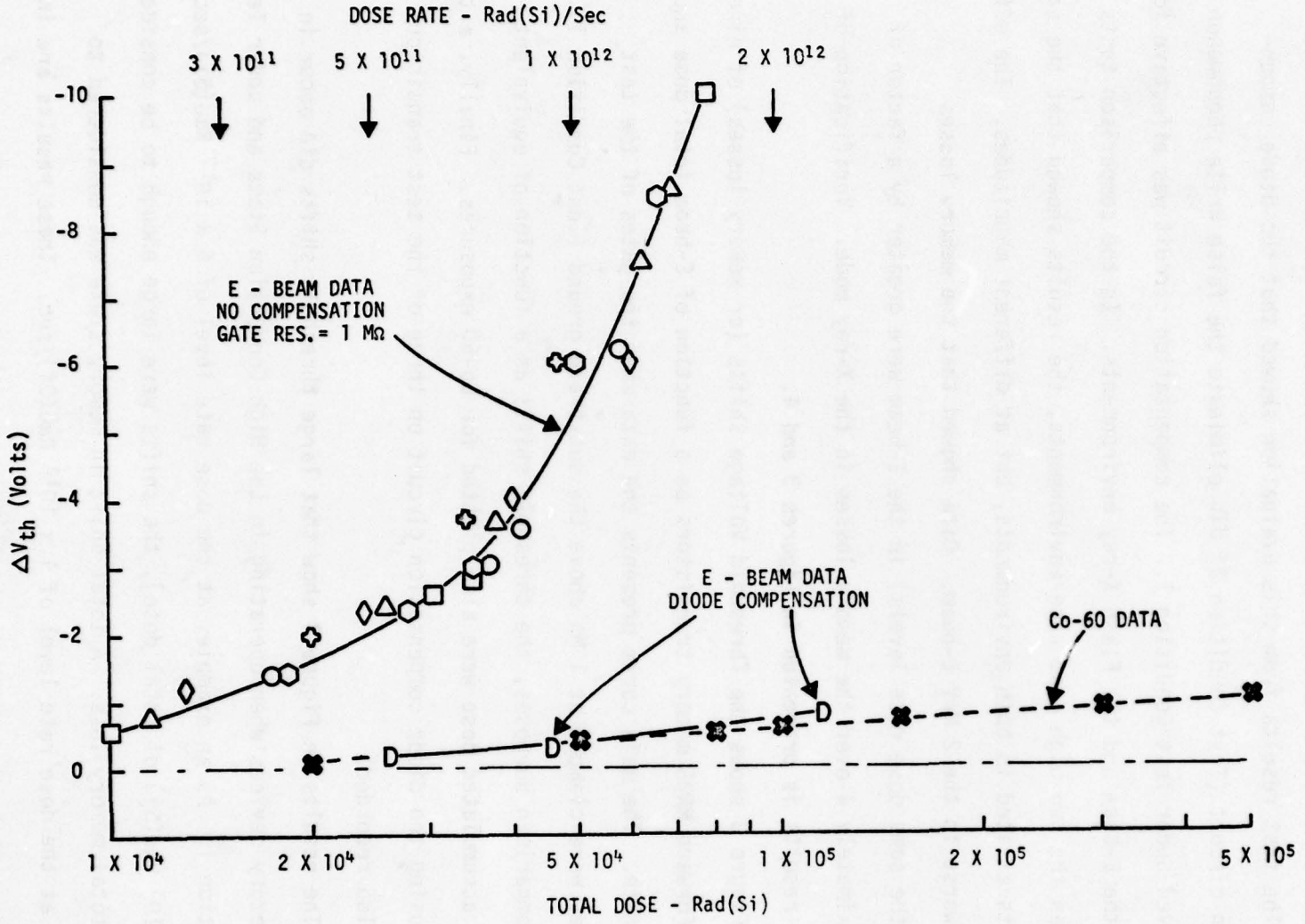

Figure 3. FAST FORWARD MNOS. Threshold Voltage Shifts as a function of 2 MeV E-beam Total Dose and Dose Rate. Co-60 presented for Comparison.

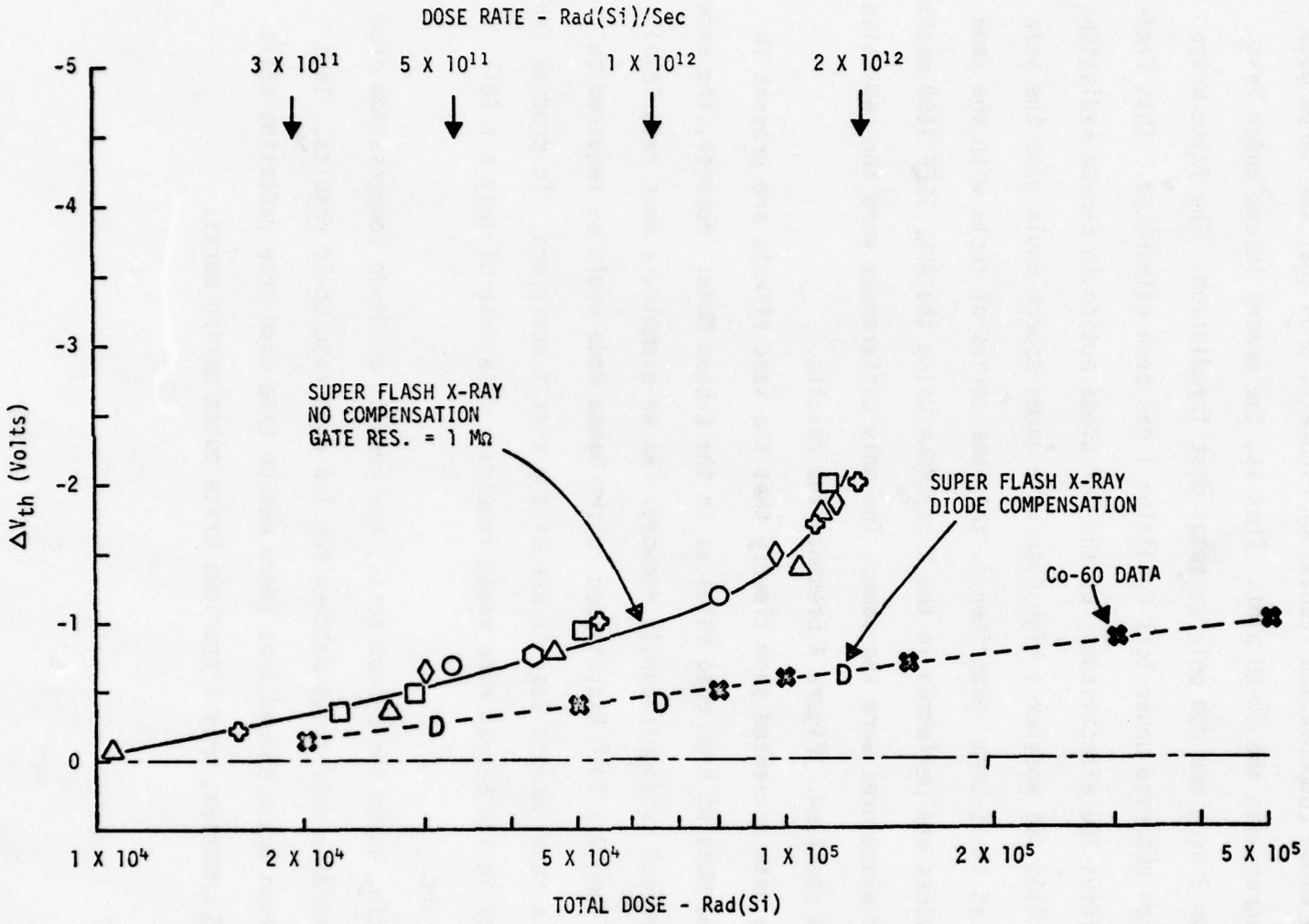

Figure 4. FAST FORWARD MNOS. Threshold Voltage Shifts as a function of 10 MeV Gamma Total Dose and Dose Rate. CO-60 presented for Comparison.

The diode compensation results of Figure 3, show that the three data points agree with the Co-60 plot. That is, the memory losses under Test Condition 3 were now due only to total dose irradiation. The false Write phenomenon observed under Test Condition 1 has been eliminated. This finding verifies the effectiveness of the PNP diode action in E-beam radiation.

To find out whether a high dose rate gamma source would give the same results as the E-beam experiments, the same series of tests with the same test devices was performed in the X-ray Mode using the AFWL TREF 1590 machine. All test procedures were the same. The only differences were the radiation type and spectrum. Figure 4 presents the results.

The data presented show clearly that the same effects are present in the Gamma Mode at high dose rates as in the E-beam Mode. However, the extent of the effect is significantly reduced. As an example, a dose rate level greater than 2×10^{12} Rad(Si)/sec in the Gamma Mode would be required to produce a total memory loss in one of the test transistors. To produce the same loss in the E-beam Mode would require a dose rate of only 6×10^{11} Rad(Si)/sec.

Again, as in the E-beam tests, the results of Diode Compensation from the gamma dose rate tests matched the low dose rate Co-60 results. This information again showed that there was no true dose rate radiation shift for MNOS memories, only a spurious Write pulse during burst.

FINAL CONCLUSIONS

From this test evaluation and from Phases 1 and 2, the following conclusions were formulated.

1. The MNOS transistor can survive and operate in a high dose rate radiation environment with no permanent changes in its electrical operating characteristics. This means that even after a possible memory loss at a high dose rate, the device can be re-written and operated as if it was never irradiated.

2. If major memory losses do occur in a high dose environment, they are attributed to a negative Write voltage generated across the Gate-Substrate junction during the radiation burst. This is true only if there is a moderately high impedance between the Gate, Substrate, and ground.

3. When there is a high impedance between the Gate, Substrate, and the ground terminal of the MNOS device, the memory losses will be greater in high dose rate E-beam environment than in a high dose rate gamma environment. A reason for this conclusion is presented in the DISCUSSION.

4. Shunting the charge buildup across the Gate-Substrate junction during the radiation burst will result in a MNOS memory transistor that is not dose rate dependent (only total dose dependent). That is, if the charge buildup can be prevented on the Gate-Substrate leads during the radiation shot, the resulting threshold shifts (or memory losses) will be of the same magnitude as those measured in a lower dose rate environment of equivalent total absorbed dose (Co-60).

5. Finally, the false Write phenomemon observed throughout the evaluation can be automatically circumvented by using bidirectional diode techniques.

DISCUSSION

In the above three test evaluations it was observed that there was a Write disturb mechanism that was caused by a high negative voltage being generated across a high impedance Gate-Substrate junction of the test devices during a radiation burst. This disturb mechanism was the cause of the memory losses at dose rate levels lower that predicted and was greater in the E-beam Mode than it was in the Gamma Mode. Up till this last phase of testing, the source of this sudden charge buildup was not idenified. But, as a result of the false Write effect appearing in both of the transient modes, a possible source could now be identified. This source was "Secondary Electrons". Secondary Electrons have been know to appear in both of the test environments when the beams (at high dose rates) were directed at thin metal targets. It is now believed that low energy secondary electrons were driven off the can lids of the test devices during the tests. The result was that these low energy electrons did not penetrate the target, but did attach themselves to the post and fly-wires of the memory device, creating a large negative voltage pulse across a high impedance path to ground. In some of the above tests, the external Gate to Ground to Substrate path was a high impedance. The final effect was a false Write pulse re-writing a memory during a radiation burst.

This phenomenon was greater in the 2 MeV E-beam environment because there was a greater number of low energy electrons, mainly from the beam itself. Adding the bidirectional diode to the circuit simply removed the high impedance path during the irradiation, thereby preventing a charge build-up. The result was there was no false Write.

From these three series of high dose rate tests, it was concluded that the MNOS memory transistor is a viable candidate for use in nuclear and space

radiation environments. The device was inherently hard to neutron irradiation, Co-60 irradiation, and high dose rate irradiation. All that was necessary was to reduce the susceptibility to large voltage buildups resulting from secondary electrons. Using a circumvention technique like the one presented in Phases 2 and 3 of this evaluation would solve this problem.

As a result of this effort, the Air Force Weapons Laboratory became actively involved in 1973 (with Sperry Rand) to design, test, and fabricate a fully decoded radiation hardened MNOS RAM array.

SECTION II

DISCRETE PMOS STUDIES

IONIZING DOSE RATE AND TOTAL DOSE TESTS ON RADIATION HARDENED PMOS TRANSISTORS

ABSTRACT

This report presents the ionizing radiation total dose and dose-rate evaluation performed on a radiation hardened P-channel Metal Oxide Semiconductor (PMOS) transistor fabricated in 1973 by Sperry Rand. The objective of this evaluation was to determine the susceptibility of the PMOS technology (on bulk silicon) which was to be used for the decoder circuitry of a radiation hardened LSI MNOS RAM array under development by the Air Force Weapons Laboratory. Results from the effort showed that the permanent degradation of the Gate Threshold Voltages for the test devices was directly dependent upon the total dose absorbed and the Applied Gate Bias during irradiation. The greatest degradation occurred when the test devices were under a positive bias, and the least degradation occurred when the transistors were under zero or negative bias. The optimum Gate to Substrate bias was zero volts. Under this condition, the PMOS devices could absorb a total dose of Co-60 irradiation of at least 1×10^6 Rad(Si) and a dose rate of flash x-ray irradiation of at least 2×10^{12} Rad(Si)/sec before the failure criterion was met. The results also showed that for the same total dose absorbed, at the same Applied Gate Bias, the degradation of the Gate Threshold Voltage was greater in the high dose rate environment than in the low dose rate environment. This phenomenon was attributed to an effective positive Gate Bias (proportional to the dose rate level) being generated across the external Gate to Substrate resistance path and to a "Photovoltaic" Bias Effect being generated within the Substrate of the test device itself.

INTRODUCTION

In the preceding evaluations, it was shown that the MNOS memory transistor had a high tolerance to nuclear radiation. As a result, the Air Force Weapons Laboratory initiated an effort with Sperry Rand to design, fabricate and test a Large Scale Intergrated (LSI) MNOS RAM array suitable for application in a nuclear and space radiation environment.

One of the first objectives of this new effort was to develop a hardened peripheral technology which could be incorporated on the same chip as the MNOS memory cells and be used as the decoder circuitry. In selecting the the proper technology, "Available Resources", "Risk", and "Time" were used as the main guide lines. Under these restraints, the P-channel Metal Oxide Semiconductor (PMOS) technology was chosen. This technology differed from the MNOS in that the PMOS was a Fixed Threshold device was subjected to permanent Gate Threshold changes in radiation environments. However, in the 1974 to 1975 time frame, this technology had a broad exposure and showed a high probability for success, when integrated with MNOS.

The main objective of this paper is to evaluate this PMOS technology in ionizing radiation environments. This was done with the use of special Enhancement Mode PMOS (on bulk silicon) devices incorporating a "clean" Gate oxide for radiation hardness. Environments used for this evaluation were the Sandia Laboratories Co-60 source and the AFWL PI-1590 10 MeV peak Flash X-ray machine (FXR). Total dose and dose rate data were obtained.

THE PMOS TEST TRANSISTOR

The device type tested in this evaluation was chosen from a group of four PMOS gate structures, all fabricated for the AFWL by Sperry Rand in November of 1973. Major characteristics of the device chosen were that it had a Gate structure of approximately 1150 Angstroms of "Aubuchon" clean oxide, a Drain-Source Breakdown Voltage of approximately 48 volts, and a pre-radiation Gate Threshold Voltage of approximately -2 volts.

Selection of this particular structure over the other three was made from preliminary radiation tests performed at the Sandia Laboratories SPR II nuclear reactor and Co-60 source (ref. 1). The test results showed that the clean oxide structure could survive 1 MeV neutron irradiation up to 10^{15} n/cm^2 with no degrading effects, and suffer a permanent shift in Gate Threshold Voltage of less than 2 volts (under zero bias) after absorbing a total dose of Co-60 radiation of 1×10^6 Rad(Si). The three other device types (with oxynitride gates) suffered the same shift after absorbing a total dose of only 1×10^5 Rad(Si), an order of magnitue lower in total gamma radiation hardness than the clean oxide structure.

Each of the transistors tested in this evaluation was packaged in a four-lead TO-5 transistor can. The mask configuation was the same design used in the previous MNOS test devices (See Figure 1 in the first test phase of the MNOS evaluation).

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1. Marraffino, P, et al. Design and Fabrication of Radiation Hardened MNOS Memory Array, AFWL-TR-74-209.

TEST OBJECTIVES AND APPROACH

The objective of this evaluation was to determine the effects of total dose and dose rate radiation on the "Static Characteristics" of the PMOS test device. The Static Characteristics define the operation of the test transistor under the influence of applied DC voltages. In this test, the primary interest is in determining the permanent changes in the Gate Threshold Voltage before and after a particular total dose or dose rate radiation.

The basic setup for this series of tests is illustrated below in Figure 1.

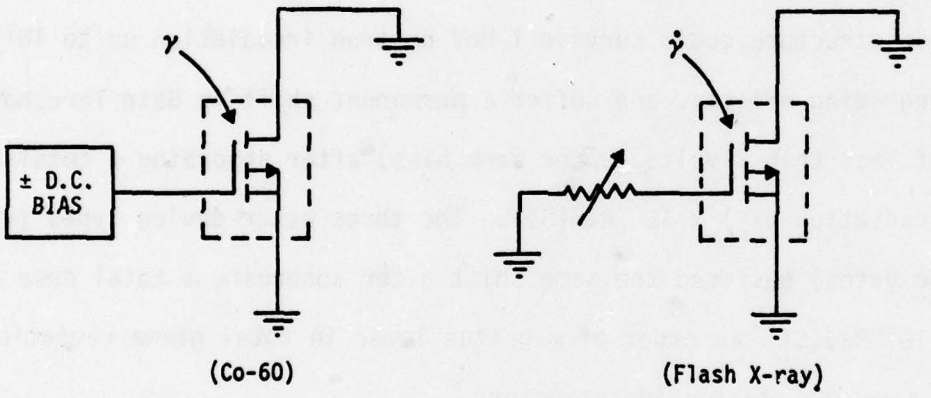

Figure 1. Co-60 and Flaxh X-ray PMOS Test Configurations.

In the total dose tests, the PMOS devices were irradiated (while under different Gate biases) in a Co-60 source at Sandia Laboratories. The devices were irradiated beyond a total dose level of 1×10^6 Rad(Si) at the low dose rate of 4.7×10^2 Rad(Si)/sec. The data showed the permanent changes in the Gate Threshold Voltage as a function of total gamma dose and applied Gate bias.

In the high dose rate tests, the devices were irradiated in the X-ray Mode at the AFWL 1590 Super Flash X-ray Facility. The dose rate levels of exposure ranged from 2×10^{11} to 2×10^{12} Rad(Si)/sec. The transistors were irradiated with resistors of different values installed between the Gate and grounded Substrate leads. Values of these resistors ranged from 100 ohms to 1 Megohm. No Gate bias voltage was applied during the radiation period. The motivation for using this setup was to measure the effects of charge and Gate voltage buildup under high and low Gate to Ground impedance. Data showed the permanent changes in the Gate Threshold Voltage as a function of applied dose rate and external Gate to Substrate resistance.

CO-60 TEST RESULTS

The Co-60 test results are presented in Figures 2 through 4. Basically, the data show that the special PMOS test transistor is "bias dependent" when operating in a total dose gamma environment. That is, the permanent Gate Threshold Voltage Shift (ΔV_{th}) is not only a function of the total absorbed radiation dose, but also dependent upon the applied Gate bias during the radiation.

The results show that the test device has a high resistance to the total dose irradiation while operating under zero or negative Gate bias conditions (See Figure 2). At zero Gate bias, the permanent shift in the Gate Threshold was less than -2 volts, even after absorbing 1×10^6 Rad(Si) of total dose. At this high dose level, under -30 volts Gate bias, the shift was still only approximately -2.5 volts. This was not the case for positive bias.

Under positive bias conditions, the permanent shift in Gate Threshold Voltage as a function of total dose were more pronounced (See Figure 3).

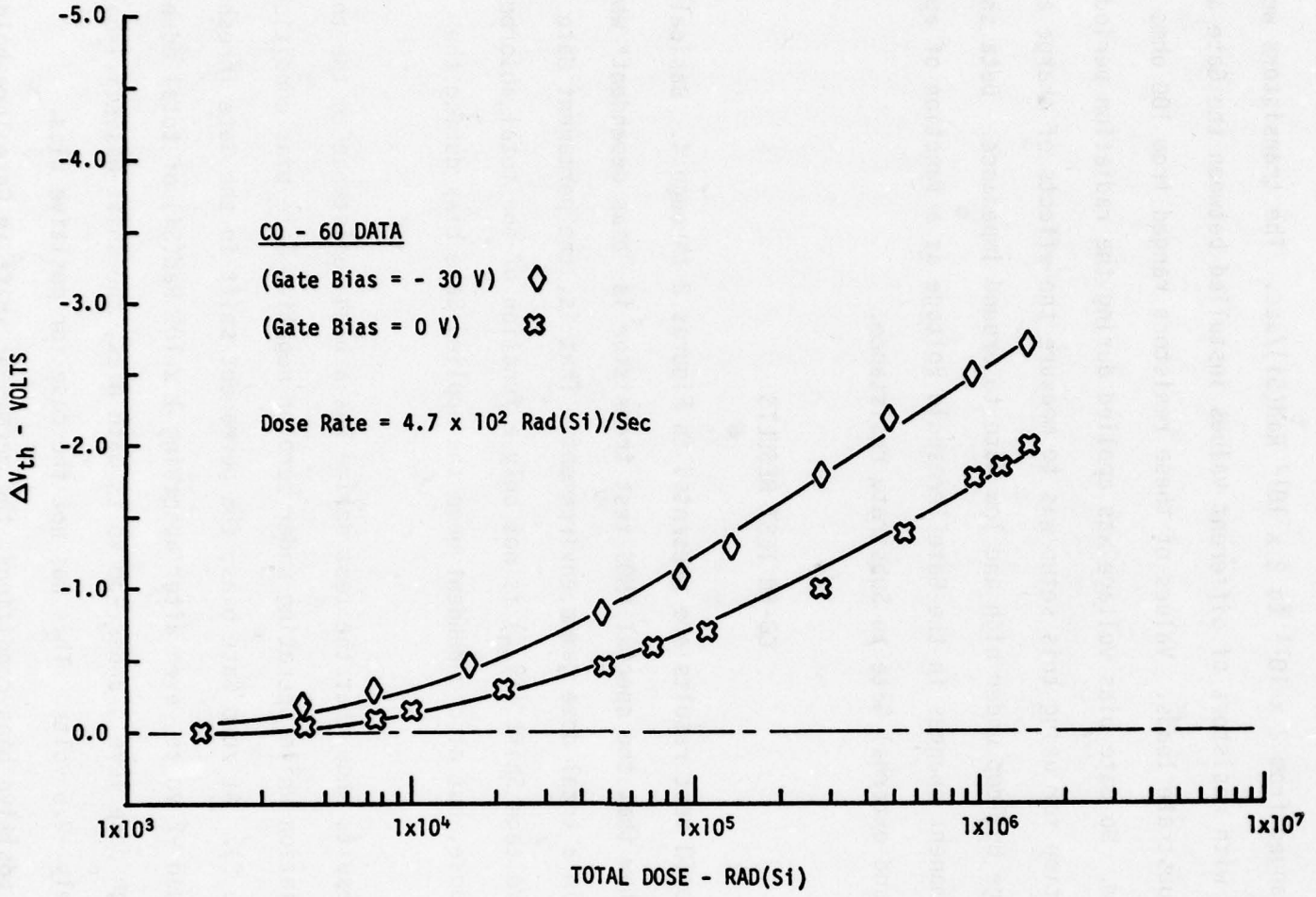

Figure 2. Co-60 Data. Gate Threshold Voltage Shift versus Total Gamma Dose for the PMOS Test Transistors with NEGATIVE Applied Gate Bias Voltages.

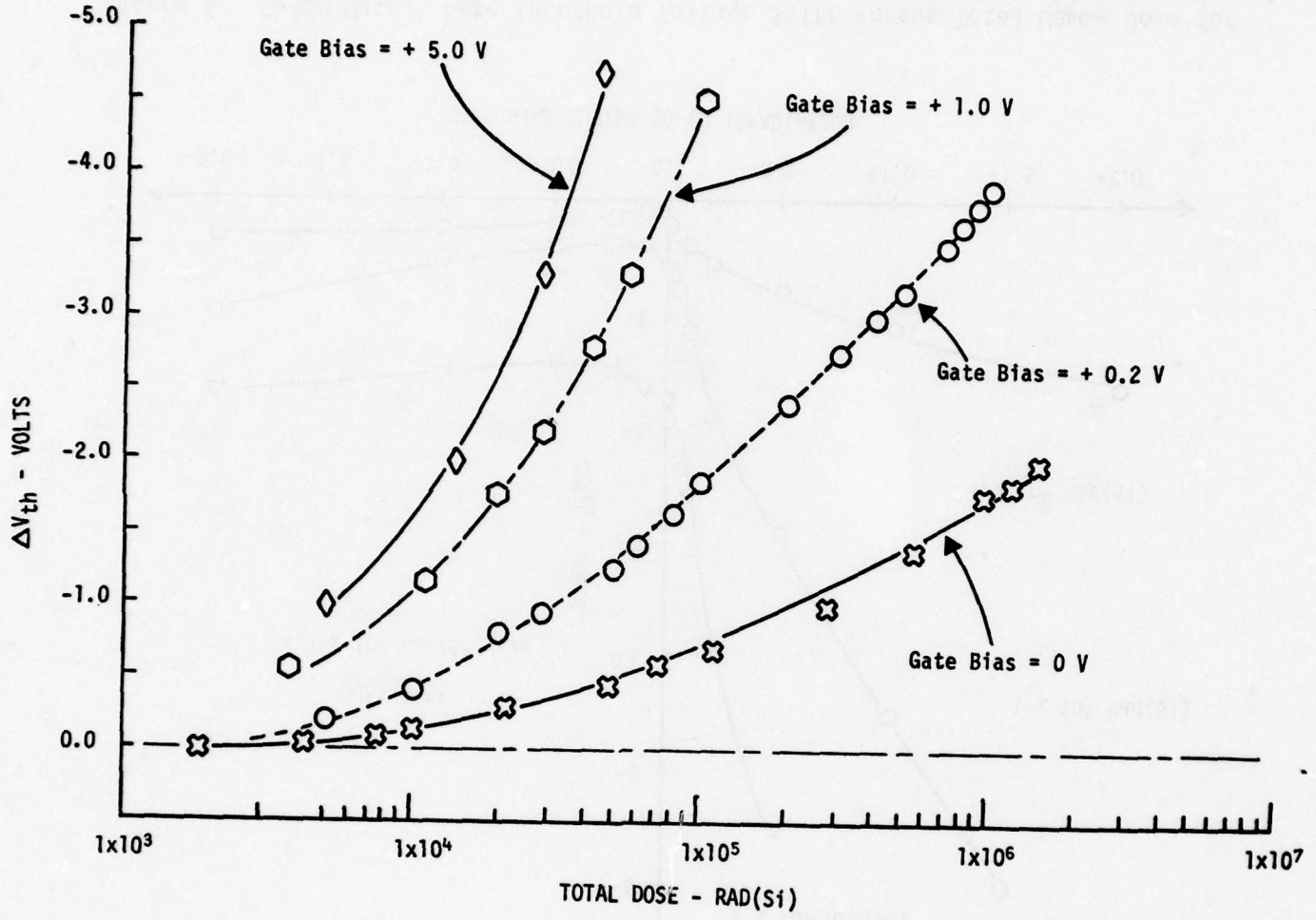

Figure 3. Co-60 Data. Gate Threshold Voltage Shift versus Total Gamma Dose for the PMOS Test Transistors with POSITIVE Applied Gate Bias Voltages.

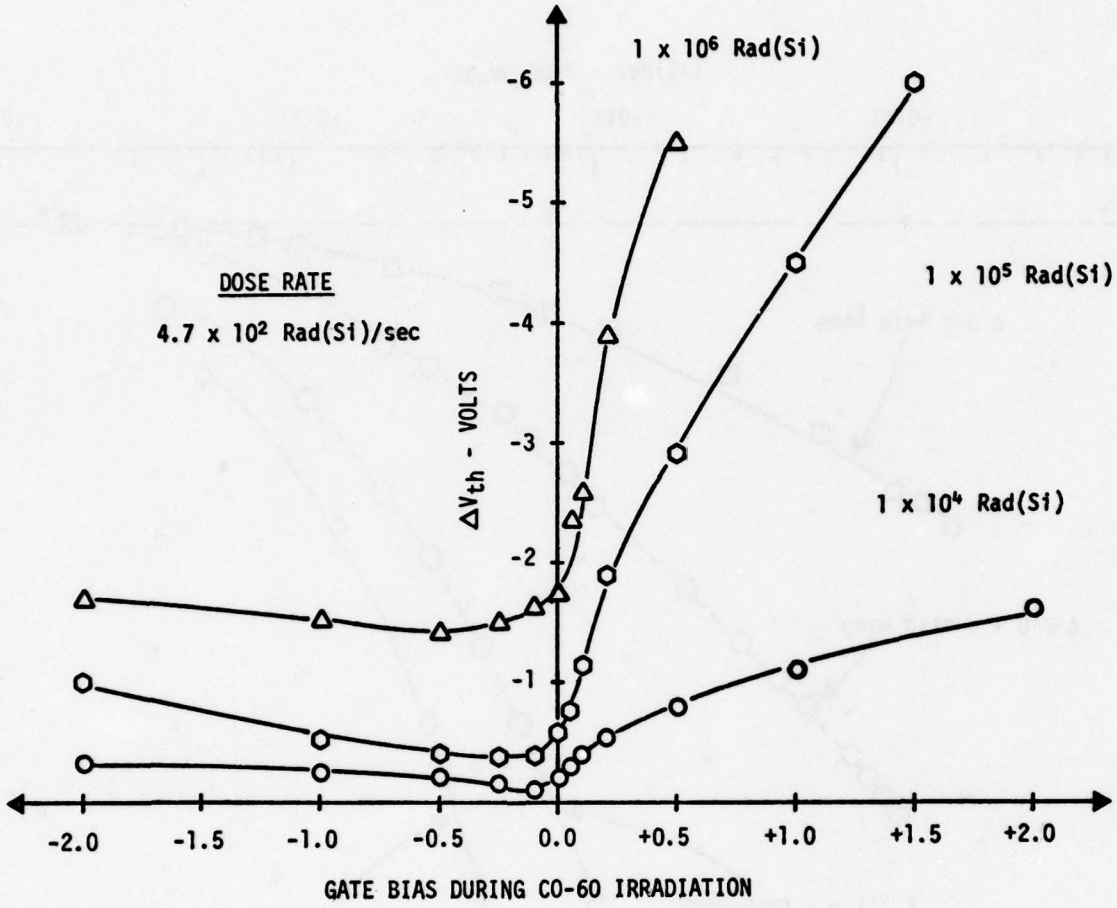

Figure 4. Co-60 Data. Gate Threshold Voltage Shift versus Total Gamma Dose for the PMOS Test Transistors operating with a POSITIVE or NEGATIVE Applied Gate Bias.

For example, under a Gate bias of +5.0 volts, the threshold voltages suffered permanent shifts of approximately -2 volts after absorbing a total dose of only a little over 1 x 10^4 Rad(Si). This amounts to a radiation hardness level of at least two orders of magnitude lower than that observed under zero bias. In fact, even with a positive bias of only +0.2 volts, the threshold was still greater than those measured under -30 volts.

The magnitude of this bias dependency is best seen in Figure 4. Shown are the permanent shifts in the Gate Threshold Voltage (for three different levels of total dose) as a function of positive and negative Gate bias. Basically, the plots show that the PMOS test transistors will have a high resistance to total dose radiation as long as the applied Gate bias remains negative. However, if the bias were allowed to go positive (even by a few millivolts), the susceptibility to radiation would be greatly increased.

FLASH X-RAY TEST RESULTS

The flash x-ray evaluation showed that the PMOS test transistor had a susceptibility to high dose rate ionizing radiation. This was especially true if there was a high external impedance between the Gate lead and the Substrate junction. Figure 5 shows this sensitivity.

The results showed that the permanent Gate Threshold Voltage shifts recorded on the test devices and as a function of dose rate radiation, were directly dependent upon the size of the Gate resistor. As an example, using a -2 volt shift as a failure criterion, the data show that the test devices would fail at a dose rate level of approximately 6 x 10^{11} Rad(Si)/sec with a 10 KΩ Gate resistor, fail at 9 x 10^{11} Rad(Si)/sec with a 100 ohm Gate

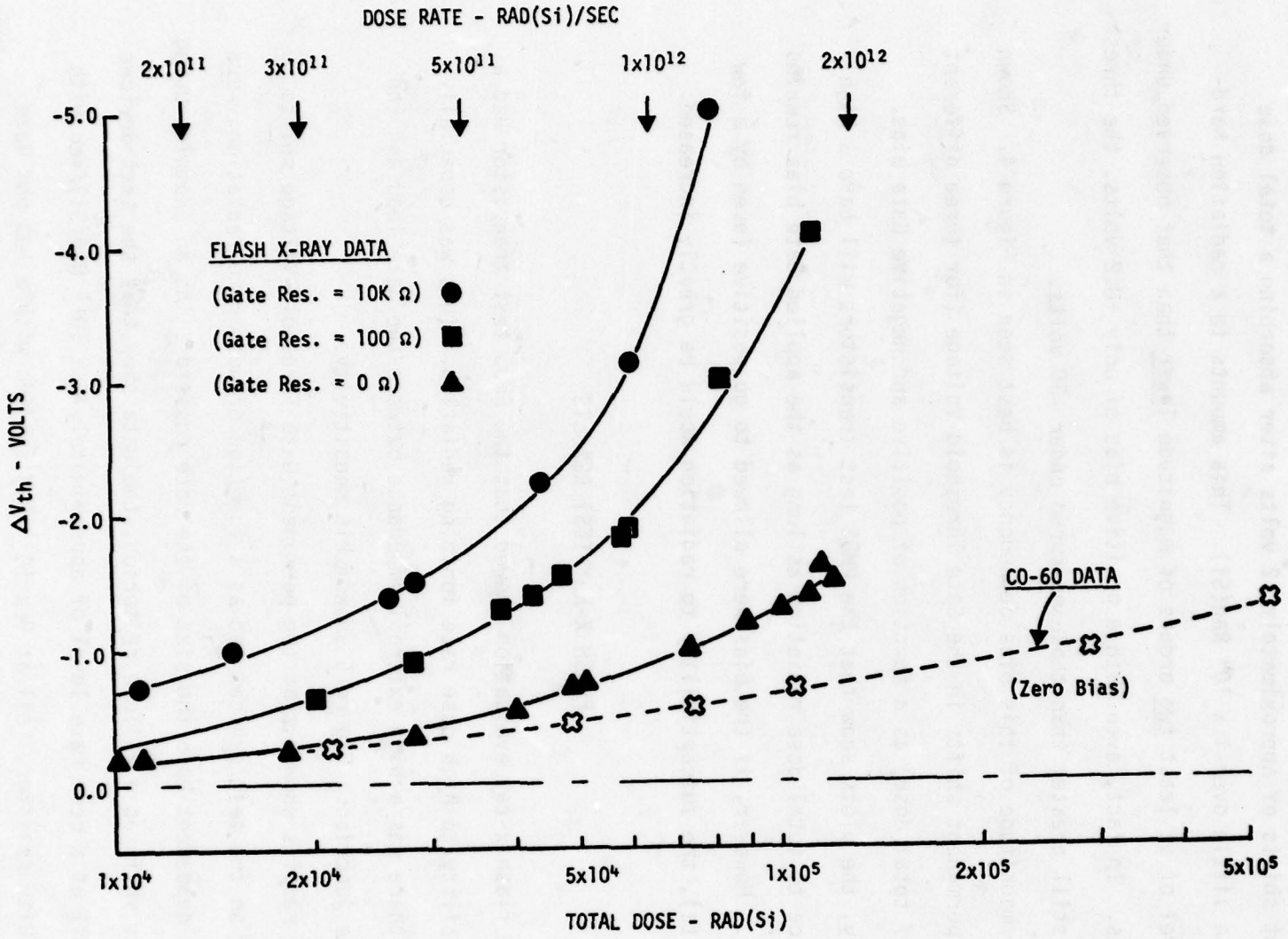

Figure 5. Flash X-ray and Co-60 Data. Comparison of the Gate Threshold Voltage Shift versus Total Gamma Dose for the PMOS Test Transistors. The Dose Rate Scale is for Flash X-Ray Only.

resistor, and fail somewhere beyond 2 x 10^{12} Rad(Si)/sec with zero Gate resistance.

The results also showed that, no matter how small the external Gate to Substrate resistance was made, the recorded shifts in the high dose rate environment were still greater that those obtained in the low dose rate Co-60 source. This can be seen in Figure 5 where the flash x-ray results taken under zero Gate resistance (all leads clamped at ground) did not match the Co-60 data. This phenomenon could not be explained by the preceding MOS or MNOS model. As a result, a new model had to be formulated. This model is presented in the Analysis.

ANALYSIS

In the total dose or Co-60 tests, the data showed that the permanent Gate Threshold Voltage Shifts were a function of the total absorbed radiation dose and the applied Gate Bias. This effect is not new, for it was predicted back in 1967 (ref. 2). In that prediction, the shift in the Gate Threshold Voltage of a MOS device in a <u>low</u> dose rate radiation environment was attributed to a net positive "space-charge" within the Gate oxide of the device itself. The amount of space-charge buildup was found to be a function of the total irradiated dose and the applied Gate Bias. A positive bias during irradiation produced the greatest net charge. When the irradiation ceased, the net positive space-charge remined in the oxide and produced the same effect as a positive Gate Bias. When this occurred in the PMOS test devices, the

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2. Mitchell, J.P., <u>Radiation Induced Space-Charge Buildup in MOS Structures</u>, IEEE Trans. on Electron Devices, ED-14, No.11, November 1967.

effective threshold (or turn-on voltage) was shifted towards a more negative value. This action resulted in a decrease in the turn-on speed and a slowing down of the device operation.

In the dose rate or flash x-ray tests, the findings showed that the permanent Gate Threshold Voltages occurring in the PMOS test devices were a function of the dose rate and the Gate to Substrate resistor. The results also showed that (for the same test conditions) the resulting threshold shift for the same absorbed total dose was greater in the high dose rate flash x-ray environment than in the low dose rate Co-60 environment. This finding suggested an existence of a "dose rate effect" associated with the test device.

In studying the dose rate results and associated literature, it was discovered that there was no available model which would satisfactorily predict the recorded data. As a result, it became necessary to develope a new model which could explain the results. In formulating the new model, it was generally agreed that the large permanent threshold shifts recorded in the high dose rate tests were enhanced by a positive Gate Bias being generated across the Gate-Substrate junction during the radiation burst. This assumption was based upon two facts:

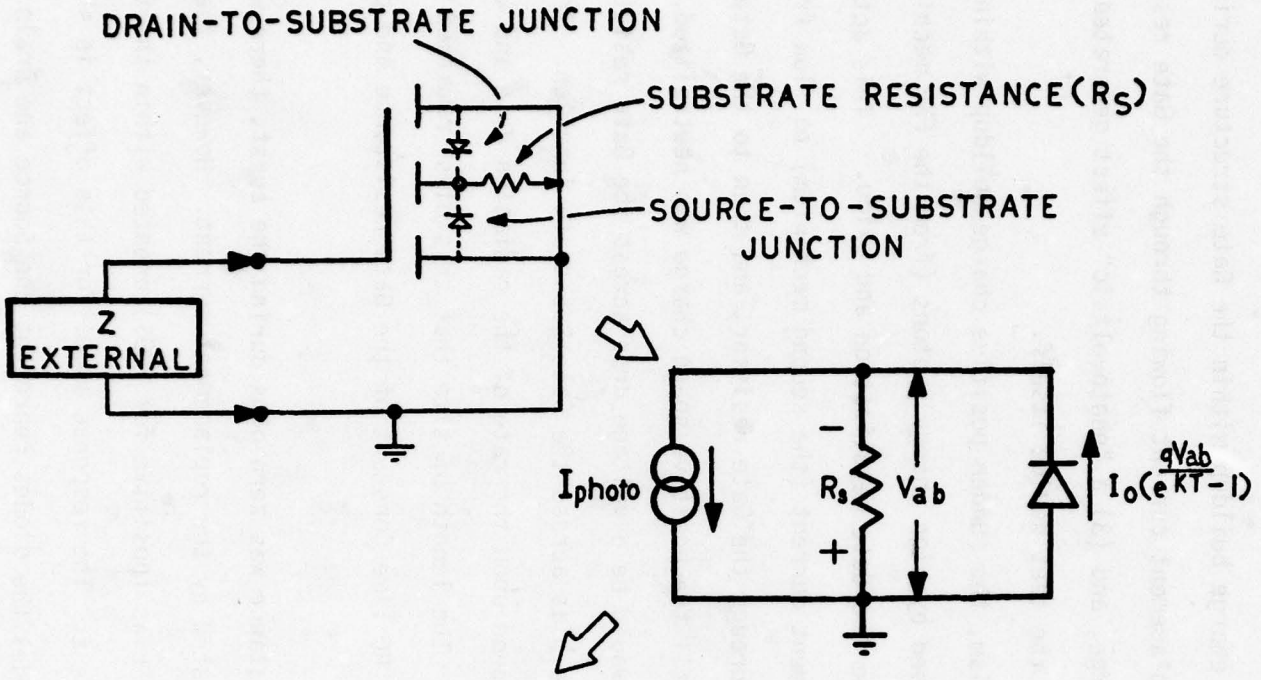
1. A change in the external Gate resistance (with no voltage applied) had a large effect on the recorded threshold shifts. This indicated that a bias voltage was being generated across this resistor by some type of "replacement current" during the irradiation.

2. The Co-60 results showed the same magnitudes of threshold shifts when the test devices were irradiated under positive Gate Biases of less than +5.0 volts. Equivalent shifts were never obtained with a negative bias, even if the value was as high as -30 volts.

A model was then proposed using the positive bias assumption as a base. The construction of this model was centered around three dose rate disturb mechanisms, all occurring at the same time. These mechanisms were: (1) a sudden positive space charge buildup within the Gate structure during the irradiation, (2) a replacement current flowing through the Gate resistor offsetting the space charge, and (3) a "photovoltaic" effect generated within the bulk substrate of the test device itself.

The first mechanism, the sudden positive charge buildup within the Gate, was assumed to be caused by high energy photons (from the FXR machine) knocking off electrons from the Gate metalization and oxide. This action then caused a replacement current (the second mechanism) to flow from the ground terminal, up through the Gate resistor, and then to the Gate. This current would flow until the positive space charge was neutralized. A result of this current flow would be a voltage drop across the Gate resistor, thereby creating a positive bias across the Gate-Substrate junction. The magnitude of this bias would depend upon the rate of the radiation dose and the size of the Gate resistor. The length of time that this bias remained on the Gate would depend upon the RC Time Constant of the Gate resistance and capacitance.

If the Gate resistance was zero ohms during the burst, there would be no Gate Bias generated by the replacement current. However, there would still be an effective bias (positive for PMOS) created within the Substrate by a photovoltaic effect. The response model for this effect is shown in Figure 6. In this model the diodes represent the Source and Drain of the test device. The resistance is the Substrate located between the channel region and the Substrate ground contact. This resistance includes the radiation



$$I_{PHOTO} = V_{AB}/R_S + I_O(e^{\frac{qV_{ab}}{KT}} - 1)$$

Figure 6. PMOS Transistor Transient Radiation Response Model.

induced conductivity modulation, plus any lead and metalization impedance. During intense irradiation, the diodes become photovoltaic cells loaded by the substrate resistor. The resulting voltage across this substrate resistor, negative in P-channel MOS, increases with increasing dose rate until a saturation level is reached. This photovoltaic effect results in an additional bias being generated across the Gate oxide (positive for PMOS and negative for NMOS) during the burst. For a silicon substrate, this additional bias can vary from 0 to 1 volt.

Analyzing the model further, by noting that the channel region is separated from ground by the Source and Drain junctions on one side and the Substrate resistance on the other, results in a small signal model with the following equation:

$$I_{photo} = V_{ab}/R_s + I_o\ (e^{qV_{ab}/KT} - 1)$$

This equation states that the photocurrent (I_{photo}) being generated in the Substrate of the device during a transient radiation pulse is equal to the current flowing through the substrate resistor (R_s) plus the diode current $I_o\ (e^{qV_{ab}/KT} - 1)$. The voltage term ($V_{ab}$) represents the potential being generated across the parallel combination of the substrate resistor and the source-drain diode. This voltage is the term that actually changes the effective Gate voltage. Note that the effective Gate voltage is the actual voltage appearing across the Gate oxide, which is the difference between the Gate-to-ground voltage and (V_{ab}). The $I_o\ (e^{qV_{ab}/KT} - 1)$ term is the D.C. Source-Drain-Substrate diode forward current and is a function of Applied Gate Bias. The "q" in the exponential term is the electron charge.

This particular response model was verified at the Air Force Weapons Laboratory in the spring of 1975, and the results were published in the IEEE Transactions (See Reference 3).

CONCLUSIONS

From this test evaluation, the following conclusions were formulated on the hardened Gate PMOS test transistors:

In both radiation environments (Co-60 and flash x-ray), the permanent degradation of the Gate Threshold Voltages for the test devices was directly dependent upon the total dose absorbed and the Applied Gate Bias during irradiation. The greatest degradation occurred when the devices were irradiated under a positive Gate bias. The least degradation occurred when they were irradiated under a zero or negative bias. The optimum Gate bias for minimum degradation was zero volts. Under this condition, the PMOS test transistors could absorb a total dose of Co-60 irradiation of at least 1×10^6 Rad(Si) and a dose rate of flash x-ray irradiation of at least 2×10^{12} Rad (Si)/sec before failure would occurred.

Also, for the same absorbed total dose and for the same Applied Gate Bias, the degradation of the Threshold Voltages was greater in the high dose rate flash x-ray environment than in the low dose rate Co-60 environment. This phenomenon was attributed to an additional positive Gate bias that was generated across the external Gate to Substrate resistance path, and across

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3. Maier, R.J. and Tallon, R.W., Dose-Rate Effects in the Permanent Threshold Voltage Shifts of MOS Transistors, IEEE Trans. on Nuclear Science, Vol. NS-22, No. 6, December 1975.

the internal resistance path of the Substrate itself, during the radiation burst. The additional positive Gate bias being generated across the external Gate to Substrate resistance was attributed to replacement currents being created during the irradiation. The additional positive bias generated within the silicon substrate was attributed to a Photovoltaic effect. Both of these effects were concluded to be dose rate dependent.

DISCUSSION

From this evaluation and others, the feasibility of using this PMOS technology for the peripheral circuitry of a radiation hardened MNOS RAM array has been demonstrated. The only major detectable weakness to ionizing radiation occurs when the PMOS Gate Bias is a positive voltage during the irradiation. Under this condition, the PMOS is highly susceptible. However, this should not be a problem in a low dose rate environment (such as Co-60), because the normal designed operating Gate Bias for this technology ranges between 0 and -30 volts. The only possibility of the Gate Bias inadvertently going positive (during the radiation period) is in a high dose rate environment when there is a high external impedance betwwen the Gate and Substrate terminals. This potential problem can be eliminated by using the same bidirectional diode compensation technique developed earlier in the discrete MNOS evaluation (See Phase 3 of the discrete MNOS test section). The other high dose rate phenomenon, the Photovoltaic Bias Effect, should not be a problem. This effect will not become a factor until the dose rate level of radiation goes well beyond 5×10^{11} Rad(Si)/sec. Even with this effect, the above PMOS technology should survive beyond 1×10^{12} Rad(Si)/sec.

SECTION III

MNOS MEMORY ARRAY STUDIES

IONIZING DOSE RATE AND TOTAL DOSE TESTS ON THE NITRON NONVOLATILE 256-BIT MNOS EAROM ARRAY NO. (NCM 7040)

ABSTRACT

Ionizing dose-rate and total dose tests have been performed on the Nitron NCM 7040 EAROM array. Results from these tests have shown that the devices can survive dose-rate levels as high as 7×10^{11} Rad(Si)/sec with no loss of memory data or permanent degradation in device operation. However, under certain test conditions, the "Read" and "Write" modes of the arrays can be temporarily interrupted. In the Read mode, this interruption can be induced at dose-rate levels of 2×10^{7} Rad(Si)/sec and higher, if the radiation burst is applied when "Data Output" information is just starting to come out of the memory. In the Write mode, upsets can be induced at dose-rate levels as low as 2.5×10^{7} Rad(Si)/sec, if the burst is applied at the start of a "Write Setup Time." Also, the total dose tests have shown that the memory array can accumulate a total dose of gamma radiation in excess of 1.5×10^{4} Rad(Si) and survive, while cycling through its Operational Modes at the maximum rate.

INTRODUCTION

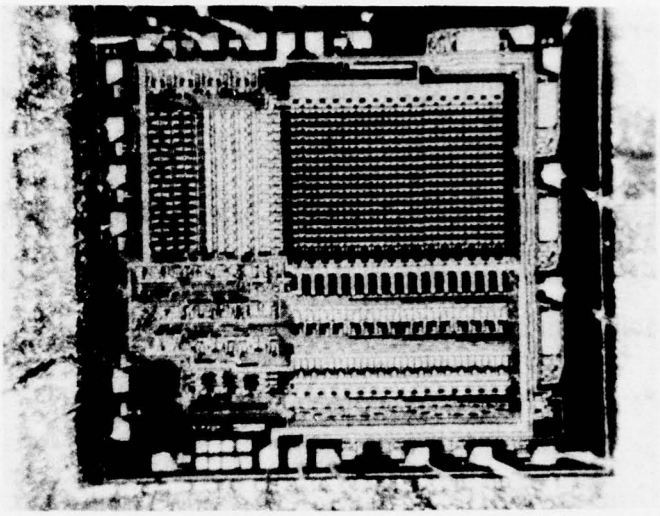
This evaluation covers the ionizing dose-rate and total dose radiation tests performed on the Nitron 256-bit, bulk silicon, MNOS EAROM array labeled NCM 7040. The dose-rate tests were performed at the Air Force Weapons Laboratory's Transient Radiation Facility using a Febetron 705 X-ray machine. The tests were performed using the Febetron 705 in the X-ray mode and in the E-beam mode. The total dose tests were performed at a Co-60 source located at Sandia Laboratories, New Mexico. The overall objective of these tests was to obtain background data and evaluate test procedures which could be used in future radiation tests on other MNOS arrays now under development.

THE NITRON NCM 7040

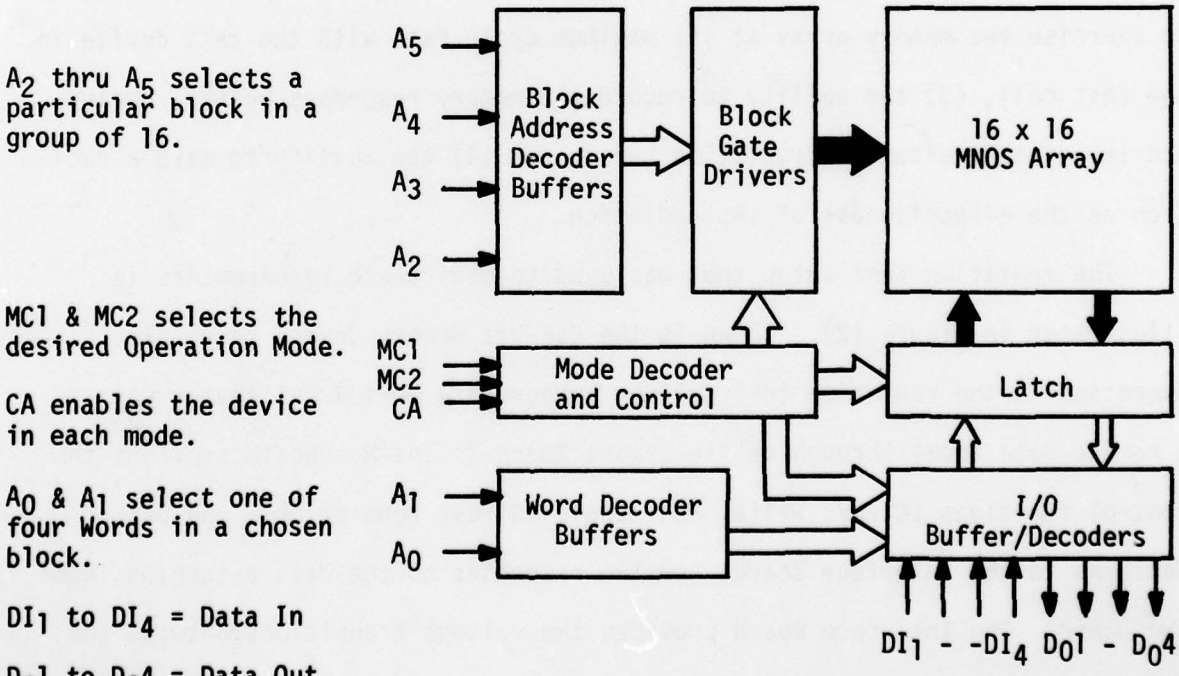
The NCM 7040 was chosen for this evaluation because it was one of the first fully decoded MNOS memory arrays that was commercially available. A photograph and simplified block diagram of the device is shown in Figure (1). The device is a 64 by 4-bit word, electrically alterable, non-volatile memory. It uses standard supply voltages of +5 and $\pm$15 volts. Other major features are: (1) fully decoded addressing, (2) four words per block erasability, and (3) tri-level I/O for T^2L and CMOS compatibility. Basically, the NCM 7040 is designed for applications where data must be stored for indefinite periods without power.

RADIATION TEST OBJECTIVES

Dose-Rate: The objectives of the dose-rate tests were to determine (1) the dose-rate levels needed to upset or jam the operational modes of the device,



(A)



(B)

Figure 1. Photograph and Simplified Block Diagram of the Nitron NCM 7040, 256-bit, MNOS EAROM Array.

(2) the maximum dose-rate levels the device could withstand and still operate after the burst, and (3) the length of time needed to recover from a particular radiation burst.

Total Dose: In the Co-60 tests, the objective was to determine the permanent or temporary changes in the memory's characteristics (under different operating conditions) as a result of a given amount of ionizing radiation.

TEST SETUP

In order to achieve the above objectives (especially in the dose-rate tests), the test setup had to have the following capabilities: (1) the ability to place the radiation burst at any point within the test cycle, (2) the ability to exercise the memory array at its maximum cycle rate with the test device in the test cell, (3) the ability to record the memory responses before, during, and immediately after the radiation burst, and (4) the ability to make a decision on the effectiveness of the radiation.

The radiation test setup that was used to meet these requirements is illustrated in Figure (2). Shown is the 256-bit memory device being electrically exercised in the radiation test cell by a Macrodata MD-104 LSI tester (in a remote data room) through as "Interface Board." The Macrodata provides the control functions (Clear, Write, and Read), address generations, the data patterns to the Interface Board, and the responses to the data returning from the board. The Interface Board provides the voltage transitions between the TTL output levels of the Macrodata and the ± 15 volt levels of the test device.

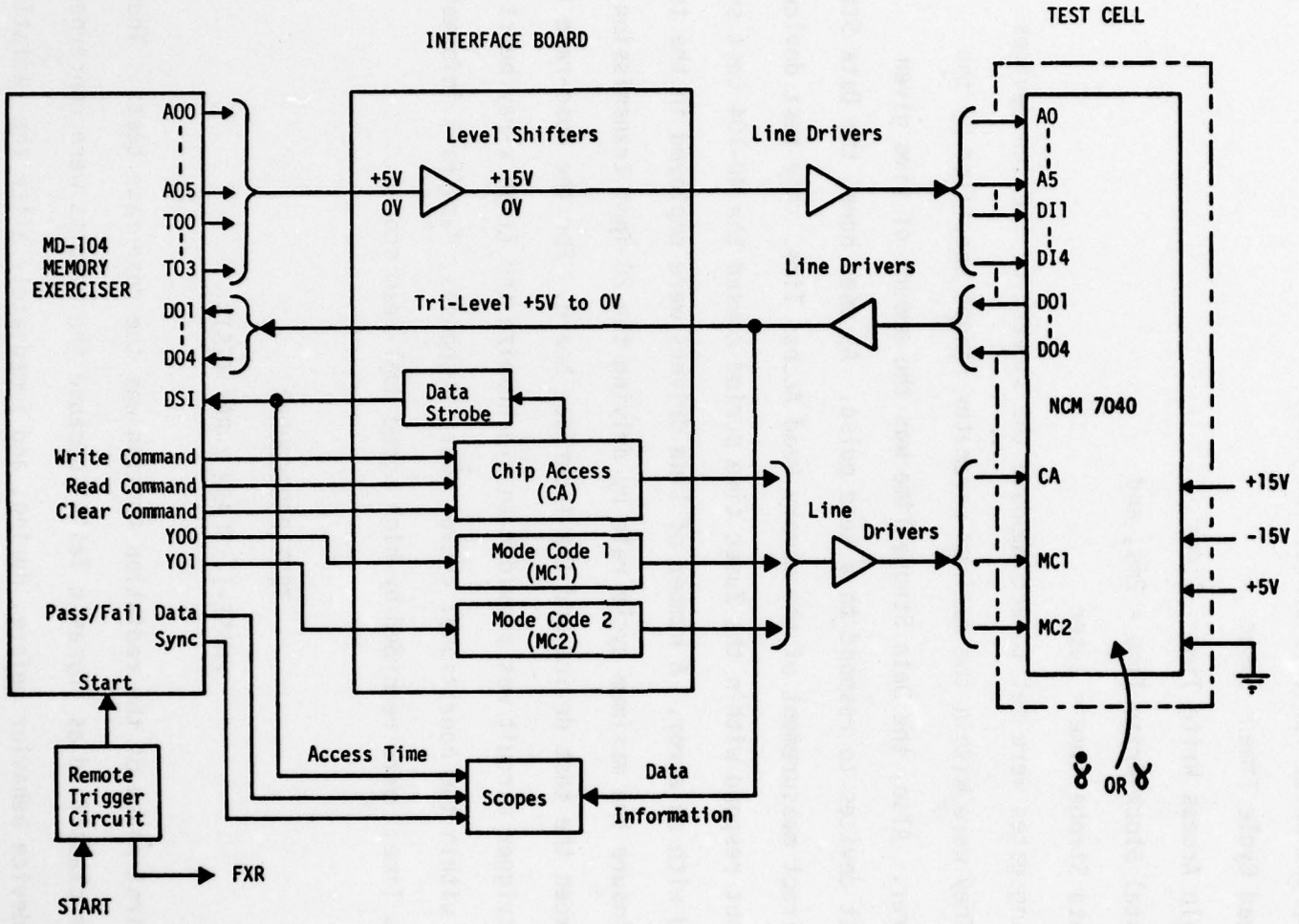


Figure 2. Radiation Test Setup for the Nitron 64 by 4 Bit Word MNOS EAROM Array No. (NCM 7040).

The board also provides adjustable controls over the timing and the pulse widths of the memory gating signals. Some of the major timing parameters provided by the setup for this evaluation were:

(1) Read Cycle Time = 5μsec

(2) Chip Access Write Time = 1.4ms

(3) Total Block Write Time = 2ms, and

(4) Data Strobe Time = 2μsec

These timing gates were set to accommodate the slowest of the ten devices tested. They were within the maximum parameter ranges specified by the manufacturer. Also, the Data Strobe Time was the amount of time given to the test devices to respond to a Read pulse. As used here, the Data Strobe is an indirect measurement of the memory Read Access Time. Any test device that did not respond within the 2μsec time period caused the MD-104 test system to respond with an error. A number of line drivers were employed in the test setup to insure the maximum cycle rate by driving the 20-foot transmission lines between the test device and the interface board. For the dose-rate tests, a remote trigger circuit was provided to synchronize the flash x-ray burst with any point within the operational cycle. Data responses, Pass/Fail information and Access Times were recorded by high speed dual-beam scopes.

TEST PROCEDURES

PHASE-I, FLASH X-RAY TESTS

The first phase of the radiation testing was the dose-rate tests. These tests were classified as "Dynamic Tests" because the results were concerned with the device behavior <u>before</u>, <u>during</u>, and <u>immediately after</u> the radiation burst. The type of tests fell into three general areas, these were: (1) the <u>Operational Disturb</u> Tests, (2) the <u>Survival</u> Tests, and (3) the <u>Recovery</u> Tests.

(1) The Operational Disturb Tests

The first series of transient tests was the Operational Disturb Tests. The main objective of these tests was to determine the minimum dose-rate levels which would produce an error in the device response. This test was divided into two groups: (a) the Read Disturb Tests, and (b) the Write Disturb Tests. The dose-rates of interest for these two groups ranged from 10^7 Rad(Si)/sec to 10^{10} Rad(Si)/sec.

(a) The Read Disturb Tests: The Read Disturb was performed first because the memory device was thought to be more sensitive to transient upsets when it was operating in the Read Mode. In this test, the radiation burst was applied in the Read Cycle with the objective of producing errors in the recorded memory responses. The exact test point is illustrated in Figure (3). This test burst point was chosen because it was given the greatest probability of upsetting the Read Cycle at the lowest possible dose-rate. It was applied at the beginning of a data output response for some arbitrarily chosen word. The objective was to determine the lowest dose-rate level which would prevent or delay the memory from being read in the required Access Time.

(b) The Write Disturb Test: The second group under the Disturb Phase was the Write Disturb Test. The objective of this test was to determine the disturb mechanism of a radiation burst which occurs in the Write Cycle. The radiation test points chosen are shown in Figure (4). All three burst points were chosen with the objective of preventing data from being written into the memory. TP2 was considered to be the most damaging, for a successful jam of the Chip Access gate in this mode would prevent an entire block of four data words from being clocked into the memory. Successful jams at TP3 or TP4

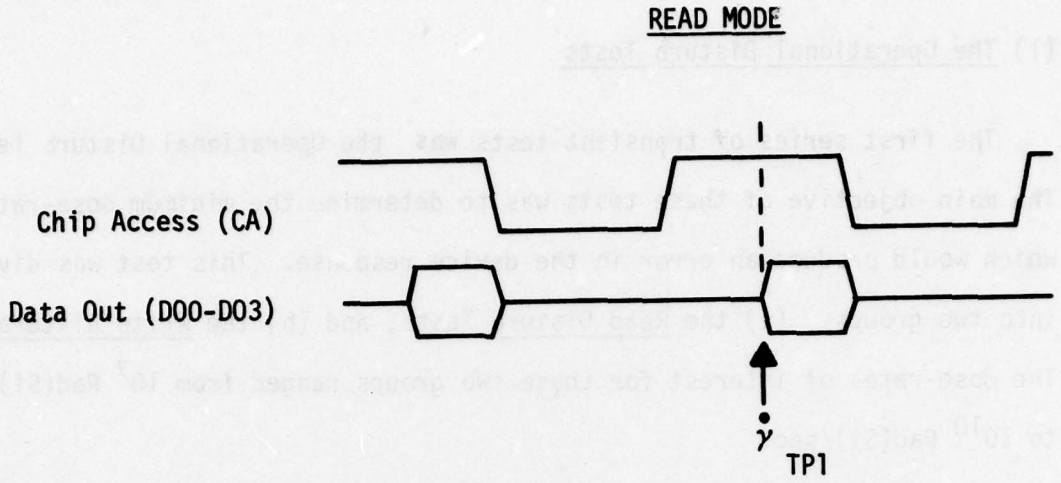


Figure 3. Flash X-ray Test Point in Relation to the Chip Access (CA) Gate and the Data Output Pulses of the Read Mode.

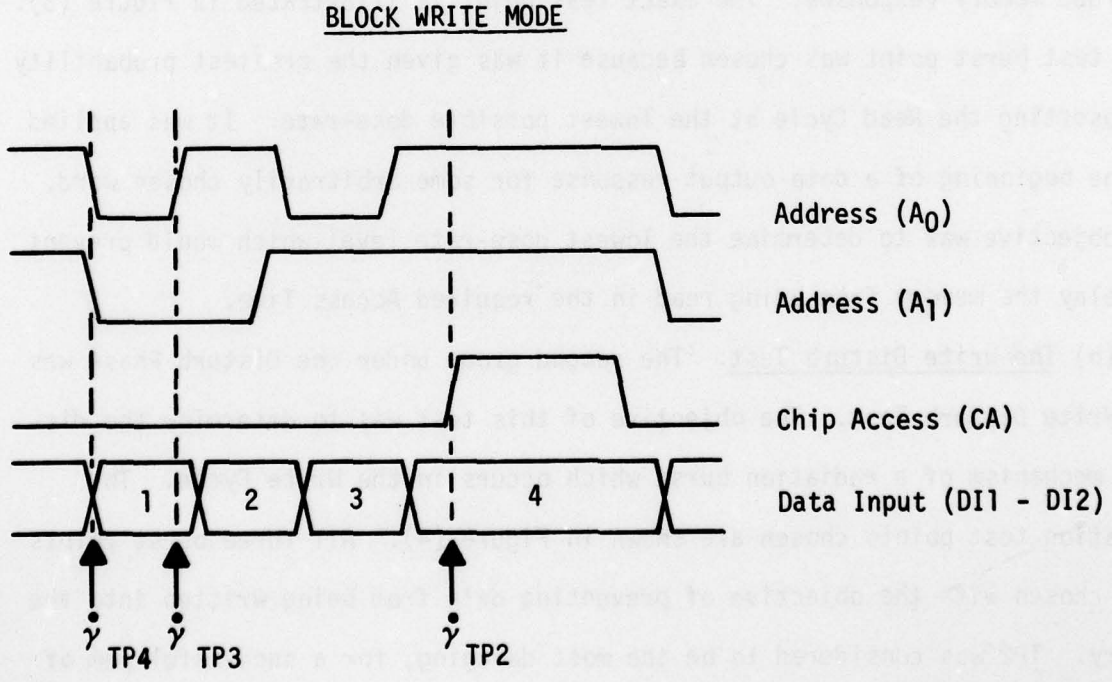


Figure 4. Flash X-ray Radiation Test Points in Relation to a Block Write Mode. Note that this Mode allows for the Sequential Clocking of four Data Words into the Memory with only one Write pulse.

would only prevent one data word from being written. Several Write Blocks (of the sixteen available) were arbitrarily chosen for the tests. From the recorded data, two items were determined: (1) the minimum dose-rate levels which would prevent the chosen Write Blocks from functioning, and (2) the effects on the other Write periods which occur in the same Write Cycle.

(2) Survival and (3) Recovery Tests

The last part of the dose-rate tests was the Survival and Recovery measurements. The primary objectives in these tests were to : (1) determine the maximum dose-rate levels the devices could withstand and still operate after the burst, and (2) determine the recovery time. The dose-rate levels for these tests ranged from 2×10^7 Rad(Si)/sec to levels greater than 1×10^{12} Rad(Si)/sec. For the survival tests, above 2.1×10^{10} Rad(Si)/sec, only the "Pause" or "Wait" period was subjected to radiation. This was because of the limited amount of devices and the probability that the survival level would be higher for the Pause period.

The final step of the dose-rate tests was to measure the Recovery times. This measurement was made throughout the entire Operational Disturb evaluation, and was obtained mainly during the Read Cycles of the devices. From the data, Recoverery Time versus Dose-Rate was obtained.

PHASE-II, Co-60 TESTS

The second major phase of the radiation testing was the total dose tests. This series was composed of three types of tests, each type representing an operational condition of the device. These were:

(1) the Clear/Write/Read Cycle test

(2) the Read Only Cycle test, and

(3) the Pause test.

The first two tests were classified as Dynamic and the last test was Static. The Dynamic tests were concerned with the device behavior before, during and immediately after the radiation. The Static tests were concerned with device behavior directly before and after a specified level of exposure.

The Clear/Write/Read Cycle Test

In this test, the memory device was continuously cycled through all of its operational modes (at the maximum rate) while being irradiated. In the meantime, the data output from the memory device along with the Read Access Time was continuously monitored. The changes in Access Time were recorded during the test. The test was continued until the data output signals no longer showed the correct test patterns. From the results, the total dose that the test device could withstand while operating under a maximum stress condition was known. Also, the Read Access Time as a function of total dose was plotted. Note that this test (of the three presented) was considered to be the "Worst-Case."

The Read Only Cycle Test

This test was also classified as a dynamic test and is similar to Test #1. The only difference is that the memory device was being continuously read while being irradiated. The same parameters were recorded and plotted.

The stress conditions while under radiation for this test were less severe than the conditions in Test Setup #1. As a result, the total dose absorbed before a Read error occurs should be greater than in Test #1.

The Pause Only Test

This was the Static test. The test device was only subjected to radiation during the Pause or Wait period of operation. No Clear, Write, or Read pulse was applied during irradiation. However, all other D.C. voltages were present. Again, as in the previous two tests, the total absorbed dose for Read errors was recorded and the Read Access Time as a function of total dose was plotted. The total dose failure level from this test should correlate approximately with the Pause Mode Survival Test performed in the dose-rate tests.

TEST RESULTS

PHASE-I, FLASH X-RAY

(1) Operational Disturb Tests

All of the Operational Disturb Tests were performed in a Febetron 705 2 MeV Flash X-ray environment (X-ray Mode), using a 20 nsec. radiation pulse. The results are given below:

(a) Read Disturb Upsets: Transient radiation upsets were recorded in the test device's Read Mode at dose-rate levels as low as: 2.0×10^7 Rad (Si)/sec. The lowest levels of upset occurred when the radiation burst was

applied at the beginning of a Logic "1" Data Output response. For Data Output responses of Logic "0", a dose-rate level of approximately 1×10^8 Rad (Si)/sec was needed for an upset. To illustrate these types of upsets, the results of two Read Disturb dose-rate tests are presented below in Figures 5 through 7.

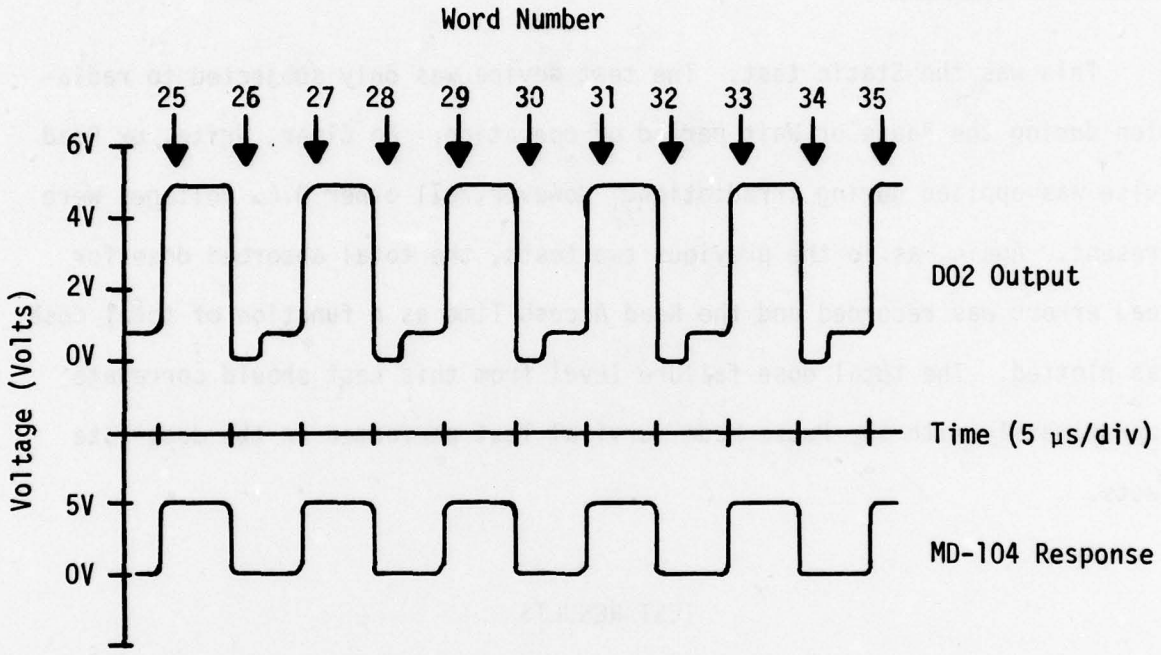


Figure 5. Pre-radiation Data taken on Test Device NCM 7040 EAROM No. 7 (Lot No. 7604-1113440). Top Trace: "Checkerboard" Output Response via Data Output Line DO2 for Words No. 25 through 35. Bottom Trace: Macrodata Response to the above DO2 Output Line.

Figure (5) above, illustrates the test method used to record and evaluate the dose-rate responses in the Operational Disturb Tests. The top trace shows a section of the memory readout (a checkerboard pattern) via one of the Data Output Lines. The bottom trace shows the simultaneous Macrodata response to the above data out. Both responses are correct for the stored pattern. In a like manner, three other dual-beam scopes are used for the other data lines.

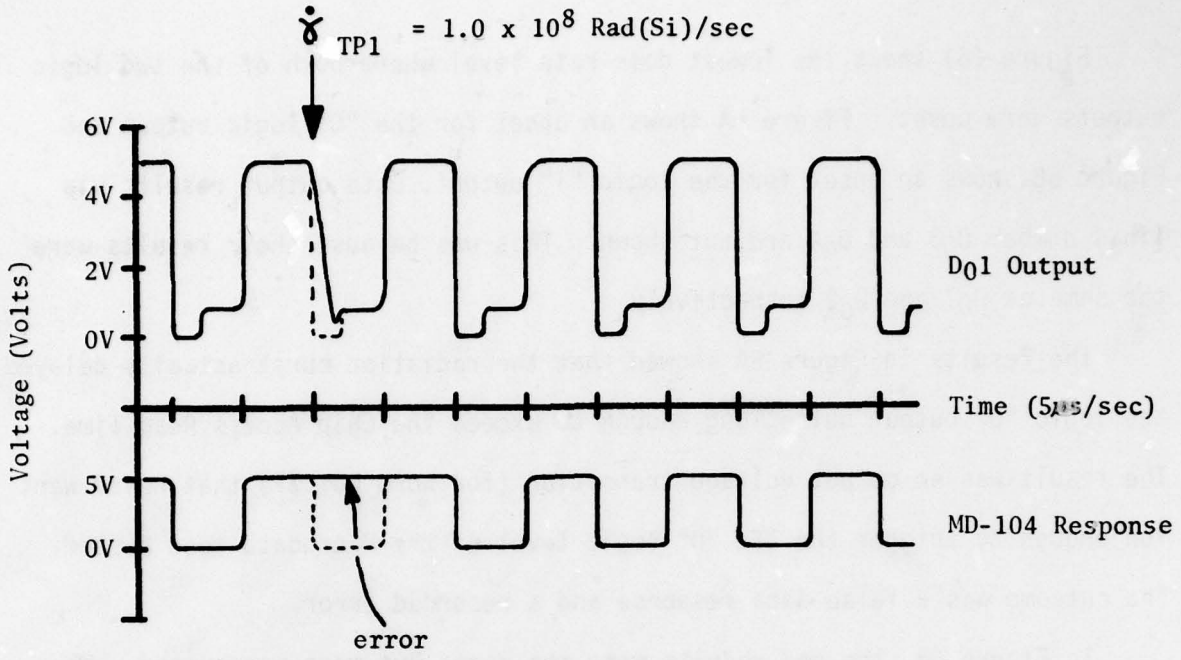
Figure (6) shows the lowest dose-rate level where both of the two logic outputs were upset. Figure 6A shows an upset for the "0" logic output and Figure 6B shows an upset for the logic "1" output. Data output results via lines number $D_0 3$ and $D_0 4$ are not shown. This was because their results were the same as $D_0 1$ and $D_0 2$ respectively.

The results in Figure 6A showed that the radiation burst actually delayed the logic "0" output pulse long enough to exceed the Chip Access Read Time. The result was an output voltage transition (for Word No. 27) that never went low enough to trigger the TTL "0" logic level of the Macrodata test system. The outcome was a false data response and a recorded error.

In Figure 6B, the end results were the same, but more pronounced. When the burst hit the start of the logic "1" output, the resulting response never (during the entire Read Cycle) reached the required level to correctly activate the test system's logic "1" level. As a result, an error was again recorded.

Figure (7) presents the same type of information as shown in Figure (6), with one exception. The applied radiation burst was set at the highest level available in the X-ray Mode. The results were predictable. Upset errors were recorded in more than one Read cycle. Figure 7A shows that two Read cycles were affected. These were the word being read during the burst and the word being read immediately after the burst. Figure 7B shows the worst case, that is, when the radiation burst hits at the start of a logic "1" output. For this situation, three Read cycles were affected, the one during the burst, and the following two words. The result was an error period or Recovery Time of approximately 15 μs.

These error periods or Recovery Times recorded in the above Read Disturb



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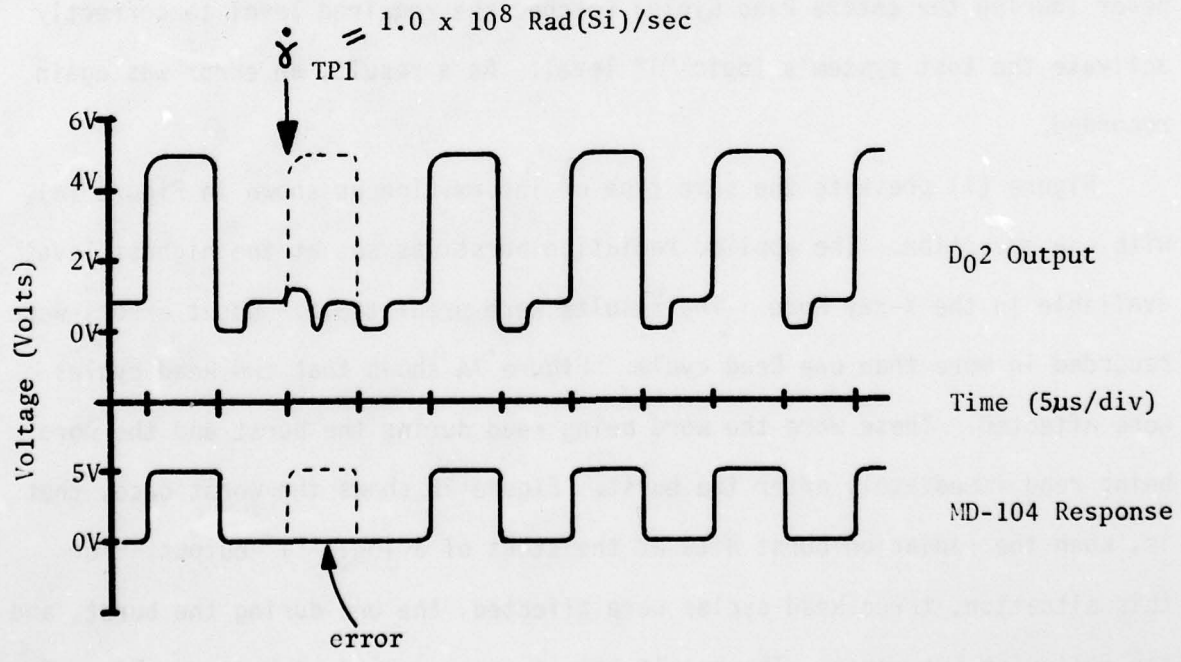

(B)

Figure 6. Transient Radiation Response for Read Disturb Test taken at the Dose-Rate level of 1.0 x 10^8 Rad(Si)/sec. Test Device: NCM 7040 EAROM No. 7 (Lot No. 7604-1113440). Responses: Checkerboard Readout for memory words No. 25 to 35 via Data Lines D01 and D02. Total Dose delivered during burst = 2.0 Rad(Si).

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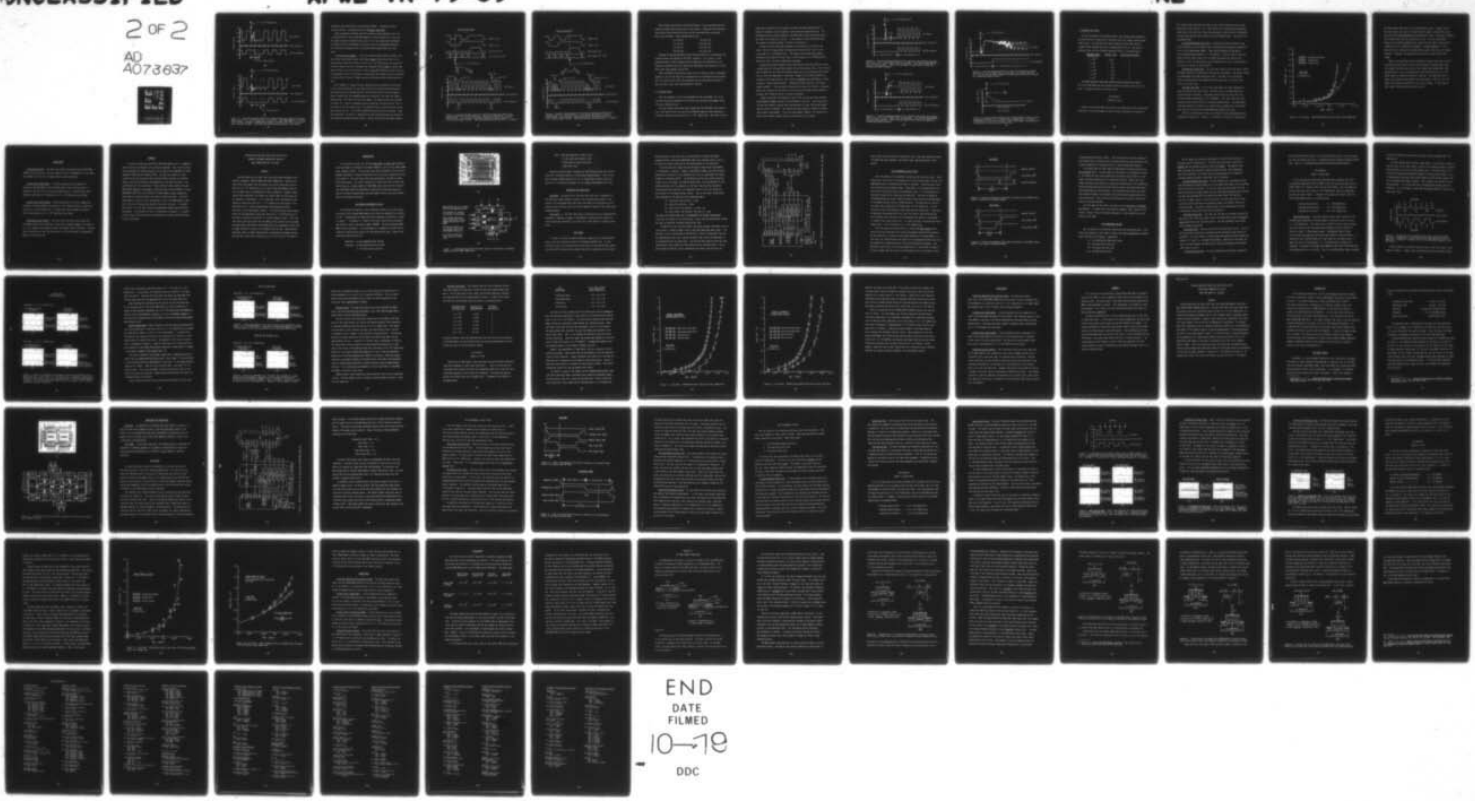

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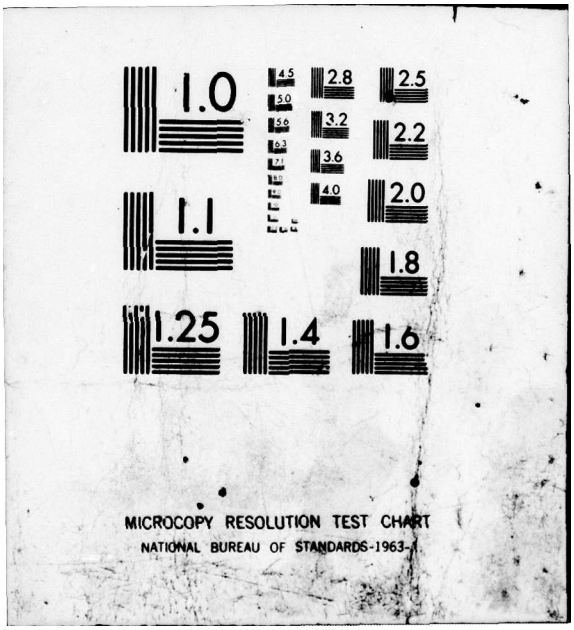
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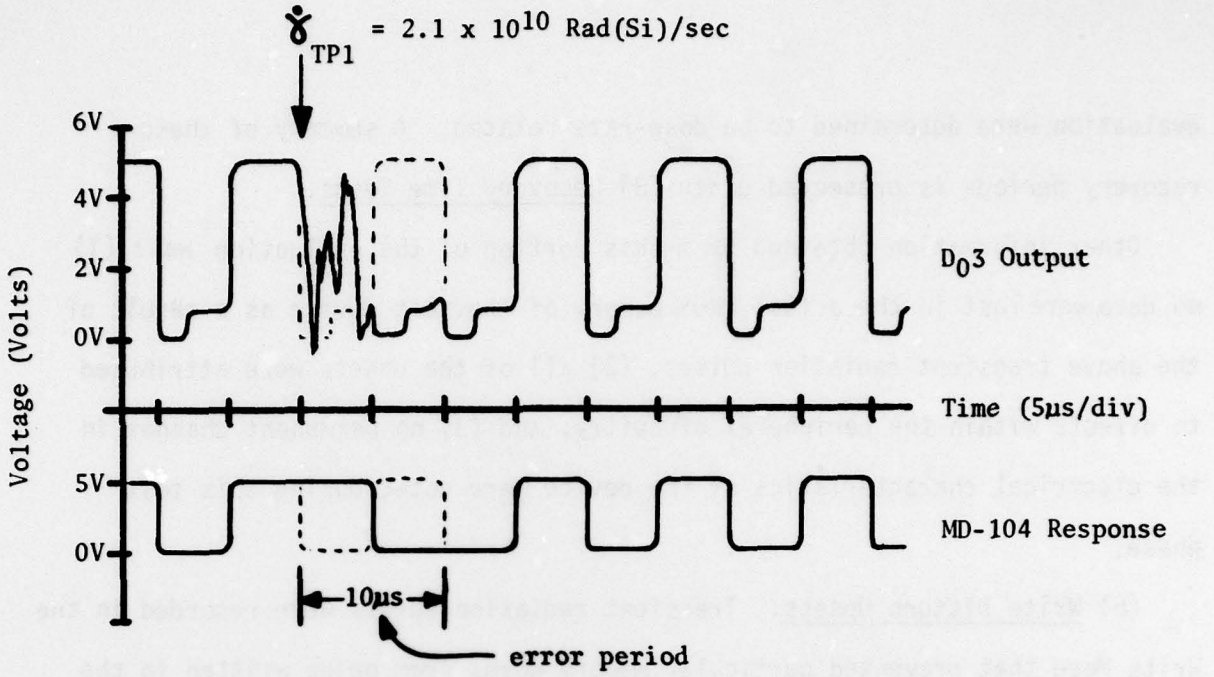
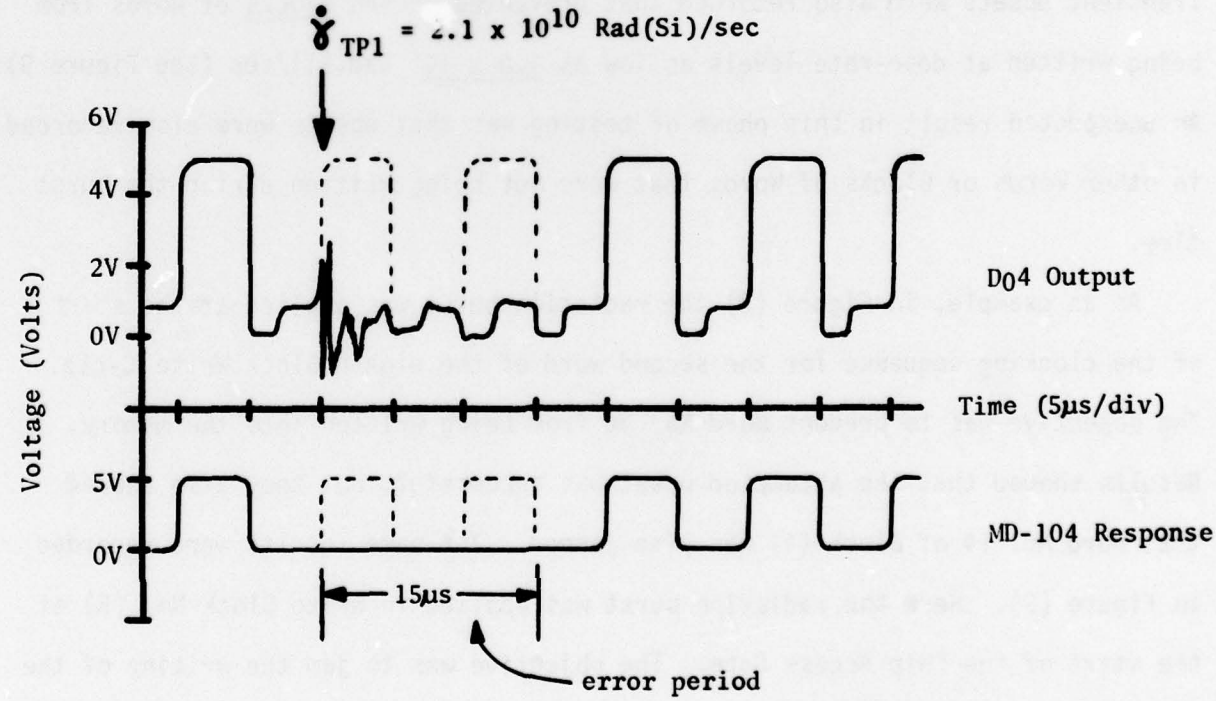


(A)



(B)

Figure 7. Transient Radiation Response for Read Disturb Test taken at the Dose-Rate level of 2.1 x 10^{10} Rad(Si)/sec. Test Device: NCM 7040 EAROM No. 3 (Lot No. 7604-1111440). Responses: Checkerboard Readout for Memory Words No. 5 to 15 via Data Lines D03 and D04. Total Dose delivered during the burst = 420 Rad(Si).

evaluation were determined to be dose-rate related. A summary of these recovery periods is presented under (3) Recovery Time Tests.

Other information obtained from this portion of the evaluation was: (1) no data were lost in the actual MNOS memory of the test device as a result of the above transient radiation pulses, (2) all of the upsets were attributed to effects within the peripheral circuitry, and (3) no permanent changes in the electrical characteristics of the device were noted during this test phase.

(b) Write Disturb Upsets: Transient radiation upsets were recorded in the Write Mode that prevented particular memory words from being written in the test device at dose-rate levels as low as 2.5×10^7 Rad(Si)/sec (See Figure 8). Transient upsets were also recorded that prevented chosen blocks of words from being written at dose-rate levels as low as 4.0×10^7 Rad(Si)/sec (See Figure 9). An unexpected result in this phase of testing was that upsets were also recorded in other Words or Blocks of Words that were not being written during the burst time.

As an example, in Figure (8) the radiation burst was applied at the start of the clocking sequence for the second word of the eighth Block Write Cycle. The objective was to prevent Word No. 30 from being written into the memory. Results showed that the attempted upset was successful; but they also showed that Word No. 14 of Block (4) was also jammed. The same results were recorded in Figure (9). Here the radiation burst was applied in Write Block No. (8) at the start of the Chip Access Gate. The objective was to jam the writing of the entire Block No. (8). The results showed that two blocks were affected. These were Block Nos. (4) and (8). Repeating the test with Write Block (4) being hit by radiation produced the same results. Blocks (4) and (8) were again jammed.

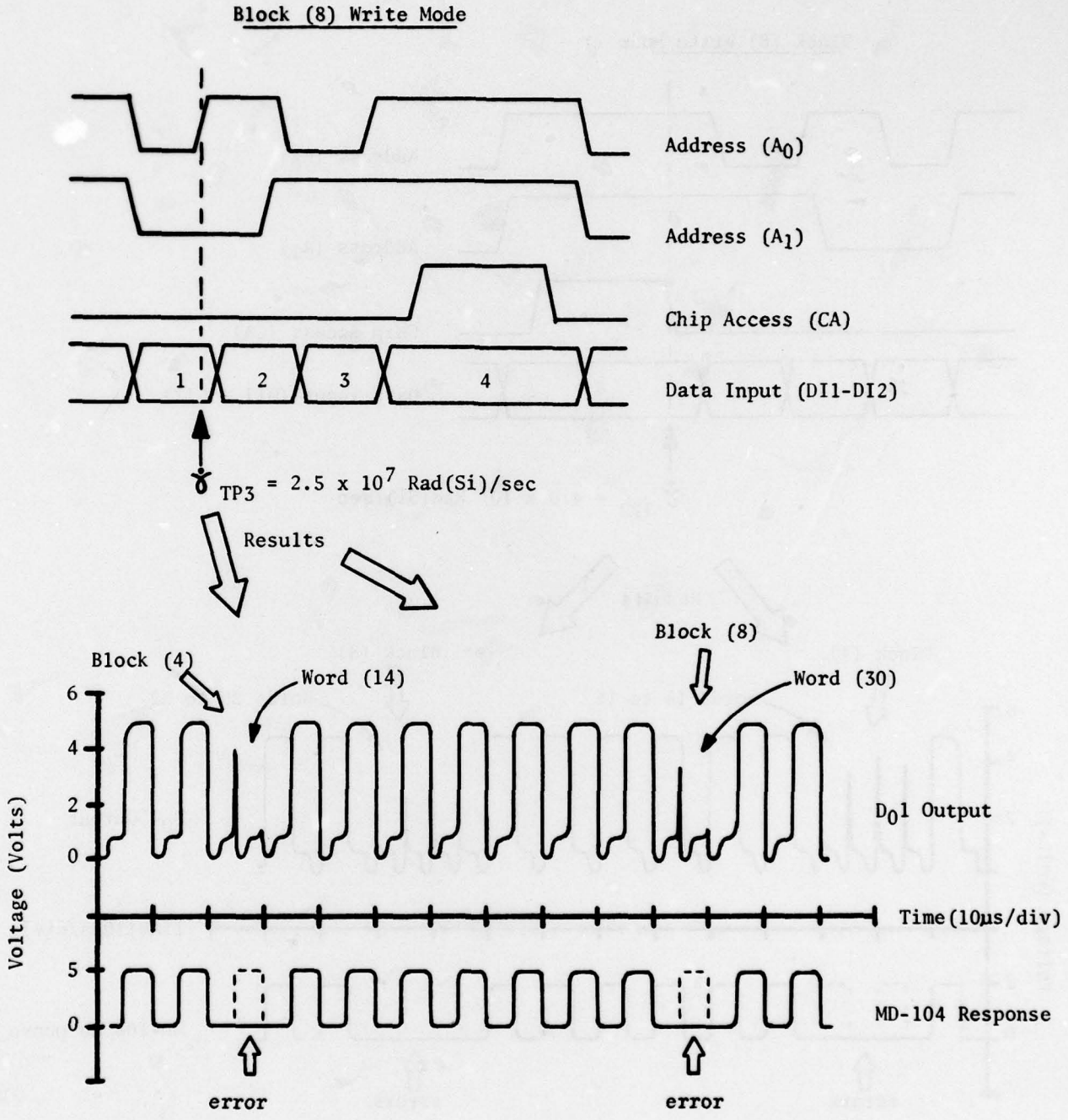


Figure 8. Transient Radiation Results for the Write Disturb Test taken at the Dose-Rate level of 2.5 x 10^7 Rad(Si)/sec. Test Device: NCM 7040 No. 5 (Lot No. 7604-1113440). Lower Response: Checkerboard Readout for Memory Words No. 10 to 34 via Data Output Line $D_0$1. Total Dose delivered during the Burst = 0.5 Rad(Si).

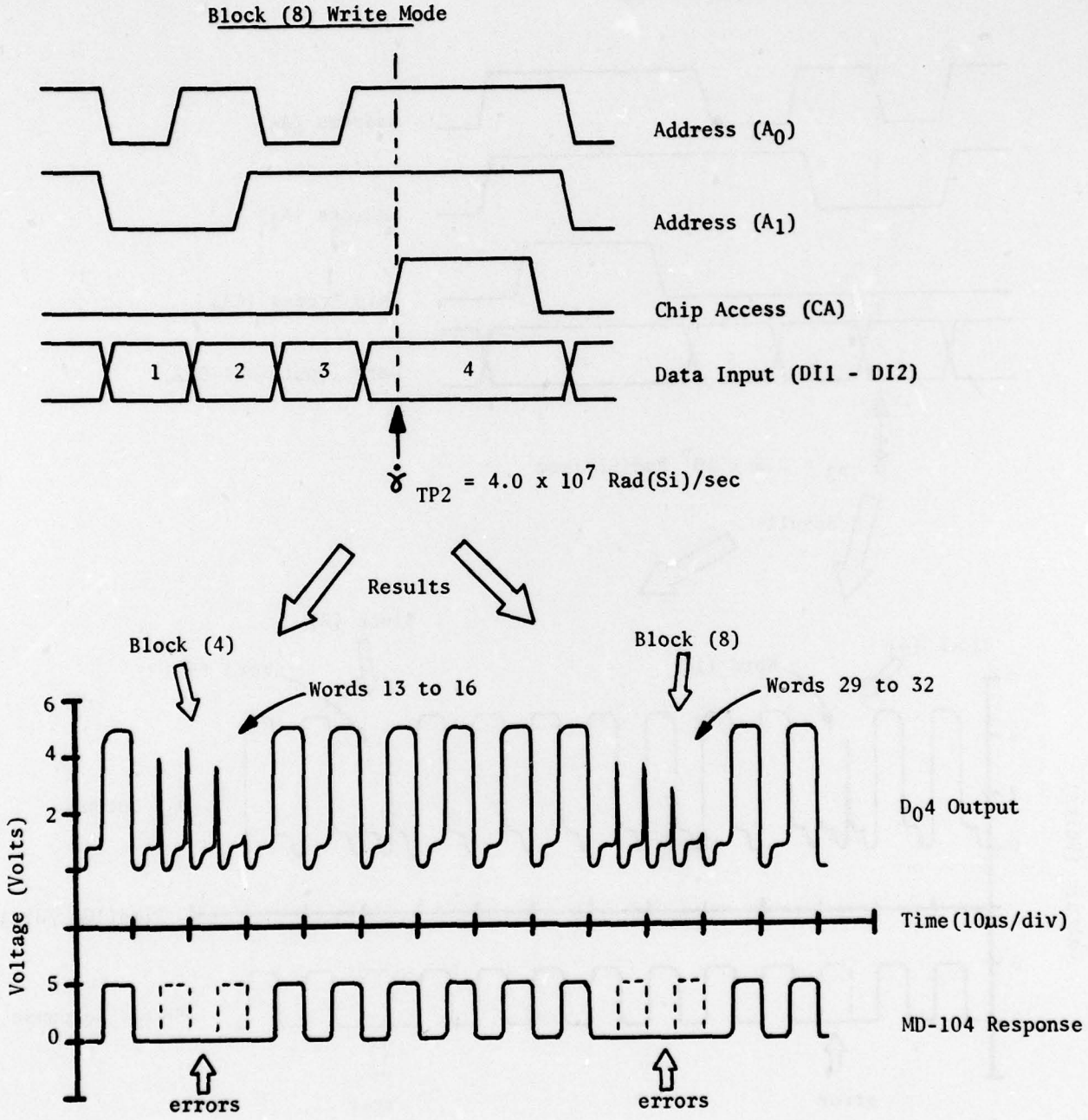


Figure 9. Transient Radiation Results for the Write Disturb Test taken at the Dose-Rate level of 4 x 10^7 Rad(Si)/sec. Test Device: NCM 7040 No. 6 (Lot No. 7604-1113440). Lower Responses: Checkerboard Readout for Memory Words No. 11 to 35 via Data Output Line D_04. Total Dose delivered during the Burst = 0.8 Rad(Si).

After further testing with other Write Blocks, it was concluded that the radiation upsets would always occur in two blocks. These were the particular block being written during the burst and an associated block (no matter when it was written). These related blocks are:

(1) and (5)	(9) and (13)
(2) and (6)	(10) and (14)
(3) and (7)	(11) and (15)
(4) and (8)	(12) and (16)

Although no data are presented, Write Disturbs were also recorded when the radiation burst was applied at TP4 (Ref. Figure 4). As a result, it was determined that a Write Disturb could be obtained on the NCM 7040 for any transient radiation pulse (of significant magnitude) being applied in a Block Write time frame between TP2 and TP4.

Other information worth noting from this test phase was that no permanent changes in any of the electrical characteristics or parameters were recorded. Also, no Clear Disturb Tests were performed on the test devices because of the long Block Clear Time (approximately 1 second).

(2) Survival Tests

With the exception of one test performed in the X-ray Mode, all of the Survival Tests were performed in the Flash X-ray (E-beam) environment using a 50 nsec radiation burst.

The main results from these tests showed that the NCM 7040, while operating in the Pause Period, can survive and operate properly after absorbing a transient radiation burst as high as 7×10^{11} Rad(Si)/sec. Note that survival

means that the device can be cleared, written, and read properly after a period of recovery, with no changes in the electrical characteristics. The minimum period of recovery needed for the NCM 7040 at the highest dose-rates was found to be from 20 to 25 μsec. A few samples of tests performed under this phase are presented below in Figures 10 through 13.

Figures 10 and 11 show the responses of two devices that actually survived. The first figure shows the response at the high test level in the X-ray mode (2.1×10^{10} Rad(Si)/sec). The second figure shows the response recorded at the highest survival level in the E-beam (7.3×10^{11} Rad(Si)/sec). Above this level, no device completely recovered.

Analyzing the above responses shows that shortly after the radiation burst, a sudden positive voltage charge appears on the data output lines. This positive charge remains on the lines for periods ranging up to a millisecond (See Figure 13), or until the Read Mode is activated. Because of the PMOS and MNOS construction of the test devices, this charging phenomena was attributed to "Photocurrents," "Space-charge Buildup," "Secondary Electron Capture," and "Photovoltaic Effects." This particular voltage build-up does not appear to adversely affect the operation of the device, for as soon as the Read gating sequence is started, the voltage build-up is quickly discharged.

Figure 12 presents the response of one of the test devices that suffered some permanent damage in parts of the peripheral circuitry. Total failure was not the case however, because after approximately 80 μsec, the device showed partial signs of recovery. The recovery was good enough to detect the proper data stored in the memory. It was not good enough, however, to transmit this data at the correct voltage levels to the external test systems.

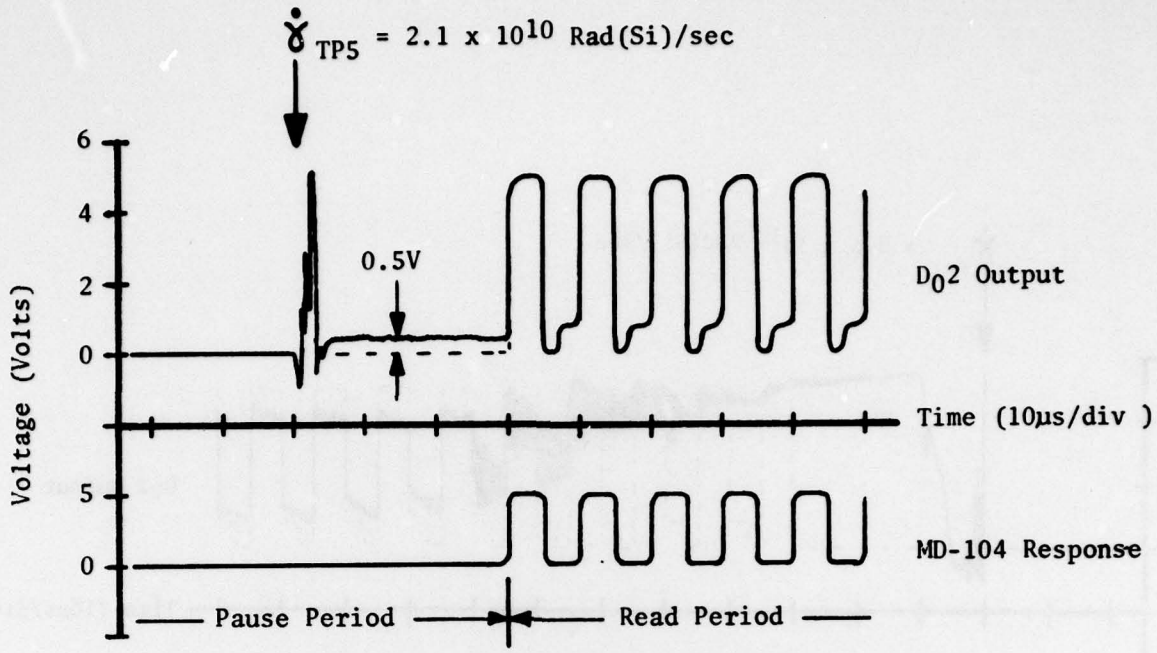


Figure 10. Transient Radiation Results for a Survival Test taken at the Dose-Rate level of 2.1 x 10^{10} Rad(Si)/sec (X-ray Mode). Test Device: NCM 7040 No. 3 (Lot No. 7604-1111440). Trace: Trailing edge of Pause Period followed by a Checkerboard Memory Readout.

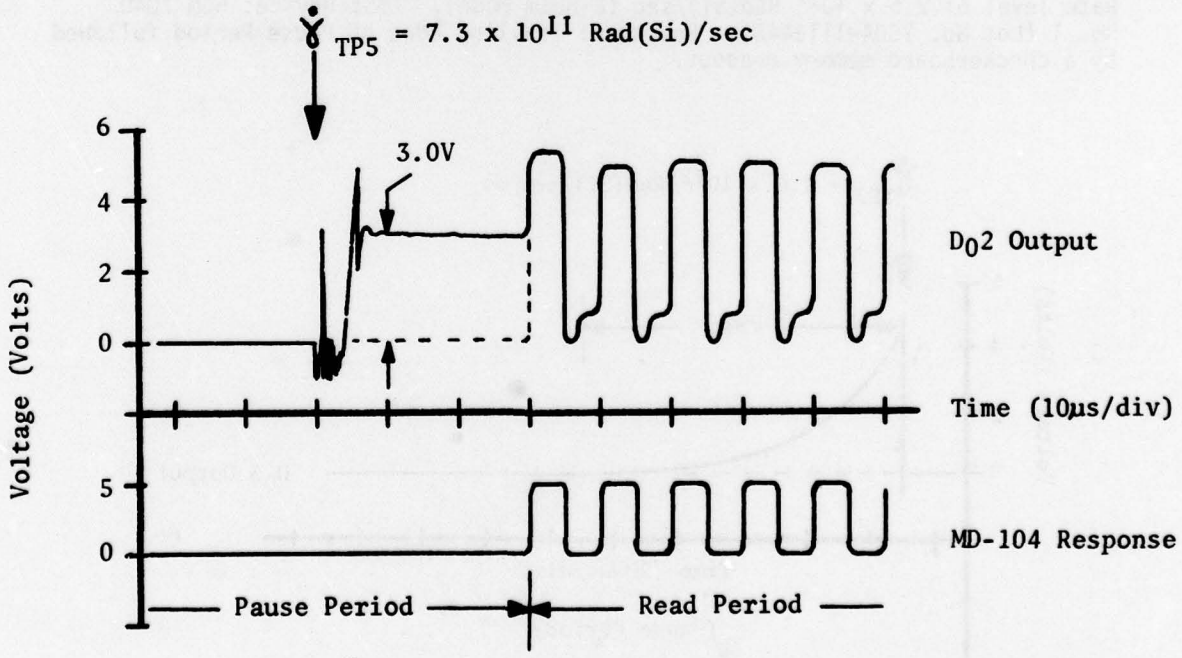


Figure 11. Transient Radiation Results for a Survival Test taken at the Dose-Rate level of 7.3 x 10^{11} Rad(Si)/sec (E-beam Mode). Test Device: NCM 7040 No. 4 (Lot No. 7604-1113440). Trace: Trailing edge of Pause Period followed by a Checkerboard Memory Readout.

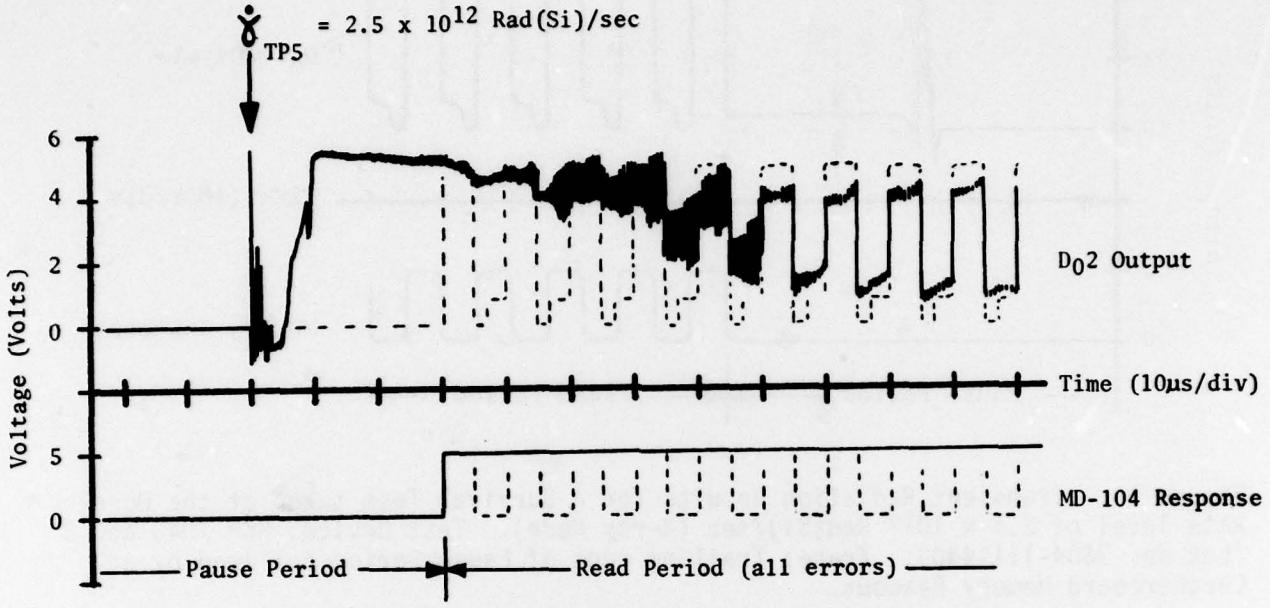


Figure 12. Transient Radiation Results for a Survival Test taken at the Dose-Rate level of 2.5 x 10^{12} Rad(Si)/sec (E-beam Mode). Test Device: NCM 7040 No. 1 (Lot No. 7604-1113440). Response: Trailing edge of Pause Period followed by a checkerboard memory readout.

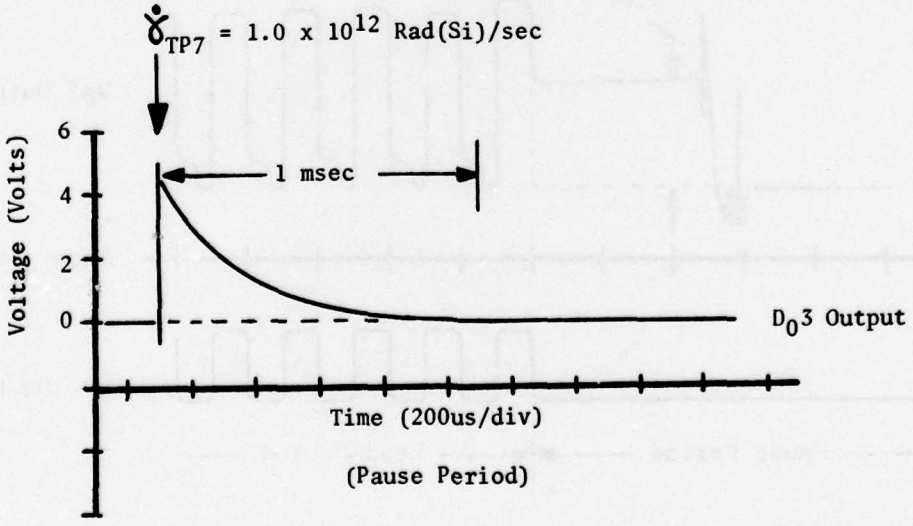


Figure 13. Transient Radiation Results for a complete Recovery Time test taken at the Dose-Rate level of 1 x 10^{12} Rad(Si)/sec (E-beam Mode). Test Device: NCM 7040 No. 6 (Lot No. 7604-1113440). Trace: Trailing edge of discharge curve resulting from a high dose-rate radiation pulse.

(3) Recovery Time Tests

In this evaluation, the recovery time is the minimum period needed by the test device to recoup from a radiation burst and resume a normal operational cycle. For the dose-rate levels tested, the NCM 7040 requires recovery times ranging from 0.2μs to approximately 25 μs. The table of Recovery Times for the different Dose-Rate levels is presented below:

Dose-Rate Level (Rad(Si)/sec)	Recovery Time	Read Cycles Affected
2×10^7	≃ 0.2μs	1
1×10^8	≃ 5μs	1
1×10^9	≃ 10μs	2
1×10^{10}	≃ 15μs	3
1×10^{11}	≃ 20μs	4
7×10^{11}	≃ 25μs	5

The above Recovery Times were obtained when the device was operating in the Read Mode and the radiation burst was applied at the start of a logic "1" output from one of the data lines.

TEST RESULTS

PHASE-II, Co-60

Three of the ten NCM 7040 test devices were subjected to total dose tests performed in Co-60 environment located at Sandia Laboratories, New Mexico.

All three devices were from the same Lot (No. 7604-1111440) and had similar Read Access Times (approx. 1μs). Each device was irradiated while operating under one of the three test conditions presented in the Co-60 Test Procedures. The dose-rate applied during these tests was 28 Rad(Si)/sec. The results are presented below:

The Clear/Write/Read Cycle Test: Following the steps outlined in the Test procedures, the first device was irradiated while operating continously in all of its operational modes. Total failure occurred in the device after absorbing approximately 1.7×10^4 Rad(Si). Total failure is the point where the data output signals are no longer presenting the correct test patterns. Also, the Read Access Time increased from 1 μsec to approximately 2.4 μsec as a result of the radiation.

The Read Only Cycle Test: This test was similar to the one above, except the memory device was continuously Read during irradiation. The devices failed at approximately the same total dose level. This was 1.75×10^4 Rad(Si). Again, the Read Access Time showed about the same rate of increase, from 1.05 μsec to 2.25 μsec.

The Pause Only Test: In this test, the device was only subjected to radiation during the Pause period. No Clear, Write, or Read pulses were applied during irradiation. Operational failure did not occur until the device absorbed approximately 3.8×10^4Rad(Si). This dose level was twice as great as the failure levels of the two preceding tests. The Read Access Time also showed an increase (at a slower rate), ranging from a preirradiation value of 1.07 μsec to a postirradiation value of 2.48 μsec.

Plots of the Read Access Time as a function of total absorbed dose are Presented in Figure (14). Below 1×10^4 Rad(Si), the rates of increase for

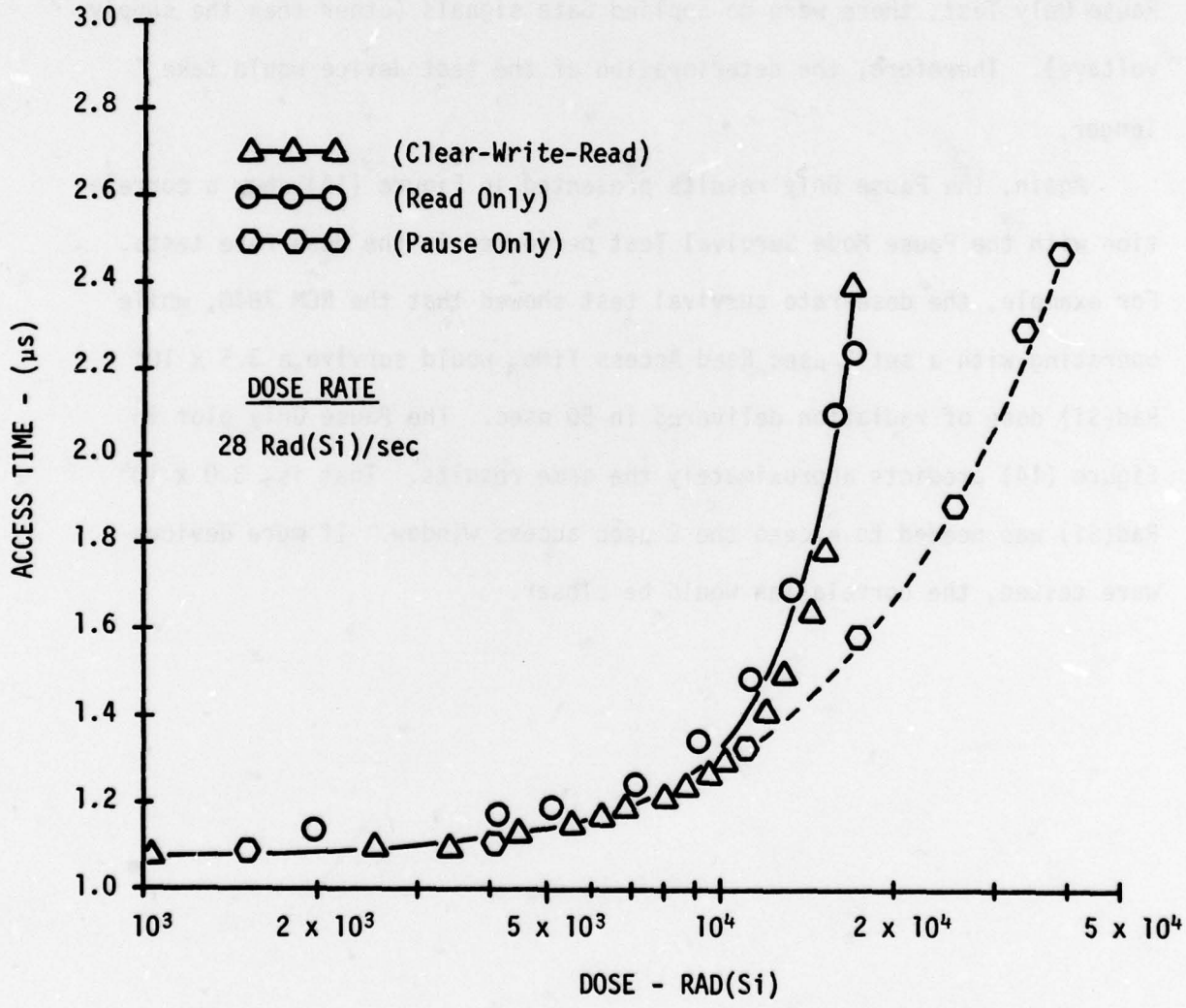


Figure 14. Co-60 Data. NCM 7040 Read Access Time versus Total Gamma Dose.

all three access times were low and approximately equal. However, above this dose level, the rates of increase showed a marked acceleration, especially for the Clear/Write/Read and the Read Only tests. The rate of increase for the Pause Only test was significantly less. This was predictable because of the known phenomenon that states that the rate of deterioration of MOS devices in a radiation enviroment is voltage dependent. In the Pause Only Test, there were no applied Gate signals (other than the supply voltage). Therefore, the deterioration of the test device would take longer.

Again, the Pause Only results presented in Figure (14) show a correlation with the Pause Mode Survival Test performed in the dose-rate tests. For example, the dose-rate survival test showed that the NCM 7040, while operating with a set 2 μsec Read Access Time, would survive a 3.5×10^4 Rad(Si) dose of radiation delivered in 50 nsec. The Pause Only plot in Figure (14) predicts approximately the same results. That is, 3.0×10^4 Rad(Si) was needed to exceed the 2 μsec access window. If more devices were tested, the correlation would be closer.

CONCLUSIONS

Survivability Level. The dose-rate results have shown that the NCM 7040 EAROM array can survive a 50 nsec radiation burst of 35 KRad(Si), in an E-beam environment, with no loss of memory data or device operation.

Disturb Level (Read Mode). A disturb mechanism can be temporarily induced in the Read Mode of the NCM 7040 array if the radiation burst is applied at the exact start of the Data Output pulses. The dose-rate levels needed to generate this interruption are 2×10^7 Rad(Si)/sec and higher.

Disturb Level (Write Mode). Disturb mechanisms can also be temporarily induced in the Write Mode of the devices if the radiation burst is applied at the start of a Write Setup Time. The dose-rate levels needed to generate these interruptions are 2.5×10^7 Rad(Si)/sec and higher.

Accumulating Dose Effects. The Co-60 total dose tests have shown that the memory devices can accumulate a total dose of gamma radiation in excess of 1.5×10^4 Rad(Si) while operating under the maximum stress conditions. Maximum stress conditions are when the test device is cycling through its Operational Modes at the maximum rate.

COMMENTS

It should be noted that the Nitron NCM 7040 EAROM array is a commercial device and was not designed to be radiation hardened. Thus, the low radiation susceptibility levels measured in this report were comparable to other commercial PMOS devices tested at AFWL. The one real surprise in this evaluation was the discovery that two Write Blocks (written at different times), could be interrupted simultaneously by one radiation burst. The significance of this occurrence is that a block of words written into the MNOS memory before or even after a radiation burst can be affected. If this phenomenon turns out to be universal in other memory arrays (especially those that are radiation hard), the results could be serious. From this experimenter's point of view, the problem is not in the MNOS memory itself, but in the circuit design and layout of the Write circuitry. It appears that there is a cross over effect being generated between one Write Block and another. The solution (if this is considered a problem), is to design a Write circuit that electrically and physically isolates each Write Block from all the others.

IONIZING DOSE RATE AND TOTAL DOSE TESTS ON THE GENERAL INSTRUMENT NONVOLATILE 4096-BIT MNOS EAROM ARRAY NO. (ER 3400)

ABSTRACT

Ionizing dose-rate and total dose tests have been performed on the General Instrument 4096-bit MNOS (ER 3400) EAROM array. Results from these tests have shown that the devices can survive dose-rate levels as high as 9.0×10^{11} Rad(Si)/sec (in a 2 MeV E-beam environment) with no loss of memory data or degradation in device operation. However, under certain test conditions, the "Read" and "Write" modes of the arrays can be temporarily interrupted. In the Read mode, this interruption can be induced at dose-rate levels of 1.1×10^{8} Rad(Si)/sec and higher if the radiation burst is applied approximately 200 nanoseconds before the start of the "Data Output" signals. In the Write mode, disturb mechanisms can be generated at dose-rate levels of 3.1×10^{8} Rad(Si)/sec if the burst is applied at the start of a "Write Enable" signal. Also, the total dose tests have shown that the memory arrays (while cycling through the operational Read mode at the maximum rate) can accumulate a total dose of gamma radiation in excess of 15 kRad(Si) and survive. Under optimum conditions (with no power applied during irradiation) the memory devices survived total dose levels ranging up to 4.0×10^{4} to 6.0×10^{4} Rad(Si).

INTRODUCTION

This evaluation covers the ionizing dose-rate and total dose radiation tests performed on the General Instrument 4096-bit, bulk silicon, MNOS EAROM array labeled ER 3400. The dose-rate tests were performed at the Air Force Weapons Laboratory's Transient Radiation Facility using a Febetron 705 Flash X-ray machine. The total dose tests were performed at the AFWL low dose-rate Co-60 source. The overall objective of these tests was to obtain radiation data on a second commercial PMOS MNOS array which could be incorporated with other baseline information to measure the relative success of special radiation hardened MNOS prototype memory devices now under development at the Weapons Laboratory.

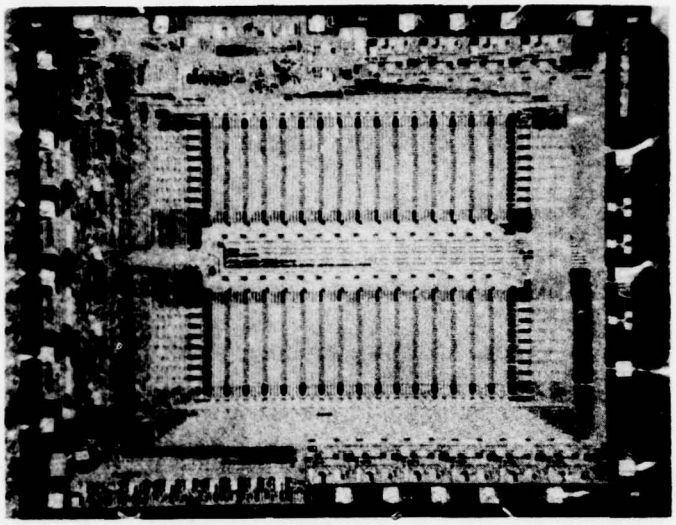
THE GENERAL INSTRUMENT ER 3400

The ER 3400 was chosen for this evaluation because it was the newest and fastest fully decoded MNOS memory array that was commercially available in 1977. A photograph and simplified block diagram of the device is shown in Figure 1. The memory is a 1024 by 4-bit word, electrically alterable, non-volatile, static read-mostly memory (EAROM). The device employs PMOS/MNOS on bulk technology. It was packaged in a standard 22 pin DIP and designed to interface with bipolar TTL with Resistor Pull-ups. Some of the electrical specifications are:

Retention: 10 Year Unpowered Data Storage

Endurance: 10^5 Erase-Write Cycles per Word

2×10^{11} Read Cycles per Word



(A)

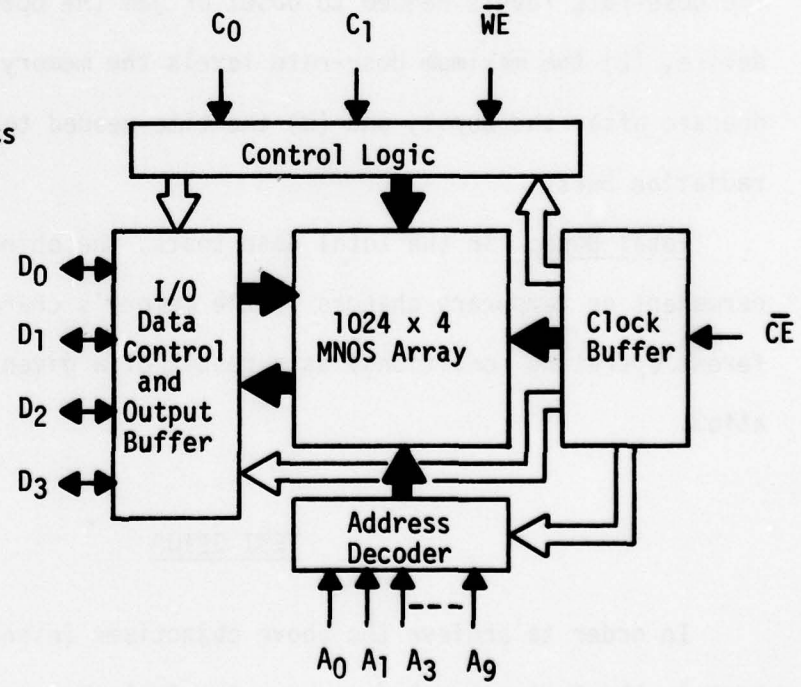
Mode Control C_0 & C_1 selects the desired Operation Mode.

Chip Enable CE, enables the device in each mode.

Write Enable WE allows data to be stored in the memory during the Write Mode.

10-Bit Word Address A_0-A_9, select one of the 1024 Memory Addresses.

D_0 to D_3 are the Data Input and Data Output Pins.



(B)

Figure 1. Photograph and Simplified Block Diagram of the General Instrument ER3400, 4096-bit, MNOS EAROM Array.

Speed: 900 nSec Read Access Time or Less

1.8 μSec Read Cycle Time or Less

10 mSec Word or Block Erase Time

1 mSec Write Time

Basically, the ER 3400 is designed for applications where data must be stored for indefinite periods of time without applied power. A few of the more prominent design features are: (1) a single Word or Block electrical erase, (2) tri-level Data Outputs, and (3) common Input/Output Data Lines.

RADIATION TEST OBJECTIVES

Dose-Rate: The objective of the dose-rate tests was to determine (1) the dose-rate levels needed to upset or jam the operational modes of the device, (2) the maximum dose-rate levels the memory can withstand and still operate after the burst, and (3) the time needed to recover from a particular radiation burst.

Total Dose: In the total dose tests, the objective was to determine the permanent or temporary changes in the memory's characteristics (under different operating conditions) as a result of a given amount of ionizing radiation.

TEST SETUP

In order to achieve the above objectives (especially in the dose-rate tests), the test setup had to have the following capabilities: (1) the ability to place the radiation burst at any point in the desired test cycle, (2) the ability to exercise the memory array at its maximum cycle rate with

the test device in the test cell, (3) the ability to record the memory response before, during and immediately after the radiation burst, and (4) the ability to make a decision on the effectiveness of the radiation.

The radiation test setup that was designed to meet these requirements is illustrated in Figure 2. Shown is the 4096-bit memory test device being electrically exercised in the radiation test cell by a Macrodata LSI tester through an "Interface Board". The Macrodata provided the control functions (Clear, Write, and Read), the address generations, the data patterns to the Interface Board, and the responses to the data returning from the board. The Interface Board provided the adjustable controls over the timing and pulse widths of the memory gating signals. Some of the major timing parameters provided by the setup for this evaluation were:

(1) Read Cycle Time Setting ≃ 3 μSec

(2) Write Time Setting ≃ 2 mSec

(3) Block Erase Time Setting ≃ 11 mSec, and

(4) Data Strobe Time Setting = 400 nSec to 1 μSec

The above timing gates were set to accommodate the longest transmission lines and the slowest of the test devices. Note, that the Data Strobe setting was used to determine the memory Read Access Time.

In addition to the interface board, the setup includes a multipex circuit, line drivers, a remote trigger circuit, and high speed dual-beam scopes. The multiplex circuit (controlled by the MD-104) is used to "time-share" the common Input/Output Data Lines, thereby allowing Clear, Write and Read data to be transmitted over the same lines. Line Drivers were used to drive the long transmission lines between the test device and the interface board. The remote trigger system was used to synchronize the flash x-ray burst to any

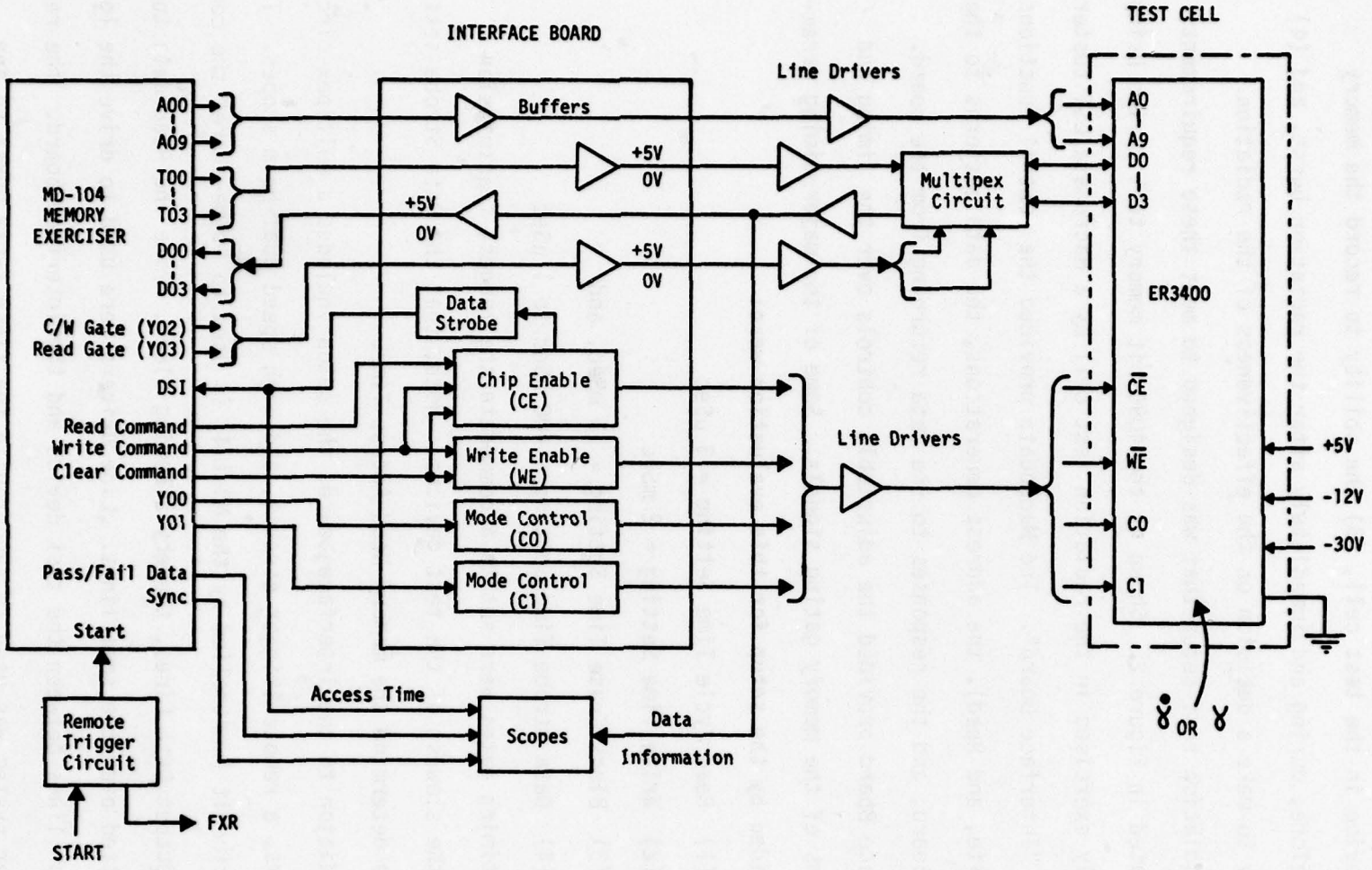


Figure 2. Radiation Test Setup for the General Inst. 1024 x 4 Bit Word MNOS EAROM Array No. (ER 3400).

point within the test device's operational cycle. Dual-beam scopes were used to record the data responses, the access times, and the pass/fail information .

TEST PROCEDURES (FLASH X-RAY)

The first phase of the radiation testing was the dose-rate tests. Under these tests, the results of the behavior of a test device before, during, and immediately after a radiation burst were of interest. These dose-rate tests were divided into two general areas. These were: (1) the Operational Disturb Tests, and (2) the Survival and Recovery Tests. In the Operational or Transient Disturb Tests, there was one objective. This was to determine the minimum dose-rate levels needed to upset or jam the Write and Read Modes of the memory devices during a radiation burst. The dose-rate of interest for these tests ranged from 10^7 Rad(Si)/sec to 10^{11} Rad(Si)/sec. In the Transient Survival and Recovery Tests there were two objectives. These were to determine the maximum dose-rate level the devices could withstand and still operate after the burst, and to determine the length of time needed to recover from a particular burst. In these two tests, the dose-rate levels ranged from 2×10^{10} Rad(Si)/sec to 2×10^{12} Rad(Si)/sec.

The first group of disturb tests was called the Read Disturb Tests. These tests were performed first because the memory devices were thought to be more sensitive to transient upsets when operating in the Read Mode. In this test, the radiation burst was applied in a predetermined Read Cycle with the objective of producing errors in the recorded memory responses. The radiation testing zone for the chosen Read Cycle is illustrated in Figure 3. The zone ranged from the start of a Chip Enable pulse to the middle of the

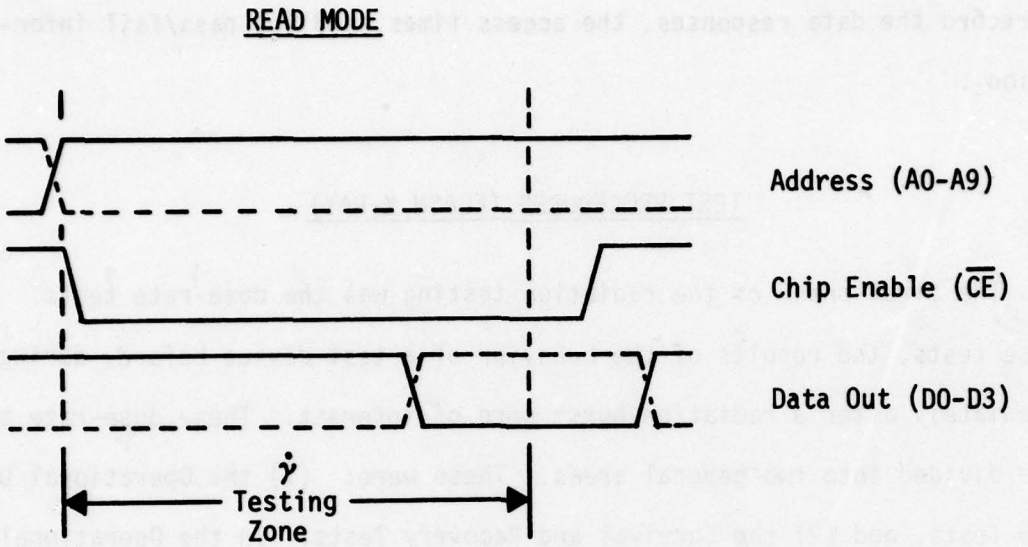


Figure 3. Flash X-ray Radiation Test Zone in Relation to the READ Timing Gates of the General Instrument ER3400.

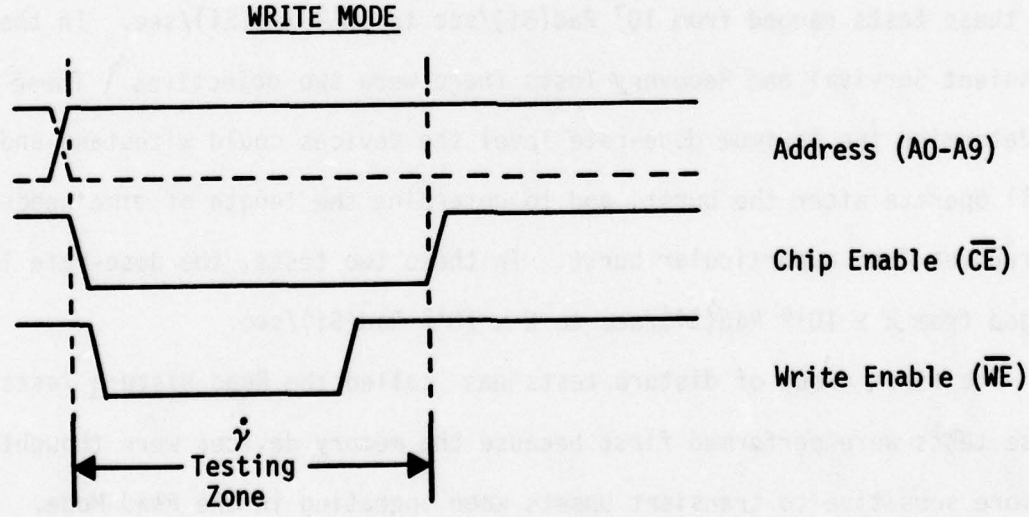


Figure 4. Flash X-ray Radiation Test Zone in Relation to the WRITE Timing Gates of the General Instrument ER3400.

corresponding Data Output signals. This testing zone was chosen because it was believed that a radiation burst hitting within this area would have the highest probability of producing errors in the recorded Data Outputs.

The second group of tests under the Operational Disturb phase was the Write Disturb Tests. The test zone for this phase is illustrated in Figure 4. As shown, the test zone extends over the entire time period of a Chip Enable and Write Enable gate of a chosen Write Cycle. Within this time frame, the point most sensitive to transient radiation was first determined, and the minimum dose-rate level which would prevent the chosen Write Cycle from functioning was then measured. Also monitored during this test were the radiation effects on the other Write Cycles which occurred within this same Write period. Note, that the ER 3400 may have as many as 1024 Write Cycles in one Write Period.

The last phase of the flash x-ray tests was the Survival and Recovery measurements. In these tests, the radiation exposures were limited to the device's "Pause" period of operation because of a high probability of surviving in this mode.

TEST PROCEDURES (CO-60)

The last phase of the radiation testing was the total dose tests. This series was composed of four types of tests, each type representing an operational condition of the device. These were:

(1) the Clear/Write/ Read Cycle test,

(2) the Read Only Cycle test,

(3) the Pause Only test, and

(4) the Passive Only test.

All of these four tests were performed in the AFWL Co-60 source at a low dose-rate of 22 Rad(Si)/sec. The first two tests were classified as Dynamic and the remaining two were classified Static. The Dynamic tests were concerned with the device behavior before, during, and immediately after the radiation. The Static tests were concerned with the behavior directly before and after a specified level of exposure.

Clear/Write/Read Cycle Test: In this dynamic test, the memory devices were continuously cycled through all of the operational modes (at the maximum rate) while being irradiated. At the same time, the data output from the device along with the Read Access Time was continously monitored and recorded. The test was continued until the device failed or until the Data Output was no longer correct. From the results, the total dose that the memory device could withstand while operating under this dynamic stress conition was known. The rate of deterioration is then determined with plots of Read Access Time versus total dose irradiation.

Read Only Cycle Test: This test was the same as the above Clear/Write/Read Cycle Test, with the exception that the memory device would now continuously Read during the radiation period. The same parameters and outputs were recorded and plotted.

Pause Only Test: This was the first of the two Static tests. The test device was only subjected to radiation during the Pause or Wait period of operation. No Clear, Write, or Read pulses were applied during irradiation; however, all other D.C. voltages were present. Again (as in the above two tests) the Data Outputs and Read Access Times were monitored and recorded until device failure.

The Passive Only Test: The test procedures and radiation conditions

for this test were the same as in the above Pause Only test, with the exception that the devices were now in a completely passive condition during irradiation. That is, no voltages were applied during the radiation period.

TEST RESULTS

PHASE I, FLASH X-RAY

All of the dose-rate tests were performed with a Febetron 705 Flash X-ray machine operating in an X-ray Mode using a 20 nsec pulse width and in a 2 MeV E-beam (in a vacuum) using a 50 nsec pulse width. The X-ray Mode was used for dose-rate tests below 6×10^{10} Rad(Si)/sec, and the E-beam Mode was used for higher levels. A summary of the dose-rate disturb levels for the ER 3400 memory arrays is presented below.

Transient Read Disturb	1.1×10^{8} Rad(Si)/sec
Transient Write Disturb . . .	3.1×10^{8} Rad(Si)/sec
Transient Bit Survival	9.0×10^{11} Rad(Si)/sec

Read Disturb Tests: Transient radiation upsets were recorded in the ER 3400 (while operating in the Read Mode) at dose-rate levels as low as 1.1×10^{8} Rad(Si)/sec. The lowest level of upset (or worst case) occurred when the radiation burst was applied approximately 200 nsec before the start of a Logic "1" Data Output signal. The Recovery Time of these initial upsets was one Read cycle (the time required to read one word). To generate an error period beyond this time frame (for two Read cycles), a dose-rate level of approximately 1.4×10^{8} Rad(Si)/sec or greater was required. The effect of the Read Cycle Number on the level of the dose-rate was determined not to be a factor. That is, the Read Disturb levels recorded

on the first Read Cycle were about the same as those recorded after 10^6 Read Cycles.

The test method used to record a Read upset is illustrated in Figure 5. The top trace in the figure shows a section of the memory readout (a checkerboard pattern) via one of the Data Output lines. The bottom trace illustrates the simultaneous Macrodata response to the above data output. There is approximately one Read Cycle delay between the Data Output response and the corresponding Macrodata response. Both responses are correct for the stored pattern. If an error did occur, the Macrodata response would be different. In a like manner, three other dual-beam scopes are used for the other data lines.

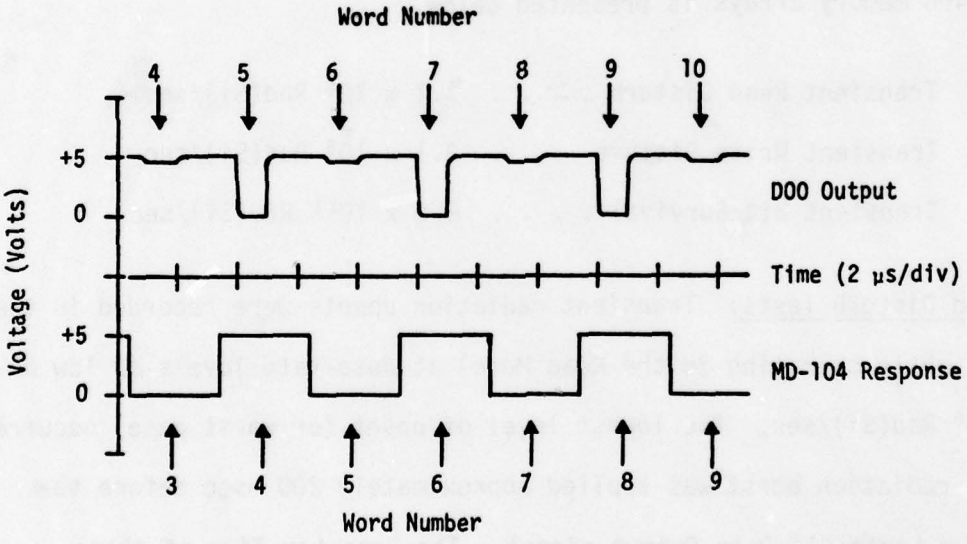


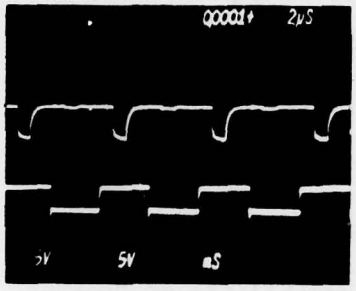
Figure 5. Illustration of Pre-radiation Data taken on Memory ER 3400. Top Trace: "Checkerboard" Output Response via Data Output Line D00 for Words No. 4 through 10. Bottom Trace: Correct Macrodata Response to the D00 Output.

Actual samples of two Read Disturbs for one of the test arrays is presented in Figure 6. Shown is the Pre-radiation and the Shot data of Read

FLASH X-RAY
READ DISTURB DATA

Dose Rate = 1.1×10^8 Rad(Si)/sec

Pre-Radiation Data
2 µSec/Div

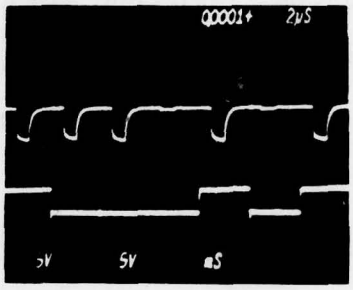


DO3 Output
(010101--)

MD Response
(No Errors)

(A)

Shot Data
2 µSec/Div



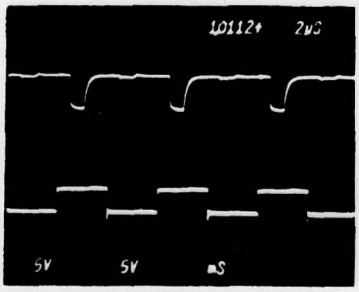
DO3 Output
(0?0101--)

MD Response
Error-Word (5)

(B)

Dose Rate = 2.0×10^{10} Rad(Si)/sec

Pre-Radiation Data
2 µSec/Div

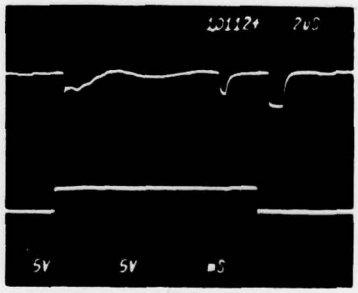


DOO Output
(010101--)

MD Response
(No Errors)

(C)

Shot Data
2 µSec/Div



DOO Output
(0????1--)

MD Response
Errors in Words
(5) through (8)

(D)

Figure 6. Flash X-ray Response for two Read Disturb Tests recorded at Dose Rate Levels of 1.1×10^8 and 2.0×10^{10} Rad(Si)/sec. Responses: Checkerboard Readout of Data Output Lines, DO3 & DOO [Words (4) to (10)] with MD-104 Interpretation. For the Shot Data, the Radiation Burst hit approx. 200 ns BEFORE the Data Out signal of Word (5).

Disturb Tests recorded at dose-rate levels of 1.1×10^8 and 2.0×10^{10} Rad(Si)/sec. In both cases, the radiation burst was applied in the Read Cycle for Word 5. Recovery Time from these two upsets was one Read Cycle for the lower dose-rate and four Read Cycles for the higher dose-rate.

Other information obtained from this portion of the evaluation was: (1) no data were lost in the actual MNOS memory of the test device as a result of the transient radiation, (2) all of the upsets were attributed to effects within the peripheral circuitry, and (3) no permanent changes in the electrical characteristics of the memory device were noted during these Read Disturb Tests.

Write Disturb Tests: When a transient radiation burst was applied during a Write operation, a dose-rate level of 3.1×10^8 Rad(Si)/sec or greater was required to produce an error in the stored memory. To produce this false Write, the radiation burst had to be applied at the start of a Write Enable gate of a chosen Write Cycle. An example of this type of disturbance is presented in Figure 7. Shown are the results of a radiation burst being applied in the fourth Write Cycle, producing a false Logic "1" storge in the memory instead of the correct Logic "0".

The overall results in this phase showed that a radiation burst (no matter what the magnitude) would only cause a false Logic "1" to be written. If the radiation burst was applied when a true Logic "1" was being written, there was no effect. There was only an effect when a true Logic "0" was being written. Also, only the memory word that was being written at the time of the burst was affected. Memory words written before and after the irradiation were not affected.

Other information worth noting from the Write Disturb Tests was that

WRITE DISTURB DATA

Dose Rate = 3.1×10^8 Rad(Si)/sec

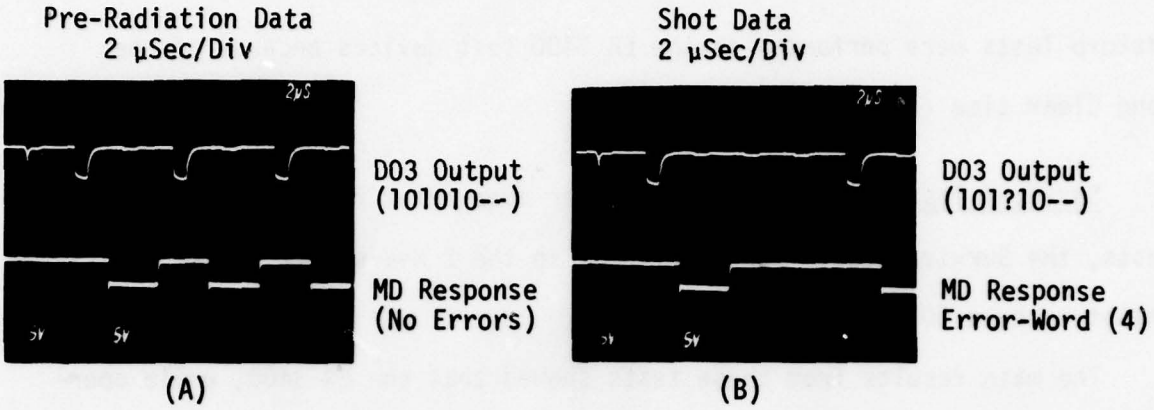


Figure 7. Flash X-ray Results for a Write Disturb Test recorded at a Dose Rate of 3.1×10^8 Rad(Si)/sec. Responses: Checkerboard Readout of Data-Out Line DO3 [Words (1) to (7)] after burst hit in the forth Write Cycle.

SURVIVAL AND RECOVERY DATA

Dose Rate = 9.0×10^{11} Rad(Si)/sec

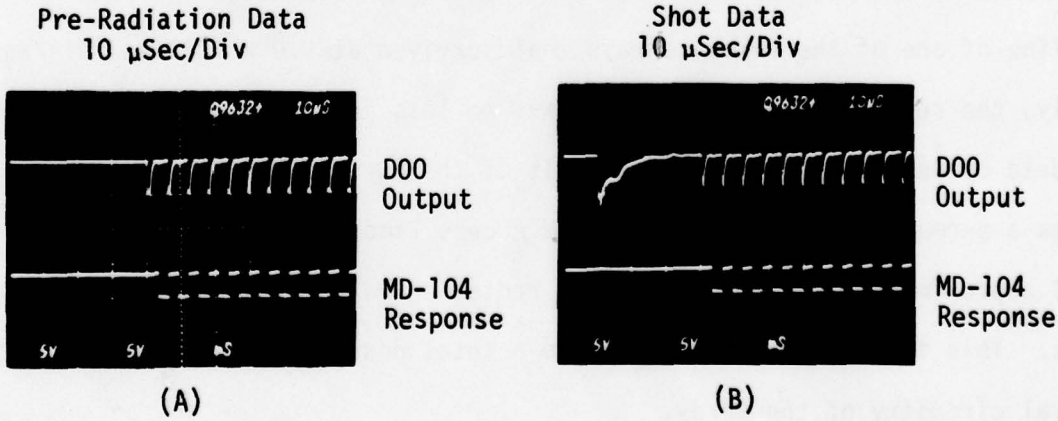


Figure 8. Flash X-ray Response for a Survival Test recorded in a 2 MeV Vacuum E-beam Environment. Responses: Trailing edge of Pause Period followed by a Checkerboard Readout. Flash X-ray burst hit approx. 30 µSec before the start of the Read Period. Recovery Time was approx. 25 µSec.

there were no permanent changes in any of the electrical characteristic or device parameters as a result of the transient radiation. Also, no Clear Disturb Tests were performed on the ER 3400 test devices because of the long Clear time (approximately 10 msec).

Survival Tests: To obtain the higher dose-rates required for these tests, the Survival tests were performed in the 2 MeV electron-beam environment using a 50 nsec radiation burst.

The main results from these tests showed that the ER 3400, while operating in the Pause Period, can survive and operate properly after absorbing a transient radiation burst as high as 9.0×10^{11} Rad(Si)/sec. This means that the device can be cleared, written, and read properly after a period of recovery, with no changes in the electrical characteristics. The minimum period of recovery needed for the ER 3400 at the above high dose rate was approximately 25 μsec. A sample of a Survival Test is presented in Figure 8. The figure shows the pre-radiation and post-radiation responses of a data output line of one of the memory arrays that survived at 9.0×10^{11} Rad(Si)/sec. Basically, the results showed that there was no loss in the pre-radiation memory data or device operation as a result of the burst. The only change noted was a permanent increase in the Read Access Time from a pre-radiation value of approximately 600 nsec to a post radiation value of approximately 800 nsec. This increase was attributed to a total dose effect in the PMOS peripheral circuitry of the array.

Memory devices tested beyond the above dose-rate level did not completely survive. Failures began to occur in some of the Data Output circuitry. There were no recoveries.

Recovery Time Tests: The recovery time for the ER 3400 was the minimum time needed to recoup from a radiation burst and resume normal operation. For the dose-rate levels tested, the ER 3400 required a recovery time ranging from 3 μsec to approximately 25 μsec. A table of the Recovery Times for the different dose-rate levels is presented below:

Dose-Rate Level in Rad(Si)/sec	Recovery Time (approximate)	Affected Read Cycles
1.1×10^8	3 μsec	1
1.4×10^8	6 μsec	2
1.2×10^9	9 μsec	3
2.0×10^{10}	12 μsec	4
6.2×10^{10}	18 μsec	6
9.0×10^{11}	25 μsec	8

The above Recovery Times were measured when the test devices were operating in the Read Mode, and the radiation burst was applied approximately 200 nsec before the start of the Data Output signals.

TEST RESULTS

PHASE-II, Co-60

Twenty-four ER 3400 memory arrays obtained from two different production lines were subjected to total dose Co-60 tests. Each of the devices was irradiated until failure occurred, while operating under one of the four test conditions presented in the Co-60 Test Procedures. The dose-rate applied during all of these tests was 22 Rad(Si)/sec. A summary of the results is presented below.

Test Conditions	Total Dose Failure Level [Rad(Si)]
Continuous Read	$2.0 - 3.0 \times 10^4$
Clear/Write/Read	$2.3 - 3.5 \times 10^4$
Pause Only	$2.5 - 4.0 \times 10^4$
Passive Only	$4.0 - 6.0 \times 10^4$

The overall results showed that the ER 3400 could survive (depending upon the operating conditions) a total dose of ionizing radiation ranging from 2×10^4 to 6×10^4 Rad(Si). The "worst-case" condition was when the memory device was continuously Read during the radiation period. Under this mode, total dose failures were recorded as low as 2×10^4 Rad(Si). The most optimum test condition was when the memory was operated in the Passive Only state. That is, no voltage was applied to the test device during irradiation. Under this mode, the arrays were capable of surviving up to a total dose level of 6×10^4 Rad(Si). A comparison between these two operating modes is best shown in Figures 9 and 10.

Shown is the degradation in Read Access Time as a function of total radiation absorbed. These plots show the performance of the ER 3400 operating in Co-60 radiation. Figure 9 presents the results of an ER 3400 lot fabricated on a production line located in the United States. Figure 10 shows the Co-60 results of another lot fabricated in Taiwan. The results plotted are typical for the two memory lots tested.

The plots in Figure 9 (for memory Lot No. ER3400-GI0978-419192) show that while operating under a maximum stress condition (Continuous Read), the Read Access Times will exceed the designed spec. limits of 900 nsec after absorbing a total gamma dose of approximately 2×10^4 Rad(Si)/sec.

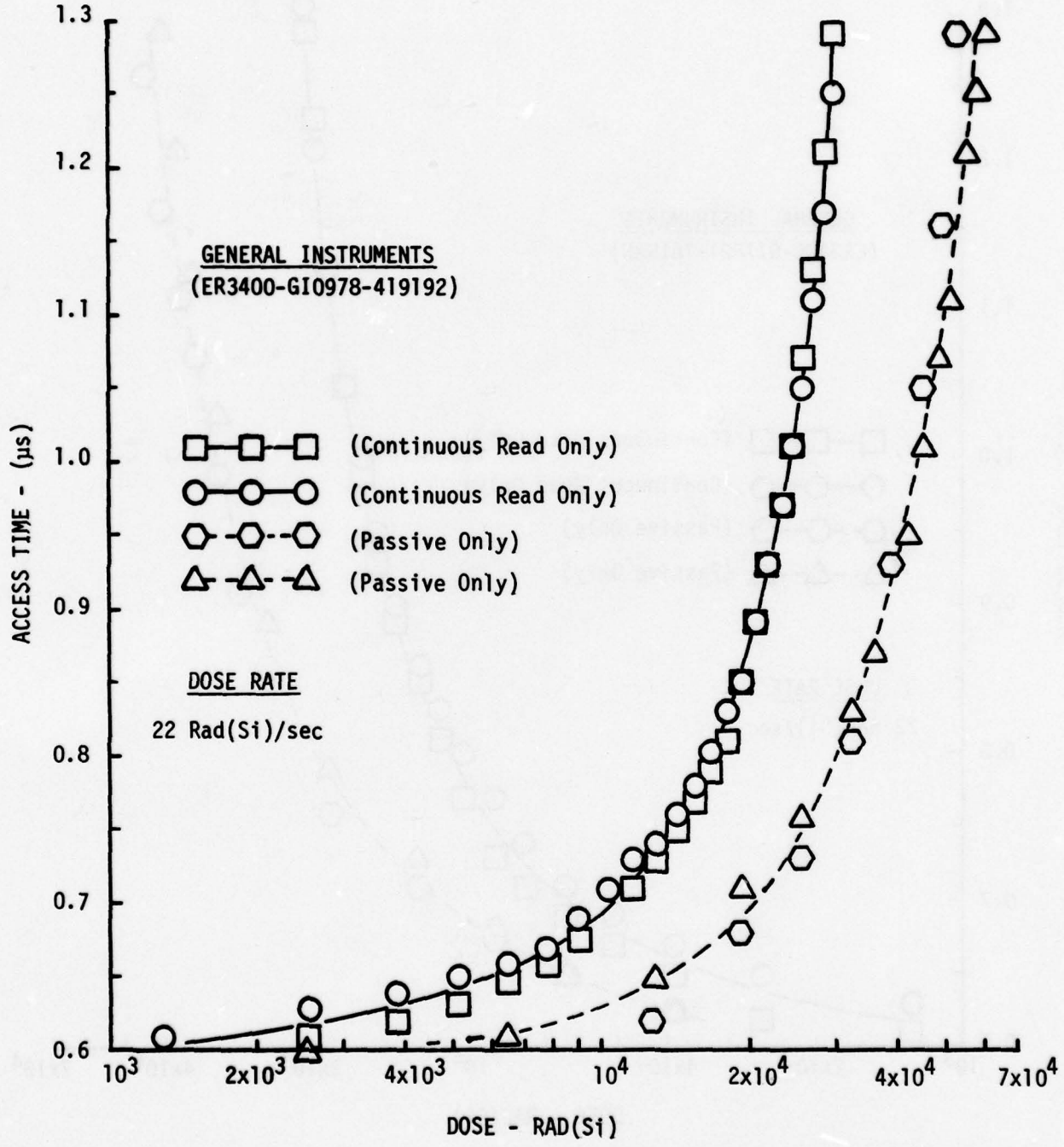


Figure 9. Co-60 Data. ER3400 Read Access Time versus Total Gamma Dose.

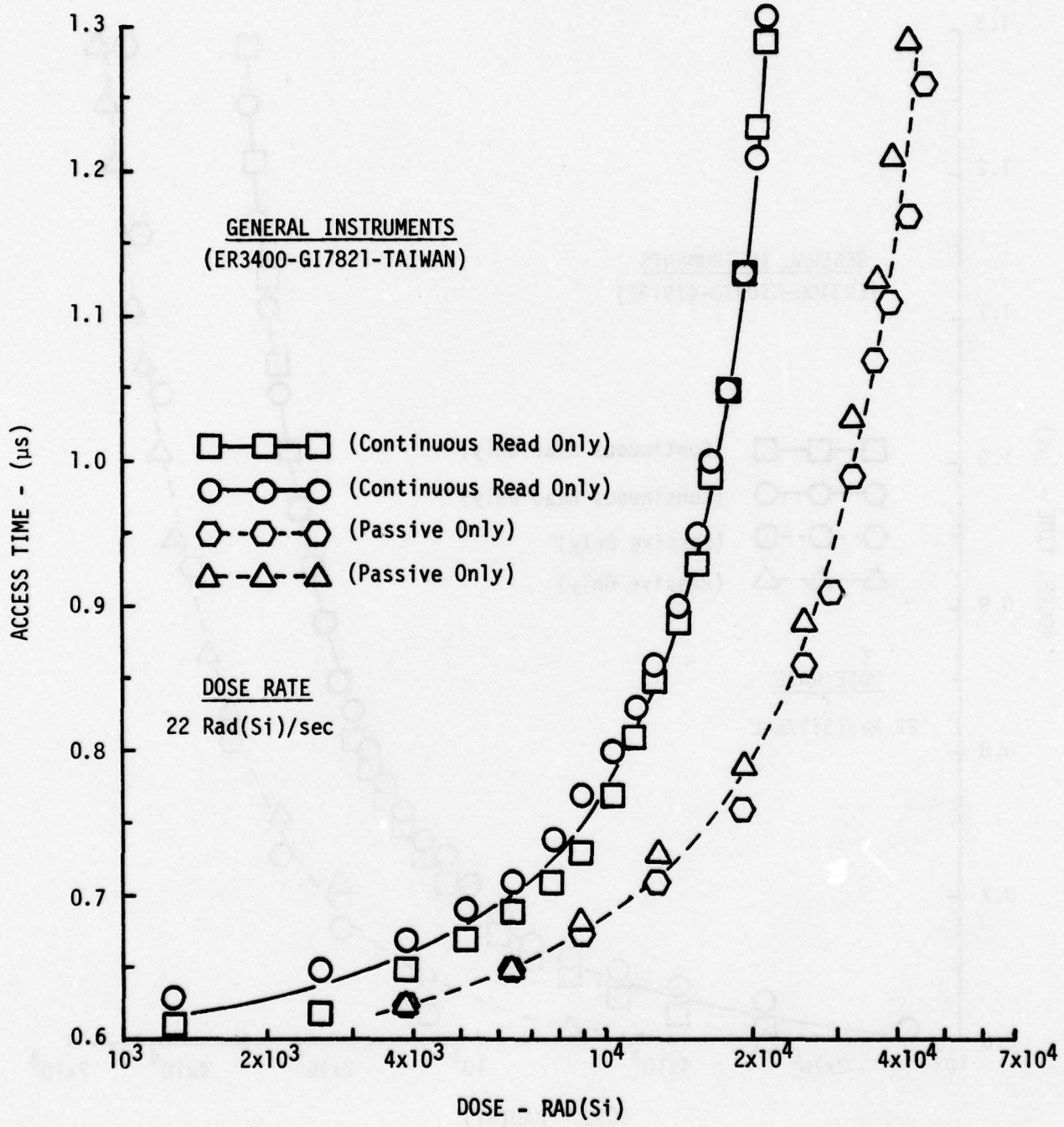


Figure 10. Co-60 Data. ER3400 (Taiwan Made) Read Access versus Total Dose.

However, the same curve shows that if the Read Cycle Rate was reduced, and the Read Access Time was allowed to increase, the devices could survive and operate up to a total dose of 3×10^4 Rad(Si). Shown also is the radiation performance while operating under the optimum conditions (Passive Only Test). Here, with no voltage applied during the radiation period, the memory arrays were made to operate and survive up to total dose levels of 6×10^4 Rad(Si).

Figure 10 (covering Lot No. ER3400-GI7821-TAIWAN) presents the same two types of curves. For this memory lot, the data show that the Read Access Time (while operating in the Continuous Read Mode) will exceed the designed limit of 900 nsec after absorbing a total dose level of 1.5×10^4 Rad(Si)/sec. This level of hardness is approximately 5×10^3 Rad(Si) lower than the same datum point in Figure 9. Reducing the Cycle Rates of the Taiwan memories also increased the radiation survival levels. While operating in the Continuous Read Mode, the Taiwan arrays could be made to survive at total dose levels up to 2×10^4 Rad(Si), and removing the power from the devices during irradiation increased this survival level up to 4×10^4 Rad(Si). Again, however, these last two survival levels were still below the levels obtained from the lot tested in Figure 9 [approx. 10 to 20 kRad(Si) lower].

CONCLUSIONS

Transient Radiation Survivability Level: The dose-rate results show that the ER 3400 MNOS EAROM array can survive a 50 nsec radiation burst of 45 kRad(Si) or a dose-rate level of 9×10^{11} Rad(Si)/sec in a 2 MeV E-beam environment with no loss of memory data or device operation.

Disturb Level (Read Mode): A disturb mechanism can be temporarily induced in the Read Operating Mode of the ER 3400 if the radiation burst (in the X-ray Mode) is applied to the device approximately 200 nsec before the Data Output pulses. The dose-rate levels needed to generate these interruptions are 1.1×10^{8} Rad(Si)/sec and higher.

Disturb Level (Write Mode): Disturb mechanism can be temporarily induced in the Write Mode of the devices if the radiation burst is applied at the start of a Write Enabled gate. The dose-rate levels needed to generate these interruptions are 3.1×10^{8} Rad(Si)/sec and higher.

Accumulating Dose Effects: The Co-60 total dose tests have shown that the ER 3400 memories can accumulate a total dose of gamma radiation up to 15 kRad(Si) while operating under its maximum stress conditions. Maximum stress conditions for the ER 3400 are when the devices are operating in the Continuous Read Mode at the maximum cycle rate (Read Access Time setting equal to or less than 900 nsec). However, the devices can be made to survive at higher total dose levels by operating at reduced cycle rates. The optimum condition is when the memories are operating in the Passive Only state. Under this condition, the arrays are capable of surviving total dose levels ranging up to 60 kRad(Si).

COMMENTS

As in the case of the previously tested Nitron NCM 7040, the General Instrument ER 3400 is also a commercial device and was not designed to be radiation hard. The main reason is that both devices employ oxide/nitride PMOS in the peripheral circuitry. This technology is not known for radiation hardness. As a result, the low radiation susceptibility levels for both arrays were comparable.

The most interesting find in the ER 3400 evaluation was in the Co-60 or total dose tests. In this phase, the results showed that the total dose failure levels were not the same for the two different lot numbers. The arrays fabricated in Taiwan were consistently lower in total dose hardness than the lot fabricated in the United States. Since appearance and electrical performance were the same for both chips, it was concluded that the differences in the total dose results was due to "Process-Control". The significance of this finding is that it shows the important role that process-control can play in determining the radiation hardness levels of a paricular memory device.

IONIZING DOSE-RATE AND TOTAL DOSE TESTS ON THE SPERRY RAND NONVOLATILE 256-BIT MNOS RAM ARRAY NO. (SR2256)

ABSTRACT

Ionizing dose-rate and total dose tests have been performed on the Sperry Rand 256-Bit MNOS (SR2256) RAM array. Results from these tests have shown that the devices can survive dose-rate levels as high as 1.0×10^{12} Rad(Si)/sec in a 2 MeV electron-beam environment with no loss of memory data or permanent degradation in device operation. However, under certain test conditions, the "Read" and "Write" modes of the arrays can be temporarily interrupted. In the Read mode, this interruption can be induced at dose-rate levels of 4×10^{8} Rad(Si)/sec and higher if the radiation burst is applied approximately 1 microsecond before the start of the "Data Output" signals. In the Write mode, a disturb mechanism can be generated in a 2 MeV electron beam at dose-rate levels of 2.4×10^{11} Rad(Si)/sec and higher if the burst is applied at the start of the "Memory Enable" signal. Also, the total dose tests have shown that the memory arrays (while cycling through the operational modes at the maximum rates) can accumulate a total dose of gamma radiation in excess of 1×10^{5} Rad(Si) and survive. At reduced cycle rates, the arrays can operate and survive up to 3×10^{5} Rad(Si).

INTRODUCTION

In the preceding evaluations, the Air Force Weapons Laboratory conducted ionizing radiation studies on various MNOS memory devices and related PMOS circuitry. The overall objective of these evaluations was to obtain data which would assist in optimizing the radiation hardness levels and electrical characteristics of MNOS memories for possible application in nuclear and space radiation environments. A result from these efforts was the fabrication of a special prototype device. This device was the Sperry Rand SR2256 MNOS RAM array. This report presents the results from the radiation testing performed on this device at the Air Force Weapons Laboratory. Included are the ionizing dose-rate and total dose test results obtained from Febetron 705 flash X-ray and Co-60 environments. A total of 15 memory arrays was evaluated. No neutron tests were performed on these arrays because earlier neutron tests conducted on related discrete PMOS and MNOS components showed no degrading effects on the majority carrier devices at exposure levels to 10^{15} n/cm^2 (See Reference 1).

THE SPERRY SR2256

The SR2256 is a fully decoded, 64-word by 4-bit, electrically alterable, non-volatile, static Read/Write RAM designed to interface with TTL and CMOS. The device employs enhancement mode, clean oxide PMOS with conventional MNOS (non-step gate) on bulk silicon technology. It is packaged in a standard 40 pin DIP with separate Data Inputs and Outputs. Some of the important

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1. Marraffino, P., et al. Design and Fabrication of Radiation Hardened MNOS Memory Array, AFWL-TR-74-209, July 1975.

electrical specifications obtained from the Reliability Tests in Reference 2 are:

Clear/Write Cycle Time	1.4 μSec - 2.8 μSec
Read Access Time	1.0 μSec - 1.8 μSec
Retention	>24 Hrs with 10^6 Read Cycles
Endurance	>10^{11} Clear/Write Cycles
Power Dissipation	780 mW (Worst Case)

The Retention Time is determined by the length of the Clear/Write Cycle. As as example, for a retention of 24 hours plus 10^6 Read cycles, a 2.8 μSec Clear/Write Time would be needed. Also, the worst case power dissipation corresponds to operating in the Clear and Read modes.

A photomicrograph and simplified block diagram of the SR2256 are shown in Figure 1. The prominent design features of the 256 mils by 224 mils chip are: (1) the division of the memory cells into two 32 by 4 bit arrays to reduce substrate capacitance, (2) the use of two MNOS transistors for each memory cell for longer storage capacity, and (3) the use of two extra timing signals [data latch (DL) and memory enable (ME)] designed to reduce transient upsets in the Read/Write modes. In the technology tradeoffs, speed was emphasized over power and total dose hardness was emphasized over chip area.

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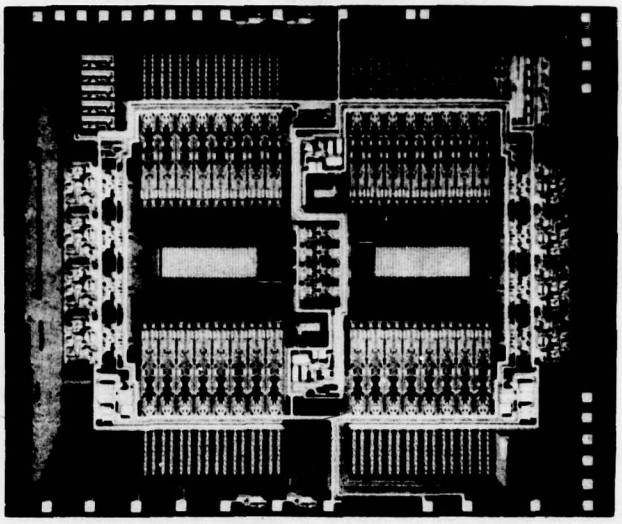
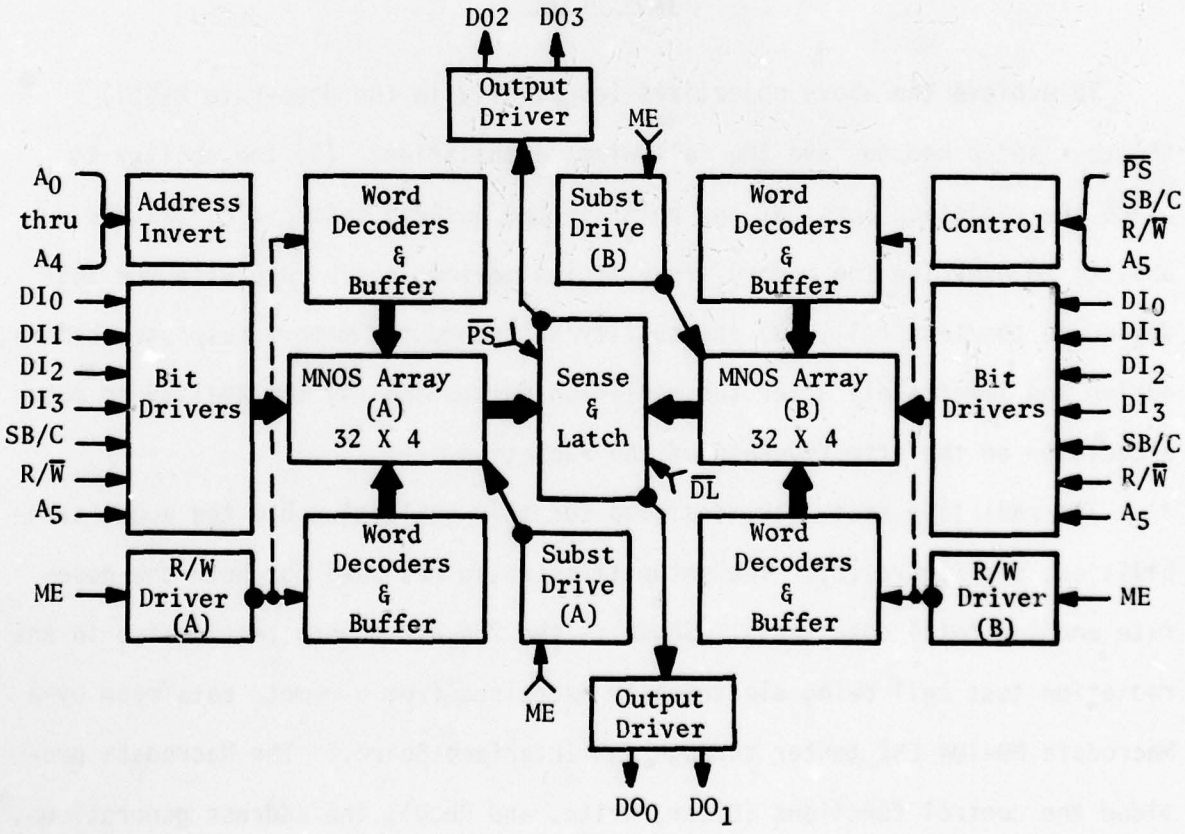
2. Marraffino, P., et al. Design and Fabrication of Radiation Hardened MNOS Memory Array, AFWL-TR-78-48, 1979.



(A)



(B)

Figure 1. Photograph and Simplified Block Diagram of the Sperry Rand SR2256, 256-Bit MNOS RAM Array.

RADIATION TEST OBJECTIVES

Dose-Rate: The objectives of the dose-rate tests were to determine (1) the dose-rate levels needed to upset or jam the operational modes of the device, (2) the maximum dose-rate levels the memory can withstand and still operate after the burst, and (3) the time needed to recover or anneal from a particular radiation burst.

Total Dose: In the total dose tests, the objective was to determine the permanent of temporary changes in the memory's characteristics (under different operating conditions) as a result of a given amount of ionizing radiation.

TEST SETUP

To achieve the above objectives (especially in the dose-rate tests) the test setup had to have the following capabilities: (1) the ability to place the radiation burst at any point in the desired test cycle, (2) the ability to exercise the memory array at its maximum cycle rate with the test device in the test cell, (3) the ability to record the memory responses before, during and immediately after the radiation burst, and (4) the ability to make a decision on the effectiveness of the radiation.

The radiation test setup designed for this evaluation had the above capabilities; see Figure (2). The setup illustrated was used for both the dose-rate and the total dose tests. Shown is the 256-bit memory test device in the radiation test cell being electrically exercised from a remote data room by a Macrodata MD-104 LSI tester through an "Interface Board." The Macrodata provided the control functions (Clear, Write, and Read), the address generations, the data patterns to the Interface Board, and the response to the data returning

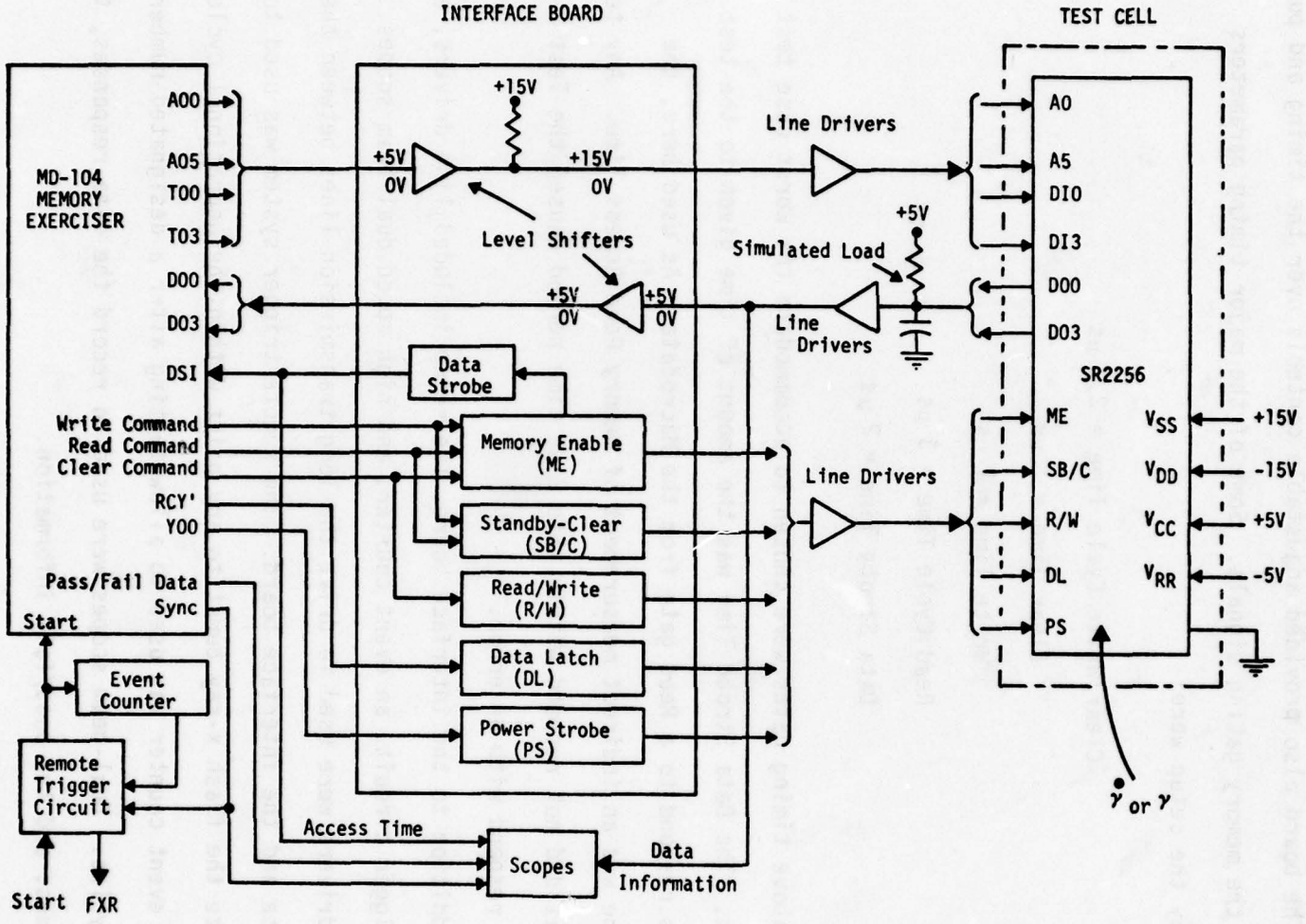


Figure 2. Radiation Test Setup for the Sperry Rand SR2256 MNOS RAM Array.

from the board. The Interface Board provided the voltage transitions between the TTL output levels of the Macrodata and the $\pm$ 15 volt levels of the test device. The board also provided adjustable controls over the timing and pulse widths of the memory gating signals. Some of the major timing parameters provided by the setup were:

Clear/Write Cycle Time = 2.7 μs

Clear Time = 1 μs

Write Time = 1 μs

Read Cycle Time = 3 μs

Data Strobe Time = 2 μs

The above timing gates were chosen to accommodate the worst case test conditions. The Data Strobe Time was the amount of time given to the test devices to respond to a Read gate from the Macrodata. As used here, the Data Strobe was an indirect measurement of memory Read Access Time. Any test device that did not respond within this 2 μs time period caused the Test System to respond with an error.

In addition to the interface board, the setup included line drivers, a remote trigger circuit, an event counter, and high speed dual-beam scopes. The line drivers were used to drive the long transmission lines between the test device and the interface board. The remote trigger system was used to synchronize the flash x-ray burst to any point within the oeprational cycle. A control event counter was used to allow testing after a designated number of Read cycles. Dual-beam scopes were used to record the data responses, the access times, and the pass/fail information.

TEST PROCEDURES (FLASH X-RAY)

The first phase of the radiation testing was the dose-rate tests. These tests were classified as "Dynamic Tests" because the concern was in the device behavior before, during, and immediately after the radiation burst. These tests covered two general areas. These were: (1) the Operational Disturb Tests, and (2) the Survival and Recovery Tests.

Operational Disturb Tests: The first series of transient radiation tests was the Operational Disturb Tests. The main objective of these tests was to determine the minimum dose-rate levels which would produce an error in the memory response. The dose-rates of interest for these tests ranged from 10^7 Rad(Si)/sec to 10^{11} Rad(Si)/sec. Further, this group of tests was divided into two areas. These were: (1) the Read Disturb tests, and (2) the Clear/Write Disturb tests.

The Read Disturb Tests: The Read Disturb tests were performed first because the memory device was thought to be more sensitive to transient upsets when operating in the Read Mode. In this test, the radiation burst was applied in a predetermined Read Cycle with the objective of producing errors in the recorded memory responses. The radiation testing zone for the chosen Read Cycle is illustrated in Fugure (3). The zone ranged from the start of the Read Power Strobe to the start of the Data Output responses. This testing zone was chosen because it was believed that a radiation burst hitting within this area would have the highest probability of producing errors in the recorded Data Outputs.

In addition, the effects of the Read Cycle Number as a function of dose-rate upset were also determined. These effects were found by performing the Read Disturb Test under two conditions. The first condition (which was considered

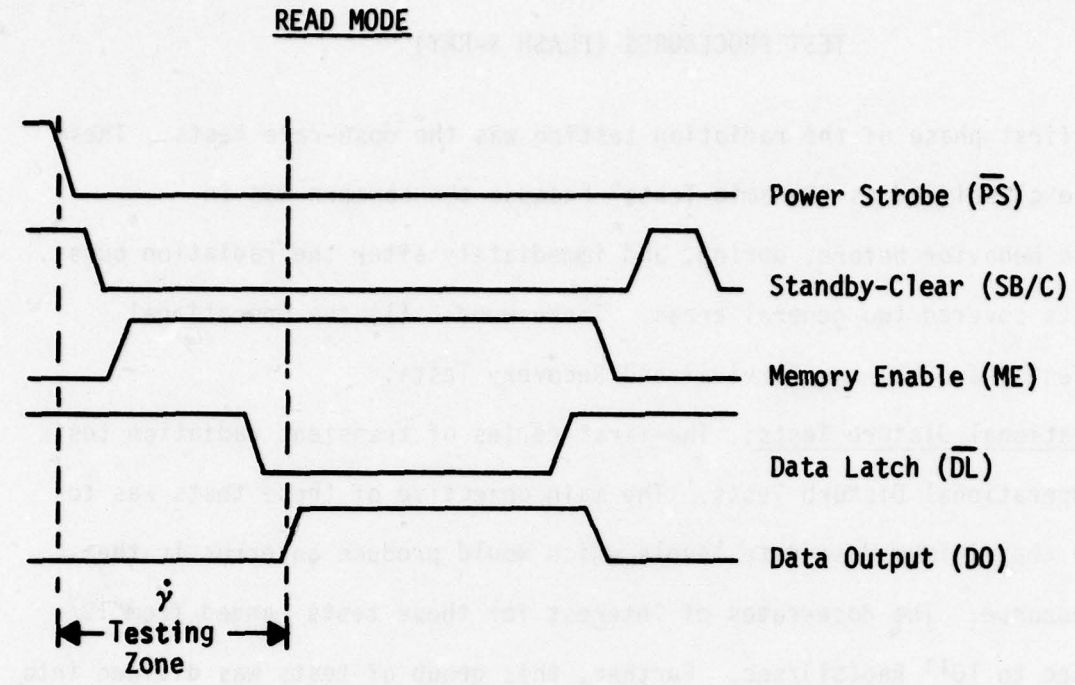


Figure 3. Flash X-ray Radiation Test Zone in Relation to the Read Timing Gates of the Sperry Rand SR 2256.

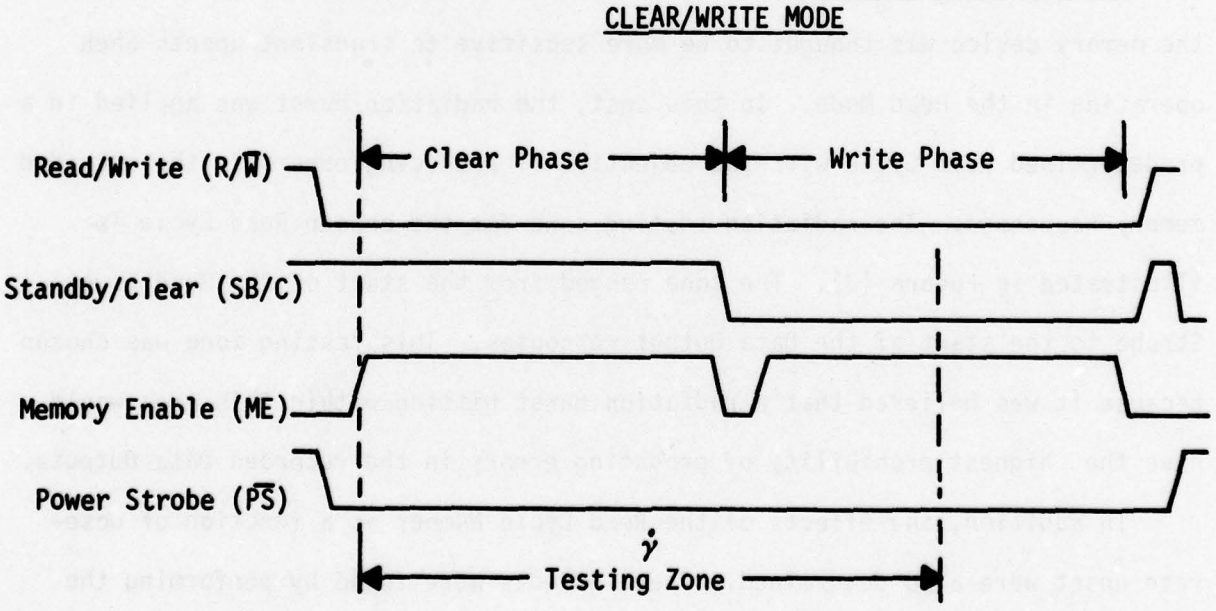


Figure 4. Flash X-ray Radiation Test Zone in Relation to the Clear/Write Period of the Sperry Rand SR 2256.

the Worst-Case) was to perform the tests on the first Read cycle after the memory had been Read continuously for 10^6 times. The second condition was to perform the same test on the first Read cycle after a Clear/Write period. The reason for choosing these two limits was that the stored Threshold Voltages within the memory cells would be lower under condition (1) and higher under condition (2). As a result, the susceptibility level of the device to transient upsets will be different for the above two conditions (higher for Number 1 and lower for Number 2). The results did answer the question on Read Cycle Number affecting the Read Disturb level.

The Clear/Write Disturb Test: The second group of tests under the disturb phase was the Clear/Write Disturb Test. In these tests, the objective was to determine tbe disturb mechanism of a radiation burst occurring within a Clear/Write cycle. The test zone for this phase is illustrated in Figure (4). As shown, the test zone extends from the start of the Clear Memory Enable gate to the middle of the Write Memory Enable gate. Within this time frame, the point most sensitive to transient radiation was first determined, and then the minimum dose-rate level which would prevent the particular Write cycle from functioning was measured. Also monitored were the radiation effects on the other Write cycles of the same period.

Survival and Recovery Tests: The last phase of the flaxh X-ray tests was the Survival and Recovery measurements. In this phase, the primary objectives were to determine the maximum dose-rate levels the devices could withstand and still operate after the burst and to measure the recovery time. Dose-rate levels of exposure ranged from 2×10^{10} Rad(Si)/sec to 2×10^{12} Rad(Si)/sec. The operating mode subjected to exposure was limited to the device's "Pause" period because of the limited amount of devices and the higher probability of survival in this period.

TEST PROCEDURES (Co-60)

The last phase of the radiation testing was the total dose tests. This series was composed of three types of tests. Each type represented an operational condition of the device. These tests were:

1. The Clear/Write/Read Cycle test,
2. The Pause Only Test, and
3. The Passive Only Test.

All three tests were performed in the AFWL Co-60 source at a low dose-rate of 77 Rad(Si)/sec. The first test was classified as Dynamic and the remaining two were classified Static. The Dynamic tests were concerned with the device behavior before, during, and immediately after the radiation. The Static tests were concerned with the behavior directly before and after a specified level of exposure.

Clear/Write/Read Cycle Test: In this dynamic test, the memory device was continuously cycled through all of the operational modes (at the maximum rate) while being irradiated. In the meantime, the data output from the memory device, along with the changing Clear/Write/Read Cycle, and Access Time was continuously monitored and recorded. Also recorded was the changing gate threshold voltage of the PMOS test transistor provided with the array for evaluation. The test was continued until the device failed or until the Data Output was no longer correct. From the results, the total dose that the test device could withstand while operating under the maximum electrical stress condition was known. Also, the Read Access Time along with the Gate Threshold shift as a function of total dose was plotted.

Pause Only Test: This test was the first of two Static tests. The test device was subjected to radiation only during the Pause or Wait period of operation. No Clear, Write, or Read pulse was applied during irradiation. However, all other D.C. voltages were present. Again (as in the above test) the Data Output along with the Clear/Write, Read, and Access Time was recorded. This test was also continued until device failure, and the Access Time along with the Gate Threshold shift as a function of total dose was plotted.

The Passive Test: The test procedures and radiation conditions for this test were the same as in the previous two tests, except that the device was in a completely passive condition during irradiation. That is, no voltage was applied to the device, and all pin leads were grounded. Irradiation was continued until failure occurred; the same parameters were monitored, recorded, and plotted.

TEST RESULTS

PHASE I, FLASH X-RAY

All of the dose-rate tests were performed with a Febetron 705 Flash X-ray machine operating in a X-ray Mode using a 20 nsec pulse width, and in a 2 MeV E-beam Mode (in vacuum) using a 50 nsec pulse width. The X-ray Mode was used for dose-rate tests up to 6×10^{10} Rad(Si)/sec, and the E-beam Mode was used for higher levels. A summary of the dose-rate disturb levels for the SR2256 memory array is presented below.

Transient Read Disturb . . . . 4.0×10^{8} Rad(Si)/sec

Transient Write Disturb . . . 2.4×10^{11} Rad(Si)/sec

Transient Bit Survival . . . . 1.0×10^{12} Rad(Si)/sec

Read Disturb Tests: Transient radiation upsets were recorded when the SR2256 array was in the Read Mode at dose-rate levels as low as 4×10^8 Rad (Si)/sec. The lowest level of upset (or worst case) occurred when the radiation burst was applied approximately 1 microsecond before the start of a Logic "0" data output signal. For data output responses of Logic "1", a dose-rate level of approximately 4.2×10^8 Rad(Si)/sec was needed for an upset. The recovery time of these initial upsets was one Read Cycle (the time required to read one word). To generate an error period beyond this time frame (for two Read Cycles), a dose-rate level of approximately 2×10^{10} Rad(Si)/sec or greater was required. The effect of the Read Cycle Number on the level of the dose-rate upset was determined not to be a factor. That is, the Read Disturb levels recorded on the first Read Cycle were about the same as those recorded after 10^6 Read Cycles.

The test method used to record a Read upset is illustrated in Figure 5. The top trace in the figure shows a section of the memory readout (a checkerboard pattern) via one of the Data Output lines. The bottom trace illustrates the simultaneous Macrodata response to the above data out. Both responses are correct for the stored pattern. If an error did occur, the Macrodata response would be different. Similarly, three other dual-beam scopes are used for the other data lines.

A sample of a Read Disturb for one of the arrays is presented in Figure 6. Shown is the lowest dose-rate value where both of the two logic output levels were upset simultaneously. For this case, the transient radiation burst was applied approximately 1 μsec before the start of Data Output of Word three in the first Read Cycle following 10^6 continuous Reads.

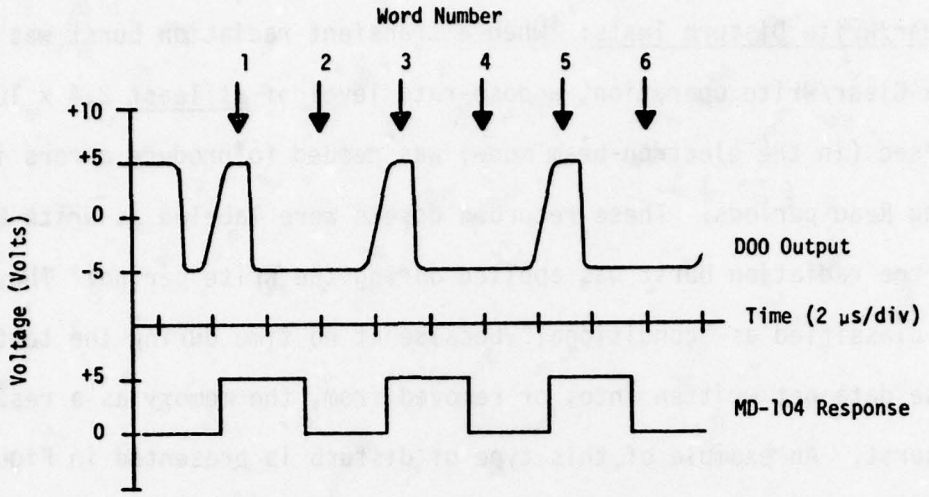


Figure 5. Illustration of Pre-radiation Data taken on Memory SR2256. Top Trace: "Checkerboard" Output Response via Data Output Line D00 for Words No. 1 through 10. Bottom Trace: Correct Macrodata Response to the D00 Out.

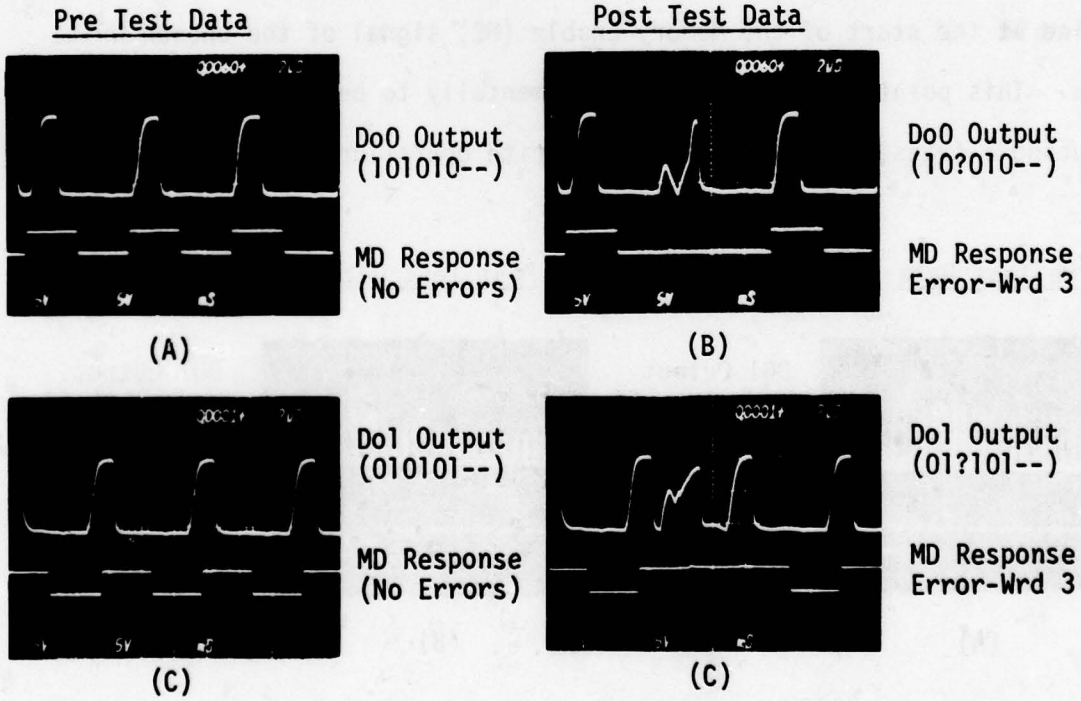


Figure 6. Read Disturb Data. Flash X-ray Response for a Read Disturb Test recorded at a Dose-Rate Level of 4.2×10^8 Rad(Si)/sec. Responses: Checkerboard Readout of Data-Out Lines, D00 & D01 [Words (1) to (6)] with MD-104 Interpretation.

Clear/Write Disturb Tests: When a transient radiation burst was applied during a Clear/Write operation, a dose-rate level of at least 2.4 x 10^{11} Rad(Si)/sec (in the electron-beam mode) was needed to produce errors in the following Read periods. These recorded upsets were labeled as Write Disturbs because the radiation burst was applied during the Write period. They were further classified as "conditional" because at no time during the tests did any false data get written into, or removed from, the memory as a result of the burst. An example of this type of disturb is presented in Figure 7. The results in the figure show that the errors produced in the subsequent Read Period were the result of a decrease in the peak output voltage levels of the data out signals, and not the result of false data generated.

It should be noted for this group of tests, that the radiation burst was applied at the start of the Memory Enable (ME) signal of the chosen Write Cycle. This point was determined experimentally to be the most sensitive in producing a transient upset in a Clear/Write operation.

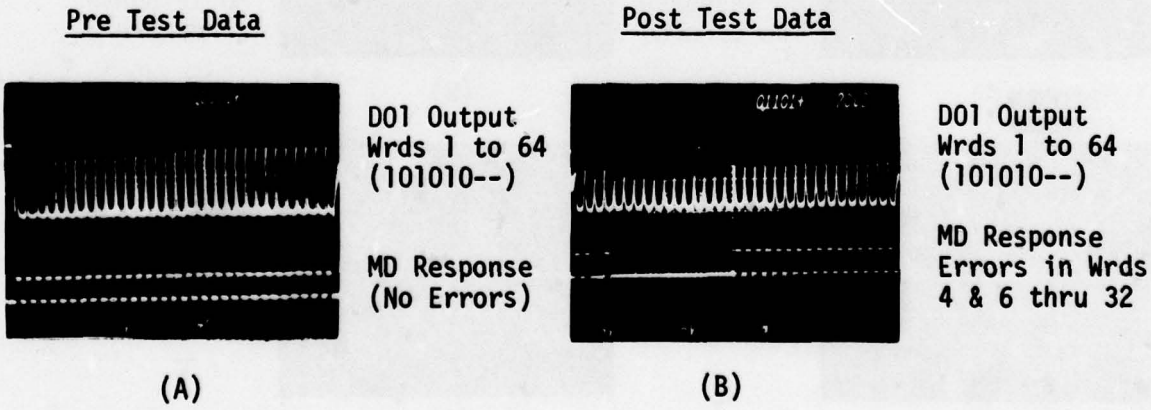


Figure 7. CLEAR/WRITE DISTURB DATA. Flash X-ray Results for a Clear/Write Disturb Test recorded at a Dose-Rate of 2.4 x 10^{11} Rad(Si)/sec. Responses: Checkerboard Readout of Data Output Line DO1 [Words (1) to (64)] after burst hit in the forth Write Cycle.

Survival and Recovery Tests: To obtain the higher dose-rates required for these tests, the Survival and Recovery Tests were performed in the 2 MeV electron-beam environment using a 50 nsec radiation burst.

The main results from these tests showed that the SR2256, while operating in the Pause Period, can survive and operate properly after absorbing a transient radiation burst as high as 1.0×10^{12} Rad(Si)/sec. The minimum period of time needed by the array to recover from this high dose-rate was approximately 80 μsec. A sample of a survival test is presented in Figure 8. The figure shows the pre-radiation and post-radiation responses of a data output line of one of the memory arrays that survived at the dose-rate of 1.1×10^{12} Rad(Si)/sec. Other post testing on the same array showed that there was no loss of the pre-radiation memory data or device operation as a result of the burst.

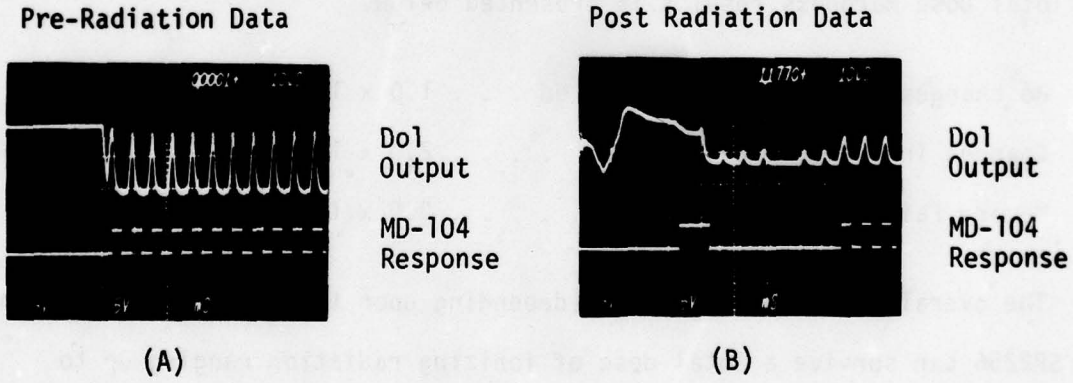


Figure 8. SURVIVAL and RECOVERY DATA. Flash X-ray Response for a Survival Test recorded at a Dose-Rate of 1.1×10^{12} Rad(Si)/sec in a 2 MeV E-beam Environment. Responses: Trailing edge of Pause Period followed by a Checkerboard Readout. Flash X-ray burst hit 30 μsec before the Read Period. Recovery Time = 80 μsec.

Two other arrays were tested at higher dose-rate levels. One was tested at 1.3×10^{12} Rad(Si)/sec and the other tested at 2.03×10^{12} Rad(Si)/sec. The device tested at the highest level was completely destroyed, and the memory

tested at the lower level survived conditionally. Conditional survival means that the memory's electrical timing parameters had to be changed in order for the device to operate properly after the burst. Also, the device that survived conditionally did not lose its memory as a result of the burst.

TEST RESULTS

PHASE II, CO-60

Six of the 15 arrays evaluated were subjected to total dose Co-60 tests. All six of the devices were selected from different lots, but with similar pre-radiation Read Access Times (approximately 1.0 to 1.2 μsec). Each of the six devices was then irradiated while operating under one of the three test conditions listed in the "Test Procedures". A summary of the Total Dose Hardness results is presented below.

No changes in Cycle Times Required . . . 1.0×10^5 Rad(Si)

Changes in Cycle Times Required . . . . 2.0×10^5 Rad(Si)

Memory Failure . . . . . 3.0×10^5 Rad(Si)

The overall results showd that (depending upon the operating conditions), the SR2256 can survive a total dose of ionizing radiation ranging up to 3.0×10^5 Rad(Si). The results also showed that the three operating test conditions had no apparant effect on the degradation rate of the devices exposed to Co-60 radiation. In all three cases, the rate of increase in the Read Access Time was approximately equal. The results also showed that all devices were still functioning (with timing changes in the Clear/Write/Read gating limits) after absorbing 2×10^5 Rad(Si) of total dose.

Finally, the results showed that at 3 x 10^5 Rad(Si), all the devices were inoperative, regardless of the cycle time setting. These results are shown in Figure 9.

Figure 9 shows the Read Access Time degradation versus total dose for three SR2256 arrays tested under the three operating conditions. The results presented are typical for all of the devices tested. The data show that the test devices can accumulate a total dose in excess of 1 x 10^5 Rad(Si) and operate within the pre-radiation timing limits (1 μsec Write Time and 1.8 μsec Read Access Time). For operating beyond this level and up to 2 x 10^5 Rad(Si), the Access Time would have to be extended to approximately 2.8 μsec. The Clear and Write time would also have to be increased (approximately 2 μsec each at this dose level). Above 2 x 10^5 Rad(Si), and until failure, another microsecond would have to be added to each of the timing limits.

The above data show that the SR2256, when irradiated in Co-60, will "slow down" before failure. A major reason for this slow-down is indicated in Figure 10. Figure 10 shows the Gate-Threshold-Shifts (as a function of total dose) of three fixed-gate PMOS test transistors incorporated one each on the test arrays presented in Figure 9. The importance of the data in Figure 10 is that they show a sample measurement of the relative radiation hardness of the PMOS technology employed in the test array's peripheral circuitry. More specifically, the curves show that the PMOS test transistors (while under radiation and protected with fixed bias) suffered negative shifts in their Gate turn-on voltages. These shifts continued until levels of -1.5 to -2.0 volts were reached. At these levels, the associated memory arrays were no longer operating properly. That is, the arrays

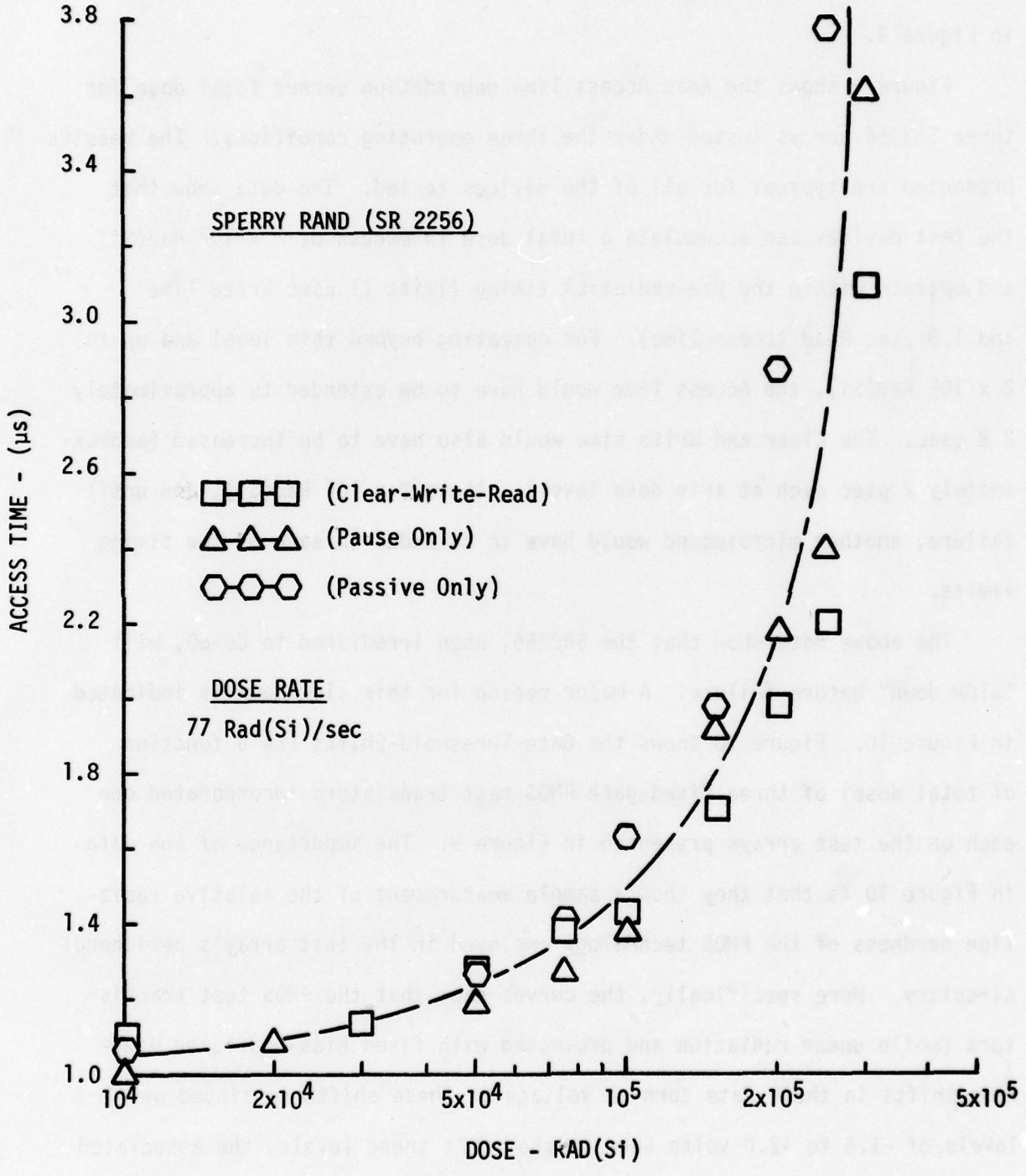


Figure 9. Co-60 Data. SR2256 Read Access Time (after 10^6 continuous Read) versus Total Gamma Dose.

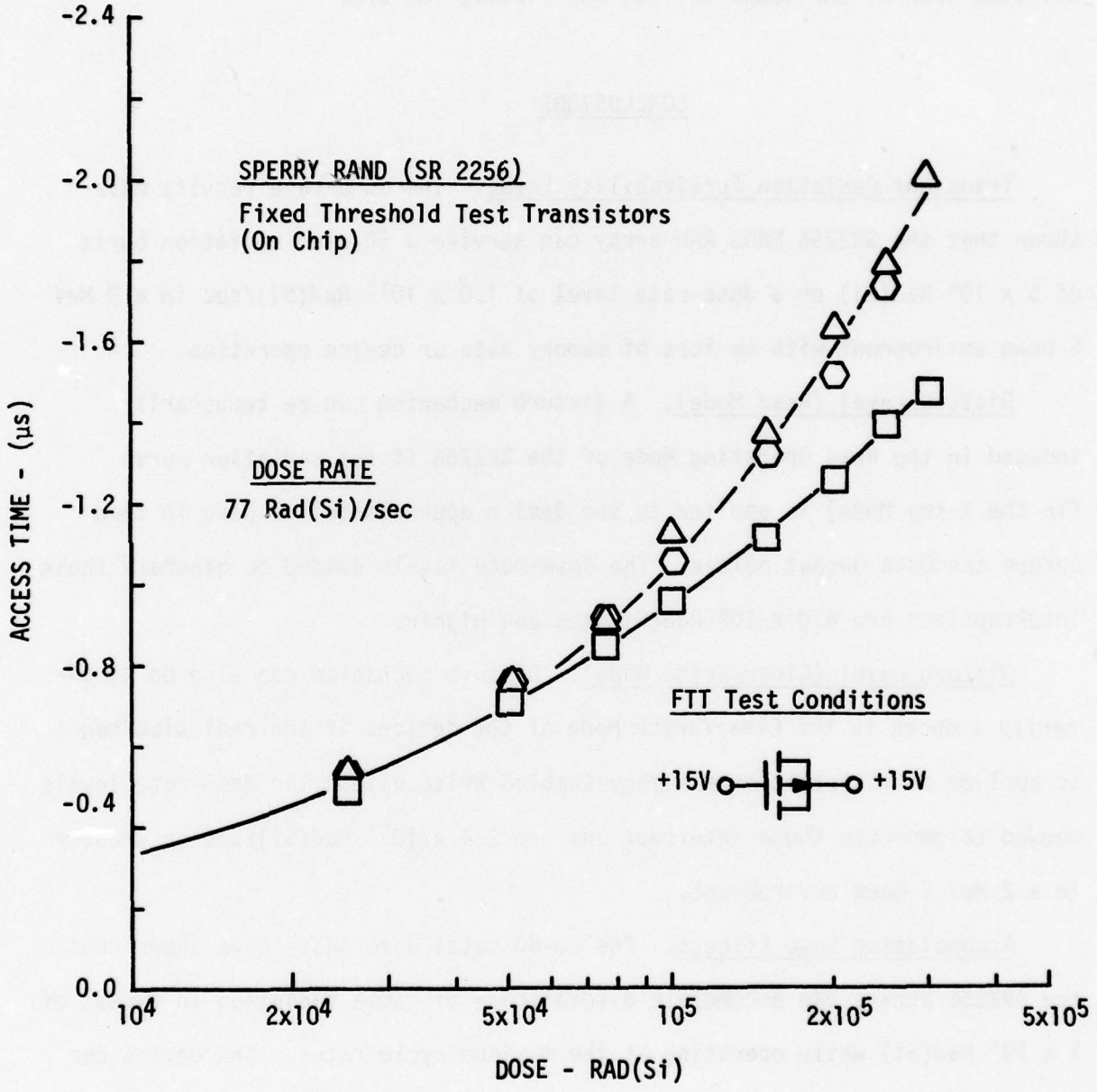


Figure 10. Co-60 Data. Gate Threshold Shifts of SR2256 Fixed Threshold Test Transistors versus Gamma Dose.

could no longer be cleared, written, or read correctly even though the internal MNOS memory transistors showed no signs of malfunction. The implication of these results is that some PMOS transistors within the peripheral circuitry of the array suffered similar gate shifts which resulted in overall slow-down of the total device, and finally failure.

CONCLUSIONS

Transient Radiation Survivability Level. The dose-rate results have shown that the SR2256 MNOS RAM array can survive a 50 nsec radiation burst of 5×10^4 Rad(Si) or a dose-rate level of 1.0×10^{12} Rad(Si)/sec in a 2 MeV E-beam environment with no loss of memory data or device operation.

Disturb Level (Read Mode). A disturb mechanism can be temporarily induced in the Read Operating Mode of the SR2256 if the radiation burst (in the X-ray Mode) is applied to the device approximately 1 μsec in time before the Data Output pulses. The dose-rate levels needed to generate these interruptions are 4.0×10^8 Rad(Si)/sec and higher.

Disturb Level (Clear/Write Mode). Disturb mechanism can also be temporarily induced in the Clear/Write Mode of the devices if the radiation burst is applied at the start of a Memory Enabled Write gate. The dose-rate levels needed to generate these interruptions are 2.4×10^{11} Rad(Si)/sec or greater in a 2 MeV E-beam environment.

Accumulating Dose Effects. The Co-60 total dose tests have shown that the SR2256 arrays can accumulate a total dose of gamma radiation in excess of 1×10^5 Rad(Si) while operating at the maximum cycle rates. The device can survive up to 3×10^5 Rad(Si) at reduced cycle rates. Total failure of the devices was attributed to permanent Gate-Threshold-Shifts (radiation induced) in the PMOS peripheral circuitry.

DISCUSSION

The results of this effort showed that a radiation hardened LSI MNOS RAM using bulk silicon technology can be built. This can be seen by comparing the test results of the SR2256 with the two previously tested commercial PMOS MNOS arrays (the ER 3400 and the NCM 7040). See table below.

	Read Disturb [Rad(Si)/s]	Write Disturb [Rad(Si)/s]	Survival [Rad(Si)/s]	Total Dose [Rad(Si)]
Sperry Rand SR 2256	4.0×10^{8}	2.4×10^{11}	1.0×10^{12}	$2 - 3 \times 10^{5}$
General Inst. ER 3400	1.1×10^{8}	3.1×10^{8}	9.0×10^{11}	$4 - 5 \times 10^{4}$
Nitron's NCM 7040	2.0×10^{7}	2.5×10^{7}	7.0×10^{11}	$2 - 3 \times 10^{4}$

The above comparisons show that the SR2256 is harder in all categories, with the most noted improvements in the "Write Disturb" and the "Total Dose" area. The Write Disturb hardness for the SR2256 shows an improvement of at least several orders of magnitude over the two commercial devices, and the total dose hardness is an improvement of approximately one order of magnitude. However, it was also concluded that there were several areas for potential improvement, mainly in the speed, power and total dose hardness of the memory peripherals.

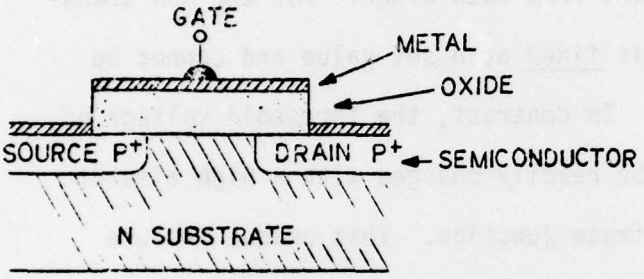
In the above SR2256 tests, data taken on the special PMOS test transistors

incorporated in each memory chip indicated that the total dose failure was due to radiation induced gate-threshold-shifts in the PMOS peripheral and not the failure of the MNOS memory bits. There was general agreement on this finding, and it was concluded that the problem area was associated with the gate oxide thickness of the PMOS peripherals. It was the opinion of Sperry Rand that the thinner the gate insulator, the smaller the gate-threshold-shift under radiation (see Reference 2). In the SR2256, the thinnest gate insulator that could be used, and still withstand the 30 volt Write voltage, was estimated to be 1000 Angstroms. However, because of initial yield problems, this minimum thickness was never realized. As a result, the total dose hardness level was less than optimum. It was felt, that the optimum condition could be obtained through "fine-tuning" of process controls and a reduction of the die size. However, even if the optimum condition was obtained, there would still exist a larger need for an MNOS memory with lower power consumption, faster Access Time, and a larger bit density than the SR2256. To get these improvements, the AFWL felt that a different peripheral technology had to be used. The present PMOS technology could not deliver the desired low power and high speed requirements needed for a competitive radiation hardened RAM. As a result, the AFWL is now engaged in a joint effort with Sandia Laboratories to develop an MNOS compatible, radiation hardened CMOS process leading to a radiation hard bulk silicon CMOS/MNOS RAM array with low power and high speed.

APPENDIX A

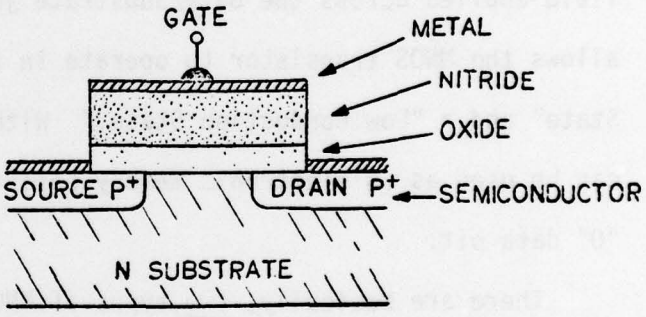
THE MNOS MEMORY TRANSISTOR

The MNOS memory transistor is basically a double layer Insulated-Gate-Field-Effect-Transistor (IGFET) operating in the Enhancement Mode. The device is closely related to the MOS transistor, for both of their active regions are described by a vertical metal-insulator-semiconductor structure (See Figure A1).



(A)

SCHEMATIC REPRESENTION OF A P-CHANNEL ENHANCEMENT MODE MOS TRANSISTOR



(B)

SCHEMATIC REPRESENTION OF A MNOS MEMORY TRANSISTOR

Figure A1.

The major physical difference between the MOS and the MNOS devices is in the construction of the gate insulator. The gate insulator of the MOS transistor is composed of a single layer of silicon oxide. In the MNOS device, the gate region has a two insulator structure (silicon-nitride on top of silicon-oxide).

The electrical operation of these two devices is also similar. Some of these similarities are: (1) a current channel must be created between the Source and Drain terminals, (2) this current channel is controlled by a voltage applied across the Gate/Substrate junctions, and (3) the Gate voltage that initiates current flow through this channel is called the "Gate Threshold Voltage."

It is this last similarity (the Gate Threshold Voltage) that also sets the MOS and the MNOS transistor apart from each other. For the MOS transistor, the Gate Threshold Voltage is fixed at a set value and cannot be changed by normal operating means. In contrast, the threshold voltage of a MNOS device is variable and can be readily changed with a high electric field applied across the Gate/Substrate junction. This unique feature allows the MNOS transistor to operate in two states, a "High Conduction State" and a "Low Conduction State." With this capability, the MNOS device can be used as an electronic memory cell to store a logic "1" or a logic "0" data bit.

There are basically, two types of MNOS memory transistors; (1) the "Forward Write" device, and (2) the "Reverse Write" device. The Forward Write transistor requires a large positive voltage on the Gate to Write the memory into the High Conduction State, and a large negative voltage to Write a Low Conduction State. For the Reverse Write transistor, the procedure is reversed. A large positive Gate voltage will Write a Low Conduction State, and a large negative voltage will Write a High Conduction State.

The MNOS memory transistor that is used exclusively today is the Forward Write device. The Gate of this device consists of a thin layer of

oxide (less than 35 Angstroms), covered by 200 to 500 Angstroms of nitride. This memory distinguishes itself from the Reverse Write device in that the mechanism that writes a memory in the forward device is due mainly to charge transport (tunneling) through the thin gate oxide. This tunneling occurs for both electrons and holes.

Figure A2 illustrates the negative charge tunneling that shifts the Forward Write memory into a High Conduction State. This mechanism is made possible

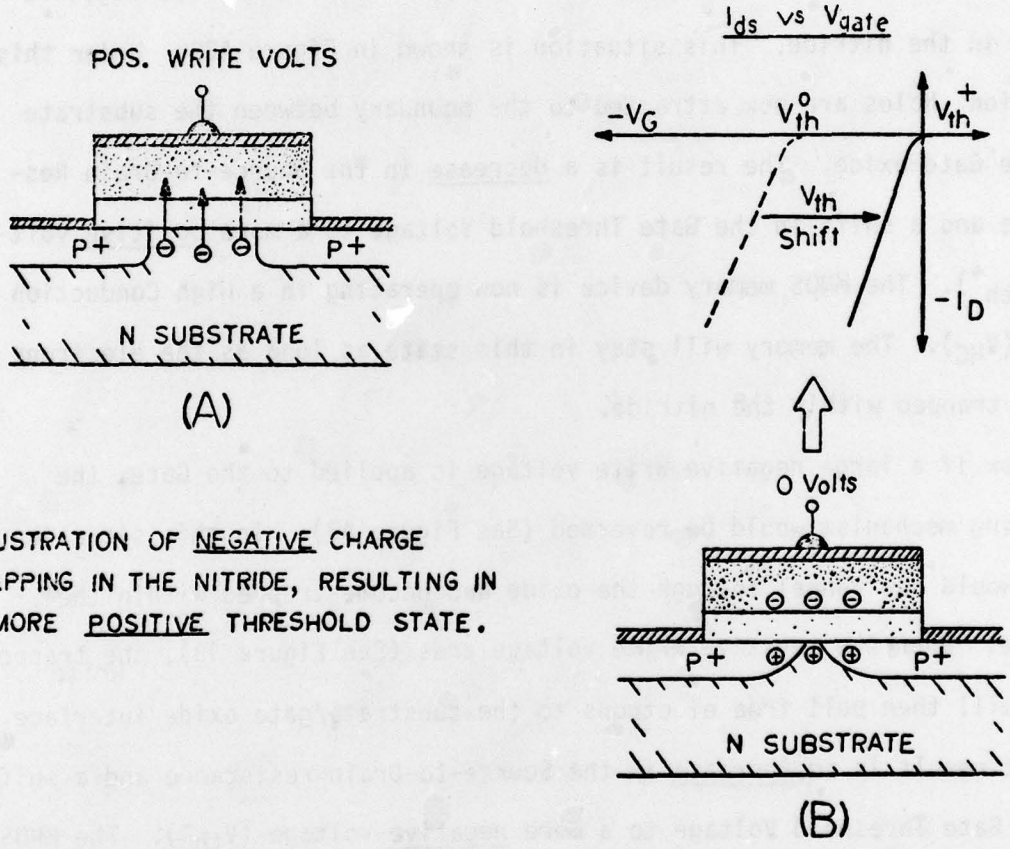


Figure A2. Illustrations of a Forward Write MNOS Memory Transistor being electrically Shifted into a more Positive Threshold or High Conduction State.

by applying a large positive Write voltage across the Gate/Substrate junction, creating an electric field that draws electrons from the substrate, to the

oxide-semiconductor interface. Because of the thinness of the Gate oxide, these electrons would have a high probability of penetrating the oxide and some parts of the nitride by quantum-mechanical tunneling (See Figure A2A). As a result, electrons soon become trapped in deep states within the nitride, most likely near the nitride-oxide interface. Saturation occurs when the field across the oxide due to the trapped electrons equals the field due to the externally applied Write voltage. When the positive Write voltage is removed from the Gate, the device is left with a net negative charge in the nitride. This situation is shown in Figure A2B. Under this condition, holes are now attracted to the boundary between the substrate and the Gate oxide. The result is a <u>decrease</u> in the Source-to-Drain Resistance and a shift in the Gate Threshold Voltage to a more <u>positive</u> voltage (V_{th}^{+}). The MNOS memory device is now operating in a High Conduction State (V_{HC}). The memory will stay in this state as long as the electrons remain trapped within the nitride.

Now if a large negative Write voltage is applied to the Gate, the tunneling mechanism would be reversed (See Figure A3). In this situation, holes would now tunnel through the oxide and become trapped within the nitride. When the negative Write voltage ends (See Figure 3B), the trapped holes will then pull free electrons to the substrate/gate oxide interface. The net result is an <u>increase</u> in the Source-to-Drain resistance and a shift in the Gate Threshold Voltage to a more <u>negative</u> voltage (V_{th}^{-}). The MNOS memory device is now operating in a Low Conduction State (V_{LC}). Again, the memory will remain in this state as long as the excess holes remain trapped within the nitride. Note however, that the trapped charge will eventually decrease (through leakage and recombination), and the Gate

Threshold Voltage will shift to a "stable" condition (no memory stored). This stable state is labeled V_{th}^{o} in Figures A2 and A3.

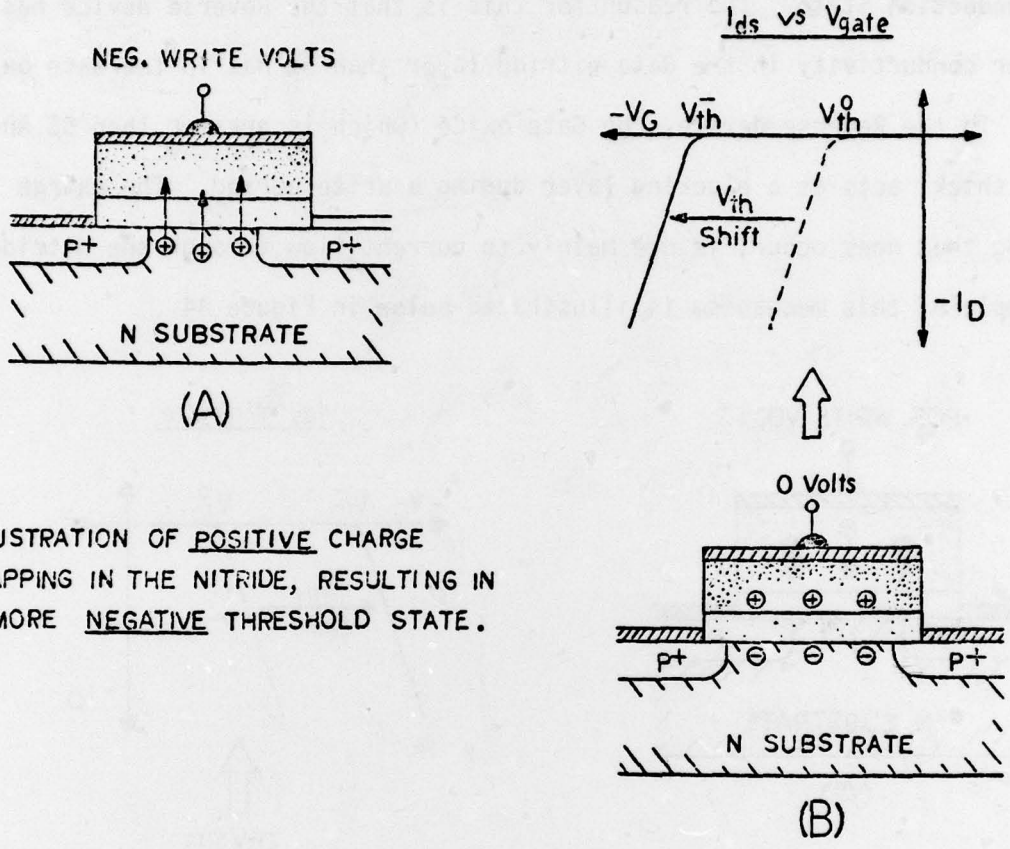


Figure A3. Illustrations of a Forward Shifting MNOS Memory Transistor being electrically Written into a More Negative Threshold or Low Conduction State.

A more detailed discussion of the above mechanisms of charge transport in Forward Write MNOS memory devices is presented below in Reference A1.

A second type (but less known) MNOS memory device is the Reverse Write transistor. The electrical operation of this transistor is just the opposite

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A1. Chang, J.J., Theory of MNOS Memory Transistor, IEEE Transactions on Electron Devices, ED-24, pp 511-518, May 1977.

from that of a Forward device. That is, a large positive Gate voltage will Write a Low Conduction State, and a large negative voltage will Write a High Conduction State. The reason for this is that the Reverse device has a higher conductivity in the Gate nitride layer than it has in the Gate oxide layer. In the Reverse device, the Gate oxide (which is greater than 35 Angstroms thick) acts as a blocking layer during a Write period. The charge trapping that does occur, is due mainly to current flow through the nitride. An example of this mechanism is illustrated below in Figure A4.

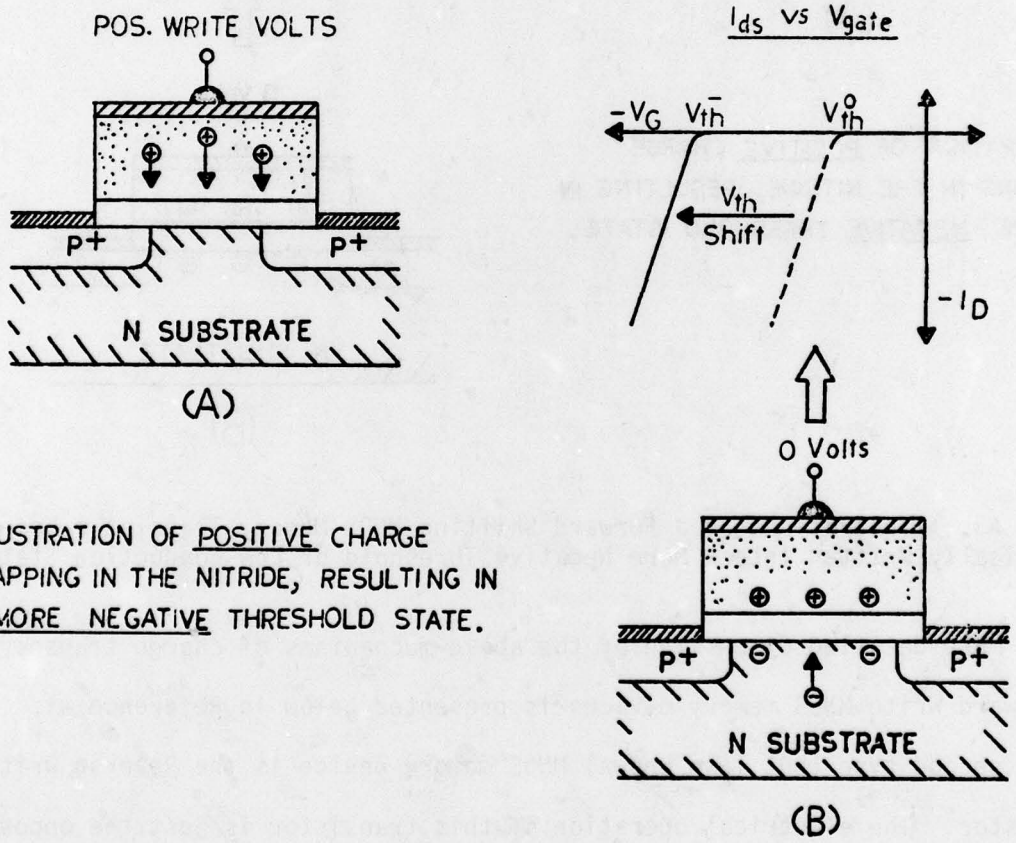

ILLUSTRATION OF POSITIVE CHARGE TRAPPING IN THE NITRIDE, RESULTING IN A MORE NEGATIVE THRESHOLD STATE.

Figure A4. Illustrations of a Reverse Write MNOS Memory Transistor being electrically written into a More Negative Threshold or Low Conduction State.

Figure A4A shows that when a large positive voltage is applied to the

Gate of the Reverse device, positive charge will flow from the Gate terminal, through the nitride and become trapped at the nitride/oxide interface. When the positive Gate voltage is removed (See Figure A4B), a net positive charge is left trapped near the interface. Under this condition, electrons are attracted to the substrate/oxide interface resulting in an increase in the Source-to-Drain resistance and a shift in the Gate Threshold Voltage to a more negative voltage (V_{th}^-). The memory is now operating in a Low Conduction State (V_{LC}).

To drive a Reverse device into a High Conduction State (V_{HC}), a large negative Write voltage is required (See Figure A5). In this case, electrons

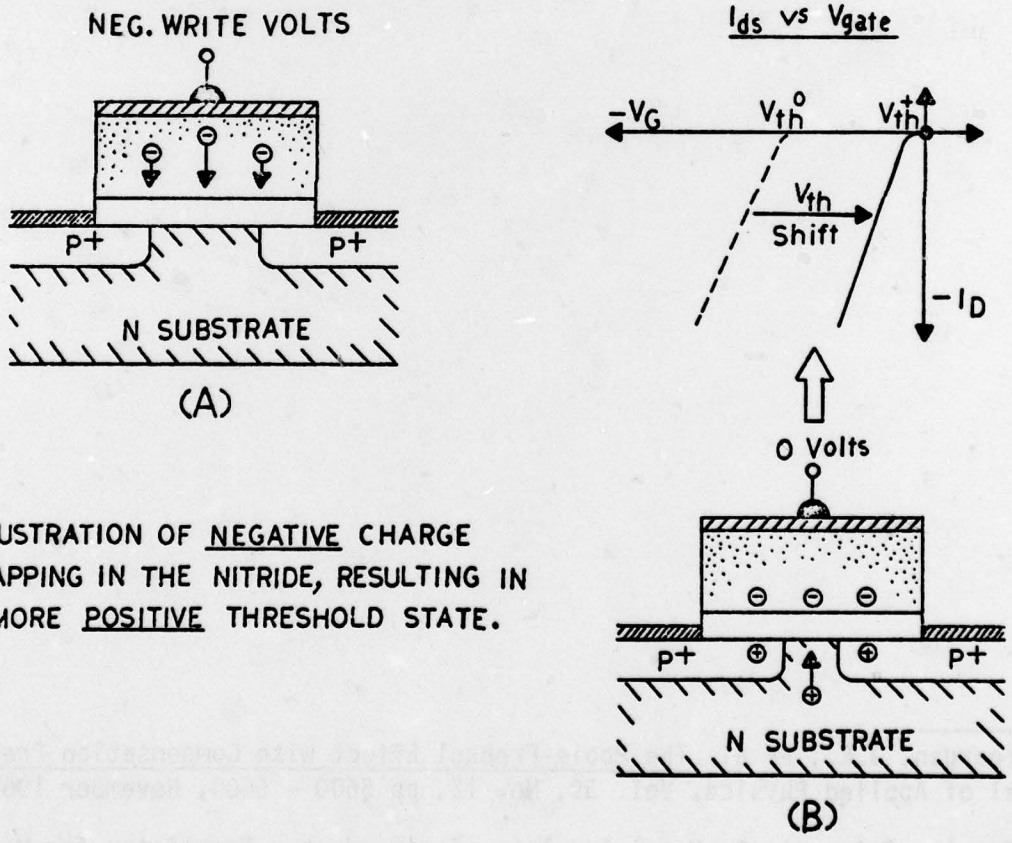

ILLUSTRATION OF NEGATIVE CHARGE TRAPPING IN THE NITRIDE, RESULTING IN A MORE POSITIVE THRESHOLD STATE.

Figure A5. Illustrations of a Reverse Write MNOS Memory Transistor being electrically written into a More Positive Threshold or High Conduction State.

will now flow through the conductive nitride and become trapped at the nitride/oxide interface. When the negative Write voltage ends, the trapped electrons will pull holes up to the other side of the interface (See Figure A5B). The Source-Drain resistance will now be decreased and the Gate Threshold Voltage will shift to a more positive voltage (V_{th}^{+}). The device is now in the High Conduction State (V_{HC}).

A more detailed discussion of the Write mechanisms in a Reverse Write MNOS memory device is available in References A2 and A3.

A2. Yeargan, J.R., et al. The Poole-Frenkel Effect with Compensation Present, Journal of Applied Physics, Vol. 39, No. 12, pp 5600 - 5604, November 1968.

A3. Sewell, F.A., et al. Metal Insulator Semiconductor Transistor for Use as a Nonvolatile Read-Write Memory Element, Technical Report AFAL-TR-71-170, July 1971.

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