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RELIABILITY TEST AND EVALUATION OF MIL-M-38510 LINEAR MICROCIRCUITS

McDonnell Douglas Astronautics Company

Roy C. Maurer

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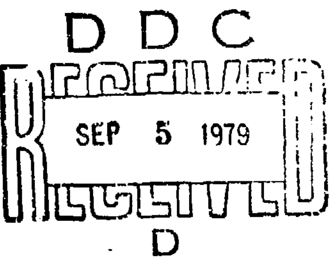

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APPROVED:

W. KEITH CONROY, JR.
Project Engineer

APPROVED:

JOSEPH J. NARESKY
Chief, Reliability & Compatibility Division

FOR THE COMMANDER:

JOHN P. HUSS
Acting Chief, Plans Office

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The objective of this effort is to provide analysis and evaluation of high reliability linear microcircuits to assure adequate test methods, reliability prediction and specification for high reliability Air Force Electronics. Data from this effort including processing information, materials, design characteristics, electrical measurements, temperature coefficients, stabilities, application information, test methods, burn-in procedures, specification, and reliability data will be used by the Government to assure high reliability in systems using these devices.

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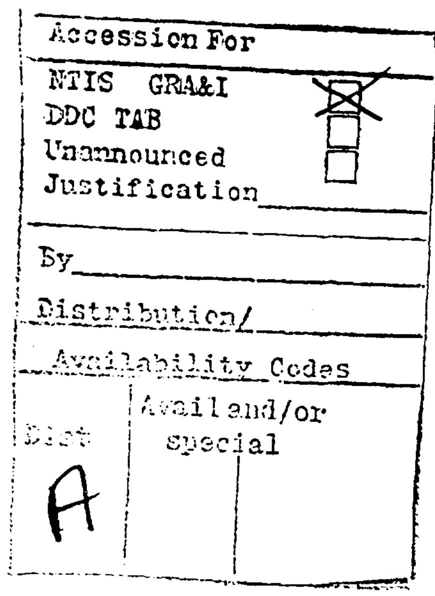
PREFACE

The work described in this report was performed by the Parts Evaluation Laboratory section of the McDonnell Douglas Astronautics Company-St. Louis Engineering Reliability department during the period between July 1976 and November 1978. The work was performed for the USAF Rome Air Development Center under Contract Number F30602-76-C-0371. The RADC project engineer was W. Keith Conroy. Significant technical contributions were made by Messrs. Gordon Johnson, Gary Keller, Ron Mackin, Michael Roberts and Edward Sisul.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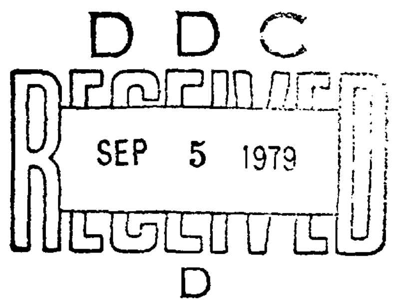

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EVALUATION

It is usually desirable, but not always possible, to fully characterize and evaluate the reliability of linear microcircuits before a MIL-M-38510 detail specification is generated. The specification must be verified to prevent manufacturers from qualifying inferior products either because the specification doesn't accurately reflect the screening conditions that were intended, or these conditions, however accurate, are insufficient. In this effort, both the selected linear devices and their respective detail slash sheets were evaluated. After the specifications were verified, sample parts were screened to the verified specification, stressed, and tested in order to measure their fitness for military applications. The result of this screening and testing is a reliability determination based on a failure rate extrapolation. The reliability data generated in this contractual effort will be used to determine which vendors of the products tested have potential for supplying reliable, military grade linear microcircuits, and also to provide some insight into the state of the art in linear microcircuit production. In addition, the vendors participating in this study can use the failure analysis data provided to improve their product which will result in increased yield, higher reliability, and lower cost. Recommendations for improvement of the procurement specification will be implemented in both MIL-STD-883, "Test Methods and Procedures for Microelectronics," and MIL-M-38510, "General Specification for Microcircuits," resulting in an improved standard for procuring reliabile linear microcircuits as part of the R5B TPO thrust in Solid State Device Reliability.

W. Keith Conroy Jr.

W. KEITH CONROY, JR.
Project Engineer

1.0 INTRODUCTION

The objective of this program was to evaluate the reliability of selected MIL-M-38510 linear microcircuits. Included in the evaluation were a) device electrical characterizations, b) analyses of device physical characteristics, c) determinations of device thermal characteristics, and d) high temperature accelerated test studies of device aging characteristics. Results of the evaluation were intended to provide information related to the following:

a) Adequacy of MIL-M-38510 specifications and test methods of the selected linear devices,
b) Relationship of device physical characteristics and processing techniques to device reliability,
c) Failure mechanisms,
d) Failure distributions at accelerated test conditions, and
e) Arrhenius model parameters and failure rates.

This report provides a general description of the overall program and presents the results of tests and evaluations performed prior to, during, and subsequent to long-term high temperature accelerated life tests. Included in these tests are all tests and evaluations required as a prerequisite to initiating long-term high temperature life testing, as well as the interim and final electrical measurements, results of characterization testing, analysis of failed devices, and analysis of failure data to determine device aging characteristics.

2.0 PROGRAM DESCRIPTION

The overall reliability test and evaluation of the MIL-M-38510 linear microcircuits program is depicted in Figure 1. A total of five device types from two manufacturers each were included in the program. The specific device types and manufacturers are shown in Table 1. At the time of procurement both the LM109 and the 78M05 devices were specified in MIL-M-38510/10701 as electrically equivalent 5 volt regulators, and the LM109 was only available from Manufacturer B. Therefore, the Manufacturer D 78M05 was used as the second source for the LM109 regulator. However, for clarity, the Manufacturer D device is referenced as a LM109 throughout this report. A total of 150 of each manufacturer's device type were procured to MIL-M-38510 Class B, or equivalent processing requirements. Upon receipt at MDAC-St. Louis, all devices were subjected to external visual examination, hermeticity tests and electrical tests. The electrical testing consisted of MIL-M-38510 Group A, dc tests at 25°C, -55°C and 125°C. However, when a high percentage of devices failed to meet the MIL-M-38510 parameter limits, the end-point limits were adjusted as required, to obtain an adequate number of devices for accelerated life testing.

Subsequent to performing the initial examinations and tests, acceptable devices were assigned by serial number to test groups. Device allocation for each manufacturer's device type is shown in Figure 1.

Electrical characterization testing was performed to provide a complete description of the electrical characteristics of each manufacturer's device type. The testing included, in addition to the initial dc electrical tests performed with all devices, sample tests of ac parameters and transfer characteristics.

Construction analyses require destructive physical analyses to determine construction methods, manufacturing process techniques and workmanship used in the fabrication of devices. Results were used to predict potential reliability problems, determine possible accelerated life test limitations (due to materials used in device fabrication), and to facilitate subsequent failure analyses.

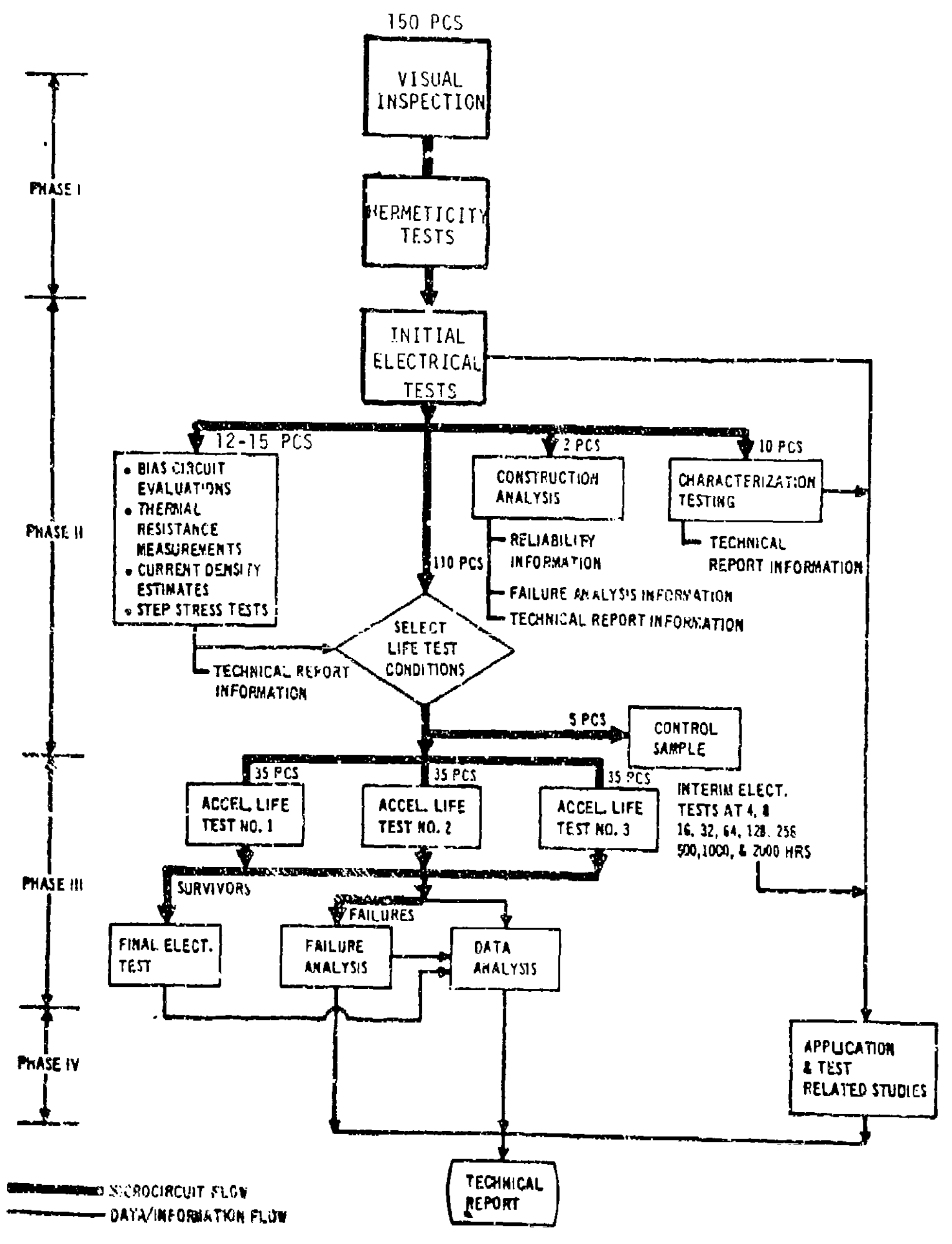


FIGURE 1. LINEAR MICROCIRCUIT TEST PROGRAM

TABLE 1. LINEAR MICROCIRCUIT TYPES

M38510 PART NO. REFERENCE	COMMERCIAL PART NO.	PART TYPE	MFR	PROCUREMENT SPEC
M38510/10104 BGC	LM108A	OPERATIONAL AMPLIFIER	A B	MFR'S ELECTRICAL* MFR'S ELECTRICAL*
M38510/10107 BGC	LM118	OPERATIONAL AMPLIFIER, HIGH SPEED	C B	MFR'S ELECTRICAL* MRF'S ELECTRICAL*
M38510/10201 BIC	723	PRECISION VOLTAGE REGULATOR	D C	JM38510 MFR'S ELECTRICAL*
M38510/10304 BGC	LM111	PRECISION VOLTAGE COMPARATOR/BUFFER	D B	MFR'S ELECTRICAL* MFR'S ELECTRICAL*
M38510/10701 BXC	78M05 LM109	VOLTAGE REGULATOR, 5 VOLT	D B	MFR'S ELECTRICAL* MFR'S ELECTRICAL*

* DEVICES WERE TO MEET THE MIL-M-38510 ELECTRICAL CHARACTERISTICS, BUT DID NOT NEED TO BE TESTED TO THESE REQUIREMENTS IF JAN TEST TAPES WERE NOT AVAILABLE.

The initial device studies were prerequisite to performing the accelerated life tests and included an evaluation of the MIL-M-38510 bias circuits for accelerated testing, development of new bias circuits as required, and thermal resistance measurements for computing device junction temperatures at anticipated test temperatures.

Three accelerated life tests were performed to provide information about device failure mechanisms, failure distributions and life acceleration factors. Actual life test temperatures were determined from results obtained in bias circuit evaluations and step-stress tests. Each life test was conducted for 4,000 hours or a minimum of 50% failure, whichever occurred first. Interim electrical tests were performed on life test devices after cool-down to room temperature with bias applied. These measurements consisted of MIL-M-38510 dc tests at 25°C and were performed at 4, 8, 16, 32, 64, 128, 256, 500, 1,000 and 2,000 hours of life testing. Unless otherwise directed by the Project Test Engineer, all parts that failed an interim test were removed from the life test and subjected to failure analysis. At the conclusion of each life test, surviving devices were subjected to the same set of MIL-M-38510 electrical tests performed prior to life testing.

A control sample of each manufacturer's devices was subjected to electrical testing each time the test devices were subjected to interim or final electrical tests. The purpose of the control sample was to provide a check on the long term stability of the automated test equipment.

Application and test related studies were performed to determine application-related reliability problems associated with system use of the linear devices included in this program. Application and test related experience derived throughout the program was used to develop design guides for items such as board layout, compensation, bypassing, and interfacing.

3.0 RESULTS OF PRE-LIFE TESTS AND EVALUATIONS

3.1 EXTERNAL VISUAL EXAMINATIONS AND HERMETICITY TESTS

Upon receipt at MDAC-St. Louis, all devices were examined for conformance to purchase order requirements for device type, package style, lead finish, and marking. Each device was examined at 3X magnification for evidences of gross damage to package, package seals, and leads. Fine and gross leak tests were then performed per MIL-STD-883, Method 1014.1, Conditions A1 and C2.

With one exception, no major visual or hermetic defects were found in the delivered devices. One manufacturer's devices were rejected for incorrect lead finish and were subsequently replaced. Results of examinations and tests performed with this manufacturer's replacement devices and all other manufacturers' devices are shown in Table 2.

Replacements for electrical test rejects were also subjected to visual examinations and hermeticity tests. Thus, the total quantity of devices shown in Table 2 exceeds, in some cases, the procurement quantity of 150 devices.

3.2 BASELINE ELECTRICAL PERFORMANCE TESTS

With the exception of the devices noted in Table 2, all devices surviving the initial visual inspections and hermeticity tests were subjected to electrical performance tests at 25°C, -55°C, and 125°C. These tests consisted of selected subgroups of the MIL-M-38510 Group A tests. Specific subgroups for the MIL-M-38510/10104 (LM108A), /10107 (LM118) devices were A1 through A6. Specific subgroups for the MIL-M-38510/10201 (723) and /10701 (LM109) devices were A1, A2, and A3. The specific subgroups for the /10304 (LM111) device were A1, A2, A4, and A5. LM111 testing at -55°C (Subgroups A3 and A6) was not performed due to device/test fixture oscillation at -55°C. Details of the electrical test conditions and end-point limits used for testing each device type are contained in Appendix B. In most cases the end-point limits are those contained in the current MIL-M-38510 slash sheet. However, in several instances the end-point limits were relaxed to obtain a sufficient number of "good" devices for subsequent testing. A summary of the MIL-M-38510 parameter

TABLE 2. INITIAL INSPECTION AND HERMETICITY TEST RESULTS

COMMERCIAL PART NO.	MANUFACTURER	VISUAL INSPECTION		HERMETICITY TESTS				TOTAL NO. FAILED DEVICES	SUBMITTED FOR ELECTRICAL TEST
				FINE LEAK		GROSS LEAK			
		NO. TESTED	NO. FAILED	NO. TESTED	NO. FAILED	NO. TESTED	NO. FAILED		
LM108A	A	198	0	198	1	197	3	4	194
	B	150	2	148	1	147	3	6	144
LM118	C	150	0	150	0	150	3	3	147
	B	150	0	150	3	147	0	3	147
723	D	150	2	148	1	147	0	3	147
	C	188	3	185	0	185	0	3	185
LM111	D	150	0	150	2	148	0	2	129 (1) (2)
	B	150	0	150	0	150	0	0	133 (1) (3)
7805	D	150	1	149	1	148	0	2	146
LM109	B	150	0	150	0	150	1	1	149

(1) 3 Devices used for construction analysis and 3 devices were subjected to Gas Mass Spectrometer Analysis.
(2) 13 Devices used for test fixture development.
(3) 11 Devices used for test fixture development.

limits that were revised is shown in Table 3. Results of the initial electrical testing using the revised end-point limits are summarized in Table 4. Parametric data taken at 25°C is shown for each device type in Tables 5 thorugh 9. The tables providing parametric data contain the parameter limits, a computed mean value of the parameter for all devices meeting the revised specification limits, and a computed standard deviation of the measured parameter values. Examination of the test data revealed no marked differences between manufacturers for the majority of parameters. However, the gain tests on both the LM108A and LM118 devices do show a difference of approximately one order of magnitude. This is caused by nonlinearities in the dc transfer responses and is discussed in more detail in Appendix E. Also the I_{IO} values for the LM118 devices differ by an order of magnitude. The LM109 also exhibited an appreciable difference in line regulation (V_{RLN}) and load regulation (V_{RLD}) parameters. Manufacturer D's devices exhibited better line regulation while Manufacturer B's devices exhibited better load regulation. The Manufacturer D device was actually a 78M05 device, and has different circuit design which accounts for the differences in these characteristics.

The only JAN qualified device was Manufacturer D's MIL-M-38510/10201 of which five devices were rejected. There were two visual, one hermetic, and two electrical failures noted in the initial examination of the JAN devices. All data on the failed devices can be found in Appendix G.

3.3 MICROCIRCUIT CONSTRUCTION DETAILS

A destructive physical analysis of at least two of each manufacturer's device type was performed to determine the materials, construction methods, process techniques and quality of workmanship used in the device fabrication. Complete results of these analyses including schematics and chip topography are contained in Appendix A. With the exception of the basic package type and material, no major construction differences were noted between manufacturers' device types. All devices had the following construction characteristics in common, a) aluminum internal wire and chip metalization, b) gold plated Kovar external lead and internal post, c) gold-silicon die attach, and d) a welded

TABLE 3. REVISED MIL-M-38510 PARAMETER LIMITS

MIL-M-38510 SLASH SHEET	SUBGROUP	PARAMETER (TEST NO.)	MIL-M-38510 LIMIT		REVISED LIMIT		UNITS
			MIN	MAX	MIN	MAX	
10104	1	+PSRR	0	16	-16	+6	µV/V
	1	-PSRR	0	16	-16	16	µV/V
(LM108A)	1	$-I_{OS}$	2.0	15	2.0	20	nA
	2	I_{IC}	-0.2	+0.2	-0.3	+0.3	mA
	2	$+I_{IB}$	-2.0	+2.0	-3.0	+3.0	mA
	2	$-I_{IB}$	-2.0	+2.0	-3.0	+3.0	nA
	3	$+I_{IB}$	-0.1	+3.0	-0.1	+4.0	nA
	3	$-I_{IB}$	-0.1	+3.0	-0.1	+4.0	nA
	3	$-I_{OS}$	4.0	15.0	4.0	40	mA
10107 (LM110)	1	V_{IC}	-3.0	+3.0	-4.0	+4.0	mV
	1	+PSRR	0	100	-100	+100	µV/V
	1	-PSRR	0	100	-100	+100	µV/V
	1	$-I_{OS}$	12	40	12	55	mA
	2	V_{IC}	-4.0	+4.0	-7.0	+7.0	mV
	2	$-I_{OS}$	12	40	10	90	mA
	3	V_{IC}	-4.0	+4.0	-7.0	+7.0	mV
	3	$I_{OS}(-)$	15	55	15	70	mA
	5	$-A_{VS}$ (80)	40	---	3	---	V/mV
	5	$+A_{VS}$ (83)	40	---	20	---	V/mV
	5	$-A_{VS}$ (84)	40	---	20	---	V/mV
	5	$+A_{VS}$ (85)	40	---	20	---	V/mV
	5	$-A_{VS}$ (86)	40	---	20	---	V/mV
	6	$+A_{VS}$ (89)	40	---	20	---	V/mV
	6	$-A_{VS}$ (90)	40	---	20	---	V/mV
	6	$+A_{VS}$ (91)	40	---	20	---	V/mV
	6	$-A_{VS}$ (92)	40	---	20	---	V/mV
	6	$+A_{VS}$ (93)	40	---	4	---	V/mV
	6	$-A_{VS}$ (94)	40	---	4	---	V/mV
	6	$+A_{VS}$ (95)	40	---	4	---	V/mV
	6	$-A_{VS}$ (96)	40	---	4	---	V/mV
10701	1	I_{SCD} (LINE)	-0.8	0	-0.8	+0.8	mA
(LM109)	1	I_{OS}	-0.7	-0.1	-2.0	-0.1	A
	2	V_{OUT}(17)	4.75	5.75	4.50	5.25	
	2	V_{RLOAD}	-75	+75	-500	+500	mV
	3	V_{START}	---	9	---	---	V

MIL-M-38510 SLASH SHEET	SUBGROUP	PARAMETER (TEST NO.)	MIL-M-38510 LIMIT		REVISED LIMIT		UNITS
			MIN	MAX	MIN	MAX	
10304 (LM111)	1	V_{IO}	-2	+2	-4	+4	mV
	1	$V_{IO(R)}$	-2	+2	-4	+4	mV
	1	I_{IB}	-100	+0.1	-150	+0.1	nA
	1	I_O	0	10	0	500	nA
	1	I_G	-0.1	0	-10	0	uA
	1	I_{I1}	0	20	0	100	nA
	1	I_{I2}	0	20	0	100	nA
	2	V_{IO}	-3	+3	-5.5	+5.5	mV
	2	$V_{IO(R)}$	-4	+4	5.5	+5.5	mV
	2	I_{IB}	-100	0.1	-150	0.1	nA
	2	I_G	[illegible]	0	-100	0	uA
	2	I_{I1}	0	20	0	500	nA
	2	I_{I2}	0	20	0	500	nA
	2	$V_{IO(ADJ)+}$	5	-	4	-	mV
	2	$V_{IO(ADJ)-}$	5	-	4	-	mV
	2	CMR	80	0	75	-	dB
	3	ALL	-	-	DELETED		mV
	4	A_{VE}	50	-	DELETED		mV
	5	A_{VE}	10	-	DELETED		mV
	6	ALL	-	-	DELETED		-
	1	$V_{IO(ADJ)+}$	5	-	4	-	mV
	1	$V_{IO(ADJ)-}$	5	-	4	-	mV

TABLE 4. INITIAL ELECTRICAL TEST RESULTS

PART NO.	MFR	NO. INTO TEST	FAILURES 25°C	125°C	-55°C	TOTAL	AVAILABLE FOR TEST
723	D	147	6	4	4	6 (1)	141
723	C	185	40	9	39	62	123
LM108A	B	144	4	17	9	27	117
LM108A	A	194 (4)	42	13	10	51	143
LM118	C	147	2	11	0	13	134
LM118	B	147	4	6	5	13	134
LM109	B	149	5	4	6	13	136
LM109	D	148	0	10	136 (2)	10	138
LM111	B	133	4	4	(3)	4	129
LM111	D	129	4	3	(3)	4	125

Four (4) parts were destroyed by test equipment failure.

Two (2) parts also failed at 125°C. The remaining 134 were -55°C V_{START} parameter test failures which were ignored for the life test program.

The -55°C tests were not performed for this device due to excessive oscillation.

Of the 194 devices which were submitted for electrical tests, 28 devices failed the initial 25°C electrical tests and were returned to the manufacturer for replacements. Since the 125°C and -55°C electrical tests were not performed on the 28 returned devices only 166 devices were tested at -55°C and 125°C.

TABLE 5. M38510/10104 (LM108A) INITIAL ELECTRICAL 25°C PARAMETER CHARACTERIZATION

PARAMETER	TEST NOS.	LIMITS		MANUFACTURER B		MANUFACTURER A		UNITS
		MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	
V_{IO}	1-4	-0.5	+0.5	-0.007	0.204	-0.003	0.137	mV
$+A_{VS}$	71	80	---	1,614	1,892	865.8	1,568	V/mV
$-A_{VS}$	72	80	---	1,920	3,039	203.5	87.26	V/mV
$+A_{VS}$	75	20	---	1,120	1,373	252.6	255.2	V/mV
$-A_{VS}$	76	20	---	2,934	8,859	141.4	47.95	V/mV
I_{IO}	5-8	-0.2	+0.2	-0.012	0.041	-0.007	0.026	nA
I_{IB}	9-12	-0.1	2.0	1.067	0.413	1.056	0.305	nA
$-I_{IB}$	13-15	-0.1	2.0	1.078	0.415	1.063	0.302	nA
+PSRR	17	0	16	0.470	1.636	2.438	0.903	µV/V
-PSRR	18	0	16	1.707	0.925	1.118	2.078	µV/V
CMR	19	96	---	124.7	8.916	121.124	7.240	dB
$+I_{OS}$	22	-15	-2.0	-5.406	0.155	-9.033	0.627	mA
$-I_{OS}$	23	2	20	11.41	0.269	12.289	4.302	mA
P_D	24	2	24	11.38	0.874	13.958	2.584	mW
V_{OP+}	67	16	---	19.493	0.090	19.167	0.078	V_P
V_{OP-}	68	---	-16	18.836	0.056	18.914	0.064	V_P

TABLE 6. M38510/10107 (LM118) INITIAL ELECTRICAL 25°C PARAMETER CHARACTERIZATION

PARAMETER	TEST NOS.	LIMITS		MANUFACTURER C		MANUFACTURER B		UNITS
		MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	
V_{IO}	1-4	-4.0	+4.0	0.053	1.273	-0.319	1.393	mV
$+A_{VS}$	69	80	---	2068	3915	151.9	29.11	V/mV
$-A_{VS}$	70	80	---	2966	8711	112.0	16.46	V/mV
$+A_{VS}$	71	80	---	964.4	2321	154.0	81.50	V/mV
$-A_{VS}$	72	80	---	140.9	129.9	174.9	65.18	V/mV
$+A_{VS}$	73	40	---	161.2	129.1	169.5	98.31	V/mV
$-A_{VS}$	74	40	---	228.9	778.1	115.9	18.21	V/mV
$+A_{VS}$	75	40	---	525.8	1037	123.2	70.73	V/mV
$-A_{VS}$	76	40	---	738.6	1852	1139.8	3037	V/mV
I_{IO}	5-8	-40	+40	-9.499	9.523	-0.317	6.401	nA
$+I_{IB}$	9-12	+1	250	173.5	31.44	108.0	23.82	nA
$-I_{IB}$	13-16	+1	250	187.0	31.23	111.2	24.05	nA
+PSRR	17	0	100	-14.768	10.15	-26.08	10.37	μV/V
-PSRR	18	0	100	-35.373	12.13	-14.95	6.447	μV/V
CMR	19	80	---	100.1	6.568	105.3	8.658	dB
$V_{IO\ ADJ(+)}$	20	7.5	---	16.92	1.193	12.52	0.830	mV
$V_{IO\ ADJ(-)}$	21	7.5	---	-16.83	1.397	-12.68	0.844	mV
$I_{OS}(+)$	22	-40	-12	-30.19	1.358	-31.18	1.205	mA
$I_{OS}(-)$	23	12	55	24.94	2.533	39.42	1.553	mA
P_D	24	10	280	204.3	11.65	262.6	9.72	mW
V_{OPP}	67	34	---	37.81	0.147	37.77	0.117	V_{P-P}
V_{OPP}	68	32	---	36.60	0.138	36.25	0.123	V_{P-P}

TABLE 7. M38510/10201 (723) INITIAL ELECTRICAL 25°C PARAMETER CHARACTERIZATION

PARAMETER	TEST NO.	LIMITS		MANUFACTURER D		MANUFACTURER C		UNITS
		MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	
V_{RLINE}	1	-0.10	0.10	-0.017	0.004	-0.019	0.011	% V_{OUT}
V_{RLINE}	2	-0.3	0.3	-0.117	0.029	-0.141	0.049	% V_{OUT}
V_{RLINE}	3	-0.2	0.2	-0.011	0.005	-0.013	0.010	% V_{OUT}
V_{RLOAD}	4	-0.15	0.15	-0.011	0.009	-0.007	0.010	% V_{OUT}
V_{RLOAD}	5	-0.5	0.5	0.000	0.014	0.001	0.005	% V_{OUT}
V_{RLOAD}	6	-0.2	0.2	0.003	0.008	0.003	0.003	% V_{OUT}
V_{REF}	7	6.95	7.35	7.243	0.056	7.208	0.097	V
I_{SCD}	8	0.5	3.0	2.472	0.143	2.185	0.412	mA
I_{OS}	9	45	85	59.19	5.217	58.58	2.801	mA

TABLE 8. M38510/10701 (LM109) INITIAL ELECTRICAL 25°C PARAMETER CHARACTERIZATION

PARAMETER	TEST NO.	LIMITS		MANUFACTURER D		MANUFACTURER B		UNITS
		MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	
V_{OUT}	1	4.80	5.20	5.039	0.061	5.044	0.042	Vdc
V_{OUT}	2	4.80	5.20	5.033	0.060	5.044	0.041	Vdc
V_{OUT}	4	4.80	5.20	5.061	0.063	5.029	0.044	Vdc
V_{RLN}	6	-20	+20	5.710	2.626	-17.388	1.908	mVdc
V_{RLD}	7	-50	+50	35.689	3.510	-2.798	2.626	mVdc
I_{SCD}	9	-10.0	0	-4.084	0.350	-7.168	0.342	mAdc
I_{SCD}	10	-10.0	0	-4.070	0.367	-7.224	0.367	mAdc
I_{SCD}	11	-10.0	0	-4.056	0.349	-7.130	0.368	mAdc
ΔI_{SCD}	12	-0.8	-0.8	0.014	0.047	-0.056	0.046	mAdc
ΔI_{SCD}	13	-0.5	0	-0.028	0.028	-0.038	0.067	mAdc
I_{OS}	14	-2.0	-0.1	-0.905	0.149	-1.221	0.003	Adc
V_{START}	15	---	9 0	5.017	0.061	5.037	0.046	Vdc

TABLE 9. M38510/10304 (LM111) INITIAL ELECTRICAL 25°C PARAMETER CHARACTERIZATION

PARAMETER	TEST NOS.	LIMITS		MANUFACTURER D		MANUFACTURER B		UNITS
		MIN	MAX	MEAN	SIGMA	MEAN	SIGMA	
V_{IO}	1-4	-4	+4	-.335	.414	-.243	.458	mV
$V_{IO(R)}$	5-7	-4	+4	-.743	.389	-.229	.467	mV
AVC+	92	150	-	459	73.3	925	1354	V/mV
AVC-	94	150	-	302	88.8	1371	2028	V/mV
I_{IO}	8-10	-10	+10	.678	1.66	1.24	1.18	nA
$I_{IO(R)}$	11	-25	+25	3.99	4.44	3.81	3.15	nA
I_{IB+}	12-14	150	+.1	-56.4	27.4	-53.8	14.7	nA
I_{IB-}	12-14	-150	+.1	-57.1	27.8	-55.0	15.0	nA
$V_{IO(ADJ)+}$	23	4	-	8.829	.289	5.22	.251	mV
$V_{IO(ADJ)-}$	24	-	4	-8.81	.290	-5.369	.266	mV
CMRR	25	75	-	105	5.76	110	5.95	dB
$V_{OL\ 1}$	26-27	0	.400	.230	.018	.276	.015	V
$V_{OL\ 2}$	28-29	0	1.500	.833	.021	.915	.037	V
I_O	16	0	.500	.123	.007	.123	.007	μA
I_G	17	-10	0	-.855	.966	-1.30	1.34	μA
I_{I1}	18	0	.100	.048	.003	.048	.003	μA
I_{I2}	19	0	.100	.049	.003	.048	.004	μA
$+I_{CC}$	20	.5	5.0	4.11	.244	3.25	.267	mA
$-I_{CC}$	21	-4.0	-.5	-2.95	.226	-2.306	.209	mA
I_{OS}	22	70	200	164	5.01	140	13.0	mA
PD	15	30	270	211	13.9	167	14.1	mW

lid seal. A summary of the differences in package type and material is shown in Table 10. There were no physical features observed that would have a major impact on life test results or would limit life test temperature to below 250°C.

Thirty devices (three of each manufacturer's device type) were subjected to Gas Mass Spectrometer Analysis. This analysis was performed by RADC and the results are shown in Table 11. Manfacturer D's 723 devices contained only traces of oxygen and carbon dioxide, but his LM111 devices contained significant amounts of water vapor, argon, and carbon dioxide. All of Manufacturer B's devices (LM108A, LM118, LM109, and LM111) contained only nitrogen and carbon dioxide, suggesting that this manufacturer has good control of the package atmosphere during device fabrication. Although surface related mechanisms are related to water vapor content in the package, the life test results disclosed no fference between devices with or without water vapor.

3.4 BIAS CIRCUIT LUATION

Short-term high temperature tests of a sample of each manufacturer's device type were conducted to a) verify the suitability of the MIL-M-38510 bias circuit for operating devices at ambient temperature up to 250°C, or b) evaluate candidate life test bias circuits for those device types that did not operate satisfactorily in the MIL-M-38510 bias circuit. A suitable bias circuit was considered to be one that maintained maximum rated voltage across the device without causing excessive current at ambient temperature up to 250°C. A constant output voltage over the desired life test temperature range was also desired.

The bias circuit tests indicated that the LM108A, LM109, and LM111 devices were capable of operating at temperatures up to 250°C without exhibiting thermal runaway. Thermal runaway was encountered with the 723 and LM118 devices, at ambient temperatures above 200°C.

TABLE 10. MICROCIRCUIT CONSTRUCTION DIFFERENCES

PART TYPE	MANUFACTURER	PACKAGE TYPE	PACKAGE MATERIAL
M38510/10104	B	TO-99	Nickel
LM108A	A	TO-99	Au Plated Nickel
M38510/10107	B	TO-99	Nickel
LM118	C	TO-99	Ni Plated Kovar
M38510/10201	C	10 Lead TO-5	Nickel
723	D	10 Lead TO-5	Nickel
M38510/10304	D	8 Lead TO-5	Nickel
LM111	B	8 Lead TO-5	Nickel
M38510/10701	B	TO-5	Nickel
LM109	D	TO-5	Nickel

TABLE 11. SUMMARY OF GAS MASS SPECTROMETER ANALYSIS

CONSTITUENT	CONCENTRATION % (V/V)									
	LM108A		LM118		LM109		723		LM111	
	MFR A	MFR B	MFR B	MFR C	MFR B	MFR D	MFR C	MFR D	MFR B	MFR D
NITROGEN	98.77	99.87	99.97	99.77	99.87	99.77	99.67	99.97	99.93	99.57
CARBON DIOXIDE	0.17	0.10	0.03	0.17	0.10	0.10	0.10		0.03	0.10
ARGON	0.33									0.30
WATER VAPOR	0.53			0.03		0.13	0.23			0.17
OXYGEN	0.20			0.03						

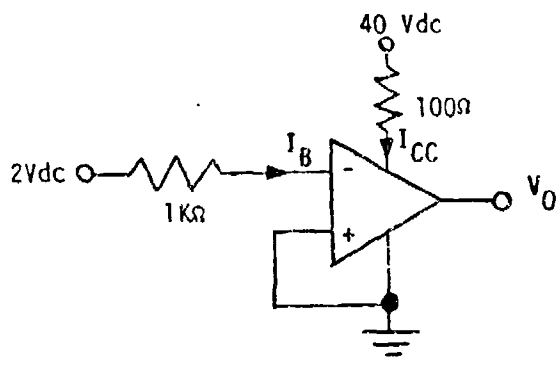
NOTE: VALUES ARE AVERAGES OF THREE DEVICES

The bias circuits used for each accelerated life test are shown in Figure 2. The details and results of the bias circuit evaluation are contained in Appendix D.

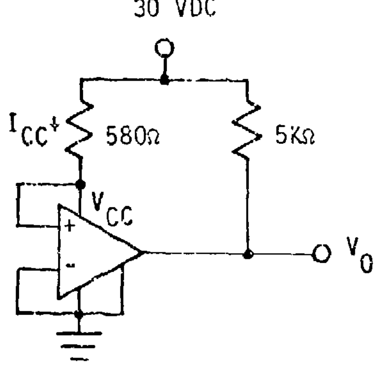
3.5 STEP STRESS TESTS

When a non MIL-M-38510 bias circuit was used, step stress testing was performed to evaluate that circuit and to obtain additional device failure data to aid in the final determination of accelerated life test conditions. Step stress testing was performed on the LM108A, LM118 and LM111 devices. Five of each manufacturer's devices were operated in the selected bias configuration for 16 hours in a test oven at 75°C. After 16 hours of operation at 75°C, devices were allowed to cool down under bias, and electrical testing was performed at 25°C. The surviving devices were then returned to test at an ambient temperature of 100°C for an additional 16 hours of operation. This sequence was repeated in 25°C increments until all surviving devices experienced thermal runaway at 275°C. Thermal runaway was not observed in the LM111 devices. The results of the LM108A, LM118, and LM111 step stress tests are shown in Table 12.

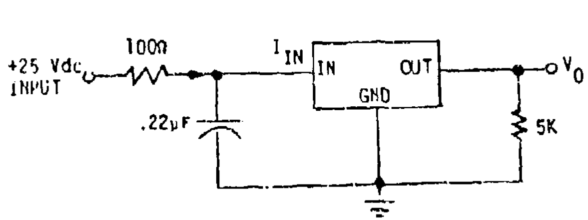
With the exception of the Manufacturer C LM118 devices, all LM108A and LM118 failures were due to bake-recoverable surface related mechanisms. The Manufacturer C LM118 devices experienced a thermal runaway failure mode at 200°C and exhibited melted open metalization due to excessive current. Prior circuit evaluation tests had indicated a thermal runaway problem above 225°C. Thermal runaway was not observed with the Manufacturer B LM118's since all devices had failed after the 150°C step due to a surface related mechanism. As a result of these findings, LM118 life test temperatures were limited to a maximum of 175°C to avoid thermal runaway and to enhance the failure time resolution of Manufacturer B devices at the maximum test temperature.



MIL-M-38510/10104 (LM108A)
MIL-M-38510/10107 (LM118)



MIL-M-38510/10304 (LM111)



MIL-M-38510/10701 (LM109)

MIL-M-38510/10201 (723)

FIGURE 2. ACCELERATED LIFE TEST BIAS CIRCUITS

TABLE 12. STEP STRESS RESULTS

MANUFACTURER	P/N	CUMULATIVE NO. OF FAILURES									NOTES
		75°C	100°C	125°C	150°C	175°C	200°C	225°C	250°C	275°C	
B	LM108A	0	0	1	2	3	3	4	4		2,4
A	LM108A	0	0	0	0	0	0	0	0		2
B	LM118	0	0	3	5	---	---	---	---		4
C	LM118	0	0	0	0	0	1	1	2	4	3,5
B	LM111	---	---	---	---	3	3	3	3	5	6
D	LM111	---	---	---	---	0	1	2	2	3	7

Notes:

1. Each test started with five (5) devices, and each temperature step lasted 16 hours.
2. Devices drew excessive current at 275°C. Step stress test terminated @ 250°C.
3. Devices drew excessive current at 275°C. Step stress terminated after 1/2 hour @ 275°C.
4. All failures were due to surface instability.
5. All failures were due to thermal runaway.
6. Two devices failed I_{IB} due to operation of device near the saturation limit of the amplifier and three failed I_{IO} due to surface instability.
7. One device failed I_{IO} and two devices failed V_{IO} due to surface instability.

As had been suggested by the prior circuit evaluation test results, the LM108A devices did not exhibit thermal runaway at 250°C indicating that the maximum life test temperature for the LM108A's could be as high as 250°C. However, subsequent attempts to initiate life tests at 250°C did reveal a thermal runaway problem with a high percentage of devices, and the maximum test temperature was reduced to 225°C.

With the exception of two Manufacturer B LM111 device I_{IB} failures at the 175°C step, and two Manufacturer D LM111 device V_{IO} failures at 275°C, all LM111 step stress failures were due to out-of-tolerance I_{IO} parameters. The apparent failed values of I_{IB} were attributed to device operation at common mode voltages too close to the supply voltage. Therefore the baseline electrical parameters were revised and performed at common mode voltages (V_{CM}) of 0V, -13.5V, and 12.0V rather than the 0V, -14.5V, and 13.0V specified in MIL-M-38510/10304. Both the I_{IO} and V_{IO} failures were due to surface instability, therefore life testing at 250°C was considered reasonable.

3.6 THERMAL RESISTANCE DETERMINATIONS

Upon completion of the bias circuit evaluation and step stress tests, the thermal resistance of each manufacturer's device type was determined to estimate maximum junction temperatures that would be experienced during life testing. An electrical test technique utilizing the forward voltage of a substrate diode as a temperature sensitive parameter was used to determine device junction temperatures. A MDAC-St. Louis thermal resistance tester was used to make the substrate diode forward voltage measurements. This tester operates the device in a power dissipating mode for 99.9% of the time and only briefly (1 millisecond every second) forward biases the substrate diode. Ambient temperatures and circuit configurations were consistent with expected accelerated life test conditions during the time junction temperature measurements were being performed. However, the actual power dissipation was somewhat less than the expected life test conditions. Thus, the thermal resistance values determined from these tests were used to compute junction temperatures at the power dissipation conditions expected during life testing.

The results of these tests are shown in Table 13. Thermal resistance values for each device type are similar for both manufacturers, and the variations between device types are inversely related to die size.

3.7 CURRENT DENSITY DETERMINATIONS

The current density in the V_{CC} stripes of each manufacturer's device type was determined from measurements of V_{CC} stripe dimensions during construction analyses and measurements of device currents during bias circuit evaluations. Results of these calculations are shown in Figures 3 and 4 for ambient temperatures up to 250°C. The maximum calculated current density at anticipated life test temperatures was less than 1×10^4 A/cm^2. Therefore only minimal metal migration failures were anticipated in 4,000 hours of 250°C life testing at current densities below 1×10^4 A/cm^2.

TABLE 13. MICROCIRCUIT THERMAL RESISTANCE

PART NUMBER	MANUF.	THERMAL RESISTANCE JUNCTION TO AMBIENT θ_{JA} - °C/WATT
MIL-M-38510/10104 (LM108A)	A	107.8
	B	118.2
MIL-M-38510/10107 (LM118)	C	67.0
	B	79.0
MIL-M-38510/10201 (723)	C	65.7
	D	65.5
MIL-M-38510/10701 (LM109)	B	60.0
	D	75.0
MIL-M-38510/10304 (LM111)	B	199.9
	D	218.6

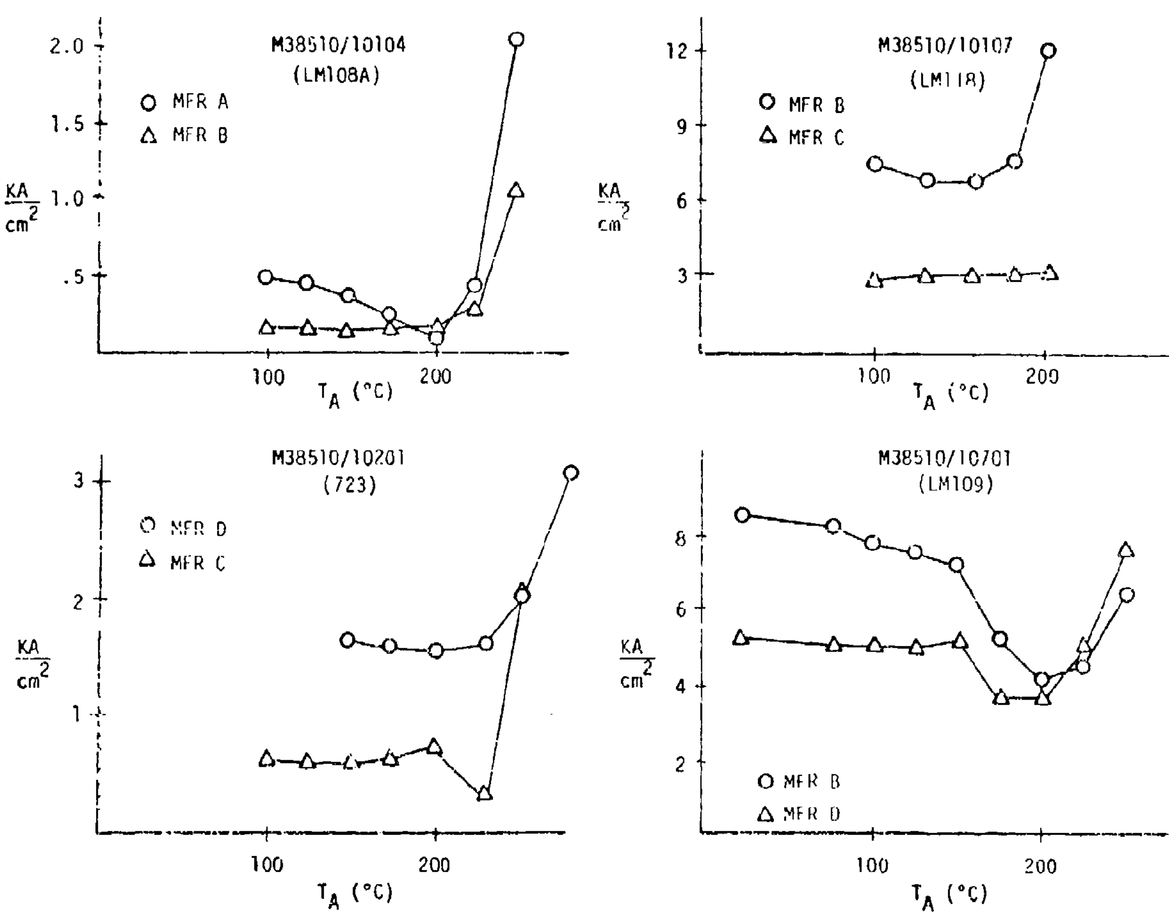


FIGURE 3. MICROCIRCUIT CURRENT DENSITY; LM108A, LM118, 723 & LM109

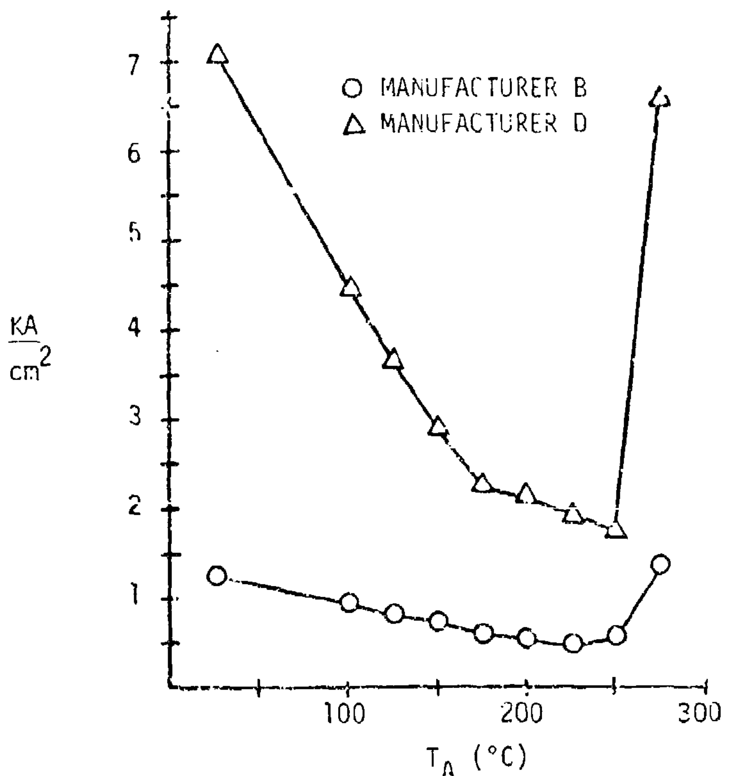


FIGURE 4. M38510/10304 (LM111) MICROCIRCUIT CURRENT DENSITY

4.0 ELECTRICAL CHARACTERIZATION TEST RESULTS

Characterization testing was performed in addition to initial baseline electrical tests to gain further insight into device performance characteristics. Those dynamic tests not performed during baseline testing such as ripple rejection, output noise, transient response, and slew rate, were performed with a sample of ten of each manufacturer's device type. The specific tests performed for each device are described in Appendix B. In addition, the transfer characteristics of two of each manufacturer's device type were evaluated at various conditions of temperature, voltage, load, and frequency. Summaries of the dynamic test results and details of the device transfer function studies are contained in Appendix E.

4.1 DYNAMIC TEST RESULTS

The dynamic test results are summarized in Table 14. At least 50% of each manufacturer's devices fail one or more of the dynamic parameter tests. Subsequent revisions to MIL-M-38510 contain relaxed end-point limits for these parameters. A review of the new specification limits and the data from these tests indicate that no further revisions of the specifications are necessary.

4.2 TRANSFER FUNCTION STUDIES

A study to determine the transfer function (the curve of the output response as a function of input voltage) of two of each manufacturer's devices was performed. The purpose of the study was to determine the response of transfer function curves to variations in temperature, voltage, load, and frequency.

The transfer function of the LM108A and LM118 operational amplifiers would ideally be the open-loop gain and would appear as in Figure 5. However, internal thermal effects cause the slope and linearity to change, as can be noted in Figures 6 and 7. In addition to Manufacturer B's LM108A and LM118 devices, the LM111 devices exhibited one or both of these thermal effects. Differences in phase and linearity are caused by thermal gradients which exist between the input and output circuits. These temperature gradients are produced by the

TABLE 14 DYNAMIC TEST RESULTS

DEVICE TYPE	TOTAL FAILED			
	MFR A	MFR B	MFR C	MFR D
LM108 A	7	10	-	-
LM118	-	6	10	-
723	-	-	10	5
LM109	-	10	-	10
LM111	-	10	-	10

1 TEN (10) DEVICES OF EACH MANUFACTURER WERE SUBJECTED TO DYNAMIC TESTING.

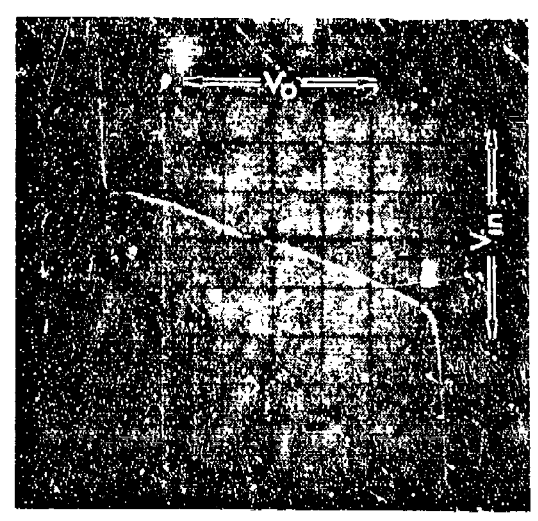


FIGURE 5. IDEAL OPERATIONAL AMPLIFIER OPEN LOOP GAIN CURVE

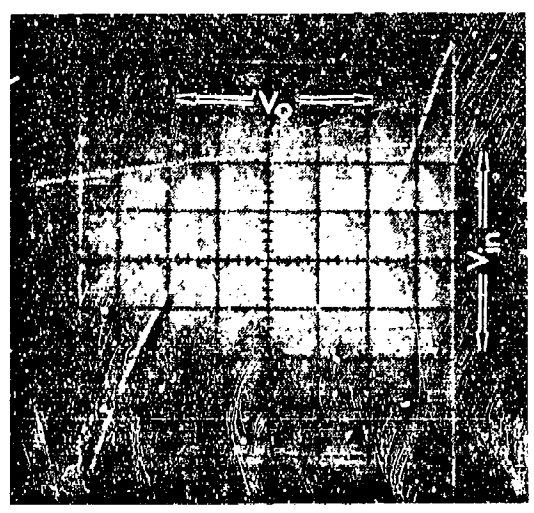


FIGURE 6. RESULTS OF THERMAL EFFECTS ON THE IDEAL OPERATIONAL AMPLIFIER OPEN LOOP GAIN CURVE

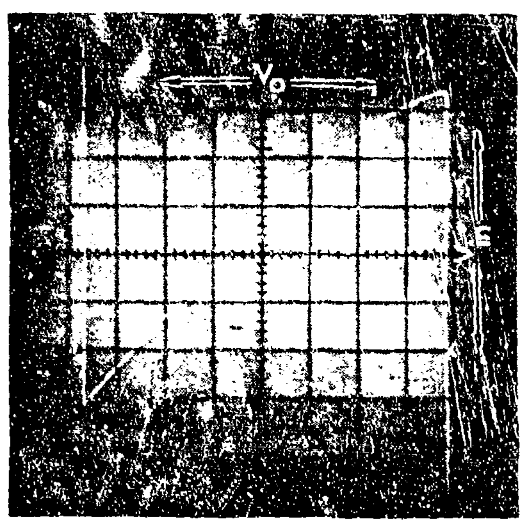


FIGURE 7. RESULTS OF THERMAL EFFECTS (180° PHASE SHIFT) ON THE MANUFACTURER B LM118 OPEN LOOP GAIN CURVE

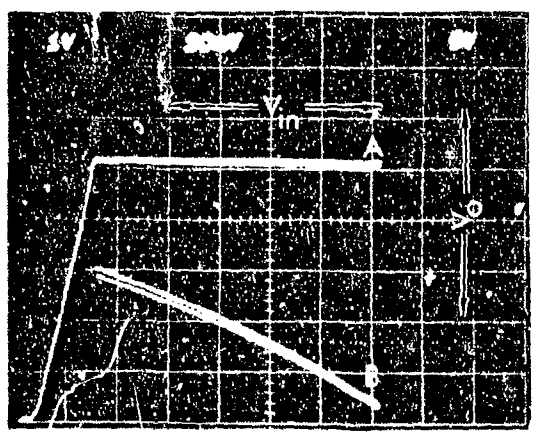


FIGURE 8. TYPICAL VOLTAGE REGULATOR TRANSFER CHARACTERISTIC CURVE

power dissipated in the output stages of the amplifier. The resulting heat conducts through the silicon chip causing uneven heating of the input components. Since all input components are not on isothermal lines, the resulting temperature differences in these components cause the device to produce other than ideal open loop gain curves.

The identification of device characteristics which produce linear transfer curves within operational amplifiers could not be fully determined. Although linearity is improved by minimizing temperature differences in the input circuitry, devices with nearly identical die layouts (Manufacturer B and C LM118) produce different transfer curves. Likewise, devices from different manufacturers with similar junction temperatures produced dissimilar transfer curves. In all cases the best transfer curves were obtained by operating the device at no load, thereby reducing the magnitude of the thermal effects within the die.

The transfer curve of the LM109 and 723 voltage regulators was normally a steady output voltage after there was sufficient input voltage to achieve turn-on. The curves in Figure 8 are typical of the voltage regulator transfer characteristic curve, and show the overall response (curve A), and a magnified response of the normal output of the device (curve B).

5.0 APPLICATION/TEST RELATED STUDY RESULTS

The application/test related studies were performed to provide information and recommendations related to the application of these linear devices in electronic equipment. Consideration was given to requirements for board layout, supply voltage filtering, shielding, compensation, loading, and interfacing. This information was derived from the results of characterization tests, development of electrical test programs and fixtures, and a literature survey of application guidelines. Test results were also used to formulate recommendations for improving the applicable MIL-M-38510 specifications.

5.1 APPLICATION GUIDELINES

The following recommendations are suggested as aids to optimal application of the linear devices studied in this program:

LM108A - The LM108A is a precision operational amplifier with very low offset voltage drift and high common mode rejection. The input is shunted with back-to-back diodes for overvoltage protection. Therefore the input differential voltage must be kept below 1 Vdc or excessive input currents will result. To improve power supply noise rejection, a 100 pF capacitor should be added from pin 8 to ground. In laying out a circuit using these devices care should be taken to keep package leads short and input leads close together, not only to minimize the possibility of parasitic oscillations and noise, but also to minimize offset errors due to thermal effects. Thermocouple effects, due to package lead to printed circuit board connections, can create microvolts of error if the temperature of the input lead connections differ by only a few degrees centigrade. Maintaining both ends of resistors at the same temperature is also important since carbon, oxide film and some metal film resistors can cause large thermocouple errors. Wirewound resistors of evenohm (20% Cr + 75% Ni + 2.75% Al + 2.75 Cu) or manganin (84% Cu + 12% Mn + 4% Ni) only generate about 2 μV/°C referenced to copper [1], but the inductance of wirewound resistors should be considered. Likewise, the gain fixing resistors should be of the same material to assure tracking with temperature. Since the device input bias currents are in the range of 1.0 nanoampere, care must be taken to reduce leakage currents by properly cleaning the printed circuit boards. To prevent subsequent contamination, the board should be covered with

an epoxy or silicone rubber coating. To futher reduce leakage currents on a printed circuit board that has b en properly cleaned and coated, a guard ring is suggested by both manufacturers. By designing the guard ring around the device input pins, as shown in Figure 9, the voltage differential between device pins is reduced, thereby reducing potential leakage currents.

LM118 - The LM118 device is a precision high speed operational amplifier with wide bandwidth and high slew rate. These devices also have diode input protection, but Manufacturer B's devices have a 1 volt breakdown limit while Manufacturer C's devices have a 5 volt breakdown limit. To achieve the high gain and large bandwidth of the device the circuit layout should be arranged to keep all lead lengths as short as possible and the output separated from the inputs. The values of the feedback and source impedance should be kept small to reduce the effect of stray capacitance at the inputs. The power supplies should be bypassed to ground at the supply leads of the amplifier with low inductance 0.1 μF capacitors. Capacitive loading must be kept to a minimum.

LM109 - The LM109 device is a complete five volt regulator. The regulator is current limited and goes into thermal shutdown at junction temperatures greater than 165°C. When operated at 25°C with no heat sinks, the device will go into thermal shutdown with a constant current load of 500 milliamperes. For a constant current of 500 milliamperes, proper heat sinks must be used. Output capacitors are not needed for stability, but a 1.0 μF capacitor from the output to ground improves the transient response. Also, an input capacitor of 0.2 μF is required if the regulator is located an appreciable distance from the power supply filter.

723 - The 723 device is a precision voltage regulator. The device has low standby current drain, low temperature drift, and high ripple rejection. The device can be used as a series, shunt, switching, or floating regulator in positive or negative power supplies. In using the device as a low voltage regulator the circuit shown in Figure 10 is used. For this circuit R3 should be equal to R1 in parallel with R2 for minimum temperature drift, since the device is susceptible to temperature drift under high dissipation conditions.

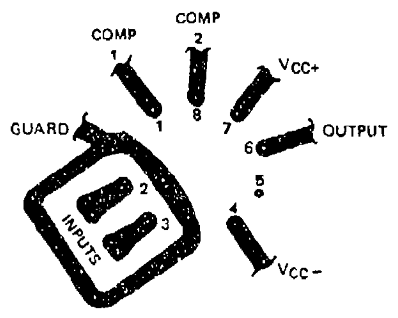


FIGURE 9. SUGGESTED PRINTED CIRCUIT BOARD LAYOUT OF INPUT PROTECTION FOR LM108 DEVICES

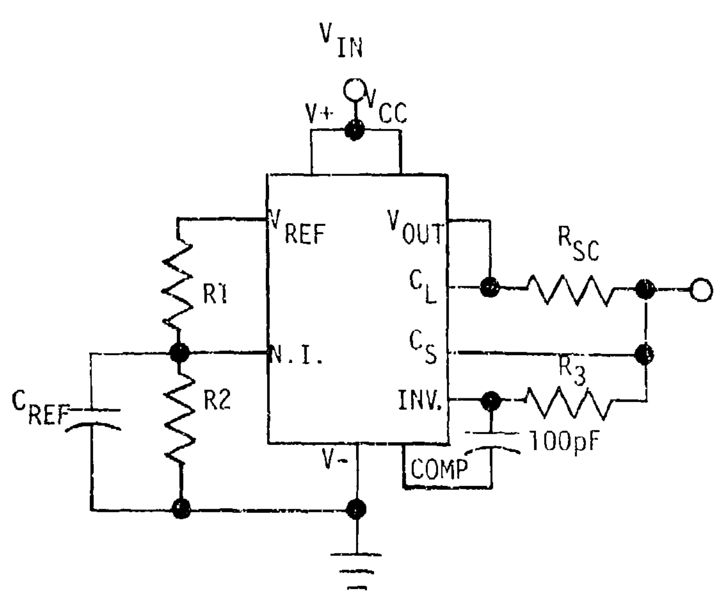


FIGURE 10. 723 APPLICATIONS CIRCUIT

LM111 - The LM111 device is a voltage comparator with input bias currents typically in the 50 nanoampere range. When the LM111 device is used in a circuit which does not use feedback, there are no special precautions to recommend, but in a feedback loop type circuit the device is susceptible to oscillations. To eliminate these oscillations lead lengths should be kept as short as possible and power supply bypass capacitors should be placed as close to the device as possible. Details of the compensation necessary to reduce oscillation for the MIL-M-38510 test circuit are contained in the next section.

5.2 STATIC TEST CIRCUIT MODIFICATIONS

The circuits used in the static electrical tests were those contained in the appropriate MIL-M-38510 specification. The compensation and filtering capacitors were as shown in the specification except as noted below.

(a) Capacitors connected to the device under test were placed as close to the device as possible.

(b) MIL-M-38510/10104 and /10107 (LM108A and LM118) - an additional 1 microfarad capacitor was added from $+V_{CC}$ (pin 7) to $-V_{CC}$ (pin 4). This was done to eliminate transients caused by relay switching between the specific tests.

(c) MIL-M-38510/10304 (LM111) - The LM111 device in the static test circuit was extremely susceptible to oscillation. By constructing the test fixture as compact as possible and attaching all capacitors associated with the device under test directly to the test socket, the oscillations were eliminated or reduced to an acceptable level, except for the emitter gain tests. The oscillation could not be reduced to an acceptable level for the emitter gain test so this test was deleted from the testing sequence. Additionally, the I_O and I_G test parameters were out of tolerance and test repeatability was poor due to ripple and transient currents in capacitors used to stabilize the test fixture. The automated system used to test these devices measures an instantaneous rather than an average current. Thus, it was necessary to fabricate a separate test fixture for measuring the I_O and I_G parameters. Since the compensating capacitors also permitted large current transients through the relay

contacts used for switching between tests, the fixture used for the I_O and I_G measurements was also used for V_{OL}, I_{CC} and I_I measurements. The two circuits and their compensation capacitors are shown in Figures 11 and 12.

5.3 MIL-M-38510 ELECTRICAL TEST DEFICIENCIES

During the course of preparing software for automated tests of the linear microcircuits, a number of deficiencies were noted in the MIL-M-38510 slash sheets. A brief description of each discrepancy is as follows:

(a) MIL-M-38510/10104 and MIL-M-38510/10107 - The static test circuit (Figure 8) in the 15 September 1975 revision of the specification has a 50K ohm resistor in the minus input to ground path. This should be a 50 ohm resistance to match the impedance to the positive terminal. This discrepancy was corrected in Amendment 3, dated 22 February 1977. In addition, the Power Supply Rejection Ratio (PSRR) test limits should be double sided since it is possible to have a negative PSRR.

(b) MIL-M-38510/10304 - With the exceptions of the I_{OS} and I_I tests, all LM111 test conditions require the inputs (LM111 device pins 2 and 3) to be the same voltage. During preparations for electrical testing, a separate power supply was programmed for each input. While checking out the static test fixture it was noted that separate power supplies could not provide exactly the same voltage to the test socket, and millivolt differences in these voltages caused invalid test results. The difference in these supplies should be less than ± 10 microvolts. To insure that identical voltage conditions were present on each input, two additional relays were added to the /10304 static test circuit. The first of these relays shorts pins 2 and 3 together when the same voltage is required on each input, thus eliminating the error induced when using a second power supply. A second relay was added which provides ground on the device inputs when both of the additional relays are energized, thereby eliminating the need for either power supply on the device inputs during many tests. By installing

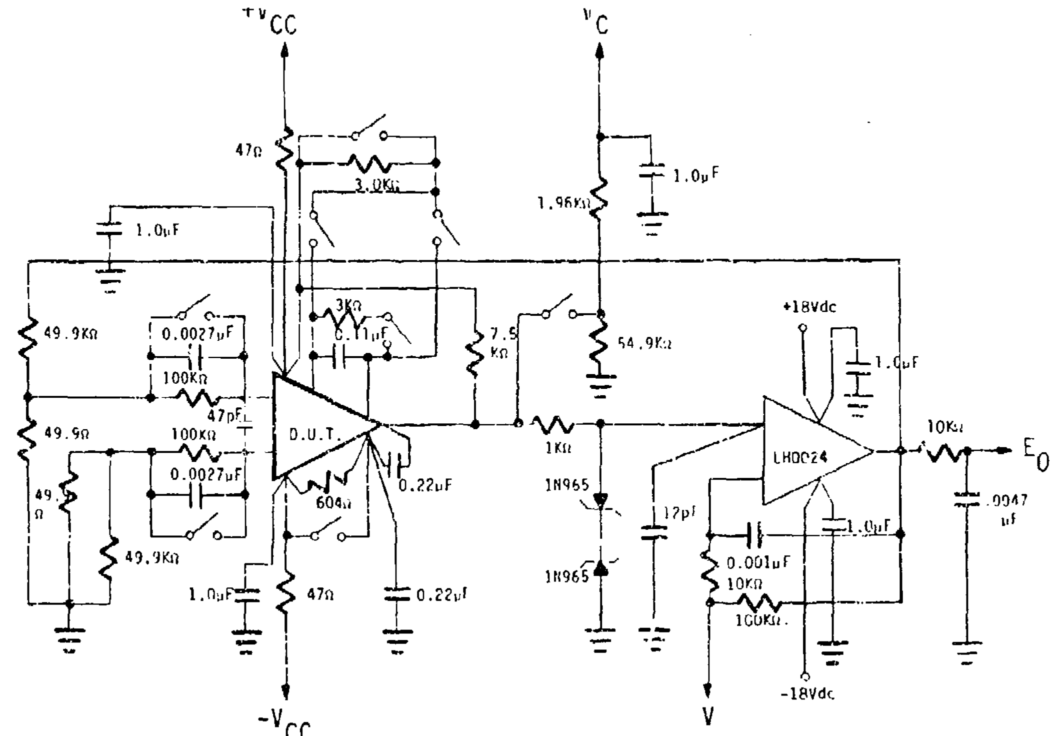


FIGURE 11. LM111 STATIC TEST CIRCUIT

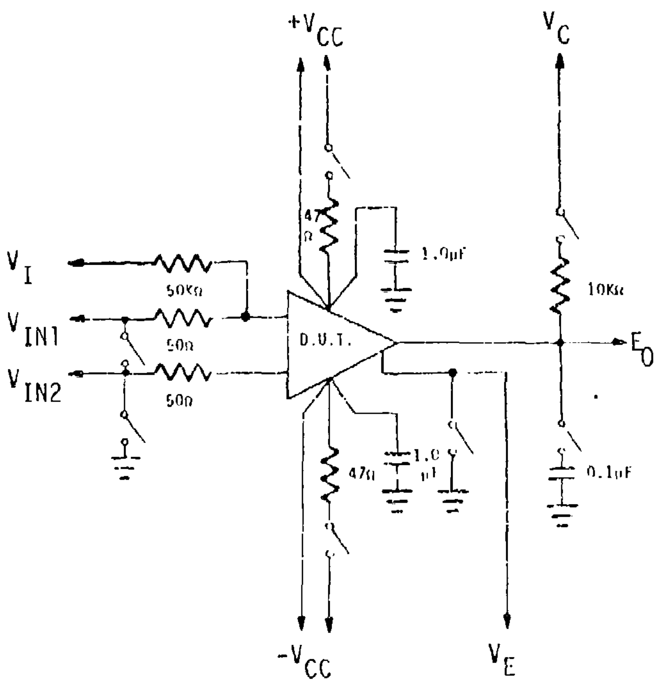


FIGURE 12. LM111 STATIC TEST CIRCUIT FOR I_O, I_G, V_{OL}, I_{CC} AND I_I MEASUREMENTS

the two (2) relays as close as possible to the test socket, invalid test conditions in the input offset voltages were eliminated. The static test circuit was also changed for the emitter gain test. The device under test should have $+V_{CC}$ connected to pin seven (7) to provide a voltage across the output transistor.

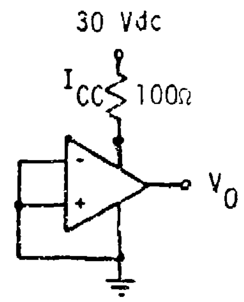
(c) MIL-M-38510/10701 - The test limits for the Delta Standby Current Drain (I_{SCD}) for the line current should be double sided since it is possible to have negative delta results.

5.4 MIL-M-38510 ACCELERATED LIFE TEST CIRCUIT DEFICIENCIES

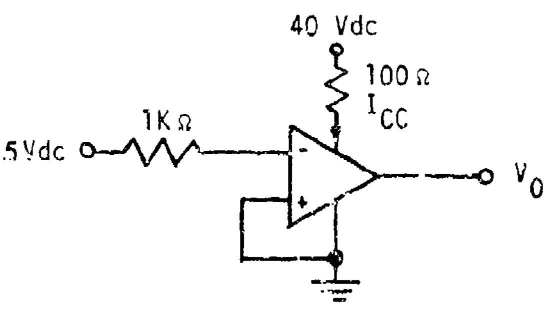
The circuits in MIL-M-38510/101D (15 September 1975), MIL-M-38510/101E (29 September 1977), and MIL-M-38510/103A did not provide adequate biasing conditions for accelerated life tests. New accelerated life test circuits were developed for the operational amplifier and the voltage comparator. The MIL-M-38510 bias circuits which were evaluated and the recommended life test bias configurations are shown in Figure 13.

The MIL-M-38510/101D bias circuit, which applied 30Vdc to V_{CC} and ground to the device inputs, did not provide maximum stress conditions across the device. The MIL-M-38510/101E bias circuit increased the applied V_{CC} voltage from 30Vdc to 40Vdc which provided the maximum rated V_{CC} voltage across the device. However, by applying 5Vdc to the (+) input of the device this configuration allowed the input protection network to draw excessive current. The recommended bias circuit was preferred since it reduces the input current by lowering the input bias voltage from 5Vdc to 2Vdc in addition to applying the maximum rated device voltage (40 Vdc) across the devices.

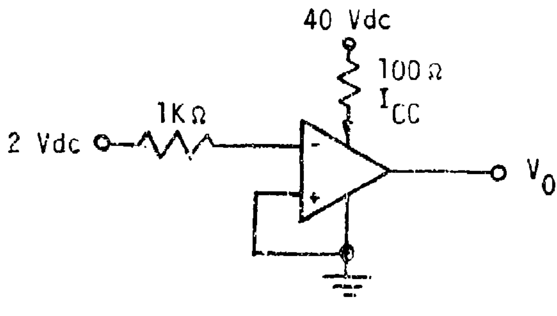
In the recommended life test bias circuit for the comparators, a 5K ohm current limiting resistor is connected between the output (pin 7) and the 30 Vdc power supply. The MIL-M-38510/10304 life test circuit has the output connected directly to $+V_{CC}$ (pin 8). In the MIL-M-38510/10304 configuration the voltage across the device would depend on the state of the device output, and if the output switched low there would be no voltage across the device. Any test circuit which does not insure that 85% of the supply voltage would



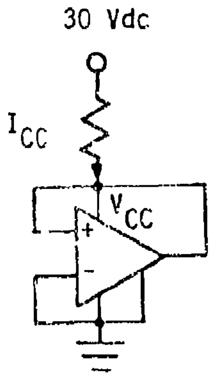
MIL-M-38510/101D AMPLIFIER LIFE TEST CIRCUIT



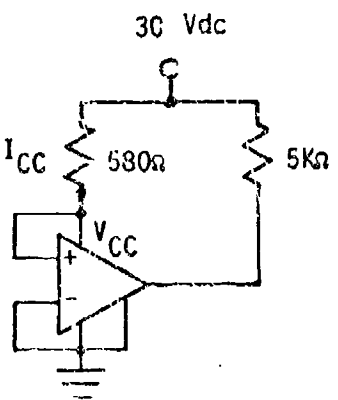
MIL-M-38510/101E AMPLIFIER LIFE TEST CIRCUIT



RECOMMENDED AMPLIFIER LIFE TEST CIRCUIT



MIL-M-38510/103A COMPARATOR LIFE TEST CIRCUIT



RECOMMENDED COMPARATOR LIFE TEST CIRCUIT

FIGURE 13. MIL-M-38510 VS. RECOMMENDED LIFE TEST CIRCUITS

always be present across the device is considered unacceptable. This condition was eliminated by connecting the device output to the power supply through a 5K ohm resistor.

Both recommended life test circuits provide adequate life test conditions and no bias circuit related failures resulted during the actual life tests.

5.5 MIL-STD-883 DEFICIENCIES

The MIL-M-38510/101E and MIL-M-38510/103B contain a Group A inspection table (Table III) which lists the electrical test requirements for the applicable linear devices. Within each table is a column of MIL-STD-883 test methods which can be referenced for most electrical tests. The information found in each referenced MIL-STD-883 test method can be categorized by one of the following:

(a) The test method does not apply to the MIL-M-38510 electrical test in question,

(b) The test method was written for testing of digital microcircuits, or

(c) The test method is outdated by test information contained in the respective MIL-M-38510 slash sheet.

Since all Group A electrical tests for the LM108A, LM118, and LM118 devices can be implemented with the information found in MIL-M-38510, the column of MIL-STD-883 3000 and 4000 series test methods should be deleted, or the test methods should be revised.

5.6 DEVICE OPERATION CHARACTERISTICS

The MIL-M-38510/10304 (LM111) device was found to exhibit erratic behavior in the extreme common mode voltage regions. Analysis of device operation in these regions showed that electrical tests performed at common mode voltages of -14.5 Vdc and +13 Vdc resulted in device operation at or close to the saturation limits of the input transistors. Figure 14 shows a typical plot of I_{IB} current versus common mode voltage. At common mode voltages of -14.5 and +13 Vdc the device is at or near the point where it is driven into saturation. Thus, the output of the nulling amplifier is also driven into saturation, resulting in a large out-of-tolerance value of I_{IB}. It is suggested that the tests on these devices be modified to common mode voltages of -13.5 Vdc and +12 Vdc.

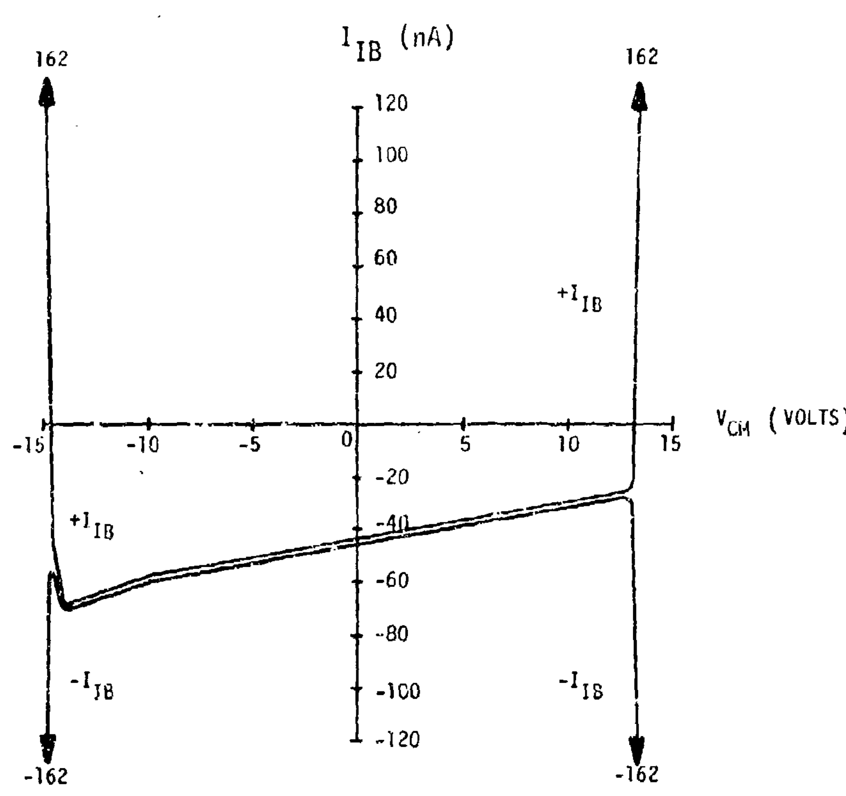


FIGURE 14 . PLOT OF M38510/10304 (LM111) I_{IB} VS. COMMON MODE VOLTAGE (V_{CM})

6.0 ACCELERATED LIFE TESTS

6.1 LIFE TEST CONDITIONS

Based on the results of the prelife test evaluations, the life test temperatures shown in Table 15 were selected. These temperatures appeared to avoid thermal runaway problems and the selected circuits maintained a constant device output voltage with minimal current drain. However, after operation of LM108A life test devices at 250°C for 1/2 hour, 43% of the Manufacturer A devices drew excessive current due to thermal runaway. The 15 devices which drew excessive current had a different date code (7642) than the devices used for circuit evaluation and step-stress (7643), and is apparently why this problem was not encountered during the prelife evaluations. Due to the thermal runaway problem, the maximum LM108A life test temperature was reduced to 225°C and the other two life tests were conducted at 200°C and 175°C. Unfortunately at 175°C, the output voltage of some of the Manufacturer B LM108As is low, whereas at 200°C and 225°C, the output of every device is thermally biased high. Although an undesirable condition, it was anticipated that most life test failures would not involve the output transistor, but would involve other transistors on the die where the junction stresses were the same at all temperatures. Actual failure modes for this device were not associated with the output transistors.

During initiation of LM111 life testing, more than 50% of the devices at life test temperatures of 225°C and 250°C failed within 32 hours. Almost all failures were due to slightly out-of-tolerance I_{IO} and V_{IO} values. In order to provide a reasonable failure distribution, the I_{IO} and V_{IO} limits were relaxed and life tests were continued. Previously failed devices were then subjected to the new failure criteria, and those passing were returned to life test. The I_{IO} limits were changed from $\pm$10nA to $\pm$20nA and the V_{IO} limits were changed from $\pm$4mV to $\pm$5mV.

A summary of voltage, current, power dissipation, and junction temperature conditions at the selected ambient test temperatures is shown for each device type in Figures 15 through 19.

The sequence for performing the life tests is shown in Figure 20.

TABLE 15 LIFE TEST TEMPERATURES

PART TYPE	TEST TEMPERATURES (°C)					
	125	150	175	200	225	250
M38510/10104BGC (LM108A)			X	X	X	X/1
M38510/10107BGC (LM118)	X	X	X			
M38510/10201BIC (723)		X	X	X		
M38510/10701BIC (LM109)				X	X	X
M38510/10304BGC (LM111)				X	X	X

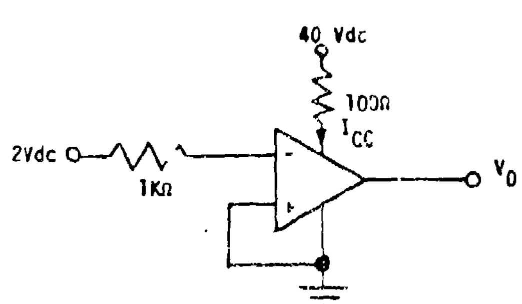
/1 Initial attempts to operate LM108s at 250°C resulted in thermal runaway and the devices were subsequently placed on test at 175°C.

ACCELERATED LIFE TEST CIRCUIT

MANU-FACT-URER	T_A AMBIENT TEMPERATURE (°C)	V_{CC} DEVICE VOLTAGE (VOLTS)	I_{CC} DEVICE CURRENT (MICROAMPS)	P_d POWER DISSIPATION (MILLIWATTS)	V_O OUTPUT VOLTAGE (VOLTS)	T_J JUNCTION TEMPERATURE (°C)
A	175	39.981	108	5.1	39.6	175.5
	200	39.994	61	3.3	39.6	200.4
	225	39.972	282	12.0	39.2	226.3
B	175	39.988	173	7.8	15.6	175.9
	200	39.977	192	8.5	38.4	201.0
	225	39.961	340	14.4	34.6	226.7

1. DEVICE CONDITIONS ARE APPROXIMATE AVERAGE VALUES
2. JUNCTION TEMPERATURES BASED ON A CALCULATED THERMAL RESISTANCE (θ_{JA}) OF 107°C/WATT FOR MANUFACTURER A AND 118°C/WATT FOR MANUFACTURER B.

FIGURE 15. M38510/10104 (LM108A) SUMMARY OF LIFE TEST CONDITIONS

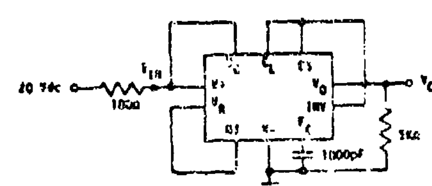


ACCELERATED LIFE TEST CIRCUIT

MANU-FACT-URER	T_A AMBIENT TEMPERATURE (°C)	V_{CC} DEVICE VOLTAGE (VOLTS)	I_{CC} DEVICE CURRENT (MILLIAMPS)	P_d POWER DISSIPATION (MILLIWATTS)	V_O OUTPUT VOLTAGE (VOLTS)	T_J JUNCTION TEMPERATURE (°C)
C	125	39.70	3.0	119	1.44	132.9
	150	39.69	3.0	121	1.42	158.1
	175	39.68	3.0	122	1.58	183.2
B	125	39.78	1.9	76	.925	131.0
	150	39.81	1.9	76	.813	156.0
	175	39.79	2.1	86	.726	181.8

1. DEVICE CONDITIONS ARE APPROXIMATE AVERAGE VALUES
2. JUNCTION TEMPERATURES BASED ON A CALCULATED THERMAL RESISTANCE (θ_{JA}) OF 67°C/WATT FOR MANUFACTURER C AND 79°C/WATT FOR MANUFACTURER B.

FIGURE 16. M38510/10107 (LM118) SUMMARY OF LIFE TEST CONDITIONS

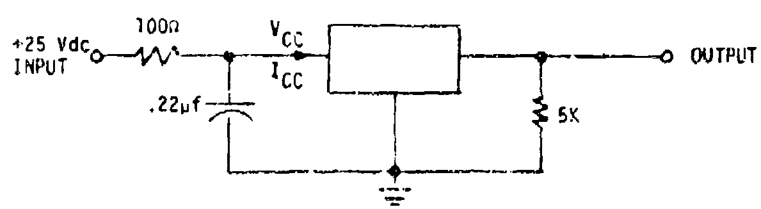


ACCELERATED LIFE TEST CIRCUIT

MANU-FACT-URER	T_A AMBIENT TEMPERATURE (°C)	V_{CC} DEVICE VOLTAGE (VOLTS)	I_{CC} DEVICE CURRENT (MILLIAMPS)	P_d POWER DISSIPATION (MILLIWATTS)	V_O OUTPUT VOLTAGE (VOLTS)	T_J JUNCTION TEMPERATURE (°C)
C	150	19.7	2.78	45	7.15	153.0
	175	19.7	2.69	47	7.45	178.1
	200	19.7	3.21	54	7.06	203.6
D	150	19.7	2.8[illegible]	55	7.25	154.1
	175	19.8	2.72	44	7.25	178.3
	200	19.8	2.67	43	7.25	203.2

1. DEVICE CONDITIONS ARE APPROXIMATE AVERAGE VALUES
2. JUNCTION TEMPERATURES BASED ON A CALCULATED THERMAL RESISTANCE (θ_{JA}) OF 65.7°C/WATT FOR MANUFACTURER C AND 65.5°C/WATT FOR MANUFACTURER D.

FIGURE 17. M38510/10201 (723) SUMMARY OF LIFE TEST CONDITIONS

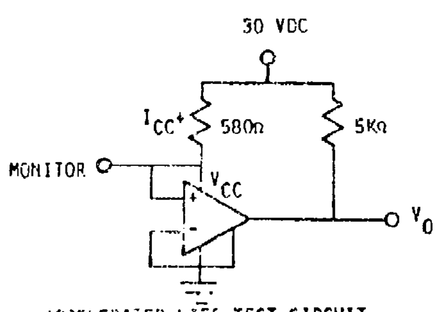


ACCELERATED LIFE TEST CIRCUIT

MANU-FACT-URER	T_A AMBIENT TEMPERATURE (°C)	V_{CC} DEVICE VOLTAGE (VOLTS)	I_{CC} DEVICE CURRENT (MILLIAMPS)	P_d POWER DISSIPATION (MILLIWATTS)	V_o OUTPUT VOLTAGE (VOLTS)	T_J JUNCTION TEMPERATURE (°C)
B	200	24.66	4.25	104	.561	206.3
	225	24.54	4.55	112	.460	231.8
	250	24.35	6.51	159	.430	259.6
D	200	24.62	3.99	98	.892	207.4
	225	24.35	5.09	124	.753	234.4
	250	24.13	7.68	185	.718	264.0

1. DEVICE CONDITIONS ARE APPROXIMATE AVERAGE VALUES
2. JUNCTION TEMPERATURES BASED ON A CALCULATED THERMAL RESISTANCE (θ_{JA}) OF 60°C/WATT FOR MANUFACTURER B AND 75°C/WATT FOR MANUFACTURER D.

FIGURE 18. M38510/10701 (LM109) SUMMARY OF LIFE TEST CONDITIONS



ACCELERATED LIFE TEST CIRCUIT

MANUFACTURER	T_A AMBIENT TEMPERATURE (°C)	V_{CC} DEVICE VOLTAGE (VOLTS)	I_{CC} DEVICE CURRENT (MILLIAMPS)	P_d POWER DISSIPATION (MILLIWATTS)	V_O OUTPUT VOLTAGE (VOLTS)	T_J JUNCTION TEMPERATURE (°C)
B	200	29.570	.879	24.8	29.78	205.0
	225	29.683	.77[illegible]	25.[illegible]	29.20	230.1
	250	29.628	.848	48.1	25.53	259.6
D	200	29.652	.738	49.0	23.35	210.7
	225	29.682	.772	48.1	6.75	235.5
	250	29.657	.798	54.8	10.47	262.0

1. DEVICE CONDITIONS ARE APPROXIMATE AVERAGE VALUES.
2. JUNCTION TEMPERATURES BASED ON A CALCULATED THERMAL RESISTANCE (θ_{JA}) OF 200°C/WATT FOR MANUFACTURER B AND 219°C/WATT FOR MANUFACTURER D.

FIGURE 19. M38510/10304 (LM111) SUMMARY OF LIFE TEST CONDITIONS

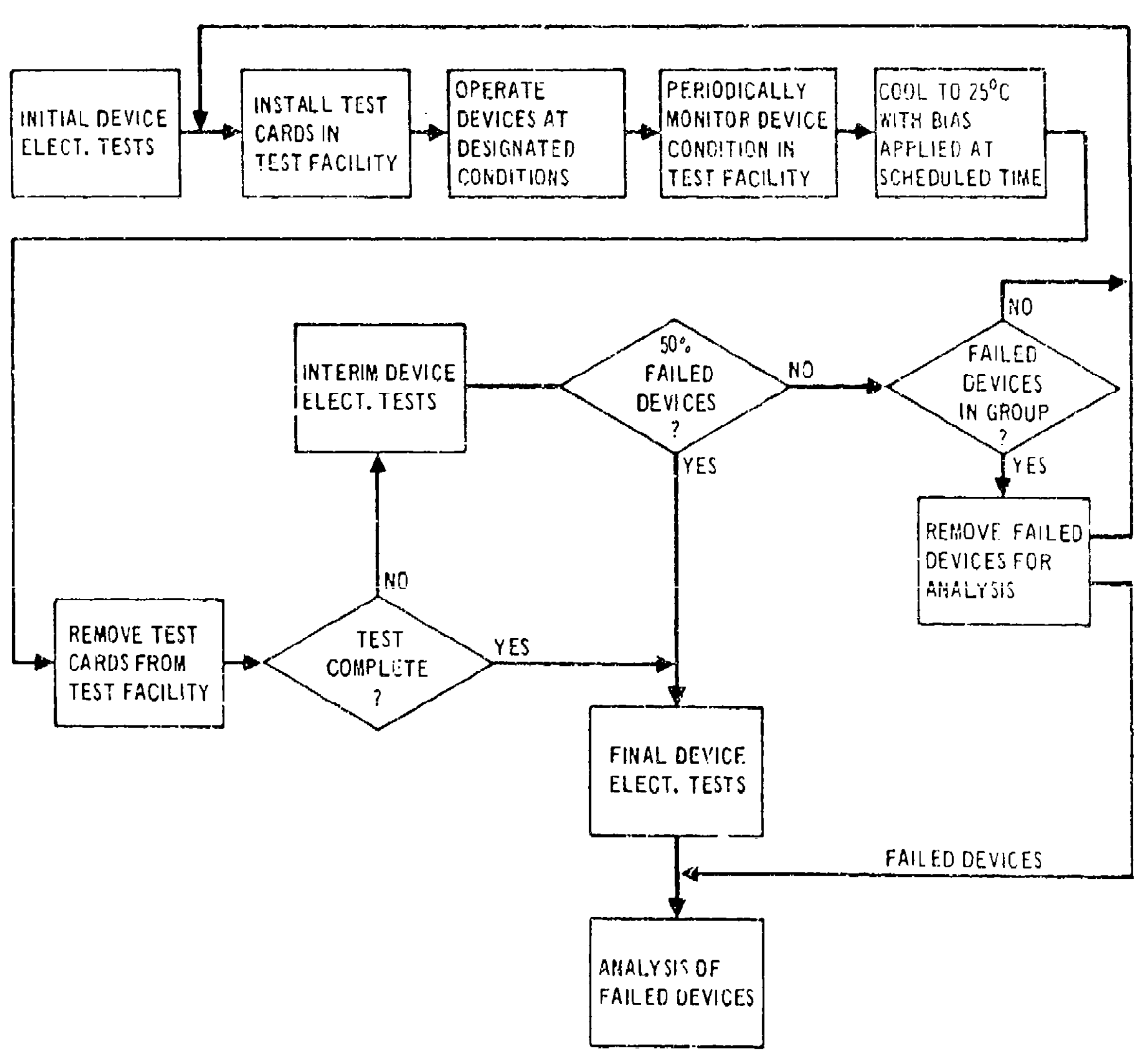


FIGURE 20. LIFE TESTING SEQUENCE

6.2 ACCELERATED LIFE TEST RESULTS

Accelerated life tests were continued to the 4,000 hour point or to the 70% failure level , and the results are summarized in Table 16. This table shows the cumulative number of devices failing the 25°C dc electrical tests at each measurement point, and the number of devices failing the final 125°C and -55°C tests.

TABLE 16. LIFE TEST FAILURE SUMMARY

PART	CELL	NO. ON TEST	MANUFAC-TURER	TEMP	CUMULATIVE NUMBER OF FAILURES AT HOURS OF TEST													
					1	2	4	8	16	32	64	128	256	500	1000	2000	4000	FINAL
LM108A	115	35	A	225	-	-	0	1	2	2	4	10	11	12	17	20	23	26
	114	35		200	-	-	1	1	2	2	3	3	4	9	13	14	17	17
	113	35		175	1	2	2	4	4	5	6	6	6	7	9	11	16	17
	215	30	B	225	-	-	18	19	20	20	21	24	25	27	29	-	-	29
	214	30		200	-	-	14	18	18	18	20	22	22	23	26	-	-	29
	213	30		175	11	12	16	18	19	19	19	20	20	23	27	-	-	28
LM118	233	34	B	175	22	23	24	24	25	25	25	26	26	26	28	-	-	28
	222	34		150	17	22	25	26	26	26	27	27	27	27	30	-	-	33
	221	33		125	0	0	6	15	18	20	21	23	23	23	23	-	-	27
	323	34	C	175	1	1	2	2	2	2	3	3	3	3	3	4	8	8
	322	35		150	0	0	1	1	1	1	1	1	1	1	1	2	2	3
	321	34		125	1	1	1	1	1	1	1	2	2	2	3	3	6	6
723	434	35	D	200	-	-	0	0	0	0	0	0	0	0	0	0	0	0
	433	34		175	-	-	1	1	1	1	2	2	2	2	2	2	3	3
	432	35		150	-	-	0	0	0	0	0	0	0	0	0	0	0	0
	334	30	C	200	-	-	0	0	0	0	0	0	0	0	0	6	6	8
	333	35		175	-	-	0	0	0	0	0	0	0	0	0	0	0	0
	332	35		150	-	-	0	0	0	0	0	0	0	0	0	0	0	0
LM109	256	35	B	250	-	-	0	0	0	0	0	1	2	2	2	2	3	3
	255	35		225	-	-	0	1	1	1	2	2	2	2	2	2	3	3
	254	35		200	-	-	0	0	0	0	0	0	0	2	2	2	3	3
	456	35	D	250	-	-	2	2	3	3	3	3	3	3	3	4	4	4
	455	35		225	-	-	0	0	1	1	1	1	1	1	1	2	2	2
	454	35		200	-	-	2	2	2	3	3	3	3	3	3	3	3	3
LM111	246	35	B	250	-	-	4	5	6	11	12	14	16	19	23	-	-	24
	245	35		225	-	-	2	2	2	3	8	10	16	22	25	-	-	25
	244	35		200	-	-	0	0	0	0	0	3	4	16	25	-	-	29
	446	35	D	250	-	-	0	2	2	5	5	5	12	14	34	-	-	34
	445	33		225	-	-	1	6	7	12	12	12	16	19	29	-	-	29
	444	35		200	-	-	0	1	1	2	9	9	18	19	35	-	-	35

7.0 FAILURE ANALYSIS

All devices failing an interim or final electrical test during step stress and life testing were analyzed to determine the failure mode, mechanism, and probable cause. However, only a limited analysis was performed for those few devices that exhibited a random, isolated failure mode and most of the devices that exhibited parametric failures at +125°C only. Summaries of the failure analysis findings for each manufacturer's device type are shown in Tables 17 through 21. Complete details of the failure analysis procedures and findings are contained in Appendix F.

TABLE 17. MIL-M-38510/10107 (LM118) FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS) BY TEST CELL							
	MANUFACTURER B				MANUFACTURER C			
	STEP STRESS	ACCELERATED LIFE 125°C	ACCELERATED LIFE 150°C	ACCELERATED LIFE 175°C	STEP STRESS	ACCELERATED LIFE 125°C	ACCELERATED LIFE 150°C	ACCELERATED LIFE 175°C
A. V_{IO} AND/OR PSRR B. CHANNEL CURRENT FROM R15 TO THE SUBSTRATE C. INVERSION OF THE RESISTOR TUB DUE TO CHARGE MIGRATION D. MOBILE IONS OR CHARGES IN THE PASSIVATION	3@125°C 2@150°C	5@4 9@8 2@16 2@32 1@64 2@128	15@1 5@2 3@4 1@8 1@64 1*@1000	22@1 1@2 1@4 1@16 1@1000				
A. I_{IO} @ V_{CM} = -15V B. V+ TO INPUT CHANNEL CURRENT C. PROBABLY INVERSION OF THE C-B JUNCTION OF THE INPUT TRANSISTOR D. MOBILE IONS IN THE PASSIVATION			3@1000 1*@1000			1@4000		1@4
A. I_{IO} OR I_{IB} B. LOW GAIN IN INPUT TRANSISTOR C. PROBABLY DEPLETION OF THE BASE D. MOBILE IONS OR CHARGES IN THE PASSIVATION				1@128 1@1000		1@1 2@4000		1@2000
A. V_{IO} LATCHED UP B. MELTED STRIPES AND SHORTED JUNCTIONS C. PROBABLY THERMAL RUNAWAY OF C1 D. UNKNOWN					1@200°C 1@250°C 2@275°C			1@1 2@4000
A. V_{IO} LATCHED UP B. SHORTED CAPACITOR C. DIELECTRIC BREAKDOWN D. DEFECT IN DIELECTRIC SiO_2						1@128	1@4 1@2000	2@4000
A. V_{IO} LATCHED UP B. OPEN STRIPE OR SHORTED JUNCTION C. ELECTRICAL OVERSTRESS D. TEST ERROR		1@4				1@1000	1*@4000	
RANDOM FAILURES-NOT ANALYZED IN DETAIL								
A. V_{IO} AND PSRR (RECOVERED UPON DELIDDING)								1@64
A. P_D B. NONE C. NONE D. TEST ERROR (INITIALLY FAILED)		4*@1000	2@1 1*@1000					
TOTAL NUMBER OF FAILED PARTS	5	27	33	28	4	6	3	8

* @ + 125°C ONLY.

TABLE 18. MIL-M-38510/10104 (LM108A) FAILURE ANALYSIS SUMMARY

<table>
<tr><td rowspan="3">A. FAILED PARAMETERS OR SYMPTOMS
B. FAILURE MODE
C. FAILURE MECHANISM
D. CAUSE OF FAILURE</td><td colspan="8">QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS) BY TEST CELL</td></tr>
<tr><td colspan="4">MANUFACTURER B</td><td colspan="4">MANUFACTURER A</td></tr>
<tr><td>STEP STRESS</td><td>ACCELERATED LIFE 175°C</td><td>ACCELERATED LIFE 200°C</td><td>ACCELERATED LIFE 225°C</td><td>STEP STRESS</td><td>ACCELERATED LIFE 175°C</td><td>ACCELERATED LIFE 200°C</td><td>ACCELERATED LIFE 225°C</td></tr>
<tr><td>A. V_{IO} AND/OR A_{VS}
B. CHANNEL CURRENT FROM R7 TO THE SUBSTRATE
C. INVERSION OF THE R7 RESISTOR TUB
D. MOBILE IONS OR CHARGES IN THE PASSIVATION</td><td>1@125°C
1@150°C
1@175°C
1@225°C</td><td>10@1
1@2
4@4
2@8
1@16
3@500
4@1000
1*@1000</td><td>14@4
3@8
2@64
2@128
3@1000
3*@1000</td><td>18@4
1@8
1@16
1@64
3@128
1@250
2@500
2@1000</td><td></td><td></td><td></td><td></td></tr>
<tr><td>A. V_{IO} LATCHED UP
B. MELTED STRIPES AND SHORTED JUNCTIONS
C. THERMAL RUNAWAY AT Q6
D. UNKNOWN</td><td></td><td></td><td></td><td></td><td></td><td>1@5000
2@2000
4@4000</td><td>1@256
4@500
4@1000
1@2000
3@4000</td><td>1@8
3@64
3@128
1@256
1@500
3@1000
2@2000
3@4000</td></tr>
<tr><td>A. A_{VS}
B. NOT DETERMINED (RECOVERED)
C. SURFACE INSTABILITY
D. PROBABLY IONIC CONTAMINATION</td><td></td><td></td><td></td><td></td><td></td><td>1@1
1@8
2@1000
1@2000</td><td>1@500</td><td>2@1000
1@2000
●1@4000</td></tr>
<tr><td>A. I_{IO} AND/OR I_{IB}
B. PROBABLY DEGRADED INPUT TRANSISTORS
C. PROBABLY CHARGE ACCUMULATION
D. TEST ANOMALY (STATIC DISCHARGE)</td><td></td><td>1@1
1@128</td><td>1@8
1@500</td><td></td><td></td><td>1@2
1@32
1@64</td><td>1@4
1@16
1@64</td><td>1@16
2@128</td></tr>
<tr><td colspan="9">+125°C FAILURES AND RANDOM FAILURES - NOT ANALYZED IN DETAIL</td></tr>
<tr><td>A. V_{IO} @ +125°C ONLY</td><td></td><td></td><td></td><td></td><td></td><td>1@4000</td><td></td><td>1@4000</td></tr>
<tr><td>A. I_{IO} @ + 125°C ONLY</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>1@4000</td></tr>
<tr><td>A. I_{OS} (-) (RECOVERED WHEN LEFT ON TEST)</td><td></td><td></td><td></td><td></td><td></td><td>1@8</td><td></td><td></td></tr>
<tr><td>TOTAL NUMBER OF FAILED PARTS</td><td>4</td><td>28</td><td>29</td><td>29</td><td>0</td><td>17</td><td>17</td><td>26</td></tr>
</table>

NOTES: * @ +125°C ONLY. ● @ -55°C ONLY.

TABLE 19. MIL-M-38510/10701 (LM109) FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS) BY TEST CELL					
	ACCELERATED LIFE					
	MANUFACTURER D			MANUFACTURER B		
	200°C	225°C	250°C	200°C	225°C	250°C
A. OPEN PIN B. LIFTED WIRE BOND AT THE POST C. KIRKENDALL VOIDING IN $AuAl_2$ D. EXCESSIVE $AuAl_2$ GROWTH DURING BONDING	•			1@500	1@64 1@4000	1@250
A. OPEN PIN 1 OR 3 B. BROKEN EXTERNAL LEAD C. MECHANICAL OVERSTRESS D. MISHANDLING		1@2000			1@8	
A. OPEN PIN 3 B. BROKEN EXTERNAL LEAD C. Au LEACHING D. TIN SOLDER				1@4000		1@120
A. ΔI_{SCD} [13] B. NONE C. NONE D. INITIALLY FAILED OR MARGINAL	2@4 1@64	1@16	2@4 1@16 1@2000			1@4000
RANDOM FAILURES - NOT ANALYZED IN DETAIL						
A. V_{OUT} [4] (ONLY MARGINALLY FAILED)				1@500		
TOTAL NUMBER OF FAILED PARTS	3	2	4	3	3	3

TABLE 20. MIL-M-38510/10201 (723) FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS) BY TEST CELL					
	ACCELERATED LIFE					
	MANUFACTURER D			MANUFACTURER C		
	150°C	175°C	200°C	150°C	175°C	200°C
A. I_{SCD} B. NONE C. NONE D. TEST SET DRIFT						6@2000
A. $V_{RE.}$ OR $V_{R\ LINE}$ [1] + $V_{R\ LOAD}$ [4] @ -55°C B. NONE C. NONE D. PROBABLY AN INTERMITTENT TEST SOCKET						2@4000
A. I_{OS} B. NOT DETERMINED C. SURFACE INSTABILITY + INITIALLY MARGINAL D. MOBILE CONTAMINANT IONS		1@4 1@64				
RANDOM FAILURES - NOT ANALYZED IN DETAIL						
A. $V_{R\ LINE}$ [1] (ONLY MARGINALLY FAILED)		1@4000				
TOTAL NUMBER OF FAILED PARTS	0	3	0	0	0	8

TABLE 21. MIL-M-38510/10304 (LM111) FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS) BY TEST CELL							
	MANUFACTURER B				MANUFACTURER D			
	STEP STRESS	ACCELERATED LIFE			STEP STRESS	ACCELERATED LIFE		
		200°C	225°C	250°C		200°C	225°C	250°C
A. V_{IO} B. LOW h_{FE} IN Q4 C. INVERSION OF THE BASE OF Q4 D. PROBABLY IONIC CONTAMINATION		3@1000	1@4 1@64 1@1000		1@225°C 1@275°C	1@8 1@32 5@64 9@256 1@500 16@1000	3@8 1@16 5@32 4@256 3@500 10@1000	1@8 3@32 7@256 1@500 20@1000
A. I_{IO} B. LOW h_{FE} IN Q2 C. SURFACE INSTABILITY AND BULK-RELATED MECHANISMS D. PROBABLY IONIC CONTAMINATION	1@175°C 2@275°C	1@128 1@256 12@500 6@1000	1@4 1@32 4@64 2@128 6@256 5@500 7@1000	3@4 1@16 5@32 1@64 2@128 2@256 3@500 3@1000	1@200°C	1@64	1@4	1@8 1@500
A. I_{IB} B. NONE C. NONE D. V_{CM} TOO HIGH	2@175°C							
A. I_O B. DEGRADED Q15 COLLECTOR - SUBSTRATE DIODE C. PROBABLY INVERSION OF THE COLLECTOR D. PROBABLY CATION CONTAMINATION		1@128		1@4 1@8				
+125°C ONLY FAILURES AND RANDOM FAILURES - NOT ANALYZED IN DETAIL								
A. CMR (RETEST OK)						1@64	2@8	
A. A_{VC} (RECOVERED)		1@128	1@500					
A. A_{VC} @ +125°C ONLY		4@1000		1@1000				
A. V_{OL} [30]				1@1000				
TOTAL NUMBER OF FAILED PARTS	5	29	25	24	3	35	29	34

8.0 DATA EVALUATIONS AND CORRELATIONS

Evaluations and correlation of the data generated during the program were performed to determine device aging characteristics. This was accomplished through comparisons of the types of failure modes observed in each test, plots of failure distributions, Arrhenius model evaluations, and calculations of use temperature failure rates. The determination of failure distributions, Arrhenius model parameters, and use temperature failure rates generally followed published techniques [2], [3], and [4].

8.1 FAILURE MECHANISM IDENTIFICATION

The types of failure mechanisms generated for each device type during step-stress and accelerated life testing are summarized in Table 22. The first three mechanisms (inversion of an N-type tub, collector or base, depletion or inversion of a P-type base, and surface instability mechanisms which could not be traced to a specific mechanism) are all surface related mechanisms. These surface related mechanisms accounted for 75% of the total number of device failures. The second largest group of failures (9%) was attributed to a localized thermal runaway mechanism. This mechanism was time-temperature dependent but the cause of this dependency could not be determined. Only a small percentage of devices (approximately 1% for each mechanism) failed due to dielectric breakdown (oxide related), Kirkendall voiding (wire bond related), and gold leaching (package related). The failure mechanisms for a small percentage (3%) of the failures are classified as unknown because either the devices had recovered before the failure mechanism could be established, or the devices were not investigated since the devices exhibited only a single marginally out-of-tolerance parameter, or a single parametric failure at 125°C only, or a random isolated type of failure.

A summary of the types of defects observed and the suspected defect causes is shown in Table 23 for each manufacturer's device type. The absolute cause of failure could not be positively determined in many cases, consequently many of the failures identified as process-related may ultimately or indirectly involve the design or materials of the device. Nevertheless, the failures

TABLE 22. FAILURE MECHANISM SUMMARY

FAILURE MECHANISM	LM118				LM108A				723				LM109				LM111			
	MFR B		MFR C		MFR A		MFR B		MFR C		MFR D		MFR B		MFR D		MFR B		MFR D	
	NO.	%	NO.	%	NO.	%	NO.	%	NO.	%	NO.	%	NO.	%	NO.	%	NO.	%	NO.	%
1. INVERSION OF N-TYPE TUB, COLLECTOR, OR BASE	83	89	2	10			86	96									67	81	5	5
2. DEPLETION OR INVERSION OF P-TYPE BASE	2	2	4	19													6	7	93	92
3. SURFACE INSTABILITY ⚠					10	17					2	67								
4. THERMAL RUNAWAY			7	33	37	62														
5. DIELECTRIC BREAKDOWN			5	23																
6. KIRKENDALL VOIDING													4	45						
7. Au LEACHING													2	22						
8. STATIC CHARGE ACCUMULATION					9	15	4	4												
9. MECHANICAL OVERSTRESS													2	22	1	11				
10. ELECTRICAL OVERSTRESS	1	1	2	10																
11. NONE (TEST SET ERROR)	7	8							8	100					8	89	2	2		
12. UNKNOWN			1	5	4	6					1	33	1	11			8	10	3	3
TOTAL	93	100	21	100	60	100	90	100	8	100	3	100	9	100	9	100	83	100	101	100

⚠ Specific Mechanism Unknown

TABLE 23. DEFECT/CAUSE SUMMARY

PRIMARY DEFECTS AND CAUSES	NUMBER OF FAILED DEVICES									
	LM118		LM108A		723		LM109		LM111	
	MFR B	MFR C	MFR A	MFR B	MFR C	MFR D	MFR B	MFR D	MFR B	MFR D
DEFECT CATEGORY										
1. SURFACE RELATED	85	6	10	86	0	2	0	0	73	98
2. OXIDE RELATED	0	5	0	0	0	0	0	0	0	0
3. WIRE BOND RELATED	0	0	0	0	0	0	4	0	0	0
4. PACKAGE RELATED	0	0	0	0	0	0	2	0	0	0
5. ELECTRICAL OVERSTRESS	1	2	9	4	0	0	0	0	0	0
6. TEST ERROR	7	0	0	0	8	0	2	9	2	0
7. UNDEFINED	0	8	41	0	0	1	1	0	8	3
TOTALS	93	21	60	90	8	3	9	9	83	101
CAUSE CATEGORY										
1. PROCESS RELATED	85	11	10	86	0	2	4	0	73	98
2. DESIGN RELATED	0	0	0	0	0	0	0	0	0	0
3. MATERIAL RELATED	0	0	0	0	0	0	2	0	0	0
4. WORKMANSHIP RELATED	0	0	0	0	0	0	0	0	0	0
5 TEST RELATED	8	2	9	4	8	0	2	9	2	0
6. UNKNOWN	0	8	41	0	0	1	1	0	8	3

attributed to process-related problems probably can be reduced by a tightening of process controls.

8.2 FAILURE TIME CALCULATION

The failed devices exhibited out-of-tolerance parameter values or, in some cases, catastrophic failures. Thus, the parametric data was examined for time dependent degradation and, where feasible, interpolation methods were used to determine the actual device failure time. Where the interpolated failure times were gathered about the measurement times or where the device failed catastrophically, the midpoint between the last two measurement times was used as the estimated failure time.

8.3 FAILURE DISTRIBUTIONS

Distributions of the times to failure were determined for each manufacturer's device type whenever sufficient failure data was available. The failures due to test-set related problems, and those failures that occurred only at 125°C and -55°C were not included in these analyses. In all cases, the failure time distributions were assumed to be either single lognormal distributions, or bimodal distributions that could be represented by two lognormal distributions. The bimodal distributions were represented by two lognormal distributions [6], an early distribution of failures (freak), and a later distribution of failures (main). This bimodal failure distribution is

$$\mathrm{Cdf}\{\mathrm{life}\}_{TOTAL} = \left\{\frac{1}{\sigma_F\sqrt{2\pi}}\int_0^t \frac{1}{t'}\ \exp\left\{-\frac{(\ln t' - \mu_F)^2}{2\sigma_F^2}\right\} dt'\right\} \quad (\%_F)$$
$$+ \left\{\frac{1}{\sigma_M\sqrt{2\pi}}\int_0^t \frac{1}{t'}\ \exp\left\{-\frac{(\ln t' - \mu_M)^2}{2\sigma_M^2}\right\} dt'\right\} \quad (\%_M) \qquad (1)$$

where

μ_F = ln (median life of the freak distribution)

σ_F = standard deviation of the freak distribution

μ_M = ln (median life of the main distribution)

σ_M = standard deviation of the main distribution

$\%_F$ = the percentage of the total population that is described by the freak distribution

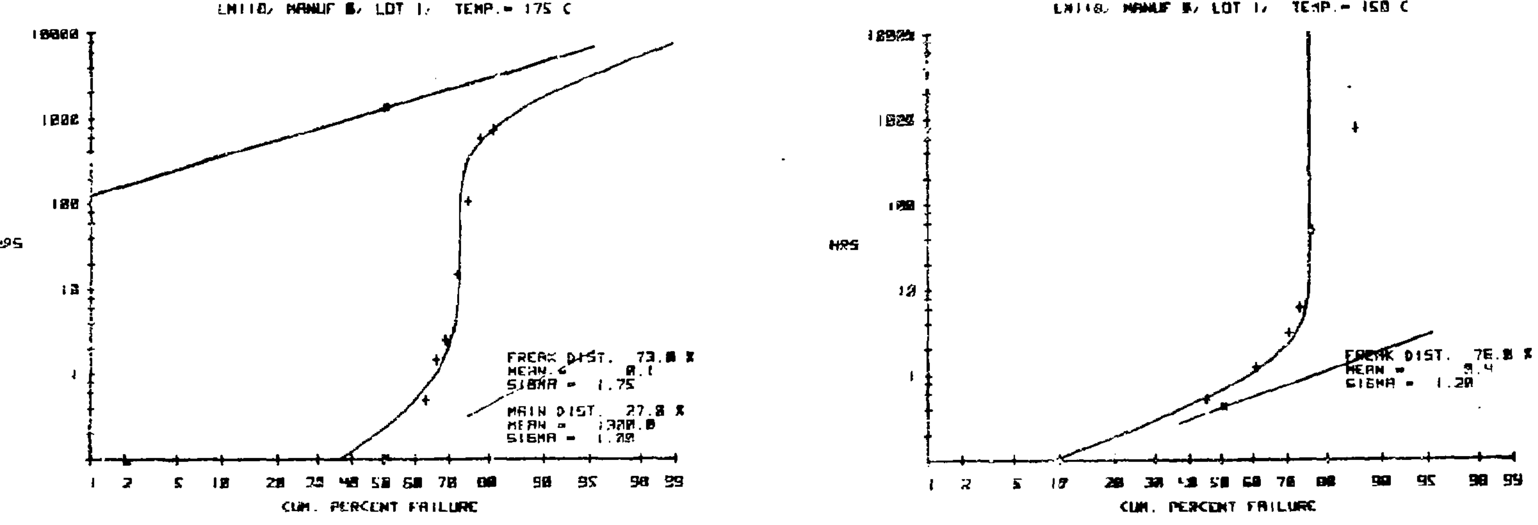
$\%_M$ = the percentage of the total population that is described by the main distribution

t = use time

The bimodal distribution was fitted using a graphical method [3], [4]. Then the graphic result was used with equation (1) and the calulated probability was compared to the test probability at each failure time. From this starting point the values of the unknowns in equation (1) were iterated and the probabilities compared until plots of the resulting equation appeared to provide a good representation of the observed data.

8.3.1 LM118 Failure Distributions - The primary failure mechanism for Manufacturer B's LM118 devices was inversion of a resistor tub, most probably caused by either the separation of mobile ionic species in the fringing field of the reverse biased junction, or electron drift in the fringing field along defects in the glass/insulator interface. Also included in the failure distributions were failures due to inversion of the collector-base junction of an input transistor and failures due to depletion of the base region of an input transistor. Both mechanisms are suspected to be caused by mobile ions or charges in the passivation layers. The failure distributions for these surface related mechanisms at each test temperature are shown in Figure 21. A bimodal distribution is indicated but the data was only sufficient to determine the main distribution median life at the highest test temperature (175°C). Even for this temperature, there are only a few data points, and the actual failure distribution of the main population cannot be accurately determined.

Only a small percentage (16.5%) of Manufacturer C's LM118 devices failed and the failures were divided into the following time-temperature dependent mechanisms: a) inversion of an input transistor, b) depletion in the base of a transistor, c) thermal runaway at C1, and d) dielectric breakdown in a capacitor. There were insufficient data to permit a valid evaluation of the Manufacturer C failure distributions.



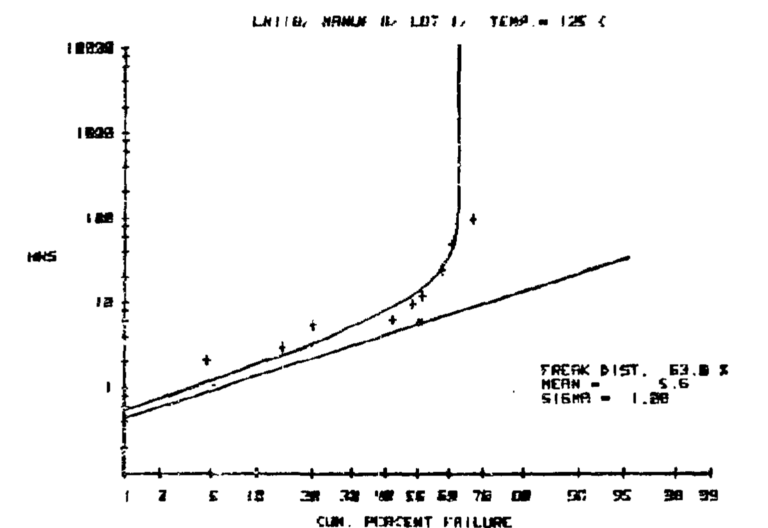
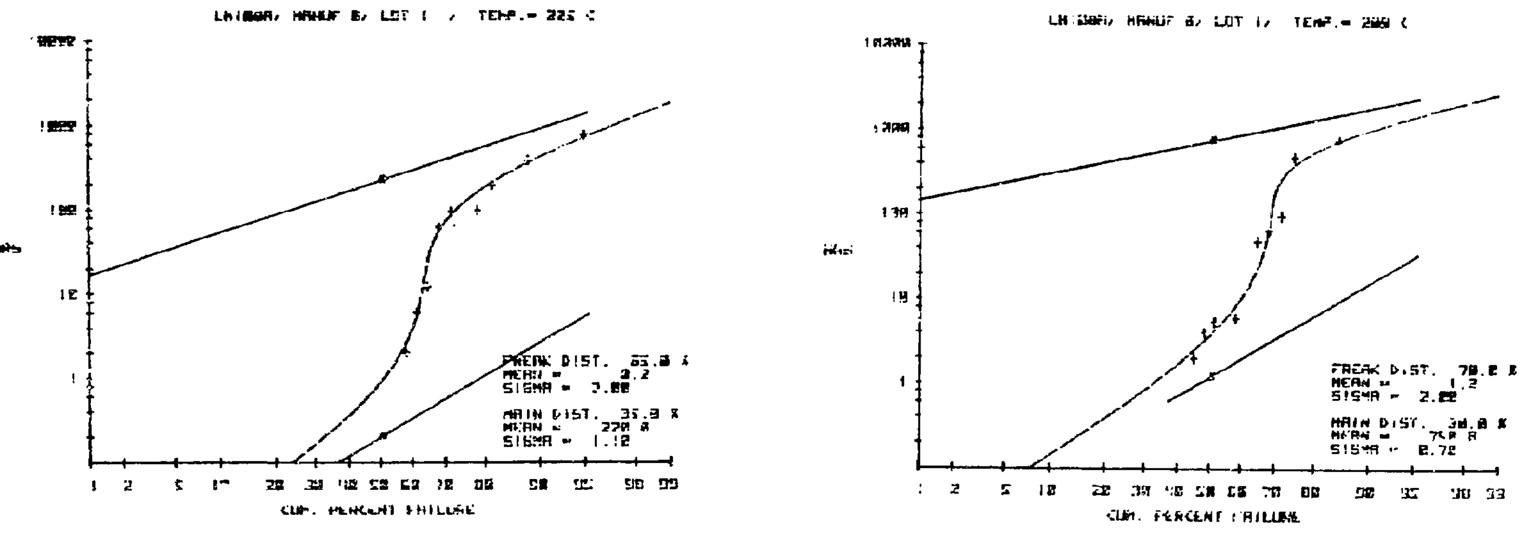


FIGURE 21. MANUFACTURER B LM118 FAILURE DISTRIBUTIONS - RESISTOR TUB INVERSION

8.3.2 LM108A Failure Distributions - The primary mechanism of failure for Manufacturer B's LM108A devices was also channel current from a resistor to the substrate due to inversion of the resistor tub. The most probable causes of this mechanism were the same as those previously mentioned for Manufacturer B's LM118 devices: either the separation of mobile ionic species in the fringing field of the reverse biased junction, or electron drift in the fringing field along defects in the glass/junction interface. The failure distributions for this mechanism are shown in Figure 22. The distributions are bimodal and the freak population accounts for approximately 65% to 70% of the total population.

The primary failure mode for Manufacturer A's devices was thermal runaway of PNP transistor Q6. Several devices also failed the gain test (A_{VS}), but these devices were left on test and most of the devices recovered. Three of the gain failures later failed at the 2000 hour test point due to thermal runaway and are included in the failure distributions. The other gain failures are not included, since the gain measurements are not representative of actual gain, and are not necessarily indicative of failure, as was discussed in Section 4.0. The failure distributions for the thermal runaway mechanism are shown in Figure 23, and are single lognormal distributions. Although thermal runaway would normally be considered a temperature dependent only mechanism, the failure distributions do indicate a time-temperature dependency. The exact cause of this dependency was not established, but is probably linked to the bulk degradation of the emitter of Q6.

8.3.3 LM111 Failure Distributions - The majority of Manufacturer B's LM111 failures were due to excessive I_{IO} and the failures were attributed to two mechanisms, a surface related (reversible) mechanism which predominated at 200°C and a bulk related (nonreversible) mechanism which predominated at 225°C and 250°C. Also included in the failure distribution plots were the two other surface related mechanisms, inversion of the base of an input transistor, and inversion of the collector region in an output transistor. Both mechanisms were probably caused by ionic contamination in or on a passivation layer. The 25°C collector gain (A_{VC}) failures were excluded from the distributions due



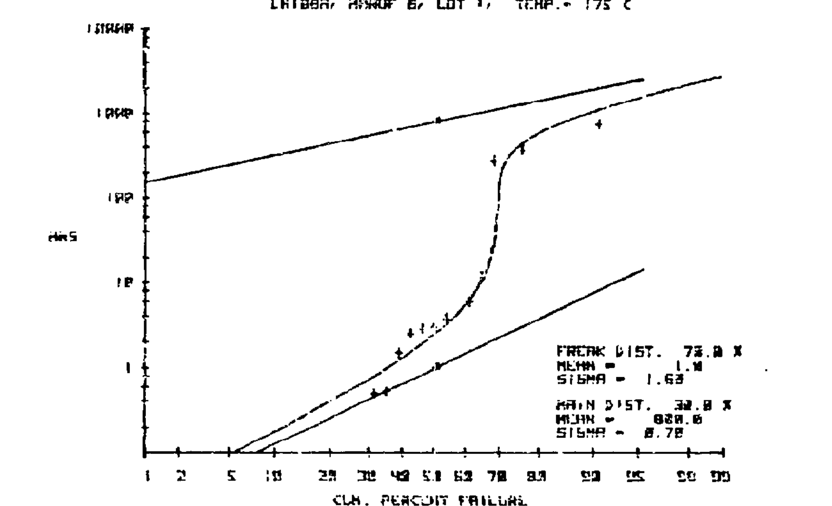
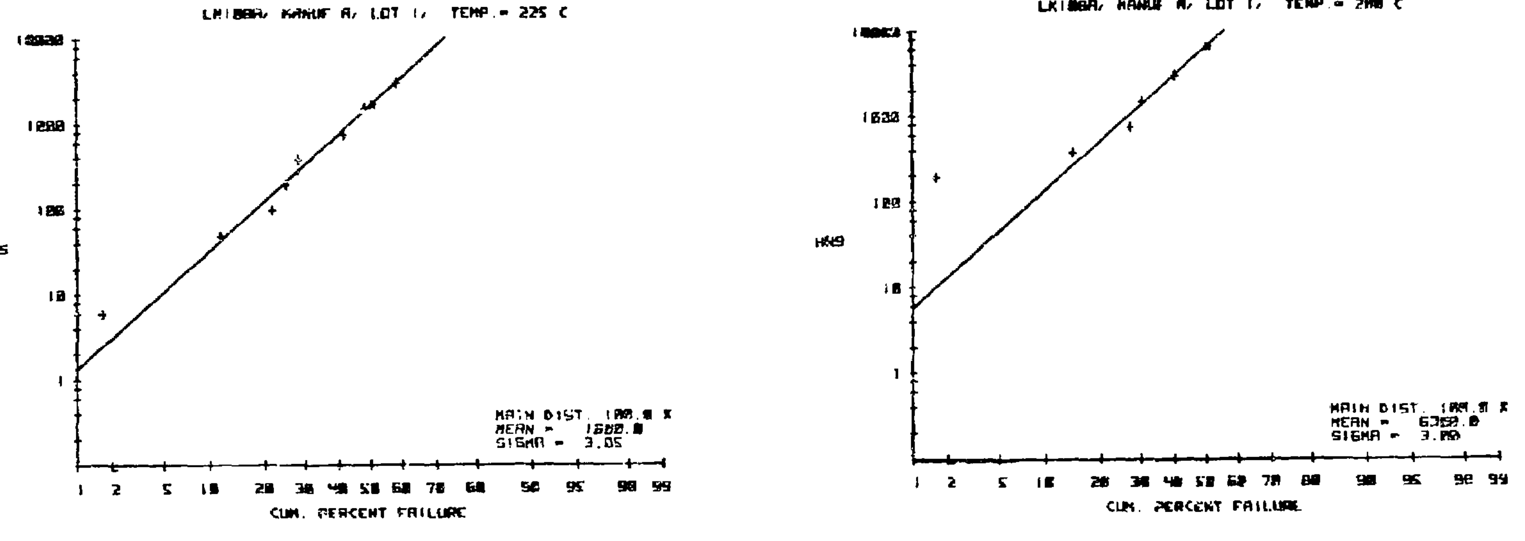


FIGURE 22. MANUFACTURER B LM108A FAILURE DISTRIBUTIONS- RESISTOR TUB INVERSION



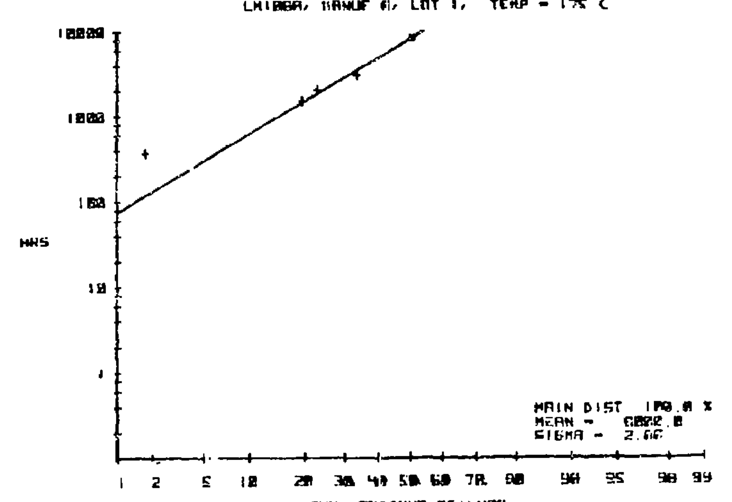


FIGURE 23. MANUFACTURER A LM108A FAILURE DISTRIBUTIONS- LOCALIZED THERMAL RUNAWAY

to the nonlinearity of the gain measurements. The resulting failure distributions shown in Figure 24 indicate single lognormal distributions at each test temperature. The difference in standard deviation (sigma) between the 200°C plot and the higher temperature plots supports the failure analysis findings suggesting different mechanisms predominating at those temperatures.

The primary mechanism for Manufacturer D's LM111 devices was an inversion of the base of an input transistor, a surface related mechanism most probably caused by ionic contamination in or on a passivation layer. Also included in the failure distribution plots were four I_{IO} failures due to the surface instability and bulk mechanism discussed above. The failure distribution plots indicate a bimodal distribution at all test temperatures as shown in Figure 25.

8.3.4 LM109 and 723 Failure Distributions - Insufficient failure data was generated in the accelerated life tests of both the 723 and LM109 devices to permit evaluation of the failure distributions.

8.4 AGING CHARACTERISTICS

Sufficient multiple temperature data was generated during the accelerated life tests of the Manufacturer B LM118 and both manufacturers' LM108 and LM111 devices to evaluate aging characteristics for these device types. The Arrhenius reaction rate model [4] was found to provide a good representation of the aging characteristics for the freak and main device populations, and was used to relate median lifetime and junction temperatures as follows:

$$t_{50\%} = A \exp\left(\frac{E_A}{kT}\right) \quad (2)$$

where

$t_{50\%}$ = freak or main population median lifetime at a junction temperature
A = A constant
E_A = Experimental activation energy - eV
k = Boltzman's constant - 8.617 x 10^{-5} eV/Kelvin
T = Absolute junction temperature - Kelvin

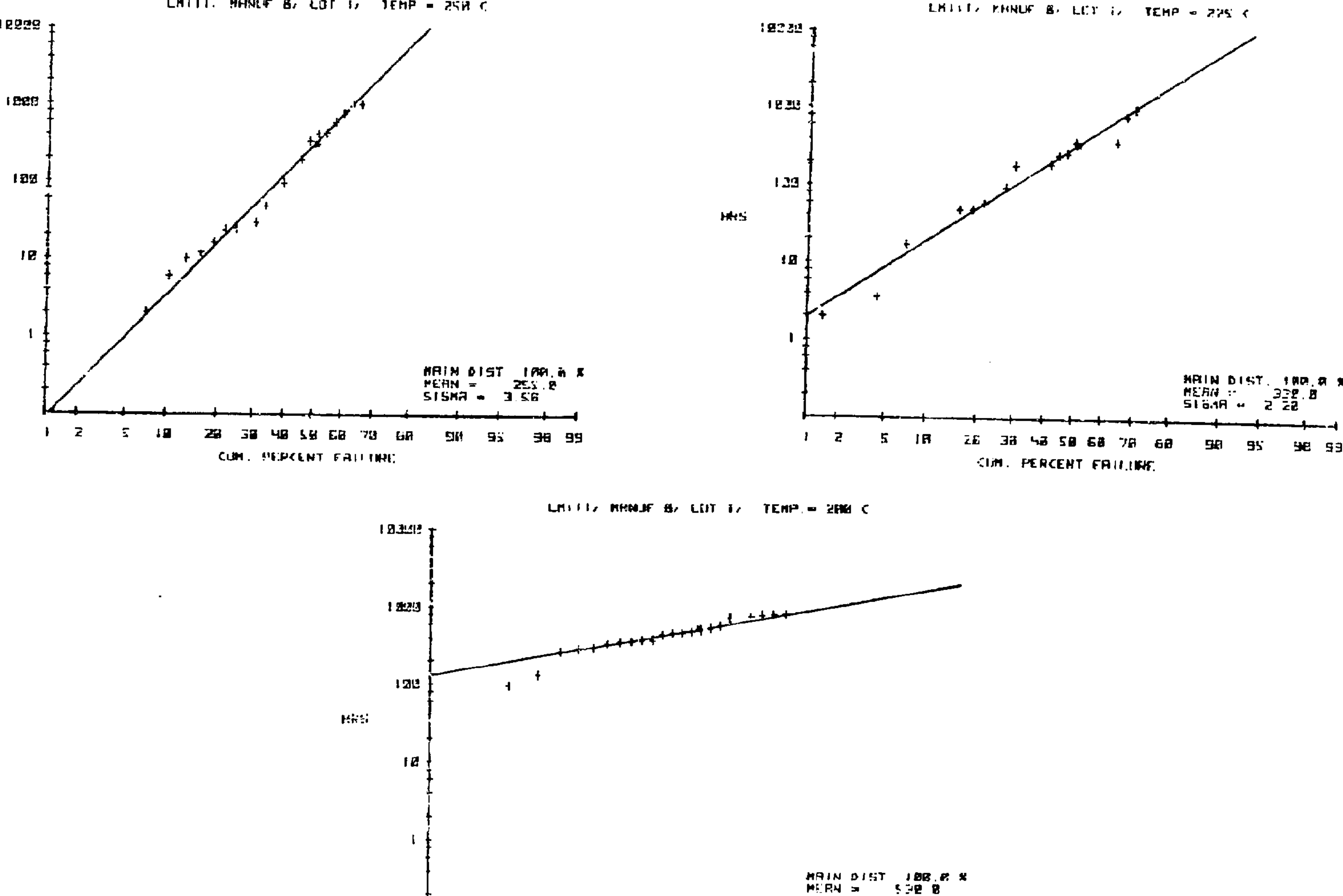
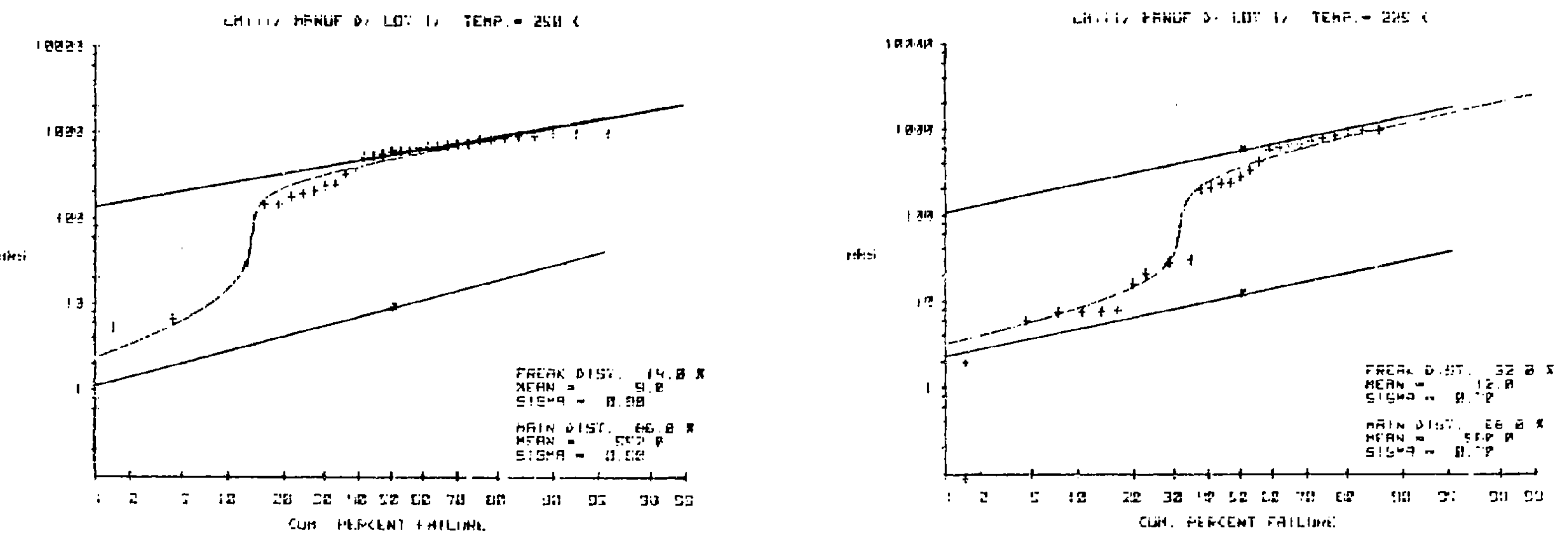


FIGURE 24. MANUFACTURER B LM111 FAILURE DISTRIBUTIONS - SURFACE INSTABILITY & BULK RELATED



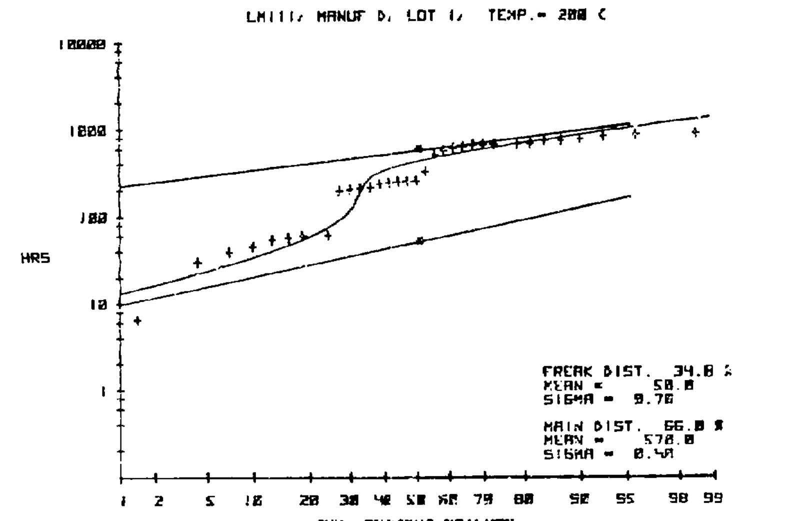


FIGURE 25. MANUFACTURER D LM111 FAILURE DISTRIBUTIONS - TRANSISTOR BASE INVERSION

The linear transform of this equation is

$$\ln t_{50\%} = \ln A + \frac{E_A}{k} \left[\frac{1}{T}\right] \tag{3}$$

The transformed Arrhenius equation was evaluated using a linear regression analysis that assumes the junction temperature is a known value and $\ln t_{50\%}$ is the only variable [7], [8].

8.4.1 Manufacturer B's LM118 Devices - The Arrhenius plot for Manufacturer B's LM118 freak population failures is shown in Figure 26. The activation energy was calculated to be 1.24 eV for the surface instability mechanisms responsible for the failures. The freak population consisted of approximately 72% of the sample size. There was insufficient data to calculate the main population activation energy.

8.4.2 Manufacturer A's LM108A Devices - Sixty-two percent of Manufacturer A's LM108A device failures were attributed to thermal runaway at the Q6 transistor. At elevated temperatures the current in the transistor reached excessive levels, resulting in catastrophic damage to the device. Normally this would not be considered a time-temperature dependent mechanism, but evaluation of the failure data indicated that the failures were time-temperature dependent as shown in Figure 27. The activation energy for this mechanism was calculated to be 0.61 eV.

8.4.3 Manufacturer B's LM108A Devices - Manufacturer B's LM108A time-temperature related device failures were due to inversion of a resistor tub. The Arrhenius plot for this failure mechanism is shown in Figure 28. The activation energy was calculated to be 0.61 eV for the freak population and 0.49 eV for the main population. Both these activation energies differ from the 1.24 eV activation energy calculated for the Manufacturer B LM118 freak population with a similar failure mechanism. The failure mechanism in both devices was suspected to be either separation of the mobile ionic species in the fringing field of the reverse biased junction, or electron drift in the fringing field

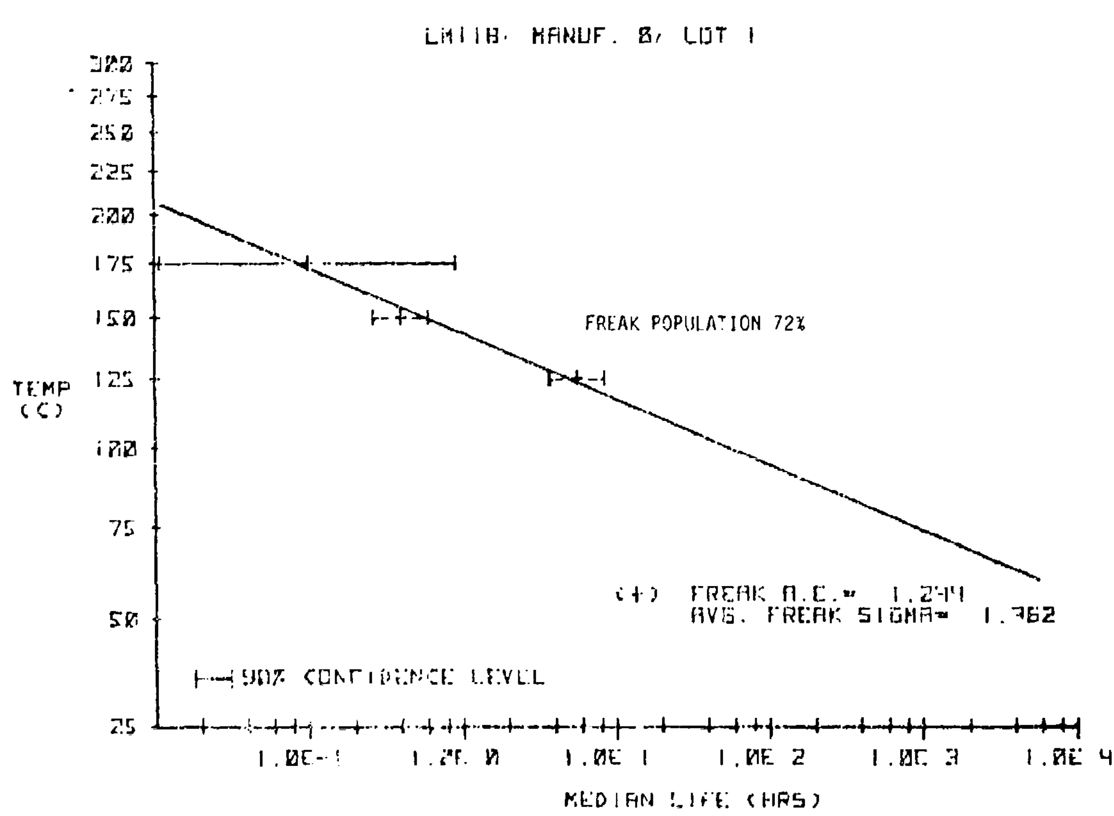


FIGURE 26. MANUFACTURER B LM118 ARRHENIUS PLOT - RESISTOR TUB INVERSION

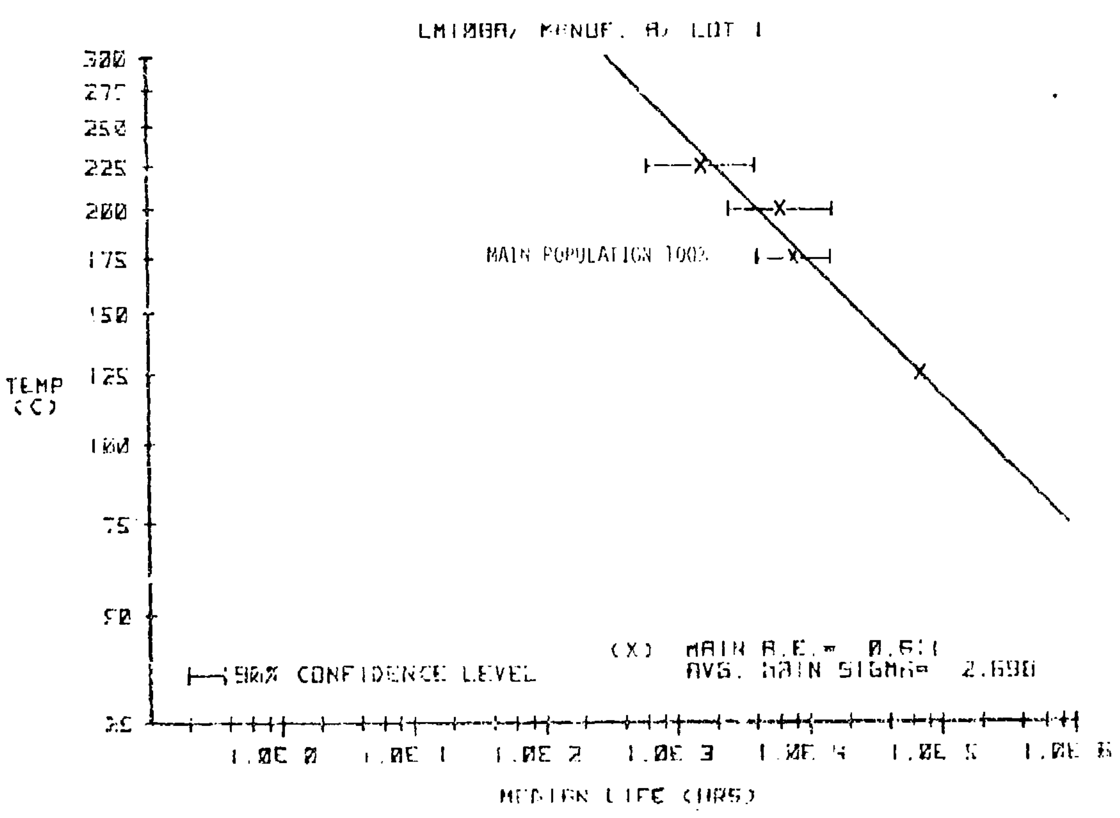


FIGURE 27. MANUFACTURER A LM108A ARRHENIUS PLOTS - LOCALIZED THERMAL RUNAWAY

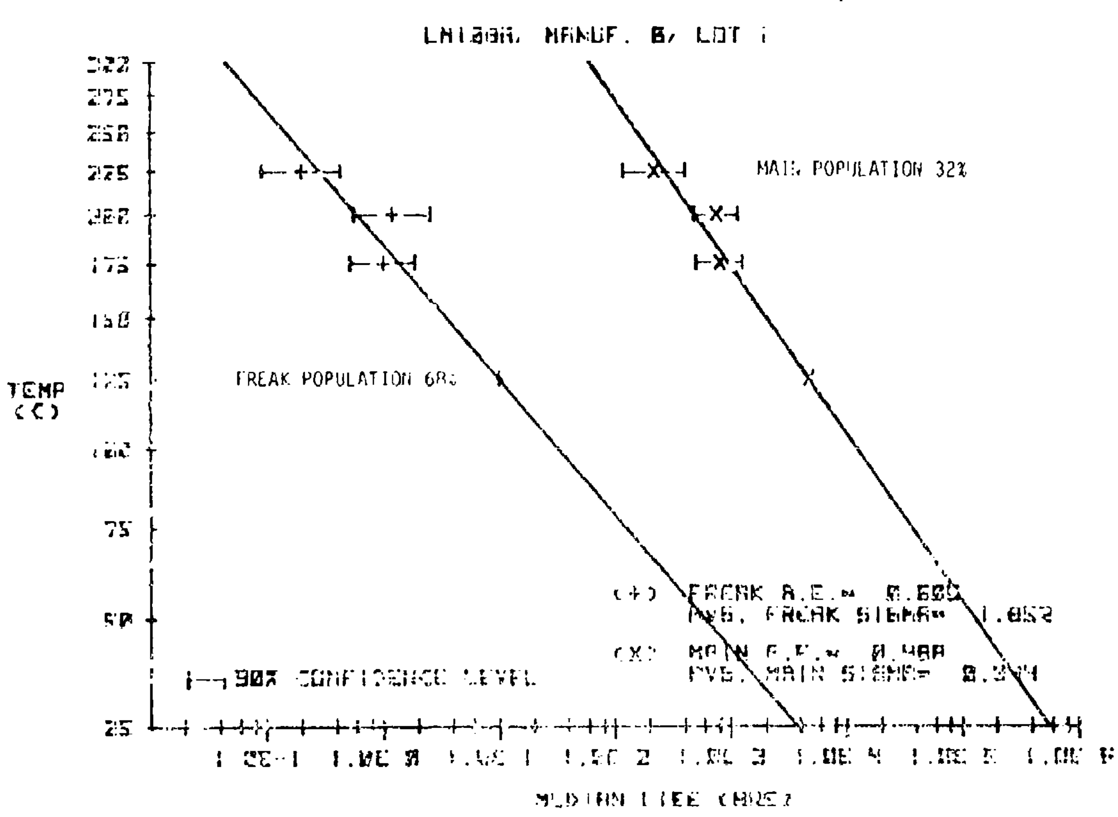


FIGURE 28. MANUFACTURER B LM108A ARRHENIUS PLOTS - RESISTOR TUB INVERSION

along defects in the glass/junction interface. Thus, the difference in activation energies is possibly due to one mechanism predominating in one device and the other mechanism predominating in the other device.

8.4.4 Manufacturer B's LM111 Devices - The Arrhenius plot shown in Figure 29 is for the bulk failure mechanism which predominated at the 225°C and 250°C temperatures. This mechanism exhibited an apparent activation energy of 0.10 eV. Also shown on the plot is the median life of the 200°C failures which were attributed to a surface related mechanism. Since no 200°C life test failures were attributed to the bulk related mechanism, the Arrhenius plot for this mechanism should not be extended below 225°C. However, the exact nature of both the bulk and surface related mechanisms could not be determined, and it is possible that the two mechanisms are related. Therefore, as a means of establishing a conservative estimate of use-temperature failure rates, the Arrhenius plot has been extended below 225°C.

8.4.5 Manufacturer D's LM111 Devices - The freak population accounted for an average of 28% of Manufacturer D's LM111 devices and exhibited an activation energy of 0.74 eV as shown in Figure 30. The main population exhibited a very low activation energy of 0.01 eV. This indicates a non-temperature dependent failure mechanism. Approximately 50% of the failures due to this mechanism occurred between the 500 and 1000 hour measurement points at each test temperature. Also, the calculated median lifetimes of the main population at each test temperature were all approximately 600 hours. An examination of the parameter drift data was made in an effort to determine the reason for this low activation energy. The value of the failing parameter (V_{IO}) was plotted versus test time as shown in Figure 31. It was noted that the parameter value would sometimes increase if the device were left on bias at 25°C for a period longer than 24 hours prior to being electrically tested. However, the overall drift of the devices does appear to be independent of temperature. The failure analysis of the devices determined that the mechanism was bake recoverable and that the failures were due to a gain mismatch in the input transistors, most probably caused by ionic contamination. This mechanism is generally time-temperature dependent, but there were no other anomalies that would account for the temperature independent nature of the failures.

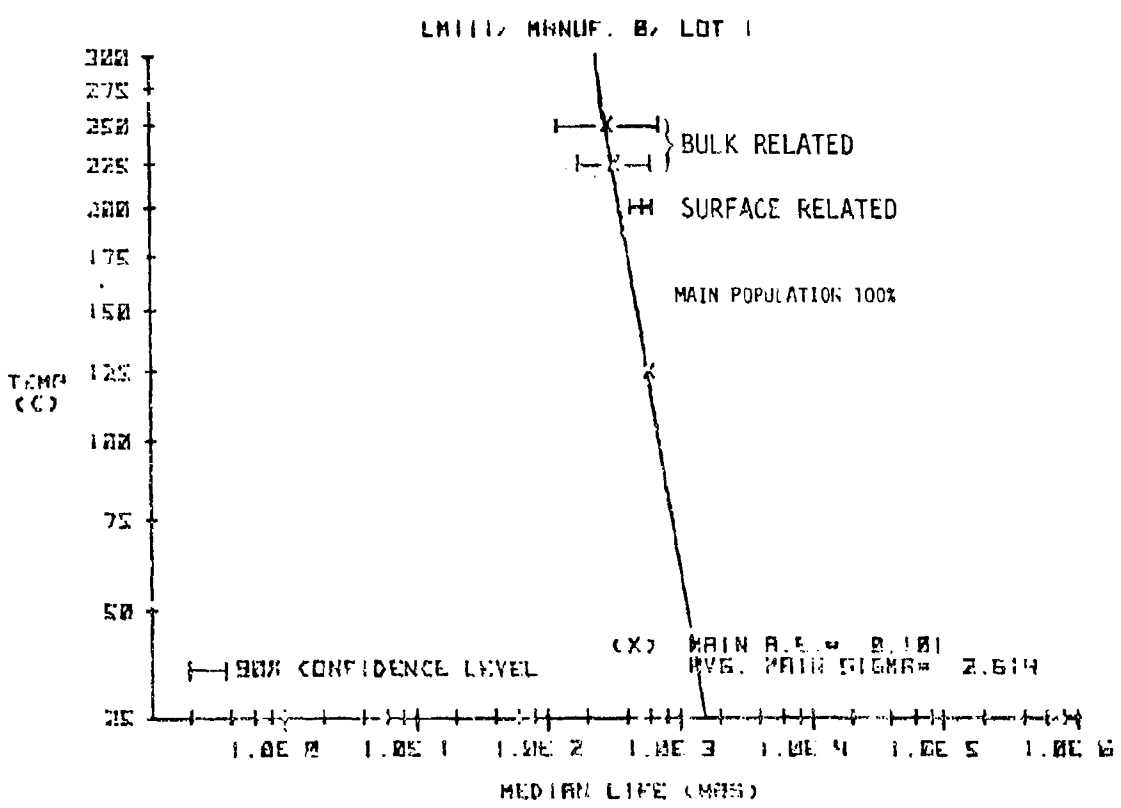


FIGURE 29. MANUFACTURER B LM111 ARRHENIUS PLOTS - SURFACE INSTABILITY AND BULK RELATED

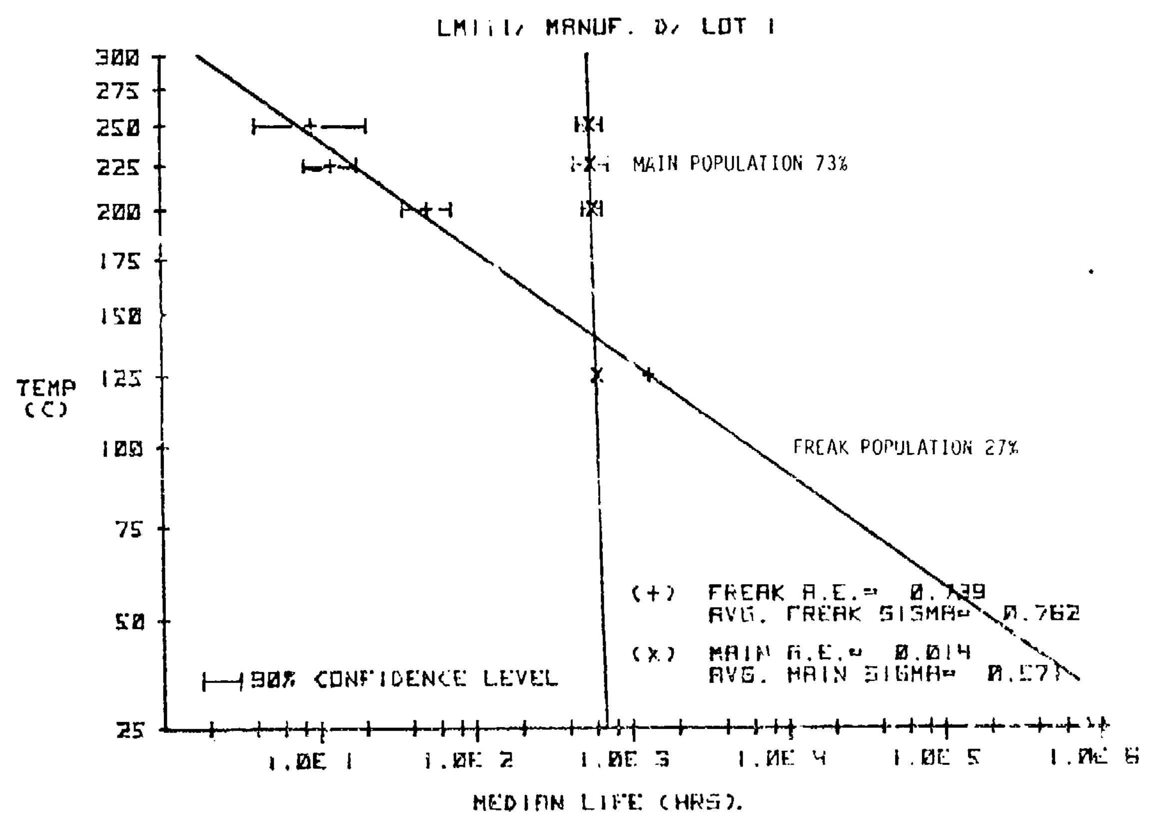


FIGURE 30. MANUFACTURER D LM111 ARRHENIUS PLOTS - TRANSISTOR BASE INVERSION

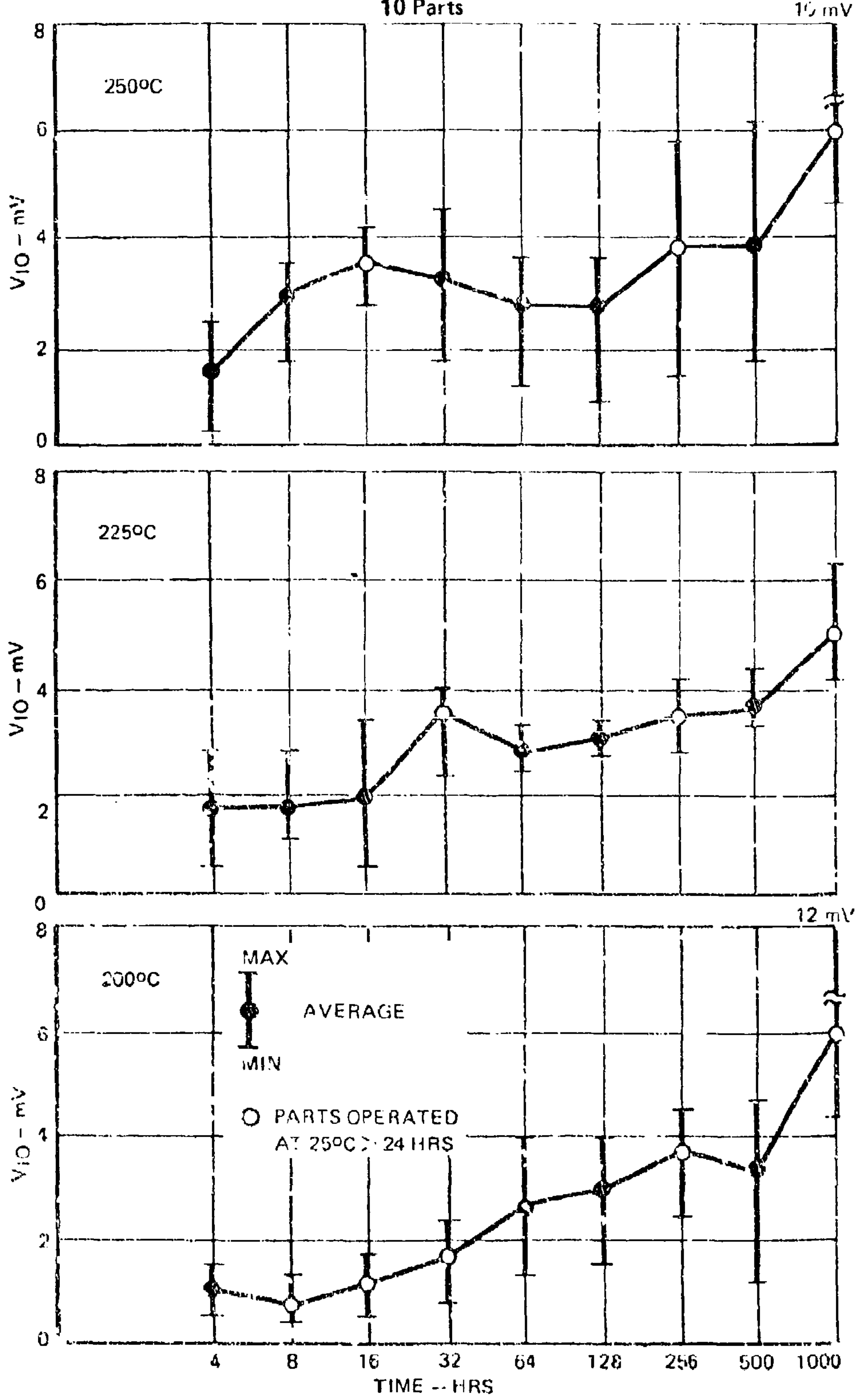


FIGURE 31. MANUFACTURER D LM111 OFFSET VOLTAGE PARAMETER DRIFT

8.5 FAILURE RATES

Use-temperature failure rates were calculated using the values shown in Table 24 for Arrhenius model parameters (constant "A" and activation energy "E_A"), average value of lognormal distribution standard deviation and percent freak and main population. The failure rate for a single distribution is defined as [9]

$$\lambda(t) = \frac{f(t)}{R(t)} \tag{4}$$

where

$\lambda(t)$ = the instantaneous failure rate at time

$f(t)$ = the failure density at time t

$R(t)$ = the reliability at time t.

Also, a lognormal failure rate for a single distribution is defined as [10]

$$\lambda(t) = \frac{\frac{1}{t\,\sigma\sqrt{2\pi}} \exp\left\{-\frac{(\ln t - \mu)^2}{2\sigma^2}\right\}}{\frac{1}{\sigma\sqrt{2\pi}}\int_t^\infty \frac{1}{t'} \exp\left\{-\frac{(\ln t - \mu)^2}{2\sigma^2}\right\} dt'} \tag{5}$$

where

μ = ln (median life)

σ = the standard deviation.

Assuming that an Arrhenius equation defines the median life at a junction temperature provides the following temperature dependent, lognormal failure rate:

$$\lambda(t) = \frac{\frac{1}{t\,\sigma\sqrt{2\pi}} \exp\left\{-\frac{[\ln t - (\ln A + E_A/k\,T)]^2}{2\sigma^2}\right\}}{\frac{1}{\sigma\sqrt{2\pi}}\int_t^\infty \frac{1}{t'} \exp\left\{-\frac{[\ln t' - (\ln A + E_A/k\,T)]^2}{2\sigma^2}\right\} dt'} \tag{6}$$

TABLE 24. SUMMARY OF FAILURE RATE PARAMETERS

PART TYPE	MFR	FAILURE MECHANISM	AVG % FREAK	AVG % MAIN	FREAK			MAIN		
					E_A (eV)	A	σ AVG	E_A eV	A	σ AVG
LM108A	A	THERMAL RUNAWAY AT QE	0	100	-	-	-	0.63	1.30×10^{-3}	2.70
LM108A	B	RESISTOR TUB INVERSION	68	32	0.61	2.15×10^{-7}	1.92	0.49	3.13×10^{-3}	0.84
LM118	B	RESISTOR TUB INVERSION	72	28	1.24	8.56×10^{-16}	1.36	⚠	-	-
LM111	B	TRANSISTOR BASE INVERSION	0	100	-	-	-	0.10	1.03	2.42
	D	BULK RELATED	27	73	0.74	5.68×10^{-7}	0.76	0.01	4.07×10^{2}	0.57

NOTE:

⚠ INSUFFICIENT DATA TO CALCULATE PARAMETER VALUES.

For a bimodal distribution consisting of two lognormal failure rates, the total failure rate is defined as

$$\lambda(t)_{TOTAL} = (t)_{freak} \ (\% \text{ freak}) + (t)_{main} \ (\% \text{ main}) \qquad (7)$$

These techniques were used to calculate the maximum instantaneous failure rates shown in Table 25 Comparison of the 125°C and 50°C failure rates illustrate the value of junction temperature derating to achieve improved failure rates for the predominant failure mechanisms. Additional factors for secondary failure modes must be included in the total device failure rate prior to using the failure rates for reliability estimates.

The failure rates shown are for device junction temperatures of 125°C and 50°C. The failure rates are based on the predominant failure mechanism for all devices. The devices were burned-in by the manufacturer for 168 hours at 125°C. The specified additional hours of 125°C burn-in shown in Table 25 would be required to eliminate 99.9% of the freak population. Removal of 99.9% of the freak population can be assumed to constitute removal of all freak devices. An additional 271 hour burn-in at 225°C for Manufacturer B's LM108A devices would result in an improvement in failure rate, but would eliminate 22% of the main population, and since the freak population consisted of 68% of the sample, this would result in 75% of the devices being removed. An additional burn-in of 30 hours at 175°C would remove the freak population of Manufacturer B's LM118 device, but there was insufficient data to evaluate the main population failure rate. Also the freak population accounted for 72% of the sample size. An additional burn-in for Manufacturer D's LM111 device would actually increase the failure rate due to the fact that the median lifetime of the main population is actually less than the freak population at temperatures less than 150°C. Additional burn-in for those devices which exhibited a single lognormal distribution would not result in improved failure rates without sacrificing a high percentage of the total population. In general, additional burn-in is not recommended since either it is not cost effective, or the failure rates cannot be greatly improved.

TABLE 25. FAILURE RATE SUMMARY

DEVICE	MFR	MAXIMUM INSTANTANEOUS FAILURE RATE IN 10^5 HOURS OF USE TIME (FAILURE/HOUR)				BURN-IN CONDITIONS	
		WITHOUT BURN-IN		WITH BURN-IN			
		125°C	50°C	125°C	50°C	TIME (HRS)	T_j (°C)
LM108A	A	8.02×10^{-5}	2.27×10^{-8}	△1	-	-	-
LM108	B	8.44×10^{-2}	1.94×10^{-3}	1.78×10^{-4}	6.52×10^{-6}	271	225
LM118	B	1.22×10^{-1}	2.69×10^{-5}	△2	-	30	175
LM111	B	7.77×10^{-3}	3.93×10^{-3}	△1	-	-	-
	D	2.14×10^{-3}	1.35×10^{-3}	1.89×10^{-3}	1.73×10^{-3}	201	250

NOTES:

△1 SINGLE LOGNORMAL DISTRIBUTION, ADDITIONAL BURN-IN NOT RECOMMENDED.

△2 INSUFFICIENT DATA TO CALCULATE MAIN FAILURE RATES.

9.0 CONCLUSIONS

The results of this study indicate that linear microcircuit manufacturers have the capability of producing high reliability devices which would be acceptable for use in military applications. Also the MIL-M-38510 specification for testing the linear devices studied in this program appear adequate to fully electrically characterize the devices. However, there were differences between the same device type from different manufacturers and between different device types from the same manufacturer. These differences indicate that tighter controls over both the electrical testing and the manufacturing processes are necessar to produce high reliability devices.

Although the devices were procured as capable of meeting the MIL-M-38510 specifications, several of the devices failed to conform to all of the test specification limits. Initial electrical failures were a minimum in the one JAN qualified device, but were numerous in all other devices. In most cases the parameter end-point limits were expanded to obtain a sufficient number of devices for further evaluations. With the expanded limits, as many as 33% of a particular manufacturer's devices failed initial electrical tests. Although many parameter end-point limits had to be expanded, the MIL-M-38510 electrical test limits are adequate with the exception of the LM111 device. Each manufacturer's device failed different electrical parameters, and not all devices from a particular manufacturer failed a specific electrical parameter, indicating that the MIL-M-38510 electrical test limits were capable of being met.

Information obtained in testing the LM111 devices indicate the current MIL-M-38510/10304 (8 March 1977) is in need of revision. With the LM111 devices, the static and dynamic test circuit was impossible to stabilize. Several attempts to construct the MIL-M-38510 test circuit resulted in severe oscillations in the device under test. Attempts to reduce these oscillations for a particular parameter test only produced worse conditions for other parameters. The devices were eventually tested with two separate test fixtures, each of which was specially designed to dampen oscillations for specific parameters without affecting other test results. Due to oscillations, several tests were not performed with either fixture, including all

tests required at -55°C. It was beyond the scope of this program to further investigate the oscillating LM111s because the oscillations may have been partly or entirely the fault of the particular devices available at the time of procurement.

Revisions are necessary to some of the MIL-M-38510 specifications due to the nonlinearities of the gain of the operational amplifiers and the comparators, and the instability of the comparators. Linearity in the gain measurements can be increased by reducing the load current during the gain tests. It is further recommended that the emitter gain tests for the comparators be deleted due to the instability of the part in this configuration. Minor revisions to the specifications should also be made as detailed in section 5.4. With the above exceptions, all remaining MIL-M-38510 specifications/ methods are adequate to electrically characterize the devices evaluated in this report.

Maximum temperatures at which the linear microcircuits would operate satisfactorily during accelerated life tests were widely dispersed for the devices evaluated. Particular maximum temperatures varied for device types within the same family (LM108A and LM118) and also varied for different devices fabricated by the same manufacturer. A maximum temperature of 175°C was utilized for the LM118 devices, while a 250°C maximum was utilized for the LM109 and LM111 devices. During life tests, the output voltages of several device types were different from the voltage levels which would be present had the devices operated in the -55°C to +125°C temperature range. Devices were either thermally biased (LM108A and LM111) or the outputs were suppressed by thermal protection networks within the die (LM109). It is believed that thermally biasing operational amplifiers and suppressing the output voltages of the regulators represent valid accelerated life test conditions. Therefore, the temperature at which thermal runaway occurs should be considered the limiting factor in selecting life test temperatures, not the temperature at which thermal biasing or voltage suppression occurs.

In procuring sufficient good devices from a single manufacturer some devices which failed initial electrical tests were returned for replacements.

Date codes on the replacement devices were different from the date codes on the original devices indicating the devices were from different lots. Although subsequent construction analysis noted no differences, the replacement devices exhibited parameter failures different from the failures of the initial devices. Lot to lot variations in linear devices were not determined in this contract due to limited sample sizes, but these variations should be considered in reliabiltiy evaluations.

The failure rates for the operational amplifiers (LM108A and Manufacturer B's LM118) ranged from 1.22×10^{-1} failures per hour to 8.02×10^{-5} failures per hour. The failure rates for the comparators (LM111) were in the 1×10^{-3} failure per hour range. The failure rates indicate that these particular devices would not be acceptable for most military applications. Also, additional burn-in would not reduce the failure rate for these devices. The voltage regulators (LM109 and 723) and Manufacturer C's LM118 operational amplifiers exhibited too few failures during the 4000 hour life tests to compute failure rates, but it is expected that these devices would have median lives greater than 4000 hours when operated at life test temperatures, and could be expected to exhibit acceptable failure rates for military applications.

The primary failure mechanisms for the LM108A operational amplifiers, Manufacturer B's LM118 operational amplifier, and the LM111 comparators were surface related. As a group, surface related failure mechanisms accounted for 76% of the total number of failures. Although, in many cases, the absolute cause of the failure could not be positively determined, those failures which are due to surface related mechanisms can be greatly reduced by tightening process controls.

10.0 REFERENCES

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[9] I. Bazovsky, "Reliability Theory and Practice", Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1961.

[10] L. R. Goldthwaite, "Failure Rate Study for the Log Normal Lifetime Model", IRE (NSRQCE) Conference, pp. 208-213, 1961.

APPENDIX A

CONSTRUCTION ANALYSIS

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CONSTRUCTION ANALYSIS

M38510/10104BGC

MANUFACTURER A

OPERATIONAL AMPLIFIER

DATE CODE 7543

MICROCIRCUIT CONSTRUCTION INFORMATION

S/N: 11 DATE CODE: 7643 DATE: 5/9/77

PART NAME: Operational Amplifier

MANUFACTURER'S PART NO.: 108A883B MANUFACTURER: A

GENERIC PART NO.: LM108A PACKAGE TYPE: 8 Pin Can

MILITARY SPECIFICATION NO.: M38510/10104BGC

A. PACKAGE DETAILS (See Figure A1-1)

Lead Material: Gold Plated Kovar

Lead Finish - Internal: Gold Plate

- External: Gold Plate

- Feed Through: None

Header Material: Gold Plated Kovar

Cap Material: Gold Plated Nickel

Case Seal Method: Weld

Lead Seal Material/Method: Matched Glass

B. INTERCONNECTION DETAILS (See Figure A1-2)

Die Mounting Material: Gold-Silicon Eutectic

Interconnect Wire Material: Aluminum

Interconnect Wire Diameter: 0.0012 inch

Longest Interconnect Wire Length: 0.086 inch

Wire Bond Type(s) Post: Ultrasonic (See Figure A1-4)

Die: Ultrasonic (See Figure A1-3)

C. DIE DETAILS (See Figure A1-6)

Passivation Type: Silicon Dioxide

Glassivation Type: Vapor Deposited Glass

Basic Die Construction: Epitaxial Planar

Die Dimensions: 0.056 inch x 0.041 inch

Metalization Type: Aluminum

Metalization Thickness: 13,748Å

Scribe Method: Mechanical

Bond Pad Size: 0.007 inch x 0.007 inch

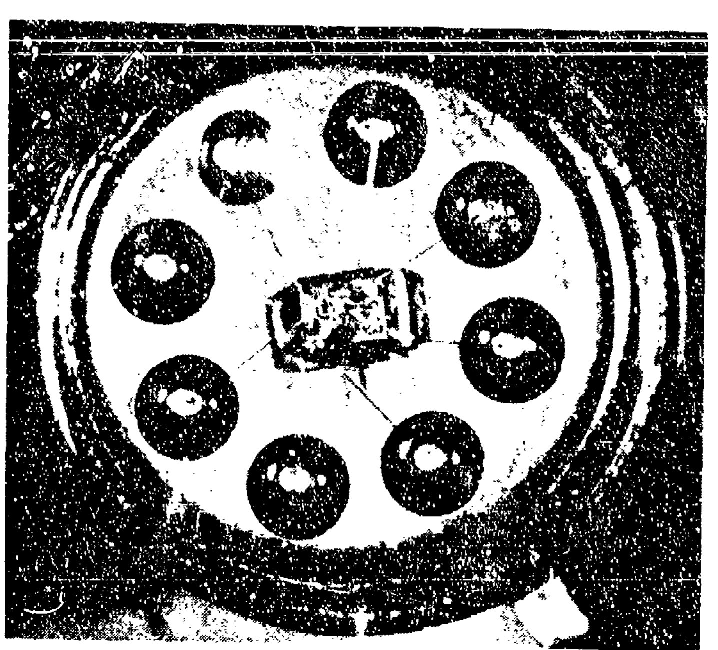
V_{CC} Stripe Cross-Sectional Area: 1.37×10^{-4} cm x 4.65×10^{-3} cm = 6.39×10^{-7} cm^2

5X

S/N11

FIGURE A1-1 - PACKAGE PHOTOGRAPH

10X



S/N11

FIGURE A1-2 - INTERCONNECT PHOTOGRAPH

530X
SEM
(SEM-1.2KV)

S/N11

FIGURE A1-3 - WIRE BOND AT DIE

530X
SEM
(SEM-1.2KV)

S/N11

FIGURE A1-4 - WIRE BOND AT POST

D. ELECTRICAL SCHEMATIC

Since the schematic for Manufacturer A was not included in military specification MIL-M-38510/10104, a schematic diagram was obtained from Manufacturer A. The accuracy of this schematic was confirmed by a detailed microscope examination of the die after glassivation removal. The schematic was found to be correct. The schematic is included as Figure A1-5 and the die photograph with circuit elements identified is included as Figure A1-6.

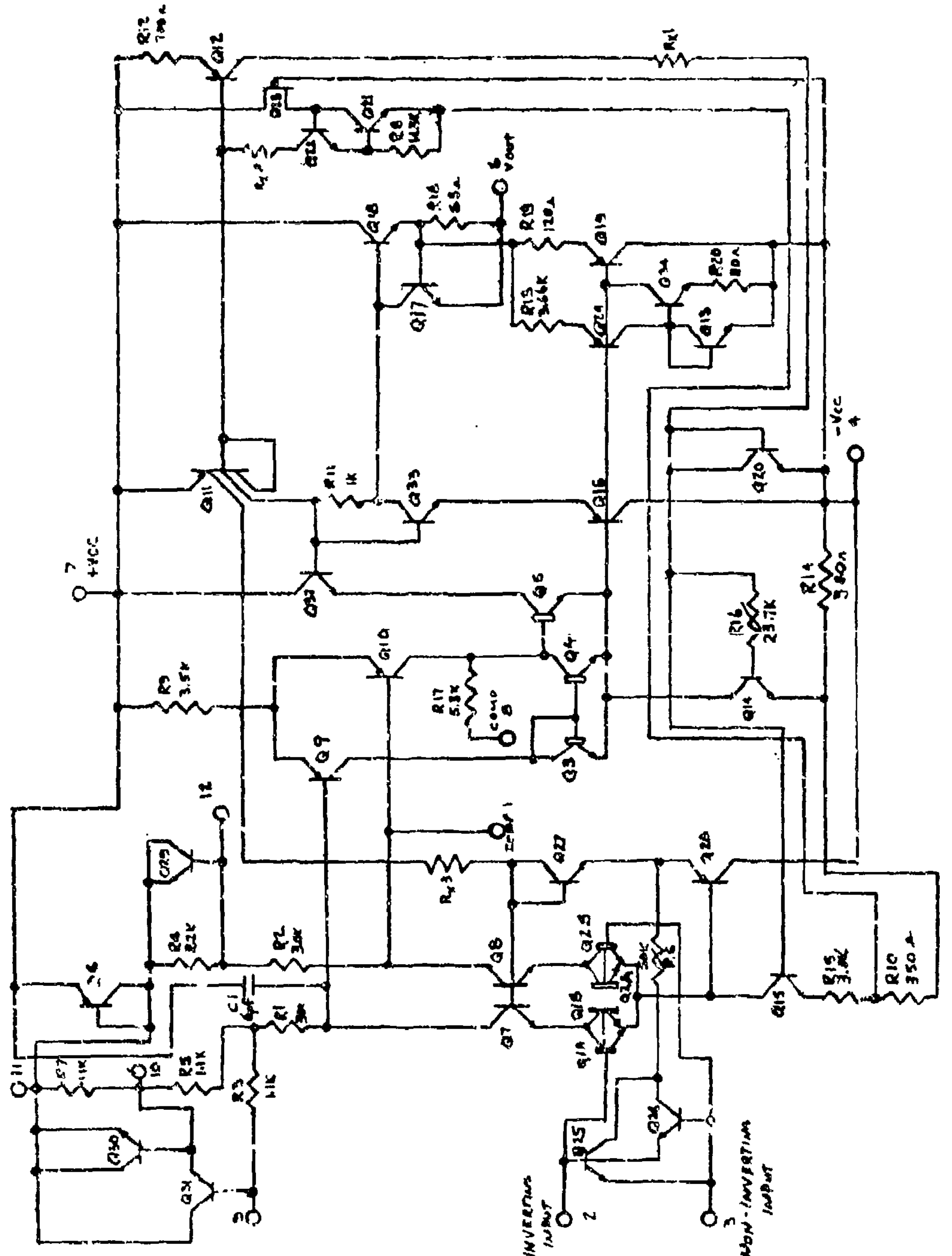
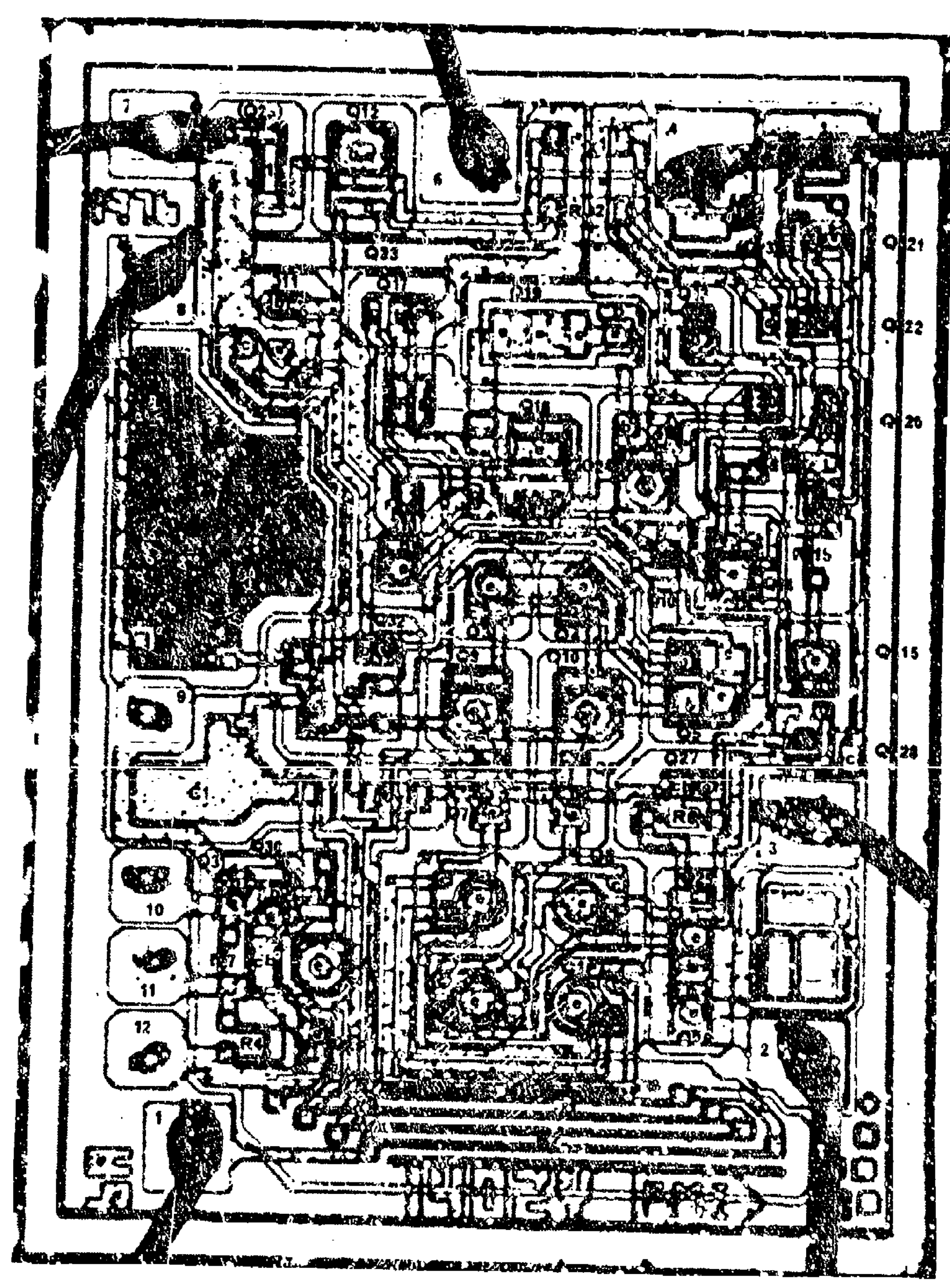


FIGURE A1-5 - SCHEMATIC DIAGRAM



134X S/N11

FIGURE A1-6 - DIE PHOTOGRAPH

C. COMPONENT DESCRIPTION

An examination of the die surface was conducted in order to determine the structure of each circuit element.

1. TRANSISTORS (Transistors listed together share a common N type collector or base tub.)

Vertical NPN	Vertical PNP	Lateral PNP	N Channel J FET
Q1 ⊛	Q16	Q6*	Q23
Q2 ⊛	Q19	Q9	
Q3* ⊛	Q28	Q10	
Q4 ⊛		Q11	
Q5 ⊛		Q12	
Q7		Q24	
Q8		Q28	
Q13*			
Q14, Q34			
Q15			
Q17			
Q18			
Q20*			
Q21			
Q22			
Q25, Q26			
Q27*			
Q29*, Q30*, Q31			
Q32			
Q33			

* Diode connected transistor.

⊛ Super beta transistor.

2. RESISTORS

P Type	Squeezed P Type	N+ Crossunders
R1 thru R5	R6	R_x1 thru R_x3
R7 thru R15	R16	
R17 thru R20		

3. CAPACITORS

MOS Thin Oxide Over N+

C1

The schematic supplied by the manufacturer and the die itself contained a number of circuit elements and bonding pads not connected in this device. These are used to trim offset voltage by selectively zapping the transistors Q29, Q30 or Q31. Shorting Q29 removes R4 from the circuit, shorting Q30 removes R7 and shorting Q31 removes R3 and R5 from the circuit. In the particular part being evaluated, transistor Q30 had been zapped (see Figure A1-7) removing R7 from the circuit.

An attempt was made to examine in detail the construction of the super-beta transistors Q1, Q2, Q3, Q4, and Q5. Several devices were angle sectioned and stained in an attempt to delineate the junctions. However all attempts failed to define the base, as shown in Figure A1-8. A discussion with the manufacturer revealed that the base is very near intrinsic and extremely difficult to show. They stated it could be done with limited success using diffraction in a scanning electron microscope. This is beyond the scope of this investigation and was not attempted.

F. QUALITY OF WORKMANSHIP

The quality of workmanship is considered acceptable per MIL-STD-883, Method 2010.3.

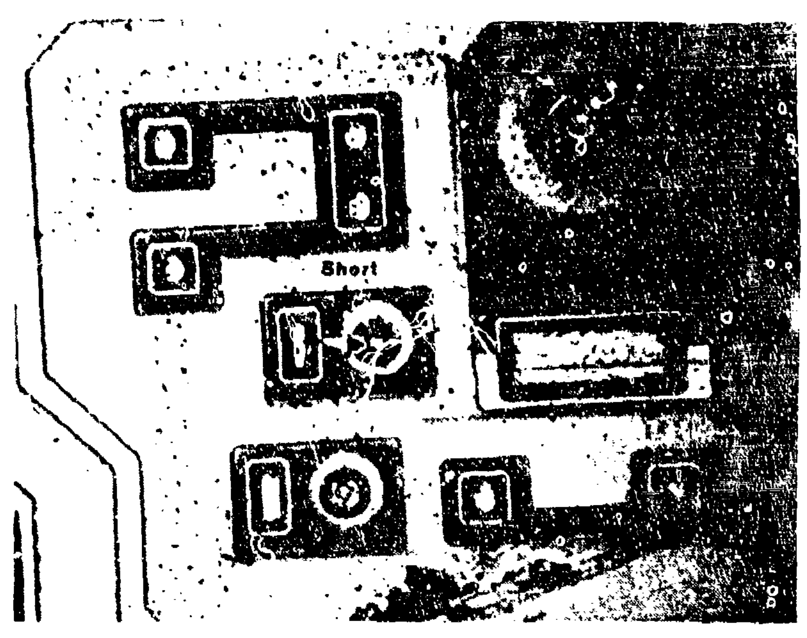


FIGURE A1-7 - TRANSISTOR Q31 WITH EMITTER BASE SHORT (METALIZATION REMOVED)

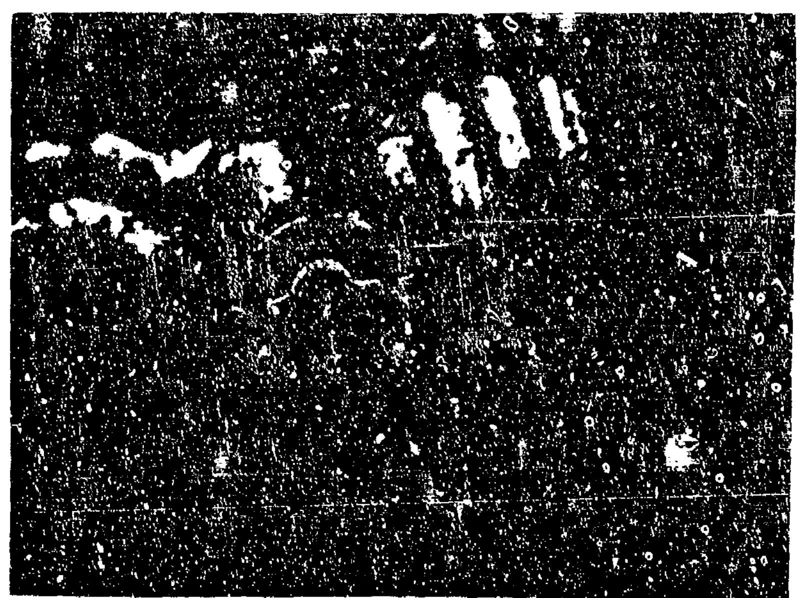


FIGURE A1-8 - CROSS SECTION OF A TYPICAL SUPER BETA TRANSISTOR

CONSTRUCTION ANALYSIS

M38510/10104BGC

MANUFACTURER B

OPERATIONAL AMPLIFIER

DATE CODE 7608

MICROCIRCUIT CONSTRUCTION INFORMATION

S/N: 45 DATE CODE: 7608 DATE: 5/9/77

PART NAME: Operational Amplifier

MANUFACTURER'S PART NO.: LM108AH/10104BGC MANUFACTURER: B

GENERIC PART NO.: LM108A PACKAGE TYPE: 8 Pin Can

MILITARY SPECIFICATION NO.: M38510/10104BGC

A. PACKAGE DETAILS (See Figure A2-1)

Lead Material: Kovar

Lead Finish - Internal: Gold Plate

- External: Gold Plate

- Feed Through: None

Header Material: Gold Plated Kovar

Cap Material: Nickel

Case Seal Method: Weld

Lead Seal Material/Method: Matched Glass

B. INTERCONNECTION DETAILS (See Figure A2-2)

Die Mounting Material: Gold Silicon Eutectic

Interconnect Wire Material: Aluminum

Interconnect Wire Diameter: 0.001 inch

Longest Interconnect Wire Length: 0.101 inch

Wire Bond Type(s) Post: Ultrasonic (See Figure A2-4)

Die: Ultrasonic (See Figure A2-3)

C. DIE DETAILS (See Figure A2-7)

Passivation Type: Silicon Dioxide

Glassivation Type: Phosphorous Glass

Basic Die Construction: Epitaxial Planar

Die Dimensions: 0.058 inch x 0.057 inch

Metalization Type: Aluminum

Metalization Thickness: 22,913Å

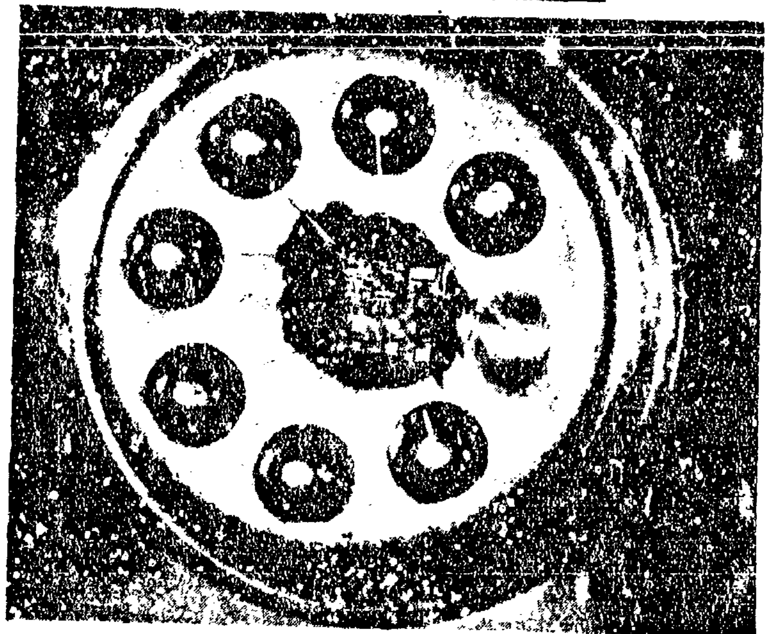
Scribe Method: Mechanical

Bond Pad Size: 0.0047 inch x 0.0047 inch

V_{CC} Stripe Cross-Sectional Area: $2.29 \times 10^{-4} cm \times 5.59 \times 10^{-3} cm = 1.28 \times 10^{-6} cm^2$

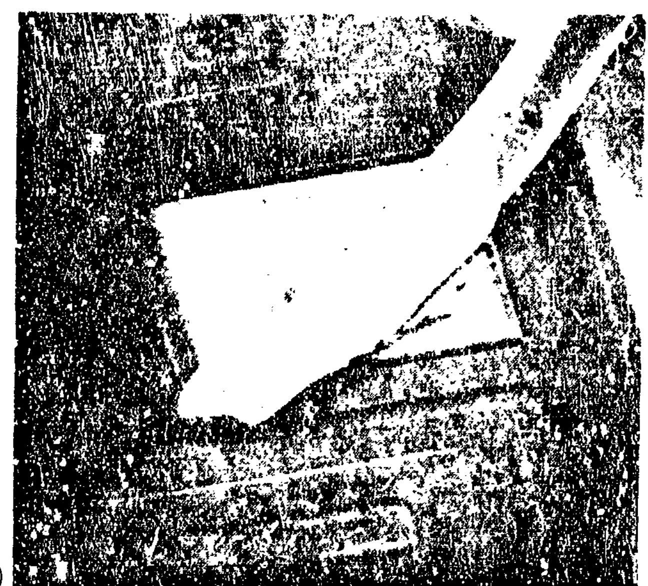
5X S/N45

FIGURE A2-1 - PACKAGE PHOTOGRAPH



10X S/N45

FIGURE A2-2 - INTERCONNECTION PHOTOGRAPH



430X
(SEM-1.2KV)

S/N45

FIGURE A2-3 - WIRE BOND AT DIE

380X
(SEM-1.2 KV)

S/N45

FIGURE A2-4 - WIRE BOND AT POST

D. ELECTRICAL SCHEMATIC

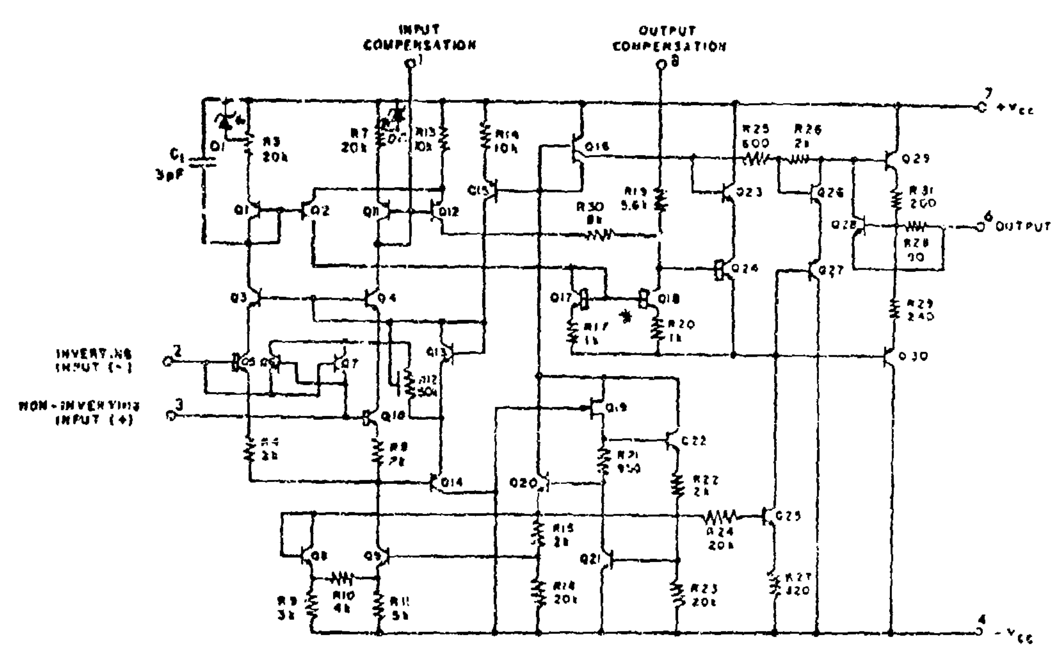
An electrical schematic of the device was prepared by modifying the schematic given in MIL-M-38510/10104 to conform to the actual circuitry on the die. The modification resulted from a microscopic examination of the die after removal of the glassivation and metalization. The corrected schematic is shown in Figure A2-5 and the die photomicrograph with components identified is Figure A2-6. The schematic modifications were as follows:

1. The MIL-M-38510/10104 schematic included a resistor between the bases of Q17 and Q18 which is on the die but shorted by metalization and, therefore, not used.

2. Two zener diodes D1 and D2 added across a small portion of R3 and R7.

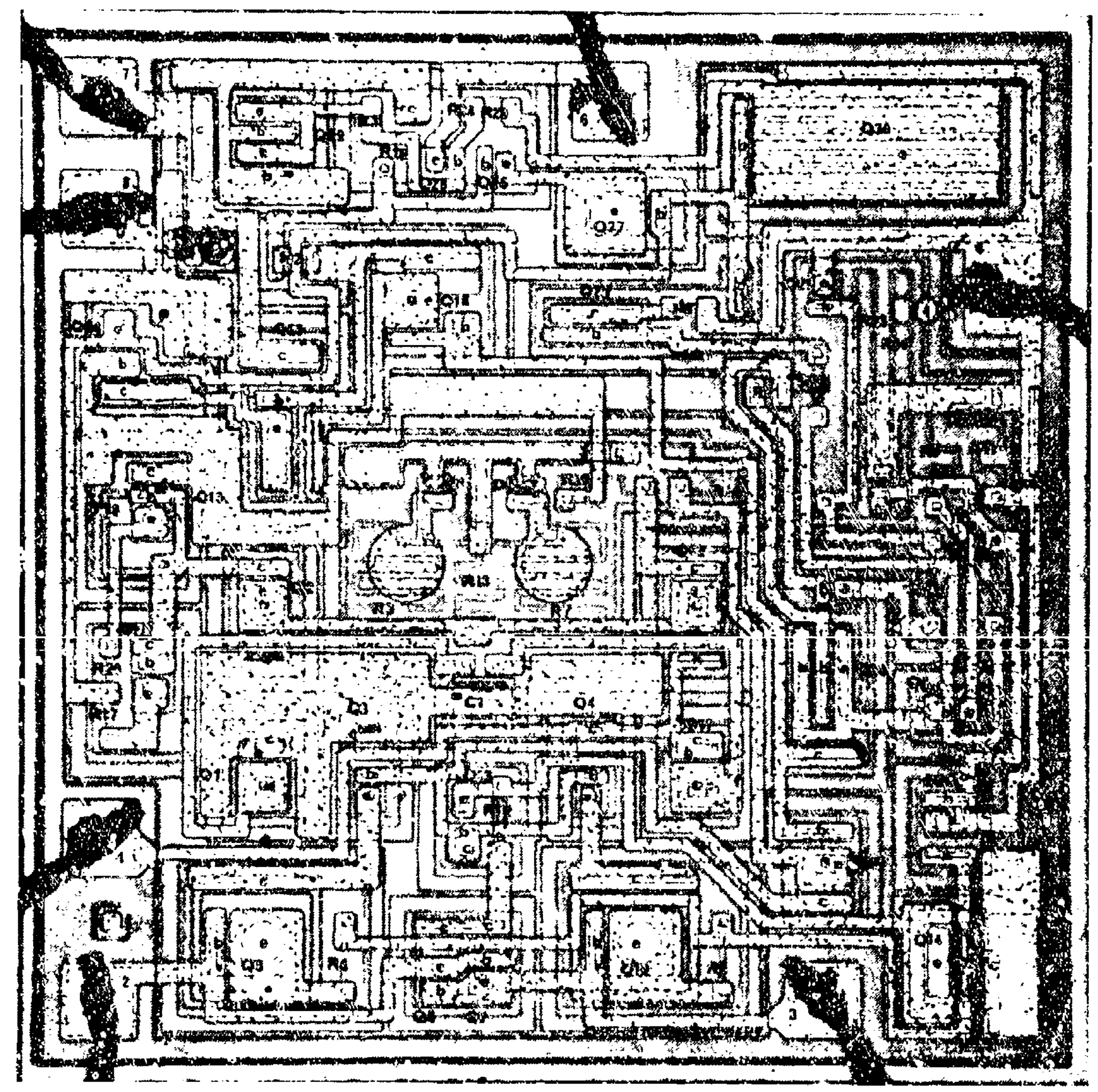
The modifications are indicated on the schematic by an asterisk (*).

Resistors R3 and R7 and diodes D1 and D2 require additional explanation. These resistors have a small resistance path in series with the zener diodes. If the zener diodes are zapped a small reduction in the total resistance of either R3 or R7 will result. A discussion with the manufacturer revealed that at one time these were used to adjust offset. The manufacturer stated that they no longer find it necessary to adjust the device. The large circular pads over R3 and R7 were used to make contact during the diode zapping operation.



* Modifications to MIL-M-38510/10104 schematic.

FIGURE A2-5 - SCHEMATIC DIAGRAM



110X S/N45

FIGURE A2-6 - DIE PHOTOGRAPH

E. COMPONENT DESCRIPTION

The structure of each component was determined from examination of the die surface.

1. TRANSISTORS (Transistors listed together share a common N type collector or base tub.)

Vertical NPN	Vertical PNP	Lateral PNP	N Channel FET
Q3	Q14	Q1*	Q19
Q4	Q27	Q2	
Q5 (*)	Q30	Q11 *	
Q6 - Q7		Q12	
Q8*		Q15	
Q9		Q16	
Q10 (*)			
Q13*			
Q17* (*)			
Q18 (*)			
Q20			
Q21			
Q22			
Q23			
Q24 (*)			
Q25			
Q26, Q28			
Q29			

* Diode connected transistors.

(*) Super beta transistors.

2. RESISTORS

P Type	Squeezed P Type	N Epitaxial
R3	R12	R21
R4	R24	
R7 thru R11		
R13 thru R17		
R19		
R20		
R22		
R23		
R25		
R26		

Reference designations R1, R2, R5, R6 and R18 are not used.

3. CAPACITORS

MOS plus PN junction

C1

Capacitor C1 is a metal oxide silicon capacitor with a parallel PN junction to increase capacitance. Figure A2-7 illustrates the construction of this capacitor.

F. QUALITY OF WORKMANSHIP

The quality of workmanship is considered acceptable per MIL-STD-883, Method 2010.3.

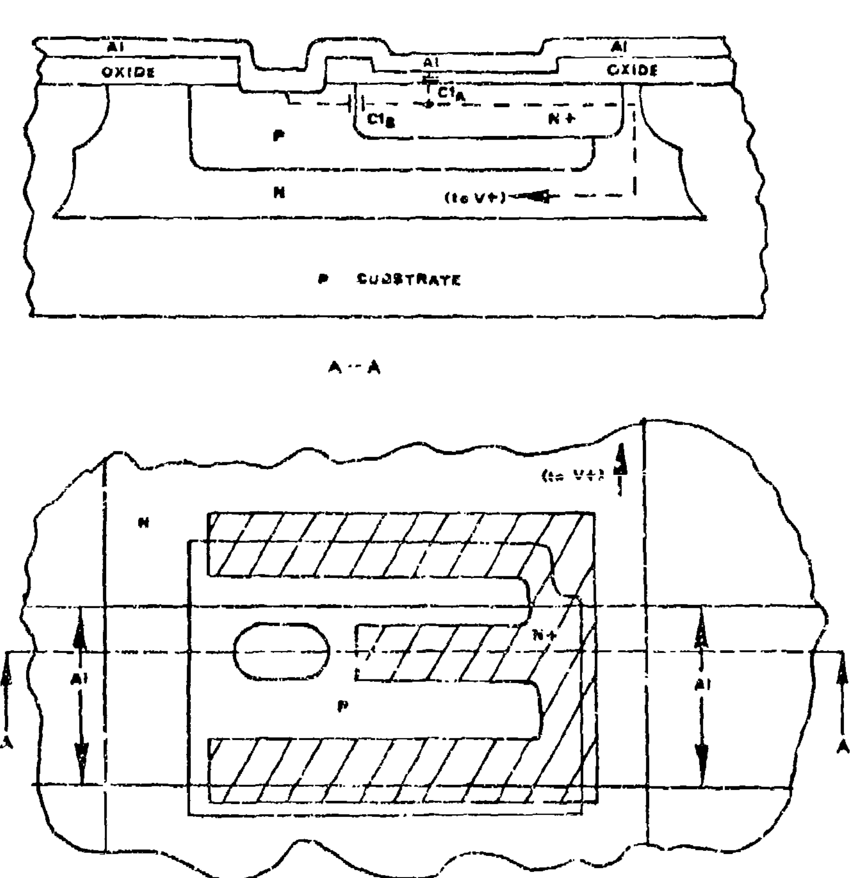


FIGURE A2-7 - CONSTRUCTION OF C1

CONSTRUCTION ANALYSIS

M38510/10107BGC

MANUFACTURER B

OPERATIONAL AMPLIFIER

DATE CODE 7632

MICROCIRCUIT CONSTRUCTION INFORMATION

S/N: 82 DATE CODE: 7632 DATE: 5/9/77

PART NAME: Operational Amplifier

MANUFACTURER'S PART NO.: LM118/10107BGC MANUFACTURER: B

GENERIC PART NO.: LM118 PACKAGE TYPE: 8 Pin Can

MILITARY SPECIFICATION NO.: M38510/10107BGC

A. PACKAGE DETAILS (See Figure A3-1)

Lead Material: Kovar

Lead Finish - Internal: Gold Plate

- External: Gold Plate

- Feed Through: None

Header Material: Gold Plated Kovar

Cap Material: Nickel

Case Seal Method: Weld

Lead Seal Material/Method: Matched Glass

B. INTERCONNECTION DETAILS (See Figure A3-2)

Die Mounting Material: Gold Silicon Eutectic

Interconnect Wire Material: Aluminum

Interconnect Wire Diameter: 0.001 inch

Longest Interconnect Wire Length: 0.077 inch

Wire Bond Type(s) Post: Ultrasonic (See Figure A3-4)

Die: Ultrasonic (See Figure A3-3)

C. DIE DETAILS (See Figure A3-6)

Passivation Type: Silicon Dioxide

Glassivation Type: Phosphorus Glass

Basic Die Construction: Planar Epitaxial

Die Dimensions: 0.075 x 0.050 inch

Metalization Type: Aluminum

Metalization Thickness: 10,160Å

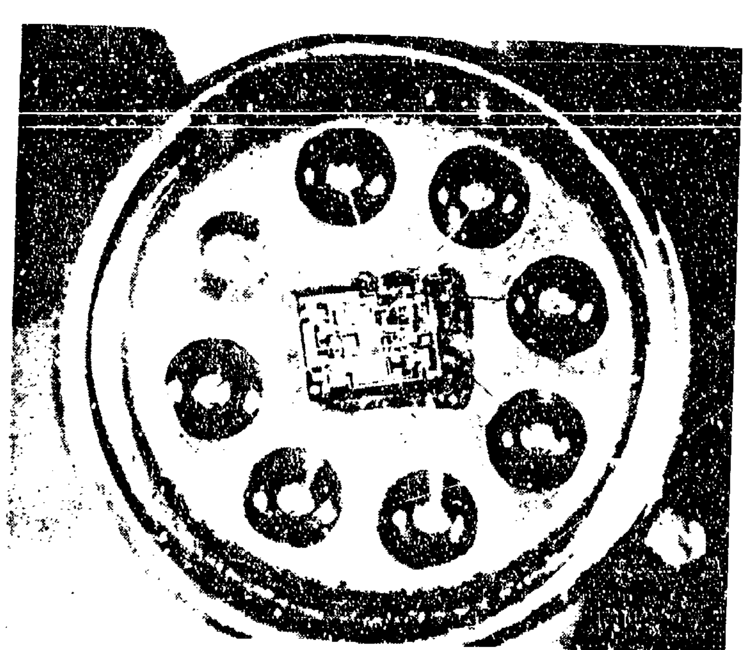
Scribe Method: Mechanical

Bond Pad Size: 0.005 x 0.005 inch

V_{CC} Stripe Cross Sectional Area: $1.02 \times 10^{-4} cm \times 2.67 \times 10^{-3} cm = 2.71 \times 10^{-7} cm^2$

5X S/N82

FIGURE A3-1 - PACKAGE PHOTOGRAPH



10X S/N82

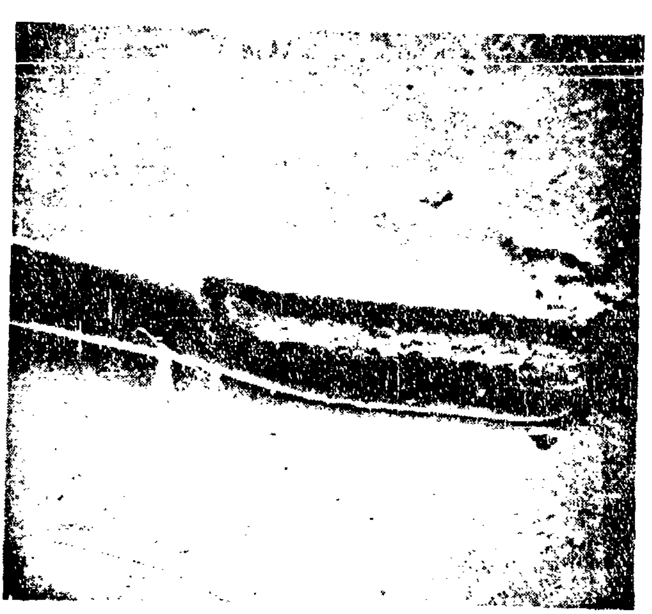
FIGURE A3-2 - INTERCONNECTION PHOTOGRAPH

360X
(SEM-1.2KV)

S/N82

FIGURE A3-3 - WIRE BOND AT DIE

440X
(SEM-1.2KV)



S/N82

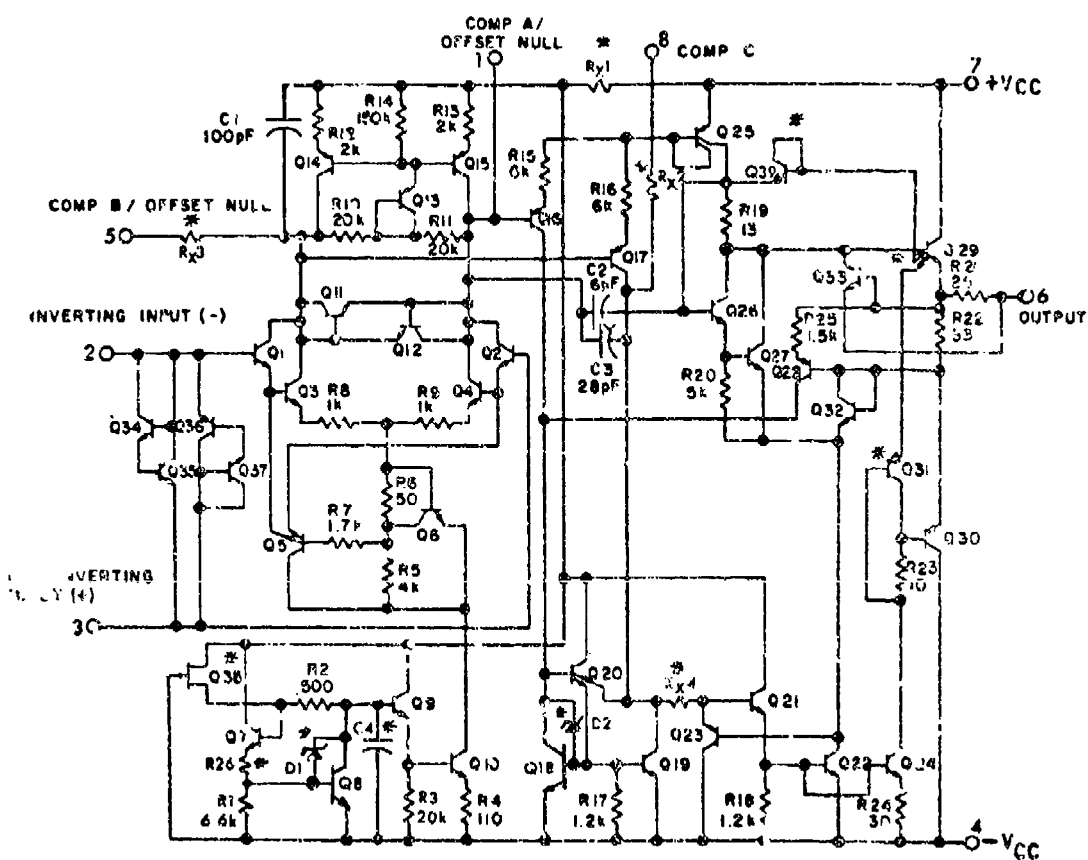
FIGURE A3-4 - WIRE BOND AT POST

D. ELECTRICAL SCHEMATIC

An electrical schematic of the device was prepared by modifying the schematic given in MIL-M-38510/10107 to conform to actual circuitry on the die. The modification resulted from a microscopic examination of the die with glassivation and metalization removed and from a metallurgical cross section. The corrected schematic is shown in Figure A3-5 and the components are identified in the die photograph shown in Figure A3-6. The schematic modifications consist of the following:

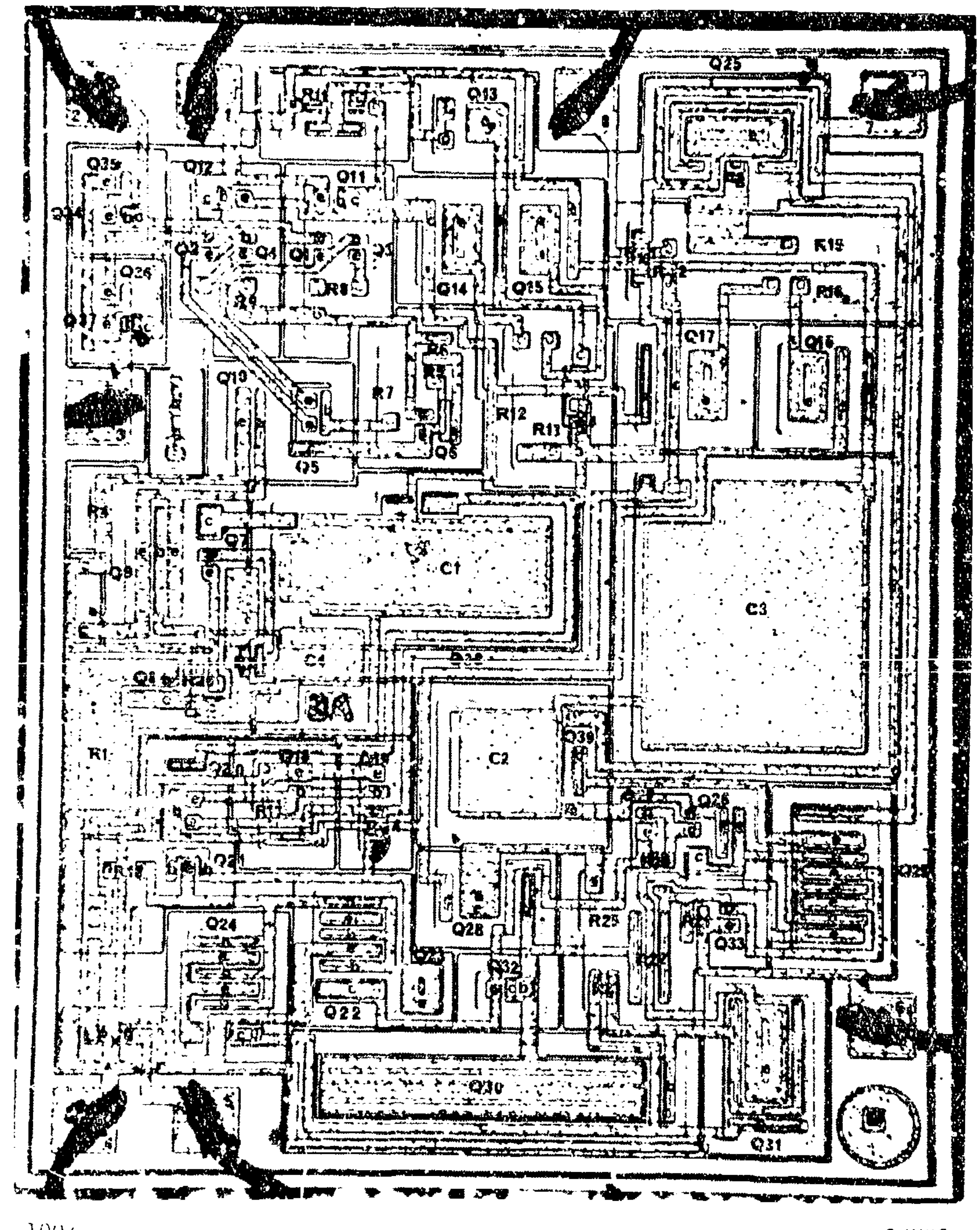
1) Added four diffused cross unders (R_X1 - R_X4)
2) Added resistor (R26)
3) Added a diode connected transistor (Q39)
4) Added collector-base clamp diodes to Q8 and Q18
5) Added a small value metal over substrate capacitor (C4)
6) Changed Q31 from NPN to PNP
7) Changed JFET reference designation to Q38 (to correct duplication of numbers)

The changes are indicated on the schematic with an asterisk (*).



* Additions or corrections to the MIL-M-38510/10107 schematic.

* FIGURE A3-5 - COMPLETE ELECTRICAL SCHEMATIC



100X S/N82

FIGURE A3-6 - DIE PHOTOGRAPH AND COMPONENT IDENTIFICATION

E. COMPONENT DESCRIPTION

From examination of the die surface and the cross sections, the structure of each component was determined.

1. TRANSISTORS (Transistors listed together share a common N-type collector or base tub.)

Vertical NPN	Vertical PNP	Lateral PNP	N Channel JFET
Q1, Q3, Q11*	Q23	Q13*	Q38
Q2, Q4, Q12*	Q30	Q14, Q15	
Q5, Q10		Q16	
Q6		Q17	
Q7, Q9		Q25	
Q8		Q28	
Q18		Q31	
Q19			
Q20, Q21			
Q22			
Q24			
Q26, Q27, Q33			
Q29			
Q32*			
Q34*, Q35			
Q36, Q37*			
Q39*			

* Diode connected transistor.

2. RESISTORS

P Type	Squeezed P Type	N epitaxial	N^+ Crossunders
R1	R5	R2, 3	R_x1, 2, 3, 4
R4	R10, 11		
R6 thru 9	R14		
R12, 13	R20		
R15 thru 19			
R21 thru 26			

3. CAPACITORS

MOS (thin oxide over N^+)	MOS (thick oxide over substrate)	MOS + PN Junctions
C2, 3	C4	C1

The structure of the four capacitors and transistors Q38 and Q39 require further discussion. Figure A3-7 is an etched metallurgical cross section of C1, C2 and Q38. The N channel junction field effect transistor Q38 is a squeezed N epitaxial resitor. The channel region is composed of N epitaxial silicon. The gate is composed of a P type base diffusion (upper channel boundary), a deep P type isolation diffusion (sidewall boundary) and the P type substrate (lower boundary). The drain contact of the JFET is the N^+ diffusion of the R14 squeezed P type resistor and the source contact is the N^+ upper contact to R2.

Capacitors C2 and C3 are normal MOS N^+ capacitors except that the N^+ diffusion is preceeded by a P type base diffusion. In C2, the P type diffusion is shorted to the N type tank via an N^+ diffusion and the ohmic contact as shown in Figure A3-8(a). This contact is connected to an emitter of Q29 which results in a diode connected transistor Q39 being added to the schematic between Q29 and the N^+ side of C2. The complete equivalent circuit for C2 is shown in Figure A3-8(b). In C3, all three diffusions, the N^+, the P type and the N tank are shorted together and, therefore, no additional circuit element exists.

C1 contains a P-N junction capacitor in parallel with a MOS capacitor to increase its capacitance as shown in Figure A3-9(a). The P-N capacitor is part of the MOS capacitor and uses a deep P^+ isolation diffusion. The equivalent circuit of this capacitor is shown in Figure A3-9(b).

C4 is formed by expanding the metallization connected to the Q9 base/R2 contacts which adds additional capacitance between these points and the underlying substrate (V-).

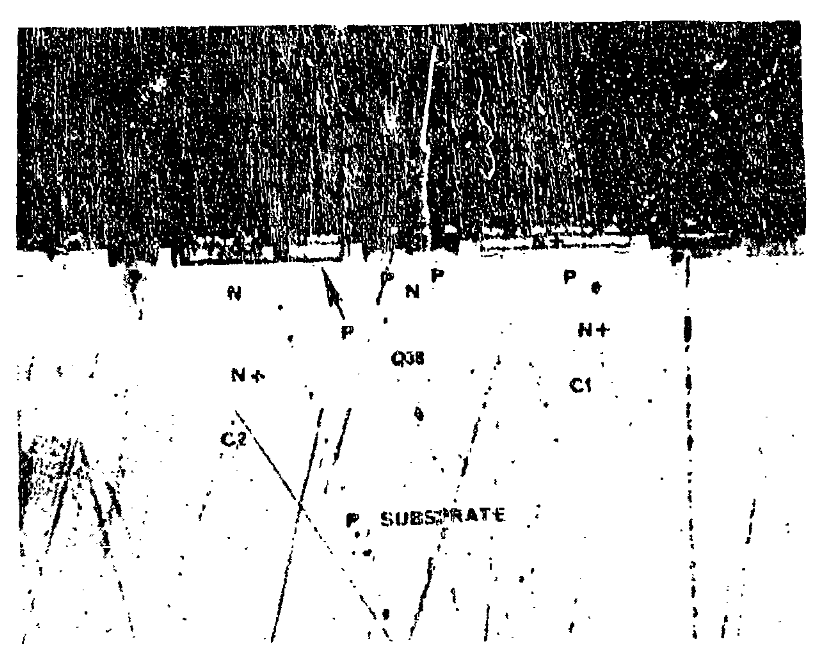
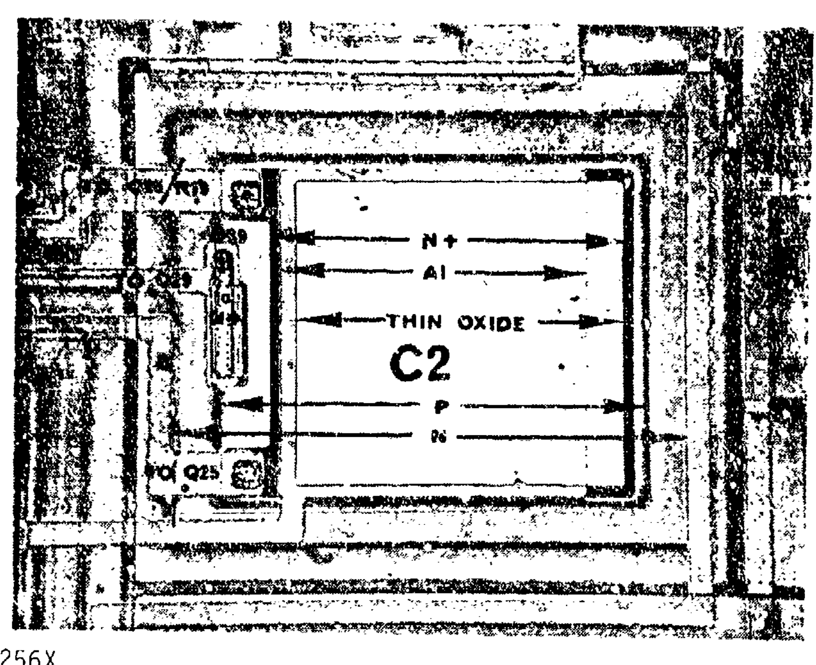


FIGURE A3-7 - METALLURGICAL CROSS SECTION (ETCHED) OF C2, Q38 AND C1

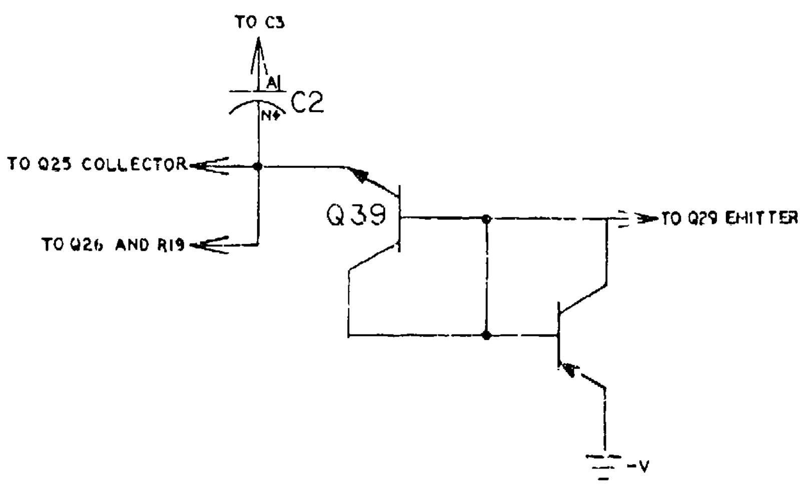
F. QUALITY OF WORKMANSHIP

The quality of workmanship is considered acceptable per MIL-STD-883, Method 2010.3.



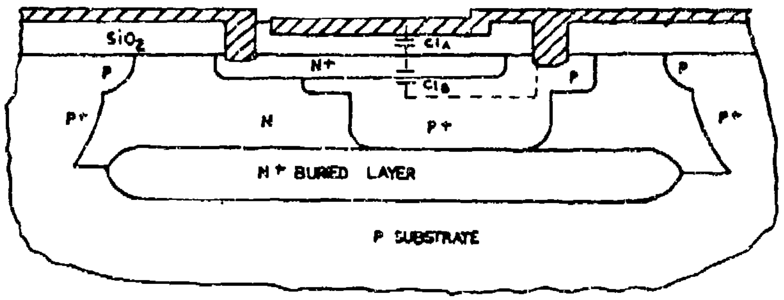
256X

a) PHOTO OF C2 AFTER REMOVING THE METALLIZATION

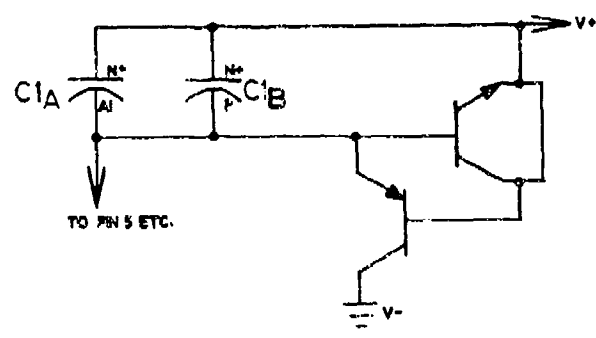


b) EQUIVALENT CIRCUIT OF C2

FIGURE A3-8 - PHOTOMICROGRAPH AND EQUIVALENT CIRCUIT OF C2



a) CROSS-SECTIONAL SKETCH OF C1



b) EQUIVALENT CIRCUIT OF C1

FIGURE A3-9 - DIFFUSION PROFILE AND EQUIVALENT CIRCUIT OF C1

CONSTRUCTION ANALYSIS

M38510/10107BGC

MANUFACTURER C

OPERATIONAL AMPLIFIER

DATE CODE 7651Q

MICROCIRCUIT CONSTRUCTION INFORMATION

S/N: 12 DATE CODE: 7651Q DATE: 5/9/77

PART NAME: Operational Amplifier

MANUFACTURER'S PART NO.: M38510/10107BG MANUFACTURER: C

GENERIC PART NO.: LM118 PACKAGE TYPE: 8 Pin Can

MILITARY SPECIFICATION NO.: M38510/10107BGC

A. PACKAGE DETAILS (See Figure A4-1)

Lead Material: Kovar

Lead Finish - Internal: Gold Plate

- External: Gold Plate
- Feed Through: None

Header Material: Gold Plated Kovar

Cap Material: Nickel

Case Seal Method: Weld

Lead Seal Material/Method: Matched Glass

B. INTERCONNECTION DETAILS (See Figure A4-2)

Die Mounting Material: Gold Silicon Eutectic

Interconnect Wire Material: Aluminum

Interconnect Wire Diameter: 0.0011 inch

Longest Interconnect Wire Length: 0.128 inch

Wire Bond Type(s) Post: Ultrasonic (See Figure A4-4)

Die: Ultrasonic (See Figure A4-3)

C. DIE DETAILS (See Figure A4-6)

Passivation Type: Silicon Dioxide

Glassivation Type: Phosphorus Glass

Basic Die Construction: Planar Epitaxial

Die Dimensions: 0.084 inch x 0.077 inch

Metalization Type: Aluminum

Metalization Thickness: 49,988 Å

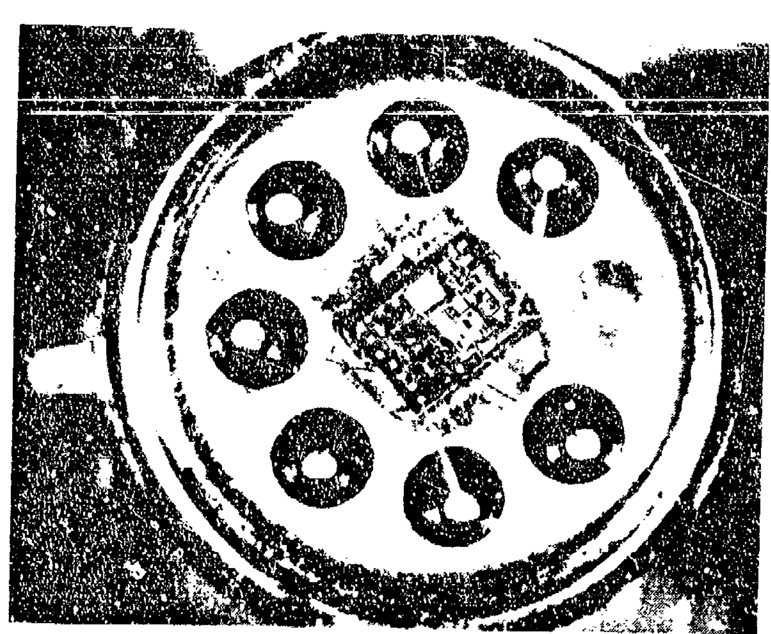
Scribe Method: Mechanical

Bond Pad Size: 0.007 inch x 0.007 inch

V_{CC} Stripe Cross-Sectional Area: 4.50×10^{-4} cm $\times$ 1.98×10^{-3} cm = 9.90×10^{-7} cm^2

5X S/N11

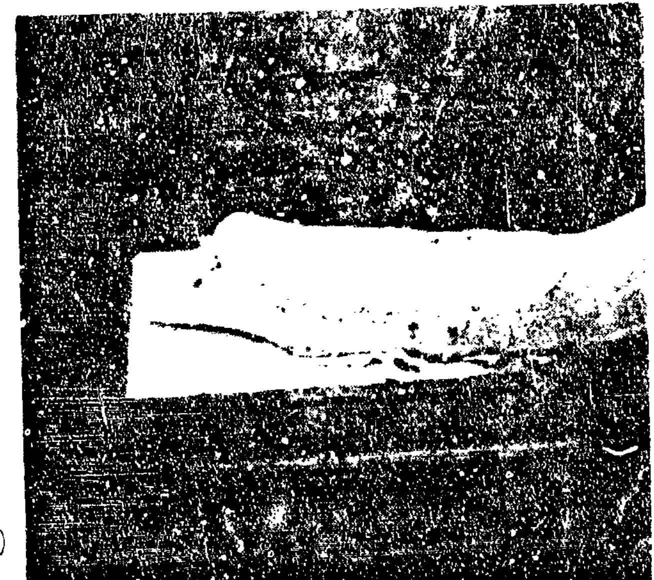
FIGURE A4-1 - PACKAGE PHOTOGRAPH



10X S/N12

FIGURE A4-2 - INTERCONNECTION PHOTOGRAPH

530X
(SEM-1.2KV)



S/N12

FIGURE A4-3- WIRE BOND AT DIE

440X
(SEM-1.2KV)

S/N12

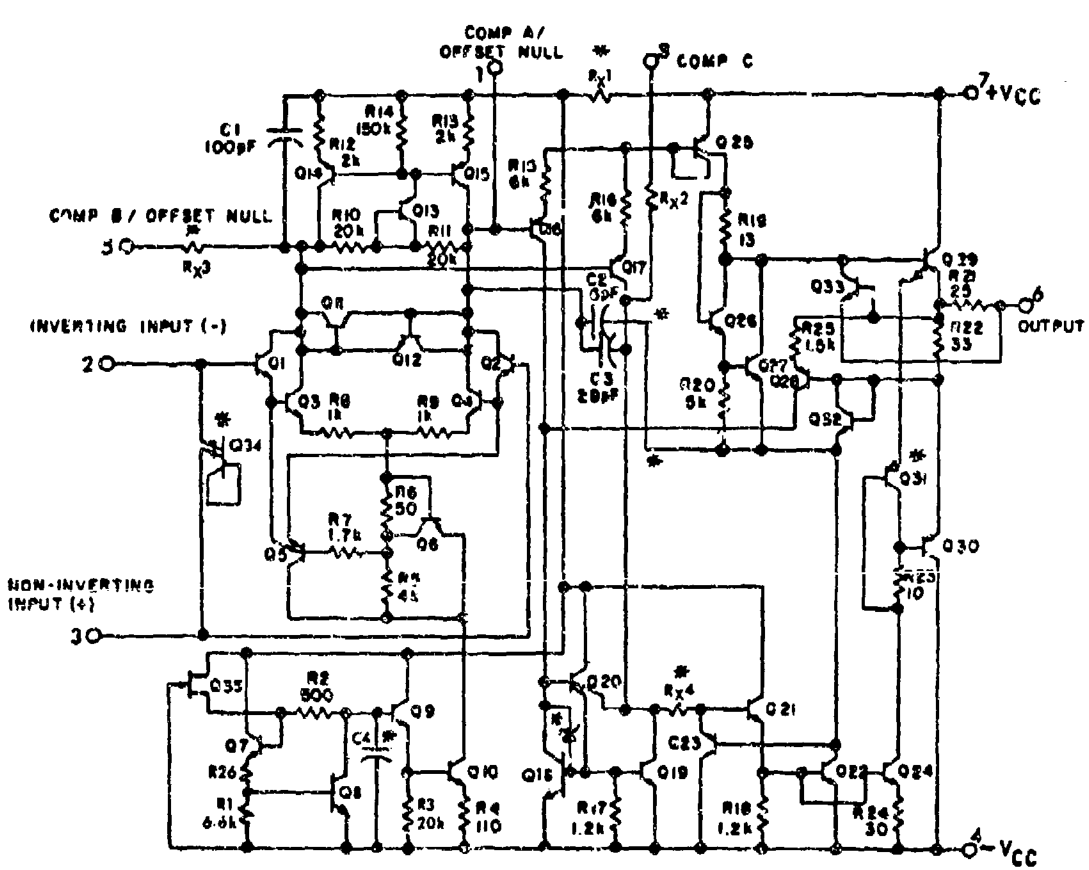
FIGURE A4-4- WIRE BOND AT POST

D. ELECTRICAL SCHEMATIC

An electrical schematic of the device was prepared by modifying the schematic given in MIL-M-38510/10107 to conform to the actual circuitry on the die. The modification resulted from a microscopic examination of the die after glassivation removal and was aided by the previous study of the Manufacturer B device. The corrected schematic is shown in Figure A4-5 and the components are identified on the die photograph shown in Figure A4-6. The schematic modifications consist of the following.

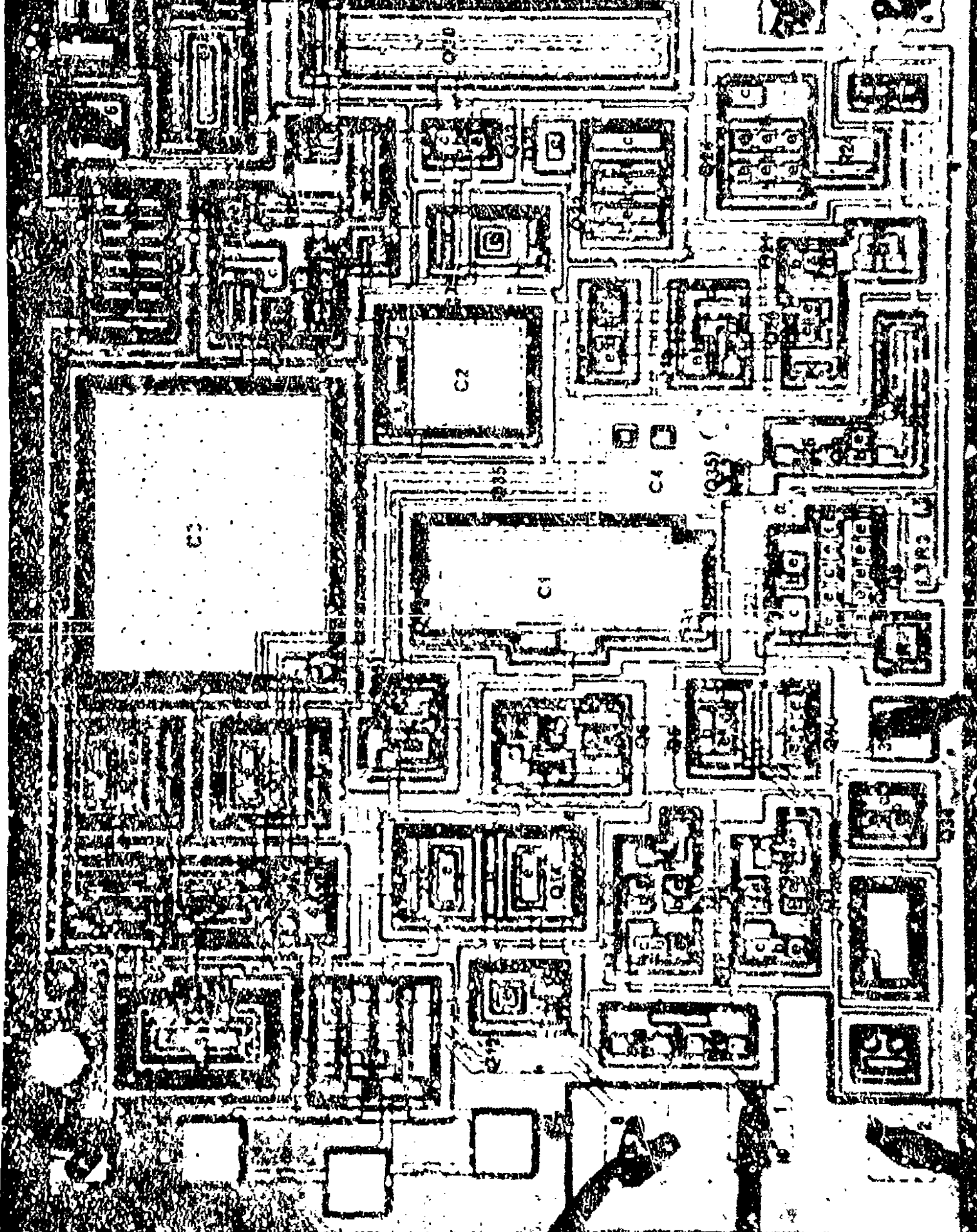
a) Added four diffused crossovers (R_x1, R_x2, R_x3, R_x4)
b) Added resistor (R26)
c) Added a small value metal over substrate capacitor (C4)
d) Changed Q31 from NPN to PNP
e) Changed JFET reference designation to Q35 (duplication)
f) Added collector-base clamp diode to Q18
g) Changed input protection from 4 transistors to one dual emitter transistor (Q34)
h) Removed connection between C2 and Q26 base, R19
i) Added connection between C2 and R20, Q27 emitter, Q32 emitter, Q22 collector, Q23 base

Changes are indicated in the schematic with an asterisk (*).



* Modifications to MIL-M-38510/10107 schematic.

FIGURE A4-5 - SCHEMATIC DIAGRAM



S/N82

32X

FIGURE A4-6 - DIE PHOTOGRAPH

E. COMPONENT DESCRIPTION

From examination of the die surface and the similarity between this device and the Manufacturer B version, the structure of each component was determined.

1. TRANSISTORS (Transistors listed together share a common N-type collector or base tub.)

Vertical NPN	Vertical PNP	Lateral PNP	N Channel JFET
Q1, Q3, Q11*	Q23	Q13*	Q35
Q2, Q4, Q12*	Q30	Q14, Q15	
Q5, Q10		Q16	
Q6		Q17	
Q7, Q9		Q25	
Q8		Q28	
Q18		Q31	
Q19			
Q20, Q21			
Q22			
Q24			
Q26, Q27, Q33			
Q29			
Q32*			
Q34*			

* Diode connected transistor.

2. RESISTORS

P Type	Squeezed P Type	N Epitaxial	N+ Crossunders
R1	R5	R2	R_x1
R4	R10	R3	R_x2
R6 thru 9	R11		R_x3
R12	R14		R_x4
R13	R20		
R15 thru 19			
R21 thru 26			

3. CAPACITORS

MOS (thick oxide over N+)	MOS (thick oxide over substrate)	MOS + PN Junction
C2	C4	C1
C3		

The structure of the four capacitors and transistor Q35 require further discussion. The N-channel junction field effect transistor Q35 is a squeezed N-channel epitaxial resistor. The channel region is composed of N-epitaxial silicon. The gate is composed of a P-type base diffusion (upper channel boundary), a deep P-type isolation diffusion (sidewall boundary) and the P-type substrate (lower channel boundary). The drain contact of the JFET is the N+ diffusion of the R14 squeezed P-type resistor and the source contact is the N+ upper contact of R2. Refer to Figure A3-7 in Appendix A3 for a metallurgical cross section of the JFET since Q35 is constructed identically to Q38 in the Manufacturer B device.

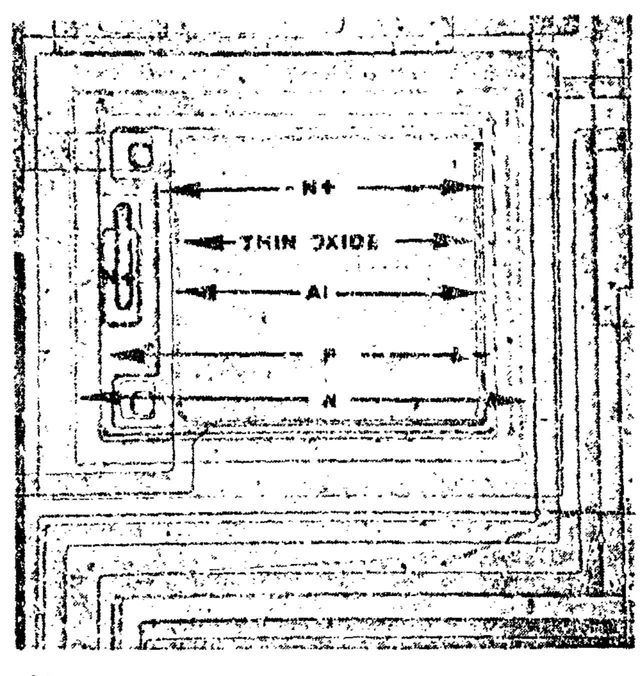
Capacitors C2 and C3 are also of the same construction as the same capacitors in the Manufacturer B device (Appendix A3). They are normal MOS N+ capacitors except the N+ diffusion is preceeded by a P-type base diffusion. In C2 the P-type diffusion is shorted to the N-type tank via an N+ diffusion and the ohmic contact as shown in Figure A4-7(a). This contact is left unconnected in this device. The equivalent schematic of C2 is as shown in Figure A4-7(b). In C3 the three diffusions, the N+, the P type and the N tank are shorted together.

C1 contains a P-N capacitor in parallel with a MOS capacitor to increase its capacitance. As shown in Figure A4-8(a), the P-N capacitor is part of the MOS capacitor and uses a deep P+ isolation diffusion. The equivalent circuit of this capacitor is shown in Figure A4-8(b).

C4 is formed by expanding the metalization connected to the Q9 base/R2 contacts which add capacitance between these points and the underlying substrate (V-).

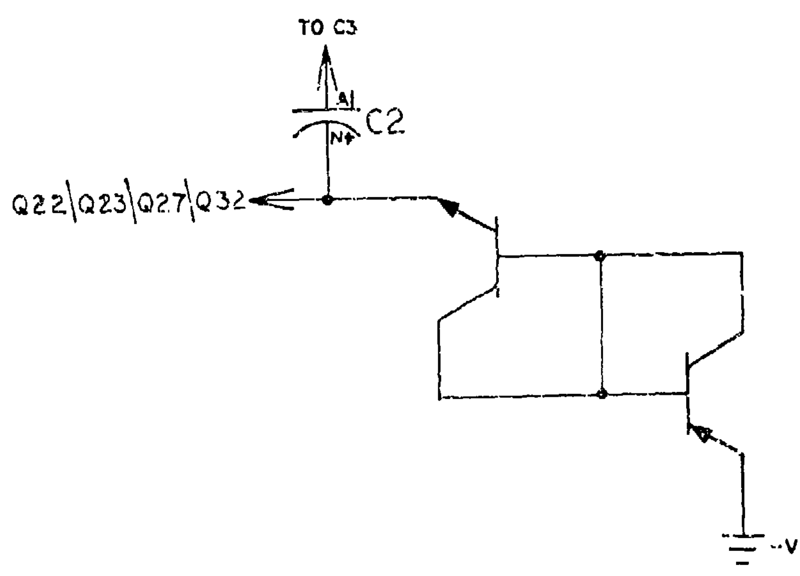
F. QUALITY OF WORKMANSHIP

The quality of workmanship is considered acceptable per MIL-STD-883, Method 2010.3.



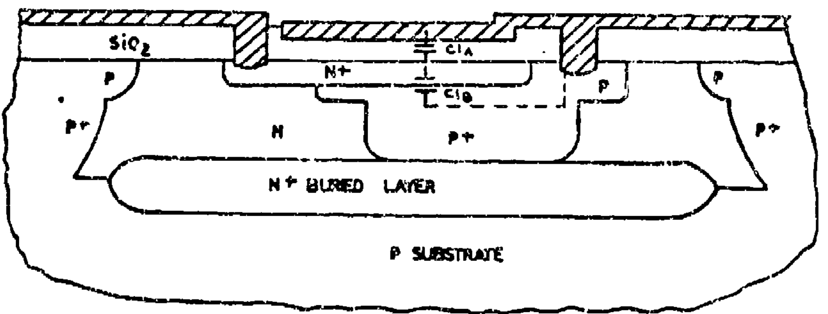
256X

a) PHOTOMICROGRAPH OF C2 AFTER METALIZATION REMOVAL

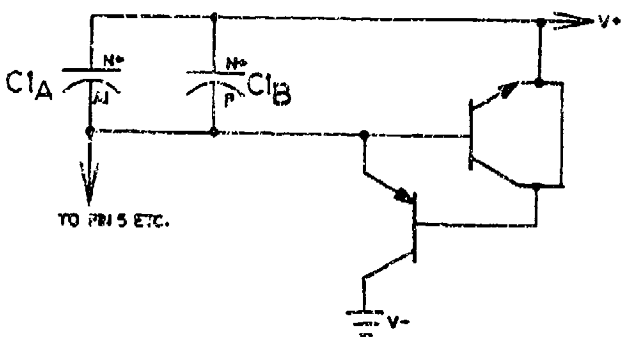


b) EQUIVALENT CIRCUIT OF C2

FIGURE A4-7 - PHOTOMICROGRAPH AND EQUIVALENT CIRCUIT OF CAPACITOR C2



a) CROSS-SECTIONAL SKETCH OF C1



b) EQUIVALENT CIRCUIT OF C1

FIGURE A4-8 - DIFFUSION PROFILE AND EQUIPMENT CIRCUIT OF C1

CONSTRUCTION ANALYSIS

M38510/10201BIC

MANUFACTURER D

PRECISION VOLTAGE REGULATOR

DATE CODE 7630

MICROCIRCUIT CONSTRUCTION INFORMATION

S/N: 51 DATE CODE: 7630 DATE: 7/8/77

PART NAME: Precision Voltage Regulator

MANUFACTURER'S PART NO.: M38510/10201BIC MANUFACTURER: D

GENERIC PART NO.: 723 PACKAGE TYPE: 10 Pin Can

MILITARY SPECIFICATION NO.: M38510/10201BIC

A. PACKAGE DETAILS (See Figure A5-1)

Lead Material: Kovar

Lead Finish - Internal: Gold Plate

- External: Gold Plate
- Feed Through: None

Header Material: Gold Plated Kovar

Cap Material: Nickel

Case Seal Method: Weld

Lead Seal Material/Method: Matched Glass

B. INTERCONNECTION DETAILS (See Figure A5-2)

Die Mounting Material: Gold-Silicon Eutectic

Interconnect Wire Material: Aluminum

Interconnect Wire Diameter: 0.001 inch

Longest Interconnect Wire Length: 0.105 inch

Wire Bond Type(s) Post: Ultrasonic (See Figure A5-4)

Die: Ultrasonic (See Figure A5-3)

C. DIE DETAILS (See Figure A5-6)

Passivation Type: Silicon Dioxide

Glassivation Type: Vapox

Basic Die Construction: Planar Epitaxial

Die Dimensions: 0.057 inch x 0.048 inch

Metalization Type: Aluminum

Metalization Thickness: 22,811Å

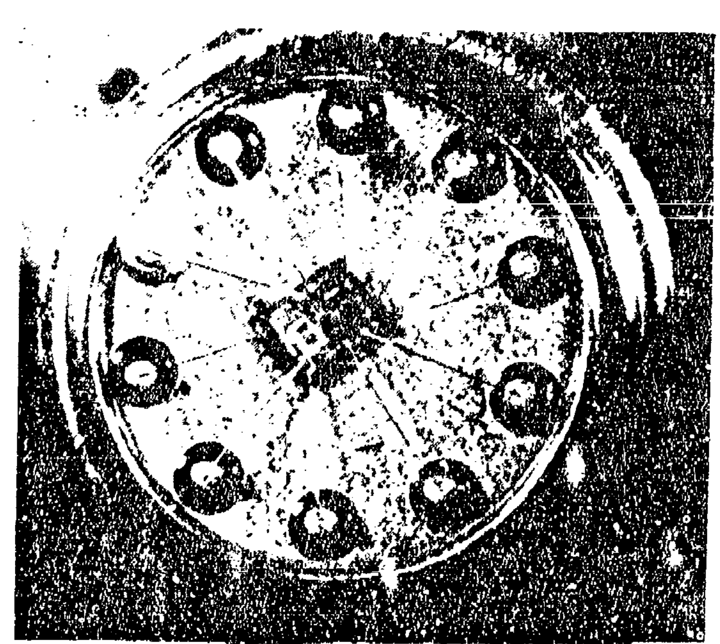
Scribe Method: Mechanical

Bond Pad Size: 0.0044 inch x 0.0044 inch

V_{CC} Stripe Cross-Sectional Area: 2.28×10^{-4}cm x 7.34×15^{-3}cm = 1.67×10^{-6} cm^2

3X S/N51

FIGURE A5-1 - PACKAGE PHOTOGRAPH



10X S/N51

FIGURE A5-2 - INTERCONNECTION PHOTOGRAPH

700X
(SEM-1.2KV)

S/N51

FIGURE A5-3 - WIRE BOND AT DIE

380X
(SEM-1.2KV)

S/N52

FIGURE A5-4 - WIRE BOND AT POST

D. ELECTRICAL SCHEMATIC

An electrical schematic of the device was obtained from MIL-M-38510/`0201 (Circuit C) and compared with the actual die configuration. The die layout agreed with the military specification schematic except for one area. Transistor Q14 shown in the schematic as a single emitter transistor actually has two emitters tied together and transistor Q18 is not connected in this device. The corrected schematic diagram is included as Figure A5-5 and a die photomicrograph with circuit elements identified is included as Figure A5-6.

E. COMPONENT DESCRIPTION

From examination of the die surface, the structure of each component was determined.

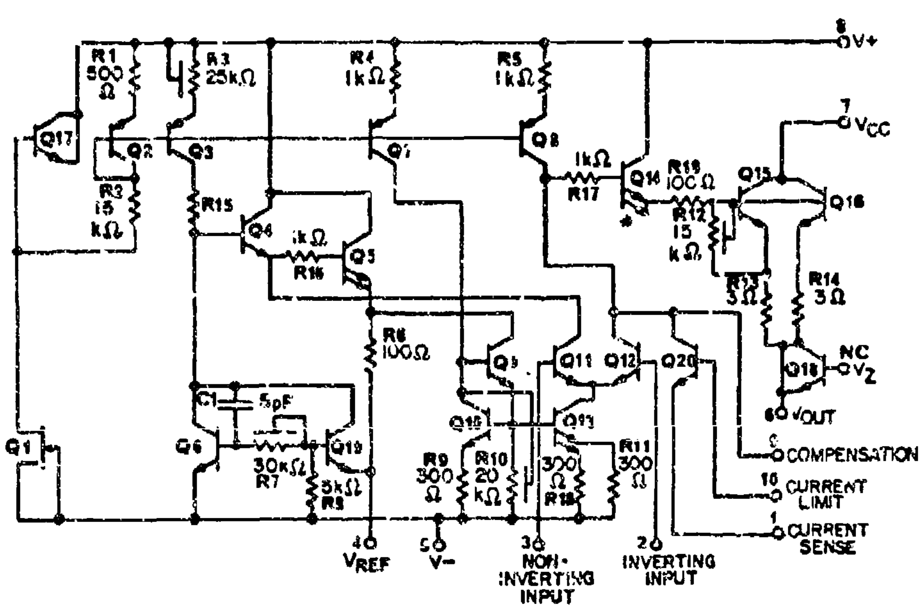
1. TRANSISTORS (Transistors listed together share a common N-type collector or base tub.)

Vertical NPN	Lateral PNP	N Channel JET
Q4, Q5, Q14, Q17*	Q2*, Q3, Q7 Q8	Q1
Q6, Q19		
Q9		
Q10		
Q11		
Q12, Q20		
Q13		
Q15, Q16		
Q18		

* Diode connected transistors.

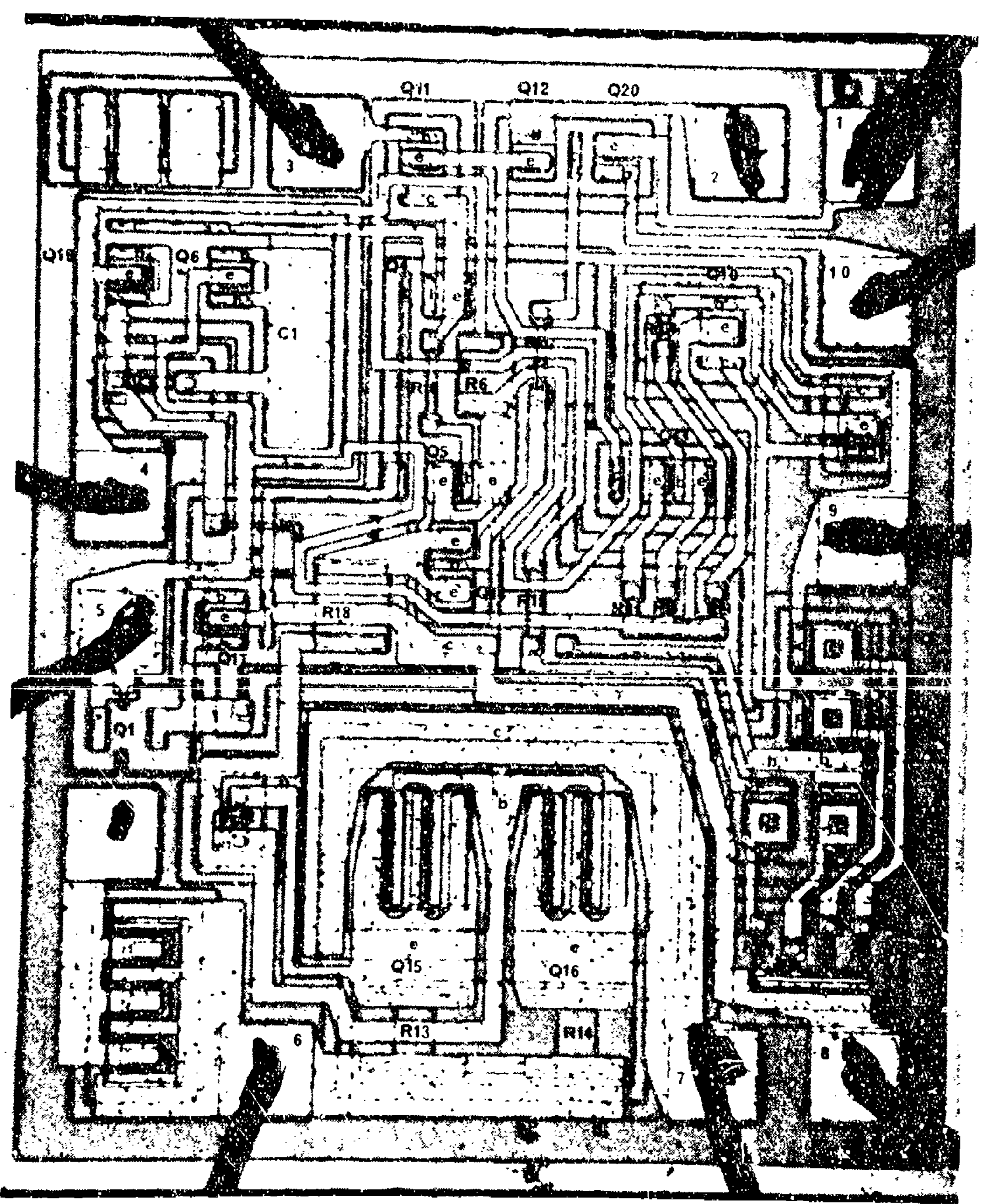
2. RESISTORS

P Type	Squeezed P Type	N+
R1, R2	R3	R13
R4 thru R6	R7	R14
R8, R9	R10	
R11	R12	
R15 thru R18		



* Modifications to MIL-M-38510/10201 schematic.

FIGURE A5-5 - ELECTRICAL SCHEMATIC DIAGRAM



127X

S/N51

FIGURE A5-6 - DIE PHOTOGRAPH

3. CAPACITORS

MOS (thin oxide over N+)

C1

F. QUALITY OF WORKMANSHIP

The quality of workmanship is considered acceptable per MIL-STD-883, Method 2010.3.

CONSTRUCTION ANALYSIS

M38510/10201BIC

MANUFACTURER C

PRECISION VOLTAGE REGULATOR

DATE CODE 7649P

MICROCIRCUIT CONSTRUCTION INFORMATION

S/N: 51 DATE CODE: 7649P DATE: 2/8/77

PART NAME: Precision Voltage Regulator

MANUFACTURER'S PART NO.: 723HMB MANUFACTURER: C

GENERIC PART NO.: 7?3 PACKAGE TYPE: 10 Pin Can

MILITARY SPECIFICATION NO.: M38510/10201BIC

A. PACKAGE DETAILS (See Figure A6-1)

Lead Material: Kovar

Lead Finish - Internal: Gold Plate

- External: Gold Plate

- Feed Through: None

Header Material: Gold Plated Kovar

Cap Material: Nickel

Case Seal Method: Weld

Lead Seal Material/Method: Matched Glass

B. INTERCONNECTION DETAILS (See Figure A6-2)

Die Mounting Material: Gold Silicon Eutectic

Interconnect Wire Material: Aluminum

Interconnect Wire Diameter: 0.0012 inch

Longest Interconnect Wire Length: 0.162 inch

Wire Bond Type(s) Post: Ultrasonic (See Figure A6-4)

Die: Ultrasonic (See Figure A6-3)

C. DIE DETAILS (See Figure A6-6)

Passivation Type: Silicon Dioxide

Glassivation Type: Silox

Basic Die Construction: Planar

Die Dimensions: 0.037 inch x 0.049 inch

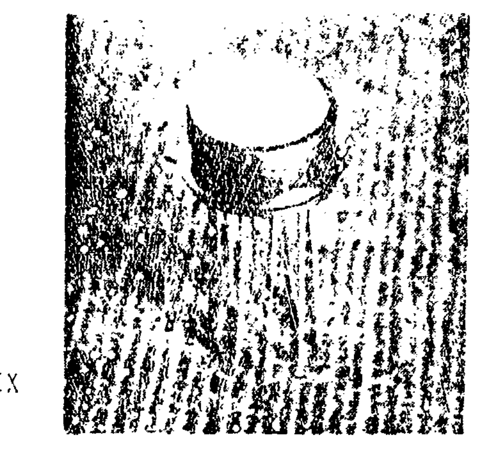
Metalization Type: Aluminum

Metalization Thickness: 19,522Å

Scribe Method: Mechanical

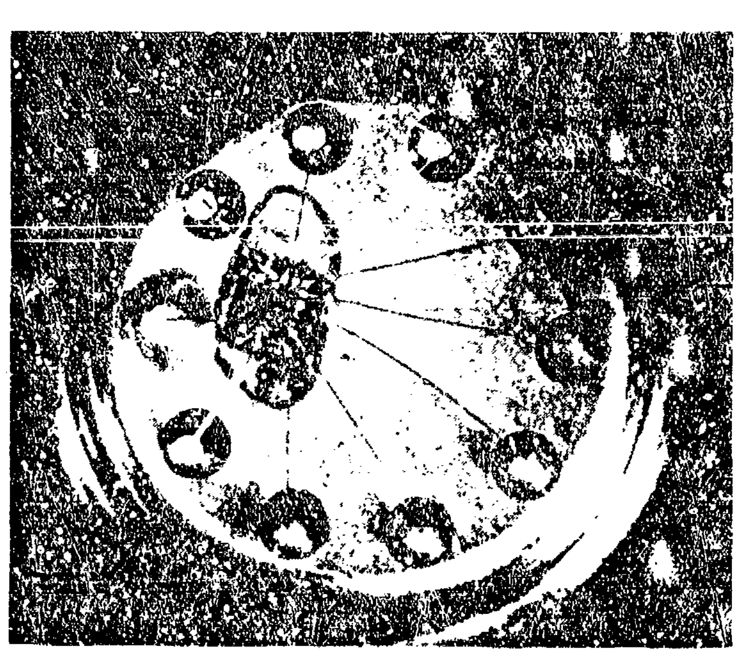
Bond Pad Size: 0.004 inch x 0.004 inch

V_{CC} Scribe Cross-Sectional Area: $1.96 \times 10^{-4} cm \times 2.26 \times 10^{-2} cm = 4.42 \times 10^{-6} cm^2$



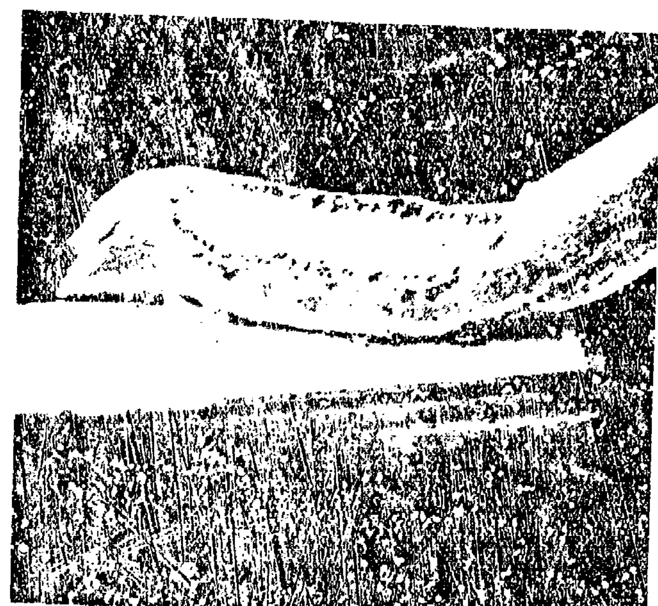
EX S/N51

FIGURE A6-1 - PACKAGE PHOTOGRAPH



10X S/N51

FIGURE A6-2 - INTERCONNECTION PHOTOGRAPH



520X
(SEM-1.2KV)

S/N51

FIGURE A6-3 - WIRE BOND AT DIE

430X
(SEM-1.2KV)

S/N51

FIGURE A6-4 - WIRE BOND AT POST

D. COMPONENT DESCRIPTION

Since a schematic for Manufacturer C device is not included in MIL-M-38510/10201, the closest equivalent was selected (Circuit C) and this schematic was modified to agree with the actual circuit determined from a microscopic examination of the die. The actual schematic is included as Figure A6-5 and the die photograph with circuit elements identified is included as Figure A6-6. The following modification was made:

1. The resistor between Q3 collector and Q4 base does not exist and was removed from the schematic.

The change is indicated on the schematic by an asterisk (*).

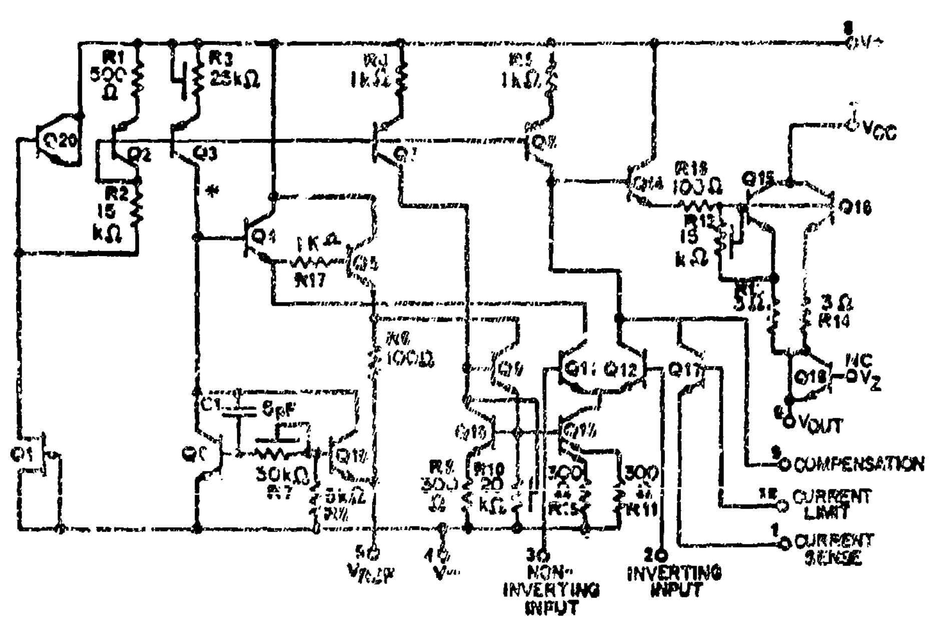
E. COMPONENT DESCRIPTION

From examination of the die surface, the structure of each component was determined.

1. TRANSISTORS (Transistors listed together share a common N-type collector or base tub.)

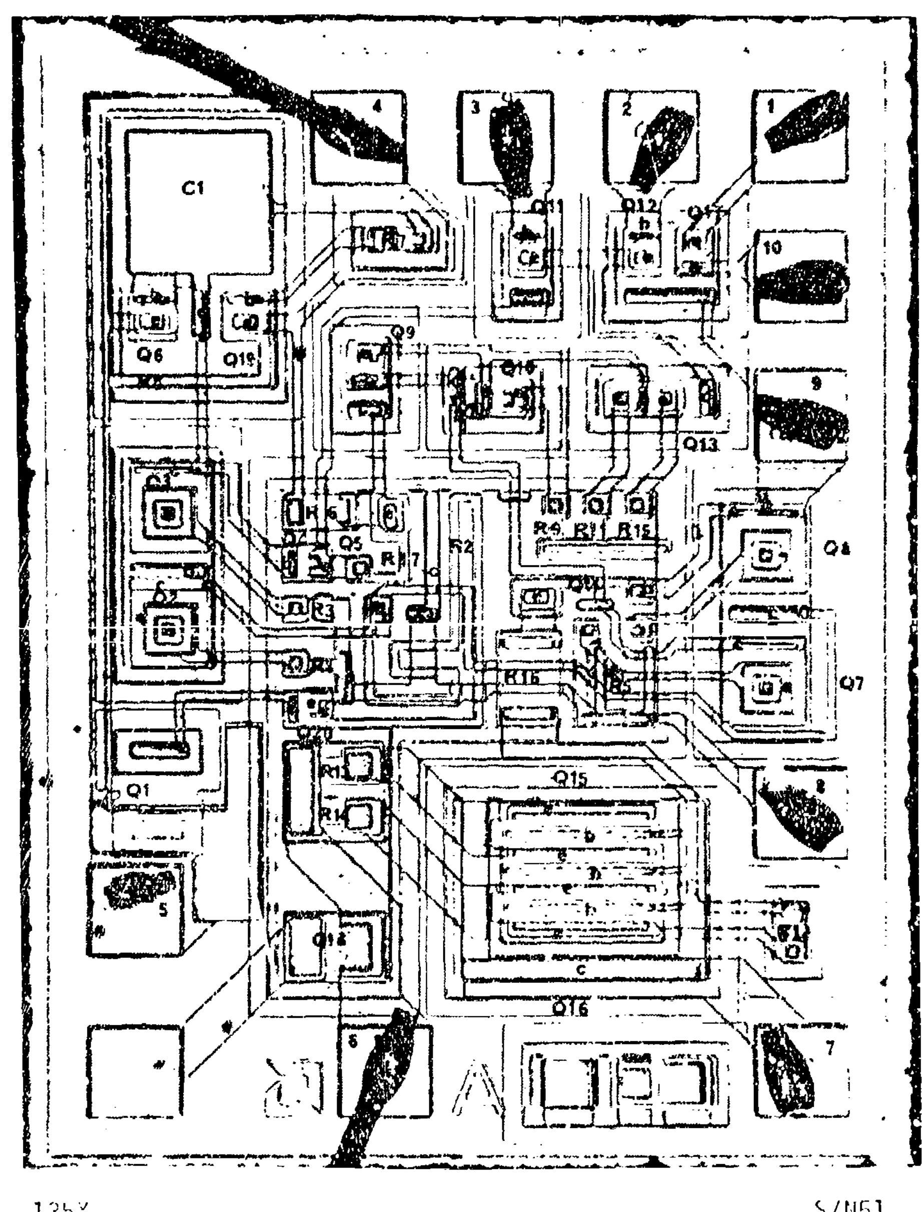
Vertical NPN	Lateral PNP	N Channel JFET
Q4, Q5, Q14, Q20*	Q2*, Q3	Q1
Q6, Q19	Q7, Q8	
Q9		
Q10		
Q11		
Q12, Q17		
Q13		
Q15, Q16		
Q18*		

* Diode connected transistor.



* Modifications to MIL-M-38510/10201 schematic.

FIGURE A6-5 - ELECTRICAL SCHEMATIC DIAGRAM



135X S/N51

FIGURE A6-6 - DIE PHOTOGRAPH

2. RESISTORS

P Type	Squeezed P Type	N^+
R1, R2	R3, R7, R10, R12	R13, R14
R4 thru R6		
R8, R9		
R11		
R15 thru R17		

3. CAPACITORS

MOS (thin oxide over N^+)
C1

F. QUALITY OF WORKMANSHIP

The quality of workmanship is considered acceptable per MIL-STD-883, Method 2010.3.

CONSTRUCTION ANALYSIS

M38510/10701BXC

MANUFACTURER D

VOLTAGE REGULATOR

DATE CODE 7432

MICROCIRCUIT CONSTRUCTION INFORMATION

S/N: 105 DATE CODE: 7432 DATE: 5/9/77

PART NAME: VOLTAGE REGULATOR

MANUFACTURERS PART NO. F78M05HMQB MANUFACTURER: D

GENERIC PART NO: 78M05 PACKAGE TYPE: TO-5

MILITARY SPECIFICATION NO: M38510/10701BXC

A PACKAGE DETAILS (See Figure A7-1)

Lead Material: Kovar
Lead Finish - Internal: Gold Plate
- External: Gold Plate
- Feed Through: None
Header Material: Gold Plated Kovar
Cap Material: Nickel
Case Seal Method: Weld
Lead Seal Material/Method: Matched Glass

B INTERCONNECTIONS DETAILS (See Figure A7-2)

Die Mounting Material: Gold Silicon Eutectic
Interconnect Wire Material: Aluminum
Interconnect Wire Diameter: 0.002 inch
Longest Interconnect Wire Length: 0.097 inch
Wire Bond Type (s) Post: Ultrasonic (See Figure A7-4)
Die: Ultrasonic (See Figure A7-3)

C. DIE DETAILS (See Figure A7-6)

Passivation Type:	Silicon Dioxide
Glassivation Type:	Vapox
Basic Die Construction:	Planar Epitaxial
Die Dimensions:	0.074 inch x 0.069 inch
Metalization Type:	Aluminum
Metalization Thickness:	12,988A
Scribe Method:	Mechanical
Bond Pad Size:	0.0066 inch x 0.0068 inch

Vcc Stripe Cross-Sectional Area: $1.30 \times 10^{-4} cm \times 1.35 \times 10^{-2} cm = 1.76 \times 10^{-6} cm^2$

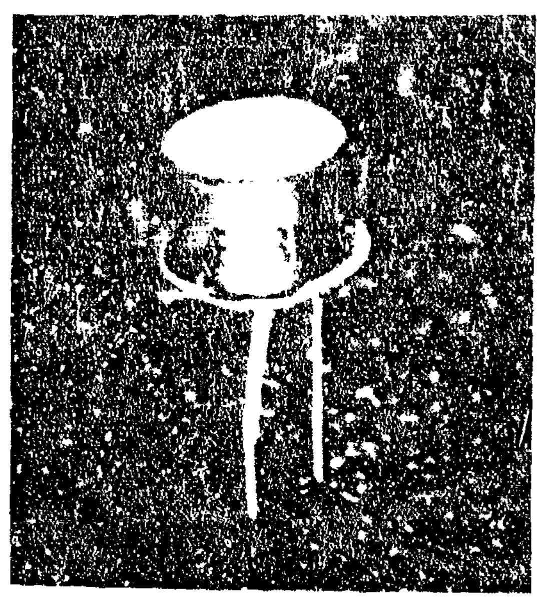
4X  S/N104

FIGURE A7-1- PACKAGE PHOTOGRAPH

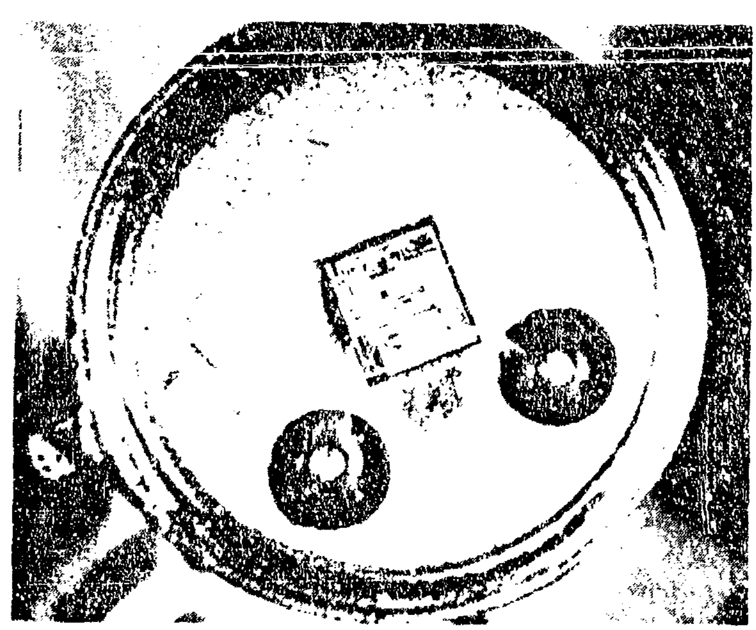
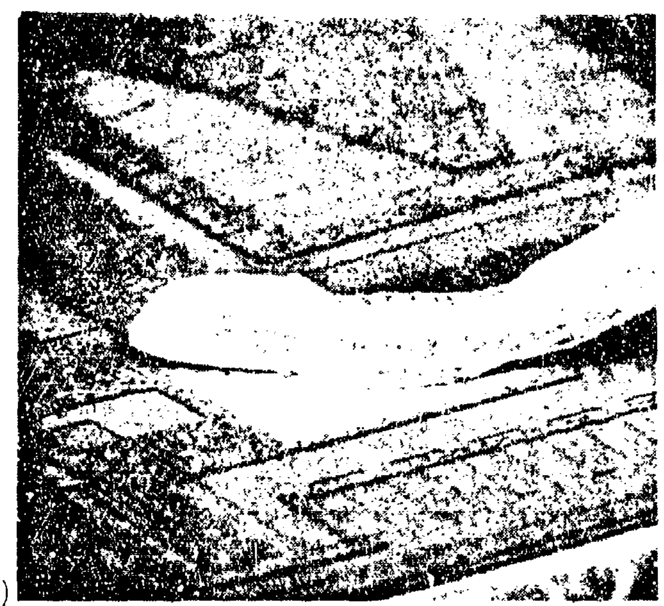
10X  S/N104

FIGURE A7-2- INTERCONNECTION PHOTOGRAPH

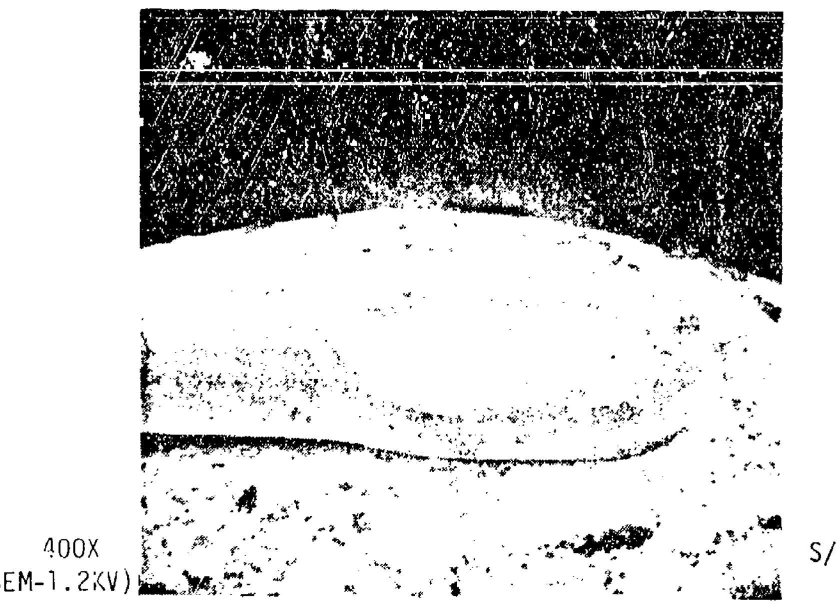
270X
(SEM-1.2KV)



S/N105

FIGURE A7-3- WIRE BOND AT DIE

400X
(SEM-1.2KV)



S/N105

FIGURE A7-4- WIRE BOND AT POST

D. ELECTRICAL SCHEMATIC

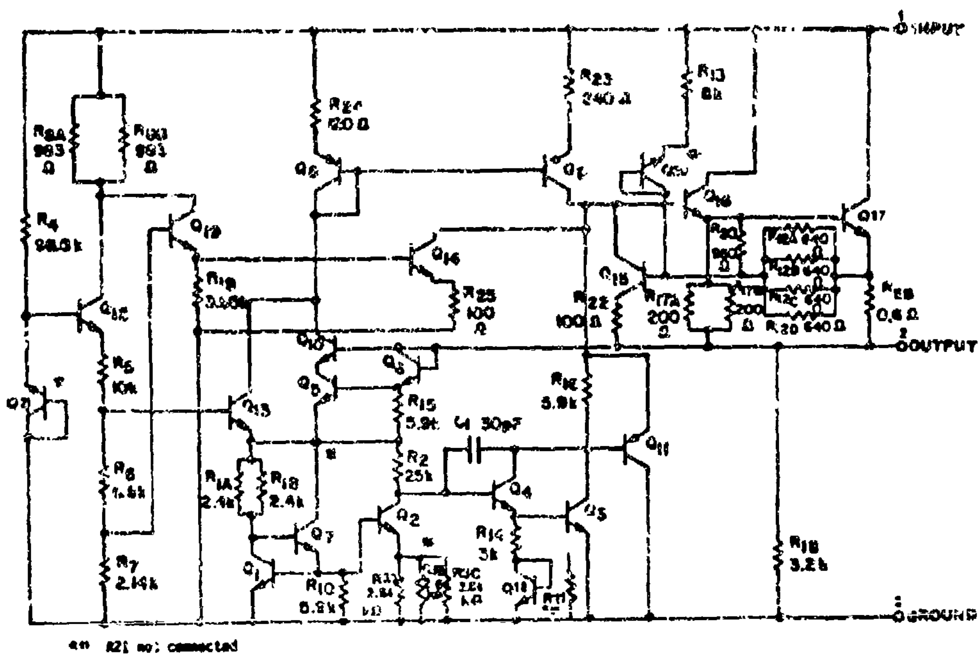
An electrical schematic of the device was prepared by modifying the schematic in MIL-M-38510/107. Schematic "C" for device 02 was selected as being the closest match to the circuitry on the die. The corrected schematic is included as Figure A7-5 and the die photomicrograph with circuit elements identified is shown in Figure A7-6. The schemacic modifications consisted of the following:

1. Diodes D1 and D2 of the military specifications were changed to diode connected transistor Q20 and Q21.

2. Q5 emitter was connected to Q13 and the junction of R2 and R15.

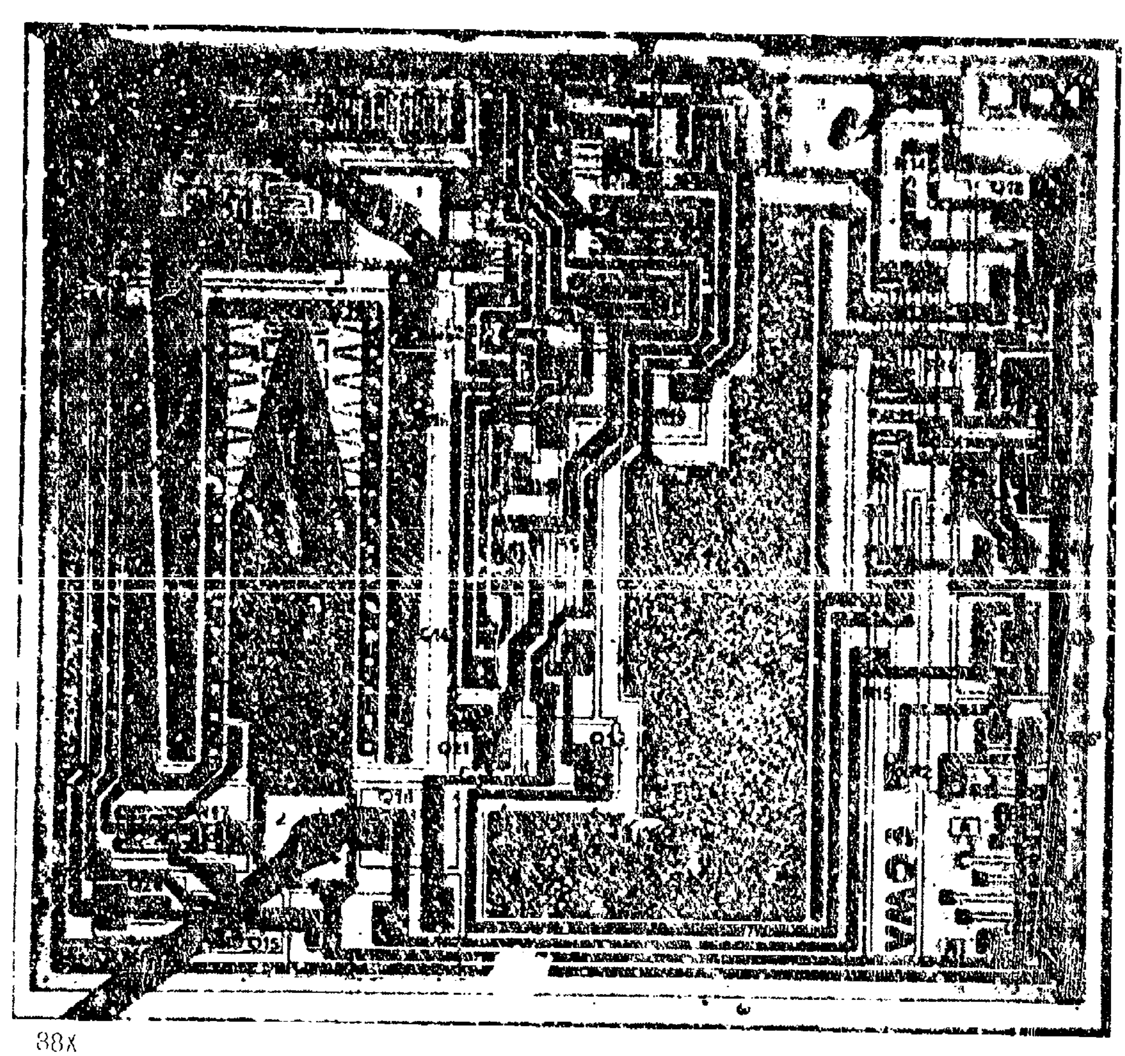
3. R3 was changed to 3 parallel resistors.

The changes are indicated on the schematic diagram with an asterisk (*). In addition there are nine unconnected and undesignated resistors since this same die is used for a number of different voltages.



*MODIFICATIONS TO MIL-M-38510/10702 SCHEMATIC

FIGURE A7-5 - ELECTRICAL SCHEMATIC DIAGRAM



88X

FIGURE A7-6 - DIE PHOTOGRAPH

E. COMPONENT DESCRIPTION

An examination of the die surface was conducted after removal of the glassivation and metallization in order to determine the structure of each circuit element.

1. TRANSISTORS (Transistors listed together share a common N type collector or base type diffusion)

Vertical NPN	Vertical PNP	Lateral PNP
Q1	Q11	Q8*, Q9
Q2		
Q3, Q4		
Q5		
Q6*		
Q7		
Q10		
Q12, Q19		
Q13		
Q14		
Q15		
Q16, Q17		
Q18*		
Q20*		
Q21*		

*diode connected transistors

2. RESISTORS

P type

R1 through R8

R10

R12 through R25

(Reference designations R9 and R11 are not used in the MIL-M-38510/10702 schematic C)

R_{EB}: The resistor designated REB represents a group of parallel emitter ballast resistors incorporated into the large power transistor Q17 to equalize the current distribution over the full length of the transistor. A photomicrograph of a portion of transistor Q17 after removal of the glassivation and metalization is included as Figure A7-7. The extra base type diffusions around the emitter contacts create restricted current paths to the emitter contactor.

3. CAPACITORS

MOS (thick oxide over N)

C1

F. QUALITY OF WORKMANSHIP

The quality of workmanship is considered acceptable per MIL-STD-883. Method 2010.3.

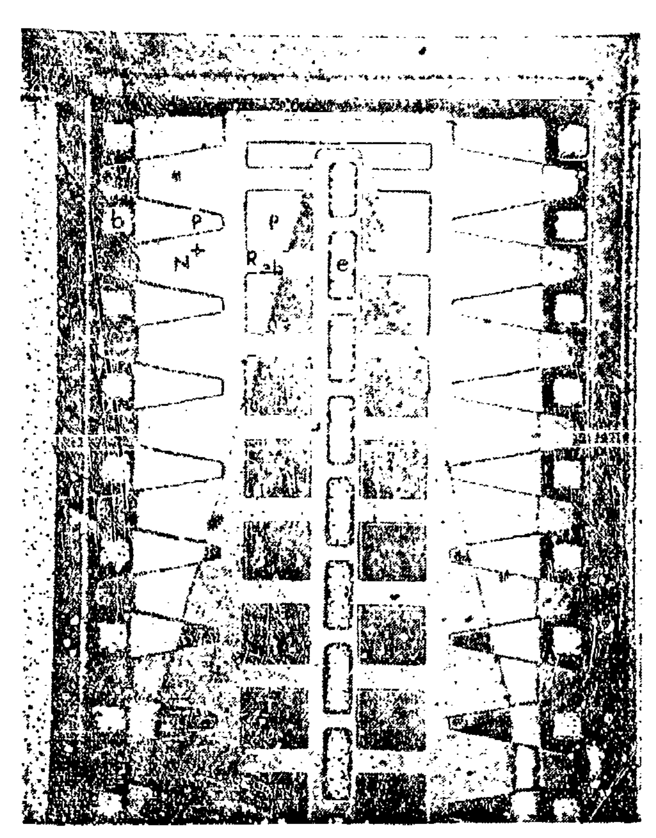


FIGURE 7-7 - TRANSISTOR Q17

CONSTRUCTION ANALYSIS

M38510/10701BXC

MANUFACTURER B

VOLTAGE REGULATOR

DATE CODE 7552

MICROCIRCUIT CONSTRUCTION INFORMATION

S/N: 43 DATE CODE: 7552 DATE: 5/9/77

PART NAME: VOLTAGE REGULATOR

MANUFACTURERS PART NO: LM109/10701/BXC MANUFACTURER: B

GENERIC PART NO: LM109 PACKAGE TYPE: TO-5

MILITARY SPECIFICATION NO: M38510/10701BXC

A PACKAGE DETAILS (See Figure A8-1)

Lead Material: Kovar
Lead Finish - Internal: Gold Plate
- External: Gold Plate
- Feed Through: None

Header Material: Gold Plated Kovar
Cap Material: Nickel
Case Seal Method: Weld
Lead Seal Material/Method: Matched Glass

B INTERCONNECTION DETAILS (See Figure A8-2)

Die Mounting Material: Gold - Silicon Eutectic
Interconnect Wire Material: Aluminum
Interconnect Wire Diameter: .0032 inch
Longest Interconnect Wire Length: 0.128 inch
Wire Bond Type (s) Post: Ultrasonic (See Figure A8-4)
Die: Ultrasonic (See Figure A8-3)

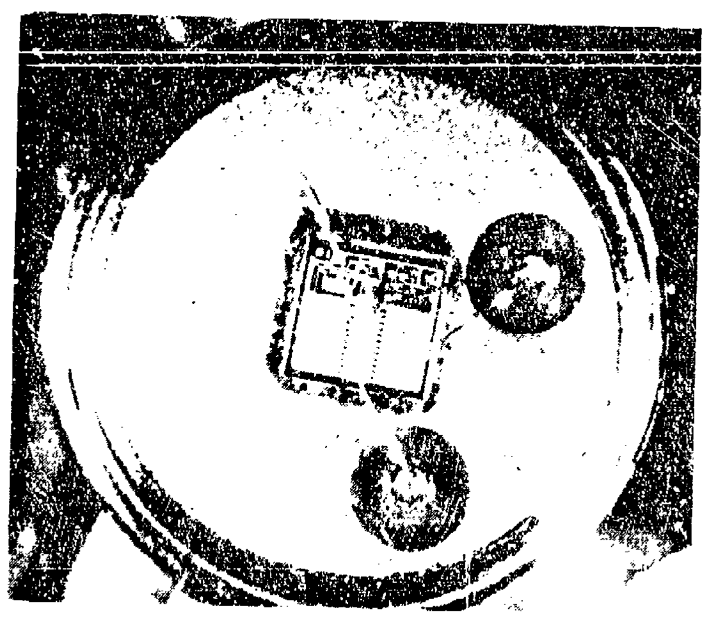
C. DIE DETAILS (See Figure A8-6)

Passivation Type:	Silicon Dioxide
Glassivation Type:	Phosphorus Glass
Basic Die Construction:	Planar Epitaxial
Die Dimensions:	0.084 inch x 0.077 inch
Metalization Type:	Aluminum
Metalization Thickness	11,006Å
Scribe Method:	Mechanical
Bond Pad Size:	0.007 inch x 0.007 inch

Vcc Stripe Cross-Sectional Area: 1.10×10^{-4}cm $\times$ 1.34×10^{-2}cm $= 1.47 \times 10^{-6}$cm^2

5X S/N42

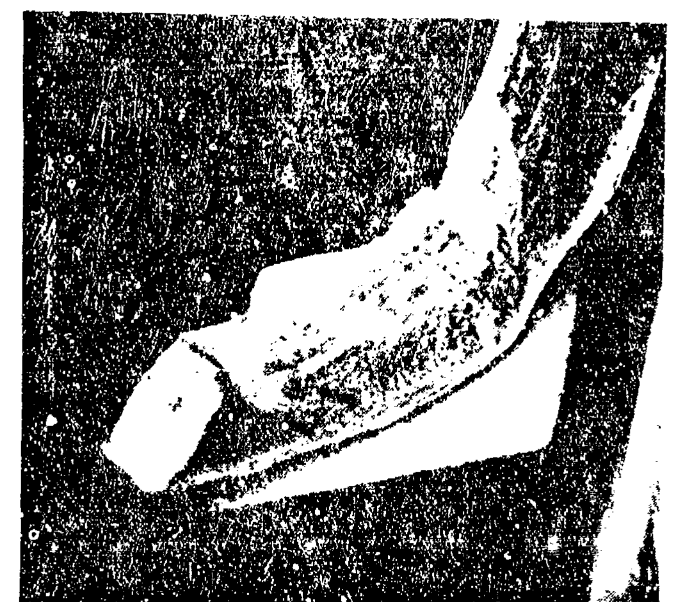
FIGURE A8-1- PACKAGE PHOTOGRAPH



10X S/N43

FIGURE A8-2- INTERCONNECTION PHOTOGRAPH

300X
(SEM-1.2KV)



S/N43

FIGURE A8-3 - WIRE BOND AT DIE

250X
(SEM-1.2KV)

S/N43

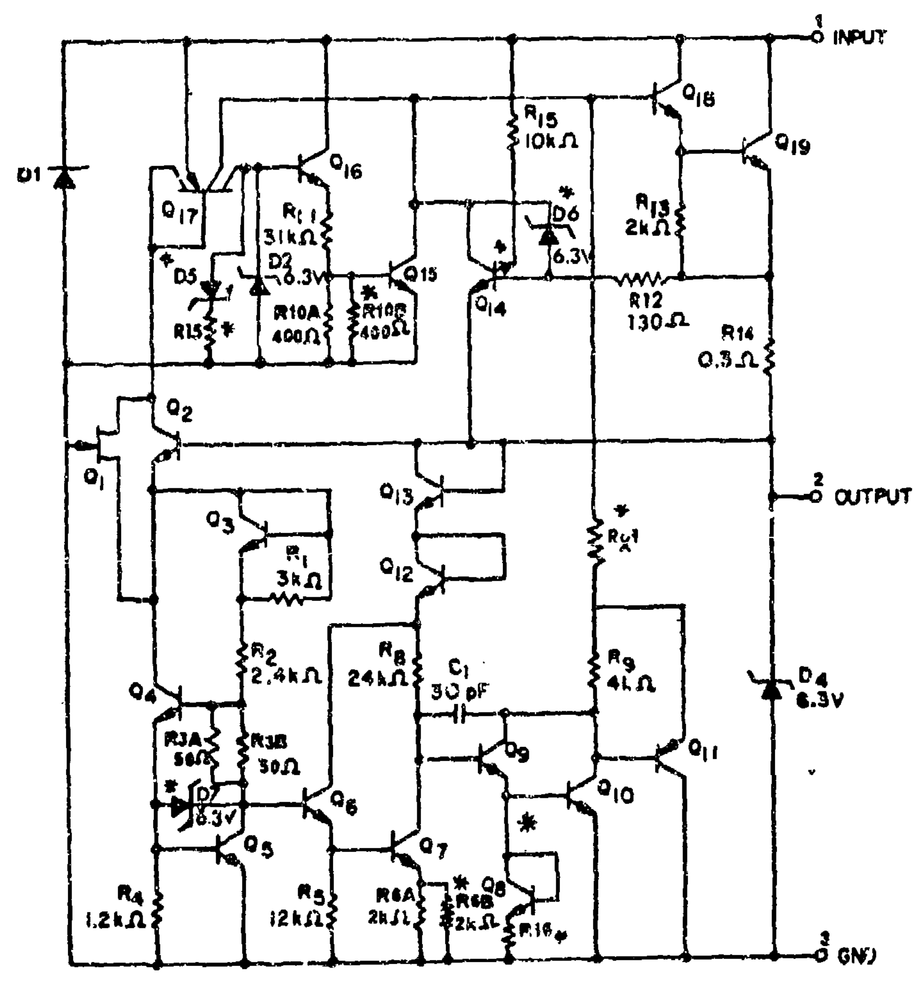
FIGURE A8-4 - WIRE BOND AT POST

D. ELECTRICAL SCHEMATIC

An electrical schematic diagram was prepared by modifying the schematic included in MIL-M-38510/107 for device 01 to conform to the actual circuitry on the die. The modifications resulted from a detailed microscopic study of the die and included removal of the glassivation and metalization. The modified schematic is shown as Figure A8-5. A die photomicrograph with the circuit components identified is included as Figure A8-6. The schematic modifications were as follows:

1. Resistor R10 is two resistors in parallel.
2. Resistor R6 is two resistors in parallel.
3. Diode D3 of the MIL-M-38510 schematic was changed to an additional emitter on Q14.
4. Crossunder Rx1 was added.
5. Resistor R16 was added between Q8 emitter and terminal 3.
6. Resistor R7 does not exist on the die.
7. Resistor R15 and diode D5 were added across D2.
8. Added D6 across the C-B junction of Q14.
9. Added D7 across the C-B junction of Q5.

The modifications are indicated on the schematic diagram with an asterisk (*).



*MODIFICATIONS TO MIL-M-38510/10701 SCHEMATIC

FIGURE A8-5 - ELECTRICAL SCHEMATIC DIAGRAM

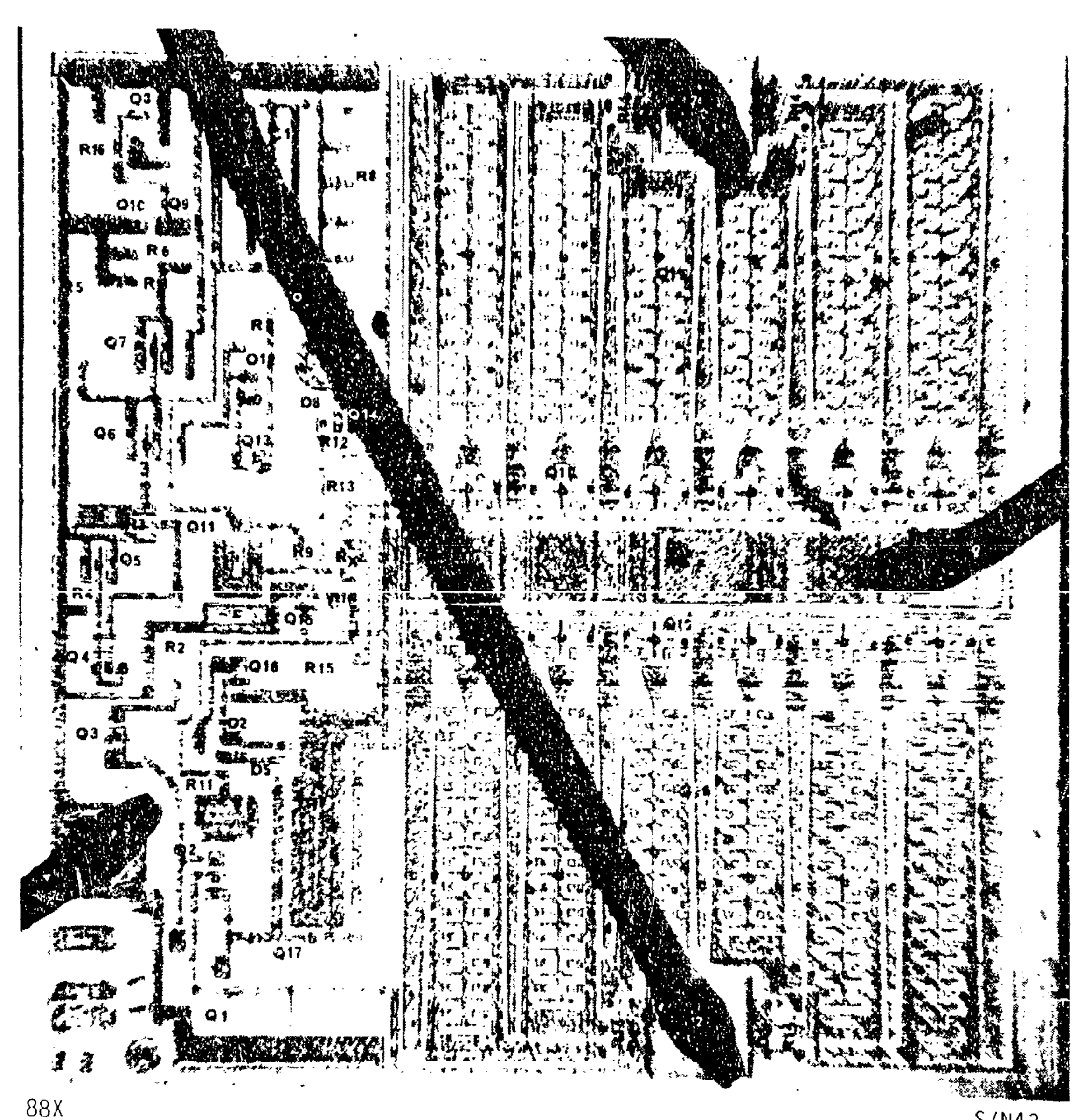


FIGURE A8-6 - DIE PHOTOGRAPH

E. COMPONENT DESCRIPTION

An examination of the die was conducted in order to determine the structure of each circuit element.

1. TRANSISTORS (Transistors listed together share a common N type collector or base tub)

Vertical NPN	Vertical PNP	Lateral PNP	N Channel J FET
Q2	Q11	Q17	Q1
Q3*, Q4			
Q5			
Q6			
Q7			
Q8*			
Q9, Q10			
Q12*			
Q13*			
Q14, Q15			
Q16			
Q18			
Q19			

*diode connected transistors

2. DIODES

PN	PN+
D1⚠	D2
	D4
	D5
	D6
	D7

⚠ Collector isolation diode of Q19

3. RESISTORS

P type	N+	Squeezed P type
R1 thru R6	R14	R15
R8 thru R13	Rx1	
R16		

Reference designation R7 removed

4. CAPACITOR

Emitter - Base Junction Capacitor

C1

F. QUALITY OF WORKMANSHIP

The quality of workmanship is considered acceptable per MIL-STD-883, Method 2010.3.

CONSTRUCTION ANALYSIS

M38510/10304BGC

MANUFACTURER D

PRECISION VOLTAGE COMPARATOR/BUFFER

DATE CODE 7612

MICROCIRCUIT CONSTRUCTION INFORMATION

S/N: 311 DATE CODE: 7612 DATE: 7/20/77

PART NAME: PRECISION VOLTAGE COMPARATOR/BUFFER

MANUFACTURERS PART NO. µA111HMQB MANUFACTURER: D

GENERIC PART NO: LM111 PACKAGE TYPE: 8 LEAD CAN

MILITARY SPECIFICATION NO: M38510/10304BGC

A. PACKAGE DETAILS (See Figure A9-1)

Lead Material:	Kovar
Lead Finish - Internal:	Gold Plate
- External:	Gold Plate
- Feed Through:	None
Header Material:	Gold Plated Kovar
Cap Material:	Nickel
Case Seal Method:	Weld
Lead Seal Material/Method:	Matched Glass

B. INTERCONNECTION DETAILS (See Figure A9-2)

Die Mounting Material:	Gold-Silicon Eutectic
Interconnect Wire Material:	Aluminum
Interconnect Wire Diameter:	0.0012 inch
Longest Interconnect Wire Length:	0.102 inch
Wire Bond Type (s) Post:	Ultrasonic (See Figure A9-4)
Die:	Ultrasonic (See Figure A9-3)

C. DIE DETAILS (See Figure A9-8)

Passivation Type: Silicon Dioxide
Glassivation Type: Silicon Dioxide
Basic Die Construction: Planar Epitaxial
Die Dimensions: 0.048 inch x 0.064 inch
Metalization Type: Aluminum
Metalization Thickness: 11,938Å
Scribe Method: Mechanical
Bond Pad Size: 0.004 inch x 0.004 inch
Vcc Stripe Cross-Sectional Area: 1.19×10^{-4} cm $\times$ 2.54×10^{-3} cm = 3.02×10^{-7} cm^2

3X S/N 311

FIGURE A9-1 - PACKAGE PHOTOGRAPH

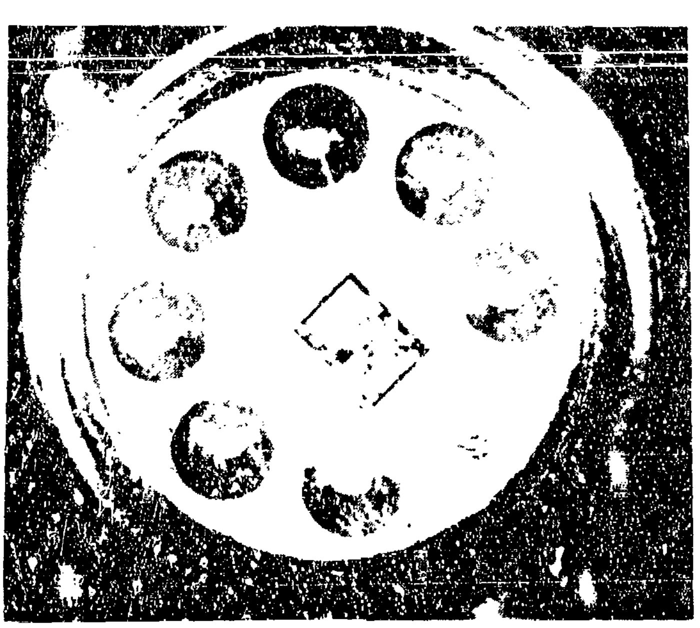
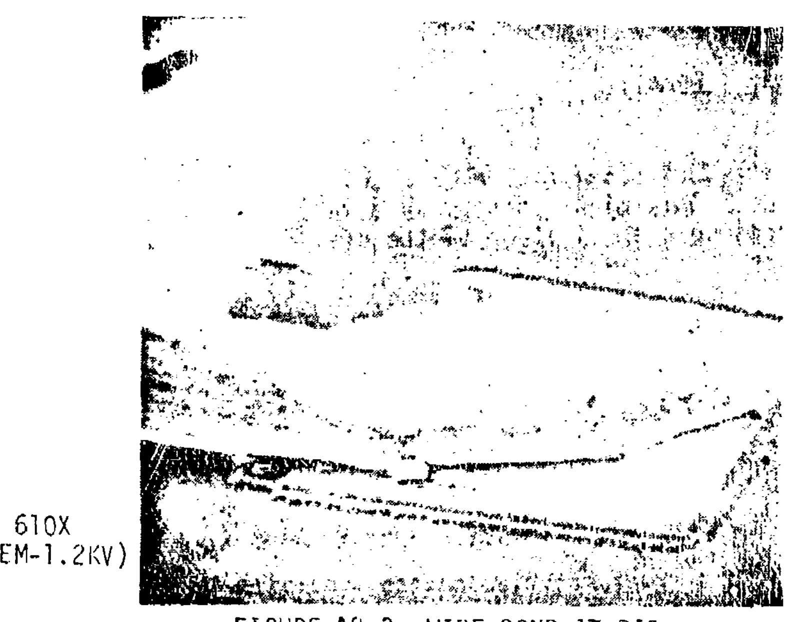
10X  S/N 311

FIGURE A9-2 - INTERCONNECTION PHOTOGRAPH

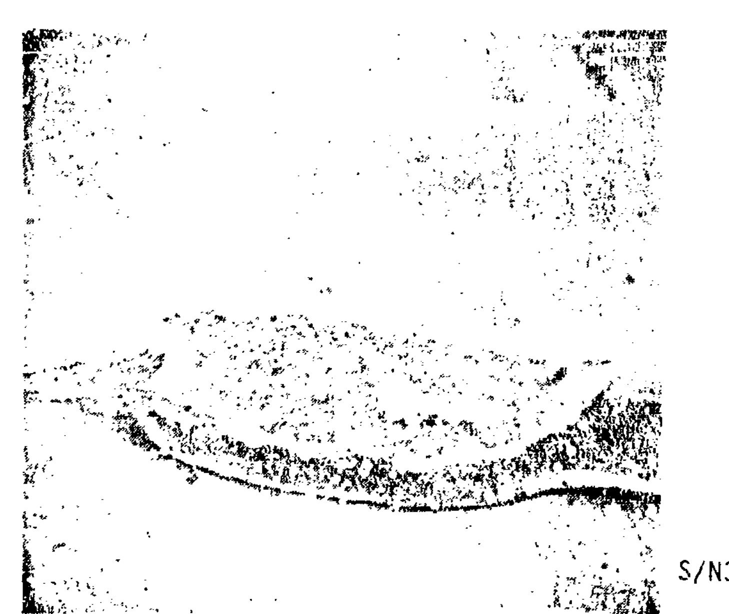
610X
(SEM-1.2KV)



S/N311

FIGURE A9-3 WIRE BOND AT DIE

610X
(SEM-1.2KV)



S/N311

FIGURE A9-4 WIRE BOND AT POST

D. ELECTRICAL SCHEMATIC

The MIL-M-38510/10304 schematic "A" was determined to be the schematic for this device. Only minor changes were made to this schematic as a result of microscopic examination of the die. The schematic modifications are as follows:

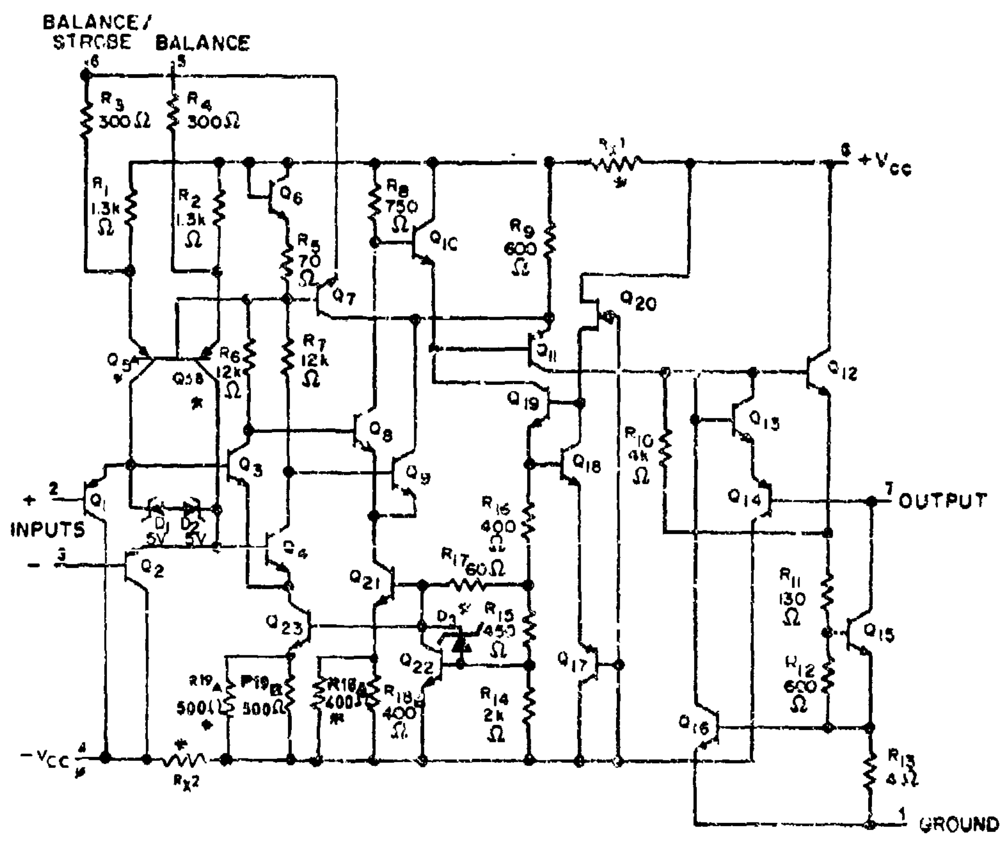
1. Q5 is actually two separate transistors, therefore one is designated Q5A and the other Q5B.

2. Crossunders Rx1 and Rx2 were added.

3. R18 and R19 are actually two resistors in parallel.

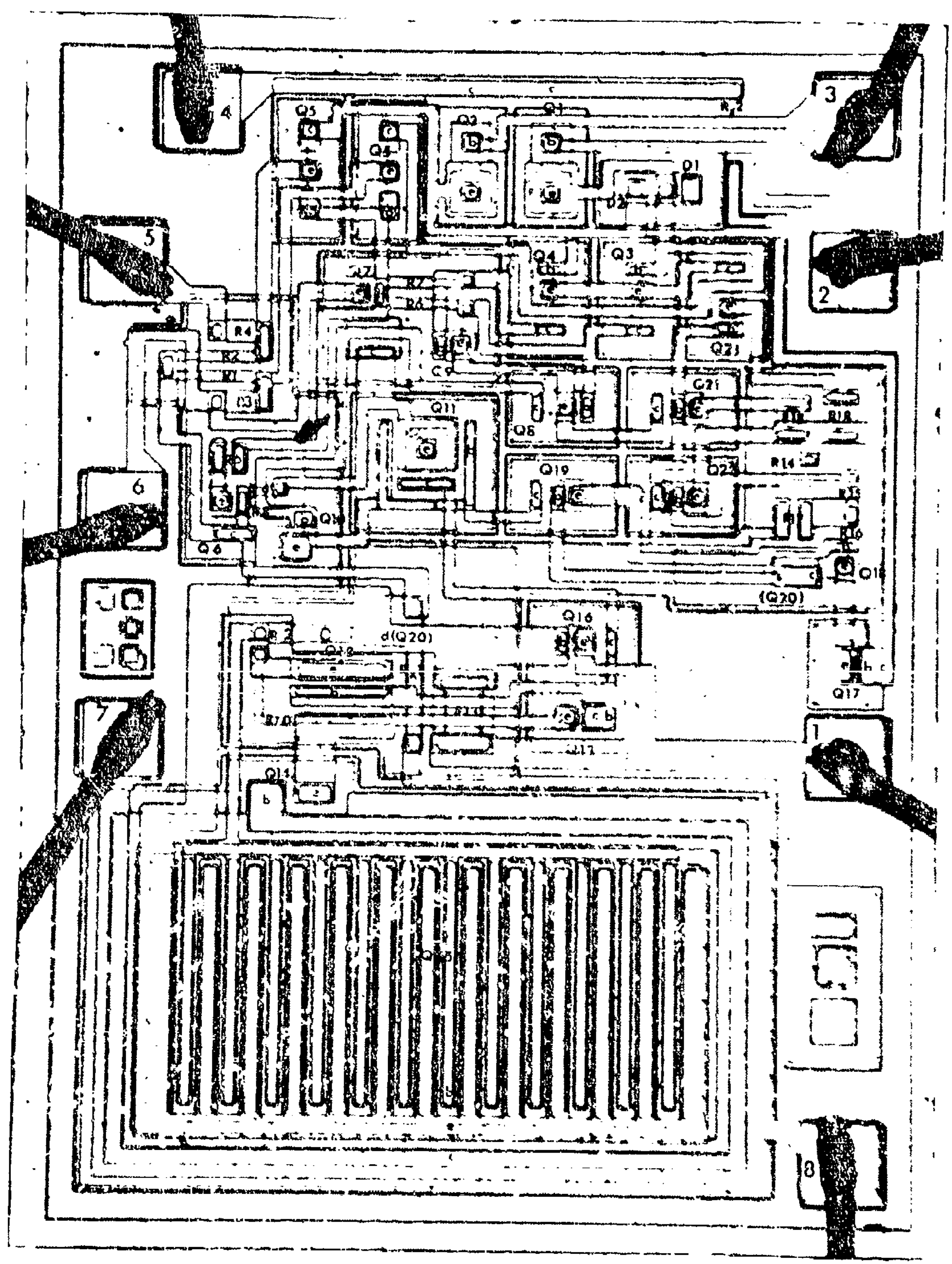
4. D3 was added across the C-B junction of Q22.

These modifications are identified on the schematic diagram (Figure A9-5) by an asterisk (*). A die photomicrograph with the circuit elements identified is included as Figure A9-6.



*MODIFICATIONS TO MIL-M 38510/10304 SCHEMATIC

FIGURE A95 - ELECTRICAL SCHEMATIC DIAGRAM



130X

S/N 311

FIGURE A9-6 - DIE PHOTOGRAPH

E. COMPONENT DESCRIPTION

An examination of the die surface was conducted after removal of the glassivation and metallization in order to determine the structure of each circuit element.

1. TRANSISTORS (Transistors listed together share a common N type collector or base tub)

Vertical NPN	Vertical PNP	Lateral PNP	N Channel J FET
Q3	Q1	Q5A	Q20
Q4	Q2	Q5B	
Q6*, Q10	Q14	Q11	
Q7, Q9	Q17*		
Q8			
Q12			
Q13*, Q16			
Q15			
Q18			
Q19			
Q21			
Q22			
Q23			

*Diode connected transistors.

2. DIODES

PN+
D1
D2
D3

3. RESISTORS

P type	N+
R1 thru R12	R13
R14 thru R19	Rx1
	Rx2

F. QUALITY OF WORKMANSHIP

The quality of workmanship is considered acceptable per MIL-STD-883, Method 2010.3.

CONSTRUCTION ANALYSIS

M38510/10304BGC

MANUFACTURER B

PRECISION VOLTAGE COMPARATOR/BUFFER

DATE CODE 7601

MICROCIRCUIT CONSTRUCTION INFORMATION

S/N: 311 DATE CODE: 7601 DATE: 7/20/77

PART NAME: PRECISION VOLTAGE COMPARATOR/BUFFER

MANUFACTURERS PART NO. LM111H/10304BGC MANUFACTURER: B

GENERIC PA[illegible] NO. LM111 PACKAGE TYPE 8 LEAD CAN

MILITARY SPECIFICATION NO: M38510/10304BGC

A. PACKAGE DETAILS (See Figure A10-1)

Lead Material:	Kovar
Lead Finish - Internal:	Gold Plate
- External:	Gold Plate
- Feed Through:	None
Header Material:	Gold Plated Kovar
Cap Material:	Nickel
Case Seal Method:	Weld
Lead Seal Material/Method:	Matched Glass

B. INTERCONNECTION DETAILS (See Figure A10-2)

Die Mounting Material:	Gold Silicon Eutectic
Interconnect Wire Material:	Aluminum
Interconnect Wire Diameter:	0.0011 inch
Longest Interconnect Wire Length:	0.102 inch
Wire Bond Type (s) Post:	Ultrasonic (See Figure A10-4)
Die:	Ultrasonic (See Figure A10-3)

C. DIE DETAILS (See Figure A10-6)

Passivation Type:	Silicon Dioxide
Glassivation Type:	Silicon Dioxide
Basic Die Construction:	Planar Epitaxial
Die Dimensions:	0.045 inch x 0.063 inch
Metalization Type:	Aluminum
Metalization Thickness:	14.732Å
Scribe Method:	Mechanical
Bond Pad Size:	0.0034 inch x 0.0034 inch
Vcc Stripe Cross Sectional Area:	9.88×10^{-3} cm $\times 1.47 \times 10^{-4}$ cm $= 1.46 \times 10^{-6}$ cm^2

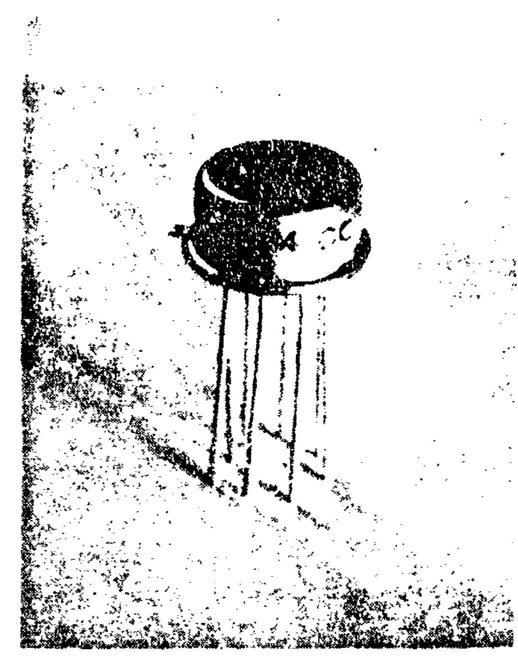
3X  S/N 311

FIGURE A10-1-PACKAGE PHOTOGRAPH

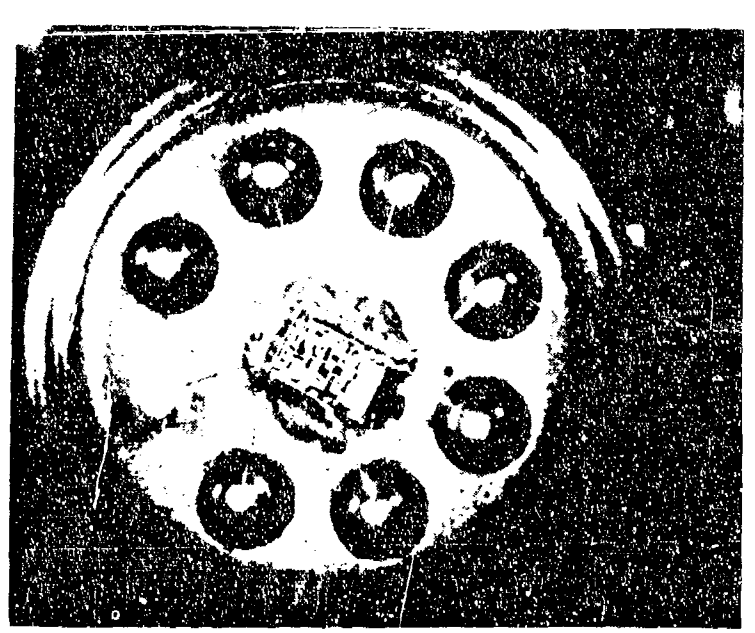
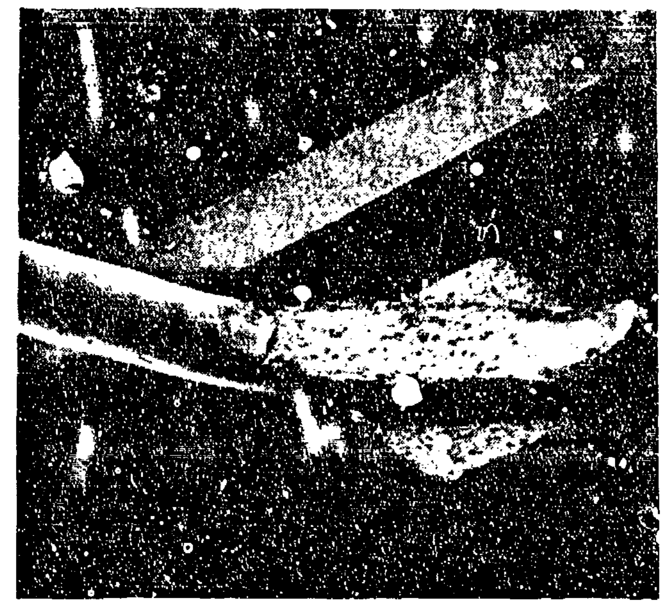
10X  S/N 311

FIGURE 10-2- INTERCONNECTION PHOTOGRAPH

450X
(SEM-1.2KV)



S/N 311

FIGURE A-10 - WIRE BOND AT DIE

680X
(SEM-1.2KV)

S/N 311

FIGURE A10-4-WIRE BOND AT POST

D. ELECTRICAL SCHEMATIC

The MIL-M-38510/10301 schematic "B" was determined to be the schematic for this device. A comparison between this schematic and the actual die layout was made after removal of glassivation and metalization. A number of changes in the schematic were required to produce agreement with the actual die layout.

1. Crossunders Rx1 and Rx2 were added.

2. Q5 is actually two separate transistors; therefore, one is designated Q5A and the other Q5B.

3. The diode shown connected to the collector of Q15 is actually a verticle PNP transistor (there is no buried layer under the emitter diffusion); therefore, the diode was changed to Q24.

4. Diode D5 was added across the C-B junction of Q22.

Changes in the schematic are indicated on the schematic diagram (Figure A10-5) with an asterisk (*). The die photomicrograph with the circuit elements identified is included as Figure A10-6.

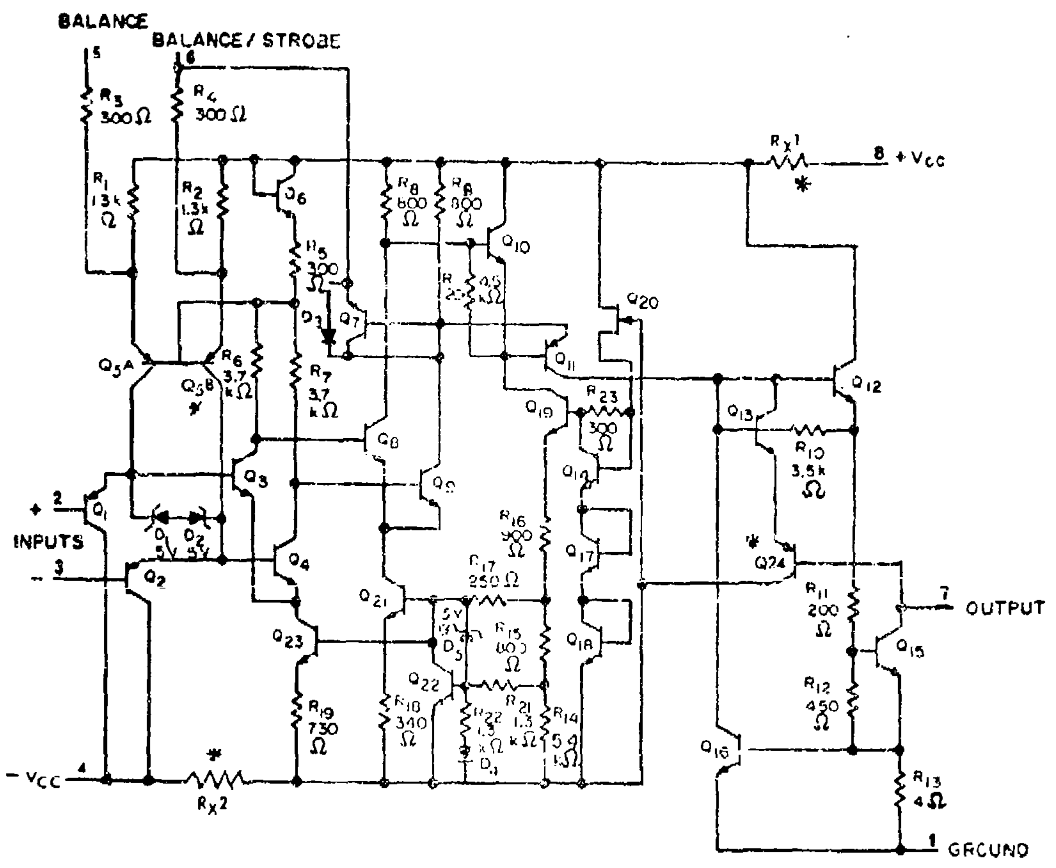
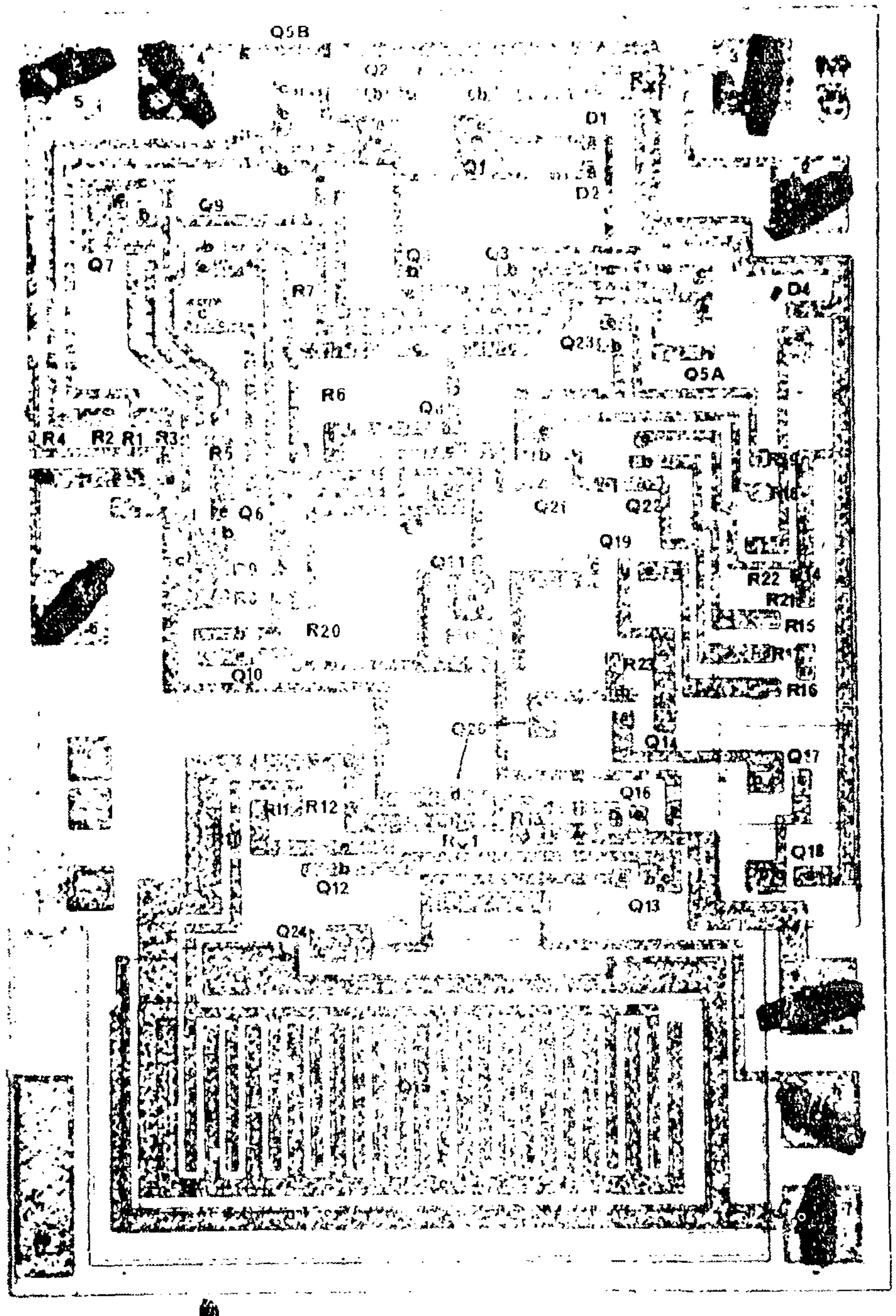


FIGURE A10-5 - SCHEMATIC DIAGRAM



130X S/N 311

FIGURE 10-6 - DIE PHOTO

E. COMPONENT DESCRIPTION

An examination of the die surface was conducted after removal of glassivation and metalization to determine the structure of each circuit element.

1. TRANSISTORS (Transistors listed together share a common N type collector or base diffusion)

Vertical NPN	Vertical PNP	Lateral PNP	N Channel J-FET
Q3	Q1	Q5A	Q20
Q4	Q2	Q5B	
Q6*, Q10		Q11	
Q7*, Q9			
Q8			
Q12			
Q13*, Q16			
Q14			
Q15			
Q17*			
Q18*			
Q19			
Q21			
Q22			

*diode connected transistors

2. DIODES

PN	Diode connected NPN transistor
D1	D4
D2	
D3	
D5	

D3 Removed

3. RESISTORS

P	N+
R1 thru R12	R13
R14 thru R23	Rx1
	Rx2

F. QUALITY OF WORKMANSHIP

The quality of workmanship is considered acceptable per MIL-STD-883, Method 2010.3.

APPENDIX B

ELECTRICAL TEST CONDITIONS

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TABLE E1. INITIAL/FINAL AND INTERIM TESTS FOR MIL-M-38510/10104 & MIL-M-38510/10107

PARAMETER	INITIAL/FINAL TEST #'S			INTERIM TEST #
	25°C	125°C	-55°C	25°C
V_{IO}	1, 2, 3, 4	25, 26, 27	46, 47, 48	1, 2, 3, 4
I_{IO}	5, 6, 7, 8	31, 32, 33	52, 53, 54	5, 6, 7, 8
$+I_{IB}$	9, 10, 11, 12	37, 38, 39	58, 59, 60	9, 10, 11, 12
$-I_{IB}$	13, 14, 15, 16	40, 41, 42	61, 62, 63	13, 14, 15, 16
+PSRR	17	-	-	17
-PSRR	18	-	-	18
CMR	19	-	-	19
V_{IO} ADJ(+)	20	-	-	20
V_{IO} ADJ(-)	21	-	-	21
I_{OS} (+)	22	43	64	22
I_{OS} (-)	23	44	65	23
P_D	24	45	66	24
V_{OPP}	67, 68	77, 78	87, 88	67, 68
$+A_{VS}$	69, 71, 73, 75	79, 81, 83, 85	89, 91, 93, 95	69, 71, 73, 75
$-A_{VS}$	70, 72, 74, 76	80, 82, 84, 86	90, 92, 94, 96	70, 72, 74, 76

TABLE B2. CHARACTERIZATION TESTS FOR MIL-M-38510/10104 & MIL-M-38510/10107

PARAMETER	CHARACTERIZATION TEST #'S		
	25°C	125°C	-55°C
TR	97, 98	108, 109	115, 116
SR	99, 100	110, 111	117, 118
t_s *	106, 107	113, 114	120, 121
$\Delta V_{IO}/\Delta T$	----	28, 29, 30	49, 50, 51
$\Delta I_{IO}/\Delta T$	----	34, 35, 36	55, 56, 57

* DEVICE 38510/10107 ONLY

TABLE B3. TEST SPECIFICATIONS FOR MIL-M-38510/101 (continued)

Subgroup	Symbol	MIL-STD-883 method	Test no.	Conditions $\pm V_{CC} = \pm 20$ Vdc, FIG. B1. UNLESS OTHERWISE SPECIFIED.	-04 Limits Min	-04 Limits Max	-07 Limits Min	-07 Limits Max	Unit
1 $T_A = 25°C$	V_{IO}	4001	1	$V_{CM} = -15$ V 1/	-0.5	+0.5	-4.0	+4.0	mV
↓	↓	↓	2	$V_{CM} = +15$ V 1/	↓	↓	↓	↓	↓
↓	↓	↓	3	$V_{CM} = 0$ V	↓	↓	↓	↓	↓
↓	↓	↓	4	$\pm V_{CC} = \pm 5$ V, $V_{CM} = 0$ V	↓	↓	↓	↓	↓
↓	I_{IO}	4001	5	$V_{CM} = -15$ V 1/	-0.2	+0.2	-40	+40	nA
↓	↓	↓	6	$V_{CM} = +15$ V 1/	↓	↓	↓	↓	↓
↓	↓	↓	7	$V_{CM} = 0$ V	↓	↓	↓	↓	↓
↓	↓	↓	8	$\pm V_{CC} = \pm 5$ V, $V_{CM} = 0$ V	↓	↓	↓	↓	↓
↓	$+I_{IB}$	4001	9	$V_{CM} = -15$ V 1/	-0.1	2.0	+1.0	250	nA
↓	↓	↓	10	$V_{CM} = +15$ V 1/	↓	↓	↓	↓	↓
↓	↓	↓	11	$V_{CM} = 0$ V	↓	↓	↓	↓	↓
↓	↓	↓	12	$\pm V_{CC} = \pm 5$ V, $V_{CM} = 0$ V	↓	↓	↓	↓	↓
↓	$-I_{IB}$	4001	13	$V_{CM} = -15$ V 1/	-0.1	2.0	+1.0	250	nA
↓	↓	↓	14	$V_{CM} = +15$ V 1/	↓	↓	↓	↓	↓
↓	↓	↓	15	$V_{CM} = 0$ V	↓	↓	↓	↓	↓
↓	↓	↓	16	$\pm V_{CC} = \pm 5$ V, $V_{CM} = 0$ V	↓	↓	↓	↓	↓
↓	+PSRR	4003	17	$+V_{CC} = 10$ V, $-V_{CC} = -20$ V	-16	16	-100	100	µV/V
↓	-PSRR	4003	18	$+V_{CC} = 20$ V, $-V_{CC} = -10$ V	-16	16	-100	100	µV/V
↓	CMR	4003	19	$V_{CM} = \pm 15$ V	96	---	80	---	dB
↓	$V_{IO\ ADJ(+)}$		20		---	---	7.5	---	mV
↓	$V_{IO\ ADJ(-)}$		21		---	---	7.5	---	mV
↓	$I_{OS(+)}$ 5/	3011	22	$\pm V_{CC} = \pm 15$ V, 5 sec. minimum 8/	-15	-2.0	-40	-12	mA
↓	$I_{OS(-)}$ 5/	3011	23	$\pm V_{CC} = \pm 15$ V, 5 sec. minimum 8/	2.0	20	12	55	mA
↓	P_D	4005	24		2	24	10	280	mW
2 $T_A = 125°C$	V_{IO}	4001	25	$V_{CM} = -15$ V 1/	-1.0	+1.0	-7.0	+7.0	mV
↓	↓	↓	26	$V_{CM} = +15$ V 1/	↓	↓	↓	↓	↓
↓	↓	↓	27	$V_{CM} = 0$ V	↓	↓	↓	↓	↓

TABLE B3. TEST SPECIFICATIONS FOR MIL-M-38510/101 (continued)

Subgroup	Symbol	MIL STD-883 method	Test no.	Conditions $\pm V_{CC} = \pm 20$ Vdc, FIG. B1. UNLESS OTHERWISE SPECIFIED.	-04 Limits Min	-04 Limits Max	-07 Limits Min	-07 Limits Max	Unit
$T_A = 125°C$ 2	$\Delta V_{IO}/\Delta T$ 6/	4001	28	$\Delta V_{IO}/\Delta T$ = [V_{IO} (test 25) - V_{IO} (test 1)] x 10	-5.0	+5.0	-15	+15	µV/°C
			29	$\Delta V_{IO}/\Delta T$ = [V_{IO} (test 26) - V_{IO} (test 2)] x 10					
			30	$\Delta V_{IO}/\Delta T$ = [V_{IO} (test 27) - V_{IO} (test 3)] x 10					
	I_{IO}	4001	31	V_{CM} = -15 V 1/	-0.3	+0.3	-40	+40	nA
			32	V_{CM} = +15 V 1/					
			33	V_{CM} = 0 V					
	$\Delta I_{IO}/\Delta T$ 6/		34	$\Delta I_{IO}/\Delta T$ = [I_{IO} (test 31) - I_{IO} (test 5)] x 10	-2.4	+2.4	-200	+200	pA/°C
			35	$\Delta I_{IO}/\Delta T$ = [I_{IO} (test 32) - I_{IO} (test 6)] x 10					
			36	$\Delta I_{IO}/\Delta T$ = [I_{IO} (test 33) - I_{IO} (test 7)] x 10					
	$+I_{IB}$	4001	37	V_{CM} = -15 V 1/	-3.0	+3.0	+1.0	250	nA
			38	V_{CM} = +15 V 1/					
			39	V_{CM} = 0 V					
	$-I_{IB}$	4001	40	V_{CM} = -15 V 1/					
			41	V_{CM} = +15 V 1/					
			42	V_{CM} = 0 V					
	$I_{OS(+)}$ 5/	3011	43	$\pm V_{CC} = \pm 15$ V, 5 sec. minimum 8/	-15	-2.0	-40	-12	mA
	$I_{OS(-)}$ 5/	3011	44	$\pm V_{CC} = \pm 15$ V, 5 sec. minimum 8/	2.0	15	10	90	mA
	P_D	4005	45		2	15	10	240	mW

TABLE B3. TEST SPECIFICATIONS FOR MIL-M-38510/101 (continued)

Subgroup	Symbol	MIL-STD-883 method	Test no.	Conditions $\pm V_{CC} = \pm 20$ Vdc, FIG. B1. UNLESS OTHERWISE SPECIFIED.	-04, Limits Min	-04, Limits Max	-07 Limits Min	-07 Limits Max	Unit
3 $T_A = -55°C$	V_{IO}	4001	46	$V_{CM} = -15$ V 1/	-1.0	+1.0	-7.0	+7.0	mV
↓	↓	↓	47	$V_{CM} = +15$ V 1/	↓	↓	↓	↓	↓
↓	↓	↓	48	$V_{CM} = 0$ V	↓	↓	↓	↓	↓
↓	ΔV_{IO} 6/ / ΔT	4001	49	$\Delta V_{IO}/\Delta T$ = [V_{IO} (test 1) - V_{IO} (test 46)] x 12.5	-5.0	+5.0	-15	+15	μV/°C
↓	↓	↓	50	$\Delta V_{IO}/\Delta T$ = [V_{IO} (test 2) - V_{IO} (test 47)] x 12.5	↓	↓	↓	↓	↓
↓	↓	↓	51	$\Delta V_{IO}/\Delta T$ = [V_{IO} (test 3) - V_{IO} (test 48)] x 12.5	↓	↓	↓	↓	↓
↓	I_{IO}	4001	52	$V_{CM} = -15$ V 1/	-0.4	+0.4	-80	+80	nA
↓	↓	↓	53	$V_{CM} = +15$ V 1/	↓	↓	↓	↓	↓
↓	↓	↓	54	$V_{CM} = 0$ V	↓	↓	↓	↓	↓
↓	ΔI_{IO} 6/ / ΔT	4001	55	$\Delta I_{IO}/\Delta T$ = [I_{IO} (test 5) - I_{IO} (test 52)] x 12.5	-2.5	+2.5	-500	+500	pA/°C
↓	↓	↓	56	$\Delta I_{IO}/\Delta T$ = [I_{IO} (test 6) - I_{IO} (test 53)] x 12.5	↓	↓	↓	↓	↓
↓	↓	↓	57	$\Delta I_{IO}/\Delta T$ = [I_{IO} (test 7) - I_{IO} (test 54)] x 12.5	↓	↓	↓	↓	↓
↓	$+I_{IB}$	4001	58	$V_{CM} = -15$ V 1/	-0.1	4.0	+1.0	400	nA
↓	↓	↓	59	$V_{CM} = +15$ V 1/	↓	↓	↓	↓	↓
↓	↓	↓	60	$V_{CM} = 0$	↓	↓	↓	↓	↓
↓	$-I_{IB}$	4001	61	$V_{CM} = -15$ V 1/	-0.1	4.0	+1.0	400	nA
↓	↓	↓	62	$V_{CM} = +15$ V 1/	↓	↓	↓	↓	↓
↓	↓	↓	63	$V_{CM} = 0$ V	↓	↓	↓	↓	↓
↓	$I_{OS(+)}$ 5/	3011	64	$\pm V_{CC} = \pm 15$ V, 5 sec. minimum 8/	-15	-4.0	-55	-15	mA
↓	$I_{OS(-)}$ 5/	3011	65	$\pm V_{CC} = \pm 15$ V, 5 sec. minimum 8/	4.0	40	15	70	mA
↓	P_D	4005	66		2	32	10	320	mW

TABLE B3. TEST SPECIFICATIONS FOR MIL-M-38510/101 (continued)

Subgroup	Symbol	MIL-STD-883 method	Test no.	Conditions $\pm V_{CC} = \pm 20$ Vdc, FIG. 37. UNLESS OTHERWISE SPECIFIED.	-04, Limits Min	-04, Limits Max	-07 Limits Min	-07 Limits Max	Unit
4 $T_A = 25°C$	V_{OPP}	4004	67	$R_L = 10$ kΩ	32	---	34	---	V_{p-p}
↓	V_{OPP}	↓	68	$R_L = 2$ kΩ			32	---	V_{p-p}
↓	$+A_{VS}$	↓	69	$R_L = 2$ kΩ, $V_{OUT} = \pm 15$ V			80	---	V/mV
↓	$-A_{VS}$	↓	70	$R_L = 2$ kΩ, $V_{OUT} = \pm 15$ V			80	---	V/mV
↓	$+A_{VS}$	↓	71	$R_L = 10$ kΩ, $V_{OUT} = \pm 15$ V	80	---	80	---	V/mV
↓	$-A_{VS}$	↓	72	$R_L = 10$ kΩ, $V_{OUT} = \pm 15$ V	80	---	80	---	V/mV
↓	$+A_{VS}$	↓	73	$R_L = 2$ kΩ, $\pm V_{CC} = \pm 5$ Vdc, $V_{OUT} = \pm 2$ V			40	---	V/mV
↓	$-A_{VS}$	↓	74	$R_L = 2$ kΩ, $\pm V_{CC} = \pm 5$ Vdc, $V_{OUT} = \pm 2$ V			40	---	V/mV
↓	$+A_{VS}$	↓	75	$R_L = 10$ kΩ, $\pm V_{CC} = \pm 5$ Vdc, $V_{OUT} = \pm 2$ V	20	---	40	---	V/mV
↓	$-A_{VS}$	↓	76	$R_L = 10$ kΩ, $\pm V_{CC} = \pm 5$ Vdc, $V_{OUT} = \pm 2$ V	20	---	40	---	V/mV
5 $T_A = 125°C$	V_{OPP}	4004	77	$R_L = 10$ kΩ	32	---	34	---	V_{p-p}
↓	V_{OPP}	↓	78	$R_L = 2$ kΩ			32	---	V_{p-p}
↓	$+A_{VS}$	↓	79	$R_L = 2$ kΩ, $V_{OUT} = \pm 15$ V			40	---	V/mV
↓	$-A_{VS}$	↓	80	$R_L = 2$ kΩ, $V_{OUT} = \pm 15$ V			3	---	V/mV
↓	$+A_{VS}$	↓	81	$R_L = 10$ kΩ, $V_{OUT} = \pm 15$ V	40	---	40	---	V/mV
↓	$-A_{VS}$	↓	82	$R_L = 10$ kΩ, $V_{OUT} = \pm 15$ V	40	---	40	--	V/mV
↓	$+A_{VS}$	↓	83	$R_L = 2$ kΩ, $\pm V_{CC} = \pm 5$ Vdc, $V_{OUT} = \pm 2$ V			20	---	V/mV
↓	$-A_{VS}$	↓	84	$R_L = 2$ kΩ, $\pm V_{CC} = \pm 5$ Vdc, $V_{OUT} = \pm 2$ V			20	---	V/mV
↓	$+A_{VS}$	↓	85	$R_L = 10$ kΩ, $\pm V_{CC} = \pm 5$ Vdc, $V_{OUT} = \pm 2$ V	20	---	20	---	V/mV
↓	$-A_{VS}$	↓	86	$R_L = 10$ kΩ, $\pm V_{CC} = \pm 5$ Vdc, $V_{OUT} = \pm 2$ V	20	---	20	---	V/mV
6 $T_A = -55°C$	V_{OPP}	4004	87	$R_L = 10$ kΩ	32	---	34	---	V_{p-p}
↓	V_{OPP}	↓	88	$R_L = 2$ kΩ			32	---	V_{p-p}
↓	$+A_{VS}$	↓	89	$R_L = 2$ kΩ, $V_{OUT} = \pm 15$ V			20	---	V/mV
↓	$-A_{VS}$	↓	90	$R_L = 2$ kΩ, $V_{OUT} = \pm 15$ V			20	---	V/mV
↓	$+A_{VS}$	↓	91	$R_L = 10$ kΩ, $V_{OUT} = \pm 15$ V	40	---	20	---	V/mV
↓	$-A_{VS}$	↓	92	$R_L = 10$ kΩ, $V_{OUT} = \pm 15$ V	40	---	20	---	V/mV

TABLE B3. TEST SPECIFICATIONS FOR MIL-M-38510/101 (Continued)

Subgroup	Symbol	MIL-STD-883 method	Test no.	Conditions $\pm V_{CC} = \pm 20$ Vdc, FIG. B1. UNLESS OTHERWISE SPECIFIED.	-04, Limits Min	-04, Limits Max	-07 Limits Min	-07 Limits Max	Unit
6 $T_A = -55°$	$+A_{VS}$	4004	93	$R_L = 2$ kΩ, $\pm V_{CC} = \pm 5$ Vdc, $V_{OUT} = \pm 2$ V			4	---	V/mV
	$-A_{VS}$		94	$R_L = 2$ kΩ, $\pm V_{CC} = \pm 5$ Vdc, $V_{OUT} = \pm 2$ V			4	---	V/mV
	$+A_{VS}$		95	$R_L = 10$ kΩ, $\pm V_{CC} = \pm 5$ Vdc, $V_{OUT} = \pm 2$ V	20	---	4	---	V/mV
	$-A_{VS}$		96	$R_L = 10$ kΩ, $\pm V_{CC} = \pm 5$ Vdc, $V_{OUT} = \pm 2$ V	20	---	4	---	V/mV
7 $T_A = 25°C$	$TR(t_r)$		97	FIG. B2.	---	1000	--	40	ns
	$TR(OS)$		98	FIG. B2.	---	40	---	30	%
	SR(+)	4002	99	FIG. B2. $A_V = 1$, $V_{IN} = -5$ V to +5 V	0.1	---	75	---	V/µs
	SR(-)	4002	100	FIG. B2. $A_V = 1$, $V_{IN} = +5$ V to -5 V	0.1	---	50	---	V/µs
	$t_s(+)$		106	FIG. B2. $V_{IN} = -5$ V to +5 V			---	800	ns
	$t_s(-)$		107	FIG. B2. $V_{IN} = -5$ V to +5 V			---	800	ns
8	$TR(t_r)$		108	$T_A = 125°C$, FIG. B2.	---	1000	---	40	ns
	$TR(OS)$		109	$T_A = 125°C$, FIG. B2.	---	40	---	30	[illegible]
	SR(+)	4002	110	$T_A = 125°C$, $A_V = 1$, $V_{IN} = -5$ V to +5 V FIG. B2.	0.1	---	75	---	V/µs
	SR(-)	4002	111	$T_A = 125°C$, $A_V = 1$, $V_{IN} = +5$ V to -5 V FIG. B2.	0.1	---	50	---	V/µs
			112						
	$t_s(+)$		113	$T_A = 125°C$, FIG. B2.			---	1200	ns
	$t_s(-)$		114	$T_A = 125°C$, FIG. B2.			---	1200	ns
	$TR(t_r)$		115	$T_A = -55°C$, FIG. B2.	---	1000	---	40	ns
	$TR_{(OS)}$		116	$T_A = -55°C$, FIG. B2.	---	40	---	30	%
	SR(+)	4002	117	$T_A = -55°C$, Figure ., $A_V = 1$, $V_{IN} = -5$ V to +5 V FIG. B2.	0.08	---	75	---	V/µs

TABLE B3. TEST SPECIFICATIONS FOR MIL-M-38510/101 (continued)

Subgroup	Symbol	MIL-STD-883 method	Test no.	Conditions $\pm V_{CC} = \pm 20$ Vdc, FIG. B1, UNLESS OTHERWISE SPECIFIED.	-04, Limits		-07 Limits		Unit
					Min	Max	Min	Max	
8	SR(-)	4002	118	$T_A = -55°C$, figure 9, $A_V = 1$, $V_{IN} = +5$ V to -5 V FIG. B2.	0.08	---	50	---	V/µs
			119						
	$t_s(+)$		120	$T_A = -55°C$			---	1200	ns
	$t_s(-)$		121	$T_A = -55°C$			---	1200	ns

1/ V_{CM} is achieved by algebraically subtracting the common mode voltage from each supply and algebraically adding the common mode voltage to V (i.e., for $V_{CM} = -15$ V, $+V_{CC} = +35$ V, $-V_{CC} = -5$ V, V = -15 V).

5/ Due to the significant power dissipation and associated device heating, these tests shall always be the last tests performed in any given sequence, followed by operational verification (e.g., such tests as V_{OPP}, A_{VS}, TR, SR).

6/ Tests 28, 29, 30, 34, 35, 36, 49, 50, 51, 55, 56, and 57, which require a read and record measurement plus a calculation, may be omitted except when subgroups 2 and 3 are being accomplished for group A sampling inspection and groups B and C endpoint measurements.

8/ The five second minimum test duration for I_{OS} test shall apply only for group A sampling inspections and groups B and C endpoint tests. For final electrical test, test duration for I_{OS} may be reduced to be consistent with automated test procedures provided that the 5 second test limits are guaranteed.

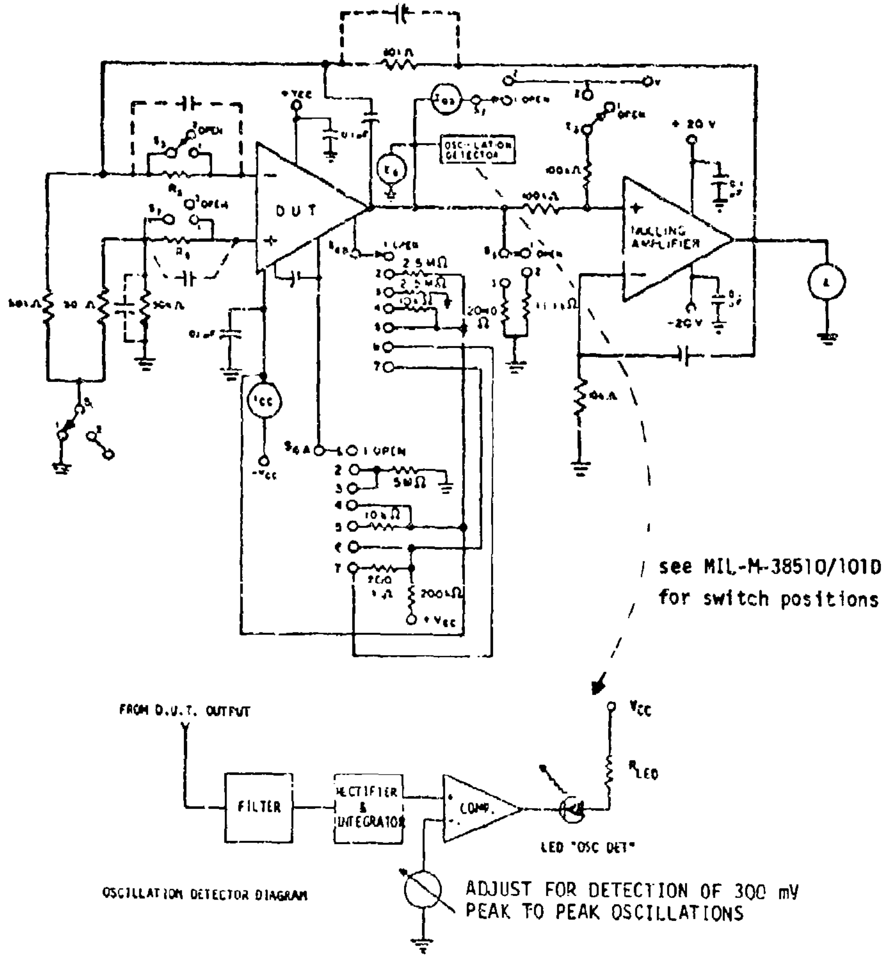
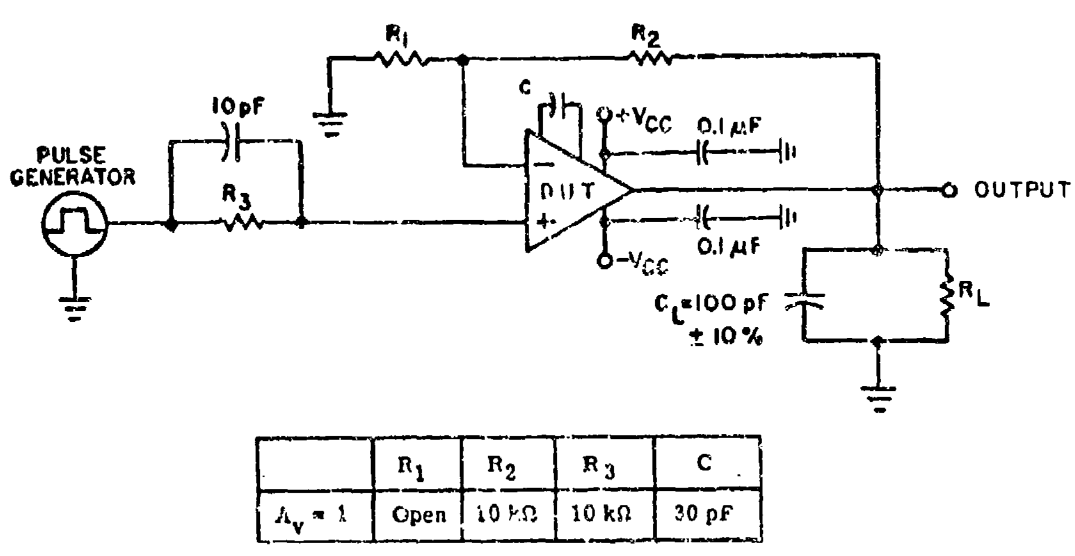


FIGURE B1. TEST CIRCUIT FOR STATIC AND DYNAMIC TEST

Device type 04



	R_1	R_2	R_3	C
$A_V = 1$	Open	10 kΩ	10 kΩ	30 pF

Device type 07

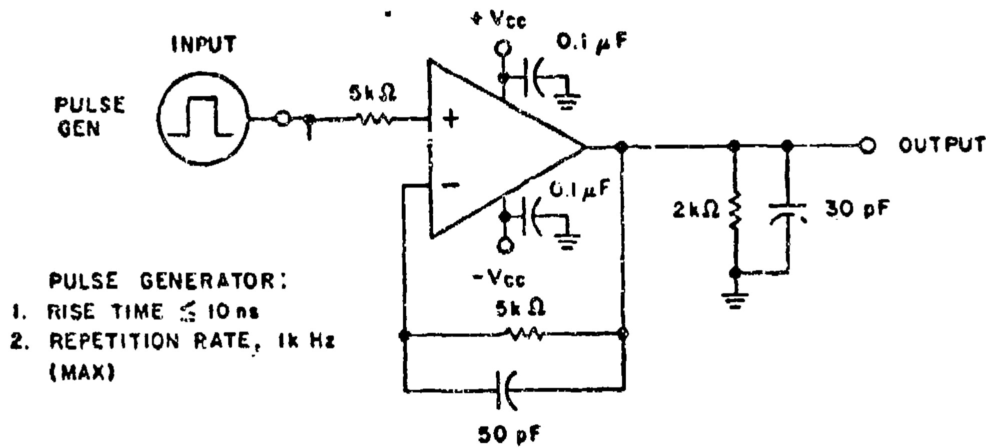


FIGURE B2. TRANSIENT RESPONSE TEST CIRCUIT

TABLE B4. INITIAL/FINAL AND INTERIM TESTS FOR MIL-M-38510/10201

PARAMETER	INITIAL/FINAL TEST #'S			INTERIM TEST #
	25°C	125°C	-55°C	25°C
V_{RLINE}	1, 2, 3	11	16	1, 2, 3
V_{RLOAD}	4, 5, 6	12	17	4, 5, 6
V_{REF}	7	13	18	7
I_{OS}	8	-	-	8
I_{SCO}	9	15	20	9

TABLE B5. CHARACTERIZATION TESTS FOR MIL-M-38510/10201

PARAMETER	CHARACTERIZATION TESTS TEST #'S		
	25°C	125°C	-55°C
T_C V_{OUT}	-	14	19
RIPPLE REJECTION	21,22	-	-
OUTPUT NOISE	23,24	-	-
LINE TRANSIENT RESPONSE	25	-	-
LOAD TRANSIENT RESPONSE	26	-	-

TABLE B6. TEST SPECIFICATIONS FOR MIL-M-38510/10201

* ALL TESTS REFER TO FIG. B2. UNLESS OTHERWISE SPECIFIED.

Subgroup	Symbol	Test	Conditions	Limits Min	Limits Max	Units
1 $T_A = +25°C$	V_{RLINE}	1	$V_{OUT} = 5$ V, $I_L = 1$ mA $V_{IN} = 12$ to 15 V	-0.10	0.10	% V_{OUT}
	V_{RLINE}	2	$V_{OUT} = 5$ V, $I_L = 1$ mA $V_{IN} = 9.5$ to 40 V	-0.3	0.3	% V_{OUT}
	V_{RLINE}	3	$V_{OUT} = 2$ V, $I_L = 1$ mA $V_{IN} = 12$ to 15 V	-0.2	0.2	% V_{OUT}
	V_{RLOAD}	4	$V_{OUT} = 5$ V, $V_{IN} = 12$ V $I_L = 1$ to 50 mA	-0.15	0.15	% V_{OUT}
	V_{RLOAD}	5	$V_{OUT} = 37$ V, $V_{IN} = 40$ V, $I_L = 1$ to 10 mA	0.5	0.5	% V_{OUT}
	V_{RLOAD}	6	$V_{OUT} = 7.5$ V, $V_{IN} = 10$ V $I_L = 6$ to 12 mA	-0.2	0.2	% V_{OUT}
	V_{REF}	7	$V_{IN} = 12$ V $I_{REF} = 1$ mA	6.95	7.35	V_{DC}
	I_{OS}	8	$R_{SC} = 10\,\Omega$, $R_L = 0$ $V_{OUT} = 5$ V, $V_{IN} = 12$ V 3/	55	85	mA
	I_{SCD}	9	$I_L = I_{REF} = 0$, $V_{IN} = 30$ V, $V_{OUT} = V_{REF}$	0.5	3.0	mA
2 $T_A = +125°C$	V_{RLINE}	11	$V_{OUT} = 5$ V, $I_L = 1$ mA $V_{IN} = 12$ to 15 V	-0.2	0.2	% V_{OUT}
	V_{RLOAD}	12	$V_{OUT} = 5$ V, $V_{IN} = 12$ V $I_L = 1$ to 50 mA	-0.4	0.4	% V_{OUT}
	V_{REF}	13	$I_{REF} = 1$ mA, $V_{IN} = 12$ V	6.90	7.40	V_{DC}
	TC_{VOUT}	14	$V_{OUT} = 5$ V, $V_{IN} = 12$ V $I_L = 1$ mA	-0.010	0.010	%/°C
	I_{SCD}	15	$I_L = I_{REF} = 0$, $V_{IN} = 30$ V, $V_{OUT} = V_{REF}$	0.5	2.4	mA
3 $T_A = -55°C$	V_{RLINE}	16	$V_{OUT} = 5$ V, $I_L = 1$ mA $V_{IN} = 12$ to 15 V	-0.3	0.3	% V_{OUT}
	V_{RLOAD}	17	$V_{OUT} = 5$ V, $V_{IN} = 12$ V $I_L = 1$ to 50 mA	-0.6	0.6	% V_{OUT}
	V_{REF}	18	$I_{REF} = 1$ mA, $V_{IN} = 12$ V	6.90	7.40	V_{DC}
	TC_{VOUT}	19	$V_{OUT} = 5$ V, $V_{IN} = 12$ V $I_L = 1$ mA	-0.015	0.015	%/°C
	I_{SCD}	20	$I_L = I_{REF} = 0$, $V_{IN} = 30$ V, $V_{OUT} = V_{REF}$	0.5	3.5	mA
4 $T_A = +25°C$	Ripple rej	21	$f = 10$ kHz, $C_{REF} = 0$, see figure B5.	64		dB
	Ripple rej	22	$f = 10$ kHz, $C_{REF} = 5\,\mu F$, see figure B5.	76		dB
	Output noise	[illegible]	BW = 100 Hz to 10 kHz, $C_{REF} = 0$, see figure B5.		60	μV_{rms}
	Output noise	24	BW = 100 Hz to 10 kHz, $C_{REF} = 5\,\mu F$, see figure B5.		7.0	μV_{rms}
	Line transient response	25	$V_{IN} = 12$ V, $V_{OUT} = 5$ V, $I_L = 1$ mA, $R_{SC} = 0\,\Omega$, $\Delta V_{IN} = 3$ V, see figure B4.	0	[illegible]	mV/V
	Load transient response	26	$V_{IN} = 12$ V, $V_{OUT} = 5$ V, $I_L = 40$ mA, $R_{SC} = 0\,\Omega$, $\Delta I_L = 10$ mA, see figure B4.	-1.5	0	mV/mA

3/ To eliminate heating, test must be made in less than a 10 mS duty cycle of less than 5%. V_{OUT} is the nominal output voltage prior to application of short circuit.

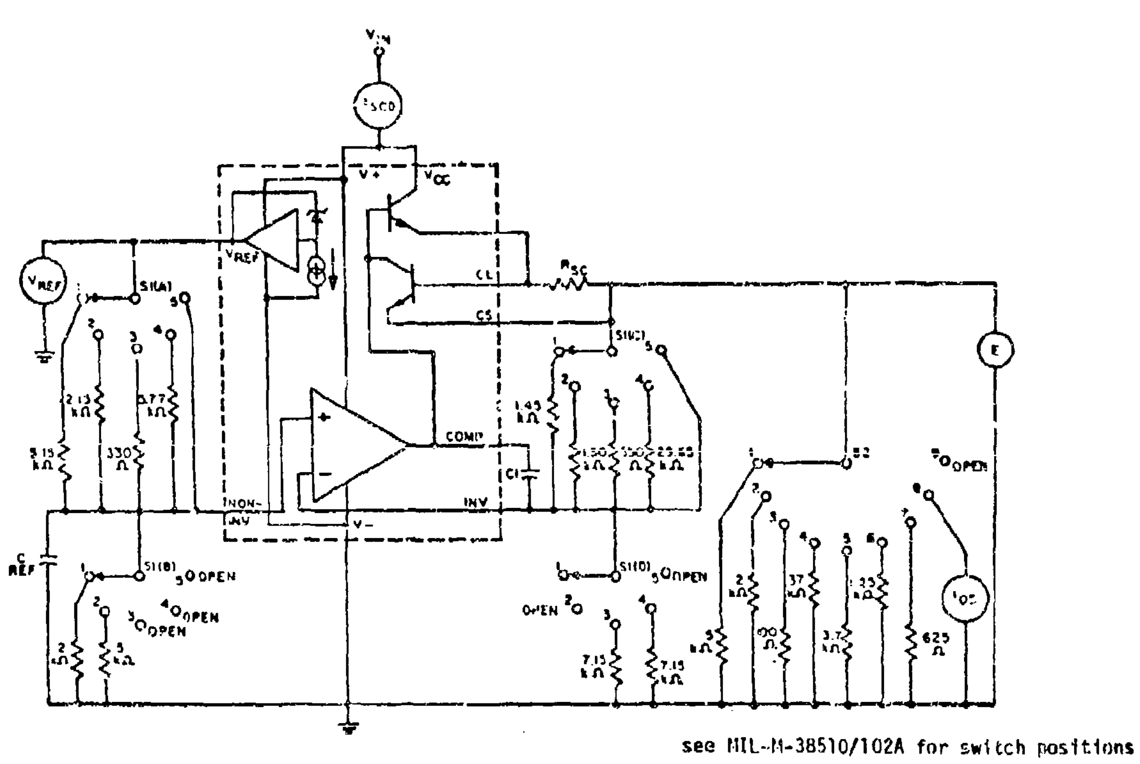
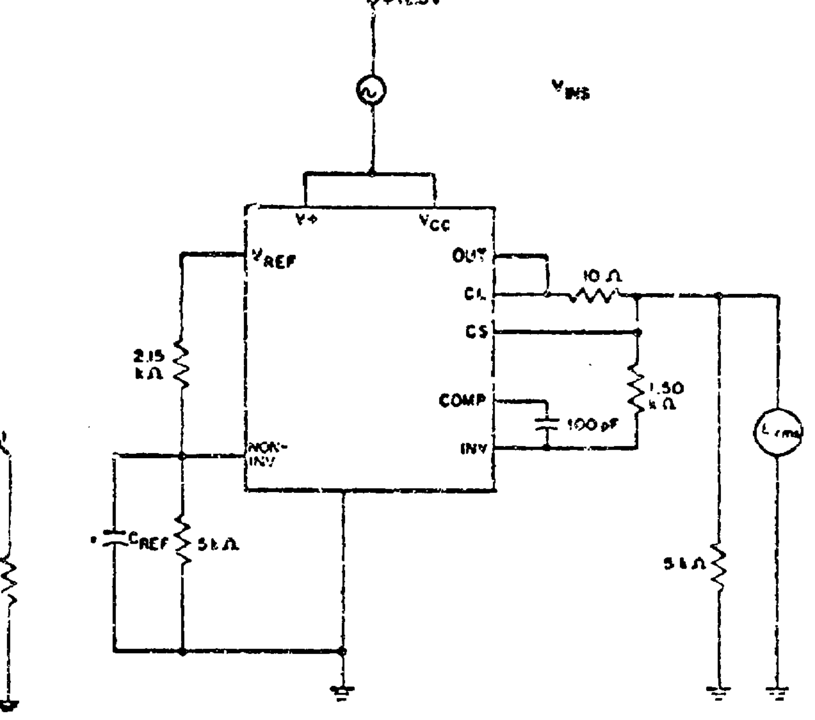


FIGURE B3. TEST CIRCUIT FOR STATIC AND DYNAMIC TESTS

NOTES:
1. For line transient response, S1 in position 1
   Pulse 1 equals 3 V high, 25 µsec wide, 3% duty cycle,
   $t_{TLH} = t_{THL} = 500$ ns.
2. For load transient response, S1 in position 2
   Pulse 1 = 0
   Pulse 2 equals -750 mV, 25 µsec wide, 3% duty cycle,
   $t_{TLH} = t_{THL} = 500$ ns.

FIGURE B4. TRANSIENT RESPONSE TEST CIRCUIT



NOTES:
1. For ripple rejection
   V_{INS} = 2 Vrms, 10 kHz

$$\text{RIPPLE REJECTION (db)} = 20 \log \frac{V_{INS}}{E_{rms}}$$

2. For noise
   V_{INS} = 0 Vrms
   E_{rms} is over a band width of 100 Hz to 10 kHz = noise µVrms.
3. C_{REF} is as specified in table 32-1

FIGURE B5. RIPPLE REJECTION AND NOISE TEST CIRCUIT

TABLE 87. INITIAL/FINAL AND INTERIM TESTS FOR MIL-M-38510/10304

PARAMETER	INITIAL/FINAL TEST #'S		INTERIM TEST #'S
	25°C	125°C	
V_{IO}	1, 2, 3, 4, 5, 6, 7,	30, 31, 32, 33, 34 35, 36	1, 2, 3, 4, 5, 6, 7,
I_{IO}	8, 9, 10, 11	38, 39, 40, 41	8, 9, 10, 11
I_{IB}	12, 13, 14	43, 44, 45	12, 13, 14
P_D	15	46	15
I_O	16	47	16
I_G	17	48	17
I_{I1}	18	49	18
I_{I2}	19	50	19
+Icc	20	51	20
-Icc	21	52	21
I_{OS}	22	53	22
$V_{IO(ADJ+)}$	23	54	23
$V_{IO(ADJ-)}$	24	55	24
CMRR	25	56	25
V_{OL}	26, 27, 28, 29	57, 58, 59, 60	26, 27, 28, 29
A_{VC}	92	94	92

TABLE B8. CHARACTERIZATION TESTS FOR MIL-M-38510/10304

PARAMETER	CHARACTERIZATION TEST #'S		
	25°C	125°C	-55°C
t_{RLHC}	98	98	98
t_{RHLC}	99	99	99
t_{RLHE}	100	100	100
t_{RHLE}	101	101	101

TABLE B9. TEST SPECIFICATIONS FOR MIL-M-38510/103

USE FIGURE B6, UNLESS OTHERWISE NOTED

Subgroup	Symbol	Test No.	Conditions	Limits Min	Limits Max	Unit	
T_A = 25°C [1]	V_{IO}	1	R_S = 50Ω, V_{IC} = 0, ±V_{CC} = ±15V	-4	+4	mV	*
		2	R_S = 50Ω, V_{IC} = -13.5V; ± V_{CC} = ±15V	-4	+4	mV	*
		3	R_S = 50Ω, V_{IC} = +12V; ± V_{CC} = ±15V	-4	+4	mV	*
		4	R_S = 50Ω, V_{IC} = 0, ±V_{CC} = ±2.5V	-4	+4	mV	*
		5, 6, 7	Repeat tests 1, 2, and 3 with BAL/STB and BAL connected to +V_{CC}	-5	+5	mV	*
	I_{IO}	8	R_S = 100 kΩ, V_{IC} = 0, ±V_{CC} = ±15V	-10	+10	nA	
		9	R_S = 100 kΩ, V_{IC} = -13.5V; ± V_{CC} = ±15V	-10	+10	nA	*
		10	R_S = 100 kΩ, V_{IC} = +12V; ± V_{CC} = ±15V	-10	+10	nA	*
		11	Repeat test 8 with BAL/STB and BAL connected to +V_{CC}	-25.0	+25.0	nA	*
	I_{IB}	12	±V_{CC} = ±15V, V_{IC} = 0	-100	+ 0.1	nA	*
		13	±V_{CC} = ±15V, V_{IC} = -13.5V	-150	+ 0.1	nA	*
		14	±V_{CC} = ±15V, V_{IC} = 17V	-150	+ 0.1	nA	*
	P_D	15	P_D = 15 (/+I_{CC}/+/-I_{CC}/)	30	270	mW	*
	I_O	16	±V_{CC} = ±18V, V_{ID} = 5 mV	0	500	nA	*
	I_G	17	±V_{CC} = ±18V, V_{ID} = 5 mV	-10000	0	nA	*
	I_{I1}	18	±V_{CC} = ±18V	0	100	nA	*
	I_{I2}	19	±V_{CC} = ±18V	0	100	nA	*
	+I_{CC}	20	±V_{CC} = ±15V	0.5	5.0	mA	*
T_A = 25°C [1]	-I_{CC}	21	±V_{CC} = ±15V	-4.0	-0.5	mA	
	I_{OS}	22	10 ms maximum test duration, ±V_{CC} = ±15V	70	200	mA	*
	$V_{IO(ADJ)+}$	23	±V_{CC} = ±15V, V_{IC} = 0	4.0	-	mV	*
	$V_{IO(ADJ)-}$	24	±V_{CC} = ±15V, V_{IC} = 0	4.0	-	mV	*
	CMR	25	±V_{CC} = ±15V, V_{IC} = +12V and -13.5V	80		dB	*
	V_{OL}	26	+V_{CC} = 4.5V, -V_{CC} = 0, V_{IN} = 0.5V, V_{ID} = 6 mV	0	400	mV	
		27	+V_{CC} = 4.5V, -V_{CC} = 0, V_{IN} = 3.0V; V_{ID} = 6 mV	0	400	mV	
		28	±V_{CC} = ±15V, V_{IN} = 12V; V_{IO} = 7 mV	0	1,500	mV	*
		29	±V_{CC} = ±15V, V_{IN} = -13V; V_{ID} = 7 mV	0	1,500	mV	*
T_A = +125°C [2]	V_{IO}	30	R_S = 50Ω, V_{IC} = 0, ±V_{CC} = ±15V	-3	-3	mV	
		31	R_S = 50Ω, V_{IC} = -13.5V; ± V_{CC} = ±15V	-5.5	+5.5	mV	*
		32	R_S = 50Ω, V_{IC} = +12V; ± V_{CC} = ±15V	-5.5	+5.5	mV	*
		33	R_S = 50Ω, V_{IC} = 0, ±V_{CC} = ±2.5V	-5.5	+5.5	mV	*
		34, 35, 36	Repeat tests 31, 32, 33 with BAL/STB and BAL connected to +V_{CC}	-5.5	+5.5	mV	*
	$\Delta V_{IO}/\Delta T$	37	$\frac{\Delta V_{IO}}{\Delta T} = \frac{V_{IO}\text{(test 41)} - V_{IO}\text{(test 1)}}{100°C}$	-25	+25	μV/°C	*
	I_{IO}	38	R_S = 100 kΩ, V_{IC} = 0, ±V_{CC} = ±15V	-10.0	+10.0	nA	*
		39	R_S = 100 kΩ, V_{IC} = -13.5V; ± V_{CC} = ±15V	-10.0	+10.0	nA	*
		40	R_S = 100 kΩ, V_{IC} = +12V; ± V_{CC} = ±15V	-10.0	+10.0	nA	*
		41	Repeat test 39 with BAL/STB and BAL connected to +V_{CC}	-50.0	+50.0	nA	

* Indicates changes proposed for MIL-M-38510/10304 are shown.

TABLE B10. TEST SPECIFICATIONS FOR MIL-M-38510/103

USE FIGURE B6. UNLESS OTHERWISE NOTED

Subgroup	Symbol	Test No.	Conditions	Limits Min	Limits Max	Unit	
2 $T_A = +125°C$	$\Delta I_{IO}/\Delta T$	42	$\frac{\Delta I_{IO}}{\Delta T} = \frac{I_{IO}\text{(test 49)} - I_{IO}\text{(test 8)}}{100°C}$	-700	+700	µA/°C	*
	I_{IB}	43	$\pm V_{CC} = \pm 15V$, $V_{IC} = 0$	-100	+0.1	nA	*
	↓	44	$\pm V_{CC} = \pm 15V$, $V_{IC} = -13.5V$	-100	+0.1	nA	*
	↓	45	$\pm V_{CC} = \pm 15V$, $V_{IC} = +12V$	-100	+0.1	nA	*
	P_D	46	$P_D = 15(/+I_{CC}/+/-I_{CC}/)$	30	210	mW	*
	I_O	47	$\pm V_{CC} = \pm 18V$, $V_{ID} = 5$ mV	0	500	nA	*
	I_G	48	$\pm V_{CC} = \pm 18V$, $V_{ID} = 5$ mV	-100	0	uA	
	I_{I1}	49	$\pm V_{CC} = \pm 18V$	0	500	nA	
	I_{I2}	50	$\pm V_{CC} = \pm 18V$	0	500	nA	
	$+I_{CC}$	51	$\pm V_{CC} = \pm 15V$	0.5	4.0	mA	*
	$-I_{CC}$	52	$\pm V_{CC} = \pm 15V$	-3.0	-0.5	mA	*
	I_{OS}	53	10 ms maximum test duration, $\pm V_{CC} = \pm 15V$	50	150	mA	*
	$V_{IO(ADJ)+}$	54	$\pm V_{CC} = \pm 15V$; $V_{IC} = 0$	4.0		mV	*
	$V_{IO(ADJ)-}$	55	$\pm V_{CC} = \pm 15V$; $V_{IC} = 0$	4.0		mV	*
	CMR	56	$\pm V_{CC} = \pm 15V$; $V_{IC} = +15V$ and $-14.5V$	75		dB	*
	V_{OL}	57	$+V_{CC} = 4.5V$, $-V_{CC} = 0$, $V_{IN} = 0.5V$, $V_{ID} = 8$ mV	0	400	mV	
	↓	58	$+V_{CC} = 4.5V$; $-V_{CC} = 0$, $V_{IN} = 4.0V$, $V_{ID} = 8$ mV	0	400	mV	
	↓	59	$\pm V_{CC} = \pm 15V$, $V_{IN} = 13V$, $V_{ID} = 5$ mV	0	1,500	mV	
↓	↓	60	$\pm V_{CC} = \pm 15V$; $V_{IN} = -14V$, $V_{ID} = 5$ mV	0	1,500	mV	
		61	$R_S = 50\Omega$, $V_{IC} = 0$; $\pm V_{CC} = \pm 15V$	-3	+3	mV	

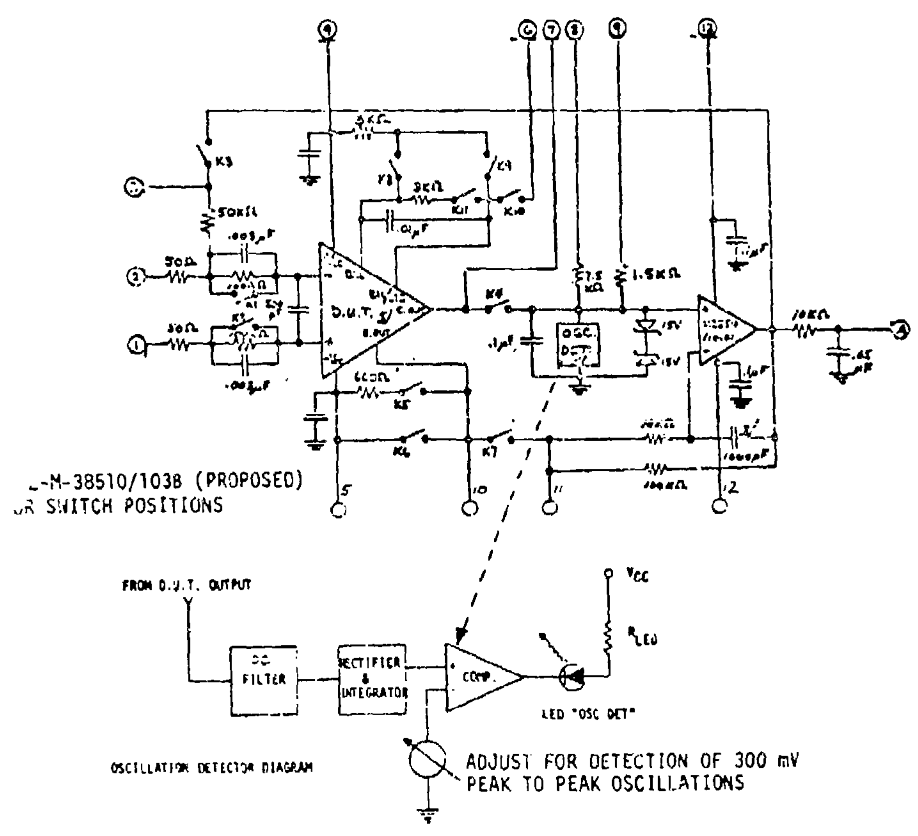
*** Indicates changes proposed for MIL-M-38510/10304 are shown.**

TABLE B11. TEST SPECIFICATIONS FOR MIL-M-38510/103

USE FIGURE B6. UNLESS OTHERWISE NOTED

Subgroup	Symbol	Test No.	Conditions	Limits Min	Limits Max	Unit	
4 T_A = 25°C	A_{VC}	93	35V through a 1 kΩ load	150		V/mV	*
5 T_A = +125°C	A_{VC}	94	35V through a 1 kΩ load	35		V/mV	*
							*
7 T_A = 25°C	t_{PLHC}	98	V_{OD} = 5 mV, ΔV_{IN} = 100 mV SEE FIGURE B7.		300	ns	
	t_{PHLC}	99	V_{OD} = 5 mV; ΔV_{IN} = 100 mV, SEE FIGURE B7.		300	ns	
	t_{PLHE}	100	V_{OD} = 5 mV; ΔV_{IN} = 100 mV, SEE FIGURE B8.		800	ns	
	t_{PHLE}	101	V_{OD} = 5 mV; ΔV_{IN} = 100 mV, SEE FIGURE B8.		1,300	ns	
8 T_A = +125°C	t_{PLHC}	98	V_{OD} = 5 mV, ΔV_{IN} = 100 mV SEE FIGURE B7.		500	ns	*
	t_{PHLC}	99	V_{OD} = 5 mV, ΔV_{IN} = 100 mV, SEE FIGURE B7.		450	ns	*
	t_{PLHE}	100	V_{OD} = 5 mV, ΔV_{IN} = 100 mV, SEE FIGURE B8.		2,500	ns	*
	t_{PHLE}	101	V_{OD} = 5 mV; ΔV_{IN} = 100 mV, SEE FIGURE B8.		3,500	ns	*
9 T_A = -55°C	t_{PLHC}	98	V_{OD} = 5 mV; ΔV_{IN} = 100 mV SEE FIGURE B7.		300	ns	
	t_{PHLC}	99	V_{OD} = 5 mV; ΔV_{IN} = 100 mV, SEE FIGURE B7.		300	ns	
	t_{PLHE}	100	V_{OD} = 5 mV; ΔV_{IN} = 100 mV. SEE FIGURE B8.		800	ns	
	t_{PHLE}	101	V_{OD} = 5 mV; ΔV_{IN} = 100 mV, SEE FIGURE B8.		1,300	ns	

* Indicates changes proposed for MIL-M-38510/10304 are shown.



FIGURF B6. TEST CIRCUIT FOR MIL-M-38510/10304

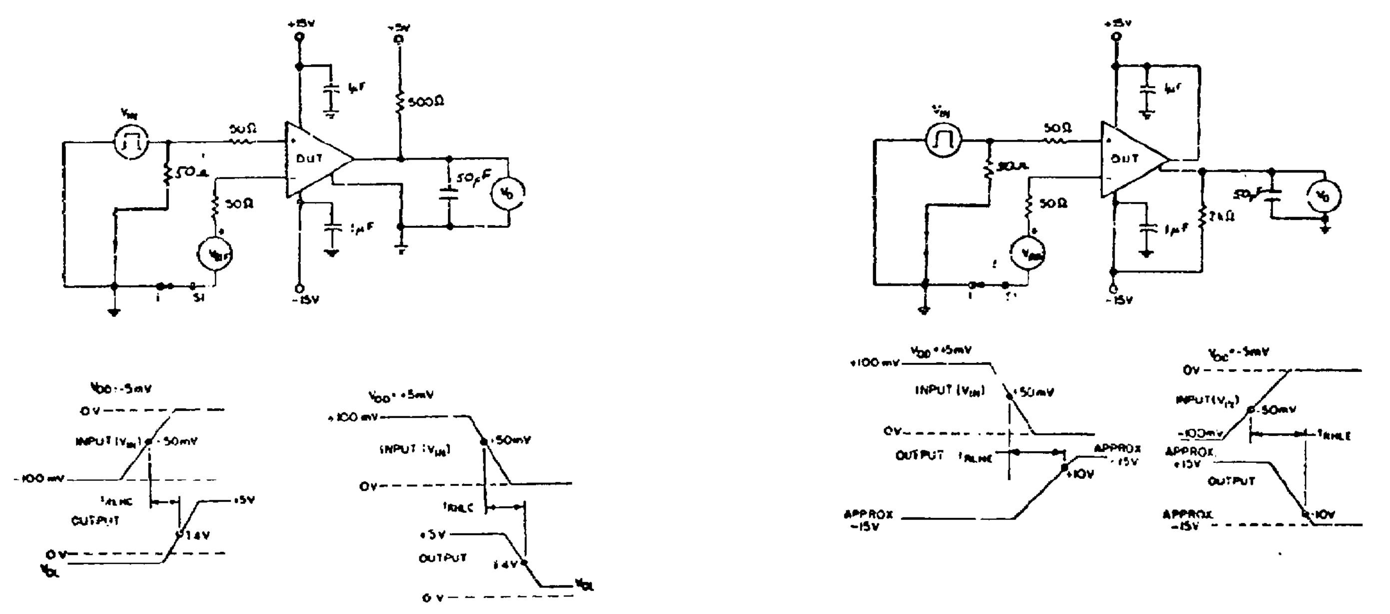


FIGURE B7. RESPONSE TIME TEST CIRCUIT AND WAVEFORMS FOR COLLECTOR OUTPUT. (DEVICE TYPE 04)

FIGURE B8. RESPONSE TIME TEST CIRCUIT AND WAVEFORMS FOR EMITTER OUTPUT. (DEVICE TYPE 04)

TABLE B12. INITIAL/FINAL AND INTERIM TESTS FOR MIL-M-38510/10701

PARAMETER	INITIAL FINAL TEST #'S			INTERIM TEST #'S
	25°C	125°C	-55°C	
V_{RLINE}	6	21	37	6
V_{RLOAD}	7	22	38	7
V_{OUT}	1, 2, 4	16, 17, 19	32, 33, 35	1, 2, 4
I_{SCD}	9, 10, 11	25, 26, 27	41, 42, 43	9, 10, 11
ΔI_{SCD}	12, 13	28, 29	44, 45	12, 13
I_{OS}	14	30	46	14
V_{START}	15	31	47	15

This table refers to tests specified in this appendix. These tests are in accordance with the proposed changes in MIL-M-38510/10701.

TABLE B13. CHARACTERIZATION TESTS FOR MIL-M-38510/10701

PARAMETER	CHARACTERIZATION TEST #'S		
	25°C	125°C	-55°C
$\frac{\Delta V_{OUT}}{\Delta T}$	-	24	40
$\frac{\Delta V_{IN}}{\Delta V_{OUT}}$	48	52	55
N_O	49	-	-
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	50	53	56
$\frac{\Delta V_{OUT}}{\Delta I_{IL}}$	51	54	57
I_{CL}	58	-	-
$T_{J(SH)}$	-	59	-

This table refers to tests specified in this appendix. These tests are in accordance with the proposed changes in MIL-M-38510/10701.

TABLE B14. MIL-M-38510/10701 SPECIFIED TESTS/LIMITS

SUBGROUP	SYMBOL	TEST NO	CONDITIONS (FIGURE B9. UNLESS OTHERWISE SPECIFIED) INPUT VOLTAGE	LOAD CURRENT	LIMITS MIN	MAX	UNITS
1 $T_A = 25°C$	V_{OUT}	1	$V_{IN} = 7V$	$I_L = -5mA$	4.80	5.20	V *
		2	$V_{IN} = 10V$	$I_L = -0.5A$	↓	↓	↓
		4	$V_{IN} = 35V$	$I_L = -50mA$			
	V_{RLINE}	6	$7V \leq V_{IN} \leq 25V$	$I_L = -5mA$	-20	+20	mV *
	V_{RLOAD}	7	$V_{IN} = 10V$	$-0.5A \leq I_L \leq -5mA$	-50	+50	mV *
	I_{SCD}	9	$V_{IN} = 7V$	$I_L = -5mA$	-10.0	0	mA *
		10	$V_{IN} = 25V$	$I_L = -5mA$	↓	↓	↓
		11	$V_{IN} = 7V$	$I_L = -0.5A$			
	ΔI_{SCD} (LINE)	12	$7V \leq V_{IN} \leq 25V$	$I_L = -5mA$	-0.8	+0.8	mA
	ΔI_{SCD} (LOAD)	13	$V_{IN} = 7V$	$-0.5A \leq I_L \leq -5mA$	-2.0	0	mA
	I_{OS}	14	$V_{IN} = 10V.$		-0.7	-0.1	A *
↓	V_{START}	15	SEE FIG B11.		-	9.0	V
2 $T_A = 125°C$	V_{OUT}	16	$V_{IN} = 7V$	$I_L = -5mA$	4.75	5.25	V *
		17	$V_{IN} = 10V$	$I_L = -0.5A$	4.50	↓	↓
		19	$V_{IN} = 35V$	$I_L = -50mA$	4.75		
	V_{RLINE}	21	$7V \leq V_{IN} \leq 25V$	$I_L = -5mA$	-25	+25	mV *
	V_{RLOAD}	22	$V_{IN} = 10V$	$-0.5A \leq I_L \leq -5mA$	-500	+500	mV *
↓	$\frac{\Delta V_{OUT}}{\Delta T}$	24	$V_{IN} = 7V$	$I_L = -5mA$	-1.25	+1.25	mV/°C *

* INDICATES TEST (OR TEST LIMIT) CHANGES FROM EXISTING MIL-M-38510/10701 SHEET, AND SHOWS TESTS (OR TEST LIMITS) IN ACCORDANCE TO THE NEW PROPOSED SPECIFICATIONS.

TABLE B14. MIL-M-38510/10701 SPECIFIED TESTS/LIMITS (continued)

SUBGROUP	SYMBOL	TEST NO	CONDITIONS (FIGURE B9.), UNLESS OTHERWISE SPECIFIED) INPUT VOLTAGE	LOAD CURRENT	LIMITS MIN	MAX	UNITS
T_A = 125°C [2]	I_{SCD}	25	V_{IN} = 7V	I_L = -5mA	-10.0	0	mA
↓		26	V_{IN} = 25V	I_L = -5mA	↓	↓	↓
↓		27	V_{IN} = 7V	I_L = -0.5A	↓	↓	↓
↓	ΔI_{SCD} (LINE)	28	$7V \leq V_{IN} \leq 25V$	I_L = -5mA	-0.8	0	mA
↓	ΔI_{SCD} (LOAD)	29	V_{IN} = 7V	$-0.5A \leq I_L \leq -5mA$	-0.5	0	mA
↓	I_{OS}	30	V_{IN} = 10V		-0.7	-0.1	A
↓	V_{START}	31	SEE FIG B11.		-	9.0	V
T_A = -55°C [3]	V_{OUT}	32	V_{IN} = 7V	I_L = -5mA	4.75	5.25	V *
↓		33	V_{IN} = 10V	I_L = -0.5A	↓	↓	↓
↓		35	V_{IN} = 35V	I_L = -50mA	↓	↓	↓
↓	V_{RLINE}	37	$7V \leq V_{IN} \leq 25V$	I_L = -5mA	-25	+25	mV *
↓	V_{RLOAD}	38	V_{IN} = 10V	$-0.5A \leq I_L \leq -5mA$	-75	+75	mV *
↓	$\frac{\Delta V_{OUT}}{\Delta T}$	40	V_{IN} = 7V	I_L = -5mA	-1.25	+1.25	mV/°C*
↓	I_{SCD}	41	V_{IN} = 7V	I_L = -5mA	-10.0	0	mA *
↓		42	V_{IN} = 25V	I_L = -5mA	↓	↓	↓
↓		43	V_{IN} = 7V	-0.5A = I_L	↓	↓	↓
↓	ΔI_{SCD} LINE	44	$7V \leq V_{IN} \leq 25V$	I_L = -5mA	-0.8	0	mA
↓	ΔI_{SCD} (LOAD)	45	V_{IN} = 7V	$-0.5 \leq I_L \leq -5mA$	-0.5	0	mA
↓	I_{OS}	46	V_{IN} = 10V		-0.7	-0.1	A *
↓	V_{START}	47	SEE FIG B11.		-	0	V

* Indicates test (or test limit) change, from existing MIL-M-38510/10701 sheets, and shows tests (or test limits) in accordance with the new proposed specifications.

TABLE B14. MIL-M-38510/10701 SPECIFIED TESTS/LIMITS (continued)

SUBGROUP	SYMBOL	TEST #	CONDITIONS (V_{IN} = 10V)	NOTES	LIMITS MIN	LIMITS MAX	UNITS
4 T_A = 25°C	$\Delta V_{IN} / \Delta V_{OUT}$	48	I_L = -50mA	See Figure B10. ΔV_{IN} = 1Vrms BW=10Hz to 100KHz	60	-	dB
	N_0	49	I_L = -50mA	See Figure B10. BW = 10Hz to 100KHz	-	120	µV *
	$\Delta V_{OUT} / \Delta V_{IN}$	50	I_L = -1mA	See Figure B12. ΔV_{IN} = 3V	-	4.0	mV/V *
	$\Delta V_{OUT} / \Delta I_L$	51	I_L = -40mA	See Figure B10. ΔI_L = -10mA	-	1.0	mV/mA *
5 T_A = 125°C	$\Delta V_{IN} / \Delta V_{OUT}$	52	I_L = -50mA	See Figure B12. ΔV_{IN} = 1Vrms BW=10Hz to 100KHz	60	-	dB
	$\Delta V_{OUT} / \Delta V_{IN}$	53	I_L = -1mA	See Figure B12. ΔV_{IN} = 3V	-	4.0	mV/V *
	$\Delta V_{OUT} / \Delta I_L$	54	I_L = -40mA	See Figure B10. ΔI_L = -10mA	-	1.0	mV/mA *
6 T_A = -55°C	$\Delta V_{IN} / \Delta V_{OUT}$	55	I_L = -50mA	See Figure B10. ΔV_{IN} = 1Vrms BW=10Hz to 100KHz	60	-	dB
	$\Delta V_{OUT} / \Delta V_{IN}$	56	I_L = -1mA	See Figure B12. ΔV_{IN} = 3V	-	4.0	mV/V *
	$\Delta V_{OUT} / \Delta V_{IL}$	57	I_L = -40mA	See Figure B12. ΔI_L = -10mA	-	1.0	mV/mA *
7 T_A = 25°C	I_{CL}	58		See Figure B13.	-1.0	-0.7	A **
8 T_A = 125°C	$T_{J(SH)}$	59	I_L = -5mA	See Figure B14.	165	185	°C **

* Indicates test (or test limit) changes from existing MIL-M-38510/10701 sheets, and shows tests (or test limits) in accordance with the new proposed specifications.

** Indicates new test.

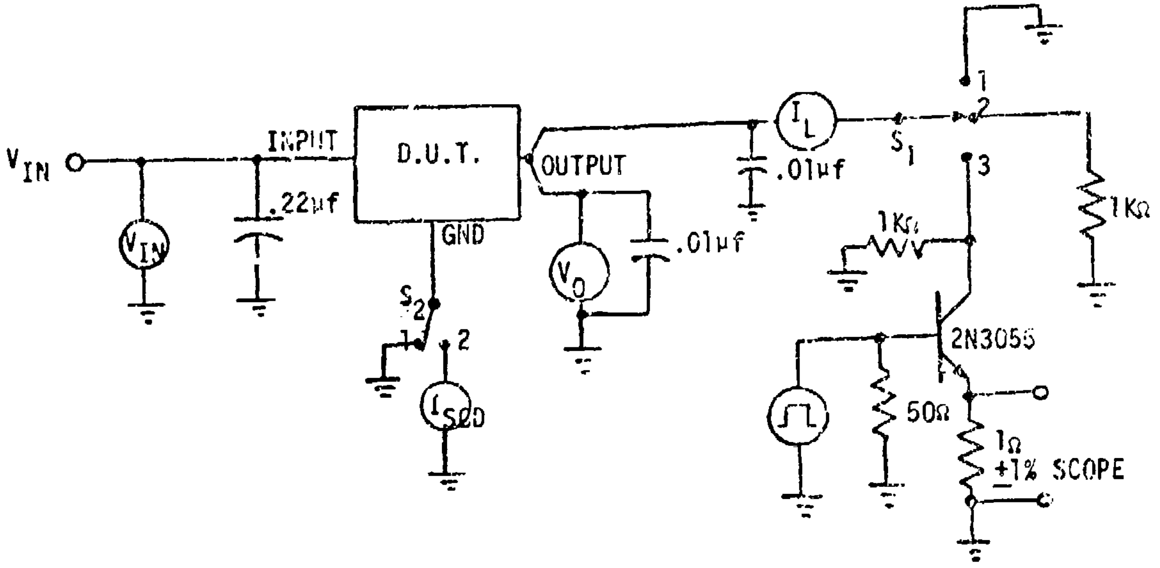


FIGURE B9. TEST CIRCUIT FOR MIL-M-38510/107

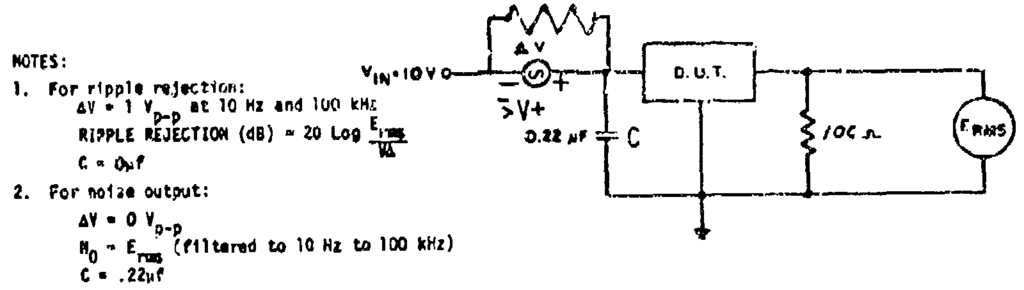
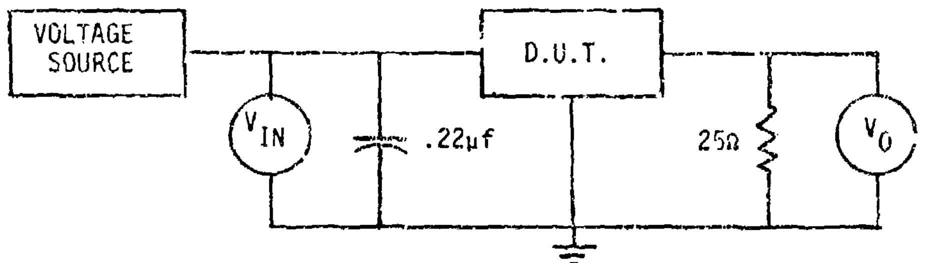


FIGURE B10. RIPPLE REJECTION & NOISE CIRCUIT



Voltage source shall be a variable power supply capable of producing the following input waveform. Device shall turn on at $V_{IN} \leq 9$ V and shall remain on when the input is returned to 7 V.

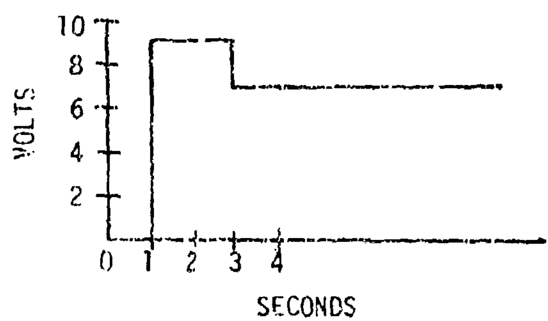
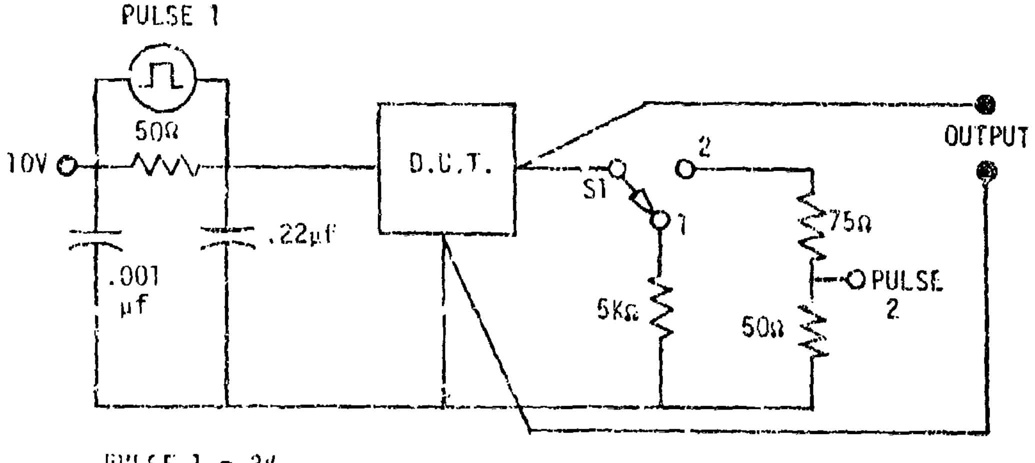


FIGURE B11. START-UP INPUT VOLTAGE TEST CIRCUIT



PULSE 1 = 3V

PULSE 2 = -750mV

FIGURE B12. TRANSIENT RESPONSE TEST CIRCUIT

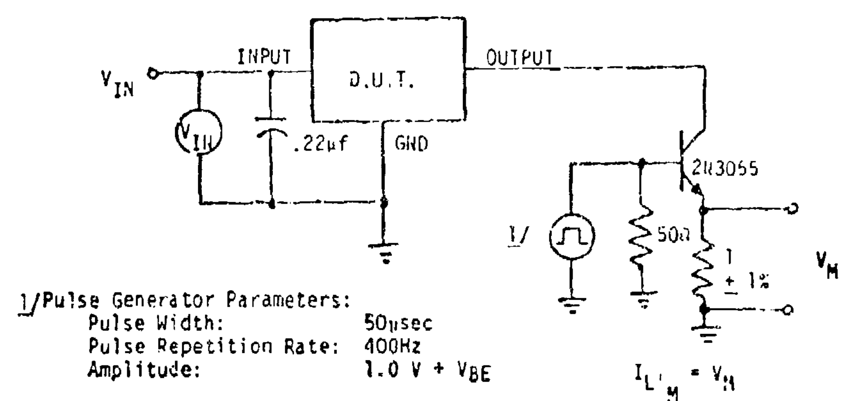
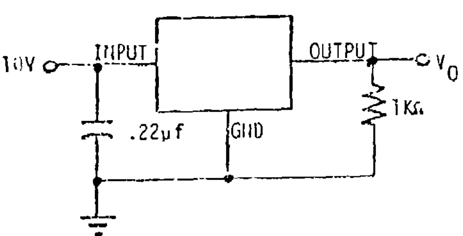


FIGURE B13. CURRENT LIMITING TEST CIRCUIT



The temperature chamber shall be stabilized at $T_A = 165°C$. The temperature shall be increased to $T_A = 185°C$ over a 10 minute period and allowed to stabilize at $T_A = 185°C$.

Accept/Reject Criteria: At $T_A = 165°C$; V_O must be ≥ 4.6 V.
At $T_A = 185°C$, all devices must be shut down; $V_O < 1.0$ V.

FIGURE B14. THERMAL SHUTDOWN TEST CIRCUIT

APPENDIX C
PARAMETER CHARACTERIZATION

APPENDIX C
PARAMETER CHARACTERIZATION

Electrical parameter measurements were performed initially on all devices, and also during and after life tests.

The final electrical parameter measurements were compared to the initial results to detect any shift in parameter values. These results are shown in Tables C1 through C10.

An examination of the data was made by comparing manufacturer to manufacturer differences in initial data and comparing initial and final life test parametric data of each device type. This comparison of initial/final parametric data of each device type revealed only minor shifts in the parametric values. Where apparent differences in parameter values were noted, the control data also shifted indicating test set drift or variations due to test set recalibration. Also, comparison of the initial data to cells which have only a few survivors is not completely valid. In those cases, individual device parameter values were examined at each test time, and no major shift in values was noted. Differences in the gain parameters ($\pm A_{VS}$) were noted in the manufacturer to manufacturer comparison of MIL-M-38510/10104, MIL-M-38510/10107, and MIL-M-38510/10304 device types. A study of the transfer plots for these devices showed that the curves were nonlinear and that the two-point dc electrical measurements are not a valid indication of open loop gain. A further discussion of the open loop gain differences can be found in Appendix E.

TABLE C1. MANUFACTURER A MIL-M-38510/10104 25°C PARAMETER CHARACTERIZATION

Parameter	Test No.	Limits		Initial Data		FINAL ACCELERATED LIFE TEST DATA: 225°C 4000 HRS. NO. OF PARTS - 12		200°C 4000 HRS. NO. OF PARTS - 19		175°C 4000 HRS. NO. OF PARTS - 23		Units
		MIN	MAX	Mean	Sigma	Mean	Sigma	Mean	Sigma	Mean	Sigma	
V_{IO}	△1	-0.5	+0.5	-0.003	0.137	-0.132	0.095	0.003	0.125	-0.022	0.158	mV
$+A_{VS}$	69	80	---	865.8	1568	3745.142	5904.629	2453.999	4766.953	496.480	194.350	V/mV
$-A_{VS}$	70	80	---	203.5	87.26	166.405	79.274	239.161	79.717	142.351	45.134	V/mV
$+A_{VS}$	71	20	---	252.6	255.2	269.178	220.429	3085.472	11724.695	203.711	136.622	V/mV
$-A_{VS}$	72	20	---	191.4	47.95	134.7[illegible]1	56.092	144.252	39.944	124.384	43.304	V/mV
I_{IO}	△2	-0.2	+0.2	-0.007	0.026	0.004	0.018	-0.013	0.017	-0.009	0.029	nA
I_{IB}	△3	-0.1	2.0	1.056	0.305	0.979	0.147	0.957	0.140	1.099	0.236	nA
$-I_{IB}$	△4	-0.1	2.0	1.063	0.302	0.980	0.151	0.970	0.140	1.105	0.246	nA
+PSRR	17	0	16	2.438	0.903	-2.525	0.944	-2.612	0.868	-2.445	1.765	µV/V
-PSRR	18	0	16	1.118	2.078	2.304	1.638	-0.839	2.583	2.680	2.352	µV/V
CMRR	19	96	---	121.124	7.240	119.923	5.018	125.291	8.081	118.996	4.008	dB
$+I_{OS}$	22	-15	-2.0	-9.033	0.627	-9.345	0.208	-8.749	0.428	-9.226	0.473	mA
$-I_{OS}$	23	2	20	12.289	4.302	13.835	0.856	8.647	3.064	14.046	2.425	mA
P_D	24	2	24	13.958	2.584	14.462	1.168	12.498	2.099	14.825	0.861	mW
V_{OP+}	67	16	---	19.167	0.078	19.459	0.016	19.439	0.035	19.441	0.091	Vp
V_{OP-}	68	--	16	18.914	0.064	-18.732	0.027	-18.706	0.044	-18.710	0.035	Vp

△1 Average values for Test Numbers 1-4.
△2 Average values for Test Numbers 5-8.
△3 Average values for Test Numbers 9-12.
△4 Average values for Test Numbers 13-16.

TABLE C2. MANUFACTURER B MIL-M-38510/10104 25°C PARAMETER CHARACTERIZATION

Parameter	Test No.	Limits		Initial Data		FINAL ACCELERATED LIFE TEST DATA						Units
						225°C 1000 HRS NO. OF PARTS - 1		200°C 1000 HRS NO. OF PARTS - 5		175°C 1000 HRS NO. OF PARTS - 4		
		MIN	MAX	Mean	Sigma	Mean	Sigma	Mean	Sigma	Mean	Sigma	
V_{IO}	△1	-0.5	+0.5	-0.007	0.204	0.015	0.055	0.708	0.179	0.036	0.140	mV
$+A_{VS}$	69	80	---	1,614	1,892	228.892		1163.350	1834.343	10'34.512	14315.242	V/mV
$-A_{VS}$	70	80	---	1,920	3,039	174,267		2052.478	2187.422	1129.867	675.704	V/mV
$+A_{VS}$	71	20	---	1,120	1,373	170.314		397.930	109.976	653.753	267.677	V/mV
$-A_{VS}$	72	20	---	2,904	8,059	152 987		1172.205	1398.600	2509.917	1647.569	V/mV
I_{IO}	△2	0.2	+0.2	0.012	0.041	-0.022	0.003	-0.050	0.052	-0.008	0.012	nA
I_{IB}	△3	-0.1	2.0	1.067	0.413	0.633	0.045	0.707	0.091	0.687	0.053	nA
$-I_{IB}$	△4	0.1	2.0	1.078	0.415	0.686	0 074	0.757	0.107	0.699	0.057	nA
+PSRR	17	0	16	0.070	1.635	4.551		-0.286	1.370	-0.762	1.635	μV/V
-PSRR	18	0	16	1.707	0.925	2.536		2.264	1.770	2.008	0.807	μV/V
CMRR	19	96	---	124.7	8 916	116.137		125.644	5.694	117.269	2.757	dB
$+I_{OS}$	22	15	2.0	-5.406	0.155	-5.279		-5.227	0.126	-5.233	0.233	mA
$-I_{OS}$	23	2	20	11.41	0.269	11.314		11.167	0.155	10.810	0.118	mA
P_D	24	2	24	11.38	0.074	10.268		10.889	0.492	10.980	0.351	mW
V_{OP+}	67	16	---	18.493	0.090	18.951		18.947	0.027	18.918	0.031	V_p
V_{OP-}	68	---	16	-18.836	0.056	18.739		-18.732	0.031	-18.693	0.022	V_p

△1 Average values for Test Numbers 1-4.
△2 Average values for Test Numbers 5-8.
△3 Average values for Test Numbers 9-12.
△4 Average values for Test Numbers 13-16.

TABLE C3. MANUFACTURER B MIL-M-38510/10107 25°C PARAMETER CHARACTERIZATION

Parameter	Test No.	Limits		Initial Data		FINAL ACCELERATED LIFE TEST DATA						Units
						175°C 1000 HRS. NO. OF PARTS - 4		150°C 1000 HRS NO. OF PARTS - 4		125°C 1000 HRS NO. OF PARTS - 6		
		MIN	MAX	Mean	Sigma	Mean	Sigma	Mean	Sigma	Mean	Sigma	
V_{IO}	△1	-4.0	+4.0	-0.319	1.393	-1.062	1.370	-0.369	1.311	-0.244	1.638	mV
$+A_{VS}$	69	80	---	151.9	29.11	156.609	28.131	138.755	21.843	158.162	74.727	V/mV
$-A_{VS}$	70	80	---	112.0	16.46	111.004	22.457	103.808	19.014	112.073	20.133	V/mV
$+A_{VS}$	71	60	---	154.0	81.50	170.061	45.984	172.847	79.574	247.665	113.493	V/mV
$-A_{VS}$	72	80	---	174.9	65.18	161.578	118.307	144.645	38.858	166.892	74.111	V/mV
$+A_{VS}$	73	40	---	169.5	98.31	180.070	51.433	161.810	37.531	480.114	688.503	V/mV
$-A_{VS}$	74	40	---	115.9	18.21	115.194	30.827	95.201	11.125	17.325	26.046	V/mV
$+A_{VS}$	75	40	---	123.2	70.73	135.569	36.273	216.996	183.822	224.247	119.670	V/mV
$-A_{VS}$	76	40	---	1139.8	3037	231.374	86.480	212.954	116.275	483.305	504.467	V/mV
I_{IO}	△2	-40	+40	-0.317	6.401	11.331	17.257	-1.118	3.596	-6.009	8.296	nA
$+I_{IB}$	△3	+1	250	108.0	23.82	147.399	51.231	125.516	25.903	121.255	29.962	nA
$-I_{IB}$	△4	+1	250	111.2	24.05	109.201	37.151	127.563	25.093	128.444	31.828	nA
+PSRR	17	0	100	-26.08	10.37	-22.8[illegible]	11.245	-31.069	12.942	-21.349	11.902	μV/V
-PSRR	18	0	100	-14.95	6.447	-18.760	2.740	-16.099	16.420	-10.096	13.710	μV/V
CMR	19	80	---	105.3	8.658	110.746	18.444	108.061	11.605	107.764	10.032	dB
$V_{IOADJ(+)}$	20	7.5	---	12.52	0.830	12.906	0.802	12.889	0.534	13.161	0.843	mV
$V_{IOADJ(-)}$	21	7.5	---	-12.68	0.844	-12.896	0.647	-13.086	0.652	-13.368	0.810	mV
$I_{OS}(+)$	22	-40	-12	-31.18	1.205	-30.663	0.718	-30.811	0.743	-30.656	1.849	mA
$I_{OS}(-)$	23	12	55	39.42	1.553	40.236	2.243	33.340	1.771	37.988	3.292	mA
P_D	24	10	200	262.6	9.72	261.452	5.156	256.111	4.507	260.301	21.113	mW
V_{OPP}	67	34	---	37.77	0.117	37.930	0.022	37.813	0.027	37.942	0.073	V_{P-P}
V_{OPP}	68	32	---	36.25	0.123	36.530	0.141	36.440	0.124	36.598	0.173	V_{P-P}

△1 Data listed represent average values for test numbers 1 through 4.

△2 Data listed represent average values for test numbers 5 through 8.

△3 Data listed represent average values for test numbers 9 through 12.

△4 Data listed represent average values for test numbers 13 through 16.

TABLE C4. MANUFACTURER C 25°C MIL-M-38510/10107 PARAMETER CHARACTERIZATION

Parameter	Test No.	Limits		Initial Data		FINAL ACCELERATED LIFE TEST DATA 175°C 4000 HRS NO. OF PARTS - 23		150°C 4000 HRS NO. OF PARTS - 30		125°C 4000 HRS NO. OF PARTS - 23		Units
		MIN	MAX	Mean	Sigma	Mean	Sigma	Mean	Sigma	Mean	Sigma	
V_{IO}	△1	-4.0	+4.0	0.053	1.273	0.673	1.561	0.273	1.239	0.537	1.374	mV
$+A_{VS}$	69	80	---	2068	3915	2723.077	6429.410	1716.619	2094.006	923.154	803.507	V/mV
$-A_{VS}$	70	80	---	2966	8711	5272.578	18963.809	4675.023	16405.414	767.412	602.991	V/mV
$+A_{VS}$	71	80	---	964.4	2321	549.678	497.054	743.035	1209.795	622.427	986.223	V/mV
$-A_{VS}$	72	80	---	140.9	129.9	70.044	30.501	71.146	21.862	75.495	28.030	V/mV
$+A_{VS}$	73	40	---	161.2	129.1	204.720	220.265	149.579	103.002	164.300	77.997	V/mV
$-A_{VS}$	74	40	---	228.9	778.1	142.521	41.387	136.108	27.495	2584.124	11294.500	V/mV
$+A_{VS}$	75	40	---	525.8	1037	464.529	726.873	412.515	469.878	749.231	2221.062	V/mV
$-A_{VS}$	76	40	---	738.6	1852	1150.085	2296.207	626.233	832.009	1499.613	4007.146	V/mV
I_{IO}	△2	-40	+40	-9.499	9.523	-5.130	9.865	-7.704	8.540	-9.130	7.046	nA
$+I_{IB}$	△3	+1	250	173.5	31.94	185.541	35.442	185.446	34.016	177.005	34.359	nA
$-I_{IB}$	△4	+1	250	187.0	31.23	197.005	36.594	197.407	33.469	199.958	34.470	nA
+PSRR	17	0	100	-14.768	10.15	-18.511	10.169	-16.283	6.698	-17.778	12.359	V/V
-PSRR	18	0	100	-35.373	12.13	-35.303	12.130	-35.941	9.560	-35.185	14.001	V/V
CMRR	19	80	---	100.1	6.568	100.526	4.951	98.735	4.094	101.773	5.581	dB
$V_{IO\&ADJ(+)}$	20	7.5	---	16.92	1.133	16.828	1.654	17.114	1.026	17.364	1.208	mV
$V_{IO\&ADJ(-)}$	21	7.5	---	-16.83	1.397	-16.987	1.502	-17.360	1.389	-17.270	1.206	mV
$I_{OS}(+)$	22	-40	-12	-30.19	1.358	-30.549	1.299	-30.893	1.168	-30.813	1.405	mA
$I_{OS}(-)$	23	12	55	24.94	2.533	25.093	3.239	24.694	1.835	24.759	2.238	mA
P_D	24	10	280	204.3	11.65	206.444	13.963	204.720	8.091	201.535	10.837	mW
V_{OPP}	67	34	---	37.81	0.147	37.756	0.243	37.789	0.112	37.838	0.083	V_{p-p}
V_{OPP}	68	32	---	36.60	0.188	36.464	0.300	36.476	0.202	36.564	0.132	V_{p-p}

△1 Average values for Test Numbers 1-4.
△2 Average values for Test Numbers 5-8.
△3 Average values for Test Numbers 9-12.
△4 Average values for Test Numbers 13-16.

TABLE C5. MANUFACTURER D 25°C MIL-M-38510/10201 PARAMETER CHARACTERIZATION

Parameter	Test No	Limits MIN	Limits MAX	Initial Data Mean	Initial Data Sigma	200°C 4000 HRS NO. OF PARTS - 35 Mean	200°C Sigma	175°C 4000 HRS NO. OF PARTS - 32 Mean	175°C Sigma	150°C 4000 HRS NO. OF PARTS - 35 Mean	150°C Sigma	Units
V_{RLINE}	1	-0.10	0.10	-0.017	0.004	-0.020	0.007	-0.019	0.005	-0.018	0.003	% V_{OUT}
V_{RLINE}	2	-0.3	0.3	-0.117	0.029	-0.144	0.040	-0.141	0.025	-0.176	0.018	% V_{OUT}
V_{RLINE}	3	-0.2	0.2	-0.011	0.005	-0.015	0.009	-0.013	0.005	-0.012	0.004	% V_{OUT}
V_{RLOAD}	4	-0.15	0.15	-0.011	0.009	-0.015	0.012	-0.012	0.001	-0.014	0.006	% V_{OUT}
V_{RLOAD}	5	-0.5	0.5	0.000	0.014	-0.001	0.004	-0.002	0.001	0.002	0.002	% V_{OUT}
V_{RLOAD}	6	-0.2	0.2	0.003	0.008	0.005	0.005	0.006	0.001	0.006	0.001	% V_{OUT}
V_{REF}	7	6.95	7.35	7.243	0.056	7.230	0.058	7.248	0.034	7.228	0.052	V
I_{SCD}	9	0.5	3.0	2.472	0.143	2.552	0.117	2.591	0.108	2.646	0.143	mA
I_{OS}	8	45	85	59.19	5.217	61.760	3.001	62.628	2.426	62.737	1.922	mA

TABLE C6. MANUFACTURER C 25°C MIL-M-38510/10201 PARAMETER CHARACTERIZATION

Parameter	Test No.	Limits		Initial Data		FINAL ACCELERATED LIFE TEST DATA						Units
						200°C 4000 HRS NO. OF PARTS - 27		175°C 4000 HRS NO. OF PARTS - 35		150°C 4000 HRS NO. OF PARTS - 35		
		MIN	MAX	Mean	Sigma	Mean	Sigma	Mean	Sigma	Mean	Sigma	
V_{RLINE}	1	-0.10	0.10	-0.019	0.011	-0.017	0.011	-0.023	0.013	-0.019	0.011	% V_{OUT}
V_{RLINE}	2	-0.3	0.3	-0.141	0.049	-0.107	0.027	-0.127	0.038	-0.118	0.024	% V_{OUT}
V_{RLINE}	3	-0.2	0.2	-0.013	0.010	-0.012	0.011	-0.017	0.012	-0.012	0.010	% V_{OUT}
V_{RLOAD}	4	-0.15	0.15	-0.007	0.010	-0.017	0.005	-0.012	0.006	-0.021	0.006	% V_{OUT}
V_{RLOAD}	5	-0.5	0.5	0.001	0.005	-0.001	0.002	-0.000	0.004	0.000	0.003	% V_{OUT}
V_{FLOAD}	6	-0.2	0.2	0.003	0.003	0.003	0.001	0.007	0.018	0.004	0.001	% V_{OUT}
V_{REF}	7	6.95	7.35	7.208	0.097	7.146	0.087	7.254	0.50	7.253	0.039	V
I_{SCD}	9	0.5	3.0	2.185	0.412	2.556	0.287	2.211	0.316	2.201	0.368	mA
I_{OS}	8	45	85	58.58	2.801	60.441	2.543	60.626	1.151	61.600	1.121	mA

TABLE C7. MANUFACTURER D 25°C MIL-M-38510/10701 PARAMETER CHARACTERIZATION

Parameter	Test No.	Limits		Initial Data		FINAL ACCELERATED LIFE TEST DATA 250°C 4000 HRS NO. OF PARTS - 32		225°C 4000 HRS NO. OF PARTS - 32		200°C 4000 HRS NO. OF PARTS - 32		Units
		MIN	MAX	Mean	Sigma	Mean	Sigma	Mean	Sigma	Mean	Sigma	
V_{OUT}	1	4.80	5.20	5.044	0.042	5.032	0.035	5.047	0.035	5.037	3.025	Vdc
V_{OUT}	2	4.80	5.20	5.044	0.041	5.024	0.036	5.040	0.035	5.029	0.023	Vdc
V_{OUT}	4	4.80	5.20	5.029	0.044	5.035	0.035	5.051	0.035	5.038	0.024	Vdc
V_{RLN}	6	-20	+20	-17.388	1.908	-14.437	1.540	-14.750	1.479	-15.093	1.284	mVdc
V_{RLO}	7	-50	+50	-2.790	2.626	6.219	2.103	4.563	1.967	5.438	2.703	mVdc
I_{SCO}	9	-10.0	0	-7.168	0.342	-6.777	0.346	-6.890	0.214	-6.876	0.241	mAdc
I_{SCO}	10	-10.0	0	-7.224	0.367	-6.684	0.357	-6.781	0.233	-6.772	0.269	mAdc
I_{SCO}	11	-10.0	0	-7.130	0.368	-6.622	0.346	-6.733	0.216	-6.735	0.277	mAdc
ΔI_{SCO}	12	-0.8	-0.8	-0.056	0.046	0.093	0.064	0.109	0.042	0.104	0.048	mAdc
ΔI_{SCO}	13	-0.5	0	-0.038	0.067	-0.155	0.130	-0.157	0.115	-0.143	0.110	mAdc
I_{OS}	14	-2.0	-0.1	-1.221	0.003	-1.226	0.000	-1.228	0.001	-1.230	0.002	Adc
V_{START}	15	---	9.0	5.037	0.046	5.042	0.035	5.057	0.036	5.047	0.025	Vdc

TABLE C8. MANUFACTURER B 25°C MIL-M-38510/10701 PARAMETER CHARACTERIZATION

Parameter	Test No.	Limits Min	Limits Max	Initial Data Mean	Initial Data Sigma	Final Accelerated Life Test Data: 250°C 4000 HRS, No. of Parts - 32 Mean	Sigma	225°C 4000 HRS, No. of Parts - 32 Mean	Sigma	200°C 4000 HRS, No. of Parts - 32 Mean	Sigma	Units
V_{OUT}	1	4.80	5.20	5.039	0.061	5.015	0.051	5.010	0.055	4.999	0.045	Vdc
V_{OUT}	2	4.80	5.20	5.003	0.060	4.931	0.050	4.905	0.055	4.967	0.044	Vdc
V_{OUT}	4	4.80	5.20	5.061	0.063	5.053	0.054	5.056	0.057	5.036	0.046	Vdc
V_{RLN}	6	-20	+20	5.710	2.626	7.344	2.217	7.061	1.456	6.437	1.002	mVdc
V_{RLD}	7	-50	+50	35.639	3.510	35.031	2.779	33.454	2.464	33.500	3.270	mVdc
I_{SCD}	9	-10.0	0	-4.084	0.350	-4.043	0.276	-4.061	0.307	-3.996	0.326	mAdc
I_{SCD}	10	-10.0	0	-4.070	0.367	-3.926	0.283	-3.942	0.307	-3.869	0.346	mAdc
I_{SCD}	11	-10.0	0	-4.056	0.349	-3.762	0.261	-3.780	0.323	-3.757	0.344	mAdc
ΔI_{SCD}	12	-0.8	-0.8	0.014	0.047	0.115	0.044	0.118	0.033	0.130	0.036	mAdc
ΔI_{SCD}	13	-0.5	0	-0.028	0.028	-0.301	0.129	-0.281	0.107	-0.241	0.091	mAdc
I_{OS}	14	-2.0	-0.1	-0.905	0.149	-0.910	0.138	-0.941	0.139	-0.948	0.158	Adc
V_{START}	15	---	9.0	5.017	0.061	5.013	0.052	5.015	0.056	4.995	0.045	Vdc

TABLE C9. MANUFACTURER B MIL-M-38510/10304 25°C PARAMETER CHARACTERIZATION

Parameter	Test No.	Limits		Initial Data		FINAL ACCELERATED LIFE TEST DATA						Units
						250°C 500 HRS No. of PARTS-20		225°C 500 HRS No. of PARTS-34		200°C 500 HRS No. of PARTS-17		
		Min	Max	Mean	Sigma	Mean	Sigma	Mean	Sigma	Mean	Sigma	
V_{IO}	1-4	-5	+5	-0.243	0.458	2.142	1.131	2.747	0.724	3.452	0.751	mV
V_{ICR}	5-7	-5	+5	-0.299	0.467	0.618	0.727	0.887	0.432	1.293	0.324	mV
$+A_{VC}$	92	150	-	925.260	1354.266	650.605	522.605	523.588	323.444	899.990	405.188	V/mV
$-A_{VC}$	93	150	-	1371.064	2028.147	331.953	149.427	331.471	132.577	240.000	67.578	V/mV
I_{IO}	8-10	-20	+20	1.740	1.181	-3.938	5.141	-4.040	4.474	-3.021	2.831	nA
I_{IOR}	11	-25	+25	1.387	3.150	-2.972	13.589	-8.965	10.053	13.834	6.890	nA
$+I_{IB}$	12-14	-150	0.1	-53.829	14.778	-58.260	18.245	-65.936	18.275	-53.018	13.115	nA
$-I_{IB}$	12-14	-150	0.1	-55.014	15.055	-55.018	17.726	-62.689	17.057	-50.733	11.826	nA
$+V_{IO}$(ADJ)	23	4.0	-	5.219	0.251	5.784	0.225	5.699	0.405	6.073	0.403	mV
$-V_{IO}$(ADJ)	24	4.0	-	-5.369	0.266	-5.318	0.305	-5.132	0.326	-5.345	0.301	mV
CMRR	25	80	-	110.727	5.946	88.884	1.914	87.617	1.275	86.251	1.581	dB
$V_{OL\ 1}$	26-27	0	.400	0.276	0.015	0.312	0.021	0.328	0.024	0.326	0.018	V
$V_{OL\ 2}$	28-29	0	1.500	0.915	0.037	0.935	0.048	0.939	0.055	0.922	0.048	V
I_O	16	0	.500	0.123	0.007	0.095	0.020	0.083	0.005	0.076	0.004	µA
I_G	17	-10.0	0	-1.295	1.342	-0.412	0.519	-0.895	0.815	-0.029	0.108	µA
I_{I1}	18	0	.100	0.048	0.003	0.072	0.004	0.071	0.003	0.069	0.001	µA
I_{I2}	19	0	.100	0.048	0.004	0.070	0.000	0.070	0.000	0.067	0.004	µA
$+I_{IC}$	20	0.5	-5.0	3.250	0.267	3.177	0.275	3.382	0.286	3.020	0.198	mA
$-I_{IC}$	21	-4.0	-0.5	-2.306	0.209	-2.147	0.211	-2.334	0.178	-2.063	0.088	mA
I_{OS}	22	70	200	140.112	12.962	129.469	13.204	140.191	15.415	139.490	12.696	mA
P_D	15	30	270	166.653	14.072	160.518	14.470	171.461	13.683	152.487	5.689	mW

TABLE C10. MANUFACTURER D MIL-M-38510/10304 25°C PARAMETER CHARACTERIZATION

Parameter	Test No.	Limits Min	Limits Max	Initial Data Mean	Initial Data Sigma	FINAL ACCELERATED LIFE TEST DATA: 250°C 500 HRS No. of PARTS-20 Mean	Sigma	225°C 500 HR No. of PARTS-14 Mean	Sigma	200°C 500 HRS No. of PARTS-17 Mean	Sigma	Units
V_{IO}	1-4	-5	+5	-0.335	0.414	3.570	0.640	3.259	0.702	3.402	0.789	mV
V_{IOR}	5-7	-5	+5	-0.743	0.389	0.597	0.522	0.383	0.528	0.501	0.338	mV
$+A_{VC}$	92	150	-	459.867	73.339	823.617	429.181	586.830	628.532	177.441	577.447	V/mV
$-A_{VC}$	93	150	-	302.513	98.799	269.437	731.412	1075.414	757.561	362.708	534.965	V/mV
I_{IO}	8-10	-20	+20	0.678	1.661	-6.592	4.065	-5.480	2.778	-1.611	2.241	nA
I_{IOR}	11	-25	+25	3.992	4.446	-9.345	5.664	-5.465	5.382	10.027	6.855	nA
$+I_{IB}$	12-14	-150	0.1	-56.370	27.401	-64.108	27.085	-54.975	24.628	-59.702	26.778	nA
$-I_{IB}$	12-14	-150	0.1	-57.132	27.791	-59.413	27.491	-49.865	22.341	-59.726	29.651	nA
$+V_{IO}(ADJ)$	23	4.0	-	8.929	0.289	9.404	0.264	9.359	0.278	9.722	0.345	mV
$-V_{IO}(ADJ)$	24	4.0	-	-8.812	0.290	-8.202	0.256	-8.190	0.203	-8.465	0.298	mV
CMRR	25	80	-	105.366	5.760	91.286	3.977	91.997	7.004	88.091	2.746	dB
VOL 1	26-27	0	.400	0.230	0.018	0.271	0.020	0.271	0.019	0.285	0.026	V
VOL 2	28-29	0	1.500	0.833	0.021	0.845	0.022	0.829	0.021	0.856	0.080	V
I_O	16	0	.500	0.123	0.007	0.089	0.003	0.094	0.006	0.091	0.008	A
I_G	17	-10.0	0	-0.855	0.966	0.017	0.021	-0.003	0.046	-0.011	0.043	A
I_{I1}	18	0	.100	0.048	0.003	0.074	0.004	0.074	0.005	0.070	0.002	A
I_{I2}	19	0	.100	0.049	0.003	0.070	0.002	0.070	0.000	0.070	0.002	A
$+I_{IC}$	20	0.5	-5.0	4.113	0.244	4.225	0.221	4.079	0.191	4.106	0.239	mA
$-I_{IC}$	21	-4.0	-0.5	-2.951	0.226	-2.850	0.191	-2.707	0.116	-2.776	0.199	mA
I_{OS}	22	70	200	163.697	5.014	171.275	4.335	168.893	3.858	163.947	4.245	mA
P_D	15	30	270	211.924	13.962	212.250	12.227	203.571	6.305	205.471	12.987	mW

APPENDIX D

BIAS CIRCUIT EVALUATION

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1.0 INTRODUCTION

Valid accelerated life test results at ambient temperatures up to 250°C depend upon the selection of the proper bias circuit. The existing MIL-M-38510 bias circuits were evaluated up to ambient temperatures of 275°C. In those instances where the existing circuit was unacceptable, or a MIL-M-38510 circuit did not exist, several candidate circuits were evaluated to find a bias circuit that

(a) Maintained maximum rated voltage at the device terminals over the temperature range to provide maximum acceleration of surface effect failure mechanisms.

(b) Maintained the device current at a controlled low level to minimize failures due to thermal runaway and electromigration.

(c) Maintained a consistent set of internal microcircuit stress (primarily voltage) conditions over the temperature range. A drastic difference between circuit node voltages at different accelerated test temperatures may invalidate subsequent calculations of acceleration factors.

2.0 MIL-M-38510/10104 (LM108A) EVALUATION

Prior to selecting a suitable bias circuit for the LM108A devices the accelerated life test bias circuit contained in MIL-M-38510/101D (15 September 1975) was updated by the circuit contained in Amendment 3 (22 February 1977) and subsequently included in MIL-M-38510/101E. The original bias circuit (as shown in MIL-M-38510/101D) did not apply maximum stress across the device, therefore the circuit configuration was updated. Operation of LM108A devices in the accelerated life test circuit shown in Amendment 3 indicated the circuit was not suitable for the LM108A operational amplifier. The circuit places 40 Vdc across the device through a 100 ohm resistor, 5 Vdc to the non-inverting input through a 1K ohm resistor, and grounds the inverting input. Two problems were experienced with this configuration: a) the 5 Vdc input voltage results in excessive input current due to transient protection diodes between the inverting and non-inverting inputs of the amplifier, and b) device output voltage would switch state (due to thermal biasing) above 150°C. Lowering the 5 Vdc input voltage to 2 Vdc reduced the input current to acceptable levels, but the device output voltage would still switch state above 150°C. Applying a 2 Vdc voltage to the inverting input of the amplifier and grounding the non-inverting input provided a fairly consistent output voltage between temperatures of 200°C and 250°C. Although the output is thermally biased high, previous experience had indicated that most operational amplifier failures were input related, and operating the device in this configuration was not considered a problem. The average performance of five devices in this circuit configuration is shown in Figures D1 and D2. As indicated in these figures, the output voltage is high and consistent (between 35 Vdc and 39 Vdc) at ambient temperatures above 200°C. Also, the input bias current is below 2 mA at ambient temperatures up to 250°C. Above 250°C the total device current became excessive due to thermal runaway. During step-stress testing, thermal runaway occurred at the 275°C step. These results indicated that life tests could be performed at temperatures up to a maximum of 250°C. However, when the 250°C life tests were initiated, 43% of the Manufacturer A devices drew excessive current after one half hour at 250°C. All of these devices had a 7642 date code whereas the circuit evaluation and step-stress test devices had a 7643 date code. Apparently the 7642 date coded devices were susceptible to

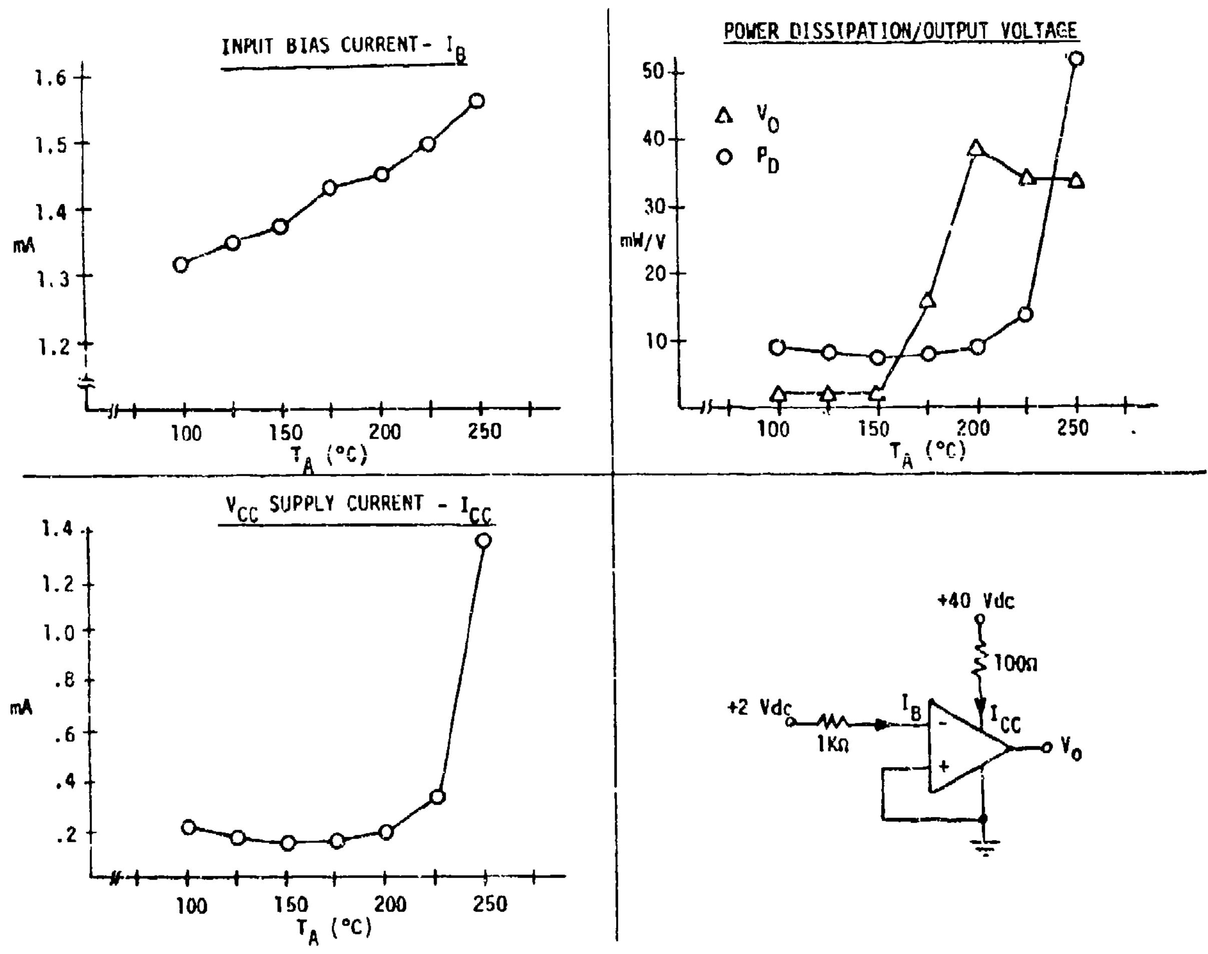


FIGURE D1. MANUFACTURER B MIL-M-38510/10104 (LM108A) CIRCUIT EVALUATION

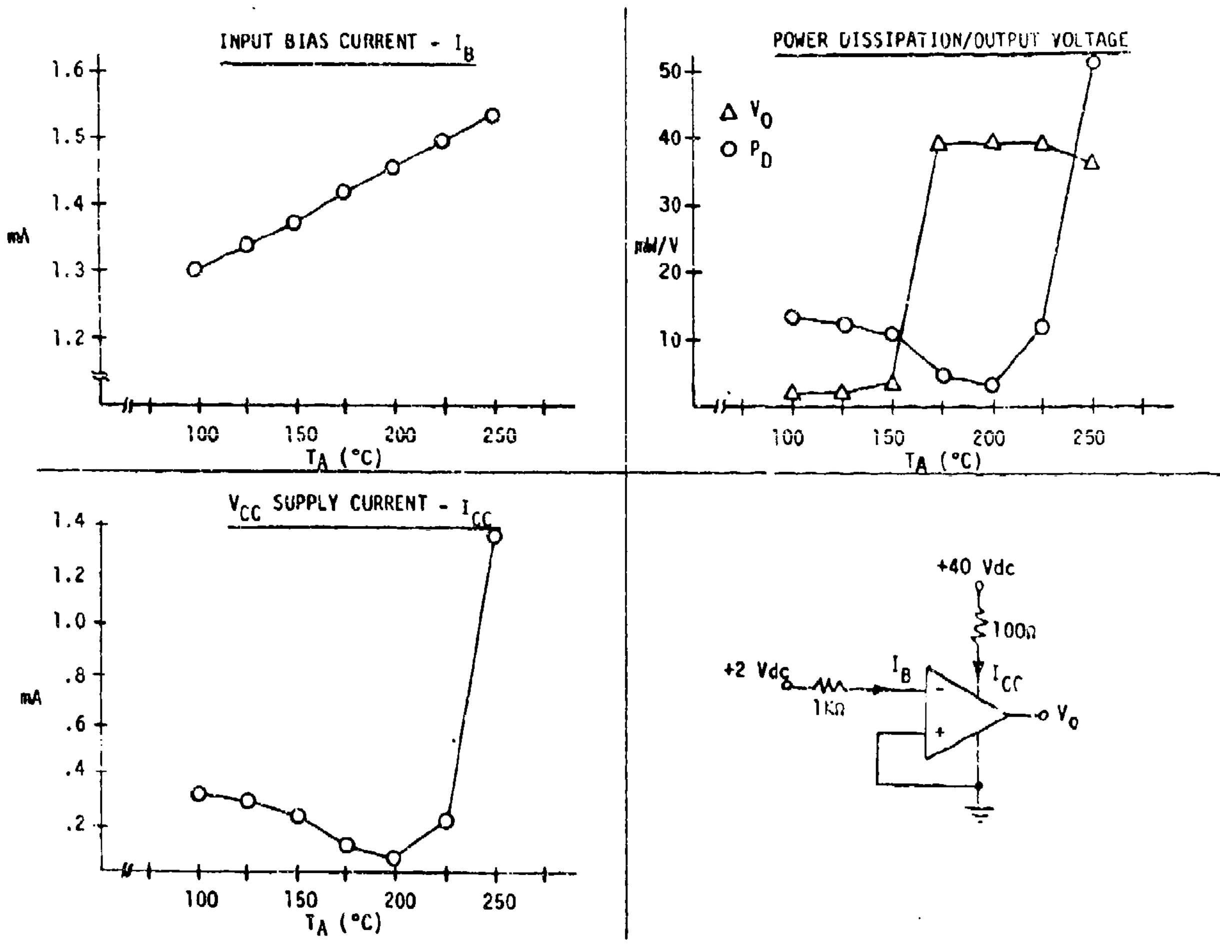


FIGURE D2. MANUFACTURER A MIL-M-38510/10104 (LM108A) CIRCUIT EVALUATION

thermal runaway at a lower temperature (250°C) than were the 7643 date coded devices, but examinations of these devices disclosed no physical difference between the devices of each date code. Consequently, the 250°C life test was immediately terminated and, after electrical testing, the devices were returned to life test and the temperature was reduced to 175°C. Thus, the LM108A life test temperatures were 175°C, 200°C and 225°C.

3.0 MIL-M-38510/10107 (LM118) EVALUATION

Operation of LM118 devices in the accelerated life test circuit shown in Amendment 3 (22 February 1977) of MIL-M-38510/101D indicated the circuit was not suitable for the LM118 operational amplifiers. This circuit is identical to the previously described MIL-M-38510/101D circuit for the LM108A, and identical problems were experienced with the LM118 (the input bias currents were excessive and the output voltage changed state). Operation of LM118 devices in the bias circuit selected for the LM108A resulted in the performance characteristics (average of 5 devices) shown in Figures D3 and D4. As indicated in the figures, the output voltage is constant up to 200°C and input bias currents are less than 1.3 mA. However, the output voltage changes state due to thermal biasing at temperatures slightly above 200°C and one Manufacturer B LM118 drew excessive current at 225°C. The Manufacturer C LM118 device did not draw excessive current until 250°C. Attempts to find a biasing configuration that would avoid the thermal biasing problem were unsuccessful. Two candidate circuits evaluated in attempts to avoid thermal biasing are shown in Figure D5 as Circuits B and C. Also shown in the figure for comparison is the selected LM108A/LM118 bias circuit (Circuit A). Circuit B reduces the voltage across the device from 40 Vdc to 30 Vdc, but devices still experience thermal biasing slightly above 200°C. Circuit C maintains 40 Vdc across the devices by applying plus and minus 20 Vdc, but total device current is higher than with the 40 Vdc configuration of Circuit A. Thus, since none of the circuits avoided thermal biasing above 200°C and Manufacturer B's devices were susceptable to thermal runaway around 225°C, the life test temperatures were selected as 175°C, 150°C, and 125°C. Circuit A was selected because it placed maximum rated voltage across the device at the lowest total device current.

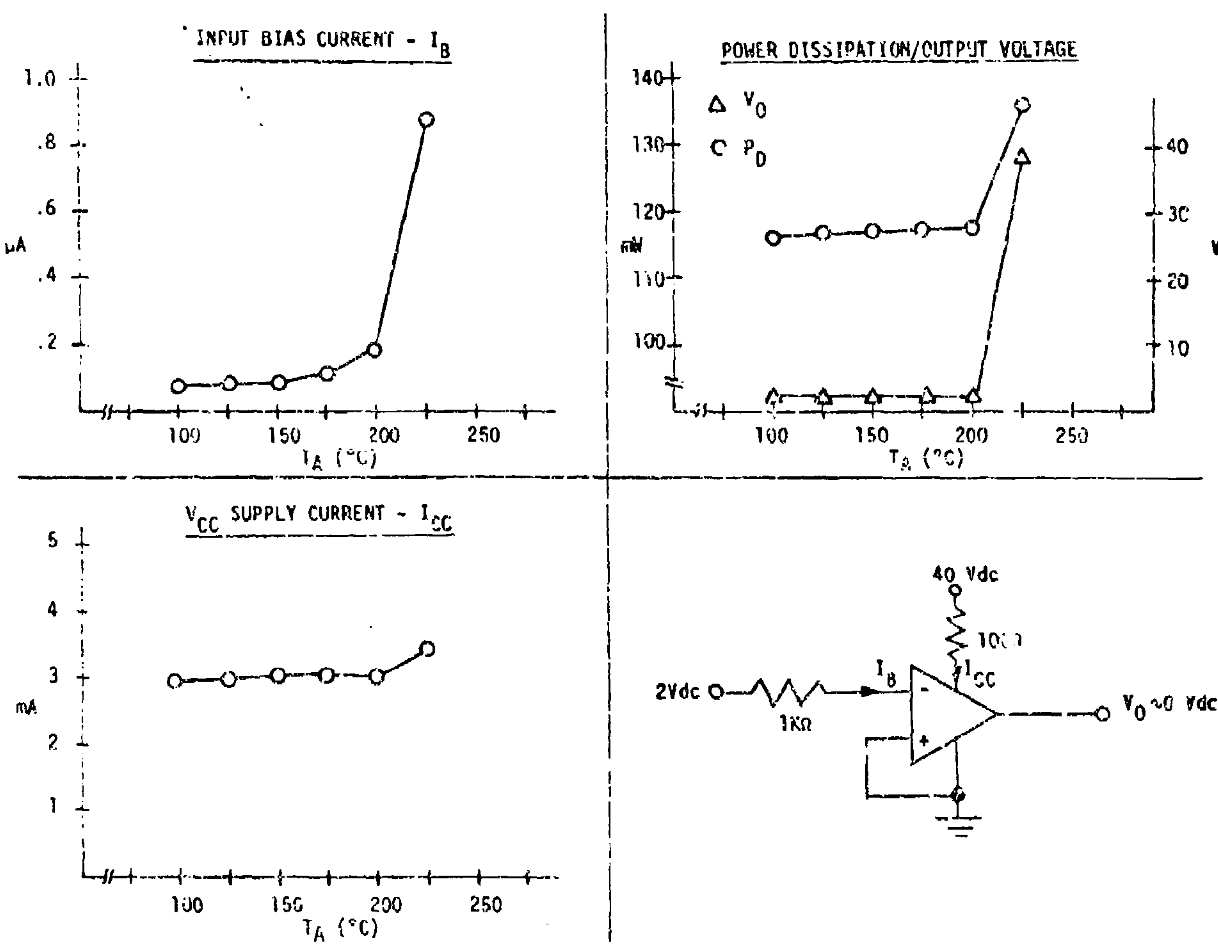


FIGURE D3. MANUFACTURER C MIL-M-38510/10107 (LM118) CIRCUIT EVALUATION

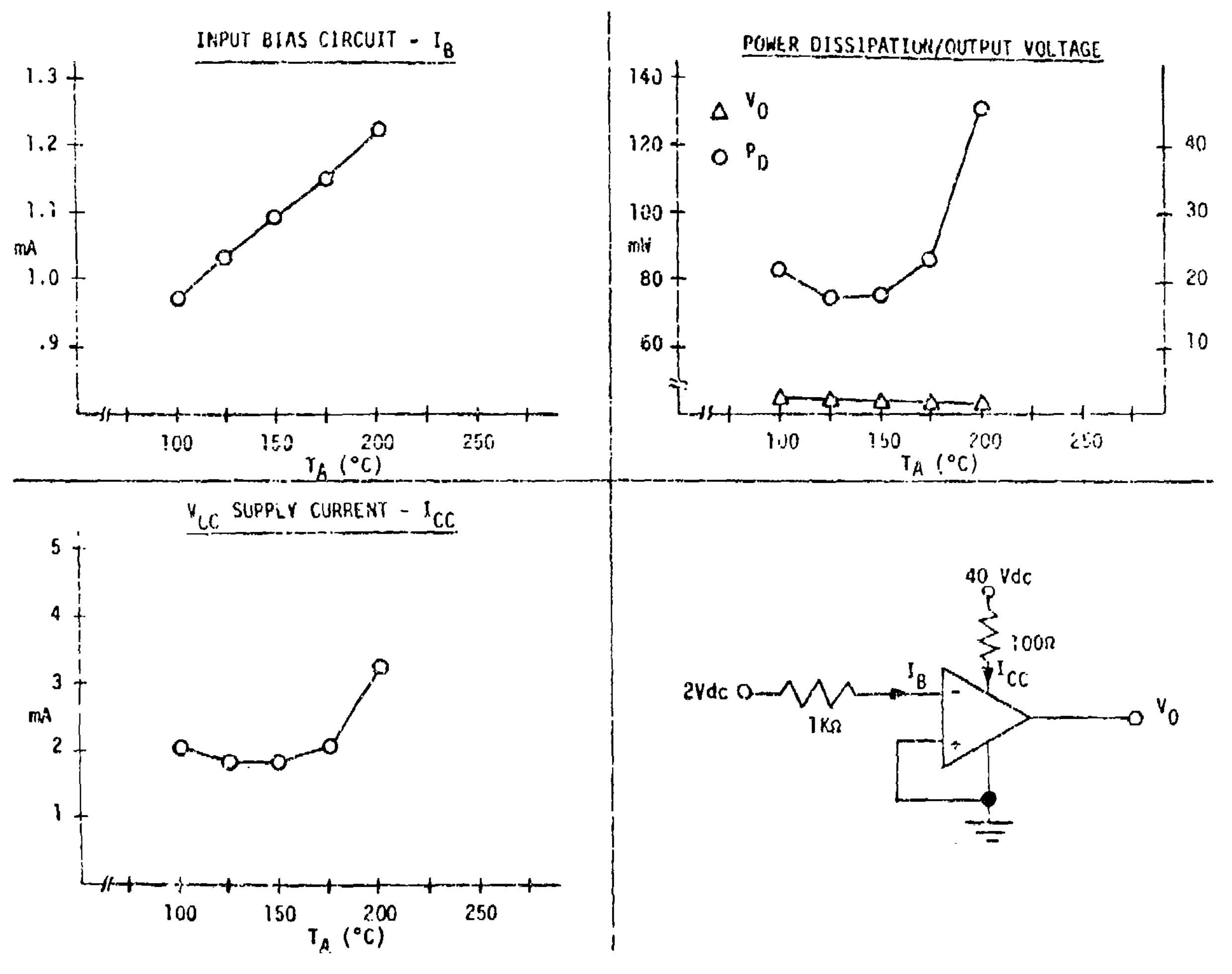


FIGURE D4. MANUFACTURER B MIL-M-38510/10107 (LM118) CIRCUIT EVALUATION

	CIRCUIT A ACCEPTABLE		CIRCUIT B UNACCEPTABLE		CIRCUIT C UNACCEPTABLE	
T_A (°C)	I_{CC} (mA)	V_O (VOLTS)	I_{CC} (mA)	V_O (VOLTS)	I_{CC} (mA)	V_O (VOLTS)
25	2.6	1.3	2.5	1.4	7.5	-12.8
125	2.4	1.18	2.2	1.10	5.3	-16.7
150	1.9	0.81	1.5	0.80	6.4	-18.3
175	2.1	0.73	1.5	0.69	6.2	-18.4
200	3.2	8.2	1.6	0.60	5.8	-18.5
225	2.6 ⚠1	39.56	2.2	UNSTABLE ⚠2	4.5	+10.4
250	THERMAL RUNAWAY	—	THERMAL RUNAWAY	—	THERMAL RUNAWAY	—

NOTES: (AVERAGE VALUES FOR DATA FROM BOTH MANUFACTURERS.)

⚠1 ONE MANUFACTURER B DEVICE WENT INTO THERMAL RUNAWAY, AND IS NOT INCLUDED IN THE AVERAGE.

⚠2 MANUFACTURER B'S DEVICE OUTPUT SWITCHED TO A HIGH STATE WHILE MANUFACTURER C'S OUTPUT REMAINED IN THE LOW STATE.

FIGURE D5. MIL-M-38510/10107 (LM118) CANDIDATE BIAS CIRCUITS

4.0 MIL-M-38510/10201 (723) EVALUATION

Operation of the 723 devices in the MIL-M-38510/10201 accelerated life test bias circuit indicated, as shown in Figures D6 and D7, that the circuit was satisfactory for the Manufacturer D devices, but unsatisfactory for the Manufacturer C devices at life test temperatures above 200°C. The average performance of five Manufacturer D devices exhibited an abrupt 300 mV change in output voltage between 225°C and 250°C. A 300 mV change is not considered excessive. However, the Manufacturer C devices exhibited a 5 Vdc change in output voltage between 200°C and 225°C and a 15 Vdc change between 225°C and 250°C. These changes are considered excessive and the MIL-M-38510/10201 bias circuit was deemed unacceptable at ambient temperatures above 200°C. Attempts to find an alternate circuit configuration that was satisfactory above 200°C were unsuccessful and it was decided that accelerated life tests of the 723 devices should be conducted at ambient temperatures of 200°C, 175°C, and 150°C.

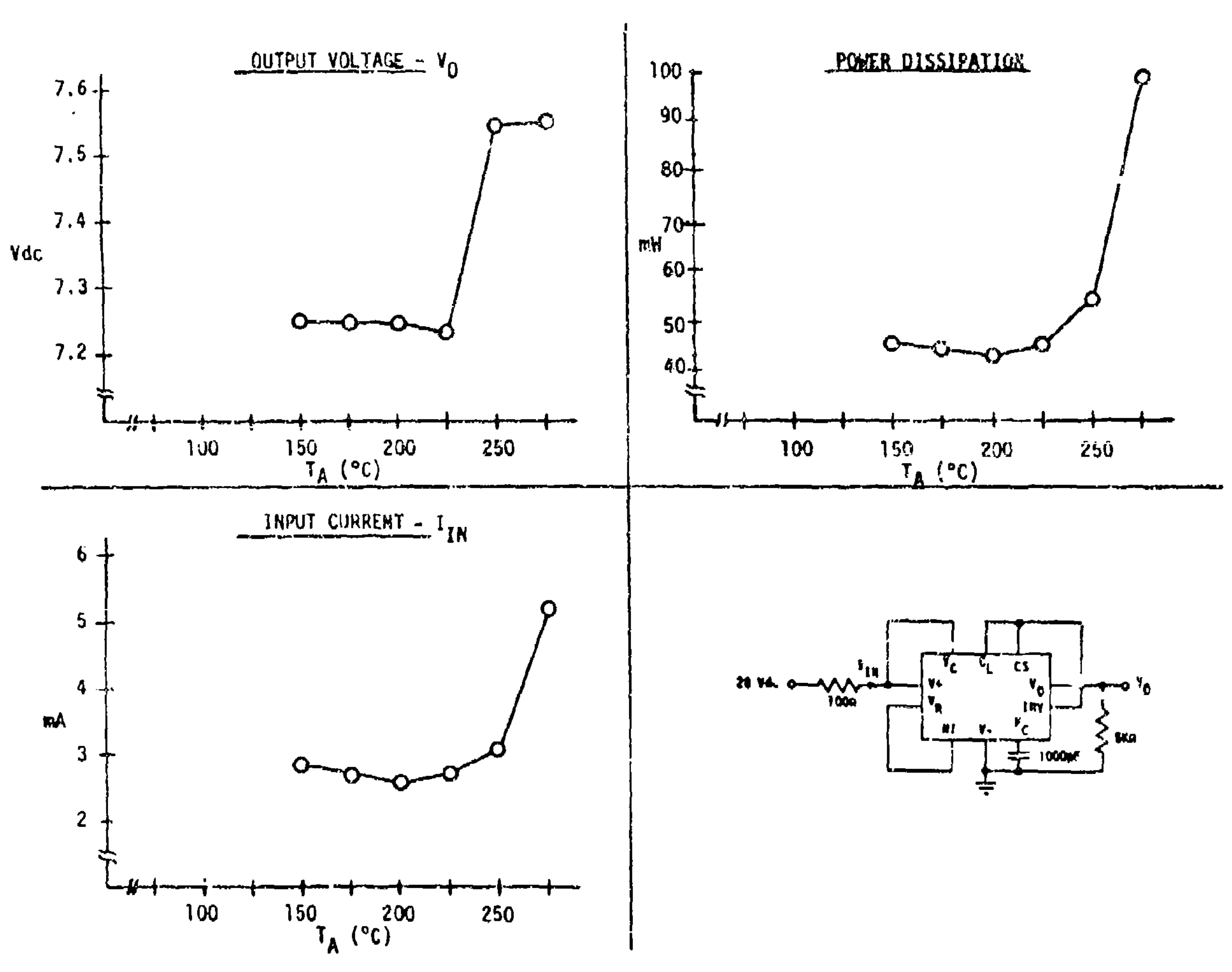


FIGURE D6. MANUFACTURER D MIL-M-38510/10201 (723) CIRCUIT EVALUATION

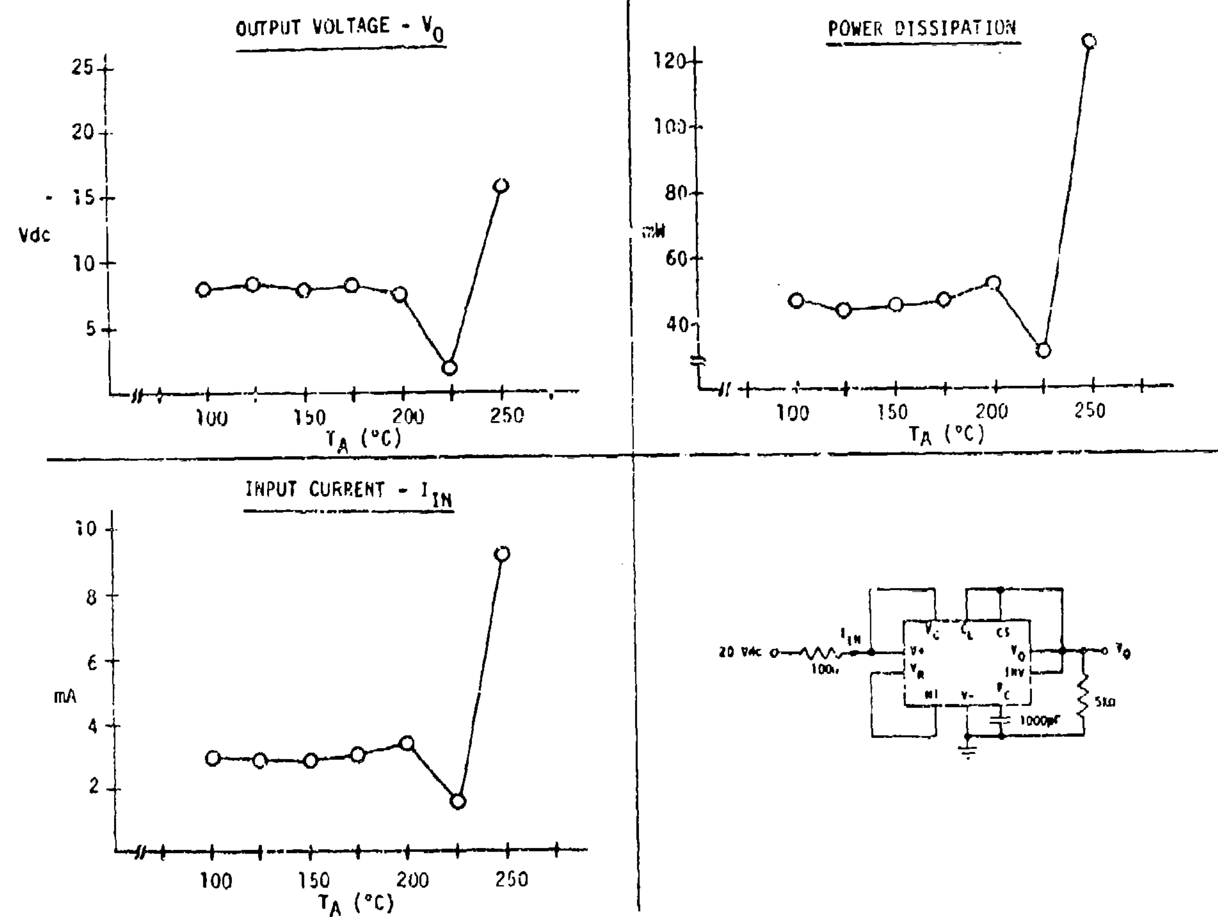


FIGURE D7. MANUFACTURER C MIL-M-38510/10201 (723) CIRCUIT EVALUATION

5.0 MIL-M-38510/10701 (LM109) EVALUATION

Operation of five of each manufacturer's LM109 devices in the MIL-M-38510/10701 accelerated life test bias circuit indicated that the circuit configuration was satisfactory for life testing at ambient temperatures between 200°C and 250°C. Results of the LM109 bias circuit evaluation (average performance of five devices) are shown in Figures D8 and D9, and indicate the devices are in their thermal shutdown mode above 175°C. Although this is not the normal mode of operation, most of the microcircuit junctions, especially the failure prone input transistor junctions, are stressed in a manner similar to normal operation. The output voltage also remains low (≈1 Vdc) above 200°C, and the total device current is less than 10 mA. Thus, the circuit meets the established criteria for an accelerated life test circuit at ambient temperatures of 250°C, 225°C, and 200°C.

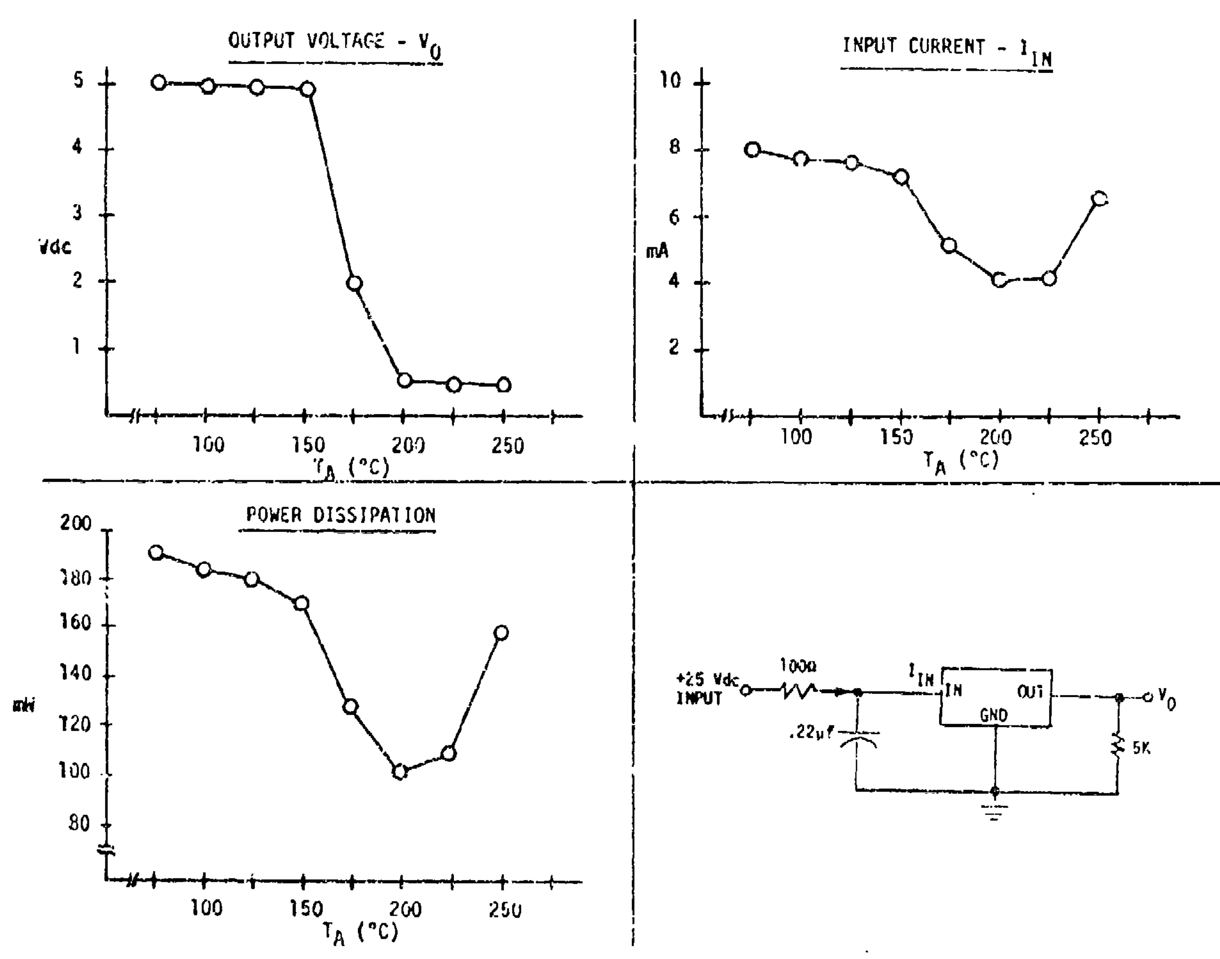


FIGURE D8. MANUFACTURER E MIL-M-38510/10701 (LM109) CIRCUIT EVALUATION

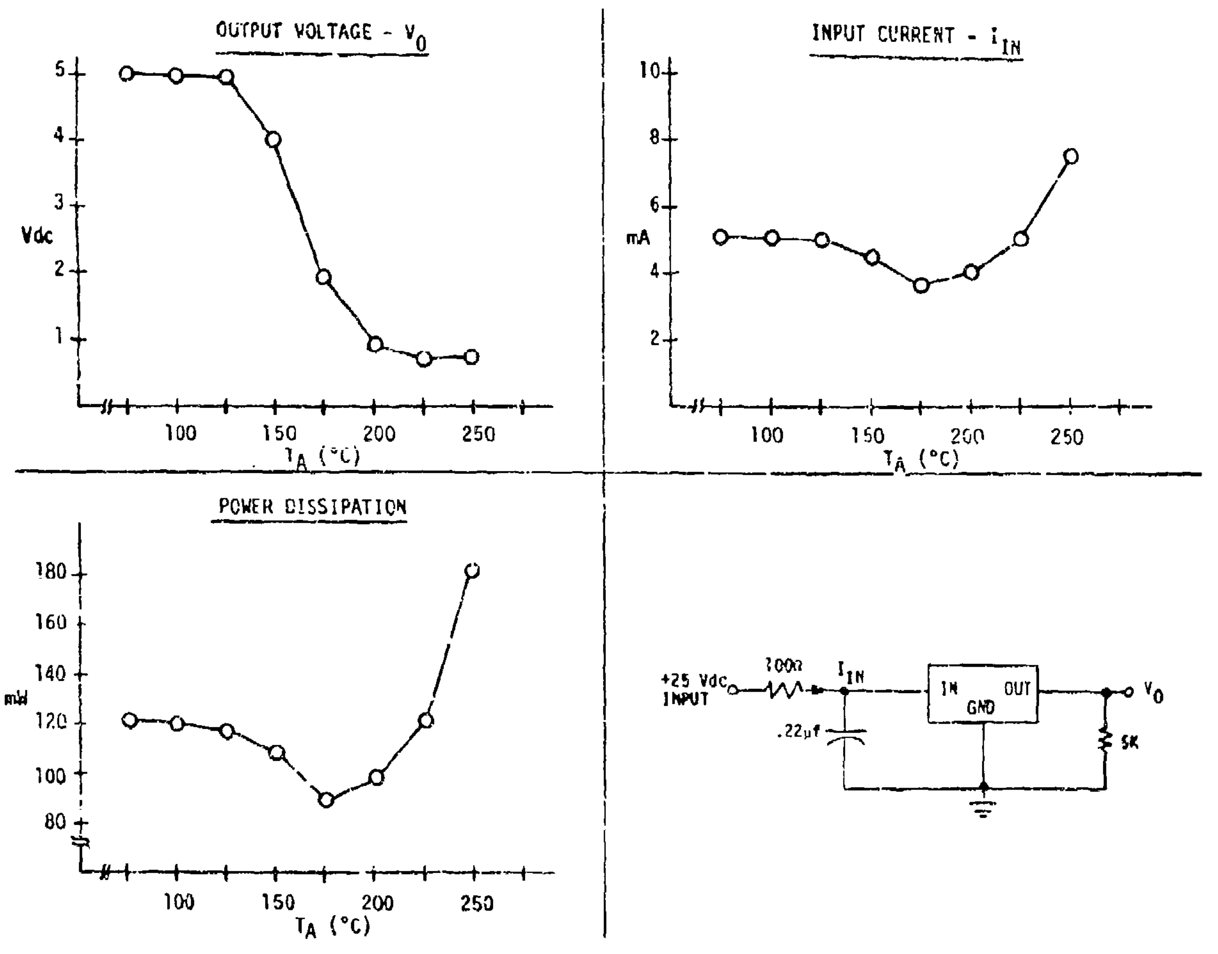
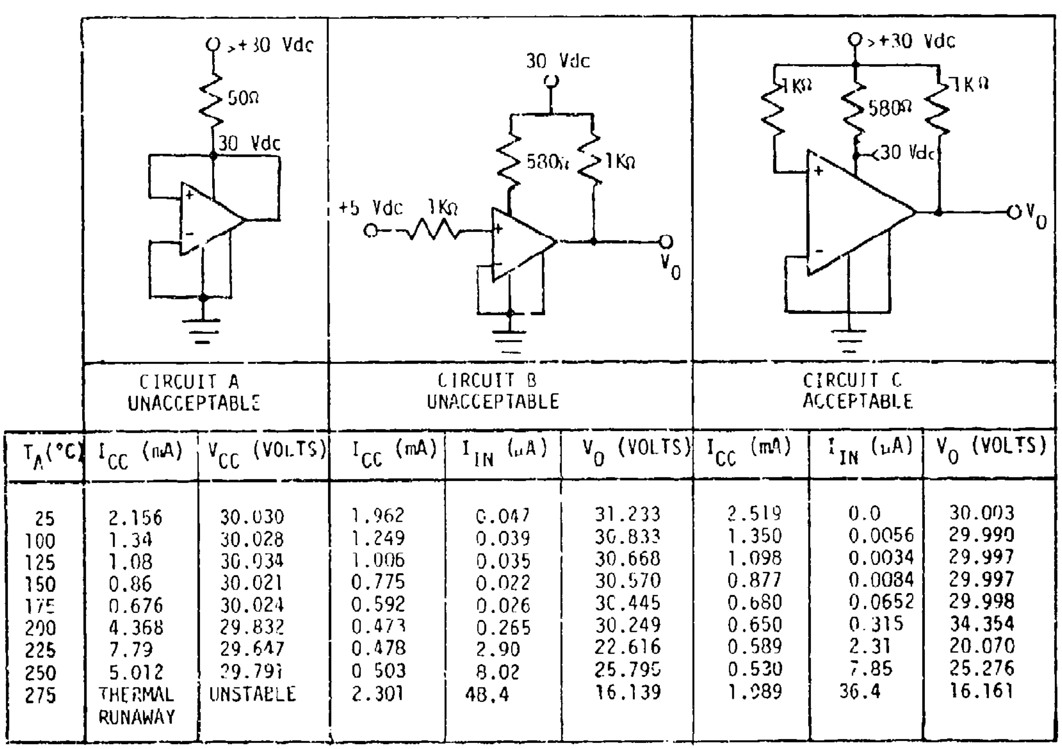


FIGURE D9. MANUFACTURER D MIL-M-38510/10701 (LM109) CIRCUIT EVALUATION

6.0 MIL-M-38510/10304 (LM111) EVALUATION

Operation of LM111 devices in the MIL-M-38510/103A accelerated life test circuit shown as Circuit A of Figure D10 indicated the circuit was not acceptable for use as an accelerated life test circuit. In this circuit the output was tied directly to V_{CC}, which forced the output to a high state and caused the device to draw excessive current at temperatures above 200°C. The circuit was modified, as shown in Circuit B of Figure D10, to current limit the input and output pins. Although this circuit operated acceptably, the circuit was modified at the request of RADC to apply the maximum voltage stress at the inputs. This circuit was evaluted, Circuit C of Figure D10, and operated satisfactorily up to 250°C. The results of the bias circuit evaluation on this circuit are shown in Figures D11 and D12. However, to maintain the output current to a reasonable level if the device should fail with the output in a low state, the resistor tied to the output was changed from 1K to 5K ohms for life testing. The input current was not sufficient to warrant a current limiting resistor; therefore, it was removed from the positive input (pin two) and this input was connected to V_{CC} at pin eight. The final life test circuit is shown in Figure D13. The life test temperatures were selected to be 250°C, 225°C, and 200°C.



	CIRCUIT A UNACCEPTABLE		CIRCUIT B UNACCEPTABLE			CIRCUIT C ACCEPTABLE		
T_A (°C)	I_{CC} (mA)	V_{CC} (VOLTS)	I_{CC} (mA)	I_{IN} (μA)	V_0 (VOLTS)	I_{CC} (mA)	I_{IN} (μA)	V_0 (VOLTS)
25	2.156	30.030	1.962	0.047	31.233	2.519	0.0	30.003
100	1.34	30.028	1.249	0.039	30.833	1.350	0.0056	29.990
125	1.08	30.034	1.006	0.035	30.668	1.098	0.0034	29.997
150	0.86	30.021	0.775	0.022	30.570	0.877	0.0084	29.997
175	0.676	30.024	0.592	0.026	30.445	0.680	0.0652	29.998
200	4.368	29.832	0.473	0.265	30.249	0.650	0.315	34.354
225	7.79	29.647	0.478	2.90	22.616	0.589	2.31	20.070
250	5.012	29.791	0.503	8.02	25.795	0.530	7.85	25.276
275	THERMAL RUNAWAY	UNSTABLE	2.301	48.4	16.139	1.089	36.4	16.161

AVERAGE VALUES FOR 5 DEVICES

FIGURE D10. MIL-M-38510/10304 (LM111) CANDIDATE BIAS CIRCUITS

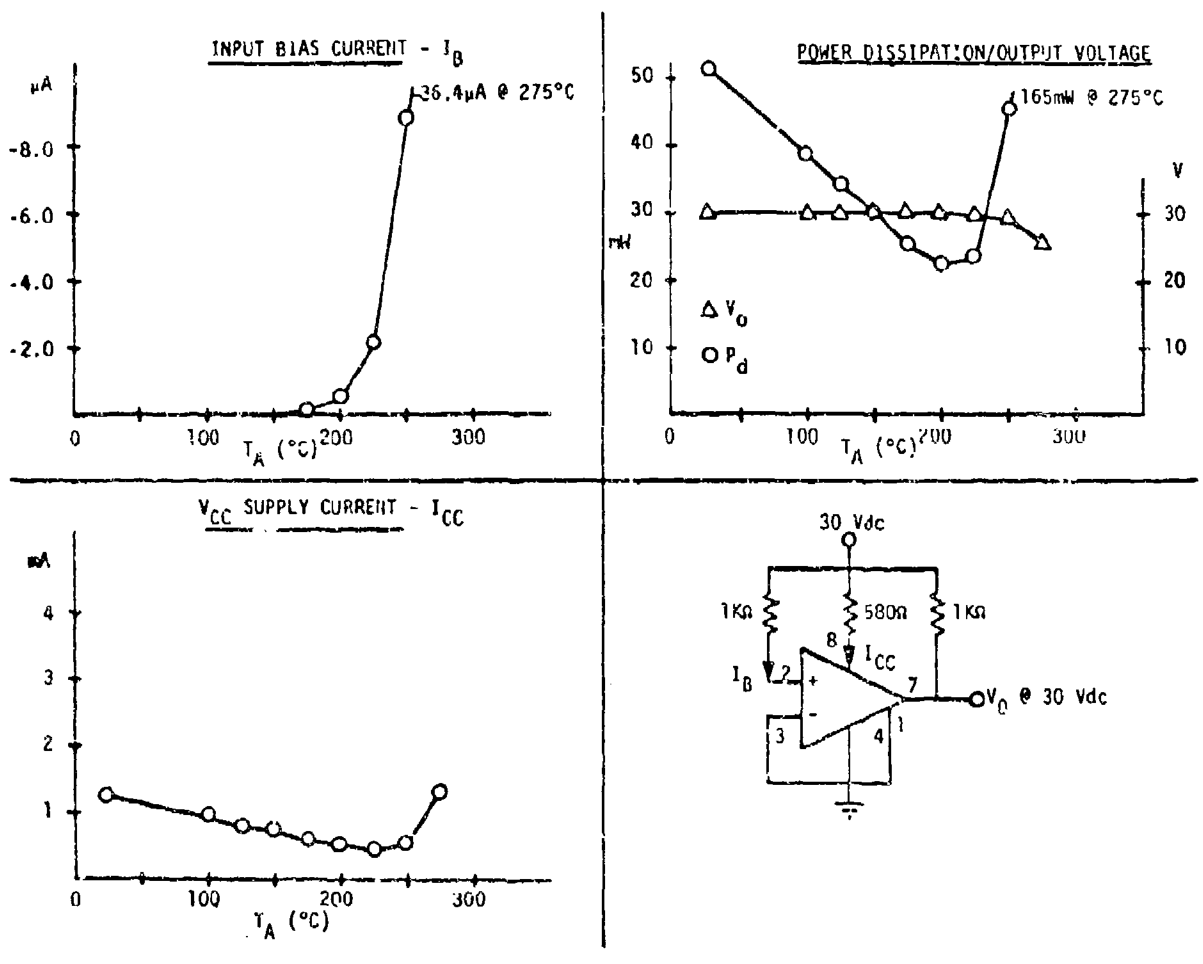


FIGURE D11. MANUFACTURER B M38510/10304 (LM111) CIRCUIT EVALUATION

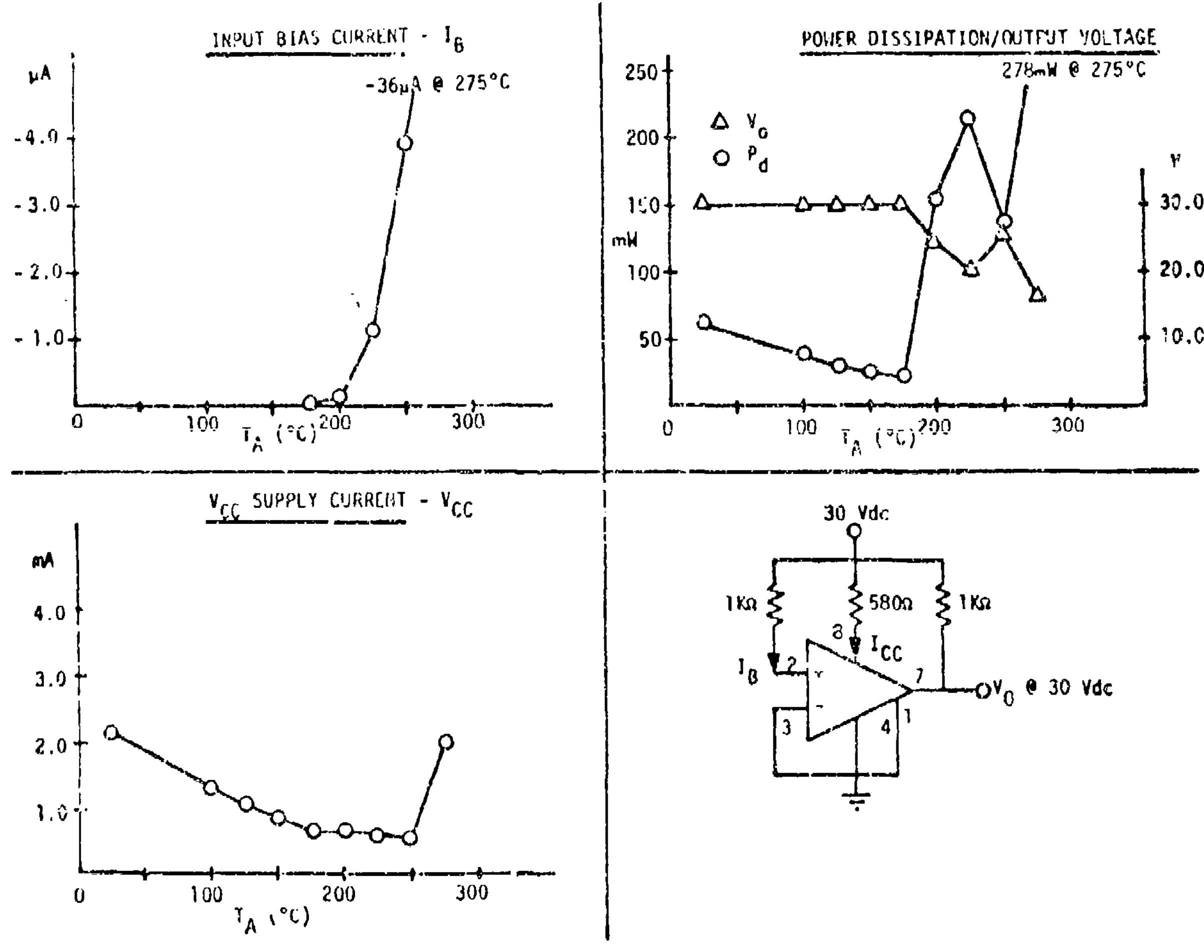


FIGURE D12. MANUFACTURER D M38510/10304 (LM111) CIRCUIT EVALUATION

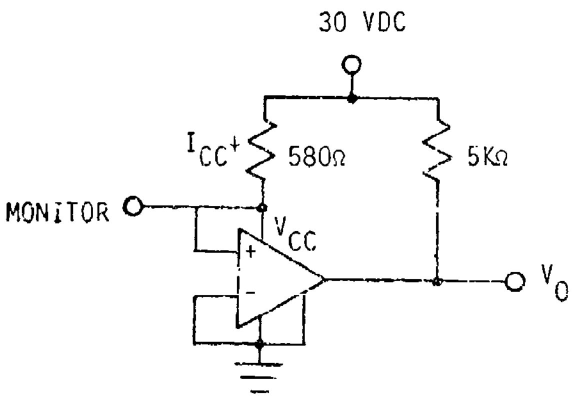


FIGURE D13. M38510/10304 LIFE TEST CIRCUIT

APPENDIX E

CHARACTERIZATION TESTS

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2.0	DYNAMIC TEST RESULTS	E3
3.0	RESULTS OF TRANSFER CHARACTERISTIC STUDY	E13
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1.0 INTRODUCTION

Characterization tests were performed to supplement the device electrical performance information obtained during initial electrical testing. The characterization testing was performed on a sample basis and consisted of two test groups: dynamic testing, and transfer characteristic studies. The dynamic test group consisted of ten of each manufacturer's device type that had passed the initial baseline tests. These devices were subjected to all the MIL-M-38510 Group A tests not performed during baseline testing. Although these devices were tested to the MIL-M-38510 specifications, only one device, the Manufacturer D 723 device, was a JAN qualified device. This may account for the large number of failures noted in the dynamic testing. The transfer characteristic group consisted of two of each manufacturer's device type. The transfer characteristics of these devices were examined under various conditions of temperature, load, voltage and frequency.

2.0 DYNAMIC TEST RESULTS

The results of subjecting ten of each manufacturer's device type in the MIL-M-38510 dynamic test subgroups are contained in the following sections. The dynamic tests subgrouns are those contained in the specific revision of MIL-M-38510 shown in Table E1. Subsequent amendments and revisions of the particular MIL-M-38510 documents have revised the limits, and in some cases the conditions for the dynamic subgroups. In most cases, the revisions have widened the limits so that more devices would now pass these tests. The results of subjecting ten of each manufacturer's device type to the MIL-M-38510 dynamic test subgroups are as follows:

2.1 MIL-M-38510/10104 (LM108A)

The results of the dynamic tests for the LM108A device are summarized in Table E2. Five of Manufacturer B's devices failed the transient response overshoot test at 25°C and all ten devices failed at 125°C. Figures E1 and E2 show the transient response curve of a typical good Manufacturer A device and of a failed Manufacturer B device at 125°C. The Manufacturer B device exhibited considerably more ringing and higher overshoot than Manufacturer A's devices. Five of Manufacturer A's devices and two of Manufacturer B's devices also failed the positive slew rate test at -55°C. Two additional Manufacturer A's devices also failed the three Input Offset Current Sensitivity tests at -55°C.

2.2 MIL-M-38510/10107 (LM118)

Table E3 shows the results of the LM118 dynamic tests. Nine devices from Manufacturer C failed the 25°C and 125°C positive slew rate test. One device of each manufacturer was inadvertently destroyed during the positive slew rate test at 25°C. Also, there were four Manufacturer C failures at -55°C. The minimum for this test was 75V/μs. Nine of Manufacturer C's devices also failed the negative slew rate test. Comparison of the two manufacturer's devices as to slew rate indicate that Manufacturer B's devices are faster and have less sensitivity to temperature for this particular test. All Manufacturer C's

TABLE E1. M38510 SPECIFICATION USED FOR DYNAMIC TESTING

MIL-M-38510 SPECIFICATION	REVISION
/101	D - 15 September 1975
/102	A - 10 May 1974
/103	B - 8 March 1977
/107	A - 15 November 1977

TABLE E2. MIL-M-38510/10104 (LM108A) CHARACTERIZATION TEST SUMMARY

Parameter		Temperature (°C)	Manuf. A			Manuf. B			Units
			Mean	Sigma	No. Failed	Mean	Sigma	No. Failed	
Transient Response Rise Time	$TR_{(tr)}$	25	387.0	23.36	0	362.5	13.59	0	ns
		125	332.5	14.39	0	366.0	12.20	0	
		-55	477.5	134.0	0	55[illegible].5	56.34	0	
Transient Response Overshoot	$TR_{(os)}$	25	12.7	2.4	0	40.3	2.3	5	%
		125	22.6	3.5	0	[illegible]5.5	1.8	10	
		-55	8.6	2.8	0	21.[illegible]	3.0	0	
Slew Rate	SR (+)	25	.133	.016	0	.[illegible]90	.013	0	V/μs
		125	.154	.015	0	.223	.013	0	
		-55	.095	.028	5	.[illegible]10	.012	2	
Slew Rate	SR (-)	25	.171	.01[illegible]	0	.220	.014	0	V/μs
		125	.238	.012	0	.257	.0[illegible]7	0	
		-55	.124	.034	0	.128	.010	0	
Input Offset Voltage Temperature Sensitivity	$\Delta V_{IO}(-15)/\Delta T$	125	.675	.867	0	.525	.921	0	μV/°C
		-55	.384	1.157	0	1.184	1.667	0	
Input Offset Voltage Temperature Sensitivity	$\Delta V_{IO}(+15)/\Delta T$	125	.675	.705	0	.250	.935	0	μV/°C
		-55	.319	.947	0	.994	1.609	0	
Input Offset Voltage Temperature Sensitivity	$\Delta V_{IO}(0)/\Delta T$	125	.751	.772	0	.470	.920	0	μV/°C
		-55	.301	1.004	0	1.036	1.612	0	
Input Offset Current Sensitivity	$\Delta I_{IO}(-15)/\Delta T$	125	-.189	.382	0	.243	.479	0	pA/°C
		-55	.938	1.653	2	.008	.151	0	
Input Offset Current Sensitivity	$\Delta I_{IO}(+15)/\Delta T$	125	-.062	.406	0	-.045	.209	0	pA/°C
		-55	.940	.940	2	.044	.174	0	
Input Offset Current Sensitivity	$\Delta I_{IO}(0)/\Delta T$	125	-.141	.406	0	.135	.337	0	pA/°C
		-55	.836	1.784	2	.048	.167	0	
			TOTAL FAILED		7	TOTAL FAILED		10	

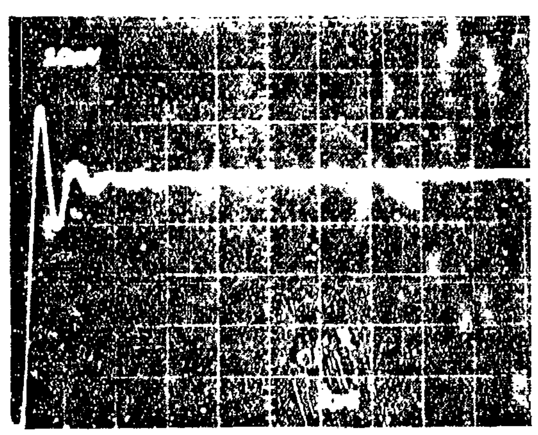


FIGURE L1. TYPICAL CURVE OF NORMAL MANUFACTURER A LM108A TRANSIENT RESPONSE AT 125°C

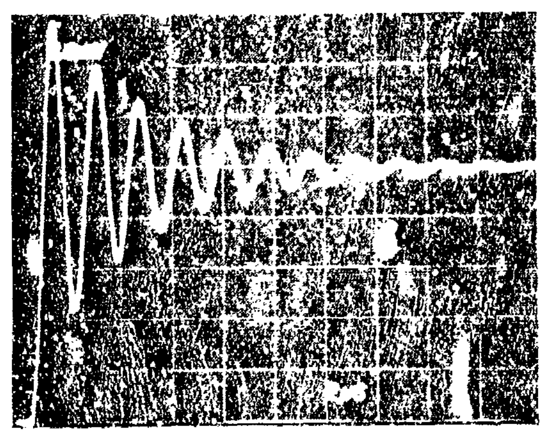


FIGURE L2. CURVE OF MANUFACTURER B LM108A FAILING TRANSIENT RESPONSE TEST AT 125°C

TABLE E3. MIL-M-38510/10107 (LM118) CHARACTERIZATION TEST SUMMARY

Parameter		Temperature (°C)	Manuf. C Mean	Manuf. C Sigma	Manuf. C No. Failed	Manuf. B Mean	Manuf. B Sigma	Manuf. B No. Failed	Units
Transient response rise time	$TR_{(tr)}$	25	23.10	0.782	0	17.00	1.000	0	ns
		125	27.00	2.872	0	20.78	1.641	0	
		-55	22.30	1.000	0	16.33	1.000	0	
Transient reponse overshoot	$TR_{(os)}$	25	6.800	1.398	0	6.0	0.943	0	%
		125	13.00	1.944	0	17.60	1.578	0	
		-55	4.300	0.483	0	[illegible].500	0.527	0	
Slew rate	SR (+)	25	59.41	8.608	9	117.2	7.040	0	V/μs
		125	[illegible]0.39	16.26	9	104.9	5.604	0	
		-55	73.18	7.609	4	118.7	6.959	0	
Slew rate	SR (-)	25	61.44	9.509	1	75.51	3.064	0	V/μs
		125	39.08	7.259	9	81.49	2.209	0	
		-55	77.08	8.022	0	81.66	2.765	0	
Input offset voltage temperature sensitivity	$\Delta V_{IO}(-15)/\Delta T$	125	25.02	3.428	10	6.359	5.009	0	μV/°C
		-55	44.43	12.69	10	17.59	9.408	6	
"	$\Delta V_{IO}(+15)/\Delta T$	125	25.62	3.234	10	7.258	5.263	0	μV/°C
		-55	46.68	13.23	10	15.76	10.30	6	
"	$\Delta V_{IO}(0)/\Delta T$	125	25.62	3.401	10	6.593	5.172	0	μV/°C
		-55	44.85	12.88	10	17.82	9.558	6	
Input offset current temperature sensitivity	$\Delta I_{IO}(-15)/\Delta T$	125	35.31	11.27	0	28.74	37.18	0	pA/°C
		-55	-26.19	293.1	1	36.39	74.34	0	
"	$\Delta I_{IO}(+15)/\Delta T$	125	12.25	16.10	0	40.60	68.[illegible]	0	pA/°C
		-55	32.16	41.99	0	48.85	92.02	0	
"	$\Delta I_{IO}(0)/\Delta T$	125	31.17	28.89	0	44.14	55.39	0	pA/°C
		-55	-5.128	142.8	0	40.35	76.58	0	
Settling time	ts (+)	25	385.0	43.96	0	279.0	34.79	0	ns
		125	392.5	102.0	0	992.0	180.8	0	
		-55	356.[illegible]	24.95	0	256.0	29.23	0	
"	ts (-)	25	469.0	17.45	0	322.5	107.5	0	ns
		125	580.5	33.04	0	490.0	149.7	0	
		-55	390.5	20.06	0	292.5	48.16	0	
			TOTAL FAILED		10	TOTAL FAILED		6	

1. One device of each manufacturer was accidentally electrically damaged in the test setup reducing this sample size to nine (9) devices.

devices also failed the Input Offset Voltage Temperature Sensitivity Test and six of Manufacturer B's devices failed the 25°C to -55°C portions of this test. As can be seen from the data, the offset voltage of Manufacturer C's devices is more than twice as sensitive to temperature as the offset voltage of the other manufacturer's devices.

2.3 MIL-M-38510/10201 (723)

The results of the 723 dynamic tests are shown in Table E4. All of Manufacturer C's devices and four of Manufacturer D's devices failed the Line Transient Response test. The four Manufacturer D failed devices are only slightly out-of-tolerance, while the parameter value of Manufacturer C's failures are an order of magnitude greater than Manufacturer D's failed values.

2.4 MIL-M-38510/10701 (LM109)

The results of the dynamic tests for the LM109 devices are shown in Table E5. One of Manufacturer D's devices failed the Average Temperature Coefficient of Output Voltage test at 25°C to 125°C, and eight failed the same test in the 25°C to -55°C temperature differential. The Manufacturer D failures in the 25°C to -55°C differential test, however, were the results of start-up problems in the -55°C tests. The V_{OUT} test for these devices failed at -55°C due to start-up problems at this temperature. Three of Manufacturer B's devices failed this same test in the 25°C to +125°C temperature differential. Nine of Manufacturer D's devices also failed Ripple Rejection at 125°C and 100 kHz. Two of these devices also failed Ripple Rejection at -55°C and 100 kHz. All Ripple Rejection failed values were only slightly below the 60db minimum limit and except for one failed value all of the values were less than 60-0.5dB. This device subsequently failed both the 125°C and the -55°C Ripple Rejection tests. Also, five of Manufacturer D's devices failed the Load Transient Response test at 25°C and all this manufacturer's devices failed the test at 125°C and -55°C. All of Manufacturer B's devices also failed the -55°C portion of this test. Manufacturer D's devices were very sensitive to load transients. Both manufacturers exhibited sensitivity to load at -55°C.

TABLE E4. MIL-M-38510/10201 (723) CHARACTERIZATION TEST SUMMARY

Parameter	Ambient Test Temp.		Manuf. D			Manuf. C			Units
			Mean	Sigma	No. Failed	Mean	Sigma	No. Failed	
Average Temp. Coefficient of Output Voltage (TC_{Vout})	125°C		0.006	0.001	0	0.002	0.001	0	%/°C
	-55°C		0.009	0.001	0	0.006	0.001	0	%/°C
Ripple Rejection $\left(\frac{\Delta Vin}{\Delta Vout}\right)$	25°C	C_{REF}= 5µF	87.23	1.612	0	90.43	2.264	0	dB
	25°C	C_{REF}= 0µF	77.85	1.567	0	77.66	4.091	0	dB
Output Noise (N_o)	25°C	C_{REF}= 5µF	2.560	0.640	0	2.270	0.380	0	µV
	25°C	C_{REF}= 0µF	42.50	32.90	0	42.40	27.70	0	µV
Line Transient Response $\left(\frac{\Delta Vout}{\Delta Vin}\right)$	25°C		1.107	0.180	5	12.70	7.25	10	$\frac{mV}{V}$
Load Transient Response $\left(\frac{\Delta Vout}{\Delta I_L}\right)$	25°C		-0.102	0.004	0	-0.071	0.006	0	$\frac{mV}{mA}$
			TOTAL FAILED		5	TOTAL FAILED		10	

TABLE E5. MIL-M-38510/10701 (LM109) CHARACTERIZATION TEST SUMMARY

Parameter		Test Ambient		Manufacturer D			Manufacturer B			Units
				Mean	Sigma	Number Failed	Mean	Sigma	Number Failed	
Average Temperature Coefficient of Output Voltage	$\frac{\dot{V}_{OUT}}{T}$	125°C		0.59	0.31	1	0.99	0.99	3	mV/°C
		-55°C		30.2	23.5	8	0.52	0.14	0	
Ripple Rejection	$\frac{V_{IN}}{V_{OUT}}$	25°C	10 Hz	82.7	6.25	0	68.0	0.78	0	dB
			100 kHz	61.8	1.47	2	74.0	0.90	0	
		125°C	10 Hz	78.7	4.51	0	66.6	1.20	0	
			100 kHz	58.8	0.78	9	65.8	0.56	0	
		-55°C	10 Hz	78.4	5.07	0	66.0	0.78	0	
			100 kHz	61.6	2.98	2	80.8	0.84	0	
Output Noise	N_O	25°C		41.9	1.79	0	27.0	1.05	0	μV
Line Transient Response	$\frac{V_{OUT}}{V_{IN}}$	25°C		1.72	0.12	0	0.78	.54	0	mV/V
		125°C		1.09	0.14	0	1.07	0.12	0	
		-55°C		1.95	0.10	0	1.34	1.97	0	
Load Transient Response	$\frac{V_{OUT}}{I_L}$	25°C		1.49	0.73	5	0.52	0.08	0	mV/mA
		125°C		1.28	0.03	10	0.79	0.03	0	
		-55°C		17.4	5.17	10	11.05	3.58	10	
Current Limiting Point	I_{CL}	25°C		-.93	0.05	0	-.98	0.00	0	A
Thermal Shutdown Point	$T_{J(sh)}$	--		162.2	3.59	0	179.0	5.16	0	°C
				TOTAL FAILED		10	TOTAL FAILED		10	

2.5 MIL-M-38510/10304 (LM111)

The results of the LM111 dynamic test results are shown in Table E6. One Manufacturer D device failed the t_{RHLC} test at 25°C. While at 125°C, nine of Manufacturer D's devices and ten of Manufacturer B's devices also failed the t_{RLHC} test. Two additional Manufacturer D device failures occurred at 125°C during the t_{RLHE} tests.

The current MIL-M-38510/10304 (8 March 1977) does not include the emitter response time tests (t_{RLHE} or t_{RHLE}) and the test limits for the 125°C collector response time were expanded. Seven Manufacturer B devices and two Manufacturer D devices would pass the revised t_{RLHC} tests at 125°C.

TABLE E6. MIL-M-38510/10304 (LM111) CHARACTERIZATION TEST SUMMARY

PARAMETER		TEST AMBIENT	MANUFACTURER B			MANUFACTURER D		
			MEAN	SIGMA	NUMBER FAILED	MEAN	SIGMA	NUMBER FAILED
RESPONSE TIME (COLLECTOR)	t_{RLHC}	25°C	140.0	16.3	0	259.0	50.6	1
		125°C	637.0	109.0	10	986.0	358.0	9
		-55°C	119.0	8.6	0	132.0	9.8	0
	t_{RHLC}	25°C	155.0	10.3	0	165.1	4.7	0
		125°C	259.0	41.9	0	244.0	13.8	0
		-55°C	142.0	8.9	0	148.0	12.6	0
RESPONSE TIME (EMITTER)	t_{RLHE}	25°C	438.0	25.6	0	367.0	20.8	0
		125°C	1338.0	157.0	0	2126.0	944.0	2
		-55°C	348.0	18.0	0	275.0	16.3	0
	t_{RHLE}	25°C	840.0	46.4	0	824.0	50.8	0
		125°C	1544.0	115.0	0	1942.0	126.0	0
		-55°C	571.0	39.2	0	556.0	22.7	0
			TOTAL FAILED		10	TOTAL FAILED		10

3.0 TRANSFER CHARACTERISTIC STUDIES

Device transfer characteristics (output voltage as a function of input voltage) were evaluated to determine the device response to variations in temperature, supply voltage, load conditions, and frequency. Transfer functions were obtained by testing two (2) devices from each manufacturer on a curve tracer or test fixture and varying the conditions such as temperature, frequency, load, and supply voltage. For the regulators (MIL-M-38510/10201 and /10701) and the /10104 operational amplifier varying the load conditions had the most dramatic effect. For the /10107 operational amplifier, varying the temperature produced the more notable effects. The LM111 devices were affected by variations in both load and temperature. The specific test conditions for evaluating device transfer characteristics are detailed in Tables E7 and E8. The particular effects of varying these test conditions are noted in the following sections:

3.1 MIL-M-38510/10104 (LM108A)

Comparison of the two curves shown in Figure E3 revealed that Manufacturer A's devices exhibited much more linearity than Manufacturer B's devices. Non-linearity is caused by differences in the thermal gradient between the output and each of the input transistors. Manufacturer A's die layout has the input transistors criss-crossed as shown in Figure E4, to equalize the thermal effects.

However, the slope of Manufacturer A's device curve is positive, and not the expected negative slope of an ideal amplifier. This inversion of the slope is caused by thermal feedback [1]. Varying the temperature had very little effect on the linearity of Manufacturer B's devices, as is shown in Figure E5. Varying the load had no measureable effect on Manufacturer A's devices but an increase in load resistance, as shown in Figure E6, did tend to reduce the non-linearity of Manufacturer B's transfer curve.

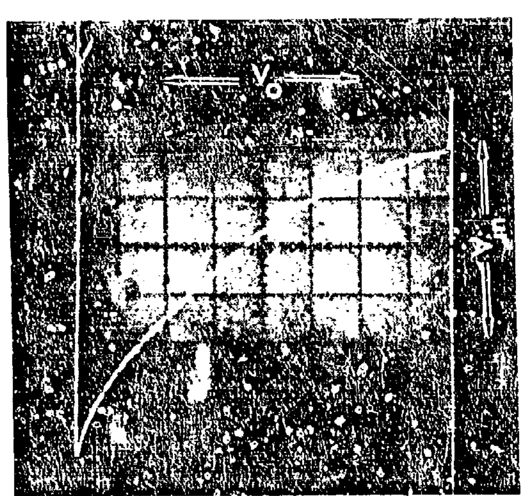
Ideally, an increase in the operating frequency should improve the linearity of the device since effects of thermal gradients are minimized.

TABLE E7. OPERATIONAL AMPLIFIER/COMPARATOR TEST CONDITIONS

DEVICE TYPE	TEST NUMBER	TEST CONDITIONS				
		AMBIENT TEMP. (°C)	LOAD RESISTANCE (ohm)	FREQ (Hz)	POWER SUPPLY (Vdc)	COMMON MODE (Vdc)
LM108A	1	25	20K	0.1	±20.0	0.0
	2	-55	20K	0.1	±20.0	0.0
	3	125	20K	0.1	±20.0	0.0
	4	25	10K	0.1	±20.0	0.0
	5	25	50K	0.1	±20.0	0.0
	6	25	20K	4.0	±20.0	0.0
	7	25	20K	0.1	±12.5	0.0
	8	25	20K	0.1	± 5.0	0.0
	9	25	20K	0.1	±20.0	+10.0
	10	25	20K	0.1	±20.0	-10.0
LM118	1	25	10K	0.1	±20.0	0.0
	2	-55	10K	0.1	±20.0	0.0
	3	125	10K	0.1	±20.0	0.0
	4	25	2K	0.1	±20.0	0.0
	5	25	50K	0.1	±20.0	0.0
	6	25	10K	2.0	±20.0	0.0
	7	25	10K	0.1	±12.5	0.0
	8	25	10K	0.1	± 5.0	0.0
	9	25	10K	0.1	±20.0	+10.0
	10	25	10K	0.1	±20.0	-10.0
LM111	1	25	2K	0.1	±18.0	0.0
	2	-55	2K	0.1	±18.0	0.0
	3	125	2K	0.1	±18.0	0.0
	4	25	1K	0.1	±18.0	0.0
	5	25	10K	0.1	±18.0	0.0
	6	25	2K	3.0	±18.0	0.0
	7	25	2K	1.0K	±18.0	0.0
	8	25	2K	0.1	±12.0	0.0
	9	25	2K	0.1	± 6.0	0.0
	10	25	2K	0.1	±16.0	+12.0
	11	25	2K	0.1	±18.0	-12.0

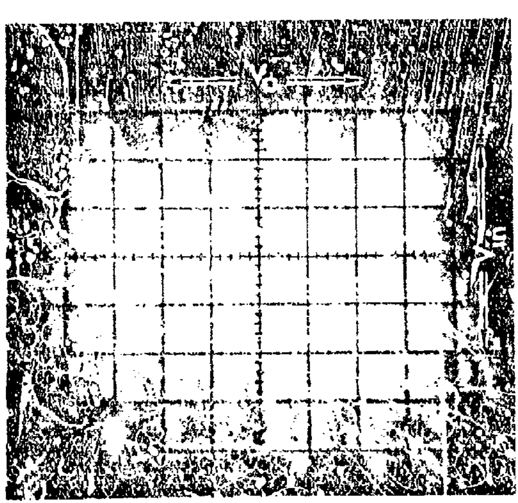
TABLE E8. REGULATOR TEST CONDITIONS

DEVICE TYPE	TEST NUMBER	TEST CONDITIONS		
		AMBIENT TEMP. (°C)	I_L (mA)	FREQ (Hz)
LM109	1	25	5.0	0.1
	2	-55	5.0	0.1
	3	125	5.0	0.1
	4	25	50.0	0.1
	5	25	500.0	0.1
	6	25	5.0	10.0
	7	25	5.0	1000.0
723	1	25	1.0	0.1
	2	-55	1.0	0.1
	3	125	1.0	0.1
	4	25	10.0	0.1
	5	25	50.0	0.1
	6	25	1.0	10.0
	7	25	1.0	1000.0



MANUFACTURER A

V_{IN} = 20μV/DIV. V_O = 5V/DIV.
T_A = 25°C R_L = 20kΩ
V_{CC} = ±20 Vdc V_{CM} = 0 Vdc
Freq. = 0.1 HZ



MANUFACTURER B

FIGURE E3. MIL-M-38510/10104 (LM108A) TRANSFER CHARACTERISTIC COMPARISON

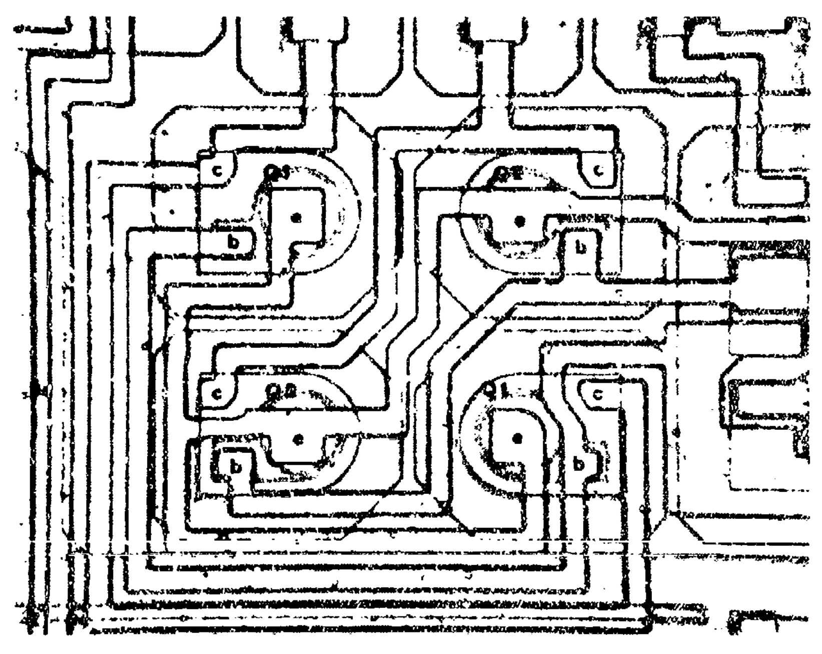
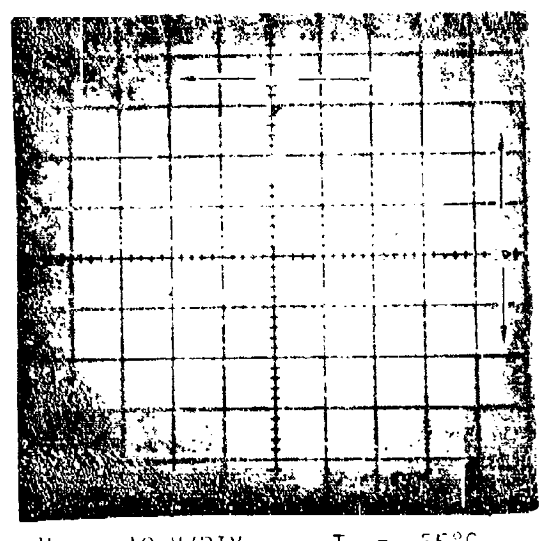
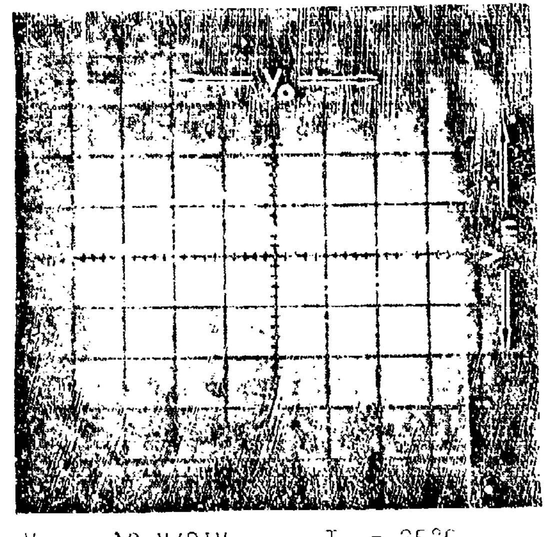


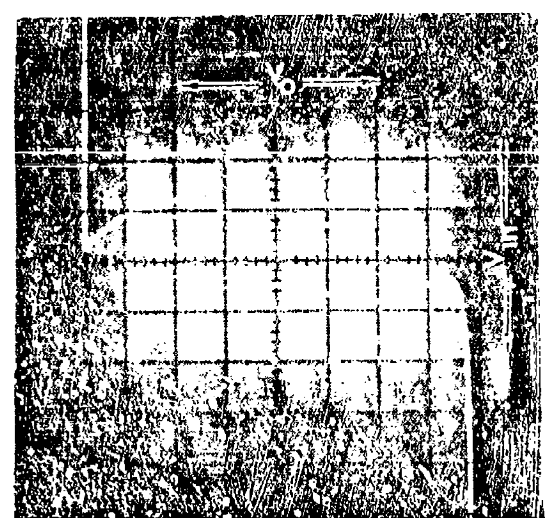
FIGURE E4. MIL-M-38510/10104 (LM108A) MANUFACTURER A INPUT TRANSISTOR CONFIGURATION



V_{IN} = 10μV/DIV. T_A = -55°C



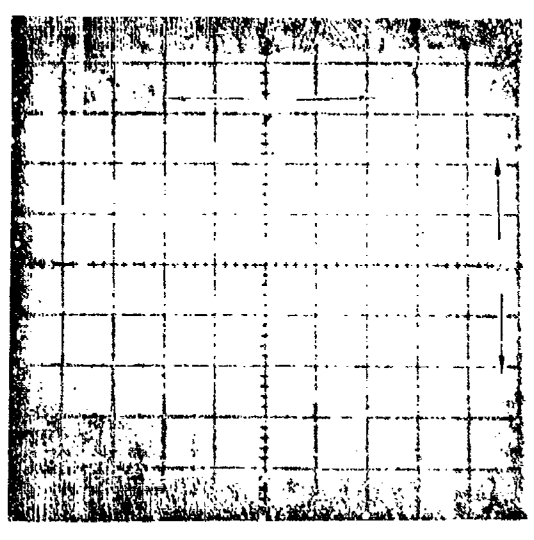
V_{IN} = 10μV/DIV. T_A = 25°C



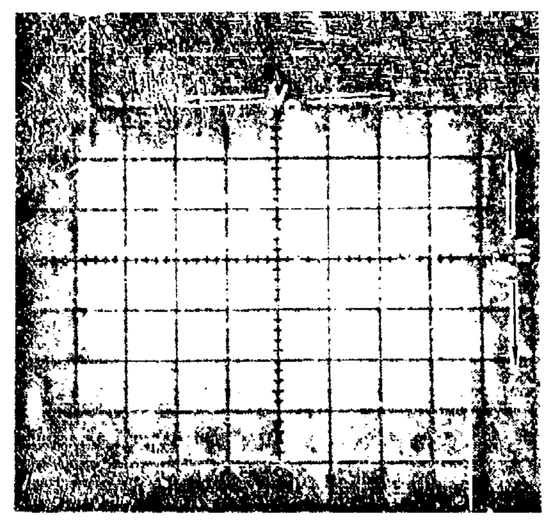
T_A = 125°C

MANUFACTURER B	V_{CC} = ±20 Vdc	V_O = 5V/DIV.
T_A = AS NOTED	V_{CM} = 0 Vdc	V_{IN} = 20μV/DIV.
R_L = 20KΩ	FREQ = 0.1 HZ	(UNLESS NOTED)

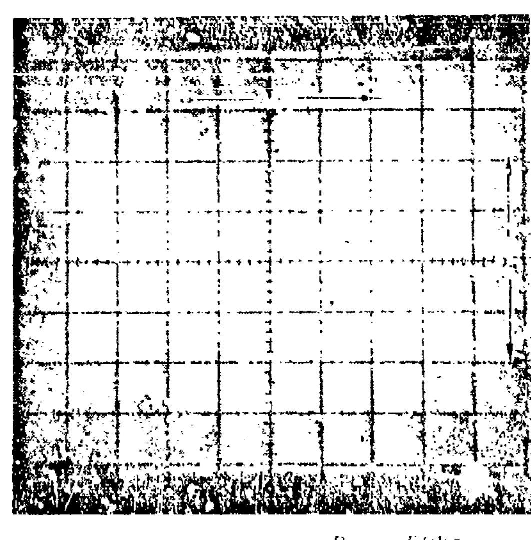
FIGURE F5. M38510/10104 (LM108A) TYPICAL TRANSFER CHARACTERISTICS VS. TEMPERATURE



R_L = 10KΩ



R_L = 20KΩ



R_L = 50kΩ

MANUFACTURER B
T_A = 25°C
R_L AS NOTED

V_{CC} = ±20 Vdc
V_{CM} = 0 Vdc
FREQ = 0.1 HZ

V_O = 5V/DIV.
V_{IN} = 10μV/DIV.

FIGURE 86. M38510/10104 (LM108A) TYPICAL TRANSFER CHARACTERISTICS VS LOAD

However, attempts to obtain transfer curves at frequencies above 1.0 Hz resulted in excessive hysteresis for both manufacturer's devices, as shown in Figure E7. Thus, our test results were inconclusive as to whether the increased frequency would have an effect on the transfer curves.

Varying the device supply voltage had little effect on the slope or linearity of Manufacturer A's device transfer curves, but decreasing the supply voltage did improve the linearity of Manufacturer B's device transfer curves, as shown in Figure E8. However, decreasing the common mode voltage decreased the slope (V_{IN}/ V_0) of the transfer curve and also tended to exaggerate any nonlinearities. Figure E9 shows the operation of Manufacturer A's devices under common mode conditions of +10 Vdc, 0 Vdc, and -10 Vdc.

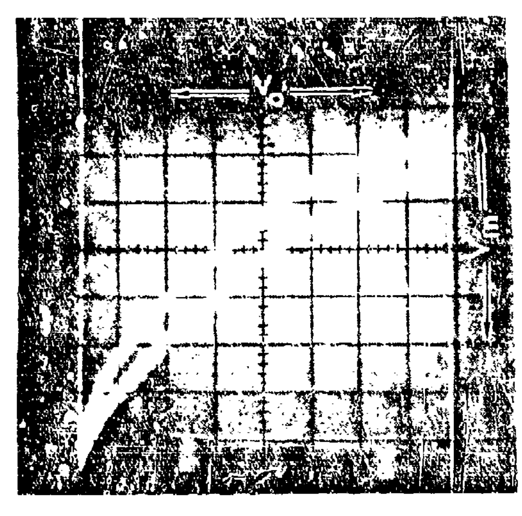
In general, the linearity of the MIL-M-38510/10104 (LM108A) transfer curves was affected by changes in temperature and load. The slope of the LM108A's transfer curve was most affected by changes in common mode voltage.

3.2 MIL-M-38510/10107 (LM118)

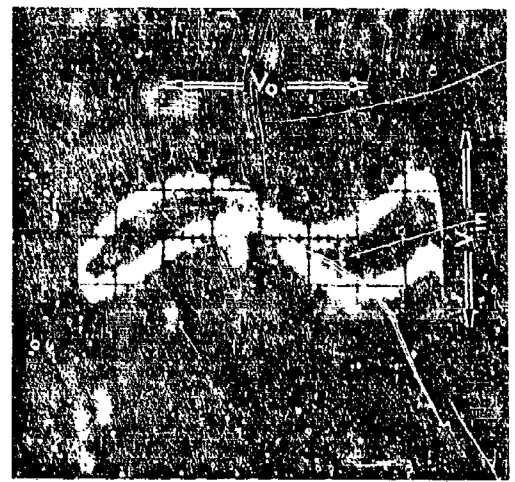
Figure E10 shows the difference in linearity between the two manufacturers of the MIL-M-38510/10107 devices. Although the die layout of Manufacturer C's devices is similar to Manufacturer B's layout, the former transfer curve exhibits much less linearity. Temperature had little effect on either the linearity or the slope of the transfer curve for Manufacturer C's devices, as is shown in Figure E11. However, the curves of Figure E12 show that for Manufacturer B's devices, operating them at -55°C tends to decrease the slope of the curve.

Increasing the load resistance slightly increased the slope of Manufacturer B's devices but had little effect on the linearity of the curves. However, increasing the load resistance of Manufacturer C's devices removed most of the non-linearity, as shown in Figure E13.

Variation in power supply voltage and common mode voltage had minimal effect on the linearity of the transfer plots, as is shown in Figures E14 and



MANUFACTURER A FREQ = 4.0 HZ



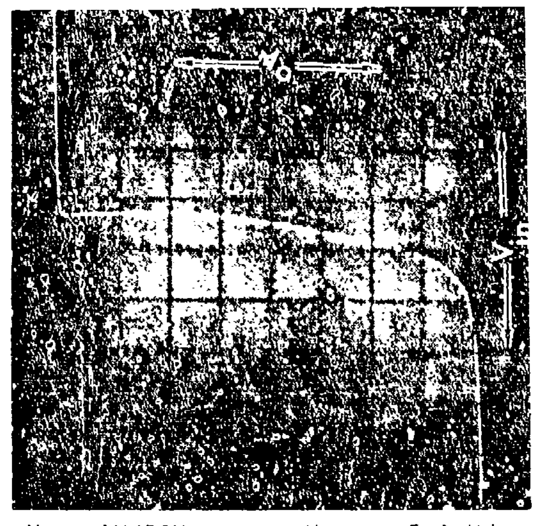
MANUFACTURER B FREQ = 4 HZ

T_A = 25°C
R_L = 20 KΩ

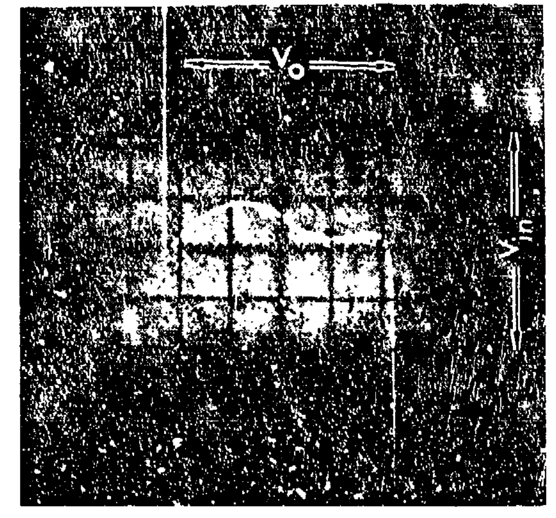
V_{CC} = ±20 Vdc
V_{CM} = 0 Vdc
FREQ AS NOTED

V_O = 5V/DIV.
V_{IN} = 20μV/DIV.

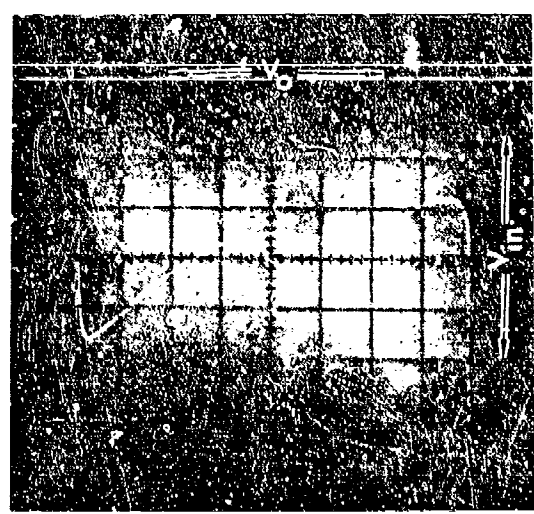
FIGURE E7. M38510/10104 (LM108A) TYPICAL TRANSFER CHARACTERISTICS VS. FREQUENCY



V_0 = 1V/DIV. V_{CC} = $\pm$5.0 Vdc



V_{CC} = $\pm$12.5 Vdc



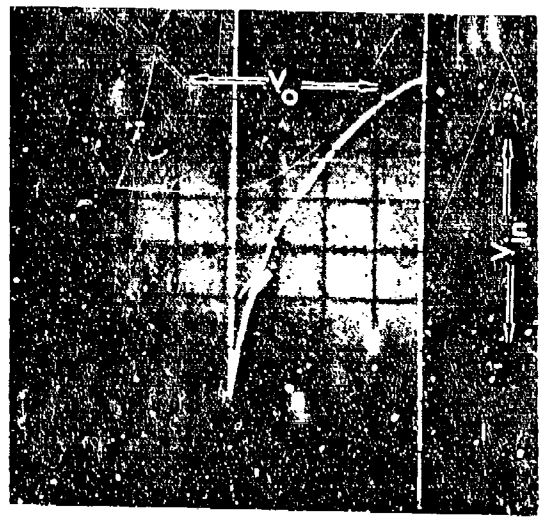
V_{CC} = $\pm$20 Vdc

MANUFACTURER B
T_A = 25°C
R_L = 20K

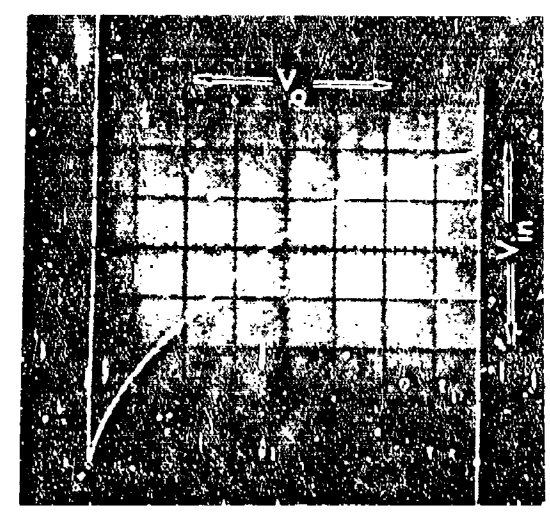
V_{CC} AS NOTED
V_{CM} = 0 Vdc
FREQ. = 0.1 HZ

V_0 = 5V/DIV. (UNLESS NOTED)
V_{IN} = 10μV/DIV.

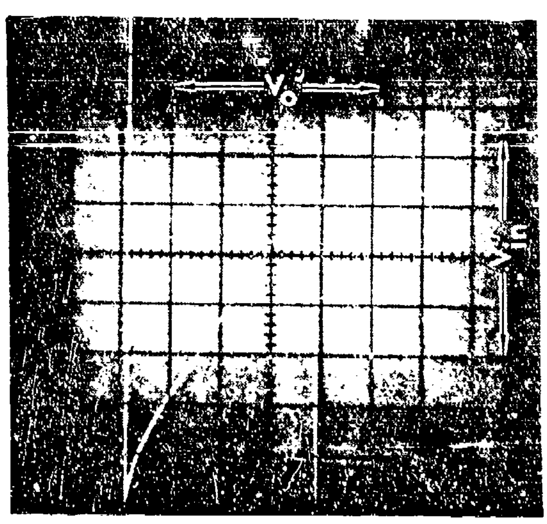
FIGURE E8. M38510/10104 (LM108A) TYPICAL TRANSFER CHARACTERISTICS VS. SUPPLY VOLTAGE



V_{CC} = +30V/-10V V_{CM} = -10 Vdc



V_{CC} = ±20V V_{CM} = 0 Vdc
V_O = 5V/DIV.



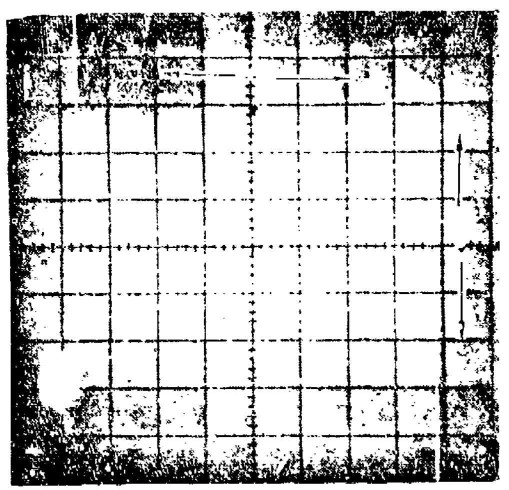
V_{CC} = 10V/-30V V_{CM} = +10 Vdc

MANUFACTURER A
T_A = 25°C
R_L = 20KΩ

V_{CC} AS NOTED
V_{CM} AS NOTED
FREQ = 0.1 HZ

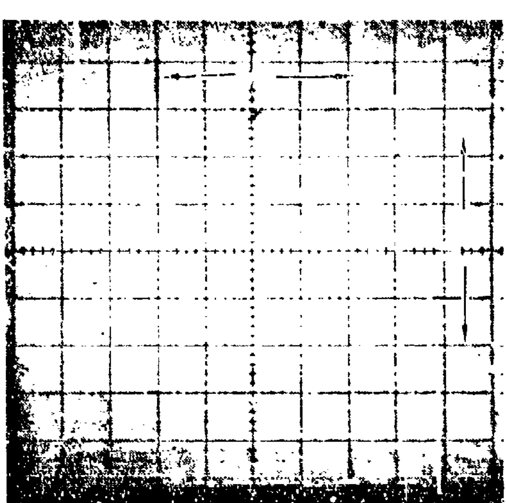
V_O = 10V/DIV. (UNLESS NOTED)
V_{IN} = 20μV/DIV.

FIGURE E9. M38510/10104 (LM108A) TYPICAL TRANSFER CHARACTERISTICS VS. COMMON MODE VOLTAGE



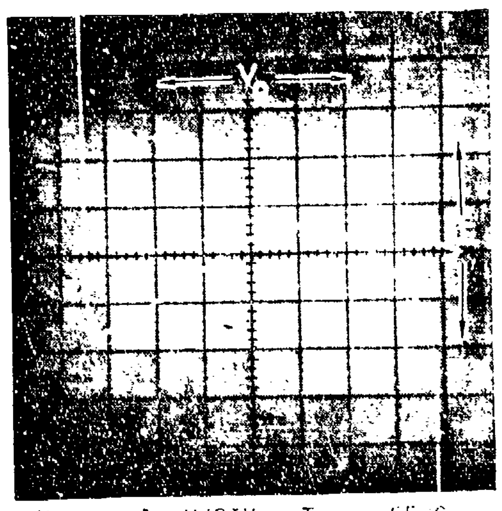
MANUFACTURER B

V_{IN} = 50μV/div. V_O = 5V/div.
T_A = 25°C R_L = 10k
V_{CC} = ±20 Vdc V_{CM} = 0 Vdc
Freq. = 0.1 HZ

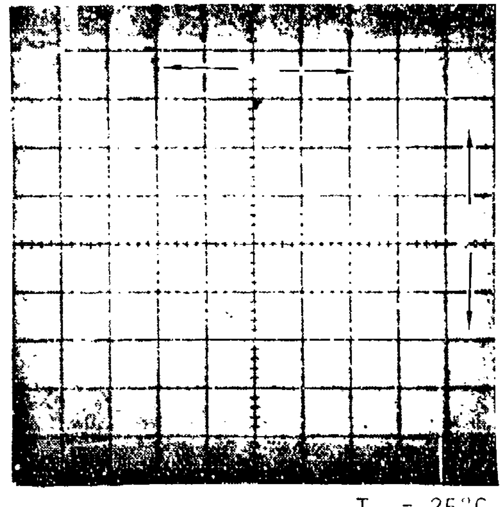


MANUFACTURER C

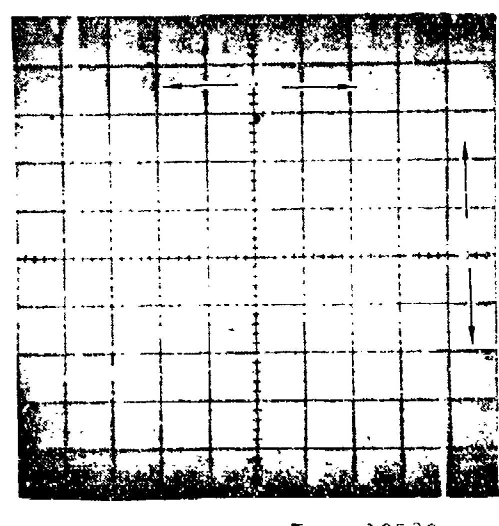
FIGURE L10. MIL-M-38510/10107 (LM113) COMPARISON OF TRANSFER PLOTS



V_{IN} = .1 mV/DIV. T_A = -55°C



T_A = 25°C



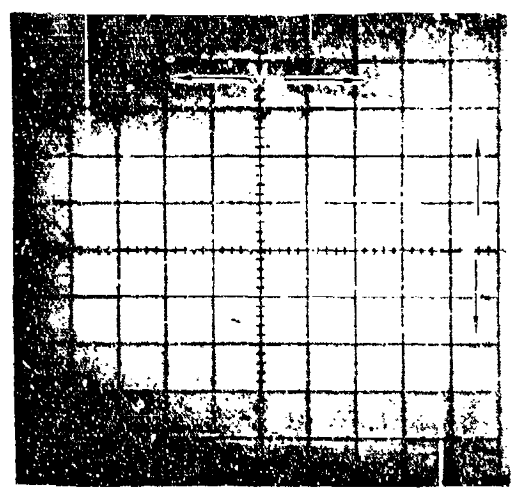
T_A = 125°C

T_A AS NOTED
R_L = 10KΩ

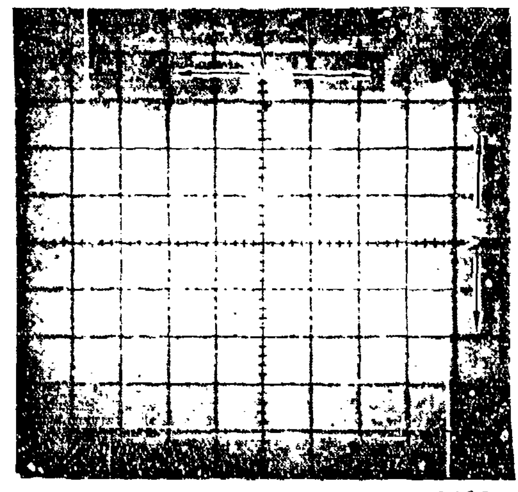
V_{CC} = ±20 Vdc
V_{CM} = 0.0 Vdc
FREQ 0.1 HZ

V_O = 5V/DIV.
V_{IN} = 50μV/DIV.
(UNLESS NOTED)

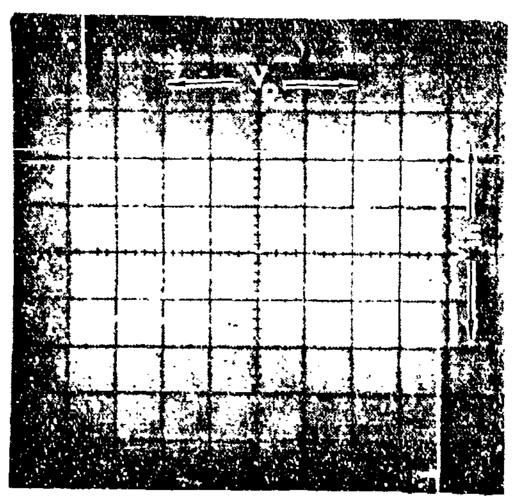
FIGURE E11. M38510/10107 (LM118) TYPICAL MANUFACTURER C TRANSFER CHARACTERISTICS VS. TEMPERATURE



T_A = -55°C



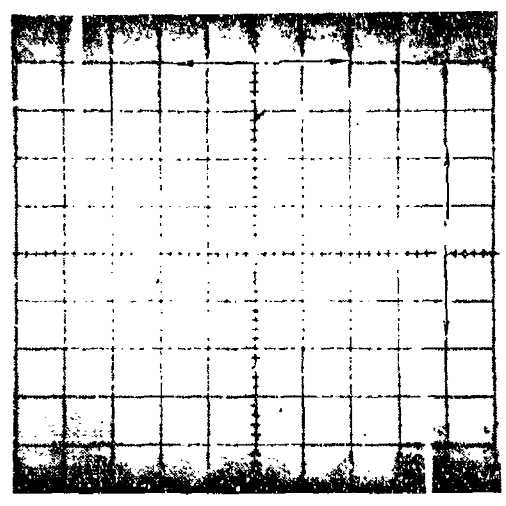
V_{IN} = 50μV/DIV. T_A = 25°C



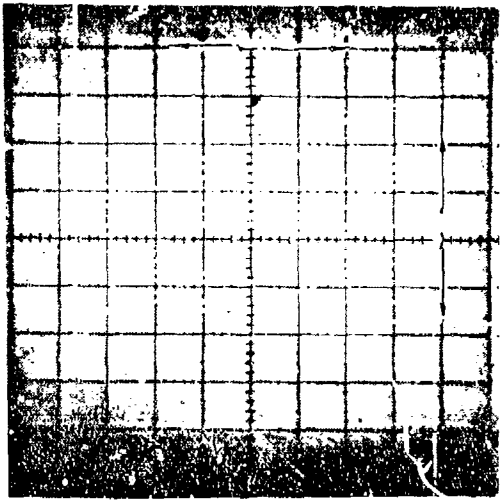
T_A = 125°C

	V_{CC} = ±20 Vdc	V_O = 5V/DIV.
T_A AS NOTED	V_{CM} = 0 Vdc	V_{IN} = 0.1mV (UNLESS NOTED)
R_L = 10KΩ	FREQ = 0.1 HZ	

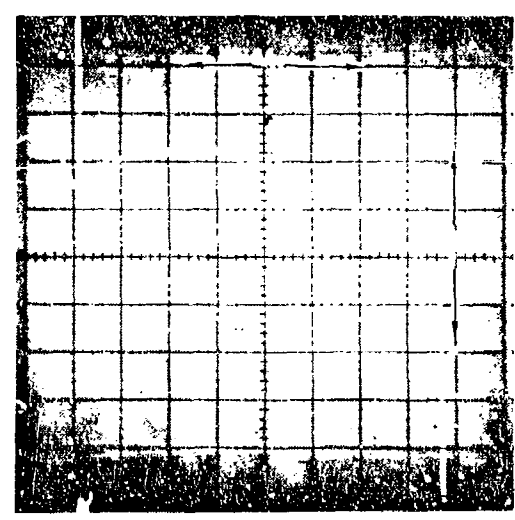
FIGURE E12. M38510/10107 (LM118) TYPICAL MANUFACTURER B TRANSFER CHARACTERISTICS VS. TEMPERATURE



R_L = 2KΩ



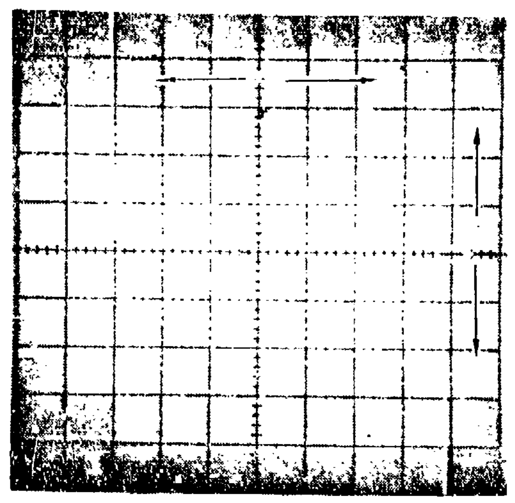
R_L = 10KΩ



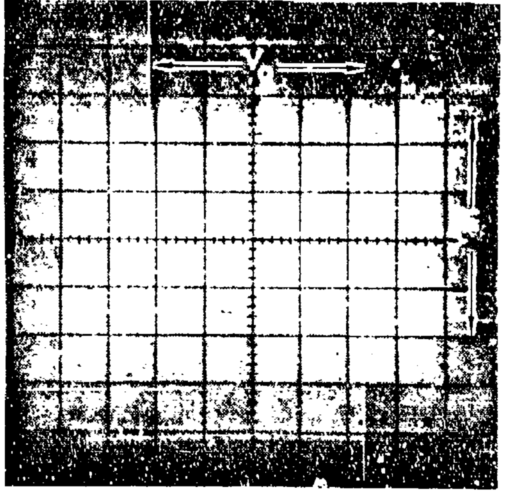
R_L = 50KΩ

MANUFACTURER B V_{CC} = ±20 Vdc V_O = 5V/DIV.
T_A = 25°C V_{CM} = 0 Vdc V_{IN} = 50μV/DIV.
R_L AS SHOWN FREQ = 0.1 HZ

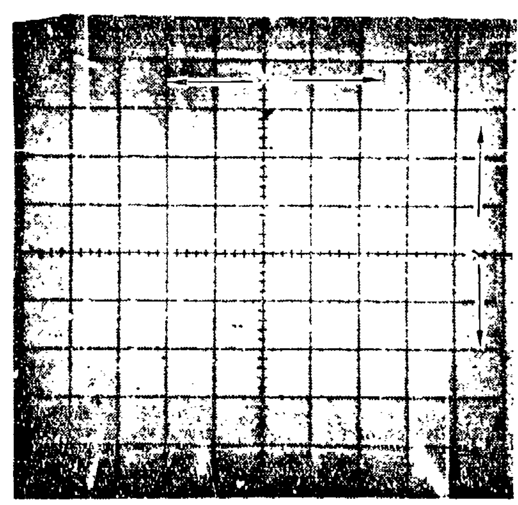
FIGURE E13. M38510/10107 (LM118) TYPICAL TRANSFER CHARACTERISTICS VS. LOAD



V_O = 1V/DIV. V_{CC} = ±5 Vdc
V_{IN} = 10μV/DIV.



V_{CC} = ±12.5 Vdc



V_{CC} = ±20 Vdc

MANUFACTURER B
T_A = 25°C
R_L = 10KΩ

V_{CC} AS NOTED
V_{CM} = 0.0 Vdc
FREQ = 0.1 HZ

V_O = 5V/DIV. (UNLESS NOTED)
V_{IN} = 50μV/DIV.

FIGURE L14. M38510/10107 (LM118) TYPICAL TRANSFER CHARACTERISTICS VS. SUPPLY VOLTAGE

E15. Like the previous operational amplifier, the /10107 devices exhibited excesive hysteresis on the curve tracer at frequencies above 1 Hz, as is shown in Figure E16. Thus, the response of the device to frequency was not determined.

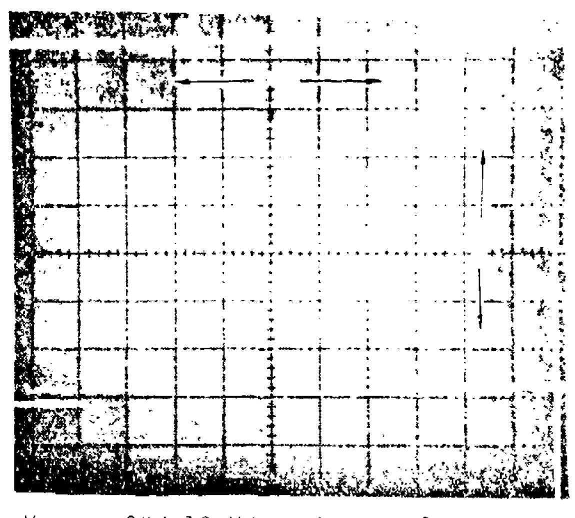
3.3 MIL-M-38510/10201 (723)

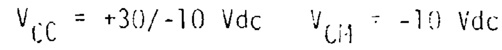
There were no major differences in the transfer plots of both manufacturer's MIL-M-38510/10201 devices. The output of both manufacturer's devices varied only 50 millivolts when the temperature was varied from 125°C to -55°C. However, Manufacturer D's device has small (200 - 300 mV peak-to-peak) oscillation at -55°C. The devices also exhibited very little sensitivity to load, as is shown in Figure E18.

The transfer plots showed considerable hysteresis at frequencies above 5 Hertz. This was found to be directly related, as shown in Figure E19, to the capacitor across the non-inverting input and V-. The transfer plots were run with this capacitor removed and the plots, as shown in Figure E20, showed little sensitivity to frequency other than a slight decrease (.2 - .3 Vdc) in the output voltage at the higher frequencies. In general the MIL-M-38510/10201 devices exhibited very little sensitivity to temperature, load, or frequency.

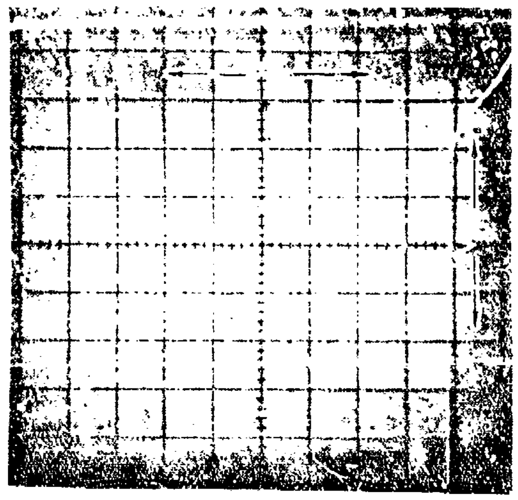
3.4 MIL-M-38510/10701 (LM109)

Manufacturer B's MIL-M-38510/10701 devices exhibited line regulation characteristics with 50 mA of load current similar to those with 5 mA. Also, both manufacturer's devices were relatively insensitive to changes in ambient temperature, as is shown in Figure E21. Subjecting the devices to a constant 500 milliampere load at 25°C without a heat sink induces a sufficient junction temperature rise to cause the devices to go into thermal shutdown.

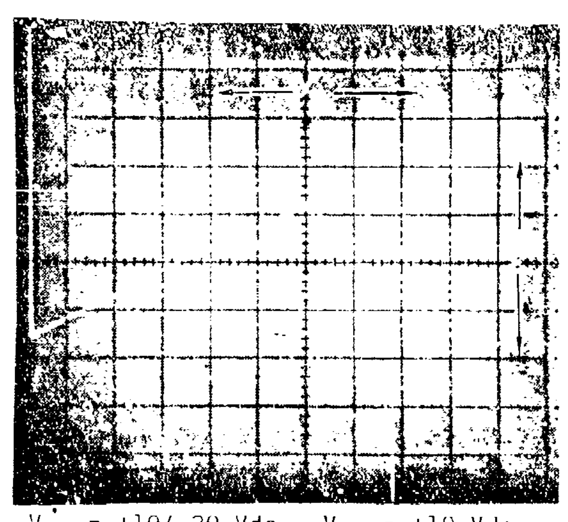




V_{CC} = +30/-10 Vdc V_{CM} = -10 Vdc



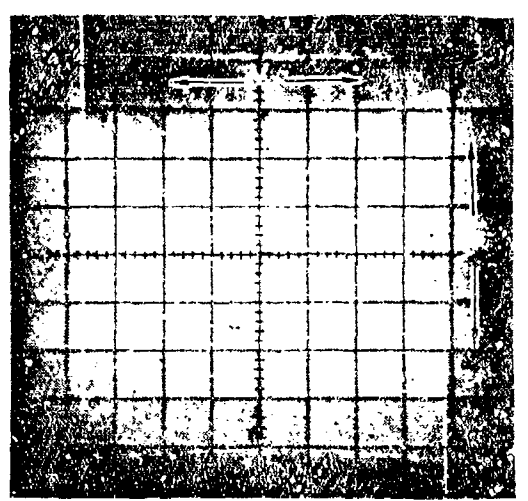
V_{CC} = ±20.0 Vdc V_{CM} = 0.0 Vdc
V_{IN} = 50 µV/DIV.



V_{CC} = +10/-30 Vdc V_{CM} = +10 Vdc

MANUFACTURER B	V_{CC} AS NOTED	V_O = 5V/DIV.
T_A = 25°C	V_{CM} AS NOTED	V_{IN} = 100µV/DIV. (UNLESS NOTED)
R_L = 10KΩ	FREQ = 0.1 HZ	

FIGURE E15. M38510/10107 (LM118) TYPICAL TRANSFER CHARACTERISTICS VS. COMMON MODE VOLTAGE



FREQ = 0.1 HZ

FREQ = 2 Hz

MANUFACTURER B

T_A = 25°C

R_L = 10KΩ

V_{CC} = ±20 Vdc

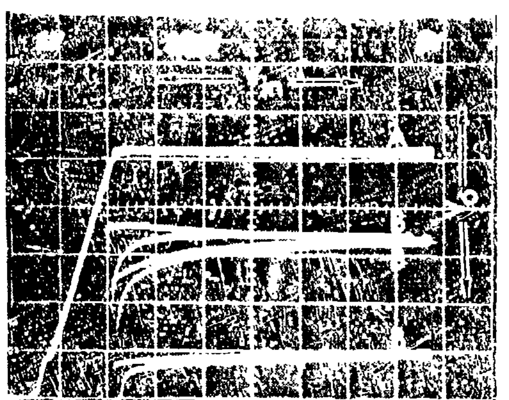
V_{CM} = 0.0 Vdc

FREQ = AS NOTED

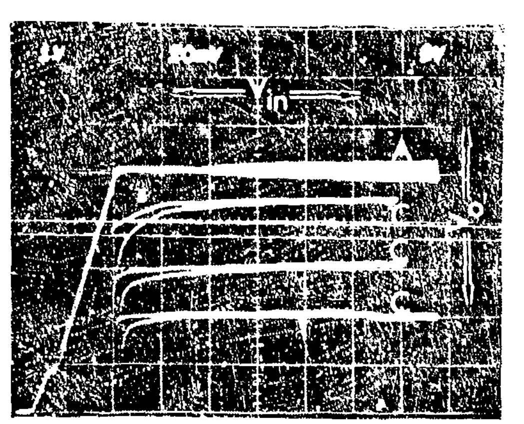
V_O = 5V/DIV.

V_{IN} = 50μV/DIV.

FIGURE E16. M38510/10107 (LM118) TYPICAL TRANSFER CHARACTERISTICS VS. FREQUENCY



MANUFACTURER C



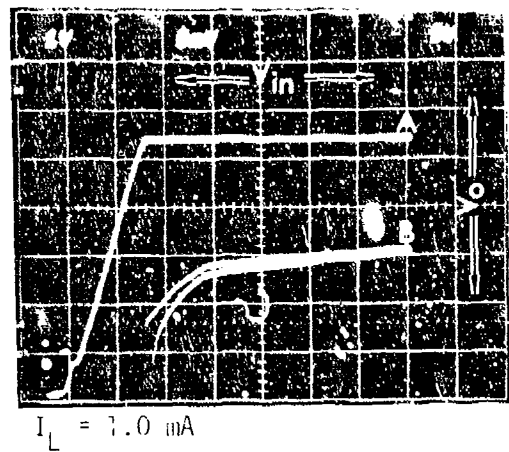
MANUFACTURER D

T_A = AS NOTED
I_L = 1 mA
FREQ = 0.1 HZ

V_{IN} = 5V/DIV.
V_0A = 1V/DIV.
V_0B = 10mV/DIV.

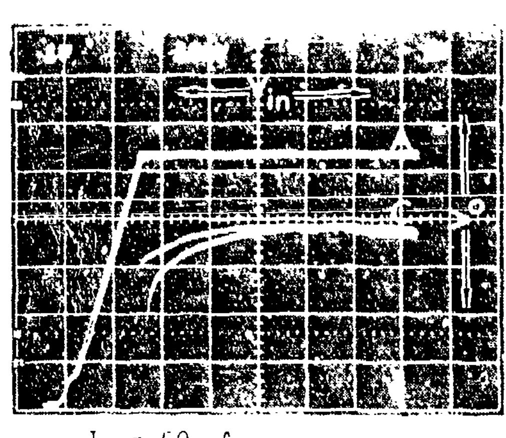
V_0C = 20mV/DIV.

FIGURE E17. M38510/10201 (723) TYPICAL TRANSFER CHARACTERISTICS VS. TEMPERATURE



I_L = 1.0 mA

I_L = 10 mA

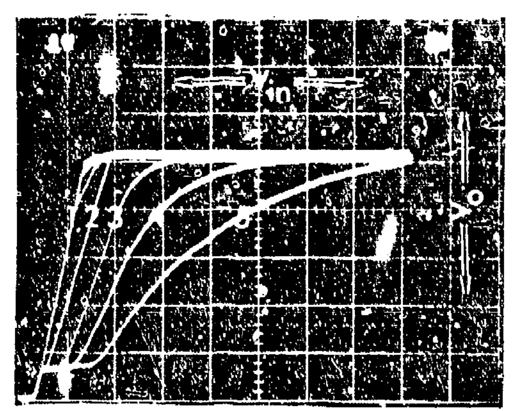


I_L = 50 mA

MANUFACTURER C | I_L AS NOTED | V_{IN} = 5V/DIV. | V_0B = 5mV/DIV.

T_A = 25°C | FREQ = 0.1 HZ | V_0A = 1V/DIV. | V_0C = 10mV/DIV.

FIGURE E18. M38510/10201 (723) TYPICAL TRANSFER CHARACTERISTICS VS. LOAD CURRENT



C_{REF}	0V-40V TRACE	40V-0V TRACE
0μF	2	2
1μF	3	1
2.5μF	4	1
5.0μF	5	1

MANUFACTURER C

T_A = 25°C

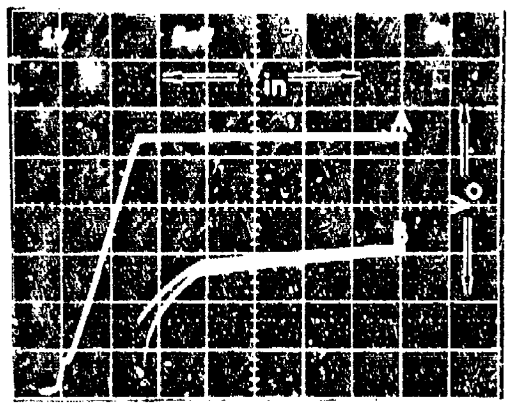
I_L = 1.0 mA

FREQ = 5 HZ

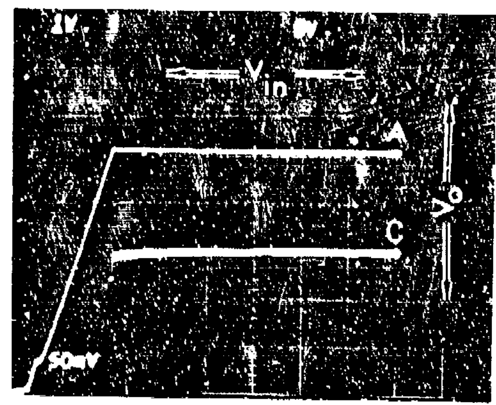
V_O = 1V/DIV.

V_{IN} = 5V/DIV.

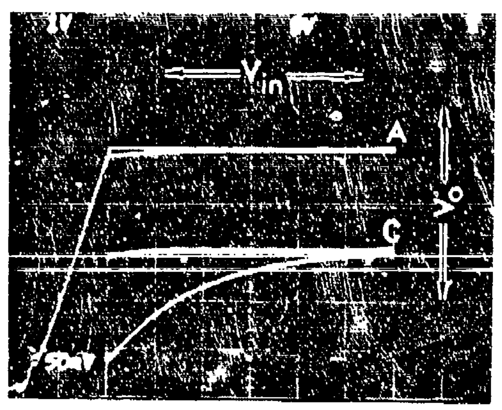
FIGURE E19. M38510/10201 (723) TRANSFER CHARACTERISTICS VS. C_{REF}



FREQ = 0.1 HZ



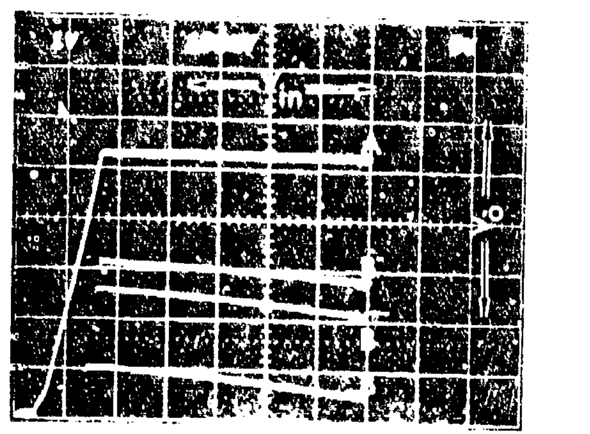
FREQ = 10 HZ



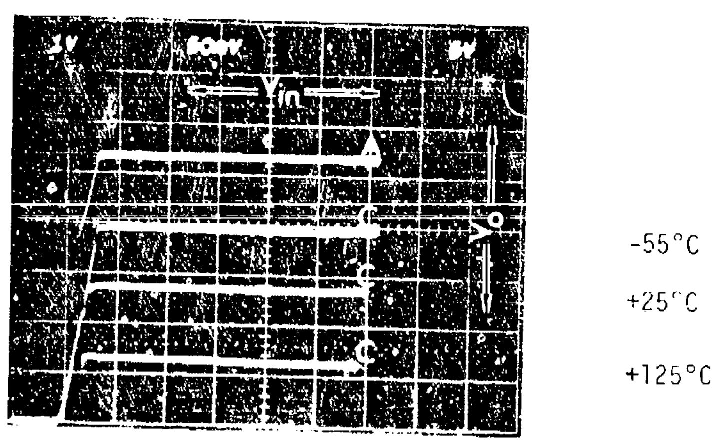
FREQ = 1K HZ

MANUFACTURER C	I_L = 1.0 mA	C_{REF} = 0μf	V_0A = 1V/DIV.
T_A = 25°C	FREQ = AS NOTED	V_{IN} = 5V/DIV.	V_0B = 5mV/DIV.
			V_0C = 50mV/DIV.

FIGURE E20. M38510/10201 (723) TYPICAL TRANSFER CHARACTERISTICS VS. FREQUENCY



MANUFACTURER B



MANUFACTURER D

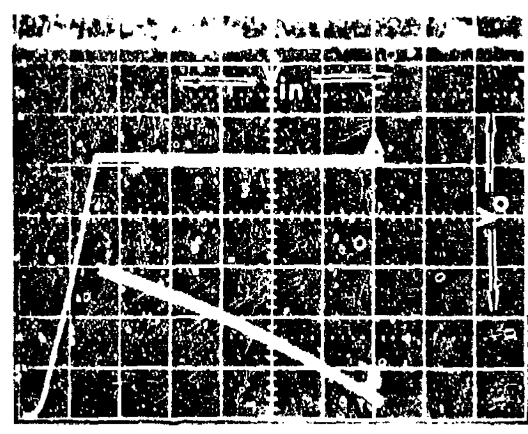
T_A AS NOTED
I_L = 5.0mA
FREQ = 0.1 HZ

V_{IN} = 5V/DIV.
V_0A = 1V/DIV.
V_0B = 100mV/DIV.

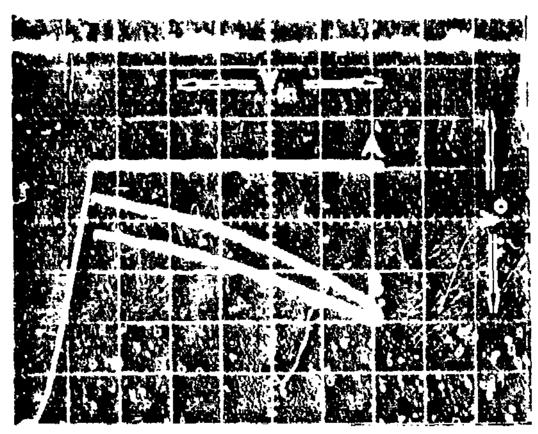
V_0C = 50mV/DIV.

FIGURE E21. M38510/10701 (LM109) TRANSFER CHARACTERISTICS VS. TEMPERATURE

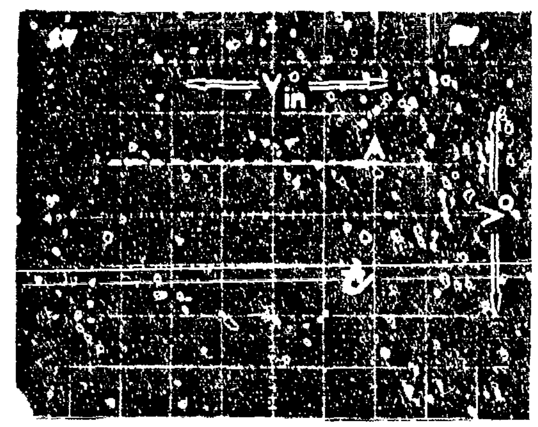
Thus, the devices were subjected to a 300 microsecond 500 milliampere pulsed load at 50% duty cycle. Figure E22 shows that there was minimal deviation in output when the devices were operated at junction temperatures below their rated shut-down temperature. Since the 500 milliampere load curve was made using the pulsed mode of the curve tracer, a magnified curve of the output voltage was not able to be made. The devices also exhibited little senitivity to frequency except that Manufacturer B's device exhibited an increase in line regulation at the 1.0 kHz frequency, as shown in Figure E23. In general, the MIL-M-38510/10701 devices were relatively insensitive to temperature, load, and frequency with the restriction that the load duty cycle does not cause the junction temperature to exceed the thermal shut-down temperature.



I_L = 5.0 mA



I_L = 50.0 mA

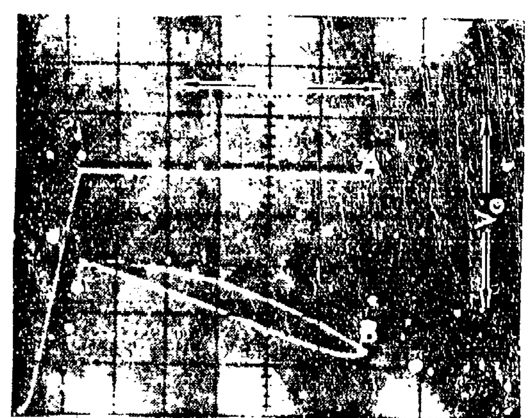


V_{IN} (SEE BELOW) I_L = 500.0 mA

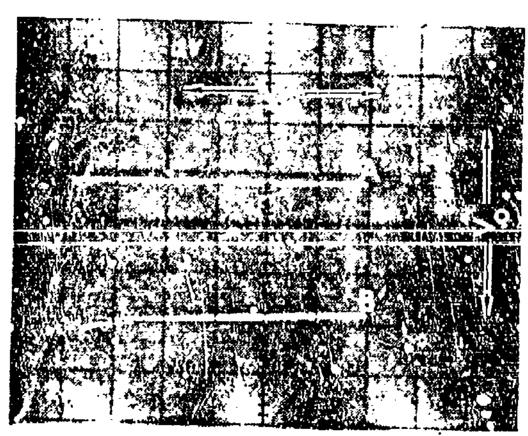
MANUFACTURER B	I_L AS NOTED	V_{IN} PULSE WIDTH = 300μSEC
T_A = 25°C	FREQ = 0.1 HZ	PULSE AMP = 0-35 Vdc
	V_OA = 1V/DIV.	V_OB = 20mV/DIV.

FIGURE E22. M38510/10701 (LM109) TYPICAL TRANSFER CHARACTERISTICS VS. LOAD CIRCUIT

FREQ = 0.1 HZ



FREQ = 10.0 HZ



FREQ = 1.0K HZ

MANUFACTURER B

T_A = 25°C

I_L = 5.0 mA

FREQ = AS NOTED

V_{IN} = 5V/DIV.

V_CA = 1V/DIV.

V_OB = 20mV/DIV.

FIGURE E23. M38510/10701 (LM109) TYPICAL TRANSFER CHARACTERISTICS VS. FREQUENCY

3.5 MIL-M-38510/10304 (LM111)

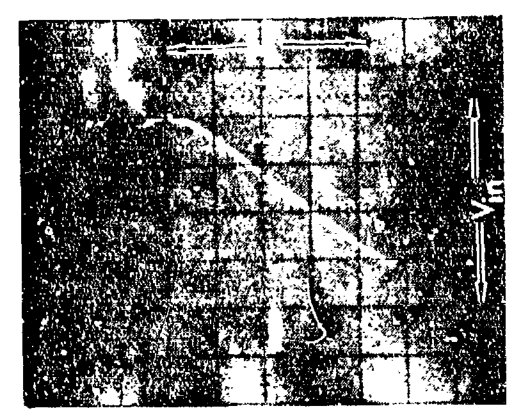
The MIL-M-38510/10304 transfer characteristics were performed for the collector (pin seven) output only and a comparison of Manufacturer B's and D's devices is shown in Figure E24. Varying the temperature degraded the linearity of Manufacturer B's devices as shown in Figure E25. At an ambient temperature of -55°C the slope of the transfer curve increased while at 125°C the slope of the curve is distorted. Temperature variations improved the linearity of Manufacturer D's device transfer curves as shown in Figure E26. The slope of the curves also increased as the temperature increased from -55°C to +125°C.

Similar results were noted in both manufacturer's devices when changes were made in the device load conditions as shown in Figures E27 and E28. A load resistance of 10K ohms in each case provided the best linearity and only slight differences were noted between the 1K ohm load and 2K ohms load curves.

Figure E29 shows the effects caused by varying the input frequency of Manufacturer D's devices. These results are inconclusive since the effects may have been related to the test fixture and not to the device under test. Manufacturer B's devices exhibited similar curves at frequencies of 1.0 Hz and 1.0 kHz.

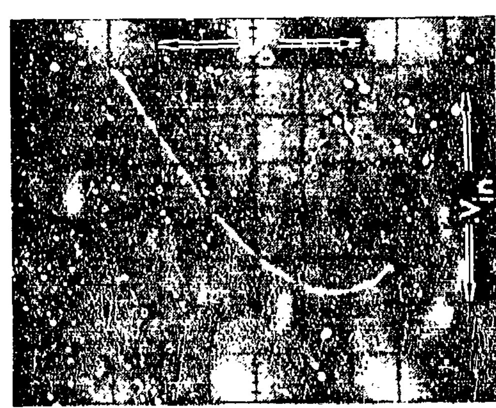
Variations in the supply voltage had no effect on the linearity or slope of either manufacturer's device transfer curves. Changing the common mode voltage of Manufacturer B's devices likewise had no effect on the transfer curves. However, the linearity improved on both common mode voltage transfer curves (±12 Vdc) for Manufacturer D's devices as shown in Figure E30.

The MIL-M-38510/10304 is most affected by changes in ambient temperature and load resistance. For Manufacturer D's devices, optimum performance is provided by reducing the ambient temperature or by increasing the load resistance. Manufacturer B's devices are adversely affected by either temperature extreme; however, at an ambient temperature of 25°C and load resistance of 10K ohms, Manufacturer B's devices provided an optimum transfer curve.



MANUFACTURER B

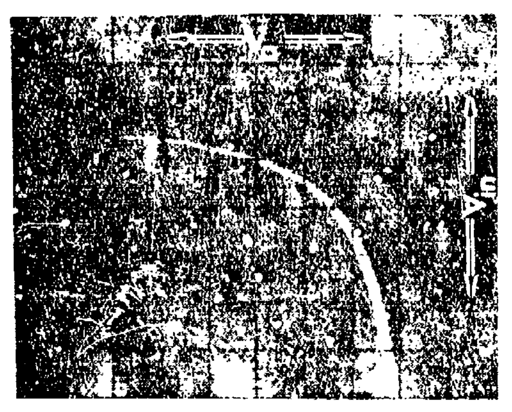
V_{in} = 20 μV/DIV. V_O = 5V/DIV.
T_A = 25°C R_L = 2 k.
V_{CC} = ±18 Vdc V_{CM} = 0 Vdc
FREQ = 0.1 HZ



MANUFACTURER D

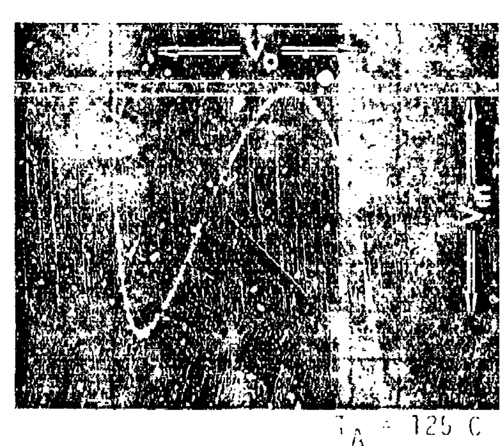
V_{in} = 50 μV/DIV

FIGURE E24. MIL-M-38510/10304 (LM111) TRANSFER CHARACTERISTIC COMPARISON



V_{IN} = 200 . V/DIV. T_A = -55 C

T_A = 25 C



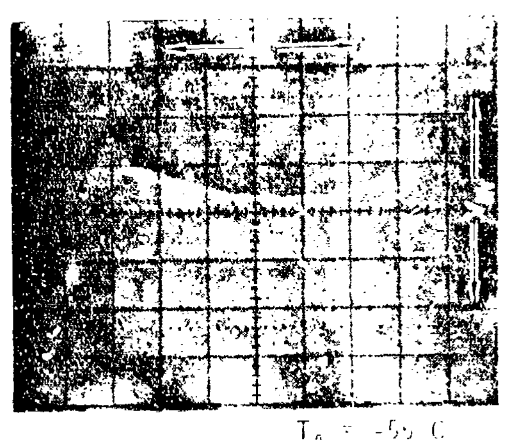
T_A = 125 C

MANUFACTURER B
T_A = AS NOTED
R_L = 2 K

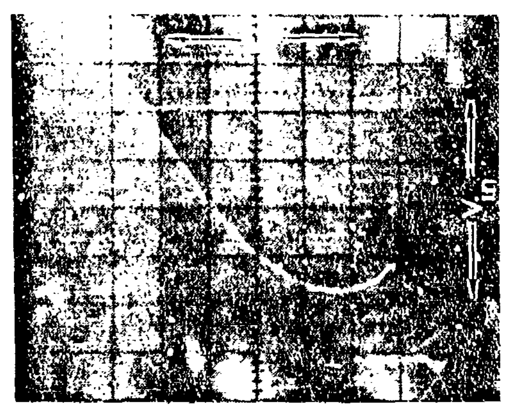
V_{CC} = ±18 Vdc
V_{CM} = 0 Vdc
FREQ 0.1 HZ

V_O = 5V/DIV.
V_{IN} = 20 mV/DIV.
(UNLESS NOTED)

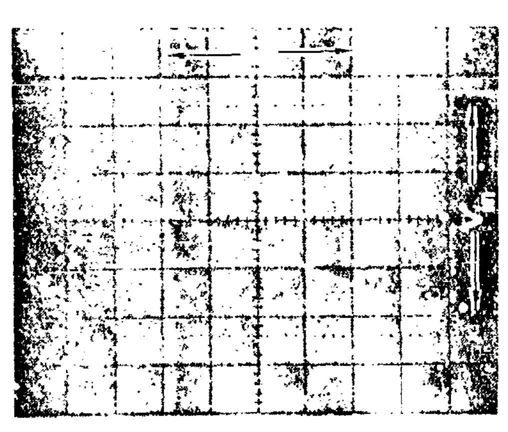
FIGURE L25. M38510/10304 (LM111) TYPICAL TRANSFER CHARACTERISTICS VS. TEMPERATURE



T_A = -55 C



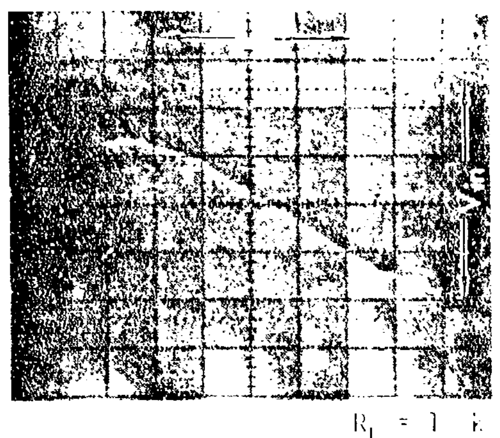
T_A = 25 C



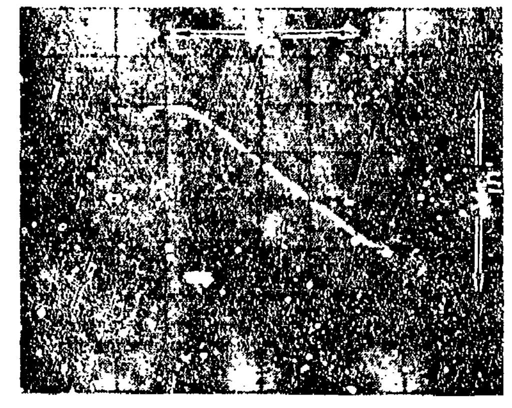
V_{IN} = [illegible] mV/DIV. T_A = 125 C

MANUFACTURER D	V_S = ±1[illegible] Vdc	V_O = 5V/DIV.
T_A AS NOTED	V_{CM} = 0 Vdc	V_{IN} = 50 [illegible]V/DIV. (UNLESS NOTED)
R_L = 2 K	FREQ = 0.1 Hz	

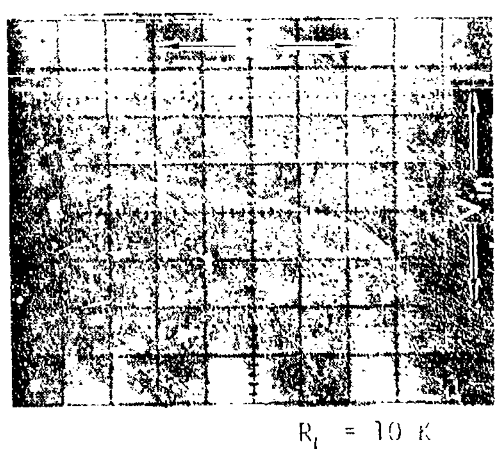
FIGURE [illegible]26. M38510/10304 ([illegible]) TYPICAL TRANSFER CHARACTERISTICS VS. TEMPERATURE



R_L = 1 K



R_L = 2 K



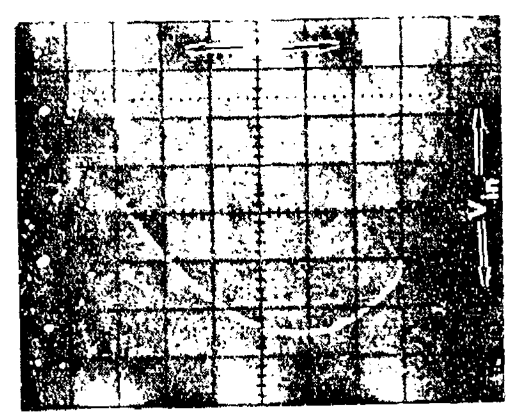
R_L = 10 K

MANUFACTURER B
T_A = 25°C
R_L AS NOTED

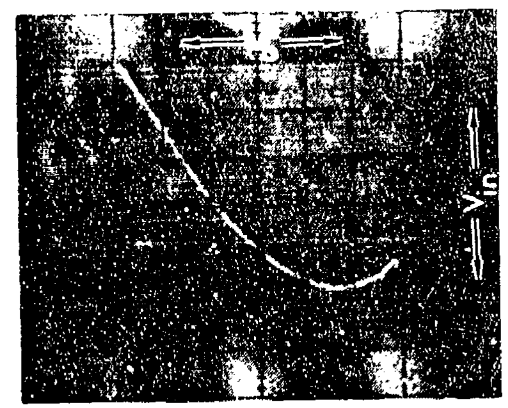
V_{CC} = ±18 Vdc
V_{CM} = 0 Vdc
FREQ = 0.1 HZ

V_O = 5V/DIV.
V_{IN} = 20 μV/DIV.

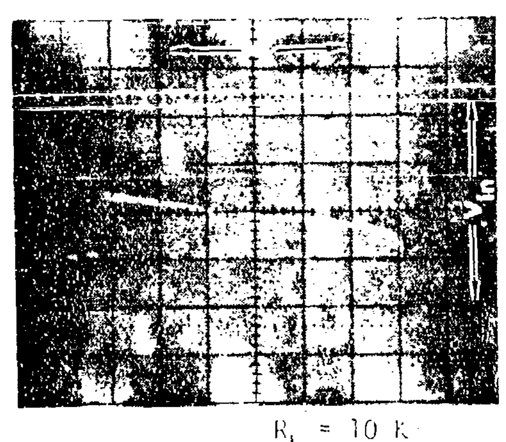
FIGURE E27. M38510/10304 (LM111) TYPICAL TRANSFER CHARACTERISTICS VS. LOAD



R_L = 1 KΩ



R_L = 2 KΩ



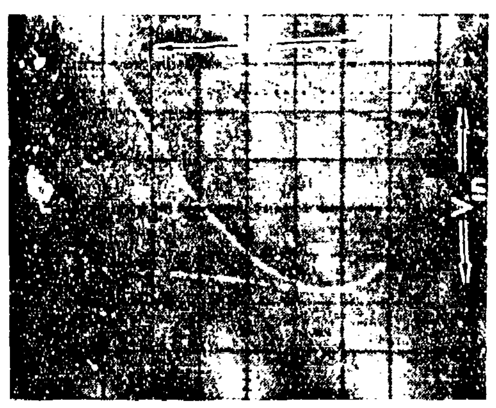
R_L = 10 KΩ

MANUFACTURER D
T_A = 25°C
R_L AS NOTED

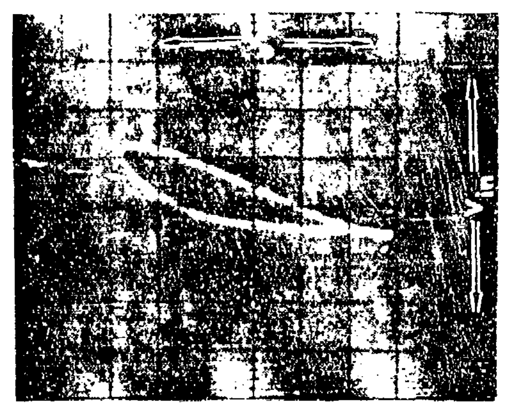
V_{CC} = ±18 Vdc
V_{CM} = 0 Vdc
FREQ = 0.1 HZ

V_O = 5V/DIV.
V_{IN} = 50 μV/DIV.

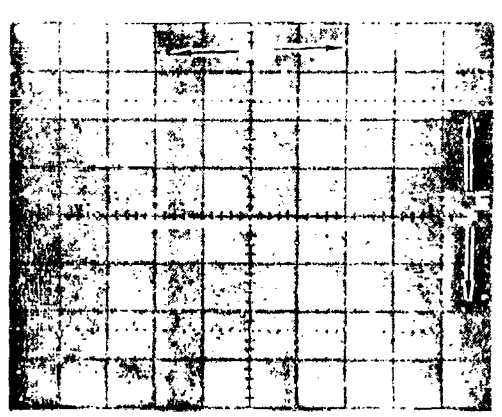
FIGURE L28. M38510/10304 (LM111) TYPICAL TRANSFER CHARACTERISTICS VS. LOAD



FREQ = 0.1 HZ



FREQ = 1.0 HZ



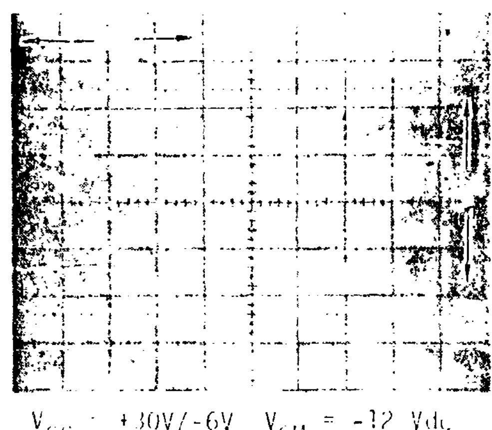
FREQ = 1.0 KHZ

MANUFACTURER D
T_A = 25 C
R_L = 2 K

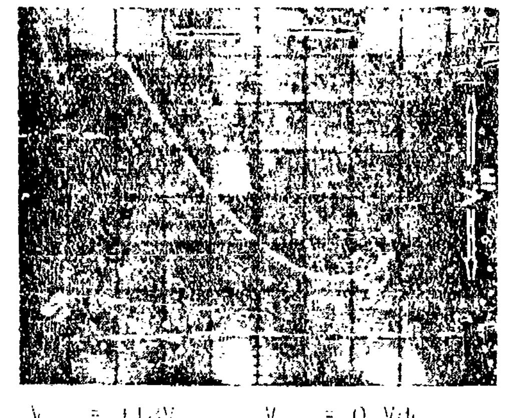
V_{CC} = ±18 Vdc
V_{CM} = 0 Vdc
FREQ AS NOTED

V_O = 5V/DIV.
V_{IN} = 50 μV/DIV.

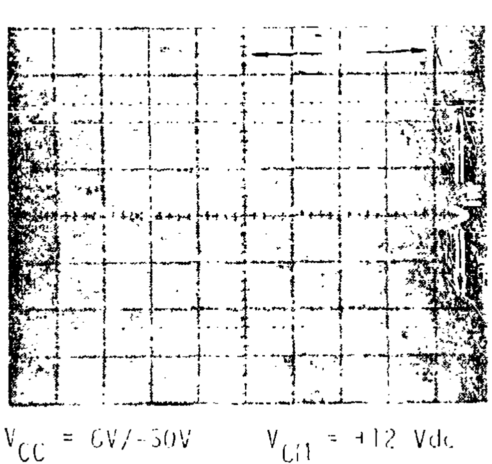
FIGURE [illegible] M38510/10504 (TMI[illegible]) TYPICAL TRANSFER CHARACTERISTICS VS. FREQUENCY



V_{CC} = +30V/-6V V_{CM} = -12 Vdc



V_{CC} = ±18V V_{CM} = 0 Vdc



V_{CC} = 6V/-30V V_{CM} = +12 Vdc

MANUFACTURER D
T_A = 25 C
R_L = 2 K

V_{CC} AS NOTED
V_{CM} AS NOTED
FREQ = 0.1 HZ

V_O = 5V/DIV.
V_{IN} = 50 . V/DIV.

FIGURE E 30. M38510/10304 (LM111) TYPICAL TRANSFER CHARACTERISTICS VS. COMMON MODE VOLTAGE

4.0 REFERENCES

[1] J. E. Solomon, "The Monolithic OP AMP: A Tutorial Study," IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, December 1974.

APPENDIX F

FAILURE ANALYSIS

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1.0 INTRODUCTION

This appendix presents a condensation of the failure analyses performed during the program.

To facilitate reader use of this appendix, an overview of all failure analysis results is presented in Section 3.0. Individual failure analysis reports are contained in Sections 4.0 through 8.0, and the paragraph numbers for specific reports are cross-referenced in the Section 3.0 overview.

2.0 PROCEDURE

All parts that failed an electrical test during Step Stress and Accelerated Life testing were analyzed to determine the particular failure mode, failure mechanism and probable cause of failure. The general analysis procedure was as follows:

1) All failures were retested on the automated microcircuit tester to verify the failure, and to obtain final dc electrical parameter measurements.
2) Failed parameters were confirmed using a curve tracer or, if necessary, a bench test set.
3) The failure was isolated to a specific junction or element to the extent possible via external pin-pin curve tracer measurements.
4) Failures were classified into subgroups (failure categories) on the basis of the analysis findings.
5) A representative sample of devices from each subgroup was subjected to a detailed analysis.
6) The remaining samples from each subgroup were subjected to the following steps to confirm their categorization and to obtain any additional information:

    a) Unpowered Bake - Each device was subjected to an unpowered bake and retested at 25°C to obtain post bake electrical data. The exact time and temperature of the bake depended on the time and temperature at which the failure occurred. Usually, an overnight bake (16 hours) at the test temperature sufficed.
    b) Leak Tests - Each device was subjected to a helium bomb fine leak test and a fluorocarbon gross leak test.
    c) Delidding - Each device was delidded and subjected to routine optical examinations and documentations.

3.0 FAILURE ANALYSIS OVERVIEW

Summaries of the failure analysis results for each device type are contained in Tables F1 through F5. Each table contains a brief description of each of the different failure symptoms, failure modes, failure mechanisms, causes of device failure, and a paragraph number reference to the related failure analysis report. Certain random failures were not analyzed in detail and are not discussed in the reports, thus no reference paragraph number is listed for them.

TABLE F3-1. MIL-M-38510/10107 (LM118) FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS) BY TEST CELL								F/A REPORT PARAS. NUMBER
	MANUFACTURER B				MANUFACTURER C				
	STEP STRESS	ACCELERATED LIFE			STEP STRESS	ACCELERATED LIFE			
		125°C	150°C	175°C		125°C	150°C	175°C	
A. V_{IO} AND/OR PSRR B. CHANNEL CURRENT FROM R15 TO THE SUBSTRATE C. INVERSION OF THE RESISTOR TUB DUE TO CHARGE MIGRATION D. MOBILE IONS OR CHARGES IN THE PASSIVATION	3@125°C 2@150°C	5@4 9@8 3@16 2@32 1@64 2@128	1@1 5@2 3@4 1@8 1@64 1*@1000	2@1 1@2 1@4 1@16 1@1000					4.1
A. I_{IO} @ V_{CM} = -15V B. V+ TO INPUT CHANNEL CURRENT C. PROBABLY INVERSION OF THE C-B JUNCTION OF THE INPUT TRANSISTOR D. MOBILE IONS IN THE PASSIVATION			3@1000 1*@1000			1@4000		1@4	4.2
A. I_{IO} OR I_{IB} B. LOW GAIN IN INPUT TRANSISTOR C. PROBABLY DEFLETION OF THE BASE D. MOBILE IONS OR CHARGES IN THE PASSIVATION				1@128 1@1000		1@1 2@4000		1@2000	4.3
A. V_{IO} LATCHED UP B. MELTED STRIPES AND SHORTED JUNCTIONS C. PROBABLY THERMAL RUNAWAY OF C1 D. UNKNOWN					1@200°C 1@250°C 2@275°C			1@1 2@4000	4.4
A. V_{IO} LATCHED UP B. SHORTED CAPACITOR C. DIELECTRIC BREAKDOWN D. DEFECT IN DIELECTRIC SiO_2						1@128	1@4 1@2?00	2@4000	4.5
A. V_{IO} LATCHED UP B. OPEN STRIPE OR SHORTED JUNCTION C. ELECTRICAL OVERSTRESS D. TEST ERROR		1@4				1@1000	1*@?000		4.6
RANDOM FAILURES-NOT ANALYZED IN DETAIL									
A. V_{IO} AND PSRR (RECOVERED UPON DELIDDING)								1@64	
A. P_D B. NONE C. NONE D. TEST ERROR (INITIALLY FAILED)		4*@1000	2@1 1*@1000						
TOTAL NUMBER OF FAILED PARTS	5	27	33	28	4	6	3	8	

* @ + 125°C ONLY.

TABLE F3-2. MIL-M-38510/10104 (LM108A) FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS) BY TEST CELL								F/A REPORT PARAG. NUMBER
	MANUFACTURER B				MANUFACTURER A				
	STEP STRESS	ACCELERATED LIFE			STEP STRESS	ACCELERATED LIFE			
		175°C	200°C	225°C		175°C	200°C	225°C	
A. V_{IO} AND/OR A_{VS} B. CHANNEL CURRENT FROM R7 TO THE SUBSTRATE C. INVERSION OF THE R7 RESISTOR TUB D. MOBILE IONS OR CHARGES IN THE PASSIVATION	1@125°C 1@150°C 1@175°C 1@225°C	10@1 1@2 4@4 2@8 1@16 3@500 4@1000 1*@1000	14@4 3@8 2@64 2@128 3@1000 3*@1000	18@4 1@8 1@16 1@64 3@128 1@250 2@500 2@1000					5.1
A. V_{IO} LATCHED UP B. MELTED STRIPES AND SHORTED JUNCTIONS C. THERMAL RUNAWAY AT Q6 D. UNKNOWN						1@5000 2@2000 4@4000	1@256 4@500 4@1000 1@2000 3@4000	1@8 3@64 3@128 1@256 1@500 3@1000 2@2000 3@4000	5.2
A. A_{VS} B. NOT DETERMINED (RECOVERED) C. SURFACE INSTABILITY D. PROBABLY IONIC CONTAMINATION						1@1 1@8 2@1000 1@2000	1@500	2@1000 1@2000 ●1@4000	5.3
A. I_{IO} AND/OR I_{IB} B. PROBABLY DEGRADED INPUT TRANSISTORS C. PROBABLY CHARGE ACCUMULATION D. TEST ANOMALY (STATIC DISCHARGE)		1@1 1@128	1@8 1@500			1@2 1@32 1@64	1@4 1@16 1@64	1@16 2@128	5.4
+125°C FAILURES AND RANDOM FAILURES - NOT ANALYZED IN DETAIL									
A. V_{IO} @ +125°C ONLY						1@1000		1@4000	
A. I_{IO} @ + 125°C ONLY								1@4000	
A. I_{OS} (-) (RECOVERED WHEN LEFT ON TEST)						1@6			
TOTAL NUMBER OF FAILED PARTS	4	28	29	29	0	17	17	26	

NOTES: * @ +125°C ONLY. ● @ -55°C ONLY.

TABLE F3-3. MIL-M-38510/10701 (LM109) FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS) BY TEST CELL						F/A REPORT PARAG.
	ACCELERATED LIFE						
	MANUFACTURER D			MANUFACTURER B			
	200°C	225°C	250°C	200°C	225°C	250°C	
A. OPEN PIN B. LIFTED WIRE BOND AT THE POST C. KIRKENDALL VOIDING IN $AuAl_2$ D. EXCESSIVE $AuAl_2$ GROWTH DURING BONDING				1@500	1@64 1@4000	1@250	6.1
A. OPEN PIN 1 OR 3 B. BROKEN EXTERNAL LEAD C. MECHANICAL OVERSTRESS D. MISHANDLING		1@2000			1@8		6.2
A. OPEN PIN 3 B. BROKEN EXTERNAL LEAD C. Au LEACHING D. TIN SOLDER				1@4000		1@128	
A. ΔI_{SCD} [13] B. NONE C. NONE D. INITIALLY FAILED OR MARGINAL	2@4 1@64	1@16	2@4 1@16 1@2000			1@4000	6.3
RANDOM FAILURES - NOT ANALYZED IN DETAIL							
A. V_{OUT} [4] (ONLY MARGINALLY FAILED)				1@500			
TOTAL NUMBER OF FAILED PARTS	3	2	4	3	3	3	

TABLE F3-4. MIL-M-38510/10201 (723) FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS) BY TEST CELL						F/A REPORT PARAG.
	ACCELERATED LIFE						
	MANUFACTURER D			MANUFACTURER C			
	150°C	175°C	200°C	150°C	175°C	200°C	
A. I_{SCD} B. NONE C. NONE D. TEST SET DRIFT						6@2000	7.1
A. V_{REF} OR $V_{R\ LINE}$ [1] + $V_{R\ LOAD}$ [4] @ -55°C B. NONE C. NONE D. PROBABLY AN INTERMITTENT TEST SOCKET						2@4000	7.2
A. I_{OS} B. NOT DETERMINED C. SURFACE INSTABILITY + INITIALLY MARGINAL D. MOBILE CONTAMINANT IONS		1@4 1@64					7.3
RANDOM FAILURES - NOT ANALYZED IN DETAIL							
A. $V_{R\ LINE}$ [1] (ONLY MARGINALLY FAILED)		1@4000					
TOTAL NUMBER OF FAILED PARTS	0	3	0	0	0	8	

TABLE F3-5. MIL-M-38510/10304 (LM111) FAILURE ANALYSIS SUMMARY

A. FAILED PARAMETERS OR SYMPTOMS B. FAILURE MODE C. FAILURE MECHANISM D. CAUSE OF FAILURE	QUANTITY OF FAILURES AND TIME OF FAILURE (HOURS) BY TEST CELL								F/A REPORT PARAG. NUMBER
	MANUFACTURER B				MANUFACTURER D				
	STEP STRESS	ACCELERATED LIFE			STEP STRESS	ACCELERATED LIFE			
		200°C	225°C	250°C		200°C	225°C	250°C	
A. V_{IO} B. LOW h_{FE} IN Q4 C. INVERSION OF THE BASE OF Q4 D. PROBABLY IONIC CONTAMINATION		3@1000	1@4 1@64 1@1000		1@225°C 1@275°C	1@8 1@32 5@64 9@256 1@500 15@1000	3@8 1@16 5@32 4@256 3@500 10@1000	1@8 3@32 7@256 1@500 20@1000	8.1
A. I_{IO} B. LOW h_{FE} IN Q2 C. SURFACE INSTABILITY AND BULK-RELATED MECHANISMS D. PROBABLY IONIC CONTAMINATION	1@175°C 2@275°C	1@128 1@256 12@500 6@1000	1@4 1@32 4@64 2@128 6@256 5@500 2@1000	3@4 1@16 5@32 1@64 2@128 2@256 3@500 3@1000	1@200°C	1@64	1@4	1@8 1@500	8.2
A. I_{IB} B. NONE C. NONE D. V_{CM} TOO HIGH	2@175°C								8.3
A. I_O B. DEGRADED Q15 COLLECTOR - SUBSTRATE DIODE C. PROBABLY INVERSION OF THE COLLECTOR D. PROBABLY CATION CONTAMINATION		1@128		1@4 1@8					8.4
+125°C ONLY FAILURES AND RANDOM FAILURES - NOT ANALYZED IN DETAIL									
A. CMR (RETEST OK)						1@64	2@8		
A. A_{VC} (RECOVERED)		1@128	1@500						
A. A_{VC} @ +125°C ONLY		4@1000		1@1000					
A. V_{OL} [30]				1@1000					
TOTAL NUMBER OF FAILED PARTS	5	29	25	24	3	35	29	34	

4.0 LM118 FAILURE ANALYSIS REPORT

4.1 RESISTOR TUB INVERSION (MANUFACTURER B ONLY)

Seventy-nine Manufacturer B parts failed V_{IO} and/or PSRR during step stress and accelerated life. Ten parts failed V_{IO} only, 27 parts failed PSRR only, and 42 parts failed both V_{IO} and PSRR. The failures were bake recoverable, indicative of a surface instability mechanism.

The 52 parts which had failed V_{IO} exhibited excessive V_{IO} at a supply voltage of $\pm$20V (V_{CM} = +15, -15V, 0V) ranging from -4mV (the specified minimum limit) to -18 mV (latch limit of the test circuit). The failed values were always negative.

V_{IO} was almost always within specification at a supply voltage of $\pm$5 volts indicating that V_{IO} was supply voltage sensitive. Measurement of V_{IO} (V_{CM} = 0V) vs. supply voltage of representative failures disclosed that V_{IO} exceeded the limit of -4mV at supply voltages ranging from $\pm$6V to $\pm$20V. Below the critical supply voltage, V_{IO} was fairly constant and above the critical voltage, V_{IO} increased (in the negative direction) rapidly. Since this suggested a possible internal low breakdown/excessive leakage current, the I-V characteristic from V+ (pin 7) to V- (pin 4) of each part was examined on the curve tracer. Each failed part exhibited anomalous leakage from V+ to V- beginning at a voltage proportional to the supply voltage at which V_{IO} became excessive. For example, Figure F4-1 shows the I-V characteristic of a normal part, control sample S/N 24, with a V_{IO} ($\pm$20V, V_{CM} = 0V) of -0.9mV. The characteristic is essentially I_{DSS} of J-FET Q38 amplified by Q7-Q9 until breakdown occurs at 45 volts. S/N's 74, 102 and 61 each had failed V_{IO} after one hour of 175°C life and were found to have critical supply voltages of 6V, 15V and 20V, respectively. The three parts exhibited excessive leakage above V+ to V- equal to 5V, 13V and 33V, respectively, as shown in Figure F4-2. The fourth trace in Figure F4-2 is that of S/N 92 which had normal V_{IO} (+.36mV) after four hours at 175°C. V_{IO} of S/N 92 would

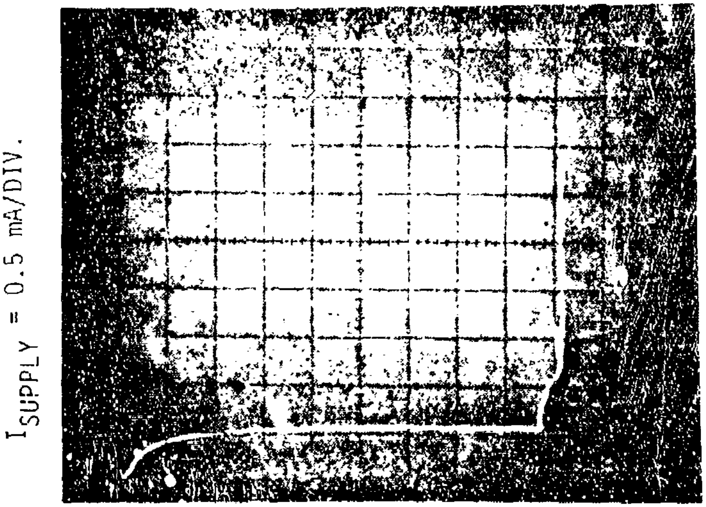


FIGURE F4-1. I-V CHARACTERISTIC FROM V+ TO V- OF A NORMAL PART (CONTROL SAMPLE S/N 24)

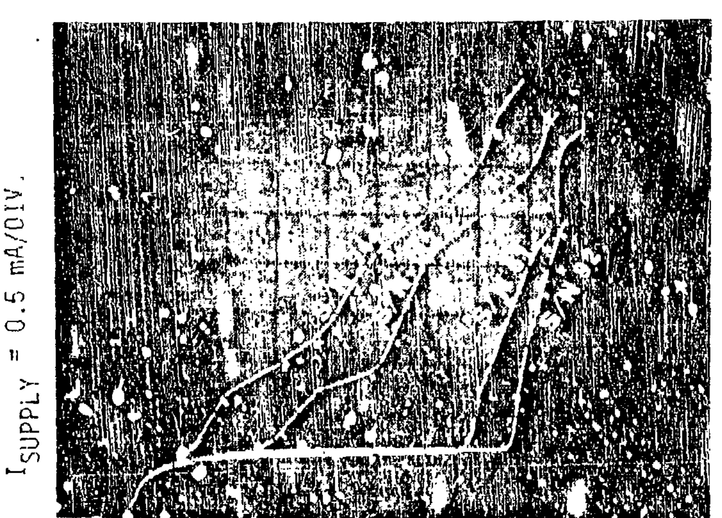
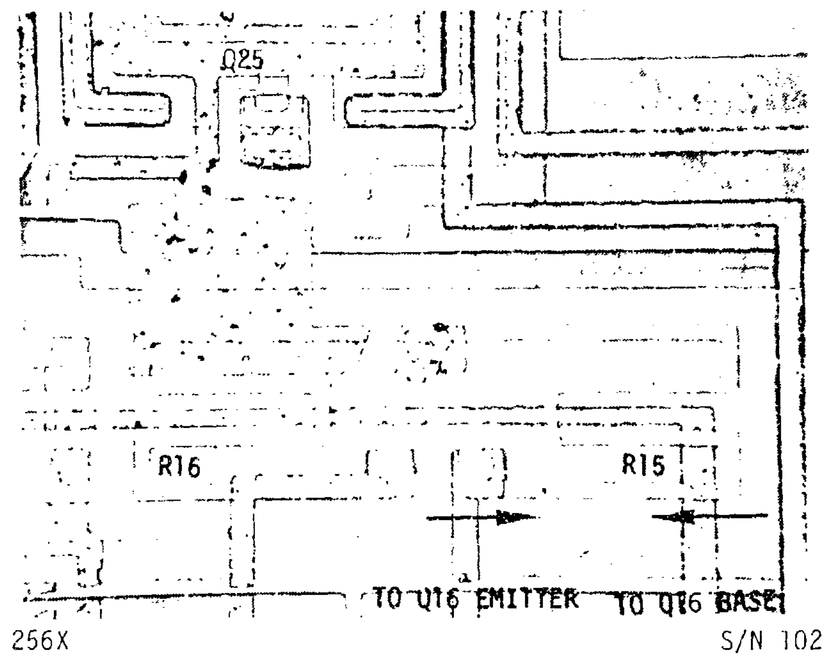


FIGURE F4-2. I-V CHARACTERISTIC FROM V+ TO V- OF THREE V_{IO} FAILURES (S/Ns 74, 102 AND 61) AND A PART WITH NORMAL V_{IO} AFTER STRESS (S/N 92)

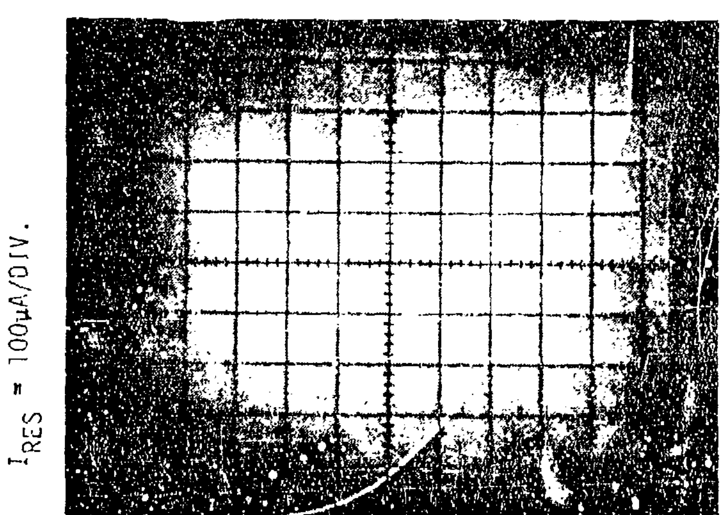
not exceed -4mV until the supply voltage was increased to ± 23 volts and its leakage from V+ to V- became excessive at 37 volts.

The anomalous leakage was traced to channel leakage from resistors R15 and R16 to the substrate (V-). Figure F4-3 shows R15 and R16 of S/N 102 after severing the stripes for isolation. Figure F4-4 shows the leakage from the common contact to R15 and R16 (+) to the substrate (-). This leakage, amplified by Q25, was primarily reponsible for the anomalous current observed between V+ and V-. The pn junction between the resistor diffusion and the n-epi resistor isolation tub and the junction between the tub and the substrate exhibited no leakage and nominal reverse breakdown voltages of 90V and 98V, respectively. This indicated that the leakage from R15/16 to V- was caused by a channel in the tub which extended from the resistors to the substrate due to inversion of the n-type tub. Inversion of n-type material is caused by the accumulation of a net negative charge in or on the passivation layers. To further pin-point the location of the channel, a high potential field effect probe technique [1] was used. A manipulator probe, biased either positively or negatively with respect to the n-tub, was scanned over the region of the tub between the resistor and the substrate isolation diffusion of representative failures (before and after removing the glassivation) while monitoring V_{IO} of the part. It was found that positive potentials of up to 150 volts over any point on the tub did not reverse the inversion and improve V_{IO}. This indicated that the width of the anomalous channel was probably much greater than the diameter of the probe and simply could not be totally pinched off with the probe. Negative potential, as low as -75V, would affect V_{IO}. The area of greatest sensitivity was found to be along the outside of resistor R15, between the stripe to the emitter of Q16 and the stripe to the base of Q15 (see Figure F4-3). V_{IO} would latch negative at a probe potential of -125 volts above the tub along this area. This is because the negative field enhanced the inversion thereby increasing the conductance of the channel. Negative potential applied above the tub anywhere along the outside of R15 would worsen V_{IO} to some degree which indicated that the channel was distributed along the entire length of R15. A channel also existed along the



256X S/N 102

FIGURE F4-3. R15 AND R16 AFTER REMOVAL OF THE GLASSIVATION AND STRIPE SEVERING



I_{RES} = 100μA/DIV.

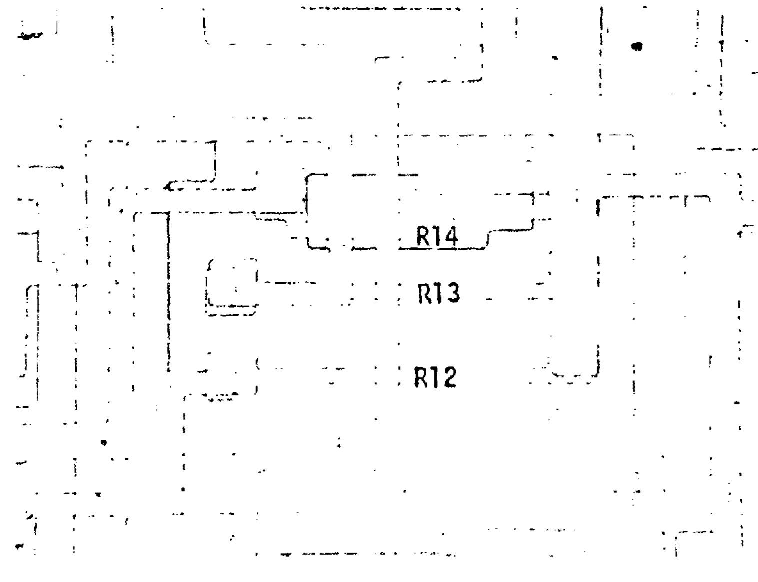
$V_{RES-SUBST.}$ = 10 VOLTS/DIV.

FIGURE F4-4. I-V CHARACTERISTIC FROM R15-R16 TO THE SUBSTRATE OF S/N 102

outside of R16, but increasing the inversion with negative probe potential caused V_{IO} to increase a few millivolts in the positive direction. This indicated that leakage to the substrate from R15 increased V_{IO} in the negative direction and leakage from R16 increased V_{IO} in the positive direction. It is suspected that V_{IO} was always negative at the time of failure because R15 has a greater amount of its perimeter adjacent to the p-isolation than does R16. Using the voltage probe it was discovered in the same manner that the n-epi tub containing R12, R13 and R14, shown in Figure F4-5, had also inverted or at least depleted. The exact amount of leakage from these resistors to the substrate could not be determined because other inherent circuit elements existed between the resistors and the substrate that could not be disconnected.

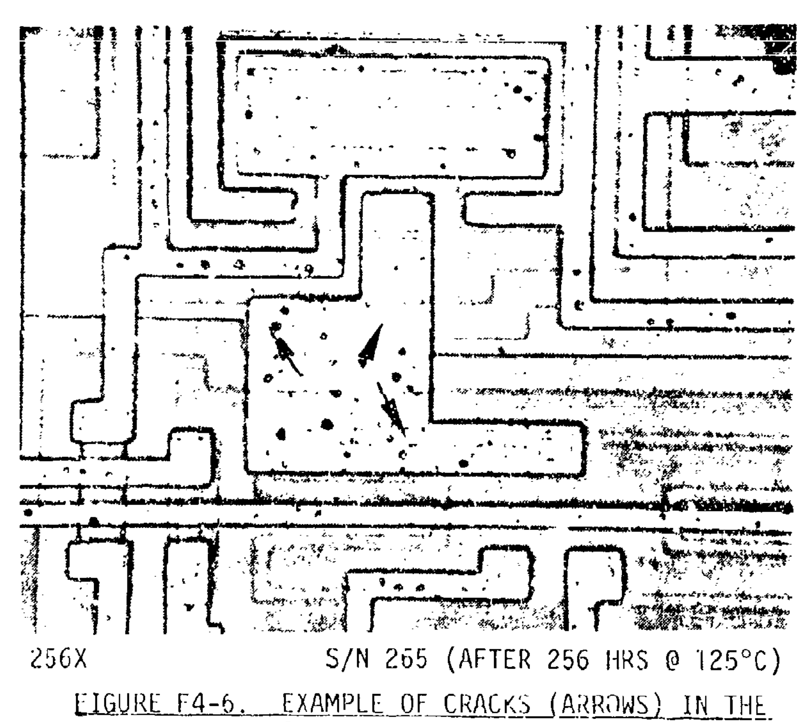
The parts that had failed PSRR only were found to exhibit channel leakage from V+ to V- as did the V_{IO} failures, but the leakage was not as severe in the PSRR only failures and usually saturated. Again, this leakage was traced to inversion of the R15-R16 resistor isolation tub. Thus, it is probable that the PSRR failure differed from the V_{IO} failures only in degree. This was further substantiated by the fact that any part failing PSRR only, that was left on test, eventually failed V_{IO} also.

The resistor tub to substrate junction was reverse biased at 40 Vdc during the tests. Thus, the accumulation of negative charge over the tub was probably the result of separation of mobile ionic species in the fringing field of the reverse biased junction or electron drift in the fringing field along defects in the glass/insulator interface [2]. Microscopic examinations of failed parts disclosed two types of anomalies in the glassivation layer which probably contributed to the failure. One hundred percent of the parts examined (27 out of 27) contained one to three cracks in the glassivation over the wide metalization stripe between Q25 and R15/16, as illustrated in Figure F4-6 and F4-7. Sixty-six percent of the parts (18 out of 27) contained one or more cracks elsewhere on the die, principally over the wide emitter contacts of the PNP transistors and the capacitor electrodes. One hundred percent of



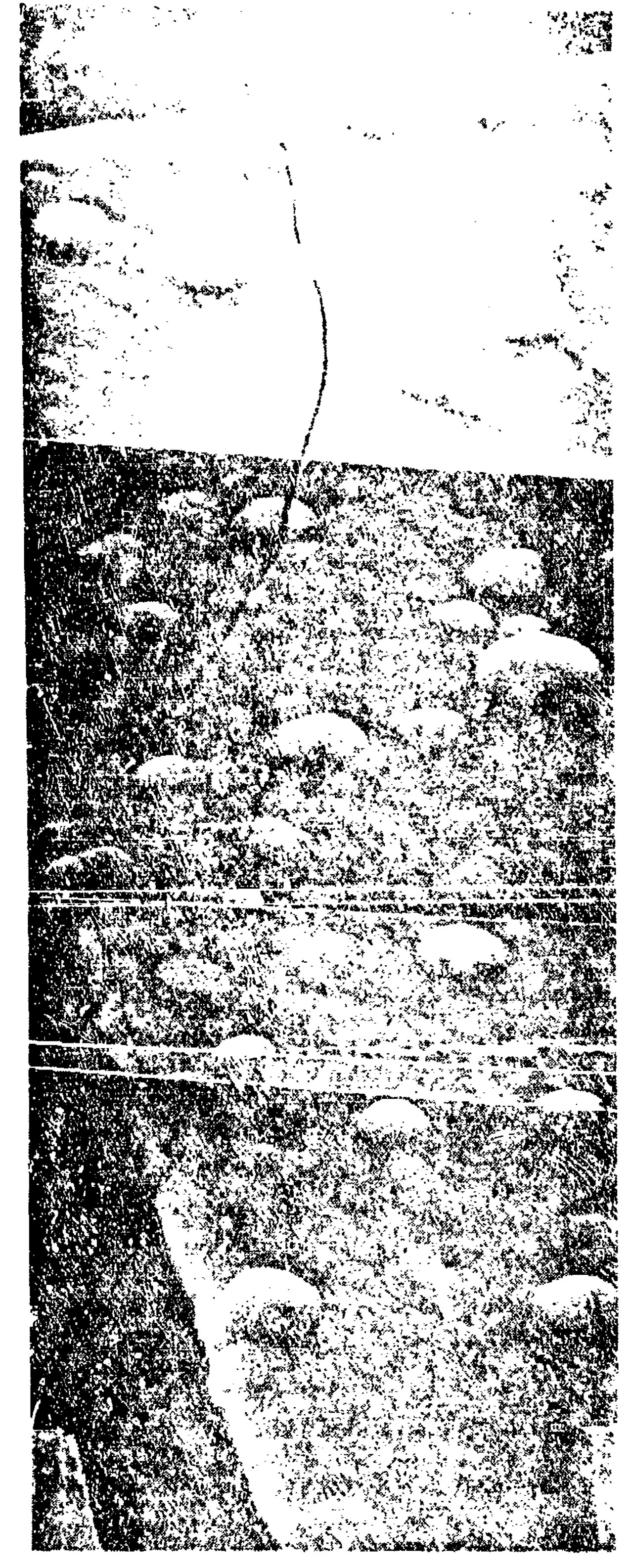
256X

FIGURE F4-5. R12, R13 AND R14 OF THE LM118



256X S/N 265 (AFTER 256 HRS @ 125°C)

FIGURE F4-6. EXAMPLE OF CRACKS (ARROWS) IN THE GLASSIVATION OVER THE R15/R16 STRIPE



4500X S/N 293 (STEP STRESS @ 64 HRS/150°C)

FIGURE 14-7. SEM PHOTO OF A CRACK IN THE GLASSIVATION OVER THE R15/R16 STRIPE

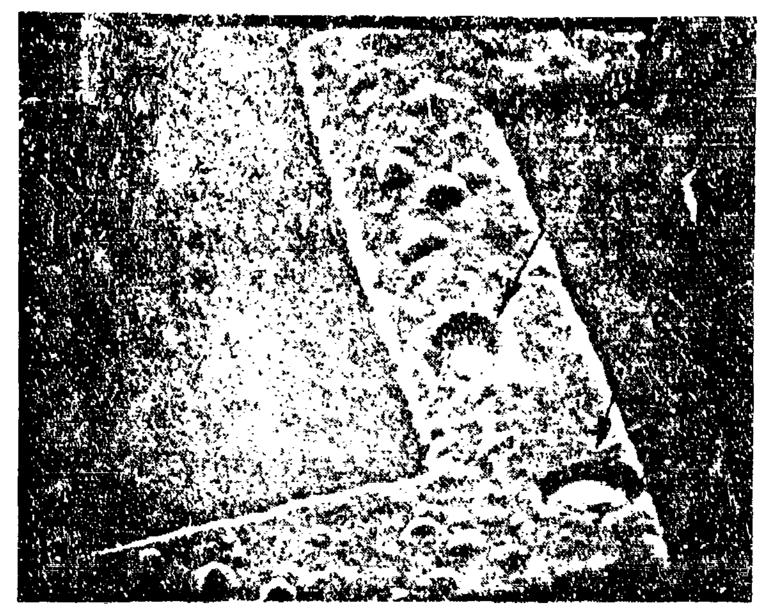
the parts also contained pinholes in the glassivation over hillocks in the metalization. As shown in Figure F4-8 and F4-9, the holes appeared to be etched into the glass which indicates that they probably were caused by pinholes in the photo resist during etching of the bonding pad openings. The pinholes were probably caused by flaking of the photo resist over hillocks in the metalization.

4.2 I_{IO} (V_{CM} = -15V) FAILURE

Four Manufacturer B and two Manufacturer C parts failed I_{IO} at a common mode voltage of -15V during accelerated life. The failed values ranged from -592 nA to +143 nA. Three of the Manufacturer B parts also failed $+I_{IB}$ (V_{CM} = -15V) and one of the Manufacturer C parts also failed $+I_{IB}$ (-15V) and $-I_{IB}$ (-15V).

I_{IO} of five of the parts was excessive at a common mode voltage of -15V because the inverting input bias current ($-I_{IB}$) was normal, but the non-inverting input bias current ($+I_{IB}$) was too low or negative at negative common mode voltages, as illustrated in Figures F4-10 and F4-11. This was indicative of excessive current from V+ to the non-inverting input (pin 3). Examination of the I-V characteristic from V+ to pin 3 (with V- and pin 2 grounded) of each part disclosed the presence of anomalous channel current, as illustrated in Figure F4-12. I_{IO} of the sixth part (Manufacturer C, 125°C failure) was excessive at V_{CM} = -15V because $+I_{IB}$ was excessive and $-I_{IB}$ was negative.

The two Manufacturer C parts recovered prior to bench testing and two of the Manufacturer B parts were baked and both recovered, indicating that the anomalous leakage was caused by a surface related mechanism. The other two Manufacturer B parts were delidded for analysis but both recovered instantly upon delidding and neither contained any visible defects. Thus, the specific failure mode of these parts was not determined. During life test, 38 and 40



900X S/N 293

FIGURE F4-8. SEM PHOTO OF TWO PINHOLES (ARROW) IN THE GLASSIVATION

10,000X S/N 293

FIGURE F4-9. SEM CLOSE-UP OF A GLASSIVATION PINHOLE

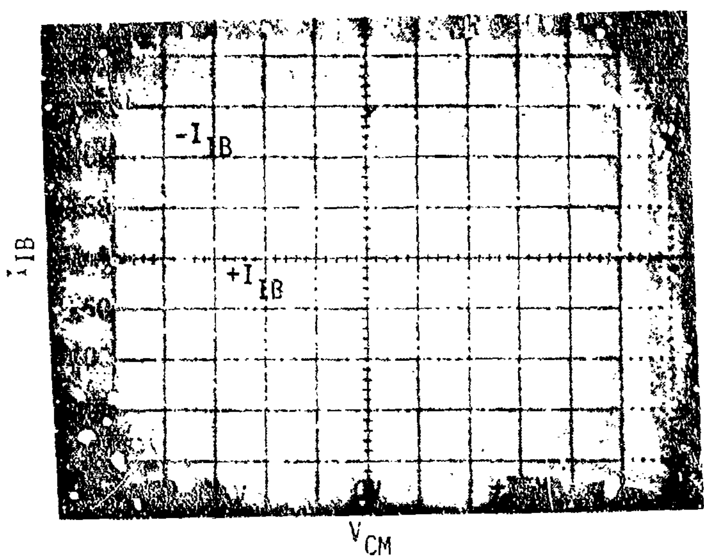


FIGURE F4-10. $+I_{IB}$ AND $-I_{IB}$ VS. V_{CM} OF A PART (S/N 174) THAT HAD FAILED I_{IO} DUE TO LOW $+I_{IB}$ AFTER 1,000 HRS AT 150°C

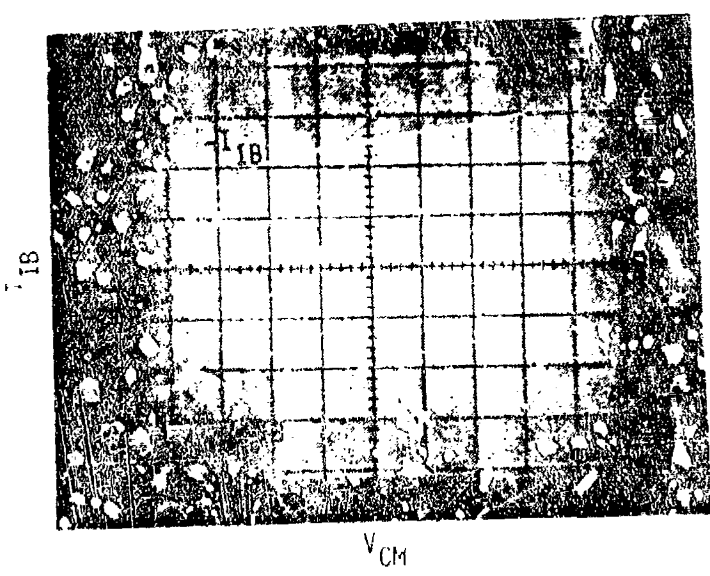


FIGURE F4-11. $+I_{IB}$ AND $-I_{IB}$ VS. V_{CM} OF A PART (S/N 144) THAT HAD FAILED I_{IO} DUE TO NEGATIVE $+I_{IB}$ AFTER 1,000 HOURS AT 150°C

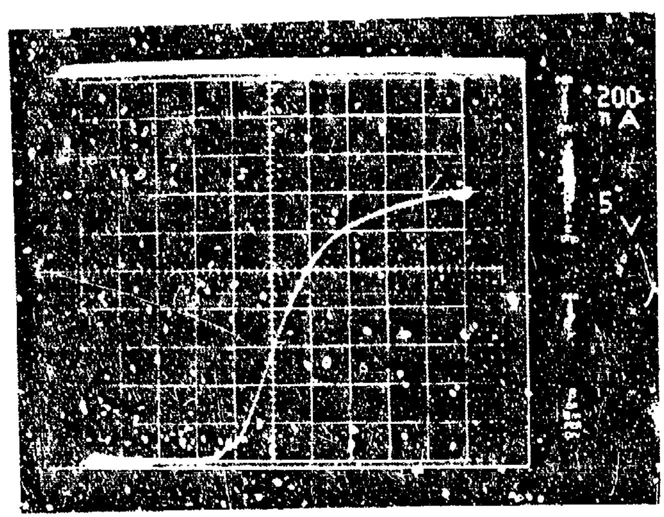


FIGURE F4-12. I-V CHARACTERISTIC FROM V+ TO PIN 3 WITH V- AND PIN 2 GROUNDED OF A PART (S/N 175) THAT HAD FAILED I_{IO} DUE TO NEGATIVE $+I_{IB}$ AFTER 1,000 HRS AT 150°C

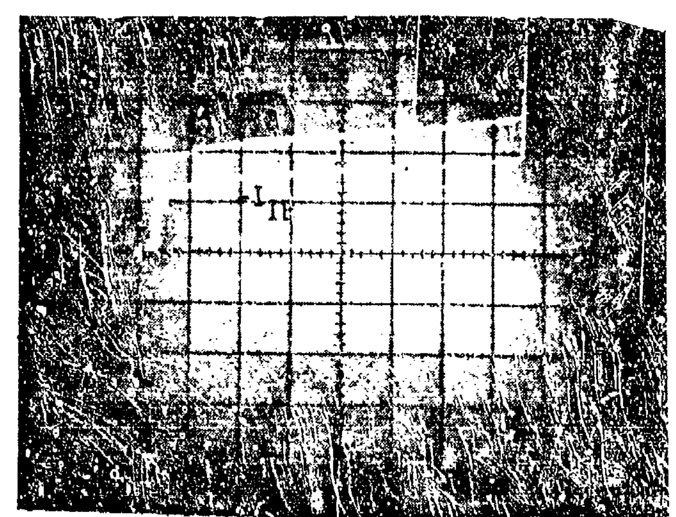


FIGURE F4-13. $+I_{IB}$ AND $-I_{IB}$ VS. V_{CM} OF A PART (S/N 35) THAT HAD FAILED I_{IO} DUE TO EXCESSIVE $+I_{IB}$ AFTER 1,000 HOURS AT 175°C

Vdc was applied from V+ to the inputs. This reversed biased the collector-base junctions of the input transistors. Consequently, it is believed that the anomalous leakage was the result of inversion of the c-b juntion of an input transistor caused by mobile ions or charges in or on a passivation layer.

4.3 I_{IO} and/or I_{IB} FAILURE

Two Manufacturer B and four Manufacturer C parts failed combinations of I_{IO} and $+I_{IB}$ or $-I_{IB}$, usually at all three common mode voltages during accelerated life. This was because one of the input bias currents was significantly higher than the other, as illustrated in Figure F4-13. The problem was traced to a gain mismatch in the input transistors. For example, the part illustrated in Figure F4-13 had (at V_{CM} = +15V) an I_{IO} of 75 nA, a $+I_{IB}$ of 246 nA, and a $-I_{IB}$ of 173 nA at the time of failure (1000 hours). Die level probing established that, at a V_{CB} of 5 volts and a collector current of 25 μA, h_{FE} of Q3 (the -input transistor) was 83 and h_{FE} of Q4 (the +input transistor) was 52. $+I_{IB}$ was 42% higher than $-I_{IB}$, and h_{FE} of the +input transistor was 37% lower than h_{FE} of the -input transistor, thus, the gain difference accounted for the excessive I_{IO}. The life test data indicated that the gain of both inputs had degraded during life. Initially, $+I_{IB}$ and $-I_{IB}$ at V_{CM} = +15 were 133 and 132 nA, respectively. At the time of failure $+I_{IB}$ was 246 nA and $-I_{IB}$ was 173 nA. The other parts displayed similar degradation except that in one part at the time of failure $-I_{IB}$ was greater than $+I_{IB}$. The gain degradation was present only at low collector currents. The gain of both transistors in the example was 156 at I_C = 1 mA. This indicated that the low gain was caused by degradation of the base-emitter junction, probably due to depletion of the p-type base region. I_{IO} and I_{IB} would recover upon baking, indicating that the degradation was the result of a surface related mechanism, probably caused by ionic contamination in the passiviation.

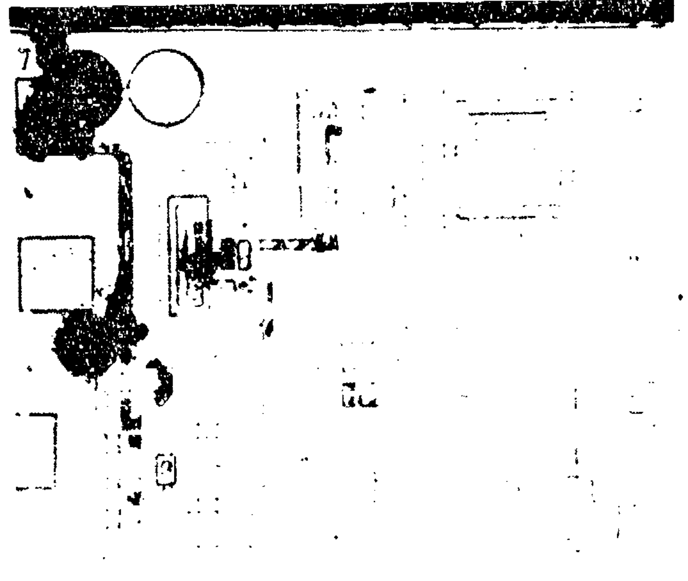
4.4 CATASTROPHIC DAMAGE DUE TO THERMAL RUNAWAY (MANUFACTURER C ONLY)

During step stress, four Manufacturer C parts drew excessive supply current at temperature and failed. The 200°C failure drew nominal current upon reaching temperature, but was drawing excessive current upon completion of the step and was found to be latched up to V- when measured during the post-step parametric tests. Examination of the part disclosed that the V+ wire and the metallization stripes had melted, as shown in Figure F4-14. All of the damage occurred at the V+ ohmic contacts of the circuit elements, and this indicated that the damage was caused by thermal runaway. The other three parts drew excessive current after reaching temperature (250°C or 275°C) and were removed and tested at this point. One part was latched to V+, one part exhibited V_{IO}'s of -7mV, and one part failed only $-A_{VS}$ [74]. Examination of these parts disclosed that each contained spears of aluminum extending from a contact of the cross-under (RX1) between V+ and C1, as illustrated in Figure F4-15, and either spears extending from the ohmic contacts of C1 or a flash-over short across the p-n junction of C1, as illustrated in Figure F4-16, and no other damage. This indicated that the thermal runaway probably initiated at C1, but the p-n junction contained no apparent defect or deficiency.

The accelerated life test temperatures were limited to 175°C, but three Manufacturer C parts displayed the same failure mode as did the step-stress parts. One part was latched-up after one hour at 175°C and two parts were latched after 4,000 hours at 175°C. As illustrated in Figure F4-17, all three parts contained damage almost identical to that found in the 200°C step-stress failure. The failures indicated that the thermal runaway mechanism was not strictly temperature dependent, but was time dependent as well. However, no reason for the time dependency was found.

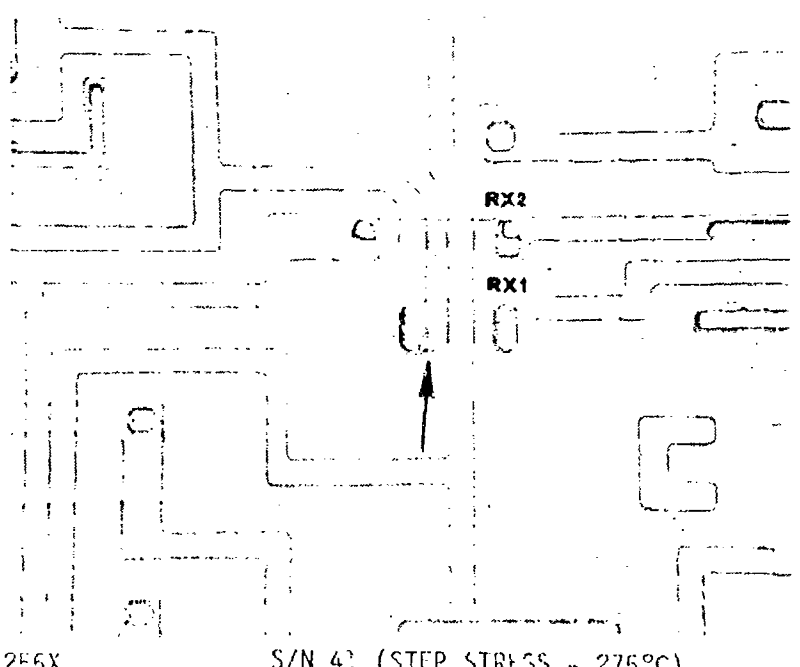
4.5 SHORTED CAPACITOR (MANUFACTURER C ONLY)

Five Manufacturer C failures during accelerated life were caused by



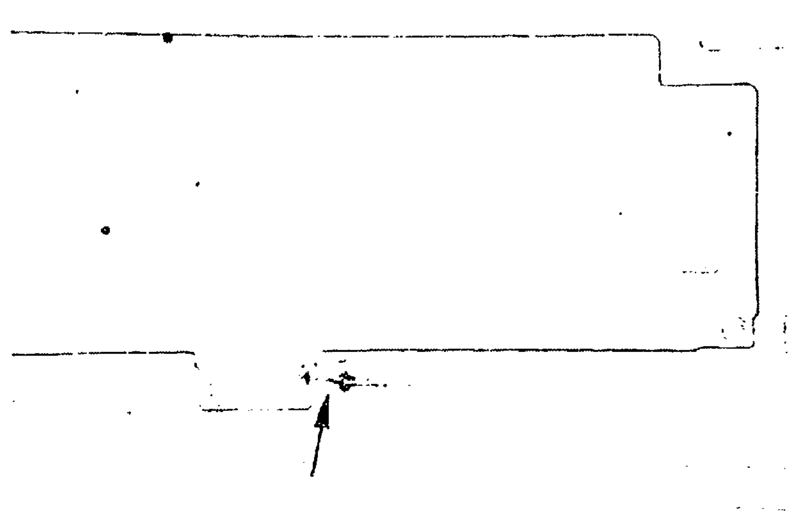
105X S/N 34 (STEP STRESS - 200°C)

FIGURE F4-14. DAMAGE SUSTAINED BY THE 200°C STEP STRESS FAILURE



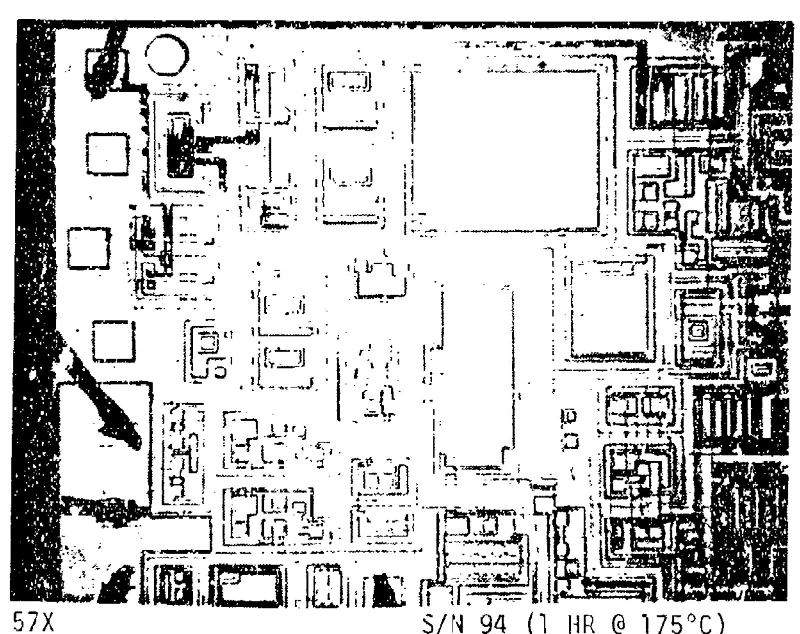
256X S/N 41 (STEP STRESS - 275°C)

FIGURE F4-15. SPEARS OF ALUMINUM-SILICON (ARROW) EXTENDING FROM THE CROSS-UNDER OHMIC CONTACT (GLASS AND ALUMINUM STRIPES REMOVED)



256X S/N 42 (STEP STRESS - 275°C)

FIGURE F4-16. FLASH-OVER SHORT (ARROW) IN C1 (DELINEATED BY SIRTL ETCH)



57X S/N 94 (1 HR @ 175°C)

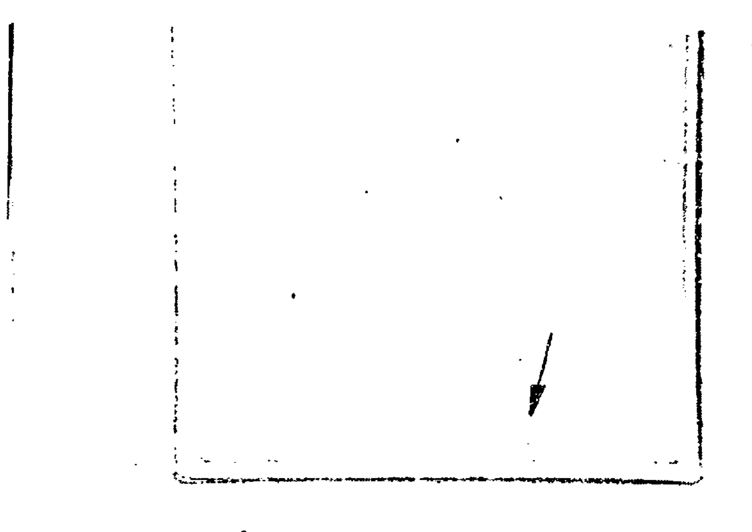
FIGURE F4-17. DAMAGE SUSTAINED BY AN ACCELERATED LIFE TEST FAILURE

defects in the dielectric oxide of one of the MOS capacitors, C2 or C3. Two parts were latched-up to V+, one after 128 hours at 125°C and one after 4,000 hours at 175°C. Examination of the dice revealed no visible damage or defect. In each part, the latch-up was traced to a 40 ohm short-circuit in the MOS capacitor C2. Removal of the aluminum electrode of the 125°C failure disclosed a minute breakdown site in the dielectric at an imperfection in the SiO_2, as shown in Figure F4-18. The 175°C failure contained a pinhole defect in the dielectric of C2, as shown in Figure F4-19. Three parts were latched-up to V-, one after four hours at 150°C, one after 2,000 hours at 150°C, and one after 4,000 hours at 175°C. Examination of each die disclosed thermal runaway damage similar to that displayed by parts shown in Figures F4-14 and F4-17. However, die level probing of the capacitors disclosed that in each part, C3 contained a 15-150 ohm short. Removal of the aluminum electrode revealed a pinhole defect in the C3 dielectric of each part, as illustrated in Figures F4-20 and F4-21. Thus it is believed that the thermal runaway in these three parts was initiated by failure of C3 caused by the oxide pinholes.

4.6 CATASTROPHIC DAMAGE DUE TO ELECTRICAL OVERSTRESS

One Manufacturer C part was latched to the positive supply after 1,000 hours at 125°C. Examination of the die revealed that the pin 2 (-input) metalization stripe had vaporized open due to excessive current, as shown in Figure F4-22. A small particle bridged between the pin 2 stripe and the edge of the substrate, but the particle was nonconductive (transparent) and could not have caused the excessive current. Therefore, this failure was probably caused by electrical overstress of pin 2.

One Manufacturer C part had passed the 25°C parametric tests after 4,000 hours at 150°C, but was latched to the negative supply during the +125°C parametric tests. When bench tested, the part was found to be latched negative at 25°C. Examination of the die revealed flash-overs through the cross-under in the V+ (pin 7) line, RX1, and the cross-under in the COMP C (pin 8) line,

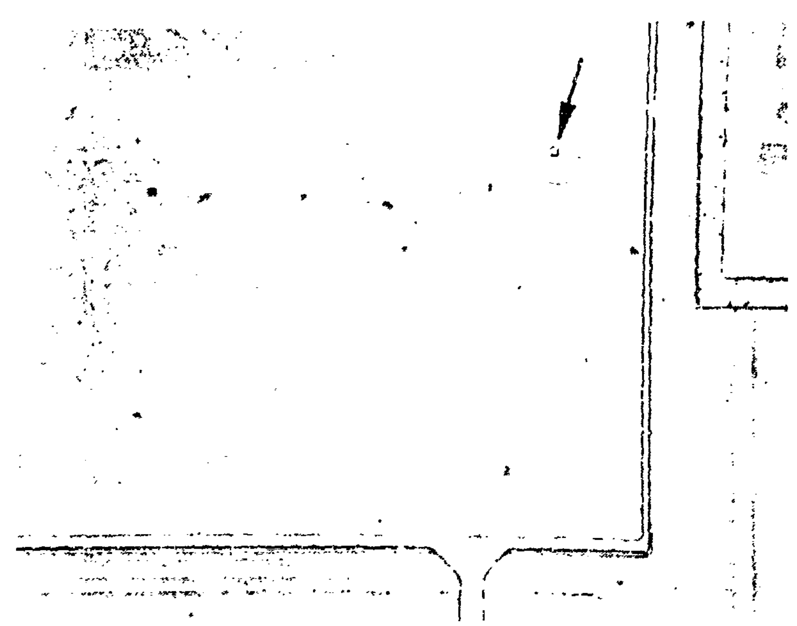


400X S/N 282 (128 HRS @ 125°C)

FIGURE F4-18. C2 AFTER REMOVAL OF THE ALUMINUM ELECTRODE SHOWING THE BREAKDOWN SITE (ARROW)

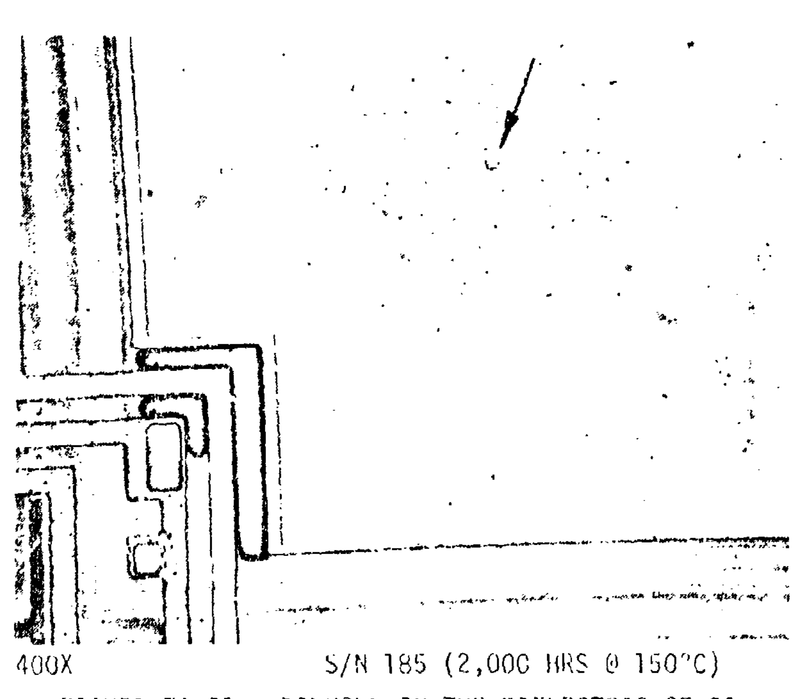
400X S/N 121 (4,000 HRS @ 175°C)

FIGURE F4-19. C2 AFTER REMOVAL OF THE ELECTRODE SHOWING THE OXIDE PINHOLE (ARROW)



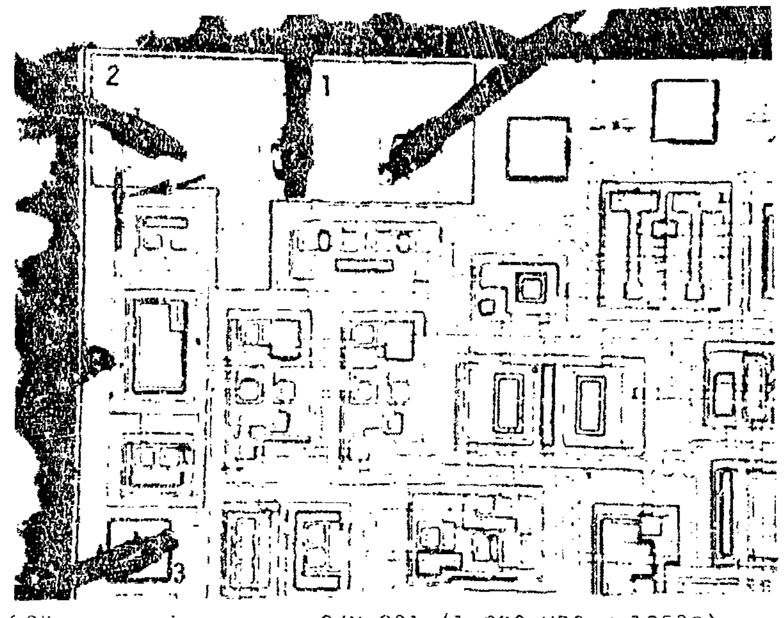
256X S/N 132 (4 HRS @ 150°C)

FIGURE F4-20. PINHOLE IN THE DIELECTRIC OF C3



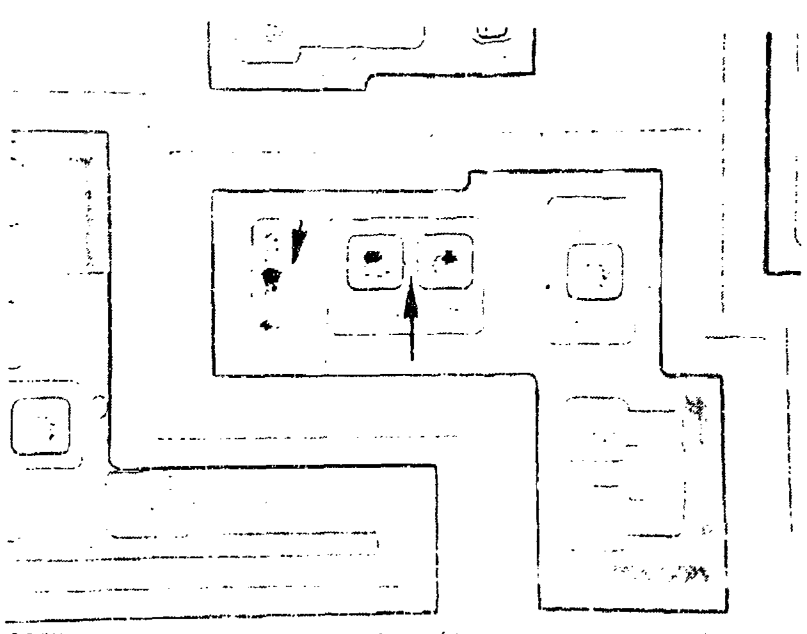
400X S/N 185 (2,000 HRS @ 150°C)

FIGURE F4-21. PINHOLE IN THE DIELECTRIC OF C3



80X S/N 221 (1,000 HRS @ 125°C)

FIGURE F4-22. MELTED OPEN PIN 2 STRIPE (ARROW)

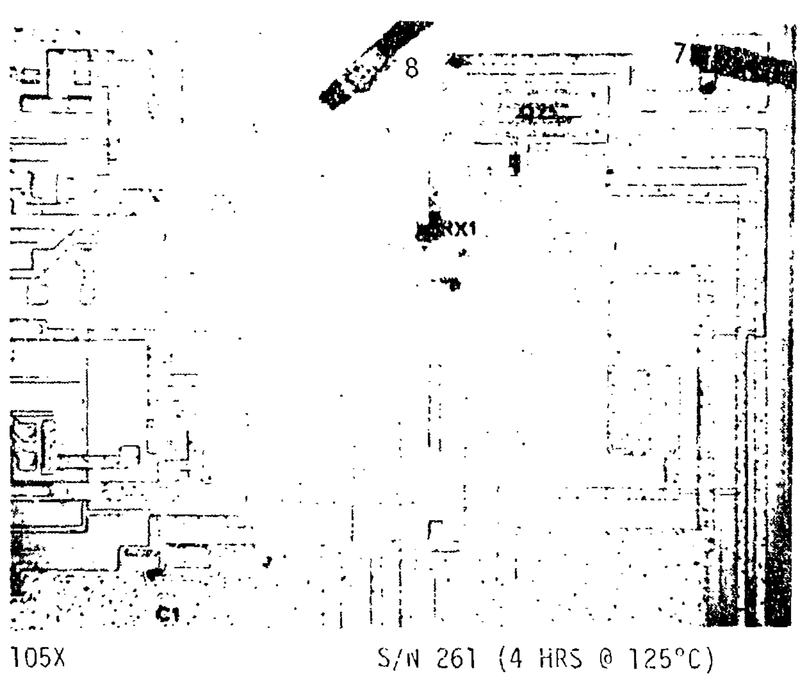


256X S/N 175 (4,000 HRS @ 150°C)

FIGURE F4-23. FLASH-OVER DAMAGE (ARROWS) IN Q20 REVEALED BY SIRTL ETCH

RX2. Examination of Q20, which is connected between pin 8 and V+, disclosed that it contained flashover shorts, as shown in Figure F4-23. Consequently, this failure was attributed to electrical overstress of Q20 probably caused by a transient or static discharge across pins 7 and 8 prior to the +125°C parametric tests.

One Manufacturer B part was latched-up after four hours at 125°C. This part contained damage at Q25, C1 and a cross-under, as shown in Figure F4-24, indicating that it probably had been electrically overstressed.



105X S/N 261 (4 HRS @ 125°C)

FIGURE F4-24. DAMAGE SUSTAINED BY THE MANUFACTURER B CATASTROPHIC FAILURE

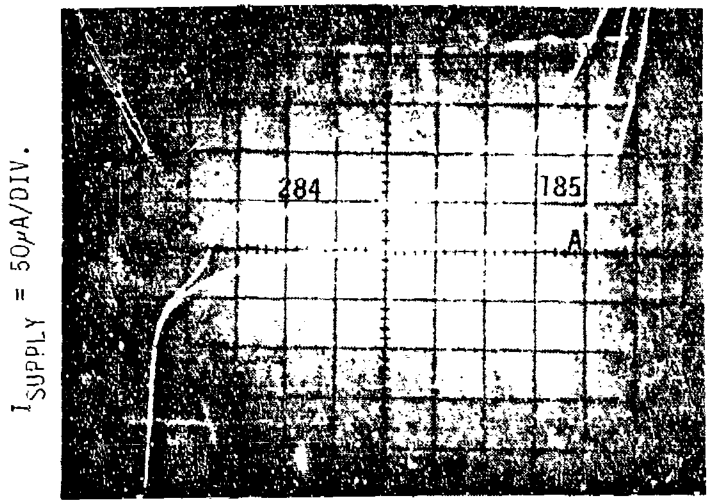
5.0 LM108A FAILURE ANALYSIS REPORT

5.1 RESISTOR TUB INVERSION (MANUFACTURER B ONLY)

Eighty-six Manufacturer B parts failed V_{IO} and/or A_{VS} during step-stress and accelerated life. Sixty-five parts failed V_{IO}, ten parts failed A_{VS}, and eleven parts failed both V_{IO} and A_{VS}. Many of the parts also failed other associated parameters such as I_{IO}, PSRR and CMR because V_{IO} was severely degraded. The failures were bake recoverable, indicative of a surface instability mechanism.

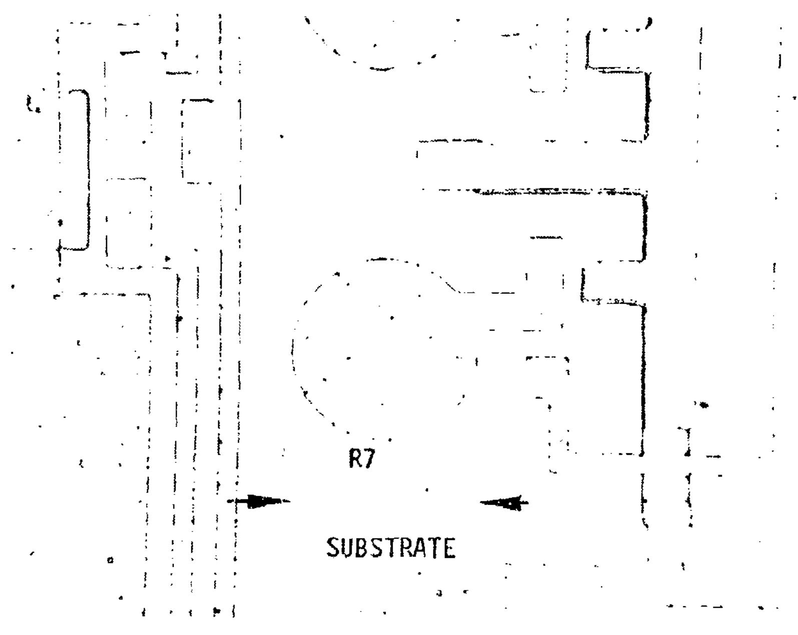
Of the 75 parts which failed V_{IO}, the predominant failure was V_{IO} at a supply voltage of $\pm$20V and V_{CM} of -15V. The failed values were always positive and ranged from 0.5mV (the specified maximum limit) to 19mV (the latch limit of the test circuit). These parts exhibited anomalous current from V+ to V- proportional to the degree of V_{IO} failure, as illustrated in Figure F5-1. S/N A is a sample part with normal V_{IO}. Its I-V characteristic is essentially I_{DSS} of J-FET Q19 amplified by Q22. S/N 185 exhibited a V_{IO} of +.63mV after four hours at 225°C and exhibits anomalous current beginning at V+ to V- equal to about 20 volts. S/N 284 exhibited a V_{IO} of >19mV after four hours at 225°C and exhibits anomalous current beginning at V+ to V- equal to about 4 volts.

V_{IO} of these parts would recover instantly upon delidding, as illustrated in Table F5-1. Because the symptoms of these failures were very similar to those of the Manufacturer B LM118 device (reference paragraph 4.1), it was suspected that LM108A failures might also be due to inversion of an n-type resistor tub. To determine if any tub was still slightly inverted or depleted after delidding, a manipulator probe biased at -100 volts was scanned over the resistor tubs. It was found that the failure, i.e., excessive positive V_{IO}, could be reinduced by applying negative potential across the oxide above the tub containing R3, R7, R13, R14 and R30 in the region along the perimeter of R7 adjacent to the isolation diffusion were shown in Figure F5-2. The leakage



V_{SUPPLY} (+ TO -) = 5 VOLTS/DIV.

FIGURE F5-1. I-V CHARACTERISTICS FROM V+ TO V- OF A NORMAL PART (S/N A) AND OF TWO PARTS THAT HAD FAILED V_{IO} (S/Ns 185 AND 284)



256X S/N 282

FIGURE F5-2. RESISTOR R7 SHOWING THE REGION OF ANOMALOUS CURRENT (ARROWS) AS DETERMINED VIA THE VOLTAGE PROBE

TABLE F5-1. EXAMPLES OF V_{IO} RECOVERY DISPLAYED BY THE MANUFACTURER B LM108A UPON DELIDDING

S/N	CELL	t_F	t_R	V_{IO} @ V_{CM} = -15V (mV) @ t_0	@ t_F	@ t_R	PRIOR TO DELIDDING 1/	IMMEDIATELY AFTER DELIDDING 1/
282	225°C LIFE	4 HR	4 HR	-0.03	>+19	-	+10	-0.01
141	225°C LIFE	4 HR	1000 HR	+0.05	>+19	>+19	+37	+0.24
62	200°C LIFE	4 HR	1000 HR	-0.20	>+19	+11	+7.2	+0.05
202	175°C LIFE	1000 HR	1000 HR	-0.35	>+19	-	+3.2	-0.20

NOTES

t_F = Time of Failure

t_R = Time of Removal From Life Test

t_0 = Prior to Life Test

1/ = Curve Tracer Test

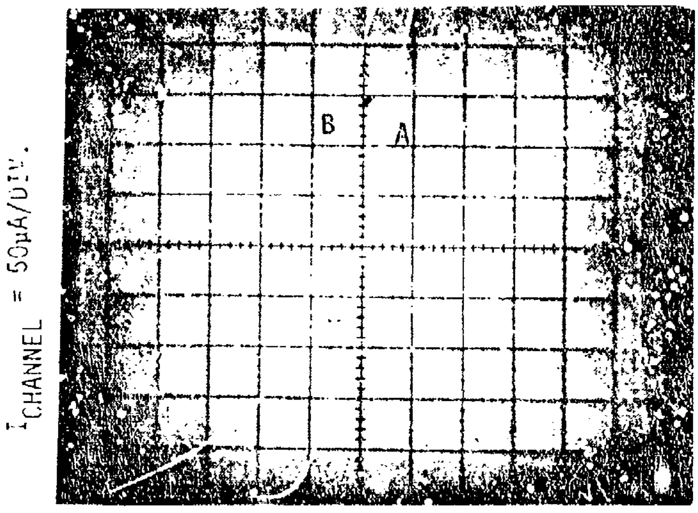
current from the resistors to the substrate (determined after severing appropriate stripes) would increase upon application of the negative field in this region of the tub, as shown in Figure F5-3. This indicated that the failures probably had been caused by anomalous channel current from the resistors to the substrate due to inversion of the n-type resistor tub. Inversion of n-type material is caused by the accumulation of a net negative charge in or on the passivation layers.

The parts that had failed only A_{VS} exhibited two basic types of anomalous gain. Some parts exhibited negative gain that was too low at V_{OUT} = +15V and -15V as illustrated in Figure F5-4 and others exhibited positive gain that was too low at V_{OUT} = +15V as illustrated in Figure F5-5. The gain characteristics indicated that the low gain was probably caused by gain distortion due to variation in V_{IO} with output voltage. These parts exhibited anomalous current from V+ to V-, as illustrated in Figure F5-6 and recovered instantly upon delidding, as shown in Table F5-2. These findings indicate that the failure mode of the parts failing only A_{VS} was probably the same as that of the V_{IO} failures, i.e., inversion of the R7 resistor tub.

The resistor tub to substrate junction was reverse biased at 40 Vdc during the tests. Thus, the accumulation of negative charge over the tub was probably the result of separation of mobile ionic species in the fringing field of the reverse biased junction or electron drift in the field along defects in the glass insulator interface [2]. Microscopic examination of failed parts disclosed anomalies in the glassivation similar to, but not as severe as, those found in the Manufacturer B LM118 failures. Seventy percent of the parts examined (21 out of 30) contained at least one crack in the glassivation, as illustrated in Figure F5-7. Using an aluminum etch it was determined that 30% (10 out of 30) of the parts also contained glassivation pinholes.

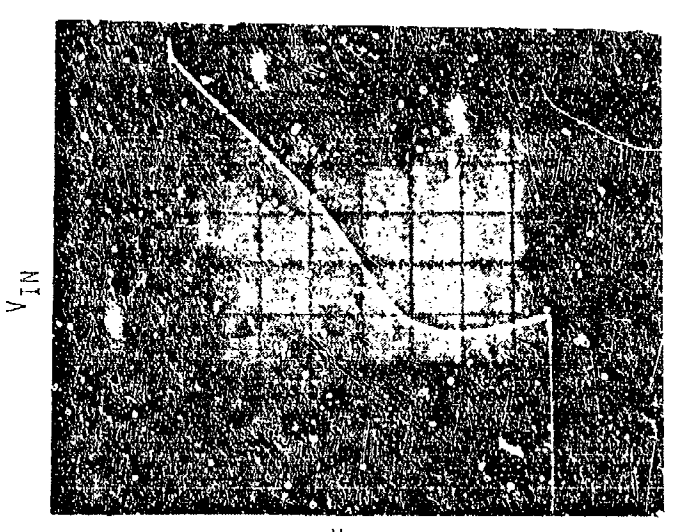
5.2 CATASTROPHIC DAMAGE DUE TO THERMAL RUNAWAY (MANUFACTURER A ONLY)

Thirty-seven Manufacturer A parts failed during accelerated life that



$V_{RESISTOR\text{-}SUBSTRATE}$ = 5 VOLTS/DIV.

FIGURE F5-3. I-V CHARACTERISTIC FROM R7 TO THE SUBSTRATE WITH NO FIELD (TRACE A) AND WITH A NEGATIVE FIELD (TRACE B) APPLIED ACROSS THE OXIDE OVER THE TUB



V_{OUT}

FIGURE F5-4. GAIN CURVE OF A PART WITH LOW $+A_{VS}$ [71] AND $-A_{VS}$ [72].

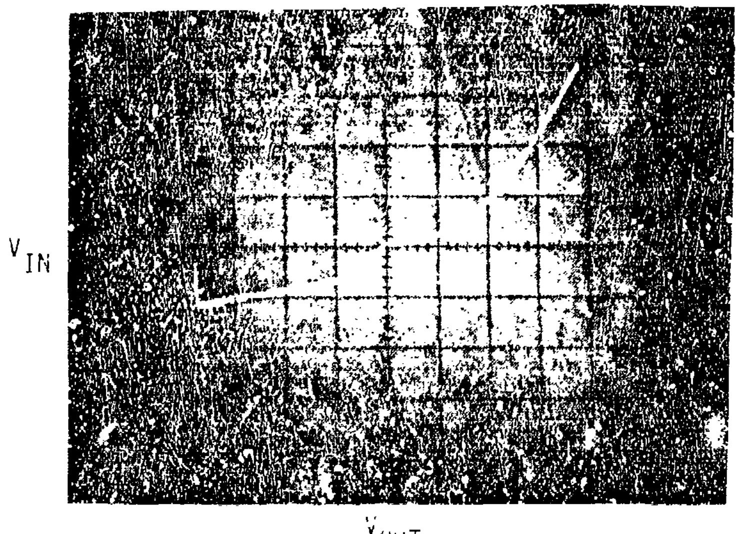


FIGURE F5-5. GAIN CURVE OF A PART WITH LOW $\pm A_{VS}$ [71]

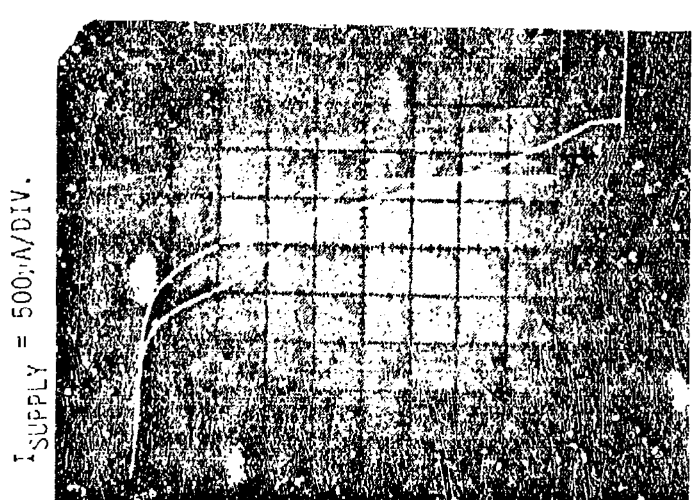


FIGURE F5-6. I-V CHARACTERISTICS FROM V+ TO V- OF TWO PARTS WITH LOW GAIN

TABLE F5-2. EXAMPLES OF A_{VS} RECOVERY DISPLAYED BY THE MANUFACTURER B LM108 UPON DELIDDING

S/N	CELL	t_F	t_R	PARAMETER	PARAMETER HISTORY @ t_0	@ t_F	@ t_R	PRIOR TO DELIDDING 1/	IMMEDIATELY AFTER DELIDDING 1/
235	175°C LIFE	1000 HRS	1000 HRS	$+A_{VS}$ [71] (V/mV)	361	49	-	75	375
				$-A_{VS}$ [72] (V/mV)	377	19	-	25	375
104	200°C LIFE	1000 HRS	1000 HRS	$+A_{VS}$ [71] (V/mV)	438	51	-	75	500
171	225°C LIFE	256 HRS	1000 HRS	$+A_{VS}$ [71] (V/mV)	3628	24	17	19	750
				$-A_{VS}$ [72] (V/mV)	264	97	16	19	341
				$+A_{VS}$ [75] (V/mV)	530	177	4	3	200
				$-A_{VS}$ [76] (V/mV)	267	1754	4	5	100

NOTES

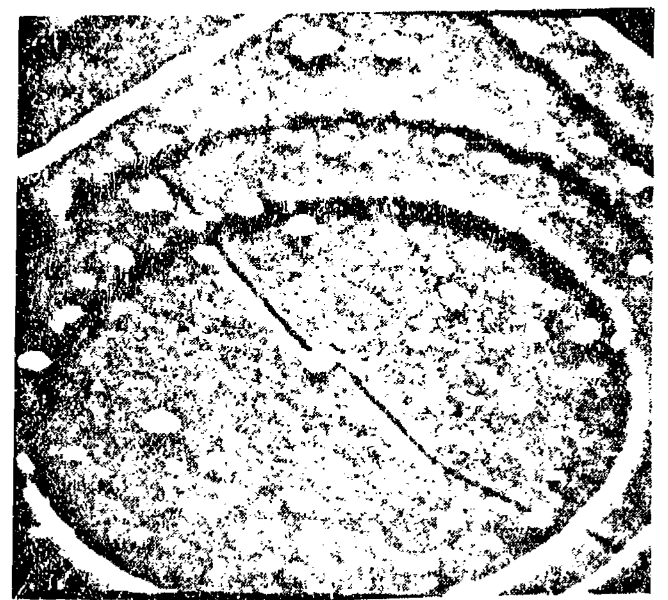
t_F = TIME OF FAILURE

t_R = TIME OF REMOVAL

t_0 = PRIOR TO LIFE TEST

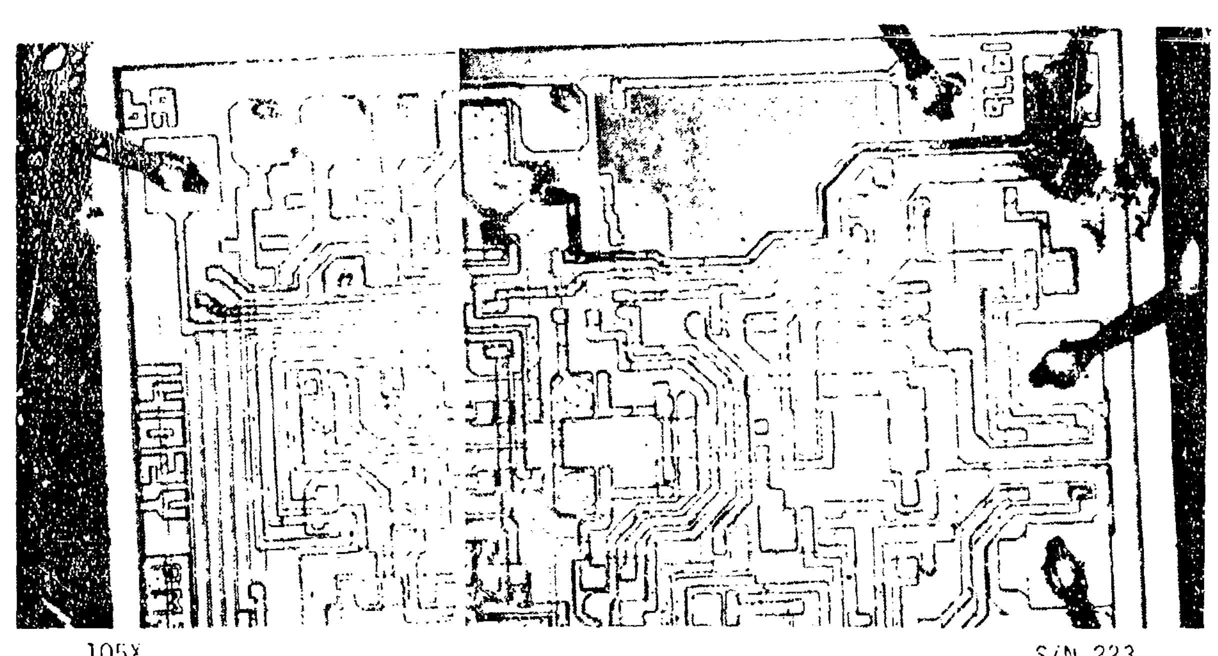
1/ = CURVE TRACAER TEST

FAILED PARAMETERS ARE UNDERLINED.



200X S/N 374

FIGURE F5-7. EXAMPLE OF GLASSIVATION CRACK IN THE MANUFACTURER B LM108A (SEM PHOTO)



105X S/N 223

FIGURE F5-8. EXAMPLE OF MOST SEVERE DAMAGE SUSTAINED BY A MANUFACTURER A LM108A

were latched to either V+ or V-. Twenty-six parts were date coded 7642, ten parts were date coded 7643, and one part was date coded 7652. Examination of the parts disclosed catastrophic damage such as depleted or melted aluminum along the V+ stripe and aluminum spears protruding from various ohmic contacts to V+. An example of the most severe damage found is shown in Figure F5-8. Some parts contained only depleted aluminum and aluminum spears at the Q6 emitter contact, as illustrated in Figure F5-9. Every failed part, regardless of the amount of total damage present, contained depleted aluminum or spears at the Q6 emitter contact, which indicated that the problem originated at Q6. The life test monitor readings revealed that the failed devices drew excessive current indicating that the failures had occurred while the parts were at elevated temperature, consequently, a thermal runaway mechanism was suspected as the cause rather than any external electrical overstress condition. Furthermore, the life test start-up had indicated that the 7642 date coded parts were susceptible to thermal runaway (Ref: Section 6.1).

Q6 is a lateral PNP transistor. The failed Q6 transistors almost always contained an aluminum-silcon melt-channel or an aluminum spear extending from the emitter contact, indicative of excessive emitter current. The emitter of Q6 is connected directly to V+, but its collector-base is connected to circuitry of sufficient impedance to limit the collector current. However, a lateral parasitic PNP transistor exists between the emitter of Q6 and the substrate. As shown in Figure F5-10, the base current, I_B, of Q6 can cause a slight parasitic PNP collector current, I_{CP}, to flow from the Q6 emitter to V-. At elevated temperature, this current can possibly increase to damaging levels since there is no series limiting resistance for the parasitic current path. The path of damage emanating from the Q6 emitter always pointed in the direction of the c-b contact (the direction of base current flow), as illustrated in Figure F5-11, indicating that the damage probably was the result of excesssive parasitic PNP collector current. Transistor Q6 is adjacent to three "zappable" transistors, Q29, Q30, and Q31, that are used to trim the offset voltage. However, in many of the failed parts, none of the three transistors had been zapped; therefore, the proximity of Q6 to these transistors was not considered significant.

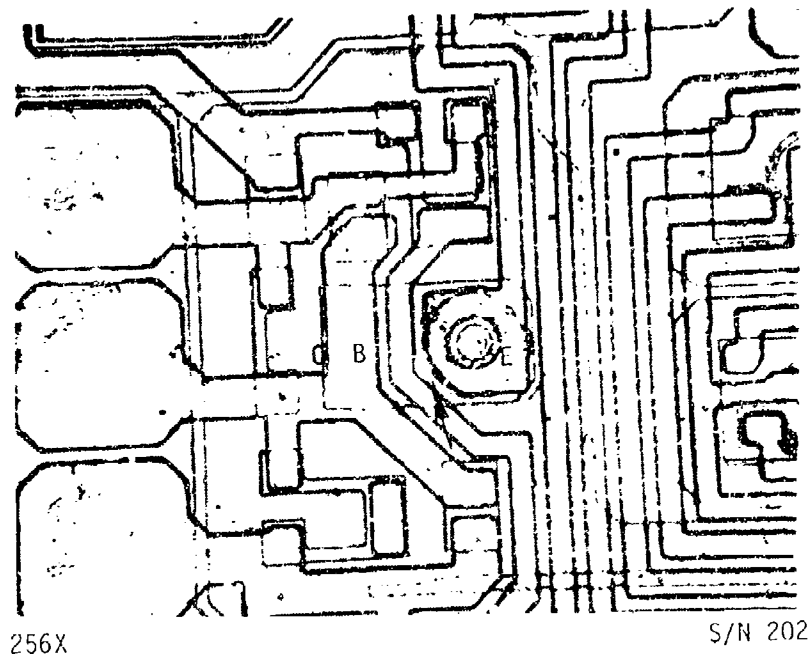


FIGURE F5-9. DEPLETED ALUMINUM AND ALUMINUM SPEAR (ARROW) AT THE Q6 EMITTER

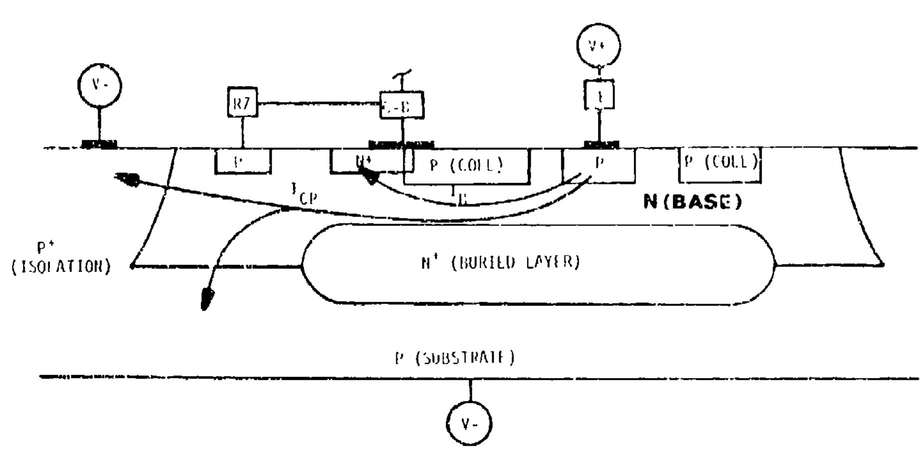
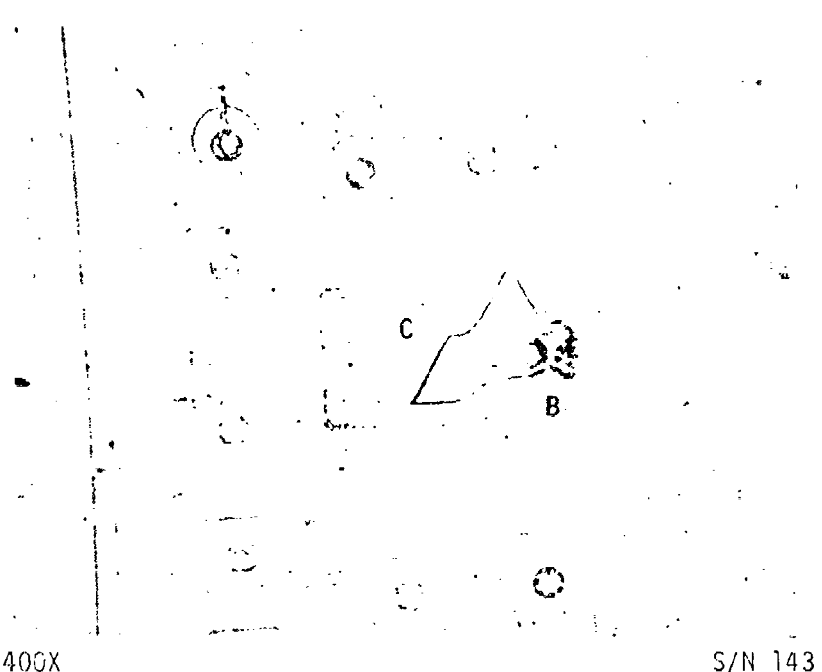


FIGURE F5-10. CROSS-SECTIONAL SKETCH OF Q6



400X S/N 143

FIGURE F5-11. PATH OF DAMAGE EMANATING FROM THE Q6 EMITTER AS DELINEATED WITH SIRTL ETCH

The failure data showed a time-temperature dependency but the exact cause of the dependency was not established. The failure mechanisms identified in these parts involved parasitic PNP current and localized thermal runaway which led to excessive Q6 emitter current and aluminum melting or migration/silicon dissolution which led to the opens and shorts. The physical appearance of the melting and migration indicated that the damage probably occurred relatively rapidly with little time dependency. Parasitic PNP current and thermal runaway are temperature dependent, but ordinarily are not time dependent mechanisms. Examination of the life test monitor readings disclosed no sign of supply current increase with time in the parts that failed. The supply current of each part was constant until the time of failure at which point the current jumped and the part failed.

5.3 A_{VS} FAILURE DUE TO SURFACE INSTABILITY (MANUFACTURER A ONLY)

Nine Manufacturer A parts failed $+A_{VS}$ [71] during accelerated life. The failed values ranged from 79 to 30 V/mV. All nine parts were left on test. Three parts failed catastrophically at 2000 hours due to thermal runaway at Q6. By 4000 hours, $+A_{VS}$ [71] of the other six parts had recovered as illustrated in Table F5-3. The recovery indicated that the gain failures probably were caused by a surface related mechanism. Since the parts had recovered the exact failure mode could not be determined.

TABLE F5-3. EXAMPLES OF $+A_{VS}$ [71] RECOVERY

S/N	CELL TEMP	FAILURE	VALUE OF $+A_{VS}$ [71] (V/mV) INITIAL	1 HR	256 HR	1000 HR	2000 HR	4000 HR
332	175°C	1 HR	103	<u>79</u>	101	142	128	139
194	175°C	1000 HRS	717	680	620	<u>36</u>	<u>23</u>	656
214	175°C	2000 HRS	509	409	402	91	<u>32</u>	104

NOTES

FAILED VALUES ARE UNDERLINED

5.4 I_{IO}/I_{IB} FAILURES - TEST ANOMALY

Four Manufacturer B parts and nine Manufacturer A parts failed $+I_{IB}$, $-I_{IB}$, and/or I_{IO} through 500 hours of accelerated life. During the same time period, three Manufacturer A control parts also failed I_{IO} and $\pm I_{IB}$. All three exhibited excessive $+I_{IB}$ and $-I_{IB}$ at each common mode voltage and supply voltage. One part was analyzed and found to contain no anomaly. The other two parts were baked for 16 hours at 250°C, and both recovered. The history of $+I_{IB}$ and $-I_{IB}$ at V_{CM} = 0 volts and $\pm V$ = ± 20 volts of each control part is presented in Table F5-4. The accelerated life failures likewise recovered when baked.

In view of the failure of the three control parts, it was suspected that the degradation was caused by the parametric testing or by handling of the parts. Experiments were conducted which established that the parametric testing did not induce any detectable degradation. Therefore, it was decided to treat the LM108As as static sensitive parts and implement all precautionary measures for handling such parts. This was done immediately after the 500 hour test point and, as a result, no further I_{IO}/I_{IB} failures of this type were encountered. Apparently, the input transistors of the failed parts had been degraded by static charge generated during handling. For reasons unknown, the damage was not permanent and could be annealed by baking.

TABLE F5-4 - I_{IB} HISTORY OF THE THREE FAILED MANUFACTURER A CONTROL PARTS

	I_{IB} (nanoamperes)					
	S/N 61		S/N 62		S/N 63	
	$+I_{IB}$ (0,20)	$-I_{IB}$ (0,20)	$+I_{IB}$ (0,20)	$-I_{IB}$ (0,20)	$+I_{IB}$ (0,20)	$-I_{IB}$ (0,20)
INITIAL VALUE (3/24/77)	0.706	0.683	0.997	1.050	0.695	0.682
VALUE PRIOR TO FAILURE (10/5/77)	0.766	0.740	1.116	1.082	0.743	0.733
VALUE AT THE TIME OF FAILURE (10/11/77)*	8.2	8.5	14.0	13.9	8.0	8.5
VALUE AFTER BAKING	1.100	1.073	⊛	⊛	1.157	1.158

NOTES

* VALUE OBTAINED DURING BENCH TEST
⊛ DELIDDED FOR F/A

6.0 LM109 FAILURE ANALYSIS REPORT

6.1 OPEN PIN DUE TO INTERMETALLIC GROWTH (MANUFACTURER B ONLY)

Four Manufacturer B parts failed during accelerated life due to an open internal wire bond at the post. Three parts contained an open bond at pin 1, one after 500 hours at 200°C, one after 4,000 hours at 225°C, and one after 250 hours at 250°C. One part contained an open bond on one of the pin 2 wires after 64 hours at 225°C. In each case, the three mil aluminum wire lifted from the gold-plated post. Separation occurred in the intermetallic zone, as shown in Figure F6-1 and F6-2, and the fracture surfaces were purple-colored. This indicated that the failure mechanism was Kirkendall voiding in $AuAl_2$. Because these failures were random, the excessive $AuAl_2$ was probably generated during the wire bonding operation.

6.2 OPEN PIN DUE TO BROKEN EXTERNAL LEAD

Three Manufacturer B and one Manufacturer D parts had to be removed from test because one of their external leads broke or fell off during insertion or removal from the test socket. In the earliest (8 hour) Manufacturer B failure, the pin 1 lead broke at its point of egress from the glass insulator and most likely was mechanically overstressed by mishandling. In the other three instances, the pin 3 lead broke above the weld to the case. The Manufacturer D part broke cleanly with no sign of deterioration. Thus, the break probably was caused by mishandling or flexure of the leads during insertion and removal from the test socket. The welds of the two Manufacturer B parts were blackened, as illustrated in Figure F6-3. This condition was not present upon receipt of the parts and visual examination of life test survivors after 4,000 hours disclosed that the welds of almost every part had degraded to some degree. Usually the weld was blackened and there was a ring of discoloration in the gold plating of the header around the weld. Apparently, the weld of the Manufacturer B part also contains tin based solder and the tin had scavenged or leached gold from the header and the joint at elevated temperature thereby weakening the welds.

200X S/N 174 (64 HRS @ 225 C)

FIGURE F6-1. LIFT-OFF PATTERN OF THE PIN 2 WIRE BOND

200X S/N 243 (250 HRS @ 250°C)

FIGURE F6-2. EXAMPLE OF THE LIFT-OFF PATTERN OF A PIN 1 WIRE BOND

10X S/N 264 (128 HRS @ 250°C)

FIGURE F6-3. EXAMPLE OF A PIN 3 LEAD FAILURE WITH A BLACKENED WELD

6.3 ΔI_{SCD} FAILURES

Eight Manufacturer D parts and one Manufacturer B part failed during accelerated life due to excessive standby current drain change with load change (ΔI_{SCD}[13]). ΔI_{SCD}[13] is the difference between the drain current at I_L = -5 mA (I_{SCD}[9]) and the drain current at I_L = -500 mA (I_{SCD} [11]). ΔI_{SCD}[13] has a specified minimum limit of -0.5 mA. The failed values ranged from -0.501mA to -0.640 mA. Bench tests of the parts confirmed the failed values, but examination of the test data disclosed that the ΔI_{SCD} [13] of these parts was probably out of tolerance or marginal upon receipt and this was not detected during the pre-life tests due to a test set malfunction. As shown in Table F6-1, ΔI_{SCD}[13] of the Manufacturer D parts was in tolerance and near zero (in some cases) initially and then out of tolerance or marginal at the next test point (4 hours into life). Two of the parts were left on test after failing and, through 4,000 hours, ΔI_{SCD}[13] did not vary more than two percent from the 4 hour value.

Examination of the control sample data revealed the same pattern. As shown in Table F6-2, the ΔI_{SCD}[13] of the four control samples was near zero during the initial test and then significantly higher during every subsequent test. One part was marginal or out of tolerance during every subsequent test. Consequently, it is suspected that the 500 mA test current was not being applied to the part during the initial I_{SCD}[11] measurement, due to a test set malfunction, and this caused the ΔI_{SCD}[13] values to be near zero or too low initially. The problem is suspected to be a stuck relay contact in the test set which corrected itself, since normal ΔI_{SCD}[13] values were obtained during the life tests. As indicated by the four hour values, ΔI_{SCD}[13] of these eight parts probably was out of tolerance or marginal upon receipt, consequently, these failures were not valid accelerated life failures.

TABLE F6-1. PARAMETER HISTORY OF THE ΔI_{SCD}[13] FAILURES

CELL	S/N	ΔI_{SCD}[13] - mA INITIAL	AT 4 HOURS	AT TIME OF FAILURE	AT 4,000 HOURS
200°C	44	-0.000	-0.540	(See 4 hours)	N/A
	145	-0.111	-0.640	(See 4 hours)	N/A
	143	-0.100	-0.500	-0.530 (64 hours)	N/A
225°C	164	-0.070	-0.490	-0.520 (16 hours)	N/A
250°C	264	-0.050	-0.530	(See 4 hours)	-0.540
	282	-0.111	-0.520	(See 4 hours)	N/A
	233	-0.120	-0.500	-0.560 (16 hours)	N/A
	271	-0.060	-0.500	-0.500 (1000 hrs)	-0.490

NOTE: FAILED VALUES ARE UNDERLINED.

TABLE F6-2. ΔI_{SCD}[13] HISTORY OF THE CONTROL SAMPLES

S/N	ΔI_{SCD}[13] - mA 4/8/77 (INITIAL)	8/1/77 (4 HOUR I)	8/8/77 (4 HOUR II)	4/22/78 (4,000 HRS)
11	-0.010	-0.500	-0.500	-0.540
12	-0.111	-0.290	-0.290	-0.290
13	-0.030	-0.350	-0.350	-0.350
14	-0.010	-0.350	-0.340	-0.330
15	-0.000	-0.230	-0.230	-0.240

7.0 723 FAILURE ANALYSIS REPORT

7.1 I_{SCD} FAILURE (MANUFACTURER C ONLY)

Six Manufacturer C parts exhibited excessive standby current drain (I_{SCD}) after 2,000 hours at 200°C. I_{SCD} has a specified maximum limit of 3.0 mA and the failed values ranged from 3.001 to 3.066 mA. Three of the parts were returned to life test after failing, and all were within specification at 4,000 hours. All six parts were then returned to life test for an additional 2,000 hours, after which their I_{SCD} values were virtually the same as the pre-stress values. The I_{SCD} history of the parts is shown in Table F7-1. Examination of the control sample data, also given in Table F7-1, indicated that a current sensing resistor in the test set had drifted causing an average error of +0.153 mA in I_{SCD} of the control samples at the 2,000 hour test point. Adjusting the I_{SCD} values of the six 2,000 hour failures accordingly brings all of the values to within specification. Consequently, these failures were attributed to test set drift rather than any part deficiency.

7.2 -55°C FAILURES (MANUFACTURER C ONLY)

One Manufacturer C part failed V_{RLINE}[1] and V_{RLOAD}[4] at -55°C at 4,000 hours and one Manufacturer C part failed V_{REF} at -55°C at 4,000 hours. The failures appeared to be catastrophic; therefore, the parts were retested at 25°C and were found to be within specification. The parts were returned to life for an additional 2,000 hours after which the failed parameters were within specification and virtually the same as the pre-life values, as shown in Table F7-2. Microscopic examination of the interior of the parts plus pull testing of the wire bonds disclosed no intermittencies which could account for the 4,000 hour failures. Therefore, these failures were probably caused by test socket intermittencies during the -55°C test at 4,000 hours.

7.3 I_{OS} FAILURES (MANUFACTURER D ONLY)

Two Manufacturer D parts failed I_{OS} during 175°C accelerated life. As shown in Table F7-3, one part was marginal upon receipt and simply drifted out of specification at the first test point (4 hours). Consequently, this

TABLE F7-1. I_{SCD} HISTORY

CELL	S/N	I_{SCD} @ 25°C (mA) [SPEC = 3.0 mA MAX.] PRE-STRESS	1,000 HOURS	2,000 HOURS	4,000 HOURS	ADDITIONAL 2,000 HOURS
200°C	232	2.658	2.830	3.001	2.916	2.668
	235	2.641	2.839	3.035	2.927	2.672
	313	2.656	2.792	3.015	2.885	2.630
	341	2.673	2.801	3.066	-	2.646
	363	2.626	2.760	3.024	-	2.603
	371	2.662	2.796	3.058	-	2.637
CONTROL	11	2.105	2.240	2.231	2.322	2.087
	12	1.643	1.758	1.792	1.816	1.630
	13	2.059	2.184	2.223	2.262	2.043
	14	1.863	1.975	2.013	2.048	1.849
	15	1.539	1.634	1.665	1.699	1.532
	MEAN	1.842	1.953	1.995	2.029	1.828
	MEAN Δ ($t-t_{PRE-STRESS}$)		+0.116	+0.153	+0.187	-0.014

TABLE F7-2. PARAMETER HISTORY OF THE -55°C FAILURES

CELL	S/N	PARAMETER	PARAMETER VALUES AT -55°C			SPECIFIED LIMIT
			INITIAL	4,000 HOURS	6,000 HOURS	
200°C	325	V_{RLINE}[1] (%)	-0.016	-162.878	-0.012	-.3 to .3
		V_{RLOAD}[4] (%)	-0.018	+1.704	-0.016	-.6 to +.6
	334	V_{REF} (VDC)	7.075	0.000	7.076	6.90-7.40

NOTES

1. FAILED VALUES ARE UNDERLINED.

TABLE F7-3. PARAMETER HISTORY OF THE I_{OS} FAILURES

I_{OS} (mA) (SPECIFIED LIMIT = 45 - 85 mA)

CELL	S/N	INITIAL	4 HOUR	32 HOUR	64 HOUR	BENCH TEST
175°C	175	83.3	86.1	-	-	-
	162	50.6	56.1	56.2	86.0	64.0
REF: CONTROL	(MEAN OF 5 PARTS)	62.4	63.4	62.0	61.2	-

NOTES

1. FAILED VALUES ARE UNDERLINED.

failure was not investigated further. The other part failed marginally and was back within specification when bench tested. This indicated that the failure mechanism was probably surface related and no further investigation was performed on this single isolated failure.

8.0 LM111 FAILURE ANALYSIS REPORT

8.1 V_{IO} FAILURE DUE TO DEGRADED Q4

During step-stress and life test, 93 Manufacturer D parts and 6 Manufacturer B parts failed due to excessive V_{IO}. These parts failed combinations of the first four specified V_{IO} parametric tests and the failed values ranged from +5.01 mV to +11.02 mV. The parts would recover when baked which indicated that the failures were caused by a surface instability mechanism.

Analysis of these parts established that the excessive V_{IO} was caused by a gain mismatch in the NPN input transistors, Q3 and Q4. In each part examined, h_{FE} of Q4 was lower than that of Q3 as illustrated in Table F8-1. When baked (100 hours at 250°C), h_{FE} of Q4 improved two to three-fold as also illustrated in Table F8-1. The bake also caused a slight decrease in h_{FE} of Q3 but this is apparently due to a separate annealing effect since h_{FE} of both transistors of a unstressed control part decreased when baked as shown in Table F8-1.

The reversible gain decrease displayed by Q4 indicates that the degradation probably was caused by depletion or inversion of the p-type base region due to the accumulation of a net positive charge in or on the passivation over the base. The collector-base junction of Q4 was reverse biased during life test, consequently the accumulation was the result of charge separation in the fringing field of the reverse biased junction.

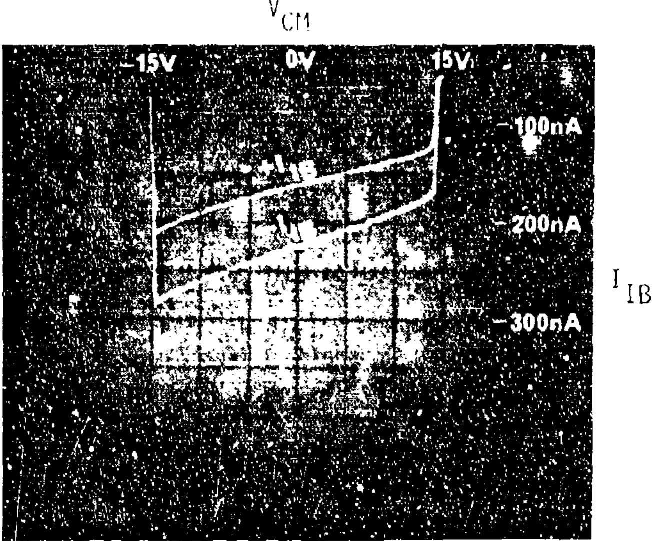
TABLE F8-1 - EXAMPLE OF THE RESULTS FROM DIE LEVEL PROBING OF REPRESENTATIVE V_{IO} FAILURES

MANUF	CELL TEMP	S/N	TIME OF FAILURE	TRANSISTOR	h_{FE} @ I_C = 29 mA, V_{CE} = 15V: @t_F	h_{FE} @ I_C = 29 mA, V_{CE} = 15V: POST BAKE
D	250°C	62	1,000 HRS	Q3	210	180
				Q4	43	104
D	200°C	135	1,000 HRS	Q3	174	145
				Q4	32	101
D	CONTROL (REFERENCE)	15	(UNSTRESSED)	Q3	207	174
				Q4	235	154

8.2 I_{IO} FAILURE DUE TO SURFACE AND BULK MECHANISMS

During step-stress and life test, 64 Manufacturer B parts and 5 Manufacturer D parts failed due to excessive I_{IO}. Of these 69 parts, 61 failed I_{IO}[11]. Seven parts failed I_{IO}[9] and one part failed I_{IO}[8]. I_{IO}[11] is the raised input offset current, $I_{IO(R)}$, which is the difference of the input bias currents, $-I_{IB(R)}$ and $+I_{IB(R)}$, measured at $\pm V = \pm 15V$ and $V_{CM} = 0V$ and with BAL/STB and BAL connected to +V. $I_{IO(R)}$ has specified limits of -25 nA MIN and +25 nA MAX. In 56 parts $I_{IO(R)}$ was positive, because the inverting input bias current, $-I_{IB(R)}$, was greater than the noninverting input bias current, $+I_{IB(R)}$, as illustrated in Figure F8-1. The failed values ranged from +25 nA to +151 nA. In five parts $I_{IO(R)}$ was negative, because $+I_{IB(R)}$ was greater than $-I_{IB(R)}$, and the failed values ranged from -26 nA to -30 nA.

Analysis of parts with positive excessive $I_{IO(R)}$ established that the failures were caused by a gain mismatch in the PNP input transistors. The input bias currents are the base currents of the PNP input transistors Q1 and Q2. $+I_{IB}$ is the quotient of h_{FE} of Q1, the noninverting input transistor, and I_C of Q1 ($+I_{IB} = I_{C1}/h_{FE}$). Likewise, $-I_{IB}$ is the quotient of h_{FE} of Q2, the inverting input transistor, and I_C of Q2 ($-I_{IB} = I_{C2}/h_{FE}$). Die level probing of representative failures established that the collector currents of Q1 and Q2 were equal, but that h_{FE} of Q2 was lower than h_{FE} of Q1, as shown in Table F8-2, which is why $-I_{IB(R)}$ was greater than $+I_{IB(R)}$. To determine what change took place during life test, the test data was examined. $+I_{IB(R)}$ and $-I_{IB(R)}$ were not measured during the tests (they are not specified parameters), but $+I_{IB}$[12] and $-I_{IB}$[12] were measured. $+I_{IB}$[12] and $-I_{IB}$[12] are the input bias currents at $\pm V = \pm 15V$ and V_{CM} = 0 volts with BAL and BAL/STB open (dc wise). As shown in Table F8-3, the values of $+I_{IB}$[12] and $-I_{IB}$[12] of the representative failure before and after accelerated life indicate that the gain of both transistors decreased during life, but that h_{FE} OF Q2 decreased more than did h_{FE} of Q1.



S/N 265 (500 HRS @ 225°C)

FIGURE F8-1 - $+I_{IB}$ AND $-I_{IB}$ (RAISED) VS. COMMON MODE VOLTAGE OF A PART WITH EXCESSIVE $I_{IO(R)}$

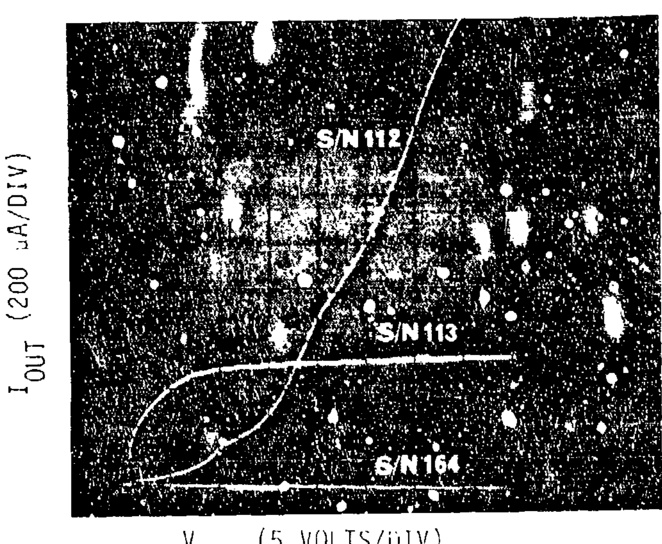


FIGURE F8-2 - I-V CHARACTERISTIC FROM OUTPUT (+ ON PIN 7) TO SUBSTRATE (- ON PIN 4) OF THE THREE PARTS WHICH HAD FAILED I_O

TABLE F8-2 - RESULTS OF DIE LEVEL PROBING OF Q1 AND Q2 OF REPRESENTATIVE $I_{IO(R)}$ FAILURES

MANUF	CELL TEMP	S/N	TIME OF FAILURE	TIME OF REMOVAL FROM LIFE TEST	$I_{IO(R)}$*	$-I_{IB(R)}$*	$+I_{IB(R)}$*	h_{FE} @ I_C = 20μA & V_{CE} = 5V Q1	Q2	$+I_{IB(R)}/-I_{IB(R)}$	Q2 h_{FE}/Q1 h_{FE}
B	200°C	155	1,000 HR	1,000 HR	+80 nA	-260 nA	-180 nA	250	182	.69	.73
B	225°C	211	256 HR	1,000 HR	+100 nA	-310 nA	-210 nA	238	168	.68	.71
B	250°C	52	500 HR	1,000 HR	+65 nA	-250 nA	-185 nA	286	213	.74	.74
B	UNSTRESSED	231	-	-	+12 nA	-192 nA	-180 nA	260	260	.94	1.00
D	250°C	42	500 HR	500 HR	+40 nA	-190 nA	-150 nA	370	278	.79	.75

*CURVE TRACER TEST DATA AT TIME OF REMOVAL

TABLE F8-3 - $\pm I_{IB}$ (V_{CM} = 0V) HISTORY OF THE REPRESENTATIVE $I_{IO(R)}$ FAILURES

MANUF	S/N	PARAMETERS	PARAMETER VALUES (nA) INITIAL	TIME OF REMOVAL
B	155	$+I_{IB}$[12]	-59	-67
		$-I_{IB}$[12]	-60	-75
B	211	$+I_{IB}$[12]	-71	-77
		$-I_{IB}$[12]	-73	-96
B	52	$+I_{IB}$[12]	-63	-73
		$-I_{IB}$[12]	-65	-80
D	42	$+I_{IB}$[12]	-38	-41
		$-I_{IB}$[12]	-38	-45

Sample failed parts were baked (some after delidding and removing the glassivation) for about 80 hours at the test cell temperature. In each part, $I_{IO(R)}$ recovered as shown in Table F8-4. In the 200°C failures, $-I_{IB(R)}$ decreased after baking which indicated that h_{FE} of Q2 improved (increased) upon baking. However, in the 225°C and 250°C failures, $-I_{IB(R)}$ and $+I_{IB(R)}$ usually increased after baking which indicated that h_{FE} of Q1 and Q2 further decreased upon baking. The decrease in h_{FE} of Q1 was greater than that of Q2; consequently, $I_{IO(R)}$ was within specification after baking. These findings indicated that the I_{IO} failures were caused by two degradation mechanisms, a surface related (reversible) mechanism predominant at 200°C and a bulk related (nonreversible) mechanism which predominated at the higher temperatures. The surface related mechanism probably was similar to that responsible for the V_{IO} type failures described in Section 8.1. The cause of the bulk mechanism was not established. Electrical evaluations of the p-n junctions of degraded transistors disclosed no abnormal characteristics and optical examinations of the transistors disclosed no visible anomaly which could account for the gain degradation.

8.3 I_{IB} FAILURE DUE TO AMPLIFIER SATURATION (MANUFACTURER B ONLY)

During step-stress two parts failed due to excessive $+I_{IB}$[13]. In each case $+I_{IB}$[13] was positive (+32 nA and +107 nA); normally $+I_{IB}$ is negative. $+I_{IB}$[13] is the noninverting input bias current at a common mode voltage of -14.5V and supply voltages of ±15V. Examination of the input bias currents of these parts on the curve tracer disclosed that as the common mode voltage approached the specified values of -14.5V and +13V, $+I_{IB}$ decreased sharply toward positive values due to saturation of the amplifier. This effect is illustrated in Figure 13 of the main report. Repeated retests of the two failed parts and other sample parts on the test set disclosed that all parts would intermittently pass and fail $+I_{IB}$. This indicated that the device could not operate consistently at the specified common mode voltages; i.e., the specified common mode voltages were too close to the supply voltages. Consequently, the common mode voltages were reduced to -13.5V and +12V. Subsequent to this change no further $+I_{IB}$ failures of this type were encountered during step-stress and accelerated life.

TABLE F8-4 - RESULTS OF BAKE OF REPRESENTATIVE $I_{IO(R)}$ FAILURES

CELL TEMP	S/N	TIME OF FAILURE	PARAMETER	VALUE PRIOR TO BAKE (nA)	VALUE AFTER BAKE (nA)	DIRECTION OF CHANGE IN h_{FE} of Q1 or Q2
250°C	114	1,000 HRS	$+I_{IB(R)}$	-220	-300	DECREASE
			$-I_{IB(R)}$	-246	-285	DECREASE
			$I_{IO(R)}$	26	-15	
	102	1,000 HRS	$+I_{IB(R)}$	-240	-242	NONE
			$-I_{IB(R)}$	-287	-235	INCREASE
			$I_{IO(R)}$	47	7	
	84	500 HRS	$+I_{IB(R)}$	-149	-176	DECREASE
			$-I_{IB(R)}$	-183	-193	DECREASE
			$I_{IO(R)}$	34	17	
	92*	4 HRS	$+I_{IB(R)}$	-161	-218	DECREASE
			$-I_{IB(R)}$	-187	-218	DECREASE
			$I_{IO(R)}$	26	0	
225°C	242	1,000 HRS	$+I_{IB(R)}$	-136	-200	DECREASE
			$-I_{IB(R)}$	-176	-200	DECREASE
			$I_{IO(R)}$	40	0	
	223	1,000 HRS	$+I_{IB(R)}$	-128	-205	DECREASE
			$-I_{IB(R)}$	-180	-205	DECREASE
			$I_{IO(R)}$	52	0	
	192	64 HRS	$+I_{IB(R)}$	-128	-200	DECREASE
			$-I_{IB(R)}$	-168	-210	DECREASE
			$I_{IO(R)}$	40	10	
200°C	142	1,000 HRS	$+I_{IB(R)}$	-188	-174	INCREASE
			$-I_{IB(R)}$	-220	-186	INCREASE
			$I_{IO(R)}$	32	12	
	144*	1,000 HR	$+I_{IB(R)}$	-192	-190	NONE
			$-I_{IB(R)}$	-222	-192	INCREASE
			$I_{IO(R)}$	30	2	
	143	500 HRS	$+I_{IB(R)}$	-222	-224	NONE
			$-I_{IB(R)}$	-257	-226	INCREASE
			$I_{IO(R)}$	30	2	

* BAKED WITH THE LID REMOVED AND THE GLASSIVATION STRIPPED

NOTES:

1. ALL PARTS WERE BAKED AT THE CELL TEMPERATURE FOR 80 HOURS.
2. PARAMETER VALUES WERE MEASURED ON A 577 CURVE TRACER.

8.4 I_0 FAILURE DUE TO DEGRADED Q15 (MANUFACTURER B ONLY)

During accelerated life, three Manufacturer B parts failed due to excessive I_0[16] which is the output leakage current with 32V applied to the collector of Q15. The failed values ranged from 0.589 to 60.1 microamperes. Examination of the parts on the curve tracer disclosed a channeled charactersitic between pin 7 (output) and pin 4 (-V) in one device, a quasi-exponential characteristic in one device, and no leakage in one device (I_0 had recovered) as shown in Figure F8-2. The leakage was traced to the collector-to-substrate diode (isolation junction) of the NPN output transistor Q15. The leakage dropped to zero when the parts were baked indicating that the degradation was caused by a surface related mechanism, probably inversion of the n-type collector tub of Q15. During life test the collector-substrate junction of Q15 was reverse biased (the output was high); consequently, the inversion probably was the result of charge separation in the fringing field of the reverse biased junction.

9.0 REFERENCES

[1] J. M. Patterson, " A Technique to Locate Leakage Current on Semiconductor Devices," Proceedings of Advanced Techniques in Failure Analysis, September 1977, pages 90-93.

[2] J. R. Haberer and J. J. Bart, "Charge Induced Instabilities in 709 Operational Amplifiers," 10th Annual Proceedings, Reliability Physics 1972, pages 106-111.

APPENDIX G

INITIAL JAN QUALIFIED DEVICE FAILURES

APPENDIX G
JAN QUALIFIED DEVICE FAILURES

Upon receipt at MDAC-St. Louis, all devices were subjected to external visual examinations, hermeticity test, and electrical test. During these tests, five of Manufacturer D's MIL-M-38510/10201 JAN qualified devices were found to be defective. Two devices were rejected during the visual inspection test. Shown in Figure G1 is a device which has been physically damaged and in Figure G2 a device is shown with a cavity in the package base. During the fine leak hermeticity tests one device failed with a leak rate of 2.0×10^{-6} atm cc/sec. Initial data taken at 25°C, +125°C and -55°C is shown in Figure G3 for the two devices (S/N 301 and S/N 302) which did not meet the electrical specifications. No further data was taken on any of the five failed devices.

FIGURE G1. DAMAGED M38510/10201

FIGURE G2. CAVITY IN BASE OF M38510/10201

DEVICE P/N M38510/10201 TEST TIME 0 HRS

TEST CELL: 0 CELL TEMP 25 C

DATE 10/15/76 TESTED AT 25 C

S/N	VRLINE(1)	VRLINE(2)	VRLINE(3)	VRLOAD(4)	VRLOAD(5)	VRLOAD(6)	VREF	IOS	ISCD
	%	%	%	%	%	%	VDC	MADC	MADC
301 *	-0.020	-0.138	-0.015	-0.316*	0.000	0.005	7.132	58.719	2.660
302 *	-0.016	-0.104	-0.010	-0.246*	-0.003	0.005	7.242	57.126	2.453

DEVICE S/N M38510/10201 TEST TIME: 0 HRS

TEST CELL: 0 CELL TEMP. 25 C

DATE. 10/15/76 TESTED AT: 125 C

S/N	VRLINE(1)	VRLINE(2)	VRLINE(3)	VRLOAD(4)	VRLOAD(5)	VRLOAD(6)	VREF	IOS	ISCD
	%	%	%	%	%	%	VDC	MADC	MADC
301	-0.050	0.000N	0.000N	-0.380	0.000N	0.000N	7.154	0.000N	2.035
302	-0.018	0.000N	0.000N	-0.343	0.000N	0.000N	7.279	0.000N	1.810

DEVICE P/N M38510/10201 TEST TIME 0 HRS.

TEST CELL 0 CELL TEMP. 25 C.

DATE: 10/20/76 TESTED AT -55 C

S/N	VRLINE(1)	VRLINE(2)	VRLINE(3)	VRLOAD(4)	VRLOAD(5)	VRLOAD(6)	VREF	IOS	ISCD
	%	%	%	%	%	%	VDC	MADC	MADC
301	-0.018	0.000N	0.000N	-0.273	0.000N	0.000N	7.106	0.000N	3.356
302	-0.014	0.000N	0.000H	-0.186	0.000N	0.000N	7.201	0.000N	3.170

FIGURE G3. INITIAL ELECTRICAL DATA FOR MANUFACTURER D'S M38510/10201 FAILED DEVICES

MANUFACTURER CODE

MANUFACTURER	CODE
Precision Monolithics Inc.	A
National Semiconductor Corp.	B
Advanced Micro Devices	C
Fairchild Semiconductor Corp.	D

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