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BASELINE DESIGN ITEM 0002 OF MICROPROCESSOR-BASED POWER CONDITI--ETC(U)
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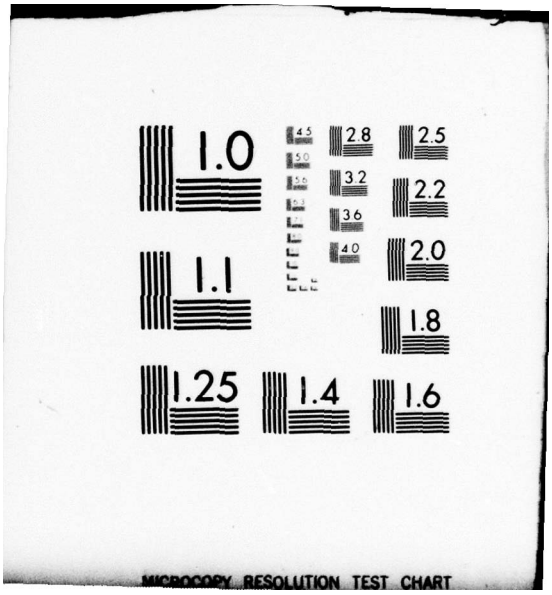
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MICROCOPY RESOLUTION TEST CHART

LEVEL II

(1) (B.S.)

(6) BASELINE DESIGN

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OF

MICROPROCESSOR-BASED POWER CONDITIONER CONTROLLER

CONTRACT NO. (15) DAAK70-78-C-0117

PREPARED FOR

U. S. ARMY MERADCOM

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1.0.0 SUMMARY

This report covers effort under contract DAAK70-78-C-0117 to develop the baseline design for a microprocessor based power conditioner controller.

From reviewing the controller functions listed in the previous monthly reports several design considerations evolved and a general block diagram of the controller was developed. The block diagram consisted of several modules surrounding a centrally located microprocessor and its interface. Design considerations for a particular module involved one or more approaches in the development of that module. In the latter case, the optimum approach was selected. The combination of these approaches form the baseline design. The modules were designed to interface to existing Delco SCR gate driver circuitry. All of the existing sense signals will remain intact. Additional conditioning of some existing sense signals may be required. The inverter output voltages will be sensed directly through precision attenuators.

The individual modules were designed to perform their functions with minimum control and supervision from the main microprocessor. This permits the main microprocessor to accept more tasks at a later date and spend more time monitoring the overall operation of the power conditioner via sense signals without the burden of generating complex timing signals.

The term "main microprocessor" is used to differentiate between the centralized microprocessor and any satellite microprocessors that may be implemented at a later date.

Considerations for the main microprocessor interface and a partial list of some of the microprocessor duties, along with software descriptions throughout the report were included at this time to facilitate a more accurate choice of an optimum microprocessor, the next task.

2.0.0 PREFACE

The work described in this report was performed by Yucca International, Inc. under the direction of the U. S. Army Mobility Equipment Research and Development Command. This report completes the second task of the first phase (CLIN0002, Phase 1) of the U. S. Army contact no. DAAK70-78-C-0117. The Contracting Officer's Representative is Dr. David Lee at the U. S. Army MERADCOM headquarters at Fort Belvoir, Virginia.

3.0.0 COPYRIGHT PERMISSION

The following documents served as information sources during the period reported.

Source No. 1

Contract No. DAAK70-78-C-0117 Microprocessor-Based Power Conditioner Controller	CLIN0001 Report	Sept. 1978

Source No. 2.

Contract No. DAAK70-77-C-0035 15 KW General Purpose Power Conditioner	Final Report AC-DC Section	April 1978

Source No. 3

Contract No. DAAK70-77-C-0157 15 KW General Purpose Power Conditioner	Prelim. Report Inverter	July 1978

Source No. 4

Delco Electronics
400 Hz Malor PCU Timing Diagram
Code Ident. No. 13160
(Supplied by MERADCOM during this reporting period)

4.0.0 INTRODUCTION

This is a report of the second task of six tasks of the U. S. Army contract no. DAAK70-78-C-0117. Performed during this task was the baseline design of a microprocessor-based controller to replace an existing controller in the Delco 15 KW power conditioner. The design was performed to a detailed block diagram level. The microprocessor to be used will be selected in the next task and following that will be the selection of individual components in the hardware.

Throughout the report, references will be made to the reports listed in Section 3.0.0. It will be assumed the reader has these available.

The report details controller operating concepts and considerations derived from a review of the required and desired controller functions listed in the previous report for Task 1. Next is a breakdown of the controller into functional modules and additional design considerations for each module. Following that are the approaches developed for each module using the design considerations. The baseline design is a combination of the selected approaches. Included in the investigation are plans for the selection of the optimum microprocessor, the next task.

5.0.0 INVESTIGATIONS

5.1.0 DESIGN CONSIDERATIONS

5.1.1 OVERALL

When the power conditioner is turned on, power to the controller is needed to reset all control signals to a state which will de-activate the power conditioner. The power conditioner will not be activated unless a self-test of the controller is executed properly. Following a succesful self-test, the controller will determine the required mode of operation by reading the front panel switch settings. The controller hardware is initialized for operation as programmed by the front panel settings. After verification of an operational converter, the inverter is activated. That circuitry used for self-test and initialization, but not used after operation begins will be protected to assure a change does not occur during operation. It may be enabled again by a reset. For instance, the output frequency cannot be changed unless an orderly converter and inverter de-activation sequence and reset occurs.

5.1.1.1 Power is applied to the load as follows. The controller, initially unaware of load requirements (up to 15 KW), must adjust the inverter output voltage to the desired level (120 VRMS, user adjustable -5%, +15%) in an algorithm which produces the least amount of overshoot and undershoot (less than 12% at rated load) in the least amount of time (less than 250 ms) and maintain that level at a specified regulation (1%). The required accuracy of the output is not specified. The baseline design will assume a value of 1%.

The correct voltage needed into the inverter to approximately produce the desired RMS voltage out of the inverter can be calculated by the controller using a "load profile" table (discussed in Section 6.0.0 of Source 1) stored in memory. The controller, after determining that the converter output voltage is not at a desired level, will measure the inverter input current. If a large voltage deviation from the previous level had occurred for an unknown reason, the cause can possibly be determined as illustrated in Figure 2. Assuming the change can be attributed to a change in load, the controller will calculate the magnitude of the new load from the two measured values. This load is the total power demand presented on the converter output by the losses in the inverter and the actual load. The inverter, which may be represented as a small impedance in series with the load, is assumed to vary slightly with inverter output load and frequency. Thus, the need for the "load profile" table, to compensate for these variables, which influence the relationship between converter output voltage and inverter output voltage. The converter operating frequency will be adjusted to reach the new level of converter output voltage obtained from the table. It is important to note that the table may be subject to a correction factor once operation begins, if the inverter output voltage is determined to have a slight error due to the individual differences between Delco 15 KW power conditioners.

5.1.1.2 Inverter output voltage regulation response time will be limited by the converter response time if the computer response time is ignored. The computer response time will be defined as the time between an output voltage change and the correction to the converter operating frequency and the resultant effect on the converter output voltage. When the operating frequency is changed, the resultant change in converter output voltage may require one or more operating cycles at the new frequency. At an operating frequency of 345 Hz (See Table 3 of first report) the period at this frequency would be approximately 2.90 ms. This would exceed the period of a 400 Hz output frequency which is 2.5 ms. Therefore, sub-cycle regulation (see requirement no. 5 of Section 5.2.0 of Source 1) may not be obtainable at the operating conditions just described.

5.1.1.3 It will be a design objective to make the computer response time small compared to the converter response time so that the total regulation response time can be defined as one or two cycles at the converter operating frequency. Therefore, if the converter operating frequency is higher than the inverter output frequency, sub-cycle regulation can be recognized.

To achieve this objective, an effort will be made to regulate the inverter output voltage initially by accurately measuring and regulating the converter output voltage. This will improve response time (for reasons discussed in Section 6.0.0 of Source 1) but the inverter output voltage may require further optimization by accurately measuring the inverter voltages directly. A detailed description of the method to be used to regulate the converter output voltage follows.

5.1.1.4 For the reasons described above, it will be desirable to do the following:

1) Monitor the converter output voltage often;
2) Properly condition the inverter input current sense signal to provide a DC voltage level proportional to the average current into the inverter so that it may be randomly measured.

The storage capacity of the converter output filter will influence the necessary interval between measurements to assure good regulation response to sudden applications and removal of loads. The storage capacity of the converter output filter, will minimize the effects caused by transient loads (see Section 5.1.4 of Source 1). This capacitance will affect the converter response time, which is arbitrarily determined to be one converter operating cycle. It will also supply increased current demands to the inverter input for a short period of time.

It is desireable to base the interval between converter output voltage measurements on the converter response time for reasons described below.

If, instead an arbitrary time, 500 μs for instance, is chosen to be the time interval between measurements, then at a converter operating frequency of 500 Hz, the converter output voltage would be measured four times (2 ms ÷ 500 μs = 4) in one operating cycle. This may be unnecessarily fast, depending on filter storage ability.

At a converter operating frequency of 9 KHz, which may be necessary in order to supply a 200% overload for 5 seconds, the voltage would be measured only once in every 4.5 (500 μs $\div \frac{1}{9\text{KHz}}$ = 4.5) operating cycles. If the 200% overload was removed immediately, then 4.5 operating cycles at that frequency driving an open load could cause the inverter output voltage to go excessively high.

5.1.1.6. It will be a design objective to allow the converter output voltage to be sampled every converter operating cycle if it is desired, even at 9 KHz (See Appendix A) which is the resonant frequency (upper limit) of the converter.

The period at 9 KHz is approximately 111 μs. During this time the controller must make a measurement and a decision based on that measurement, and on a long term basis, control other parts of the power conditioner.

5.1.1.7 From the required and desired controller functions of the previous report, Section 5.2.0 and 5.3.0 respectively, a basic block diagram shown in Figure 1 was constructed. It was intended as a starting place for the development of the design approaches.

A centrally located microprocessor, hereafter referred to as the main microprocessor, will serve to coordinate the activities of the various modules shown and thus perform a large variety of tasks. In an attempt to minimize the burden on the main microprocessor, low level tasks (such as SCR timing pulse generation) that can easily and economically be performed externally, will be restricted from the main microprocessor duties. The main microprocessor may in the final

phase of controller development reduce the external hardware by assuming low level tasks if microprocessor time is available.

5.1.1.8 The inverter and converter SCR gate driver circuitry and sense signal conditioning circuitry used by the existing controller will be used by the new controller if performance is not limited.

5.1.1.9 It is expected that the main microprocessor will spend much of its time interfacing with the sense signal data acquisition circuitry. Therefore, design efforts will be directed to minimize the number of microprocessor instruction cycles necessary to perform a measurement of a given sense signal.

The controller will be required to operate in the electromagnetic operating environment of the controller.

5.1.2 CONVERTER SCR TIMING CONSIDERATIONS

This module, shown in Figure 1, in combination with the main microprocessor, will maintain the converter output voltage at a desired level by adjusting the repetition rate of 12 SCR timing signals applied to the converter.

5.1.2.1 Figure 4 is a general block diagram of the necessary converter SCR timing circuitry. An oscillator (which might be a VCO or phase lock loop) will supply gate logic circuitry with pulses at a repetition rate which is adjustable by the main microprocessor.

5.1.2.2 The gate logic will limit the pulse width of the incoming pulses to 12 μs. The pulses are then sequentially distributed to the 6 inverted output lines. Each output line becomes two lines that interface to the Delco converter gate driver card CCAA3 on pages 6-13 and 6-14 of Source no. 2.

5.1.2.3 The frequency out of the oscillator will be six times that of the converter operating frequency, the frequency of pulses applied to the same pair of converter SCR's. Six pulses out of the oscillator is one complete revolution of the SCR firing sequence. Appendix A indicates that the resonant frequency of the three DC to DC resonant converters is 9 KHz. The oscillator maximum frequency capability will be at least 6 X 9 KHz. The minimum frequency capability of the oscillator does not necessarily need to be zero. The minimum frequency should be below that frequency which will not provide enough converter output voltage to properly fire the inverter SCR's with the inverter output unloaded.

5.1.2.4 Contained in Section 5.1.5, are considerations for the converter SCR commutation sense signals. The converter SCR timing module will be designed to verify that correct commutation signals are received from the commutation sense circuits. A positive or negative voltage at the output of a sense circuit (one per converter) will indicate which pair of SCR's in that converter were just commutated off.

If the commutation sense signal is not received, (indicating the SCR's just fired did not naturally commutate off) the opposite pair of SCR's in that converter must not be fired until after a significant delay period. This delay period is necessary to prevent a short circuit across the DC input bus caused by SCR's in opposite pairs being on at the same time. The delay period used in the existing controller is 22 ms (from page 6-2 of Source no. 2).

5.1.2.5 The existing controller disables all three converters if a commutation failure in one converter occurs. At full loads, this may be necessary, but at light loads, possibly two converters could supply the inverter while the third is temporarily disabled. It is important to note that the converters are designed to supply 200% of rated load for 5 seconds so perhaps two could supply 100% of rated load for the length of time that the third is disabled (22 ms).

5.1.3 INVERTER SCR TIMING CONSIDERATIONS

This module will generate the necessary timing signals to construct three phases of sine waves at the inverter outputs. Figure 5, a basic block diagram of the required circuitry, indicates that 3 clocks necessary for the waveform generation timing circuitry will be derived by dividing down from a crystal oscillator (chosen for a low temperature coefficient and frequency accuracy).

5.1.3.1 The 28 output lines, labeled at the right, connect to the existing Delco inverter SCR gate driver circuitry shown on pages 90-92 of Source no. 3. An inverter SCR is fired when one of the outputs goes low. Delco requires that the signal remain low for 12 μs, nominal. The design must not send glitches or spurious data to the Delco SCR gate drivers.

5.1.3.2 The Delco inverter SCR gate driver circuitry may be disabled by making the disable line shown in Figure 5 go high. A similar feature may be designed into the waveform generation timing circuitry module.

5.1.3.3 Source 4 is a 28 SCR Delco inverter timing chart. The signal "CLK" operates at a frequency that is 81 times the frequency of the output sine wave. The signals "CLKDP" and "$\overline{\text{CLKP}}$" go true for 12 μs each time "CLK" makes a positive transition or a negative transisiton respectively. Therefore, "CLKDP" and "$\overline{\text{CLKP}}$" can be used to fire SCR's on both transitions of "CLK." Within a 360° period of the output sine wave, 162 timing divisions occur. Each division starts and ends with a transition of "CLK." At the beginning of each division a 12 μs

pulse (independent of output frequency) occurs, which will fire none or many SCR's depending on the position of the division in the 360^{o} timing pattern.

The lines at the bottom of the diagram indicate the length of time in divisions that the corresponding SCR is on. An SCR is turned off by firing the next SCR in the required sequence.

From the diagram it can be determined that the step times in the output waveform are each 4 divisions or 8.8889 degrees. The center pulse width time is 42 divisions or 93.3333 degrees. (This conflicts with Source no. 3 pages 10 and 11 which state that the step time (9^{o}) is a sub-multiple of the center pulse width (99^{o}). See Section 6.0.0 for further information.)

5.1.3.4 During the development of the inverter, Delco has found it necessary to change the timing occasionally. Therefore, ease of implementing a timing modification at a later date will be a design consideration. A method of quickly changing the timing pattern delivered by the timing circuitry would be to change the contents of an ultraviolet erasable programmable read only memory (EPROM). The EPROM may be substituted with ROM when the controller is released from engineering development.

5.1.3.5 Pages 10 and 11 of Source no. 3 noted the advantages of different time durations of each step in the sine wave stair-step, but due to the complexities of designing and building the logic, equal step times were settled for. The center

pulse time was made a multiple of the step time for the same reason (Source no. 3, page 10). Therefore, timing signal resolution will be a design consideration. Increased resolution will permit a finer adjustment of the timing signals, which will remove the constraint of equal step times and permit a slight delay or advance of any SCR timing pulse. A timing resolution of 1/2 degree or less will be considered.

5.1.3.6 From the progress report of October 1 to November 1, 1977, for contract no DAAK70-77-C-0157, the following statement was made on page 2 under the subtitle BASELINE WAVEFORM. "The timing given is in terms of a 400 Hertz waveform but the timing sequences provided can be directly scaled to 60 Hertz."

This has been interpreted to mean that the same timing pattern used for 400 Hz can be used for 60 Hz and possibly 50 Hz.

5.1.4 SENSE SIGNAL CONDITIONING CONSIDERATIONS

Figure 7 shows the circuitry used to condition the power conditioners sense signals for use by the existing controller. All 17 sense signals except the converter output voltage sense are isolated through a transformer and rectified. The converter output voltage sense is attenuated by a resistor divider.

5.1.4.1 The power conditioner input voltage sense signals, ϕA, ϕB, and ϕC are configured to sense the line to line voltages of the 3 input phases. If a phase were missing or low, the error would be indicated on two sense signals instead of one. For instance, if phase A were missing, the ϕA input voltage sense and ϕC input voltage sense signals would each drop to half the normal voltage. Because of the method of sensing the input voltages and the Delta configuration connection of the AC input to the three DC to DC converters (see page 25 of Source no. 1). The power conditioner cannot be expected to function with one input phase missing, because two of the DC to DC converters would receive only half of the normal input voltage. The controller will monitor the low quality three phase AC inputs to protect the inverter and the load against input overvoltage, undervoltage, and lost phase. (The power conditioner input in its present configuration cannot be protected against input overvoltage with the controller.) Sense signals that would provide a DC voltage proportional to the RMS voltages, would be satisfactory for measurement by an analog to digital converter in the sense signal data acquisition circuitry.

5.1.4.2 The converter SCR commutation sense signals are diode clamped. These signals are intended to indicate the time duration of current flow through anti-parallel diodes across the SCR's in the converter. An important parameter of this signal

besides pulse width, is the voltage polarity, which will identify the SCR pair being turned off. Circuitry in the controller must detect if the sense signal pulse widths are longer than 15.5 μs which is the required minimum. (Delco suggests 16 μs on page 7-4 of Source no. 2 but requires only 15.5 μs in the existing controller circuitry.)

5.1.4.3 The inverter output current sense signals can facilitate a measurement of current to the actual load if it is desired, but at the present time, no use, other than for trouble shooting and diagnostics, can be determined for these signals. Current limiting of the inverter output can be performed by sensing and limiting the inverter input current.

5.1.4.4 The inverter input current sense signal will be used for determining total power demand on the converter output as described in Section 5.1.1.3.

5.1.4.5 The converter output voltage sense signal is also described in Section 5.1.1.3. The nominal voltage out of the converter to produce 120 VRMS at the inverter output is expected to be ± 140 VDC. (Section 5.1.4 of Source no. 1). The positive and negative voltages are with reference to the inverter output neutral wire. Since there is no means of controlling the two voltages to have the same absolute value, and because the circuit design practically assures that the voltages will be approximately equal, only the positive voltage will be measured for voltage regulation purposes. The negative voltage can be measured for comparison purposes, however. The converter output voltage will be randomly sampled with respect to the inverter output frequency. It is possible that an unknown amount of ripple and noise on the converter output voltage may cause

erroneous measurements. If ripple is excessive, a small amount of filtering of the converter sense signal may be required.

5.1.4.6 The converter output current sense signals can be useful for verifying that each converter is supporting its share of the load. If a failure in a converter is suspected but cannot be verified with any of the other sense signals then measurements can be compared to identify the failing converter. Because no correction method exists for equalizing the currents, then routine sampling of these signals cannot be justified.

5.1.4.7 The inverter output voltage sense signals will be conditioned to allow the voltage to be measured with better than 1% accuracy. The inverter output voltage is specified in RMS. Therefore, either a true RMS or an RMS measuring method can be implemented. Unfortunately, this method would provide no check on distortion and several cycles may be required before the averaging circuit would accurately indicate a change in output voltage.

An alternate method would be to take samples of the output sine wave at known points in time with reference to zero crossing. The samples would be compared to a sine table to detect distortion or incorrect amplitude on the positive half and negative half of the sine wave.

If the sampling method described above is used, then isolation by a transformer and rectification performed by the existing sense signals is undesired. With rectification, the negative half of the sine wave will be difficult to identify and the diode drop will introduce a variable error in the sense signal voltage.

If the same calibrated measurement system is to measure all three sense signals, then transformer isolation can introduce individual errors that cannot be removed. Isolation of the sense signals are desirable. This may be obtained by using a differential input analog multiplexer to connect a sense signal for measurement and to disconnect it when another sense signal is being measured.

5.1.5 SENSE SIGNAL DATA ACQUISITION CONSIDERATIONS

Interfacing the power conditioner voltage and current sense signals (not the commutation sense signals) to the main microprocessor will require the following:

1) Analog to digital conversion;
2) Analog multiplexer. A multiplexer is an economical alternative to having a separate A/D for each sense signal;
3) Sample and hold. This assures that the voltage being measured will not change during conversion.

5.1.5.1 There are presently 17 sense signals in the power conditioner. Three of these are commutation sense signals which will be monitored by the converter SCR timing circuitry.

5.1.5.2 The converter output current sense signals will not be monitored on a regular basis (see Section 5.1.4). It may be necessary to measure these sense signals during self-test or for diagnostic purposes. The accuracy needed will be 10% or better.

5.1.5.3 The remaining 11 signals will be measured on a routine basis. The sense signals directly involved in voltage regulation and current limiting will require more frequent monitoring and better accuracy than the others.

5.1.5.4 The following items will be considered:

1) The number of sense signals to be measured;
2) The minimum number of A/D converters and multiplexers to arrive at a cost and performance effective design;

3) The speed of multiplexing, sampling, holding and converting devices available on the market today. Also, the accuracy and resolution from A/D converters presently available;

4) The measurement accuracy required of inverter output voltage sense signals. These are expected to impose the strictest accuracy requirements of all the sense signals. Other sense signal measurements will ben. it because they may use the same A/D;

5) The design objective set in Section 5.1.1.6;

6) Minimize the number of control signals necessary to measure a sense signal.

5.1.6 FRONT PANEL AND ADDITIONAL SENSING CONSIDERATIONS

A front panel display will be used to indicate messages to the user. It will probably be a multi-character 7 segment display with blanking capability. The following front panel switch settings will be sensed by the controller.

1) Output frequency selection;

2) Output voltage adjust.

The temperature at undetermined points in the power conditioner will be sensed by the controller.

The revolution speed of the fan blades in the power conditioner will probably be detected photo electrically.

Design of the above modules will be deferred until after the microprocessor selection and additional specific information becomes available.

5.2.1 CONVERTER SCR TIMING CIRCUITRY DESIGN APPROACHES

Two approaches were developed for this module from the applicable requirements outlined in the first task and the converter timing circuitry design considerations of Section 5.1.2. Both approaches use the same gate logic circuitry of Figure 4, they differ only in the oscillator section. Method one uses a DAC and a VCO combination to form a programmable oscillator. Method two uses a frequency synthesizer which contains a counter and a phase-locked loop.

The converter SCR gate logic block used in the two approaches is shown in Figure 10 with the inputs and outputs detailed.

The gate logic block is intended to do the following:

1) Remove from the main microprocessor's duties the task of verifying that each commutation sense signal was received correctly;
2) Interrupt the main microprocessor if a commutation fail occurs;
3) Allow information concerning the failing converter and SCR pair to be read by the main microprocessor;
4) Permit the microprocessor to selectively disable a converter without affecting the two remaining operational converters; or, permit all three converters to be disabled together.

The incoming oscillator pulse widths are changed to 12 μs. Each pulse will be delivered to one of the six outputs in a sequential order unless a valid commutation pulse is not detected for an SCR pair just fired. Although two converters would continue to receive their pulses at the normal times, the converter with the failing SCR pair will continue to get pulses delivered to the failing SCR pair instead of the opposite SCR pair. If a valid commutation sense is received, then the opposite pair of SCR's will be permitted to fire. The circuitry will inform the main microprocessor of the commutation failure, when it detects that two consecutive pulses to a DC to DC converter went to the same pair of SCR's. The circuitry will also permit the failing pair of SCR's to be identified by the main microprocessor. The main microprocessor will have three options. It may allow the gate logic circuitry to continue sending pulses to the failing pair of SCR's, by taking

no action. It may disable the failing DC to DC converter for a Delco recommended period of 22 ms, or it may disable all three phases for 22 ms to duplicate the existing controller action. (Duplication is not exact, because the existing controller does not permit another pair of SCR's to be fired again for 22 ms if a valid commutation pulse is not received.)

After examining the circuitry of the Delco 4 SCR resonant converter, it was decided by Yucca that no apparent harm would be caused by firing the failing pair of SCR's again at least once. This will simultaneously inform the main microprocessor of a failure and give the converter one more chance.

Figure 12 is a portion of the Delco Converter Gate Control Schematic on page 6-10 of Source no. 2.

Zero volts from one of the three sense circuits will cause both of the corresponding comparator outputs to be high. A positive voltage or a negative voltage (not exceeding +1.4V or -1.4V respectively) will cause one or the other of the two comparator outputs to go low. The comparator outputs are designed to interface to a C-MOS CD4093B, a quad 2 input NAND gate with Schmitt trigger inputs.

The connection of the Delco circuitry of Figure 12 to the converter SCR gate logic is shown in Figure 10. The comparator outputs are designated according to the pair of SCR's that are being turned off (reverse biased) when the comparator output is low.

The Delco circuitry of Figure 12 may be replaced at a later date with circuitry that will perform the equivalent function.

Figure 11 and Figure 13 show detailed circuitry that perform the functions that have been described. The circuitry shown in Figure 13 is preliminary and was included only to demonstrate a concept.

Converter oscillator Approach #1 is shown in Figure 14. It uses a 10 bit digital to analog converter and a voltage controlled oscillator. A particular DAC and a particular VCO will be selected at a later date. The VCO will be chosen for its linearity, temperature stability (less than 25 ppm), and wide sweep range (1000:1). The minimum frequency will be greater than 54 KHz.

The 10 bit DAC must function properly with the VCO and will be selected on that basis. It may be desirable to choose a DAC which will use an externally supplied reference.

Not shown in the diagram of this approach is a frequency counter that will be used during self-test to calibrate the oscillator and store in RAM memory a digital input vs. frequency output profile prior to power conditioner activation.

A table located in ROM will contain the converter operating frequency vs. converter power output curve. With the information available from the above table and profile, the controller can quickly correct for changes in the load after determining the new load requirements.

During a commutation failure delay period, when one of the three converters is temporarily disabled, the table described above will not be valid.

Converter oscillator approach #2 is shown in Figure 15. It shows an approach using a 16 bit presetable binary down counter and a phase lock loop integrated circuit. This, in combination with a 16 bit latch and a reference frequency will form a programmable frequency synthesizer. The circuit may be designed to allow the main microprocessor to store in the latch a binary representation of the converter operating frequency it desires. Thus, eliminating the need for a digital input vs. frequency output profile.

The counter will count to zero and preset the counter with the contents of the latch and begin counting again. The frequency out of the phase lock loop determines the counting rate. The phase lock loop will adjust the output frequency so that the input frequency will equal the reference frequency. When the counter reaches zero a pulse will be delivered to the PLL frequency input. Therefore, the time it takes for the counter to count from its preset value to zero will be made equal to the period of the reference frequency.

A disadvantage of this approach, is slow response time. It may take up to two periods at the reference frequency between the time the main microprocessor writes a new frequency value to the latch and the time the phase lock loop begins correcting the PLL output frequency.

If the reference frequency is low the reponse time can be significant.

A limit is placed on the maximum reference frequency by the highest binary value that will be loaded into the counter and the upper frequency limitations of the phase lock loop output. Additional factors such as frequency capture range, frequency lock range, and accidental lock on harmonics can make this approach difficult to use in this application.

5.2.2 INVERTER SCR TIMING CIRCUITRY DESIGN APPROACHES

Two approaches were developed for this module. The first approach to be described is intended to do the following:

1) Remove the constraint of equal step times in the sine wave (which can possibly reduce the total harmonic distortion out of the inverter) by offering a timing resoultion of 1/2 degree. (If necessary, a 1/4 degree resolution can be provided.)
2) Provide an easy way to change timing;
3) By incorporating a simple change, 400 Hz timing can be separated from 50 Hz and 60 Hz timing;
4) Permit the timing pattern to be verified before activating the inverter. (To prevent against open sockets, incorrect PROM installation, unauthorized PROMS, etc.)
5) The PROM device may at a later date be substituted pin for pin with a RAM device, with some additional circuitry and software the microprocessor can change timing during inverter operation to correct for detected perturbations. Although the possibility of needing this feature is very remote at this time, it is an added feature.

The first approach due to item number 1 cannot duplicate Delco step times exactly.

The second approach will perform items 2, 3, and 4 above and exactly duplicate the timing that Delco is presently using.

Figure 17 shows the required 28 SCR output signals at the extreme right of the diagram. When the 32 bit latch is tri-stated the outputs will float. Pull-up resistors can be used to assure a TTL logic "1" for the existing Delco inverter SCR gate driver circuitry. This will prevent an inverter SCR from firing since a TTL logic "0" is required to cause a 288 KHz frequency in the gate driver to fire an SCR. Data in the 1K address X 32 bit EPROM (actually four 1K X 8 bit EPROMS) will normally be "1's" unless it is desirable to fire an SCR which requires that the corresponding data bit contain a "0" in *either one or a number of* consecutive address locations (for reasons presented later). Note that the inverter cannot be activated unless the 32 bit latch is enabled, which will occur shortly after self-test and converter activation.

The EPROM address will be decremented once every 1/2 degree of the 360 degree output sine wave. This requires 720 addresses of the available 1024 addresses to contain the timing pattern.

The starting address and ending address of the timing pattern in the EPROM will be determined by the count direction and method of loading the 12 bit binary counter that generates the EPROM address.

The counter will count down from an initial count loaded from a switch setting of 10 dip switches. Loading and decrementing is performed in the counter on the positive transition of the clock. Note that although the addresses to the PROM's become valid shortly after the positive clock transition, the data contained in that location is not delivered to the inverter until the falling edge of the clock. This allows enough time for EPROM data to become valid after a stable memory address. (Access time for a 2708 EPROM is .450 μs max; @ 400 Hz output a half cycle of the clock will be 2.5 ms ÷ 360 ÷ 2 ÷ 2 = 1.74 μs) The counter continues to decrement until a count of zero is reached. The next state of the counter will be the switch setting count, effected by the $\overline{\text{carry}}$ signal going low causing $\overline{\text{load}}$ to go low. The load will be syncronous with the clock pulse resulting in a smooth transition of the counter from address 0 the address that was loaded. Counting backwards through the EPROM requires that the timing sequence in the EPROM be backwards. The starting address (arbitrarily corresponding to 0 degrees in the timing pattern) is loc. 719 decimal or loc. 2CF hexadecimal. The ending address is loc. 0. EPROM locations 2D0H through 3FFH are unassigned and will contain all "1's" as data.

A 4 line to 1 line multiplexer is selected to channel, the clock rate necessary for a desired inverter output frequency (50 Hz, 60 Hz, or 400 Hz), to the counter. During self-test, the main microprocessor will select the multiplexer to channel the fourth input to the counter. This multiplexer input line, labeled, external clock, will be pulsed twice by the main microprocessor to to decrement the counter. This feature will be used to read the entire EPROM contents during self-test.

Separate 400 Hz timing and 50 Hz/60 Hz timing can be facilitated by changing the 1K X 32 bit EPROM to a 2K X 32 bit EPROM. The 50/60 Hz timing can occupy

the lower 1K of memory and 400 Hz timing can occupy the upper 1K. The most significant address line (A10) would be used to select between the two.

Delco currently fires an inverter SCR by applying an inverted 12 μs pulse to the corresponding input line of the gate driver.

To fire an SCR using the new approach, "0's" contained in memory will be used. Suppose one of the 32 bits in four consecutive memory location was programmed to "0."

The resulting inverted pulse duration would not be the same for 60 Hz as 400 Hz. Four consecutive memory locations would be a 2 degree interval of the output sine wave. At 400 Hz the pulse duration would be 2.5 ms ÷ 180 or 13.8 μs. At 60 Hz it would be 16.67 ms ÷ 180 = 92.6 μs.

If pulse durations, defined in number of degrees, instead of number of microseconds, is unsatisfactory, then two solutions to the problem exist.

One solution will require making separated timing mandatory. The other would require the need for a 12 μs one-shot inserted in each of the 28 output lines.

Figure 18 is a detailed block diagram of the second approach which duplicates Delco timing. The circuitry is very similar to that of the first approach. One major difference is that 162 clock pulses are applied to the 8 bit binary counter in one cycle of the output frequency.

Additional differences are:

1) Only 162 locations of the available 256 locations will be used;
2) Exact 12 μs SCR pulses, independent of output frequency can be obtained with the aid of a single monostable multivibrator;
3) A logic "0" in a ROM address location will deliver a 12 μs pulse to the Delco gate drive circuitry. Logic "0's" in consecutive locations are undesired because this will cause multiple 12 μs pulses to be delivered to the same gate driver.

A disadvantage of this approach is that 10^{0} and $1/4^{0}$ interval signals used by the data acquisition circuitry (described in Section 5.2.3) are not readily available, instead 2.222222^{0} interval signals are available.

5.2.3 SENSE SIGNAL DATA ACQUISTION APPROACH

The approach shown in Figure 19 is the only approach developed for this module.

Shown are two independent sub-modules. Each has its own A/D, sample and hold, multiplexer, and control circuitry.

Each multiplexer (mux) will select one of eight signals to be applied to the input of a sample and hold. Seven are used for sense signals and one is reserved for calibration purposes or for expansion using another multiplexer.

Listed beside each mux are the seven sense signals the mux will select.

Sub-module 2 at the top of Figure 19 will measure an analog voltage between 0 and +10V. Normally $\overline{\text{convert}}$ 2 will be high causing the sample and hold to follow (sample) the selected sense signal. Conversion into an unsigned 8 bit binary number will be initiated by $\overline{\text{convert}}$ 2 going low and remaining low until $\overline{\text{complete}}$ 2 goes low, which indicates to the main microprocessor that the conversion is complete. $\overline{\text{Convert}}$ 2 will be returned to a high level causing the result of the conversion to be latched in the 8 bit data latch. The microprocessor may then read the latch. The microprocessor after reading the data may not start another conversion until 25 μs has elapsed since $\overline{\text{convert}}$ 2 was returned high or the mux select was changed, which ever occurred last. This is necessary to allow the sample and hold to recover from the hold state (that it was in during conversion) and to begin sampling (following) the selected analog signal.

After reviewing specifications of components currently available on the market the above process can be performed in less than 60 μs. This does not include the time necessary to recognize a conversion complete signal and to respond by bringing $\overline{\text{convert}}$ 2 high, which will depend on the microprocessor instruction cycle time and the manner in which the $\overline{\text{complete}}$ 2 is detected.

Sub-module 1 at the bottom of Figure 19 will convert an analog voltage between -5V and +5V into a signed 10 bit binary number. The most significant bit (MSB) is used to indicate polarity and the remaining nine bits will represent magnitude. The control circuitry can be operated in a manner identical to that of sub-module 1 except that an extra microprocessor read will be required to read the two least significant bits (LSB) of the 10 bit binary value.

If the mode select line is brought low a different mode will be selected. This mode will be used when measuring the inverter output voltages. The following is description of this mode.

When it is desired to measure a selected inverter output voltage the $\overline{\text{convert 1}}$ will go low. Upon the next positive transition of the 10^{o} sync signal the following two things occur simultaneously:

1) The sample and hold enters the hold mode, to hold the analog value stable during the conversion;
2) The contents of a 10 bit binary counter are latched.

The 10 bit binary counter at that instant, contained the number of $1/4^{o}$ intervals from the last zero crossing of the Phase A inverter output voltage. The counter will be reset for an equal time before and after zero is crossed. This interval, which will be determined later, will be corrected for in the software by adding counts to the count read from the counter latches. The signal to latch the counter will occur a minimum of 40 ns after the 10^{o} sync pulse is applied to increment the counter, to assure that the counter outputs have stabilized.

Approximately 300 ns after the 10^{o} sync signal occurs, control circuitry #1 issues a convert signal to A/D converter. The $\overline{\text{complete 1}}$ signal informs the main microprocessor that the data is ready to be latched. To latch the data and to release the sample and hold from the hold mode, $\overline{\text{convert 1}}$ is brought high.

The sub-module #1 when operated in the 10^{0} syncronized mode will allow measurements to be made at 10^{0} intervals on the same phase or a different phase.

5.2.4 SENSE SIGNAL CONDITIONING APPROACH

Figure 19 lists 2 sets of 7 sense signals. The seven sense signals measured by the 8 bit A/D converter will be conditioned to provide signals in the 0V to +10V range.

The sense signals measured by the 10 bit A/D converter will be conditioned to provide signals in the -5V to +5V range.

Detailed information concerning existing sense signal output voltage levels and waveforms is required before any additional conditioning circuitry can be detailed.

The inverter output voltage sense conditioning approach is detailed below, since it uses no transformer.

To sense the inverter output voltages directly the maximum expected peak output voltage must be attenuated to a level suitable for measurement. Precision resistors (.1%) will be used to attenuate ($120 \times \sqrt{2} \times (100\% + 15\% + 1\%) = 196.9$ vpK. Allowing a safety margin, then 210V will be attenuated to +5V, which will require a 42:1 attenuation.

5.3.0 MICROPROCESSOR INTERFACE CONSIDERATIONS

The main microprocessor will be interrupted from several sources. The interrupting source must be identified so that the corresponding interrupt routine can be executed. Interrupt polling and interrupt vectoring are common methods used. Interrupt vectoring will save time and will be the preferred method if the selected microprocessor has this feature.

It is mandatory that control signals to the various modules are latched. It is good practice to group signals that control the same module or submodule together. This is done so that a software routine intended for controlling one module can write to a latch dedicated for that module and not concern itself with operations in other modules. To attain maximum speed of generating control signals to a module and reading data from a module it may be desirable to make the latches appear as memory locations to the main microprocessor. This would allow data to be written or read in one memory write or read-instruction over a common data bus.

5.4.0 MICROPROCESSOR DUTIES

The following microprocessor duties will be performed while the power conditioner is operating:

1) Measure converter output voltage often;
2) Measure inverter input current when large changes occur in converter output voltage;
3) After converter output voltage is stabilized, then sample the inverter output voltage to determine error. Correlate that sample to a position on the sine wave. Determine the error;
4) Correct the converter operating frequency;
5) Regularly measure power conditioner input voltage;
6) Respond to a commutation failure interrupt;
7) Occasionally measure temperature sensors and speed of fans;
8) Occasionally measure user adjustable output voltage setting on the front panel;
9) Occasionally sense front panel frequency select switch. If disturbed, then do an orderly power down and reset.

5.5.0 SELF-TEST

The self-test, executed shortly after the power conditioner is turned on, is intended to verify proper operation of the controller and power conditioner before applying power to the load.

STEPS

1. Hardware reset
2. Hardware comes up with control signals to power conditioner deactivated.
3. Interrupts are disabled. Without using RAM for storing results or using stack, execute some arithmetic instructions.
4. Verify the portion of RAM memory used for stack by writing and reading various patterns.
5. Verify the entire RAM.
6. Read the waveform generation PROM. Verify that all PROMS are present, aligned correctly, in the right socket, contain authorized timing pattern, etc.
7. Enable interrupts.
8. Verify the A/D's with a DAC if available and calibrate the A/D's with a precision reference voltage if available.
9. If a timer/counter is available calibrate the digitally controlled converter oscillator. Store a digital input vs. frequency output profile in RAM.
10. Verify AC input voltages are correct.

11 Check fan speed, temperature sensors, etc.

12 Keeping the inverter SCR's disabled, program the converter control frequency to a low frequency.

13 Enabling, one converter phase at a time, check if each is operational.

End of self-test.

If an error occurred, then,

1) Do not go to operate;
2) Display an error code to warn the user;
3) Allow the user to override the controller and proceed to operate if the error condition is minor.

5.6.0 PLANS FOR TASK THREE

Task three will be the selection of a microprocessor. The following is a partial list of features that will be desirable in the microprocessor.

1) Ample availability of general purpose registers and index registers;
2) Efficient instruction repertoire and fast execution time;
3) Reputation of manufacturer, availability of development tools and product support, second sources, possible Mil-Spec;
4) Vectored interrupts;
5) Timer/counter; either in microprocessor or support devices;
6) Single power supply operation;
7) Low power consumption.

1) Study, further, the interface requirements of the baseline design modules. Investigate various popular methods of input/output interfacing. For instance, memory mapped I/O, peripheral interface adapters, parallel peripheral interface, etc.;
2) Quickly narrow the possible selection to 8 microprocessors;
3) Based on trade offs of the seven items above narrow the possible selection to two microprocessors;
4) Compare and evaluate the two microprocessors. Perform a trade off study based on the interface requirements determined in Step 1.

6.0.0 DISCUSSION

An updated timing chart, supplied by MERADCOM during this reporting period, was found to conflict with the information on pages 10 and 11 of Source No. 3. The timing chart, Source Number 4, is dated 9/25/78 by A. H. Barrett, and will be considered as new information that supercedes the Delco report dated July 1978.

The approaches presented in this report form the baseline design of the controller, except the approaches listed below:

1) Converter oscillator approach; DAC/VCO or frequency synthesizer;
2) Inverter SCR timing circuitry approach; Approach #1, provide more resolution; or Approach #2, duplicate existing Delco timing.

The optimum approach for the converter oscillator is discussed below.

The DAC and VCO output frequency will respond to a binary input faster than the frequency synthesizer will. At high converter operating speeds the frequency synthesizer delay can be expected to slow regulation significantly. Although the frequency synthesizer approach offers very desirable features, unknowns such as overshoot and undershoot, capture range, looking on to harmonics, etc., noise sensitivity, may cause delays in development. For reasons presented in Section 5.2.1, correlation between a binary input and the frequency out is advantageous.. The frequency synthesizer offers this feature, but If a counter is made available, then a profile of the DAC and VCO combination can be determined during self-test and stored in RAM. By correlating the binary input to the oscillator output frequency at only a few points, the entire frequency range can be correlated since the VCO will be linear.

The DAC and VCO approach will be selected and a frequency counter will be incorporated into the design. Some microprocessor devices include a timer/counter so design of the counter will be delays until after the microprocessor selection.

The optimum approach for the inverter SCR timing circuitry is discussed below. Approach #1 will provide $1/2^{o}$ resolution of inverter SCR timing signals. A $1/4^{o}$ resoultion can be provided with a modification. Therefore, each of the timing signals to the 28 SCR's may be advanced or delayed slightly, permitting the step-approximated sinewave to be optimized with very few constraints. This may reduce the total harmonic distortion at the inverter output, before filtering.

Approach #2 will duplicate Delco timing exactly with circuitry similar to Approach #1. The breadboard may be built to allow both approaches to be tried with minimum difficulty.

Approach #1 will require that a new timing pattern be developed, but a proven timing pattern is preferred. Therefore, Delco authorized timing will be duplicated by the baseline design using Approach #2. Approach #2 will include additional circuitry to provide 10^{o} and $1/4^{o}$ timing signals to the sense signal data acquisition module.

Consideration was given to designing the modules to require minimum control from the main microprocessor. Possible approaches were abandoned and not presented because of the extensive use of hardware to minimize the control required from the main microprocessor.

The approaches presented offered optimum compromises. The effort to simplify the control interface and minimize low level tasks performed by the microprocessor was successful. Reviewing the duties that are required of the microprocessor it is believed that several microprocessors available on the market today can qualify for evaluation in the next task. However, several tasks may be required of the selected microprocessor that are not foreseen at this time. Rather than limiting the selection to a very powerful microprocessor to prepare for tasks that may not occur, the following alternative exists.

A low cost single chip microcomputer can act as a satellite to the main microprocessor. It may be used to assume part of the main microprocessor duties. However, the need of an additional microprocessor at present seems remote.

7.0.0 CONCLUSIONS

The baseline design has been completed to the maximum extent practical before selection of the microprocessor and detailed design of the breadboard.

It is concluded that all existing Delco SCR gate driver circuitry can be utilized by the new controller. Also, all the existing sense signal circuitry can remain intact, and most will be used. As development proceeds it may be necessary to add additional conditioning circuitry to some sense signals. The existing inverter output voltage sense signals will remain intact but not be used, at the present. Instead, a direct connection through a precision attenuator is preferred. It is also concluded that duplicating the Delco authorized inverter SCR timing pattern rather than modifying it, is the direction that will be taken at this time.

8.0.0 RECOMMENDATIONS

1) It is recommended that the baseline design presented in this report be used to begin hardware development, after the microprocessor is selected.

2) It is recommended that a technical conference be held at Yucca International before the completion of the microprocessor selection, for the purpose of review and concurrence with the baseline design.

3) It is recommended that Yucca International proceed immediately to the next task, the selection of a microprocessor.

9.0.0 DISTRIBUTION

Three copies to -- W. David Lee, DRDME-EA

Two copies to -- John A. Gabby, DRDME-PE-1

APPENDIX A

The following are answers received from MERADCOM in response to the questions listed in Appendix B of the report on Task 1.

1) The converter resonant frequency is approximately 9KHz;
2) The transformers shown on page 6-15 are not the same as those on page 6-13. Transformers on page 6-14 drive those on page 6-15;
3) Transistor controlling ends of center tapped transformers on page 6-13 are turned on alternately. The oscillator on page 6-14 runs about 330 KHz. On Figure 21 U14 should be U15 and vice-versa.

The charts and graphs requested have been received.

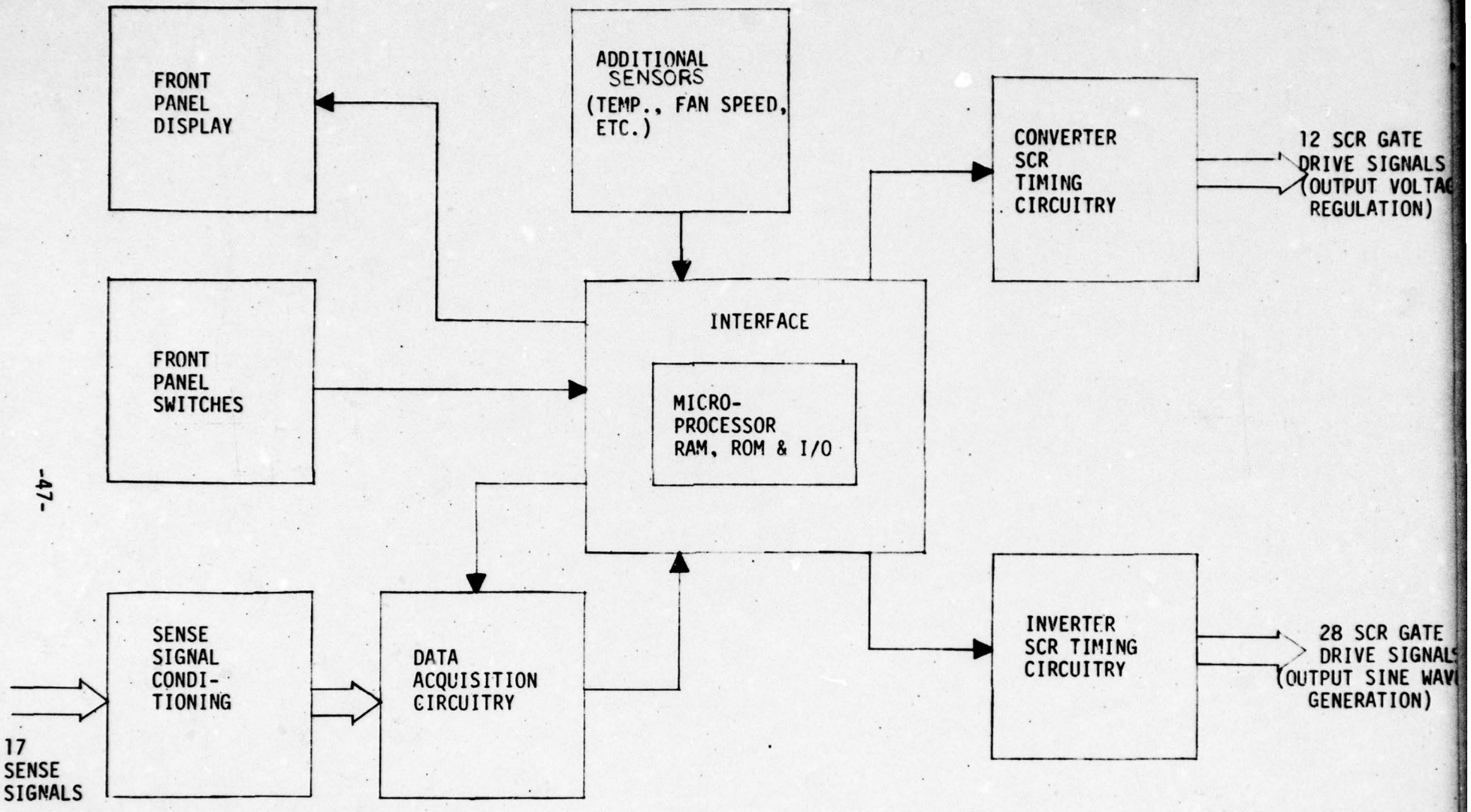


FIGURE 1: CONTROLLER FUNCTIONAL BLOCKS

CONVERTER OUTPUT VOLTAGE	INVERTER INPUT CURRENT	POSSIBLE CAUSE FOR CHANGE
DECREASE	DECREASE	LOW AC INPUT VOLTAGE, MISSING PHASE, FAULTY CONVERTER
DECREASE	INCREASE	INCREASED LOAD REQUIREMENTS
INCREASE	DECREASE	DECREASED LOAD REQUIREMENTS
INCREASE	INCREASE	HIGH AC INPUT VOLTAGE. UNAUTHORIZED CHANGE IN CONVERTER FREQUENCY

FIGURE 2: TRUTH TABLE FOR IDENIFYING CAUSE OF CONVERTER OUTPUT VOLTAGE CHANGE

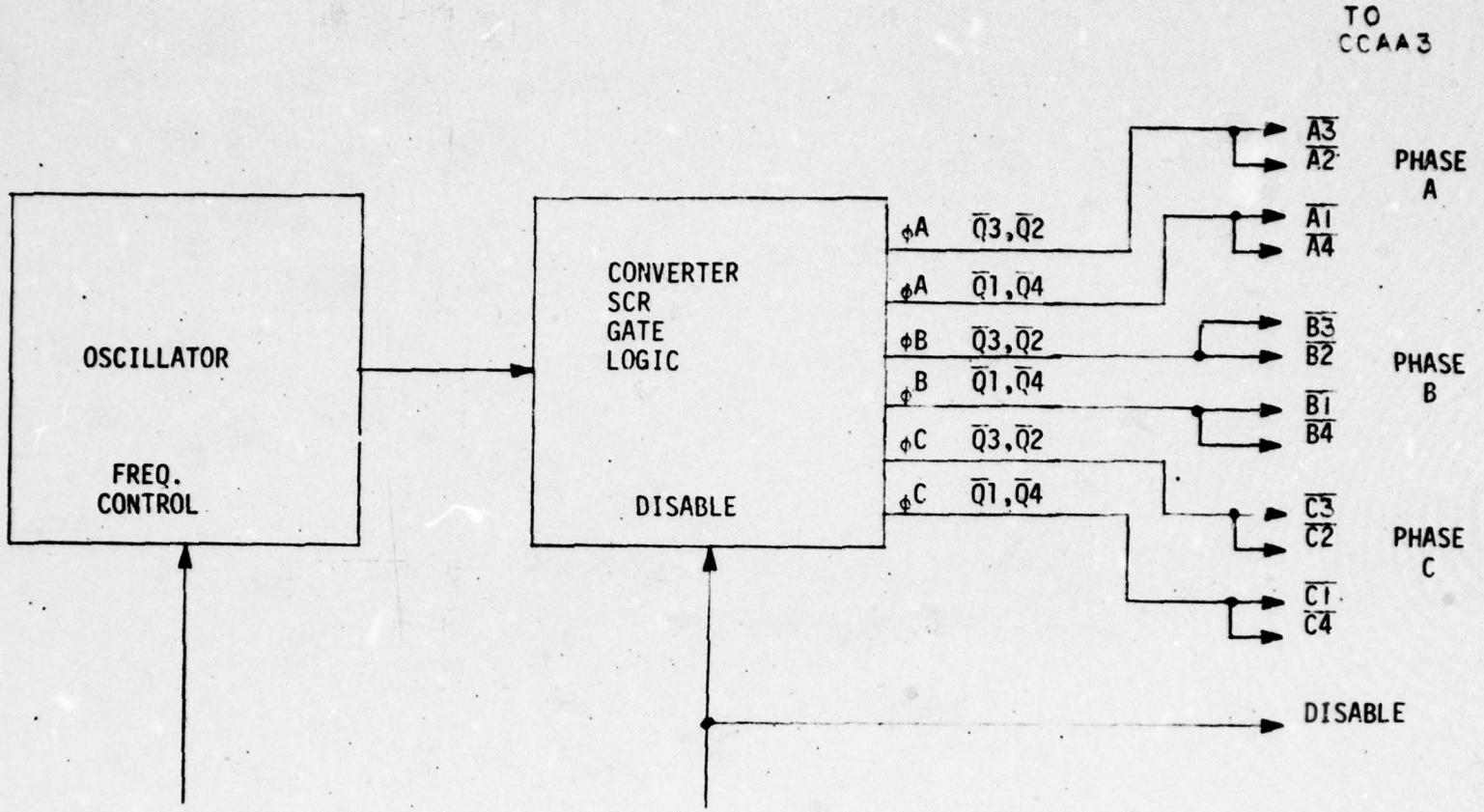


FIGURE 4: CONVERTER SCR TIMING CIRCUITRY BLOCK DIAGRAM

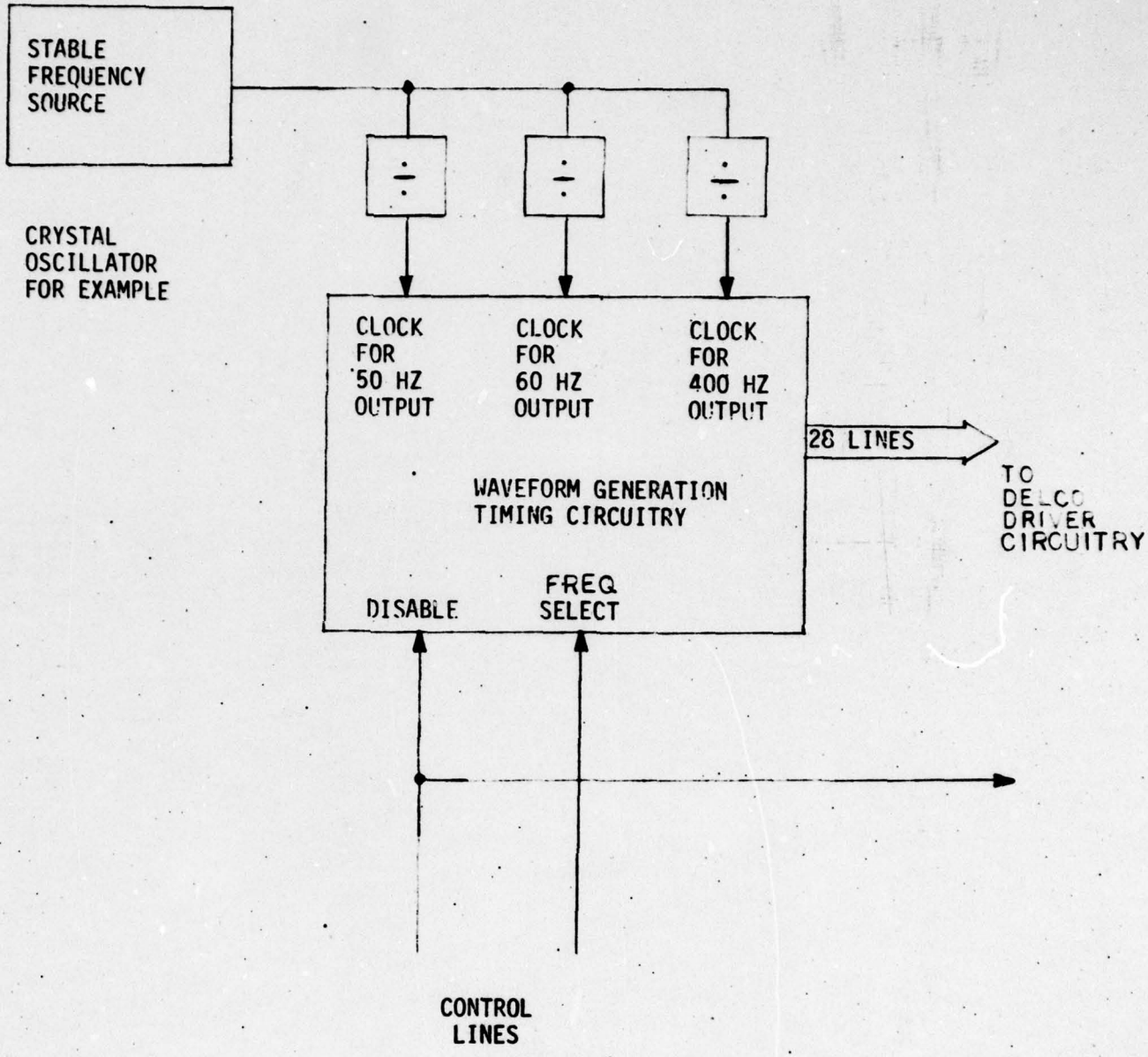
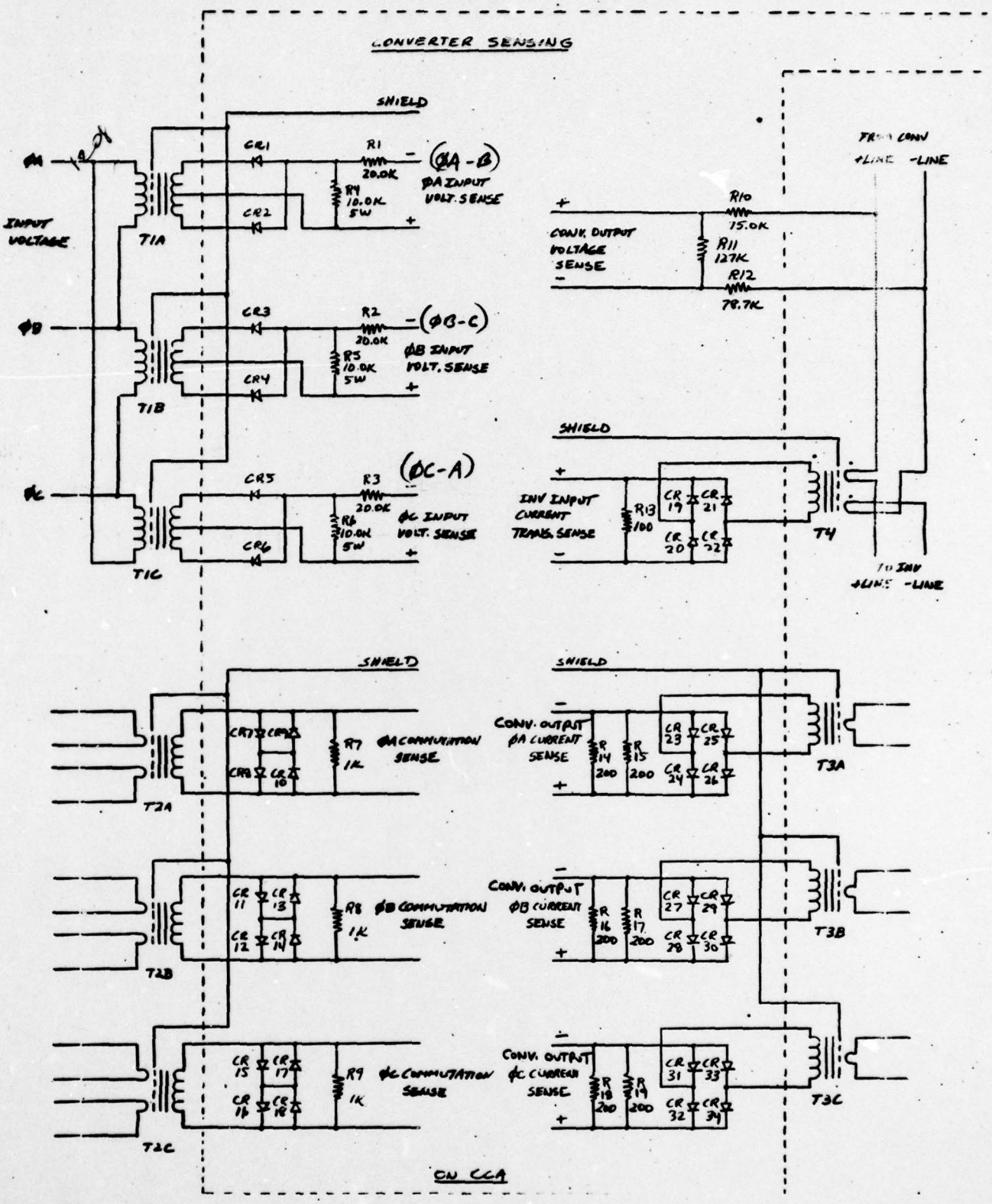
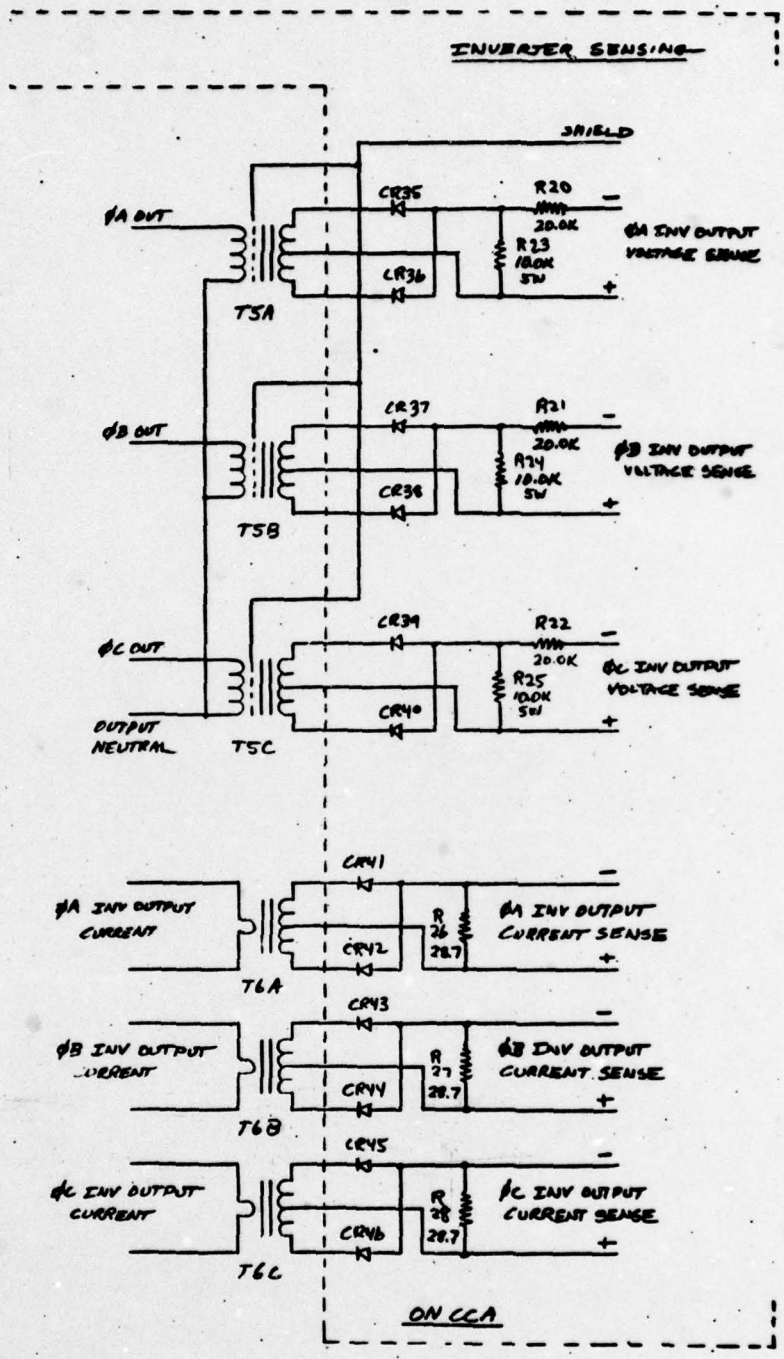


FIGURE 5: INVERTER SCR TIMING CIRCUITRY BLOCK DIAGRAM



PART 1 OF 2: REPRODUCED FROM FINAL REPORT AC-DC SECTION
CONTRACT NO. DAAK70-77-C-0035, P. 6-4

FIGURE 7: EXISTING SENSE SIGNAL CIRCUITRY



PART 2 OF 2

FIGURE 7: (CONTINUED)

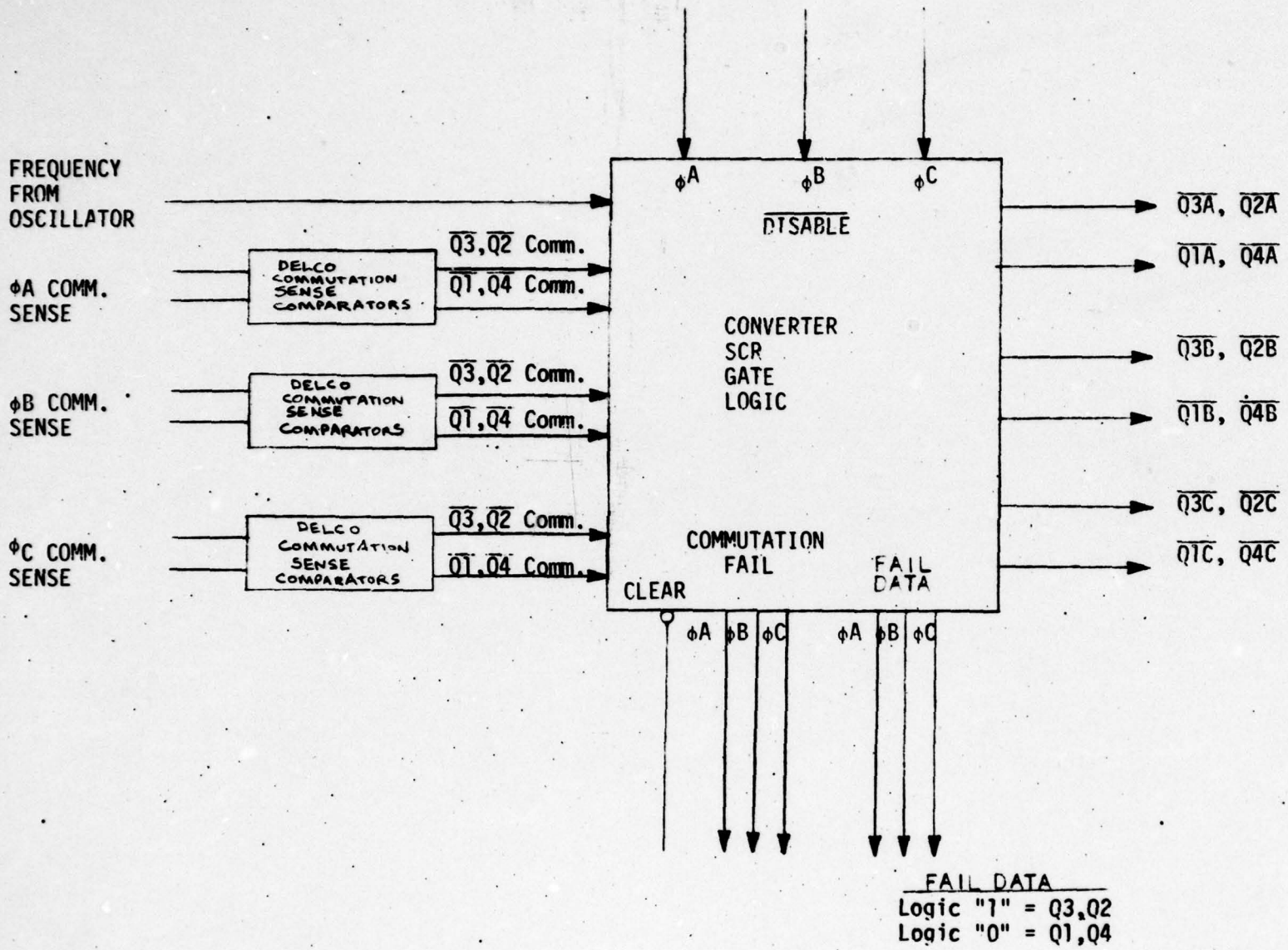
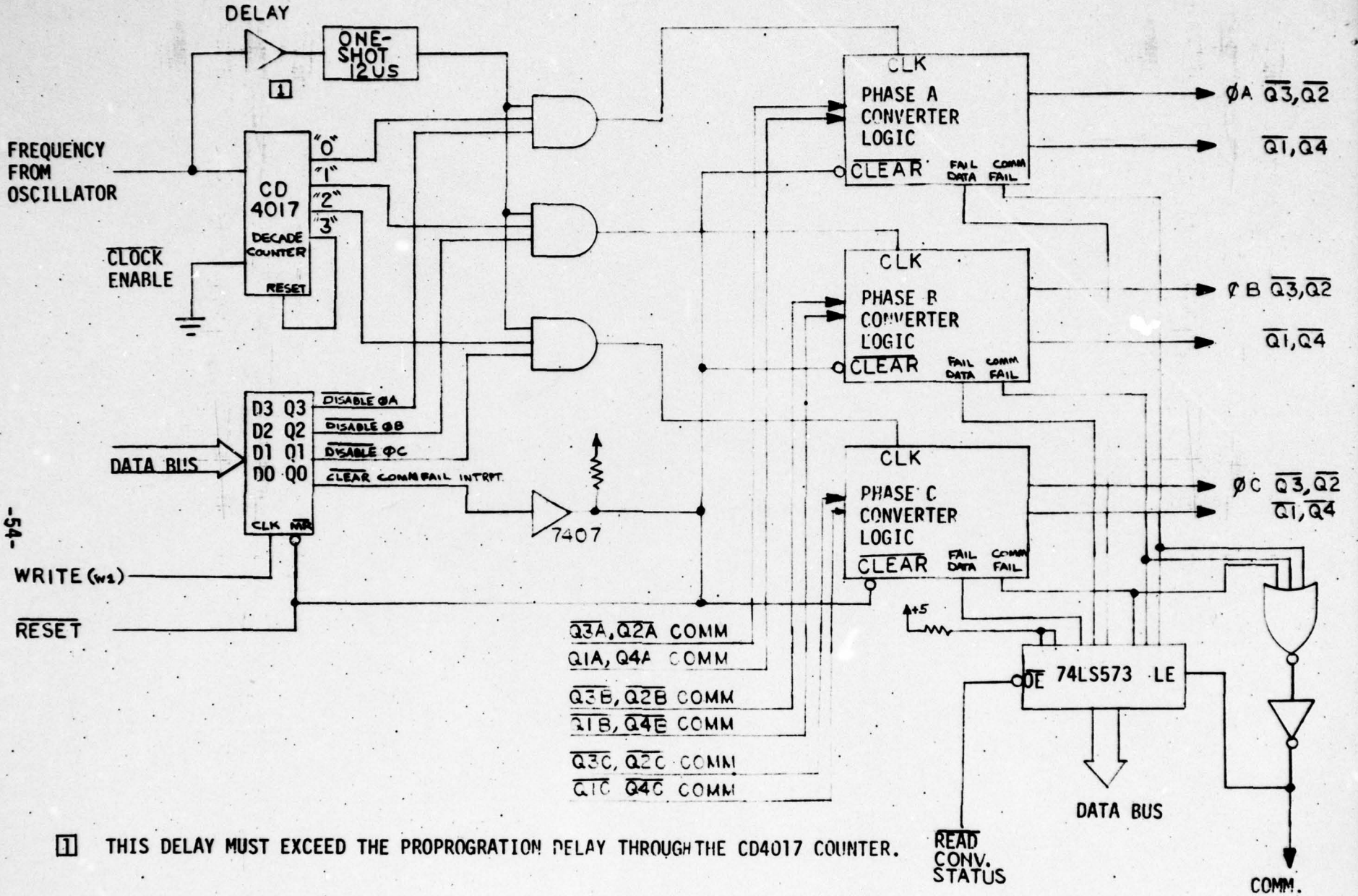


FIGURE 10: CONVERTER SCR GATE LOGIC CIRCUITRY BLOCK DIAGRAM



1 THIS DELAY MUST EXCEED THE PROPROGRATION DELAY THROUGH THE CD4017 COUNTER.

FIGURE 11: CONVERTER SCR GATE LOGIC DETAILED BLOCK DIAGRAM

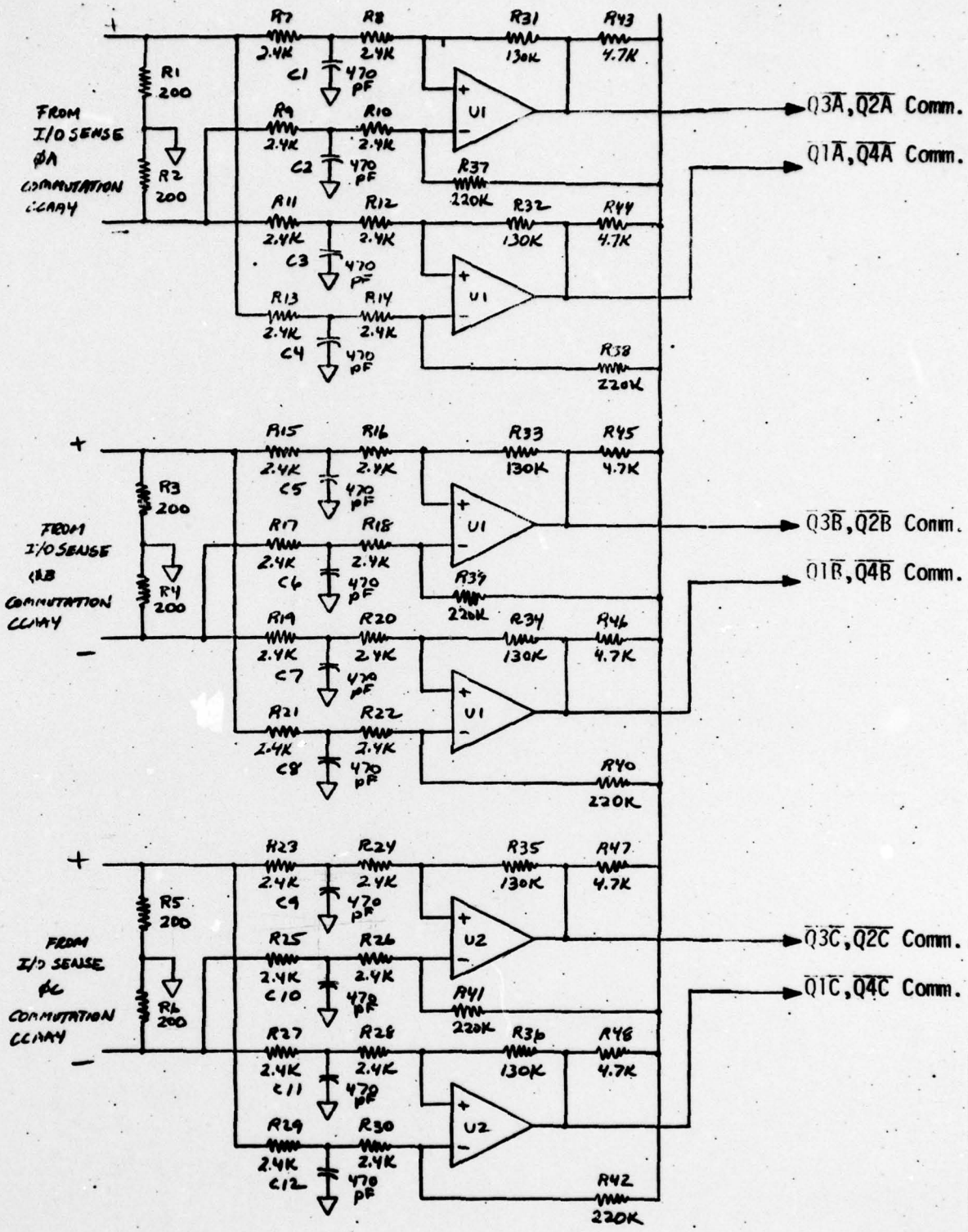
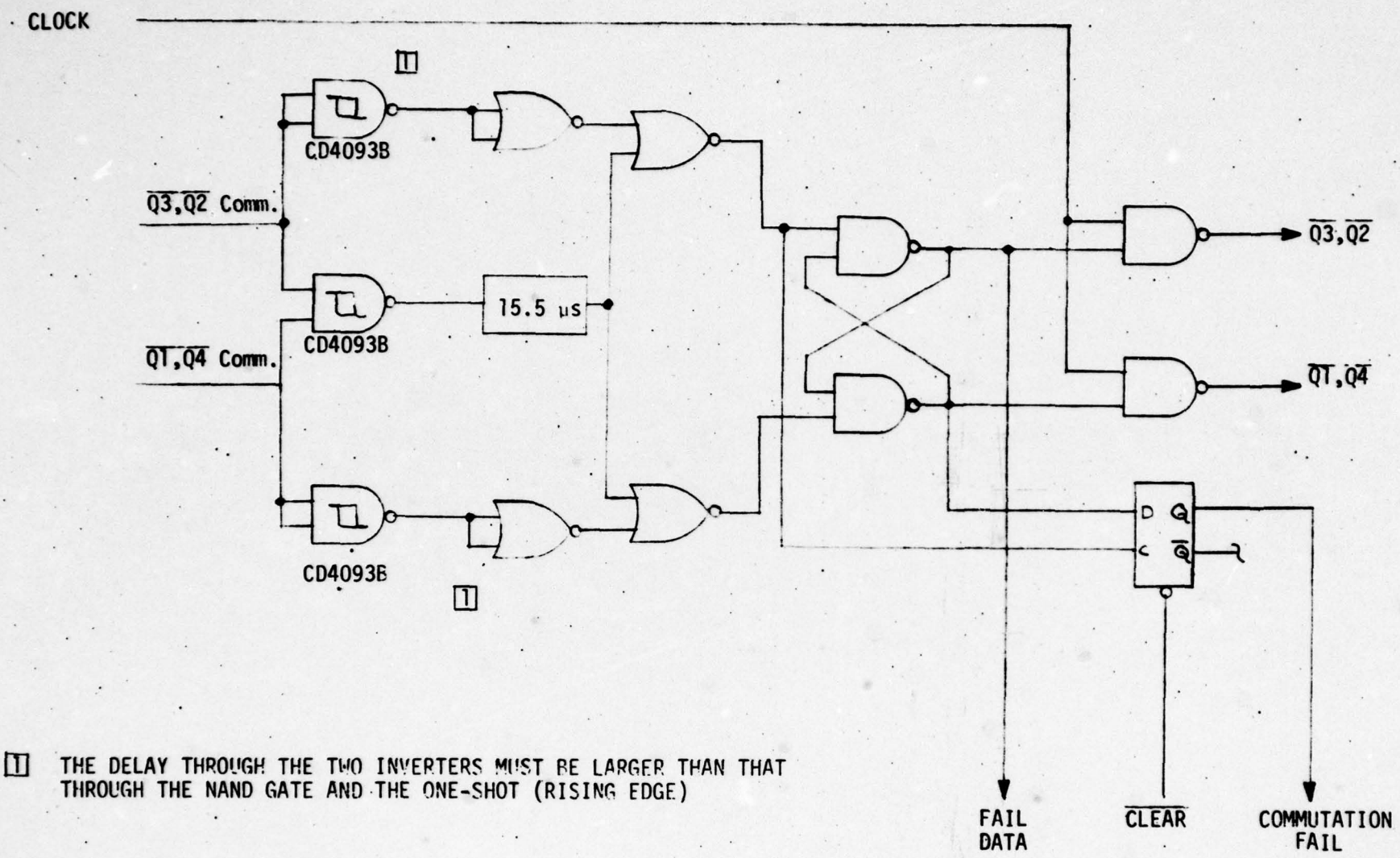


FIGURE 12: DELCO COMMUTATION SENSE COMPARATORS



[1] THE DELAY THROUGH THE TWO INVERTERS MUST BE LARGER THAN THAT THROUGH THE NAND GATE AND THE ONE-SHOT (RISING EDGE)

FIGURE 13: CONVERTER LOGIC

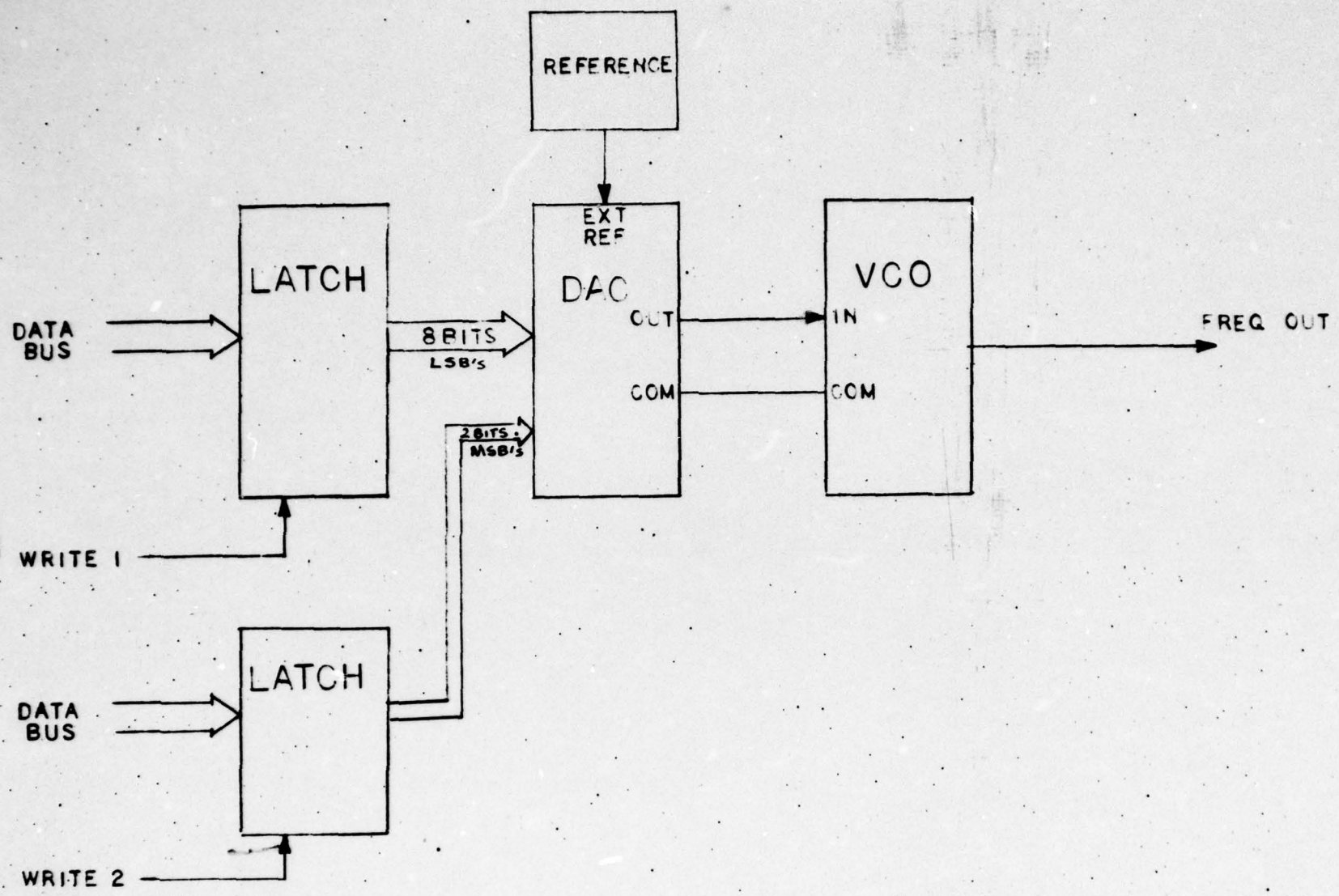


FIGURE 14: CONVERTER OSCILLATOR APPROACH #1

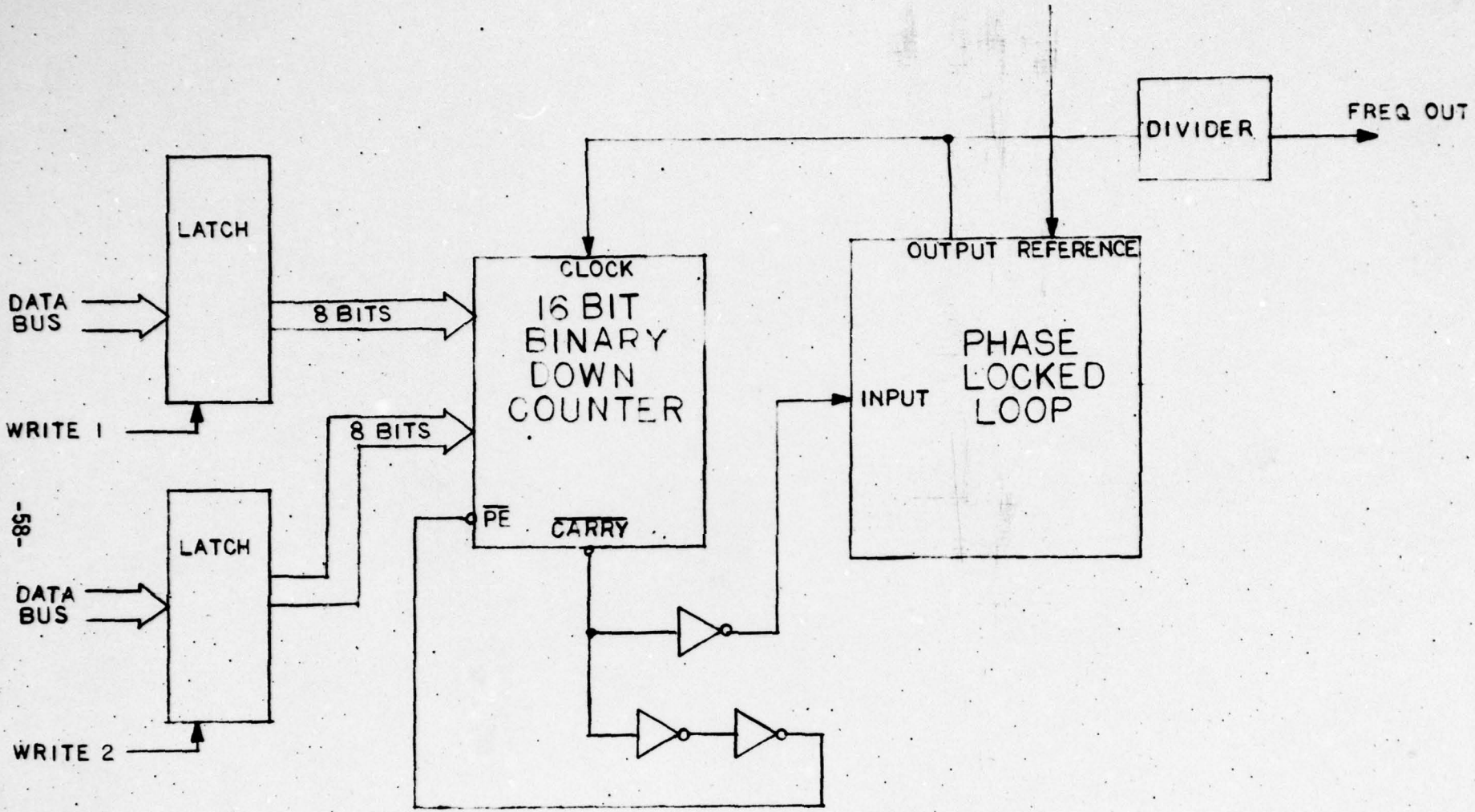
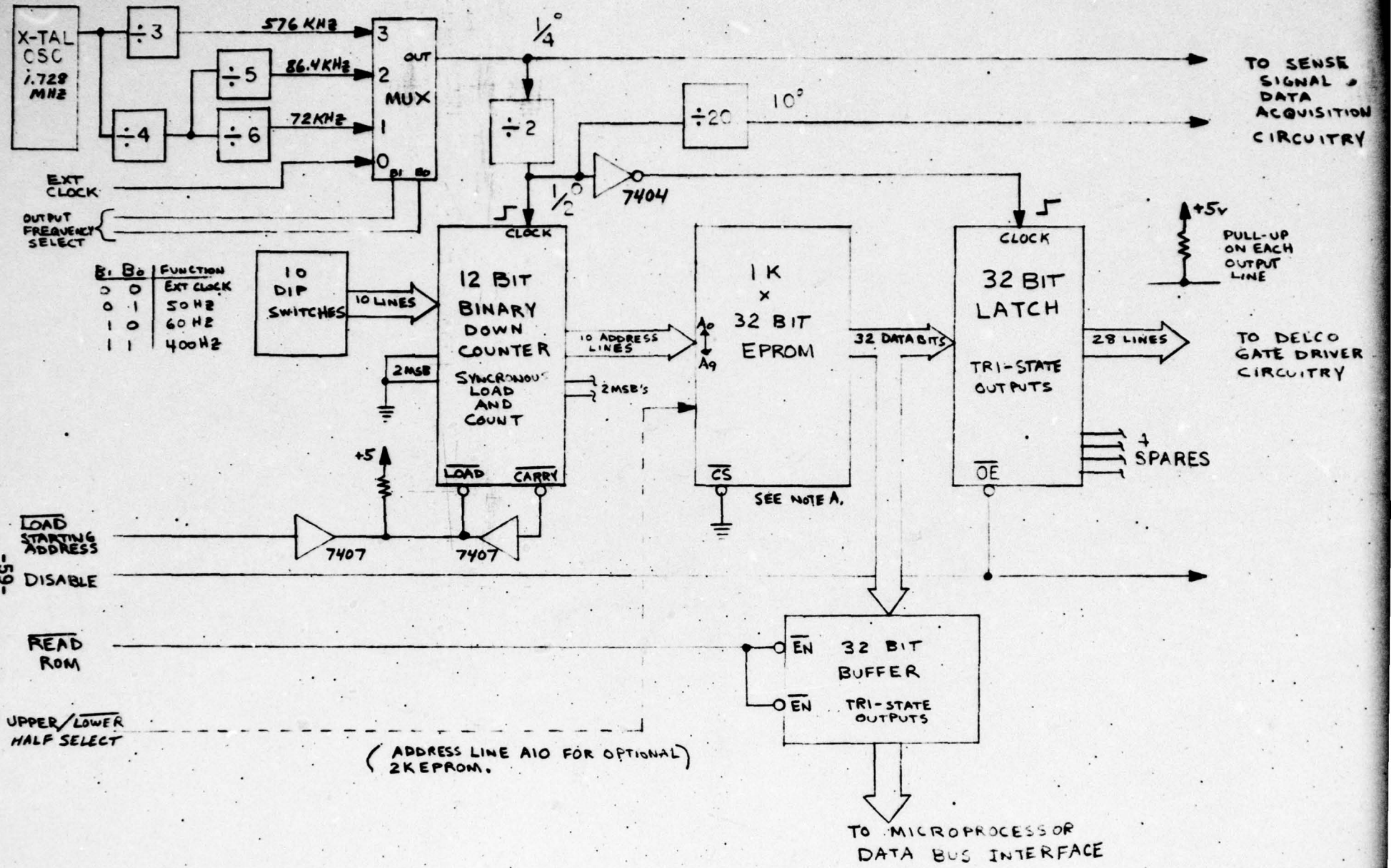
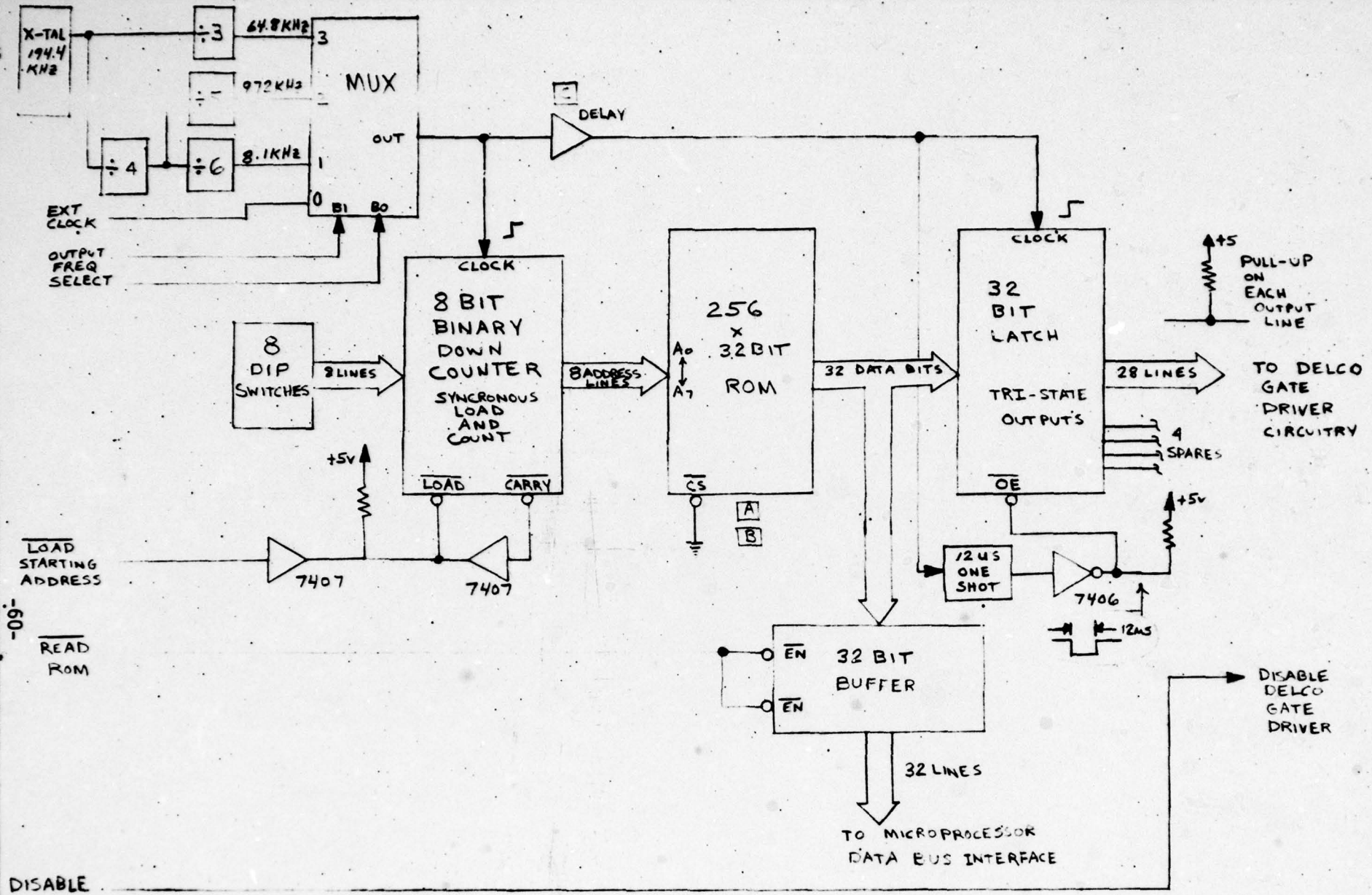


FIGURE 15: CONVERTER OSCILLATOR APPROACH #2



NOTE A. THIS CIRCUIT ASSUMES THE SAME TIMING PATTERN WILL BE USED FOR 50HZ, 60HZ, AND 400HZ. THE CIRCUIT MAY BE MODIFIED TO USE DIFFERENT TIMING FOR 400HZ AND 50HZ/60HZ. THE MODIFICATION WOULD CONSIST OF CHANGING THE 1K ROM TO A 2K ROM. THE MOST SIGNIFICANT ADDRESS LINE (A10) WOULD BE USED TO SELECT BETWEEN THE LOWER HALF OF MEMORY (50HZ/60HZ) AND THE UPPER HALF (400HZ).

FIGURE 17: INVERTER SCR TIMING CIRCUITRY APPROACH #1



A TO FIRE AN SCR, PROGRAM A LOGIC "0" INTO ONE LOCATION ONLY BECAUSE "0"'S IN SUCCESSIVE LOCATIONS WILL CAUSE MULTIPLE 12 µs PULSES.

B TIMING PATTERN WILL BE BACKWARDS IN ROM

C DELAY THROUGH NON-INVERTER MUST EXCEED SETTLING TIME OF COUNTER AND ROM DATA ACCESS TIME.

FIGURE 18: INVERTER SCR TIMING CIRCUITRY - APPROACH #2

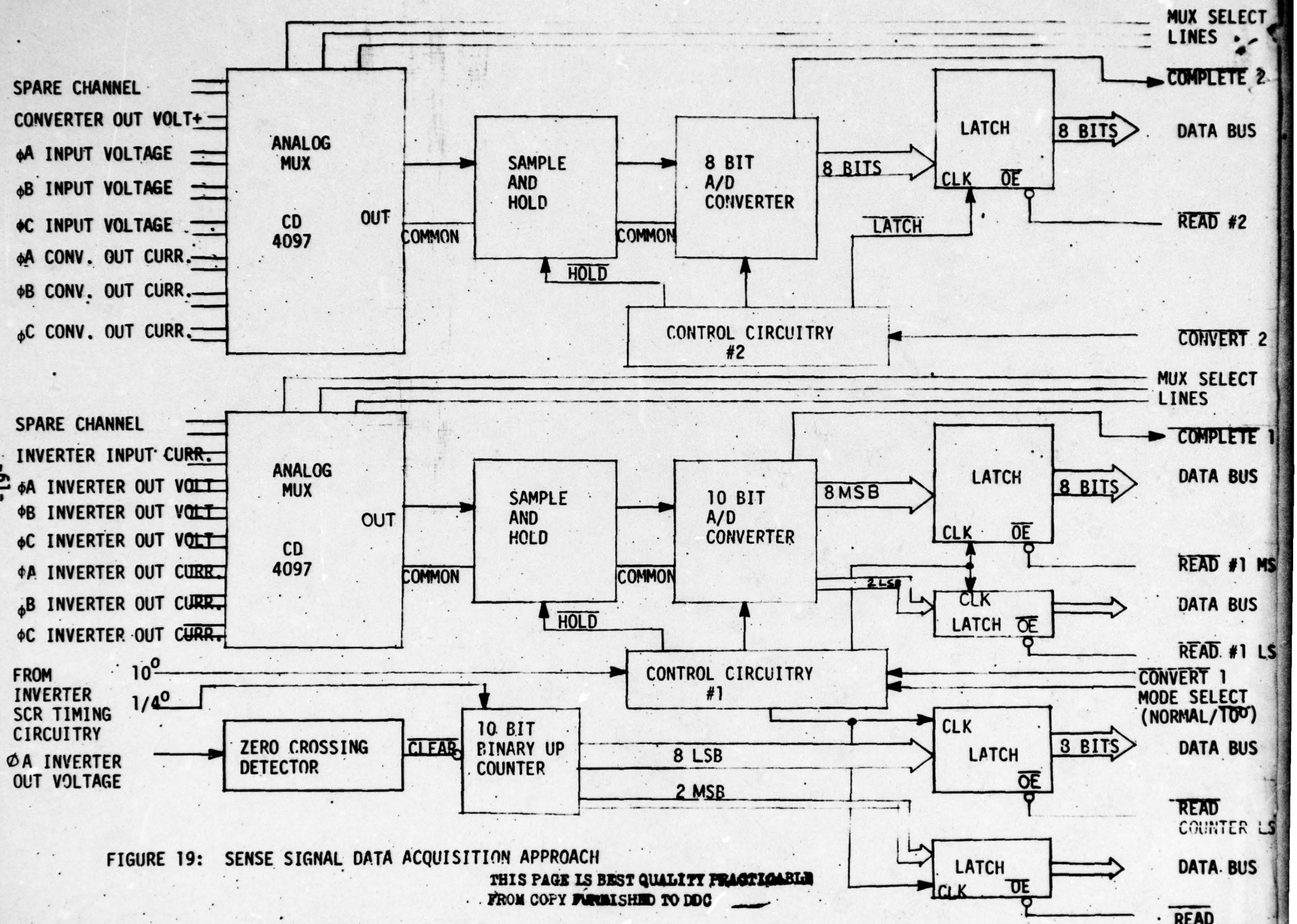


FIGURE 19: SENSE SIGNAL DATA ACQUISITION APPROACH