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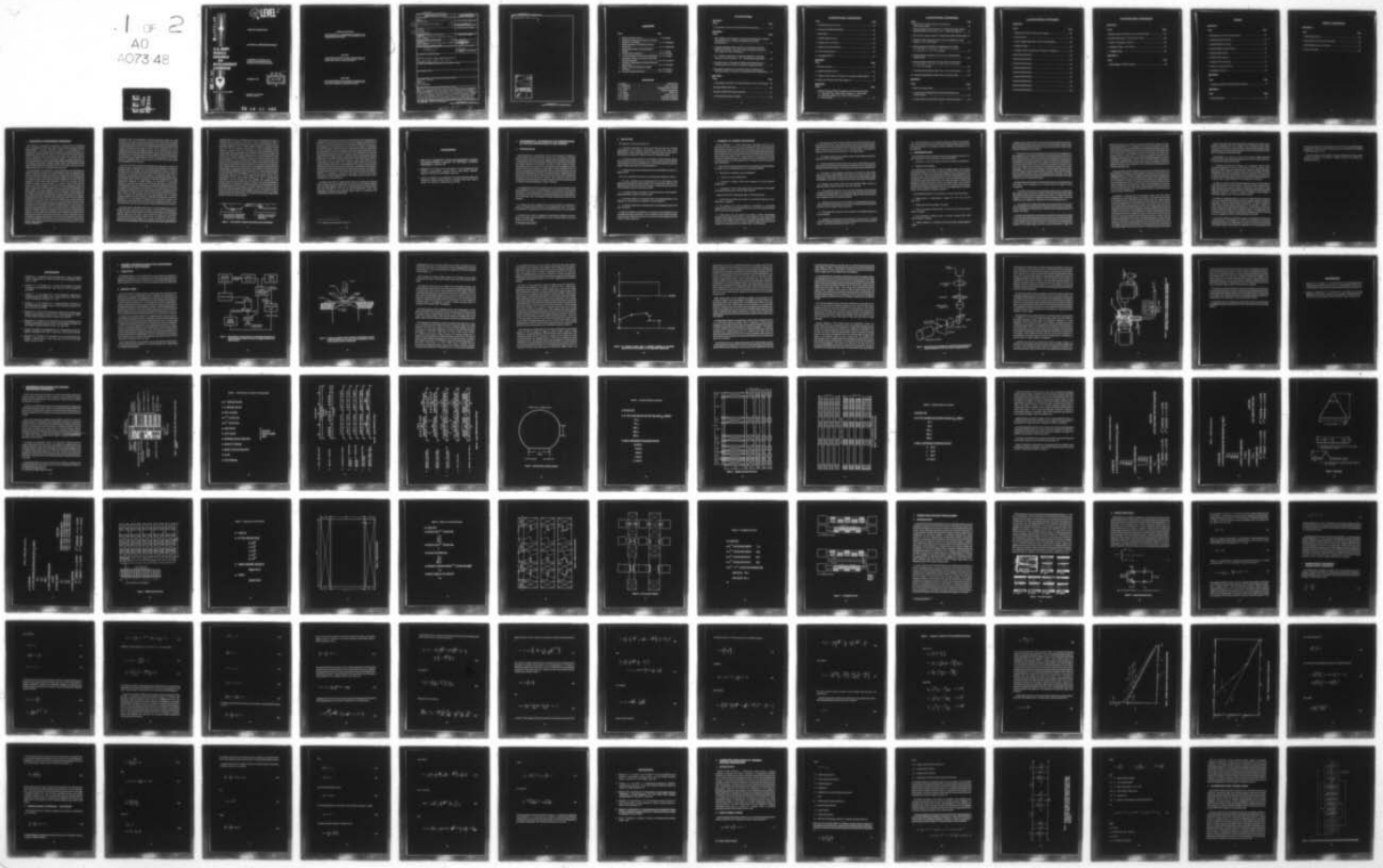

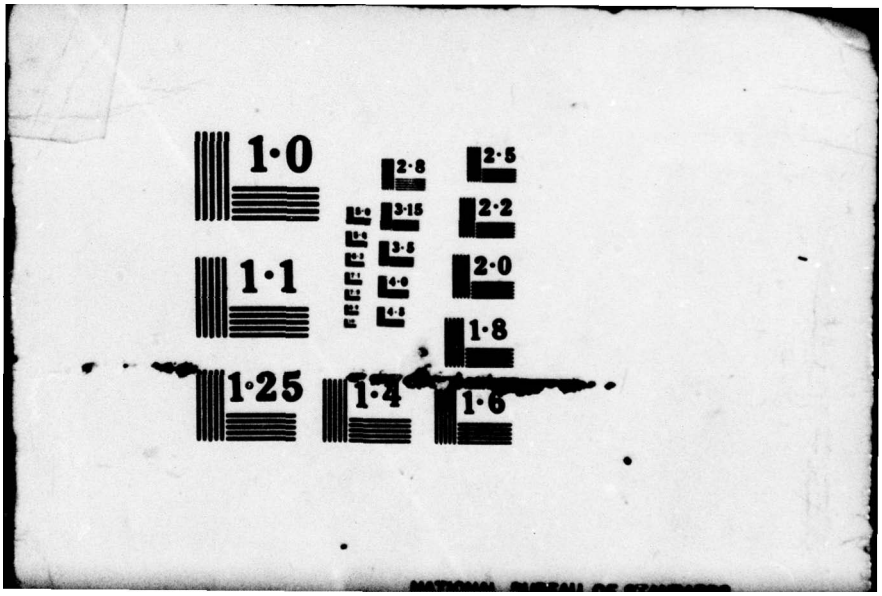
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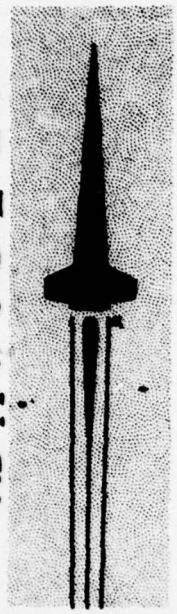

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TECHNICAL REPORT E-78-22

ELECTRICAL OVERSTRESS PROGRAM

D. Mathews, P. P. Budenstein, et al.
Advanced Systems Development and
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U.S. ARMY
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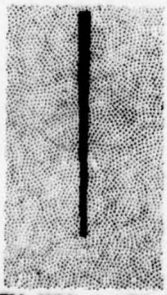

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This report is a description of initial work, ~~1 February 1977 to 30 September 1977~~, on a program at the US Army Missile Research and Development Command (MIRADCOM) to provide information needed in the development of a nondestructive screen to eliminate junction bipolar devices especially suspectible to damage after second breakdown. Based on the results of the first 8 months of work, the decision has been made that the major thrust of the program should be towards identifying the reasons why specific samples of a given device type are unusually susceptible, rather than determining nominal → next page

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susceptibility of generic types.

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1. ELECTRICAL OVERSTRESS PROGRAM*

The following is a description of initial work, 1 February 1977 to 30 September 1977, on a program at the US Army Missile Research and Development Command (MIRADCOM) to provide information needed in the development of a nondestructive screen to eliminate junction bipolar devices especially susceptible to damage after second breakdown. Based on the results of the first eight months of work, the decision has been made that the major thrust of the program should be towards identifying the reasons why specific samples of a given device type are unusually susceptible, rather than determining nominal susceptibility of generic types. The program is sponsored by Defense Nuclear Agency, with additional kick-off support by MIRADCOM and SAMSO, Norton Air Force Base. This report is thus a combined final report on work during the first fiscal year.

The first problem to be considered is a rigorous definition of second breakdown. There have been many definitions of second breakdown which have appeared in the literature, especially in the early years of research. The definition to be used here is that any process in which a sudden drop in avalanche voltage occurs after the application of a sufficiently large current step input will be considered to be a form of second breakdown. Current mode second breakdown is thus also consistent with this definition. Questions of physical details, e.g., whether a current constriction has occurred, are avoided. Damage is not a part of the second breakdown process but rather a consequence of second breakdown and can be prevented. Depending on the details, quality, and normal variability of device production, different devices will have higher or lower threshold characteristics for susceptibility to second breakdown and, consequently, different probabilities for damage under identical test conditions. Some generic types will be inherently better than others, and some lots of nominally identical devices will have both a statistical distribution and a certain number of anomalous or "maverick" devices. Most, but not all, of the latter are usually weeded out as part of normal acceptance testing for other parameters, since they are a result of production errors or exceeding of production tolerance limits. It is thus necessary to determine what additional tests, if any, are required to weed out "weak" devices not caught by standard acceptance screening and to develop necessary additional test procedures. It is likely that much information will be available from standard tests if additional data reduction is performed. Just as flash x-ray tests provide data on device susceptibility to gamma-induced photo-currents which can be used both as a measure of relative susceptibility in comparing devices and as input data for a computer circuit analysis code, pulsed current data can provide the same information for second

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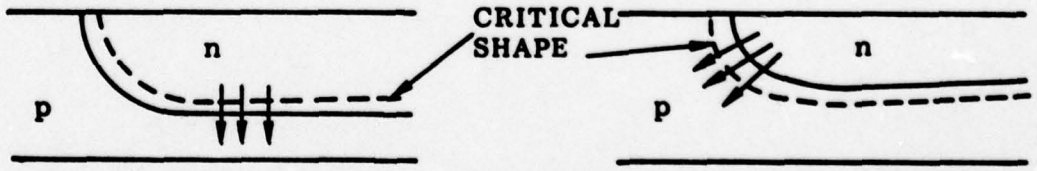
breakdown. While the development of electrical equivalent circuits for second breakdown is not a part of the program under discussion, such an effort could benefit from the analyses performed as part of this program. Just as we know the basic physics of ordinary operation of a transistor but find *detailed* mathematical calculation of the transient three-dimensional nonlinear process almost intractable (or at least impractical) even with a large digital computer, so it is with these special cases of breakdown; in both situations, engineering approximations must be made in order to get useful results. The analytical portion of this program is devoted to development and verification of such approximations. Moreover, a large portion of the work is devoted to "reliability physics," since the goal is to find out why certain samples deviate significantly from the norm.

The work in FY77 has consisted of determining what information is needed from laboratory research, planning the tests, obtaining and developing the necessary test equipment and test samples, and performing background analyses of physical processes known to be significant in the second breakdown process. These topics are discussed by the respective principal investigators in subsequent sections. First, a description of second breakdown in special silicon-on-sapphire (SOS) diodes is given. These devices permit "direct" measurement of hot spot temperatures by a light transmissivity technique. A similar technique for observation in conventional transistors is currently under development. This project has begun so recently that it will be reported at a later date. SOS test samples are discussed, followed by summaries on analysis of second breakdown in ideal devices. Some special effects seen at high currents are then reported, and some initial analyses relevant to nonideal devices are given. Finally, a nominal test plan is given for batch testing of SOS devices after a series of overview tests determines the most serious problem areas. A detailed computer analysis of hot-spot formation in ideal SOS test diodes has recently been initiated by T. W. Tang. Electrical conduction in the silicon film is treated in two dimensions and heat conduction in the silicon film, the sapphire substrate, and the silox passivation is treated in three dimensions. Results will be reported at a later date.

It has been noted, in agreement with theories of a critical temperature or a critical energy, that when reverse biasing current pulses of less than a few milliseconds in duration are used as the driving source, the hot-spots always begin in the avalanching depletion region. For this reason, a large portion of the early work was directed toward determining the physical location where first breakdown would occur. Information on sustaining voltages for nonplanar structures was also obtained. Previous work by many authors had already indicated that hot spots normally form in

avalanche regions, but not necessarily at the point of maximum electric field as calculated from the geometry of the device. As shown schematically in *Figure 1*, variations in the geometrical dimensions of a given device may be sufficient to cause avalanche breakdown to occur in entirely different locations in nominally the same device [1]. This has important consequences for second breakdown, because avalanche is usually the first step in the sequence starting with application of the transient signal, passing through second breakdown, and ending in damage. One sample may be nearly impossible to damage in a given circuit configuration, while a second will be extremely susceptible to damage. It is important to note that while second breakdown, in the reverse-bias case, begins in an avalanching region, the location of the second breakdown site seldom coincides with the location of maximum field. Microstructural defects have been proposed by some authors as the explanation of this situation, because they could account for local high field concentrations. Other authors disagree. A large local electric field could be located at or near the hot spot if a microstructural inhomogeneity existed. Budenstein et al. [2] have shown by calculation that the effect of an inhomogeneity is to shift the hot spot location from its geometrically predicted site to an intermediate location between the site of the inhomogeneity and the geometrically predicted site. Thus, a submicroscopic examination of the new hot spot site would probably show nothing out of the ordinary. Moreover, the hot spot locations are known to vary with the amplitude of the driving pulse. Any attempt to correlate the presence of an inhomogeneity with an externally-measured electrical parameter should be expected to require driving the device into avalanche, because the inhomogeneity may very well be dormant as far as electrical activity is concerned until the avalanche condition is reached. For example, conditions required for the generation of certain types of electrical noise might include driving the device into heavy avalanche.



(a) AVALANCHE BREAKDOWN FROM REACH-THROUGH IN VERTICAL DIRECTION

(b) NORMAL AVALANCHE BREAKDOWN FROM SIDEWALL

Figure 1. Cross-section of devices with nearly the same dimensions.

SOS diodes have already proved to be an extremely effective tool in studying second breakdown. It should not be expected that the results of analyses of SOS diodes will carry over to conventional transistors, but rather that the SOS diodes should act as a proving ground for the analytical tools developed for the study of conventional devices. For example, the heat flow patterns in the depletion region of an SOS diode are vastly different from those in the depletion region of an epitaxial planar device, but the same general equations are used in each case. Some problems do exist with SOS diodes. Surface and interface states are important factors in determining avalanche breakdown of the samples [3]. This complicates the analysis and leads to conditions unlike those found in conventional transistors. Other bulk effects may be overshadowed by surface effects. The avalanche voltages predicted by SOS diode analysis are greater than those seen experimentally. The extensive series resistance regions tend to mask some purely junction effects and overemphasize bulk properties. The most serious limitation is that except for electrical characteristics, only changes in temperature may be observed. Thus, injection effects can only be observed indirectly. However, it is important to realize that every major, and nearly every minor, observation of second breakdown effects in SOS diodes has been found to have a counterpart in conventional devices.*

An analysis of the effects of change in bulk resistivity with temperature indicates that the voltage drop across the high resistivity side can occur quite rapidly. While this effect is probably negligible in most cases in conventional devices, because the device must heat sufficiently to cross over the resistivity-temperature "hump" while maintaining a reasonably large undepleted collector region, it is important to the understanding of SOS device phenomena.

*Dr. P. P. Budenstein, private communication, March 1977.

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2. EXPERIMENTAL TECHNIQUES FOR OBSERVATION OF SECOND BREAKDOWN IN SOS DIODES*

A. INTRODUCTION

Second breakdown in semiconductor devices occurs through the formation of current filaments under sufficiently high electrical stress. The dynamics of filament formation have been studies in silicon-on-sapphire devices by Sunshine and Lampert [1-4] and Pontius, Smith and Budenstein [5-8] under both forward and reverse biases. The features observed in these devices are similar to those observed in three-dimensional systems [4]. The reason for working with silicon-on-sapphire devices is that these devices are transparent to visible light at room temperature but, as the devices rise in temperature, their transparency decreases. Thus it is possible to view the devices with transmitted light and infer, with proper calibration, temperature over the device surface. If the light source is pulsed on for a short period, then the temperature distribution during this period can be inferred. This comprises the basis for the stroboscopic method developed by Sunshine at the RCA Laboratories and advanced by Pontius, Smith and Budenstein at Auburn University.

A considerable effort has been expended by others to develop screening tests so that the susceptibility of devices to second breakdown can be evaluated. Such tests have been based on various measurements at the device terminals, but the relationship of the measurements to the filamentation phenomena associated with second breakdown has not been clear. Thus, the attempts to develop screening criteria have not been successful.

In a similar vein, device designers have not had the means for predicting the locations of filaments and the stresses at which filamentation occurs. The roles of device geometry, doping densities, and device imperfections have not been clarified.

The present work is part of a program for enhancing the reliability of electronic devices with regard to second breakdown; effective screening methods and device design criteria are sought.

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*P. P. Budenstein, Auburn University

B. OBJECTIVES

The objectives of the present program are:

1. To perform experiments of a basic nature which will lead to an increased understanding of the nonlinear, electrothermal processes that cause current filamentation in silicon-on-sapphire diodes. Of particular concern are the roles of device geometry, doping levels, diffusion spikes and metallization spikes.

2. To develop analytical models for the influences of diode geometry, doping, diffusion spikes and metallization spikes on current filamentation under both forward and reverse biases in silicon-on-sapphire diodes. Such models will provide a basis for design of diodes more resistant to second breakdown.

3. To develop nondestructive screening tests for second breakdown in silicon-on-sapphire diodes.

The work is subdivided according to the following plan, designated as Phase I:

1. To make a detailed survey of filamentation for the wide range of diode geometries and dopings that will be available. The survey will cover pulses of 0.1 μs to 1000 μs duration in both forward and reverse biases. Voltages and current waveforms will be obtained along with stroboscopic pictures.

2. To correlate locations of filaments and filament growth to diode geometry, doping, metallization spikes and diffusion spikes.

3. To develop models for the observed effects and suitable guidelines so that designers can create devices less susceptible to second breakdown.

4. To develop nondestructive screening tests for second breakdown based on the device waveforms.

To place the objectives in perspective, it is necessary to first summarize current knowledge of filamentation (Section 3). Then a description of the overall experimental program is given, followed by a statement on the portion of the program that will be covered in Phase I (Section 4).

C. SUMMARY OF CURRENT KNOWLEDGE

Second breakdown is a current filamentation phenomenon that occurs in semiconductor junction devices and other semiconductor devices when abnormally high electrical excitations are applied. Second breakdown occurs under both forward and reverse biases, with the locations of the current filaments depending upon the bias. *Second breakdown device testing is greatly facilitated by employing constant current* pulses, because the voltage is then a unique function of the current. Our previous studies have followed the onset of current filamentation in some detail [4-8]. To create a common ground for the following discussion, it is useful to mention some features about filamentation.

1. There exists an incubation period prior to the formation of current filaments. The length of this period depends upon the current pulse amplitude.

2. Three phases of conduction may be distinguished:

   a. Uniform (no current filamentation).

   b. Formation of multiple, broad current filaments in the solid (unmelted) semiconductor.

   c. Formation of a narrow melt channel within a broad filament with multiple melt channels forming under extremely high excitations.

Stages (a) and (b) are nondamaging; stage (c) is always destructive.

3. A device with a solidified melt channel is not necessarily inoperative, but its performance is degraded.

4. The locations of the current filaments are determined, in commercially prepared devices, more by the large-scale geometry and overall material properties than by microscopic inhomogeneities.

5. Under reverse bias, the locations and numbers of broad (nondamaging) filaments depend upon pulse duration. If pulse duration is kept constant while progressively increasing the pulse amplitude, the number of filaments increases to a saturation value. Further increase in pulse amplitude simply drives more current through the existing filaments and ultimately leads to melt formation

6. The saturation number of "broad" filaments under reverse bias increases with decreasing pulse duration, single filaments being narrower for the shorter pulses. Filaments are almost uniformly spaced when the saturation number has been reached. (With a junction extending 500 μm across a thin film diode (~1-μm thick), 30 filaments were observed upon excitation by a 5-μs, 620-mA pulse.)

7. The voltage waveform shows a slight drop when "broad" filaments begin and a large drop as the melt channel forms.

8. The pulse amplitude at which melts form (for a given pulse width) is not much greater than the pulse amplitude at which filaments first start to form. (The difference was about 30% for 100-μs pulses.) This difference decreases as pulse width decreases.

9. The locations of the filaments are different on forward and reverse biases. Under reverse bias, multiple filaments occur. They start at the p-n junction. Under forward bias, a single filament forms in the hottest part of the high-resistivity region. The filaments of reverse bias are generally much narrower than those of forward bias.

10. Damage occurs under forward bias with somewhat larger currents and somewhat smaller voltages compared to the reverse bias case.

11. The temperature-resistivity curve is the most important material property associated with second breakdown. For doped materials, the resistivity attains a peak at several hundred degrees above room temperature. High-resistivity materials peak at lower temperatures than low-resistivity materials.

12. High-resistivity materials are more sensitive to second breakdown than low-resistivity materials. Filamentation occurs at lower current densities and the filaments are narrower for the higher resistivity materials.

13. The thermal time constant for heat conduction to the sapphire substrate is a few microseconds.

14. Quantitative temperature-time mappings have been made by a scanning technique yielding the temperature profile across filaments with a time resolution of about 1 μs and a spatial resolution of about 10 μm.

15. Second breakdown can be explained adequately using an electrothermal model. The local changes of resistivity and of junction properties with temperature are of primary importance. Local changes of thermal conductivity with temperature are also significant.

D. EXPERIMENTATION

The total experimental effort required to fulfill the program goals will center on two types of experiments, each employing the stroboscopic method:

1. Correlation of current and voltage waveforms with filament configurations.

2. Temperature-time mapping.

The specimens for the program are silicon-on-sapphire diodes which are being fabricated specifically for our use by the Electronics Research Division of Rockwell International. The diodes will include plane parallel and special geometries, each covering a range of sizes and doping densities. Geometries and dimensions will be representative of commercial and military devices, with some additional devices that are somewhat larger (about 500 μm across) for special test purposes. Devices with deliberately introduced metallization spikes and diffusion pikes will be included. Rockwell International will provide data on the devices including resistivities, layer thicknesses, and specimen dimensions. Wafers at each doping density, but without devices, will be provided for calibration purposes.

A more detailed breakdown of the variations of the test diode array follows.

1. Doping density of high-resistance n-region (10^{14}, 10^{15}, 10^{16}, and 10^{17} atoms/cm^3).

2. Width of diode (constant length of n-region).

3. Positive and negative diffusion spikes of constant size on junction (constant length of n-region).

4. Size distribution of diffusion spikes on junction (constant device width, variable length of n-region).

5. Diffusion spikes on n+ - n interface (constant device width, variable length of n-region).

Design variations will be included in a module approximately 200 mils by 200 mils. This module will be repeated over a wafer that is 2 inches in diameter. Wafers will be made at the doping densities indicated in (1). One-third of each wafer will be retained by Rockwell International for reference.

1. Correlation of Current and Voltage Waveforms with Filament Configurations. The interpretation of second breakdown effects is facilitated by using constant current pulses. Where possible, constant current pulses will be applied and the current-time and voltage-time waveforms recorded and related to the filament configuration as revealed by the stroboscopic method. The voltage at first follows the current and then rises further because of the increase in resistivity with temperature. As filaments start to form, the voltage changes associated with the filamentation might be more readily distinguished. If the current pulse amplitude is increased slightly (keeping the pulse duration the same), the filaments appear earlier in the pulse. Thus, there is a systematic behavior that allows filament onset to be distinguished from other effects. Also, if the pulse length is changed and the amplitude suitably adjusted, the changes in the voltage waveform occur in a characteristic manner.

Waveform data should be taken with pulses sufficiently short to be representative of EMP effects. This is important for two reasons related to the goals of these investigations;

1. The number and location of current filaments has been shown to depend upon pulse duration under reverse bias conditions. EMP pulses and subsequent ringing effects have durations of a few tens of nanoseconds to about 1 μs. These are times short compared to the thermal time constant of silicon-on-sapphire devices. Thus heat conduction can be neglected for EMP effects in silicon-on-sapphire devices.

2. The configuration of filaments depends upon the thermal history of the system from the beginning of an excitation pulse. This thermal history, in turn, is sensitive to current crowding due to specimen geometry, diffusion spikes, metallization spikes and possibly other causes.

At present, data obtained by the stroboscopic method has covered the time regime of 5 μs to dc, with most data being obtained from parallel structured diodes about 500-μm wide. Smaller diodes showed the same effects as the larger but were more difficult to study because events occurred too rapidly. In such cases the current amplitude for damage was only slightly higher than that for current filamentation to begin. This

difference becomes less as resistivity increases, devices become smaller, and pulse width becomes smaller. For a screening test to be as safe as possible, the test pulse should be relatively long and of amplitude such that filaments just begin to form. If the filament that produces damage always occurs at the same position (which might be the case in small devices), then testing could be done, for example, with 100-μs pulses instead of 100-ns or shorter pulses. To develop the background information for a meaningful screening test seems to require study of filamentation geometry on devices of dimensions and geometries similar to those of practical devices using pulses comparable to EMP's and longer. Larger devices need to be available for study also because events that occur too rapidly to follow in detail in the small devices can be followed in the larger ones.

In the stroboscopic method a triggered air arc lamp is used as the light source. The light pulses have a peak power of about 50,000 W, a duration of 10 ns, and a jitter on triggering of about 1 μs. The jitter on triggering implies that dynamic processes cannot be followed if they occur on a time scale shorter than this jitter. Thus sequential events can be followed only for pulses of several microseconds' duration or longer. However, the long thermal time constant of the devices (several microseconds) allows the final filament configuration to be observed so long as the strobe light can be turned on within 1 μs of the end of the excitation pulse. This is possible even if the main pulse is in the submicrosecond regime. Thus the stroboscopic method is useful for the short pulses of interest in EMP effects.

In addition to requiring that the stroboscopic method yield final filament configurations for short exciting pulses, it is necessary to correlate these with current and voltage waveforms. With truly constant current pulses, the voltage waveform contains the data descriptive of the filamentation process. However, it is very difficult to form high-amplitude, short-duration constant current pulses. Hence, both current and voltage waveforms should be monitored. The onset of filamentation causes small changes in these waveforms. These changes are the positive indication that destruction (formation of a melt) due to second breakdown is imminent. The changes associated with filamentation tend to be masked by resistances within the device in series with the filaments. To provide a background for screening tests requires a study of the pulse waveforms extending from a few tens of nanoseconds duration to, perhaps, 100-μsec duration. Differentiation of the voltage and current waveforms might yield a better indication of the onset of filamentation than either waveform alone. The product of the voltage and current waveforms yields the instantaneous power waveforms. This or its derivative might be still more informative in producing the desired information.

Analysis of the experiments will include qualitative judgments on the importance of geometric arrangement and role of diffusion and metallization spikes. Device waveforms will be related to junction heating, heating of the high-resistance region and filamentation by mathematically modeling the systems. Recommendations will be made on screening tests and device design.

Instrumentation now exists in the form of the Tektronix Digital Waveform Instrument (DWI) system that allows single pulse events of 5-ns to 100-μs duration to be recorded and subsequently processed.

2. Temperature-Position-Time Mapping. The stroboscopic method allows temperature mappings over the face of an SOS device at any time during or after application of the exciting current pulses. Qualitative data can be readily obtained by photographic means. However, quantitative data are much more difficult to obtain. The basis for temperature measurements is that the temperature of the silicon film strongly influences its transmissivity to light. Thus the fraction of light transmitted can be related, upon a suitable calibration, to the temperature of the device.

The light source for the stroboscobic measurements is an air arc. This arc does not produce pulses of light of constant intensity. Thus the transmitted intensity from a single pulse cannot be used as a measure of temperature. The average of a large number of pulses does give a valid representation of the transmissivity and hence of the temperature. However, to obtain the average of hundreds of pulses requires a multichannel analyzer and is a slow and tedious operation.

An alternative measuring scheme is to split the incident light pulse, using one portion as a reference beam and passing the other through the specimen. The ratio of transmitted to reference beam measures the temperature. To obtain a temperature profile requires making repeated measurements as the specimen is scanned. To properly characterize a single filament configuration requires repetition of the entire process for different positions of the strobe light relative to the leading edge of the exciting current pulse. Hundreds to thousands of readings are required for carrying out such a mapping for pulses of specific amplitude and duration.

The Tektronix DWI system offers the capability for analyzing the reference and transmitted beams. If two digitizers are used, then both beams can be recorded simultaneously. However, by using a delay on one pulse, the two pulses could be added and displayed together, thus using only one digitizer unit. The processing unit could

sense the peak amplitudes of each pulse and record their ratio. If a suitable stepping arrangement is made, the entire scanning process can be automated and mapping becomes relatively easy to do.

Temperature-position-time mappings, along with voltage and current waveforms and device parameters, will provide a valuable data base for modeling the filamentation process.

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3. DESIGN CONSIDERATIONS FOR OVERSTRESS TESTING OF SOS DIODES*

A. OBJECTIVES

The general objectives of the experimental work are to enhance the capability to observe second breakdown due to short pulses by modifying an existing technique for longer pulses, to detect the onset of filamentation by external electrical means, and to map the temperature distribution in the junction depletion region of an SOS diode.

B. SPECIFIC TASKS

First it was necessary to design a pulsed, constant-current drive source for second breakdown tests of silicon-on-sapphire diodes, compatible with specifications on source and test specimens. The arrangement previously used for observing current filamentation and voltage and current waveforms is shown in *Figures 1* and *2* (*Figures 12* and *9*, respectively, of *Reference 1*). The arrangement worked very dependably for constant current pulses between 10 μs and 10 ms and for relatively large test devices (with major dimensions of 75 μm and 500 μm). However, in the forthcoming study, the method is to be applied in a shorter time regime (100 ns to 10 μs) to devices that have major dimensions from 10 μm to 500 μm and important device features 1 μm in size. The new conditions impose additional requirements on most portions of the system.

The light source currently employed is a triggerable Xenon Corporation air arc lamp operated at atmospheric pressure. The lamp is excited with a 10 kV pulse having a rise time of 3 μs, the lamp firing on the leading edge at about 6 kV. The exact firing voltage varies from pulse to pulse. Because of the variations in the firing voltage, there is a jitter in the time of firing relative to the triggering pulse of about 1 μs. Further, there is a corresponding fluctuation in the light intensity, with arcs firing at higher voltage producing greater light intensities. The Xenon Corporation, manufacturer of the arc sources, produces two lamps with widths at half maximum intensity of 10 ns and 20 ns. Both fire on the leading edge of the 10 kV excitation pulse. According to a representative of Xenon, the jitter in the triggering can be reduced to about 10 ns by using a 10 kV pulse with a 50 ns rise time.

Xenon Corporation does not manufacture a power supply that rises from 0 to 10 kV in 50 ns. However, Pulsar Associates, Inc., produces Pulspak 10A, a triggered high

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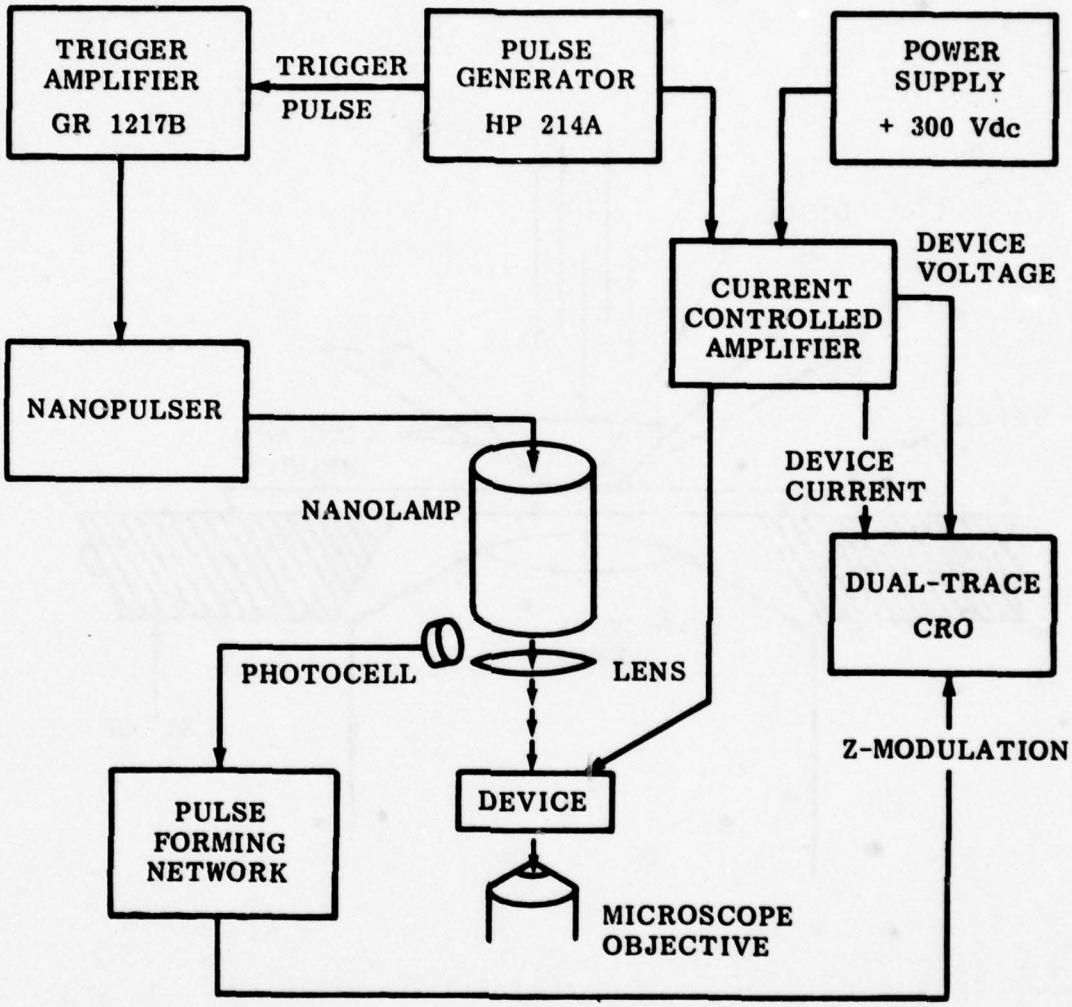


Figure 1. Block diagram of the apparatus for stroboscopic observations of optical transmission patterns of silicon-on-sapphire devices under electrical stress.

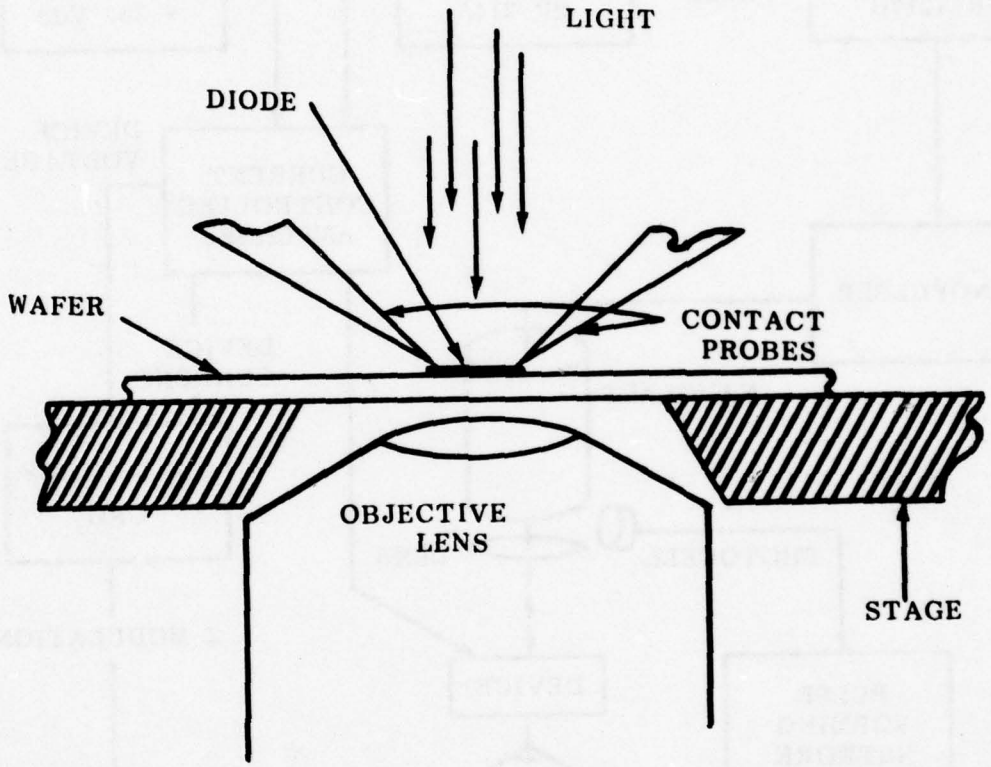


Figure 2. A silicon-on-sapphire diode in position for observation of second breakdown phenomena. The wafer, probes and stage are moved as a unit to select the area of observation.

voltage generator with a maximum repetition rate of 10 pps. The pulses have a rise time of 10 ns, 10 kV peak, 1 ns command jitter and 70 ns throughput delay. Each pulse provides about 0.2 J. The energy discharged in a single pulse of the Xenon Nanolamp is approximately 0.1 J.

With Pulspak 10A Precision High Voltage Pulse Generator and the Xenon Corporation Nanolamp, stroboscopic measurements can be made during the 100 ns pulses.

The small size of the devices to be studied and the anticipated smallness of the current filaments requires the use of an inverted microscope high-quality optics, since the devices under study must be viewed through their 10-mil sapphire substrates. Transmitted light objectives for microscopes are corrected for the presence of a cover glass, whereas reflected light objectives are not given this correction. Thus for best resolution, transmitted light objectives should be used. To cover the device sizes of interest, two objectives are required: 16× (N.A. 0.25) and 40× (N.A. 0.45), along with a condenser system. All components, including a suitable mounting carrier, are associated with a Reichert MEF metallograph.

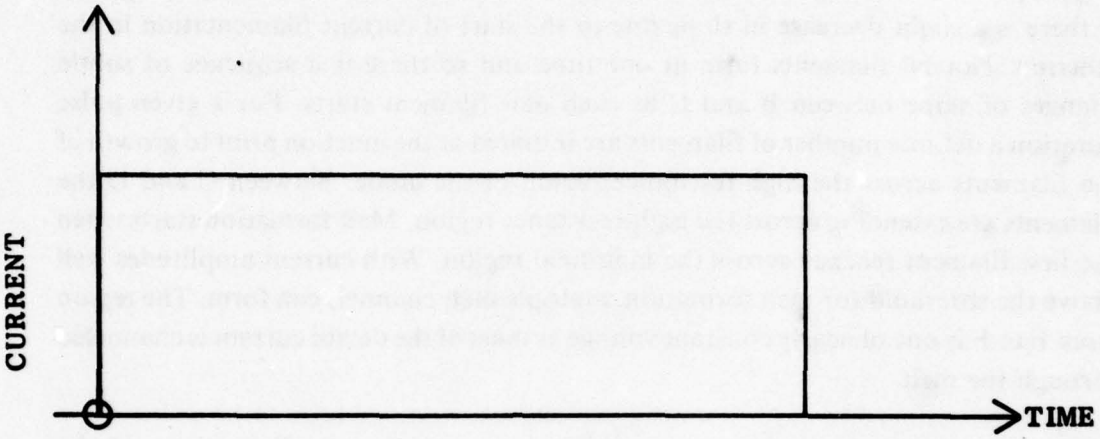
The actual firing time of the strobe light relative to the leading edge of a current pulse is determined by receiving the flash of the strobe light on a photodiode, shaping the output pulse and superimposing this pulse on the cathode-ray display of the current and voltage waveforms. Since fast photodiodes are available and the light signal is large, this marker pulse does not appear to present any fundamental problem.

The arrangement for obtaining a constant current pulse in the range of 5 μs to 10 ms was to use a Hewlett-Packard Model 214A pulser for the primary signal and a 2N3585 transistor with a 300-V power supply as a current controlled amplifier. The Model 214A pulser can produce 50 ns pulses with a rise time of 10 ns. The 2N3585 transistor has ratings P_{max} = 35 W, BV_{cbo} = 500 V, BV_{ebo} = 6 V, BV_{ceo} = 300 V, and f_{ae} = 10 MHz. For constant current pulses of 100 μs duration, the maximum voltage prior to destructive second breakdown for 0.064 Ω-cm diodes was about 100 V. In transistor studies of second breakdown with pulses of a few nanoseconds duration, voltages in the kV range are required. The PT 7959 silicon npn power transistor has ratings P_{max} = 80 W, BV_{cbo} = 325 V, BV_{ebo} = 6 V, BV_{ceo} = 300 V, and f_{ae} = 100 MHz. With this transistor and the Model 214A pulser, constant current pulses of sufficient amplitude to produce second breakdown for pulse durations of 1 to 10 μs should be obtainable.

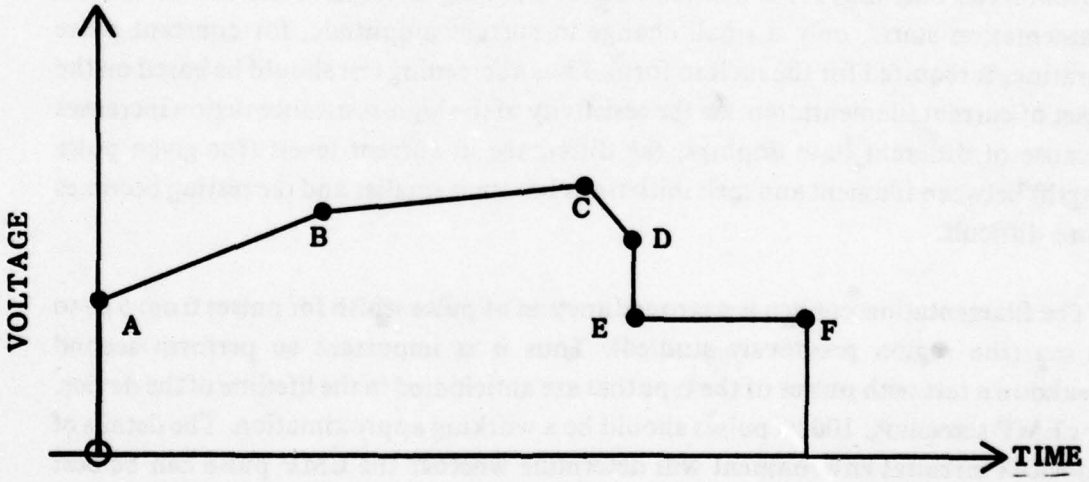
If the Model 214A pulser is used to control a beam power tube, then constant current pulses of several amperes with voltages in the kV range could be obtained. Since pulses of short duration are required, the main power supply would have to deliver only enough current to charge a capacitance of about 0.1 μF while the capacitor is supplying energy to the circuit at a pulse rate of 10 pps. The tube can be biased so that it is cut off except when the exciting pulse is applied. Thus the demands on the high-voltage supply are modest; a 5-mA, 5-kV supply should be more than adequate.

The Cober or Veloni pulsers have both the voltage and current capability for producing second breakdown with pulses of 100 ns to 10 μs. These pulsers approximate constant impedance, constant voltage sources. Our previous studies were performed with constant current pulses because diode voltage is a single valued function of current during the events leading to second breakdown. With constant current pulses, a stable filamentation pattern was obtained for a given pulse length. When double-step testing was done, with each step constrained to be at constant current [2], the filamentation pattern changed from that characteristic of the first step to that characteristic of the second with a transition time of several microseconds (the thermal time constant of the devices were several microseconds). A constant voltage pulse can be thought of as a sequence of constant current steps, each one being characterized by the device impedance level. If this impedance level does not change too much, then a stable filamentation pattern will occur. The devices to be supplied by Rockwell International will be of about half the thickness of the devices previously studied. Thus they will have a somewhat smaller thermal time constant — one about 1 μs. The time regime of 100 ns to 1 μs is less than the thermal time constant in these devices. Hence, the filamentation pattern, once it is started, will be unable to change appreciably due to heat flow. Both constant voltage and constant current testing will be done in the short time regime and the filamentation patterns compared.

A test technique for external detection of the onset of filamentation, such as a slope detector for rate of change of voltage at constant current, would be highly desirable as a screening technique. The following are some considerations in the experimental design of such a technique. In constant current testing the voltage waveform measures the impedance history of the device as heating and current filamentation occur. The principal features that distinguish the voltage waveform when destructive second breakdown occurs during the pulse are shown in *Figure 3b* for the current waveform of *Figure 3a*. The voltage jumps abruptly from zero to V_A during the rise time of the current pulse. The current and voltage at point A are



(a)



(b)

Figure 3. (a) Constant current pulse of amplitude sufficient for producing destructive second breakdown. (b) Corresponding voltage pulse.

characteristic of the device at its ambient temperature. The voltage is the sum of the junction voltage and the series IR drops in the device. A further rise in voltage occurs in the interval from A to B to C, due primarily to the heating of the n-region, although a small portion is associated with the increase in junction voltage with temperature. At B there is a slight decrease in slope due to the start of current filamentation in the junction. Not all filaments form at one time and so there is a sequence of subtle changes of slope between B and C as each new filament starts. For a given pulse duration a definite number of filaments are initiated at the junction prior to growth of the filaments across the high-resistance region of the diode. Between C and D the filaments are extending across the high-resistance region. Melt formation starts when the first filament reaches across the high field region. With current amplitudes well above the threshold for melt formation, multiple melt channels can form. The region from E to F is one of nearly constant voltage as most of the device current is channeled through the melt.

When current pulses of lower amplitude are applied, not all portions of the waveform of *Figure 3b* will occur because of termination of the pulse. Thus at low-current levels only the A to B portion will occur, at higher levels A to B to C, etc. Once filamentation starts, only a small change in current amplitude, for constant pulse duration, is required for the melt to form. Thus a screening test should be based on the onset of current filamentation. As the resistivity of the high-resistance region increases because of different base dopings, the difference in current levels (for given pulse length) between filament and melt initiations becomes smaller and the testing becomes more difficult.

The filamentation pattern is a strong function of pulse width for pulses from 5 μs to 10 ms (the region previously studied). Thus it is important to perform second breakdown test with pulses of the type that are anticipated in the lifetime of the device. For EMP screening, 100 ns pulses should be a working approximati n. The details of a device's circuital environment will determine whether the EMP pulse can be best represented by a constant-voltage pulse or a constant-current pulse. Hence the proposed studies should include tests by both types of excitations. When this is done along with the stroboscopic tests, the locations of the filaments will be correlated with each of the waveforms.

Tests should be done over a range of pulse lengths so that the filamentation patterns are determined and correlated with waveforms. Filament geometry in the previously studied SOS diodes was insensitive to microscopic junction irregularities. Thus once

the spacing between filaments is less than that of a critical device dimension (diode width, length of n-region, or other geometric parameter), tests at short pulses may be simply correlated to tests at longer pulses. Screening tests could then be performed with the longer pulses if this simplified test instrumentation.

As each filament forms, it produces a small change in slope of the voltage waveform. For long pulses there are fewer filaments and their times of formation are more widely separated than with shorter pulses. Thus the detection of filamentation in the voltage waveform becomes increasingly subtle as the pulse length decreases. The previous data suggest that the distance between filaments will be 3 μm for 100 ns pulses and each filament will have a width of about 1 μm. A device with a width of 50 μm will thus contain about 15 filaments, while a device of 500 μm width will have about 150 filaments. If the excitation pulse amplitude is chosen carefully, then the filaments will be initiated during a large portion of a single pulse. However, the current through each filament changes as the pulse continues, so the change of voltage due to a new filament is subtle.

The Tektronix Digital Waveform Instrument (DWI) allows a single pulse as short as 5 ns to be recorded and its amplitude sampled 512 times. Thus, for 100 ns pulses, sampling is done at 0.2 ns intervals. If details in this time regime are to be resolved, then the external circuit must be carefully set up to minimize lead inductance and external noise. The DWI has a waveform processing unit that can be programmed to differentiate the waveforms to emphasize the changes in slope, compute power versus time, the derivative of power with respect to time, and other modes of signal processing.

Thermal mapping of SOS diodes during the filamentation process was demonstrated in our previous studies [2]. However, the technique employed was very tedious, with several days of work required for a single scan and subsequent data analysis. The optical arrangement, shown in *Figure 4* (*Figure 31* of *Reference 1*), was the same as for other stroboscopic measurements except for the mode of recording. Instead of recording by photographic means, the transmitted light through a small region of the specimen caused by each strobing pulse was recorded by a photomultiplier tube. To delineate light from a small region of the specimen, only that light passing through a small aperture in the film plane of the camera was allowed to enter the photomultiplier. The aperture was centered on the optic axis of the microscope and different portions of the specimen were examined by moving the specimen across the stage of the microscope. The measurements were complicated by

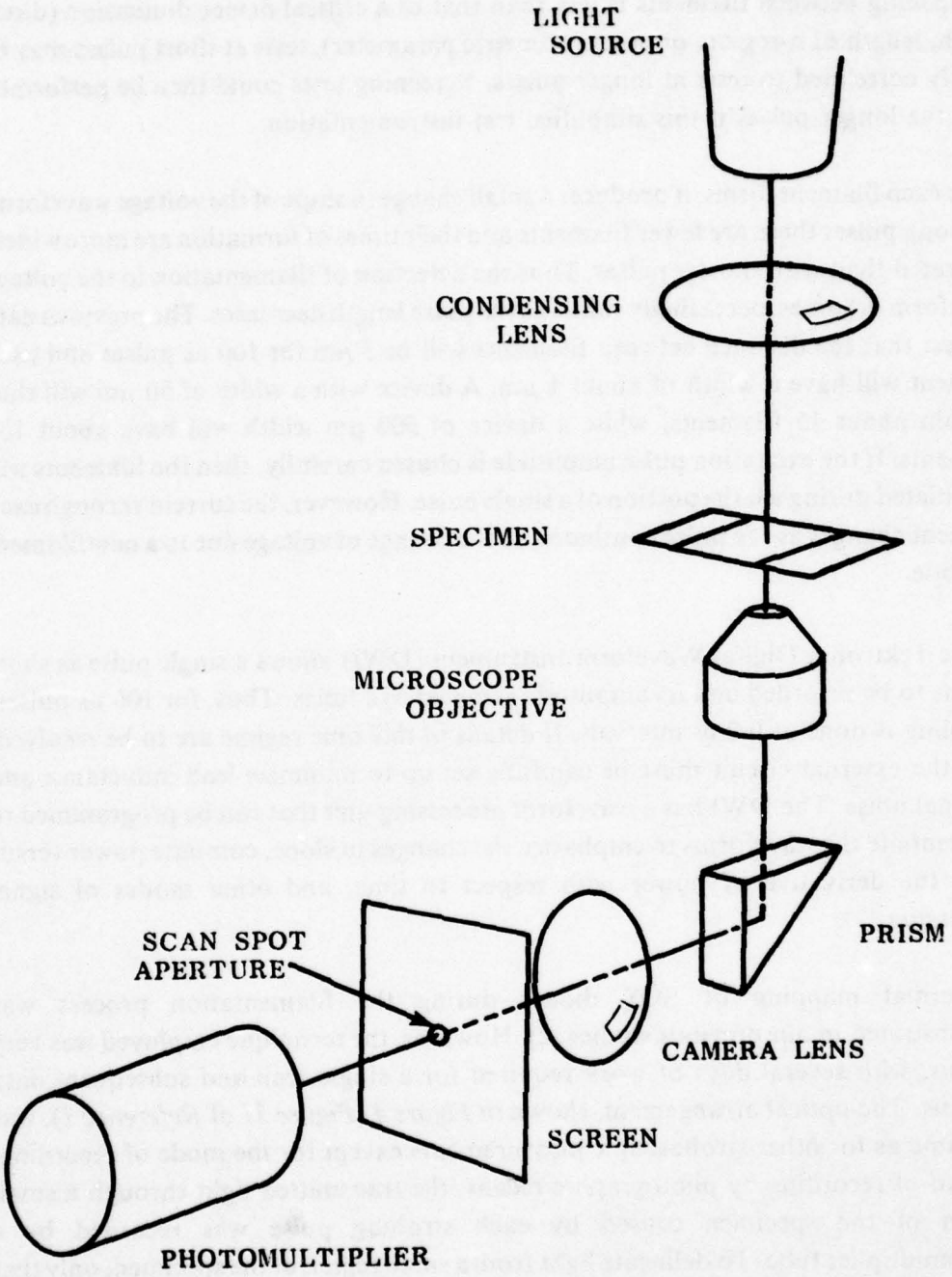


Figure 4. Schematic layout of apparatus for making direct measurements of thermal distributions on thin film silicon-on-sapphire devices.

the fact that the transmitted light for a single strobing pulse depended not only on the local temperature of the test specimen but also on the intensity of the incident light. Tests on the intensity of the incident light revealed a broad, asymmetric distribution. Thus it was necessary to measure the transmitted intensity of large numbers of pulses (about 10^3), record each pulse height on a multichannel analyzer, and compute the average pulse height for the distribution. After each such set of data the stage was translated with a micrometer movement to the next position and the procedure was repeated. The spatial resolution achieved was about 10 μm. Spatial resolution was limited by the size of the aperture opening. This size was selected as a compromise between the desire for good resolution and that of measuring the small transmittances that occur at high temperatures.

The Tektronix DWI provides the capability for a much more efficient experiment. The signal averaging technique used previously will not be employed. Rather, each strobe pulse will be divided into a reference beam and a working beam. The reference beam will be taken directly from the strobe source without passing through the specimen. The working beam will go through the specimen and the aperture in the film plane. A photodiode will be used to detect the reference beam and a photomultiplier the working beam. Each beam will go to one of the Model 7912 Waveform Digitizers of the DWI system. The processing unit will be programmed to measure the ratio of the peaks of the two pulses.

The SOS diodes in the current tests will have a thickness of about 0.6 μm compared to a thickness of 1.2 μm of the diodes previously studied. This will extend the measurable temperature range because the absorption coefficient at a given temperature will now be half of what it was previously. A stepping motor will be connected to the micrometer screw and geared so that each step will correspond to a device displacement of about 1 μm. With the new optical system, a resolution of about 0.6 μm is possible. To provide a check against spurious responses, 10 strobe flashes will be made at a single positon and their average used to describe the transmittance of that position. Their standard deviations will also provide some perspective on reproducibility of the entire system. Conversion of transmittance to temperature is done by means of a special calibration arrangement.

A calibration cell has been constructed and is shown in *Figure 5* (*Figure 2* of *Reference 1*). Dry nitrogen is heated by bunsen burner or a torch and the gases flood the region about the specimen being calibrated. Temperature is measured by a thermocouple mounted with its junction close to the specimen and in the gas stream.

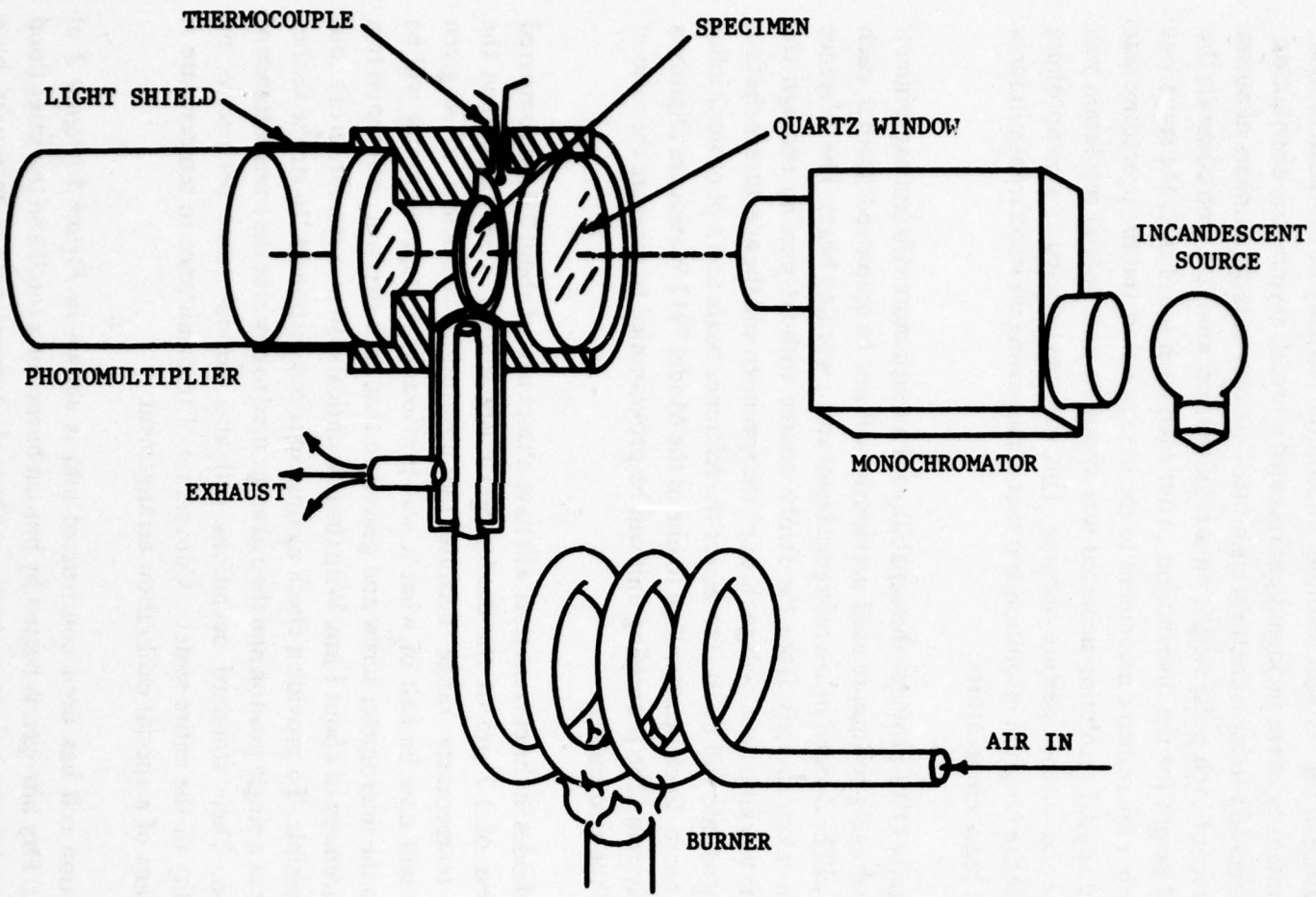


Figure 5. Experimental apparatus for determining optical transmissivity of thin silicon films as a function of temperature (shown schematically).

The devices being fabricated by Rockwell will be on wafers containing silicon epitaxial layers grown at the same time. One of the wafers will be cut by Rockwell into pieces 1 cm by 1 cm for calibration purposes. All of the wafers will originally have the same base doping of about 10^{14} atoms/cm^3. To obtain the different base dopings for the range of devices to be prepared, individual wafers are given an ion implant to the desired doping density. As each wafer is given its implant, a calibration wafer will accompany it and receive the same implant. Hence, the calibration wafers will be as close to the device wafers in physical characteristics as is possible.

The line of the scan will be positioned by manually controlling a second micrometer. In a particular test sequence, a single line would be scanned repeatedly with the same current pulse but with different positions of the strobe light relative to the onset of the current pulses. Tests would also be done for a range of pulse lengths and amplitudes. Characterization of a single device would entail hundreds of scans.

An important aspect of the temperature profile studies will be to take stroboscopic photographs for each scan condition: pulse duration, pulse amplitude, and strobe light position.

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1. Budenstein, P. P.; Pontius, D. H.; and Smith, W. B. *Second Breakdown and Damage in Semiconductor Junction Devices*. Technical Report No. RG-TR-72-15 (AD 740226), US Army Missile Command, Redstone Arsenal, Alabama, 1972.

2. Baruah, A.; Budenstein, P. P.; Pontius, D. H. and Smith, W. B. *Second Breakdown in the Presence of Intense Ionizing Radiation*. Technical Report No. RG-75-24, US Army Missile Command, Redstone Arsenal, Alabama, 1974.

4. DESIGNING SOS DIODES FOR SECOND BREAKDOWN RESEARCH*

The Rockwell International contribution to the second breakdown studies of the electrical overstress program has been to design the chip, fabricate the design-checkout wafer lots and characterize the SOS devices. These efforts have resulted in the chip shown in *Figure 1*.

An outline of the SOS Electrical Overstress Processing Steps used to fabricate this chip is sequentially listed in *Table 1*. *Figures 2a* and *2b* show this Si-Gate CMOS/SOS process in a more detailed pictorial form. It should be noted that, following step L, a doped silox passivation layer is deposited and the pad areas are etched for electrical contacts.

Devices were fabricated on sapphire wafers polished on both sides to meet the optical transmissivity requirements of the stroboscopic experiments to be performed at Auburn University. With both sides of the wafer polished, it is difficult to determine by cursory visual inspection which is the epi side. To eliminate this problem a second half-size flat was ground on the wafers (*Figure 3*). Test-device design variations contained within the chip reflect electrical-overstress-induced device failure threshold considerations as related to (1) inherent silicon properties, (2) fabrication methods and (3) quality control. These considerations are applied to simulated bipolar devices fabricated on SOS substrates.

To provide an experimental control, the "defect-free" Standard Reference Structures described in *Table 2* and *Figure 4* were designed. The range of lengths of the n region was selected to represent the smaller geometry devices (10 microns at one end) to a length sufficient to prevent punch-through at the test pulse biases (500 microns at the long end). Diode widths range from 1.2 mils (the narrowest) up to 20 mils (the largest device). The 20 mil diode was included to provide continuity with previous tests performed at Auburn University. The 8 mil diode represents the standard width device on the chip.

Geometric edge effects on hot-spot nucleation will be studied by including a set of Enclosed Reference Structure devices (*Figure 5*) of the same dimensions (*Table 3*) as the Standard Reference Structures.

*L. G. Green and D. H. Phillips, Rockwell International.

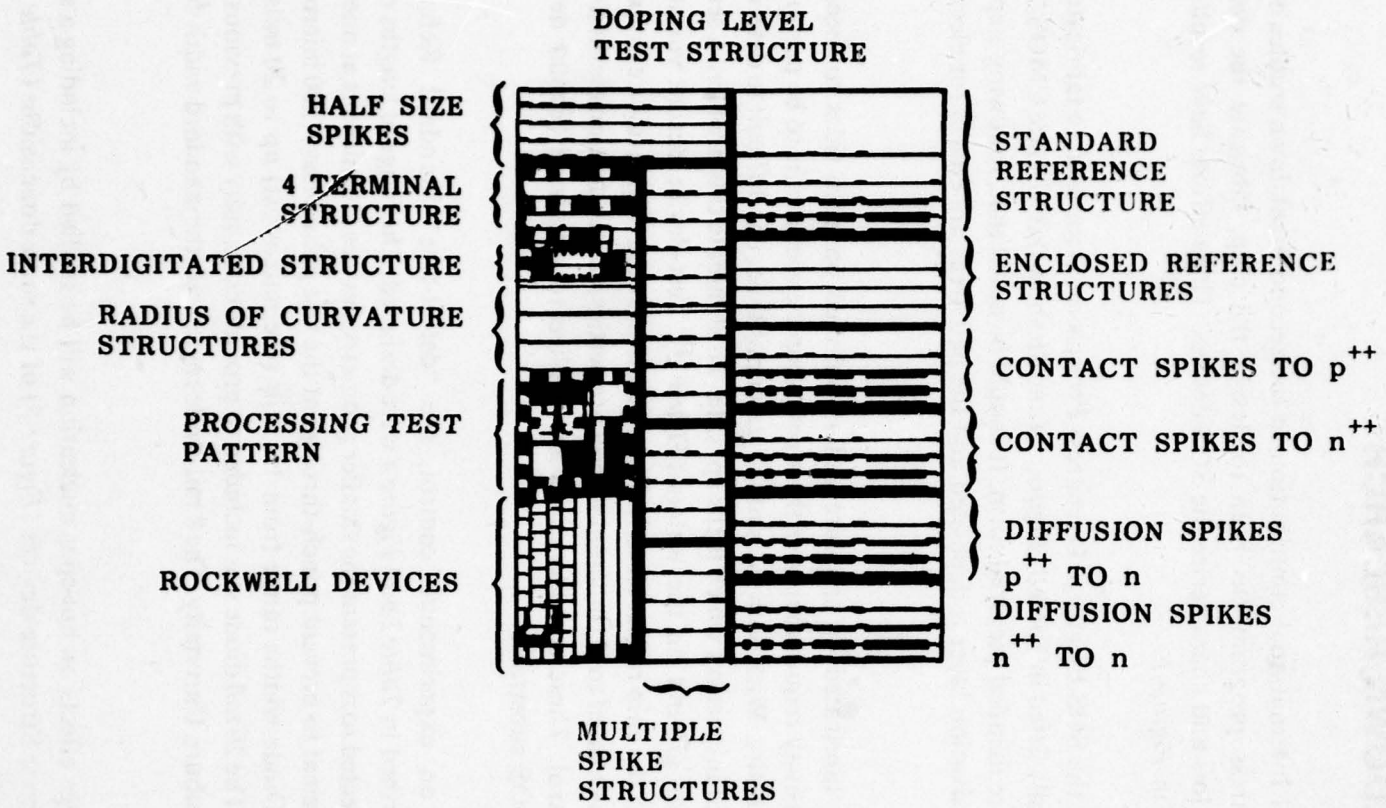


Figure 1. Photograph of the SOS diode chip, showing the array of test devices.

TABLE 1. SOS Electrical Overstress Processing Steps.

- N^- IMPLANT WAFER
- P IMPLANT WAFER
- ETCH ISLANDS
- P^{++} DIFFUSION
- N^{++} DIFFUSION
- GATE OXIDE
- POLY GATES
- EXTENDED DRAIN IMPLANTS

} FOR TEST TRANSISTORS ONLY

- CONTACT OPENING
- METALLIZATION AND ETCH
- SILOX
- PAD OPENING

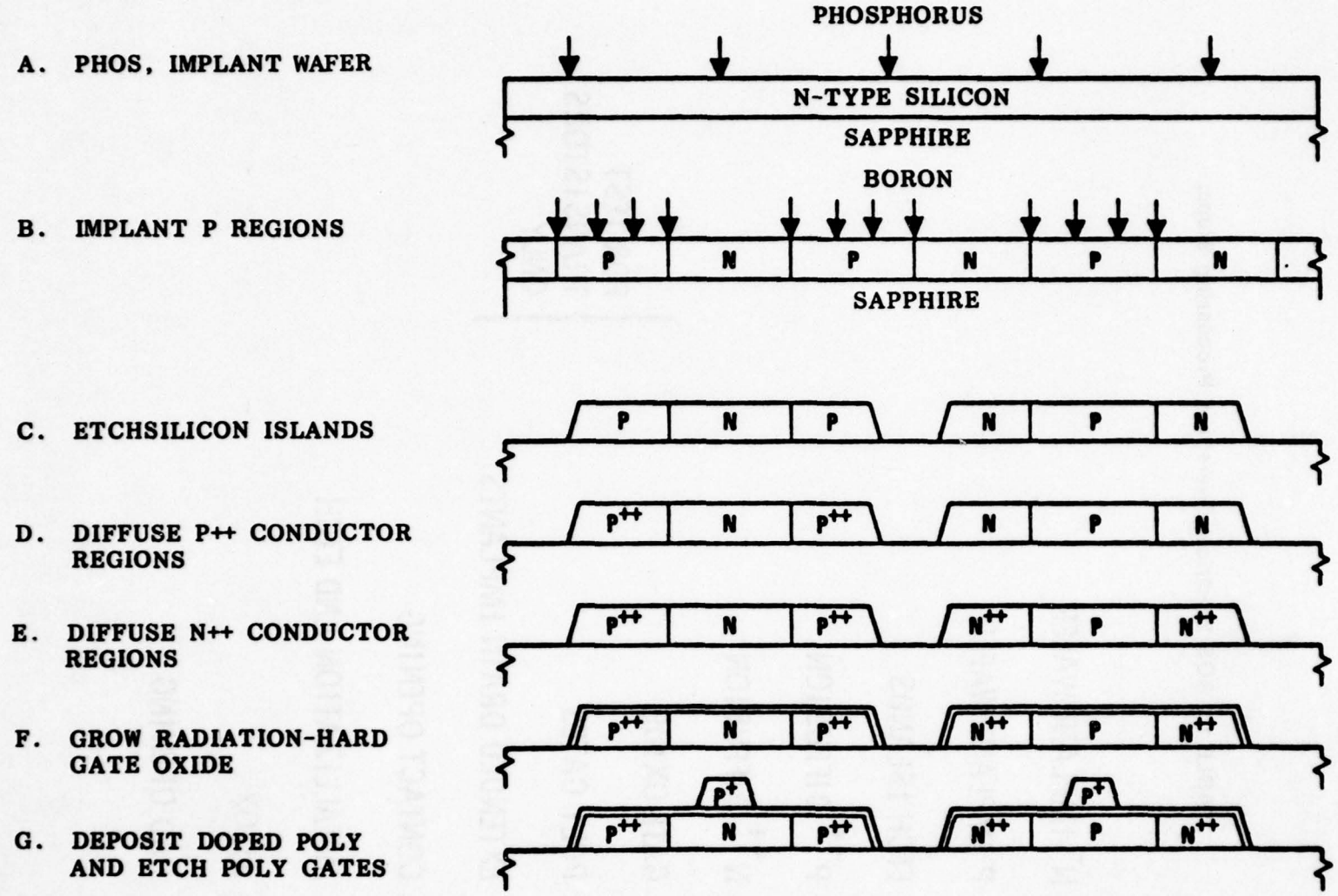


Figure 2a. SI-gate CMOS/SOS process.

H. IMPLANT P-CHANNEL SOURCE-DRAIN AREAS

I. IMPLANT N-CHANNEL SOURCE-DRAIN AREAS

J. DEPOSIT CVD OXIDE AND ACTIVATE IMPLANTS

K. ETCH CONTACTS

L. DEPOSIT AND ETCH METAL

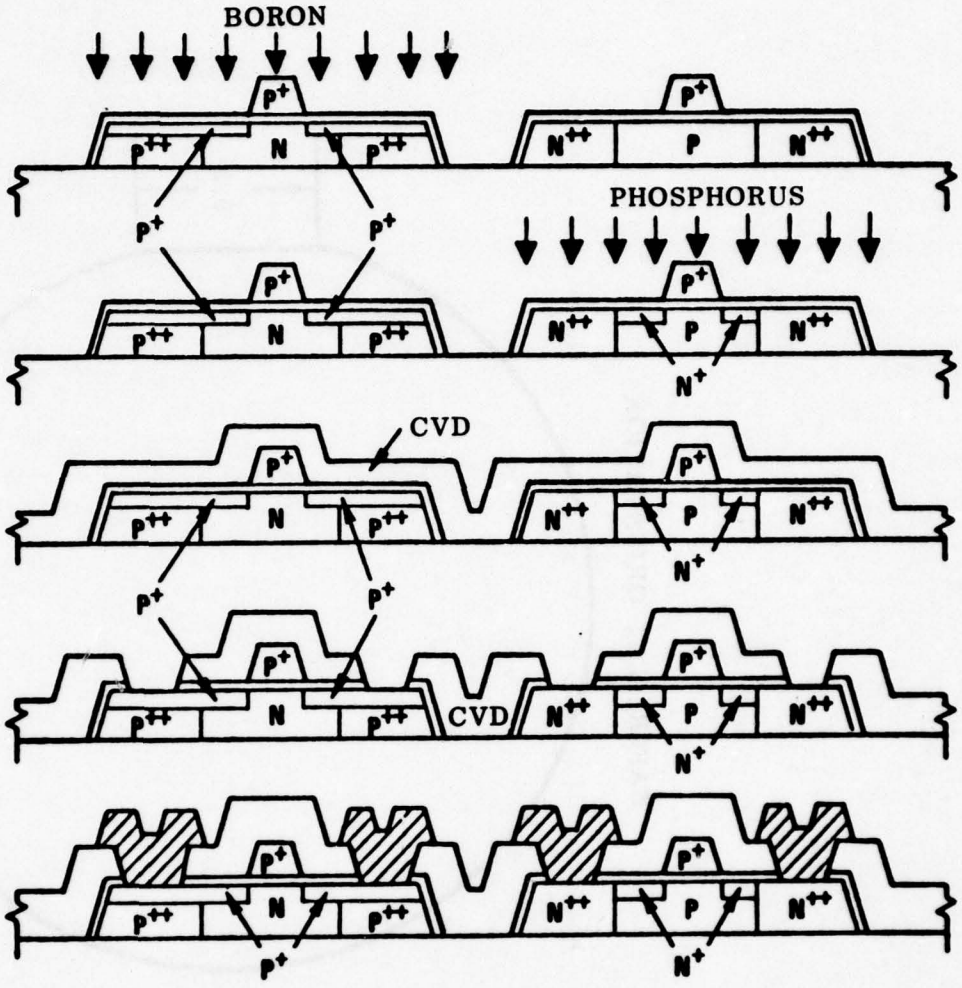


Figure 2b. S_I-gate CMOS/SOS process (continued).

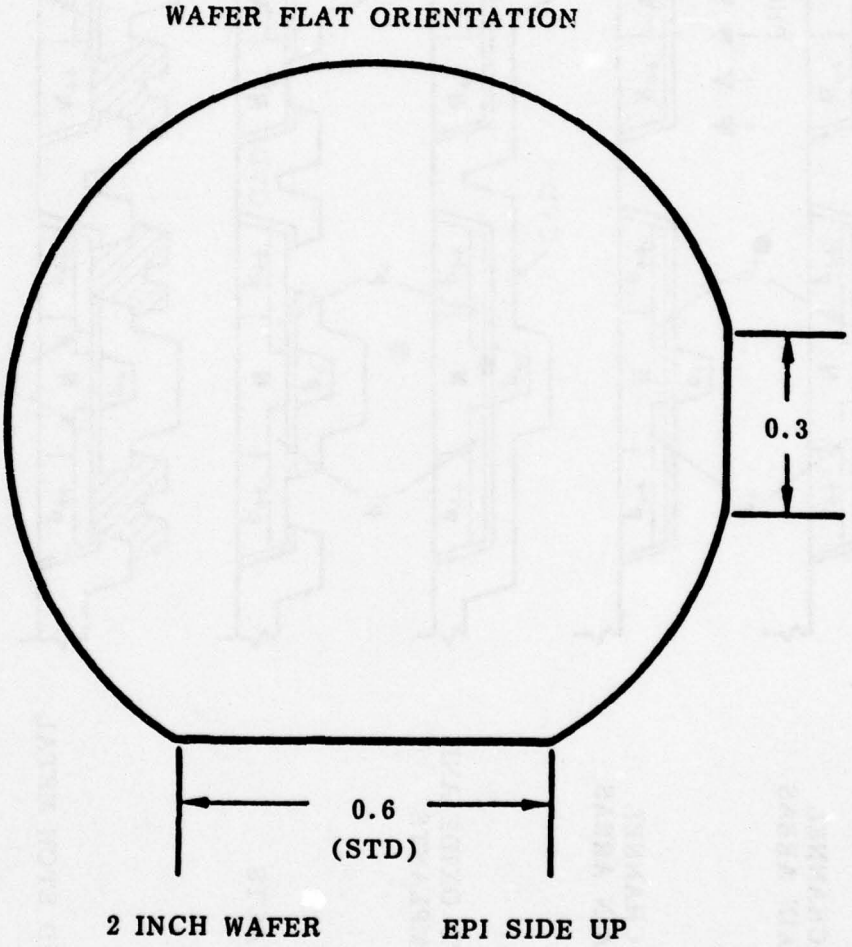


Figure 3. SOS electrical overstress program.

TABLE 2. Standard Reference Structures.

- 25 DEVICES
- N-TYPE CONTROLLED DOPING REGION (α_E) LENGTH
  - 10 μ
  - 30 μ
  - 100 μ
  - 300 μ
  - 500 μ
- BASIC REFERENCE STRUCTURE WIDTH
  - 20 MILS
  - 8 MILS
  - 4 MILS
  - 2 MILS
  - 1.2 MILS

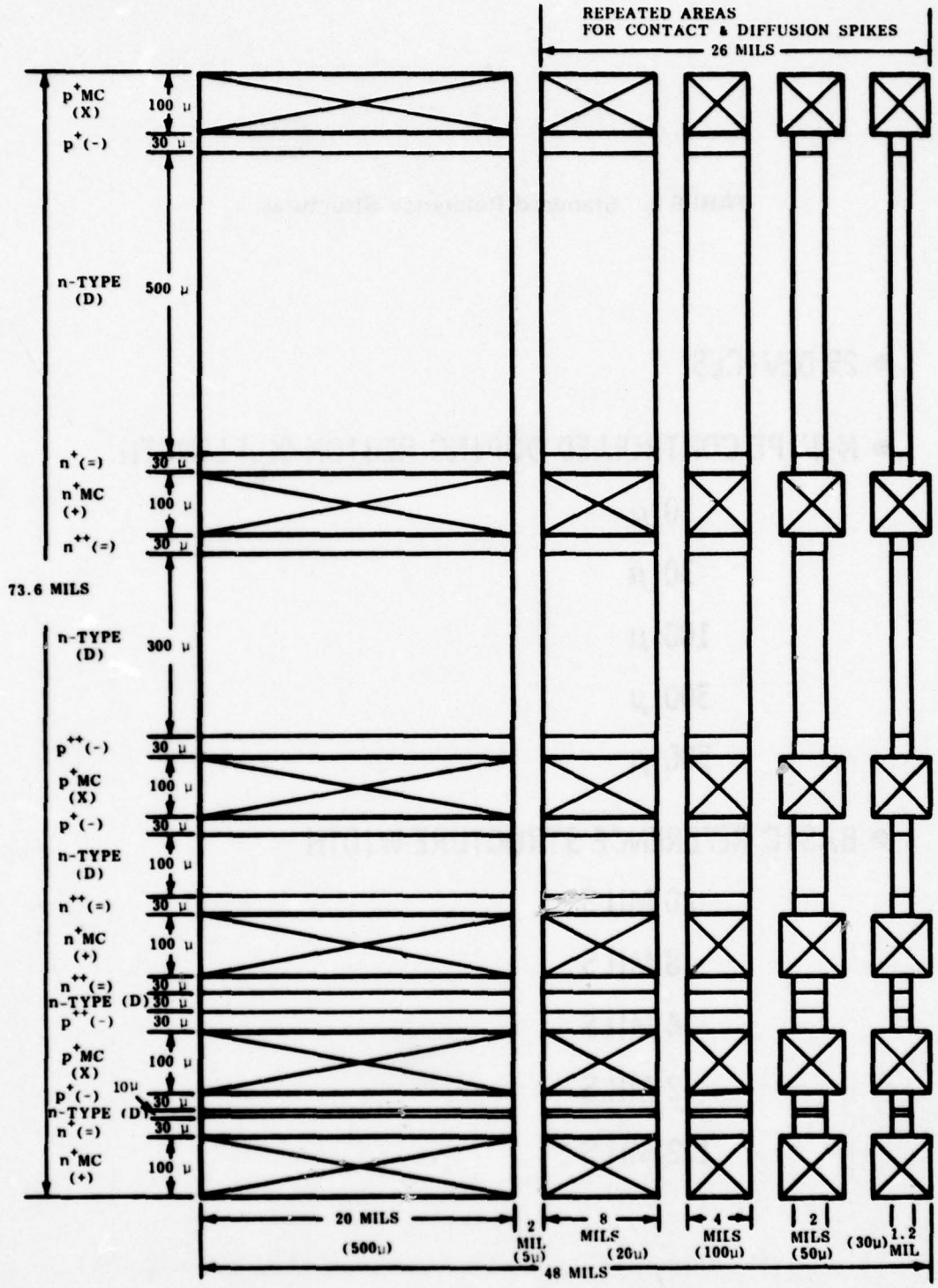
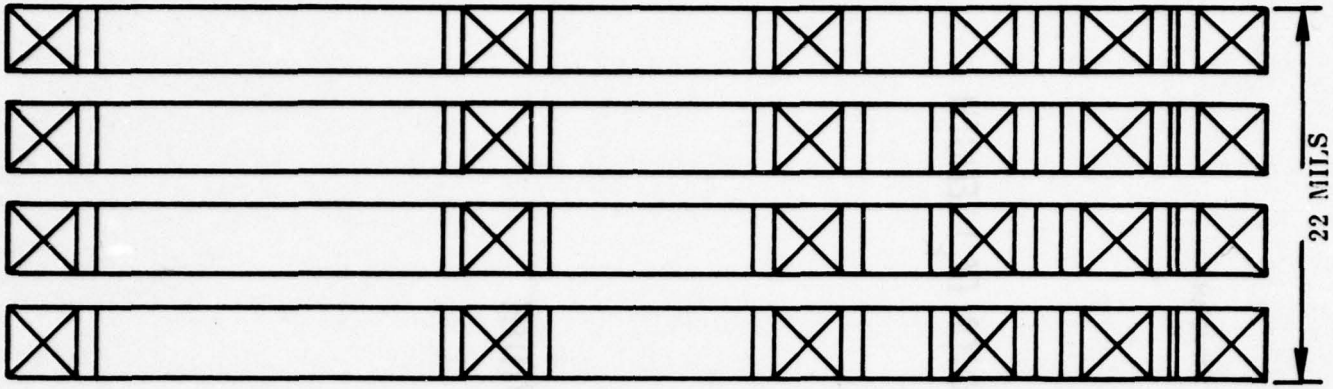
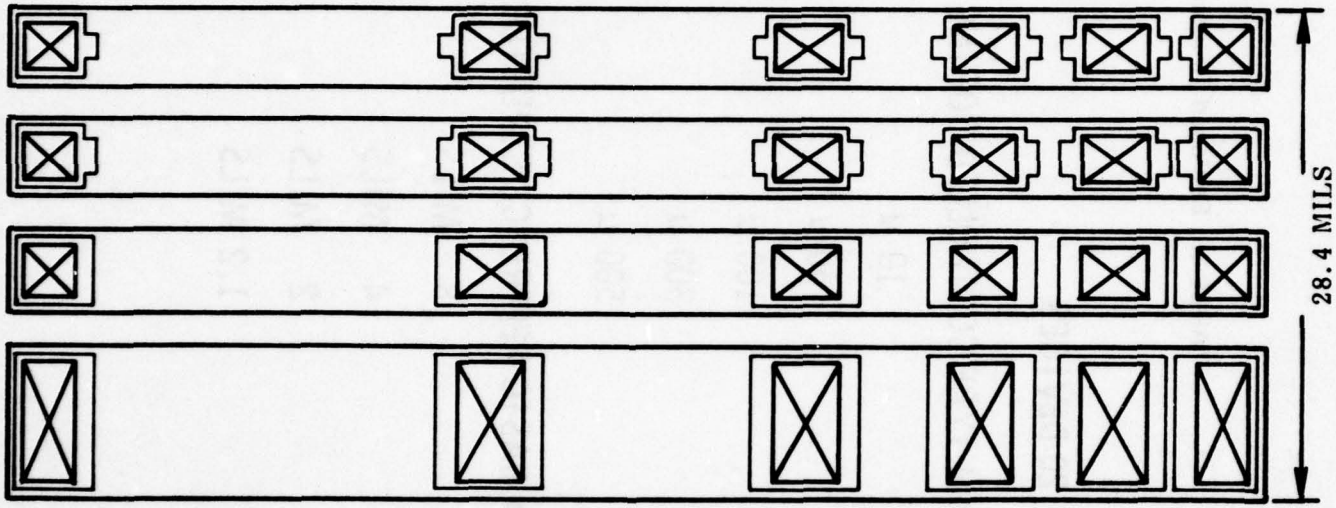


Figure. 4. Standard reference structures.



HALF SIZE SPIKE STRUCTURES



ENCLOSED REFERENCE STRUCTURES

Figure 5. Enclosed and half-size structures.

TABLE 3. Enclosed Reference Structure.

- 20 DEVICES
- N-TYPE CONTROLLED DOPING REGION (X_E) LENGTH
  - 10 μ
  - 30 μ
  - 100 μ
  - 300 μ
  - 500 μ
- BASIC REFERENCE STRUCTURE WIDTH
  - 8 MILS
  - 4 MILS
  - 2 MILS
  - 1.2 MILS

Fabrication problems resulting in metal contact spikes extending into the diffused regions or diffusion spikes extending from one diffused region into another may affect second breakdown initiation. Eighty single-spike devices as described in *Table 4* will be included on the Standard Reference Structure type of diodes in *Figure 4* to study their effects in this regard. An attempt to determine the effects of spike size will be implemented by including a set of one-half size spikes on 20 devices as described in *Table 5* and *Figure 5*. Finally, a set of diodes containing multiple spikes in combination as shown in *Figure 6* will be arranged according to the descriptions of *Table 6* and *Figure 7*. The 1 micron sawtooth edge is included to represent a nonsmooth p-n junction or metal edge. Larger spikes are placed in areas where hot-spot nucleations probably would not normally occur.

Substrate doping level plays an important role in second breakdown effects. To evaluate this effect, wafers of five different substrate implant levels were processed. A test structure to measure these levels is described in *Table 7* and *Figure 8*.

How does the sharpness of points of prominence such as the cross-sectional edge of emitter-base diffusions affect the location of hot-spot nucleation? Nine devices of varying radii of curvature as listed in *Table 8* and of the configuration in *Figure 9* are included to provide data to answer this question.

The effects of crosscurrents in the n regions of the diodes on nucleation formations will be studied using the Four-Terminal Structure (*Figure 10*).

Finally, a simulated cross-section of an interdigitated device is provided to study lateral junction effects on nucleations. The variations included in this device are listed in *Table 9*. Device layout is shown in *Figure 11*.

TABLE 4. Contact/Diffusion Spike Structures.

- 80 DEVICES
- N-TYPE CONTROLLED DOPING REGION (X_E) LENGTH

  10 μ
  30 μ
  100 μ
  300 μ
  500 μ

- BASIC STRUCTURE WIDTH

  8 MILS
  4 MILS
  2 MILS
  1.2 MILS

- SPIKE LENGTHS — LOCATION

  5 μ — 1/4 DISTANCE FROM LEFT-HAND ISLAND EDGE

- SPIKE DIRECTION

  N^{++} CONTACT ⟶ N-TYPE
  P^{++} CONTACT ⟶ N-TYPE
  N^{++} DIFFUSION ⟶ N-TYPE
  P^{++} DIFFUSION ⟶ N-TYPE

TABLE 5. Half-Size Spike Structure.

- 20 DEVICES
- N-TYPE CONTROLLED DOPING REGION (X_E) LENGTH

  10 μ
  30 μ
  100 μ
  300 μ
  500 μ

- BASIC STRUCTURE WIDTH

  4 MILS

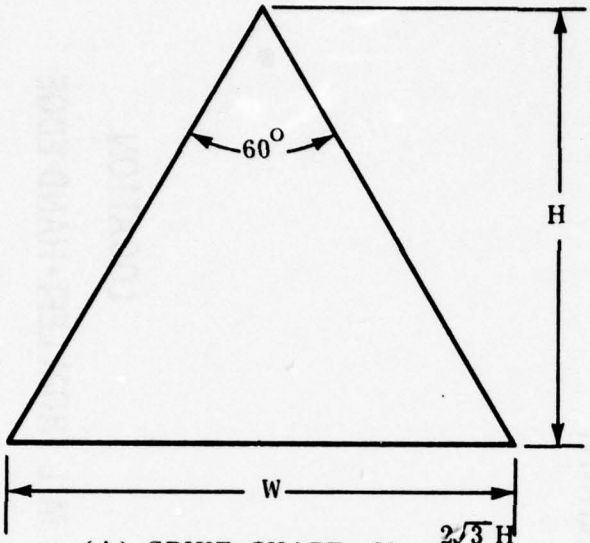
- SPIKE LENGTHS — LOCATION

  2.5 μ — 1 MIL FROM LEFT-HAND EDGE

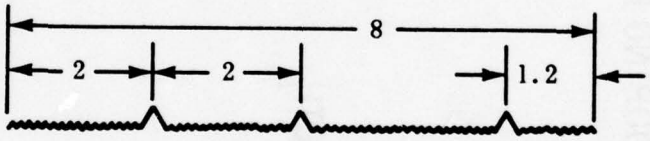
- SPIKE DIRECTION

  N^{++} CONTACT ⟶ N-TYPE — N^{++} DIFFUSION ⟶ N-TYPE

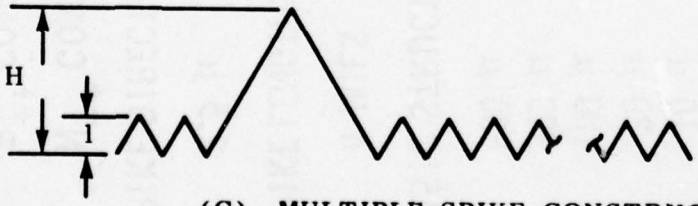
  P^{++} CONTACT ⟶ N-TYPE — P^{++} DIFFUSION ⟶ N-TYPE



(A) SPIKE SHAPE, $W = \frac{2\sqrt{3}}{3} H$



(B) MULTIPLE SPIKE LOCATIONS ON JUNCTION.
(DIMENSIONS IN MILS)



(C) MULTIPLE SPIKE CONSTRUCTION DETAIL.
H = 2,4 OR 8

Figure 6. Spike detail.

TABLE 6. Multiple Spike Structures.

- 51 DEVICES
- N-TYPE CONTROLLED DOPING REGION (X_E) LENGTH
  - 10 μ
  - 30 μ
  - 100 μ
- BASIC STRUCTURE WIDTH
  - 8 MILS
- SPIKE LENGTH

	LOCATION
1 μ	CONTINUOUS ACROSS DEVICE
2 μ	2 MIL, 4 MIL, & 6.8 MIL FROM LH EDGE
4 μ	2 MIL, 4 MIL, & 6.8 MIL FROM LH EDGE
8 μ	2 MIL, 4 MIL, & 6.8 MIL FROM LH EDGE

- SPIKE DIRECTION

N^{++} CONTACT ⟶ N-TYPE	N^{++} DIFFUSION ⟶ N-TYPE
P^{++} CONTACT ⟶ N-TYPE	P^{++} DIFFUSION ⟶ N-TYPE

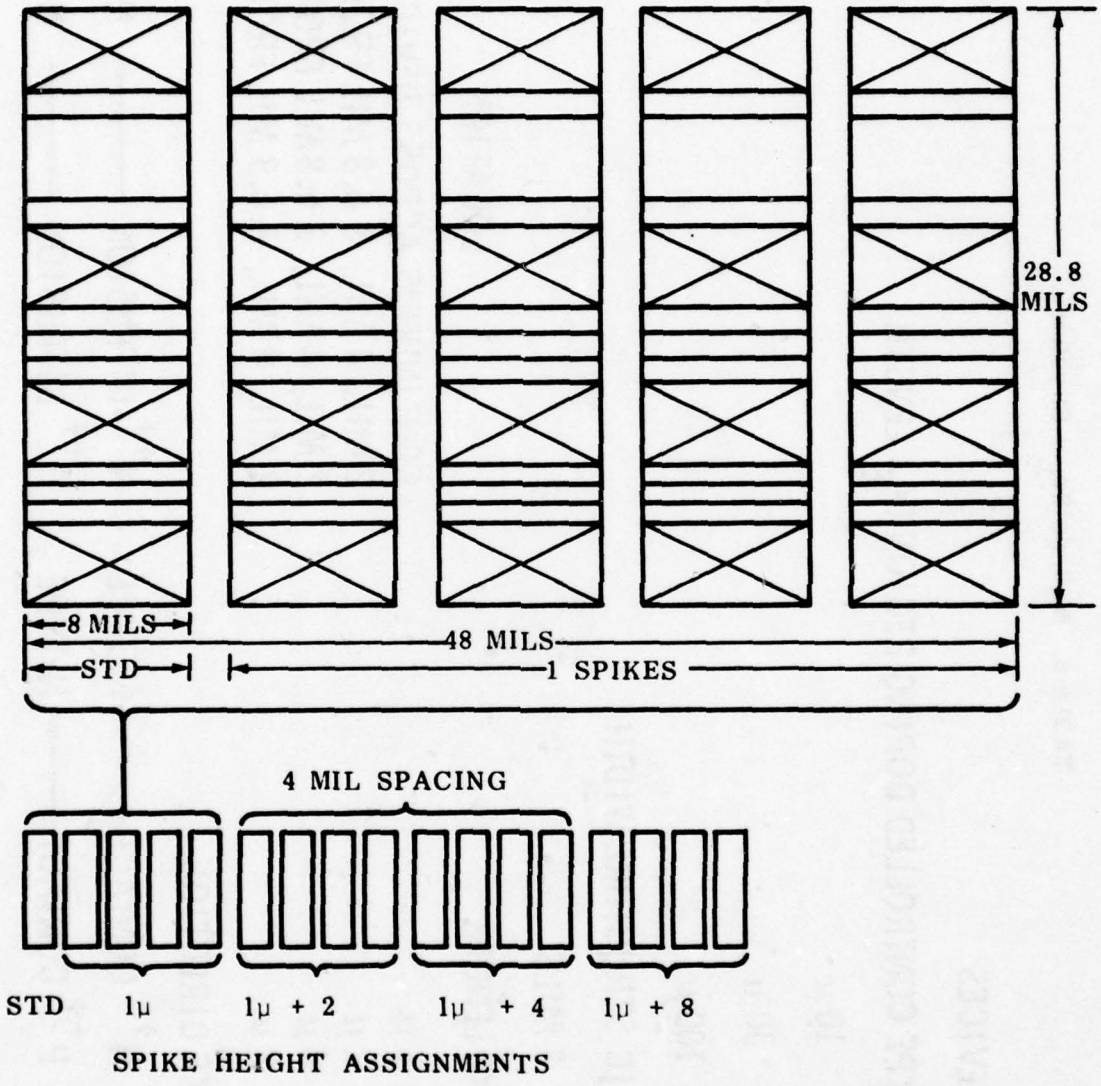


Figure 7. Multiple spike structures.

TABLE 7. Doping Level Test Structure.

- 1 DEVICE
- N-TYPE IMPLANT LEVEL

  1×10^{14}
  1×10^{15}
  1×10^{16}
  1×10^{17}
  5×10^{17}

- LENGTH BETWEEN CONTACTS

  100μ(4 MILS)

- WIDTH

  200μ(8 MILS)

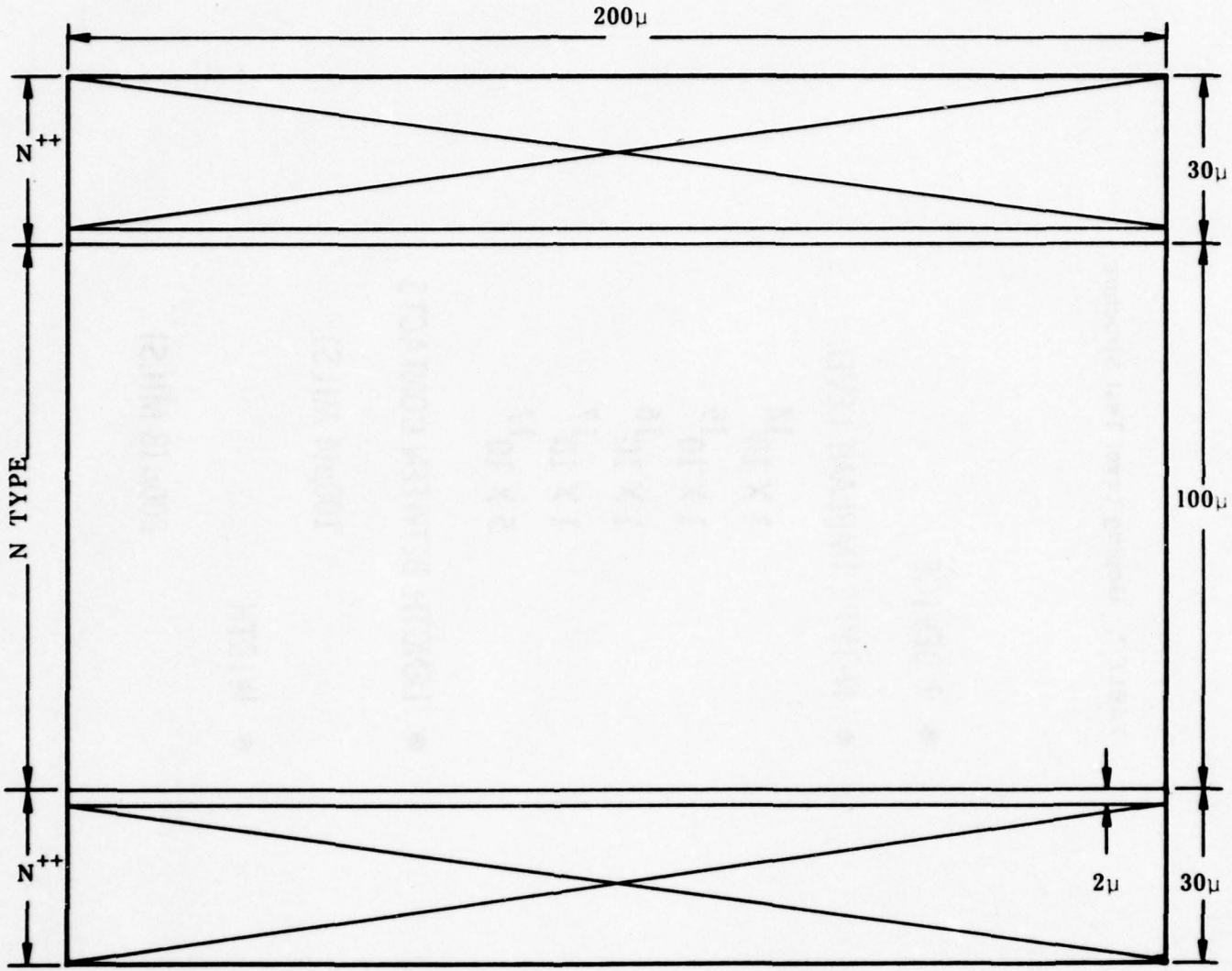


Figure 8. Doping level test structure.

TABLE 8. Radius of Curvature Structure.

- 9 DEVICES
- RADIUS ON P^{++} DIFFUSION

  5 μ
  10 μ
  30 μ
- RADIUS ON N^{++} DIFFUSION

  5
- RADIUS SEPARATION

  10 μ
  30 μ
  100 μ
- CONTACT OPENING FROM P^{++} DIFFUSION EDGE

  5 μ
- METAL OVERLAP OF CONTACT

  2 μ

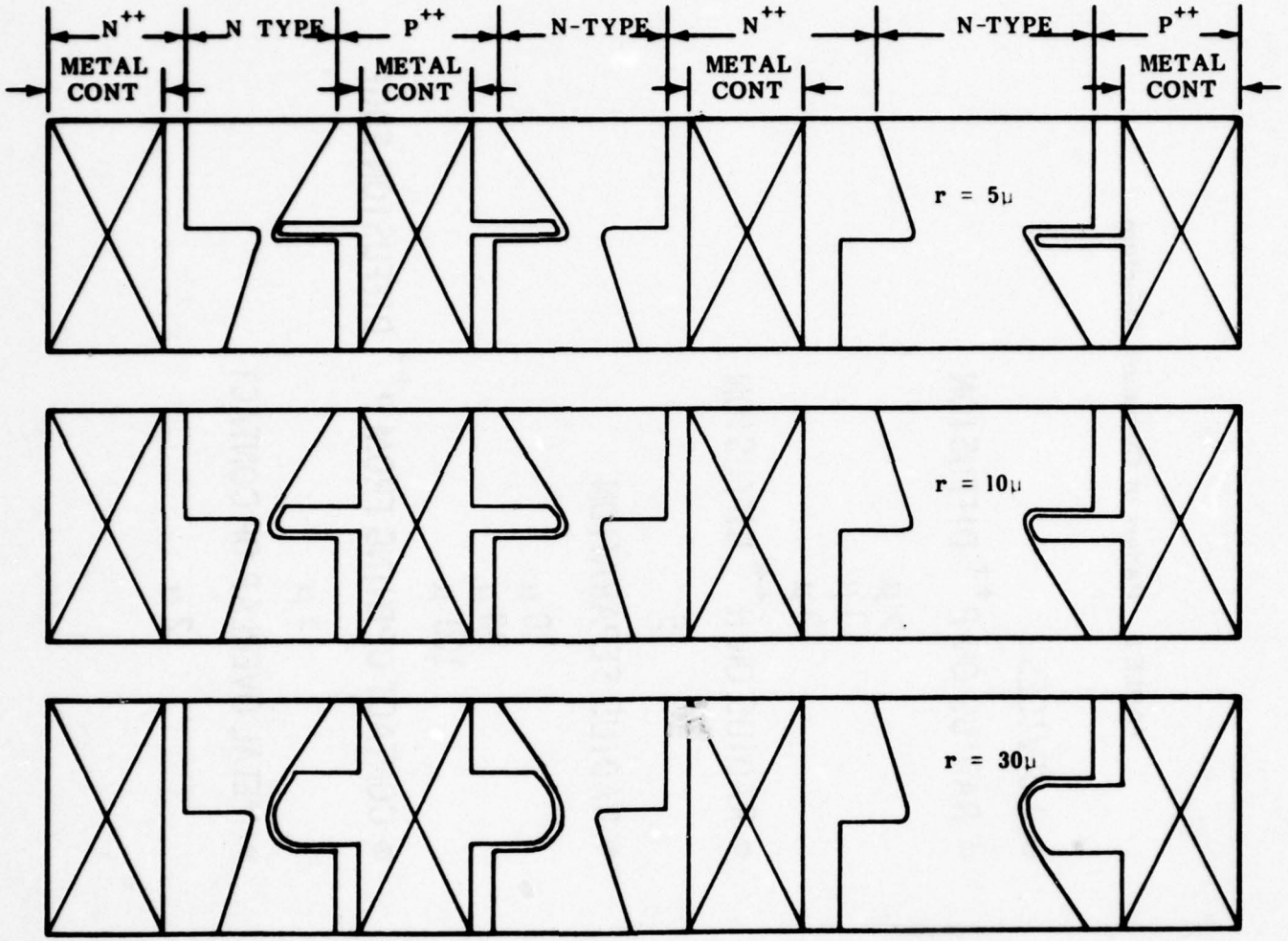


Figure 9. Radius of curvature structure.

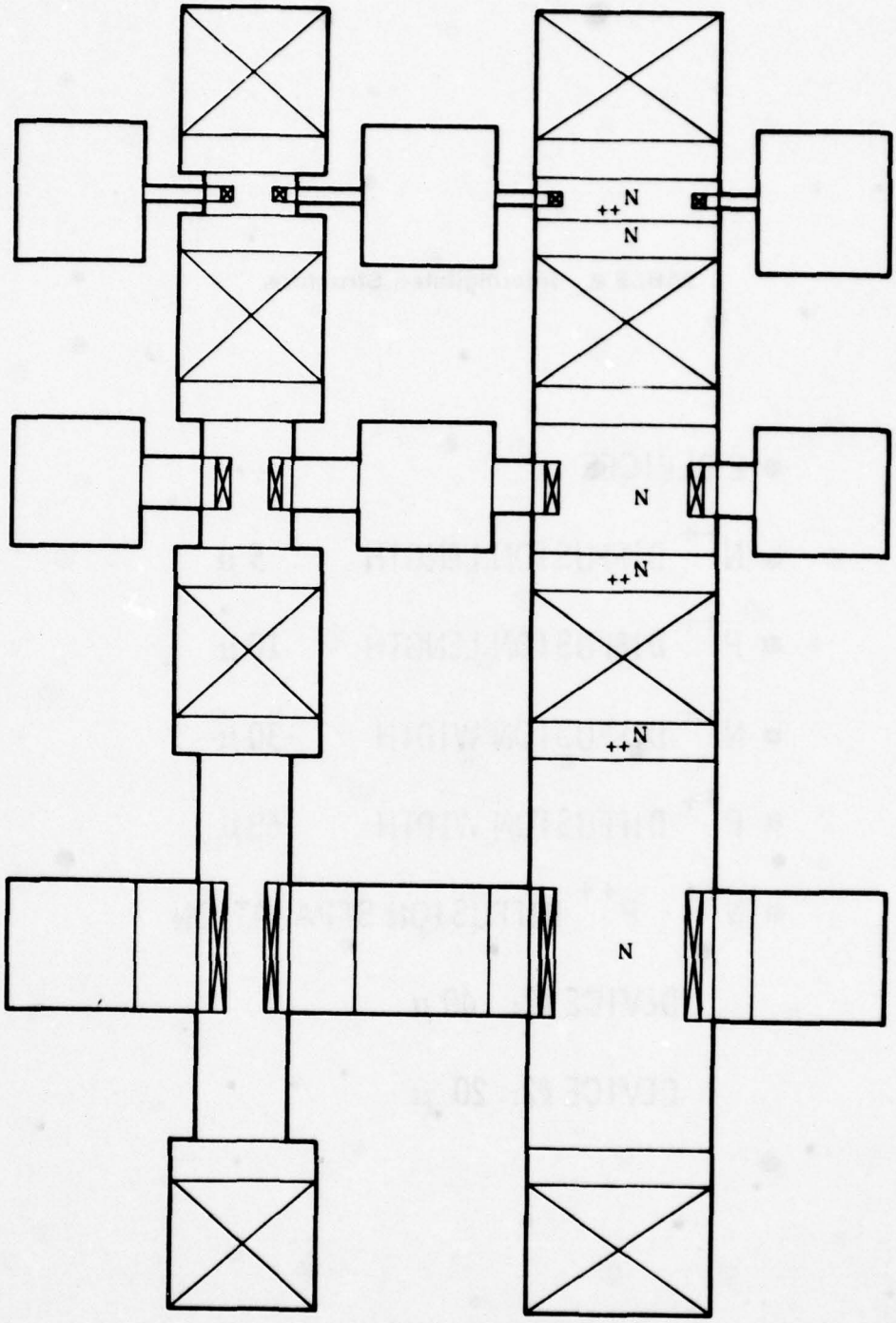


Figure 10. Four-terminal structure.

TABLE 9. Interdigitated Structure.

- 2 DEVICES
- N^{++} DIFFUSION LENGTH 5 μ
- P^{++} DIFFUSION LENGTH 10 μ
- N^{++} DIFFUSION WIDTH 30 μ
- P^{++} DIFFUSION WIDTH 60 μ
- N^{++} - P^{++} DIFFUSION SEPARATION

  DEVICE #1: 40 μ

  DEVICE #2: 20 μ

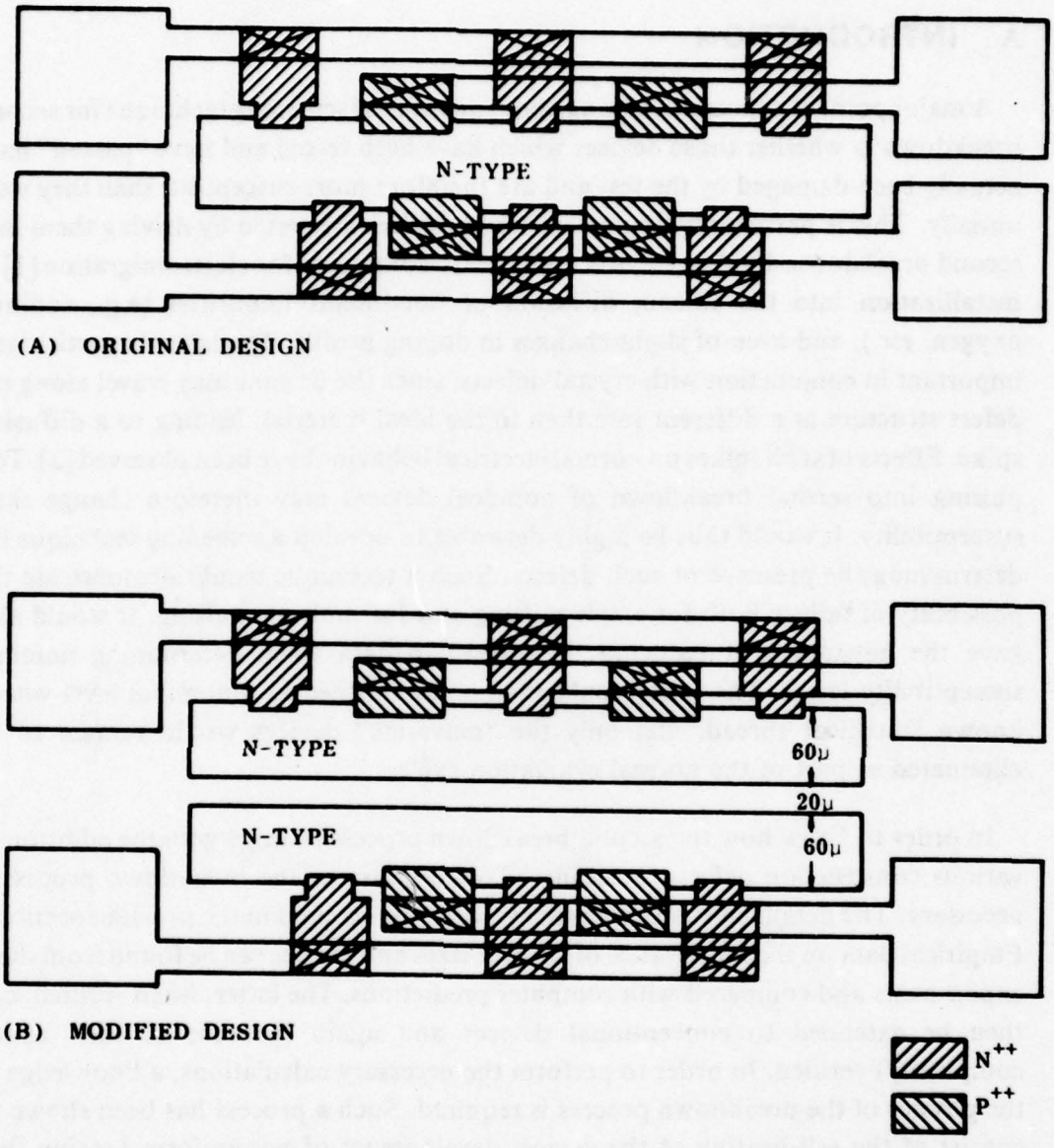


Figure 11. Interdigitated device.

5. PREDICTING SECOND BREAKDOWN*

A. INTRODUCTION

A major point of concern in talking about any sort of screening technique for second breakdown is whether those devices which have been tested and have "passed" have actually been damaged by the test and are therefore more susceptible than they were initially. This is particularly important when devices are tested by driving them into second breakdown. Evidence exists under these conditions for electromigration [1] of metallization into the silicon, diffusion of nondopant impurities (e.g., sodium, oxygen, etc.), and even of slight changes in doping profile. The latter is particularly important in conjunction with crystal defects, since the dopant may travel along the defect structure at a different rate than in the ideal material, leading to a diffusion spike. Effects of such spikes on normal electrical behavior have been observed [2]. Test pulsing into second breakdown of nonideal devices may therefore change their susceptibility. It would thus be highly desirable to develop a screening technique for determining the presence of such defects. Such a technique would demonstrate the possibility of failure both for single pulsing and for multiple pulsing. It would also have the advantage of reducing the spread in data when determining nominal susceptibility levels. The latter could then be established as a nominal level with a known statistical spread, and only the "maverick" devices would remain to be eliminated as part of the normal evaluation cycle.

In order to know how the second breakdown process changes with the addition of various construction defects, a means of observation of the breakdown process is necessary. The details of such experiments were just covered in the previous sections. Empirical data on the importance of relative sizes and shapes can be found from these experiments and compared with computer predictions. The latter, when verified, can then be extended to conventional devices and again (because of their added complexity) verified. In order to perform the necessary calculations, a knowledge of the physics of the breakdown process is required. Such a process has been shown to consist of the self-heating of the device, development of nonuniform heating (hot spots) by a complicated electrical and thermal interaction, preferential elongation of one of the hot spots until the high-resistivity region is bridged, and rapid destruction of the device thereafter [1]. The problem of the effects of geometry and structural defects on the specific locations of hot spots has already been pointed out in Section 1.

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When hot spots form, the current density becomes a function of position x, y, z, and time t. Experimental evidence from transistor and SOS diode tests indicates that the locations of the hot spots are determined primarily from geometrical/electrical field considerations, with defects seemingly playing a lesser role, while initial shapes of the hot spots seem to be only slightly affected by such considerations and depend more strongly on the thermal characteristics of the material. The hot spots later distort (elongate, etc.) because of current flow patterns, field distributions (which in turn depend on the structure, or geometry, of the device), and other factors. In bulk material the effect is that of parallel nonlinear resistors. In avalanching depletion regions an analogous situation holds. The observed behavior in SOS diodes is that cross-sectional area remains essentially the same for all hot spots, even the preferred one. The latter does enlarge very slightly in area compared to the others but elongates much more dramatically. *Figure 1* shows SOS diode data as a function of time. The success of Wunsch's model and various one-dimensional computer analyses [3,4] suggests that the current density (at least initially) also is not radically different from that of the others. Moreover, after one hot spot has distinguished itself by elongating more rapidly than the others, the others appear to continue to elongate at a rate slower than their initial one, consistent with the requirement for constant total current.

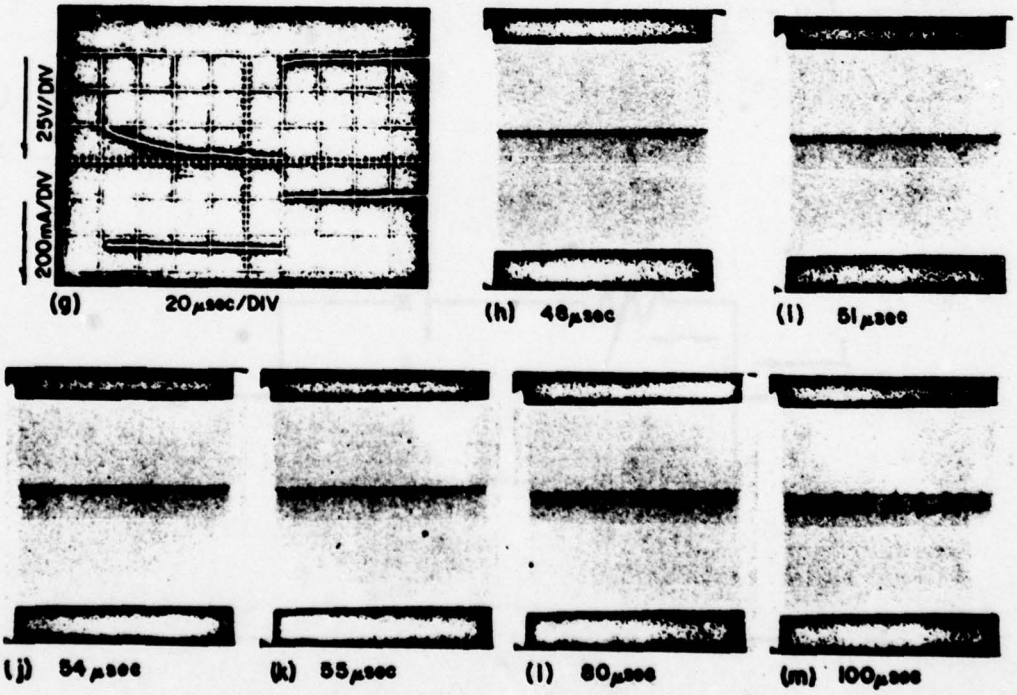

Figure 1. Hot spot formation.

B. SERIES RESISTANCE

The following is a very qualitative explanation of the effects of the variation of series resistance and, in the case of SOS diodes or of the transistor regions near a heat sink, of heat loss from this series resistance on the thermal stability of second breakdown. The SOS diodes will be considered first and then conventional bipolar devices by comparison. A very short period of time τ will be considered at various stages in the second breakdown process. During τ, change in voltage across the avalanching depletion region will be assumed to be constant, since it is such a short period of time. The diode will be divided into parallel strips, each of which will consist of a voltage V_J across the depletion layer and a nonlinear resistance. To further simplify the model, a single strip will be assumed to be hotter than the others and the remainder will be lumped into a single element. The resulting very simple equivalent circuit is shown in *Figure 2*. R_i, I_i, T_i, and V_{Ji} correspond to the unusual element, while R_e, I_e, T_e, and V_{Je} correspond to the lumped equivalent of all of the diode external to that special element. Resistivity in the series resistance varies with temperature approximately as

$$\rho(T) = \begin{cases} \rho_1 e^{aT} & T \leq T_1 \\ \rho_0 - a(T - T_p)^2 & T_1 \leq T \leq T_2 \\ \rho_2 e^{-bT} & T \geq T_2 \end{cases} \quad . \tag{1}$$

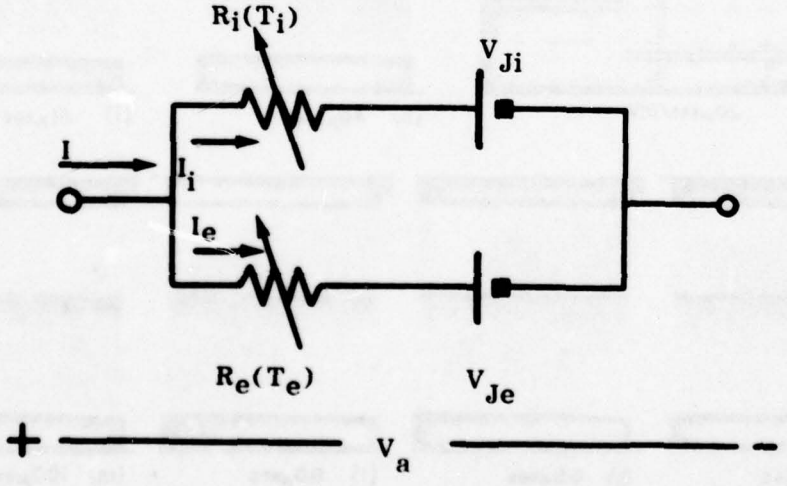

Figure 2. Lumped equivalent circuit.

As an example, for $N=10^{17}cm^{-3}$, $T_1=523°K$ and $T_2=573°K$. Ambient temperature will be denoted by T_∞. When a pulse of constant current I is applied, the equivalent battery voltages are initially equal, and $T_i=T_e$. If for some reason T_i attempts to increase above T_e, current I_i is forced to decrease, causing less dissipation, and T_i drops back "into line" with T_e. If $V_{Ji}=V_{Je}$, then

$$I_i R_i = I_e R_e \quad . \tag{2}$$

Since A_i is observed experimentally to be practically a constant fraction of A_J (multiple spots tend to initiate quite uniformly in size), $A_i=A_J/\gamma$ where γ is on the order of 500. Under this assumption, $A_E \simeq A_J$. Then,

$$\gamma I_i \rho_i = I_e \rho_e \quad . \tag{3}$$

When $\rho_i = \rho_e$, the temperature is completely uniform across the device, $\gamma I_i = I_e$. Since the total current $I = I_i + I_e$ is a constant, for T_i and T_e less than T_1,

$$I_i = \frac{I}{1 + \gamma\rho_i/\rho_e} \simeq \frac{I\rho_{Re}}{\gamma\rho_i} \simeq \frac{I}{\gamma} e^{a(T_e - T_i)} \quad . \tag{4}$$

If the difference between T_i and T_e is not zero, the sign of the exponent is such that I_i either increases or decreases until the excess or lack of ohmic heating in R_i brings T_i back to equality with T_e. Thus, the SOS diode attempts to maintain uniform temperature increase up to T_1. It can be shown, with somewhat more complicated algebra, that the same is true all the way up to T_p. At the latter temperature, the slope of the $\rho(T)$ curve changes sign. To illustrate the effect of this change in slope, suppose that conditions were so ideal that uniform conduction could exist beyond T_2. Then

$$I_i = \frac{I}{\gamma} e^{-b\,(T_e - T_i)} \quad , \tag{5}$$

so that any deviation of T_i from T_e would lead to an even greater imbalance. Diffusive flow of heat and losses to the substrate may tend to slow the effect somewhat and may even lead to a steady-state condition, but that condition will be one of inhomogeneity; i.e., there will be hot spots.

Assuming that the normal course of events has taken place, i.e., that hot spots have formed immediately at T_p, a new (and as yet unexplained) phenomenon takes place. Instead of forming at random locations, the hot spots take on a uniform pattern. Mutual repulsion of current carriers in the hot spots, voltage equalization due to current flow parallel to the junction, and "eigenvalue" solutions to the current/heat flow partial differential equations have all been suggested as possible explanations. Whatever the cause, the time required is so short that the pattern can develop before temperature variations are large enough that the nonlinear properties of the material can "lock in" the pattern. Efforts are currently under way to simulate hot-spot formation; however, computer storage requirements are a problem.

C. WUNSCH MODEL EXTENSIONS — CONVENTIONAL TRANSISTOR

The Wunsch model is probably the simplest of the second breakdown models. It averages or neglects all variation in semiconductor parameters with temperature, neglects all boundary effects, and assumes a step function power input per unit area at the origin. The heat equation is thus

$$\frac{\partial T}{\partial t} = \alpha \frac{\partial^2 T}{\partial x^2} \tag{6}$$

with conditions

$$T(x,0) = T_\infty \tag{7}$$

$$-K \frac{\partial T}{\partial x}(0,\ t) = \frac{P}{2A} \tag{8}$$

$$T(\infty,\ t) = T_\infty \quad . \tag{9}$$

The factor of two in the Fourier law boundary condition is needed because heat flows outward in both directions from the origin, and only one side of the junction is analyzed. Symmetry is implicit in the boundary conditions. As pointed out by Wunsch, the entire junction may be involved, or just a constricted area. Taking the Laplace transform,

$$S\overline{T} - T_\infty = \alpha \frac{d^2\overline{T}}{dx^2} \tag{10}$$

$$\overline{T} = \frac{P\sqrt{\alpha}\ e^{-\frac{x}{\sqrt{\alpha}}\sqrt{s}}}{2KAs^{3/2}} + \frac{T_\infty}{S} \tag{11}$$

$$T(x,\ t) = \frac{P\sqrt{\alpha}}{KA\sqrt{\pi}}\sqrt{t}\ \ e^{x^2/4\alpha t} - \frac{Px}{2KA}\ \text{erfc}\ \frac{X}{\sqrt{4\alpha t}} + T_\infty \quad . \tag{12}$$

Defining a critical temperature T_f [e.g., when $n_i\,(T) = N$] at the origin,

$$T_f = T(0,\ t_f) = \frac{P\sqrt{\alpha}\ \sqrt{t_f}}{KA\sqrt{\pi}} + T_\infty \tag{13}$$

$$\frac{P}{A} = \frac{K\sqrt{\pi}\ (T_f - T_\infty)}{\sqrt{\alpha}\ \sqrt{t_f}} = \frac{\sqrt{\pi K c \rho_M}\ (T_f - T_\infty)}{\sqrt{t_f}} \quad . \tag{14}$$

This solution provides an engineering approximation useful over several orders of magnitude. It is not valid for very short times ($t < 10$ nsec) or very long times ($t > 100$ μsec). In both extremes, the distribution of the heat source becomes important.

Consider now a model just slightly more complicated than the Wunsch model. Heat generation is distributed over the depletion region, leading to a $\vec{J} \cdot \vec{\mathcal{E}}$ term. Heat generation outside the depletion layer is taken to be negligible, but this is not a requirement, and the method to be demonstrated here is still applicable. An "average" thermal diffusion constant is taken here for simplicity; a computer solution is given in Section 7. First, the temperature must be continuous at the boundary of the depletion layer to prevent an infinite heat generation (Fourier's law). Similarly, to prevent a heat source or sink at the depletion layer edge, the gradients must match at the same point. Thus, if the one-dimensional model used previously is extended to a symmetric junction with depletion layer half-width W, the physical problem demands the following boundary conditions:

$$T(x,0) = T_{\infty} \tag{15}$$

$$\frac{\partial T}{\partial x}(x, 0) = 0 \tag{16}$$

$$T(\infty, t) = T_{\infty} \tag{17}$$

$$T(W^{-}, t) = T(W^{+}, t) \tag{18}$$

$$\frac{\partial T}{\partial \chi}(W^{-}, t) = \frac{\partial T}{\partial x}(W^{+}, t) \quad . \tag{19}$$

Condition (16) arises from the symmetry of the problem. Outside the depletion region ($x \geq W$),

$$\frac{\partial T}{\partial t} = \alpha \frac{\partial^2 T}{\partial x^2} + g_e(x, T) \tag{20}$$

where g_e is the external generation from ohmic heating of the bulk. For the present analyses, this term is neglected. A more general analysis would simply include it. Inside the depletion region,

$$\frac{\partial T}{\partial t} = \alpha \frac{\partial^2 T}{\partial \chi^2} + g(x, T) \quad . \tag{21}$$

The solutions derived must match at x=W, as noted in Equation (18). The first partial derivative must also match Equation (19) but not necessarily the second. A number of possible generation terms g(x,T)=g(x) with constant W will now be considered. First, assume that a constant, "average" generation term may be used; this is admittedly a crude assumption. For a symmetric junction, g(x) is given by

$$g(x) = g_o = \frac{I}{c\rho_M WA} \int_0^W \mathcal{E}(x)dx = \frac{P}{2c\rho_M WA} \quad , \tag{22}$$

independent of the form of $\mathcal{E}(x)$. Taking the Laplace transforms Equations (20) and (21) and matching at W, the solution to Equation (21) in Laplace form is

$$\overline{T} = \frac{g_o e^{-\sqrt{\frac{s}{\alpha}}x} \sinh\sqrt{\frac{s}{\alpha}}W}{s^2} - \frac{g_0}{s^2}\cosh\sqrt{\frac{s}{\alpha}}(W - \chi) + \frac{T_\infty}{s} + \frac{g_0}{s^2} \quad . \tag{23}$$

Assuming (by symmetry arguments) that the peak temperature is at the origin and that failure occurs when this temperature reaches T_f.

$$\frac{T_f}{s} = \bar{T}(o,s) = \frac{g_0 \sinh \sqrt{\frac{s}{\alpha}}\, W}{s^2} - \frac{g_0 \cosh \sqrt{\frac{s}{\alpha}}\, W}{s^2} + \frac{T_\infty}{s} + \frac{g_0}{s^2}$$

$$= \frac{g_0}{s^2}\left(1 - e^{-\sqrt{\frac{s}{\alpha}}\, W}\right) + \frac{T_\infty}{s} \quad . \tag{24}$$

For small W,

$$\frac{T_f - T_\infty}{s} \simeq \frac{g_0 W}{\sqrt{\alpha}}\left(\frac{1}{s^{3/2}} - \frac{W/2\sqrt{\alpha}}{s}\right) \simeq \frac{g_0 W}{\sqrt{\alpha}\, s^{3/2}} \quad . \tag{25}$$

Taking the inverse transform,

$$\left(\frac{P}{A}\right) g_0 = S_{g_o} = K\sqrt{\frac{\pi}{\alpha}}\, \frac{(T_f - T_\infty)}{\sqrt{t_f} - \frac{w}{4}\sqrt{\frac{\pi}{\alpha}}} = \frac{C_W}{\sqrt{t_f} - \sqrt{t_{g_0}}} \simeq \frac{C_W}{\sqrt{t_f}} \tag{26}$$

which is Wunsch's solution. Without the assumption of small W, the general solution is

$$T_f - T_\infty = g_0 t_f \left(1 - \frac{W^2}{2\alpha t_f} \operatorname{erfc} \frac{W}{\sqrt{4\alpha t_f}} + \frac{W e^{-W^2/4\alpha t_f}}{\sqrt{\pi \alpha t_f}} \right) . \tag{27}$$

The only new variable arising from the more general form is W, the depletion layer half-width at avalanche, which depends on the doping density, N. This lack of additional variables beyond W holds true when $\mathcal{E}$ is replaced by more complicated expressions for the electric field. For example, the field in the symmetric abrupt-abrupt junction depletion region is

$$\mathcal{E}(x) = \mathcal{E}_0 \left(\frac{W - x}{W} \right) \tag{28}$$

and

$$g(x) = \frac{J\varepsilon(x)}{C\rho_M} = \frac{VI(W - X)}{C\rho_M A w^2} = \frac{P(W - X)}{C\rho_M A w^2} \equiv \gamma_1 (W - X) \tag{29}$$

in which V is the voltage across 2W, the total width of the symmetric junction. Then,

$$\overline{T} = \frac{\gamma_1\sqrt{\alpha}}{s^{5/2}} \left[e^{-\sqrt{\frac{s}{\alpha}}W} \cosh \sqrt{\frac{s}{\alpha}}X - e^{-\sqrt{\frac{s}{\alpha}}X} \right] + \frac{T_\infty}{s} + \frac{\gamma_1(W - X)}{s^2} \qquad (30)$$

and

$$\frac{T_f}{s} = \frac{\gamma_1\sqrt{\alpha}}{s^{5/2}} \left(e^{-\sqrt{\frac{s}{\alpha}}W} - 1 \right) + \frac{\gamma_1 W}{s^2} + \frac{T_\infty}{s}$$

$$T_f - T_\infty = \gamma_1\sqrt{\alpha}(4t^{3/2}) \left[i^3\text{erfc} \frac{W}{\sqrt{4\alpha t}} - \frac{1}{6\sqrt{\pi}} \right] . \qquad (31)$$

For small W,

$$T_f - T_\infty = \gamma_1 W^2 \sqrt{\frac{t_f}{\alpha\pi}} = \frac{P}{c\rho_M A}\sqrt{\frac{t_f}{\alpha\pi}} , \qquad (32)$$

again Wunsch's solution.

Similarly, the field in a linearly graded junction depletion region is

$$\mathcal{E} = \mathcal{E}_o \left(\frac{W^2 - X^2}{W^2} \right) \quad , \tag{33}$$

leading to

$$g(x) = \gamma_2 \, (W^2 - X^2) = \frac{3P\alpha}{2KAW^3} \, (W^2 - X^2) \tag{34}$$

and solutions

$$\bar{T} = 2 \left[\frac{\gamma_2 W \sqrt{\alpha}}{s^{5/2}} + \frac{\gamma_2 \alpha}{s^3} \right] e^{-\sqrt{\frac{s}{\alpha}} W} \cosh \sqrt{\frac{s}{\alpha}} X + \frac{\gamma_2 (W^2 - X^2)}{s^2} - \frac{2\gamma_2 \alpha}{s^3} + \frac{T_\infty}{s} \tag{35}$$

and

$$\frac{T_f - T_\infty}{s} = \frac{2\gamma_2\alpha}{s^3}\left(e^{-\sqrt{\frac{s}{\alpha}}W} - 1\right) + \frac{2\gamma_2 W\sqrt{\alpha}}{s^{5/2}} e^{-\sqrt{\frac{s}{\alpha}}W} + \frac{\gamma_2 W_2}{s^2} \quad . \tag{36}$$

For small W,

$$T_f - T_\infty = \frac{4\gamma_2 W^3\sqrt{t_f}}{\sqrt{\alpha\pi}}\left[1 + \frac{\sqrt{\alpha\pi t_f}}{4W}\right] = \frac{3P\sqrt{t_f}}{c\rho_M\sqrt{\alpha\pi}A}\left[1 + \frac{\sqrt{4\alpha t_f}}{4W}\right] . \tag{37}$$

The term in square brackets is equal to one for failure times less than a few microseconds.

Results of calculations using the three models for $\epsilon(x)$ are summarized in *Table 1*. The following definitions have been used for simplicity:

$$S = P/A \tag{38}$$

and

TABLE 1. Summary of Results for Wunsch Model Extensions.

Short Time

$$S_{g_0} = \frac{2W}{\sqrt{\pi\alpha}} \frac{C_w}{t_f} = \frac{2W}{\sqrt{\pi\alpha}} \frac{S_w}{\sqrt{t_f}}$$

$$S_{\gamma_1} = \frac{W}{\sqrt{\pi\alpha}} \frac{C_w}{t_f - \frac{4}{3W}\sqrt{\frac{\alpha}{\pi}}\, t_f^{3/2}} = \frac{S_{g_0}/2}{1 - \frac{4}{3W}\sqrt{\frac{\alpha}{\pi}}\sqrt{t_f}}$$

$$S_{\gamma_2} = \frac{2W}{3\sqrt{\alpha\pi}} \frac{C_w}{t_f - \frac{2\alpha}{w^2} t_f^2} = \frac{S_{g_0}/3}{1 - \frac{2\alpha}{w^2} t_f}$$

Long Time

$$S_{g_0} = \frac{C_w}{\sqrt{t_f} - \sqrt{t_o}} \frac{S_w}{1 - \sqrt{t_o/t_f}} \qquad t_o = \frac{\pi}{\alpha}\left(\frac{W}{4}\right)^2$$

$$S_{\gamma_1} = \frac{C_w}{\sqrt{t_f} - \sqrt{t_1}} = \frac{S_w}{1 - \sqrt{t_1/t_f}} \qquad t_1 = \frac{\pi}{\alpha}\left(\frac{W}{6}\right)^2$$

$$S_{\gamma_2} = \frac{C_w}{\sqrt{t_f} - \sqrt{t_2}} = \frac{S_w}{1 - \sqrt{t_2/t_f}} \qquad t_2 = \frac{\pi}{\alpha}\left(\frac{3W}{16}\right)^2$$

$$c_W = \frac{K\sqrt{\pi}(T_f - T_\infty)}{\sqrt{\alpha}} \quad . \tag{39}$$

It is to be noted that these results are based strictly on a one-dimensional thermal model with constant thermal parameters. Short-time charge distribution effects [4], effects of temperature-dependent parameters [3], and two-dimensional (nonuniform conduction) effects are not considered. *Figures 3* and *4* illustrate some of the consequences of the formulas in *Table 1*. The main purpose of these calculations is to show that even an idealized, low-injection approximation involving the depletion width (extended Wunsch model) leads to a complicated dependence of time to failure t_f on power per unit junction area. As discussed in the Interim Report for this project, breakdown may actually be via the junction sidewall, leading to a completely different breakdown behavior. In every case considered thus far, the depletion layer width was assumed to be much narrower than the total width of the device, so that outside the depletion layer, one boundary was taken to be "infinity." This is obviously not necessary and is easily remedied. The width of the bulk region between depletion layer and the next interface (new depletion layer, passivation layer, surface, etc.) now enters the equation, and the type of boundary condition there (convective, radiative, etc.) could also add at least one new parameter. Bulk resistance self-heating could be added with great computational difficulty. Heat flow from a second depletion layer could further complicate the problem, but such difficulties are beyond the scope of this discussion.

A simple approximation for W may be found by evaluating the avalanche integral across the entire depletion layer. Assuming equal ionization coefficients [5]

$$\alpha_p = \alpha_n = \alpha_0 \mathcal{E}^7 \quad , \tag{40}$$

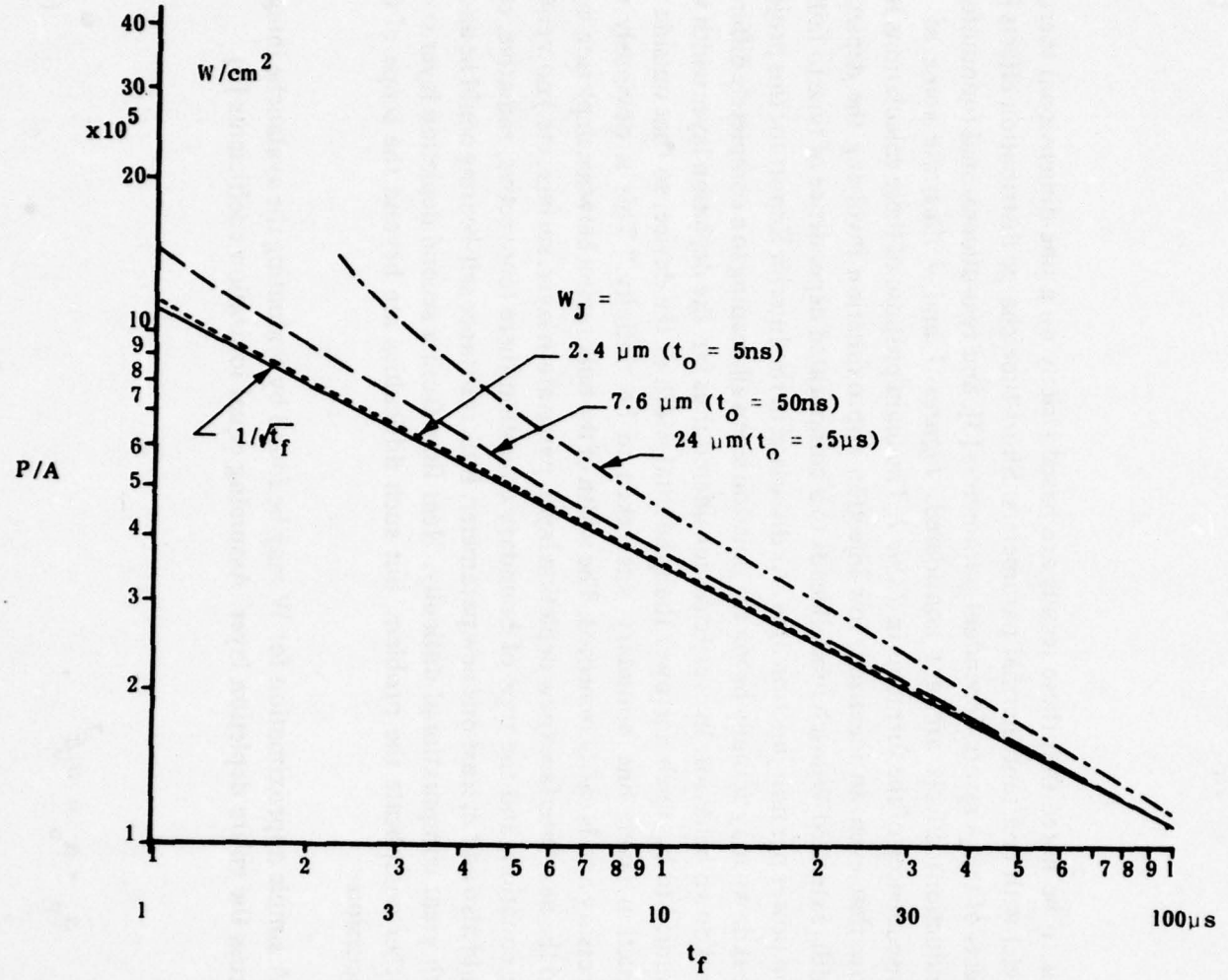

Figure 3. Depletion width effects on failure level, long-time approximation.

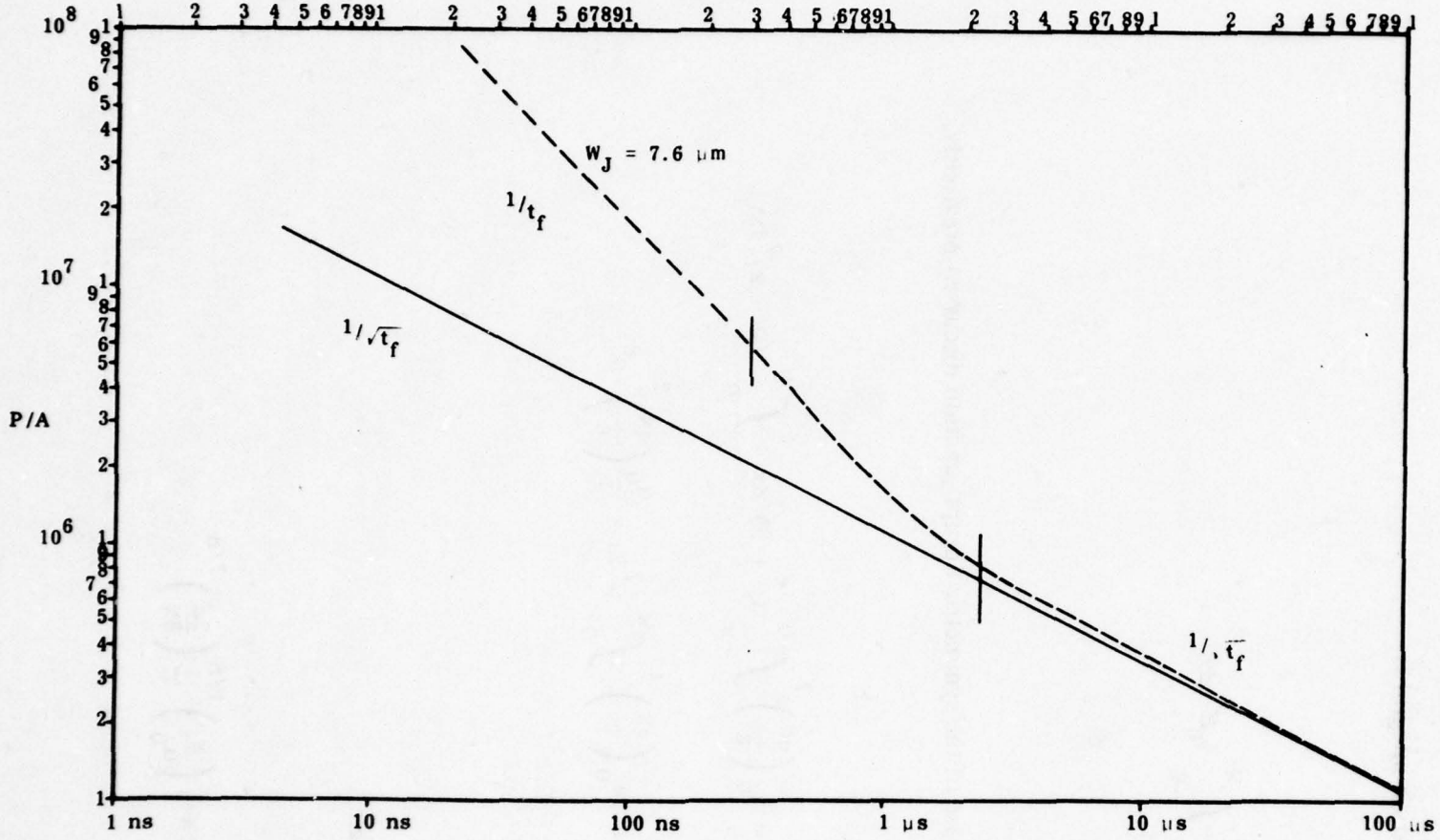

Figure 4. Failure level deviation over wide range of t_f.

the ionization integral is

$$1 = \int_{-W}^{W} \alpha_0 \mathcal{E}^7 \, dx \quad . \tag{41}$$

For the case of the symmetric abrupt junction discussed previously,

$$1 = \alpha_0 \left(\frac{qN}{\varepsilon}\right)^7 \int_{-w}^{0} (w + x)^7 dx + \int_{0}^{w} (w - x)^7 dx \tag{42}$$

$$= 2\alpha_0 \left(\frac{qN}{\varepsilon}\right)^7 \int_{0}^{W} \mu^7 d\mu = \frac{\alpha_0}{4} \left(\frac{qN}{\varepsilon}\right)^7 W^8$$

from which

$$W = \frac{1}{2} \left(\frac{8}{\alpha_0}\right)^{1/8} \left(\frac{2\mathcal{E}}{8N}\right)^{7/8} \quad . \tag{43}$$

In both the Wunsch model and the extensions considered here, an "average" value of α was used for computational simplicity. In fact, however, c,ρ_m, and K all depend on temperature. The latter varies much more significantly than the product of the first two, so that Wunsch's model could be rewritten as the solution of

$$\frac{\partial T}{\partial t} = \frac{\partial}{\partial x}\left(\alpha \frac{\partial T}{\partial x}\right) \quad . \tag{44}$$

While Crank [6] shows methods of dealing with this equation, it is really not much more accurate than the original Wunsch approximation, nor are the extensions. Although Crank's methods of finding approximate solutions could be used, some fundamental problems exist with the basic assumptions made in the analysis (boundary conditions, etc.), so that the added effort is again not justified. Since the approximate solutions using an average thermal conductivity may provide some insight, they are provided now for the finite-width depletion layer model in SOS diodes.

D. WUNSCH MODEL EXTENSIONS — SOS DIODES

The Wunsch model may be applied to Budenstein's SOS diodes if a substrate loss term is included:

$$\frac{\partial T}{\partial t} = \alpha \frac{\partial^2 T}{\partial x^2} - \beta(T - T_\infty) \tag{45}$$

in which β depends on the geometry and thermal properties of the sapphire substrate. Taking the Laplace transform,

$$\overline{T} = \frac{P\sqrt{\alpha}\, e^{\frac{\sqrt{s+\beta}}{\sqrt{\alpha}}}}{2KAs\sqrt{s+\beta}} + \frac{T_\infty}{s} \quad . \tag{46}$$

Then

$$T_f = T(o,\ t_f) = \frac{P\sqrt{\alpha}}{2KA\sqrt{\beta}}\ \text{erf}\ \sqrt{\beta t_f} \tag{47}$$

or

$$\frac{P}{A} = \frac{2K\sqrt{\beta}(T_f - T_\infty)}{\sqrt{\alpha}\ \text{erf}\ \sqrt{\beta t_f}} \tag{48}$$

since, for

$$\sqrt{\beta t_f} \ll 1, \tag{49}$$

$$\text{erf}\ \sqrt{\beta t_f} \simeq \frac{2}{\sqrt{\pi}} \sqrt{\beta t_f},$$

the ordinary Wunsch model is obtained not only for small losses to the substrate, but also for very high-power inputs (such that failure occurs before heat diffuses very far).

Consider the low-current avalanche breakdown in an SOS test diode. The variation in depletion width with T is ignored.

$$\frac{\partial T}{\partial t} = \alpha \frac{\partial^2 T}{\partial x^2} - \beta(T-T_\infty) + g(x) \quad . \tag{50}$$

Let

$$T = T_\infty + Ue^{-\beta t} \quad . \tag{51}$$

Then

$$\frac{\partial U}{\partial t} = \alpha \frac{\partial^2 U}{\partial x^2} + g(x)e^{\beta t} \tag{52}$$

with

$$\frac{\partial U}{\partial x}(0, t) = 0 \tag{53}$$

$$U(x, 0) = 0 \tag{54}$$

and outside the depletion region

$$g(x) = \gamma_1 (w-x) \ . \tag{55}$$

For the abrupt junction in SOS diodes with symmetric doping, g(x) is again

$$U(\infty, t) = 0 \quad . \tag{56}$$

Taking the Laplace transform of Equation (52),

$$s\overline{U} = \alpha \frac{d^2 \overline{U}}{dx^2} + \frac{\gamma_1 (W-x)}{s - \beta} \tag{57}$$

with solution

$$\bar{U} = \frac{\gamma_1\sqrt{\alpha}}{s^{3/2}(s-\beta)}\left(e^{-\sqrt{\frac{s}{\alpha}}W}\cosh\sqrt{\frac{s}{\alpha}}x - e^{-\sqrt{\frac{s}{\alpha}}x}\right) + \frac{\gamma_1(W-x)}{s(s-\beta)} \qquad (58)$$

for $x \leqslant W$. Then,

$$\bar{U}(0,s) = \frac{\gamma_1\sqrt{\alpha}}{s^{3/2}(s-\beta)}\left(e^{-\sqrt{\frac{s}{\alpha}}W} - 1\right) + \frac{\gamma_1 W}{s(s-\beta)} \qquad (59)$$

and

$$T_f - T_\infty = \gamma_1\sqrt{\alpha}\left[I(t_f) - \frac{1}{\beta^{3/2}}\operatorname{erf}\sqrt{\beta t_f} + \frac{2}{\beta}\sqrt{\frac{t_f}{\pi}}\,e^{-\beta t_f}\right] + \frac{\gamma_1 W}{\beta}\left(1 - e^{-\beta t_f}\right) \qquad (60)$$

where

$$I(t_f) = 2\int_0^{t_f} \sqrt{\tau}\, e^{-\beta\tau}\, \text{ierfc}\, \frac{W}{\sqrt{4\alpha\tau}}\, d\tau \quad . \tag{61}$$

For small W,

$$\frac{P}{A} = \frac{2C\rho_M\sqrt{\alpha\beta}(T_f - T_\infty)}{\text{erf}\sqrt{\beta t_f}} = \frac{2\sqrt{\beta}\, Cw}{\sqrt{\pi}\, \text{erf}\, \sqrt{\beta t_f}} \quad . \tag{62}$$

If β is also small, the solution again reduces to Wunsch's. For Budenstein's diodes this is only valid for $t_f << 1$ μsec, which is not within the normal test range. While the solution given in Equation (62) is also valid for large t_f, the value of β is so large that the dc solution is approached. Thus Equation (60) must always be used.

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6. COMPUTER SIMULATION OF THERMAL SECOND BREAKDOWN*

A. INTRODUCTION

Thermal second breakdown in semiconductor diodes involves a complex interaction of electrical and thermal mechanisms. A comprehensive numerical simulation of this phenomenon requires a similarly complex numerical model which, in turn, requires relatively long computation times. For the sake of expediency and economy, it is important that simulations of this nature be well defined with some assurance of validity. Of particular importance is the thermal second breakdown delay time. This parameter, more than any other, characterizes thermal second breakdown and is very beneficial in defining simulations for investigation of various aspects of this phenomenon. Moreover, the operation and performance of the quasi-two-dimensional diode thermal model employed in a previously developed comprehensive diode model [1,2] for investigation of thermal second breakdown warrants further consideration. Characterization of the thermal aspect of this model is difficult since it is an integral part of the comprehensive diode model and, therefore, not readily accessible for scrutiny. The purpose here is to develop an improved version of the diode thermal model in a form which can be readily characterized. Further, the electrical aspects of the diode thermal model are to be simplified to minimize computation times such as to provide an economical means of evaluating approximate thermal second breakdown delay times.

B. DIODE THERMAL MODEL

Quasi-two-dimensional thermal conduction for a one-dimensional diode electrical model is predicted by the one-dimensional energy continuity equation

$$\rho_D \, c_D \frac{\partial T}{\partial t} = K_D \frac{\partial^2 T}{\partial x^2} + |J \, E| - \Phi \qquad (1)$$

* W. D. Raburn, University of Alabama.

where:

$$T = T' - T_o$$

ρ_D = diode material density

c_D = diode material heat capacity

T = scaled temperature

T' = temperature

T_o = temperature of constant temperature heat sink

t = time

K_D = diode material thermal conductivity

x = position along diode axis

J = current density

E = electric field intensity

Φ = heat loss by mechanisms other than conduction along the diode axis.

Heat loss into the diode header (or substrate) through thermal conduction is accounted for through the Φ term to yield quasi-two-dimensional thermal conduction. The Φ term for the previously developed comprehensive diode model [1,2] was defined as

$$\Phi \equiv \frac{K_H}{x_{DT}} \left(\frac{T - T_o}{x_{DH}} \right)' \qquad (2)$$

where

K_H = header material thermal conductivity

x_{DT} = diode material thickness

x_{DH} = header material thickness

T_o = temperature of header constant temperature heat sink.

An electrical analog of this thermal model is shown in *Figure 1*. For this model, thermal conduction through the header to the constant temperature heat sink is simply proportional to the temperature difference between the respective diode node points and the constant-temperature heat sink. There are no intermediate temperature node points within the header material and there is no provision for heat storage in the header material. The header material is simply treated as a thermal resistance between the diode and the constant-temperature heat sink.

The primary advantage of this model is its simplicity. The computation time associated with thermal conduction through the header material is negligible. The simplicity of the model, however, leads to considerable error in the computation of long delay times. On the other hand, for delay times sufficiently short that negligible thermal conduction into the header material occurs, the extra computations become extraneous, making the simplicity of this model desirable.

A numerical algorithm for this diode model was developed by combining Equations (1) and (2) and applying finite-difference techniques in a fully implicit formulation [3,4] Provisions for temperature-dependent coefficients is made by employing an iterative solution scheme leading to the following system of linear equations:

$$\Delta t\ A\ T(N-1)^{s+1} + [\Delta t \Delta x^2\ B - (x^2 + 2\ \Delta t\ A)]\ T(N)^{s+1}$$

$$+ \Delta t\ A\ T(N+1)^{s+1} = -\Delta x^2\ [T(N)^s + \Delta t\ C(N)] \quad (3)$$

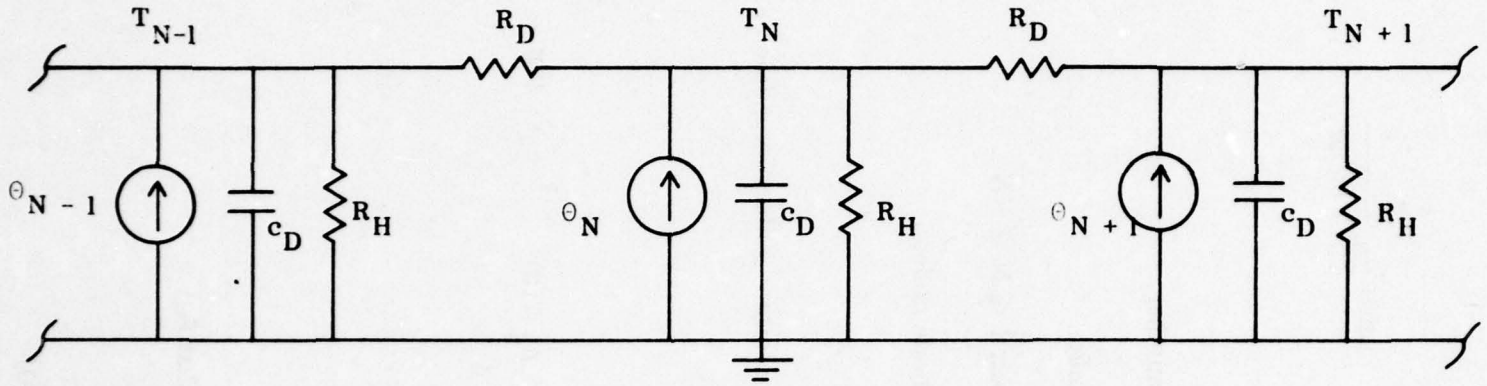

Figure 1. Electrical analog of quasi-two-dimensional diode thermal model. (T-temperature, R_D-diode thermal resistance, N-node number, c_D-diode heat capacity, R_H-header thermal resistance, Θ-heat generation).

where

$$A \equiv \frac{K_D}{\rho_D c_D} \quad , \qquad B \equiv \frac{K_H}{\rho_D c_D x_{DH} x_{DT}} \quad , \qquad C(N) \equiv \frac{|J\ E|}{\rho_D c_D}$$

and

s = present iteration number

$s+1$ = next iteration number

N = diode node number, $1 \leqslant N \leqslant NN$

NN = total number of diode nodes

Δt = time step size

Δx = distance between adjacent nodes along diode axis

or,

$$A_1\ T(N-1)^{s+1} + A_2\ T(N)^{s+1} + A_3\ T(N+1)^{s+1} = A_4 \qquad (4)$$

where

$A_1 \equiv \Delta t A$

$A_2 \equiv [\Delta t\ \Delta x^2\ B - (\Delta x^2 + 2\Delta t\ A)]$

$A_3 \equiv \Delta t\ A$

$A_4 \equiv -\Delta x^2[T(N)^s + \Delta t\ C(N)]$.

Since the second-order energy continuity equation requires two boundary conditions on temperature, the diode end point temperatures are set equal to the temperature of the constant-temperature heat sink. Equation (4) must be formulated about nodes 2 through NN-1 since the end point temperatures are maintained constant as boundary conditions. The resulting system of NN-2 linear equations must be solved each iteration to generate an improved approximation for the temperature profile at the next point in time. Iterations are performed until a specified minimum root-mean-square (RMS) change in the diode temperature profile is achieved between successive iterations or a specified maximum number of iterations are performed. With the completion of each iteration sequence, the simulation is advanced by one time step. A flow chart depicting this solution procedure is presented in *Figure 2*.

C. AN IMPROVED DIODE THERMAL MODEL

Delay times predicted by the above model may be in considerable error for long delay times. The predicted delay times are always minimum values since the header temperature profiles are assumed linear with no provision for heat storage. The linear temperature profiles between the respective diode node points and the constant temperature heat sink result in minimum thermal gradients across the header throughout the thermal transient. A more comprehensive thermal model for the header material will result in increased thermal gradients throughout the transient, thus causing an increased heat loss into the header material. Any improvement in the thermal model can be expected to increase delay times.

The obvious method for improving delay time accuracy is to implement a fully two-dimensional thermal model at the expense of a greatly increased computation time. A compromise solution which offers an increase in delay time accuracy for a modest increase in computation time is to increase the comprehensiveness of the present model by establishing intermediate node points and heat storage within the header material. Thermal conduction through the header is maintained one-dimensional as before. The header thermal model simply consists of a parallel combination of one-dimensional heat pipes or thermally conductive strips between respective diode node points and the constant-temperature heat sink. An electrical analog of this model is shown in *Figure 3*. Temperature profiles for the thermally conductive strips in the header are evaluated individually by a solution procedure similar to the one previously developed. The only difference is that there is no heat generation or loss within the header material. Otherwise the solution procedures are the same.

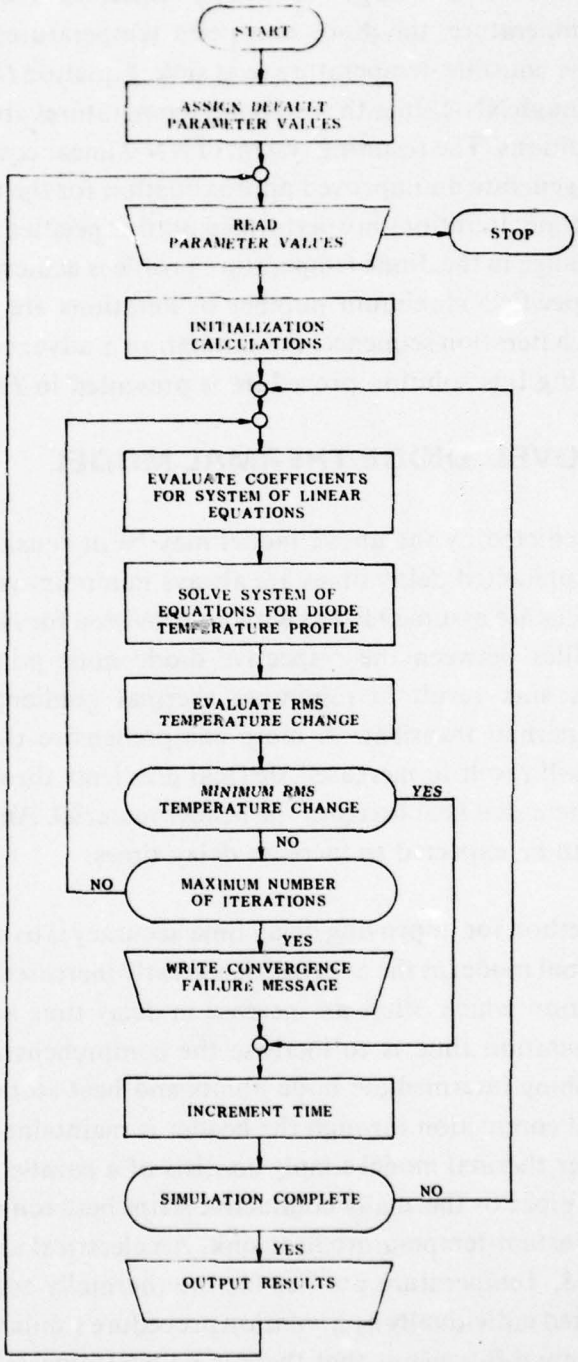

Figure 2. Flow chart for improved quasi-two-dimensional diode thermal model.

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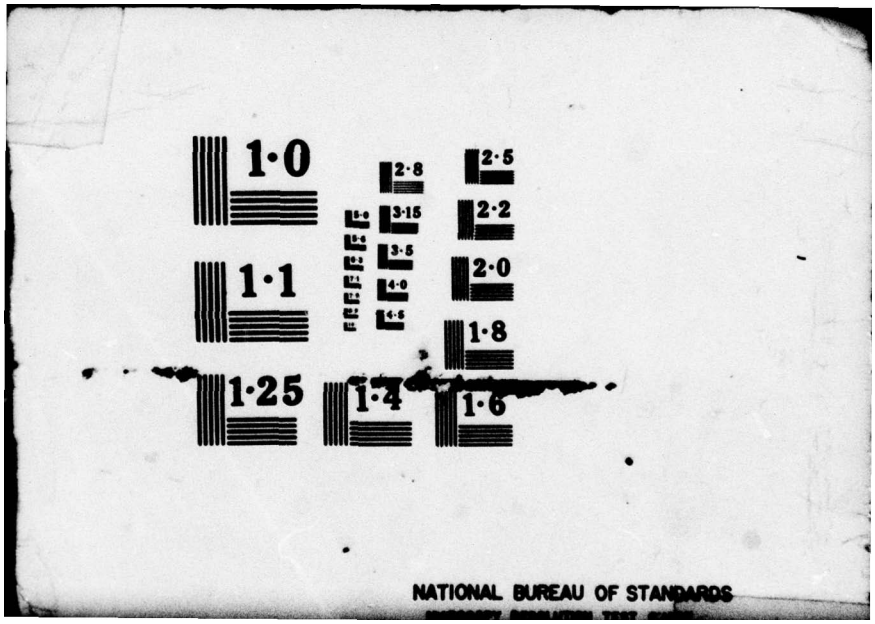
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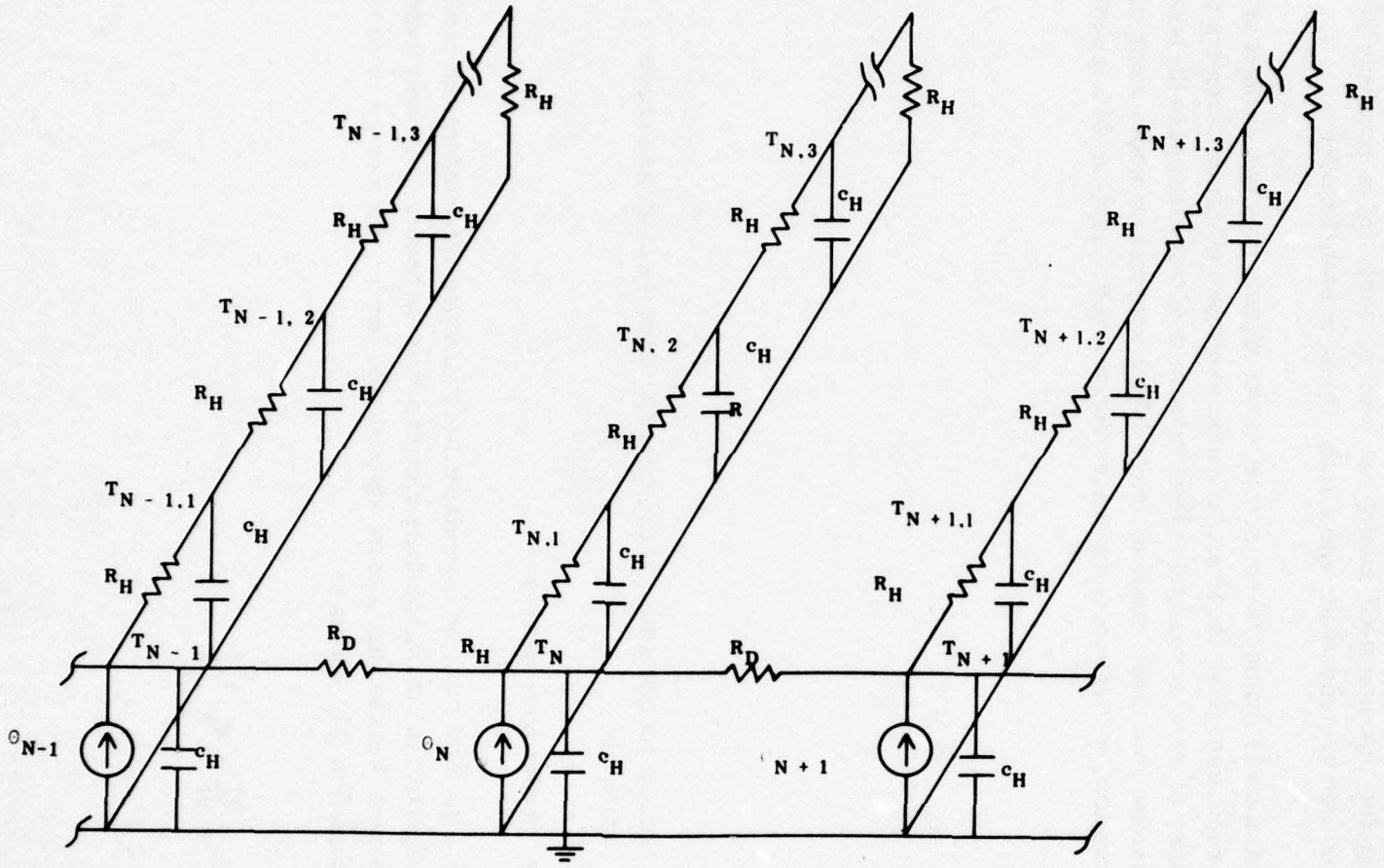

Figure 3. Electrical analog of improved quasi-two-dimensional diode thermal model. (Symbols same as Figure 1 and c_H-header heat capacity).

The absence of lateral thermal conduction within the header material is a shortcoming for this improved model but also accounts for a relatively short computation time in comparison with a fully two-dimensional model.

Implementation of the improved thermal model requires only two changes in the previous formulation. First, the header constant temperature heat sink temperature, T_o, in Equation (2) must be changed to the temperature of the first node in the header material because this model contains intermediate temperature nodes along each thermally conductive strip across the header. Accordingly, Equation (2) is rewritten as:

$$\Phi \equiv \frac{K_H}{x_{DT}} \quad \frac{T - T_H}{\Delta x_H} \tag{5}$$

where

T_H = header temperature at the interface between the diode and header materials.

Δx_H = header node spacing.

Second, an algorithm must be formulated for evaluating the temperature profiles along the respective thermally conductive strips across the header. Since only thermal conduction with heat storage occurs through the header, the energy continuity equation, Equation (1), reduces to

$$\rho_H \, c_H \frac{\partial T}{\partial t} = K_H \frac{\partial^2 T}{\partial x^2} \tag{6}$$

where

ρ_H → header material density

c_H = header material heat capacity

K_H = header material thermal conductivity.

As with the first model formulation, all temperature values are referenced to the temperature of the constant-temperature heat sink. Accordingly, the two end point temperatures are specified as the corresponding diode temperature and zero, respectively.

The numerical algorithm for solving Equation (6) is developed using the same techniques as used above for thermal conduction along the diode axis. The resulting system of linear equations can be written as:

$$A_1\, T(N-1)^{s+1} + A_2 T(N)^{s+1} + A_3\, T(N+1)^{s+1} = A_4 \qquad (7)$$

where

$$A \equiv \frac{K_H}{c_H \rho_H}$$

$A_1 = \Delta t A$

$A_2 = -(\Delta x_H^2 + 2\Delta t A)$

$A_3 = \Delta t A$

$A_4 = -\Delta x_H^2\, T(N)^s$

This algorithm is used at the end of each time step computational sequence to update the respective header temperature profiles. *Figure 4* shows a flow chart for this improved quasi-two-dimensional diode thermal model. Note that the only difference between this flow chart and the flow chart for the first model is the addition of a call to the header temperature subprogram.

D. SIMULATION RESULTS

Several different test cases were executed to check the performance of the new program. Steady-state temperature profiles were evaluated for different diode configurations yielding the anticipated temperature profiles. The transient performance was checked by simulating a thermal second breakdown transient performed by the comprehensive diode model which required some 25 minutes of computer time on a Univac 1110 computer system. The more comprehensive diode model solved the hole and electron continuity equations, Poisson's equation, and the energy continuity equation simultaneously, thus accounting for the long execution time. The thermal model for the big simulation was the simplified quasi-two-dimensional model described earlier. In this simulation, the diode and header thermal conductivities were assigned near zero values to cause high diode temperatures at a low diode current density in order to prevent excessive space charge induced deplection region widing. The maximum electric field intensity and depletion region boundaries were extracted from the big simulation in the quasi-stable region of the second breakdown transient. These values were then used to define a similar simulation for the program developed here.

The onset of thermal second breakdown for the big simulation occurred at approximately 134 μs into the simulation. The program presented here achieved the same maximum temperature with similar temperature profiles at 110 μs into the simulation and required only 15 seconds of execution time on a Univac 1106 computer system. The resulting thermal transients and temperature profiles for the two simulations are shown in *Figures 5* through *8*. The predicted delay times agree well considering the difference in model complexity and execution times.

The inability to predict thermal second breakdown delay times as a function of diode design and current density for the big simulation program has been a handicap in view of its long execution time. The program developed above

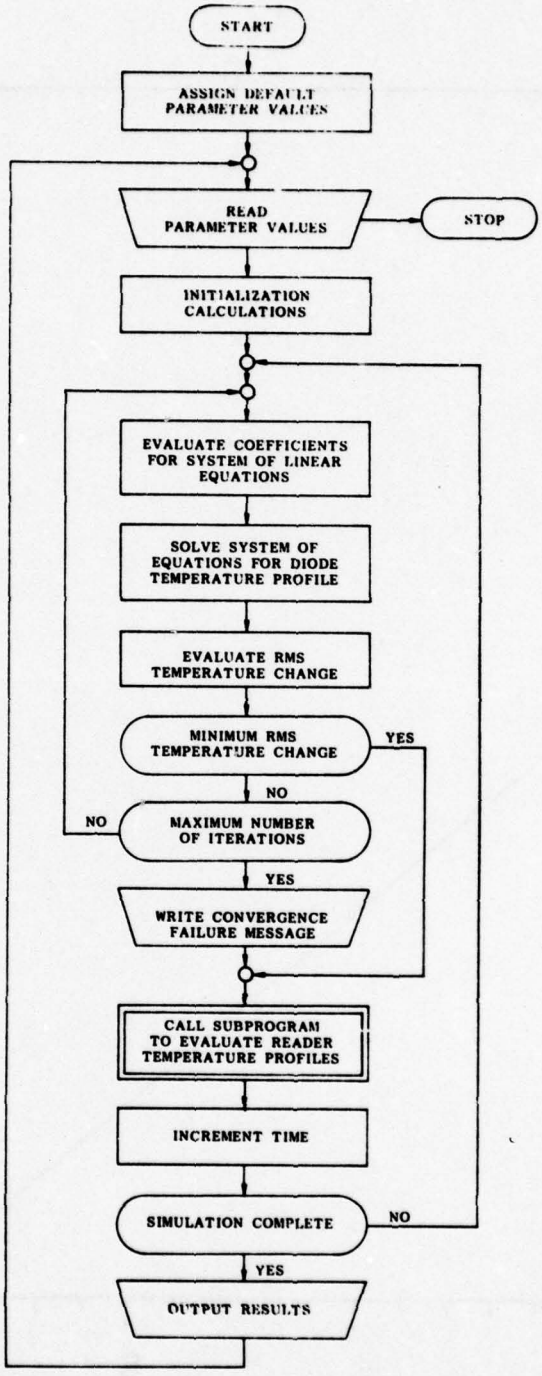

Figure 4. Flow chart for improved quasi-two-dimensional diode thermal model.

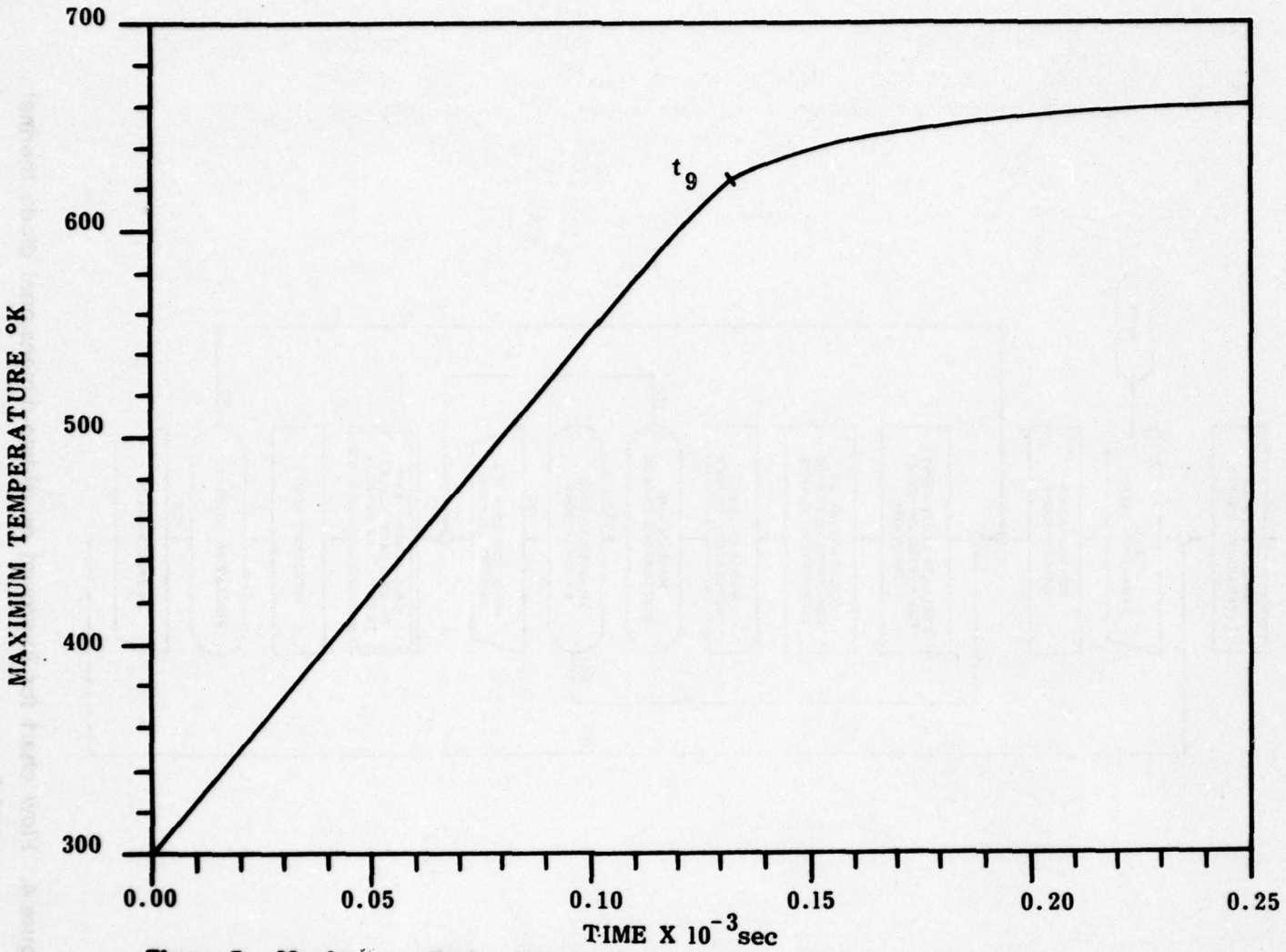

Figure 5. Maximum diode temperature versus time for comprehensive diode model ($t_9 = 1.35 \times 10^{-4}$ seconds).

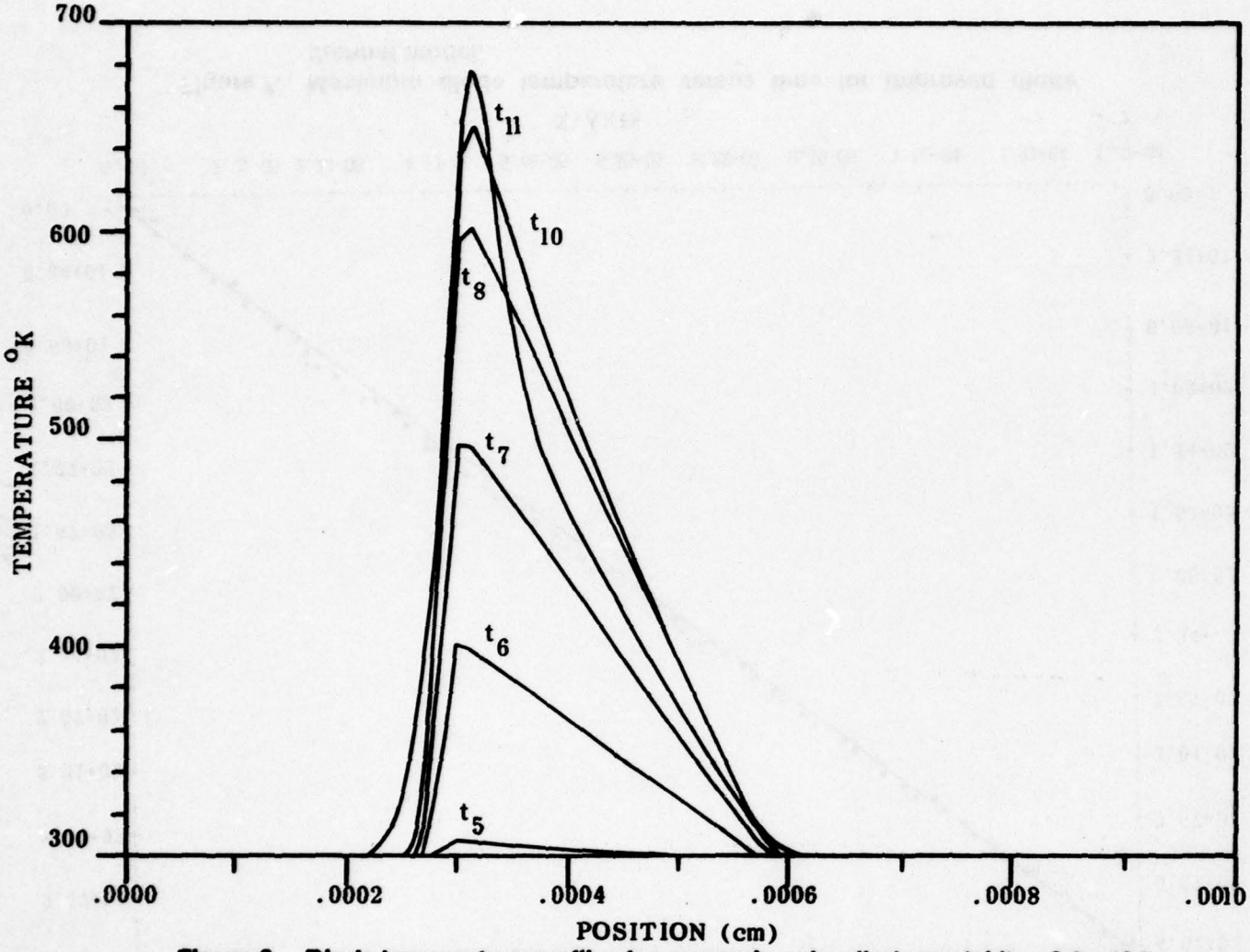

Figure 6. Diode temperature profiles for comprehensive diode model ($t_5 = 3.0 \times 10^{-6}$, $t_6 = 4.0 \times 10^{-6}$, $t_7 = 7.82 \times 10^{-6}$, $t_8 = 1.2 \times 10^{-4}$, $t_{10} = 1.78 \times 10^{-4}$, $t_{11} = 1.11 \times 10^{-3}$ seconds).

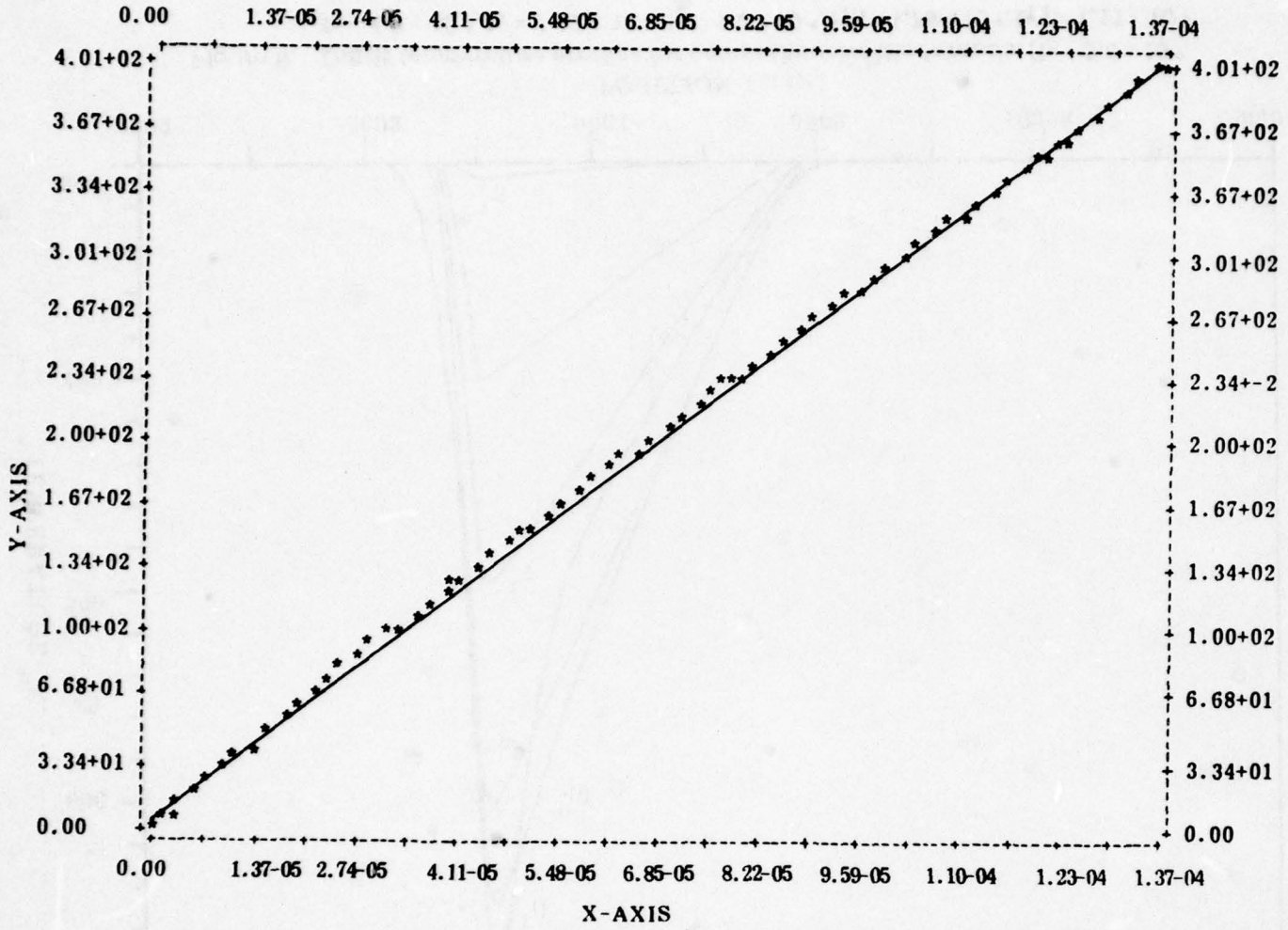

Figure 7. Maximum diode temperature versus time for improved diode thermal model.

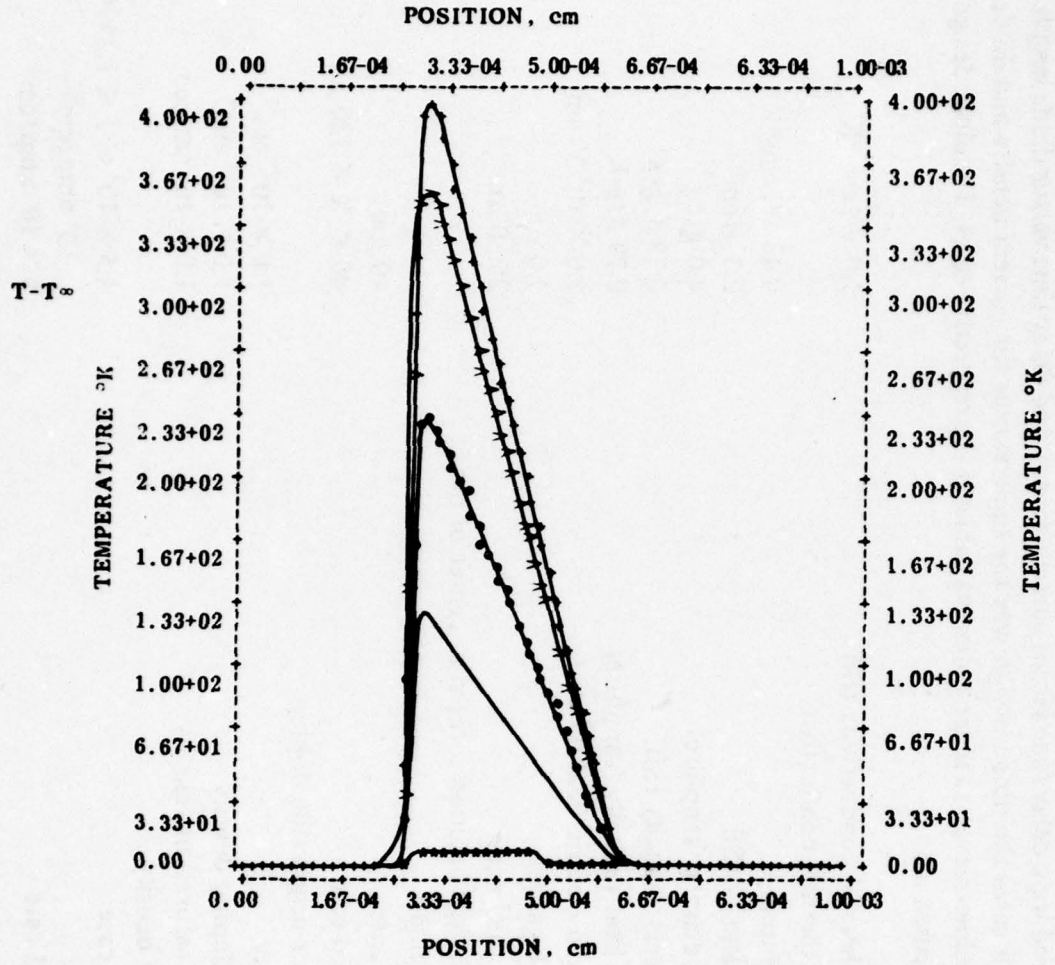

Figure 8. Diode temperature profiles for improved diode thermal model ($t_1 = 3.0 \times 10^{-6}$, $t_2 = 4.0 \times 10^{-6}$, $t_3 = 7.82 \times 10^{-5}$, $t_4 = 1.2 \times 10^{-4}$, $t_5 = 1.37 \times 10^{-4}$ seconds).

should be particularly beneficial in defining simulations for the more comprehensive diode model.

Additional data was collected to characterize the new model and to define valid regions of operation for the more comprehensive diode model. The two cases considered were delay time versus current density and delay time versus diode length. For both cases the diode design was the same except for current density and diode length, which served as independent variables in the respective cases. The diode design was specified as:

Diode thermal conductivity (Si)	1.0 W/cm-°K
Header thermal conductivity (sapphire)	0.46 W/cm-°K
Diode density (Si)	$2.3\ g/cm^3$
Header density (sapphire)	$4.0\ g/cm^3$
Diode heat capacity (Si)	0.79 J/g-K
Header heat capacity (sapphire)	0.79 J/g-K
Maximum electric field intensity	5.0×10^5 V/cm
Diode thickness	1.0 μm
Header thickness	250.0 μm
Metallurgical junction located at center of diode	
Diode length	
First case	40 μm
Second case	$40 \leqslant X \leqslant 120\ \mu m$
Lower or origin side doping density	$1.0 \times 10^{17}\ cm^{-3}$
Upper doping density	$1.0 \times 10^{16}\ cm^{-3}$
Carrier saturation velocity	1.0×10^7 cm/sec
Current density	
First case	$4.5 \times 10^3 \leqslant J \leqslant 1.25 \times 10^4\ amp/cm^2$
Second case	$5 \times 10^3\ amp/cm^2$
Diode node points	101
Header intermediate node points	
First case	
Curve 1	0
Curve 2	0
Curve 3	12

Second case	
Curve 1	0
Curve 2	12
Maximum simulation temperature	
Scaled	400° K
Absolute	700° K

For the purpose of these simulations, the thermal second breakdown delay time is defined to be that time required for the diode to achieve a maximum temperature of 700° K. Assuming that the header constant temperature head sink is maintained at 300° K, the corresponding scaled temperature for the simulations is 400° K. Then onset of thermal second breakdown is assumed to occur when the simulation reaches 400° K.

The delay time versus current density results are shown as three curves in *Figure 9*. Curve No. 1 represents no heat loss into the header. Only thermal conduction along the diode axis is allowed. Curve No. 2 represents thermal conduction into the substrate according to the simplified quasi-two-dimensional thermal model. Note that this model is essentially ineffective for representing heat loss into the header. Curve No. 3 represents the improved quasi-two-dimensional model employing 12 node points in the header. In the long delay time region, the improved model predicts delay times two orders of magnitude greater than the previous two cases. Hence, a substantial improvement in simulating thermal conduction into the header material is demonstrated. Further, curve No. 3 displays two inflection points which are attributed to the interaction of the diode and header conduction mechanisms. For delay times longer than 20 μs, thermal conduction into the header tends to dominate the delay time, whereas conduction along the diode axis dominates for delay times less than 20 μs.

The three curves for delay time versus current density are limited by an infinite delay time for current densities of less than approximately 4.5×10^3 amp/cm^2 and a depleted bulk region for current densities greater than approximately 1.25×10^4 amp/cm^2.

The delay time dependence on diode length is demonstrated in *Figure 10*. In this figure, curve No. 1 represents the simplified thermal model while curve No. 2 represents the improved thermal model. These results demonstrate a strong delay time dependence on diode length when bulk regions are narrow. Hence,

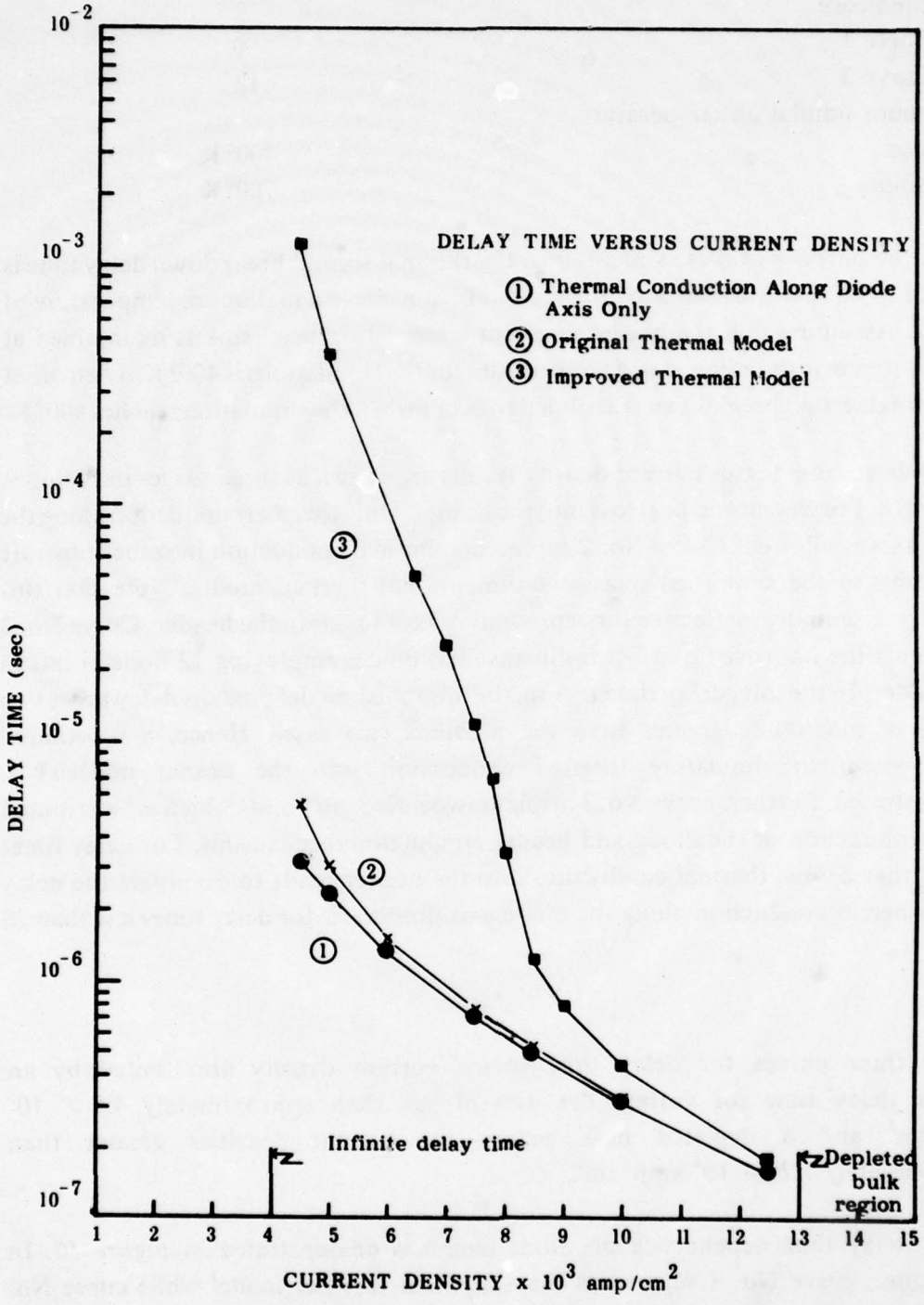

Figure 9. Thermal second breakdown delay time versus current density.

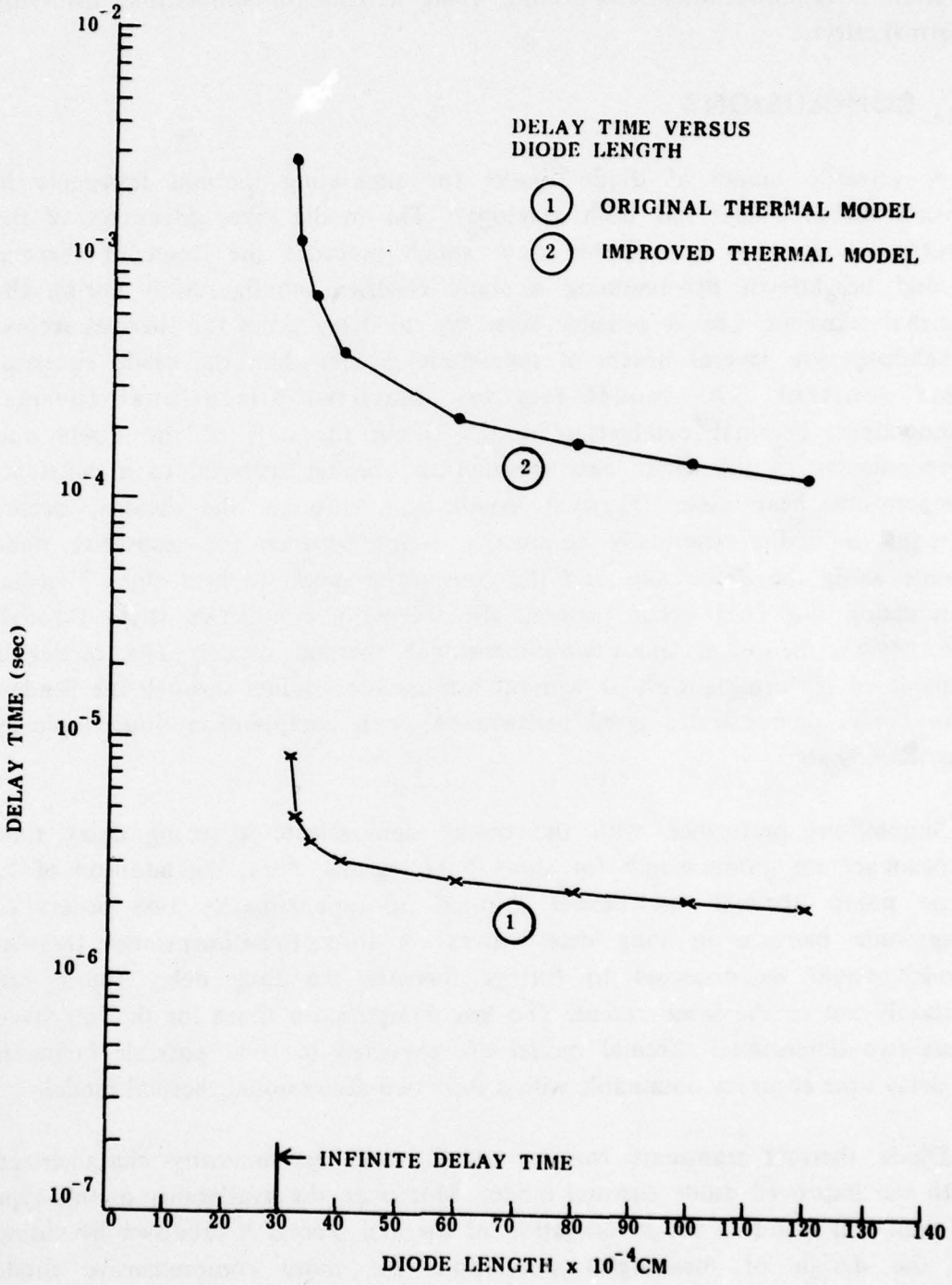

Figure 10. Thermal second breakdown delay time versus diode width.

caution is required when establishing diode lengths for simulations involving thermal effects.

E. CONCLUSIONS

A versatile numerical diode model for simulating thermal transients in reverse biased diodes has been developed. The model takes advantage of the electrically dormant quasi-stable state which precedes the onset of thermal second breakdown by assuming a static electrical configuration during the thermal transient. This is possible since typical delay times for thermal second breakdown are several orders of magnitude greater than the diode electrical time constant. The model features quasi-two-dimensional thermal conduction. Thermal conduction occurs along the axis of the diode and perpendicular to the diode axis through the header material to a constant-temperature heat sink. Thermal conduction through the header occurs through individual thermally conductive strips between the respective node points along the diode axis and the constant-temperature heat sink. Thermal conduction does not occur between the thermally conductive strips through the header; hence, a quasi-two-dimensional thermal model. The model is capable of performing with or without intermediate points through the header. The model demonstrates good performance with computation times typically less than 30 sec.

Simulations performed with the model demonstrate a strong delay time dependence on diode length for short bulk regions. Also, the addition of 12 node points through the header resulted in approximately two orders of magnitude increase in long delay times. A fully two-dimensional thermal model would be expected to further increase the long delay times, but certainly not to the same extent. The low computation times for the improved quasi-two-dimensional thermal model are expected to rival possible increases in delay time accuracy obtainable with a fully two-dimensional thermal model.

Diode thermal transients can be quickly and economically characterized with the improved diode thermal model. Moreover, the availability of this type of data will facilitate the investigation of thermal second breakdown by aiding in the design of meaningful simulations for more comprehensive diode models.

The improved diode thermal model will be made more useful for the investigation of thermal second breakdown by adding an algorithm to evaluate the thermal generation current component at the end of each time step. The increased computation time will be small. The program will determine the delay time directly by terminating the simulation when the thermal generation current becomes equal to the driving current. A modification to accept user-defined impurity profiles will allow simulations with varied and more realistic doping profiles. Implementation of a fully two-dimensional diode thermal model similar to the model developed here will also allow a direct comparison to ascertain the relative merits of the two models.

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7. APPROXIMATE ANALYSIS OF P-N JUNCTIONS UNDER HIGH ELECTRICAL OVERSTRESSES*

A. INTRODUCTION

The analysis of a p-n junction diode when subjected to both thermal and electrical stresses is extremely involved. Exact solutions are essentially unobtainable either by hand calculations or computer techniques. Therefore, approximations are required. Some of these approximations will be investigated. Although these approximations will have varying degrees of simplifications, conclusions can be drawn about the behavior of practical devices.

In general one can write the energy balance equation in a differential volume as: [the rate of increase in thermal energy] = [the rate of thermal energy production] + [the rate of thermal energy in] - [the rate of thermal energy out]. This is an electrothermal equation where the temperature will be a function of three-dimensional space and time. It will contain electrical and thermal coefficients which are, in turn, nonlinear functions of temperature. Empirical data can be obtained for the electrical and thermal coefficients. These values are then used in the energy balance equation and temperature is solved for as a function of space and time. The desired electrical equations are then written and solved to find, for example, the terminal voltage-current relation as a function of time. In practice this can be done only for greatly simplified cases and then sometimes very involved computer techniques are required.

The thermal generation term in the energy balance equation may be due to a number of causes. In this study we are primarily concerned with that due to electrical current flow although the effects of ionizing radiation will also be considered. The general approach used in this study is to look at one aspect of the problem at a time. In this way one can isolate the various contributions to thermal second breakdown and get good approximate hand solutions for specific cases. If each contribution is understood, then one can get a feeling for the overall problem even though each contribution is expected to have some influence on the others.

Some of the particular cases that will be considered are (1) the steady-state case where conductivity is not a function of temperature, (2) the steady-state

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case where the conductivity is an assumed function of temperature and (3) the transient case with negligible thermal conductivity. A comparison of critical temperatures for current constriction and junction "wash out" and an analysis of where "hot spots" are most likely to occur is also given.

B. STEADY-STATE CASE

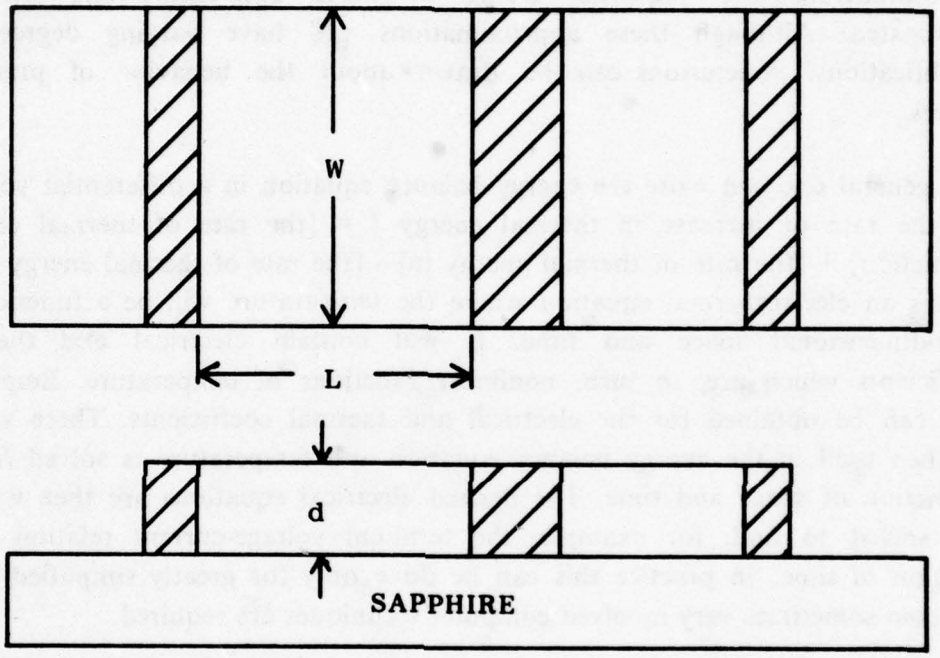

Figure 1. SOS, p-n junction diode.

For the steady-state case the energy balance equation where the energy generated is due to current flow can be written as [the electrical power] = [the thermal power out] - [thermal power in]. For a strip ΔZ in the above diode this can be written symbolically as:

$$LWJE\Delta Z = LW\phi_{z+\Delta z} - LW\phi_z \quad . \tag{1}$$

Dividing through by $LW\Delta Z$ and taking the limit as $\Delta Z \rightarrow 0$ gives

$$JE = \lim_{\Delta z \to 0} \frac{\phi_{z+\Delta z} - \phi_z}{\Delta z} = \frac{d\phi}{dz} \quad . \tag{2}$$

This is integrated for the case where J and E are not functions of Z to give

$$\phi = JEZ + C_1 \quad . \tag{3}$$

and $C_1 = 0$ if $\phi = 0$ at $Z = 0$.

If we consider that the heat flux is due only to conduction, then $\phi = -K\, dT/dz$. This can then be used in Equation (3) to give

$$T = -\frac{JE}{K} Z^2 + C_2 \quad . \tag{4}$$

If the sapphire substrate is kept at a constant temperature T_o, the constant C_2 is evaluated to give,

$$T - T_o = \frac{JE}{K} (d^2 - z^2) \quad . \tag{5}$$

For this simplified case the maximum temperature would be at the surface. It would be proportional to the current density and electric field and inversely proportional to the thermal conductivity. For semiconductors in the temperature range of interest, thermal and electrical conductivities are functions of temperature. Heat flow in the other two directions may also be important. It can be seen from the above result that the top part of the device will get the hottest. With sufficiently high current the bulk region will reach the critical temperature at the top. This will cause a decrease in resistivity there. All the current will tend to flow in a small layer near the surface and hence will probably be funneled into a small filament. A rough estimate of the current density needed to cause filamentation can be obtained from Equation (5) by taking $T - T_{cr}$, $Z = 0$, and $E = \rho_{max} J$, which gives,

$$J_{cr} = d \left[\frac{K}{\sigma_{max}} (T_{cr} - T_o) \right]^{\frac{1}{2}} \quad . \tag{6}$$

Next assume that the electrical conductivity is a function of temperature but the thermal conductivity is not. For this case it is more convenient to work with a constant voltage pulse. To a good approximation the conductivity can be

written as $\sigma\ (T) = \sigma_{cr} + a\ (T - T_{cr})^2$ where the values of σ_{cr}, a, and T_{cr} can be obtained from experimental curves. Then, writing the electric field V/L Equation (2) can be written as

$$\left(\frac{V}{L}\right)^2 \left[\sigma_{cr} + a\ (T - T_{cr})^2\right] = - K \frac{d^2T}{dz^2} \quad . \tag{7}$$

Now, assume that $T = T_{cr}$ and $\frac{dT}{dz} = 0$ at $z = 0$ and expand T in a power series about $z = 0$, i.e.,

$$T = T_{cr} + b_1 Z + b_2 Z^2 + b_3 Z^3 + - - - - - - - - .$$

Then

$$(T - T_{cr})^2 = b_1^2\ Z^2 + 2\ b_1 b_2 Z^3 + (2\ b_1 b_3 + b_2^2)\ Z^4 + - - - - -$$

$$\frac{dT}{dZ} = b_1 + 2\ b_2 Z + 3\ b_3 Z^2 + 4\ b_4 Z^3 + - - - - -$$

$$\frac{d^2T}{dZ^2}\ \ 2\ b_2 + 2.3\ b_3 Z\ + 3.4\ b_4 Z^2 + - - - - - \quad .$$

It was assumed that $dT/dZ = 0$ at $Z = 0$. Therefore, from the expression for dT/dZ above, $b_1 = 0$. The expression for $(T - T_{cr})^2$ and d^2T/dZ^2 above are put into Equation (7) and the coefficients of Z^n are equated. This gives

$$b_2 = - \left(\frac{V}{L}\right)^2 \frac{\sigma_{cr}}{2K}$$

$$b_3 = 0$$

$$b_4 = 0$$

$$b_5 = 0$$

$$b_6 = -a \left(\frac{V}{L}\right)^2 \frac{b_2^2}{6.5} = - \left(\frac{V}{L}\right)^6 \frac{a\sigma cr^2}{120K^2}$$

Then the temperature as a function of Z is given by

$$T = T_{cr} - \left(\frac{V}{L}\right) 2\ \frac{\sigma cr}{2K}\ Z^2 - \left(\frac{V}{L}\right) 6\ \frac{a\ \sigma_{cr}^2}{120\ K^2}\ Z^6 + - - - - . \tag{8}$$

The current density is

$$J = \sigma E = \left[\sigma_{cr} + (b_2 Z^2 + b_6 Z^6 + - -)^2\right]\left(\frac{V}{L}\right) \quad . \tag{9}$$

The total current is obtained by integrating Equation (9) to give

$$I = W_\sigma \int^d J\,(Z)\, d\, Z \quad . \tag{10}$$

C. TRANSIENT CASE — NO HEAT CONDUCTION

For this case assume that the whole device is at some constant temperature T_o, a large voltage pulse is applied and we wish to calculate the time required to raise the temperature to a value T_{cr}. If this is done quickly enough, there will be negligible heat flow away from its generated site. For this case the heat balance equation is

$$\lambda c \frac{\partial T}{\partial t} = JE \quad . \tag{11}$$

Again we will assume a constant voltage pulse with $J = \sigma E$. This time we will assume that we can write $\sigma = \sigma_o + b\,(T - T_o)^2$, which should be a good approximation for $T_o < T < T_{cr}$. This time we will expand T in a power series of time about T_o according to

$$T = T_o + \alpha_1 t + \alpha_2 t^2 + \alpha_3 t^3 + - - - \quad .$$

Then

$$\frac{\partial T}{\partial t} = \alpha_1 + 2\alpha_2 t + 3\alpha_3 t^2 + 4\alpha_4 t^3 + - -$$

and

$$(T - T_o)^2 = \alpha_1^2 t^2 + 2\alpha_1\alpha_2 t^3 + (2\alpha_1\alpha_3 + \alpha_2^2)\, t^4 + - - - - \, .$$

Putting these relations back into Equation (11) gives

$$\lambda c\, (\alpha_1 + 2\alpha_2 t + 3\alpha_3 t^2 + 4\alpha_4 t^3 + - -)$$
$$= \left(\frac{V}{L}\right)^2 \sigma_o + b\,\alpha_1^2 t^2 + 2b\alpha_1\alpha_2 t^3 + b\,(2\alpha_1\alpha_3 + \alpha_2^2) t^4 + - - - \quad .$$

Equating coefficients of t^n gives

$$\alpha_1 = \left(\frac{V}{L}\right)^2 \frac{\sigma_o}{\lambda c}$$

$$\alpha_2 = 0$$

$$\alpha_3 = \left(\frac{V}{L}\right)^2 \frac{b}{\lambda c}\,\alpha_1^{\,2}$$

$$\alpha_4 = \left(\frac{V}{L}\right)^2 \frac{b(2\alpha_1\alpha_3 + \alpha_2^{\,2})}{5\lambda c}$$

$$\alpha_5 = \left(\frac{V}{L}\right)^2 \left(\frac{b}{\lambda c}\right) 2\alpha_1\alpha_3 \quad .$$

The temperature as a function of time is

$$T = T_o + \alpha_1 t + \alpha_3 t^3 + \alpha_5 t^3 + - - - \quad .$$

This can be plotted as a function of time to find the time required to raise T to T_{cr}, which is the time that channelization is expected to start.

The current as a function of time can also be obtained according to

$$I = dWJ = dW \left(\frac{V}{L}\right) \left[\sigma_o + b\,(T - T_o)^2\right] \quad . \tag{12}$$

D. DEPLETION REGION VERSUS BULK REGION

A discussion is given on the relative influence of the depletion region and the bulk region in causing thermal second breakdown of abrupt one-sided p-n diodes.

The first breakdown voltage of a p-n junction diode can be very closely approximated by solving Poisson's equation. For an abrupt one-sided junction the breakdown voltage is given by

$$V_{br} = \frac{\varepsilon E_{cr}^{\,2}}{2qN} \quad , \tag{13}$$

where E_{cr} is the critical value of the electric field and N is the doping in the lightly doped side. If the current is increased sufficiently in the first breakdown state, the device will be heated, eventually reaching a high enough

temperature in some region of the diode to cause a sudden switch to a lower-voltage second breakdown state. This second breakdown state might lead to degradation or destruction of the diode, depending on the doping, geometry and heat sinking.

As will be shown, there are two regions of the diode that are affected in the second breakdown process - the lower doped bulk region and the depletion region. Once the depletion reaches a certain temperature, it will become "intrinsic" and the junction will be "washed out," i.e., the junction will no longer exist and hence cannot support a voltage. Therefore, this is a form of thermal second breakdown. This process is strictly a quasi-equilibrium state and is not degrading to the device in itself. The drop in voltage may, however, cause an increase in current that will in turn cause degradation or destruction of the device.

Since the resistivity of the bulk region of the diode is also temperature dependent it can contribute to thermal second breakdown. This can be explained by the fact that for any doping density the resistivity will first increase with increasing temperature, reach a maximum, and then decrease. Because of the construction of the diode (doping, geometric effects, etc.) it is expected that nearly always some portion of the bulk region will reach the critical temperature corresponding to maximum resistivity before the rest of the region does. This will tend to cause all the current of the diode to "funnel" through this small channel. The sudden increase in current density will cause a much larger increase in temperature, which can lead to a melt and a destruction of the diode.

The critical temperatures for second breakdown due to junction or bulk effects can be determined from calculations or experimental data. Second breakdown of the junction will occur at approximately the temperature at which the intrinsic carrier density reaches the doping density. For an n-type material the intrinsic carrier density is given by

$$n_i = N_c \exp\left[-(W_c - W_i)/kT\right] = AT^{3/2} e\left[-(W_c - W_i)kT\right] \qquad (14)$$

where A is a constant. To calculate n_i as a function of temperature, N_c was taken as $2 \times 10^{19}/cm^3$ at $T = 300°$ K and $W_c - W_i$ was taken as 0.55 eV independent of

temperature. *Figure 2* shows a plot of $n_i=N_D$ vs T. Also shown in *Figure 2* is a plot of N_D for maximum resistivity versus T. It is observed that over most of the range of doping density of interest, the temperature required for maximum resistivity is about 100° K less than that of the intrinsic temperature.

This is not to say that for a given device the "turn over" temperature of maximum resistivity being lower will always be reached first and hence a current constriction process is what controls thermal second breakdown. Limiting cases of this problem can be analyzed as follows. For current pulses much larger than the thermal time constants, all regions of the diode should reach approximately the same temperature and the bulk effect would dominate since it would occur at the lower temperature.

For current pulses short compared to the thermal time constant, essentially all of the electrical power dissipated goes into heating the small region in which it is dissipated - none being transmitted to other regions or out of the device. Hence the temperature rise in any small region will be proportional to the electrical power dissipated there for a given pulse width. The maximum electrical power density in the junction can be written as

$$P_j \text{ (max)} = JE_{cr} \quad . \tag{15}$$

The maximum electrical power density in the bulk can be written as

$$P_b \text{ (max)} = \rho_{max} J^2 \quad . \tag{16}$$

For the same temperature rise in the two regions the expressions of Equation (15) and (16) are equated. This gives

$$J = \frac{E_{cr}}{\rho_{max}} \quad . \tag{17}$$

This value of current density versus doping density is plotted in *Figure 3*. The interpretation of this plot is as follows. If for a given doping density the corresponding current density of the short current pulse falls below the line, the junction will get the hottest and the junction will probably go intrinsic before current constriction occurs in the bulk region. If, on the other hand, the current density falls above the line, the bulk region will get the hottest and current constriction will occur first. It might be mentioned here that the graphs

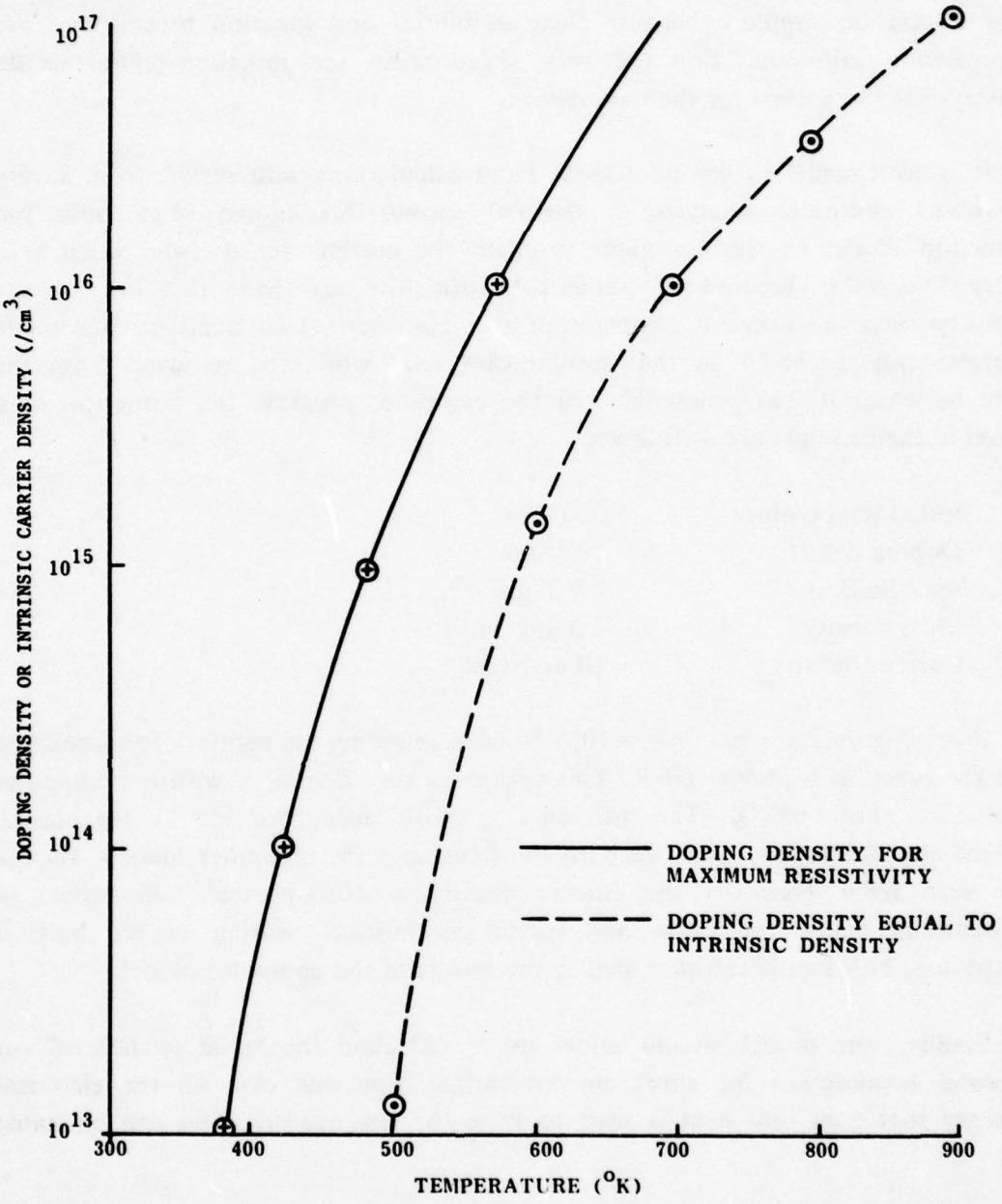

Figure 2. A comparison of temperatures for maximum resistivity and intrinsic density.

herein were calculated using data of bulk silicon and would have to be altered for silicon on sapphire because their mobilities and junction breakdowns are appreciably different. For the very short pulse the junction region would always get the hottest for the bulk devices.

It is worthwhile to compare these hand calculations with results from a very involved computer analysis of thermal second breakdown of a bulk p-n junction diode. In the computer problem the current density was taken at a very low value because of numerical difficulties. To have this low current density cause a sufficient temperature rise, the thermal conductivity was made correspondingly small so that insignificant heat would be removed from the site in which it was generated. For the computer program the numerical data used in the example are as follows:

Initial temperature	300° K
Doping density	$10^{16}/cm^3$
Specific heat	0.7 J/gm $^{-}$°K
Mass density	2.3 gm/cm^3
Current density	10 amp/cm^2

From *Figure 2* for $n_i = N_D = 10_{16}$ the corresponding temperature for a collapse of the junction is about 700° K. This compares very favorably with the computer value of about 680° K. The difference is easily accounted for by the several slight approximations made in both the hand and the computer models. As can be seen from *Figure 3* the current density of 10 amp/cm^2 falls orders of magnitude below the curve and hence insignificant heating in the bulk is expected. This fact is substantiated in the results of the computer model.

Finally, our model should allow us to calculate the "time to failure" (or second breakdown) for short current pulses. For this case all the electrical energy that goes into heat is used to raise the temperature. This can be stated as

$$JE_{cr}\Delta t = P_c\Delta T, \tag{18}$$

or

$$\Delta t = \frac{P_c\Delta T}{JE_{cr}} \quad . \tag{19}$$

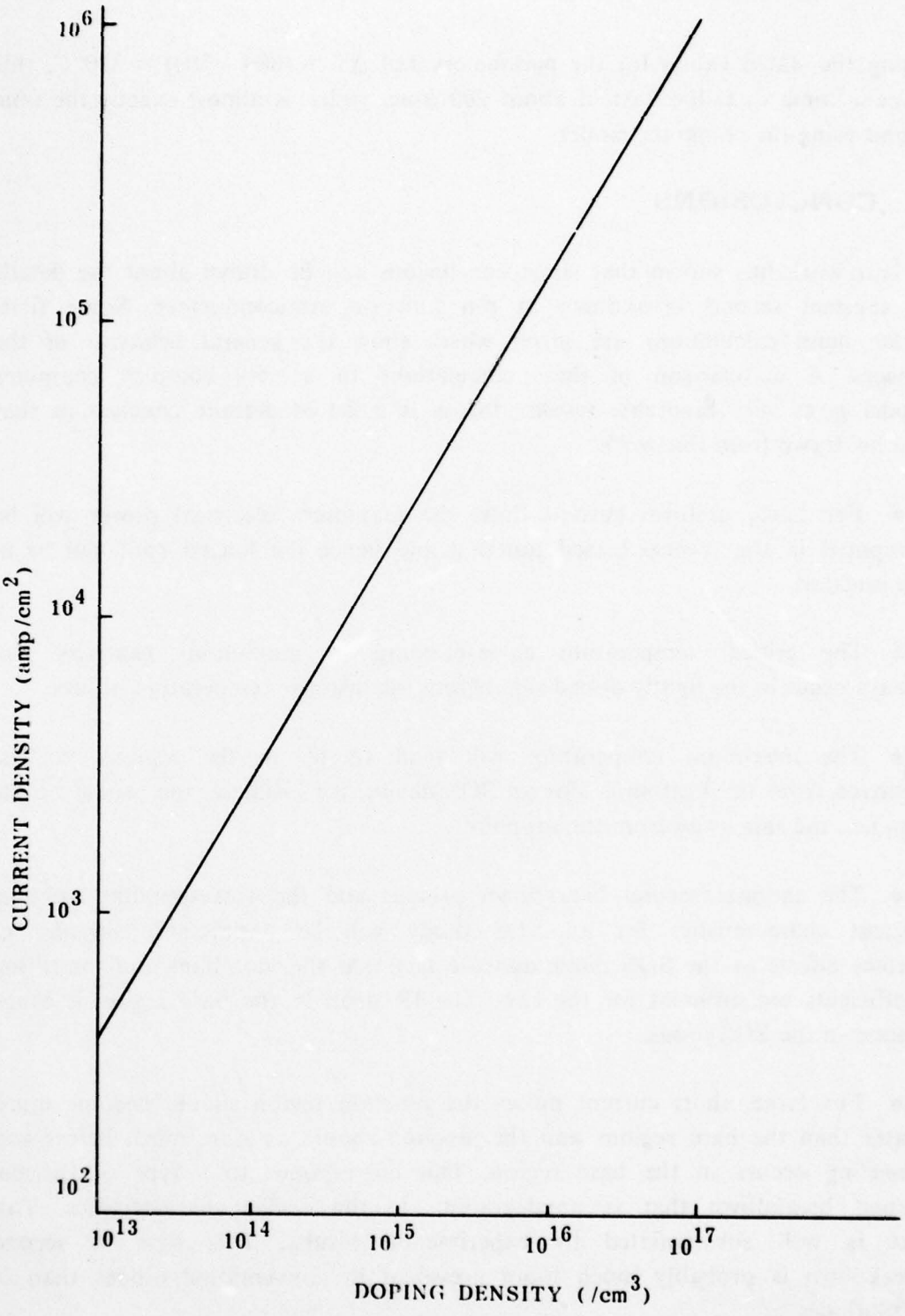

Figure 3. Current density for equal power densities in base and junction.

Using the stated values for the parameters and $\Delta T = (680 - 300) = 380°C$, this gives a "time to failure" Δt of about 200 μsec, which is almost exactly the time found using the computer model.

E. CONCLUSIONS

This work has shown that some conclusions can be drawn about the details of thermal second breakdown in p-n junction semiconductors. Some first-order hand calculations are given which show the general behavior of the devices. A comparison of these calculations to a very complex computer model gives very favorable results. Below is a list of definite conclusions that can be drawn from this work:

- For fairly uniform current flow, the maximum electrical power will be dissipated in the reverse biased junction and hence the hottest spot will be in the junction.

- The critical temperature corresponding to maximum resistivity will always occur in the lightly doped side before the intrinsic temperature occurs.

- The maximum temperature will tend to be in the regions farthest removed from the heat sink. For an SOS device, for example, this would be the top, i.e., the side away from the sapphire.

- The thermal second breakdown process and the corresponding voltage-current characteristics for an SOS diode will be appreciable because of surface effects in the SOS diode and the fact that the mobilities and ionization coefficients are different for the two. The IR drop in the base region is much greater in the SOS diode.

- For large, short current pulses the junction region should become much hotter than the base regions and the junction should collapse much before any funneling occurs in the base region. This corresponds to a type of thermal second breakdown that is nondegrading to the device characteristics. This fact is well substantiated by experimental results. This type of second breakdown is probably much more prevalent in conventional diodes than in SOS diodes.

- For small, long current pulses appreciable heat can flow in the diodes and hence the temperature tends to be much more equal in the base and in the junction. For this case the lightly doped base region will reach its critical temperature before the junction and hence there will be a tendency for the current to funnel into a small region and cause a melt channel. This process generally leads to a degrading or destruction of the device characteristics. This type of breakdown is expected to occur more in SOS diodes than in conventional diodes.

- Ionizing radiation should tend to decrease the susceptibility of diodes to second breakdown. The effect should be more noticeable in the base region than in the junction and, hence, more pronounced in SOS diodes than in conventional diodes. This is because ionizing radiation creates excess carriers and decreases the effective resistance.

LIST OF SYMBOLS

C	Specific heat
E	Electric field
I	Electric current
J	Current density
J_{cr}	Critical current density
K	Thermal conductivity
N	Doping density
N_D	Donor doping density
n_i	Intrinsic carrier density
P	Electrical power density
P_j	Power density in junction
P_b	Power density in base
q	Magnitude of the electronic charge
k	Boltzmann's constant
T	Temperature
t	Time
V	Voltage
W	Energy
λ	Mass density
ϵ	Permittivity
π	Electrical resistivity
σ	Electrical conductivity
σ_c	Critical electrical conductivity
σ_o	Electrical conductivity at room temperature
ϕ	Heat flux

8. ANOMALOUS VOLTAGE RESPONSE OF DIODES PULSED WITH HIGH CURRENTS*

A. INTRODUCTION

In previous research on the vulnerability of semiconductor junction devices, diodes and transistors, to electromagnetic pulses, it was experimentally observed that when a junction was pulsed with a very intense nonrepeating current pulse, an anomalously large voltage response was recorded [1]. This voltage response would occur in excess of the junction avalanche breakdown voltage and in some devices but not in others. This response could occur when pulsed in either the forward or reverse case. In all cases the pulse was of a sufficiently short duration and had fast rise and fall times to prevent thermal destruction [1,2] due to melt-channel formation in second breakdown.

The anomalously large voltage response is of great concern when attempting to predict when a device will enter into the second breakdown condition due to an extremely intense but short current pulse. It has been shown that in silicon-on-sapphire (SOS) devices, channel formation is due to the thermal condition of the high resistivity region of a P^+N–N^+ diode [2]. Hence, in the short intense pulse region, the anomalous response increases the instantaneous power and, therefore, total energy into the system. It is then necessary to calculate this anomalous voltage response for all types of junction devices in order to predict the temperature of the junction and when second breakdown will occur.

Present semiconductor modeling such as Ebers-Moll, Charge Control, etc., are adequate for predicting the response of junction devices in the normal operating regions. However, the current levels for permanent damage of semiconductor devices often greatly exceed the normal operating levels and these effects are not modeled by present techniques.

In the early research mentioned previously [1] the problem was to isolate, determine, and predict this anomalous voltage response from the basic physics involved in the device operation. It was felt that such large voltage must come from within the semiconductor itself, thereby eliminating such phenomena as the ohmic contacts and skin effects. This was mainly because the excess voltage could be in the order of "1000 volts for some devices where the avalanche voltage was less than 100 volts."

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The first basic phenomenon to be considered was the conduction mechanism of the N− region as the current density is raised to well beyond the normal levels in silicon. At relatively low current densities bulk silicon will obey Ohm's Law and the average drift velocity of the electron is proportional to the electric field. This proportionality is the drift mobility. If the details of the energy gain of the electrons from the electric field are considered along with the photon scattering, then at larger electric fields and higher current densities, the mobility is reduced and becomes a function of the electric field. Thus for a given current density a larger voltage is detected across the bulk silicon. In the limit, the carrier velocity reaches a scattering-limited value. For electrons in silicon this occurs at an electric field of about 2×10^4 V/cm and a velocity of 10^7 cm/sec. This means that the effective resistance of the N− region increases as the current density is raised, independent of the junction phenomena. This is true with a constant supply of electrons, before avalanching occurs.

For the N− region to conduct more current the electric field must increase to about 2×10^5 V/cm where the ionization coefficients for silicon become greater than unity. This means that the entire N− region must be in avalanche to carry this additional current in the steady state. For a 50 μ thick region this estimates to 1,000 V. If doped to $10^{15}/cm^3$ this would occur at a current density of about $n\ e\ v_d$, which is 1.6×10^3 amp/cm^2 for silicon. Therefore, it was plausible that the main source of the excess voltage response must come from the bulk N− region. To confirm this a solution to the basic device equations in the P+, N−, and N+ regions are necessary. As a first-order estimate to calculate the device voltage at extreme reverse current densities with various doping densities (N_D cm^{-3}) and widths W of the high-resistivity N− region, a numerical solution to the basic device equations was attempted. Since the time necessary for the reverse-biased junction to reach steady state is very short, depending on the scattering-limited velocity of the carriers and the width of the device, a steady-state solution is possible. The steady-state solution requires the simultaneous solution of Poisson's equation and the two carrier continuity equations at every point in the diode. This set of coupled, nonlinear second-ordered differential equations was solved for specific doping and junction widths on a digital computer.

Figure 1 illustrates the solution for the electric field in the N− region doped uniformly at $10^{15}/cm^3$ at various current densities, showing only fields greater than 10^4 V/cm. At lower current densities the electric-field profile is triangular as expected, and a simple case of avalanche breakdown is occurring with $V_B = 320$ V. At current densities near 10^3 amp/cm^2, the entire N− region is avalanching with a resulting maximum in the junction voltage of 1042 V. A further increase in current density

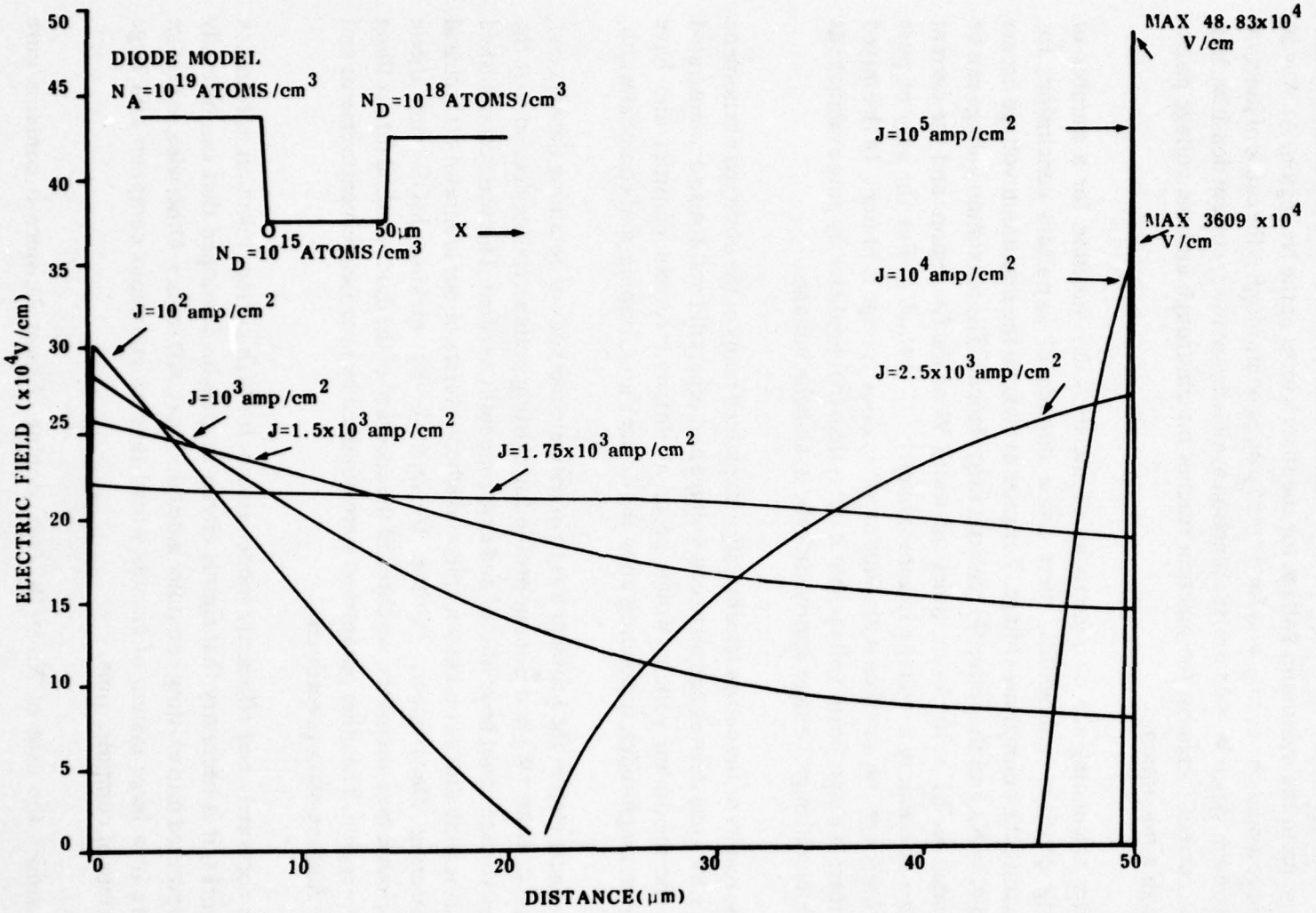

Figure 1. Solution for the electric field in the N-region.

causes a drop in the terminal voltage. *Figure 2* illustrates the current density and voltage up to the maximum voltage for the three widths of the N− region. At W = 50 μm, pure avalanche occurs, and for W = 25 μm, punchthrough is the cause of junction breakdown. When W = 25 μm, the junction avalanches at lower current densities, but, as the current increases, the junction reaches punchthrough and the voltage passes through a maximum.

After calculating the characteristics of the P+N−N+ junction for a number of doping densities and widths, there are a number of important conclusions for estimating the anomalous voltage. For pure avalanche the maximum voltage occurs when $N \simeq N_D$ and the entire N− region is in avalanche. The maximum voltage can be estimated as 2.1×10^5 V/cm times the width W of the N− region, and the current density at maximum voltage is approximately $J_m \simeq N_D e V_d$. For the case of pure punchthrough, no significant amount of anomalous voltage is present. In the mixed case there is a significant voltage, but it is less than that predicted by pure avalanche as the punchthrough voltage approaches the avalanche voltage.

The results of the computer simulation explained many of the observed phenomena as to why some devices had an excess voltage and others did not. It also demonstrated why the maximum voltage would occur at different current densities and have different magnitudes, depending upon the device's area, doping, and epitaxial width.

The next step in the problem was to investigate methods of obtaining the area (A), epitaxial width (W) and doping profile for existing commercial devices so that the excess voltage could be predicted and experimentally verified. This was accomplished by fabricating diodes on known epitaxial silicon wafers in our laboratory (Electrical Engineering Department, Purdue University). By making MOS and diode capacitance measurements, we checked the accuracy of the diode method for profiling the N− region. The other parameters were obtained by microscope measurements and angle lapping-stain procedures.

To accurately and efficiently model devices for high-current injection in complex networks, it is necessary that simple circuit models be developed that can be easily incorporated into existing computer aided design (CAD) codes. Otherwise, to predict failure in a large system of circuits would take an enormous computer and large amounts of computer time.

Consider the case of $N_D = 10^{15}/cm^3$ doping *(Figure 2)*, since it contains pure

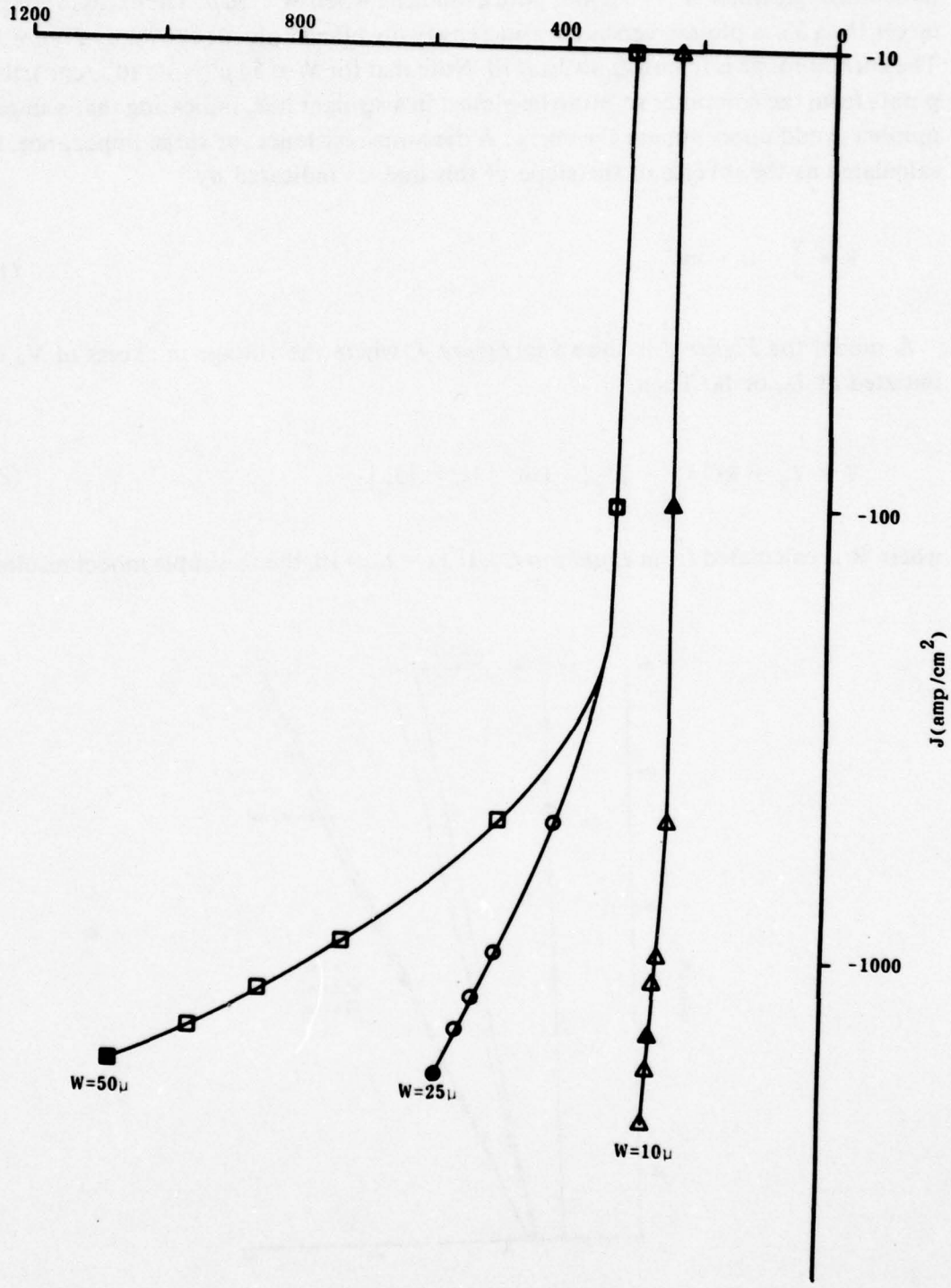

Figure 2. Reverse pulsed.

punchthrough when $W = 10\,\mu$ and pure avalanche when $W = 50\,\mu$. The excess voltage larger than V_B is plotted versus current density on a linear plot as shown by *Figure 3*. The current range is from J_{max} to $J_{max}/10$. Note that for $W = 50\,\mu$ ($N_D = 10^{15}/cm^3$), the points from the computer solution lie almost in a straight line, indicating that a single number could approximate the curve. A dynamic resistance, or surge impedance, is calculated as the inverse of the slope of this line, as indicated by

$$R = \frac{V}{J} \quad \Omega - cm^2 \ . \tag{1}$$

A model for *Figure 3* is shown in *Figure 4*, where the voltage in excess of V_B is initiated at J_B, or I_B. Then,

$$V = V_B + R(|J| - |J_B|) \text{ for } |J| > |J_B| \tag{2}$$

where R is calculated from *Equation (1)*. If $J_B = J_{max}/10$, then a simple model results.

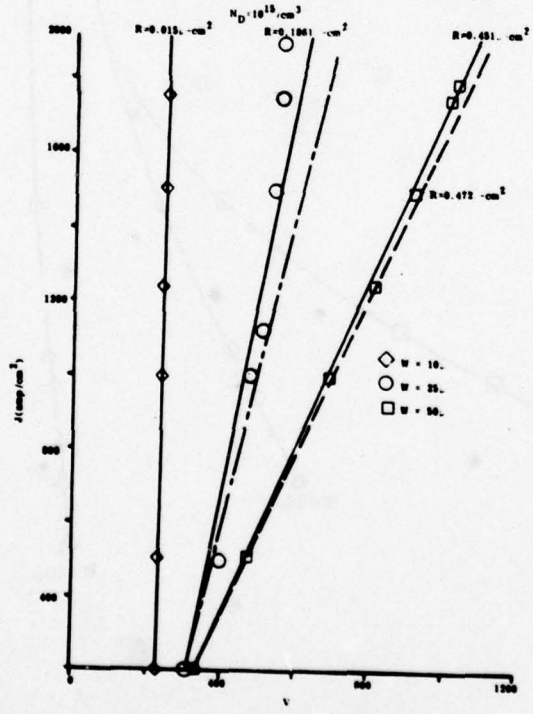

Figure 3. Excess voltage larger than V_B versus current density.

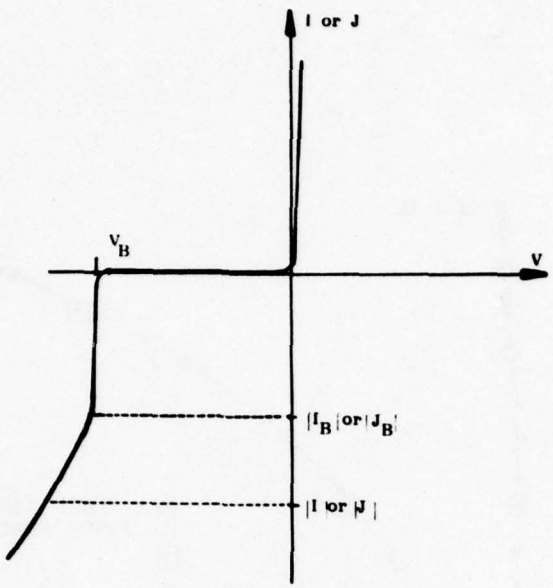

Figure 4. Model for Figure 3.

Figure 5 shows the computer's "exact" solution as compared to the model of Equation (2). For $N_D = 10^{15}/cm^3$, $W = 50\,\mu$, and R taken as the slope of the solid line of *Figure 3*, the model is calculated as the solid line in *Figure 5*. Note the excellent agreement between the computer and model solutions. The punchthrough case is illustrated also in *Figure 5*, where $W = 10\,\mu$ and $R = 0.015\,\Omega\text{-cm}^2$. As has been shown by comparing the model with the computer-generated J versus V plots, the model is very accurate for pure avalanche and pure punchthrough. As a result of these initial efforts, we were able to predict the anomalous voltage response to the reverse current pulse and to develop simple circuit models that save substantial amounts of computer time in complex networks.

To further investigate the anomalous voltage response to a current impulse and to identify other device phenomena, the numerical solution to the system equations was reformulated and a dynamic solution attempted. The main goal was to formulate the problem in a very general way so that both the forward-pulsed and the reverse-pulsed cases could be investigated. We also wanted to keep the recombination laws as general as possible and to make as few assumptions as possible.

A dynamic solution for the reverse pulse at extreme currents could then be used to justify our original steady-state solution and help predict the time necessary for that

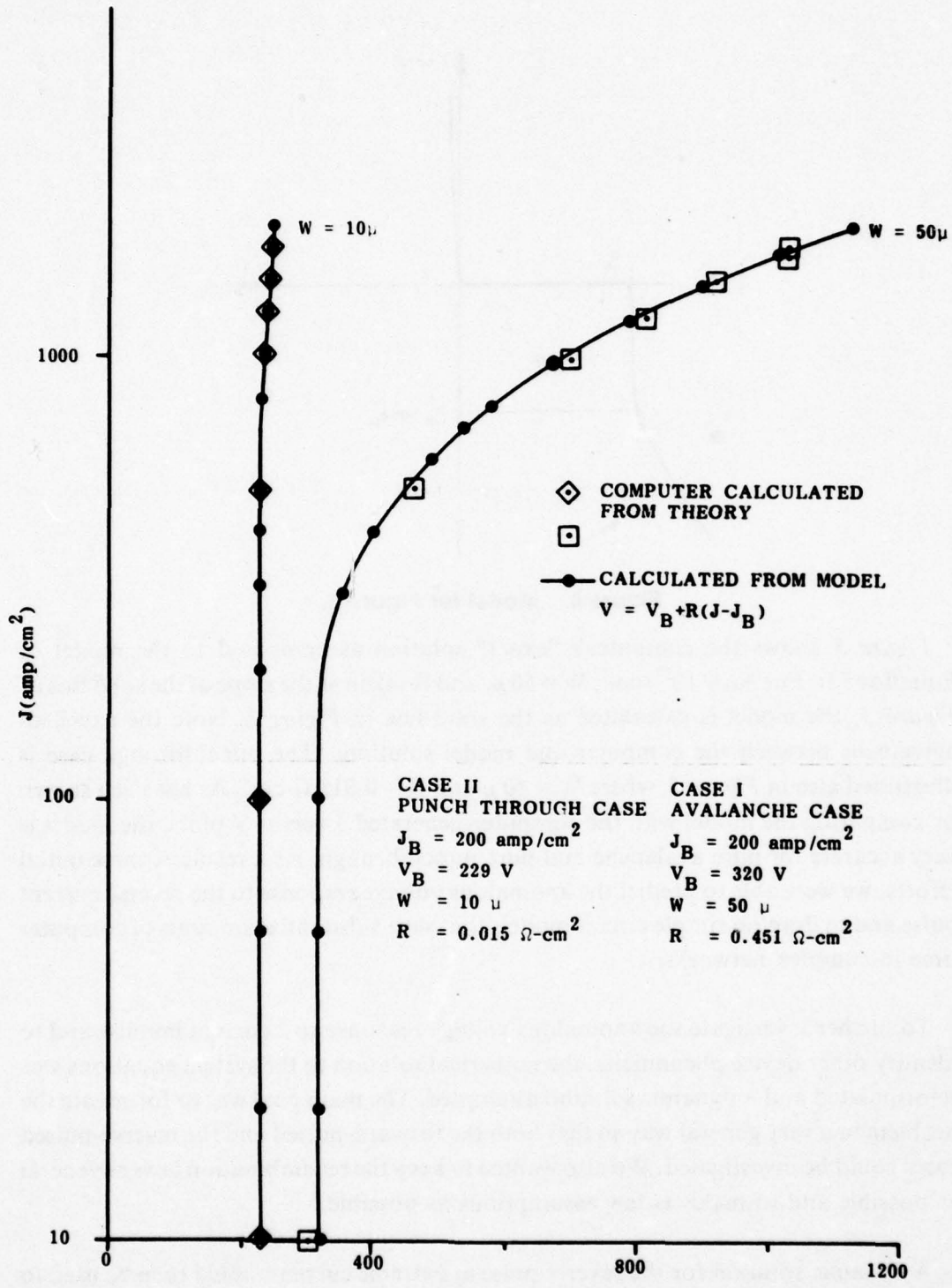

Figure 5. Computer solution compared to the model of Equation (2).

condition to be reached. By making the doping profiles completely arbitrary and the generation-recombination laws flexible, the formulation could be used to study other devices such as P-I-N diodes, BARITT, TRAPATTS, etc.

To achieve analytical results, the one-dimensional, two-carrier transport equations, along with Maxwell's and Poisson's equations, must be solved. This set of coupled, nonlinear, second-ordered partial differential equations can be solved by either the implicit or the explicit numerical techniques. When a numerical solution is obtained, then the transient and spatial distribution of all the physical quantities such as the electric field, electron and hole distributions of all the physical quantities such as the electric field, electron and hole distributions and all currents are known. These distributions can then be examined in detail for their interpretation in light of the physical phenomena in the device.

A. DeMari[5]solved this set of equations under the assumption of constant electron and hole mobilities and with no generation-recombination term. He used external excitations of low to moderate values. Scharfetter and Gummel [6] solved a set for a silicon + NP structure operating under reverse biased conditions as a Reed oscillator. The present research has been to solve these equations numerically free from any of the traditional assumptions and thereby simulate the transient behavior of a current-driven solid-state structure starting from the thermal equilibrium condition. The method used is very general and allows for complete freedom in selecting the generation-recombination laws, doping profiles, and mobility dependencies. To date no solution exists for extreme current conditions with generalized doping profiles and terminal-to-terminal boundary conditions.

Thus far, we have written the computer codes and have obtained a dynamic solution for the reverse-pulsed case and for the forward-pulsed case at low to medium current densities. Some of the reverse-pulsed results are illustrated in *Figures 6* through *8* and with the terminal voltage and time shown in *Table 1*.

B. METHOD OF ATTACK

The forward-pulsed solution is far more complex and requires additional computer time and detailed analysis. For example, at the extreme current densities involved the recombination may include band-to-band recombination as well as the more traditional forms of Shockley-Reed-Hall recombination. It is important to note that in any of those formulations, one must be very confident of the numerical techniques involved so as to distinguish between the device physics and a numerical aberration.

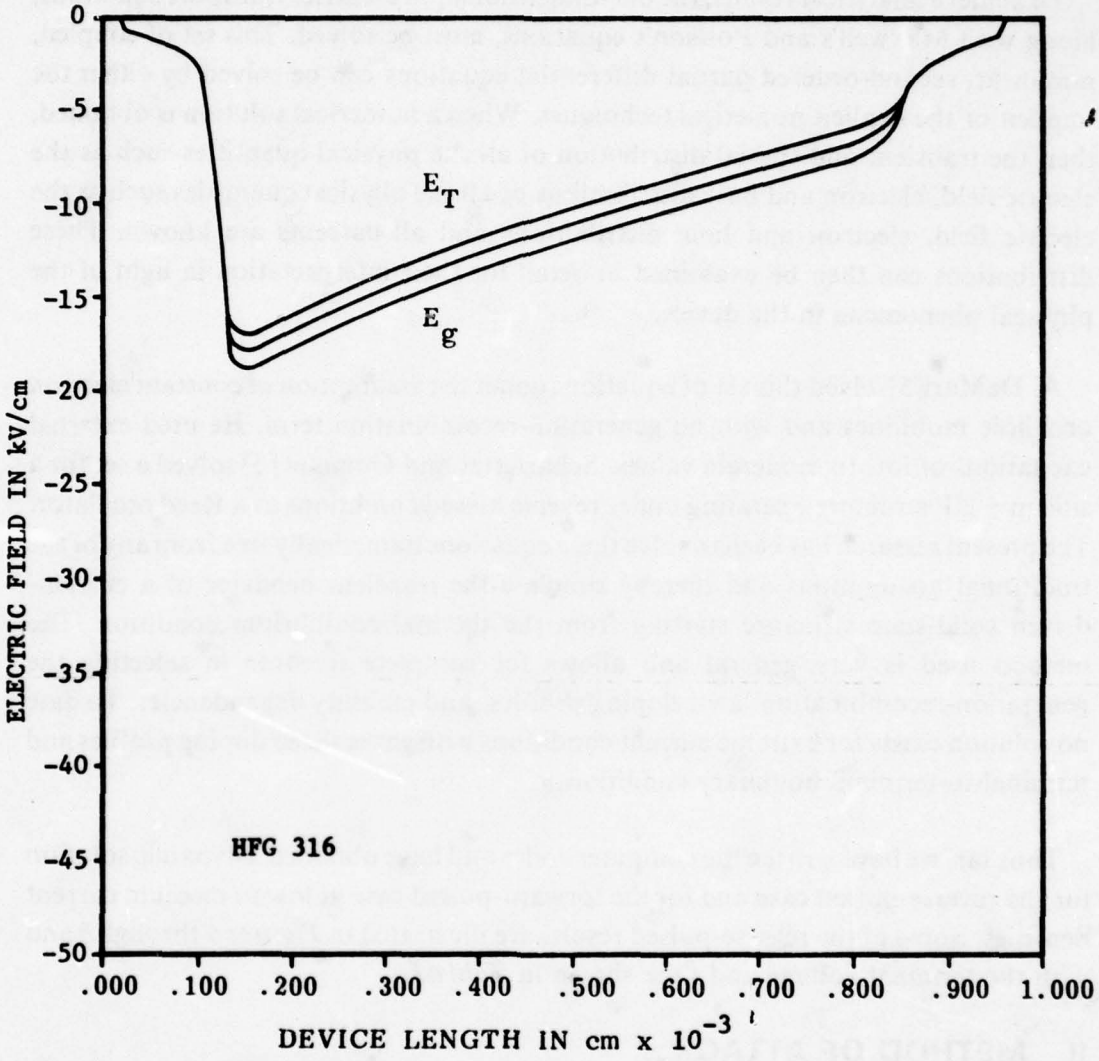

Figure 6a. Reverse-pulsed results.

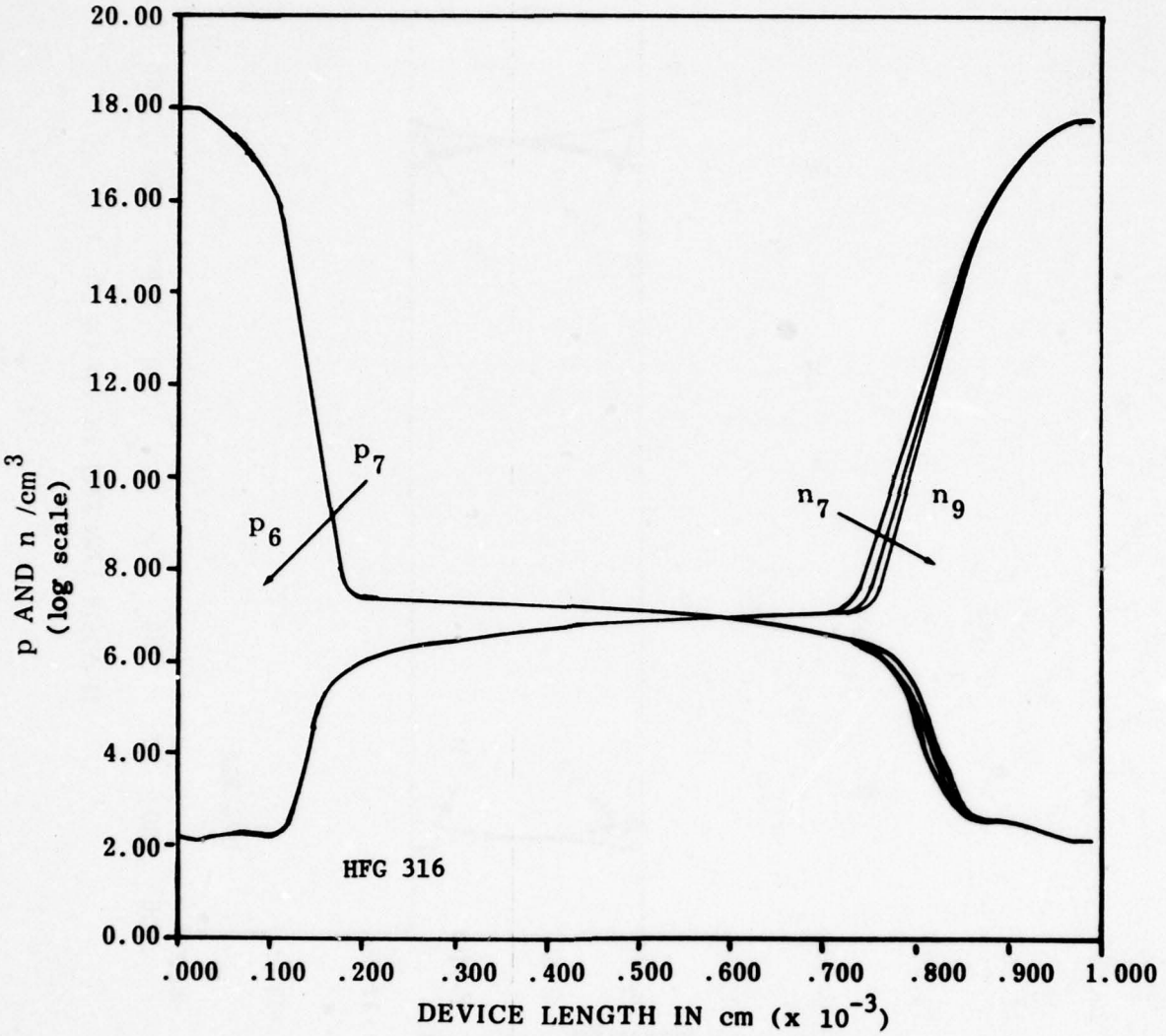

Figure 6b. Reverse-pulsed results.

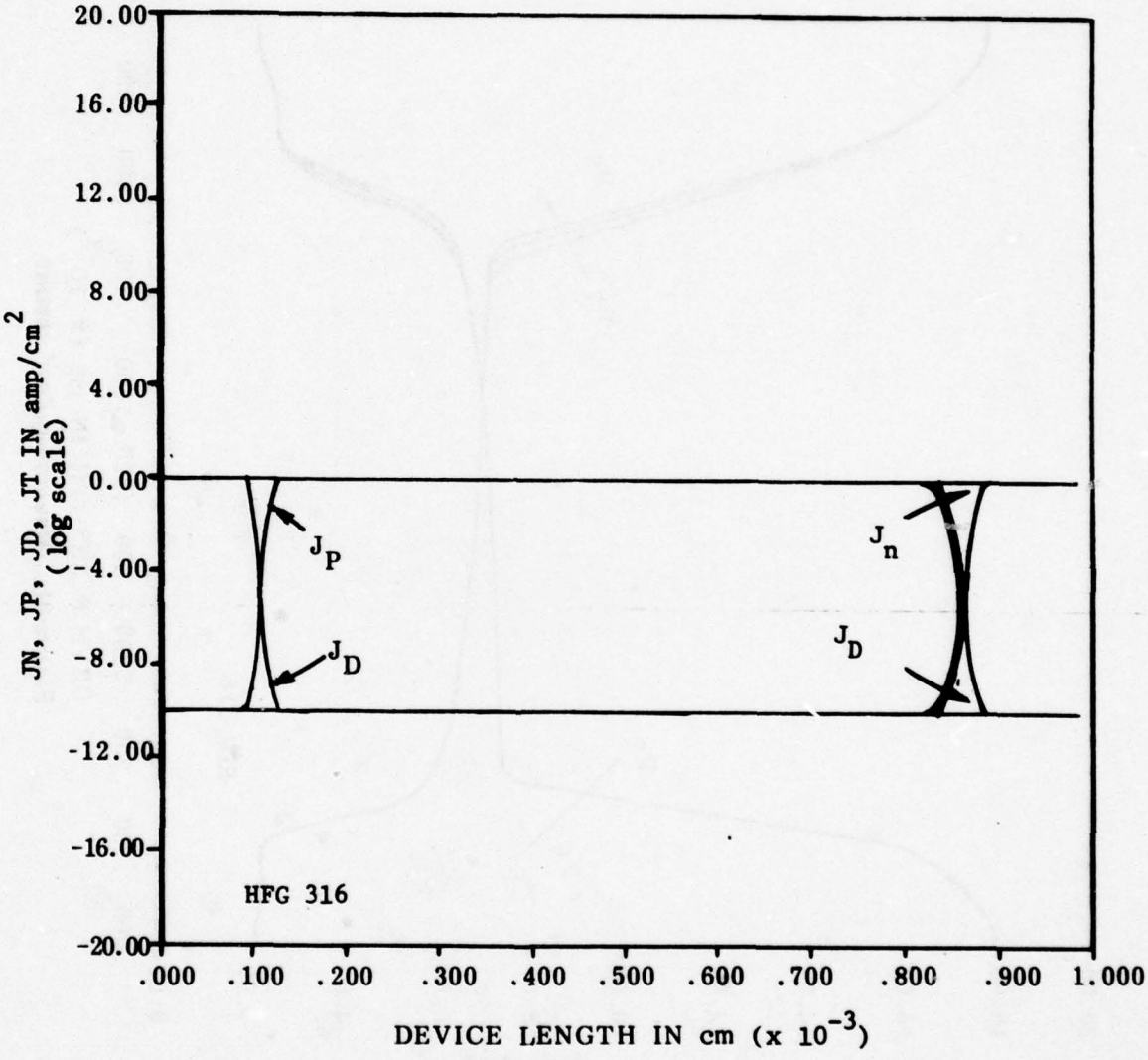

Figure 6c. Reverse-pulsed results.

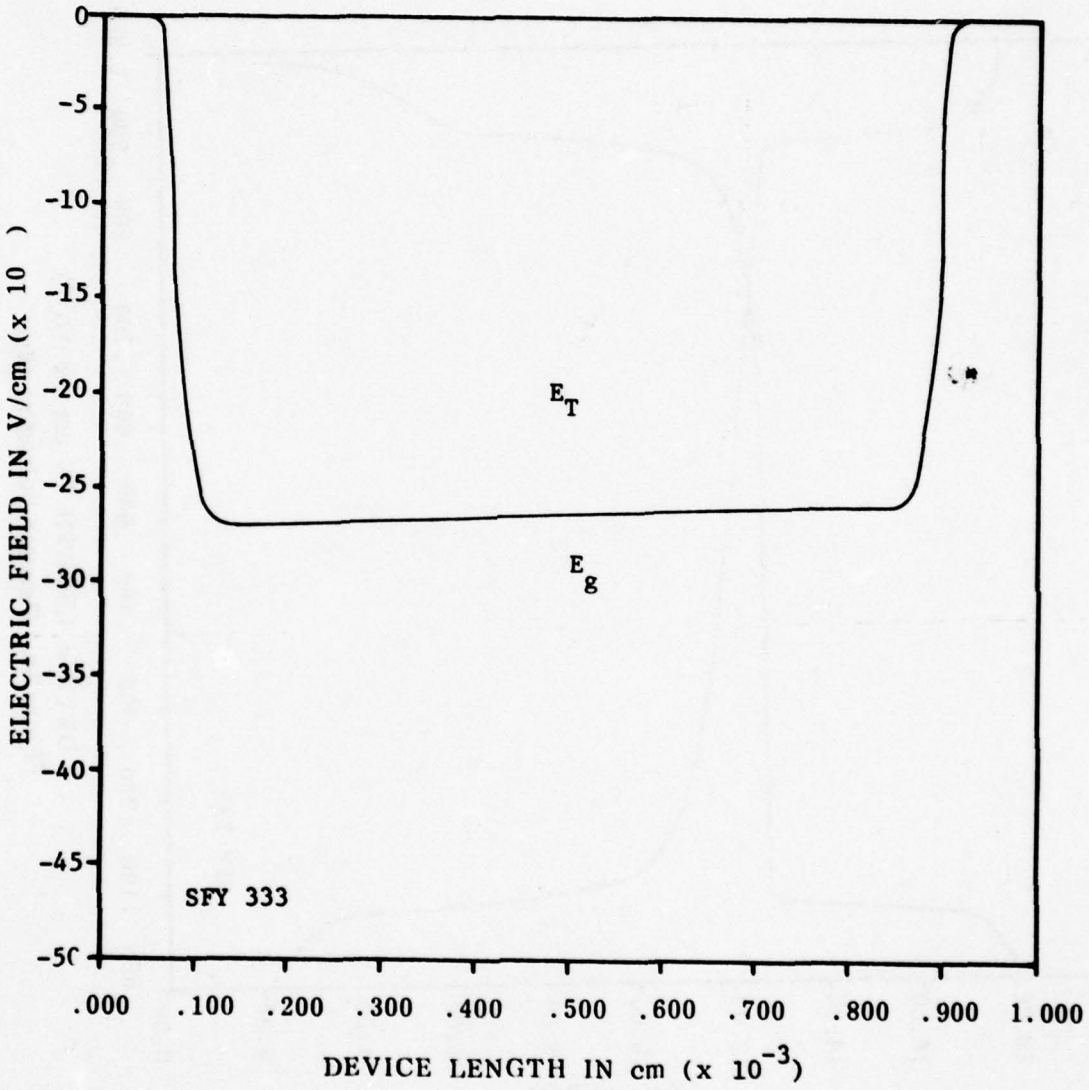

Figure 7a. Reverse-pulsed results.

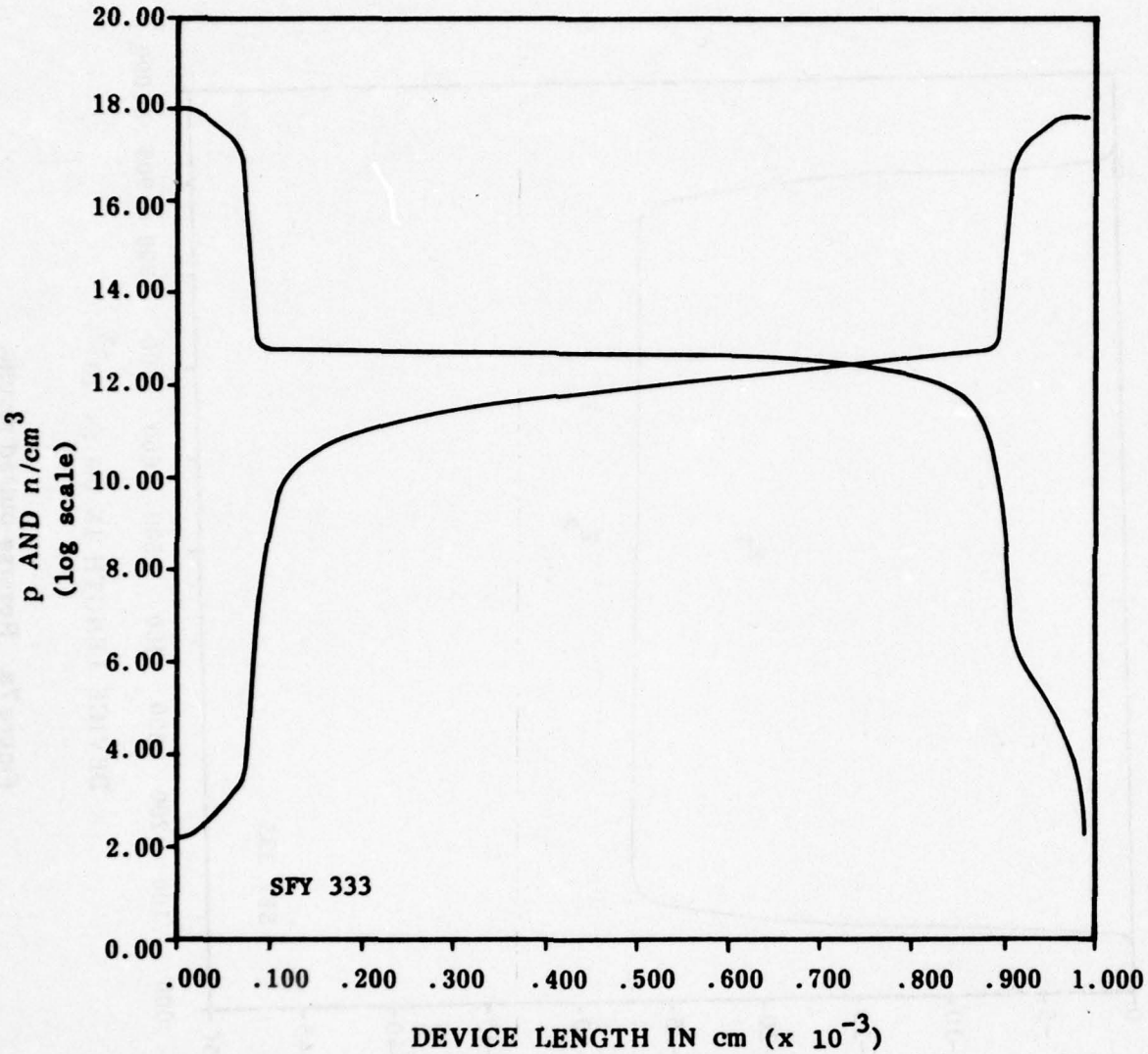

Figure 7b. Reverse-pulsed results.

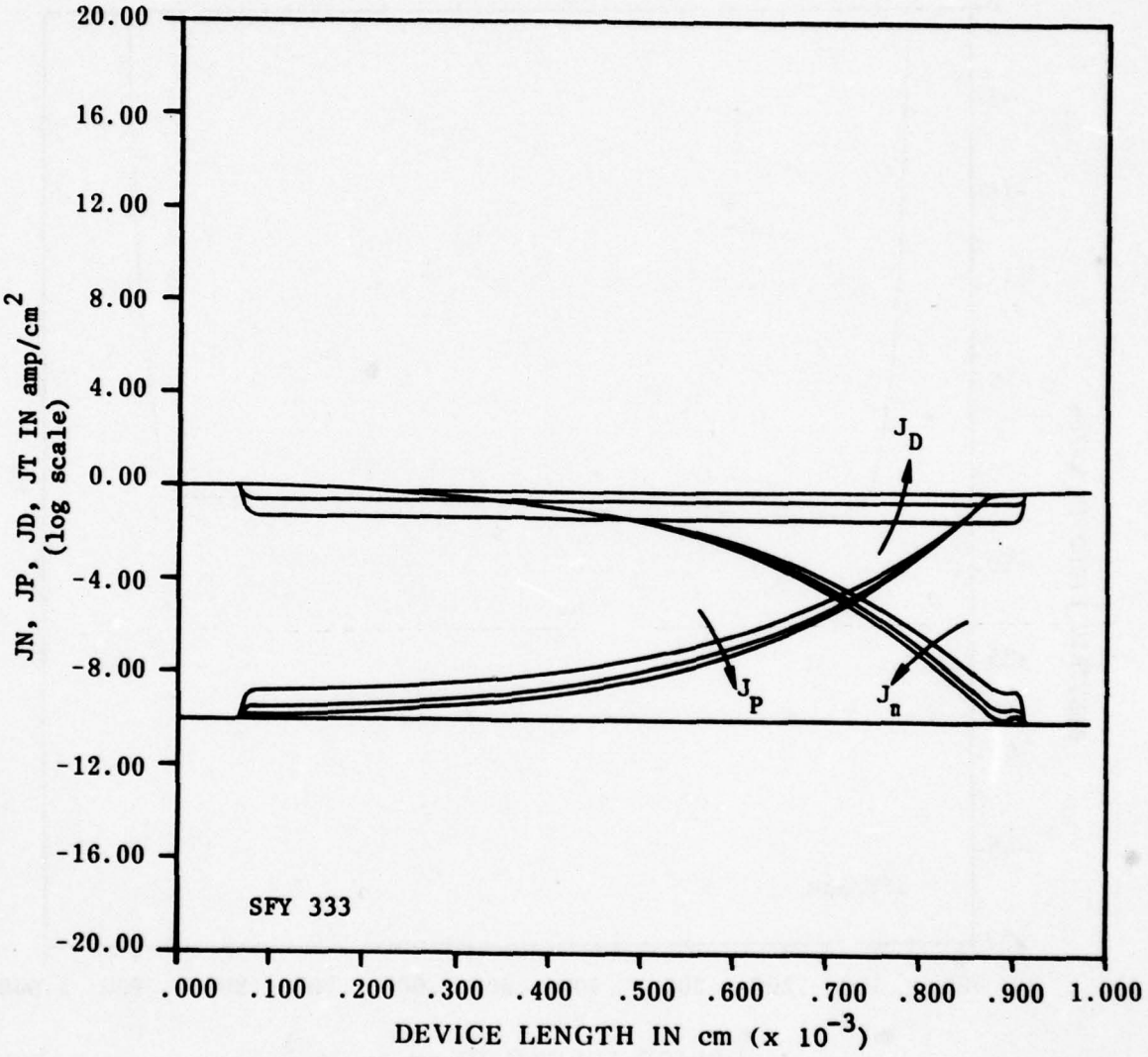

Figure 7c. Reverse-pulsed results.

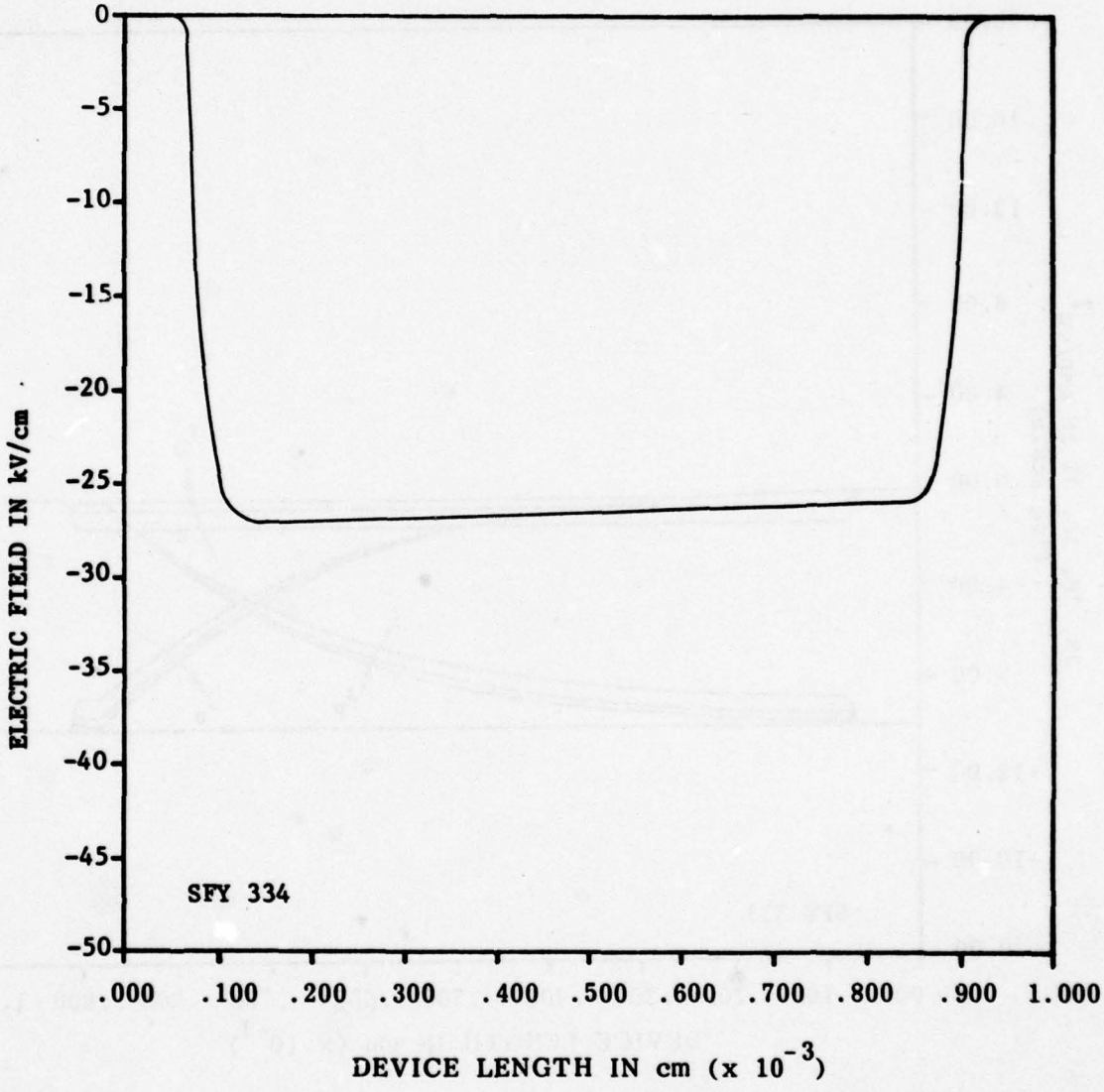

Figure 8a. Reverse-pulsed results.

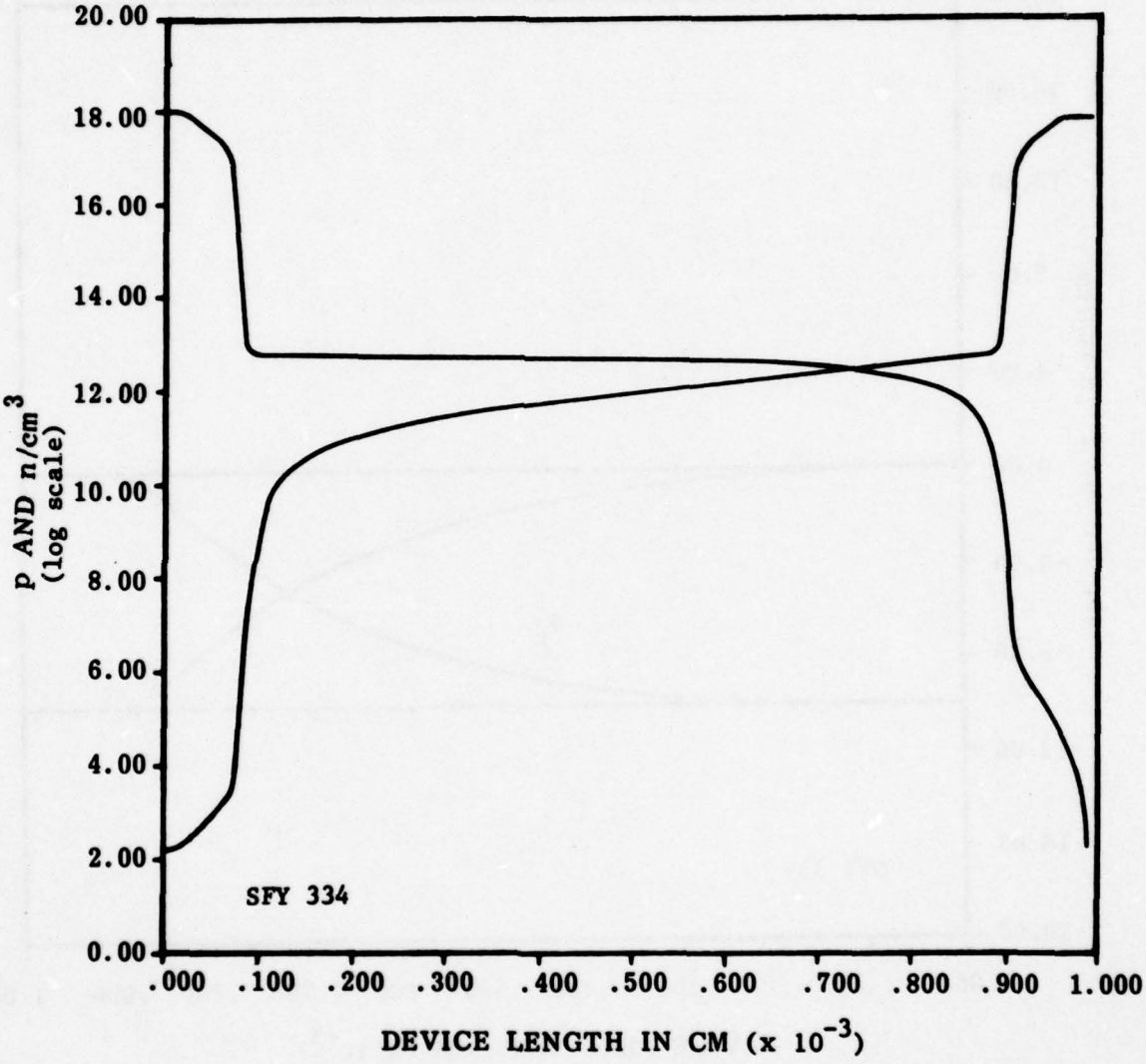

Figure 8b. Reverse-pulsed results.

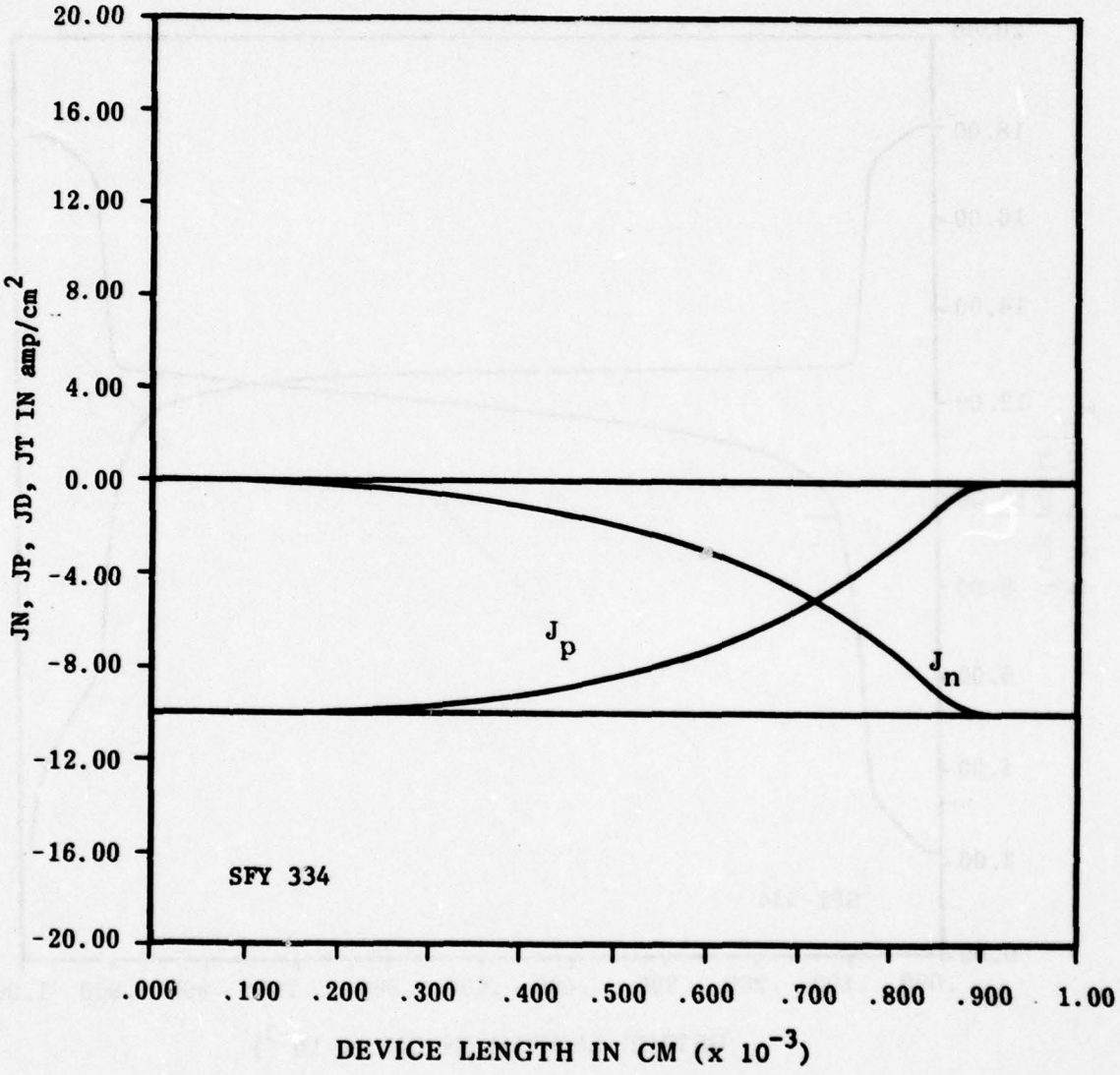

Figure 8c. Reverse-pulsed results.

TABLE 1. Reverse Bias Case

PROGRAM	k	TIME	CURRENT	VOLTAGE
HFG 314	20	2×10^{-10}	-10 amp/cm^2	- 0.606
	40	4×10^{-10}	-	- 1.38
	60	6×10^{-10}	-	- 2.38
HFG 315	80	8×10^{-10}	-	- 3.62
	100	1×10^{-9}	-	- 4.99
	120	1.2×10^{-9}	-	- 6.4
HFG 316	140	1.3×10^{-9}	-	- 7.12
	160	1.4×10^{-9}	-	- 7.84
	180	1.5×10^{-9}	-	- 8.56
SFY 329	740	1.75×10^{-8}	-	- 131.74
	760	1.95×10^{-8}	-	- 147.6
SFY 330	780	2.15×10^{-8}	-	- 163.5
	800	2.35×10^{-8}	-	- 179.4
SFY 332	820	2.55×10^{-8}	-	- 194.63
	840	2.75×10^{-8}	-	- 210.7
	860	2.95×10^{-8}	-	- 210.7
	880	3.15×10^{-8}	-	- 212.2
SFY 333	900	3.35×10^{-8}	-	- 212.8
	920	3.55×10^{-8}	-	- 213.02
	940	3.75×10^{-8}	-	- 213.05
SFY 334	960	3.95×10^{-8}	-	- 213.05
	980	4.15×10^{-8}	-	- 213.04
	1000	4.35×10^{-8}	-	- 213.04

Specifically, we intend to continue the computer simulation for the forward-pulsed P+N-N+ structures of known or determined values of area, doping profiles, and high-resistivity region widths to obtain good experimental data for the computer simulation studies. Third, and with far more difficulty, will be pulse testing the structure in the forward pulse mode to check for verification of the main features of the theoretical results. For prediction of device failure and second breakdown phenomena, it would ultimately be desirable for simple circuit models to be developed.

To accomplish the objectives of this proposed research for the forward-pulsed case, it is necessary to obtain a numerical solution that converges at extreme currents and with different generation-recombination laws. For example, generation caused by avalanche at the same time band-to-band (Auger) recombination is present. This can be accomplished with a very precise solution for the initial conditions, the starting point for a dynamic solution. Therefore, we have written a separate computer code for solving Poisson's equation numerically for the electron and hole distributions and the electric field for arbitrary doping profiles in the three regions under thermal equilibrium conditions. These results, at each spatial mesh-point, are then used as part of the input data to the dynamic program. This is an important point for obtaining a good dynamic solution. We can then obtain solutions showing the effects of band-to-band recombination and at what current densities it becomes significant. One would expect a considerable saving of computational time if band-to-band recombination could be neglected in certain problems.

The experimental verification of the forward-pulsed dynamic solution at extreme currents starts with P+N-N+ device fabrication on known starting materials and/or measurements to determine the area, width, and doping profiles. The pulse testing can be accomplished by using present pulse test facilities available to us in the NSF-MRL central facility at Purdue University. We have available pulse equipment with 20-ns rise times up to 2 amp. Using the appropriate recording medium, we can compare the computer simulation versus experimental results.

If what we have proposed is accomplished with good results, then we have developed a computer code capable of calculating the transient solution to a large number of solid-state devices made from three regions. Barritt microwave oscillators, P-I-N attenuators, Trapatts, etc., are all contained within these capabilities. We have also shown the physical source and magnitude of the anomalous voltage response under many different conditions – when it will occur and what effect it has on the instantaneous power input to the structure. This energy input will affect its thermal

threshold and in some cases when the device will reach a critical temperature and go into second breakdown. These results will also be directly applicable to transferring the second breakdown work on SOS diodes to standard device structures.

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9. ANALYSIS OF ELECTRICAL PROPERTIES IN IRREGULAR GEOMETRIES*

The electrical properties such as electric fields, current densities, voltages, etc., are generally obtained for the dc case by solving Poisson's equation. For regions where the charge density is zero, this reduces to Laplace's equation. For ideal geometries Laplace's equation is usually easily solved by conventional methods such as separation of variables. For the present discussion an ideal geometry is one such that only one coordinate varies on a given boundary. The conventional methods of solutions generally do not work for nonideal geometries. Nonideal geometries are quite common in semiconductor devices. They can occur because of deliberate design or by accident such as misalignment of circles, "glitches" on straight lines, etc. An attempt is made here to analyze some of the electrical effects that occur because of nonideal geometries.

Some of these problems lend themselves quite nicely to the method of transformations, i.e., the problem of the nonideal geometry is transformed or mapped into an ideal geometry where the problem is readily solved. The solution is transferred back to the original geometry of interest through the inverse transformation. Certainly not all geometric patterns lend themselves to this method of attack. Some problems may be transformed exactly into ideal geometries while for others the transformation is only approximate. In general, the transformations are limited to two dimensions. Some examples will now be given.

A. NON CONCENTRIC CIRCLES

Figure 1(a) shows the geometry of two nonconcentric circles where the solution of some differential equation such as Laplace's equation is desired in the area between them. These two circles might represent the areas of diffusions for two regions of a transistor (e.g., base and emitter). They might also represent the area of diffusion for one region of a device and the area of metalization for the homic contact. *Figure 1(b)* shows the transformed geometry where the circles become concentric. The solutions for most differential equations of interest are well known when the solutions on the two concentric circles are given. For the sake of analysis, let the original plane be the Z-plane and the transformed plane be the W-plane, where $Z = X + iY$ and $W = U + iV$.

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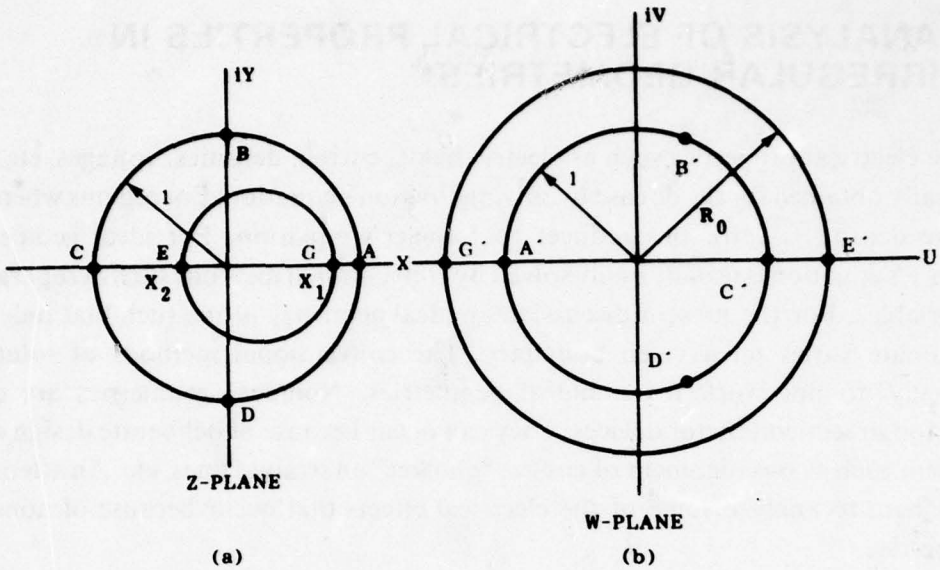

Figure 1. (a) Original geometry showing non concentric circles. (b) Transformed geometry with concentric circles.

A transformation is desired that will uniquely map the two circles in the Z-plane onto the two circles in the W-plane. All points between the two circles in the Z-plane should also be mapped one-to-one to points between the two circles in the W-plane. In addition, an inverse transformation is desired that will remap all of the above points in the W-plane back onto the original points in the Z-plane. A transformation that does the mapping described above is

$$W = \frac{Z - a}{aZ - 1}. \tag{1}$$

The inverse transform is

$$Z = \frac{W - a}{aW - 1}, \tag{2}$$

where

$$a = \frac{1 + X_1 X_2 + \sqrt{(1 - X_1^2)(1 - X_2^2)}}{X_1 + X_2} \tag{3}$$

and X_1 and X_2 are shown in *Figure 1*. Also shown in *Figure 1* are points A, B, C, etc., which map onto A', B', C', etc., respectively. The unit circle in the Z-plane maps onto the unit circle in the W-plane, and the inner circle in the Z-plane maps onto the outer circle in the W-plane. The radius, R_o, of the outer circle is given by

$$R_o = \frac{1 + X_1 X_2 + \sqrt{(1 - X_1^2)(1 - X_2^2)}}{X_1 - X_2} \quad . \tag{4}$$

As an example of how to use the above method, the voltage, electric field and current density will be obtained for a potential of V_o applied between two conducting circles. These electrical quantities will be obtained for two cases: The first case will be where the two circles are concentric and the second case will be where they are not. The radius of the outer circle will arbitrarily be taken as unity and the potential there will be taken as zero. This does not restrict the class of problems that can be solved since any radius can be scaled to unity. There are several situations in semiconductor devices where the equal potential circles or cylinders are a reasonable approximation (a cylinder is treated just like a circle if there is no variation along its axial direction). The radius of the inner circle will be taken as 1/2 and the potential there as V_o.

The well-known solutions for the case of the concentric circles give electric fields and current densities which are a function only of $r = \sqrt{X^2 + Y^2}$. The solutions in the range $1/2 \leq r \leq 1$ are

$$E(r) = \frac{V_o}{\ln 2} \quad \frac{1}{r} \quad , \tag{5}$$

$$J(r) = \sigma E(r) \quad , \tag{6}$$

$$V(r) = V_o \left[1 - \frac{\ln r}{\ln 2}\right] \quad , \tag{7}$$

Next, assume circles of the same radii as above except that the smaller circle has its center at (1/4, 0) instead of at the origin. This gives values $X_2 = -1/4$, $X_1 = 3/4$, $a = 2.91$ and $R_o = 1.45$. The potential in the W-plane at $R = 1$ is zero and at $R = R_o$ is V_o where $R = \sqrt{U^2 + V^2}$. The solutions in the W-plane for the region $1 \leqslant R \leqslant R_o$ are

$$E(R) = \frac{-V_o}{\ln R_o} \frac{1}{R} \quad . \tag{8}$$

The voltage is

$$V(R) = \frac{V_o}{\ln R_o} \ln R \quad . \tag{9}$$

These quantities in the desired Z-plane are found by use of the inverse transform of Equation (2). However, since the electric field is a vector quantity, it is usually easier to first find the scalar voltage V (X, Y) and then use its gradient to find the electric field E (X,Y). The voltage is

$$V(X,Y) = \frac{V_o}{\ln (R_o)} \ln \left| \frac{(X + iY) - A}{a(X + iY) - 1} \right|$$

$$= \frac{V_o}{2 \ln (R_o)} \left\{ \ln [(X - a)^2 + Y^2] - \ln [(aX - 1)^2 + (aY)^2] \right\}. \tag{10}$$

The electric field is given by

$$\vec{E}(X,Y) = \vec{a}_x \frac{\partial}{\partial X} V(X,Y) + \vec{a}_y \frac{\partial}{\partial Y} V(X,Y)$$

$$= \vec{a}_x E_x + \vec{a}_y E_y \tag{11}$$

where

$$E_x = \frac{V_o}{\ln R_o} \left[\frac{a(aX - 1)}{(aX - 1)^2 + (aY)^2} - \frac{(X - a)}{(X - a)^2 + Y^2} \right] ,$$

$$E_y = \frac{V_o}{\ln R_o} \left[\frac{a^2 Y}{(aX - 1)^2 + (aY)^2} - \frac{Y}{(X - a)^2 + Y^2} \right] .$$

Using the values in the above example gives

$$V(X,Y) = 1.35\, V_o \left\{ \ln [(X - 2.91)^2 + Y^2] - \ln [(2.91\, X - 1)^2 + (2.91\, Y)^2] \right\}$$

$$E_x = 2.70\, V_o \left[\frac{2.91\,(2.91\, X - 1)}{(2.91\, X - 1)^2 + (2.91\, Y)^2} - \frac{(X - 2.91)}{(X - 2.91)^2 + Y^2} \right] ,$$

and

$$E_y = 2.70\, V_o \left[\frac{8.47\, Y}{(2.91\, X - 1)^2 + (2.91\, Y)^2} - \frac{Y}{(X - 2.91)^2 + Y^2} \right] .$$

The voltage and electric field can be calculated directly for any point between the two nonconcentric circles by using the corresponding values of X and Y in the above equations. Of course, the current density is just the conductivity times the electric field. The total current is easier to calculate in the W-plane since the current density is always in a radial direction there.

B. RECTANGULAR GEOMETRIES WITH IRREGULARITIES

Next, consider the geometry in *Figure 2*. This could represent the region of interest in an SOS diode with a circular "spike" in the metalization or the heavy doping. We wish to map this region into a region where the solutions of voltage and electric field are either known or are easily obtained. A transformation that maps the curve of constant potential $V = V_o$ onto the real axis in the W-plane is

$$W = Z + 1/Z \ . \qquad (12)$$

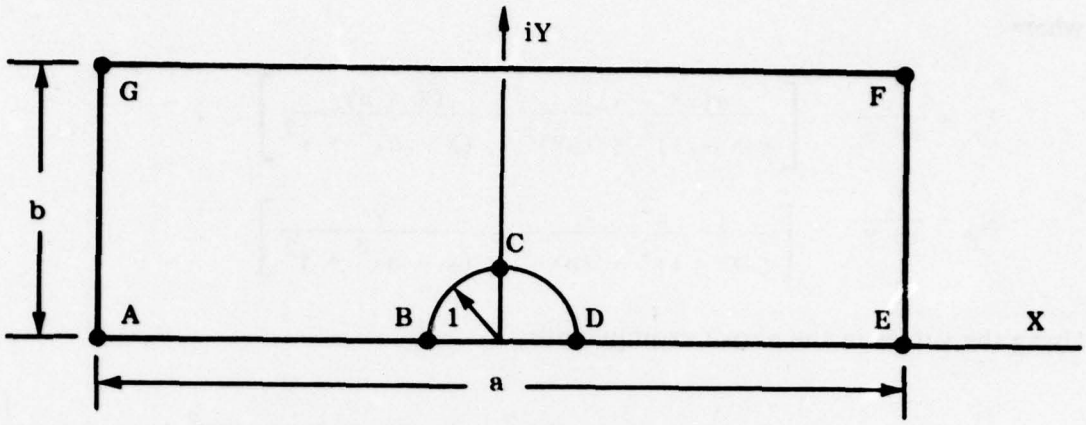

Figure 2. "Spike" in rectangular geometry.

This transformation also maps the area above the constant potential curve onto the upper half plane in the W-plane. However, it does not map the Y = b line onto a V = constant line in the W-plane. This can be seen by putting Y = b in Equation (12). The results are

$$W = U + iV = (X + ib) + \frac{1}{X + ib} \tag{13}$$

$$= X\,\frac{(X^2 + b^2 + 1)}{X^2 + b^2} + ib\,\frac{X^2 + b^2 - 1}{X^2 + b^2}$$

or

$$U = \frac{X(X^2 + b^2 + 1)}{X^2 + b^2}$$

and

$$V = b\,\frac{(X^2 + b^2 - 1)}{X^2 + b^2} \quad .$$

If $b^2 >> 1$, which is almost always the case of interest, the line Z = X + ib transforms very approximately onto the line W = X + ib. Hence the problem in the W-plane is approximately that shown in *Figure 3*.

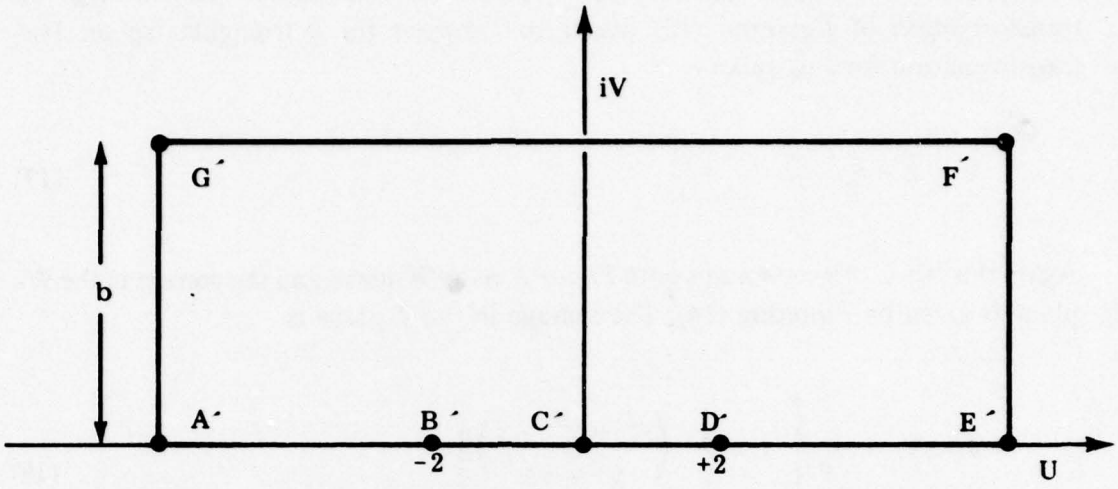

Figure 3. Mapping of Figure 2 onto W-plane.

The voltage in the W-plane is

$$V(W) = V_o \left(1 - \frac{v}{b}\right) \quad . \tag{14}$$

Then, according to Equation (12),

$$V(X,Y) = V_o \left[1 - \frac{y}{b} \frac{(X^2 + Y^2 - 1)}{X^2 + Y^2}\right] \quad . \tag{15}$$

The electric field is

$$\vec{E} = \frac{V_o}{b} \left[\frac{2\,X\,Y}{(X^2 + Y^2)^2} \vec{a}_x + \left(1 + \frac{Y^2 - X^2}{(X^2 + Y^2)^2}\right) \vec{a}_y\right] \quad . \tag{16}$$

A number of different types of single spikes can be analyzed with the type of transformation of Equation (12). Refer to *Figure 4* for a triangular spike. The transformation for this spike is

$$W = Z + \frac{C}{Z} \quad . \tag{17}$$

Again if $b >> C$, *Figure 4* maps onto *Figure 3* in the W-plane and the voltage in the W-plane is given by Equation (14). The voltage in the Z-plane is

$$V(X,Y) = V_o \left[1 - \frac{Y}{b} \left(\frac{X^2 + Y^2 - C}{X^2 + Y^2} \right) \right] \tag{18}$$

and the electric field is

$$E(X,Y) = \frac{V_O}{b} \left[\left(\frac{2\,CX\,Y}{(X^2 + Y^2)} \right) \vec{a}_x + \left(1 + C \frac{(Y^2 - X^2)}{(X^2 + Y^2)^2} \right) \vec{a}_y \right] \tag{19}$$

The technique discussed above can be used to determine the dc electric field profiles of irregular geometries. Since the current density is just a product of the electric field and conductivity, this technique also allows for the determination of the dc current density.

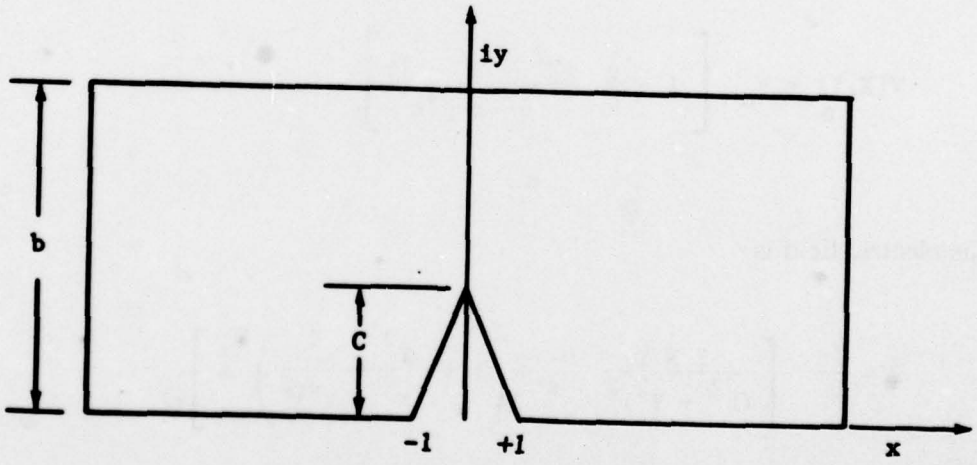

Figure 4. Triangular spike.

10. TEST PLAN FOR SPECIAL SOS DIODES*

A. INTRODUCTION

As part of the DNA/MIRADCOM hardness asurance program, a study is being conducted to determine the sensitivity of various semiconductor parameters to electrical overstress. The objective of this program is to develop effective electrical overstress hardness assurances screens which can be applied to eliminate "maverick" or early failure devices. The devices selected for use in this study are special lateral diode structures fabricated on sapphire substrates. These structures permit optical observation of the hot spot nucleation and growth which lead to catastrophic failure.

The purpose of this test plan is to describe in detail the test and data-handling procedures to be used in testing the special SOS (silicon on sapphire) diode structures. Because of time and program constraints, it is not possible to test all the separate diode structures available (approximately 150,000). The quantity and order of tests have been chosen to provide reasonable data outputs, in a timely manner, for utilization in analyses and correlation studies throughout the program.

B. TEST STRUCTURES

Special test structures have been fabricated by Rockwell for use in this study. These structures consist of lateral diodes fabricated on silicon substrates. The diodes have been designed to permit observation of the sensitivity of various semiconductor physical parameters to electrical overstress. The total test sample consists of approximately 150,000 separate diodes, which have been fabricated in two lots of five wafers each (five different doping concentrations). Each wafer contains approximately 70 identical dice. Each die is divided into 12 sections which contain diodes of similar structure but varying physical dimensions. *Table 1* gives a breakdown of the SOS diodes structures. *Table 2* gives a breakdown of the physical dimensions of each of the structure types found in every die.

C. BATCH TEST METHODOLOGY

To assure that the highest quality data are obtained in a timely manner, a

*C. R. Jenkins, BDM Corporation.

TABLE 1. SOS Diode Structures

STRUCTURE TYPE	DEVICES* PER DIE	DICE PER WAFER	WAFERS** PER LOT	DEVICES PER WAFER	DEVICES PER LOT
STANDARD REFERENCE	25	70	5	1,750	8,750
ENCLOSED REFERENCE	20	70	5	1,400	7,000
CONTACT SPIKES TO P++	20	70	5	1,400	7,000
CONTACT SPIKES TO N++	20	70	5	1,400	7,000
DIFF. SPIKES P++ TO N	20	70	5	1,400	7,000
DIFF, SPIKES N++ TO N	20	70	5	1,400	7,000
MULTIPLE SPIKES	51	70	5	3,570	17,850
HALF-SIZE SPIKES	20	70	5	1,400	7,000
FOUR TERMINAL	6	70	5	420	2,100
DOPING LEVEL	1	70	5	70	350
INTERDIGITATED	2	70	5	140	700
RADIUS OF CURVATURE	9	70	5	630	3,150
TOTALS	214	70	5	14,980	74,900

* Each diode has different physical dimensions.

** Each wafer has a different doping level (10^{14}, 10^{15}, 10^{16}, 10^{17}, 5×10^{17} cm^{-3}).

TABLE 2. SOS Diode Structures' Physical Dimensions

STANDARD REFERENCE STRUCTURES	N REGION LENGTH = 10, 30, 100, 300, 500 μ STRUCTURE WIDTH = 1.2, 2, 4, 8, 20 MILS
CONTACT/DIFFUSION SPIKE STRUCTURES	N REGION LENGTH = 10, 30, 100, 300, 500 μ STRUCTURE WIDTH = 1.2, 2, 4, 8 MILS SPIKE LENGTH = 5 μ SPIKE DIRECTION = N++ CONTACT → N-TYPE; P++ CONTACT → N-TYPE N++ DIFFUSION → N-TYPE; P++ DIFFUSION → N-TYPE
ENCLOSED REFERENCE STRUCTURES	N REGION LENGTH = 10, 30, 100, 300, 500 μ STRUCTURE WIDTH = 1.2, 2, 4, 8 MILS
HALF-SIZE SPIKE STRUCTURES	N REGION LENGTH = 10, 30, 100, 300, 500 μ STRUCTURE WIDTH = 4 MILS SPIKE LENGTH = 2.5 μ SPIKE DIRECTION = N++ CONTACT → N-TYPE, P++ CONTACT → N-TYPE N++ DIFFUSION → N-TYPE, P++ DIFFUSION → N-TYPE
MULTIPLE-SPIKE STRUCTURES	N REGION LENGTH = 10, 30, 100 μ STRUCTURE WIDTH = 8 MILS SPIKE LENGTH = 1, 2, 4, 8 μ SPIKE DIRECTION = N++ CONTACT → N-TYPE, P++ CONTACT → N-TYPE N++ DIFFUSION → N-TYPE, P++ DIFFUSION → N-TYPE
FOUR-TERMINAL STRUCTURES	N REGION LENGTH = 30, 90, 300 μ STRUCTURE WIDTH = 1.2, 4 MILS SPACING BETWEEN CONTROL AND CONTACT REGIONS = EQUAL
DOPING-LEVEL TEST STRUCTURES	LENGTH BETWEEN CONTACTS = 100 μ STRUCTURE WIDTH = 200 μ
INTERDIGITATED STRUCTURES	N++ DIFFUSION LENGTH X WIDTH = 5 μ x 30 μ P++ DIFFUSION LENGTH X WIDTH = 10 μ x 60 μ N++ - P++ DIFFUSION SEPARATION = 20, 40 μ
RADIUS OF CURVATURE STRUCTURES	RADIUS OF P++ DIFFUSION = 5, 10, 30 μ RADIUS OF N++ DIFFUSION = 5 μ MINIMUM SEPARATION = 10, 30, 100 μ

consistent test methodology is required. The methodology presented in this section has evolved over a period of several years and has been proven on many large-scale component test programs. The remainder of this section covers in detail the selection of the quantities of diodes to be tested, the priority of testing, test conduct, data storage and handling, and potential problem areas associated with the test program.

(1) TEST DIODE SELECTION. Approximately 150,000 separate diodes (two lots of 75,000) are available for testing. Because of time constraints, it will be impossible to test all of these devices. It is necessary, therefore, to restrict the number of test structures examined to allow testing of a broad sample of different structures so that the maximum information can be obtained from the tests in the allotted time.

The quantity of devices selected for testing is based on a test rate of two diodes at three pulse widths per hour. This rate was selected for planning purposes after discussions with Dr. Paul Budenstein of Auburn University. Additional time has been allotted for changes in the test setup required during testing when a diode burns out. Since many of the tests are to be performed in new areas (i.e., short pulse widths and high breakdown voltages), time will also be required to improve the test techniques in this area.

Table 3 is a breakdown of the quantity of the various diode structures to be tested on this program and the approximate time required to perform these tests. The number of diodes per wafer is based on being able to test each diode at three pulse widths (0.1, 1.0, 10 μsec). Should a diode burn out during a test, additional dice will have to be tested. The sample size for each diode of given physical dimensions is five. The total number of diodes shown is for each lot of five wafers (five doping levels).

The Doping Level Test Structure will be tested on each die used in the test program. Since only a V-I measurement is made on this structure, little time will be required for this test. As a check on consistency, the Doping Level Test Structure will be tested each time a given section of a die is tested.

(2) ORDER OF TESTING. The order of testing of the various diode structures has been chosen to provide sufficient data early in the program to proceed with the sensitivity analysis task. Although other test sequences may

TABLE 3. SOS Diode Structures to be Tested

STRUCTURE AND DIMENSIONAL VARIATIONS	DIODES PER DIE	DIODES PER WAFER*	TOTAL DIODES**	TEST TIME
STANDARD REFERENCE STRUCTURE:				
N-REGION LENGTHS = 10, 30, 100, 500 μ				
STRUCTURE WIDTHS = 1.2, 4, 8, 20 MILS	16	80	400	5 WEEKS
ENCLOSED REFERENCE STRUCTURES:				
N-REGION LENGTHS = 10, 30, 100, 500 μ				
STRUCTURE WIDTHS = 1.2, 4, 8 MILS	12	60	300	4 WEEKS
RADIUS OF CURVATURE STRUCTURES:				
RADAI OF P++ DIFFUSIONS = 5, 10, 30 μ				
RADIUS SEPARATIONS = 10, 30, 100 μ	9	45	225	3 WEEKS
CONTACT/DIFFUSION SPIKE STRUCTURES:				
N-REGION LENGTHS = 10, 30, 100 μ				
STRUCTURE WIDTHS = 1.2, 4, 8 MILS				
SPIKE DIRECTIONS = N++ CONTACT → N-TYPE	9	45	225	3 WEEKS
P++ CONTACT → N-TYPE	9	45	225	3 WEEKS
N++ DIFFUSION → N-TYPE	9	45	225	3 WEEKS
P++ DIFFUSION → N-TYPE	9	45	225	3 WEEKS
MULTIPLE SPIKE STRUCTURES:				
N-REGION LENGTHS = 10, 30, 100 μ				
SPIKE LENGTHS = 1, 8 μ				
SPIKE DIRECTIONS = N++ CONTACT → N-TYPE	6	30	150	2 WEEKS
P++ CONTACT → N-TYPE	6	30	150	2 WEEKS
N++ DIFFUSION → N-TYPE	6	30	150	2 WEEKS
P++ DIFFUSION → N-TYPE	6	30	150	2 WEEKS
HALF-SIZE SPIKE STRUCTURES:				
N-REGION LENGTHS = 10, 30, 100 μ				
SPIKE DIRECTIONS = N++ CONTACT TO N-TYPE	3	15	75	1 WEEK
P++ CONTACT TO N-TYPE	3	15	75	1 WEEK
N++ DIFFUSION TO N-TYPE	3	15	75	1 WEEK
P++ DIFFUSION TO N-TYPE	3	15	75	1 WEEK
FOUR-TERMINAL STRUCTURES:				
N-REGION LENGTHS = 30, 90, 300 μ				
STRUCTURE WIDTHS = 1.2, 4 MILS	6	30	150	2 WEEKS
INTERDIGITATED STRUCTURES:				
N++ - P++ DIFFUSION SEPARATION = 20, 40 μ	2	10	50	1 WEEK
DOPING-LEVEL TEST STRUCTURE: (ONE PER DIE)	1	***	***	1 WEEK
TOTALS	117	585*	2925**	40 WEEKS

* Assuming each diode is tested at three pulse widths (five dice per wafer), any diode failures will require that additional dice be tested.

** Each lot of five wafers.

*** Depends on the number of dice tested.

allow more diodes to be tested, they would delay the sensitivity analyses and correlation study until very late in the program and could leave insufficient time available for the completion of those tasks.

The priority of testing the various diode structure types is given in *Table 4*. The Standard and Enclosed Reference Structures will be tested first to establish a baseline for the remaining tests and to assess the sensitivity of P_f to N_D, epi thickness and epi width. The priority of testing the remainder of the structure types has been chosen so that those structures representing physical variables having the higher probability of providing a good correlation with actual device overstress data are tested first.

The tests will be performed so that all data on a given structure type will be taken before proceeding to the next structure type. This order of testing will require that each wafer be inserted and removed from the test fixture several times during the course of the program. Extreme care will be required in handling to insure that none of the wafers is damaged.

TABLE 4. Priority of Testing

PRIORITY	STRUCTURE TYPE
1	STANDARD REFERENCE
2	ENCLOSED REFERENCE
3	RADIUS OF CURVATURE
4	CONTACT/DIFFUSION SPIKE
5	HALF-SIZE SPIKE
6	MULTIPLE SPIKE
7	FOUR TERMINAL
8	INTERDIGITATED

Note: A Doping Level Test Structure will be tested each time a die is tested.

(3) OVERSTRESS TESTING.

(a) Pre-test Characterization. The pretest characterization will consist of forward and reverse I-V characteristics taken on each diode to be pulse tested. The characteristics will be taken using a Tektronix Model 576 curve tracer and photographically recording the results. Each photograph will be marked with the device identification number to allow correlation of the diode's pre-pulse characteristics with its overstress behavior.

Since Rockwell will pre-test only a small sample of diodes (five diodes per wafer), it is essential that the pre-test characterization be performed to assure that the test diodes are functional and that their characteristics are as assumed. The analysis of the results of these tests could be significantly altered if diodes of different or unusual characteristics are inadvertently included in the test sample.

(b) Pulse Testing. The basic procedure is to step stress each diode. Wherever possible, a constant current pulse source will be used to bring about the onset of filamentation. The filamentation process will be photographically recorded using the procedures developed by Dr. Paul Budenstein at Auburn University. In addition to the photomicrographs, the pulse voltage and current response of each diode will be recorded using a Tektronix WP2221 Waveform Digitizing Instrument with two R7912 Transient Digitizers and CP112 Floppy Disc. An identification number will be assigned to each diode and recorded along with the digitized data for each pulse. A block diagram of the test setup is shown in *Figure 1*.

Within each test structure type and doping concentration, five diodes having the same physical dimensions (*Table 4*) will be tested at each of three pulse widths (0.1, 1.0, 10 μsec). Testing at all three pulse widths will be performed on each diode, provided that no damage occurs during pulse testing. In the event of damage, a diode having the same physical dimensions but from a different die will be substituted for the damaged device. Degradation or failure is most likely to occur on the lightly doped wafers (high breakdown voltage), particularly if the pulsed current source is not adequately regulated.

(c) Post-test Characterization. Post-test characterization will consist of running the curve tracer I-V characteristics of each diode following testing at

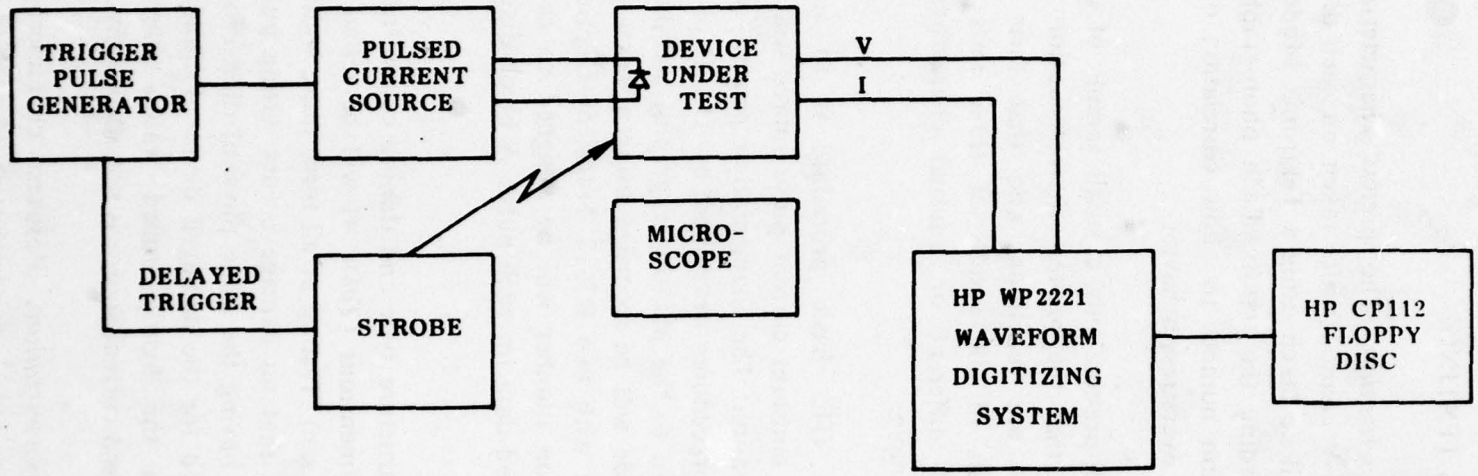

Figure 1. Block diagram of pulse test setup.

each pulse width. No waveforms will be recorded unless damage, such as increased leakage current or decreased breakdown voltage, has occurred. Since each diode is to be tested at more than one pulse width and a high probability of failure exists for many of the diodes, the post-test characterization is essential to insure that only good devices are used in every test.

(4) DATA HANDLING AND STORAGE. All pulse data will be recorded on a Tektronix CP112 Floppy Disc. The recorded data will consist of a device identification number, the digitized pulse current, and the digitized pulse voltage. The identification number will consist of eight digits and have the following format:

A B C C D D E E

where A is the lot number (1, 2), B is the wafer number (1-5), CC is the die number (01-70), DD is the structure type (01-14), and EE is the diode number (01-51). A list will be prepared showing the numbering of the dice, structure types, and diodes so that close coordination of the various test structures can be maintained between Auburn University, Rockwell, and BDM. This identification number will also be used on all photographs to identify them.

In order for BDM to utilize the data taken at Auburn University, it will be necessary to convert the data stored on the Tektronix Floppy Disc to a storage medium that is compatible with an HP9830 Calculator System (Cassette Storage) or an HP2100 series computer which utilizes a nine-track magnetic tape storage system. This problem is presently being examined to determine the most efficient method of providing this interface.

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