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0024-75-2-0739 79 The Use of Al¹⁷Ga¹¹ [¶]As Buffer Layers to Reduce Parasitic Space Charge Limited Current Flow Through the Substrate in FET Structures F. F. Eastman, D.W. Woodard, & Chandra and M. Shur Amitabh Lester simple analysis has been made of the parasitic space charge limited current flow in a GaAs substrate 22 JUN or buffer. The computed output conductance is in ()agreement with experimental values of 600 to 1000 ohms obtained on low noise FET's with 300 um gate width fabricated on GaAs buffer layers with low trap density. The parasitic current flows in the semi-insulating substrate or buffer layer, around the thin high field Gunn domain that is present in the active layer of the FET. Including the effects of changing domain length with drain bias, the parasitic current is found to rise as the square root of the drain voltage and as the 4th root of the active channel doping. (12)GaAs FET's were fabricated with undoped high purity Al Ga1- As buffer layers in order to utilize the heterojunction barrier and reduced saturation velocity to provide reduced parasitic conduction. · Output conductance of these devices are in the range of 5000 ohms. 098 850 16 N00014-75-C-0739 Date: 22 June 1979

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