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RECTIFICATION AT N-N GAAS: (GA, AL)AS HETEROJUNCTIONS,(U)
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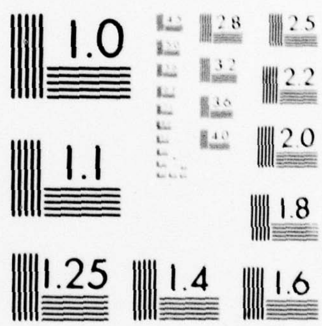

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RECTIFICATION AT n-n GaAs: (Ga,Aℓ)As HETEROJUNCTIONS

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ABSTRACT

n-n $Ga_{.7}A\ell_{.3}As$: GaAs heterojunction structures have been grown by LPE, with 1×10^{15} cm^{-3} net carriers in the ternary. N-W profiling across the heterojunction shows an accumulation region on the GaAs side and a depletion region on the (Ga,Aℓ)As side. I-V characteristics at room temperature show significant rectification.

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Introduction: A metallurgically abrupt heterojunction between n GaAs and n $Ga_{1-x}Al_xAs$ is expected to have a barrier in the conduction band edge, as shown in Fig. 1.[1,2] Current transport across this heterojunction is expected to be relatively free of the influence of interface states, whose density has been measured by Lang et al[3] to be less than $\approx 10^9$ cm^{-2}. Theoretically, therefore, thin n-n heterojunction should show rectification corresponding to a barrier height of $\sim$ .3 eV at x = 30%.[2] In addition, the barrier at a n GaAs-n^- (Ga,Al)As heterojunction should provide abrupt confinement of electrons to the GaAs side, as required in certain device concepts.[4] The rectification can therefore serve as an indicator for how effective the heterojunction is in confining electrons.

Such rectification, however, to our knowledge has not yet been reported, though Womak and Rediker[5] observed non ohmic behavior and rectification ratios of about 5:1 on a few percent of the samples examined by them. It has been suggested that the lack of a rectifying barrier is due to a metallurgical grading of the junction.[1] For a given interface transistion width, the higher the net doping in the $Ga_{1-x}Al_xAs$, the greater is the reduction of the barrier height. In attempting to obtain a rectifying barrier, therefore, both the transition width and the (Ga,Al)As net doping should be made as low as possible.

Using Auger techniques, Garner et al.[6] have measured the 10-90% Aℓ transition widths (L_c) of (Ga,Aℓ)As: GaAs heterojunctions obtained by growing a few hundred angstroms of (Ga,Aℓ)As on GaAs substrates by LPE. They obtain ∿125Å for LPE at 800°C and 100Å for LPE at 750°C. Since the heterojunction width is attributed to kinetic effects at the initiation of growth rather than the subsequent diffusion of aluminum,[5,6] it is expected that the transition width will not be any higher if thicker layers involving longer growth times are used. Furthermore, our LPE was done at 700°C, and L_c can be expected to be even lower than 100Å.

We have achieved repeatable purity in $Ga_{1-x}A\ell_xAs$, obtaining ∿ 1×10^{15} cm^{-3} in $Ga_{.7}A\ell_{.3}As$, and as low as 2.7×10^{14} cm^{-3} in $Ga_{.84}A\ell_{.16}As$.[7] Using such high purity $Ga_{1-x}A\ell_xAs$ layers in heterostructures, we have obtained significant rectification.

<u>Experiment</u>: The heterostructures grown and studied are shown in Fig. 2. They were grown on n^+ GaAs:Te substrates by LPE at 700°C using a multiple well graphite boat and the sliding technique. The heterojunction between the $Ga_{1-x}A\ell_xAs$ layer and the n^+ substrate was found to be essentially ohmic and low resistance. This was expected due to the high defect density at the interface, including the outdiffusion of donors from the substrate to a few

hundred angstroms in the layer. The GaAs adjacent to the 10^{15} n $Ga_{.7}Al_{.3}As$, at the heterojunction being studied, was doped $<10^{15}$ cm^{-3} in case (i), and 10^{17} cm^{-3} in case (ii). The 10^{17} n GaAs layer in case (i) was to prevent the low doped GaAs layer from being fully depleted at zero bias, and to provide a low resistance ohmic contact.

Samples were prepared for N-W profiling by using the self limiting anodic etch technique.[8] The voltage used (90V) was greater than the breakdown voltage of the 10^{17} n:GaAs layer, but was less than the B-V of the 10^{15} doped layers. This etching technique would enable the subsequently deposited Schottky barriers to punch through to the n^+ substrate before breakdown. After the etching, a tin dot was alloyed on the surface to form the ohmic back contact, following which gold Schottky dots were evaporated at pressures <10-6 Torr. N-W measurements were taken on an MSI junction profiler. The samples for I-V studies were prepared by evaporating Au-Ge-Ni dots with a gold over-lay, on the 10^{17} n:GaAs epilayer. The back contact to the n^+ substrate was obtained either by depositing the Au-Ge-Ni and Au on the back side, or by etching off the epilayers over a limited area to expose the n^+ substrate, and depositing ohmic dots. After the depositions, the contacts were alloyed at $\sim 460^{\circ}C$ for 20 sec. Finally, mesas were etched in $H_2O_2:NH_4OH$ (10:1) at 50^{o}C for ∿20-30 sec., using the alloyed dots as protective masks.

Results and Discussion: Fig. 3(i) shows the typical doping vs. depth profile obtained for the structure shown in Fig. 2(i). It clearly shows an accumulation region followed by a depletion region, as is expected for the n^-GaAs - n (Ga,Aℓ) As heterojucntion.[1] The presence of the former, shows that the interface barrier is not of the back to bac Schottky type as described in Reference 9. The N-W profile for the second structure (Fig 2(ii)) showed a depletion region in the n^- (Ga,Aℓ)As, as expected, but no definite accumulation region in the 10^{17} n GaAs.

No depletion region is observed in the (Ga,Aℓ)As at its interface with the n^+ substrate, suggesting that interface to be ohmic.

Fig. 4 shows typical I-V characteristics obtained at room temperature for devices of type (i). The n^+ substrate was grounded in all these measurements, and the voltage V applied to the n:10^{17} GaAs ohmic contact. Before etching the mesas, the I-V characterisitcs across various pairs of ohmic dots on the layers were tested and were always found to be ohmic with a resistiance between 15 and 25 ohms. Similarly, ohmic dots on the n^+ substrate gave ohmic resistances of ∿2-5 ohms. The I-V characteristics obtained for type (ii) devices were very similar, though slightly less rectifying (about 15% less).

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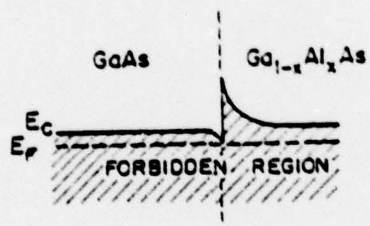
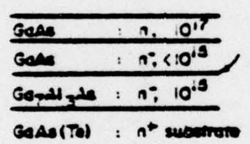
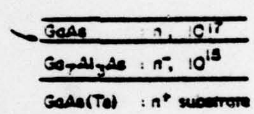
List of Illustrations



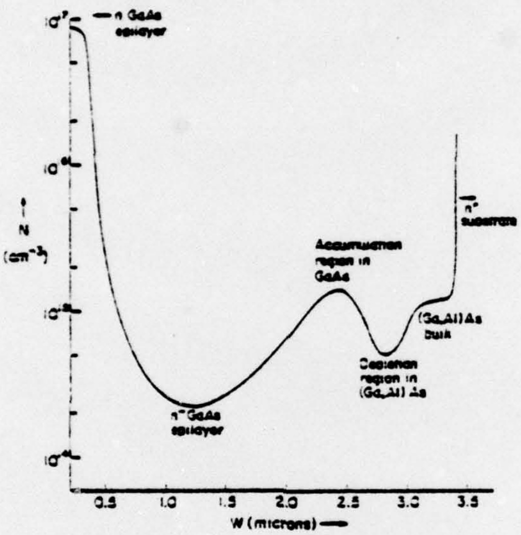
GaAs
$Ga_{1-x}Al_xAs$
E_c
E_F
FORBIDDEN REGION

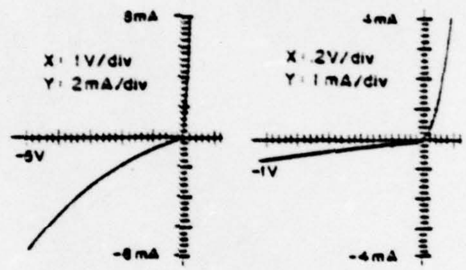

GaAs : n, 10^{17}
GaAs : n^-, $<10^{15}$
: n^-, 10^{15}
GaAs(Te) : n^+ substrate

(i)


GaAs : n, 10^{17}
: n^-, 10^{15}
GaAs(Te) : n^+ substrate

(ii)


n GaAs epilayer
N (cm^{-3})
Accumulation region in GaAs
n^{+} substrate
(Ga,Al) As bulk
Depletion region in (Ga,Al) As
n^{-} GaAs epilayer
0.5
1.0
1.5
2.0
2.5
3.0
3.5
W (microns)



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