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COMPUTER AIDED DESIGN OF PRINTED CIRCUIT BOARD LAYOUTS - WREPCL--ETC(U)
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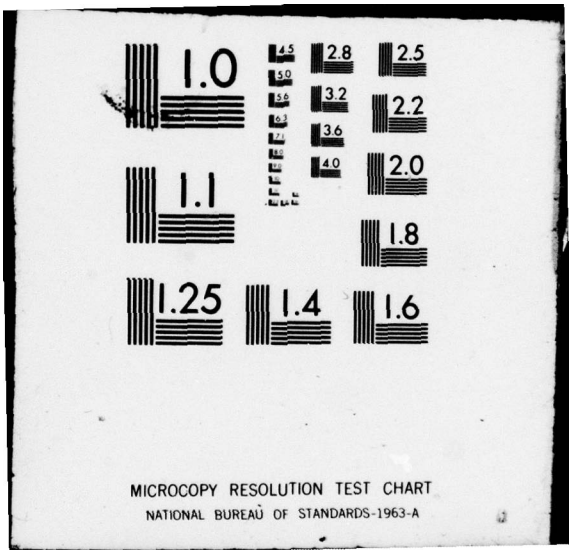
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## DEFENCE SCIENCE AND TECHNOLOGY ORGANISATION

## ADVANCED ENGINEERING LABORATORY

DEFENCE RESEARCH CENTRE SALISBURY
SOUTH AUSTRALIA

## TECHNICAL REPORT

**AEL-0012-TR**

# COMPUTER AIDED DESIGN OF PRINTED CIRCUIT BOARD LAYOUTS - WREPCL

G.L. COCK

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(10) G.L. Cock

(11) Apr 78

(12) 31p


## SUMMARY

This publication describes a program which will route wiring paths for multi-layer printed circuit boards. The results can be passed to the DRCS GRAPHICS TERMINAL or the DRCS CAPART PRINTED CIRCUIT SYSTEM where final additions or modifications may be carried out, and from which data can then be passed to a photo plotter and a numerically controlled drilling machine for board manufacture.



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# 1. INTRODUCTION

WREPCL - Wiring Routine for Printed Circuit Layouts

WREPCL has been written to suit DRCS design and manufacturing techniques for printed circuit boards and is run on the DRCS IBM370/168 computer. Incorporated within WREPCL is the program PCPATH(ref.1). WREPCL uses the Vertical/Horizontal method of conductor routing in conjunction with plated through-holes, while PCPATH uses a variation of the Lee algorithm(ref.2). The Vertical/Horizontal method is particularly suitable for board layouts containing "dual in-line" packages (DIPs). The Lee algorithm method is used when multi-layer boards are required.

In laying-out an average complexity two-layer board (e.g. twenty 16 pin DIPs on a 203,2 mm x 152,4 mm (8 in x 6 in) board), WREPCL will route approximately 95% of the wiring of the interconnections required. Completion of the board is then carried out using the DRCS Graphics Terminal(ref.3) of the DRCS CAPART Printed Circuit System which incorporates a Digitizing Plotting Table(ref.4).

On completion of the layout, photographic etching masters are produced by a photo plotter.

Coordinate and drill size information for plated through-holes and component pins is generated automatically. This information is in a format compatible with numerically controlled drilling machines.

This Technical Report describes WREPCL (Version 1.3). However, the documentation may be read in conjunction with other versions of WREPCL except that capabilities and data preparation techniques may vary slightly. Appendix I describes the WREPCL Output Data format.

A WREPCL Users Guide(ref.5) is available for DRCS personnel wishing to use the WREPCL system for the production of printed circuit boards. The WREPCL Users Guide will be updated as necessary so that users may know the capabilities, data preparation techniques and running procedures for the latest version of WREPCL that is available.

# 2. CAPABILITIES OF WREPCL (VERSION 1.3)

(1) Multi-layer board up to a total of 10 layers.

(2) Choice of routing algorithms.

(3) Maximum board size - nominal 381 mm x 381 mm (15 in x 15 in)

(4) Grid spacing - 2,54 mm (0.1 in), 1,27 mm (0.05 in) or 0,64 mm (0.025 in).

(5) Double sided connectors on one or all four edges of board.

(6) Automatic edge connector pin assignment (optional).

(7) Library of up to 20 packages (e.g. DIP) as well as provisions for discrete points. Each package may contain from 2 to 100 pins. Packages may be orientated in any of four directions (i.e. 0,90,180 or 270$^{o}$).

(8) Flexibility in placement of packages.

(9) Maximum of 150 packages per board.

(10) Maximum number of interconnected points allowable is 2000.

(11) Maximum number of interconnections (point pairs) allowable is 1500.

(12) Number of interconnected points in a single branch may vary, from 2 to 10.

(13) Priority factor for some interconnections.

(14) Provision for forced conductor routing.

(15) Provision for prohibited areas.

(16) Line printer pictures of layers.

(17) Graphical pictures of layers on Calcomp Plotter.

(18) Graphical pictures may be actual size or twice size.

(19) Easy preparation of data since the majority of points need only be referenced by a circuit diagram code and a pin number.

(20) Choice of layout characteristics. The precision of manufacturing technology will determine which class of layout should be selected.

| Characteristic | Class 1 (inches) | Class 2 (inches) | Class 3 (inches) |
|---|---|---|---|
| (i) Grid used | 0.100 | 0.050 | 0.025 |
| (ii) Conductor Widths: | | | |
| Standard | 0.030 | 0.024 | 0.016 |
| Power | 0.060 | 0.060 | 0.040 |
| (iii) Pad (Land) size: | | | |
| Plated through-holes (standard) | 0.060 | 0.060 | 0.040 |
| Plated through-holes (power) | 0.080 | 0.080 | 0.066 |
| Discrete component | 0.080 | 0.080 | 0.080 |
| Code 5 package (e.g. DIP) | 0.080 | 0.060 | 0.060 |
| Code 6 package (e.g. TO74) | 0.060 | 0.060 | 0.060 |
| (iv) Spacing: | | | |
| Min between conductors | 0.040 | 0.020 | 0.009 |
| Min between pads | 0.020 | 0.010 | 0.009 |
| Min between conductors and pads | 0.030 | 0.008 | 0.008 |
| (v) Interconnections routed for a two-layer board (approx.) | 75% | 95% | 95% |

Future versions of WREPCL could employ modifications or additions to the above list, including such items as component placement and labelling, inclusion of diagonal lines in the routing algorithm and interactive capabilities.

## 3. STRUCTURE OF PROGRAM

The basic structure of the program is shown by the flowchart in figure 1. WREPCL has been written in Fortran IV and contains approximately 5000 source instructions. An explanation of the basic operations of the major routines follows:-

(a) Main routine

This routine reads and tests the input data, calls the major sub-routines, determines the routing paths by the Vertical/Horizontal method, and transfers control to the main routine for path routing by the modified Lee algorithm (PCPATH) when required. This routine also prints the line printer pictures of the front and rear matrix for the Vertical/Horizontal layers. The front and rear of a board are each considered a matrix of points at 2,54 mm (0.1 in) spacing, or at 1,27 mm (0.05 in) spacing, or at 0.65 mm (0.025 in) spacing, depending on the grid that is

selected. A point not occupied has the value 0 and a point that is occupied has the value 1. Considerable computer storage is saved by having each point assigned to a "bit" in computer memory.

(b) Subroutine BLOP

This routine sets the matrix points to 1 for the area occupied by the edge connector. If a Calcomp plot has been requested, it draws the board outline, edge connector pins and associated pads.

(c) Subroutine CONEDG

This routine determines the actual position of edge connector pins used.

(d) Subroutine FINDER

This routine determines the position of a pin (or point) on the circuit board. Initially the code of an interconnected point is decoded. If the coordinates are supplied an exit is made from the subroutine. For a library package, the package type is first determined, then the position of its logical centre, and finally the position of the actual pin concerned.

(e) Subroutine FLIP

This routine is associated with PCPATH and is used by subroutine PUSH to flip a conductor corner.

(f) Subroutine GRAPHS

The first part of this routine optimizes the paths for Vertical/ Horizontal method so that the number of plated through-holes needed is reduced. The second part of the routine supplies the data for the Calcomp plotter for plotting the Front and Rear, and the data for the routines that convert information to a form suitable for input to the Graphics Terminal or CAPART system (see Appendix I).

(g) Subroutine PATH

This routine is associated with PCPATH and is the central routine in the path-laying part of the program. It recognises only one side of a board.

(h) Subroutine PCPATH

This is the main routine for determining paths by the Modified Lee algorithm method. PCPATH has been documented in WRE-TN-112(AP)(ref.2).

(i) Subroutine PGRID

This routine is associated with PCPATH and prints the line printer picture of a layer.

(j) Subroutine PINPT

This routine sets the appropriate matrix point to 1 for each pin point, forced point or prohibited point. If a Calcomp plot has been requested a pad is drawn at this point if it is a pin point. In some circumstances multiple matrix points are set to 1 (i.e. prohibited areas created around a pin point).

(k) Subroutine PLAYER

This routine supplies data for the Calcomp plotter for plotting each layer associated with PCPATH and the data for the routines that convert information to a form suitable for input to the Graphics Terminal or CAPART system (see Appendix I).

(l) Subroutine PUSH

This routine is associated with PCPATH and moves existing conductors clear of a grid point so that a specified adjacent unoccupied grid point remains unoccupied.

(m) Subroutine SCAN

This routine clears paths of previously connected point pairs of a branch. Hence, some paths connecting point pairs in a single branch may be coincidental (i.e. a "T" junction will occur). These paths are subsequently reset in the MAIN routine.

(n) Subroutine SEQ

This routine sequences the order in which interconnections are to be made. The basic sequence is: order of increasing distance between point pairs. The first part of the routine performs edge connector pin assignment (if necessary) and minimizes the lengths of interconnections between points in each single branch. The second part of the routine sequences interconnections in the order: prohibited points, power conductors, short connections (12,7 mm or less), standard conductor edge connector connections and then standard conductor pin to pin interconnections. The sequence of a sub-group may be altered if a priority (or weight) factor has been specified.

(o) Subroutine SETEQ

This routine clears path points (setting to 0) or sets path points (setting to 1). For power conductors, multiple rows or columns of points are set or cleared.

(p) Subroutine WANDP

This routine supplies data for the Calcomp plotter for plotting the paths for the composite picture associated with the Vertical/Horizontal method. It also prints the list of interconnections not completed and makes these available for input to subsequent layers in multi-layer applications.

(q) Subroutine WDATA

This routine lists the wiring data and makes this data available for PCPATH if the modified Lee algorithm method alone option is selected.

## 4. METHOD OF OPERATION

WREPCL permits flexibility in the positioning of components on a board. The user assigns a circuit diagram code to a library package and then places the package in any location on the layout merely by defining the coordinates of the logical centre of the package at that location. As the centre is defined by a data card, a package location can be easily changed by merely redefining the centre.

The FRONT of the board is the side containing predominantly vertical conductors. The REAR contains predominantly horizontal conductors. It is up to the WREPCL user to decide on which side the components will be placed and on which edge(s) the edge connector(s) will be placed.

When using the Vertical/Horizontal method interconnections are completed in the order: prohibited points, power conductors, short connections (12,7 mm or less), edge connector connections then standard conductor pin to pin interconnections, in order of increasing distance between pin pairs (unless a priority factor has been specified).

When using the modified Lee algorithm, only the standard conductor is avilable and interconnections are first attempted in an order that depends on the

order in which the wiring data is submitted. With this option, multiple target points are available for interconnections in any one branch. The Lee algorithm assigns the path between two points to one layer only, and hence plated through-holes are not used.

When requesting a multi-layer board, the Vertical/Horizontal method is normally used for the first two layers and the Lee algorithm for subsequent layers. WREPCL assumes that the majority of interconnections will be on the first two layers (i.e. Front and Rear).

For a multi-layer board, connections not made on the first two layers are passed on for routing on subsequent layers. The user is informed of any connections unable to be made. With the Vertical/Horizontal method eight attempts are made to connect two points, four in each direction. With each attempt the initial starting direction is altered. With the modified Lee algorithm method any path to connect a branch will be found; if previously fitted branches block the way, up to 4 earlier branches will be removed and the program will attempt to fit the branches in another order before deferring one or more to the next layer pair.

In the Vertical/Horizontal method, plated through-holes are not established if the length of a conductor in a changed direction does not exceed "one" grid unit. In this situation, the conductor path "changes direction while on the same side of the board". A similar situation arises if no "cross-overs" occur in any section of the board.

A re-tries option in the Vertical/Horizontal method allows further attempts to be made to complete connections not made on the first pass.

Depending on user options, the results are transformed into a form which can be read directly as input data for the Graphics Terminal or CAPART system.

## 5. INPUT DATA

WREPCL comprises of six types of data cards:

Label and Options card

Board outline card

Library card for creating library of packages

Locate card for positioning a package on the board

Branch Group card

Branch Interconnections card

With changes in computer technology the method of inputting data to WREPCL could take various forms. This could be by punched cards, visual display units, typewriters or partly by graphical methods.

## 6. USAGE

WREPCL requires a considerable amount of computer storage (500 k bytes for a 2-layer board, 2 M bytes for a multi-layer board) and hence can only be run on large computers. Although data preparation for WREPCL is easy, experience in component layout methods is desirable. The WREPCL Users Guide(ref.5) describes data preparation techniques, component layout methods and program execution.

## 7. LIMITATIONS

(1) For an average complexity two-layer board (e.g. twenty 16 pin DIPs on a 203,2 mm x 158,4 mm (8 in x 6 in) board) the main limitation is the percentage of interconnections not completed. This may be about 5% when using the 1,27 mm (0.05 in) grid or up to 25% when using the 2,54 mm (0.1 in) grid. When using the 0,64 mm (0.025 in) grid, the probability of all interconnections being made on two layers is close to 100%.

If only a small number of interconnections are not completed, a user could complete these by:-

(a) Repositioning components (re-LOCATE) and then rerunning job.

(b) Modifying layout using the Graphics Terminal or CAPART system.

(c) Jumper wiring.

(d) Using a multi-layer board.

(2) In multi-layer applications when using the modified Lee algorithm only, considerable computer execution time may be required to obtain a result when using the 1,27 mm (0.05 in) grid or the 0,64 (0.025 in) grid.

## 8. SAMPLE RUNS

The output for two sample runs is given in Appendix II, and Appendix III and figures 6 and 7. Sample 1 shows how to use the capabilities of WREPCL for a two layer board using the Vertical/Horizontal method. Sample 2 uses the modified Lee algorithm method, but as mentioned earlier not all the capabilities of WREPCL can be used.

Sample 1 shows how to code data for prohibited points, power conductors (including forced routing points) edge connector connections, library package pins and discrete component pins. Execution time was approximately six seconds on the IBM370/168.

Figure 8 shows only the Composite of a more complicated board using the 1,27 mm (0.05 in) grid and the Vertical/Horizontal method. Execution time for this sample was approximately forty five seconds.

Figures 9 through 12 show the plotter output of a multi-layer board using the 2,54 mm (0.1 in) grid and the combined algorithms. The various changes in direction of paths on layers 3 and 4 are due to the paths avoiding plated through-holes connecting paths on the front and rear. Execution time for this multi-layer board was approximately two minutes.

Figure 13 shows a copy of photographic etching masters produced from WREPCL via CAPART system.

## 9. ACKNOWLEDGEMENTS

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## APPENDIX I

## WREPCL OUTPUT DATA FORMAT

Record 1: Header record - Up to 50 alpha-numeric characters

Record 2: Overall layout dimensions (length and height) and number of layers - 3I7

Then may follow any combination of the following:

General Form: I J F to format 3I7, where F is function code

(1) Rectangle

| | | | |
|---|---|---|---|
| LYR | 0 | 16 | |
| ($x_1$ | $y_1$ | (-1 or -2) | -1 Absolute |
| ($x_2$ | $y_2$ | (-1 or -2) | -2 Incremental |
| | . | | |
| | . | | |
| | . | | |
| | . | | |
| | . | | |
| | . | | |
| ($x_n$ | $y_n$ | (-1 or -2) | |
| ($x_{n+1}$ | $y_{n+1}$ | (-1 or -2) | |

When LYR is non-zero it overrides the value set by the LAYER function.

If ($x_1$ ,$y_1$) and ($x_2$ ,$y_2$) are both absolute - treated as two opposite corners of a rectangle

If ($x_2$ ,$y_2$) are incremental - interpreted as length and height respectively

If ($x_1$ ,$y_1$) are incremental - treated as displacements from last (x,y) specified

(2) Track

| | | | |
|---|---|---|---|
| LYR | TWIDTH | 17 | |
| $x_1$ | $y_1$ | (-1 or -2) | -1 Absolute |
| $x_2$ | $y_2$ | . | -2 Incremental |
| . | . | . | |
| . | . | . | |
| . | . | . | |
| $x_n$ | $y_n$ | . | |

Specifies a track TWIDTH units wide between ($x_1$ ,$y_1$), ($x_2$ ,$y_2$), ....., ($x_n$,$y_n$).

If LYR is non-zero it overrides value set by LAYER function.

(3) Pad

| | | | |
|---|---|---|---|
| LYR | PSIZE | 18 | |
| $x_1$ | $y_1$ | (-1 or -2) | -1 Absolute |
| . | . | . | -2 Incremental |
| . | . | . | |
| . | . | . | |
| $x_n$ | $y_n$ | . | |

Specified 'n' pads of PSIZE centred on points ($x_1$ ,$y_1$) ....., ($x_n$,$y_n$)

If LYR is non-zero it overrides value set by LAYER function.

(4) Layer

| | | | |
|---|---|---|---|
| 0 | LAYER | 19 | |

All items following are considered to be on layer No. LAYER.
(All layers code : LAYER = 146)

(5) Group

| | | | |
|---|---|---|---|
| IDENT | 0 | 20 | (start of a group) |

Up to 20 RECTANGLE,PAD,TRACK or
GROUP SELECT elements

| | | | |
|---|---|---|---|
| IDENT | 1 | 20 | (end of a group) |

IDENT is a unique number assigned sequentially to each group defined.
Up to 32 such groups may be defined.

(6) Grid

| | | | |
|---|---|---|---|
| 0 | GRID | 21 | (not used) |

(7) Group select

| | | | |
|---|---|---|---|
| IDENT | ORIENT'N | 22 | |
| $x_1$ | $y_1$ | (-1 or -2) | -1 Absolute |
| . | . | . | -2 Incremental |
| . | . | . | |
| . | . | . | |
| $x_n$ | $y_n$ | . | |

Specifies 'n' occurrances of the GROUP indicated by IDENT

ORIENT'N = (Mx + My + R)

Mx = 2 if mirror X-axis
My = 1 if mirror Y-axis
R = 0 0°
4 90°
8 180°
12 270°

anit-clockwise rotation

(8) End of data

| | | |
|---|---|---|
| 1 | 1 | 31 |

# APPENDIX II

## LINE PRINTER OUTPUT FOR SAMPLE NO.1

```
**********************
*  dREPCL 1.3 (NOV 77)  *
**********************

TITLE:                  SAMPLE NO.1                                          DATE: 10/04/78
LAYOUT CLASS:           1
LAYER CODE:             0
PRINTER PICTURE CODE:   0
PLOT CODE:              1
PLOT SCALE:             1
OUTPUT CODE:            0
HORIZ DIST TO (0,0): 0.500      VERT DIST TO (0,0): 0.200

BOARD DIMENSIONS-- LENGTH:  2.800
                   HEIGHT:  2.500
 10 CONNECTOR PINS PER SIDE ON EDGE 1,STARTING  0.390 IN. UP
  0 CONNECTOR PINS PER SIDE ON EDGE 2,STARTING  0.0   IN. OVER
  0 CONNECTOR PINS PER SIDE ON EDGE 3,STARTING  0.0   IN. UP
  0 CONNECTOR PINS PER SIDE ON EDGE 4,STARTING  0.0   IN. OVER
SPACING FOR ALL CONNECTOR PINS:                 0.156
WIDTH OF EDGE CONNECTOR PINS:                   0.080
DIRECTION OF PIN NUMBERING AND SIDE OF PIN 1: -2

LIBRARY    CODE= 11    NO.PADS= 16    PAD POINTS= 5 -4  2, 5 -3  2, 5 -2  2, 5 -1  2, 5  0  2, 5  1  2, 5  2  2, 5  3  2
LIBRARY    CODE= 11    NO.PADS= 16    PAD POINTS= 5  3 -1, 5  2 -1, 5  1 -1, 5  0 -1, 5 -1 -1, 5 -2 -1, 5 -3 -1, 5 -4 -1
LOCATE     CIRCUIT CODE=  1     LIBRARY CODE= 11     COORDINATES OF PACKAGE LOGICAL CENTRE= ( 0.5, 1.5)
LOCATE     CIRCUIT CODE=  2     LIBRARY CODE= 11     COORDINATES OF PACKAGE LOGICAL CENTRE= ( 0.5, 0.5)
LOCATE     CIRCUIT CODE=  3     LIBRARY CODE= 11     COORDINATES OF PACKAGE LOGICAL CENTRE= ( 1.5, 1.5)
LOCATE     CIRCUIT CODE=  4     LIBRARY CODE= 11     COORDINATES OF PACKAGE LOGICAL CENTRE= ( 1.5, 0.5)

BRANCH  WIRING DATA--
PROMID    9016010 9017010 9018010 9019010 9016012 9017012 9018012 9019012 9019011 9016011
 0V         310010  310020  400116  400216  400316  400416 1002008 2010009 2005003
+5V         310001  310011  400109  400208  400308  40040A 2015018 2020010 201500A 1009017
SIGA        310018     215
SIGB        310003     103
SIGC        310015     115
SIGD        310005     402
SIGE        310004     313
SIGF        310017     201
               210     403 1013009
               112 1009015
               310 1016009
               411     211     406
               205 1005008

***** PLOTTER OUTPUT PRODUCED *****

THERE ARE  53 DATA POINTS
THERE ARE  14 BRANCHES
THERE ARE  39 POINT PAIRS

THE FOLLOWING PATHS USE POWER CONDUCTOR-
   1- PATH FOR POINT PAIR 9016010 9017010 WAS COMPLETED.
   2- PATH FOR POINT PAIR 9016010 9016011 WAS COMPLETED.
   3- PATH FOR POINT PAIR 9017010 9018010 WAS COMPLETED.
   4- PATH FOR POINT PAIR 9018010 9019010 WAS COMPLETED.
   5- PATH FOR POINT PAIR 9019010 9019011 WAS COMPLETED.
   6- PATH FOR POINT PAIR 9016012 9017012 WAS COMPLETED.
   7- PATH FOR POINT PAIR 9016012 9016011 WAS COMPLETED.
   8- PATH FOR POINT PAIR 9017012 9016012 WAS COMPLETED.
   9- PATH FOR POINT PAIR 9018012 9019012 WAS COMPLETED.
  10- PATH FOR POINT PAIR  310010  310020 WAS COMPLETED.
  11- PATH FOR POINT PAIR  310020  400716 WAS COMPLETED.
  12- PATH FOR POINT PAIR  400216 1002008 WAS COMPLETED.
  13- PATH FOR POINT PAIR  400216 2005003 WAS COMPLETED.
  14- PATH FOR POINT PAIR  400316 2010009 WAS COMPLETED.
  15- PATH FOR POINT PAIR  400416 2010009 WAS COMPLETED.
  16- PATH FOR POINT PAIR  400116 1002008 WAS COMPLETED.
  17- PATH FOR POINT PAIR  400416 2005003 WAS COMPLETED.
  18- PATH FOR POINT PAIR  310001  310011 WAS COMPLETED.
  19- PATH FOR POINT PAIR  400109 1009017 WAS COMPLETED.
  20- PATH FOR POINT PAIR  400308 2015018 WAS COMPLETED.
  21- PATH FOR POINT PAIR  400409 2015018 WAS COMPLETED.
  22- PATH FOR POINT PAIR  40040A 2020010 WAS COMPLETED.
  23- PATH FOR POINT PAIR 2015018 1009017 WAS COMPLETED.
  24- PATH FOR POINT PAIR  400208 2015009 WAS COMPLETED.
  25- PATH FOR POINT PAIR  400108 2020010 WAS COMPLETED.
  26- PATH FOR POINT PAIR  310001  400108 WAS COMPLETED.
THE FOLLOWING PATHS USE STANDARD CONDUCTOR-
  27- PATH FOR POINT PAIR     403 1013009 WAS COMPLETED.
  28- PATH FOR POINT PAIR     112 1009015 WAS COMPLETED.
  29- PATH FOR POINT PAIR     411     406 WAS COMPLETED.
  30- PATH FOR POINT PAIR     205 1005008 WAS COMPLETED.
  31- PATH FOR POINT PAIR  310018     215 WAS COMPLETED.
  32- PATH FOR POINT PAIR  310003     103 WAS COMPLETED.
  33- PATH FOR POINT PAIR  310015     115 WAS COMPLETED.
  34- PATH FOR POINT PAIR  310005     402 WAS COMPLETED.
  35- PATH FOR POINT PAIR  310004     313 WAS COMPLETED.
  36- PATH FOR POINT PAIR     310 1016009 WAS COMPLETED.
  37- PATH FOR POINT PAIR     210     403 WAS COMPLETED.
  38- PATH FOR POINT PAIR     411     211 WAS COMPLETED.
PATHS COULD NOT BE FOUND FOR THE FOLLOWING INTERCONNECTIONS
              SIGF      310017     201

   70 PATH SEGMENTS ARE USED IN THE SOLUTION.
```

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# APPENDIX III

## LINE PRINTER OUTPUT FOR SAMPLE NO.2

```
**********************
*  WRLPCL 1.3 (NOV 77)  *
**********************

TITLE:                  SAMPLE NO. 2                                    DATE: 10/04/78
LAYOUT CLASS:           1
LAYER CODE:             4
PRINTER PICTURE CODE:   0
PLOT CODE:              2
PLOT SCALE:             1
OUTPUT CODE:            0
HORIZ DIST TO (0,0): 0.500      VERT DIST TO (0,0): 0.200

BOARD DIMENSIONS-- LENGTH:  4.000
                   HEIGHT:  3.200
  8 CONNECTOR PINS PER SIDE ON EDGE 1,STARTING  0.700 IN. UP
  0 CONNECTOR PINS PER SIDE ON EDGE 2,STARTING  0.0   IN. OVER
  4 CONNECTOR PINS PER SIDE ON EDGE 3,STARTING  1.100 IN. UP
  0 CONNECTOR PINS PER SIDE ON EDGE 4,STARTING  0.0   IN. OVER
SPACING FOR ALL CONNECTOR PINS:                 0.200
WIDTH OF EDGE CONNECTOR PINS:                   0.080
DIRECTION OF PIN NUMBERING AND SIDE OF PIN 1: -2

LIBRARY    CODE= 11    NO.PADS= 14    PAD POINTS= 5 -3 -1, 5 -2 -1, 5 -1 -1, 5  0 -1, 5  1 -1, 5  2 -1, 5  3 -1, 5  3  2
LIBRARY    CODE= 11    NO.PADS= 14    PAD POINTS= 5  2  2, 5  1  2, 5  0  2, 5 -1  2, 5 -2  2, 5 -3  2,
LOCATE     CIRCUIT CODE=  2     LIBRARY CODE= 12     COORDINATES OF PACKAGE LOGICAL CENTRE= ( 2.2, 2.2)
LOCATE     CIRCUIT CODE=  4     LIBRARY CODE= 14     COORDINATES OF PACKAGE LOGICAL CENTRE= ( 0.7, 2.2)
LOCATE     CIRCUIT CODE=  1     LIBRARY CODE= 14     COORDINATES OF PACKAGE LOGICAL CENTRE= ( 2.2, 0.7)
LOCATE     CIRCUIT CODE=  3     LIBRARY CODE= 14     COORDINATES OF PACKAGE LOGICAL CENTRE= ( 0.7, 0.7)

BRANCH  WIRING DATA--
 0V         330001     114     214     414     314
+5V         330002     107     207     407     307
              308   310008
              402   310003
              404   310004
              412   310002
              109     202
              111     102     201
              103     109
              203     209     204
              210     214     213
              205   330004
              206   310001
              208     302     303
              211     305
              312     311
              114     301     304   330003
              101     212     313     112
              306     401     403     405     409     411     413

***** PLOTTER OUTPUT PRODUCED *****

***** LEE ALGORITHM ENTERED

'NODE' HERE REFERS TO ALL THE POINTS THAT ARE MUTUALLY
CONNECTED BY ONE OR MORE CONDUCTOR PATHS

NODE  1 -   330001     114     214     414     314     210     213     301     304  330003

NODE  2 -   330002     107     207     407     307

NODE  3 -      308   310008

NODE  4 -      402   310003

NODE  5 -      404   310004

NODE  6 -      412   310002

NODE  7 -      109     202

NODE  8 -      111     102     201

NODE  9 -      103     109

NODE 10 -      203     209     204

NODE 11 -      205   330004

NODE 12 -      206   310001

NODE 13 -      208     302     303

NODE 14 -      211     305

NODE 15 -      312     311

NODE 16 -      101     212     313     112

NODE 17 -      306     401     403     405     409     411     413

  55 PINS JOINED BY THE ABOVE NODES

SOLUTION FOUND.
```

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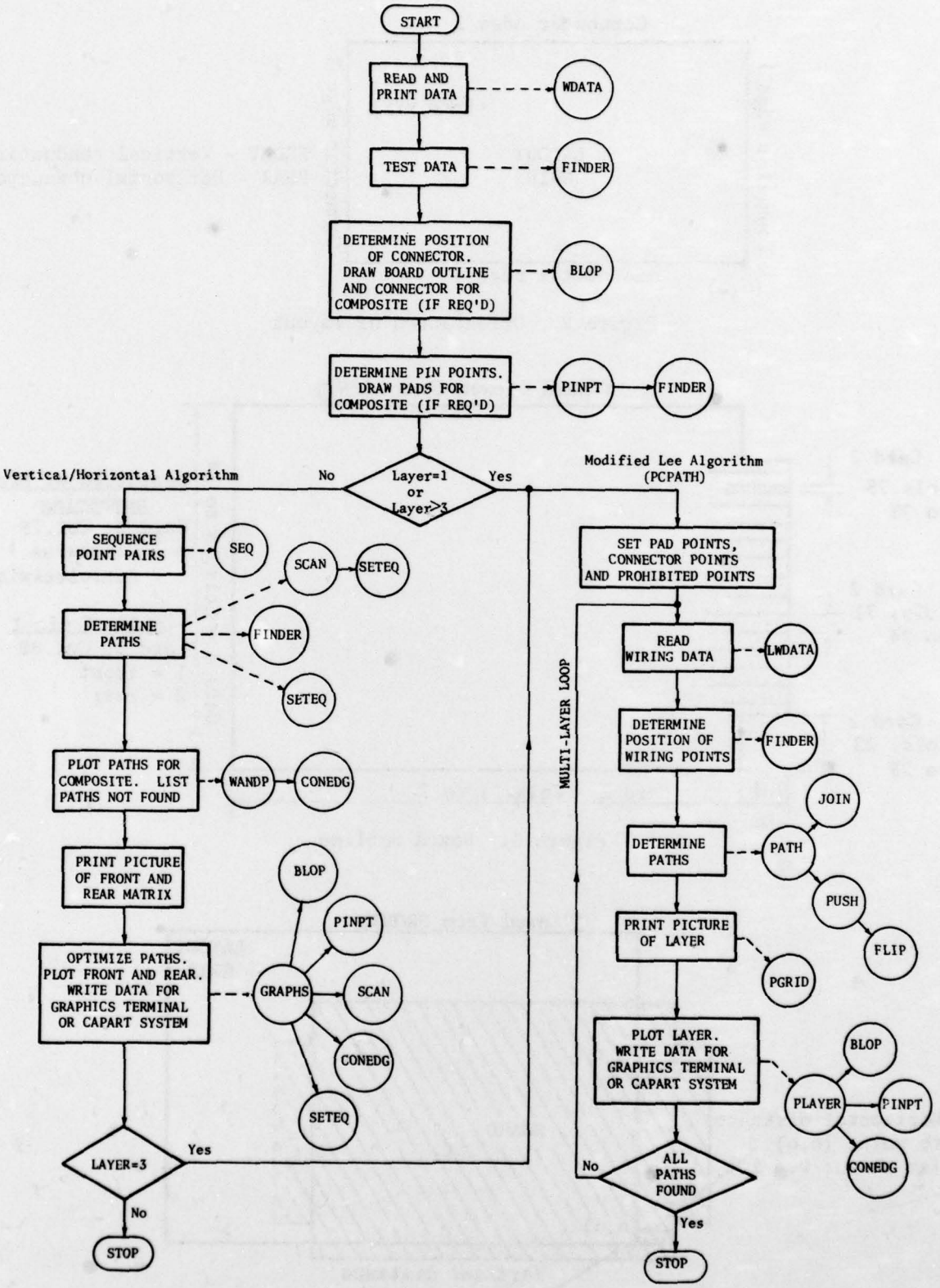



Figure 1. Flowchart of WREPCL

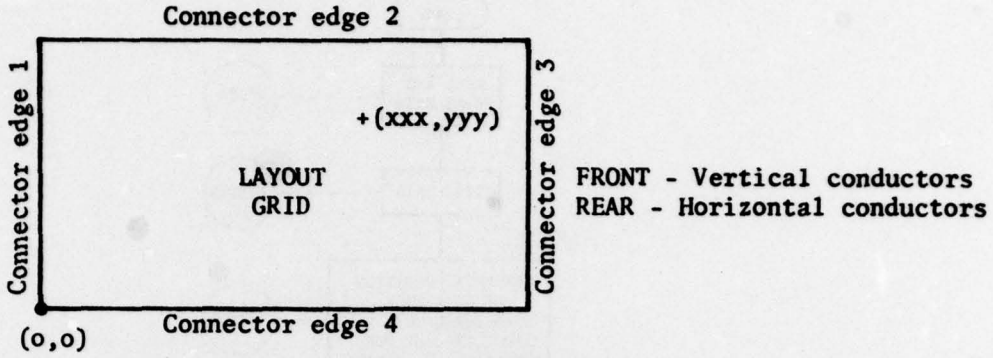



Figure 2. Orientation of layout

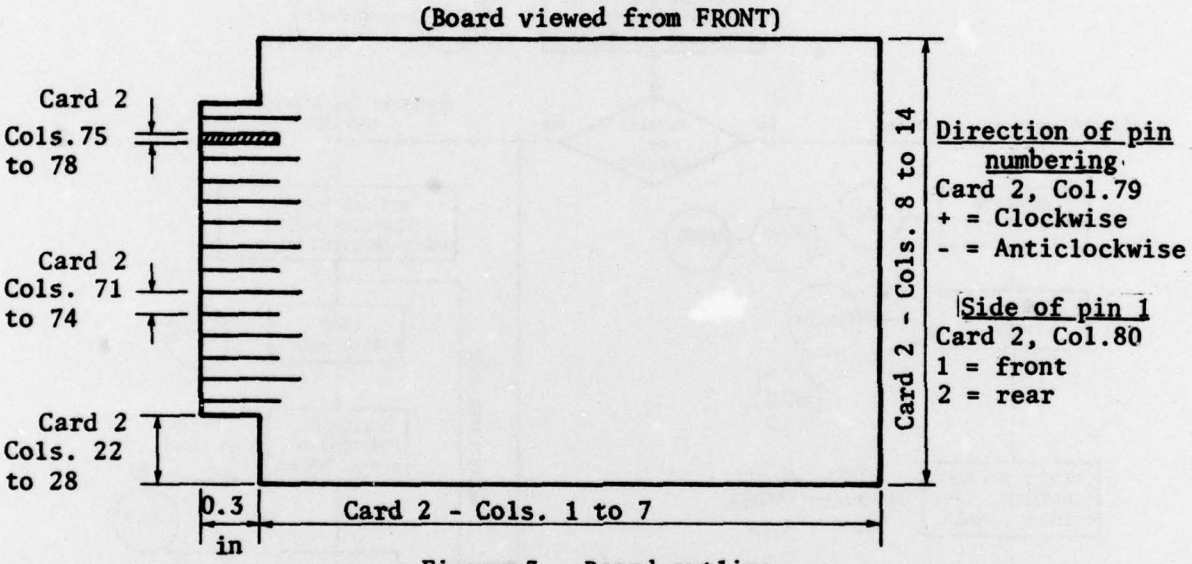



Figure 3. Board outline

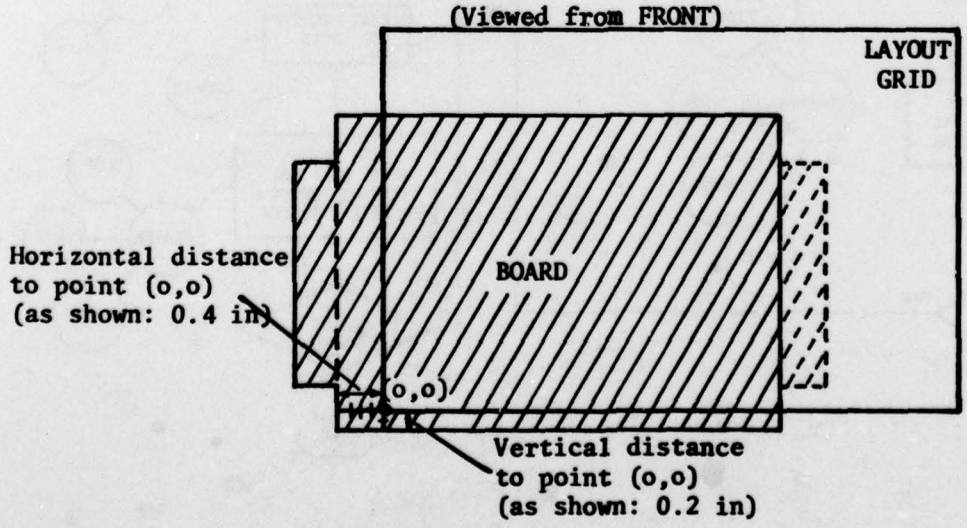
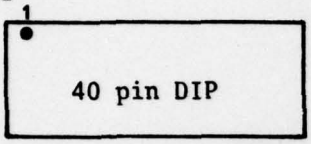
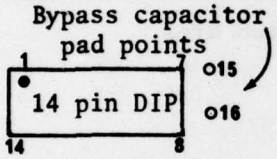
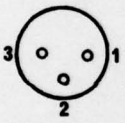
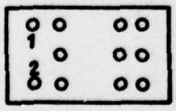



Figure 4. Locating board with respect to layout grid

| Basic orientation | Anti-clockwise rotation | | |
|---|---|---|---|
| $0^o$ | $90^o$ | $180^o$ | $270^o$ |
| 11   | 12 | 13 | 14 |
| 21   | 22 | 23 | 24 |
| 31 Bypass capacitor pad points   | 32 | 33 | 34 |
| 41 A transistor   | 42 | 43 | 44 |
| 51 A circular package   | 52 | 53 | 54 |
| 61 A miniature relay   | 62 | 63 | 64 |
| 71 | 72 | 73 | 74 |
| 81 | | | |

NOTES

1. Basic orientation only specified on LIBRARY card.
2. Any of four orientations of a package selected by quoting appropriate number code on LOCATE card.
3. A package is "LOCATED" on the board by indicating the position on the board of the "logical" centre of the package.

**Figure 5. A sample library**

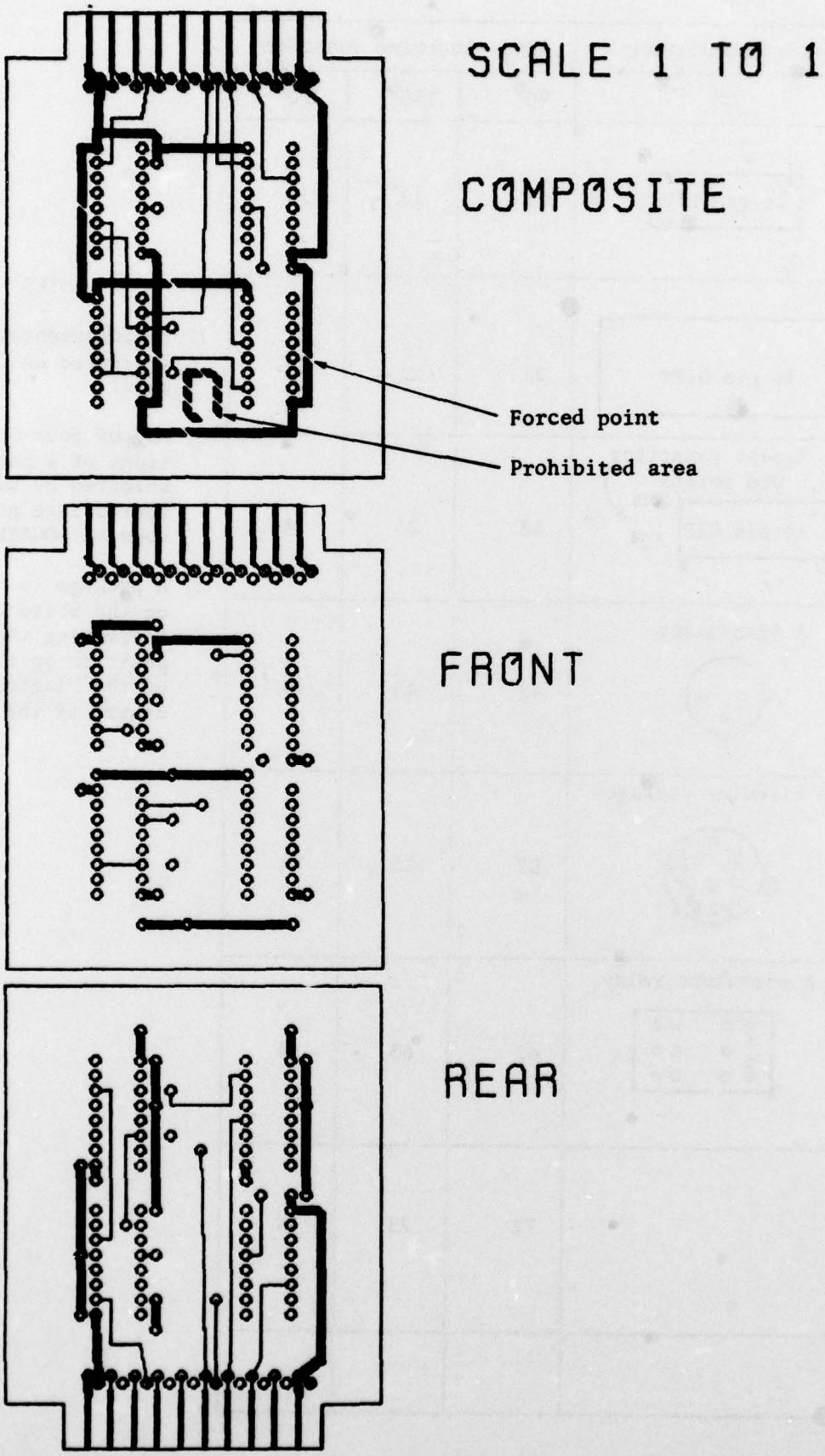
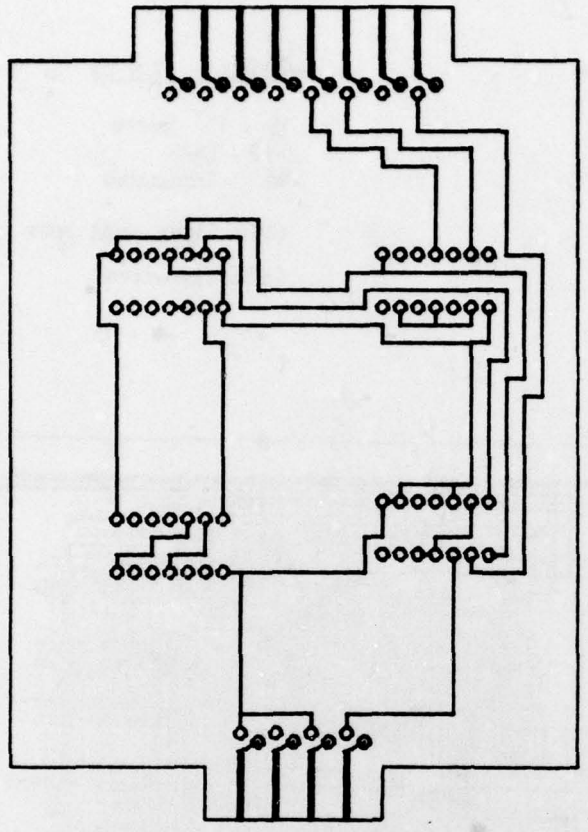



Figure 6. Plotter output for sample No.1



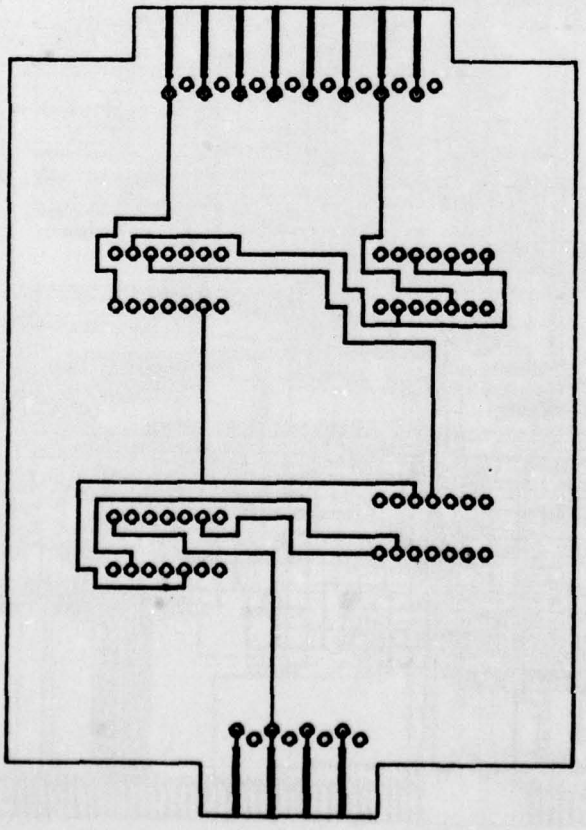




Figure 7. Plotter output for sample No.2

AEL-0012-TR
Figure 8

SCALE 1 TO 1

WREPCL - 7.8.78

15" x 15" Board
142 DIPS
14 Transistors

1259 Signal point pairs

95% Connected

COMPOSITE

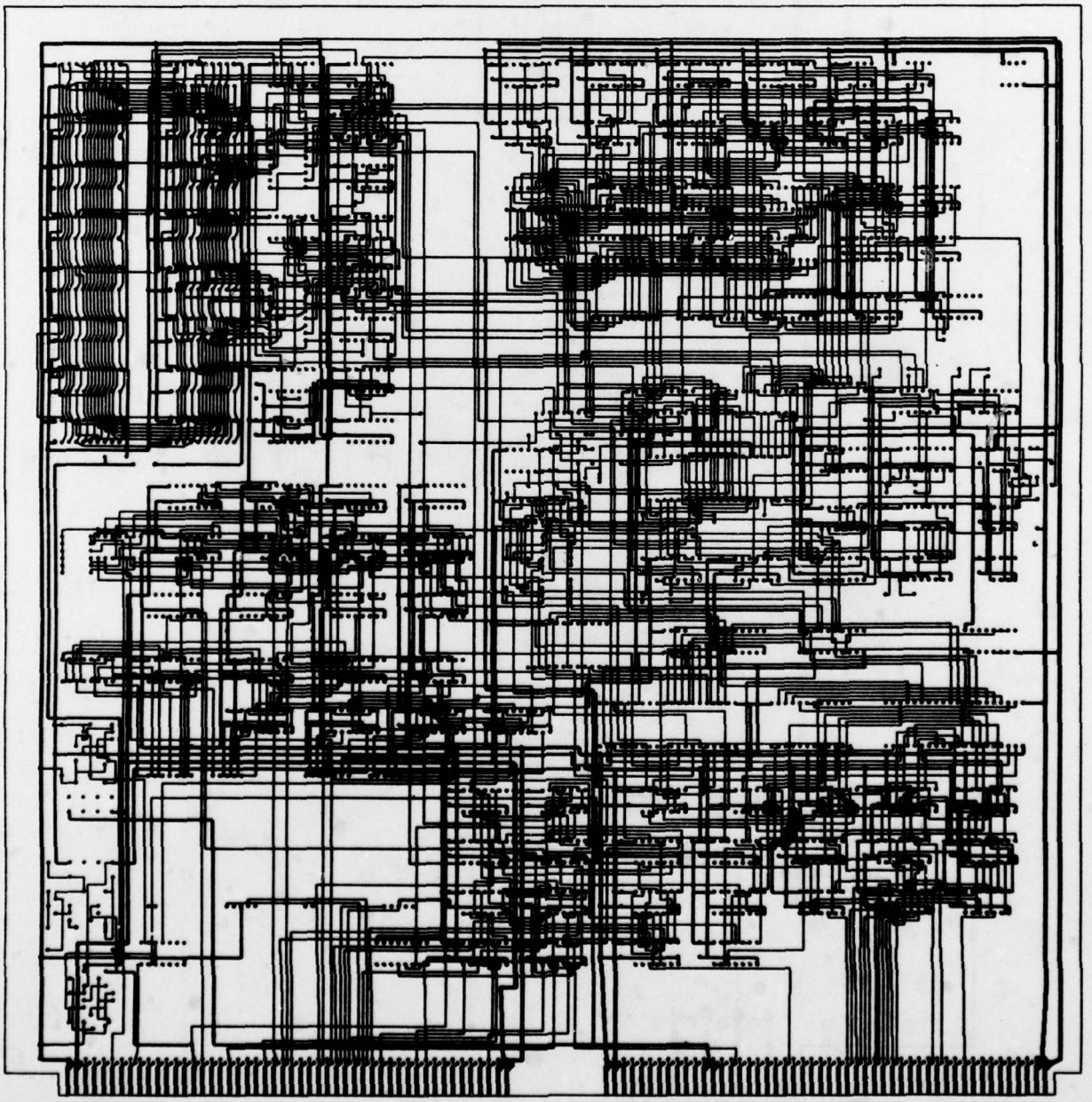


Figure 8. Composite plotter output using 1,27 mm (0.05 in) grid

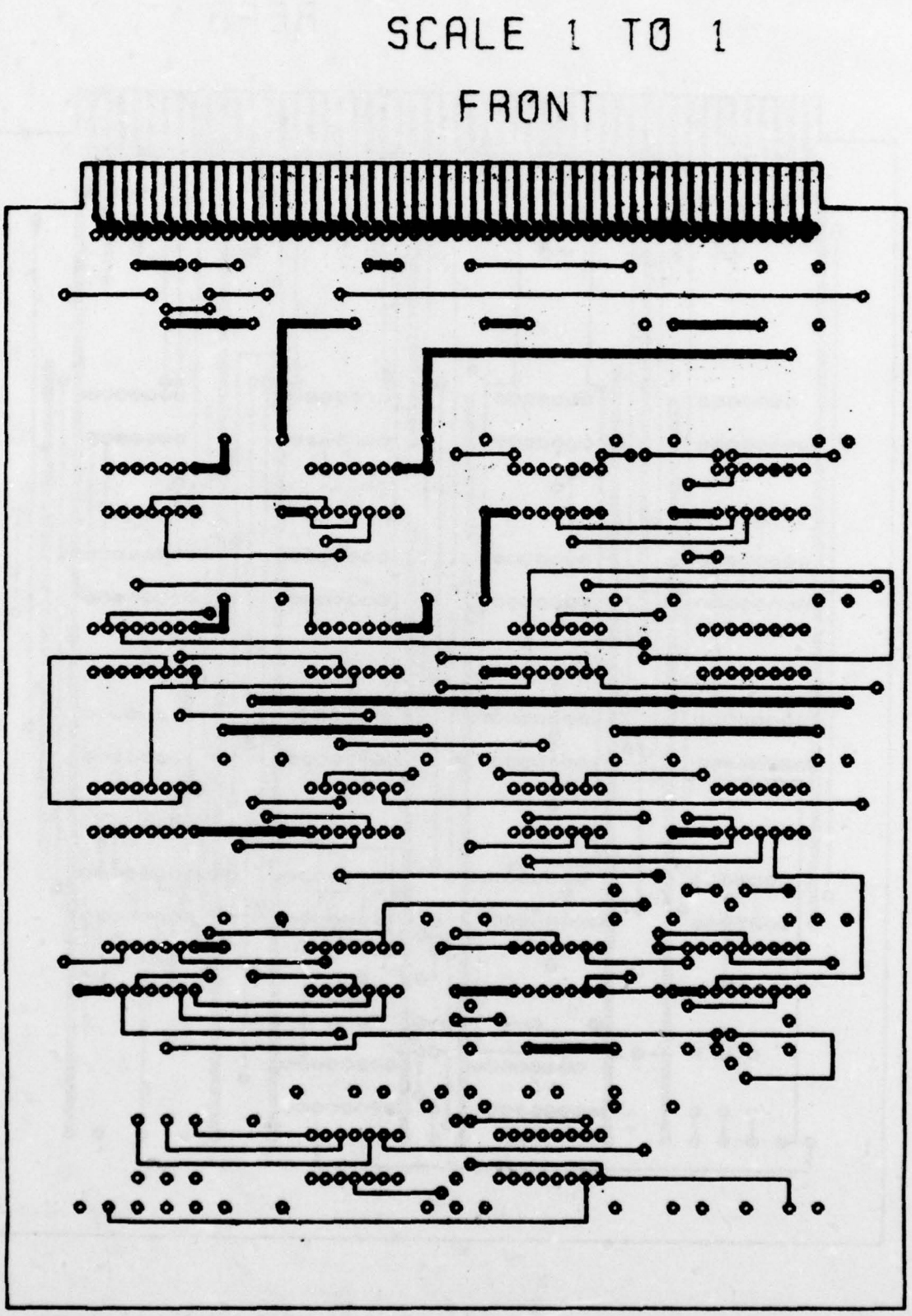



Figure 9. Multi-layer board using the 2.54 mm (0.1 in) grid - front

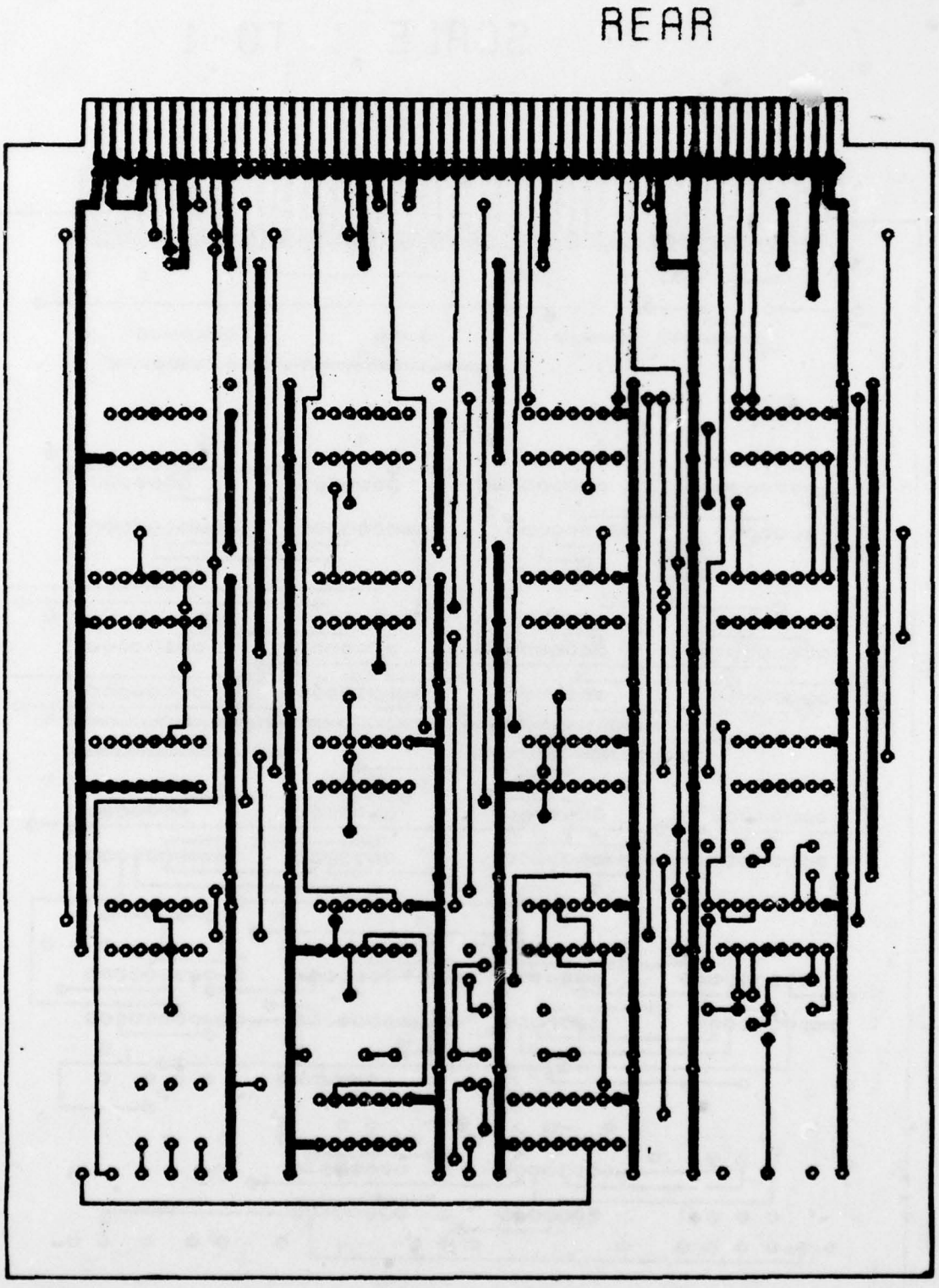



Figure 10. Multi-layer board using the 2.54 mm (0.1 in) grid - rear

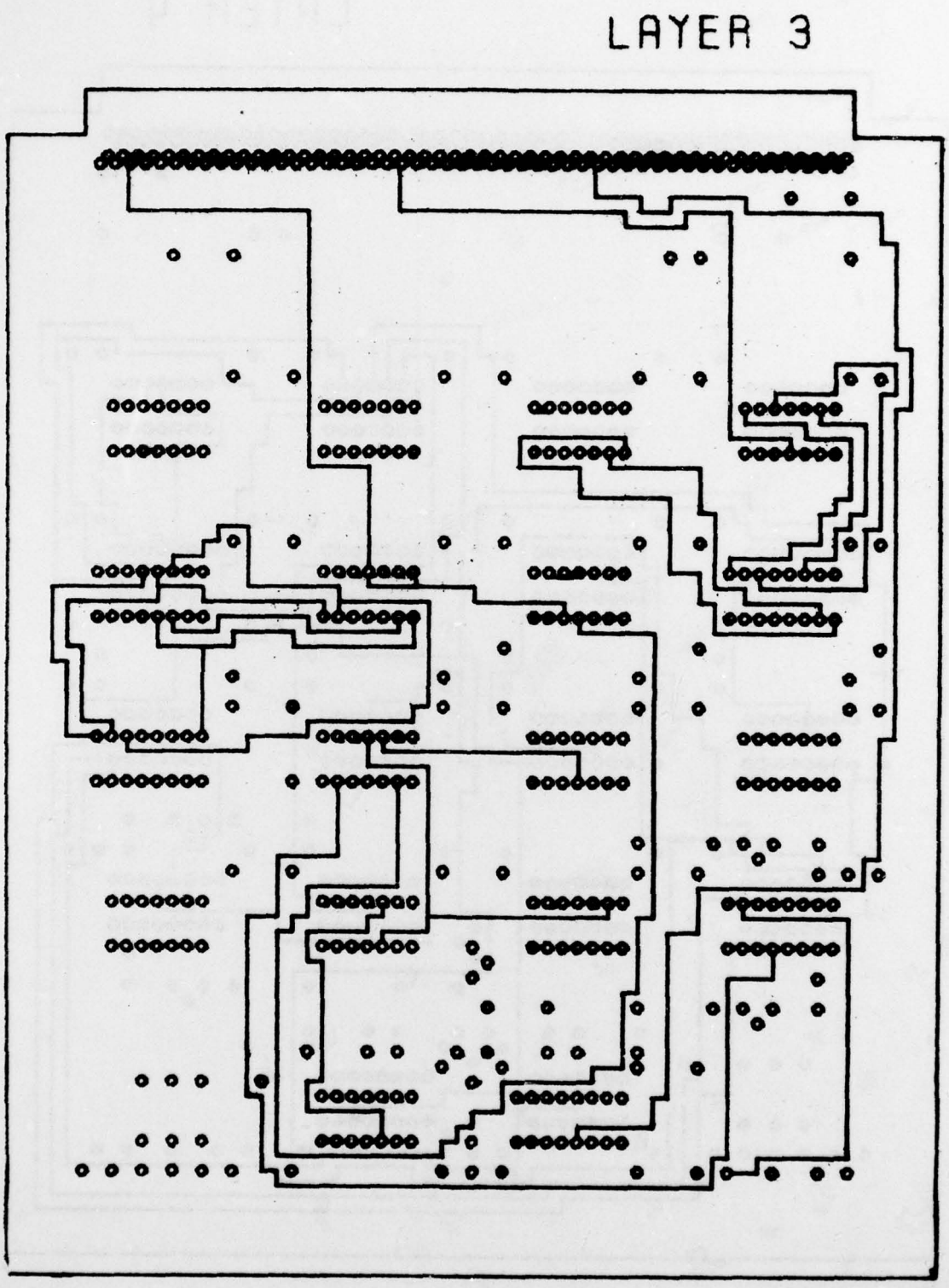



Figure 11. Multi-layer board using the 2.54 mm (0.1 in) grid - layer 3

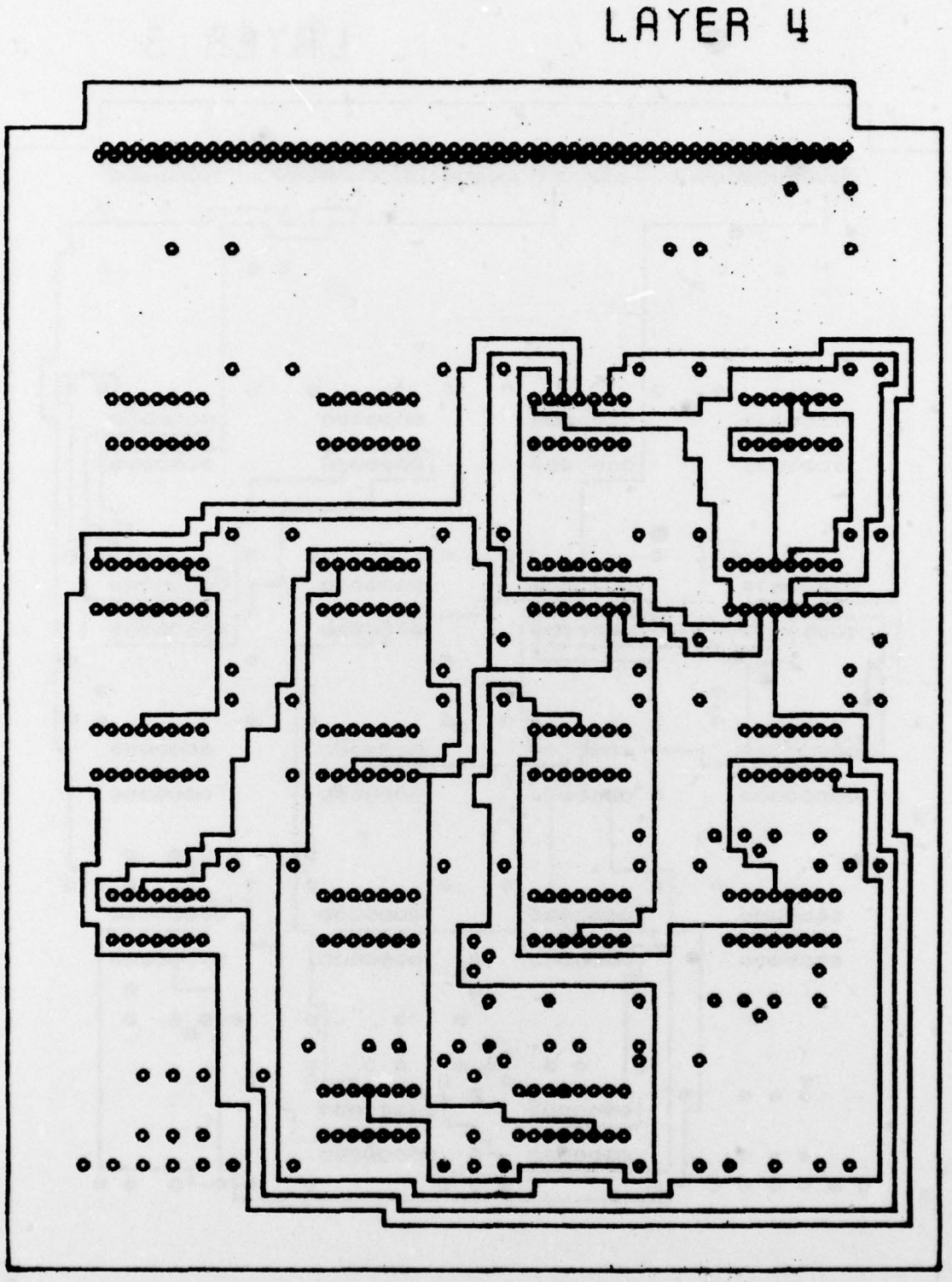



Figure 12. Multi-layer board using the 2.54 mm (0.1 in) grid - layer 4

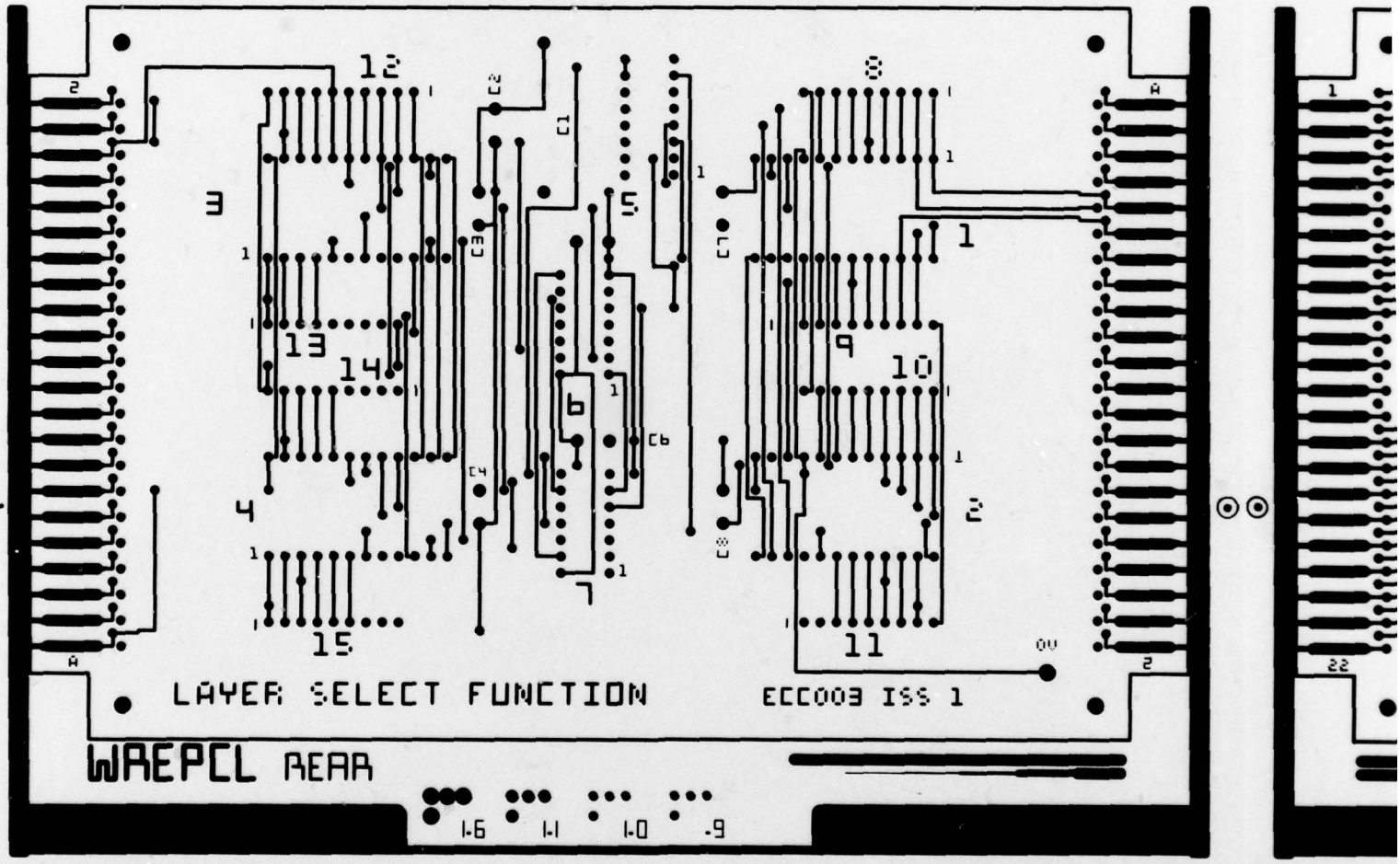
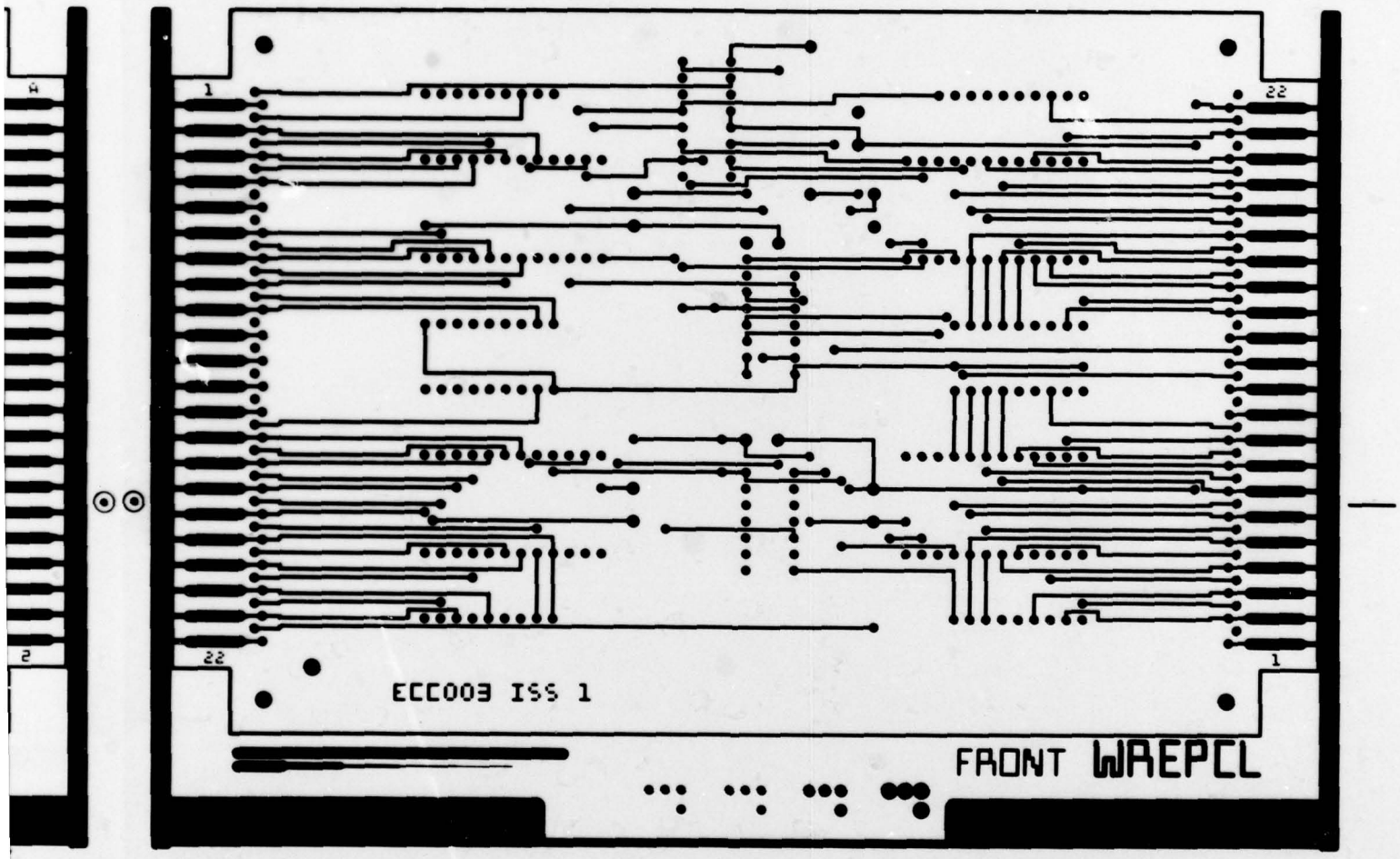



Figure 13. Copy of photographic etching masters -




ic etching masters - produced via CAPART system

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