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NANOSECOND PULSERS FOR MM WAVE TUBES. (U)

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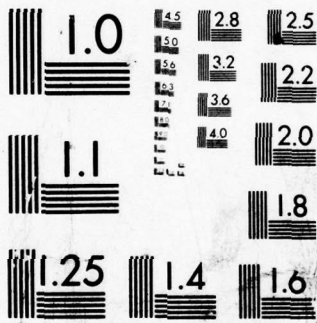
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NANOSECOND PULSERS FOR MM WAVE TUBES

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J. STOVER, N. KOMATSU
HUGHES AIRCRAFT COMPANY
GROUND SYSTEMS GROUP
FULLERTON, CA 92634

July 1979

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ABSTRACT

No decision has been reached as to the semiconductor device that will be used as the switching element for the nanosecond pulsers. The evaluation of avalanche transistors, VMOS FET, and LASS devices is continuing. A contributing factor to the lack of progress during the early months of the contract was program staffing problems and late arrival of critical test equipment.

SUMMARY

Extensive time is being expended on the selection of the switching device as the selected switching device will probably be used on all three tasks (Task A, B, and C of the technical guidelines).

Initial consideration was given to the avalanche switching transistors because of their original success in obtaining fractional nanosecond rise and fall times in the 500-600 volt region in the 1963-65 era.

Next consideration was given to the VMOS FET operating in the avalanche mode. Only the avalanche mode of operation has been considered, since fractional nanosecond rise and fall times are desired. Normal operation of these devices yields rise and fall times in the 2-5 nanosecond region.

Lastly, consideration has been given to the LASS (Light Activated Silicon Switch), but this device still exists pretty much as a laboratory curiosity and it is doubtful that hardware deliveries could be predicted based upon this device.

Through this reporting period the only switching circuitry under consideration has been the Marx modulator circuit. This circuitry has been investigated using avalanche transistors as switching devices. Up to six series cascaded stages have been investigated.

PROGRAM OBJECTIVES

The efforts of this program are directed towards the development of three separate nanosecond pulsers for MM Wave Tubes. The performance requirements for the three tasks are listed in Table 1.

The basic configuration of the pulser will be that of a Marx modulator. This is shown in Figure 1. In this modulator configuration the capacitors are all charged in parallel from d-c charging power represented in Figure 1 by a battery through isolating impedances (here represented by inductors) and isolating diodes. The capacitors, upon reaching a certain preselected voltage level determined by the breakdown voltage of the switching device used, are effectively connected in series across the output load when the switching device is caused to move from a nonconducting to a conducting state. The switching device is represented in Figure 1 by an avalanche transistor. However the Marx circuit is not limited to the use of avalanche transistors, but can be used with avalanche diodes, LASS, conventional switching transistors, spark gaps and electron tube switches.

The selection of the Marx circuit is primarily based upon the low voltage switching levels of existing semiconductor devices, and the modulator requirements of switching 2 to 13 kilovolt pulses into the load. Thus, the features of the Marx Circuit (that of charging in parallel and discharging in series) naturally lend themselves to semiconductor switching devices. Another consideration for selecting the Marx circuit was the fractional nanosecond rise and fall times achieved at the 7 kilowatt peak power level in 1963-65 era.

As presently envisioned, the Marx circuit would be utilized for the high speed sub-nanosecond switching portions of all three tasks.

PROGRAM ORGANIZATION

The importance of meeting the program requirements as contained in the contract technical guide lines, and the extreme technical challenge anticipated is mirrored in the project organization shown in Figure 2 where the top technical and managerial skills are brought to bear on this program.

Technically, the three major pulser tasks will be accomplished in three separate, but serial developments. Initially, our technical assault will be focused upon the Task A requirements (the easiest of the three tasks) and the move into the more technically difficult tasks of Task B and lastly, Task C.

Our technical approach to each task will be first to select the switching device based upon switching speed, peak current per switching device, and peak voltage switched per device. Next, we will optimize the switching device performance in a switch element (a switch element being defined as that circuitry using one switching device). Then we will optimize the switch element performance in a switch module (a switch module being defined as the maximum number of series connected switch elements that can achieve the switching speeds required). This will be followed by the parallel connection of switch modules (if required) to obtain the peak switching power required. Lastly we will develop the matching network to match the modulator to the load.

With the nanosecond pulser development completed for a given task, we will then develop the power supplies, trigger circuitry, and other ancillary circuitry required.

Continually throughout this program efforts will be expended to develop the instrumentation and magnetic components required for this program.

A detailed organizational outline of this program is shown in Figure 2.

NANOSECOND PULSER DESIGN

Switching Device Selection

Three different types of switching devices are being considered for this program. These devices are the bipolar junction transistor (BJT) operating in the avalanche mode, the VMOS FET, and the LASS (Light Activated Silicon Switch).

Both BJTs and transistors specifically made to operate in the avalanche mode have been tested. The two BJTs which have been tested were the 2N3020 and 2N2219A. The slower switching speed of the 2N3020 eliminated that device from consideration. The 2N2219A transistors tested were manufactured by Raytheon, National, and Fairchild with the highest yield of acceptable devices (25%) coming from those manufactured by Fairchild. VMOS FETs presently manufactured by Siliconix have been tested to determine if the device exhibits an avalanche mode of operation. Contrary to Siliconix technical representatives opinions that their VMOS FETs would not operate in the avalanche mode, three FETs (the VMP1, the 2N6661, and the 2N6658) operated in the avalanche mode by applying a trigger to the gate with drain to source voltage beyond the absolute maximum ratings. Rise times from 1.5 to 2.0 nanoseconds have been achieved. Further evaluation of the rise time must be made using an improved gate driving source and triggering of the drains of the devices must be investigated. A fourth unit, the VMP4 VMOS FET which incorporates r-f type construction features failed to avalanche. The reasons why the first three types of VMOS FETs avalanched successfully while the VMP4 did not, has not been determined. When sufficient data is accumulated a Siliconix technical representative will be contacted to discuss this application and resolve the outstanding questions.

Contact with the Westinghouse representative indicates the LASS is, as of now, a laboratory device and not a production item. Use of other devices such as the RBDT was suggested but these units will not operate at the nanosecond turn on region nor at the pulse repetition rate of 20 KHz. Periodic checks on the LASS will be made during the program to see if there is any change in the status of the device.

COMPARISON OF SWITCH DEVICES TO DATE

Present indication is that the Raytheon avalanche transistors, the AVK and possibly the AVG will be a suitable choice for the switching element. With all performance characteristics near equal, the advantages of utilizing transistors in the avalanche mode with avalanche parameter specified far outweighs the use of BJTs that may show favorable avalanche parameters today, and uncertain device parameters in the future.

Further evaluation of the VMOS FET must be performed on the device itself as well as the device implemented in a Marx configuration before the choice between the avalanche transistor and VMOS FET is finalized.

A. Switch Element Development

The individual switching devices were tested in the circuitry shown in Figure 3. Initially, with no trigger applied, V_{cc} was raised to the voltage where self sustained switching of the transistor under test (TUT) occurred, thereby determining the avalanche breakdown voltage of the device. Setting V_{cc} below the avalanche breakdown voltage by approximately 10 volts yields a stable quiescent operating point. The triggers are then applied and the di/dt or the rise time of the transistor output current is measured across a 50 ohm load.

Caution is exercised in the layout of the loop containing the TUT, discharge capacitor, and the load resistor to minimize stray circuit inductance that will effectively increase the current rise time of the device.

The test of the VMOS FETs thus far has been to determine whether the device exhibits some form of avalanche characteristics. Three out of the four types of FETs tested in the configuration shown in Figure 4 exhibited avalanching.

The avalanche voltage of the device was determined in the same manner used on the BJTs. The triggering of the device into avalanche was far more critical on the FETs than the BJTs. The current rate of rise of the FET devices ranged near the 2ns region. Additional investigation is required to determine the avalanche mechanism, the turn on problem encountered, and the possible rise time improvement with a faster trigger pulse applied to the gate.

Nothing has been done regarding the LASS device other than contacting Westinghouse. The response from the vendor indicated this switching device is a laboratory device, not ready yet for circuitry development.

B. Switch Module Development

The Marx modulator configuration shown in Figure 5 was fabricated and tested. The output voltage (V_o) of the unit was approximately one half of that specified (600V) for the unit illustrated in the proposal. The decreased voltage output is attributed to the impedance matching required between the output load and series switch arrangement. Reflections caused by a mismatch affects the rise time of the output voltage.

Operation of the Marx modulator switch was achieved with a set (U1 - U8) of 2N2219A BJTs as well as a set of Raytheon's line of avalanche transistors, the AVKs. Aside from a slight change in V_{cc} , no noticeable difference of the output was noted.

As soon as more tests are performed on the individual VMOS FET devices, they will be incorporated into the above described Marx modulator configuration.

C. Pulse Transformer Development

The preliminary requirements for the pulse transformer needed for the Task C requirement are shown in Table III.

The following types of designs have been considered:

- 1) Bifilar
 - a) Twisted Pair
 - b) Coaxial
- 2) Coaxial Line
- 3) Tapered Transmission Line
- 4) Helical Transmission Line

Initially work was begun by considering a simple 1:1 turns ratio pulse transformer. First, pulse transformers were wound using a Ferroxcube 1FI9 ferrite U core with a 0.5 inch outside diameter wound with approximately 18 inches of bifilar winding length driving a 50 ohm load. This gave a very poor rise time.

Next this was compared to the rise time degradation obtained by pulsing 30 inches of RG188U coaxial cable where a rise time of 27 nanoseconds was measured. There it was found that the coaxial cable approach gave improved performance. Tapered Transmission Line and Helical Transmission Line pulse transformers as well as the Coaxial Bifilar (also called a Balun) look promising.

An extensive literature search is still underway to determine the present state of the art. Present thoughts point to the use of a coaxial line pulse transformer using air as the dielectric. Recent literature states that faster rise times are achieved with this type of line.

D. Voltage Divider for Nanosecond Pulser Program

During this initial program period, requirements for a voltage divider test probe were generated. The following is a list of these requirements:

| | |
|-----------------------|------------------------|
| Voltage Divider Ratio | 5000:1 |
| Input | 2000 Volts, 100 K ohms |
| Output | ±1 Volt, 50 ohms |
| Rise Time | 100 picosec. |

A commercially available probe with these specifications has not been found. It was, therefore, decided to begin an in-house design of the required voltage divider probe. Conversations with probe manufacturers revealed a pessimism toward the success of our planned effort. A literature search revealed a lack of practical design information applicable to our needs. With this in mind, it became clear that a novel and yet basic approach to the probe design must be attempted; an approach which would be flexible enough to allow design changes dictated by

changing pulser circuit monitoring needs. The following is a list of design criterion with which we began our basic design:

- The circuit should be as small as practical to reduce stray and dimensional capacitance and inductance effects.
- The circuit should be assembled using microwave transmission line to ease impedance matching.
- Microwave circuit components should be used in keeping with a high frequency design approach.
- Lead length from test point to probe and ground to ground should be minimized to reduce loop inductance.
- A 50 ohm output impedance compatible with various transmission lines and test equipments, is recommended.
- Input impedance must be high enough to prevent pulser circuit loading.

With the above in mind, it was decided to build a stripline voltage divider utilizing microwave chip components on a 50 ohm line. The initial divider circuit to be investigated is shown in Figure 6.

Given; R_d

$$R_1 = R_2 = R_n$$

$$C_1 = C_2 = C_n$$

Resistor R_d is an optional overshoot damping resistor. The divider ratio is

$$\frac{\frac{C_n}{n}}{\frac{C_n}{n} + C} = \frac{R}{nR_n + R} \quad \text{The frequency compensation criterion is } R_n C_n = RC$$

Also $\frac{C_n}{n}$ must be small compared to the 30 pf pulser load requirement.

Component samples have been requested for evaluation in divider type circuits.

During the next reporting period the following is planned:

1. Investigate the characteristics of the three basic divider circuits; resistive, capacitive, and mixed, in relation to our proposed design.
2. Investigate the causes and effects of stray and residual inductance and capacitance in our divider circuit.

3. Determine optimum values for R_d , R_n , and C_n .
4. Order divider and probe components.
5. Assemble prototype probe for performance evaluation.
6. Optimize probe design and utilize in support of Nanosecond Pulser Program.

TABLE I. PROGRAM REQUIREMENTS

| | Task A | Task B | Task C |
|------------------------------------|--------|------------|--------|
| Output Voltage (kilovolts) | 1.2 | 2 | 12 |
| Peak Output Current, min (amperes) | 60 | 108 | 600 |
| Rise and Fall Times (nanoseconds) | ← | 0.5 → | |
| Load Capacity (picofarads) | ← | 30 → | |
| Pulse Width (nanoseconds) | ← | 4 to 100 → | |
| Jitter, max (nanoseconds) | ← | 0.5 → | |
| PRR | ← | 20 kHz → | |
| Isolation From Ground (kilovolts) | 11 | 15 | 25 |
| Input Voltage (volts dc) | ← | 28 → | |

TABLE II. PULSE TRANSFORMER SPECIFICATION

| | |
|---------------------------|--|
| Turns Ratio | 1:6 |
| Output | 12 Kv into 12 KΩ Shunted by 30 pf |
| Input | 2 Kv |
| Rise Time (10-90%) | 0.1 nsec |
| Fall Time (90-10%) | 0.2 nsec |
| PRR | 20 kHz |
| Pulse Width | 2, 4, 10, 20, 50, 100 nsec |

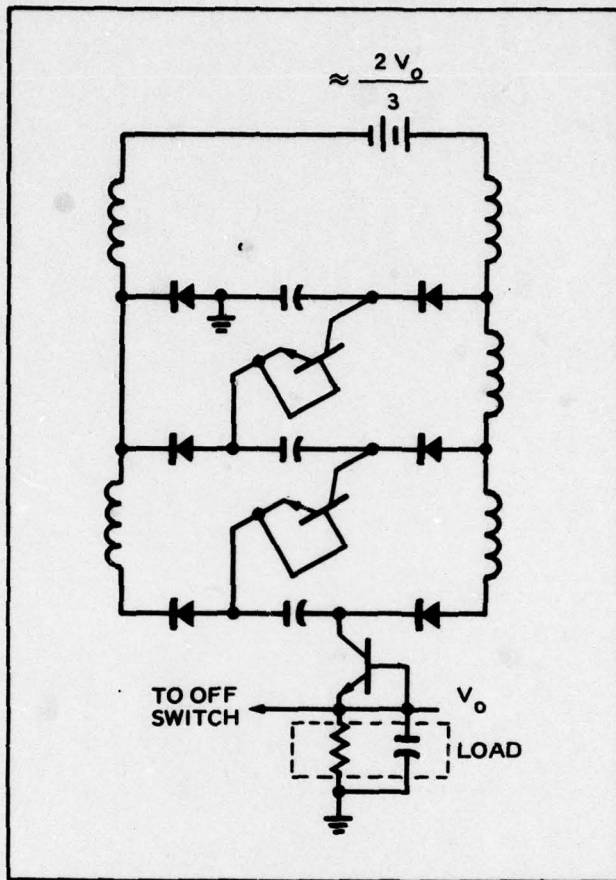


Figure 1. Marx Modulator Configuration

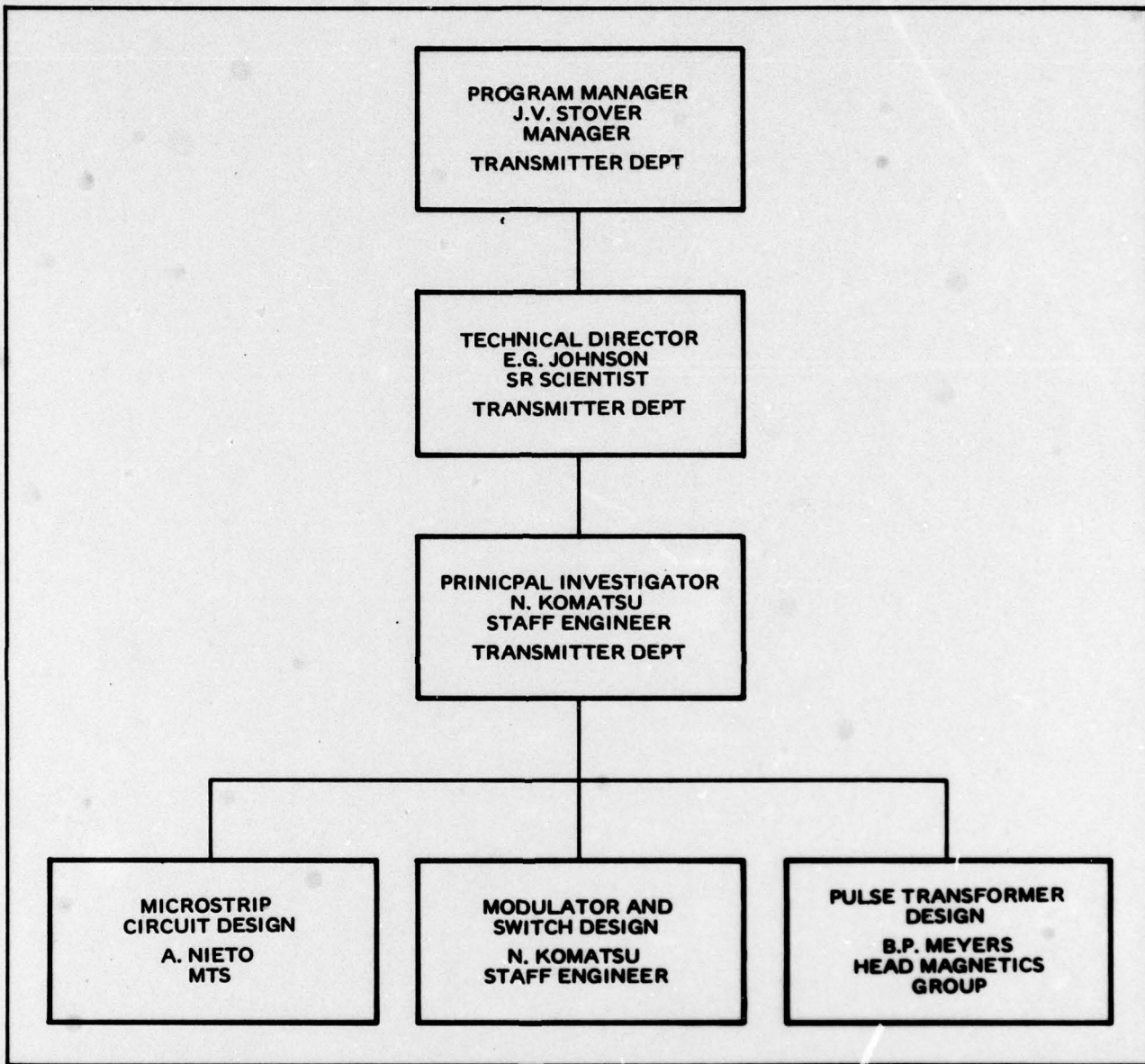
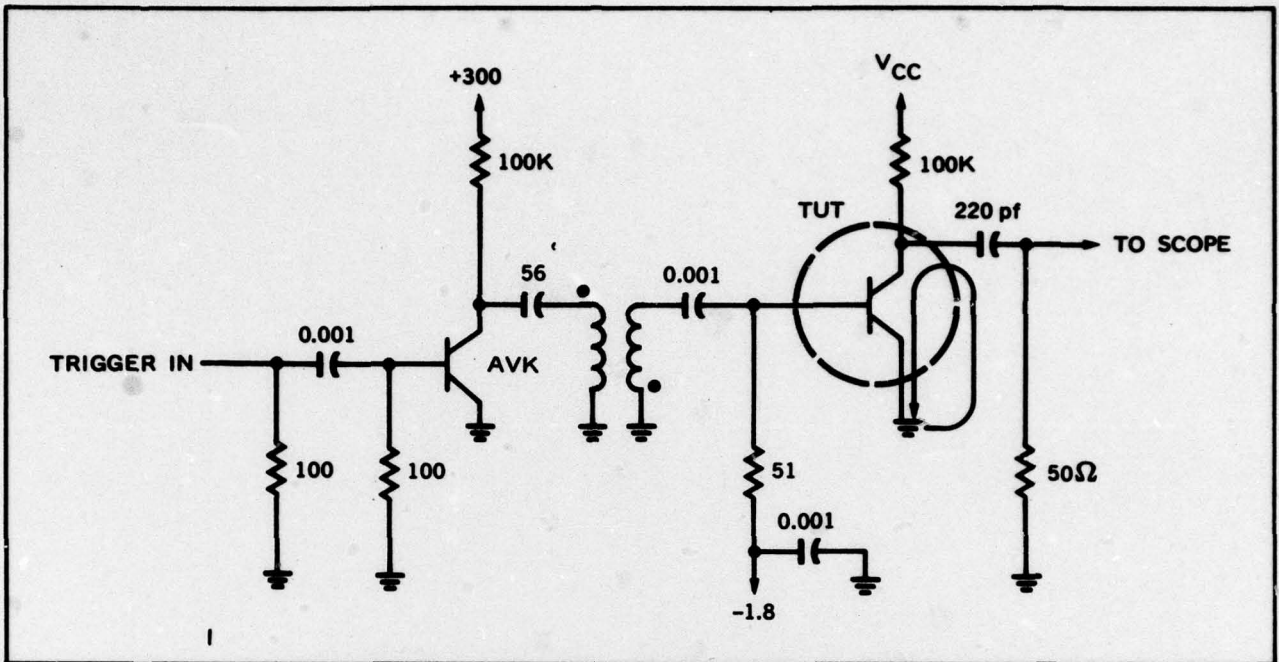
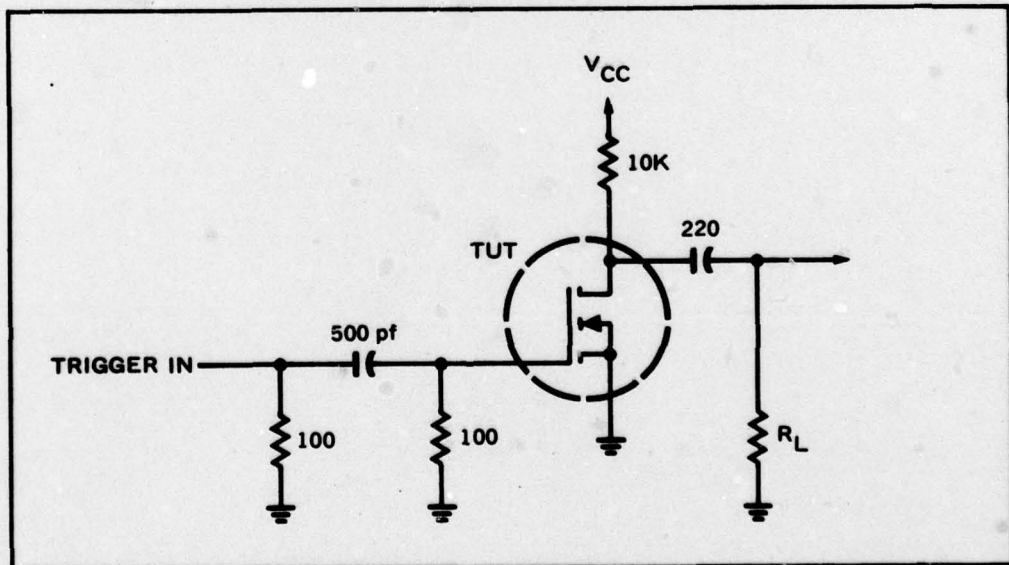


Figure 2. Organization of the Nanosecond Pulser for MM Wave Tubes Program at Hughes illustrating upper management interest in the program.



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Figure 3. Avalanche Transistor Test Setup



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Figure 4. VMOS FET Test Setup

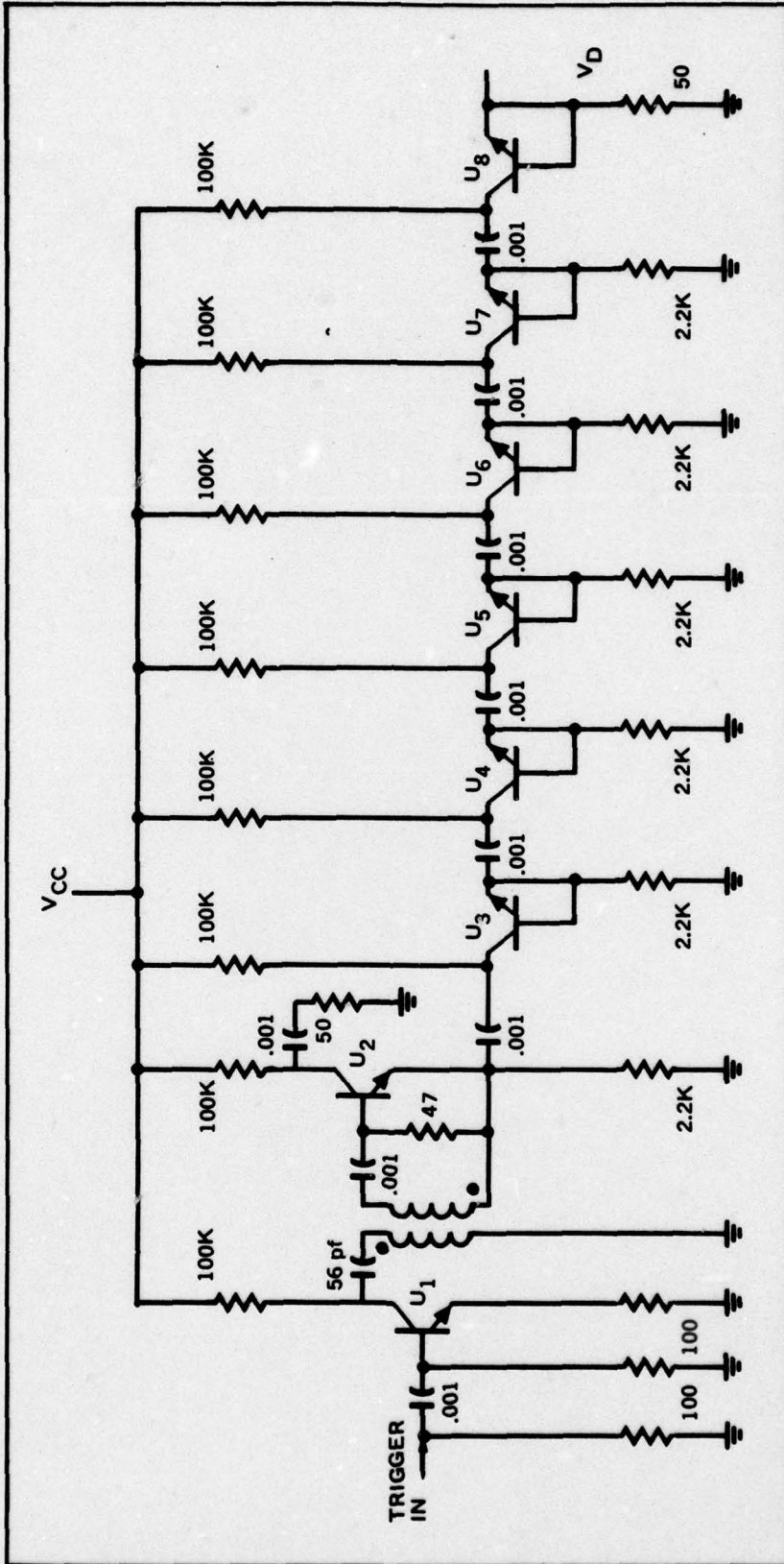
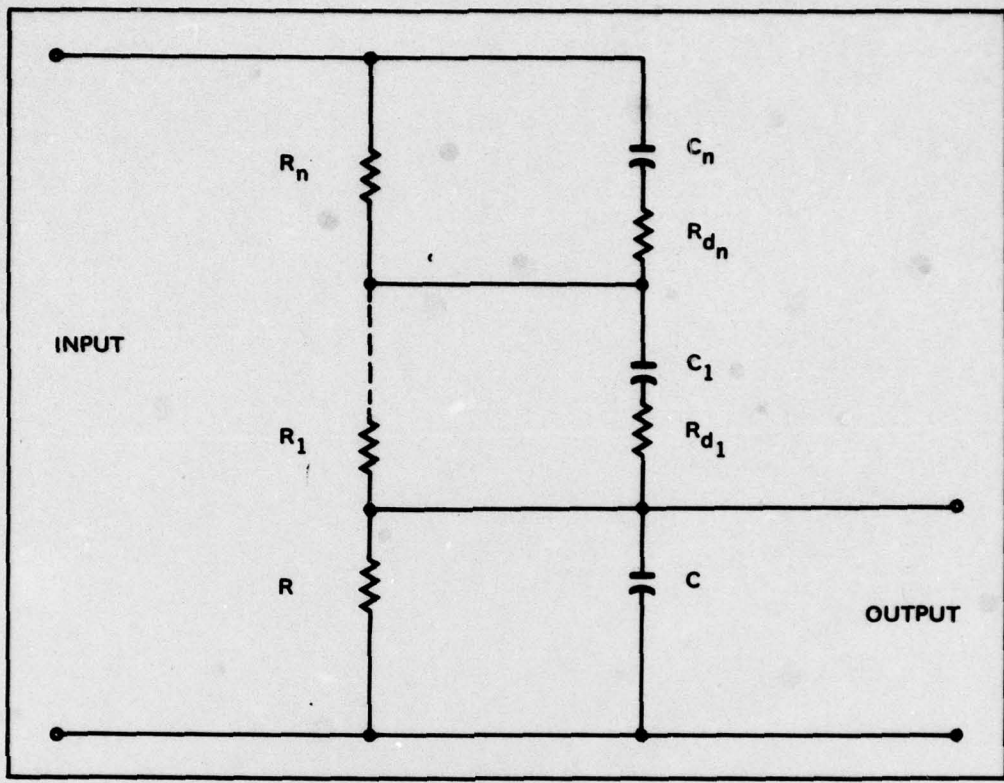


Figure 5. Marx Modulator



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Figure 6. Schematic of Voltage Divider Under Development

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