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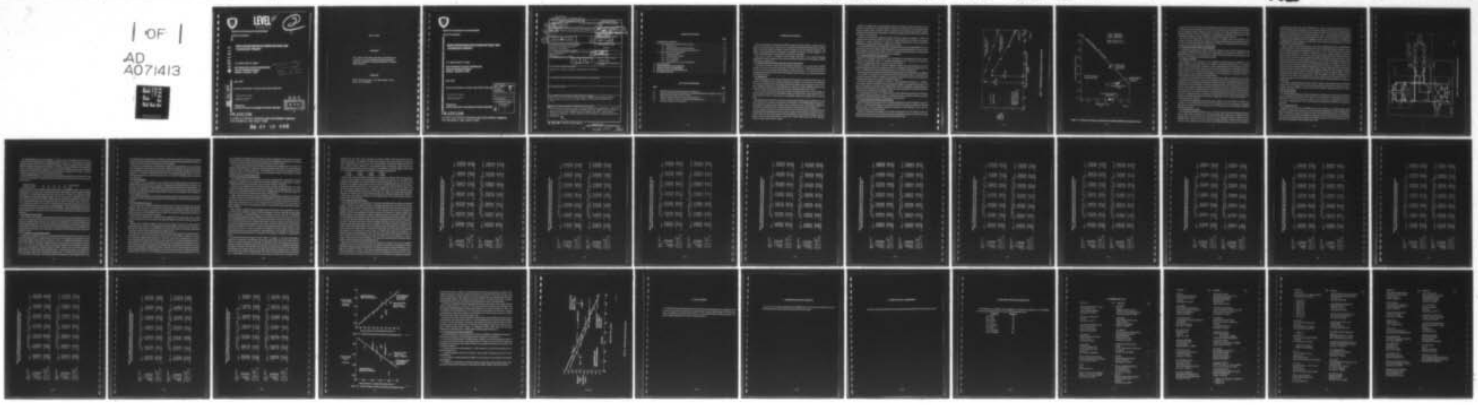

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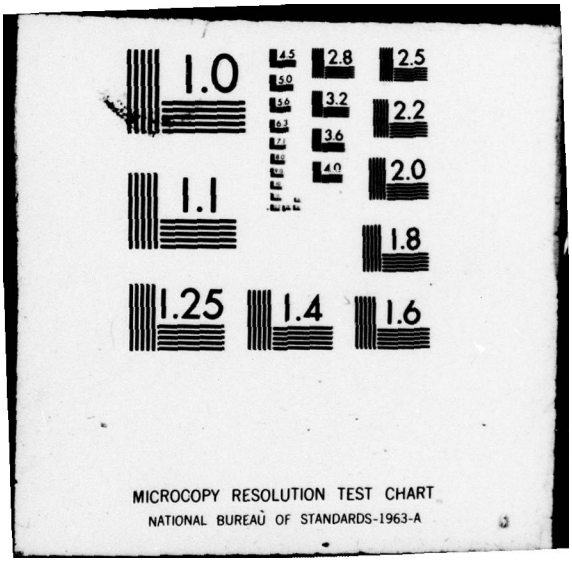
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Research and Development Technical Report

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J.E. Brewer and R.C. Lyman

WESTINGHOUSE ELECTRIC CORPORATION
Systems Development Division
Baltimore, Maryland 21203

Westinghouse Defense + Electronic Syst Center Baltimore Syst Dev. Div.

June 1979

Seventh Technical Report, for period 1 April 1978 to 31 May 1979

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A manufacturing methods project has been initiated to establish a pilot production line for metal nitride oxide semiconductor (MNOS) block oriented random access memory (BORAM) multichip hybrid circuits. This report presents an analysis of test results from an 8900 hour endurance-retention experiment.

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1. NARRATIVE AND DATA

Of all the properties associated with MNOS storage systems the subject of retention and endurance is of most concern to potential users. Retention and endurance characteristics are dependent on device fabrication procedures, transistor geometry, and cell operating conditions. The details of retention-endurance phenomena are complex, and often the system designer is confronted with conflicting and/or incomplete information on the subject.

This report provides a simplified system-oriented discussion of the retention-endurance specification concept, and then presents experimental data representative of Westinghouse MNOS BORAM two-transistor cells.

1.1 ENDURANCE-RETENTION SPECIFICATION CONCEPTS

The memory system user wants direct and definite statements as to how many times an MNOS memory can be written, and as to how long it will retain information. Unlike the device physicist, the user is not overly concerned with the details of device phenomena. Specifications which can be unambiguously interpreted, and which can be related to actual storage system operating conditions are the prime concern.

1.1.1 Background

IEEE Standard 581-1978 provides an authoritative description of retention and endurance in the context of an MNOS memory transistor. Endurance is defined as the number of write high-write low cycles accumulated before any defined unacceptable changes in device properties occur. Retention is defined as being the time period between the instant of writing an MNOS transistor into a given state and the instant when either state becomes indistinguishable from the other.

The two states of the memory transistor are referred to using various terms. The HC (high conduction) state or erased state is the threshold voltage level resulting from a write-high pulse. The LC (low conduction) state or written state is the threshold voltage level resulting from a write-low pulse.

The phenomena and concepts of transistor endurance and retention apply in a general way to the more complex case of memory cell endurance and retention. The MNOS BORAM integrated circuits employ two-transistor cells. Whenever data is written into a cell, the individual transistors in the cell may be erased and written. Changes in transistor characteristics affect cell behavior.

Data is stored in a cell by an erase-write sequence. First, both transistors are pulsed into the HC state (erased). Then depending on the data, one or the other of the transistors is pulsed into the LC state (written). The cell is constructed such that the difference in the threshold voltages of the transistors is sensed to determine whether a logic ONE or logic ZERO was stored. This difference voltage is often called the window voltage.

Because of charge decay in the individual transistors, the window decays with time. For time periods of most interest, the window closure is observed to be linear with the log of elapsed time. When the window closes to less than 100 mV, the ability of the on-chip sense amplifier to reliably distinguish ones and zeros becomes suspect. Therefore, projected closure to 100 mV can be taken as an estimate of retention time.

Erase-write cycling causes changes in window size and in decay rate. Figure 1-1 shows the changes observed in one particular cell. The slope is usually stated in volts per decade. The window magnitude is usually expressed as a voltage at a specific read-delay time. For Westinghouse BORAM data, the projected window voltage at 1 hour is used.

For a given MNOS device, the magnitude of change due to erase-write cycling depends on the applied voltage waveforms. Higher voltage amplitudes can cause rapid degradation. Transition times and pulsewidths can affect the transistors. Efforts at characterization must always be documented in the context of the specific erase-write waveforms employed.

1.1.2 Endurance-Retention Interdependence

Because of the changes which occur in the cell window with accumulated erase-write cycles, retention and endurance cannot be specified independently. For a given set of erase-write waveforms, the higher the endurance stress the lower the retention.

For the BORAM 6000 series of MNOS integrated circuits, most characterization work has centered around the use of one standard set of erase-write conditions. Devices are erased using +25 volts for 1 millisecond. Writing is accomplished using −25 volts for 0.2 millisecond.

Preliminary data for these particular operating conditions led to the development of a simplified "rule of thumb" visualization of the endurance-retention relationship. Figure 1-2 summarizes this concept by showing a region of feasible device operation. A primary motivation for the experiment described in this report was to explore the validity of figure 1-2.

The realm of interest is bounded by the line $Nt_R = 10^{12}$ cycle hours and the line $t_R = 10^6$ hours. The constant product of endurance cycles and projected retention was suggested by transistor test data (it was simply an observed trend in empirical data, and is not suggested as being fundamental in nature). The termination of the area at 10^6 hours was on the grounds that most human beings are not interested in retention times exceeding 114 years.

In a more general context, a user would be free to choose different erase and write waveforms. For different operating conditions, figure 1-2 would have to be reconsidered. Different boundary conditions should be developed for different erase-write conditions.

1.1.3 Practical Endurance-Retention Specifications

Retention and endurance specifications for different applications can be developed in the context of figure 1-2. Practical specifications must consider the realities of testing for verification. Derating from the limits of device capability should be practiced to ensure reliability, and to ease the demands on device screening procedures.

Analysis of application requirements is the proper starting point. Over the lifetime of the proposed storage system, what is the expected maximum accumulation of erase-write cycles on a single cell? What is the minimum tolerable nonvolatile data retention time?

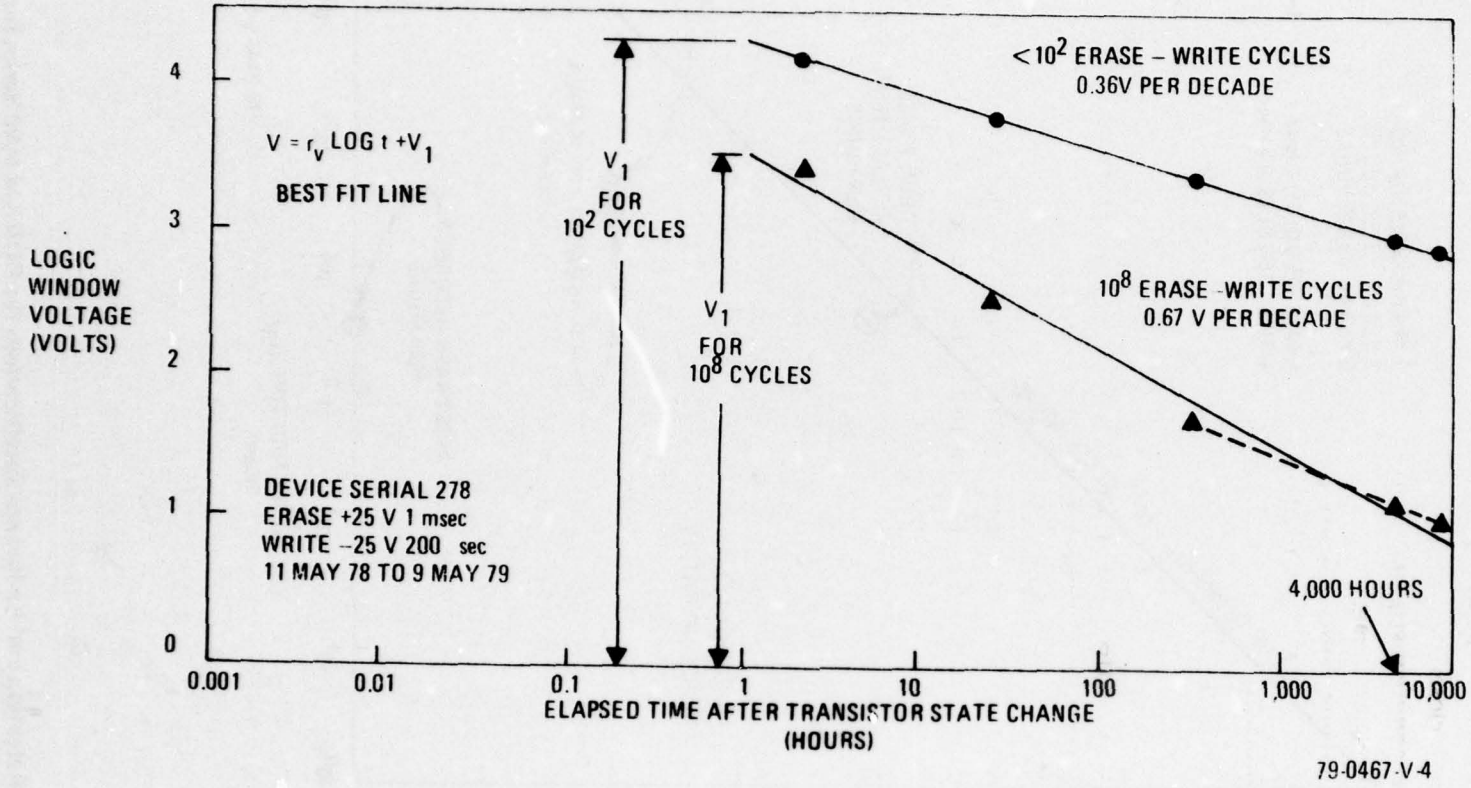


Figure 1-1. BORAM Memory Cell Window Decay Characteristic

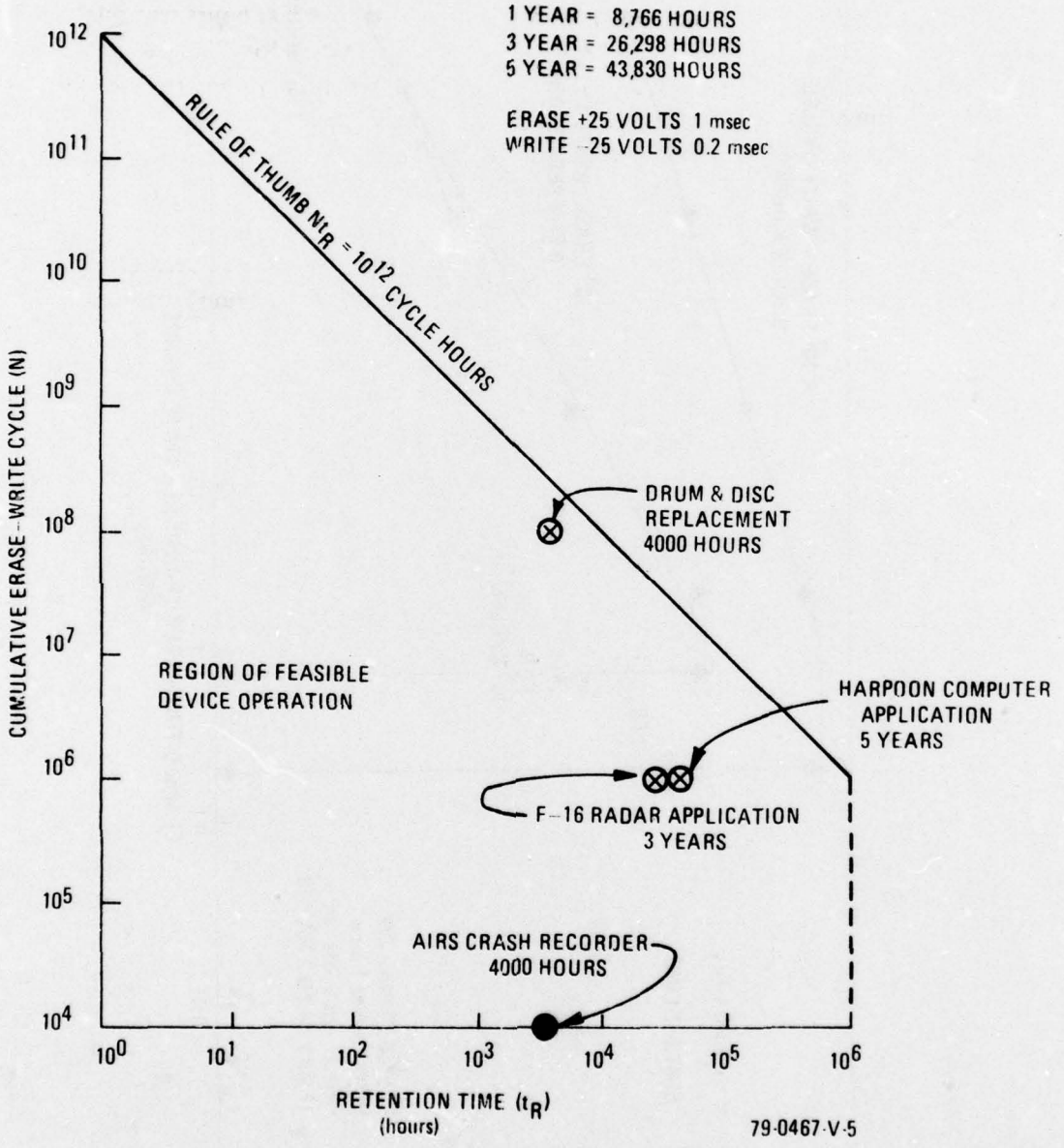


Figure 1-2. Retention and Endurance Specifications for BORAM 6000 Series Integrated Circuits

Usually one or the other factor is more important. In the case of drum and disc replacement applications, lifetime accumulations of 10^7 cycles occur frequently, and a specification of 10^8 cycles provides adequate margin. Retention times of a week or so would be adequate in most cases because data refresh is easily accomplished. A specification of 4,000 hours was selected as being compatible with figure 1-2, and providing a very confortable margin for field use.

For many other applications, the driving function is retention rather than endurance. The storage of computer programs for example is a read mostly application. Here retention times of 3 to 5 years are frequently requested. Specification of 10^6 cycles is compatible with the retention requirement, and provides generous operating margin.

1.2 ENDURANCE-RETENTION EXPERIMENT

A significant experiment on retention time after endurance stress has been conducted on the Westinghouse BORAM MNOS memory cells. Measurements of retention were collected on 512 BORAM memory cells for over 8,600 hours. Analysis of the data provides a useful guide to application of this MNOS nonvolatile memory product.

1.2.1 Objective and Plan

The objective of this experiment was to establish the endurance-retention capability of the BORAM MNOS process and memory cell design by collecting retention data on a sufficient number of cells which had been subjected to various endurance stresses. Those memory cells were to be in operating LSI memory arrays, in contrast to previous experiments on isolated single cell or single transistor test structures. Because this was a first experiment on a large number of cells, a second objective was to establish a methodology for such evaluations, to discover problems to avoid and improvements to add to future experiments.

The plan for this experiment was to subject certain memory cells in the memory array of many functional memory devices to various levels of endurance stress and to determine the retention time for those cells. The experiment is best described as three steps. First, 16 cells of the memory array in 16 MNOS parts were subjected to a range of endurance stresses. The 16 cells are one row in the memory array. Second, a pattern was written into each array. Third, the difference between the two-memory transistor threshold voltages were measured for each cell in the stressed row and for an unstressed row, at intervals of time after write which extended from 2 hours to over 8,600 hours. In all, over 4 million cell-hours of endurance-retention data has been collected and analysed. The analysis has included calculation of the window voltage decay rate for each cell and estimation of the retention time for each cell.

In the following paragraphs the memory device chosen as the test vehicle is described, the method of test is explained, and the test results are presented. These results are found to be in good agreement with previous data on retention time after endurance stress for Westinghouse BORAM MNOS memory parts.

1.2.2 The MNOS Test Vehicle

The Westinghouse BORAM MNOS process is used for several electrically alterable nonvolatile memory parts. One of these parts is a 1024-bit alterable ROM, called the 1K AROM, mask set number 6020. It was chosen as the test vehicle for this endurance-retention evaluation of the BORAM process because: (1) it has a memory transistor threshold test feature, (2) the memory transistor cell is processed in the same manner as for BORAM memory parts, and (3) the memory

cell design is the same as that used in BORAM arrays. The test circuitry incorporated in this part permits making analog measurement of the threshold voltage for each of the two memory transistors per cell in each one of the 1024 memory cells in the array. The test circuitry requires one terminal for test enable (T) and two test point terminals (+ and −) per detection circuit. The AROM 6020 has only one detection circuit, being organized 1024 by 1, so the test feature was designed into the device without significant die area or package terminal penalty. This feature is not practical in the BORAM parts because there are 32 detection circuits. The die area and terminal or wire bonding penalties would be prohibitive.

Figure 1-3 shows the memory threshold test circuitry in a simplified schematic of the 6020 device. In normal operation, the test enable terminal (T) is LOW, connecting the memory transistor source lines to the detection latch and decoupling the test points (+ and −) from those source lines. When the test enable terminal (T) is HIGH, to enable this memory transistor threshold voltage test feature, the source lines are connected to the test points and decoupled from the detection latch. Other circuitry omitted for clarity simulates the loading of the detector on the source lines. In this mode, the test points are first precharged to VCC (+15V). Then the selected pair of memory transistors operate in source follower mode to discharge each test point to a voltage level which is the memory transistor threshold voltage above ground (the gate voltage of the selected memory transistor pair). On the Macrodata MD-501 automatic tester, after a delay sufficient for each source follower waveform to reach steady-state, a high impedance voltage sense circuit samples the voltage at each test point. Each sample is converted to digital form. The two digital voltage values are substracted and outputted on the line printer. The tester deselects the part by dropping the CS waveform LOW, thereby precharging the test points, decoders and other internal circuitry, increments the address to the next memory cell, selects the part by raising CS HIGH, and repeats the measurement.

This circuitry for determining the memory window voltage has been designed into several MNOS memory parts at Westinghouse. It has been used successfully on all these parts to measure memory transistor threshold voltages, thereby to determine the window voltage and decay rate and to estimate retention time.

1.2.3 The Test Method

The methods and procedures used in this experiment on retention and on the effects of endurance stress on retention are described in three parts. First is the method of subjecting the parts to endurance stress with some comments on selection of parts. Second is writing each part with the "zero time" retention pattern. Third is the method of measuring the thresholds of the memory transistor.

1.2.3.1 Endurance Stress

Endurance stress testing for these MNOS parts involves erasing a set of memory cells, writing each cell to a certain state, erasing the set of cells again and writing each cell to the complementary state. By repetition of these two erase-write cycles, the desired endurance stress is accumulated. These two erase-write cycles have caused each transistor in each of the memory cells to have had two reversals of threshold level. Therefore, the number of erase-write cycles is the number of reversals. These are generally termed endurance stress cycles.

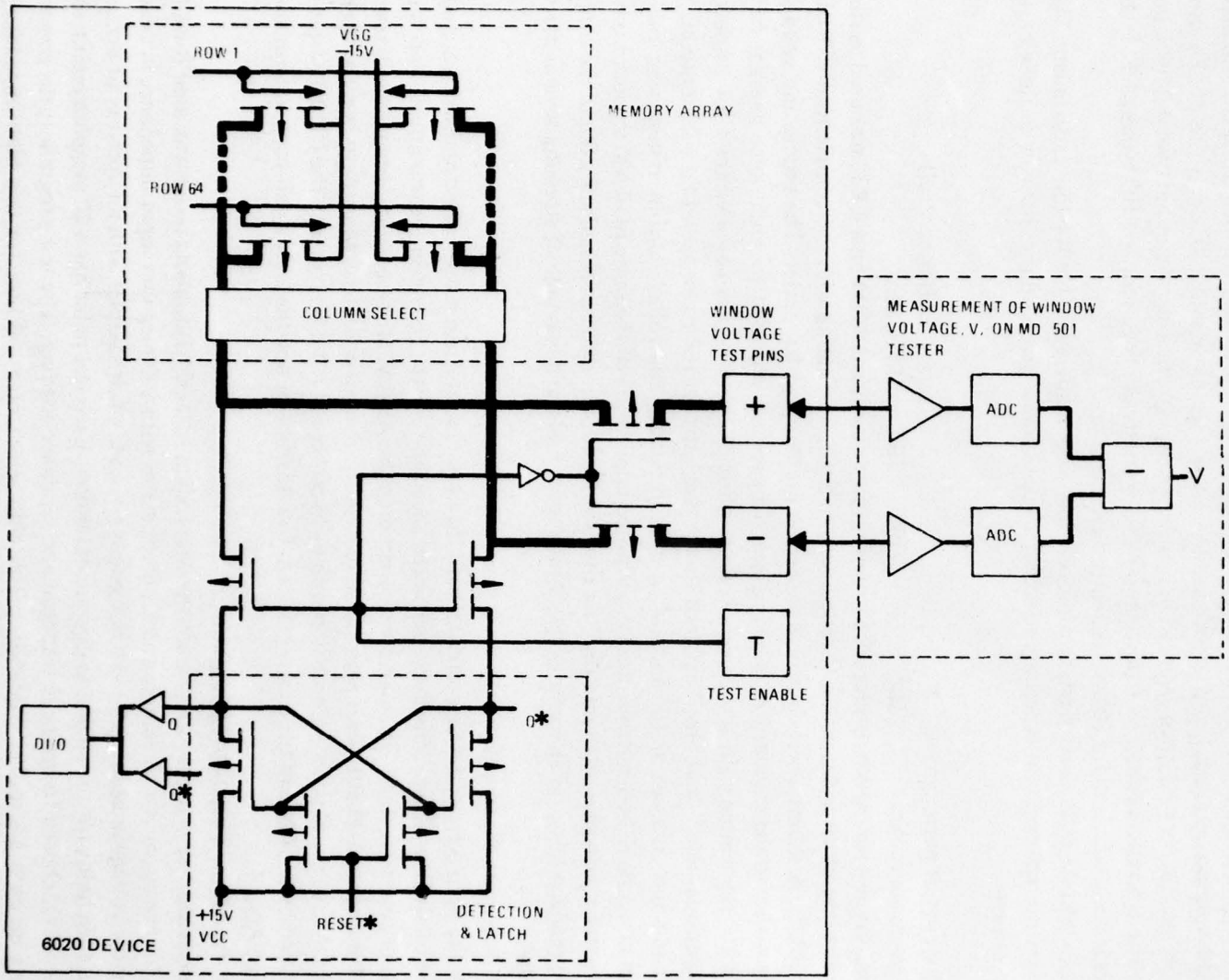


Figure 1-3. 6020 Cell Window Measurement Circuitry

The AROM 6020 has row erase capability, so that one row of 16 memory cells can be cycle-stressed with the remaining 63 rows remaining unstressed. The first row was chosen for cycle stress and the second row was used as an unstressed control row. Parts were stressed using the standard BORAM voltages and erase and write times of 1,000 μsec erase and 200 μsec write pulsewidth. That row was first erased, then each cell in turn was written, requiring somewhat over 4.2 msec per erase-write (16 cells) cycle. For 10^4cycles, only 42 seconds are required; for 10^6 cycles, 1 hour 10 minutes is necessary, and for 10^8 cycles nearly 5 days elapse.

Sixteen AROM 6020 parts from two process lots were made available for this experiment. The parts were not screened nor especially selected. The endurance stress on the first row of these parts was as follows:

Quantity of parts:	2	2	4	3	3	2 (for control)
Endurance cycles:	10^4	10^5	10^6	10^7	10^8	zero

A laboratory test set, which displays the stored bit pattern of an AROM on a CRT, was used to run repetitive erase-write cycles with a checkerboard pattern, alternating with the complement (CKBD and CKBD*). A thumbwheel control was used to preset up to 10^5 cycles. The timing and voltage was adjustable to the standard BORAM values. This test set was used for endurance stress at 10^4, 10^5 and 10^6 (by running 10^5 ten times). Because internal circuitry was designed for CRT display, there is considerable "dead time" between stress cycles, so that 10^5 cycles took 1 hour 23 minutes.

For endurance stresses of 10^7 and 10^8, a microprocessor-controlled burn-in system was used. Programming the KIM-1 microprocessor permitted application of the same BORAM standard timing. The stress pattern written into the first row was 1001100... (9999 in hexadecimal) and the complement (6666 in hex), on alternate cycles. This system had the advantage of stressing several parts in parallel.

1.2.3.2 Retention Pattern Write

After the parts were endurance stressed with the cycles desired, each was erased and written, and the time of writing noted. This is the zero reference time for the retention measurements and for analysis of retention slope. The parts were written in the AROM lab test set and immediately read on the Macrodata MD-501. Two patterns were used for the retention test. Most parts were written with all ONEs; several parts were written with a checkerboard (CKBD) pattern. The CKBD pattern is generated by the AND of the least significant row address bit and the least significant column address bit: A0-A4.

1.2.3.3 Transistor Threshold Measurement

An electrical test program written for the Macrodata MD-501 automatic tester was used for all threshold measurements. A sample and hold voltmeter with 100 megohm input impedance is used to sense the voltage at each of the two test points (+ and −). It samples with an aperture of about 30 nsec, then holds for the analog to digital conversion. Each test point has a 20 megohm pullup to VCC (+15V), chosen to optimize response and minimize loading. The test program turns power ON, sets up each address in sequence, pulses chip select, waits 50 μsec for this high impedance measurement to stabilize, then takes the sample at the (+) terminal and converts. The progam next pulses chip select, waits 50 μsec and takes the sample at the (−) terminal). Then the program sets up the next address and repeats, continuing through all 1024 addresses. Under program control, the

two measurements at each address are subtracted, while the next address is setting up, and the absolute value of the difference is printed. Test procedure includes incorporating the serial number of the part, and the date and time of reading with the test printout.

The parts were separated into three groups according to when endurance stress was complete. The write and first several reads were on 3, 8 and 11 May 1978. Readings were reported at one third to one decade intervals of time, each carefully recorded. The most recent readings were of all parts together, on 11 November 1978 and on 9 May 1979. These readings spanned a year, on 16 parts, with 16 stressed memory cells and 16 unstressed cells, for a total of 4.49 million memory cell-hours of retention data.

1.2.4 The Test Results

The purpose of this experiment was to determine the endurance-retention performance of BORAM processed memory cells as a guide to the application of BORAM memory systems. The purpose of this analysis of the data obtained is to establish the appropriate limits of application. As an example of considerations involved in evaluating the data, a careful study revealed that several parts had atypically good retention characteristics. These were not included in any averaging to establish application limits.

In the following paragraphs the method of processing the data is first described. Results of data evaluation for each part separately are presented. Then the analysis of data for all parts collectively is shown.

1.2.4.1 Initial Data Processing

The printout from the Macrodata MD-501 automatic tester is a set of 16 values per row for each 6020 part, taken at each time of measurement. The values are differences between the threshold voltages of the two memory transistors in a cell, indicative of the memory window. Several rows were printed each time, including the first row which was endurance stressed and the second row which was unstressed, and served as a control.

Some parts were measured at 11 different times, ranging from 30 seconds after write to 8,904 hours (371 days) after write. Other parts were measured eight or ten times covering the same span of time.

Because there is generally a change of decay rate in the vicinity of an hour, the measurements made earlier than 2 hours were not included in the data analysis. From the five to seven sets of printouts for times between 2 and 8,904 hours, five sets were chosen for each part, eliminating some data where the tester or printer was clearly malfunctioning.

The data from the Macrodata MD-501 automatic tester printout and the accompanying accumulated hours since the part was written were entered into an HP9825A computer for tabulation, evaluation, analysis and summary. For each part at each time of measurement, a set of 16 values represented the cells of the stressed row, and a second set of 16 values represented the cells of an unstressed row. This data taken at five different times was assembled by the computer into two 16 by 5 matrices of values. The computer was programmed to compute a least squares fit to a linear equation of the difference voltages as a function of log time for the five data values per cell. Results of this calculation include the slope (decay rate in mV per decade of time), the intercept (window voltage in mV at 1 hour, i.e., zero on the log time axis) and the correlation coefficient of fit to the

line. In addition, an estimate of retention time was made using 100 mV as the minimum voltage difference which can be reliably read by the detection circuit in BORAM memory parts. This estimate is simply a calculation of the time at which the straight line fit reaches 100 mV.

The computer stored all this data and results of calculations on magnetic tape for reference. It printed a working data sheet for each part, showing all measurement values in a matrix format and listing the results of the least squares fit. Also calculated were the mean and standard deviation (sigma) for each row of 16 cells for each time of measurement. Finally, a least squares fit to these average values was computed and printed.

1.2.4.2 Study of Data on Individual Parts

The 16 samples used for this experiment were chosen randomly from a previously unscreened population. Availability of the computer data summary provided the first opportunity to examine the detail characteristics of each sample, and to view the consistency of the data.

Three parts were dropped from the sample because of grossly atypical characteristics which would have caused rejection during normal device screening. The irregularities were small initial windows which differed significantly from that for neighboring cells. The BORAM margin test conducted at reduced write voltage eliminates devices of this nature.

Another observation based upon study of individual cell performance on all parts is that the last two cells in the first row have generally larger voltage differences than all other cells. Specifically, the 16th cell ranks first for 10 of 14 parts. In those parts, the value for the 16th cell is about 3 sigmas above the mean for the row. The value for the 15th cell ranks first for 7 of 14 parts, by about 2 sigmas. As a result, the estimates of retention time for these cells are significantly longer, by 2 to 5 decades.

There are layout considerations which indicate that the end memory cells, especially in the first row of the array, could have superior retention performance. Another significant finding gained from measurement of voltage differences on the AROM lab test set was that the Macrodata MD-501 had omitted printout of the reading for cell 0, the first memory cell of the array. Thus the first 16 readings printed by the MD are for memory cell numbers 1 through 15 of the first row, and for the first cell of the second row. Because the second row was not stressed, this finding accounts for the 16th reading having a significantly larger value. Clearly, the 16th printout value should be excluded from analysis of stressed cells. Also, for the reasons earlier noted, the 15th printout value which is the last cell in the first row, should be excluded from further analysis directed toward determining an endurance-retention limit for system applications. Accordingly, the analysis which follows was based upon memory cells 1 through 14 of the stressed row on each part, omitting cells 0 and 15.

The data for each of these 13 parts is shown in tables 1-1 through 1-13. The title for each table includes the serial number of the 6020 part and the date when the part was written, hence when the retention test started. Also given is the number of endurance cycles. For the one part that was not endurance stressed, 100 endurance cycles were assumed, to account for the regular and experimental testing of such parts. The 100 clear-write cycles are shown in the title as 1E2. Each table shows the differential cell voltages measured on the Macrodata MD-501 automatic tester, in millivolts, for each cell at each of the five times measured. The results of the least squares fit for a linear equation in voltage difference as a function of log time are given for each cell. The measure of fit is

shown by the "corr. coef." entry, the majority of which are 0.999 or 1.000. The slope of the line is decay rate, given by "mV/decade." The intercept of the line is the window voltage at 1 hour (where log t = 0), shown by the "mV at 1 hour" entry. The estimate of retention time is denoted "hours to 0.1V" because 100 mV sensitivity is the appropriate limit of detection. These estimates are presented in exponential powers of ten notation, e.g., 4,000 hours is printed 4.00E03. A few values for 1 through 10 years are given here for reference and ease of interpretation:

1 year	2 years	5 years	10 years
8.77E03	1.75E04	4.38E04	8.77E04

Data for the 14 unstressed cells of each part was studied but not plotted. The same calculations of fit to a linear voltage vs log time relationship were made with good success. Virtually all the coeficients of correlation were 1.00. The mean of window voltage decay rate, r_V, was between 341 and 407 mV per decade, with exception of one at 158. The overall mean for all parts was 354 mV per decade. Standard deviation of r_V for each part was between 3 and 18 mV per decade. The means of window voltage at one hour, V_1, ranged from 3848 to 4451 mV, with an exception at 2145 mV. The standard deviations were between 14 and 217 mV. These are all rather tightly grouped. Estimates of retention time for these unstressed (under 100 cycles) parts ranged from 1.05E10 to 1.05E13 hours, the shortest of which is over one million years. In all, the unstressed parts performance was fairly consistent.

1.2.4.3 Analysis of Data on All Parts

A working summary of the computations for each part was developed by an additional computer program. The parts were ranked in order of increasing endurance stress and listed with the key parameters for study, plotting and evaluation. This effort was directed toward presentation of the endurance-retention data in a manner which is both informative and useful for applications guidance. The first two parameters of interest were those of the linear fit of window voltage to log time for each part. These parameters, window voltage decay rate (r_V) and window voltage at 1 hour (V_1) were plotted vs the endurance stress in erase-write cycles (N), and are shown in figures 1-4 and 1-5. The mean values are plotted as small circles with one standard deviation shown by a range bar. The data is reasonably consistent in that the standard deviations are less than 7 percent of the respective means, generally around 4 percent. In figure 1-4, two parts stressed at 10^6 cycles and two at 10^7 are seen to have smaller decay rates (r_V) than other parts of the same stress. In figure 1-5, the same four parts have larger windows at one hour (V_1) than other parts of the same stress, although the separation is less apparent here than in figure 1-4. Because the purpose of the analysis is to develop a guide to system applications, these four parts with superior decay characteristics are set aside. Using the data for the remaining nine parts, least squares fits were computed for r_V and V_1 vs log N. These are shown in the same figures. They provide a good indication of the decay rate and window size to be expected from the BORAM process.

The summary of data for all parts included the estimates of retention time (t_R). The standard deviation of t_R over the 14 cells of each part was computed. But because one standard deviation each side of the mean includes only 68 percent of all parts, assuming a normal distribution, a wider range was computed. A factor of 1.96 times the standard deviation was chosen, to include 95 percent of the population. Actually, because parts with t_R on the high side of the mean are of no concern, attention should be focused on the low side. About 97.5 percent of the population should lie

Table 1-1. Retention Characteristic for 14 Cells From Part 6020 Serial 131
(Retention Test Started 8 May 1978 After 1E7 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
19.92	3280	2980	3045	3200	3270	2965	3095
212.50	2830	2520	2615	2690	2805	2520	2685
428.50	2680	2390	2510	2535	2665	2360	2560
4947.00	2205	1970	2105	2025	2175	1945	2150
8781.00	2155	1900	2040	1970	2115	1870	2080
corr. coef.	0.999	0.999	0.999	0.999	0.999	0.999	1.000
mV/decade	-434	-409	-381	-473	-444	-416	-387
mV at 1 hour	3837	3490	3522	3798	3841	3489	3589
hours to .1V	4.03E08	1.91E08	9.51E08	6.65E07	2.64E08	1.39E08	1.05E09

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 8	CELL 9	CELL10	CELL11	CELL12	CELL13	CELL14
19.92	3205	3305	2960	3090	3200	3285	2935
212.50	2695	2835	2500	2680	2680	2815	2490
428.50	2535	2690	2365	2545	2520	2670	2330
4947.00	2025	2195	1935	2140	2010	2180	1915
8781.00	1940	2110	1870	2060	1910	2090	1840
corr. coef.	1.000	1.000	0.999	1.000	1.000	1.000	0.999
mV/decade	-482	-456	-415	-391	-489	-455	-416
mV at 1 hour	3821	3896	3479	3590	3824	3874	3459
hours to .1V	5.17E07	2.07E08	1.40E08	8.37E08	4.07E07	1.93E08	1.18E08

Table 1-2. Retention Characteristic for 14 Cells From Part 6020 Serial 134 (Retention Test Started 11 May 1978 After 7E5 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
24.40	2770	2750	2745	2745	2750	2715	2795
144.50	2345	2300	2300	2315	2340	2305	2350
360.80	2130	2100	2105	2090	2125	2090	2145
4875.00	1570	1550	1540	1540	1555	1520	1570
8713.00	1475	1470	1450	1460	1460	1445	1485
corr. coef.	0.999	0.998	0.999	0.998	1.000	0.999	0.999
mV/decade	-508	-500	-506	-505	-508	-503	-514
mV at 1 hour	3453	3408	3419	3417	3442	3396	3481
hours to .1V	4.00E06	4.09E06	3.58E06	3.70E06	3.77E06	3.59E06	3.78E06

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 8	CELL 9	CELL10	CELL11	CELL12	CELL13	CELL14
24.40	2740	2765	2770	2770	2735	2765	2750
144.50	2310	2345	2345	2340	2310	2340	2654
360.80	2090	2120	2120	2120	2095	2120	2100
4875.00	1535	1555	1560	1545	1535	1550	1540
8713.00	1435	1460	1475	1460	1450	1455	1455
corr. coef.	0.999	0.999	0.999	0.999	0.999	0.999	0.974
mV/decade	-511	-513	-510	-516	-505	-515	-552
mV at 1 hour	3424	3458	3454	3464	3413	3460	3616
hours to .1V	3.25E06	3.51E06	3.81E06	3.31E06	3.60E06	3.37E06	2.34E06

Table 1-3. Retention Characteristic for 14 Cells From Part 6020 Serial 148 (Retention Test Started 3 May 1978 After 1E2 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
7.66	3540	3375	3505	3495	3570	3520	3580
75.00	3200	3030	3165	3150	3220	3170	3235
551.60	2865	2705	2835	2810	2885	2835	2905
5057.00	2870	2370	2505	2475	2545	2490	2565
8904.00	2480	2305	2440	2405	2475	2425	2495
corr. coef.	0.949	1.000	1.000	1.000	1.000	1.000	1.000
mV/decade	-296	-353	-352	-360	-361	-362	-358
mV at 1 hour	3771	3686	3815	3813	3889	3840	3897
hours to .1V	2.41E12	1.44E10	3.66E10	2.10E10	3.13E10	2.17E10	4.12E10

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 8	CELL 9	CELL10	CELL11	CELL12	CELL13	CELL14
7.66	3525	3570	3535	3615	3590	3620	3580
75.00	3180	3215	3175	3265	3250	3270	3230
551.60	2840	2880	2840	2935	2910	2935	2895
5057.00	2495	2540	2500	2590	2565	2595	2550
8904.00	2430	2470	2425	2525	2495	2530	2485
corr. coef.	1.000	1.000	1.000	1.000	1.000	1.000	1.000
mV/decade	-362	-362	-365	-360	-362	-360	-362
mV at 1 hour	3847	3888	3854	3933	3914	3937	3900
hours to .1V	2.19E10	2.86E10	1.98E10	4.47E10	3.44E10	4.57E10	3.18E10

Table 1-4. Retention Characteristic for 14 Cells From Part 6020 Serial 151
(Retention Test Started 8 May 1978 After 1E6 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
19.92	3445	3285	3280	3465	3480	3335	3330
212.50	3060	2895	2895	3075	3085	2946	2935
428.50	2940	2780	2775	2950	2960	2825	2815
4947.00	2535	2380	2375	2545	2540	2430	2415
8781.00	2445	2300	2290	2455	2450	2350	2335
corr. coef.	1.000	1.000	1.000	1.000	1.000	1.000	1.000
mV/decade	-379	-374	-376	-383	-391	-374	-378
mV at 1 hour	3939	3768	3768	3963	3991	3817	3816
hours to .1V	1.32E10	6.37E09	5.73E09	1.21E10	8.71E09	8.64E09	6.86E09

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts						
	CELL 8	CELL 9	CELL10	CELL11	CELL12	CELL13	CELL14
19.92	3475	3475	3340	3355	3505	3460	3370
212.50	3085	3080	2950	2965	3115	3070	2971
428.50	2955	2960	2835	2840	2975	2945	2845
4947.00	2545	2540	2430	2450	2555	2525	2445
8781.00	2455	2450	2345	2365	2465	2440	2360
corr. coef.	1.000	1.000	1.000	1.000	1.000	1.000	1.000
mV/decade	-387	-389	-378	-375	-396	-389	-383
mV at 1 hour	3980	3983	3829	3837	4024	3968	3862
hours to .1V	1.03E10	9.41E09	7.53E09	9.23E09	8.05E09	9.00E09	6.71E09

Table 1-5. Retention Characteristic for 14 Cells From Part 6020 Serial 152
(Retention Test Started 8 May 1978 After 1E6 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
19.92	3425	3340	3375	3415	3430	3345	3385
212.50	3030	2965	2990	3010	3035	2961	3000
428.50	2905	2850	2870	2890	2910	2840	2880
4947.00	2500	2465	2490	2465	2490	2450	2480
8781.00	2410	2395	2405	2390	2410	2380	2400
corr. coef.	1.000	1.000	1.000	1.000	1.000	1.000	1.000
mV/decade	-385	-360	-367	-391	-389	-368	-375
mV at 1 hour	3923	3803	3845	3921	3936	3817	3870
hours to .1V	8.68E09	1.94E10	1.62E10	5.91E09	7.30E09	1.29E10	1.16E10

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 8	CELL 9	CELL10	CELL11	CELL12	CELL13	CELL14
19.92	3420	3420	3350	3370	3440	3420	3385
212.50	3015	3020	2970	3000	3030	3015	3000
428.50	2885	2895	2850	2875	2905	2885	2880
4947.00	2470	2470	2460	2495	2475	2460	2485
8781.00	2390	2390	2380	2410	2390	2380	2415
corr. coef.	1.000	1.000	1.000	1.000	1.000	1.000	1.000
mV/decade	-392	-393	-368	-364	-399	-396	-370
mV at 1 hour	3925	3931	3826	3842	3958	3934	3861
hours to .1V	5.75E09	5.66E09	1.30E10	1.89E10	4.55E09	4.68E09	1.48E10

Table 1-6. Retention Characteristic for 14 Cells From Part 6020 Serial 153 (Retention Test Started 8 May 1978 After 1E7 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
19.92	3500	3100	3205	3400	3500	3120	3230
212.50	3060	2430	2565	2915	3050	2667	2790
428.50	2915	2495	2630	2765	2910	2510	2660
4947.00	2445	2060	2200	2280	2435	2080	2230
8781.00	2335	1975	2105	2190	2330	1995	2145
corr. coef.	1.000	0.976	0.979	1.000	1.000	0.999	1.000
mV/decade	-442	-406	-396	-460	-444	-427	-411
mV at 1 hour	4079	3539	3642	3989	4079	3661	3754
hours to .1V	1.01E09	3.02E08	8.70E08	2.83E08	9.16E08	2.20E08	7.68E08

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 8	CELL 9	CELL10	CELL11	CELL12	CELL13	CELL14
19.92	3420	3525	3105	3215	3425	3510	3120
212.50	2930	3070	2645	2755	2940	3060	2666
428.50	2780	2925	2510	2640	2790	2925	2510
4947.00	2300	2445	2070	2210	2305	2450	2075
8781.00	2210	2345	1995	2120	2215	2350	1990
corr. coef.	1.000	1.000	0.999	0.999	1.000	1.000	0.999
mV/decade	-459	-449	-422	-413	-460	-441	-429
mV at 1 hour	4005	4109	3637	3735	4014	4084	3664
hours to .1V	3.15E08	8.61E08	2.44E08	6.44E08	3.21E08	1.10E09	2.04E08

Table 1-7. Retention Characteristic for 14 Cells From Part 6020 Serial 156 (Retention Test Started 3 May 1978 After 1E4 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
7.66	3705	3370	3710	3380	3730	3390	3765
75.00	3360	2965	3365	2980	3380	2980	3410
551.60	2985	2555	2990	2565	3000	2565	3030
5057.00	2560	2120	2570	2125	2575	2130	2605
8904.00	2485	2025	2480	2035	2490	2040	2520
corr. coef.	0.999	1.000	0.999	1.000	0.999	1.000	0.999
mV/decade	-407	-444	-408	-446	-412	-447	-414
mV at 1 hour	4090	3776	4097	3790	4120	3796	4155
hours to .1V	6.32E09	1.88E08	6.16E09	1.90E08	5.59E09	1.89E08	6.30E09

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 8	CELL 9	CELL10	CELL11	CELL12	CELL13	CELL14
7.66	3385	3765	3385	3760	3420	3745	3400
75.00	2980	3415	2980	3410	3010	3385	2985
551.60	2570	3020	2570	3020	2595	3000	2570
5057.00	2125	2600	2145	2595	2155	2580	2135
8904.00	2030	2510	2050	2510	2060	2495	2050
corr. coef.	1.000	0.999	1.000	0.999	1.000	0.999	1.000
mV/decade	-448	-417	-441	-416	-449	-415	-447
mV at 1 hour	3797	4160	3785	4154	3830	4133	3804
hours to .1V	1.78E08	5.35E09	2.31E08	5.49E09	2.00E08	5.18E09	1.94E08

Table 1-8. Retention Characteristic for 14 Cells From Part 6020 Serial 267
(Retention Test Started 11 May 1978 After 1E8 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
2.00	2585	2640	2560	2535	2625	2630	2550
144.50	1315	1405	1290	1065	1405	1410	1085
360.80	1065	1165	1065	1040	1165	1165	1060
4875.00	560	655	590	570	660	660	575
8713.00	400	625	540	570	640	645	515
corr. coef.	0.995	0.991	0.989	0.969	0.991	0.991	0.975
mV/decade	-593	-561	-558	-539	-553	-554	-552
mV at 1 hour	2685	2716	2620	2520	2699	2703	2554
hours to .1V	2.28E04	4.64E04	3.29E04	3.07E04	4.97E04	5.00E04	2.77E04

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 8	CELL 9	CELL10	CELL11	CELL12	CELL13	CELL14
2.00	2535	2565	2590	2580	2590	2600	2970
144.50	1060	1135	1165	1115	1120	1170	1530
360.80	1035	1105	1130	1080	1095	1135	1485
4875.00	540	625	655	605	620	650	950
8713.00	465	590	625	540	595	610	915
corr. coef.	0.977	0.975	0.975	0.975	0.972	0.976	0.980
mV/decade	-561	-539	-537	-553	-545	-543	-563
mV at 1 hour	2545	2567	2591	2583	2582	2606	2994
hours to .1V	2.30E04	3.78E04	4.36E04	3.08E04	3.59E04	4.13E04	1.38E05

Table 1-9. Retention Characteristic for 14 Cells From Part 6020 Serial 269
(Retention Test Started 3 May 1978 After 1E4 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
7.66	3680	3390	3645	3330	3585	3305	3580
75.00	3305	2985	3250	2925	3200	2900	3190
551.60	2905	2585	2865	2530	2800	2510	2780
5057.00	2485	2175	2440	2135	2365	2120	2345
8904.00	2395	2095	2350	2050	2280	2035	2260
corr. coef.	0.999	1.000	1.000	1.000	0.999	1.000	0.999
mV/decade	-426	-428	-427	-422	-433	-418	-438
mV at 1 hour	4075	3773	4034	3704	3985	3674	3984
hours to .1V	2.14E09	3.76E08	1.61E09	3.49E08	9.35E08	3.53E08	7.28E08

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 8	CELL 9	CELL10	CELL11	CELL12	CELL13	CELL14
7.66	3310	3570	3310	3575	3355	3615	3400
75.00	2890	3180	2890	3180	2935	3230	2990
551.60	2495	2775	2490	2780	2540	2820	2590
5057.00	2085	2340	2080	2345	2130	2385	2180
8904.00	2000	2240	2000	2255	2050	2300	2100
corr. coef.	1.000	1.000	1.000	1.000	1.000	0.999	1.000
mV/decade	-431	-439	-432	-437	-430	-437	-430
mV at 1 hour	3691	3977	3691	3976	3734	4020	3782
hours to .1V	2.11E08	6.66E08	2.03E08	7.48E08	2.78E08	9.34E08	3.72E08

Table 1-10. Retention Characteristic for 14 Cells From Part 6020 Serial 270
(Retention Test Started 3 May 1978 After 1E5 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
7.66	3475	3120	3475	3110	3445	3100	3465
75.00	3070	2645	3075	2655	3045	2633	3050
551.60	2645	2235	2640	2220	2615	2215	2630
5057.00	2180	1805	2180	1770	2140	1770	2165
8904.00	2095	1715	2085	1685	2050	1690	2075
corr. coef.	0.999	1.000	0.999	1.000	0.999	1.000	1.000
mV/decade	-459	-460	-462	-471	-464	-465	-461
mV at 1 hour	3901	3515	3906	3527	3881	3504	3889
hours to .1V	1.90E08	2.63E07	1.75E08	1.90E07	1.39E08	2.12E07	1.67E08

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 8	CELL 9	CELL10	CELL11	CELL12	CELL13	CELL14
7.66	3105	3440	3145	3485	3165	3500	3155
75.00	2655	2986	2690	3070	2700	3085	2685
551.60	2220	2600	2255	2640	2270	2660	2265
5057.00	1780	2120	1810	2170	1820	2180	1815
8904.00	1700	2035	1730	2080	1745	2085	1735
corr. coef.	1.000	1.000	1.000	0.999	1.000	0.999	1.000
mV/decade	-465	-463	-468	-466	-470	-469	-468
mV at 1 hour	3515	3853	3557	3916	3575	3937	3562
hours to .1V	2.22E07	1.29E08	2.44E07	1.52E08	2.52E07	1.50E08	2.50E07

Table 1-11. Retention Characteristic for 14 Cells From Part 6020 Serial 271 (Retention Test Started 8 May 1978 After 1E7 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
19.92	2900	2855	2970	2830	2970	2830	2950
212.50	2268	2280	2410	2170	2310	2268	2385
428.50	2050	2105	2240	1970	2125	2075	2215
4947.00	1440	1580	1710	1360	1520	1535	1680
8781.00	1335	1480	1600	1260	1410	1430	1570
corr. coef.	0.999	0.999	1.000	0.999	0.999	0.999	1.000
mV/decade	-596	-520	-518	-596	-590	-531	-522
mV at 1 hour	3655	3505	3626	3575	3707	3505	3610
hours to .1V	9.22E05	3.53E06	6.41E06	6.74E05	1.29E06	2.55E06	5.33E06

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 8	CELL 9	CELL10	CELL11	CELL12	CELL13	CELL14
19.92	2850	2905	2880	2975	2770	2915	2765
212.50	2185	2250	2300	2415	2110	2245	2211
428.50	1975	2045	2125	2235	1910	2065	2015
4947.00	1355	1435	1590	1685	1290	1460	1495
8781.00	1265	1330	1490	1580	1195	1355	1395
corr. coef.	0.999	0.999	0.999	1.000	0.999	0.999	0.999
mV/decade	-604	-598	-526	-530	-599	-590	-520
mV at 1 hour	3605	3655	3539	3651	3521	3648	3421
hours to .1V	6.35E05	8.81E05	3.44E06	5.02E06	5.09E05	1.03E06	2.44E06

Table 1-12. Retention Characteristic for 14 Cells From Part 6020 Serial 275 (Retention Test Started 3 May 1978 After 1E6 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
7.66	2805	2820	2855	2830	2875	2865	2880
75.00	2250	2095	2315	2305	2330	2325	2335
551.60	1750	1810	1790	1820	1805	1840	1810
5057.00	1230	1325	1270	1335	1285	1355	1285
8904.00	1140	1245	1185	1255	1200	1270	1195
corr. coef.	1.000	0.991	0.999	0.999	0.999	0.999	0.999
mV/decade	-549	-497	-554	-521	-555	-526	-558
mV at 1 hour	3280	3167	3340	3278	3359	3314	3369
hours to .1V	6.17E05	1.47E06	7.10E05	1.28E06	7.45E05	1.30E06	7.23E05

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 8	CELL 9	CELL10	CELL11	CELL12	CELL13	CELL14
7.66	2715	2865	2840	2860	2835	2855	2735
75.00	2165	2320	2310	2310	2305	2310	2175
551.60	1660	1790	1815	1785	1810	1780	1675
5057.00	1160	1260	1310	1260	1320	1255	1175
8904.00	1065	1175	1215	1175	1240	1180	1080
corr. coef.	0.999	0.999	1.000	0.999	0.999	0.999	0.999
mV/decade	-543	-561	-536	-558	-528	-557	-544
mV at 1 hour	3183	3357	3308	3347	3290	3341	3200
hours to .1V	4.71E05	6.45E05	9.66E05	6.55E05	1.11E06	6.62E05	4.97E05

Table 1-13. Retention Characteristic for 14 Cells From Part 6020 Serial 278
(Retention Test Started 11 May 1978 After 1E8 Erase-Write Cycles)

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 1	CELL 2	CELL 3	CELL 4	CELL 5	CELL 6	CELL 7
2.00	3505	3480	3375	3345	3530	3475	3395
24.40	2635	2600	2435	2405	2655	2590	2460
360.80	1810	1775	1595	1565	1830	1750	1620
4875.00	1280	1155	1000	980	1215	1130	1025
8713.00	1005	1030	910	880	1150	1055	975
corr. coef.	0.996	0.997	0.994	0.994	0.995	0.995	0.993
mV/decade	-663	-668	-672	-671	-655	-665	-664
mV at 1 hour	3621	3593	3459	3428	3632	3580	3473
hours to .1V	2.05E05	1.71E05	9.95E04	9.15E04	2.46E05	1.70E05	1.19E05

READ DELAY hours	DIFFERENTIAL CELL VOLTAGE millivolts CELL 8	CELL 9	CELL10	CELL11	CELL12	CELL13	CELL14
2.00	3350	3485	3445	3410	3415	3505	3445
24.40	2410	2590	2540	2475	2470	2600	2545
360.80	1570	1760	1710	1650	1635	1770	1715
4875.00	995	1150	1100	1060	1050	1165	1100
8713.00	805	1080	1025	970	1000	1085	1045
corr. coef.	0.995	0.995	0.995	0.994	0.992	0.995	0.994
mV/decade	-683	-660	-663	-665	-662	-663	-660
mV at 1 hour	3447	3581	3539	3491	3486	3599	3538
hours to .1V	8.01E04	1.87E05	1.53E05	1.27E05	1.30E05	1.90E05	1.61E05

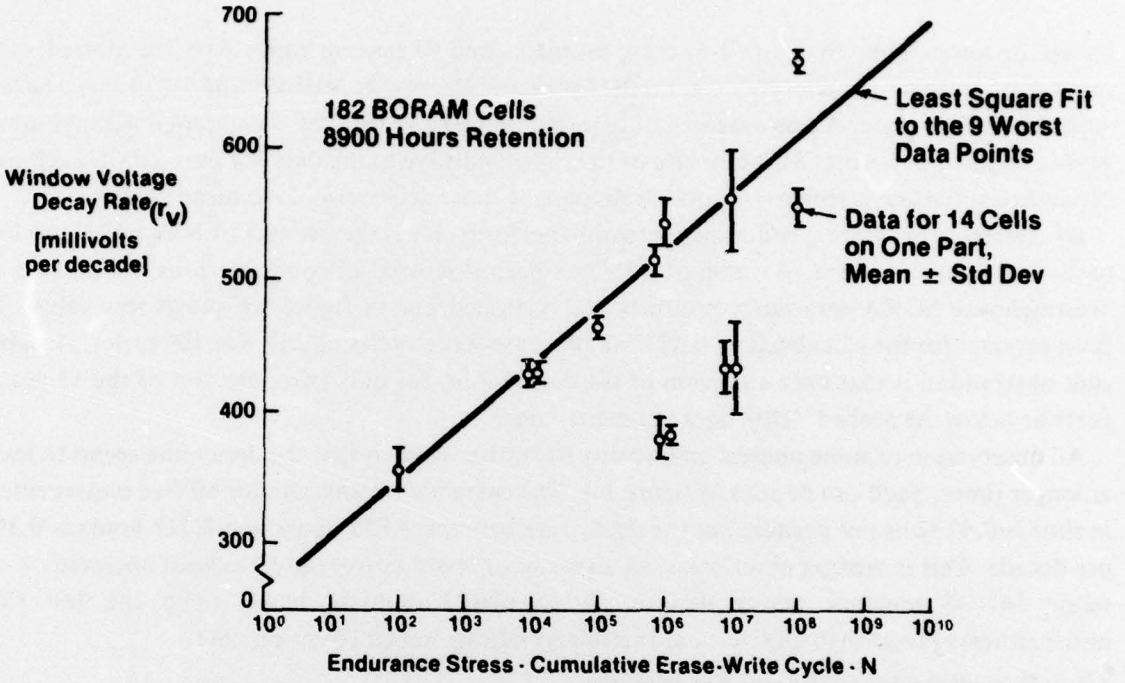
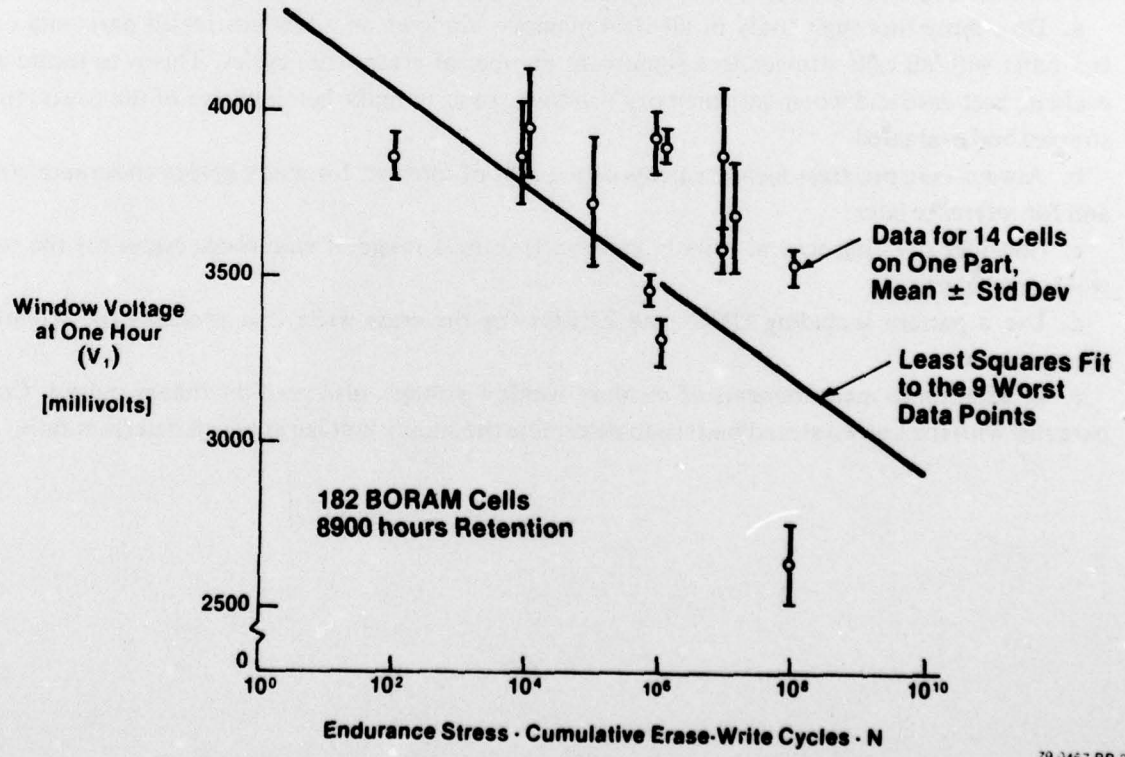


Figure 1-4. Window Decay Rate as a Function of Endurance Stress

79-0467-BB-1



79-0467-BB-2

Figure 1-5. Window Voltage at 1 Hour as a Function of Endurance Stress

above the lower limit. In figure 1-6, these estimates and 95 percent range bars are plotted vs the number of erase-write cycles (N). Again, the four parts stressed at N of 10^6 and 10^7 are seen to have superior performance. A least squares fit of a line to log t_R vs log N was computed with these four parts excluded, as before. This estimate of t_R is very sensitive to the data for each cell of each part. Nevertheless the line is seen to fit rather well, passing quite near most of the mean values.

Of interest in evaluating endurance-retention performance is the product of $N \cdot t_R$ which has been used as a figure of merit. A value of 10^{12} has been discussed in some previous writings on the Westinghouse BORAM memory products and a dashed line in figure 1-6 shows this value. The $N \cdot t_R$ product for the calculated fit is 12.7 at 10^4 erase-write cycles and 12.8 at 10^8 cycles. A significant observation is that only a portion of the distribution for only two parts out of the 13 plotted parts lie below the dashed "10^{12} figure of merit" line.

An observation of some interest and worthy of further study is that the decay rate seems to lessen at longer times. Such can be seen in figure 1-1. The calculated decay rate for all five measurements in time is 0.67 volts per decade, but the decay rate between 4,875 hours and 8,713 hours is 0.39 V per decade. This is seen on other parts, to a greater or lesser degree, and has been observed on different MNOS memory device designs. A calculated estimate based upon the last three measurements rather than all five would certainly indicate longer retention time.

1.2.5 Considerations for Future Experiments

A secondary objective of this experiment was to discover problems to avoid and improvements to add to future experiments. The following remarks are in response to that objective.

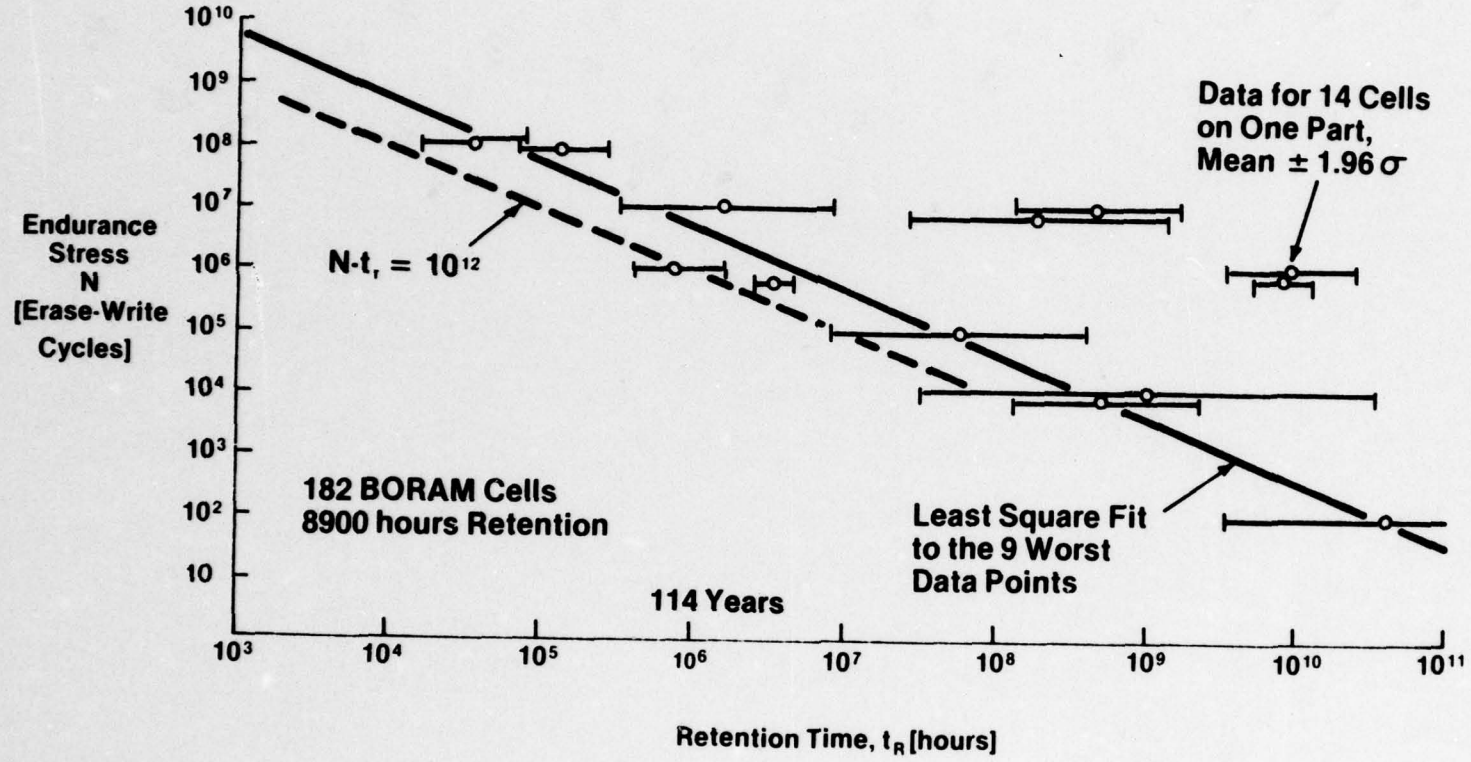
a. Do a more thorough study of all 1024 memory windows on a few unstressed parts and on a few parts with all cells stressed to a significant number of erase-write cycles. This is to locate and evaluate best-case and worst-case memory windows, so as to make better choice of the row(s) to be stressed and evaluated.

b. Always take prestress measurements of the cells of interest, for study before endurance stress and for reference later.

c. Consider stressing several rows in each part, using a range of endurance cycles for the rows within each part.

d. Use a pattern including ONEs and ZEROs for the erase-write that precedes the retention measurements.

e. In addition to measurements of memory window voltage, also read the binary output. Compare this with the known stored pattern to determine the supply voltage at which detection fails.



1-27/1-28

Figure 1-6. Endurance-Retention Characteristic

2. CONCLUSIONS

The BORAM cell design and fabrication process have been demonstrated to be compatible with the goals of providing an alternative to drum and disc memory usable through 10^8 erase-write cycles with 4,000 hours retention. The test data shows how endurance and retention are related, and allows intelligent planning for system specification purposes.

3. PROGRAM FOR NEXT INTERVAL

The pilot run is nearing completion and the MM&T project will shortly be concluding. The work remaining includes a production demonstration and the final report.

4. PUBLICATIONS AND REPORTS

During the reporting period there were no publications derived directly from this contract effort.

5. IDENTIFICATION OF TECHNICIANS

The following key engineers and management personnel were employed on the BORAM manufacturing methods project from April 1978 through April 1979.

Technician	Manhours
J.E. Brewer	78
R.C. Crebs	68
R.B. DeGraw	74
M.L. Lonky	16
T.J. O'Donnell	35
R.H. Popp	190
C.W. Waldvogel	8
Process Engineers	221

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