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A FUZE FUNCTION SETTER--BASELINE DESIGN.(U)
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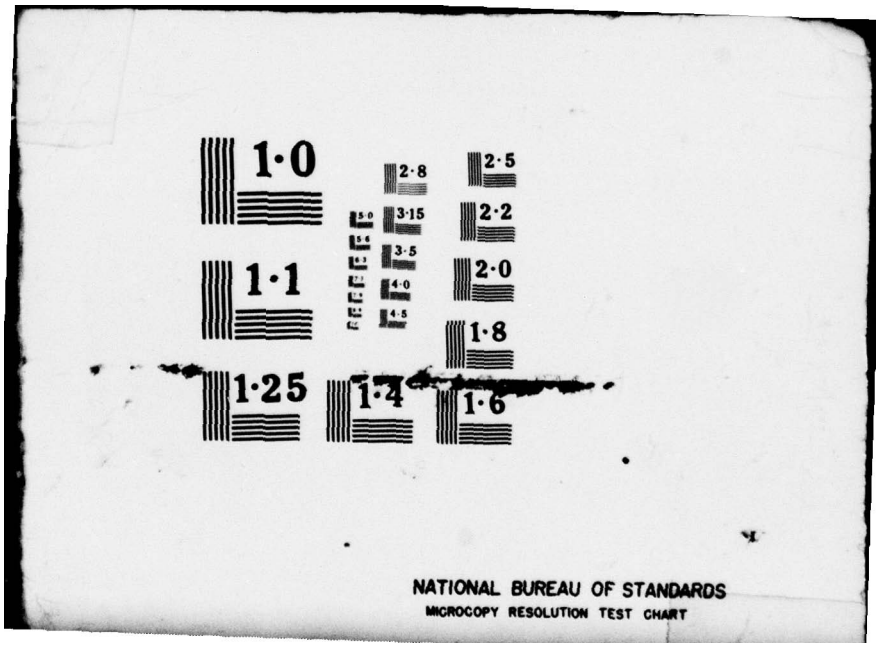
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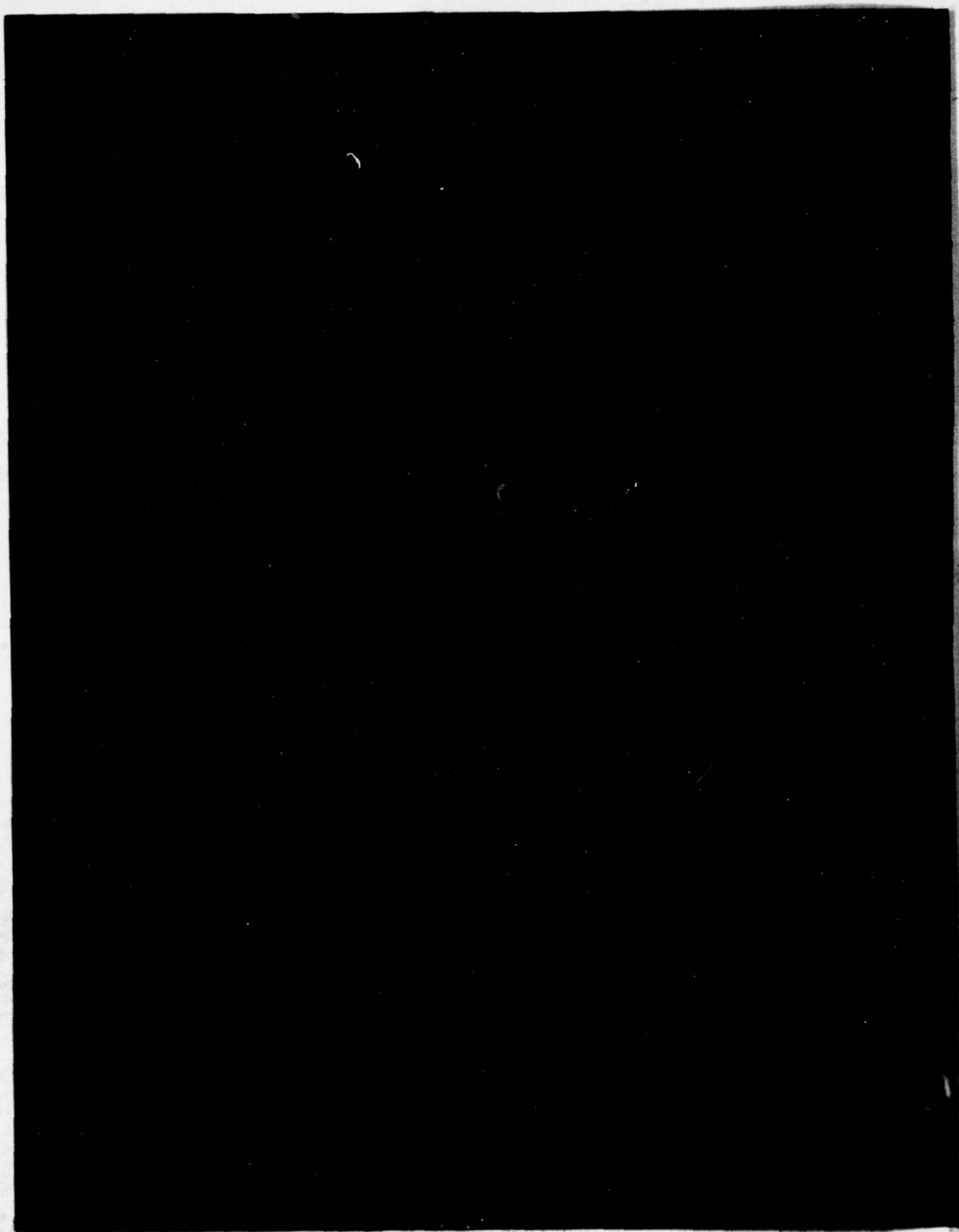

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The fuze function setter system described provides a means for inductively transmitting data and energy into an unpowered projectile prior to firing. This system was developed because of a need to program the Navy's Semi-Active Laser Guided Projectile with time delay and guidance information as it is loaded into the gun. (over)

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20. Abstract (Cont'd)

An advanced development prototype system is described that demonstrates the feasibility of this type of design. Both the setter and the projectile electronics were fabricated and tested. The system features a reverse link whereby the round retransmits the data that it receives for verification. It also incorporates a metal nitride oxide semiconductor memory for long-term storage and a custom integrated circuit for minimum volume and power requirements.

The system was successfully demonstrated in the field and will proceed to the engineering development phase.

CONTENTS

CONTENTS (Cont'd)

FIGURES

FIGURES (Cont'd)

1. INTRODUCTION

The Navy Semi-Active Laser Guided Projectile (SALGP) System requires that information be provided to the projectile just prior to firing. Present Navy systems that set information into the round, such as the mechanical fuze setter, are not adequate for this task. This report describes the advanced development of an inductive fuze function setter (FFS) system that is capable of setting information into the round during the normal loading sequence.

The system developed consists of a data entry unit (DEU), through which data are manually entered into the system, the setter unit (SU), which is mounted on the gun, and the function setter receiver (FSR), which is the receiving unit on the projectile. Data are entered through a series of switches on the DEU, which then sends the data to the SU. The SU consists of an electronics unit and a coil mounted on the face of the existing mechanical setter. The data are used to modulate a signal that drives the coil and induces a signal on a second coil located in the projectile. Energy and data are extracted by the FSR electronics and stored in the round. Upon completion of the message, it is retransmitted to the SU and then to the DEU for verification.

The DEU and the FSR were designed specifically for use with the SALGP. Ultimately, the function of the DEU will be replaced by the fire control system, but the DEU is used now as a development aid. The FSR design will be integrated into the guidance and control (G&C) section of the SALGP.

2. REQUIREMENTS

Most of the requirements in this section were developed for the 5-in. SALGP. However, they should not be restrictive for other systems that might use the FFS.

2.1 Set Time

The projectile must receive data as it cycles through the gun mount. To be compatible with the loading procedure, the FFS must set the round in less than 1.2 s.

2.2 Data Confirmation

Because of the cost of each round, some positive indication must be obtained from the projectile that a message was received and properly interpreted.

2.3 Power Source

Power required for the projectile electronics during the setting operation must be supplied through the setting link. Projectile batteries will not be available.

2.4 Memory Retention

Once programmed, the projectile may be loaded into the breech, where it may sit for several minutes until fired. While it is in this position, it is not accessible for reprogramming or having its power supply refreshed. Therefore, once set, it must retain its memory for 5 min or more without additional power.

2.5 Data

Up to 24 bits of information must be transmitted to and stored in the SALGP.

2.6 Time Delay

Part of the transmitter message defines a time delay after which the G&C battery is turned on. It does so to conserve battery power. The time delay must be generated by the FSR circuit and must meet the following specifications:

Range: 1 to 255 s

Resolution: 1 s

Accuracy: ±1 percent

2.7 Packaging

The FFS and FSR electronics must be capable of being packaged in such a way that they can survive their operational environment. In addition, the FSR electronics must not use more than 4 in.^{2} (25.4 cm^2) of printed circuit board area.

2.8 Compatibility

The FFS system must be compatible with existing mechanical fuze setters. During this development program, this compatibility was demonstrated only on the Mk 42 gun mount and associated fuze setter.

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3. SYSTEM DESCRIPTION

3.1 General

To meet the requirements of section 2, the FFS was designed with the features described below:

Inductive coupling.--An inductive link is used by the FFS for data transmission. It consists of a transmitting coil located on the present mechanical fuze setter and a pickup coil wound on the gyroscope coil form of the projectile. Energy induced on the pickup coil is stored and used to power the projectile electronics during the programming phase. Data are transmitted by amplitude modulation of the carrier signal.

Because of this inductive coupling, no physical contact is made between the round and the setter. Therefore, electrical contacts that are suceptible to corrosion and wear are not required; also, the axial orientation of the round is not critical, so some method of keying the projectile prior to setting is not required. Not requiring them makes it easier to meet the compatibility requirement between the mechanical fuze setter and the FFS.

Reverse link.--To obtain some positive indication that a message was received and properly interpreted, a method of retransmitting the data from the receiver to the transmitter has been devised. Thus, the accuracy of the data transmission can be checked, and, if it is incorrect, the data can be transmitted again. The reverse link is connected by short-circuiting the pickup coil on the projectile in a coded manner. This short-circuiting changes the impedance reflected to the primary coil, where this impedance change is detected and decoded.

Memory.--A nonvolatile metal nitride oxide semiconductor (MNOS) memory is used, which does not lose stored data if power is turned off. The memory retention requirement can therefore be met.

Custom integrated circuit.--Serious space limitations on the projectile required that a custom complementary metal oxide semiconductor (CMOS) integrated circuit be developed that would include most of the control and time delay electronics.

3.1.1 Configuration

The laboratory prototype system is shown in figure 1. The transmit coil is wound on a Bakelite form, which is mounted on the face of the present mechanical setter. Tuning capacitors also are mounted on the form and are selected to tune the coil to the carrier frequency.

An SU box houses the driving amplifier for the coil. It also houses the reverse link detector and interface electronics. Power for the system is supplied by a ±28-V power supply, which operates from a 110-V, 60-Hz line.

A DEU also is shown in figure 1. This unit was primarily designed so that data could be easily and manually selected through a series of thumbwheel and toggle switches. Its function will ultimately be performed automatically by the fire control computer.

A layout of the round showing the coil and the FSR is shown in figure 2. The receive coil is wound on the forward end of the coil form. Two wires from the coil carry the received signal to the FSR electonics located in the G&C electronics, where it is processed. A breadboard of the FSR is shown in figure 3. The integrated circuits are shown in dual in-line packages, but flat packs will be used in actual hardware. About 3 $in.^2$ (19 cm^2) of printed circuit board space is required for the FSR.

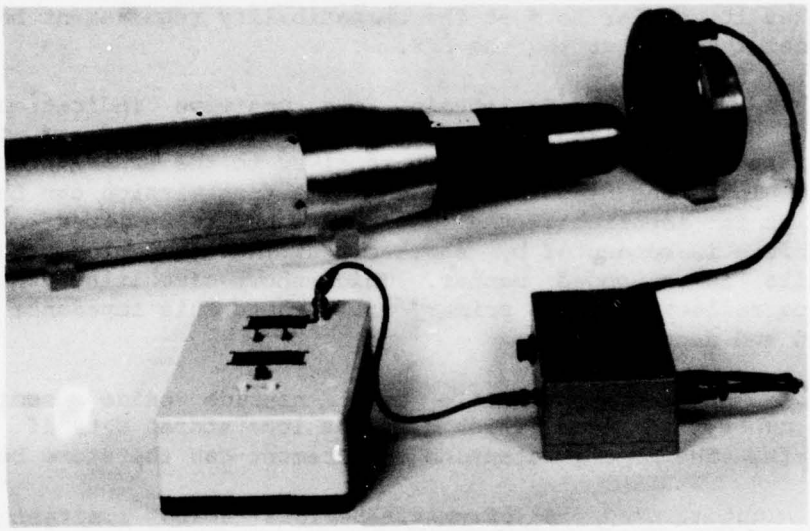


Figure 1. Prototype system of fuze function setter

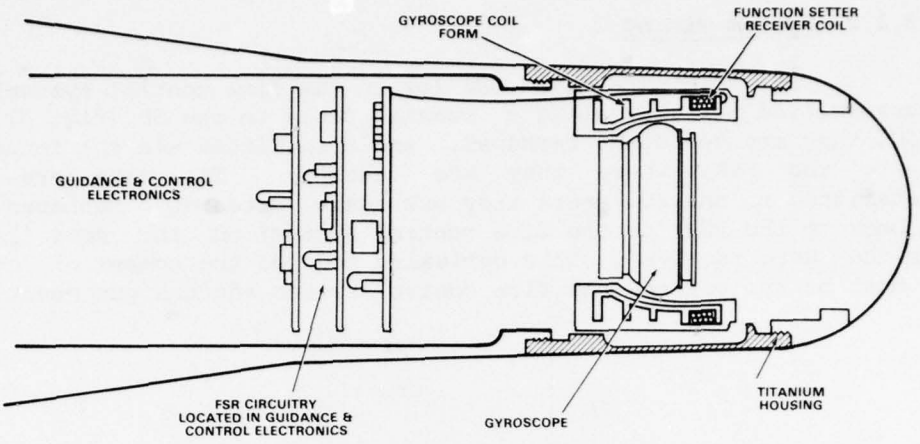


Figure 2. Function setter receiver coil and electronics.

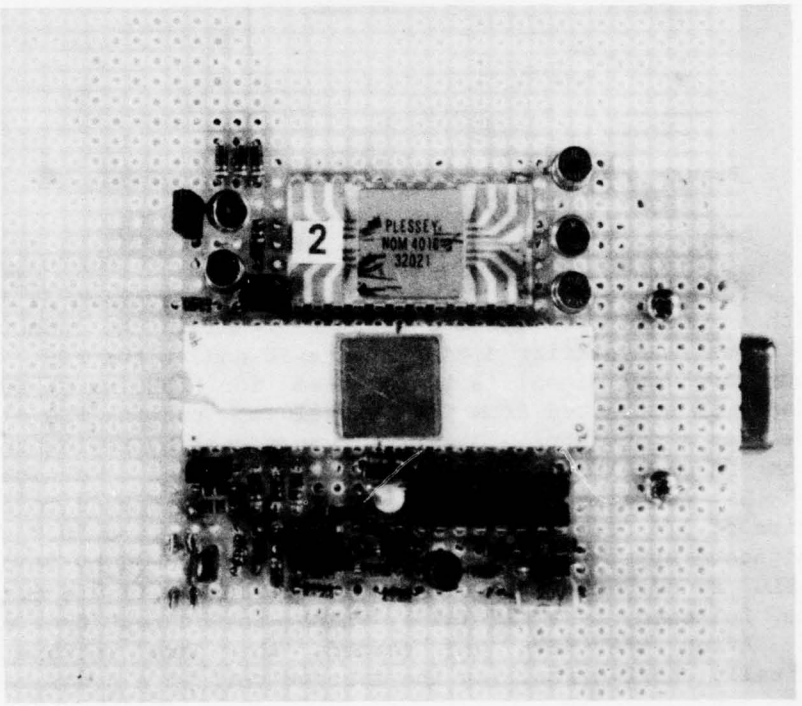


Figure 3. Function setter receiver breadboard.

3.1.2 System Timing

Data originate at a DEU (or in the fire control system) and are transmitted serially along a coaxial cable to the SU (fig. 4). In the SU, they are detected, reshaped, and transmitted via the inductive link to the FSR, where they are stored. The data are then retransmitted to the SU, where they are again detected, reshaped, and sent back to the DEU (or the fire control system) on the same line on which they were received. This duplexing reduces the number of cables that must be run between the fire control system and the gun mount.

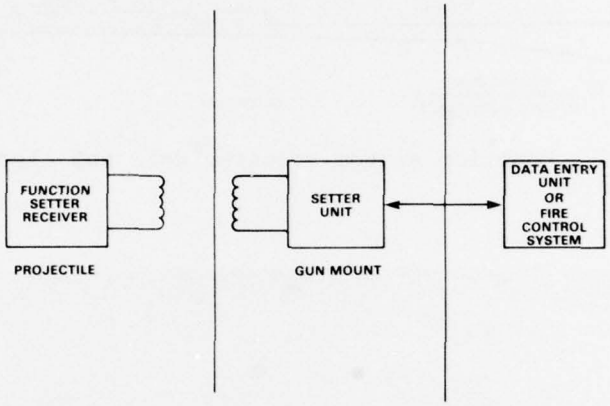


Figure 4. Fuze function setter data transmission path.

To describe the exact timing of the system, it is best to start with a description of the carrier signal in the inductive link. Figure 5 shows the carrier signal at the SU and at the FSR. A 100-kHz continuous wave (cw) signal is transmitted for 500 ms. During this time, energy is extracted from the signal to run the FSR electronics and stored on a capacitor. Data are transmitted by keying the carrier off and on at a 1-kHz rate. The off time is coded to designate a "0" or a "1." An off time of 1/2 cycle (0.5 ms) corresponds to a "1," and an off time of 1/4 cycle (0.25 ms) corresponds to a "0." The first bit, designated B0, is always a "1" and is followed by 24 data bits. In the SALGP rounds, the bit meaning is given in figure 6. The data bits are followed by a "1" (B25), which designates the end of a message. After the data are stored, they are retransmitted by electronically short-circuiting the receive coil in a coded manner.

The coding for the reverse link also is shown in figure 5. The switch across the receive coil is closed and opened at a 4.096-kHz rate in bursts. The length of these bursts corresponds to a "0" or a "1." A data rate (or burst rate) of 128 Hz is used, and, similar to

the forward link, a 1/2-cycle burst (~4 ms) means a "1," and a 1/4-cycle burst (~2 ms) means a "0." Data bits are retransmitted in the same order that they were received, except that B0 is not retransmitted.

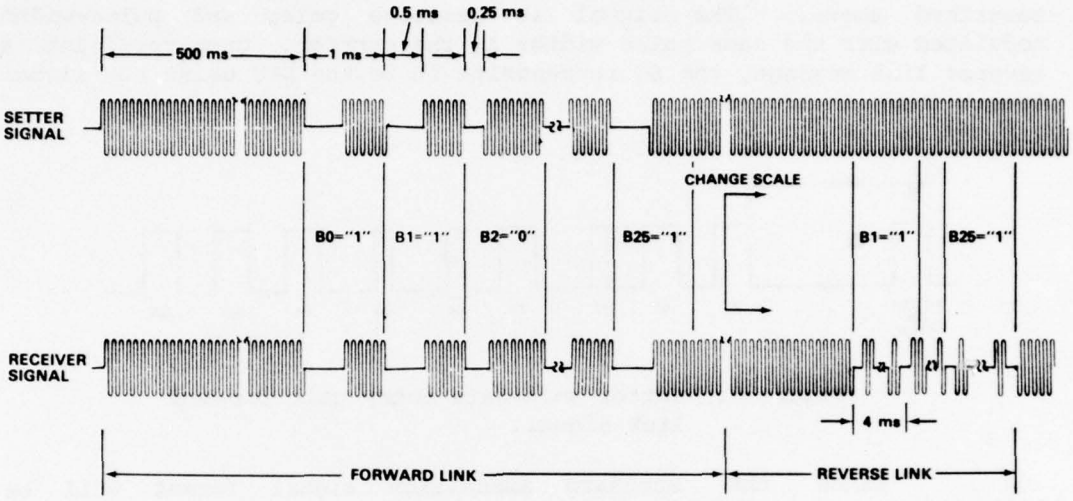


Figure 5. Fuze function setter inductive link carrier signal.

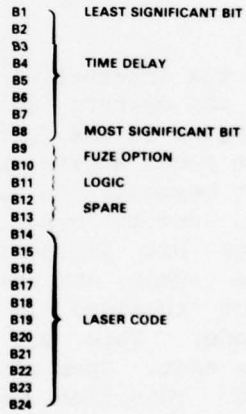


Figure 6. Bit definition for Semi-Active Laser Guided Projectile rounds.

Figure 7 shows the signals present at the interface between the SU and the fire control system. In the SALGP, the sequence begins with a "1" (0.5-ms pulse) from the DEU, which turns on the power amplifier, and the projectile power supply capacitor begins charging. After 500 ms, the 26 message bits are transmitted in the order described above. The signal is positive going and pulse-width modulated with the same pulse widths as the carrier. Upon receiving a reverse link message, the SU retransmits it to the DEU using the signal format shown in figure 7.

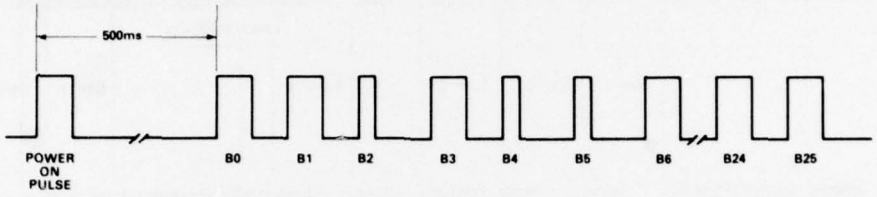


Figure 7. Setter unit-data entry unit forward link signal.

Since the standard ammunition signal format will be different from that described above, the SU was designed to be as flexible as possible, primarily by being made a "repeater." It detects, reshapes, and then transmits whatever it receives. In addition, it switches between the forward and reverse modes automatically.

A flow chart of the internal logic sequence of the SU is shown in figure 8. The SU can operate in one of two modes--forward or reverse. The sequence begins in the forward mode. When a "1" is received from the DEU, the power amplifier is turned on immediately, and the SU awaits the first message. On reception of a message bit, a 10-ms time delay begins, and the message bit is transmitted to the fuze. If another message bit is received before the time delay is over, the time-out begins again, and the new bit is transmitted. If another message bit is not received in 10 ms, the SU automatically switches to the reverse mode. This way the system is independent of the number of message bits sent. Upon switching to the listen mode, a 35-ms time delay is started. This time corresponds to the maximum time required by a projectile to respond to a message. If a response is received in this time, the data bit is sent to the DEU, and the time-out is restarted. If a response is not received within this time, a "1" is automatically sent to the DEU, and the SU switches to the forward mode and begins a 20-ms time delay. During this delay, the DEU (or the fire control system) can inspect the reverse message, and, if the message is incorrect, the DEU may send a new message before the SU turns off the power amplifier. This means that the 500-ms charge-up

period need not be used. If the data are correct or no new message is received, the SU turns off the power amplifier. Figure 9 is a timing diagram for a typical projectile and a hypothetical standard ammunition round showing the various time-outs. The standard round is assumed to require 18 bits and does not have a reverse link capability.

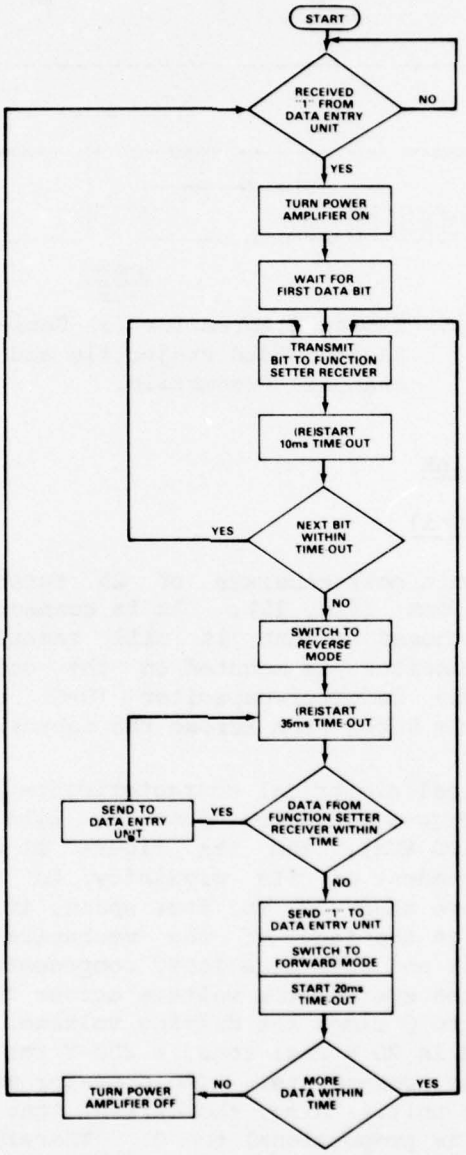


Figure 8. Setter unit logic flow chart.

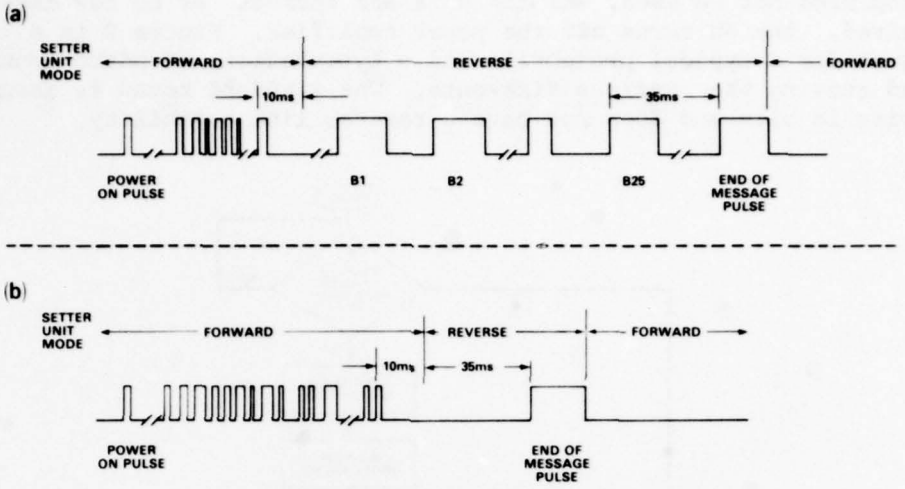


Figure 9. Timing diagram for (a) Semi-Active Laser Guided Projectile and (b) standard Projectile.

3.2 Inductive Link

3.2.1 Transmit Coil

The transmit coil consists of 25 turns of No. 22 AWG wire wound on a Bakelite form (fig. 10). It is connected in series with a capacitor, which is chosen so that it will resonate with the coil at 100 kHz. This capacitor is mounted on the coil form. A power amplifier drives the inductor-capacitor (L-C) combination, and the reverse link signal is taken from across the capacitor only (fig. 11).

The critical electrical characteristics of the coil assembly are its resonant frequency, which must be within 1 percent of the driving frequency (100 kHz), and its figure of merit (Q). Q of the coil is greatly dependent on its proximity to surrounding metals. Although Q can be more than 50 in free space, it drops to ~10 when the coil is mounted on the face of the mechanical setter because the setter loads the coil and acts as a lossy component in the L-C circuit. Before operating the system, the voltage across the L or the C is approximately equal to Q times the driving voltage. In this case, the driving voltage used is 20 V rms; thus, a 200-V rms signal is generated across each of these components. (An operator must exercise caution when working in the unit.) Also, the current that must be supplied by the power amplifier is proportional to Q. Therefore, more than five times the current may be drawn if the coil is in free space and not under the loaded conditions of the setter face. This amount may burn out the power amplifier. Thus, the power amplifier should not be turned on unless the coil is mounted on the setter or a similar metal housing.

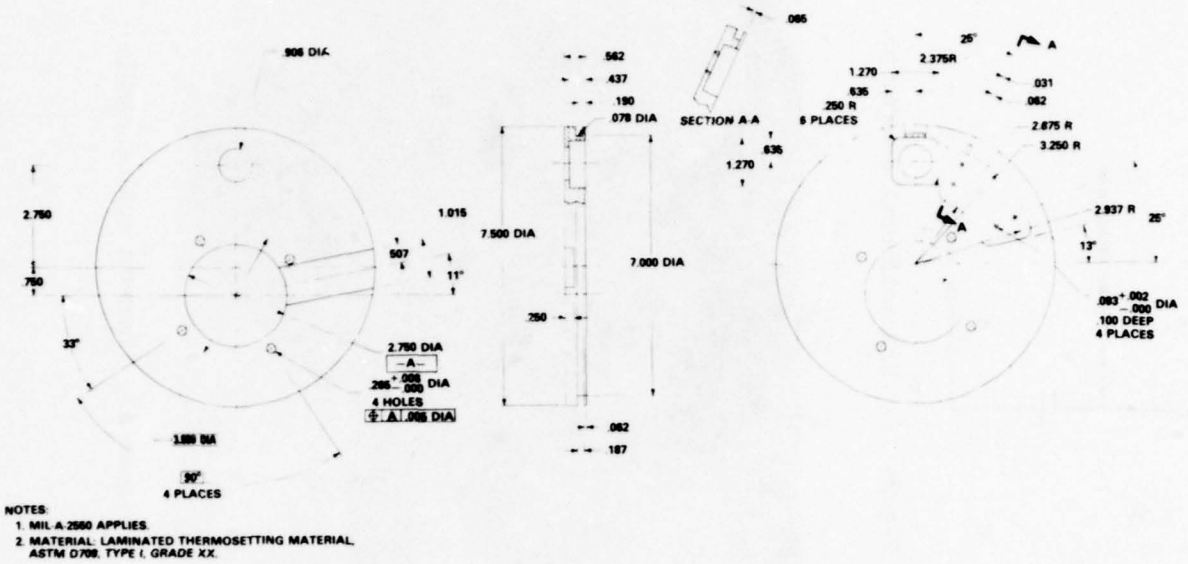


Figure 10. Transmit coil form.

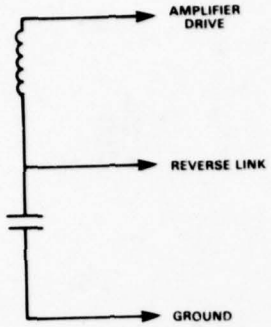


Figure 11. Transmit coil schematic.

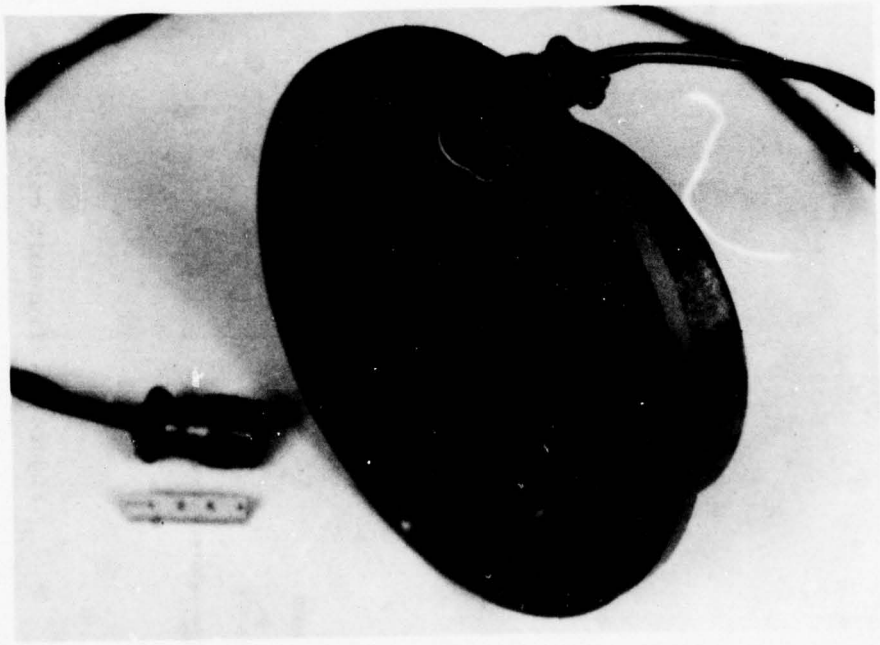


Figure 12. Transmit coil assembly.

Signals from the coil form are transmitted to the setter box through shielded cables.

3.2.2 Receive Coil

The receive coil is wound on the forward end of the gyroscope coil assembly (fig. 2). The coil consists of 300 turns of No. 31 AWG wire. A capacitor is placed in parallel with it so that the combination resonates at 100 kHz ± 1 percent. As for the transmit coil, Q is relatively low because of surrounding metal structures. It has a value of approximately 6.

This coil has only been simulated in the laboratory by using an obsolete gyroscope coil form that was modified to hold the receive coil. When a final gyroscope coil form is delivered and the system is tested on the projectile, two tests should be made. First, since the tuning capacitor is only approximately 400 pF, the parasitic capacitance of the wires leading to the coil will be significant. This capacitance must be measured, and the value of the tuning capacitor must be adjusted appropriately. Second, the coil should be measured to determine if there are any self-resonant frequencies near 100 kHz that might make tuning difficult.

3.2.3 Coupling

The degree of coupling between the transmit and receive coils is the critical factor in the operation of the FFS. It is dependent on both the geometric and the electrical characteristics of the FFS. This section describes how the coupling varies with respect to some of these characteristics. Formulas are presented, but are not derived. Their derivation will be covered in another report.

In the forward link, two parameters are of primary interest: the forward voltage transfer ratio, G_v, and the effective output impedance of the secondary coil, Z_o. G_v may be expressed as

$$G_v = \frac{E_2}{E_g} = KQ_1Q_2\left(\frac{L_2}{L_1}\right)^{\frac{1}{2}} ,$$

where

E_2 = voltage on secondary coil,

E_g = driving voltage across primary coil L-C,

K = coefficient of coupling,

Q_1, Q_2 = figures of merit for primary and secondary coils,

L_2, L_1 = inductances of secondary and primary coils.

The equation for G_V assumes that the primary and secondary coil resonant frequencies and the driving frequency are the same. But they cannot be the same in actual hardware, so the equation is a best-case solution. Analysis indicates that if these frequencies are held within the specifications of section 5, the degradation in signal level is acceptable.

The coefficient of coupling, K, is a function of geometry and accounts for such things as the distance between coils, local shielding effects, and coil diameters. It is determined empirically for a specific geometry. Measurements of K were taken on a gun mount at the Naval Surface Weapons Center, Dahlgren, VA (fig. 13). Also in the equation for G_V, since $L_{1,2} = \alpha N_{1,2}$, then G_V is proportional to the turns ratio N_2/N_1, as one would expect. Figure 14 shows a calculation of G_V based on typical parameter values. Again, this is a best-case solution.

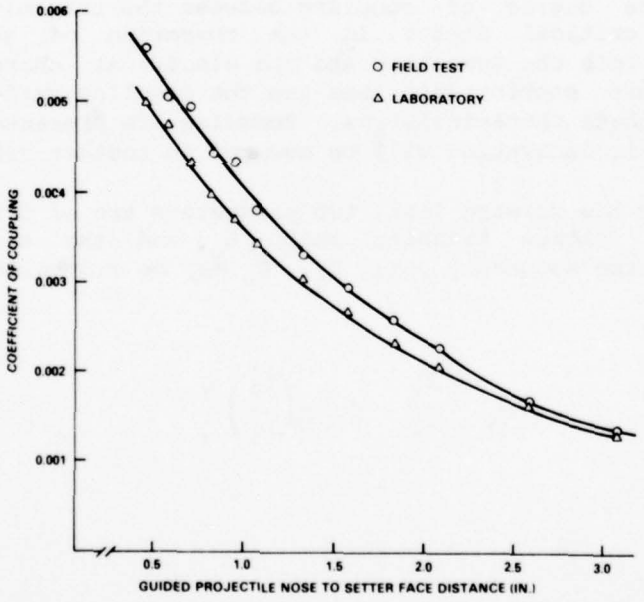


Figure 13. Coefficient of coupling.

$$G_v = \frac{E_2}{E_g} = KQ_1Q_2\left(\frac{L_2}{L_1}\right)^{1/2}$$

SINCE $f_o = 100\text{kHZ} = \left(\frac{1}{LC}\right)^{1/2}$ FOR PRIMARY AND SECONDARY COILS.

$$G_v = \frac{E_2}{E_g} = KQ_1Q_2\left(\frac{C_1}{C_2}\right)^{1/2}$$

PARAMETER VALUES FOR THIS EQUATION ARE

$K = 0.0045$ FROM FIGURE 12 AT 3/4 IN.

$Q_1 = 10.$

$Q_2 = 6.$

$C_1 = 0.016\ \mu F.$

$C_2 = 440\ pF.$

$$G_v = (0.0045)(10)(6)\left(\frac{0.016\ \mu F}{440\ pF}\right)^{1/2} = 1.63$$

IF $E_g = 60\ V_{pp}$,
THEN $E_2 = (1.63)(60)\ V_{pp}$

$E_2 = 97.6\ V_{pp}$ OPEN CIRCUIT

Figure 14. Calculation of forward voltage transfer ratio (G_V).

The other parameter besides G_V that is of interest in the forward link is Z_O. This is important because it is a measure of the charge-up time of the power supply capacitor on the projectile. Its value is difficult to express analytically because it must include the variable duty cycle effect of a rectifier charging a capacitor. Generally, it can be considered proportional to the secondary coil inductance which, in turn, is proportional to the number of secondary coil turns, N_2. Thus, to keep the charge-up time small, N_2 should be kept small. This proportion is opposed to the case for G_V, for which a large N_2 is desirable for increased voltage transfer. A trade-off therefore exists, and N_2 was made as large as possible, while still maintaining a reasonable charge-up time.

Data transmission for the reverse link is not as simple a voltage transfer as for the forward link. To discuss its significant parameters, it is best to give a brief qualitative description of what happens. As discussed in section 3.1.2, data are retransmitted in the reverse direction by electronically short-circuiting the secondary coil. This short-circuiting alters the impedance characteristics of the primary coil. Figure 15 shows what happens. The solid lines indicate the voltage and phase relationships for the primary coil L-C combination with the secondary coil open circuited. When the secondary coil is short-circuited, the curves shift slightly as indicated by the dotted lines, and the operating point moves from A to B. Since both amplitude and phase change, either could be detected. Amplitude detection, though, has a disadvantage as shown in figure 16. If the tuning of the coils with respect to the driving frequency is as shown, the amplitude for the open- or short-circuited case is the same, and

detection is impossible. This impossibility is demonstrated in the laboratory by sweeping the driving frequency and noting a null in the output of an amplitude detector. Because of this null, it was decided to sense phase changes that do not null.

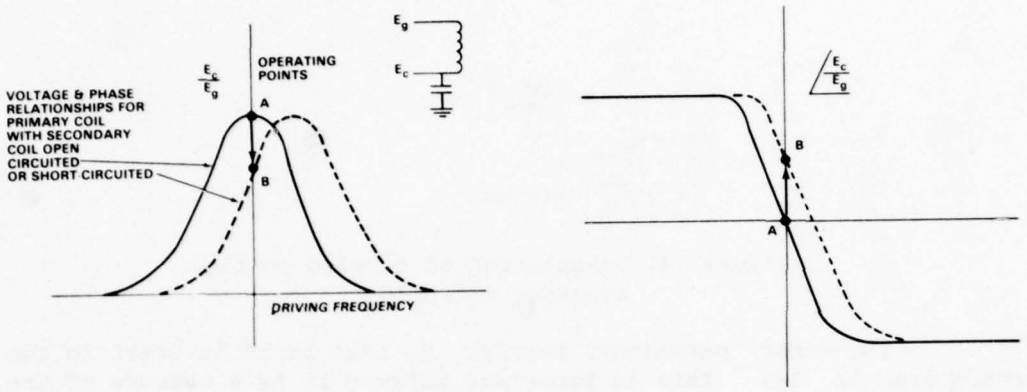


Figure 15. Reverse link resonance with amplitude change.

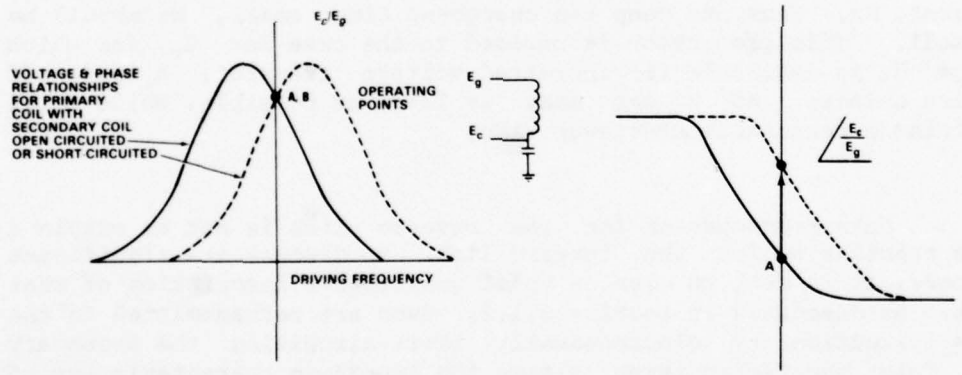


Figure 16. Reverse link resonance without amplitude change.

In addition to phase demodulation, the system uses a subcarrier frequency of 4.096 kHz and a data rate of 128 Hz as described in section 3.1.2. These are used to reduce the 1/f noise and to simplify the design of the receiver. They also reduce the bandwidth required for detection, which increases the noise immunity of the system.

Two characteristics are important to the operation of the reverse link: (1) the short- versus open-circuit phase difference, θ, and (2) the bandwidth of the primary coil. θ may be expressed as

$$\theta = \angle\left.\frac{V^2}{E_g}\right|_{\text{open}} - \angle\left.\frac{V^2}{E_g}\right|_{\text{short}} = -K^2 Q_1 \quad .$$

where V is the voltage. The derivation of the equation assumes exact tuning of the coils with the driving frequency. This relationship is interesting because it shows that the reverse link operation is not a function of Q_2, but only of Q_1. Q_1 should be as large as possible to give a large change in phase.

The other system characteristic that affects the reverse link is the bandwidth. The equation for θ is a static solution to the problem. To be sure that the dynamic case is nearly the same, the bandwidth of the primary coil must be large enough to encompass the 4-kHz sidebands generated by the secondary coil. This requirement means that the bandwidth should be at least 8 to 10 kHz, which implies $Q_{1\ \max}$ (low Q) = 10 to 12. Again, there exists a trade-off. A wide bandwidth is required to pass the system sidebands, whereas a narrow bandwidth (high Q) is desirable for large phase changes. Primary coil Q was chosen to be 10 to 12.

3.3 Function Setter Receiver

3.3.1 General

In the FSR (fig. 17), the signal picked up by the coil is rectified, and power is stored on a capacitor. The signal is also envelope detected, and the resultant serial data bits are fed into the control circuitry. In the control circuitry, the signal is pulse-width demodulated and shifted in parallel into the memory 8 bits at a time. A given amount of time after the first pulse is received, the reverse link begins. Data are read out of memory 8 bits at a time into the control circuitry. There, they are converted to a pulse-width-modulated signal as described in section 3.1.2. This

pulse-width-modulated signal then drives the switch located at the rectifier output, which effectively forms a bipolar switch across the coil, thus retransmitting the data.

Upon firing, the control circuitry reads the data out of memory and presents 16 parallel bits of data to the rest of the G&C electronics circuitry. It also begins generating the programmed time delay. At the end of the delay, a time-out pulse is generated.

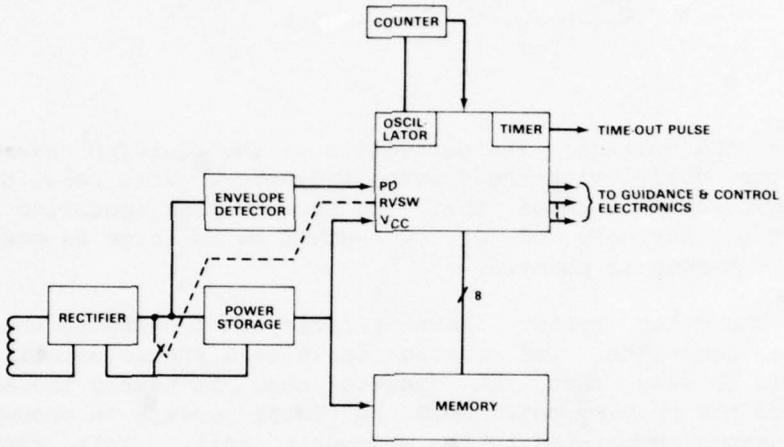


Figure 17. Block diagram of function setter receiver.

A complete schematic of the FSR is given in figure 18, and parts are listed in figure 19. Most of the control and timer circuitry is located on a custom RCA universal array (UA). A divider that divides the basic oscillator frequency of the UA is a separate off-the-shelf chip; there is not enough room to integrate it onto the UA. The memory consists of a Plessey NOM 401 memory matrix and some driver circuitry. A more detailed description of the circuit is given in the following sections.

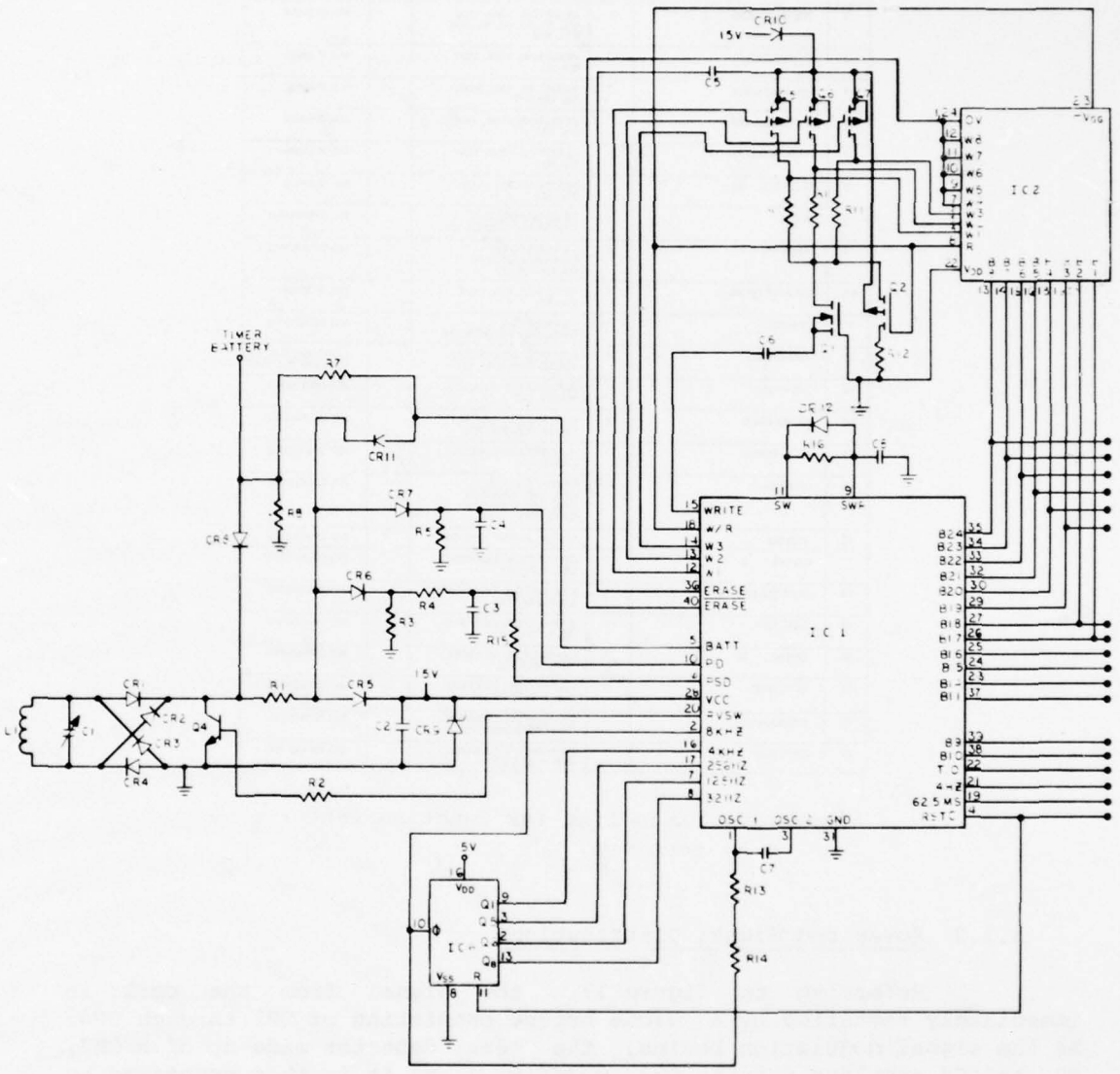


Figure 18. Schematic diagram of function setter receiver.

PARTS LIST					
INDEX NO.	PART OR IDENTIFYING NO.	QTY	DESCRIPTION	CODE IDENT	DOCUMENT NO.
1	RCR05G102JS	2	RESISTOR, 1.0K, 1/8W, 5%, R1		MIL-R-39008
2	RCR05G105JS	6	RESISTOR, 1.0M, 1/8W, 5%, R2, R4, R5, R9, R10, R11, R16		MIL-R-39008
3	RCR05G305JS	1	RESISTOR, 3.0M, 1/8W, 5%, R3		MIL-R-39008
4	RCR05G103JS	1	RESISTOR, 10K, 1/8W, 5%, R8, R15		MIL-R-39008
5	RCR05G514JS	1	RESISTOR, 510K, 1/8W, 5%, R12		MIL-R-39008
6	RCR05G624JS	1	RESISTOR, 620K, 1/8W, 5%, R13		MIL-R-39008
7	RCR05G[illegible]JS	1	RESISTOR, SEL, 1/8W, 5%, R14		MIL-R-39008
8	M116	1	TRANSISTOR, M CHANNEL MOSFET, Q1		NO DRAWING
9	MEM511	4	TRANSISTOR P CHANNEL MOSFET, Q2, Q5, Q6, Q7		NO DRAWING
9A	RCR05G101JS	1	RESISTOR, 100, 1/8W, 5%, R7		MIL-R-39008
10	2N5308	1	TRANSISTOR, DARLINGTON, NPN, Q4		NO DRAWING
11	SK5020862	1	INTEGRATED CIRCUIT, CMOS, CUSTOM, IC1		CONTRACT # DAAG39-76-C-0098
12	NOM 401	1	INTEGRATED CIRCUIT, MNOS, IC2		NO DRAWING
13	CD4050BK/3	1	INTEGRATED CIRCUIT, CMOS, IC3, IC4, IC5		NO DRAWING
14	CD4040AK/3	1	INTEGRATED CIRCUIT, CMOS, IC6		NO DRAWING
15	JANIN3611	10	DIODE, SILICON CR1, CR2, CR3, CR4, CR5, CR6, CR7, CR8, CR10, CR11, CR12		NO DRAWING
16	PD6059	1	DIODE, ZENER, 15V, CR9		NO DRAWING
17	GN15A[illegible]K	1	CAPACITOR, CERAMIC, SEL, 100V, C1		NO DRAWING
18	MZG-020-685	1	CAPACITOR, TANTALUM, 6.8μF, 20V, C2		NO DRAWING
19	C31C124K	1	CAPACITOR, CERAMIC, 12μF, 50V, C3		NO DRAWING
20	CN15A[illegible]K	1	CAPACITOR, CERAMIC, TBD, 100V, C4		NO DRAWING
21	C31C333K	2	CAPACITOR, CERAMIC, .033μF, 50V, C5, C6		NO DRAWING
22	CN15A101K	1	CAPACITOR, CERAMIC, 100pF NPO, 100V, C7		NO DRAWING
23	C31C473K	1	CAPACITOR, CERAMIC, .068μF, 50V, C8		NO DRAWING

Figure 19. Parts list for function setter receiver.

3.3.2 Power and Signal Distribution

Referring to figure 17, the signal from the coil is immediately rectified by a diode bridge consisting of CR1 through CR4. As the signal modulation begins, the peak detector made up of a CR7, R5, and C4 envelope detects the waveform, and it is then processed by the control circuitry.

The network made up of CR6, R3, R4, and C3 is a delay circuit. As power comes up, the network delays the voltage and then feeds it to the UA. It is used for generating internal power on a reset pulse. R15 is a current limiting resistor that prevents the UA

from being burned out when power is shut off. Burnout is possible since the C3 discharge time is longer than the power source (C2) discharge time.

A transistor, Q4, is used as a switch for the reverse link. It is a Darlington device to reduce drive requirements.

Upon firing, the timer battery turns on in approximately 200 ms. The battery voltage reverse biases the bridge and turns it off. Thus, the coil is effectively open circuited for any noise spikes up to the battery voltage (~20 V), minimizing the effect of the FFS coil on the gyroscope coils. The battery voltage also charges C2 through CR11 and R7 and is used to indicate in-flight conditions ("BATT") to the control circuitry.

The power consumed by the receiver must be kept to a minimum during the programming phase since it must be provided through the inductive link. The total current available at 15 V is 200 μA. This was rationed by allowing 100 μA to the UA and 100 μA to the remaining circuitry. Resistor values are, therefore, as high as possible to reduce quiescent current drain. The Plessey NOM 401 MNOS memory was chosen because it was the only MNOS memory whose current drain could be controlled and kept low.

3.3.3 Control Circuitry

Most of the control circuitry is located on the UA (fig. 20). The only off-chip components are the CD4040 12-stage divider and some tuning components. The operation of the control circuitry may be divided into four phases. In the forward link phase, data are received from the SU and stored in memory. In the reverse link phase, data are read out of memory and retransmitted to the SU. In the in-flight read-out phase, when the battery is on, data are read out of memory. In the count phase, the time delay is generated.

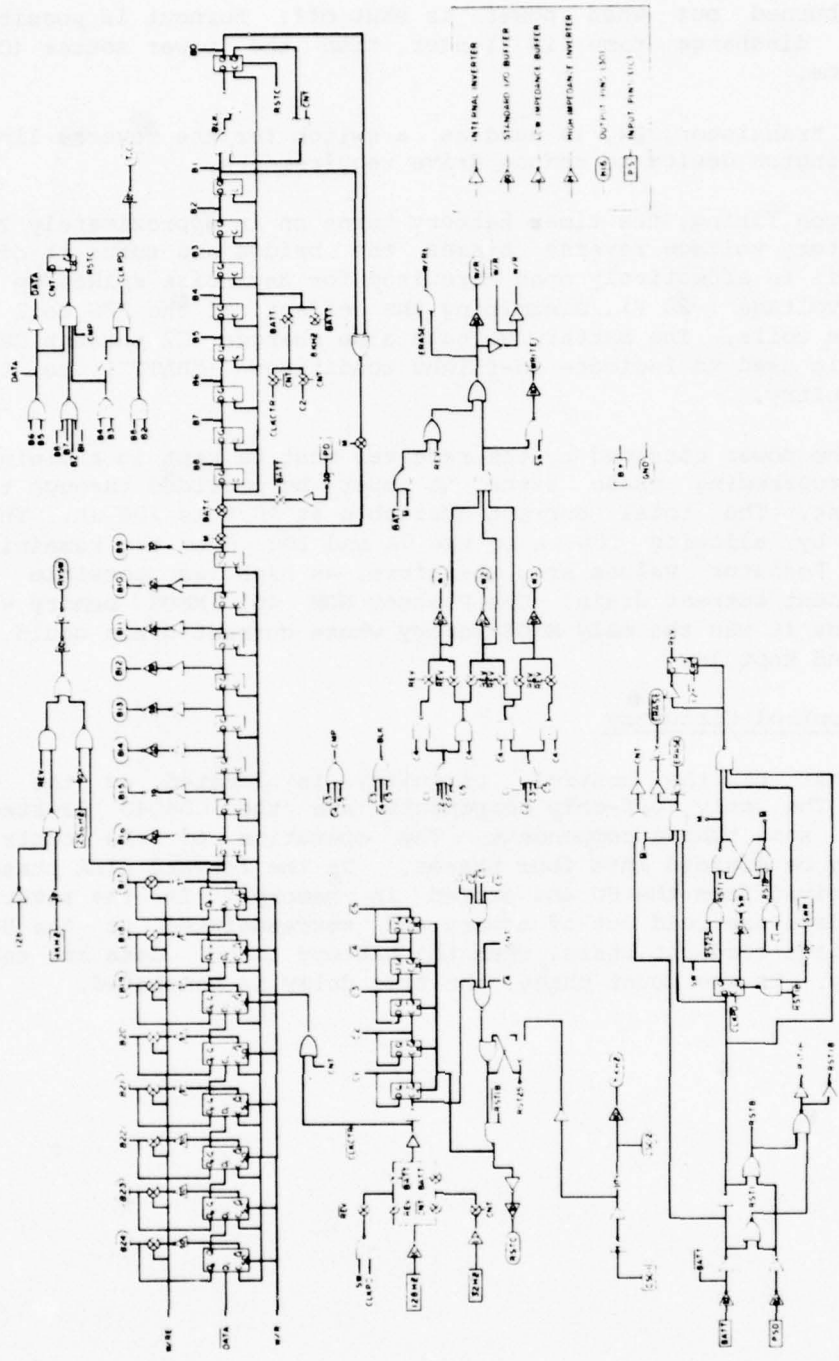


Figure 20. Schematic diagram of universal array.

The signals generated and used by the control circuitry during operation are listed below.

BATT	Signal that is high if battery is on, used to determine when circuit should be in flight modes
BLK	Signal used to blank carryover during CNT mode
CLKCTR	Signal that clocks C-counter
CLKPD	Output from demodulator when pulse-width-modulated signal is at least long enough to be "0"; used to clock demodulated data into buffer shift register (SR) (B17 to B24)
CMP	Signal used to define point at which timer counter contents are compared for final value
CNT	Signal that is high when circuit is in counting mode, that is, generating preprogrammed time delay
DATA	Demodulator output when pulse-width-modulated signal is long enough to be "1"; clocked into B24 by CLKPD
ERASE	Signal that erases entire memory
M	Signal that goes high on first data pulse and low at end of reverse message, to define mode of operation
OSC-1, OSC-2	Connections for timing components for internal oscillator OSC-2
PD	Peak detected signal from coil containing pulse-width-modulated data
PSD	Delayed power-up signal used for power on reset
REV	Signal that is high when circuit is in reverse link mode
RSTB	Reset signal generated when battery voltage rises
RSTC	RSTIB plus RST25
RSTI	Reset signal generated with FFS in programming mode
RSTIB	RSTI plus RSTB

RST25 Reset signal generated when bit counter (C-counter) counts to 25

RVSW Signal consisting of 4-kHz bursts, pulse width modulated to indicate "0" or "1"; drives transistor switch across coil

SW Monostable pulse initiated by first received pulse; reverse link sequence begins automatically at conclusion of pulse

SWR Reset line for SW; R-C combination connected here determines monostable pulse width

T.O. Time-out pulse generated at end of time delay

WRITE Signal used to initiate operation of writing into memory

W/R Programming signal that puts memory in write (high) or read (low) mode

W/RE Same signal as W/R, but also going low during ERASE signal

W1,W2,W3 Programming signals for memory section, defining which of three 8-bit words is being read or written

32HZ,128HZ 256HZ,4KHZ Clock signals derived from 8.192-kHz oscillator signal by division using off-chip 12-stage counter

8KHZ Oscillator output whose nominal frequency is 8.192 kHz.

Referring to the above list of signals, the schematic of figure 20, and the timing diagram of figure 21, one may follow the operation of the circuit.

Forward link phase.--As power comes up, RSTI goes high and resets all the circuitry. When PSD goes high, RSTI returns to 0. The circuit is now initialized, and the oscillator consisting of elements A1 through A4 is running at 8.192 kHz (8 kHZ). In this mode, shift register cells B1 through B8 and gates G5 through G9 form a demodulator. The signal PD, which is the pulse-width-modulated envelope of the carrier frequency, is clocked into the SR at an 8-kHz rate. Since the data rate of PD is 1 kHz, the data cells of PD are

"chopped" into about eight pieces. Therefore, by inspecting SR for a given number of 0's in a row, a "0" or "1" bit can be decoded by gates G5 through G9. The decoding logic is summarized in figure 22. When the first data pulse is detected, SW is initiated on the trailing edge. At the conclusion of SW, the reverse link phase automatically begins, regardless of the number of bits received. This beginning assures that the circuit cannot hang up on just one pulse. When SW goes high, ERASE also goes high and erases the memory. During the ERASE pulse, W/RE goes low and opens ports B24 through B17 to prevent their reverse overdriving. M then goes high on the leading edge of the next data pulse and causes ERASE to go low again. Data from the demodulator is now stored in SR cells B24 through B17. As bits are entered into B24, they are counted by the C-counter (C1 through C5). The state of the C-counter is decoded by gates G20 through G25, and, after every 8 data bits, the proper memory programming signals are generated to write the data into memory (that is, W1, W2, W3, WRITE). After 25 bits are counted (B0 is skipped), the C-counter automatically resets itself, and nothing happens until SW comes down.

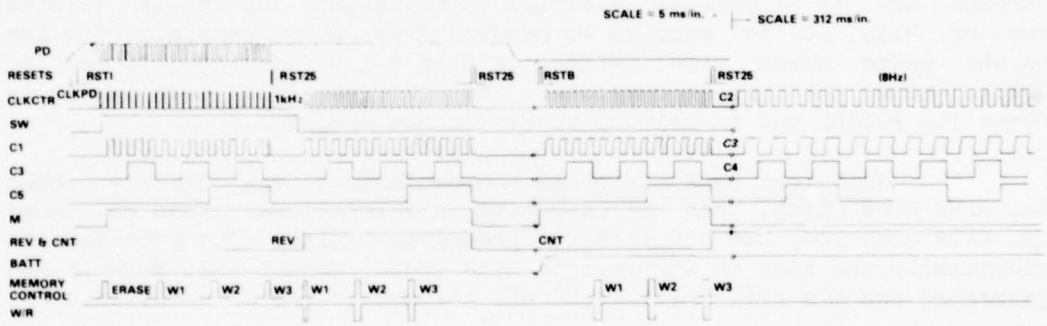


Figure 21. Timing diagram of function setter receiver.

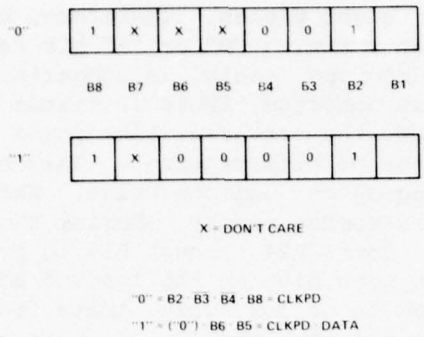


Figure 22. Demodulator logic.

Reverse link phase.--When SW comes down, REV goes high on the next 128-Hz negative edge. The C-counter is clocked by 128 Hz, and gates G20 through G25 generate the proper memory programming pulses (W1, W2, W3) before each 8-bit shift cycle. Signals W/R and WRITE also are generated.

After each 8-bit word is shifted in parallel into B24 through B17, it is shifted in serial to the right. As it is shifted out of B17, it is encoded to produce RVSW, which consists of 4-kHz bursts whose burst time defines a 0 or a 1 as described in section 3.1.2. After the circuit completes the reverse link message, it is reset (by RST25) and is able to receive a new message.

In-flight read-out phase.--Upon firing, the battery comes up, RSTB goes high, and the circuitry is initialized. When PSD comes up, RSTB goes low, and the read-out procedure begins. The procedure is essentially the same as the reverse link phase, except that RVSW is not generated and the data are shifted all the way to the B1 position.

Count phase.--At the end of the read-out cycle, the time delay desired (in seconds) is located in positions B1 through B8. If this number is decremented once each second down to 0, the time delay will have been generated. The best way to minimize the circuitry is to decrement the numbers serially. Decrementing by 1 is equivalent to adding the complement of 1 and blanking the final carryover. Since the complement of 1 is 11111111, decrementing by 1 can be done easily by serially adding a 1 to each position, storing the result, and generating a carryover. This process can be done dynamically by shifting B1 through B8 to the right at an 8-Hz rate. The output of G46 is equivalent to the sum of B1 plus the previous carryover (B0) plus 1 (from the complement) and is shifted back into B8. The present

carryover is generated by G43 and G44 and stored in B0. Every eighth carryover is blanked by BLK to prevent carrying an MSB into the LSB of the next 8-bit number. Since the operation is performed at 8 Hz, a complete addition (actually a decrement) is accomplished every 1 s.

The desired time delay is generated at the end of an addition when B1 through B8 is 0. Unfortunately, since the battery rise time and the read-out phase delay the beginning of the counting process, sensing 0 would be too late. Therefore, the contents of the SR are inspected 500 ms before the end of addition (by CMP). The end of the time delay is sensed at 0 minus 500 ms. When the end of the delay is sensed by G10, the signal T.O. is triggered.

3.3.4 Memory

The internal structure of the MNOS memory is shown in figure 23. All of the MNOS transistors, which are P-channel devices, must be erased before the memory can be programmed. They are erased by applying a positive 30-V pulse to the gates (W1 through W8) with respect to the substrate (0 V). This application shifts the turn-on threshold of the MNOS transistors to approximately 3 V. Writing is performed by putting 15 V on those bits where a 0 is to be stored, holding the others to ground, and then applying a -30 V pulse on the desired word line with respect to the substrate. This application shifts the turn-on threshold of the grounded devices to approximately 10 V. Reading is performed by applying 15 V to terminal R, which turns on the lower row of field-effect transistors (FET's) and enables the read operation. A 15-V signal also is required on terminal $-V_{GG}$. This turns on the upper row of FET's, which act as load resistors. The memory is now read by applying a "read" voltage ($\sim$7 V), chosen to fall between the two possible thresholds, to all the gates of a selected word. Those devices with a threshold of 3 V do not turn on, so 0 V results on the corresponding B terminal. Those devices with a threshold of 10 V turn on, and 15 V results on the corresponding B terminal.

All of the programming signals are generated from the UA and are either used directly or altered through special drive circuits. The operation of the drive circuitry and the memory during the erase, write, and read phases can be described as follows:

Erase.--Referring to the schematic of figure 17 and the timing diagram of figure 24, since FET's Q5, Q6, and Q7 are P-channel devices, they are normally on. Their common drain is held at 15 V through diode CR10. When ERASE is generated by the UA, it pulls 0V (the substrate) on the memory low. ERASE, meanwhile, couples through C5 and superimposes a 15-V pulse onto the existing 15 V on the FET drain. The resulting 30-V pulse drives W1, W2, and W3 through Q5, Q6, and Q7 and thus erases the memory.

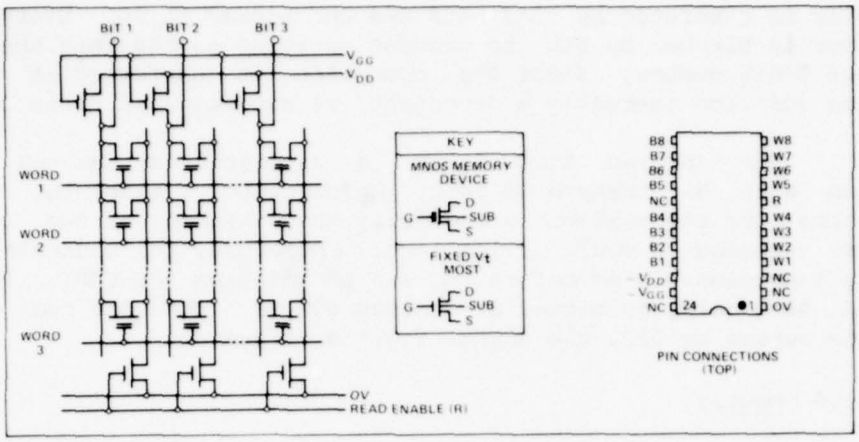


Figure 23. Metal nitride oxide semiconductor memory integrated circuit.

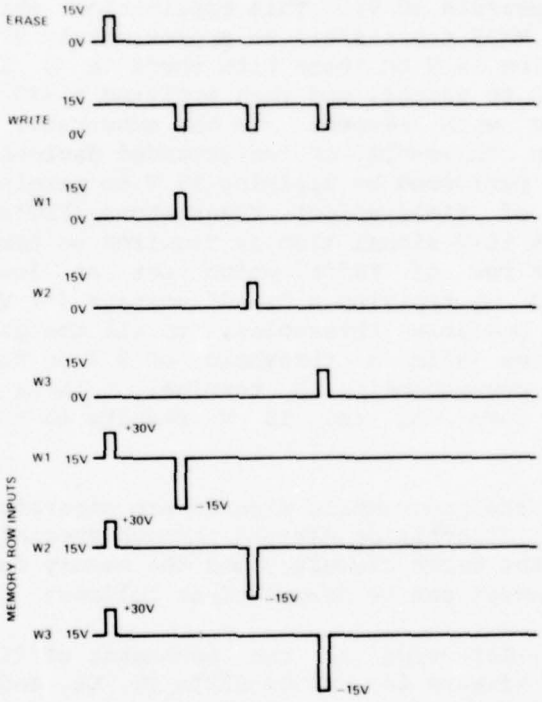


Figure 24. Memory erase-write timing.

Write.--Again Q5, Q6, and Q7 are normally on, and terminal 0V is at 15 V. An internal gate protection diode clamps the gate of Q1 to ground. A WRITE pulse (negative) couples through C6 and drops the gate of Q1 to -15 V; this turns Q1 on, and the -15 V pulse is coupled to the bottom of R9, R10, and R11. Meanwhile, Q5, Q6, or Q7 has been turned off by W1, W2, or W3, depending on the word being written. The -15-V pulse then drives the word line corresponding to the off FET. The other word lines are held to 15 V by the on FET. Thus, the selected word line is 30 V less than 0V, and the MNOS devices are programmed.

Read.--Referring to figure 25, reading is initiated when W/R goes low, turning Q2 on. In addition, Q5, Q6, or Q7 is turned off by W1, W2, or W3. The voltage on the drain of Q2 goes to that determined by the voltage divider formed by R12 and two of the resistors R9 to R11, which is approximately 7 V. This is coupled through a 1-MΩ resistor to the word line corresponding to the off FET. The data are now available on the control circuitry.

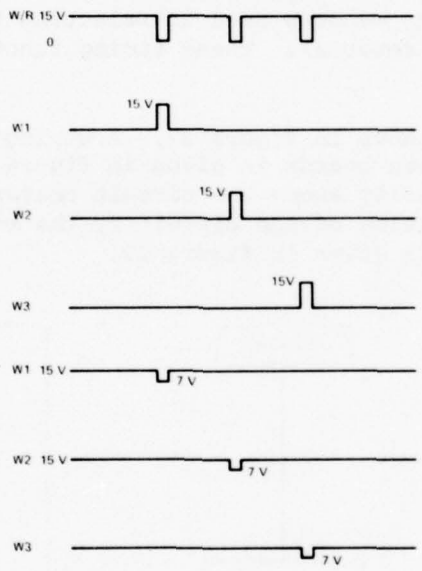


Figure 25. Memory read timing.

3.4 Setter Unit

3.4.1 General

A block diagram of the SU is shown in figure 26. The signal from the fire control system (or the DEU) is buffered and directed to the control circuit's forward link pulse shaping network, where it is detected as a "1" or a "0." The data bits are then used to generate a data gate, which keys the 100-kHz oscillator on and off. This gating is done on the demodulator board.

The return signal picked up by the coil is processed on the demodulator board, where it is phase detected, filtered, and amplified. Output from the demodulator is then detected as a "1" or a "0" by the reverse pulse shaping circuitry and then sent back to the fire control system through the interface board.

As the information is flowing from the fire control system to the projectile and back again, the control circuitry is generating the time delay and the windows used in selecting the circuit's mode of operation (forward or reverse). These timing functions are detailed in section 3.1.2.

The SU is shown in figure 27. A wiring diagram showing the interconnections between boards is given in figure 28. The electronics are divided functionally among the circuit boards, so it is desirable to describe the operation of the circuit by the boards. A parts list for the SU schematic is given in figure 29.

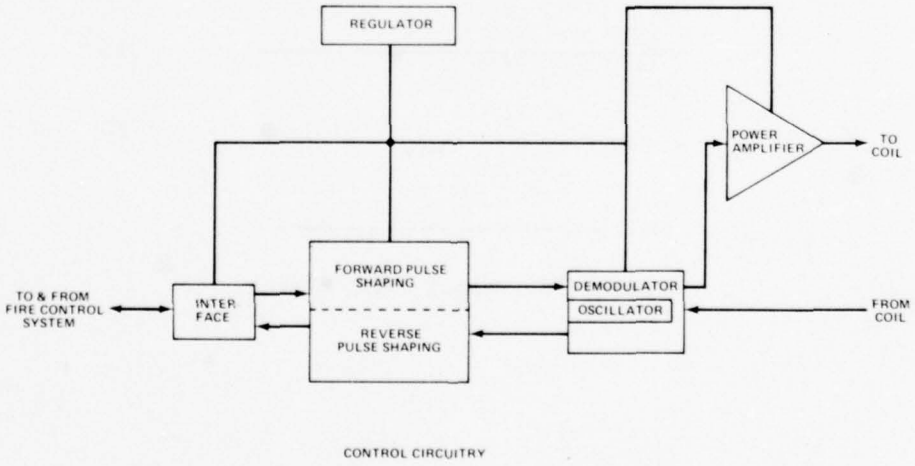


Figure 26. Block diagram of setter unit.

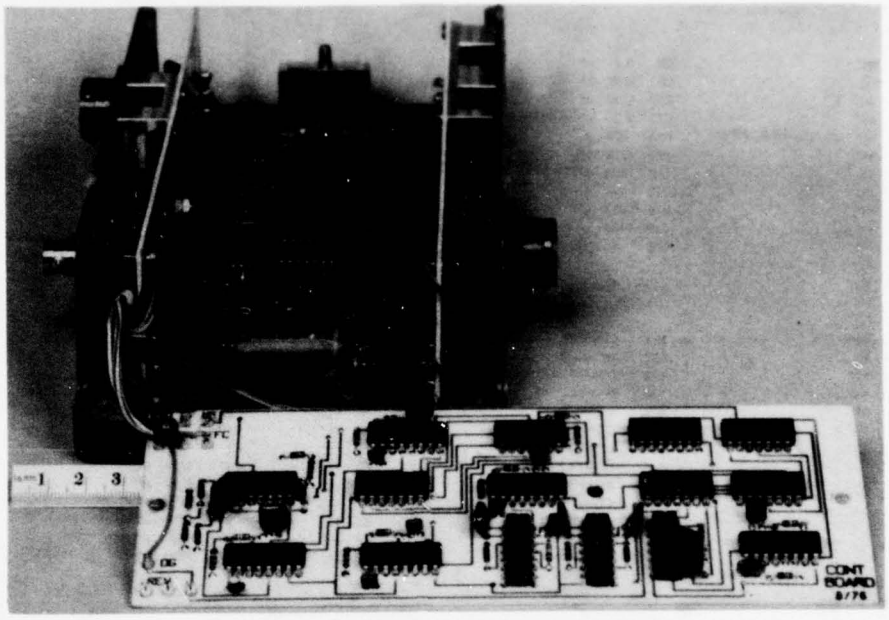


Figure 27. Setter unit.

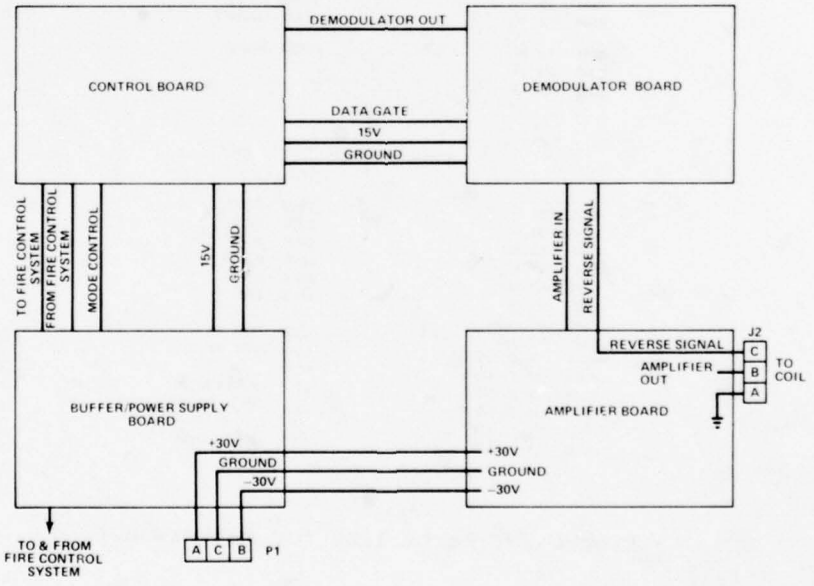


Figure 28. Wiring diagram of setter unit.

CONTROL BOARD

R1	1.2	MΩ
R2	2.7	kΩ
R3	100	kΩ
R4	240	kΩ
R5	180	kΩ (160 kΩ ON BOARD)
R6	1	MΩ
R7	750	kΩ
R8	560	kΩ
R9	10	kΩ
R10	390	kΩ
R11	10	kΩ
R12	10	kΩ
R13	100	kΩ
R14	10	kΩ
R15	100	kΩ
R16	270	kΩ
R17	220	kΩ
R18	1.0	MΩ
R19	620	kΩ
R20	10	kΩ
R21	2.7	MΩ
R22	2.7	MΩ

C1	6800	pF
C2	0.01	μF
C3	0.01	μF
C4	0.01	μF
C5	0.1	μF
C6	0.01	μF
C7	1200	pF
C8	0.1	μF
C9	1200	pF
C10	1200	pF
C11	2.2	μF, TANTALUM
C12	820	pF
C13	1200	pF
C14	1200	pF
C15	470	pF
C16	0.033	μF
C17	1200	pF
C18	10	μF, TANTALUM

CR1	1N4005

1C1	CD4093B
1C2	MC14528
1C3	CD4013
1C4	MC14528
1C5	MC14528
1C6	CD4071B
1C7	CD4081B
1C8	CD4016A
1C9	MC14528
1C10	CD4013A
1C11	CD4017A
1C12	MC14528
1C13	MC14528
1C14	CD4093B
1C15	MC14528

DEMODULATOR BOARD

R101	10	kΩ
R102	9.1	kΩ
R103	9.1	kΩ
R104	100	kΩ
R105	1	kΩ
R106	1	kΩ
R107	1	kΩ
R108	2	kΩ
R109	2	kΩ
R110	100	kΩ
R111	3.3	kΩ
R112	3.3	kΩ
R113	3.3	kΩ
R114	3.3	kΩ
R115	20	kΩ
R116	1.0	MΩ
R117	30	kΩ
R118	10	kΩ
R119	10	kΩ
R120	10	kΩ
R121	10	kΩ
R122	10	kΩ
R123	10	kΩ
R124	3.3	kΩ
R125	62	kΩ
R126	10	kΩ
R127	10	kΩ
R128	2.0	kΩ
R129	10	kΩ
R130	2	kΩ
R131	20	kΩ
R132	2	kΩ
R133	100	kΩ, 1W
R134	2.0	kΩ
R135	20	kΩ
R136	100	kΩ
R137	1.0	kΩ

C101	2200	pF
C102	2200	pF
C103	0.1	μF
C104	2200	pF
C105	2200	pF
C106	2200	pF
C107	2200	pF
C108	2200	pF
C109	2200	pF
C110	4700	pF
C111	4700	pF
C112	4700	pF
C113	4700	pF
C114	4700	pF
C115	4700	pF
C116	6800	pF
C117	4700	pF
C118	2.2	μF
C119	0.1	μF
C120	0.1	μF
C121	2.2	μF
C123	2.2	μF
C124	2.2	μF

CR101	1N4154
CR102	1N4154
CR103	1N4154
CR104	1N4154
CR105	1N4154

IC102	CD4030AE
IC103	CD4013AE
IC104	CD4024AE
IC105	MC1458
IC106	MC1458
IC107	MC1458
IC108	MC1458
IC109	MC1458

Q101	2N3904
Q102	2N2924

XTAL OSC 3.2 MH

BUFFER/POWER SUPPLY BOARD

R201	2.7	kΩ
R202	10	kΩ
R203	10	kΩ
R204	3.3	kΩ

C201	2.2	μF
C202	2.2	μF
C203	2.2	μF

Q1	MC7815C

1C201	CD4016A
1C202	CD4049B

CR201	IN4744

AMPLIFIER BOARD

R301	100	Ω
R301A	100	Ω
R302	3.3	kΩ
R303	4.7	kΩ
R304	100	Ω
R305	270	Ω
R306	100	Ω
R307	4.7	kΩ
R308	15	Ω, 1/2 W
R309	39	Ω, 1/2 W
R310	39	Ω, 1/2 W
R311	15	Ω, 1/2 W
R312	0.4	Ω, 1 W
R313	0.4	Ω, 1 W

Q301	D44C8
302	D45C8
Q303	D44C8
Q304	D45C8
Q305	D44C8
Q306	D45C8

C301	0.47	μF
C302	0.47	μF

J1	PTO7A-12-3P
J2	PTO7A-12-3S

P1	BNC UG2901

Figure 29. Parts list for setter unit.

3.4.2 Interface Board

The interface board schematic is shown in figure 30. Signals to or from the fire control system are steered by transmission gates TG201 and TG 202. TG201 and TG202 are controlled by the mode control signal, MC. If MC is high, indicating the forward mode, TG201 is closed to allow the signal to pass from the fire control system to the control circuit, while TG202 is open. If MC is low, indicating the reverse mode, TG201 is open while TG202 is short-circuited and passes the reverse signal (TFC) to the output (see p. 40 for fig. 30).

I2 and I3 are inverting buffers, and I1 generates MC for use by TG202. In addition to the buffers and the switches, the board contains the 15-V regulator, which supplies power to the control, demodulator, and amplifier boards. Zener diode CR201 is used to generate 12 V for use by the buffer circuits, which is the voltage used between the DEU and the SU.

3.4.3 Control Board

The control board schematic is shown in figure 31. Signals coming from the fire control system (FFC) via the interface board are integrated by R15 and C12 to increase noise immunity. The signal is then squared by the Schmidt trigger gate, G8, and immediately triggers the monostable multivibrator, MS10. It is also applied to the D input of FF2. When the 375-ms pulse generated by MS10 ends, it triggers FF2, MS11, and MS12. The monostable multivibrators generate pulses corresponding to a "0" and a "1," respectively. If the output of G8 is still high, Q of FF2 goes high to indicate that the input pulse was longer than 375 ms and therefore a "1." If it is low, Q of FF2 is used to select either a "0" from MS11 or a "1" from MS12 by controlling transmission gates TG3 and TG4. A detected and then reshaped signal is then available at the ouput of G9.

The first "1" detected is used also to index the Johnson counter, C1, and set flip-flop FF3, driving G11 high, since G10 is high. The output of G11, DG, is the signal that gates the 100-kHz clock into the amplifier. Thus, the first pulse turns on the amplifier. The second "1" received (B0) indexes C1, again enabling G10. Data from G9 (including B0) now pass through G10 to G11 and on to gating the amplifier.

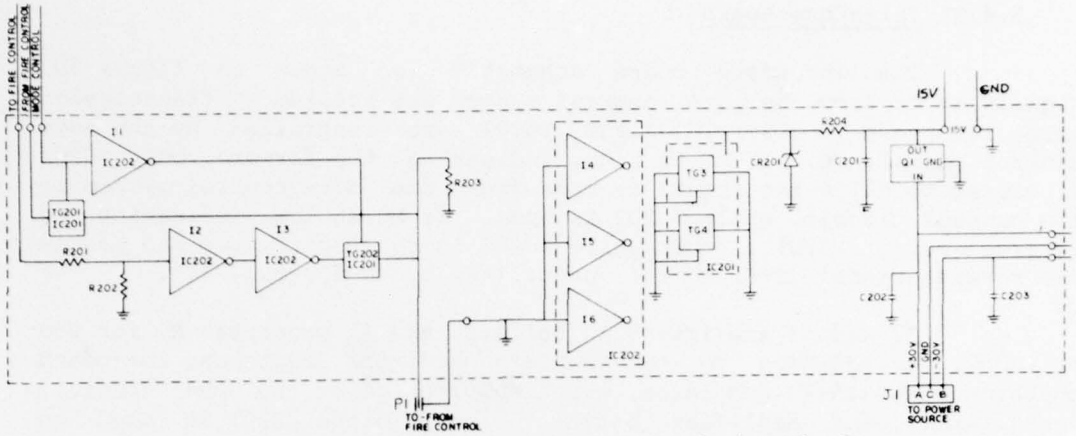


Figure 30. Interface buffer/power supply board of setter unit.

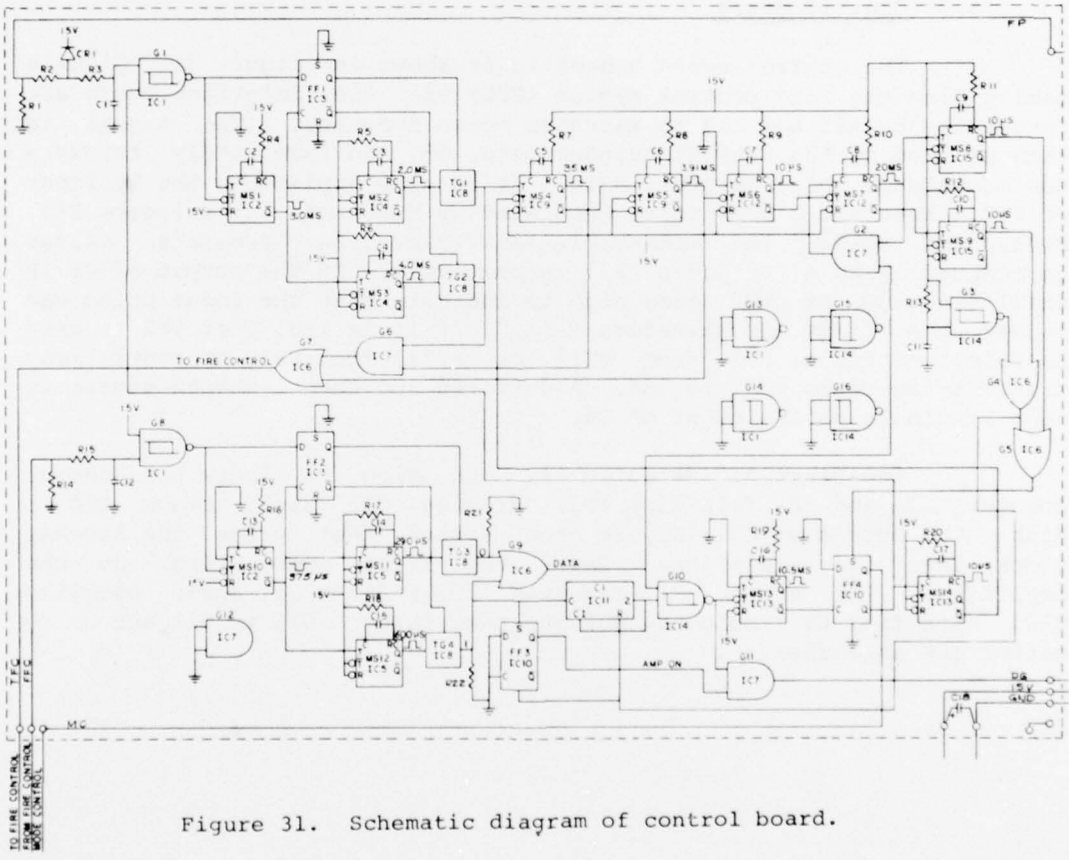


Figure 31. Schematic diagram of control board.

The output of FF4 is MC. After each data pulse, MS13 is retriggered and, if it runs out, clocks FF4 to the reverse state (Q = low). This action switches the circuitry to the reverse mode. The output line on the interface board is now connected to TFC, and data from the demodulator are enabled to pass through gate G1. The data are detected and reshaped as were the forward link data by using MS1, MS2, MS3, FF1, TG1, TG2, and the appropriate time constants for the reverse link. After FF4 goes high (via MS14) and after each data pulse, MS4 is triggered. If data are not received within the 35-ms pulse generated by this monostable multivibrator, reverse data are blocked from passing through G6, and a "1" is generated by MS5 while being transmitted to the fire control system. After the "1" is sent, another 20-ms pulse is triggered (MS7), which keeps the data gate high (and, therefore, the amplifier on). If forward data do not arrive within this 20-ms window, a reset pulse (MS9) resets C1 and FF3. This setting requires that the setting cycle begin with a power-on pulse if more data are desired to be sent. If forward data arrive before the 20-ms delay runs out, they are retriggered, and C1 and FF3 are not reset. This means that the setting cycle need not begin with the power-on pulse, but can begin with B0, thus saving 500-ms charge-up time.

3.4.4 Amplifier Board

A schematic of the amplifier board is shown in figure 32. The AMP IN signal, which is the modulated 100-kHz signal, is buffered by the push-pull emitter follower circuit consisting of Q301 and Q302. The signal is then transformer coupled to the driver and output network, which operates from -30 to +30 V (see p. 42 for fig. 32).

All the transistors in the amplifier are switched--none of them operate in the linear region. This switching greatly reduces the power that must be dissipated since the transistors are either fully saturated or off. The resultant square-wave output is effectively filtered by the L-C load so that the waveform across the coil is sinusoidal. The amplifier produces about 6 A_{p-p} into the load.

3.4.5 Demodulator Board

The demodulator board schematic is shown in figure 33. This schematic is best understood by referring to the block diagram of figure 34. FF101 and FF102 form a gate that not only gates the crystal oscillator, but synchronizes the gating frequency with the 100-kHz signal. The resultant signal (AMP IN) drives the amplifier. It also acts as the local reference frequency for the phase detector made up of G105, G106, and G107. The phase detector senses phase changes in REV with respect to the reference signal. (The operator should be cautious because REV can be up to 600 V_{p-p}.)

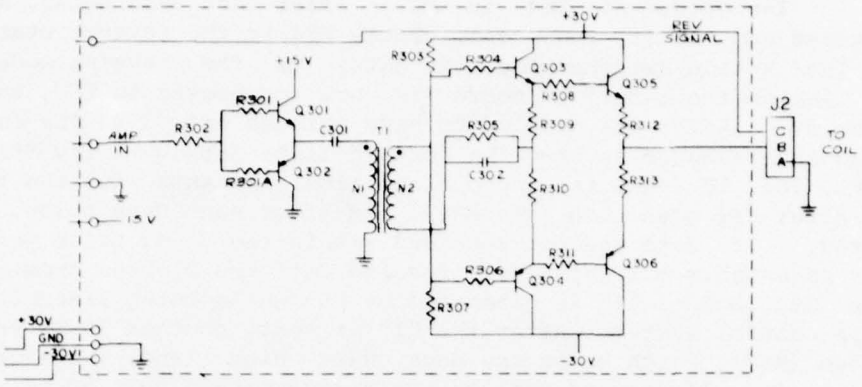


Figure 32. Schematic diagram of amplifier board.

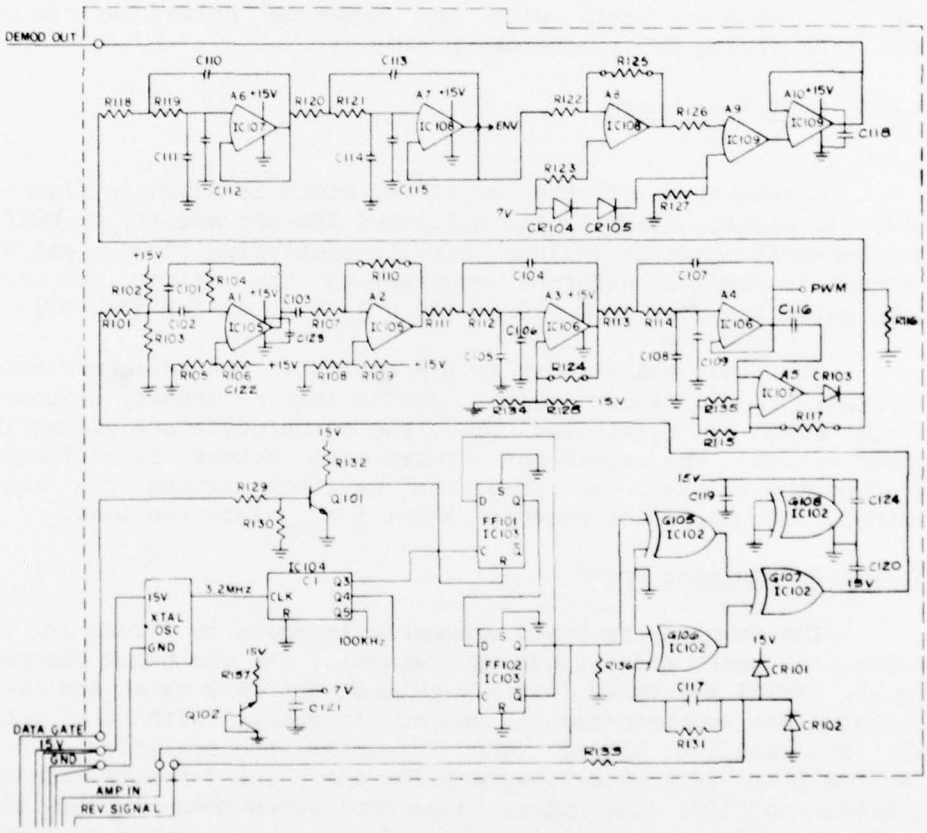
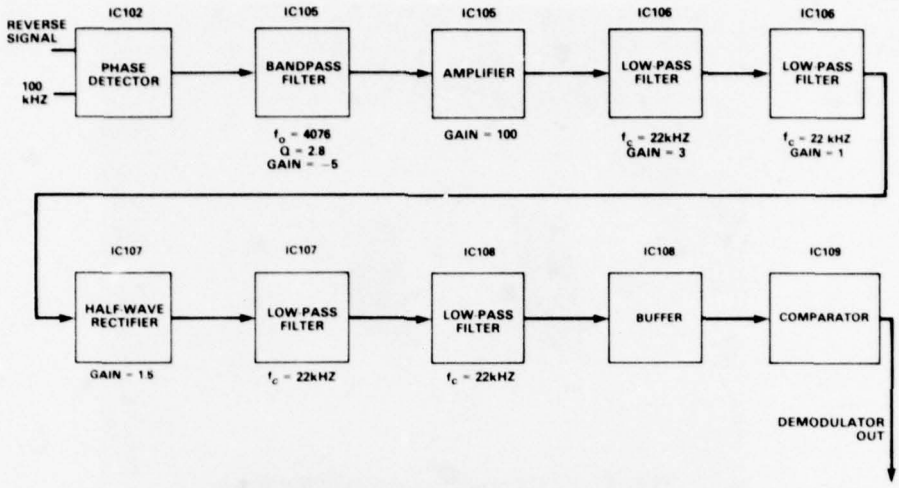


Figure 33. Schematic diagram of demodulator board.



Pigure 34. Block diagram of demodulator board.

REV is clipped by CR101 and CR102 before phase detection. After phase detection, the signal is bandpass filtered, amplified, and low-pass filtered. At this point, the waveform is a series of 4-kHz sinusoidal bursts. This series is then rectified, and the 4-kHz component is removed by filtering. This signal drives the threshold detector and, finally, the comparator. The result is a series of 15-V square-wave pulses whose widths correspond to "0" or "1."

3.5 Data Entry Unit

To properly test the FFS system, it was necessary to design and build a DEU (fig. 35) through which data could be manually entered into the system. It would format the data before sending them to the SU and also would check the accuracy of the returned data. If the data were accurate, they would light a GO or NO-GO light.

The top set of thumbwheel switches is for entering the desired time delay (bits B1 through B8) in tenths of a second. Below them is a row of toggle switches for individually entering bits B9, B10, B12, and B13. The bottom row of thumbwheel switches is a means of entering the remaining bits by encoding them and entering the actual number. The encoding scheme is summarized in figure 36.

Each unit is powered by 110-V, 60-Hz power. The desired data are entered, and the send button is pushed. The panel data are encoded and sent to the SU. When the reverse data come back, they are checked, and the appropriate GO or NO-GO light is lit.

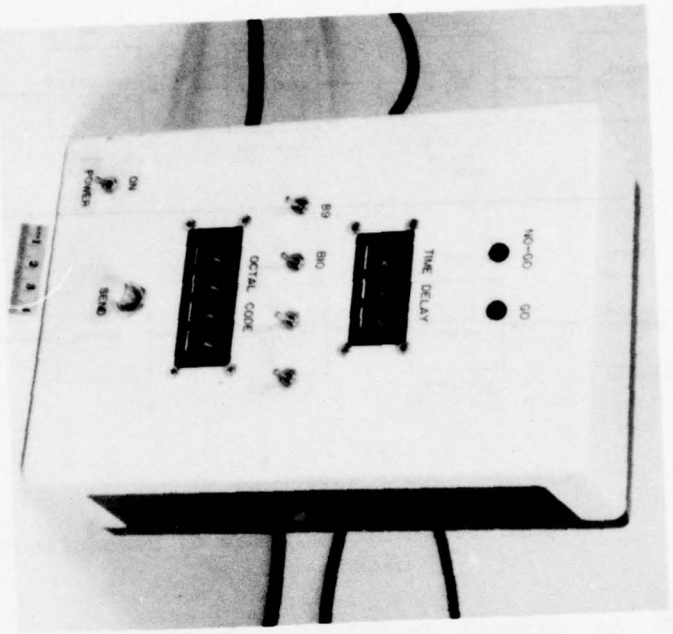
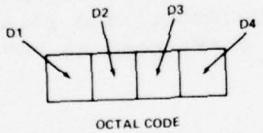


Figure 35. Data entry unit.



THUMBWHEEL DIGIT	OCTAL BIT	BIT ASSIGNMENT	OCTAL EXAMPLE OF 1533
D1	1	B11	1
D1	2	B14	0
D1	4	B15	0
D2	1	B16	1
D2	2	B17	0
D2	4	B18	1
D3	1	B19	1
D3	2	B20	1
D3	4	B21	0
D4	1	B22	1
D4	2	B23	1
D4	4	B24	0

Figure 36. Octal code for data entry unit.

3.6 Power Supply

The power supply built for the system (fig. 37) consists of two commercial power supplies, one for +28 V and the other for -28 V. They are Deltron model No. 28V-4.2A and can supply 4.2 A at 28 V. Although they exhibit some ripple at 100 kHz, this does not disturb the operation of the circuit.

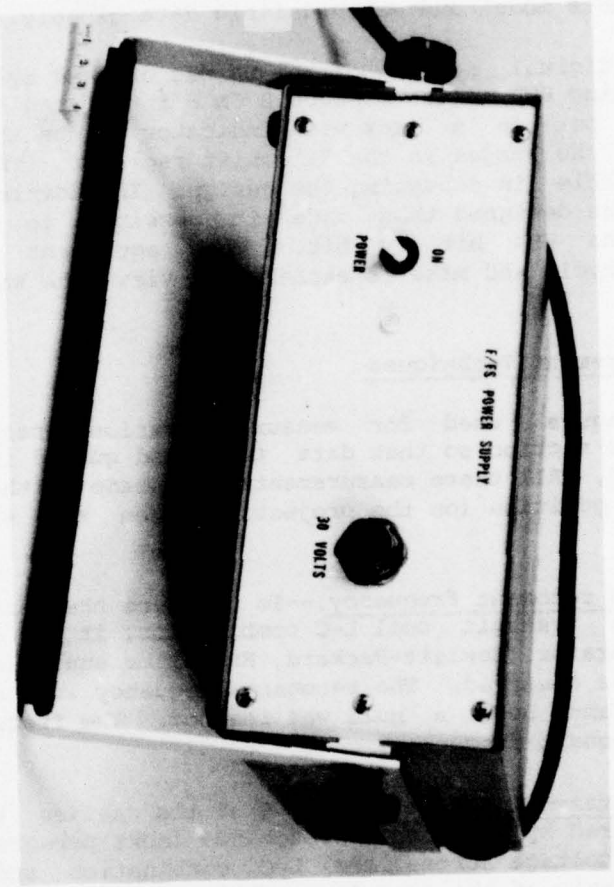


Figure 37. Power supply for fuze function setter system.

4. TESTING

4.1 Laboratory Tests

4.1.1 Laboratory Equipment

To perform laboratory testing and design, it was necessary to model the projectile and transmit coil geometry. Figure 1 shows the laboratory model used. Later actual gun-mount testing confirmed that it was a reasonable model and matched field data closely.

The digital design of the UA was checked by breadboarding the design by using RCA series CD4000A,B CMOS integrated circuits. The breadboard was put in a rack with indicator lights that showed the state of each of the stages in the "B" shift register. This indication proved very valuable in debugging the design. In addition, a piece of test equipment was designed that made it possible to exercise and troubleshoot the FSR bit by bit. The equipment also could automatically recycle and make it easier to view the waveforms on an oscilloscope.

4.1.2 Measurement Techniques

Techniques used for measuring various parameters are described in this section so that data taken and quoted in this report may be duplicated. All these measurements were made with the device under test in position (on the projectile or on the simulated FFS face).

Series resonant frequency.--To measure the series resonant frequency of the transmit coil L-C combination, it was driven with a 600-Ω signal generator (Hewlett-Packard, HP 651 or equivalent), and the driving signal was observed. The resonant frequency was determined by varying the frequency until a null was reached. The frequency at this point was the resonant frequency.

Q of transmit coil circuit.--Q of the series L-C transmit circuit was measured by tuning to resonance (next paragraph) and then by measuring the voltage across the L-C combination and across the capacitor. The ratio of the capacitor voltage to the total voltage was Q of the circuit.

Resonance for secondary coil circuit.--The resonant frequency of the secondary coil parallel L-C circuit was measured by inserting a 50-kΩ resistor in series with the circuit and driving it with a signal generator (HP 651D or equivalent). If the frequency was varied, a peak voltage was observed at the resonant frequency.

Q of secondary coil circuit.--Q was measured by connecting the secondary circuit (L-C) directly to an oscilloscope. A 50-Ω resistor attached to the end of a cable as shown in figure 38 was driven by a signal generator (HP 651D or equivalent). The resistor was held near the projectile so that energy was coupled into the secondary coil by induction. By varying the drive frequency, it was determined at which frequencies above and below the resonant frequency the oscilloscope voltage dropped to 0.7 of the peak voltage. The difference between these frequencies divided by the resonant frequency was Q.

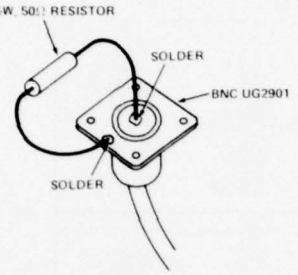


Figure 38. Q measurement probe.

Coupling coefficient.--The measurement of the coefficient of coupling, K, was based on the formula

$$K = \left(K_1 K_2\right)^{\frac{1}{2}} ,$$

where K_1 is the voltage transfer ratio of the secondary coil voltage to the primary coil voltage when driving the primary coil and measuring the secondary coil open-circuit voltage. K_2 is the voltage transfer when driving the secondary coil. The measurement was made without tuning capacitors.

4.2 Gun-Mount Tests

Gun-mount tests were conducted on 10 June 1976 on the Mk 42 Mod 9 gun mount at the Naval Surface Weapons Center. The purpose of the test was to determine if there was any interference between the gun mount and the FFS and to verify the laboratory model.

To determine whether interference was present, the gun mount was cycled, and the FFS output (fig. 39) was monitored. The bursts were the reverse link message. There was very little difference in the output when the gun mount motors were on or off. In addition, the Hall effect switches on the mount were monitored, and none of them reacted during the operation of the inductive link.

Measurements of Q and K were made with the coils mounted as in normal operation. The results (fig. 13) indicated that the laboratory model was good and the simulation was realistic.

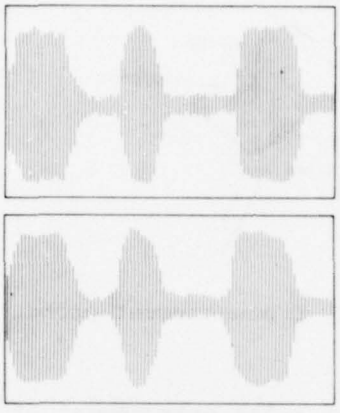


Figure 39. Gun-mount noise tests.

5. SPECIFICATIONS

The following specifications were used for the model:

Transmit coil

Turns: 25 turns, No. 22 AWG wire

Natural resonant frequency: > 0.15 MHz

Tuned resonant frequency: 100 kHz ± 1 percent (coil mounted on FFS face or equivalent)

Q: 10 to 12 (coil mounted on FFS face or equivalent)

Receive coil

Turns: 300 turns, No. 31 AWG wire

Natural resonant frequency: 150 to 200 kHz

Tuned resonant frequency: 100 kHz ± 1 percent (coil mounted in gyroscope inside projectile housing or equivalent)

Q: 5 to 7 (mounted in gyroscope inside projectile housing or equivalent)

Position: wound on gyroscope coil form within 3/8 in. (0.95 cm) from forward edge

Message

Forward: Data rate: 1 kHz ± 5 percent

"1" width: 0.5 ms ± 5 percent

"0" width: 0.25 ms ± 3 percent

Reverse: Data rate: 128 Hz ± 2 percent

"1" width: 3.90 ms ± 3 percent

"0" width: 1.95 ms ± 3 percent

Carrier frequency: 100 kHz ± 0.05 percent

Receiver

Operating voltage: 14.5 ± 0.5 V at 1 mA

Time delay accuracy: ±1 percent

Range: 1 to 256 s

Resolution: 1 s

Memory retention: 5 min

Bit assignment: classified

Transmitter

Current drive: 6 A_{p-p}

Field strength: to be determined

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