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GAAS FET DEVICE FABRICATION AND ION IMPLANTATION TECHNOLOGY (MI--ETC(U)
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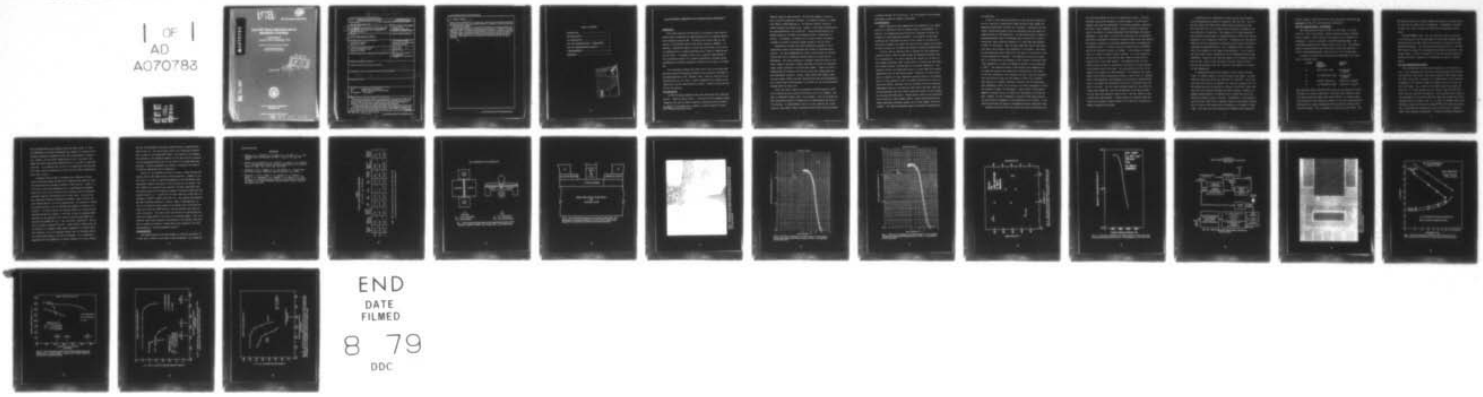

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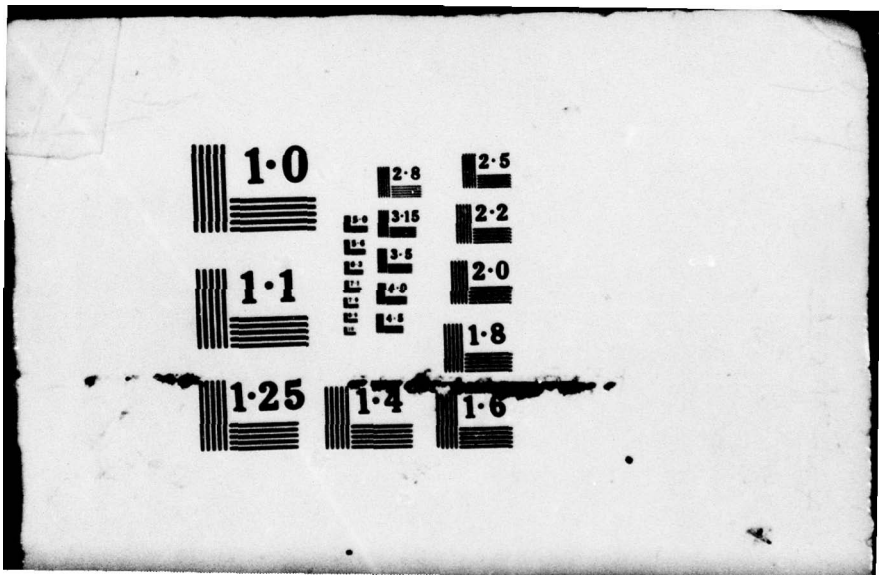
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NRL Memorandum Report 4020

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GaAs FET Device Fabrication and Ion Implantation Technology

Annual Report
1 October 1977–30 September 1978

KENNETH J. SLOBER AND HARRY B. DIETRICH

Solid State Devices Branch
Electronics Technology Division

June 27, 1979

NAVAL RESEARCH LABORATORY
Washington, D.C.

(14) NRL-MR-4020

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: NRL Memorandum Report 4020
2. GOVT ACCESSION NO.:
3. RECIPIENT'S CATALOG NUMBER:

(6) 4. TITLE (and Subtitle): GaAs FET DEVICE FABRICATION AND ION IMPLANTATION TECHNOLOGY (MICROWAVE III-V COMPOUND SEMICONDUCTORS)

5. TYPE OF REPORT & PERIOD COVERED: Summary Report 1 Oct 1977 - 30 Sept 1978

6. PERFORMING ORG. REPORT NUMBER:

(10) 7. AUTHOR(s): Kenneth J. Sleger and Harry B. Dietrich

8. CONTRACT OR GRANT NUMBER(s):

9. PERFORMING ORGANIZATION NAME AND ADDRESS: Naval Research Laboratory, Washington, DC 20375

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 62762N; ZF54-581; ZF54-581-001; NRL Problem P02-08B/C

11. CONTROLLING OFFICE NAME AND ADDRESS: Chief of Naval Material Command, Washington, DC 20360

(12) 29p.

12. REPORT DATE: June 27, 1979

13. NUMBER OF PAGES: 28

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office):

(11) 27 Jun 79

15. SECURITY CLASS. (of this report): UNCLASSIFIED

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE:

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

(16) F54581

(17) ZF54581001

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

(9) Annual Summary rept. 1 Oct 77-30 Sep 78,

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

GaAs — Microwave field effect transistors
InP — Microwave semiconductor device fabrication
Ion implanation — and evaluation

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Microwave Schottky barrier FETs and ion implantation have been selected to provide a benchmark technology for evaluation of III-V compound semiconductor materials grown at NRL and elsewhere. FETs used here employ a nominal one micron gate length and are processed by a combination of conventional contact photolithography and liftoff techniques.

Ion implantation studies have centered about creating doping profiles suitable for active layers in GaAs and InP FETs using semi-insulating (SI) substrates. These substrates are previously qualified by capping with plasma deposited Si_3N_4 and annealing between 800°C and 850°C for 15-30

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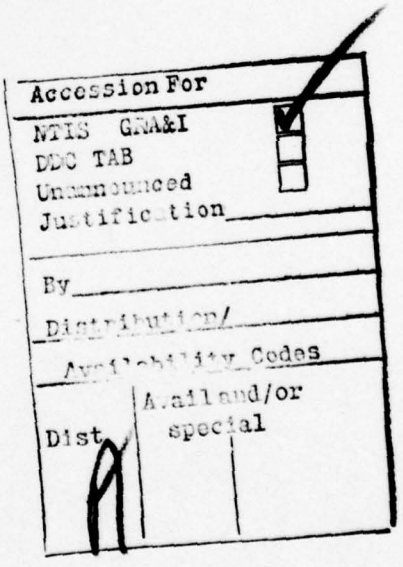
20. Abstract (Continued)

minutes (GaAs) or 700°C-750°C for 15 minutes (InP). Samples which show surface conversion after the anneal are rejected. NRL has demonstrated proficiency in being able to implant, cap and anneal both GaAs and InP SI substrates.

GaAs FETs were fabricated on ion implanted NRL SI substrates (unintentionally doped) and on commerically supplied Cr doped SI GaAs with epitaxial channel regions. At 8 GHz the noise figure ranged from 3.4 dB - 3.8 dB with 6-8 dB associated gain for these devices. Differences in microwave performance between ion implanted and epitaxial FET was correlated to differences in mobility and and velocity profiles obtained from FAT FET test structures and actual microwave FET devices, respectively. Results suggest the need for improvement in FET process technology and capping technology.

TABLE OF CONTENTS



GaAs FET DEVICE FABRICATION AND ION IMPLANTATION TECHNOLOGY

INTRODUCTION

This report describes the NRL effort in providing a bench mark microwave device technology for characterizing the III-V compound semiconductor materials grown at NRL. The device test vehicle used for this purpose is the Schottky barrier field effect transistor (MESFET). In addition, a substantial amount of effort has been devoted to the use of ion implantation as a doping technology and as a means of improved materials control. At present, there is not a complete understanding of the relationship between III-V compound semiconductor microwave device performance and materials parameters, especially in the case of the MESFET.

The relationship between this effort and to that of the entire NRL Electronic Material Technology Program has been previously discussed in NRL Memorandum Report 3701, (February 1978), figure 30, and will not be elaborated upon in this report. Rather, emphasis will be placed on ion implantation and FET characterization results. Results on both GaAs and InP will be reported.

FET FABRICATION

Two FET horizontal geometries have been used during this reporting period. These are shown in Fig. I. Note that the fine geometry design resembles that used by several industrial laboratories and thus should be capable of providing results similar to those obtained in private

Note: Manuscript submitted April 16, 1979.

industry using the same structure. FET vertical geometry is shown in Fig. II with key dimensions indicated. The channel thickness, a, ranges from 1800Å to 3500Å depending on: the material supplier, method of channel formation and doping level. Channel n type doping concentrations are between $8X10^{16}cm^{-3}$ and $2.5x10^{17}cm^{-3}$. Before FET fabrication, the channel doping and thickness are determined using a conventional C-V plotter. If necessary, a chemical etch is used to reduce the channel thickness to provide a pinchoff voltage between two and six volts.

Processing of the mesa and contact geometries proceeds by use of conventional contact photolithography and lifting of evaporated metal contacts. The area encompassing the source, drain and gate is isolated from the gate pad by chemically etching a mesa or by using neon ion bombardment. The latter technique is extremely attractive since it provides a means of achieving a planar technology and allows for relatively simple contact printing of 0.8 micron gate lengths. Figure III shows a completed NRL Fine Geometry FET with 0.8 micron gate lengths made with neon bombardment isolation. However, under another NRL program, submicron gate length InPFETs were made using electron beam photolithography.[1] This electron beam photolithography is available for the characterization program should the need occur.

Source and drain contacts are evaporated Au/Ge/Ni alloyed at 450°C for 30 seconds and then overlaid with gold to aid in wire bonding. The gate is evaporated Al(GaAs, InP) or Cr/Au (GaAs). Cr/Au is an attractive gate metalization because it adheres well to semiconductors and aids in wire bonding. Its disadvantage is that it is not reliable over a long period of time (years) unless a diffusion barrier metal such as platinum

is inserted between the Cr and the Au. For the purposes of this program, Cr/Au gates on GaAs are judged as acceptable.

ION IMPLANTATION

Several laboratories have demonstrated the usefulness of ion implantation as a technique to form the channel region of GaAs MESFETs. In addition, ion implantation may be useful as a technique to qualify the integrity of semi-insulating substrates. The integrity of GaAs semi-insulating (SI) substrates has been of vital concern to the FET microwave device community for roughly ten years and this concern has provided the major stimulus for the Electronic Material Technology Program at NRL.

In brief, GaAs SI substrates may be assessed for high temperature conversion effects using the same capping and annealing techniques used in ion implantation. If, after annealing and capping, the SI GaAs surface becomes conducting, there is good reason to believe that some impurity or defect species is moving about at the anneal temperature. Such conversion effects can significantly alter or totally mask the low-level implantation used for FET channel doping. Similarly, if a poor SI substrate is employed for high temperature epitaxial growth of the channel, there is a high probability that the channel characteristics will be altered after growth, especially near the interface with the SI substrate. Experimental results at both NRL and other laboratories have shown that SI GaAs substrates that show surface conversion effects are not suitable for microwave FET fabrication. Channel layers formed on such substrates have low mobility, deep trapping centers, unusual doping profiles and hidden deleterious depletion regions, all of which degrade FET RF performance. The physical mechanisms behind SI substrate conversions are

not understood.

At NRL, SI GaAs substrates supplied by Code 5221 and outside vendors are qualified by capping with plasma deposited Si_3N_4 (1000Å) and annealing between 800°C and 850°C for 30 minutes. Substrates that show surface resistivities greater than 10^6 ohm/square after the anneal are judged suitable for FET fabrication. The NRL plasma Si_3N_4 is capable of maintaining greater than 10^6 ohm/square sheet resistivity for Crystal Specialties, Laser Diodes and Sumitomo SI Cr doped GaAs when annealed at 800°C for 30 minutes. Under the same conditions, NRL SI GaAs wafers from boule 5-43-L showed p type conversion of the surface. This boule was unintentionally doped (high purity) and grown by the pyrolytic boron nitride encapsulation technique. The commercial SI GaAs was Cr doped and it is believed that the presence of this "excess" Cr provided sufficient compensation to render the commercial material as non-converting at 850°C. The conversion results in NRL material were unexpected and the Si_3N_4 cap integrity was suspected as contributing to this result. To test this hypothesis, 5-43-L material was sent to AFAL for encapsulation with pyrolytic Si_3N_4 and then annealed at 800°C for 30 minutes. This resulted in a surface resistance of greater than 10^5 ohms/square. After annealing at 850°C for 30 minutes, the surface resistance of 5-43-L was reduced to roughly 10^3 ohms/square. These results offered encouragement to continue the use of Si_3N_4 as an encapsulant at both NRL and AFAL. However, it will be necessary to modify the NRL Si_3N_4 system to the point where the integrity of the encapsulant can be trusted. In the interim period AFAL has agreed to encapsulate material implanted at NRL.

Material from boule 5-43-L was sliced into three orientations (111,

110, 100) and polished for use in ion implantation studies. There was originally some belief expressed by certain members of the FET device community that GaAs FET performance is orientation dependent, especially the drain to gate breakdown voltage. However, during this reporting period, the belief in orientation-dependent FET performance has greatly diminished. In any case, it was felt that fabrication of ion implanted GaAs FETs on substrates of different orientation might yield some improved FET results in addition to providing information about ion implantation orientation effects. For these structures a single 400 keV, $4x10^{12}cm^{-2}$ dose of Se^{+} was used to produce the channel. Se was chosen as a dopant since it is known to produce a sharp interface. Si is also attractive and will be tried at a later date for GaAs. Figure IV shows the N-X characteristic of the (100) material. The measured profile is quite uniform across the wafer as evidenced by the overlay of traces obtained from different areas of the wafer. The characteristics of Fig. IV are judged to be attractive for FET fabrication. The implanted (111) wafer showed an N-X profile qualitatively similar to that of Fig. IV. However, faults, following major crystallographic directions were observed subsequent to the anneal and the measured profile was non-uniform across the face of the wafer. The (110) wafer developed large pits over 10% of its surface after annealing. N-X profiles measured in the region between the pits were quite uniform as shown in Fig. V and very similar to that obtained with (100) material. Further samples are presently being processed in an attempt to deduce whether or not these are orientation dependent encapsulation problems.

A qualification and encapsulation scheme has also been developed for semi-insulating iron doped InP supplied by NRL Code 5221. This InP has been capped with 1000Å of NRL plasma Si_3N_4 and annealed between 700°C and 750°C for 15 to 30 minutes with no electrical evidence of surface conversion or conduction. The integrity of the Si_3N_4 encapsulant had previously been evaluated by encapsulating bulk, 10^{18} p-type InP and annealing it for 30 minutes at 700-750°C. A comparison was then made between the zero-bias capacitance of Schottky barrier diodes fabricated on unannealed and annealed material. Such a comparison gives a sensitive test of the integrity of the Si_3N_4 as an encapsulant. It was observed that the surface carrier concentration was not degraded during the high-temperature anneals and the Si_3N_4 was judged to be an adequate encapsulant for InP. Slices of NRL InP boules 1-91H and 1-94H were able to pass the qualification tests and, therefore, were judged to be suitable for FET implantation.

Si implantation studies were conducted on InP, wafers 1-91H and 1-94H. An implant energy of 170 keV was used on both wafers. On wafer 1-94H the fluence was varied from $3x10^{12}cm^{-2}$ to $3x10^{13}cm^{-2}$. The % activation and Hall mobility was measured for 1-94H and is shown in Fig. VI. The highest mobility was obtained at a fluence of $3x10^{12}cm^{-2}$ albeit with about half the activation obtained with higher fluences. However, the maximum observed mobility of $2600cm^2/v.sec$ is roughly 80% of the best mobilities observed in bulk n type InP. Consequently, it was decided to use the 170 keV, $3X10^{12}$ cm^{-2} Si implant receipe for FET channel implants. Fig. VII shows an N-X characteristic obtained for a Si implant on wafer 1-91H. This wafer was later fabricated into MESFETs under another NRL

research program. These FETs were the first successfully fabricated ion implanted InP FETs with x-band microwave performance.[2]

GaAs FET CHARACTERIZATION - EXPERIMENTAL

FET characterization begins as soon as a GaAs wafer is received which has a thin n type channel. Using an evaporated array of Schottky barrier contacts, the N-X curve for the channel vertical dimension is determined. If this is acceptable, then FET processing begins. The processing-characterization scheme is shown in Fig. VIII. The different types of characterization and accept/reject criteria are explained in detail in NRL Memorandum Report 3701 and will not be discussed here.

A variety of material was processed and an approximate wafer breakdown is indicated below.

# WAFERS	CHANNEL FORMATION TECHNOLOGY	SUBSTRATE SOURCE
10	LPE/no buffer (NRL)	NRL Code 5221 (undoped)
6	Ion Implantation (NRL)	NRL Code 5221 (undoped)
10	LPE/VPE (Industrial)	Industrial (Cr-doped)
10	Ion Implantation (NRL)	Industrial (Cr-doped)

Some industrial wafers employed buffer layers and all industrial material was grown on Cr doped SI substrates. The buffer layer insertion, about 5-10 microns thick and doped n-type below $10^{13}cm^{-3}$, is a popular industrial technique to both improve the quality of the active layer-substrate interface and to obviate outdiffusion from the doped SI substrate into the active channel. This is important to achieve low noise figure. The

NRL objective has been to provide undoped GaAs material of superior quality such that the buffer layer is unnecessary. Consequently, all material (LPE or SI wafers) received from NRL Code 5221 contains no buffer layers.

The FINE GEOMETRY (Fig. I (b)) was chosen for nearly all the work to be reported here since the photomasks for these FETs contained FATFET, Schottky barrier and ohmic contact test patterns not present on the RELAXED FET photomasks. The test patterns are shown in Fig. IX. The "FATFET" pattern is popular for evaluating vertical mobility profiles in the channel region. As will be pointed out in the next section, these test patterns have been a valuable aid in assessing the quality of channel layers.

GaAs FET CHARACTERIZATION RESULTS

After processing the various wafers described in the previous section, it was determined that the best microwave performance was obtained from industrial GaAs having a vapor phase epitaxial (VPE) channel region and buffer layer grown in sequence on a chromium doped SI GaAs substrate. Consequently, this material became the standard by which all other material was judged. Fig. X shows the best small signal noise figure and gain from 4 to 12 GHz obtained from a one micron T gate GaAs FET fabricated from this industrial VPE material. Also included in this figure is the performance of the next best FET type, made from the NRL boule 5-43-L implanted with Se as shown in Fig. IV. In order to determine whether the difference between the VPE and ion implanted FETs was related to processing, an experiment was conducted such that both VPE and ion implanted wafers were processed simultaneously. Microwave performance measured on

dual processed FETs was no different from that shown in Fig. X. Thus, the differences in microwave performance was judged to be related to differences in materials parameters rather than to differences in processing. However, the best noise figures given in Fig. X are about 1 dB higher than those theoretically expected from a 1 μm x 300 μm T gate FET structure. It is expected that the use of a recessed gate structure and an n^+ ohmic contact technology will lower the noise figure substantially below that of Fig. X.

A detailed study was made to determine what difference, if any, could be detected between the VPE and ion implanted FETs using the various characterization techniques available in NRL Code 5211. Table I is a listing of various FET parameters and the experimentally determined values for the two types of FETs and also includes values for similarly processed industrial LPE material with a buffer layer. Note that the most significant difference between the different types of FETs is the lower channel mobility in the ion implanted FET. The presence of looping and backside gating in the ion implanted FET suggests a problem at the interface. To further explore the interface between the channel and the nonconducting material beneath it, both VPE, LPE and ion implanted FETs were mobility and saturated drift velocity profiled using FATFET test structures and SKINNY FET (L_g = 1 μm) structures, respectively. The results are shown in figures XI and XII. These profiles clearly point out the presence of a somewhat larger spatial degradation in carrier transport properties in the ion implanted channel near the interface than in the corresponding region of the VPE, LPE channels. It is tentatively suggested that this degradation in carrier transport is in part respons-

ible for the performance difference between VPE and ion implanted FETs shown in Fig. IX. (At this writing, there is not sufficient microwave data to report on LPE (industrial) FETs.) The reasons for the degradation observed in ion implanted channels are not clear but may be related to the capping/annealing process or the quality of the semi-insulating substrate. Further experiments are underway to determine the cause of the mobility degradation and to eliminate it.

Another set of experiments involved the study of seven LPE GaAs FET samples grown at NRL using various cooling techniques. Attempts to contact print 1 μm x 300 μm T gate FET geometries on the LPE material were unsuccessful because the surface of the LPE layer was not uniform. However, FATFET test structures were obtained. The most significant characterization results were obtained on samples 13-15N and 13-20N which had channels doped to 1.5 - $1.6 \times 10^{17} cm^{-3}$ and were chemically etched back to a thickness of 2200Å to 2400Å by NRL Code 5211. Both samples had identical NRL semi-insulating substrates. However, sample 13-20N employed a Ga etch of the substrate before growth of the channel while 13-15N did not. Figure XIII shows the FATFET mobility profiles obtained from these two types of materials. Note that the Ga etch process has significantly improved the channel mobility over that of the unetched sample. This is an important result which supports the usefulness of Ga etching by NRL Code 5221 as pointed out earlier.[3] These results were reported at the 1978 Spring Meeting of the Electrochemcial Society.[4]

ACKNOWLEDGEMENTS

The authors appreciate and acknowledge the technical assistance of M. Bark and R. Corazzi in the areas of photolithography, wet etching and

capping/annealing.

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TABLE I
TYPICAL FET/MATERIALS PARAMETERS

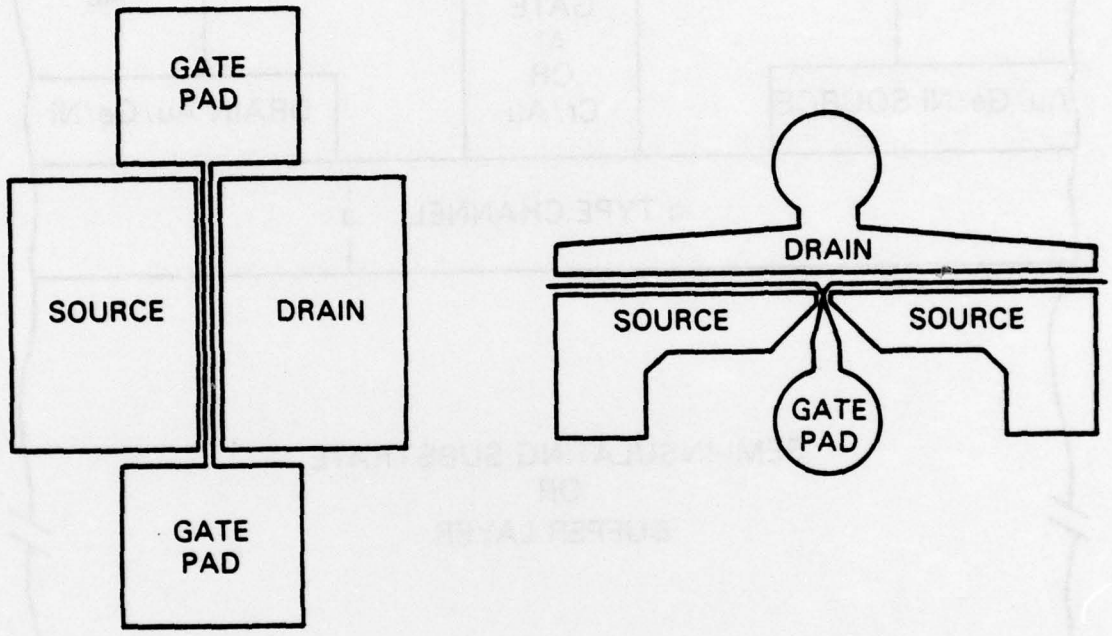
L_g = 1 micron W_g = 300 microns

	Channel Doping cm^{-3}	Channel Thickness Angstroms	Average Channel Mobility $cm^2/Vsec$	I_{DSS} mA	g_m mmho	V_p volts	R_s ohms	Observed Looping	Observed Light Sensitivity	Observed Backside Gating
VPE	$1x10^{17}$	3200	3400	75-100	26-28	6-7	8-10	none	slight	none
LPE	$2.5x10^{17}$	1600	3500	50-70	24-26	3-3.5	8-10	rarely	slight	slight
II	$2x10^{17}$	2200	2800	60-70	20-22	3.5-3.8	12-15	rarely	moderate	slight

NOTE: VPE, LPE materials industrially manufactured with buffer layer.

II material implanted at NRL into buffer free NRL substrates

NRL HORIZONTAL FET GEOMETRIES



(a)
RELAXED
L_g = 1.5-2.0 MICRONS
W_g = 250 MICRONS

(b)
FINE
L_g = 0.7-1.5 MICRONS
W_g = 150-300 MICRONS

Fig. I — NRL horizontal FET geometries used in characterization studies. FINE geometry is popular in industry. W_g is the gate width. L_g is the gate length.

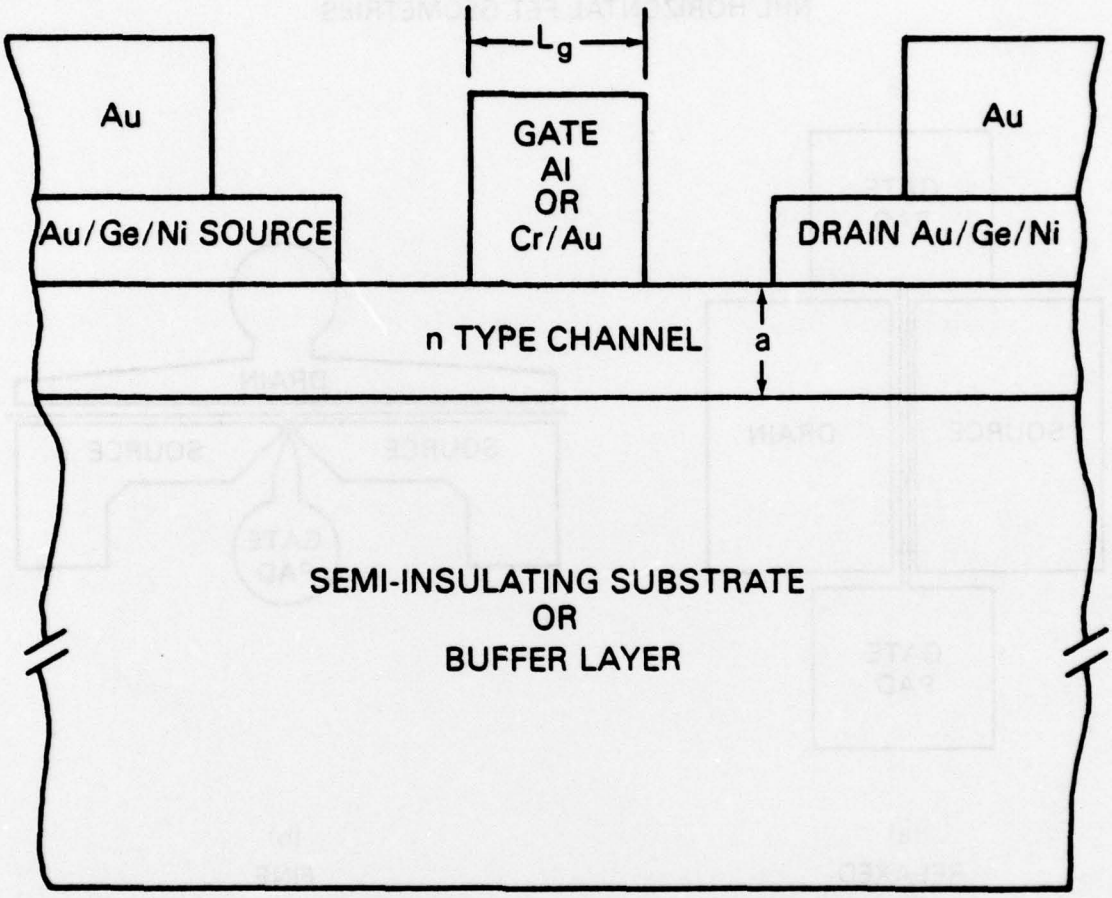


Fig. II — NRL vertical FET geometry used in all results reported herein. The gate length, L_g, the channel thickness, a, and the source to drain contact spacing are key dimensions that determine microwave performance.

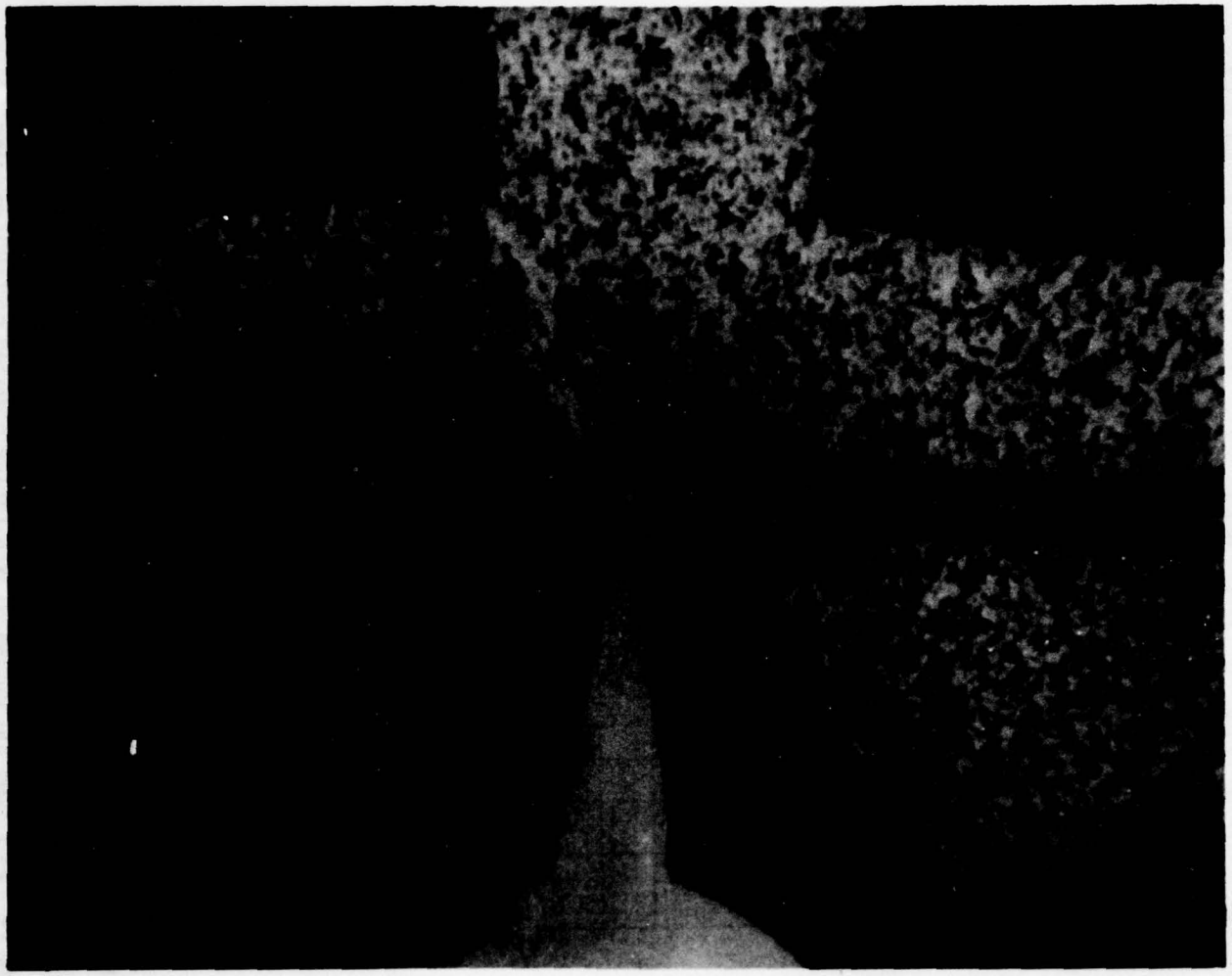


Fig. III — Optical photo of completed NRL FINE geometry FET with 0.8 micron gate length. Such submicron gate lengths are achieved using conventional contact printing and planar geometries.

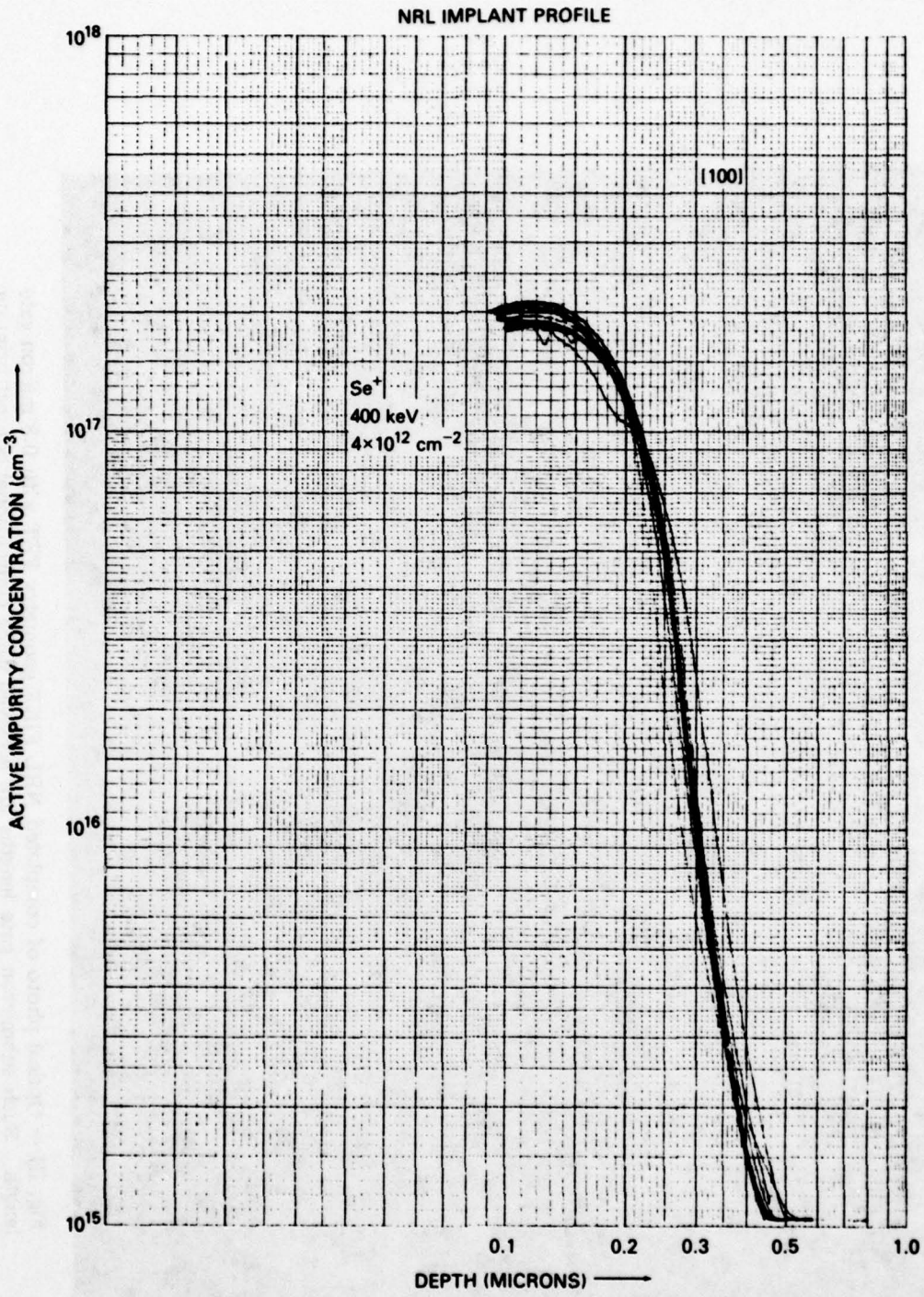


Fig. IV — FET type ion implanted N/X profile obtained on (100) oriented unintentionally doped semi-insulating GaAs grown at NRL. Ion implantation by NRL Code 5212.

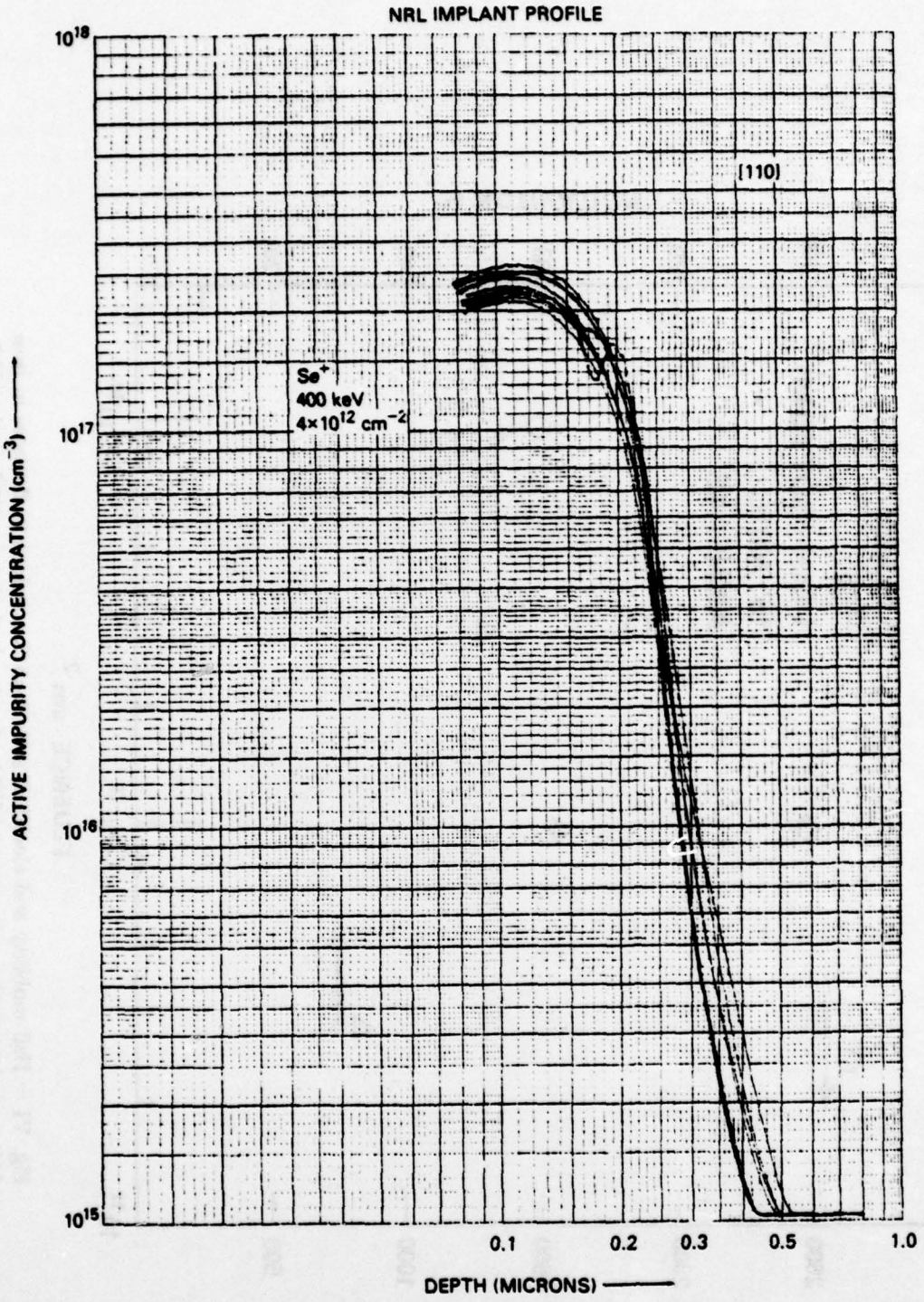


Fig. V — FET type ion implanted N/X profile obtained on (110) oriented unintentionally doped semi-insulating GaAs grown at NRL. Ion implantation by NRL Code 5212.

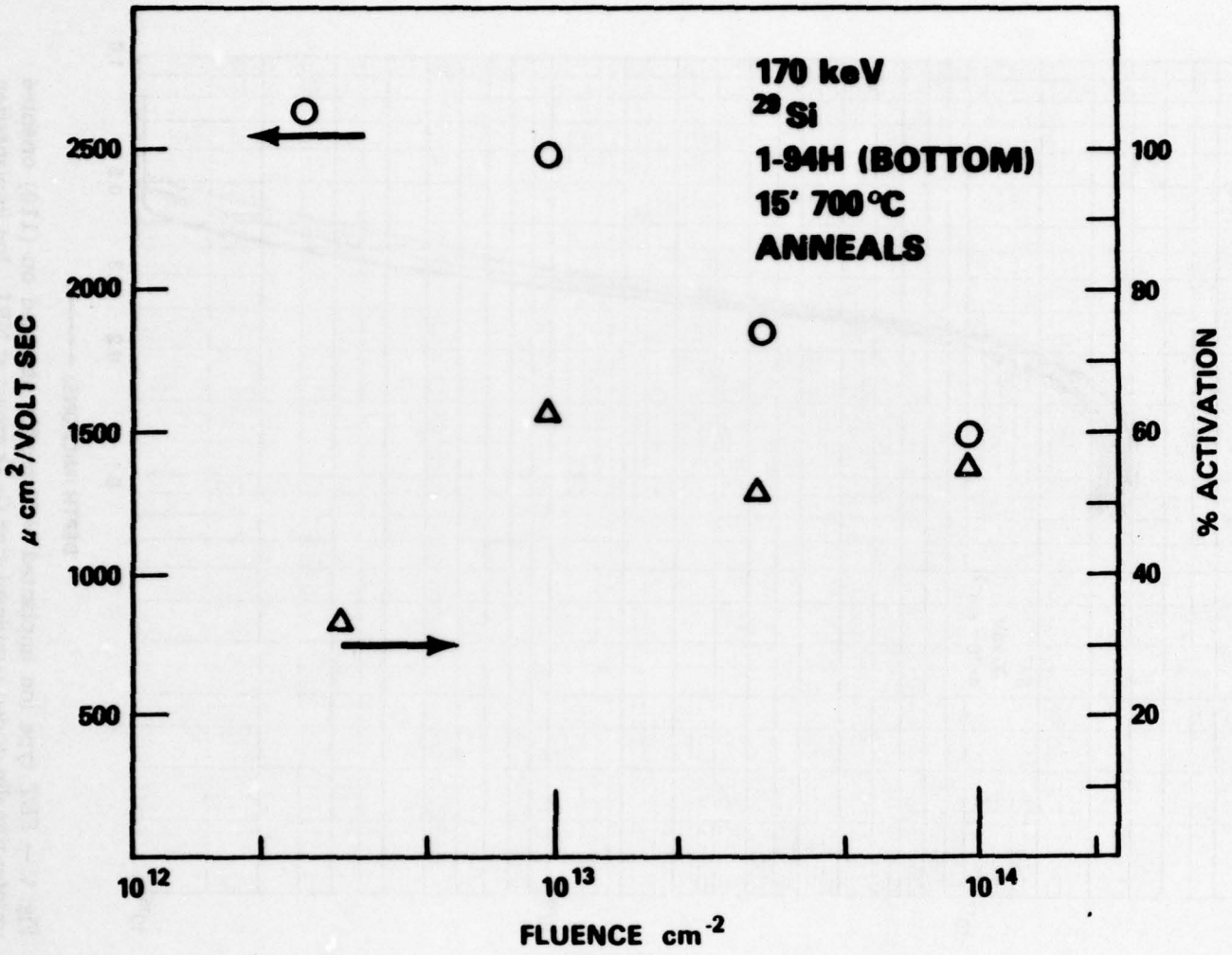


Fig. VI — Hall mobility and electrical activation for various Si fluences in iron doped semi-insulating InP grown at NRL. Ion implantation by NRL Code 5212.

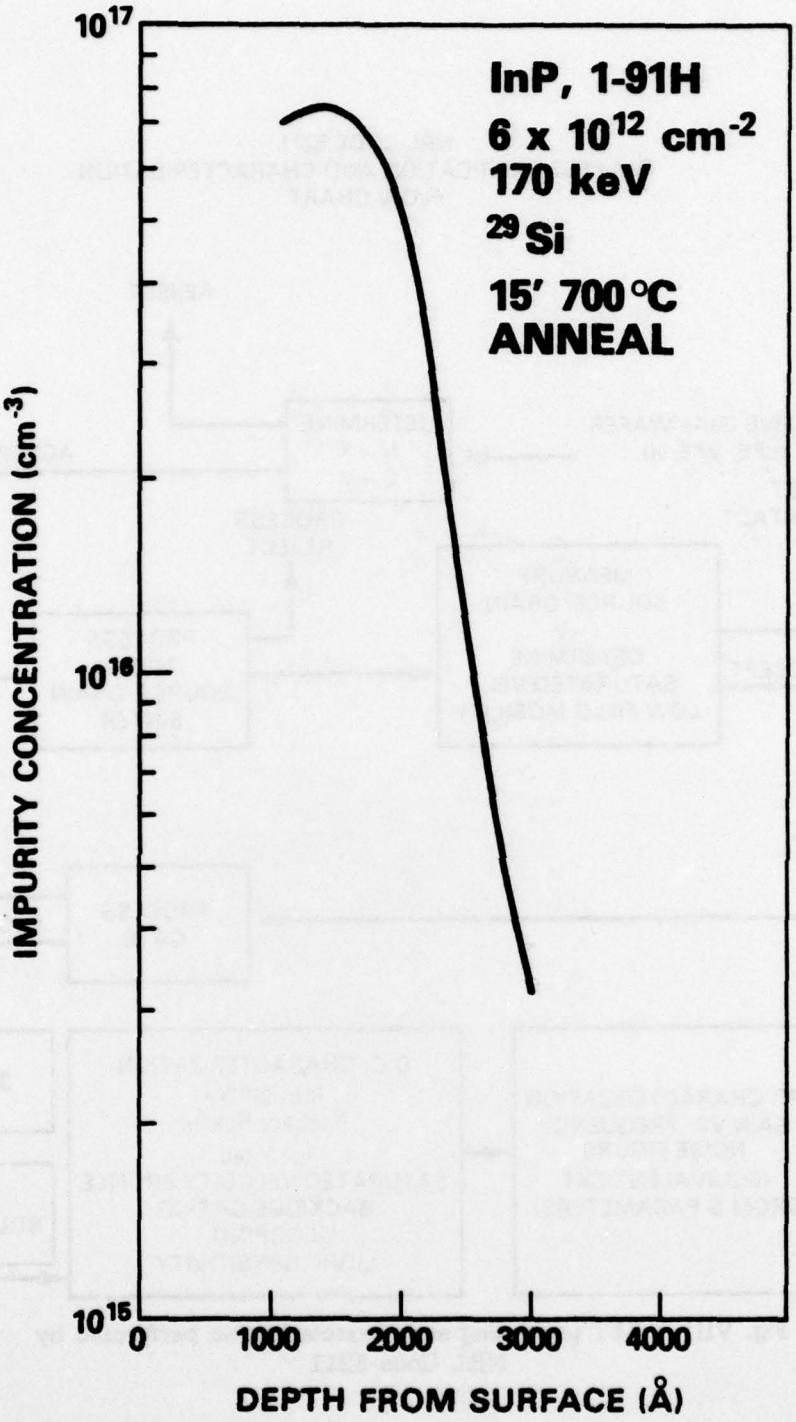


Fig. VII — FET type ion implanted N/X profile obtained on (100) oriented iron doped semi-insulating InP grown at NRL. Ion implantation by NRL Code 5212.

NRL CODE 5211
GaAs FET FABRICATION AND CHARACTERIZATION
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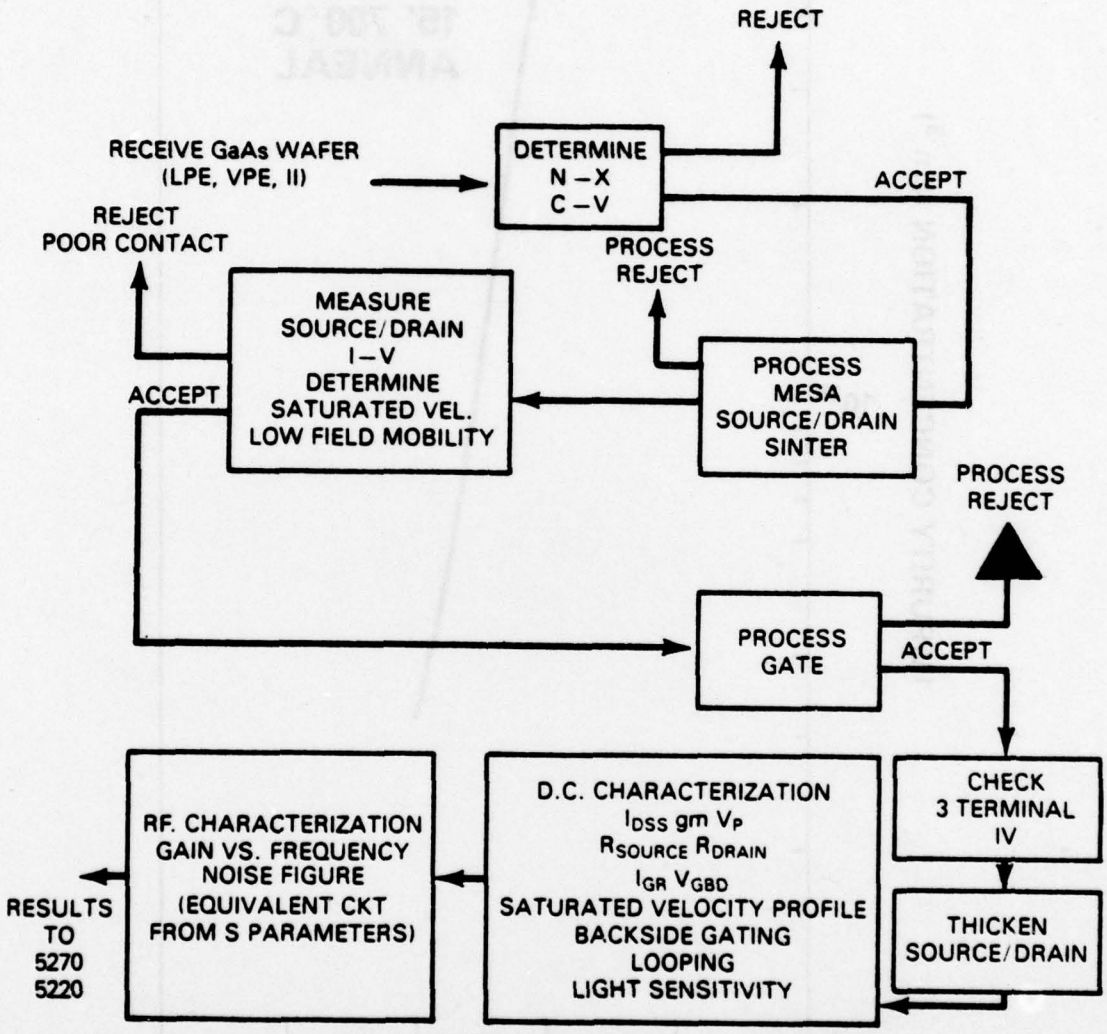

Fig. VIII – FET processing and characterization performed by NRL Code 5211

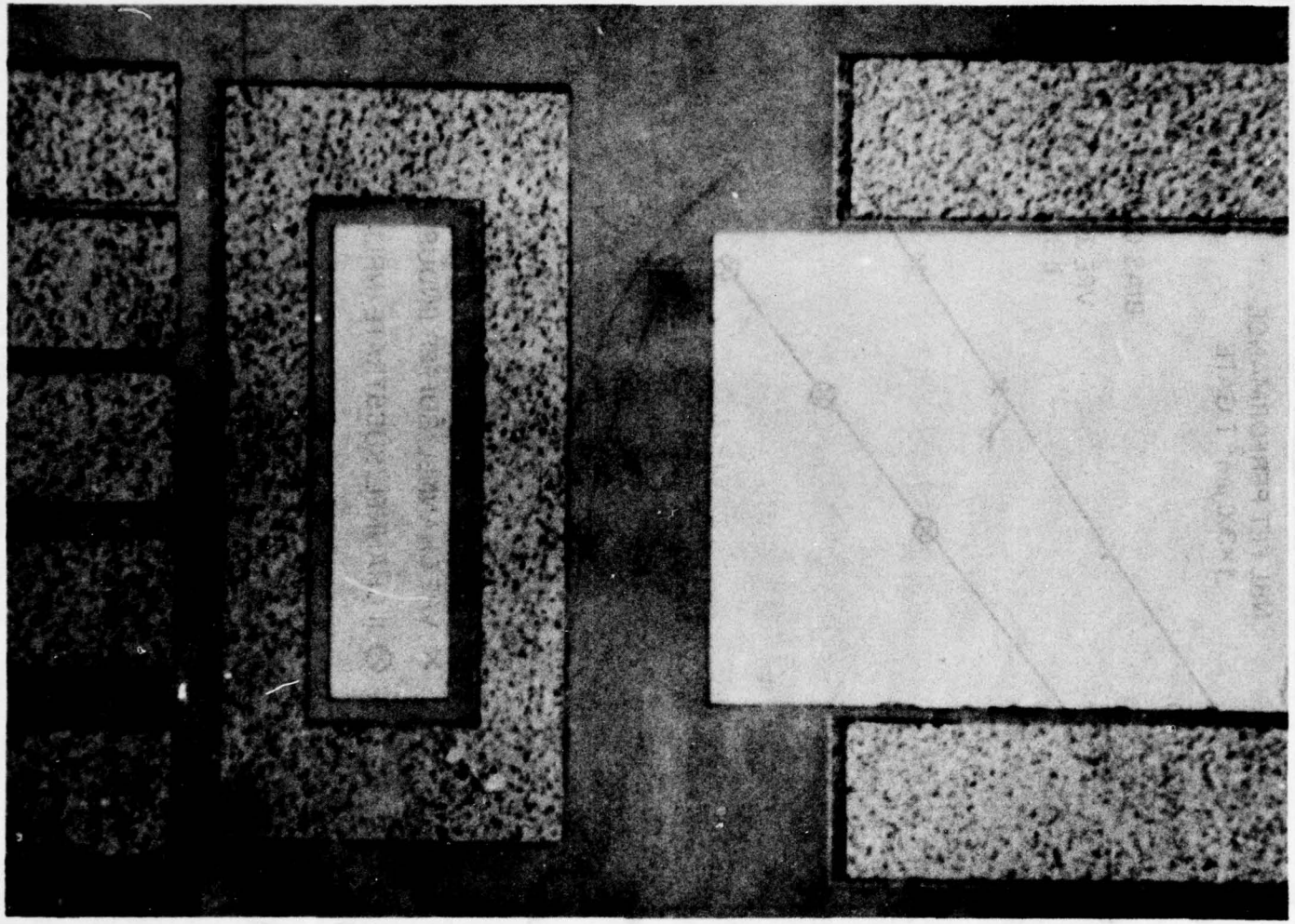

Fig. IX — Large area test structures contained on FINE geometry FET photomasks. Optical photo of completed structures. (top) FAT FET (middle) Schottky barrier/CV (bottom) ohmic contact evaluation.

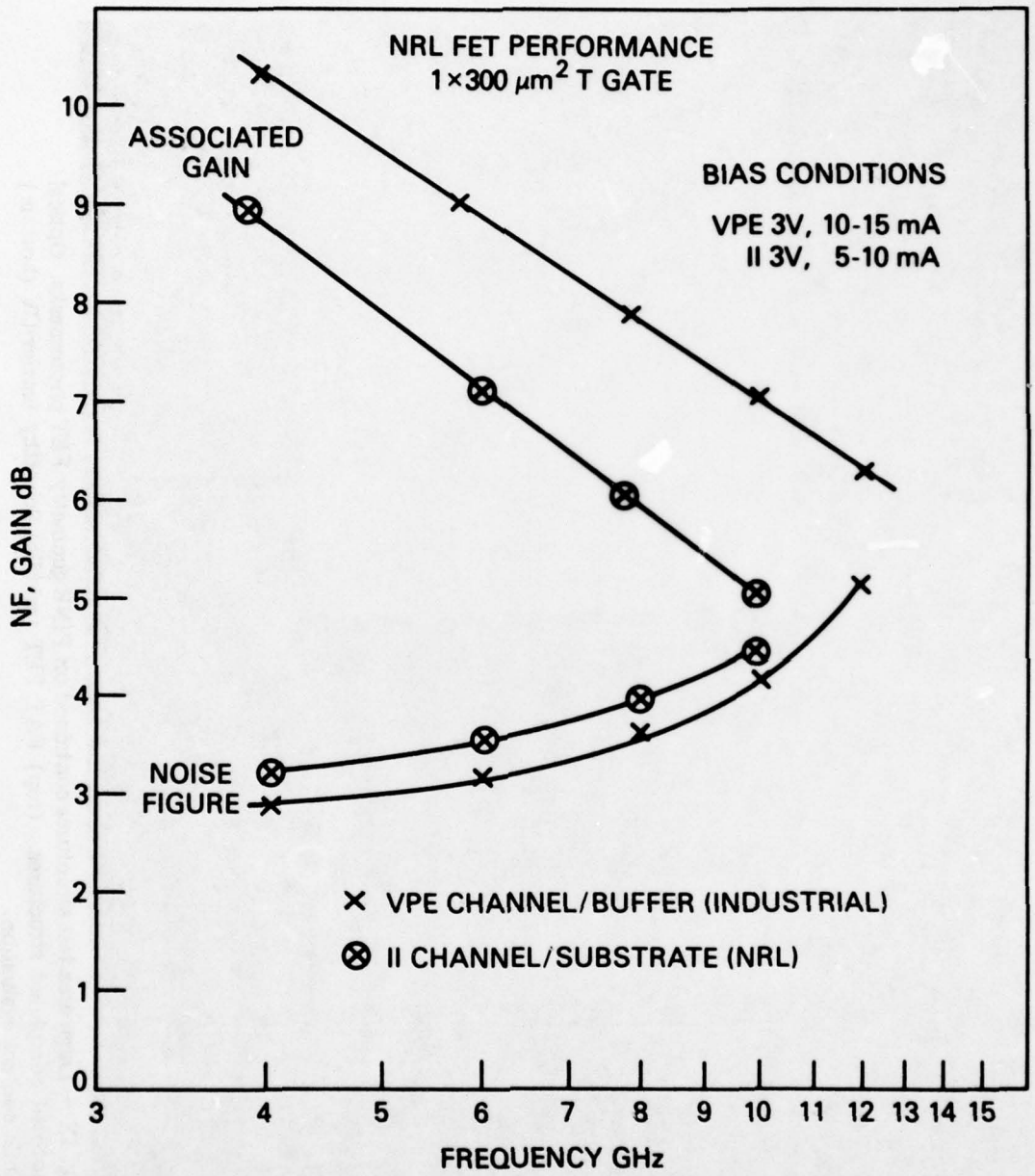

Fig. X — Microwave small signal performance of NRL FINE geometry GaAs FETs. Material with VPE channel on a buffer layer gave best performance.

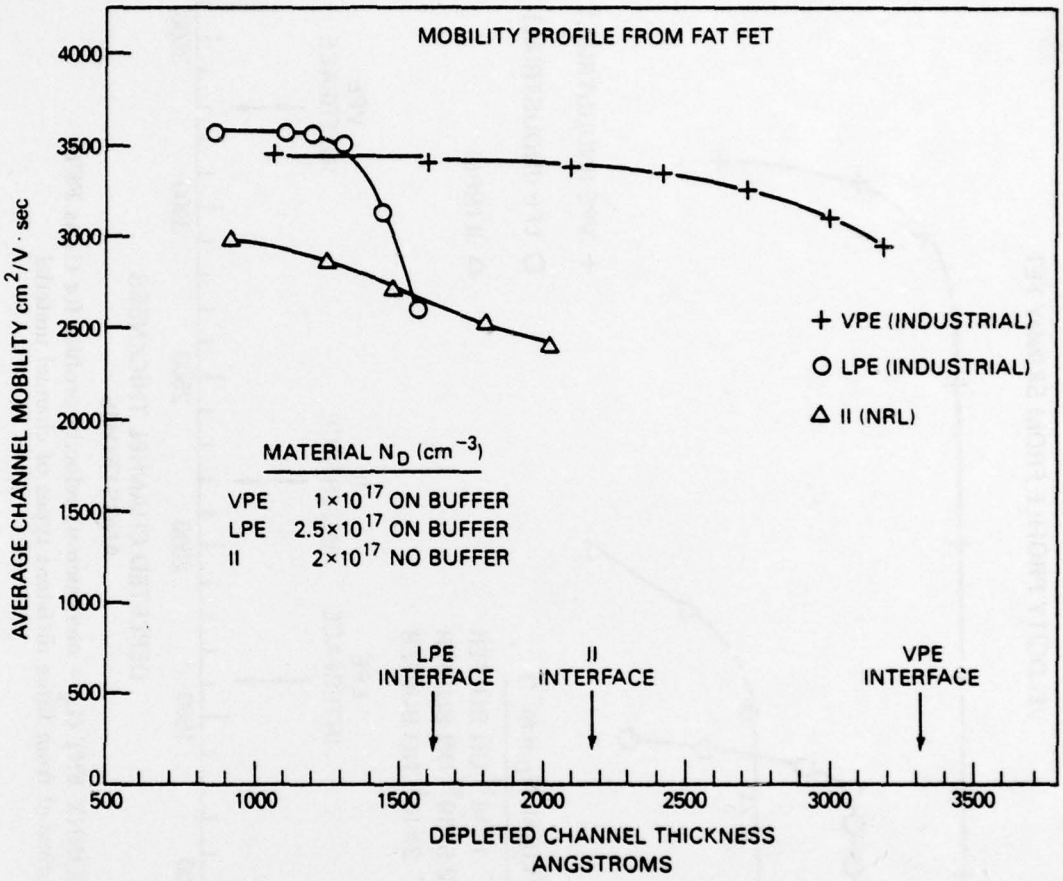

Fig. XI — FAT FET mobility profiles for GaAs FETs fabricated from three different types of channel material. A gradual spatial mobility degradation is shown for ion implanted channels.

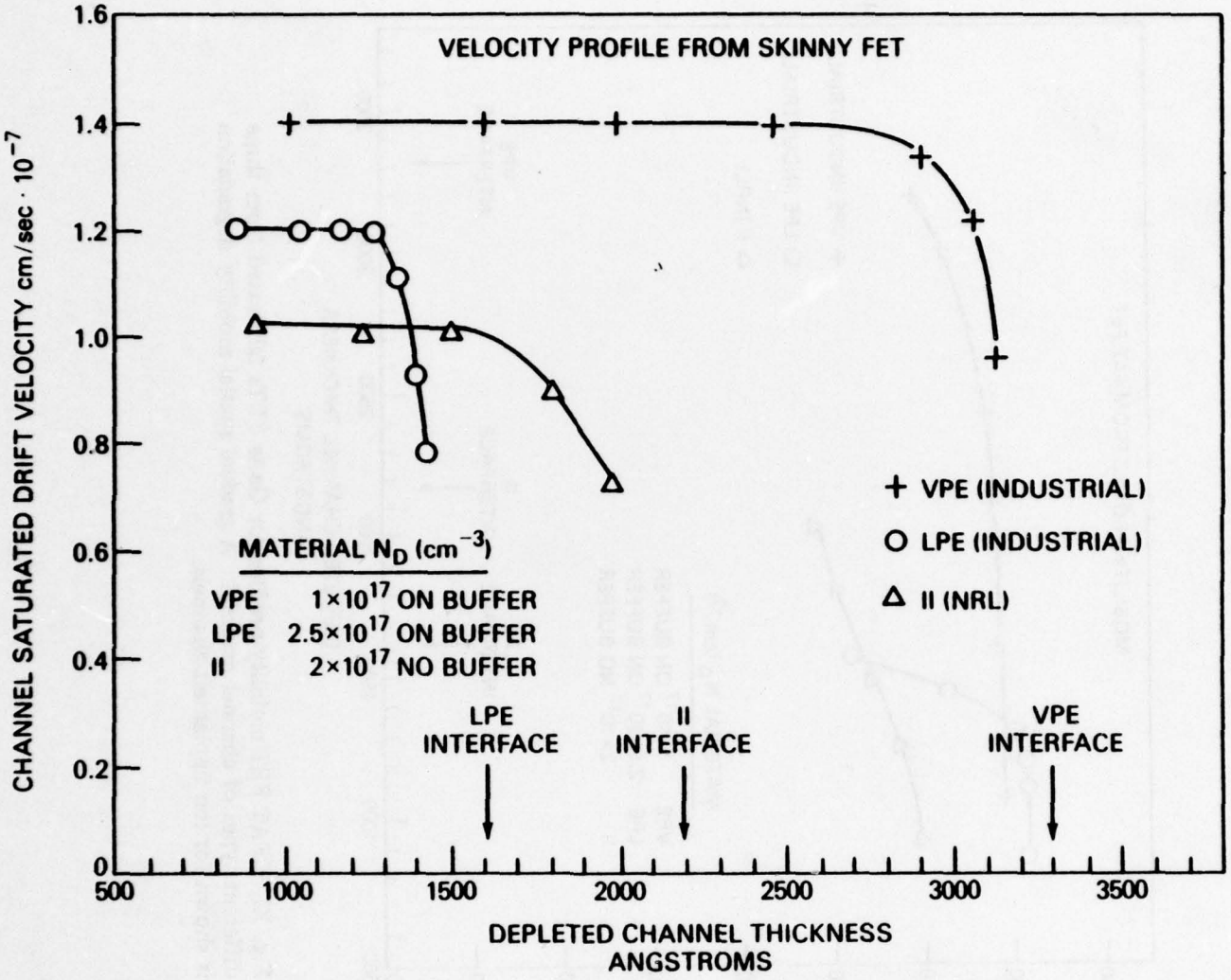

Fig. XII — SKINNY FET (L_g = one micron) velocity profiles for GaAs FETs fabricated from three different types of channel material

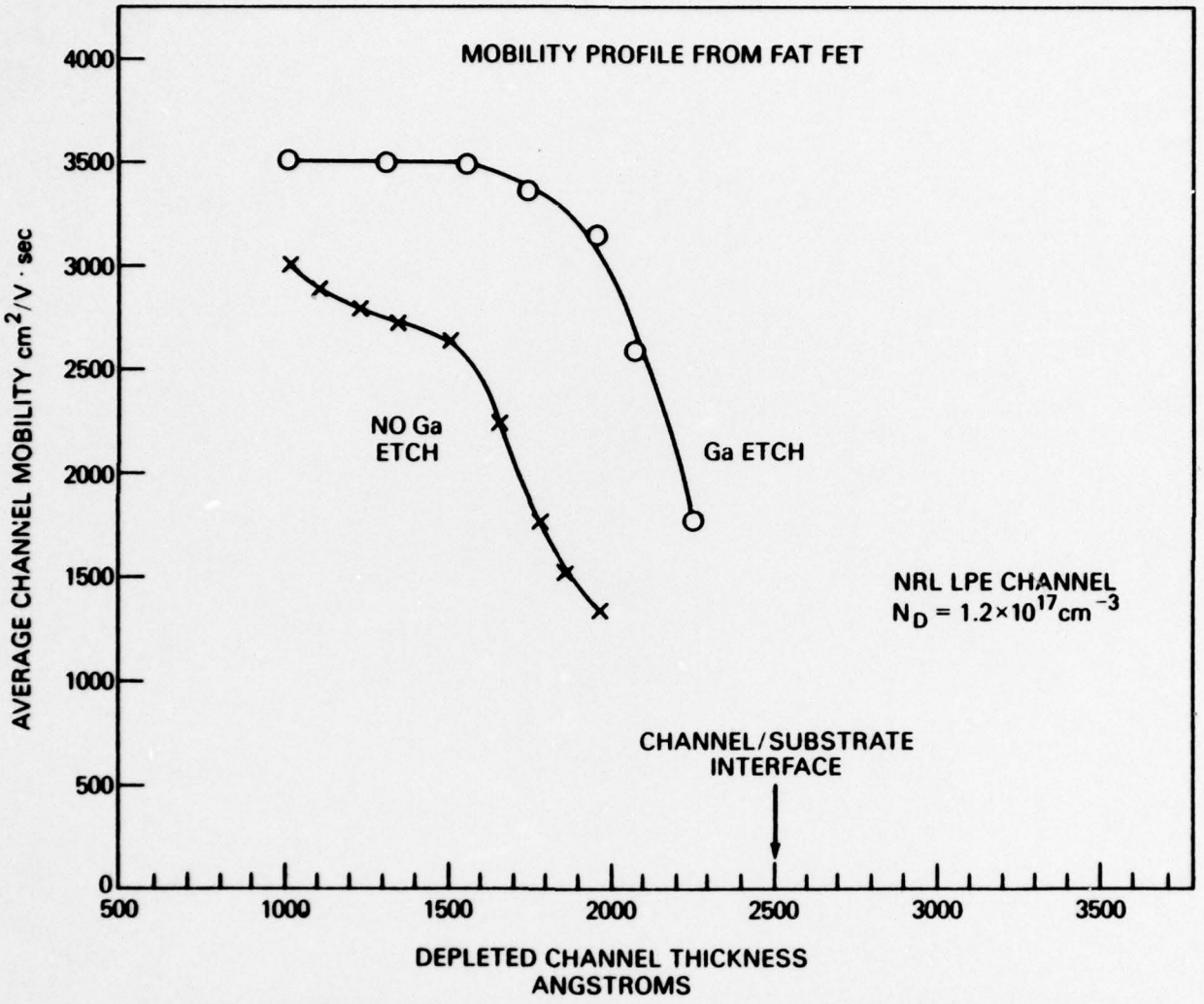

Fig. XIII — FAT FET mobility profiles for GaAs FETs made by LPE channel growth technique with and without gallium etchback before growth. The beneficial nature of the gallium etch is dramatically revealed in the mobility profiles.