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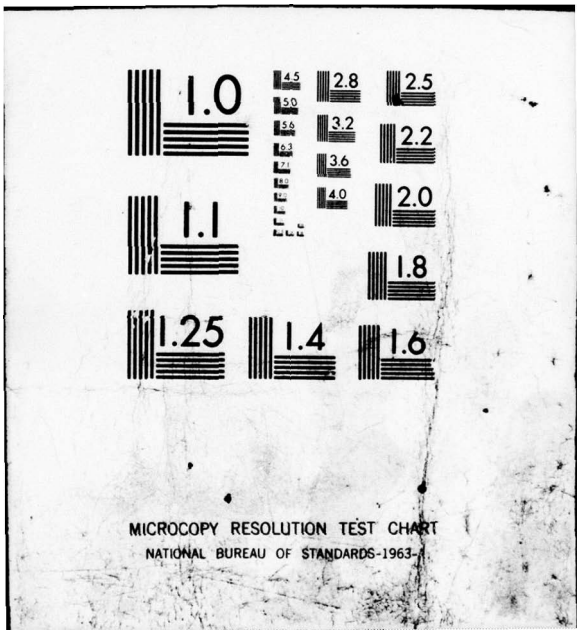
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ANNUAL REPORT NO. 3

Noncoplanar High Power FET

January 1977 - December 1977

Prepared by:

S. G. Bandy, R. Sankaran, D. M. Collins

VARIAN ASSOCIATES
611 Hansen Way
Palo Alto, CA 94303

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By using a p^+ Ge-doped substrate and an MBE active layer, common-gate noncoplanar power FET devices were fabricated. Evaluation revealed that the most serious problem with this run was the poor leakage characteristics of the p-n junction gates.

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SUMMARY

A noncoplanar device run was completed from start to finish for the first time. Cd autodoping in the vee and field growths necessitated going to p^+ Ge-doped substrates, and failure to grow continuous VPE active layers over the vees necessitated going to MBE active layer growth where a sputter clean could be done before growth. It was found that a W-Ti barrier was needed between the ohmic contacts and the overlay metal to preserve the low contact resistance and overlay conductivity. These first devices suffered from metallization breaks over the mesa edge, a conducting field growth and high gate leakage current. Consequently, no device characteristics were obtained from this run.

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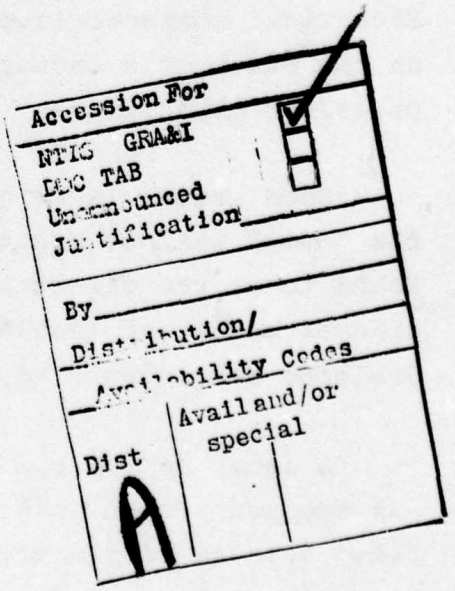

1. INTRODUCTION

Figs. 1 and 2 show the proposed noncoplanar power FET structure and fabrication sequence reproduced from Annual Report No. 2 of this contract for the sake of review. Besides the noncoplanar structure, this design offers the advantages of compactness, submicron gate lengths, p-n junction gate reliability and larger drain voltage swings, among other things.

Concerning the progress prior to the period covered by this report, no fundamental difficulties have been encountered with the structure of Fig. 1 that would preclude the realization of such a structure. The technique for etching and refilling the low-doped grooves under the source and drain contacts has been developed using a V-shape, which in fact is better than the profile shown in Fig. 1 from the point of view of achieving lower gate resistance. The slow etching rate of the (111)B surface has been found to give good control in producing submicron gate lengths over a large wafer area. Gate lengths as low as 0.2 micron have been achieved with this technique, which certainly exceeds the original expectations. Electrical characterization of the "vees" has demonstrated on the order of a factor of 50 in the reduction of the parasitic capacitance.

Good active layer growth also has been achieved over the "vees" without vapor etch, and the <100> direction was found to be the direction of minimum undercut for the formation of mesas and insulating field growth. A mask set was designed accordingly and has been received.

A dummy device run was started with in-house masks, but was stopped at the point of etching and growing the insulating field because of the high n-type background in the reactor.

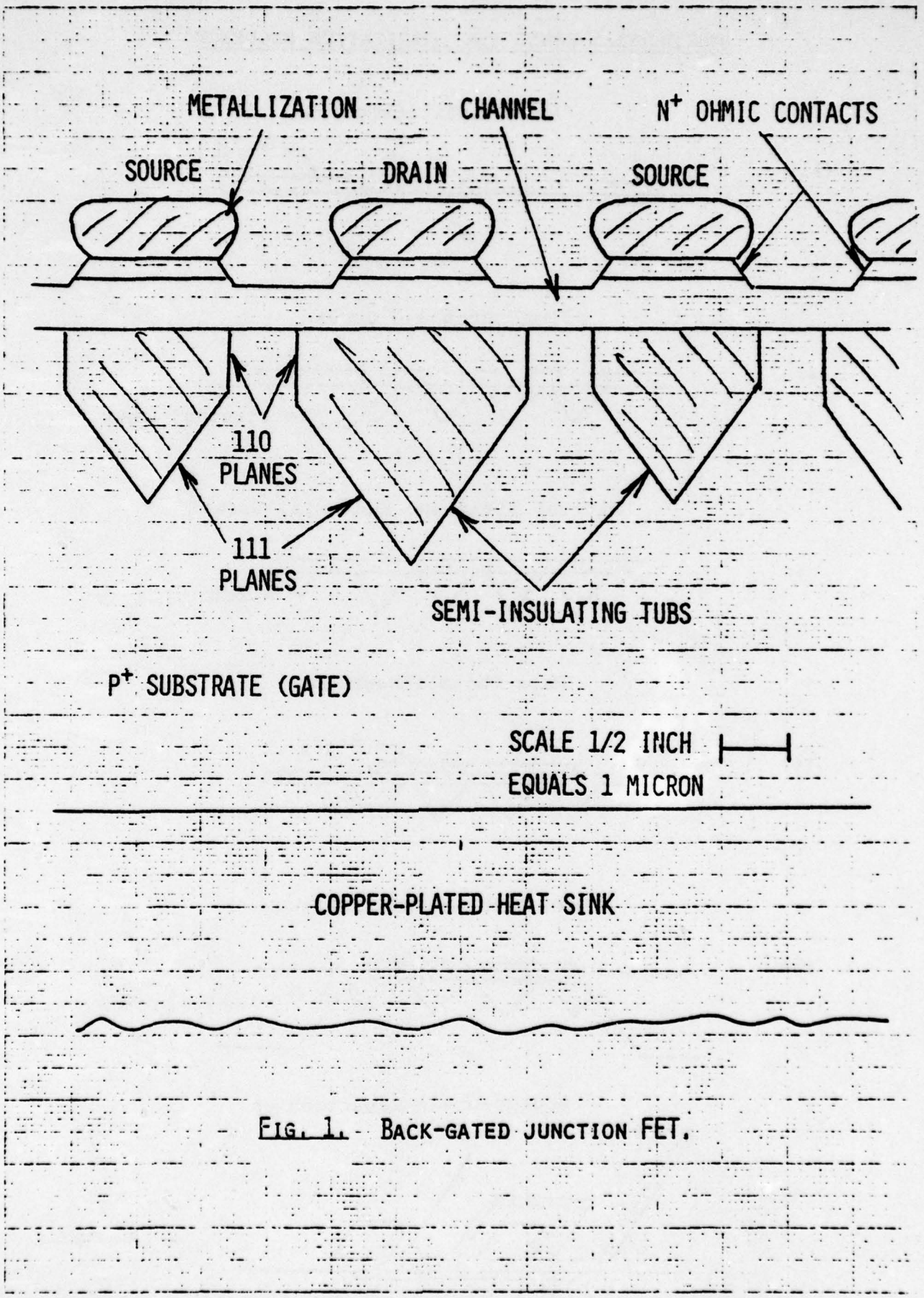

FIG. 1. BACK-GATED JUNCTION FET.

NONCOPLANAR POWER FET FABRICATION SEQUENCE

"Vee" Photolithography

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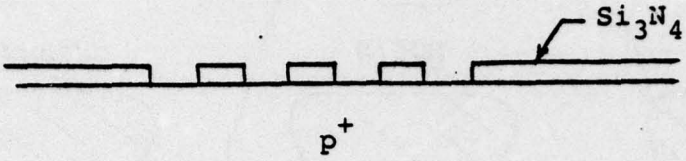

"Vee" Etch and Growth

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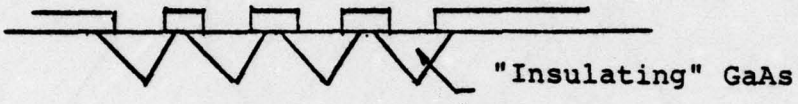

Nitride Strip and Epitaxial Growth

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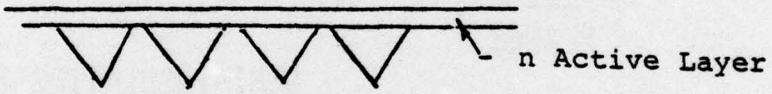

Mesa Photolithography

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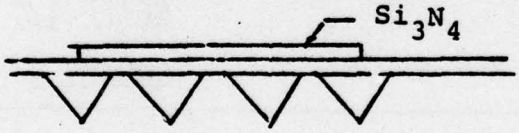

Mesa Etch and Field Growth

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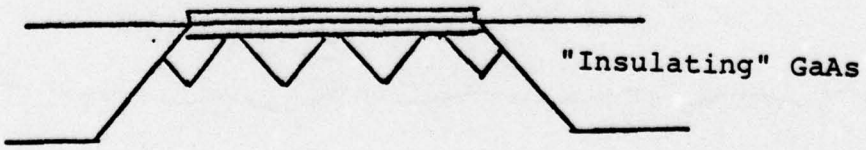

Source-Drain Metalization

(6)

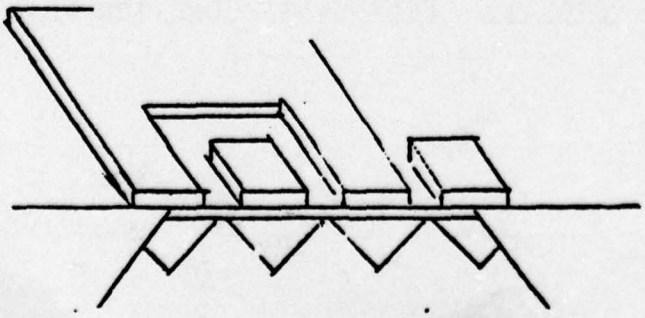

Figure 2

Eliminating the temperature gradient that had developed across the source has lowered the background, and it remains to grow and characterize insulating GaAs on Cd-doped substrates.

Problems with contact resistance were experienced when alloying was done in the presence of the needed thick overlay metal. It may be that the problem can be solved with either a barrier metal or electroplating the contacts with Au after alloying.

2. SUBSTRATE CONSIDERATIONS

2.1 High Background Doping of Cd-Doped Substrates

Having corrected the temperature profile along the Ga source and with new CrO_2Cl_2 in the bubbler, the reactor background doping was about 34 x $10^{14}/cm^3$ and the undoped layers on Cr-doped substrates had mobilities of 19400 and 94490 cm^2/V-sec at 300 and 77°K. Since a background doping of about $10^{15}/cm^3$ is sufficient to produce good quality Cr-doped material (resistivity 10^7- 10^8 ohm-cm) in the vapor phase epitaxial system, getting high resistivity material on Cr- or Te-doped GaAs test substrates was easily accomplished. However, there was no success at getting lightly-doped or semi-insulating GaAs on Cd-doped substrates. The layers (undoped as well as Cr-doped) on these substrates were relatively heavily doped (approximately in the $10^{16}/cm^3$ range) and p-type; even the layers on Cr-doped GaAs substrates inserted next to the Cd-GaAs during the VPE process turned out heavily p-type:

The impurity making the layer p-type has been verified to be Cd. There are a number of ways in which Cd can get into the epilayer.

(a) Solid state diffusion from the substrate into the epilayer during growth;

(b) release of Cd into the gas stream during vapor etching and subsequent contamination of the grown layer due to incomplete removal by the H_2 gas flow; and

(c) evaporation of Cd from the substrate surface due to its high vapor pressure.

The second and third mechanisms can dope the epilayers on the adjacent Cr-doped GaAs substrates also.

To reduce contamination due to the second mechanism, the vapor etching step was eliminated and a previously-saturated Ga source was used. A typical run under these conditions consisted of a thermal equilibration period (15 min) followed by the epitaxial growth to produce an epilayer about 8 microns thick. But this did not reduce the background doping by any significant amount.

To prevent the release of Cd from the back side of the wafer and from its edges, a thick layer of silicon nitride (about 6000 Å) was deposited. The undoped GaAs layer deposited on such a wafer was still heavily p-type, indicating that:

(a) 6000 Å thick Si_3N_4 does not prevent the loss of Cd from the surface of GaAs, and/or

(b) the Cd lost from the front surface during thermal equilibration and during the early stages of deposition of the VPE layer "poison" the liner and the substrate holder and dope the epilayer continuously.

An attempt was made to solve the second problem by using a more elaborate growth procedure involving (1) growing about 4 microns of undoped GaAs, (2) removing the substrate holder - push rod assembly from the reactor, (3) placing the wafer in a clean assembly, and (4) depositing a second 4-micron thick layer. The top layer on the Cd-GaAs substrate (with Si_3N_4 on the back and edges) was still highly doped in this case, although the corresponding layer on the neighboring Cr-GaAs was extremely lightly doped. With the addition of Cr to the system during the second stage of growth, only the layer on the Cr-doped GaAs was semi-insulating. From these experiments, it appears that layers grown on Cd-doped substrates cannot be made semi-insulating. Although the diffusivity of Cd in GaAs is nominally very low,[1] anomalously high doping of the epilayer results even for epilayer thicknesses of about 10 microns.

The large reduction in capacitance brought about by the grooves as reported in Annual Report No. 2 suggested that the vee doping was very much less than $10^{16}cm^{-3}$, apparently contradicting the indications of high acceptor contamination by the Cd substrates as just described. However, the grooves were grown during the time when the (donor) background doping was probably high as a result of the temperature gradient across the source (as previously discussed). This high n-type background may have compensated the p-type autodoping from the substrate to give a net low doping. Now that the n-type background has been reduced, the p-type autodoping has become evident.

2.2 Background Doping Investigations Using Ge-Doped Substrates

Experiments using substrates of Ge-doped (p^+) GaAs grown by the liquid phase epitaxy technique on Cr-doped GaAs

indicated that very good quality undoped (as low as $10^{14}/cm^3$) and Cr-doped layers could be obtained on Ge-doped GaAs. The main drawback of Ge doping is that bulk crystals grown by the Czochralski technique are n-type. The requirement that Ge-doped GaAs be grown by the LPE technique on some other p-type GaAs substrate, however, has the advantage that the quality of the material on which the device will be fabricated will be higher than Czochralski-grown substrates.

Further experiments were performed on VPE deposition of lightly doped n-type GaAs on Gedoped (p^+) GaAs, the latter being grown by the liquid phase epitaxial technique on Zn-doped (p^+) GaAs. While some of the epilayers were lightly doped ($N_D-N_A \approx 1 \times 10^{15}$/cc), there was difficulty reproducing these results. More often the epilayers were p-type doped to low 10^{16}/cc. The epilayer dopant making it p-type must be Zn since Ge-doped layers in the VPE system are n-type. The high diffusion coefficient of Zn in GaAs should not be a serious problem since the Ge-doped GaAs layer was quite thick (about 10 microns). Coating the back side and the edges of the wafer with thick Si_3N_4 to prevent outward diffusion of Zn improved the situation somewhat; but still the epilayers were sometimes p-type and sometimes n-type, doped to mid-10^{15}/cc. These values were unsatisfactory, since the epilayer must be about $1 \times 10^{15} cm^{-3}$ or lower and n-type for Cr doping. The Zn-doped GaAs used for these experiments was doped to $10^{19} cm^{-3}$. Since the device does not need such a highly doped substrate, it was decided to lower the doping level of the substrate to see if the quality of the epilayer improved. Even if lower Zn-doped substrates are not able to solve the problem, two options remain:

(1) Use thick (50 microns or so) Ge-doped p-type GaAs grown by LPE on Cr-doped GaAs as the substrate. High purity material may be grown on this, as per the preliminary experiments.

After the device is fabricated, the Cr-doped GaAs substrate can be removed by preferential dissolution (a technique commonly employed in our lab for making photocathodes).

(2) Use a bypass reactor to reduce the doping of the epilayer grown on the Ge-doped GaAs/Zn-doped GaAs substrates (or even on Cd-doped GaAs substrates). In this technique extra H_2+$AsCl_3$ is admitted into the VPE reactor at a point after the Ga source and before the substrate. The extra HCl in the deposition zone reduces the incorporation of impurities into the epilayer while at the same time lowering the growth rate somewhat. Nozaki et al,[2] who first described this technique, observed that the doping can be lowered from $10^{16}/cm^{-3}$ to $10^{12}/cm^{-3}$. It seems fair to assume that the technique will work for p- as well as n-type dopants. Initial experiments using Cd-doped GaAs substrates show that by using this technique the 7-micron thick epilayer is n-type doped to 1 x $10^{15}cm^{-3}$, which contrasts with the p-type epilayers doped to above $10^{16}cm^{-2}$ on Cd-GaAs using the ordinary VPE system.

Using the new batch of substrates, Ge-GaAs layers 30 microns thick were grown by LPE. Pieces cut from these were coated with Si_3N_4 on the back and the edges. Undoped epilayers grown on these pieces were clearly shown to be n-type doped to $10^{15}cm^{-3}$. Attempts to Cr-dope the epilayers were unsuccessful initially. The problem was later traced to a faulty mass flow controller supplying H_2 to the CrO_2Cl_2 bubbler. After repairing this, the epilayers on Ge-GaAs/Zn-GaAs were successfully Cr-doped. When the epilayer thickness was about 6 microns (corresponding to the tub depth), Cr-doping produced a net doping of less than $10^{13}cm^{-3}$ since the zero-voltage-capacitance on a 20-mil Au dot was less than 4 pF.

Realizing that the "vees" are only about 2 microns deep and that these will also have to be filled with high resistivity material, attempts were then made to grow Cr-doped layers 2

microns thick. In these cases, it was observed that although most of the top layer was lightly doped, the n-type doping appeared to increase upwards to at least $10^{17}cm^{-3}$ as the p^+ substrate was approached as indicated from the doping profile plots derived from the capacitance. Such a high n-doping right at the p^+ interface would lower the p-n junction breakdown voltage and increase the parasitic capacitances (thereby negating the function of the vee grooves, no matter how low a doping was achieved away from the interface). Since Ge diffusing into the grown region will produce p-type doping, any n^+ interface layer must be due to Ge contamination coming in from the vapor phase (in which case it acts as an n-type dopant).

In order to be sure that the n^+ layer at the interface was not an artifact of the profiler (i.e. an anomally due to punch-through and excessive leakage stemming from the profiling depletion region edge meeting with the depletion region of the underlying p-n junction), an n^+ layer was grown on top to facilitate ohmic contact and to prevent punch-through, and mesas were etched down to the p^+ substrate. This enabled the Cr-doped layer to be profiled from the p^+ substrate towards the surface. The low capacitance of the p^+/epilayer junction implied that the low doping at the surface continued all the way to the p^+ substrate. However, the diode dc characteristics were so unusual and uninterpretable (even to the point of showing SCR-type negative resistance) that there was a little uncertainty in arriving at this conclusion. The negative resistance SCR characteristics appeared to be due to trapping effects in the Cr-doped layer and not due to some unintentially grown multilayer structure. (Negative resistance was also observed by Hasegawa et al[3] when they grew p-type Fe-doped GaAs by the LPE process on n^+ Si-doped substrates and concluded that this was related to the presence of a high density of iron hole traps.) The low capacitance

from the p-n junction side would suggest no n^+ layer adjacent to the p^+ substrate, but if this were true it seems difficult to explain why punch-through did not occur when profiled from the Schottky-barrier side.

The identical procedure of profiling with a Schottky-barrier and then etching mesas and profiling from the p^+ substrate side was carried out for an undoped buffer layer growth on the p^+ Ge-doped substrate (for this growth the doping was lowered by an $AsCl_3$ bypass around the source[2] rather than by Cr-doping). While at zero bias the layer was fully depleted with 12 pF of capacitance for the Schottky-barrier, when profiled from the substrate side the zero-bias capacitance increased to around 30-40 pF. This implies an n^+ layer adjacent to the substrate, but not of such a magnitude as to seriously degrade device performance. It may be that the n^+ layer was completely compensated when the layer was Cr-doped, explaining why it wasn't seen previously.

2.3 Formation of Vees on Ge-Doped Substrates

Since the surfaces of the LPE layers of Ge-doped GaAs were somewhat rough showing the typical terrace pattern, they were repolished with diamond paste and then with Br-methanol. The entire polishing procedure removed about 10 microns, leaving about 20 microns of the layer. Using Si_3N_4, the mask for etching the vees was put on the repolished surfaces. Vapor etching in the reactor using techniques established previously (using Cd and Te-doped substrates) showed however that the etching proceeded sideways very fast to give shallow trapezoids rather than vees. This does not appear to be due to surface damage left during repolishing as indicated by experiments done on as-grown LPE surfaces. This was also found to be the case with SiO_2 as the masking material. Identical experiments using Te-doped GaAs produced

the required grooves, leading to the conclusion that this behavior was peculiar to the Ge doping. Whether or not this is due to the interaction of Ge with SiO_2 or Si_3N_4 to produce GeO_2 or Ge_3N_4 (or more complex Ge-Si compounds with O_2 or N_2) is not known.

Experiments with $NH_4OH:H_2O_2:H_2O$ (20:7:1000 by volume) were successful in producing good vees with the mask aligned along the [110] direction perpendicular to that for the V-etch in the VPE system. The obvious advantage of this weak solution etch is that the etch rate can be controlled quite precisely to adjust the gate length (the separation between the adjacent vees), being more difficult to do with the vapor etch. Using the solution etch to produce the vees and the VPE system for the subsequent refilling, semi-insulating vees were obtained. With the grooves aligned in the perpendicular direction, growth proceeded from each end of the groove towards the middle rather than from the sides of the vees as it had previously. Imcomplete growth thus manifested itself by completely empty vees in the middle portion of the grooves.

3. SOURCE AND DRAIN OHMIC CONTACTS

In order to minimize the power losses in the 4-micron wide source and drain fingers, the finger metallization should be at least around 0.5 micron high. Previously it was reported that when 5000 Å of Au was used as the overlay thickness, the specific contact resistance was found to degrade around an order of magnitude from the 1000 Å Au overlay value.

This result was reconfirmed by repeating the experiment. A specific contact resistance of 1.6×10^{-6} ohm-cm^2 was obtained for 1240 Å of Au-Ge/Ni/Au, 6.4×10^{-6} ohm-cm^2 for

4680 Å, and 1.54 x 10^{-5}ohm-cm^2 for 9000 Å. To see if Ge or Ni depletion by the thicker Au is the problem, a double thickness of Au-Ge (900 Å) was sputtered, followed by a double Ni thickness (150 Å) and a 4000 Å overlay. The contact resistance remained high. However, when the Au-Ge was evaporated (vs being sputtered as in all the previous trials) using double the thickness of Au-Ge/Ni and a 4000 Å Au overlay, a specific contact resistance of around 10^{-6}ohm-cm^2 was obtained. Evidently the sputtering is responsible for the degradation in the specific contact resistance with increasing Au overlay thickness. Thus it may be that sputtering is an acceptable process for thin Au overlays but not for thick Au overlays when alloying occurs after the overlay deposition.

Using Auger electron spectroscopy, Robinson[4] has found for the Au-Ge/Ni alloy that at and above 352°C a significant amount of Ga outdiffuses and accumulates on the surface without any outdiffusion of As. Since Ge is known to act as a donor in GaAs when excess As exists, it is probably this outdiffusion of Ga that is responsible for the contacts being ohmic. The diffusion of Ga in Au would not seem to account for this phenomenon, especially for the large Ga concentration at the surface. If it can be believed that the 352°C nominal sintering temperature did not in fact exceed 356°C, then the Au-Ge eutectic cannot be responsible for the large Ga removal. However since the Au-Ga eutectic is at 341°C, then quite possibly the Ga concentration at the surface can be explained by the eutectic removal of the Ga and re-precipitation at the surface upon cooling. If so, then the amount of Ga removed should be proportional to the thickness of the Au in the contact. Initially, the more Ga removed, the better the ohmic contact since this aids the Ge in acting as a donor. However, it seems obvious that as more and more Ga is removed, an As layer is formed which

effectively acts as an insulating layer, thus degrading the contact resistance. This might explain the contact resistance first improving and then degrading as the Au overlay thickness is increased (as reported in the previous annual report), although this minimum might also be caused by the higher sheet resistance of the metallization as the Au overlay decreases (which was not taken into account in computing the specific contact resistance). Although the mechanism by which the Ga separates from the As and goes into solution with the Au is not understood, it may be that the sputter cleaning and deposition damages the surface to such an extent that this interaction is enhanced and, together with the thick Au overlay, results in an increased specific contact resistance when alloyed.

By measuring the resistance of long narrow stripes of metallization, the conductivity of the metal could easily be determined. For the evaporated 1000 Å Au-Ge/Ni, 4000Å Au overlay configuration previously determined as suitable for a low specific contact resistance, the as-deposited overlay Au resistivity was determined to be around 3.9×10^{-6} ohm-cm. After alloying, it rose to 18×10^{-6} ohm-cm, which is about 7.4 times that of the 2.44×10^{-6} ohm-cm published bulk value for Au. With just the 4000 Å of Au overlay directly on GaAs, the resistivity rose to 6.5×10^{-6} ohm-cm after alloy. It thus appears that the Au-Ge/Ni interaction with the Au overlay is responsible for most of the degradation, but still there is a factor of 1.6 in degradation even without it, perhaps as the result of Ga coming out of the substrate.

Along with the resistivity measurements, specific contact resistance measurements were also made and revealed that the value was not always as low as that obtained the

first time (a value as high as 10^{-5}ohm-cm^2 was measured). It appears that the only sure and reliable way to eliminate interaction between the ohmic contact layer and the overlay layer is to insert a barrier metal such as W or Mo between them.

A run was made with the following contact structure: 1600 Å evaporated Au-Ge/Ni/Au, 1200 Å sputtered W-Ti, and an evaporated 3800 Å overlay. After alloy, the Au overlay resistivity was 2.3 x 10^{-6}ohm-cm (the alloy thus anneals the evaporated Au to the published value) and the specific contact resistance was around 6 x 10^{-7}ohm-cm^2, which indeed is a very low value. The same Au-Ge/Ni/Au contacts without the W-Ti or Au overlay gave a high specific contact resistance for some reason (the contact was "puddled" in appearance). Thus it appears that the W barrier not only can prevent the degradation caused by the thick overlay, but can, at least in some cases, improve the specific contact resistance of nonoverlaid contacts.

4. ACTIVE LAYER GROWTH AND DEVICE FABRICATION ON Ge-DOPED SUBSTRATES

4.1 Active Layer Growth

The next step in the device fabrication is the VPE deposition of the n-type (10^{17}cm^{-3}) active layer on the Ge-doped substrates after removal of the SiO_2 or Si_3N_4 used as the mask for the vee etch and growth. This process is made more difficult compared with conventional device fabrication techniques owing to the requirement that the active layer must be grown with very little vapor etch of the substrate. Appreciable vapor etch to clean the substrate surface can lead to removal of the vees. The previous procedure reported in Annual Report No. 2 of controlling the source saturation time so that a highly doped layer is grown and then just

etched off was found to be too exacting to be practical. The alternative is to use a previously saturated source or to use a slider boat to cover the wafer during the source saturation.

Difficulties were experienced in growing a continuous active layer over the V-grooves by vapor phase techniques. Various surface cleaning procedures were tried along with a small amount of vapor etch, but the growth remained discontinuous independent of whether the source was previously saturated or a slider boat was used. It may be that a residue is left on the surface during the removal of either the SiO_2 or the Si_3N_4 mask (both were used). Such discontinuities provide shoring paths for the FET ohmic contacts directly to the substrate gate below, and also make it impossible to characterize the active layer for doping and thickness (a discontinuous active layer on an insulating substrate as used for coplanar devices would not have these problems).

When the surface of the wafer was Augered in the MBE system, carbon was seen on the surface. This could very well be the cause for the discontinuous growth. There is evidence that when the surface is lightly etched, the C is not removed but simply re-deposits, explaining why the various surface cleanings were ineffective. Evidently the severe vapor etch typically done before vapor growth for conventional FETs is able to remove this C. The C was sputtered off in the MBE system and an active layer was grown by MBE that was deemed acceptable for device processing. Schottky-barrier leakage, although much less than for the vapor-grown layers, still prevented evaluation of the active layer, so it may be that the layer still has discontinuities in it.

4.2 Device Fabrication

With the V-grooves filled and the MBE active layer deposited over them, the mesas were next formed by etching the field to a depth of around 5 microns and regrowing semi-insulating GaAs back flush with the surface to provide low-capacitance areas for the source and drain pads to sit on. The field growth occurs sideways out from the mesas and at the same time grows slowly upward above the mesa surface. To avoid an excessive height of the field above the mesa surface and subsequent overlap of the growth over the oxide mask especially at the corners, the growth was continued only out far enough to provide a base for the source and drain pads.

Figure 3 shows the completed device structure. The edge of the field growth can clearly be seen. For this run the field growth did not continue uniformly out from the mesa edges as it had for the dummy runs used to calibrate the process. Device characteristics were not obtained from this run for several reasons. First of all, it appeared that the source and drain fingers were broken in crossing the step between the mesa and the field (this is probably more a fault of the ohmic contact metallization than of the step since the contacts showed a tendency to puddle when alloyed--a W-Ti barrier and overlay Au were not used to shorten the feedback loop for materials evaluation). Secondly, the field growth was not insulating as evidenced by a test structure included with the device structures, causing a leaky connection between the gate and the source and drain pads. Another device run has almost been completed where more Cr has been added to the field growth, hopefully curing this problem. Thirdly, another test structure revealed that the p-n junction between the MBE layer and the substrate was quite leaky. This may be indicative of a potential problem

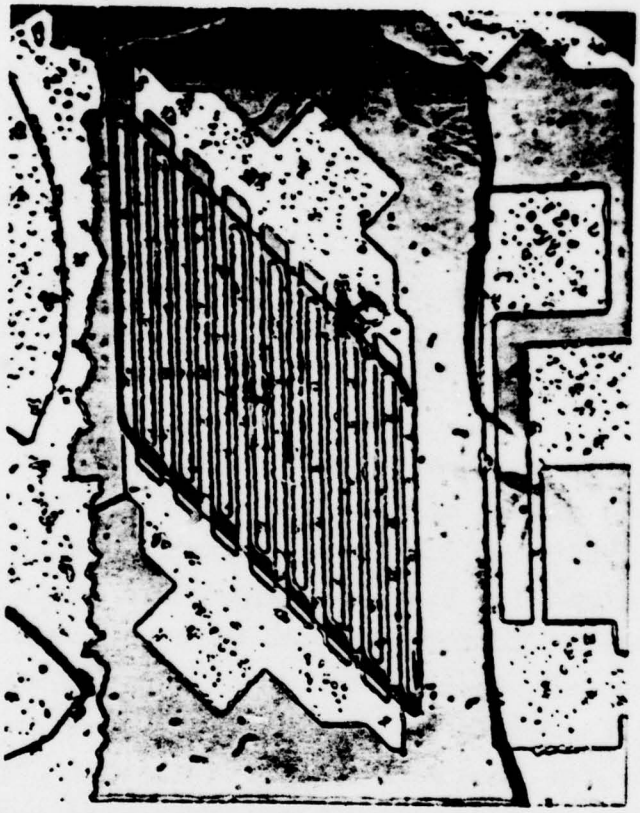

Fig. 3. Completed noncoplanar device structure.

in achieving a good p-n junction which coincides with a growth interface. The latest device run had a better sputter clean before the MBE growth (previously the Auger sputter gun was used because the normal incidence sputter gun was not functioning) and this might cure the problem.

5. CONCLUSIONS

In spite of a considerable amount of effort, low doped ($10^{15}cm^{-3}$ or lower) and insulating material could not be grown on Cd-doped substrates by VPE techniques because of heavy p-type Cd contamination, supposedly because of the high vapor pressure and/or diffusion of Cd. Evidently the high n-type background resulting from a temperature gradient across the source compensated this Cd contamination enough to account for the low background doping achieved initially. The compensation of two types of impurities to give over an order of magnitude reduction in the net doping, however, is not a dependable technique to rely upon to solve the problem of Cd contamination. Going to p^+ Ge-doped LPE layers grown on Zn-doped substrates enabled the growth of low-doped material in the vees and in the field at a slight sacrifice to the surface morphology.

The previous procedure reported in Annual Report No. 2 of controlling the source saturation time so that a highly doped layer is grown and then just etched off was found to be too exacting to be practical for VPE growth of the active layer. Instead, a previously saturated source or a slider boat to cover the wafer during the source saturation was used. In spite of numerous cleaning techniques, a continuous active layer could not be grown by VPE, perhaps because of carbon contamination on the surface as revealed by an Auger analysis. The carbon was sputtered off in the MBE system and an active layer was grown by MBE that was deemed acceptable for device processing.

The use of a W-Ti barrier between the Au-Ge/Ni ohmic contact and the thick Au overlay was found to reduce the specific contact resistance to below 10^{-6}ohm-cm^2 and also to increase the overlay conductivity to essentially its bulk value.

A device run was completed from start to finish for the first time using VPE grown vees, an MBE active layer, and VPE field growth. Device characteristics were not obtained from this run for several reasons. The source and drain figures were broken in crossing the step between the mesa and the field, the field growth was not insulating (causing leakage between the gate and the source and drain pads), and the p-n junction gate was quite leaky (which may be indicative of a potential problem in achieving a good p-n junction which coincides with a growth interface.

6. RECOMMENDATIONS FOR FUTURE WORK

Another device run has almost been completed with more Cr added to the field growth to render it insulating. This run also has a better sputter clean before the MBE growth to hopefully lower the gate leakage current. The elimination of junction leakage problems resulting from coincidence of the p-n junction with the growth interface may be the problem whose solution will require a major part of the future effort. The use of diffusion or ion-implantation should be considered as solutions to this problem.

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