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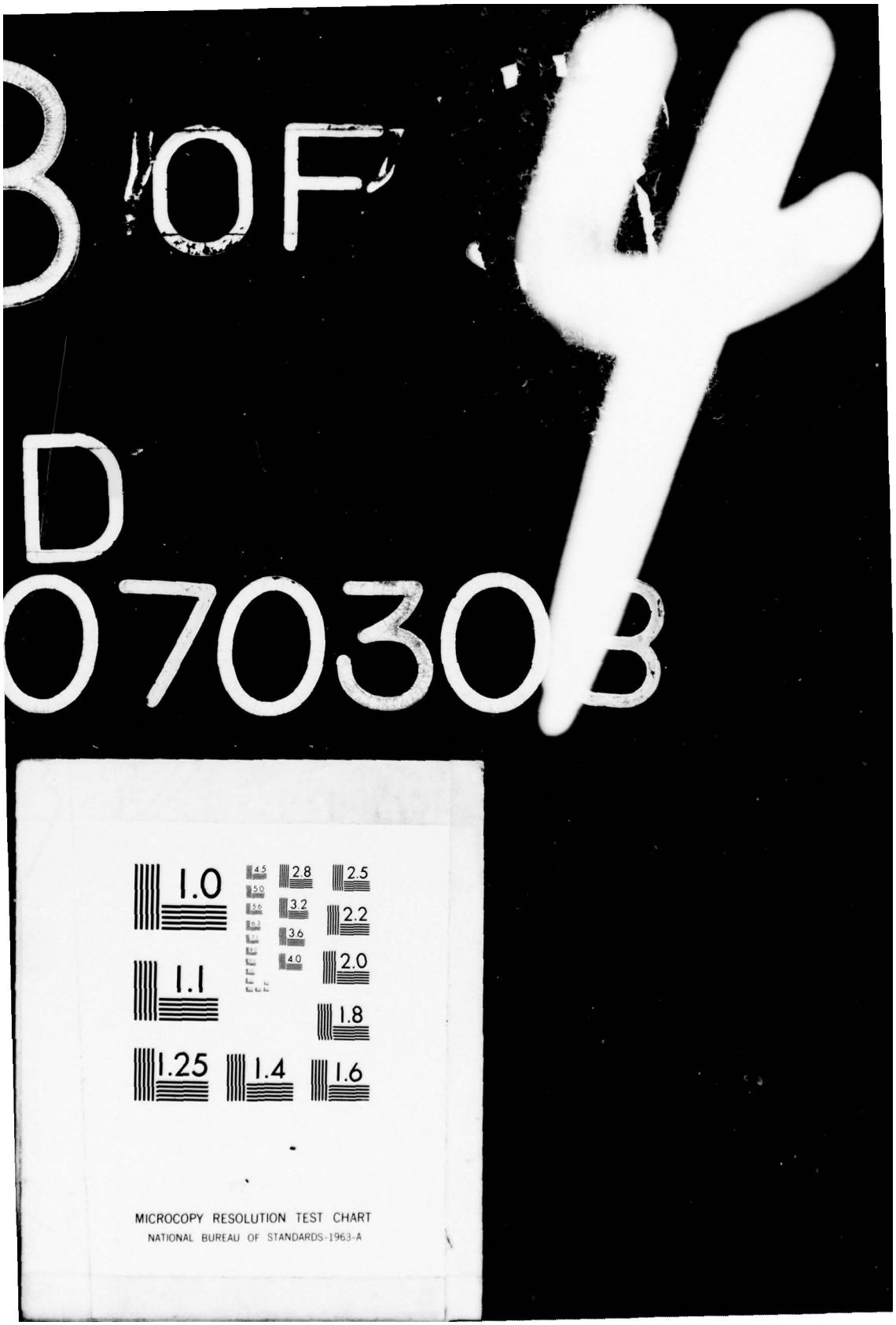
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METALLIC AND SEMICONDUCTING MATERIALS DERIVED FROM NON-METALLIC ELEMENTS

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I. Introduction

This report is directed towards the very new area of materials science which is concerned with the preparation and characterization of synthetic metals, many of which contain no atoms of any metallic element in their chemical constitution. The three main presently known classes and their potential technological significance will be described. One of the classes also encompasses a series of p- and n- semiconductors.

Although there is no immediate obvious application of these systems to ultraminiaturization of electronic devices, it would appear they warrant considerable further investigation and evaluation by specialists in the field of electronic devices.

The motivation for producing new conductors is in part a desire to achieve unusual, or even unprecedented, materials properties of technological importance. Metallic conductors are based on open-shell atoms, while non-metallic compounds typically exhibit covalent or polar bonding based on closed shells. Since open-shell electronic bands are a prerequisite for any conductor, molecular or polymeric conductors will almost certainly be unusual chemically. The stabilization of interacting open-shell non-metals in a solid, so as to prevent the exclusive formation of polar-covalent bonds, is an enormously challenging task. On the other hand, recent developments with doped polythiazyl, $(SN)_x$, and polyacetylene, $(CH)_x$ suggest that the judicious incorporation of electron donating and withdrawing groups may yet provide a fairly general scheme for achieving incompletely filled bands, as required for conductors.

The stabilization of partly-filled bands in nonmetallic conductors is primarily a chemical and structural problem. The synthesis, characterization, optimization and exploitation of conducting systems provides many opportunities for both experimental and theoretical studies. When nonmetallic open-shell systems are available, traditional chemical ideas about crystal packing, about isoelectronic substitutions, or about analogous reactions have generated essentially all of the currently known "families" of molecular metals. These have been derived from a few conductors that were originally prepared for other reasons. Finding new conductors among nonmetallic elements or compounds will consequently demand great ingenuity, with only very modest theoretical suggestions. On the other hand, the theoretical appreciation of the role of dimensionality in phase transitions and in magnetic phenomena has greatly increased interest in model compounds, whose experimental study has further enriched theory.

The bulk properties of most known conducting polymers are quite different from their intrinsic crystal properties. These bulk properties typically reflect the state of crystallite aggregation as much as the crystallite properties. For example, a variety of indirect measurements indicate metallic conductivity for $(SN)_x$ and for doped $(CH)_x$ in directions in which d.c. conductivity measurements indicate a non-metallic temperature dependence. This difference between bulk and intrinsic properties, which includes everything from mechanical strength and environmental stability to superconductivity, is a consequence of gross structural inhomogeneity in these materials. As a result, basic uncertainties exist in our knowledge of their fundamental

materials properties, which limit our ability to understand their polymer physics and to optimize their properties for possible applications.

This report concentrates on three presently known classes of metallic compounds derived from non-metals, namely those based on $(SN)_x$, $(CH)_x$ and graphite.

II. Critical Assessment of Existing Knowledge in the Field

A. $(SN)_x$ and Derivatives[1]

Polythiazyl, "polymeric sulfur nitride," is the first example of a covalent polymer containing no metal atoms which has been shown to be a conducting ($\sigma_{RT} \approx 5 \times 10^3$ ohm^{-1} cm^{-1})* and a superconducting polymer ($T_c \approx 0.3$K). Electrical contacts can be made with metal clips or by silver paint. These unique electronic properties have opened up new vistas for the scientific investigation of potentially conducting polymers. Currently available $(SN)_x$ consists of golden crystals made up of crystalline microfibrils which are fully oriented in a common chain direction, but poorly coupled together electronically. Gross twinning occurs and about 20% of the chains in each microfibril are in defect positions. However, band structure calculations based on the ideal $(SN)_x$ structure have led to a semi-quantitative understanding of its properties; in particular $(SN)_x$ has been shown to be an anisotropic semi-metal, stabilized against the Peierls distortion by interchain interactions. $(SN)_x$ crystals may be conveniently sublimed at ca 150°C and cohesive golden films may be condensed on room-temperature substrates of plastics, metals, glass, etc. These films are also highly conducting. Completely aligned epitaxial films can be deposited on appropriately "scratched" plastic or glass surfaces. These show highly anisotropic electrical and optical properties. The films on flexible substrates are also completely flexible and may be bent without cracking. $(SN)_x$ crystals and films are stable in air for extended periods.

Presently, the only known conducting derivatives of $(SN)_x$ are obtained by partial oxidation with halogens and interhalogens. Of these compounds $(SNBr_{0.4})_x$ has been the most thoroughly investigated. This material exhibits an order of magnitude higher conductivity than $(SN)_x$ and other interesting electronic properties. However, details of the crystal structure and the role of bromine are not yet entirely clear. Halogen derivatives of $(SN)_x$ have been obtained also by halogenation of S_4N_4 which eliminates the intermediate synthesis of $(SN)_x$.

B. $(CH)_x$ and Derivatives[2]

Polyacetylene, $(CH)_x$, is the simplest possible conjugated organic polymer and is therefore of special fundamental interest. It may be prepared in *cis*- or *trans*-isomeric forms as silvery, polycrystalline, flexible films by the polymerization of acetylene gas, C_2H_2, at ca 1 atm. pressure using a Ziegler catalyst at temperatures ranging from -78°C to ca 150°C. Low temp-

*For comparison, the conductivity, σ, of mercury at room temperature is ca 1×10^4 ohm^{-1} cm^{-1} and that of copper is ca 6×10^5 ohm^{-1} cm^{-1}.

erature polymerization conditions favor the formation of films of the cis-isomer which can be subsequently isomerized to films of the trans-isomer by heating at ca 200°C for 2 hours in an inert atmosphere or in vacuo. Cis-rich films have a tensile strength of ca 3 kg/mm^2 and can be stretched to 3-4 times their original length at room temperature. Electron microscopy studies show that the as-formed $(CH)_x$ films consist of randomly oriented fibrils (typical fibril diameter of a few hundred angstroms). The bulk density is ca 0.4 gm/cm^3 compared with 1.2 gm/cm^3 as obtained by flotation techniques. This shows that the polymer fibrils fill only about one-third of the total volume. In the absence of added deoxidant the films slowly undergo oxidation in air during several days. Oxidation may be prevented by covering with appropriate polymer lacquers, etc. Both isomeric forms are semiconductors; however, through chemical doping, their electrical conductivity may be controllably varied over an extraordinary 13 orders of magnitude with properties ranging from semiconducting ($\sigma<10^{-10}$ ohm^{-1} cm^{-1}) to metallic ($\sigma>1 \times 10^3$ ohm^{-1} cm^{-1})*. Electrical contacts to the films may be made by metal clips or by "Electrodag" (graphite dispersed in a polymer "cement"). The metallic state is preserved down to at least 40 mK. Studies of the chemical stability and electrical conductivity of the doped films at room temperature are presently being undertaken. The semiconductor to metal transition occurs at a few mole percent dopant concentration. Both electron acceptors (e.g. I_2, Br_2, AsF_5, $AgClO_4$, etc.) and electron donors (e.g. Li, Na, K, etc.) can be used to yield p-type or n-type material respectively. The $(CH)_x$ films can be partially chain-aligned by mechanical stretching and may also be doped. Such films exhibit anisotropic electrical and optical properties with an increase in conductivity in the direction of alignment of up to one order of magnitude. Preliminary band structure calculations suggest that $(CH)_x$ is an anisotropic semiconductor with a small band gap (~1eV) but with wide conduction and valence bands (5-10eV in the chain direction). Presently available $(CH)_x$ is morphologically complex and is not well understood.

C. Graphite Intercalation Compounds[3]

Graphite can be readily intercalated with a variety of electron acceptor or donor species to give solid materials which are generally unstable in air unless surrounded by a protective material. Graphite and its intercalates exhibit interesting anisotropic two dimensional properties in contrast to the more one-dimensional properties of $(SN)_x$ and $(CH)_x$. The electronic properties of intrinsic graphite crystals are reasonably well established with one main exception: the specific effects of crystal defects on the scattering mechanism. Both donor and acceptor intercalation compounds of graphite with a wide variety of interesting electronic properties have been made. Three general properties of these compounds which are of particular interest are mentioned below.

(1) Acceptor (e.g. HNO_3, SbF_5, AsF_5, Br_2) compounds have higher in-plane electrical conductivity ($\sigma_{RT} \approx 10^6$ ohm^{-1} cm^{-1}) than the donor (e.g. K, Cs, Rb) compounds ($\sigma_{RT} \approx 10^5$ ohm^{-1} cm^{-1}).

(2) The maximum in-plane conductivity occurs at a stage higher than one in acceptor compounds.

*For comparison, the conductivity, σ, of mercury at room temperature is ca 1×10^4 ohm^{-1} cm^{-1} and that of copper is ca 6×10^5 ohm^{-1} cm^{-1}.

(3) There is an increase in anisotropy (ratio of in-plane conductivity to conductivity normal to the planes) which accompanies increased in-plane conductivity. For example, with AsF_5 doping, an exceedingly large anisotropy of $\sim 10^6$ is observed.

In general, the donor (group I) compounds are better understood than the acceptor compounds but the acceptor compounds appear to have the potentially more interesting properties, e.g. high electrical conductivity and anisotropy.

III. Scientific and Technological Potential

A. $(SN)_x$ and Derivatives[1]

$(SN)_x$ is a unique material and has served as a model compound for understanding the metallic and superconducting properties of polymers. $(SN)_x$ and its derivatives have scientific and possible technological potential. It does not appear likely that high superconducting transition temperatures will be achieved with polymers unless novel methods for increasing the electronic density of states are discovered. $(SN)_x$ films have been used in the formation of Schottky barrier photovoltaic devices. Other potential technological applications are under investigation.

B. $(CH)_x$ and Derivatives[2]

The scientific potential of doped $(CH)_x$ derives from the fact that this new class of materials has by far the highest conductivity of any known organic polymer. It may also be doped (either p- or n-) to give semiconducting films. An understanding of the conduction and doping mechanism and the effect of alignment on the electrical and optical properties presents fundamental scientific challenges. p-n junctions having typical rectifier diode characteristics have been prepared by pressing together films of p-$(CH)_x$ and n-$(CH)_x$. A photovoltaic effect has been observed with an n-Si/p-$(CH)_x$ heterojunction. Furthermore, the ease of fabricating large sheets of p-n junction $(CH)_x$ films suggests possible use for terrestrial solar cells, etc.

C. Graphite Intercalation Compounds[3]

On the scientific level these compounds have significant potential for improving our understanding of anisotropic two dimensional systems in which electrical conductivity and anisotropy can be controlled over wide ranges. Stage 3 graphite-SbF_5 has a conductivity comparable to the best elemental metal at room temperature. As far as technological potential is concerned, three areas can be mentioned:

(1) Stage 3 graphite-SbF_5 can be swaged into a practical wire form, when protected with a thin sheath of copper, having a room temperature conductivity of 6.5×10^5 ohm^{-1} cm^{-1}. For comparison, the room temperature conductivity of copper is ca 6×10^5 ohm^{-1} cm^{-1}. In addition, the conductivity decreases less rapidly with increasing temperatures than for the best elemental metals. The stage 3 compound has density less than 3 grams/cm^3 so that considerable weight saving is possible compared to copper.

(2) The electrical conductivity of graphite fibers of the kind used to reinforce epoxy composites can also be increased by intercalation, while maintaining their high strength and elastic modulus. Conductivities of 1×10^5 ohm^{-1} cm^{-1} have been obtained and values as high as that of copper are forecast. These high conductivity fibers have been incorporated into epoxy composites which then demonstrate an increase of conductivity of about a factor of ten. The electrical conduction of the composite suggest increases applications that require high strength, light weight and conductivity such as aircraft structural members, large antennae and others.

(3) On intercalation with acceptors, the reflectivity of graphite on the c face - the outside surface of graphite fibers - is increased to substantially 100% in the infrared (specifically at the 10.6 μ laser wavelength).

IV. Useful Research Directions for Universities and Industry

From past experience it has been observed that technology advances by quantum jumps when either new materials or new techniques have become available. In the previous sections, it has been shown that completely new types of metallic conductors and semiconductors are becoming available and several potential applications based on laboratory studies have been presented. What is now required is further basic research on these materials to explore the breadth of the field while at the same time carrying out in-depth research on carefully-chosen aspects which appear to be of particular importance.

Academic institutions should be encouraged to do what they can do best (basic research) and industry should be encouraged to do what it can do best (application of new knowledge to technology). A faculty member at an academic institution can do first class fundamental research in a field which has no apparent relevance to any technological problem or objective or he can do first-class research in a field which may have relevance to some technological problem or objective. The fields mentioned in the previous sections of this report clearly fall into the second category.

It is proposed that the areas of research described be studied at least in part by government research contracts involving collaborative work by an academic institution and industry. For example, a joint contract might be given to an academic institution and to industry to evaluate the possibility of fabricating commercial solar cells for terrestrial use from $(CH)_x$ p-n junctions. The academic institution could be primarily responsible for ascertaining methods for making p-$(CH)_x$ and n-$(CH)_x$ while an industrial collaborator skilled in classical semiconductor technology could attempt the fabrication of photovoltaic devices, etc.

Specific areas for research in the systems mentioned in this report are described below.

A. $(SN)_x$ and Derivatives

There are several directions for significant research on this polymeric system: the chemistry of halogen derivatives and its relationship to the electronic properties needs further study; demonstration of donor intercalation; separation of the $(SN)_x$ chains to change the dimensionality; attempted synthesis of isoelectronic analogues; a better understanding of the "S_4N_4-halogen route" to conducting polymers, which may provide the key to obtaining a much wider class of materials based on the $(SN)_x$ polymer.

B. $(CH)_x$ and Derivatives

There are a number of important directions in which research should proceed. Essentially only one set of polymerization conditions for the synthesis of $(CH)_x$ have been investigated to date. Undoubtedly $(CH)_x$ films with considerably different electronic, optical, mechanical, etc. properties will be prepared using different conditions. Only a very few different types of dopants, which give widely different conductivities, have been investigated so far. The chemical properties of the doped and undoped $(CH)_x$ need to be studied, particularly those related to stability to heat, air and light. It is extremely important to devise methods of synthesizing completely aligned $(CH)_x$ in order to ascertain its intrinsic conductivity parallel to the $(CH)_x$ chains. Much more theoretical work needs to be done in order to gain an understanding of the conduction process.

An almost unlimited number of chemical derivatives of $(CH)_x$ are potentially available in which the hydrogen atoms of $(CH)_x$ have been replaced in whole or in part by organic, inorganic or organometallic groups. It therefore appears that it may be possible to synthesize a very large number of semiconducting and metallic polymers based on $(CH)_x$ whose electronic, optical, mechanical, etc. properties may be controlled and pre-determined by chemical fine tuning of the system.

C. Graphite Intercalation Compounds

Several significant scientific problems for these materials are briefly outlined below.

(1) Identification of the chemical species and the state of ionization in acceptor compounds.

(2) Determination of role of defects and defect-intercalant interactions in transport scattering mechanisms.

(3) Examination of other systems with a) intercalants of high electron affinities, b) donor systems other than Group I, and c) intercalate into boron nitride, $(BN)_x$, an isoelectronic system, to compare with the conductivity properties of graphite intercalates.

D. Structural Characterization

Future research on A., B., C. should fully characterize the relationship between defect structure and electronic properties. No comprehensive studies of this sort exist for $(SN)_x$, $(CH)_x$ and graphite intercalation compounds. This probably reflects the scarcity of research facilities which are equipped to accomplish all of the following: (1) prepare new materials under carefully controlled experimental conditions (2) fully characterize defect structure and (3) evaluate electronic properties. In this light, collaboration between researchers in different facilities and countries should be encouraged. Major effort should be devoted to the development of methods for producing conductive materials as high-perfection single crystals suitable for electronic and structural measurements.

V. Conclusions

It appears that the new field of polymeric conductors and the closely related area of graphite intercalation compounds are both advancing at an

extraordinarily rapid rate. However, the synthesis of new chemical systems is absolutely fundamental for the continued growth of the field. The potential for increasing the scientific knowledge in these fields by the synthesis of new compounds, by better characterization of presently-known materials, and by theoretical analysis of the new phenomena is extremely high. It presents a challenge and opportunity for collaborative interaction between chemists, physicists and materials scientists. These materials have important technological potential in electronic devices. Present knowledge suggests that we are seeing only the tip of the iceberg and that the next few years will bring forth important new materials with unusual properties.

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Report on "Contacts at Very Small Dimensions"

by

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Report on "Contacts at Very Small Dimensions" (Definitions and Introduction)

by T. E. Seidel and D. B. Fraser

Topics will be discussed in regard to successful fabrication of "contact systems" at very small dimensions.

By "contact system" we mean: (i) A dielectric(s) with a topologically adequate opening, and surfaces suitable for metallization inside and outside the opening. (ii) A contact, formed by deposition and reaction of thin film(s) with the material primarily inside but also outside the opening. For example, in applications to semiconductor contacts for integrated circuits (IC), Al reacts with Si, and Si with Al, Al also reacts and bonds well with SiO_2 which results in good adhesion to the dielectric.

After contact formation, the characterization of the performance must also be made: contact resistance, body resistance, capacitance, stability under aging, (electromigration and corrosion effects), depth of reaction-penetration, contact yield, for example as determined by reverse bias leakage of p-n junctions underneath the contact.

Formation of the window is now a <u>necessary</u> part of a useful study for a contact system. Thus the emerging disciplines of lithography for large scale integration and dry etching are the domain of this topic. We will discuss the relevant aspects of lithography as it pertains to window formation.

Finally, the scale of IC design can be used to organize the various aspects of the report. Design considerations for IC layout show that the scale of integration is $\sim$50% limited by lines and spaces and $\sim$50% by contact window size - which in turn sets up the rules for the layout of the active devices. Roughly speaking: 5-3 μm design rules imply 16-64K bit RAM, this

represents the current status; ∿1 μm rules imply 256K bit, and ∿0.2 μm rules imply 10^6 bits for a 1 cm^2 chip. The latter two scales of integration are where we wish to be in the near and more distant future, respectively.

(1) Current Status of Window Technology

Today, in industry, window sizes of 3 to 5 μm are in manufacture.[1] Projection printing lithographic techniques have replaced contact printing. This reduces (nearly eliminates) mask damage.

X-ray lithography is still in the development stage but 1 μm and 0.25 μm features have been obtained.[2,3] X-ray lithographic techniques can be a high volume process. In addition, the resolution due to Compton scattered electrons is better than that afforded by electron-electron scattering using electron-beam techniques.[3] Utilization of X-rays for 1 μm lithography requires the achievement of "error budgets" of ±0.15 to ±0.2 μm for: pattern generation, alignment, processed edge position, pattern replication, wafer bending and thermal expansion.[2]

Electron-beam techniques have utilized direct writing[4] (direct e-beam exposure of resist on chip) to produce 0.5 μm features. This procedure eliminates the use of masks and mask fabrication. The resolution is primarily limited by the thickness of the resist. If thick layers are used to reduce pin-holes and promote coverage, then lateral electron scattering limits the resolution. If one wishes to use more planar structures, and very highly filtered thin resists, smaller features could be obtained by e-beam writing. The data rate or resist sensitivity must also be increased before direct e-beam writing can be a high volume process.

For 5 μm technologies, windows are etched using wet chemical methods (isotropic), this partly characterizes the

present technology. However, plasma etching and reactive ion etching are also currently being used, and will be adopted for windows of 3 μm and smaller.[5] Dry processes incorporating reactive ion and sputter phenomena are being combined with plasma processes to develop anisotropic etching, and "degrees" of anisotropic etching.[5] In wet etching a major problem has been resist lifting, while in dry processing the resist may etch away at a rate comparable to the substrate. The latter partly controls and limits the topology of the window cut.

There is a conflict between obtaining very small feature size which implies well defined, almost vertical window walls and good step coverage of the metal running between the contact-surface and the rails on the IC chip. This conflict will be discussed below.

2. Specific Areas of Scientific and Technological Need for Window and Substrate Definitions

It is likely that industry (e.g., Perkin Elmer) will provide advances in optical lithography which result in window sizes of $\lesssim$1.5 μm by use of ultraviolet wavelengths.[1] To achieve this, improvements are needed in: (1) ultraviolet sources, (2) the mechanical stability of the projection printer system, (3) optical surfaces, wafer and mask flatness (in combination with more planar technologies), (4) better linewidth control, and (5) improvement in alignment and registration techniques for nonvisible wavelengths.[1]

Advances in X-ray lithography[6] require the above same generic improvements, and in addition need improved resists (i.e., those with higher sensitivity to X-rays, high resolution and good resistance to chemical, ion and/or plasma etching), improved life and compatibility of sources with filter-window and mask, and the development of large area, stable, low defect-density masks, and improvements in mask-to-layer registration capability.

Electron-beam techniques are limited by data rates (an engineering job), electron optics performance (the fundamental limits need study), and by electron scattering effects.

Both X-ray and electron-beam systems exist as laboratory tools today.[7,8] Although they are now not manufacturing tools, one should take advantage of their capabilities for the fabrication of ∿1 μm window sizes for tester structures. It is the position of this report that window-size effects cannot be usefully studied unless contact reactions of interest are studied on scaled down - real size windows.

It will be desirable to control topology of the small window cuts such that steep angles are achieved in a controllable manner. Vertical or reentrant features are undesirable for step coverage, and so are very gradually tapered window cuts as they limit the packing density. Window topology work should be pursued which develops a capability to make controllable steep angles for the window cuts.[9]

It would be interesting to pursue new metal deposition techniques such as CVD or plating which may improve step coverage at steep window cuts.[10] For the purpose of contact performance, doping of the window region should be carried out in a manner which (i) gives low contact resistance or controlled barrier heights and (ii) limits the defect density - by limiting the doping[11] or controlling the ambient during contact doping. It is known that very high impurity concentrations and oxygen ambients[12] promote defect expansion. It would be interesting to see work appear which introduces variations on the defect characteristics in windows and around their edges and answer the question as to what role the defects play in subsequent contact formation.

There is also a need to further characterize and understand redistribution of impurities during silicide formation.[13]

Laser annealing of implanted layers has recently resulted in the formation of very high (nonequilibrium) substitutional concentrations of dopant impurities in semiconductors.[14] It is possible that lower contact resistance may be achieved with such layers. Any such exploratory contact study should include the effects of thermal history following the laser annealing as well as the variation of sintering and/or reaction temperatures upon the nonequilibrium dopant concentrations.

(1) Current Status of Contact Formation

Aluminum metallization has been the mainstay of the industry for contacts to integrated circuit windows.[15] Dissolution of Si in Al and Al in Si has resulted in the use of Al-Si alloys of up to 2% Si in Al.[16] Too little Si in Al results in Al penetration into the underlying Si, too much Si results in precipitation of Si, extending above the plane of the Al-Si alloy/Si interface.

The situation of "too little Si" in Al is aggravated by smaller window sizes because all the Si required to satisfy solubility requirements in the Al is "pumped" from the small window region, making the interpenetration of the Al into the contact very deep. Of course, it is intended that shallower junctions are to go with smaller windows, so a situation develops which is aggravated by smaller windows.

The situation of "too much Si" may also be aggravated by smaller window sizes because the precipitate size may be a substantial fraction of the window[17] size and this could result in high resistance contacts.

In summary, Al metallization and Si-Al alloy metallization is currently being used for some window sizes and junction depths but problems may be anticipated at smaller windows and junction depths.

Silicides (e.g., PtSi, Pd_2Si, NiSi, etc.) form a class of contacts to silicon which have been used for IC and discrete device fabrication. Silicide formation may, in principle, give completed reactions which give very shallow stable metal contacts.[18]

There are a very large number of metal layered systems which could be used on silicides, Ti-Pt-Au is one example of such.[19] With silicides (e.g., PtSi) multilayer metallization schemes are used since Pt does not give good adherence to SiO_2.

It seems that contact formation can be classified into two broad areas: (1) Al (alloy) single metal, and (2) silicide with multilayer: adherence promoter layer and inter-diffusion barrier layer. Barrier diffusion layers (Ti, Cr, V) can be used between reacted silicides and Al.[18]

These two broad areas will be discussed below for future work.

Present technologies use doped polysilicon for gate and rail material in MOS devices. However, for dimensions smaller than 1.5 μm widths, increasing rail resistance limits the performance of high-speed circuits. The use of silicides on polysilicon[20] or refractory metals such as Mo or W becomes needed. There is a need to explore contacts to lower resistance materials, to characterize the interfaces between these "rails" and the primary metallization from the point of view of stability against intermetallic diffusion and interface resistance. Contacts between W, Mo, PtSi, Pd_2Si and Al should be explored in more detail.

Electromigration effects have been studied in considerable detail for Al, Au and assorted pure metals and alloys.[21] Typically, homogeneous test structures are used which have massive contact areas. For use in integrated circuits a metal-alloy, such as

Al-Cu, will terminate at the interface of a contact. The system is not homogeneous at the contact (by definition) and for a 1.0 μm window diameter and a current of 1.0 mA, the current density is $10^5 A/cm^2$, a value for which electromigration effects are observed in thin films. It is possible that stability effects associated with electromigration may be observed in very small windows at moderate currents.

(2) Specific Areas of Scientific and Technological Need for Contact Formation

Al is widely used for metallization of IC, thus an extensive effort should be made to quantify its limitations for use at small window size. The difficulties mentioned above have not been quantified in the literature. It is not clear if a range of alloy compositions exists which gives no Al penetration (Si rich alloy) and simultaneously no yield limiting precipitates (dilute Si alloy). It should be the objective of current research to define and determine the exact limitations of Al-Si in small windows.

The question of window edge stresses and doping induced stresses as they relate to contact formation (Al or silicide) should be examined. What effect do stresses have on the penetration of silicides or Al?

The effect of ambients on the interface between silicon and metal should be systematically studied in the context of contaminated interfaces.

The effect of the presence of extended defects such as stacking faults and dislocations upon Al and silicide contacts should be documented. Stacking faults and dislocations can now be intentionally introduced in a rather controlled manner. Exploratory research could well make use of this fact and form contacts in the presence of the intentionally introduced defects.

(3) Areas of Impact of Contact Research on Other Fields

Many of the fields addressed by the Subcommittee on Materials for Fabrication of Small Structures will either directly affect the topic of contacts or vice-versa. "Contact Studies" include deposition processes, all classes of thin film studies, lithography (sources, masks and resists), etching processes and fabrication of functioning device test structures to characterize the contact as well as the study of electro-migration and corrosion.

Contact layer film studies will have a continued impact on the fields of optics, superconductor devices, solar cell devices, display devices, medical microstructures and magnetic bubble devices. Implicit in the quest for smaller contact structures will be the development of commercial equipment to provide production capability.

(4) Opportunities for Industry and Universities

Industry will continue their major role where either large capital investments for equipment are needed, or the technological driving force is very strong. Universities may consider studying continuous layers or patterned gross features, i.e., undertake fundamental generic studies. Industry on the other hand may concentrate more on the technology of getting such layers into device test structures, i.e., methods of deposition, patterning and device testing. However, there may be considerable overlap and cooperative programs between universities and industry should be encouraged.

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ELECTROMIGRATION

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ELECTROMIGRATION

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STATUS OF CURRENT WORK

About ten to twelve years ago it was discovered that electromigration, the transport of metal atoms by an electric current, was the cause of failure in the aluminum thin film conductors used in microelectronic devices.[1] This caused a flurry of activity, mostly in industrial laboratories (Fairchild, Motorola, IBM), reflected by numerous publications, which went on for several years. A review published in 1973[2] summarizes the work done in this early and most active period in the history of electromigration in thin films. With the adoption of various palliative measures, which shall be briefly discussed later, the interest of industry in electromigration decreased considerably, resulting in a markedly reduced rate of publication. A relatively small output of articles from two centers of academic interest (Stevens Institute of Technology, and the University of Florida, Gainesville) overlaps the early and more recent periods. A fair idea of the work which has appeared in the open literature up to the present can be obtained from a quite recent publication[3]. Apparently quite fortuitously the decrease in the concern regarding electromigration in thin films, parallels a simultaneous decline in the interest in electromigration phenomena in general, A recent monograph [4] provides a convenient source of information about the current situation with respect to various aspects of electromigration (theory, purification of metals, liquids). It may be noted here that although electromigration phenomena in thin films have been the almost exclusive object of attention, thin films are not the only material related to the electronic technology where electromigration

is manifest. One of the early references to electromigration problems was concerned with soft solders[5] (where the related question of thermomigration[6] may be also significant); quite recently attention has been drawn to the effect of electromigration in liquids on the crystallization of III-V and II-VI compounds[7-9] (which may become of greater importance considering current activities in GaAs devices). Although many of the published studies on thin films have immediate and obvious applications to very small dimensions (width of the order of 1 μm), with a very few exceptions (e.g., ref. 10,11) authors have been concerned with conductors of normal size (width of ~10 μm).

NEEDS

In considering the work to be done in establishing a solid basis for future technology, one may start with an examination of unresolved problems and follow with an analysis of new problems anticipated to arise specifically as a result of the use of conductors with smaller geometries.

1. Problems Remaining to be Solved

a) It is recognized that electromigration in thin film is a grain boundary transport phenomenon. Yet there exist no theoretical work on the electromigration force in grain boundaries, and only very few measurements of this force: on Sb atoms in Ag[12], on Cu atoms in Al [13], for the most technologically important aspect of self transport one can quote only one study of Al in Al[14], and the value obtained there appears suspiciously too low. More work is needed here which should not be limited to thin film studies but should include boundaries between bicrystal samples.

b) Of the three techniques which are used to increase the resistance of thin film conductors to electromigration failure: large grain size, alloying, and dielectric overcoating, only the first one may be said to be thoroughly understood.

Considerable amount of work, probably on bicrystals, is needed to arrive at a realistic atomistic model of the role of impurity absorption in grain boundaries on decreasing the rate of self-diffusion along these boundaries.

The analysis of one aspect of the effect of dielectric overlayers, that of the creation of pressure and stresses and the result therefrom on grain boundary diffusion rates, has led to the paradoxical situation that if a reasonable value of the electromigration force is assumed there should be no effect of dielectric overlays on electromigration lifetimes[15], while the experimental measurement of stress effects led to the derivation of a very low electromigration force [14]. The question deserves clarification; it is conceivable that overlayers effects are not only due to pressure and stress but also to modifications of the role of the free surfaces of conductors as a sources and drains for vacancies, the behavior of which are thought to be important in electromigration failures.

2. Anticipated New Problems

In analysing the effects of decreasing geometries, it is natural to consider direct effects, resulting from a simple consideration of geometrical scaling factors (a, below), and indirect effects resulting from the increasing importance of phenomena which play only a minor role in conductors with sizes prevalent today (b, below).

a) The design of reliable electronic devices requires the knowledge not only of median failure times, but also of the distribution of failure times including the width of such distributions. A

realistic model for the effect of grain size and conductor width on electromigration failure exists [16]; however, discontinuities may be anticipated when the width of the conductors become smaller or commensurate with the grain size. The model needs to be extended and data on failure distributions need to be obtained for such conditions.

Electromigration failure at contacts have received little attention[17] presumably because they are not important with the prevalent existing geometries. It is quite conceivable that with smaller geometries contact problems may become more acute, because contact areas may not scale as other factors, e.g., the cross section of the conductors.

b) With decreasing dimensions it is anticipated that surface phenomena will play more important roles. There are a few references to electromigration at surfaces in W filaments[18] and on Au samples[19]. With thin films one may refer only one bonafide surface phenomena related to electromigration[20]. It is on Ag, and one is uncertain about possible connection to environmental corrosion effects. Of course these too are surface effects and the correlation between electromigration and environmental factors deserve attention. The beneficial effect of an H_2 environment on the electromigration behavior of Al thin film conductors[21] should be mentioned in this context.

3. Other Problems

Other problem areas shall be listed briefly: Pulse effects, largely studied in the context of magnetic bubble devices[22,23] are hardly understood, require much work. There has been very little work done on electromigration in semiconductors, much of it is quite dated [24], some applies to materials for bistable elements[25]. With shallow devices, obtained for example by ion implantation techniques, or with Schottky diodes, one may anticipate problems with electromigration, especially of fast diffusion elements, Au, Li, etc. Work needs to be done to

establish on a firm basis the electromigration rates in semiconductors, not only in the lattice but along short-circuit paths, such as dislocations, and hence to determine the limits at which electromigration phenomena can become a source of device problems.

RELATED SUPPORT

Much of the material discussed above touches upon areas of interest which are distinct from the narrower concerns of the electronic engineer. Electromigration along grain boundaries and effects thereon of alloying additions is a matter of interest to all those concerned with the properties and behavior of grain boundaries. It is a question for the more general physical and matallurgical disciplines. This is also true of course of electromigration phenomena at surfaces. The extension of systematic electromigration work to semiconductors should elicit the interest of theoreticians who attempt to define the fundamental forces at work in electromigration. The problem of migration of Li in Li drifted detectors, in the forward and reverse direction appears intriguing in this respect. The effect of electromigration on the crystallization of GaAs, and other compounds, should interest not only crystal growers but all those concerned with our understanding of the liquid state.

SPECIFIC RESEARCH

At the present time electromigration is a well known, although not universally well understood, phenomenon to the people involved in electronic technology. Industry can be counted on to carry on with the tedious lifetime tests which will continue to be required with the design of new circuits. This is at least true for thin film conductors, and may be less true for semiconductor effects per se, which have been of no concern up to now. However, in order for the technology to evolve in a meaningful fashion an understanding of the basic phenomena need to be provided. By necessity the list of suggested work below will be

somewhat repetitious of what has already been written above, and may be thought of as something of a summary.

Grain Boundaries:

In the lattice the electron "wind force" is proportional to the electric current. How can this concept be extended to grain boundaries in a meaningful way?

Experiments should be directed at a measure of the electron wind force in grain boundaries, possibly in bicrystals. The effects thereon of alloying additions, separation of the effects on the electromigration force, and on the grain boundary mobility should be investigated. How do alloying additions affect the structure of grain boundaries? Relate structural effects to mobility and force terms (above).

Surfaces

Extend work on electromigration on surfaces. The work on Ag thin films was not well controlled and needs to be repeated, and the contributions of ambient effects analysed. The possibility of surface transport effects should be looked for in very thin Au films, possibly also Pt films. However, this surface work should by no means be limited to thin films, but should include whatever type of samples is judged likely to provide information. A critical experiment on the effect of a dielectric overlayer on electromigration in thin films, separating stress effects from other (if any) effects is badly wanting.

Pulse Effects

The problem there remains ill defined and it appears difficult to provide suggestions for experiments. Apparently, once the duty cycle has been factored out the lifetimes of thin film conductors undergoing pulse testing remain longer than would be anticipated on the basis of

the results obtained under pure dc testing. This is all the more surprising, since under pulse testing one would anticipate accelerated failures due to the contributions of thermal fatigue. These latter effects have not been separately analysed. This should be done, either under ordinary ac current, or preferably with reverse square wave pulses. Beyond this one should look at possible time effects in the nucleation and growth of holes.

Liquids and Semiconductors

Experiments should be done on the electromigration of fast diffusing impurities in semiconductors, e.g., Au, Cu, Li, etc. The forces at work should be defined, the contributions of short circuit diffusion paths measured. To limit oneself to GaAs, the electromigration of Ga and As atoms in liquid GaAs should be measured, as well as the electromigration of doping additions in the medium.

Solders

Experiments on electromigration and thermomigration effects in soft solders, including possible atmosphere interactions, would contribute to the general fund of knowledge upon which a successful technology can be built.

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APPLICATIONS OF ELECTRONICS TO MEDICINE

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ABSTRACT

Due to their revolutionary rate of advance for nearly two decades, integrated electron devices can be applied in medical instruments with outstanding advantages to the quality and availability of health care. To provide an overview of activities in this field, various types of medical electronic instruments are classified in a matrix format according to their orientation relative to the patient and the generic function which they perform. Explicit examples which illustrate the utility of custom integrated electron devices are: i) totally implantable blood flow telemetry for use in research animals, ii) noninvasive ultrasonic imaging systems for diagnostic and monitoring functions, and iii) a prosthetic optical-to-tactile reading aid for the blind.

INTRODUCTION

Health care presents a singular opportunity to improve the quality of life in our society through electronics. In modern medical research a myriad of electronic instruments ranging from pinpoint-size implantable microelectrodes to 1 MeV electron microscopes contribute immeasurably to the identification, treatment, and prevention of disease. In current medical practice the premier diagnostic and monitoring tools are electronic instruments, as illustrated by the computerized x-ray tomograph, ultrasonic echograph and electrocardiograph. The electrical defibrillator commonly provides life-saving therapy for patients under cardiac arrest, while an electronic reading aid for the blind is a prosthetic instrument which offers significant social and economic benefits to the visually handicapped. Due to their revolutionary rate of advance for nearly two decades, integrated electron devices can be applied in medical instruments with outstanding advantages to the quality and availability of health care [1].

ORIENTATION AND FUNCTION MATRIX

To provide an overview of the field, various types of medical electronic instruments can be classified according to their orientation relative to the patient and the generic function which they perform, as illustrated by Fig. 1. In this representation each matrix element is a specific example of a particular type of instrument. In most instances a matrix element can be described by a rudimentary block diagram, as shown in Fig. 2, which consists of input sensor, central processor, and output or display blocks. Frequently, commercially available general purpose integrated electron devices, such as silicon microprocessors and custom software, are used to meet the peculiar requirements of a central

processor. The resulting "smart" instruments can have a remarkable impact on medicine. This is most profoundly demonstrated by the computerized x-ray tomograph which has revolutionized diagnostic radiology [2].

Moreover, output or display hardware may vary from a general purpose television monitor to quite special purpose tactile displays for the blind depending on the orientation and function of an instrument. It is the input sensor, however, which most frequently benefits from special purpose integrated electron devices. Design and fabrication of custom transducers and preprocessor circuits are often necessary to satisfy the unique requirements of hardware which must acquire data from biological systems. Consequently, the keys to many promising new medical instruments tend to be the custom integrated electron devices directly associated with the input and output interfaces. The following discussion deals with these key devices. More explicitly, examples are described of custom integrated electron devices in i) totally implantable telemetry for use in research animals, ii) noninvasive imaging systems for diagnostic and monitoring functions, and iii) a prosthetic reading aid which allows immediate access by the blind to all printed material normally used by sighted people.

IMPLANTABLE TELEMETRY IN RESEARCH

In science and engineering the contributions of models to the process of discovery and invention can hardly be overestimated. Clearly, computer-aided modeling of integrated electron devices has been a crucial factor in their rapid advance. For compelling ethical, legal, scientific and economic reasons animal models which simulate human behavior are indispensable tools in medical research. Using animals, otherwise impossible experiments can be conducted which contribute immeasurably to improved health care for man. In countless instances, the value derived from animal experiments can be enormously enhanced by acquisition of data which: i) cannot be collected from the surface of the body, ii) is available only if the animal is neither anesthetized nor restrained, and iii) must be gathered throughout the course of a study extending over many months. For such chronic animal investigations miniature telemetry units which are surgically implanted in the host animal represent a unique tool.

Because the vitality of every organ in the body depends upon the flow of blood to it, the capability for accurate estimation of blood flow is extremely valuable in many chronic animal studies. A block diagram of a recently developed implantable pulsed Doppler ultrasonic blood flowmeter is illustrated in Fig. 3. In this instrument the gated oscillator provides a short 1 μsec burst of 6 MHz high frequency excitation to a piezoelectric transducer immediately adjacent to a blood vessel. During a relatively long 50 μsec interval following each transmit burst, the associated ultrasonic pulse traverses the vessel diameter producing back-scattered signals, emanating from moving erythrocytes, which are amplified, detected and telemetered by the internal electronics. At any instant the Doppler frequency shift in the back-scattered signals is proportional to blood velocity (v) at a particular location within the lumen defined by the corresponding ultrasonic transit time of a

transmit burst. The range gated external electronics provides many spatially discrete samples of a blood velocity profile whose electronically derived integral over the lumen area is an accurate estimate of instantaneous bidirectional volume flow.

Two special purpose monolithic integrated circuits have been demonstrated to provide the high performance, small size, low power drain and reliability required in the implantable unit [3,4]. Without these custom electron devices this implantable flowmeter would be unfeasible. Application of the unit in heretofore impossible investigations of cardiac pharmacology, fetal and neonatal physiology and hepatic hemodynamics in cirrhosis is in progress [3,4].

NONINVASIVE ULTRASONIC IMAGING FOR DIAGNOSIS AND MONITORING

The ideal diagnostic instrument provides definitive data on a patient's condition, causes him no harm or discomfort, and is convenient, reliable and economical for a physician or his medical associates to operate. A monitoring instrument imposes the additional stringent objective of virtually total freedom from the need for human intervention during prolonged periods of operation. Because of its apparently harmless and noninvasive character, transcutaneous ultrasonic imaging offers great potential for fulfilling these idealized specifications. In contrast to x-rays, two principal features of ultrasonic instruments are i) their capability for real-time imaging of moving targets such as the heart, and ii) their complete avoidance of tissue damage by ionizing radiation.

A block diagram of a new electronically scanned and focused phased array system is illustrated in Fig. 4. In this instrument a short coherent burst of 2.25 MHz ultrasonic energy is emitted by a 32-element piezoelectric transducer array contained in a hand-held probe in contact with the patient. As the packet of ultrasonic energy propagates through the body, most of it is lost through tissue absorption, but a small amount is reflected or scattered at boundaries between materials of differing acoustic impedance. It is the reflected or scattered component, which returns to the transducer array, that provides useful information. Following preamplification by a matched array of 32 low noise, wide dynamic range, voltage variable gain circuits, returning signals are time delayed and summed by a 32-input four-element cascade charge coupled device (C3D) lens [5]. Through appropriate control of clock frequencies f_3 and f_4 the two linearly tapered elements of the lens provide electronic scanning in a 60°-80° sector pattern for a large field of view. Control of clock frequencies f_1 and f_2 of the quadratically tapered elements permits electronic focusing for high resolution.

Noninvasive ultrasonic instruments are very widely used in medical practice for cerebral, ophthalmic, thoracic, abdominal and fetal imaging. Extremely promising opportunities for improved capabilities are in the offing through the application of custom integrated electron devices in i) the piezoelectric transducer array [6], ii) the preamplifier array [7] where analog LSI is most desirable, iii) the high voltage transmitter array [8], and iv) the C3D electronic lens [5].

A PROSTHETIC READING AID FOR THE BLIND

For many humans the quality of life is greatly diminished by loss of some natural function. Blindness, deafness, paralysis, and loss of limbs are afflictions suffered by many. The powerful and compact sensory, computational and display capabilities of integrated electron devices make possible promising new avenues for prostheses to remedy these functional deficiencies. Sensory prostheses frequently operate transmodally, mapping information normally gathered by an impaired sense onto an intact one. The Optacon optical-to-tactile reading aid for the blind is such a prosthesis [9].

In principle the Optacon is a direct translation reading aid for the blind which converts an optical image of a printed character on a page of an ordinary book, magazine or newspaper to a vibrating tactile facsimile. A block diagram of the instrument is illustrated in Fig. 5. By means of a simple optical system contained in a hand-held camera, an image of a printed character is focused on a custom 6 X 24 monolithic array of phototransistors. Output signals from the phototransistor image sensor array are processed in a simple electronic system, and then used to control a corresponding 6 X 24 array of piezoelectric tactile stimulators or bimorphs. The bimorphs are excited by custom monolithic arrays of high voltage (100V) MOS circuits. Tiny pins cemented to the bimorph tips protrude slightly through perforations in a rectangular plastic plate. A blind reader whose fingertip is resting over the perforations can then feel an accurate tactile facsimile or vibrating image of the original printed character. Several thousand Optacons are now in daily use by blind individuals in many countries [10].

CONCLUSION

In many instances the projected market for a custom integrated electron device required in a particular medical instrument does not provide economic justification for its development by private industry. Both the small size of the market for such a custom device and the extended lead time required for its research and development, which must be followed by thorough medical evaluation of the instrument itself, mitigate against private investment. However, the overall social and economic benefits of such investments may outweigh many of those which are economically feasible for a particular private enterprise. In addition, the strong interdisciplinary teams of engineering and medical investigators which typically are required to research a radically new instrument concept are very infrequent in private industry. Considering the foregoing statements, one is led to the hypothesis that public support of research dealing with integrated electronics in medicine which is conducted in a university environment may offer a viable approach to many problems in the field of advanced medical instrumentation. From a university viewpoint such research provides both the highly stimulating intellectual challenge necessary for effective graduate education and research as well as the prospect of an important and unique benefit to the society which the institution serves.

In summary, the initial impact of integrated electron devices on health care is now visible, and consequently, it is postulated that we

are beginning a new era of revolutionary advances in medical instrumentation. Health care may indeed present the most promising opportunity to improve the quality of life in our society through electronics [11,12].

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BIOMEDICAL INSTRUMENT MATRIX - ORIENTATION VS FUNCTION

	RESEARCH	DIAGNOSTIC	MONITORING	THERAPEUTIC	PROSTHETIC
SUBCUTANEOUS	TOTALLY IMPLANTABLE TELEMETRY		CEREBRAL PRESSURE TELEMETRY	NERVE BLOCK FOR PAIN RELIEF	CARDIAC PACEMAKER
SUPERCUTANEOUS	ANIMAL BACKPACK TELEMETRY	INGESTIBLE pH TELEMETRY CAPSULE	AMBULATORY CARE ECG TELEMETRY	NERVE BLOCK FOR PAIN RELIEF	HEARING AID
PERCUTANEOUS	IMPLANTABLE TRANSDUCER WITH EXTERNAL LEADS	CATHETER-TIP BLOOD GAS SENSOR	CATHETER-TIP PRESSURE SENSOR	THERAPEUTIC MUSCLE STIMULATION WITH PERCUTANEOUS ELECTRODE	FUNCTIONAL MUSCLE STIMULATION WITH PERCUTANEOUS ELECTRODE
TRANSCUTANEOUS	X-RAY	COMPUTERIZED X-RAY TOMOGRAPHY	ULTRASONIC IMAGING	DEFIBRILLATOR	ELECTRONIC READING AID FOR THE BLIND
EXTRACUTANEOUS	ELECTRON MICROSCOPE	MASS SPECTROMETER	GAS CHROMATOGRAPH		

Fig. 1. Biomedical Instrument Matrix - Orientation versus Function

RUDIMENTARY SYSTEM BLOCK DIAGRAM

Fig. 2. Rudimentary System Block Diagram

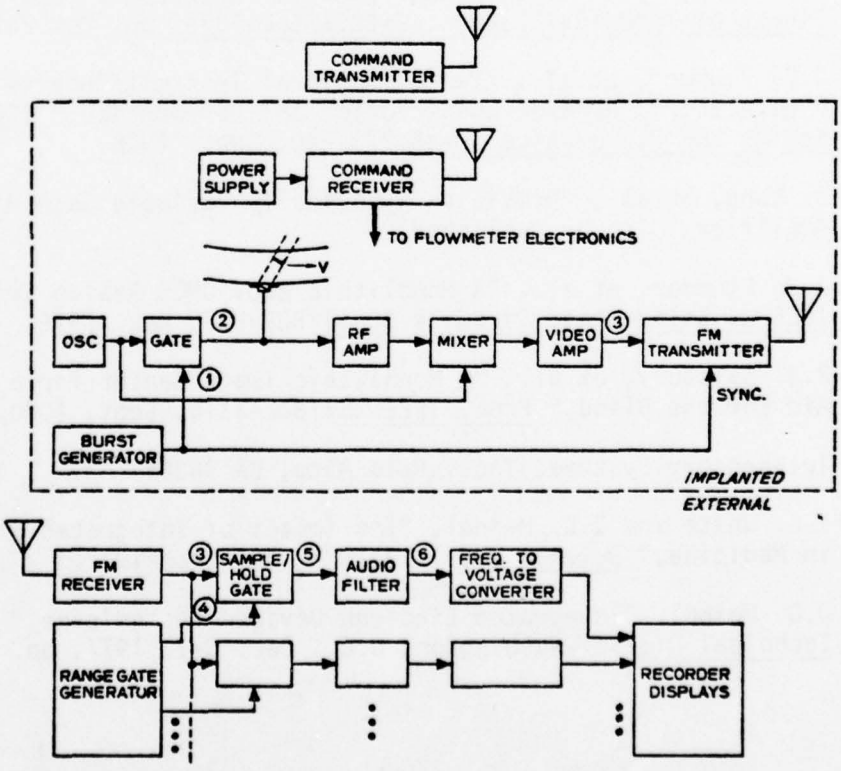

Fig. 3. Implantable Flowmeter Block Diagram

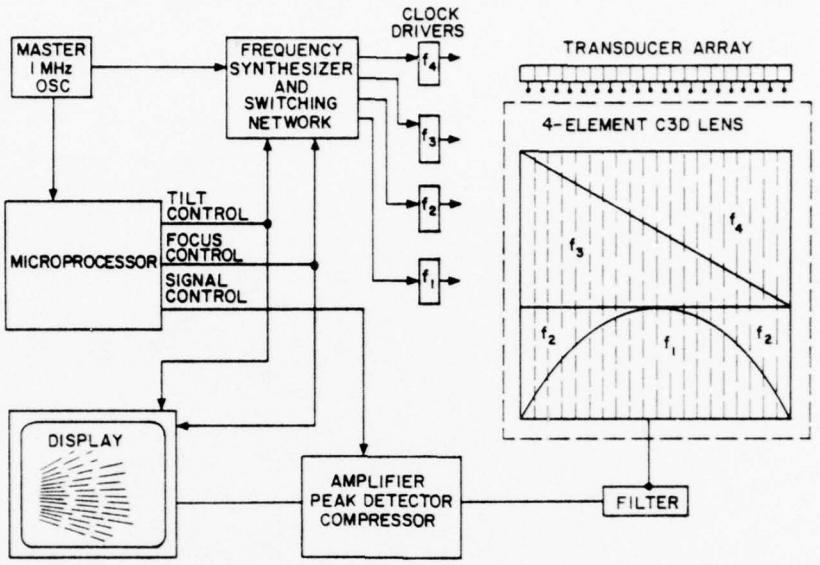

Fig. 4. C3D System Block Diagram

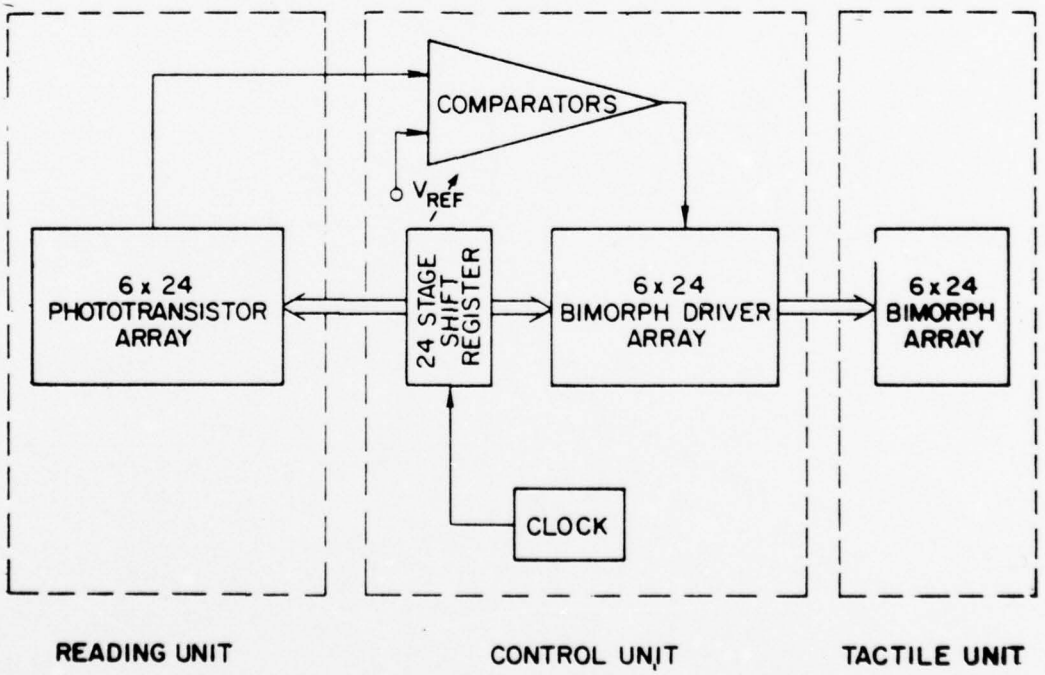

Fig. 5. Optacon Reading Aid Block Diagram

Solid State Devices as Material Probes

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I. Status

Initial device concepts usually depend on a view of a solid state device as composed of interacting regions of materials, each region having properties that have been established for the materials in bulk form. The exploitation of devices for technological purposes, however, often leads to the production of unique environments in the solids involved, in which known bulk properties do not provide a guide to the behavior of materials. Novel phenomena occur in the unusual environment created, phenomena unfamiliar and unexplored in the bulk material or involving unanticipated interactions between various parts of the material system.

The special nature of the environment to which materials are exposed in solid state devices has been accentuated by the advance of miniaturization in electronics. The dimensions of significant regions of solid state devices have become comparable to the fundamental length parameters that enter into the theory of solid state phenomena, such as optical wave lengths, electron wave lengths, screening lengths in electronic systems, widths of depleted regions in semiconductors, and thickness of magnetic domain walls. Solid state devices permit the properties of materials under the specialized constraints produced by miniaturization to be studied. The unique conditions to which materials are exposed in solid state devices have led to the discovery of, or, at least, the recognition of the importance of, many new effects in solids and furnish a valuable tool with which the scientist can investigate various properties of matter. The new phenomena discovered in devices have stimulated a large body of research in solid state science and the techniques of device fabrication have played an important role in making various avenues of research feasible.

The course of events is best illustrated by examples. Consider the p-n junction in a semiconductor. The simplest view of a junction regards it as adjacent p and n regions separated by a thin region depleted of carriers by the potential difference between n and p type semiconductors. Current flow is decribed by Shockley's model, which perturbs the concentrations of electrons and holes in the vicinity of the junction.

When junctions are made, however, it turns out that above certain voltages applied in the reverse, or low current, direction the current is orders of magnitude higher than predicted by simple theory. The effect is called dielectric breakdown, and had been known for many years. The very high fields existing in the depletion region of p-n junction, however, made breakdown a commonly encountered phenomenon, and, also, an important practical problem in that it limited the range or application of devices. Moreover, because of the ease with which high electric fields can be produced in p-n junctions, the junctions themselves became the primary vehicle for the study of the breakdown. Thus a new area of solid state physics was opened to exploration by the unique environment in the depletion region of a p-n junction.

The study of breakdown in junctions soon revealed that two effects were involved: Tunneling on "Zener" breakdown and avalanche breakdown, in which electrons acquire enough kinetic energy to excite another electron across the gap from the valence band to the conduction band. It was found that tunneling could be intentionally enhanced to create a new kind of device, the tunnel diode. The tunnel diode has not gained an important place in technology but has been realized in many semiconductors and exploited at low temperatures as a probe of the phonon and electronic energy band structures of semiconductors. Investigations of the mechanisms of avalanche breakdown led to the concept of hot electrons and eventually to the discovery of the Gunn effect and a vast field of research into scattering mechanisms of hot electrons in many semiconductors.

Electric fields high enough to produce hot electrons also occur in field effect transistors. The hot electrons are produced in close proximity to an SiO_2 layer in insulated gate FETs. A few electrons attain enough energy to surmount the potential barrier confining them to the semiconductor and escape into the SiO_2. Here they may be trapped, creating fixed charges in the SiO_2. The presence and distribution of this trapped charge affects the device characteristics, which characteristics can therefore be used a a probe of such material properties as the cross section and concentration of the traps, the motion of electrons in the SiO_2, and the effects of modifying the SiO_2 on the traps. The insulated gate FET thus constitutes an unusual materials system in which the capability of silicon to produce controlled quantities of hot electrons and its intimate contact with SiO_2 provides a means for probing the electronic properties of SiO_2.

Field effect transistors also provide a unique environment in that conduction in the semiconductor occurs in a thin layer, a layer less than 50A in thickness. The layer is so thin that motion of electrons confined in the layer is quantized in the direction normal to the surface; the quantum is much larger than kT in the cryogenic regime. The electrons in the layer thus constitute a system in which the properties of electrons with freedom to move in only two dimensions can be probed. There is a large amount of flexibility in the FET environment which makes it extraordinarily useful; the thickness of the layer can be varied by varying the electrical potentials applied to the device, and the scattering can be varied by introducing charged impurities in the SiO_2 and by doping the silicon. It is worth noting that, although the quantization effects could be predicted from physical theory, their experimental discovery was stimulated by the observation of anomalies in FET device characteristics.

The above examples all concern electronic properties of solids. This is a consequence of the fact that the exploitation of miniaturization has been most intense in the area of electron devices. However, other areas that have been invaded by miniaturization have also brought obscure phenomena into prominence. For example, Bloch lines in domain walls affect the properties of magnetic bubbles. At the high light intensities in semiconductor lasers photons can assist atomic motions, causing degradation of the lasers. There is potential for studying novel solid state phenomena with such devices.

II. Needs

Although the effects that are unexpectedly encountered in solid state devices are most often intensively investigated to achieve a more complete understanding of their role in devices, they can also often be used as a deliberate probe of material properties, a tool of material science. The use of oxide-gate FETs to study the two dimensional electron system and quantization normal to the surface, and the properties of SiO_2 have been mentioned, as has the use of tunnel diodes to locate energy levels in solids. The characteristics of bipolar transistors have been used to measure the energy gap of silicon, in particular, the dependence of the energy gap on doping, an experiment that depends on the ability of device technology to fabricate n-p-n structures in which the thickness of the p region that separates the n regions is small compared to the diffusion length of electrons.

There is a large element of accident or luck in the use of devices to probe material properties. It is infrequent that, given a material property, a device will be found that is sensitive to that property. Somewhat more often it turns out that a characteristic of a device provides a useful measure of a material property. Thus, exploitation of devices as material probes would most profitably start with a view that asks: What materials properties can be examined with a known device type? Most experimental studies that use devices to reveal the basic properties of solids have been performed with silicon, because the technology of fabricating devices in silicon is so far ahead of that in other materials. There appear to be possibilities for extending the applications of devices that have been demonstrated in silicon to other semiconductors. Furthermore, device technology can frequently be used to fabricate structures intended as materials probes, that is, devices that are not optimized to perform some useful function, but designed to extend the range of environments in which a phenomenon is studied. Thus, the field effect transistors used to study quantization in the surface layer would not be the FET's that one would use in a semiconductor memory. Some of the bipolar transistors used to measure the energy gap of silicon would have doping levels that are not very suitable for useful devices. Even further away from application are larger n-p-n devices that can be used as DC transformers but found their principal use as probes of phonon properties by means of the transmitted phonon drag effect. There are many opportunities to apply devices and device technology to problems in material science.

III. Opportunities

The fortuitous nature of the application of devices as materials probes has been pointed out. Consequently, it is not possible to manage this application in the same way as areas which are oriented towards fulfilling a recognized technological need may be managed. Devices are developed to perform useful functions and their development to serve as materials probes cannot be anticipated. The deviations of devices from their predicted performance that leads to the discovery of novel phenomena cannot be programmed nor can the inventions devices to probe specific materials properties. Thus the orientation of research towards the application of devices as probes of material properties in a general way would be fruitless.

The opportunities for the management of research and development to take advantage of the application of devices as material probes must be through an alertness to possibilities that may evolve in the course of device development. Unusual features of device performance that may represent an unexpected material phenomenon should be vigorously pursued. The conformity of device characteristics to theoretical predictions ordinarily conveys no new information. Rather, it is the failure of devices to perform as expected that may hint at the novel and unusual phenomena that can be the key to new device invention or to additional tools for the exploration of the properties of the solid-state.

The principal barrier to the use of devices as tools in the study of materials is lack of access by the materials scientist to device fabrication facilities and lack of knowledge of the complexities of device technology. Successful application of devices to the study of materials requires the participation of those skilled in the technology of device manufacture. Organization and funding of developmental and pilot device production lines should be structured to insure their availability to materials scientists. For example, since device fabrication facilities are relatively rarely found in universities, device production facilities assisted by Federal funding should be obligated to provide access to the facilities by academic research workers and partially measured by the success of the research. Funding of joint university-industry research, as in certain recent NSF programs, provides another means to increase the availability of fabrication facilities to university workers.

SEMICONDUCTOR ELECTRONICS

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ON THE OPPORTUNITIES FOR UNIVERSITY RESEARCH CONTRIBUTIONS IN VLSI RESEARCH

It is widely recognized that a turning point in the continued development of integrated circuits has been or soon will be reached. This is largely a result of two factors.

- Continued skrinking of lateral and vertical geometries in integrated circuit structures is now dependent not only on better lithographic techniques for defining such patterns but also on better understanding of the fundamental limits of device size and on a better understanding of the physical processes used to fabricate the devices.
- Continued increases in the number of components fabricated and interconnected in a single integrated circuit make detailed interaction between system architecture and integrated circuit topology essential.

Essentially these points imply that close interaction between integrated circuit engineers and material scientists on the one hand and between integrated circuit engineers and computer scientists on the other hand are essential for continued progress. Universities with their interdisciplinary environments, make such interactions potentially easier than most industrial environments currently engaged in integrated circuit manufacturing. Thus the opportunity exists for substantial university impact in both the areas outlined above.

The remainder of this report pursues this theme discussing heavily upon a number of reports and proposals prepared in the Department of Electrical Engineering at Stanford University through the contributions of J.G. Linvill, J.D. Meindl and J.D. Plummer of the Integrated Circuits Laboratory, J.F. Gibbons of the Solid State Laboratory and M.J. Flynn of the Digital Systems Laboratory.

The IC/Solid-State/Materials Science Opportunity

The rapidly increasing use of microprocessors in a wide variety of commercial and military applications has brought with it the need to increase the "functional density" on a silicon wafer by an order of magnitude or more, if possible. Such a goal is of commercial significance, since an increase in functional density will reduce the size and, hence, the cost of an integrated system with given capability. The military interest in such a development is not so much in cost as in substantially increased computational capability on a larger chip.

In either case, the integrated circuit designer is faced with the problem of designing and fabricating devices with a minimum feature size that is about an order of magnitude smaller than that presently used. This decrease in size implies that most of the important device action will be occurring in regions of the semiconductor that are within 0.5 to 1 μ of the surface and, as a result, "surface" doping and analysis techniques will be of substantially greater importance in the next decade than they have been in the past. Substantial progress in understanding surface related phenomena should be possible through an organized effort involving scientists in materials science, solid state and integrated circuit technology areas.

Although our knowledge of basic processes such as ion implantation, thermal oxidation, diffusion and epitaxy has increased dramatically in recent years, it is still in a relatively primitive state. The device implications of this are so dramatic that the need for further research is paramount. The advent of complete process simulation techniques and the coupling of process physics with device physics by means of powerful computer tools mark key steps toward achieving VLSI. Moreover, through

automation of process equipment the most widely fluctuating variable -- the human operator -- is removed from increasingly larger and more sensitive segments of the VLSI fabrication sequence. In addition, automated data logging and subsequent convenient data access via remote computer terminals provide much more accurate and timely information regarding the fabrication sequence to which a given wafer or chip was exposed. Combining this information with that generated through automated electrical testing of wafers allows much more effective feedback to the fabrication line.

Considering the arguments of the preceding paragraph, competitive pressures alone -- both domestic and foreign -- necessitate increasing use of VLSI process models. However, from another aspect, current and projected product goals clearly indicate the increasing necessity for VLSI process models. For example:

- The development of complex monolithic chips to perform in a large focal plane array including more than 10^5-10^6 IR CCD image sensing elements with on-board high speed ECL digital signal processing, entails a complex fabrication technology which demands full exploitation of available process and device models.

- The development of semiconductor RAM chips with more than 10^6 bits of storage, minimum feature sizes under 1.0 μ (approaching the fundamental physical limits of MOSFETs), superior reliability taken for granted, and a selling price less than $20, places a burden on fabrication technology which also demands full exploitation of available process and device models.

- The development of true single chip "microsystems" -- following microcomputers which in turn followed microprocessors -- with, for example, only one external power supply, all internal clocks, latches and buffers, on-chip EPROM and RAM and compatible integrated A/D and D/A converters, as well as analog preprocessors and output drivers, will place perhaps the ultimate burden on semiconductor fabrication technology and clearly will require extensive reliance on process models.

In designing the semiconductor products -- the integrated systems or single chip microsystems -- suggested in the previous paragraph, the

ultimate utility of VLSI process models will be measured in the reduced development time for a complex new chip, in reduced development cost due to time and labor savings, in reduced production costs due to higher yields, in higher product reliability resulting from tighter process control and in improved system performance due to the richer set of trade-offs available to chip designers.

In summary, better understanding of the processes used in integrated circuit fabrication (oxidation, ion implantation, diffusion and epitaxy) and their interactions are essential to the successful fabrication of very small geometry devices. Such understanding is best utilized in computer process simulation programs which permit accurate two-dimensional simulation of device structures resulting from arbitrary fabrication sequences. Understanding of these physical processes on a microscope level requires the coordinated efforts of materials scientists, solid state physicists and integrated circuit technologists. Such a combination of people might best be found in an interdisciplinary university environment although substantial contributions to these problems are to be expected from the industry as well.

The IC/Digital Systems/Computer Science Opportunity

Man's intelligence through electronics/computers has already had a profound effect on current society and human understanding. There is every indication that present technology is accelerating its capability to produce complex programmable structures. This acceleration is both a problem and a challenge.

Human organizations reflect our understanding of their mission and its decomposability; disciplinary boundaries are defined at points of

minimum contact. Representations, techniques, and solutions are constructed within a discipline, assuming that the disciplinary boundary is unchanged. Communication across boundaries is done in static terms that simplify disciplinary understanding.

Possibly nowhere is the above more true than in the computer area and its relationship to modern developments in integrated electronics; for example,

- Algorithms are still treated independent of topology interconnections while the latter dominate physical implementations.
- The microprocessor strongly resembles computer structures of a decade ago -- largely implemented on the basis of textbook tradition.
- System complexity -- both hardware and software -- becomes a pre-eminent issue: first design costs, design verification, development time are the problem; yet automated assistance tools remain primitive.

To pass beyond this stage of limited interaction requires, essentially, the restructuring of a discipline. Examples of the problem areas that need attention are:

- Programming systems: verification and design of large and complex systems.
- Computer-aided design of both hardware and software systems, including testing, testability, verification, fault-tolerant design, simulation, automated interconnection.
- Issues related directly to integrated circuit technology such as signal propagation research and low-energy switching phenomena.

In order to begin a program of holistically linking materials processing science with information systems science, a "top-down" approach to VLSI is needed. Historically the design of a digital system has often followed a four-phase, bottom up procedure. First, the process/device engineer, forecasting the requirements of the circuit engineer, developed

a compatible sequence of semiconductor fabrication processes for a new family of integrated circuits. Second, the circuit designer, anticipating the needs of the system designer, provided a set of components capable of performing various logical functions. Then the system designer, anticipating the needs of the software programmer, assembled the hardware into a digital system for solving a class of problems of interest. Finally, the programmer implemented an algorithm to solve a problem of immediate concern. Limited feedback ensued, but after the functional and physical separation had been established, the partitioning of the problem was rarely viewed as a whole, except at the final stage.

With the introduction of VLSI, this traditional evolution may no longer effectively solve many problems of interest. The complexity of the problems we can now consider solving at the level of a single chip, the blurring of the distinction between hardware and software, and their comparable complexity, call for a new segmentation of the design process which is more holistic than past approaches.

The alternative methodology, a top-down approach, separates the design of a VLSI application into two phases: an initial theoretical phase and a final practical phase. The initial phase begins with the collection of a set of problems for solution. These problems are then abstracted, and solution methods are proposed.

The second phase begins by grouping these algorithms to isolate a compatible set of problems requiring a common method of solution. A solution for a specific problem class can then be specified in terms of hardware and software, and a logical partitioning into constituent modules can be made. As the last phase of the practical design, a physical

partitioning is made, and implementation proceeds.

This top-down approach is valuable for several reasons. As the distinction between hardware and software becomes increasingly blurred, the complexity available with VLSI will undoubtedly lead to the same type and magnitude of problems that have plagued the development of large software projects in the past. The key element in such a project is a proper logical partitioning of the solution into self-contained modules with clean, general, extensible interfaces. Within this framework the physical partitioning required at an early phase by the bottom-up design is unclear; the early division into fabrication process sequence, circuit chips, circuit boards, and software modules may prove deleterious with complex systems.

For example, consider the evolution of a large computer operating system. Segmented into modules at its inception, any repartitioning after its release to customers is an expensive but feasible endeavor. However, after the customers develop applications software dependent upon that operating system, repartitioning quickly becomes prohibitively costly. With VLSI, repartitioning will presumably be as expensive, and errors will be as hard to correct.

These problems are rarely seen at the SSI and MSI circuit level when chips consist of just latches, gates, registers, counters, etc. Even today, on the eve of VLSI, industry focuses on implementing standard, well-understood logical structures and processors. This approach, however, should become decreasingly viable as VLSI is used for implementing specialized hardware designed to meet specific requirements.

The top-down approach to system partitioning problems described above, clearly requires close interaction between computer scientists, digital system designers and integrated circuit technologists. Such an

interdisciplinary team may again be effectively organized in a univeristy environment to attack these problems. As in the IC/Solid State/Materials Science opportunities previously described, however, substantial contributions come from industrial organizations where the requisite team of people exists or can be gathered.

MICROMAGNETIC DEVICES

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I. INTRODUCTION

Micromagnetic devices are an important new category of microelectronics in the steady improvement in cost/performance of electronic systems. So far micromagnetic devices have been used almost exclusively for information storage but they have properties that offer possibilities for logic or display, especially in conjunction with storage. The storage devices have a cost and speed intermediate between the lowest cost semiconductors and magnetic recording. At the same time they provide a unique combination of the best features of those other technologies (electronic speeds, modularity, non-volatility) plus a stop/wait/restart on demand capability that neither of the others have and are fabricated by an integrated circuit process, simpler even than for semiconductor devices, allowing low cost. These devices have already been used for such diverse applications as storage in a portable terminal (e.g., Texas Instruments [1]) and telephone answer-back (Bell Telephone [2]). Other applications will undoubtedly be forthcoming (e.g., storage with micro- and mini-computers [3], storage hierarchies for large computer systems in conjunction with semiconductors and disks [4], flight recorders [5], text-editing [6], etc.), especially as further microminiaturization leads to even lower costs. Thus progess toward such microminiaturization should result in a substantial payoff.

Micromagnetic devices involve the manipulation of small magnetic domains in a thin film of appropriate material. Most of the progress has been in a variety of forms using cylindrical magnetic domains, called "bubbles," but there has also been effort to develop alternate approaches such as the "crosstie" memory [7] and the domain tip, "DOT" [8,9]. Suffice

it to say that micromagnetics is not limited to a single embodiment and more variations may be invented with additional research. We will limit our discussion to the various forms of bubble storage because this is the main stream of activity and progress, is diversified enough to show the various dimensions for further progress and is sufficient to illustrate the type of fundamental work that should be fruitful in micromagnetics and the relevant materials.

There is a main thrust in magnetic bubbles that a host of companies are following and then there are variations on the theme which are being pursued in order to achieve greater circuit density and lower cost. We will first discuss the current main thrust, then the factors which hinder the achievement of greater density in this main thrust, then the variations that are already being explored to avoid these hindrances and, finally, areas of research which our current knowledge suggests as important for future progress. This discussion can be only a summary and references are included that allow the interested reader to obtain more information on any of the various items mentioned.

II. THE MAIN THRUST IN BUBBLES

As with semiconductor technology, the bubble technology involves circuit chips mounted in modules which in turn are mounted on circuit boards. The chips are fabricated with optical photoresist lithography wherein patterns of magnetic permalloy and conductors are defined on top of a thin single crystal magnetic film which has been grown by liquid phase epitaxy on a wafer of single crystal non-magnetic garnet. The

magnetic film will support small cylindrical domains, bubbles, as long as a constant bias field, H_B, is maintained perpendicular to the film. H_B is provided by permanent magnets built into the module. The bubbles move along tracks, defined by the permalloy pattern, under the influence of a rotating, in-plane magnetic field, H_{xy}. H_{xy} is generated by two out-of-phase currents in a pair of coils built into the module. The bubbles are shifted from one track to another by switches controlled by the magnetic field due to a current in a conductor line. The bubbles are detected by the voltage pulse they produce in a magnetoresistive sensor. Thus there are a few conductors on the chip which must connect to the module pins to provide for bubble generation, track switching and bubble detection. However, no physical access is needed to each bit position, in contrast to semiconductors; propagation at all bit locations is induced simultaneously by the overall rotating field.

A typical chip has the following parameters: 64-256 Kbits; 2 μm magnetic film; 0.5 μm permalloy, conductor and SiO_2 spacer layers; 3 μm diameter bubbles; permalloy patterns with 1.5-2.0 μm minimum features that repeat on a 14-16 μm scale, defining the unit bit cell; $H_B \simeq 150$ Oe, $H_{xy} \simeq 50$ Oe at 100-250 KHz; current pulses ≃150 MA to generate, 20 MA to switch, 5 MA to detect; detector output ≃3 MV.

A module contains sometimes one chip (e.g., TI), sometimes a few (e.g., BTL packages four in a module), sometimes many (e.g., Hitachi packaged 32 chips in one module).

If a complete chip with ~100 Kb is pictured, it is not possible to see the detail. Figure 1 is a pattern for a smaller experimental chip that shows the overall pattern. The storage loops are in the center, the input loop is on the left and the detector at the right. Bubbles are generated when conductor G is pulsed. These bubbles flow down the chevron input loop to an inverse generator, or annihilator, unless the write conductor, W, is pulsed, in which case they transfer to the storage loops. In this small chip the storage loops have only 40 chevrons each vs the 500-1000 that are typical of product chips. The bubbles continue to circulate in the storage loops under the influence of H_{xy} unless the read conductor, R, is pulsed, in which case they transfer to the output loop and proceed to the chevron expander. The expanding chevron pattern expands the bubble into a strip which then propagates to the right past the detector, D. The detector is a column of interconnected chevrons. Because this permalloy chevron column is magnetoresistive a change in IR drop is observed across the column when the magnetic strip passes. The detector column has to be long to increase the sensitivity and the bubble must be expanded to cover the detector and make it efficient. A shorter detector of equivalent resistance can be achieved by making it narrower and thinner and then the bubble does not require so much expansion at the cost of chip real estate. The "thin" detector, however, requires an additional fabrication step.

The permalloy elements in Fig. 1 define the bubble positions and information is coded by the presence or absence of a bubble in each bit position. When using this method of coding the bubbles must be kept 4-5 bubble spaces apart to minimize their magnetic interference. In addition,

the bubbles must be larger than the gap between elements by a certain multiple or the barrier to transfer is too great. The main influence of the design of the permalloy elements is on the ratio of bubble size, d, to gap dimension, g, that will allow propagation with good operating margins. Obviously that pattern is preferred which permits the smallest d/g because it will provide the largest circuit density for a given lithographic process capability. The resolution and reproducibility capability of the lithographic process determines the g that can be used. The circuit density is inversely proportional to the unit cell dimension or pattern repetition period, P, and P=4-5d=4-5(d/g)g. With the asymmetric chevron element, "AC", used in Fig. 1, d/g can be two or even somewhat less. With older propagation elements, such as the "TI" elements, d/g had to be greater than three and preferably four. This discussion is important because it shows first of all that circuit density can be improved by the invention of better element shapes as well as by refining the lithographic process. In addition, it shows that circuit density can be improved even more fundamentally by finding a coding scheme that allows bubbles to interact so they can be less than 4-5 spaces apart or by finding a different propagation technique that would remove the restriction that bubbles be larger than the minimum feature. Indeed, approaches are being worked on to accomplish each of these and we will discuss these after we finish reviewing the present situation.

Many companies by now are working on magnetic bubble technology: some are in an exploratory phase, some are developing commercial products and some have been engaged in the manufacture of qualified products for over

a year (e.g., Western Electric, Texas Instruments). Most of these companies have publicly disucssed the configuration and properties of their chips and modules; others, like IBM, have published technical results of their bubble research but have not yet disclosed whatever product configurations they may be working on. The following list indicates the progress that has been achieved in the main thrust of the technology, as revealed by the published literature in the summer of 1978:

1) Bell Telephone Laboratories/Western Electric:
   - 68 Kb chips with 16 μm circuit period AC elements packaged four to a module being manufactured and used for record-message playback [10].

2) Texas Instruments:
   - 92 Kb chips packaged one to a module being manufactured and available for purchase [11]. At first used TI bar propagation elements (22 μm period), but has now been phased over to AC elements (16 μm period). Application in portable terminal (TI Model 765) was announced in early 1977 [1].
   - 256 Kb chips with the 16 μm period are in development and product announcement expected [12].
   - 1000 Kb chip with 8 μm period operated in the laboratory and described at 1977 Intermag Conference [13].

3) Rockwell International:
   - 100 Kb chips with 16μm period delivered for evaluation [14]. This chip has been incorporated in a recorder for a point-of-scale terminal (POS-8) with eight chips packaged

in a module [15]. It has also been packaged 16 to a module for a NASA flight recorder [16].

- 1000 Kb chip with an 8 μm period has been operated in the laboratory and described at the 1977 Intermag Conference [17].

4) Hitachi:

- 64 Kb chips using 20 μm period TI bar elements have been produced and used in a 2 Mb memory by NTT in portable switching systems [18].
- 256 Kb chips using a smaller period have been operated and built into a 16 Mb memory [19].

5) Fujitsu:

- 73 Kb chips using a 14 μm period have been packaged four to a module to provide a removeable cassette that is interchangeable with floppy disks and paper tapes for terminals [20].
- 294 Kb chips using newer elements have been described at the 1977 MMM Conference [21].

Other companies known to be working on similar chips include Univac, Plessey, Siemans, Philips, National Semiconductor, Fairchild and Intel.

There are at least two major government programs. One is with Texas Instruments contracted by Air Force Avionics Laboratory to demonstrate the feasibility of several configurations of airborne mass memories, e.g., 16 Mb disc/drum type systems and 100 Mb recorder type systems [22]. The other is with Rockwell International contracted by NASA for a 100 Mb

satellite recorder [23]. These same agencies are sponsoring other work intended to advance bubble technology and make possible higher levels of integration and lower costs.

All of this establishes a substantial basis for the technology at a particular circuit density (and corresponding cost/bit) and performance level. Let us now discuss the opportunities for further improving cost/performance.

III. THE PATH TO IMPROVED COST/PERFORMANCE

There appear to be ample opportunities to lower the cost/bit of bubbles through increased circuit density. At the same time it is hard to see ways to increase the speed of the devices and, in fact, we have to be careful to keep the speed from deteriorating as we increase the level of integration. Fortunately, increased payoff from bubble technology will flow much more from cost reduction than speed improvement. We will explain these points a little further.

The speed parameters that are important are operating frequency, data rate and access time to the specific data desired. The operating frequency determines the rate at which the data moves in the device, as the bubbles step from cell to cell. Operating frequencies are 0.1-1.0 MHz. The data rate is this operating frequency times the number of storage registers that are operated in parallel. Thus typical data rates are 0.1 to ~10 Mbs (megabits per second). The access time depends on the length of the storage loops and are in the range 1-10 ms. The operating frequency is

limited by two different considerations. First of all the frequency is limited to that which the bubbles can follow, i.e., propagate successfully from step to step. Secondly, increased frequency increases the drive power required, the driver cost, heat generation, etc. Therefore, to increase the frequency appreciably we must find ways to propagate the bubbles faster (>10 m/sec) and circumvent the limitations of the H_{xy} drive. Increased levels of integration, allowed by further reduction in bubble and pattern size, aggravate the speed problem in two ways. In the normal approach, which we have described, the magnitude of the drive field, H_{xy}, must increase as the bubbles become smaller (should we decrease coil volume or frequency to compensate?) and the length of the storage loops increase leading to an increased access time for the same frequency (if we can't increase frequency should we reduce the size of the chip or segment the storage on the chip?). Obviously, this subject involves an elaborate discussion. Suffice it to say that we can probably sustain operating speeds, that it is very difficult to find hope for substantially increased speeds and that factors that would help in this regard are:

a) device forms for which the drive field is reduced and/or does not increase as much as the bubble size becomes smaller,

b) chip organizations that yield shorter access times and/or larger data rates for a given operating frequency, and

c) conditions under which bubbles will move at speeds above 10 m/sec.

All of these are proper areas for research and some progress has been achieved on each already.

Fortunately, speed improvement is not required to expand the utility of magnetic bubble devices. For those applications where increased speed is necessary, there are semiconductor devices. But for the applications visualized for magnetic bubbles, the important characteristics are: non-volality, modularity, stop/wait/restart, ≤10 ms access time, ≥100 KHz, ≤$0.0002 cost/bit and once these are satisfied, the applications appear to expand exponentially with lower cost/bit. Thus our major emphasis is on cost/bit.

Obviously, the most direct way to substantially decrease cost/bit is to increase the capacity on the chip. For each factor of two reduction in the device period we quadruple the chip capacity and reduce the cost/bit by 75%, if we don't aggravate any of the other cost factors. In judging which of the approaches to reduced device period is best we must take into account its impact on chip processing cost, auxilliary circuit costs (e.g., drivers, detectors), heat generation and cooling requirements, etc.

There are several ways we could achieve smaller device periods:

a) changes in the permalloy bar device form that allows a smaller d/g (as already accomplished by a factor of two in replacing the TI elements by AC type elements),

b) refined lithographic processes that would allow smaller minimum feature (gap) size,

c) change in the method of representing data that would allow bubbles to interact and the device period to be less than 4d, and

d) elimination of the gap in the propagation pattern so that the bubble size can be less than the minimum feature, not greater than, as at present.

We will now discuss some of the efforts that are underway to accomplish these improvements.

1) There is continuous effort to reduce the d/g requirement by revising the design of the permalloy propagation element. A variety of different shapes have been made and tested. None so far published are significantly better than the asymmetric chevron. This element can be designed with d/g=2 to yield the widest operating margins or with d/g reduced to 1.5 or even a little smaller if we can be satisfied with narrower margins [10]. Other designs may be found that are even more tolerant of d/g but it can be argued that no design can be achieved where d/g≤1 if the bubble position is defined by a gap. Placing alternate propagation elements on two different layers separated by a SiO_2 layer allows the "gap" to be defined by the thickness of the SiO_2 layer and the horizontal separation of the elements can be reduced to zero. The minimum feature of the horizontal pattern, W_o, is then the width of the leg of the element, W, not the gap, g. However, it is also necessary that d>W. Usually d≃2W but experiments with this configuration showed that 1.5 μm bubbles could be propagated successfully with 1.0 μm legs [24]. Thus $d/W_o \simeq 1.5$ or greater and this approach does not appear to give

significant relief from the d/W_o requirement of the more usual single level propagation pattern.

2) Many organizations are trying to develop a lithographic capability that would produce much smaller minimum pattern features, W_o. Currently, W_o=1.0-2.0 μm with visible optics. Somewhat finer patterns can be achieved with a given lithographic process in bubble devices than in semiconductor devices because the bubble devices don't have the severe mask allignment requirement that semiconductor devices do. In fact, some bubble device designs do not require any precise allignment [25]. This means that X-ray [26] and deep UV [27] lithographies can be used to reduce W_o, as well as electron beams [28]. While all of these are being worked on it may be some time before they can be applied successfully in a manufacturing environment. However, in the laboratory, bubble devices with 0.3 μm gaps have been made and tested [25].

3) "Bubble-lattice" devices utilize completely populated, close-packed arrays of bubbles in order to permit bubble spacings ≤2d instead of the 4-5d of "isolated" bubble devices. In such arrays, each bubble feels the magnetic presence of its neighbors as a component of bias field so that the array is stable in an applied bias field, H_B, of lower magnitude than for the isolated bubble devices. Because each bubble position must be occupied, data cannot be represented by the presence and absence of bubbles in the bit positions, as in isolated bubble devices. Instead, data is represented by the bubble "wall-state." This requires

methods of generating and detecting these wall states as well as establishing the conditions under which the wall states themselves will be stable, without converting from one to the other with resulting errors in the data. These methods and conditions have been extensively investigated [29]. Since the bubbles interact, it is not necessary to drive every bubble - the driven bubbles will push the undriven bubbles. It is thus possible to translate a lattice of bubbles with an overlay of conductors [30] or permalloy elements [31] that is less dense than the bubble lattice. The stability of bubble states under conductor drive [32] and under permalloy drive elements [33] has also been investigated. Almost all of the work on such devices has been done by IBM and they have reported on a 1 Kb bubble lattice device using the conductor drive with all the required functions [34]. Such a device certainly has more complications than an isolated bubble device but its advantages can be:

a) increased circuit density by 4-16X for a given lithography W_o over even the best AC isolated bubble device. This is because $P \simeq 2d$ (vs $4d$) and in addition d can be $\simeq W_o$ (vs $2W_o$) for drive patterns that are less dense than the lattice,

b) lower drive fields since the bubble interaction helps. In addition, the conductor drive can be used to completely eliminate the need for the rotating field coils in the module. In either case we can expect alleviation of the problems due to the high drive coil power of conventional bubble devices when density is increased, and

c) wider operating margins. The lattice is stable over a greater range of H_B than are isolated bubbles. It is conceivable that the other required functions can also be designed to give a wider overall operating margin than for isolated bubble devices.

Reference [31] reviews some of the complexities of lattice devices that must be provided for. Surely, there has been impressive progress made on such devices but whether the complexities can be managed and the advantages eventually realized will only be revealed by more research.

4) Significant progress has been made also on "gapless" devices such as the "contiguous disk" (CD). In this device a pattern similar to rows of slightly overlapping disks is ion-implanted in the surface of the bubble film. An impressed drive field then produces a "charged wall" magnetic structure in that surface extending out from the disks in the pattern. The charged walls move around the disk pattern as the drive field, H_{xy}, rotates and they will trap and carry bubbles with them. Thus these charged walls provide a different mechanism for positioning and propelling bubbles. This device is too complicated to describe here but ref. [35] provides a good background as well as a review of recent progess. In these devices the bubble size can be several times smaller than the minimum feature of the pattern so that this is another approach to higher density. If $d \simeq W_o/2$, instead of $d \simeq 2W_o$ as for AC devices, the density improvement is 16X while still using "isolated" bubbles spaced 4d apart. This

device does not then have the complications of the lattice devices but it does have some other complications associated with the charged wall phenomena. The chip fits directly into the AC chip environment with H_B and H_{xy} but the magnitude of H_{xy} required is less for charged wall propagation. Thus CD offers the desired relief on more than one of the AC constraints. More work on these devices and the process for making them is needed before they can displace AC devices in products.

5) Other on-going efforts are devoted to improvements in bubble materials: new compositions, multiple layer films, different techniques for depositing films, etc. This is such a multifaceted category that only a few items will be mentioned. Garnet compositions which will support bubbles of 0.4 μm diameter have been developed [36]. This is the apparent limit for garnets due to the requirement that $K \gtrsim 4\pi M_s^2$, where M_s is the saturation magnetization and K is the anisotropy energy that holds the magnetization perpendicular to the plane of the film, a necessary condition for bubbles. Smaller bubbles require larger M_s and larger M_s requires larger K. The mechanisms of K have been studied in garnets and the limit has apparently been reached in 111 oriented films for $d \simeq 0.4$ μm. There is some indication that larger values can be obtained in 100 films [37] and then there is the possibility of other compositions such as hexaferrites [38]. Work has also been done on amorphous films such as GdCo alloys which can have large K introduced by the sputter or vapor

deposition process [39]. Bubbles smaller than 0.4 μm will require substantial innovation in materials. Double layer films where the magnetic properties of the two layers are different are already in use and the virtues of three layer films are being explored. Alternation of the magnetic properties of the top surface of a bubble film by ion implantation is used to inhibit "hard" bubbles [40] and to fabricate "charged-wall" devices [41]. The different surface layer can also be obtained by depositing a film of different composition. The surface layer has also been shown to raise the maximum velocity of bubbles [42] and now the benefits to the dynamic properties of triple layer films is being investigated [43]. An in-plane field or a built-in in-plane anisotropy has also been shown to substantially raise the maximum bubble velocity [44]. The point of these diverse remarks is that the study of the physical mechanisms controlling bubble properties (especially the dynamics and anisotropy), the relation of material composition and deposition technique to these, and the exploration of new materials can lead to innovations that will extend the utility of bubbles.

IV. AREAS FOR RESEARCH

There has been significant progress in bubbles in recent years: physical phenomena, materials, devices and fabrication techniques. However, the application of bubbles has barely begun with devices having ~14 μm cells and operating at ~100 KHz. Enough work has been done already, as illustrated by the foregoing discussion, to show that additional

research can lead to substantially higher device densities and perhaps greater device speeds. This, in turn, should increase the utilization of bubble devices, bringing economic benefits.

The most obvious route to higher density is through the development of finer lithography. This is also true for semiconductor devices so the research needs in this area will be adequately covered elsewhere and need not be repeated here. It is worth repeating, however, that refinements in lithographic technique may find application to bubbles sooner than semiconductors because of the comparative simplicity of bubble devices.

Before new lithographic techniques are available significant increases in density may be produced by novel device forms that remove the constraints of the AC device forms, e.g., bubble lattice devices that allow bubbles to be closer together or contiguous disk devices that allow the bubble size to be smaller than the lithographic resolution or others that remain to be invented. Such device innovation can derive from research into new ways to propagate bubbles such as via charged walls or perhaps the newer phenomenon of "automotion" [45].

Hopefully, the relevance of the following areas for future fundamental research is now somewhat evident:

1) the mechanisms underlying both old and new methods of propagating bubbles, e.g., permalloy bars [46], charged walls [35], conductors [47] and automotion [45],

2) the dynamic properties of bubbles and ways to postpone the saturation of velocity, e.g., orthorhombic anisotropy [44], multiple layer films [43],

3) micromagnetic configurations: their static and dynamic properties, and especially how the configurations change with ambient conditions and motion. Included are isolated bubbles [48], bubble lattices [30], cross-ties [7], charged walls [35], surface domains [49], domain tips [8], exchange coupled bubbles in double layers [50] and others,

4) the equilibrium configuration, dynamic conversion and control of the variety of bubble states [29],

5) the mechanisms that induce and control anisotropy, especially how it can be controlled and even enhanced by the growth process [51][39] or composition variation [44],

6) other classes of materials which may offer better properties and/or extend the utility to smaller dimensions or higher speeds (crystalline materials, such as hexaferrites [38] or amorphous materials [52]), and

7) novel ways to manipulate domain structures, such as bubbles, without direct access to each bit position and especially where the minimum feature that needs to be defined lithographically is larger than the relevant domain structure.

V. CONCLUSION

The rate of discovery of new phenomena, understanding of fundamental mechanisms and ideas for improving the properties and extending the utility

of micromagnetic domain structures indicates that additional research will bear good fruit. Progress will come from a blend of applied and basic research and there are a variety of avenues to pursue.

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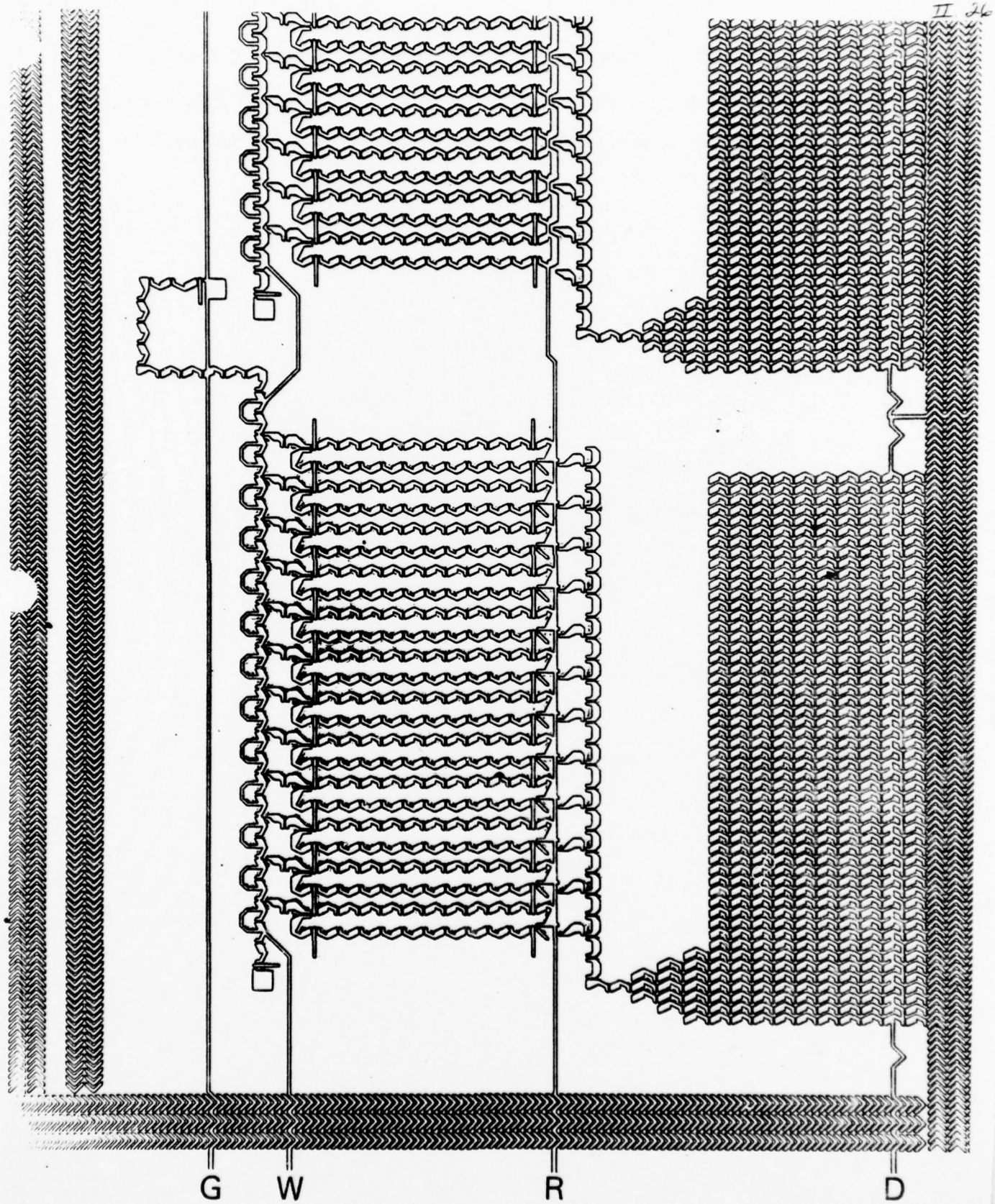

Fig. 1. Experimental Bubble Chip

Material Aspects of Integrated Optics at Very Small Dimensions

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Introduction

The basic ideas of integrated optics[1-11] were conceived in 1969-1972, at the time when the availability of low-loss optical fibers had already brought optical communication close to reality and there are definite needs to form compact optical systems. Research in integrated optics may be catalogued into two parts: one is to apply thin-film technology to the fabrication of miniature optical devices including lasers, modulators, switches, detectors, prisms, lenses, polarizers and directional couplers. The other is the integration of a large number of these devices on a single substrate. It is well known that a layer of thin dielectric film with a refractive index larger than its surroundings is a perfect optical waveguide. We may use these thin-film waveguides as the basic structures of all the optical devices which are then interconnected forming optical circuits. Typically, thin-film optical devices have one dimension ranging from hundreds of microns to a few millimeters and other two dimensions ranging from a fraction of a micron to several microns. The optical wavelength of interest is about 10^6 times smaller than ultra-high frequency radio waves and the devices should have an edge definition of about 500 Å in order to avoid excessive optical scattering. Integrated optics thus demands the finest microfabrication technology. There are a variety of materials[12] one can use to form integrated optical circuits. For passive devices such as prisms, lenses, polarizers, waveguides and grating filters and reflectors, the materials commonly used are sputtered glass, SiNO, organic polymers and amorphous Ta_2O_5, ZnO, ZnS, CdSe, CdS, Nb_2O_3 and TiO_2.[12] For modulators and switches, single-crystalline electro-optic,[13-15] acoustooptic and magnetooptic[16] films such as $LiNbO_3$, $LiTaO_3$, Bi_2O_3:TiO_2, III-V semiconductor compounds,[17,18] and rare earth

iron-garnets may be used. A great deal of the effort in the past has been concentrated to Al-Ga-As system[3,5] to form monolithic integrated optics.[11] Lately, however, the interest in the optical communication system at the wavelength near 1.3 microns has directed the attention to InP, and In-Ga-As-P related ternaries and quaternaries.[19-21] As devices are made smaller in sizes, the optical density in the devices has to increase and may reach MW/cm^2. Optical damage, optical losses, heat generated in the optical circuits, methods to form better epitaxial layers are a few of many material problems which demand most of our efforts in integrated optics.

Status of Current Work

Most of the inventions in integrated optics deal with methods which restructure bulk optical systems into thin-film forms. They include tapered-film[22] and grating couplers[23,24] thin-film prisms and lenses,[25,26] Bragg modulators[27] and directional-coupler switches,[28] distributed feedback[29] and Bragg-reflector lasers[30] and methods of forming interconnections between devices.[31] In the past seven years, research in integrated optics have involved, in U.S.A., about 150 scientists mainly from Bell Laboratories, IBM, Xerox Palo Alto, Rockwell International Science Center, RCA, Westinghouse, Hughes Research Laboratories, Lincoln Laboratory, United Technologies Research Center, Texas Instruments, University of California, Berkeley, Caltech, Cornell University, Carnegie-Mellon University, Washington University, University of Washington, Polytechnic Institute of New York, and Navy Research Laboratories in Washington D.C. and in San Diego. In spite of the scarcity of the research funds for exploring new science, the accomplishment of integrated optics has been spectacular: Research of propagating modes in waveguides has made single-mode kink-free laser-diodes[32] possible, waveguide modulators have a figure of merit of several orders of magnitude better than those in bulk forms,[33] diffused-$LiNbO_3$ directional-coupler switches have a crosstalk of about -32 dB,[34] and thin-film geodesic lenses are capable of focusing a light beam to the diffraction limit and of resolving light beams with an angular separation as small as 3.3 mrad.[35] More importantly, prism coupler and m-line spectroscopy enable one to determine refractive index and mode spectrum in waveguides better than 1 part in 10,000.[1,9,36] Gratings of period as small as 1200 Å have been fabricated[37] and their uses for band-rejection filters,[38] reflectors and distributed feedback and Bragg reflector lasers[39,40] have been demonstrated.

As of today, simple integrated optical circuits can be readily developed in $LiNbO_3$, on silicon substrates, or in III-V alloy-semiconductor compounds. A multipurpose spectrum analyzer involving a geodesic lens, an acoustooptic deflector and hundreds

of silicon detectors is being pursued at Rockwell International Science Center, Air Force Avionics Laboratory and Battelle Columbus Laboratories. A $LiNbO_3$ circuit containing 4 x 4 directional-coupler switches has been built at Bell Laboratories.[41] GaAs circuits containing lasers and modulators have been constructed at Bell Laboratories,[42] University of California, Berkeley,[43] and Tokyo Institute of Technology.[44] A circuit composed of six GaAs laser diodes and six waveguides for wavelength multiplexing is developed by Hitachi Central Research Laboratory.[45] In general, because of more ambitious policy and more liberal funding by the Japanese government toward technological advancement, integrated optics in Japan is just as good as, or even better than that of the United States, in spite of the fact that we have contributed most of the original research!

Specific Scientific and Technology Needs

Although simple integrated optical circuits have been demonstrated with existing technology, to produce them reliably and economically faces a multitude of difficult material and technology problems. In general, the areas needing extensive support may be summarized below.

(1) To form monolithic integrated optical circuits in the Al-Ga-As system, the present epitaxial layers have a loss[46] from 1 to 10 cm^{-1} which should be reduced by about a factor of 10 in order to satisfy the system requirement.

(2) Techniques of fabricating optical gratings either on deposited films or on epitaxially grown layers have to be improved. The present optical circuits containing grating filters, distributed feedback lasers, and Bragg-reflector lasers have poor quality and are generally not reliable.

(3) Research in orientation-dependent epitaxial growth[48] and etching[49] has to be carried out to form atomically flat facets for reflecting or deflecting light in optical circuits. Such techniques are also needed for forming blazed gratings structures in waveguides.

(4) It is generally recognized that to achieve long lifetimes, semiconductor lasers have to be grown on dislocation-free substrates. Methods to grow dislocation-free GaAs or InP substrates and the kinetics involved should be investigated.

(5) Typical semiconductor laser-diodes have sizes hundreds of microns long and 1 to 10 microns wide. They produce 1 to 10 mW of light and are excellent light sources. For signal processing and for performing logic operation in optical circuits, however, a large number of the lasers are required. These lasers must have much smaller sizes in order to improve packing density and need only to produce a fraction of microwatt of light to cut total power consumption. Such microlasers have yet to be developed.

(6) Switches with a speed in the subnanosecond range may be formed in Ti-diffused $LiNbO_3$ waveguides. However, $LiNbO_3$ is susceptible to optical damage. Moreover, impurity ions in the diffused waveguides may move under an intense switching electric field and thus short-circuits the field needed for switching. Research for better electrooptical and acousto-optical materials is in order.

(7) It is likely that optical circuits will be formed on $LiNbO_3$, GaAs, InP, or Si substrates. Fortunately GaAs, InP and Si are also excellent material for high speed electronics. Methods of fabrication so that optical circuits and electronics may be formed on a same substrate have yet to be developed.

(8) For a single optical fiber to carry two-way communication, the incoming and outgoing signals have to be separated and processed in different optical circuits. The device which separates the incoming and outgoing signals is a circulator or an isolator which has to be formed of magnetooptical materials such as rare earth Garnets. The present magnetooptical material has a Faraday rotation constant of 200°/cm. Materials of Faraday constant more than 1000°/cm could be developed by adding Bi or Pr into the composition of the Garnets.

One realizes that the technology needed in integrated optics is also needed in other industries. Therefore, carried with the research of integrated optics are a more refined semi-conductor industry, better methods for epitaxy and for film-deposition, and a better understanding in solid state physics regarding interfaces and dislocations.

Possible Impacts of Research

With commercially available optical fibers, lasers and detectors, it is already possible to design a communication system, 50 MHz in bandwidth and 7 to 8 kilometers in distance, for a cost comparable to that of a similar system using coaxial cables. There is no doubt in the mind of the telecommunication industry that optical fiber systems will grow for short-haul services. For long-distance telecommunication, although intensive research has reduced losses in single-mode optical fibers comparable to those of the multi-mode fibers, the commercial deployment of such long-distance single-mode systems will not be forthcoming until about the middle of the 1980's.

Integrated optical circuits serve best for multiplexing of optical signals. Such applications must, however, wait for the maturity of the optical communication. Even then, the optical communication systems must be standardized before integrated optical circuits can be designed. More immediate applications of integrated optics

are in military communication services, signal processing for warfare operations, local communication and signal-sensing in ships and airplanes. There,light weight and small volume of the fiber system are often dominant factors for the choice. The optical-fiber system has also a unique advantage as being immune to the electromagnetic interference. Optical systems have also been found to be economical for cable televisions. Japan has already used optical systems for data collection and signal processing in large electric power plants where stray magnetic fields produced by the electric cables are found to be harmful to the electronic devices. There are also increasing uses of optical systems in nuclear power plants and high-energy research facilities. Optical systems are also invaluable as a data link between two large computers or two large switching stations in order to avoid mutual electronic interferences or a common ground-current loop. For each of the above applications, there is a need of integrated optical circuits.

The real impact of integrated optics will come when high speed electronics is incorporated into the optical circuits. In fact, a chip containing a bank of the laser-diodes including the driving electronic circuits can be readily developed with the existing technology. Such chips may be used for the transmitters in the optical communication systems. They may also be designed for printing, for survey, and for controls of various industrious processes. Optical beams have the advantages that they may be pulsed in rapid sequences, can scan over wide angles and may be transmitted over any transparent space with a minimum of interference. If visible semiconductor lasers can be developed into practice, a chip containing the visible lasers with their associated electronics has many medical applications. Work to form electronic and optical devices on a same GaAs substrate has already begun.[49,50]

The development of the first practical medium-scale integrated optical circuit can be very costly. However, once the technology is established, optical circuits should not be more expansive than IC chips used in wristwatches or pocket calculators. Heavy investment from the industries is not likely since the present market for the optical circuits does not justify their initial cost. On the other hand, without actively pursuing advanced technologies such as those associated with the integrated optics, we will quickly lose the leadership in this general field of opto-electronics.

University Opportunities

Integrated optics does not compete with the present microelectronics, but rather complements it. In fact, integrated circuits containing both optical and electronic devices opens up new opportunities for

the electronics industry. To develop such circuits to their full potential, research and development should not be confined only to the fabrication of thin-film devices and circuits, but they should be directed to the exploration for new ideas of circuit designs as well as novel device-physics which combines optics to electronics. In that sense, there are plenty of the opportunities for the universities to participate in the research and development, since such studies carry as much as academic value as industrial. In particular, integrated optics is one of the few fields where fundamental science and discoveries can be made.

Microfabrication and epitaxial technologies are the foundations of the modern electronics. Both microelectronics and integrated optics demand the excellence of these technologies. Indeed, the research of integrated electronic circuits and integrated optical circuits should be carried out side-by-side. In particular, InP and GaAs used for the fabrication of the lasers are also the materials for high speed electronics. For micro-fabrication, one requires: electron-beam exposure system (EBES) for computer controlled mask fabrication and electron-beam writing, electron-resist and photo-resist facilities, a mask aligner for both contact and project printing, photo and x-ray lithography, scanning electron microscope for viewing small structures, ion-beam etch and dry plasma etch facilities, and equipments for depositing SiO_2 and Si_3N_4. The equipment required for laser research involves scanning electron microscope coupled to x-ray energy dispersive and wavelength analysis, Auger electron spectrometer with depth profiling, SIMS, mass spectrometer, diffusion furnaces, evaporation and sputtering stations, and liquid-phase and vapor-phase epitaxial growth facilities. Unfortunately, even the best universities in the United States are not equipped with all these facilities. On the other hand, both Osaka University and Tokyo Institute of Technology in Japan have the best of these equipments.

One microfabrication center is being set up in Cornell University by NSF. We believe other similar centers should be, perhaps, in Stanford University and in University of Illinois where a large pool of human resources and technical know-how are readily available. It is believed that these centers will have far-reaching consequences to maintain the momentum of our science and technology in general, and the competitive position of our electronics industry in particular.

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MATERIALS PROBLEMS IN IMPLANTABLE MEDICAL ELECTRONIC DEVICES

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INTRODUCTION

The focus of this article can be quickly set by examination of Fig. 1 which shows a photomicrograph of human brain cells (from the motor cortex) superimposed on a photomicrograph, to the same scale, of a commercially available (Intel) four kilobit random access memory. Note that the bit density of the semiconductor memory is two orders of magnitude higher than that of the human brain. With the further shrinkage of semiconductor structures now in progress the dimensional advantage of electronic intelligence over natural nervous tissue can only increase. It is now possible to contemplate the replacement of defective nervous tissue (e.g., inoperative sensory organs such as the eye or ear, stroke-damaged brain tissue) by synthetic intelligence in approximately the same volume and at approximately the same energy cost per transaction. The realization of such remarkable substitutions is now limited primarily by materials problems, in the long-term insulation and protection from attack by body fluids of the integrated circuits and by materials problems at the neural-electronic interface. This review will focus primarily on these problems.

The continuing shrinkage in size and cost of computational power affects medical electronics profoundly in many other ways, in all cases where computational power can be brought to bear on diagnosis or treatment. Cases in point would be computer-aided x-ray tomography and the various applications of microprocessors to "smart" medical instruments. This article will not deal with such cases, since they are covered elsewhere in this series of reports where the main stream of computer-oriented programs are considered. This article will also not deal with the numerous materials problems in bioengineering associated with bone, tooth, tendon, etc. implants, as not being relevant to the main theme of these reports, materials problems in microstructure fabrication.

STATUS OF CURRENT WORK

The focus of this report, as indicated above, is the development of materials and techniques for the fabrication, passivation, and protection of implantable active microelectronic circuits, active prosthetic or monitoring electronic devices. This section of the report, describing current work in industry, academia, and government, will delineate the exceedingly limited spectrum of active groups.

The largest and most active class of research and development groups in this area exist in the cardiac pacemaker companies. The cardiac pacemaker is, at present, the only widely accepted commercially important neural prosthesis. It is a relatively simple device functionally. Its output is a single pulse to a single electrode at about a one Hertz rate. Its logical function centers on the need to sense the presence of natural heartbeat signals and to suspend stimulation output when satisfactory natural signals are present. Circuits of very modest complexity can achieve these functions, without taxing even the current state of the art

in integrated circuits, in adequately small volume and at adequately small power demand. The pacemakers are relevant to this discussion because they have had to confront seriously for the first time long-term protection of electronic circuits in a biologic environment[1,2]. Early devices were constructed of discrete components potted in an epoxy resin chosen for biocompatibility and minimum permeability to body fluids; Hysol A, manufactured by the Dexter Corp., was the common choice. The lifetime of such systems against ultimate penetration by body fluids was on the order of two years, similar to the life of the batteries incorporated into such systems. Current devices place their active circuits, and batteries when possible, into a hermetically sealed can typically titanium, achieving excellent protection, but at a volume increase factor on the order of 10^5 as compared to the volume of active circuitry. Further, external to the hermetic package is only one massive electrode and its fairly massive lead elements. Since the dimensional constraints are relatively relaxed, insulation of these elements is usually achieved using thick plastic (silastic or epoxy) jacketing. The pacemaker companies have not been forced to confront the problem of insulating and protecting an array of closely spaced elements, as we will see must be confronted by more complex neural prostheses. Some pacemaker companies, however, notably VITATRON in the Netherlands, have made significant progress in developing viable long-term implantable insulation schemes other than a plastic wrapping of the sensitive elements; they have in particular been developing anodic oxidized layers as a class of tightly bonded insulation coatings, and have been particularly successful with anodized tantalum. This work is probably seminal for the micro-insulation needed for implantable microcircuitry.

A second class of research and development groups active in solving problems inherent in implantable electronics are those engaged in biotelemetry[3]. Typically biotelemetry units monitor a few (often one) physiologic parameters (body temperature or blood flow or blood pressure, for instance) and transmit to an external receiver this information. Again for this set of applications, the standard current solutions are hermetically sealed containers for as much of the circuitry as possible, with plastic coating for the elements, such as sensors or antennae, which must be external to the hermetic container. The applicability of these techniques to true microminiaturization is small.

Recently an important class of applications has been emerging which makes technical demands not satisfiable by current materials technology. These applications mostly involve multipoint contact with the nervous system[4]. This multipoint contact is required either for multielectrode stimulation of the nervous system, such as is required for sensory (ear, eye) and muscular (lung, bladder, leg) prostheses, or for multipoint recording of the nervous system such as is desired for research in many areas of neurophysiology (learning, brain disfunction, multiple sclerosis, auditory and visual physiology, etc). For these applications a multiplicity of contact elements (typically platinum microelectrodes for survival against electrolysis) are required, with spacings on the order of the size of the basic neural elements, microns to tens of microns. There is

no sensible way to make such arrays other than with the photolithographic techniques characteristic of the semiconductor industry. The materials currently used in the semiconductor industry are, however, not adequate or appropriate to the implantable application. The metals typically used, gold and aluminum, are in the one case not optimum and in the other not acceptable (toxic). The commonest current insulation material, SiO_2, does not survive protracted saline exposure. A second emerging insulation and passivation material, silicon nitride, Si_3N_4, shows promise as an impermeable insulation but has not been extensively tested. Also a possibility, but with even less documentation, is silicon carbide, SiC. No materials have been evolved for conductors or insulation in situations where a flexible structure is required. If the potential of artificial intelligence for neural prostheses and neural characterization is to be fully realized, truly multiple interface points - microelectrodes - will be necessary, perhaps hundreds or thousands of contact points, not possible without multiplexing or interspersing of passive interface elements with active logic elements. One is therefore led to the necessity of passivating active elements against multiyear saline immersion, utilizing protective coatings whose dimensions must be on the order of microns or less, compatible with the scale of the semiconductor logic elements or the neurons they excite or record. Though the value and potential of such multi-electrode stimulation and recording arrays has been appreciated for some years, especially by neurophysiologists and neurosurgeons, very little progress has been made on the generation of the appropriate hardware, and very little work is, in fact, in progress. The commercial possibilities of such devices are sufficiently modest that the semiconductor industry, wherein resides most of the appropriate talent, has not been motivated to pursue the key problems. Funding to support such materials research in universities has been almost totally lacking because its medical orientation causes all Federal agencies except the NIH to regard the NIH as the appropriate support agency, and the NIH is strongly disinclined to support the development of technology of medical potential unless tied to a specific disease or disability. Recently the NIH has commenced support of the development of such materials and technology pursuant to the development of an "artificial ear," a cochlear prosthesis which works by direct electrical stimulation of the auditory nerve[5]. Such work, at Stanford University, is in its early stages but shows promise. The NIH also has had some in-house work on microminiature electrode arrays, also pursuant to neurophysiology, but with very limited resources committed to the project. The NIH has also been supporting, in recent work, small but important projects aimed at understanding the electrolysis of metals in electrolytes such as body fluids.

In summary, the current state of relevant research is that a number of pacemaker companies are working on related but mostly not directly applicable problems, there is one substantive University project directly aimed at such problems, and a small amount of work in-house at the NIH, but no substantive activity by the effervescent semiconductor industry whose experience is most relevant to the problems involved, for the good and continuing reason the overt commercial markets for the resulting devices is small.

SPECIFIC SCIENTIFIC AND TECHNOLOGICAL NEEDS

The scientific and technological needs for high-intelligence-density implantable electronics are several. The leading need is for the development of insulation materials such that insulation a few microns, or perhaps even a few hundred Angstroms thick, will provide long-term insulation in a saline fluid environment. The structures to be protected are of similar dimensions to the insulation thickness, so the separation and protection of closely spaced elements is required. Since the performance of semiconductor devices is determined by the density and distribution of dopant ions, the protective layers must resist penetration by unwanted dopant ions, such as sodium.

It is exceedingly unlikely that the required technology will be achieved within the conceptual framework of present-day insulation technology, which basically relies on wrapping the active elements tightly with plastic or some other insulating material which is chemically and physically unrelated to the element to be protected. For all such insulation techniques, saline penetration between the insulation and the protected element is inevitable, and if penetration on the order of microns is damaging, the useful lifetime of the protection is short. The successful technology will be one in which the insulation layer is chemically bonded to the substructure. A first step in this direction has been made in certain passive (electrode lead and array) systems using tantalum as a conductor and anodically formed tantalum oxide as an insulation. Such a system shows promise for a number of applications. Shortcomings of the tantalum-tantalum pentoxide system are the unipolar nature of the insulation (the oxide reduces for the "wrong" sign of voltage) the brittle nature of the insulation, and the inapplicability of this particular system to active (i.e. silicon) electronic components. Research is required to define the parameters which make a material, particularly a thin film of material whose volume is essentially all surface volume, impermeable to a number of biologically relevant ions and molecules.

Implantable systems must be biocompatible, which usually translates into being fabricated out of materials which are chemically very inert. Yet the lithographic fabrication characteristic of integrated circuits in general and microstructure circuits in particular invariably involve multilayer structures where successive layers must bond physically and chemically to one another. Research is needed in the science of adhesion as applied to metal, semiconductor and insulating (oxide or nitride) interfaces. How does one form multilayer structures out of chemically inert (biocompatible) materials without having delamination, and failure, a major problem? A good deal of surface physics and surface chemistry must be explored before we can resolve the essential paradox of constructing active electronic microstructures which will not delaminate out of biocompatible, relatively inert, materials.

A second class of problems arising in implantable active electronic devices arises from the phenomenon of electrolysis, the dissolution of metals placed in an electrolytic solution, especially in the presence of

electrical currents. Though the electrochemistry of metal-electrolyte solutions is the subject of an extensive literature, so many of the results are compound-specific or configuration-specific that it is hard to draw generally useful and extrapolatable conclusions, except in broadest terms. Studies specific to the metals most likely to be used in implantable devices, and in situations resembling the complex environment of body fluids, need implementation.

In summary some science and technology areas needing exploration are

(1) The surface chemistry and physics of adhesion especially as applied to biocompatible materials such as may be useful in implantable devices.

(2) The physics of impermeability, especially of oxide, nitride,etc. layers.

(3) The physics and technology of various metal-metal oxide or metal-metal nitride or metal-unknown layers as "permanent" passivation layers. This study should include investigation of the technology of deposition and patterning and of practical feasibility of such passivation schemes.

(4) Studies of plastic-metal interfaces to generate biocompatible flexible systems operable in a hostile electrolytic environment.

(5) A study of electrolysis of metals in a biologic environment, with attention also to the toxicity of by-products.

POSSIBLE IMPACTS OF THE RESEARCH

The direct impact of the successful development of materials making possible long-term electronic implants of high intelligence density is upon the medical world. Successful work would make possible neural prosthesis for a variety of motor and sensory handicaps. Successful work would make possible sophisticated investigations of the operations of the neural system, especially the brain, of how it functions, and of how it is affected in such diseases as cerebral palsy. A secondary area of impact is broader and harder to define - it is the general area of passivation of semiconductor devices. Certainly the techniques which might be developed to ensure circuit survival in the hostile environment of the body, with its fluids, salts, enzymes, and invading fibrosis growths, are extensible to give greater reliability and lifetime to circuits operating in less hostile, yet still threatening environments, such as hot and humid climates. Finally, the information gained in studying the physics and chemistry of surfaces, and of the bonding mechanism of one class of materials to another, is of more general applicability than to microstructure fabrication alone, though the exact ultimate utilization of such information is difficult to identify.

To give specific examples of impact in the areas outlined above: An auditory prosthesis for the profoundly deaf which operates by direct electrical stimulation of the auditory nerve to replace the function of

a defective inner ear (cochlea) is under development in several laboratories throughout the world. It is necessary for such a prosthesis to excite differentially a number of small subsets of the nerve bundle comprising the auditory nerve. A major technological obstacle to this artificial ear is the difficulty of fabricating microelectrode arrays small enough and complex enough to achieve this stimulation, yet capable of surviving in the biological environment. Similarly, electrical stimulation of the optical nerve or the optical cortex produces bright spots in the visual field, from which a representation of the visible world can, in principle, be constructed.One obstacle to this project is, again, suitable electrode arrays and electronics. Electronic bladder control for paraplegics and others with lower body neural disfunction is an important area of neural prostheses also under development. Electronic bladder control is important not only for the obvious convenience and social advantages but is life-prolonging because it eliminates the infection risk of an indwelling catheter, now the only viable solution to bladder dysfunction. Electronic stimulation of leg muscles for gate improvement in hemiplegics is making headway, but again is obstructed by electronic technological obstacles. The operation of prosthetic limbs through the neural signals still naturally available to control the missing limb is only crudely possible at present, but could, in principle, be achieved. The list of neural prosthetic devices which might be conceived, given implementation possibilities, is mind-boggling.

In addition to playing dramatic roles of "bionic man" variety, implantable intelligence with complex high-density sensing electrodes could play a valuable role in extending our knowledge of how the nervous system, especially the brain, works. The applications extend from understanding the mechanisms of learning and memory, through the role of various chemicals on brain functions (e.g. chemical control of schizophrenia), to understanding the architecture in space, and the distribution in space and time, of the signals which characterize and govern our capabilities and behavior. The author has a thick bundle of letters from neurophysiologists of all stripe, inquiring about the availability of microelectrode arrays for studying brain function from a variety of points of view.

Proceeding to the second impact area, the passivation of semiconductor circuits has been an ongoing problem since the earliest days of the semiconductor business, since performance characteristics can be severely damaged by relatively small numbers of impurity ions reaching and infiltrating the active areas. Surfaces are currently passivated with insulating layers such as SiO_2 or Si_3N_4, and sensitive elements further encapsulated in epoxy or in hermetically sealed containers. Even so, failure due to environmental factors is still common, and a serious cause of effort and concern in the semiconductor industry. The informational gain from material studies directed in a more searching way at this problem will certainly impact the semiconductor world generally. Such impact has, in fact, already occurred through the needs of the pacemaker industry. The careful life-test and failure-mode analysis of pacemakers has produced results challenging the military-specification procedures for hermetically sealed devices,and has resulted in a major reexamination

and reevaluation of both the materials used and the procedures allowed in the high reliability circuits of our military and space programs. Such impact will undoubtedly continue if more sophisticated and penetrating results or material parameters can be generated.

Finally one is left with the unpredictable nature of the impact of scientific advances which allows major impacts to occur in areas not foreseen As a stand-alone argument for a scientific research project, such justification is inadequate. It should not be overlooked, however, as a potential benefit of a scientific program, especially one focussed so closely on real materials obstacles in a real applications environment.

UNIVERSITY AND INDUSTRY OPPORTUNITIES

The applications area of first order relevance of this class of programs is of insufficient commercial promise to attract the attention of the industrial laboratories whose facilities and manpower make them optimal for attacking the problems involved. The commercial potential of neural prosthesis or neurophysiological investigative tools is insignificant compared to that of microprocessors or central processing units or generalized memory. The role of the industrial laboratories in attacking the materials problems of implantable electronics is destined, therefore, to remain a supportive and peripheral one, not a central one. The key work must and should be done in university laboratories, and represents a major opportunity area for university laboratories, especially in those situations where a strong materials science group, a strong electronics group (with integrated circuit process capabilities) and an interested medical school exist together. The overwhelming depressant on work of this kind has been the lack of governmental funding available. The medical flavor of the problems moves them - or in the past has strongly tended to move them - outside the charter interest area of all Federal agencies other than the NIH. The NIH, on the other hand, is not set up organizationally or philosophically to support technology of relevance to medical problems until and unless that technology has reached the stage of applicability where its impact on a specific disease or disability can be demonstrated. The review procedures of the NIH involve personnel who are generally non-technical and materials and engineering grants proposals have small chance of support. If the material and technological studies described in this report are to be implemented, it is vital that funds be designated, and an agency mission assigned, to bring about the implementation. It is also clear that these funds should be directed at university laboratories, though a collaborative effort between a university and industrial laboratory would have real virtue if the industrial participation were genuine. The area of materials technology for implantable electronics represents at present a genuine, largely unrealized, scientific opportunity, in which some attention should be focussed.

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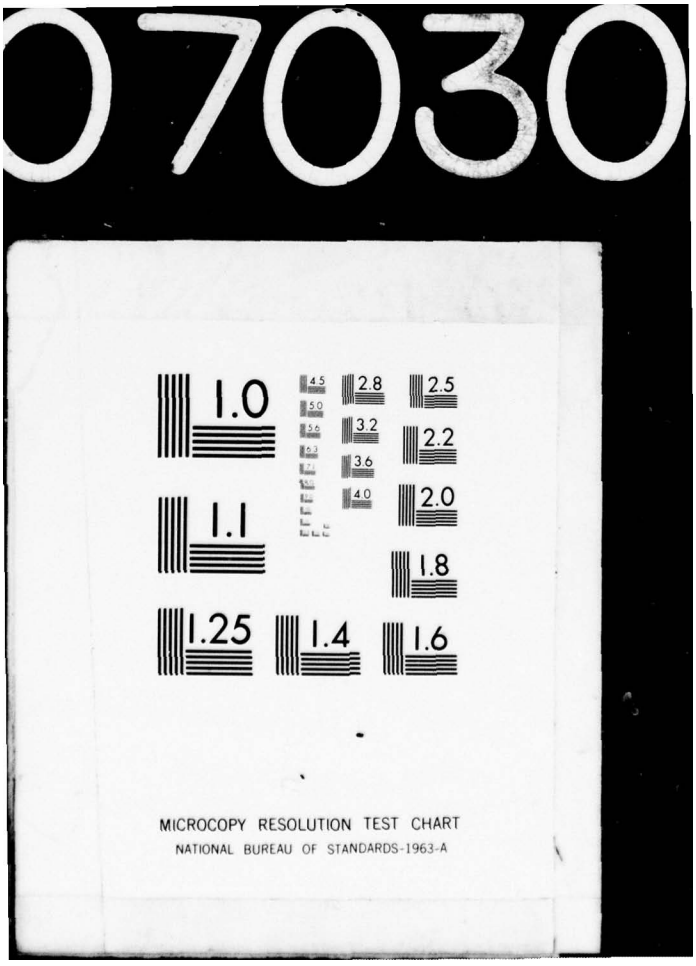
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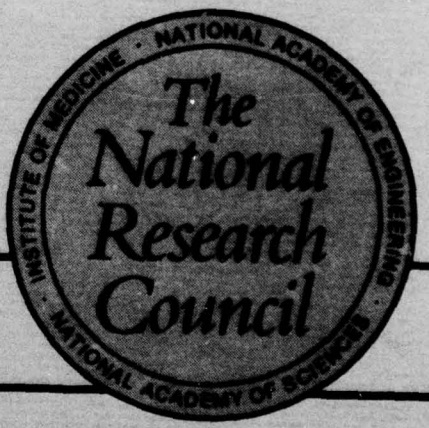
Microstructure Science, Engineering, and Technology



Panel on Thin-Film Microstructure Science and Technology

Solid State Sciences Committee

Assembly of Mathematical and Physical Sciences

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Microstructure science, engineering, and technology are essential to the continued economic well-being and security of the U.S. A sustained long-range research program directed toward an understanding of the scientific and engineering base on which future technological developments will rest is essential. A greater involvement of universities in microstructure science and engineering is necessary for continued progress in microstructure fabrication, as well as to increase the number of people trained in this field. The general ideas that need new and expanded research include: configured (over)

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materials; materials characterization and analysis; device physics and electronics; system architecture and design; pattern generation and transfer; new scientific phenomena and materials; and new instruments. An essential feature of this report is identification of research needs and opportunities. The Panel recommends that three complementary types of activities or organizational modes be established to meet national needs in microstructure science, engineering, and technology.

Microstructure Science, Engineering, and Technology

Panel on Thin-Film Microstructure Science and Technology
Solid State Sciences Committee
Assembly of Mathematical and Physical Sciences
National Research Council

NATIONAL ACADEMY OF SCIENCES
Washington, D.C. 1979

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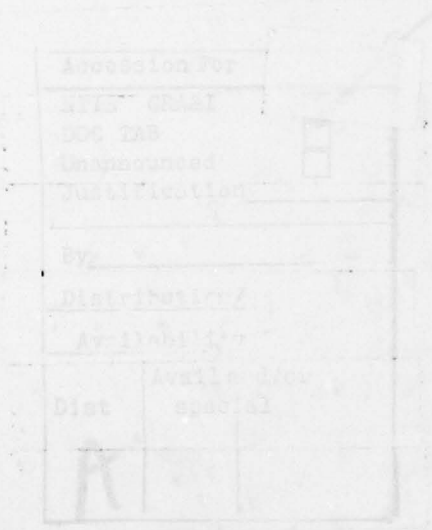
This report has been reviewed by a group other than the authors according to procedures approved by a Report Review Committee consisting of members of the National Academy of Sciences, the National Academy of Engineering, and the Institute of Medicine.



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Preface

Modern solid-state electronics depends on microstructure science, engineering, and technology, which form the basis for the fabrication and use of composite thin-film structures with specified patterns having lateral features with dimensions on the order of or less than 10 μm. Recognizing the importance of microstructure science, engineering, and technology, the Solid State Sciences Committee of the National Research Council's Assembly of Mathematical and Physical Sciences appointed a group in 1977 to make a preliminary assessment of the needs in this field and to recommend a course of action to the Committee. The group prepared a resource paper in which it concluded that U.S. leadership in microstructure science, engineering, and technology is of vital importance to the nation's economic health and security and that a higher level of research activity in microstructure science is needed to sustain that leadership. These findings, together with concern among leaders in the field, prompted the Solid State Sciences Committee to organize an *ad hoc* Panel on Thin-Film Microstructure Science and Technology. This Panel was charged with conducting a study of national needs and opportunities in thin-film microstructure science and technology. It was instructed to emphasize those opportunities most appropriate for university-based research and for cooperative efforts between universities and industry.

At its first meeting in July 1978, the Panel established four subpanels, each chaired by a panel member:

1. Materials Aspects of Microfabrication (A. Reisman)
2. Pattern Generation and Transfer (T. E. Everhart)
3. Devices, Integrated Circuits, and Integrated Systems Design (D. K. Ferry)
4. Science Opportunities (P. J. Stiles)

A series of panel and subpanel meetings took place during the period from July 1978 to April 1979. Panel members also participated in the "Workshop on Opportunities for Microstructure Science, Engineering, and Technology" held at Airlie, Virginia, in November 1978, which was jointly sponsored by the National Science Foundation and the Panel. The report and recommendations are based on the background material assembled by the subpanels and on discussion in panel and subpanel meetings and at the Workshop.

I am grateful to all members of the Panel and those whom they consulted. The time and interest they devoted to this project in spite of their busy schedules made this report possible.

I also acknowledge with gratitude the financial support provided for the study by the Army Research Office (Contract DAAG29 78C 0032), the Office of Naval Research (Contract N00014 78C 0733), and the National Science Foundation (Contract C310-T0 400).

Norman G. Einspruch, *Chairman*
Panel on Thin-Film Microstructure
Science and Technology

Contents

1
Introduction

The modern era of electronics has ushered in a second industrial revolution. With the invention of the transistor, followed by the development of the solid-state computer and the invention of the integrated circuit about a decade later, dramatic and rapid changes have taken place in communication, computation, recreation, and defense. Although this new industrial revolution is in its infancy, electronics already pervades every facet of our lives and will do so increasingly over the next few decades. No plateau is yet foreseen for this new industrial revolution; its impact on society could be even greater than that of the original industrial revolution.

The United States has led in the development and exploitation of modern solid-state electronics technology; whether it will maintain this leadership is by no means certain. Through various means of technology transfer, U.S. technical capabilities have been disseminated worldwide. Beneficiaries of this expertise now participate effectively in indigenous markets from which the United States is excluded, and they compete directly with this country in third-party markets. In particular, Japan is now a major supplier of consumer electronics. Furthermore, Japanese industry, with active and extensive support from the Japanese Government, has mounted an intense research and development effort in microfabrication; the goal of this determined effort is to become a world leader in computer technology and the semiconductor technology on which it is based. Moreover, a number of significant research and development efforts are under way in England, Holland, France, and West Germany. In addition, the technologies employed in national defense depend on semiconductor electronics; therefore, leadership in semiconductor electronics is essential to our national security.

Thus far, the semiconductor electronics industry has been based firmly in physics and chemistry. A reduction in scale of the characteristic dimensions of electronic devices into the micrometer and submicrometer range is imminent, and technical applications are outstripping their scientific base. Consequently, many future needs require new fundamental knowledge. For example, many standard devices will not operate at the submicrometer scale as they are currently designed, new lithographic techniques will have to replace optical lithography, and new capability to control materials structures at the micrometer scale will be needed. Such capability may lead to new science. These factors, together with economic and national defense considerations, indicate the need for an assessment of the status of modern semiconductor electronics.

The basis for modern semiconductor electronics is microstructure science, engineering, and technology (MSET), which encompasses the fabrication and utilization of composite thin-film structures with specified patterns having lateral features with dimensions of less than about 10 μm. *It is the primary conclusion of this study that a sustained, long-range program of research in microstructure science and engineering is necessary to provide an understanding of the base on which future technological developments must rest.*

This report consists of five chapters and an appendix. Chapter 2 is a statement of the Panel's conclusions and recommendations. Chapters 3 through 6 deal, respectively, with Materials Aspects of Microfabrication; Pattern Generation and Transfer; Devices, Integrated Circuits, and Integrated Systems Design; and Science Opportunities. The Appendix consists of a collection of expert assessments of the materials aspects of MSET.

2
Conclusions and Recommendations

In Section A, general conclusions of the Panel, based on background material assembled by the subpanels and on discussions in panel and subpanel meetings and at the Workshop, are presented. These conclusions deal with the status of microstructure science, engineering, and technology (MSET) programs in the United States and provide a basis for the Panel's recommendations, which are offered in Section B, for the establishment of a new and expanded set of research programs to ensure and enhance future advances in the field. A summary of selected research areas and problems that should be emphasized appears in Section C.

A. CONCLUSIONS

1. Microstructure science, engineering, and technology are essential to the continued economic well-being and national security of the United States. Microstructure fabrication is at the research frontier of semiconductor electronics and is basic to the communications and control and information-processing industries. A sustained long-range research program directed toward providing an understanding of the scientific and engineering base on which future technological developments will rest is essential.

2. Microstructure developments that are foreseeable require further advances in basic science. Laboratory techniques have been pushed to the limits of about 0.1 to 0.01 μm for extremely simple structures. This size falls within a range for which there is a peculiar gap in the understanding of condensed matter, since one cannot, with confidence, extrapolate upward from the atomic scale, nor downward from the bulk solid state. Readily identifiable problems, such as carrier statistics and dielectric breakdown, can prevent straightforward scaling, if indeed scaling is valid. Therefore, new effects, leading to new devices and to novel approaches to design problems of present devices, are sought, and a much deeper understanding of what modifications are induced at submicrometer dimensions is essential. New modes of thought will be necessary in other sciences. Particularly noteworthy is the prospect of extremely large arrays of computing assemblages likely to demand entirely new computer architectures.

3. A greater involvement of universities in microstructure science and engineering is necessary for continued progress in microstructure fabrication, as well as to increase the number of scientists and engineers trained in this field. Universities can effectively contribute needed long-range basic research, which underlies future technological development. Currently, the worldwide semiconductor electronics industry has annual sales of about $7 billion, with a growth rate of about 20 percent per year, and more than 200,000 employees. If the number of professionals working in the field is to increase at even a fraction of the rate of expansion of the industry as a whole, a considerable increase in the numbers of scientists and engineers being trained for it will be necessary, including university graduates trained in basic microstructure science and engineering. The competitive job market that currently characterizes this field indicates that a need already exists.

4. Microstructure science and engineering have not been generally recognized as constituting a discipline or a readily identifiable, coordinated, national set of major research programs. One serious consequence has been a lack of support for research addressed to significant problems that fall between the boundaries of the traditional disciplines and thus are not recognized.

5. The general ideas that need new and expanded research include (a) configured materials, (b) materials characterization and analysis, (c) device physics and electronics, (d) system architecture and design, (e) pattern generation and transfer, (f) new scientific phenomena and materials, and (g) new instruments. Each of these is discussed in Section C of this chapter, where selected topics are also emphasized. Chapters 3–6 and the Appendix describe over 90 specific research areas of importance to the complex, multidisciplinary, scientific and engineering base for technological developments in microstructure fabrication. Advances will depend increasingly on these activities as structural dimensions decrease and the density of elements on a chip increases.

B. RECOMMENDATIONS

1. *To ensure a sound basis for future technological advances, the Panel recommends that a new and expanded set of coordinated research programs in microstructure science and engineering be established.*

The dramatic successes of our domestic semiconductor industry have been based mainly on innovative techniques for miniaturizing semiconductor circuitry. However, a qualitative change in the nature of these developments is expected during the next decade. The scale of size is decreasing to such an extent that the basic science is not well established. Factors that could be disregarded as having only minor influences in larger devices are becoming of major importance.

There are few guides for developing even empirical approaches. Advances in fundamental understanding are needed for future technological efforts. There are challenging research problems that will attract outstanding scientists and engineers. In addition, these advances will result in novel instruments that can be expected to lead to new insights into our natural world. These insights are expected to have profound effects far beyond the realm of semiconductor electronics in which microstructure studies originated. The following specific recommendations are made to implement a coordinated research program.

2. *The Panel recommends that scientific and engineering research programs be established to encompass new and expanded activities in various selected areas of (a) configured materials, (b) materials characterization and analysis, (c) device physics and electronics, (d) system architecture and design, (e) pattern generation and transfer, (f) new scientific phenomena and materials, and (g) new instruments.* Each of these areas is broad in scope, with many outstanding needs and opportunities that should be addressed as technology advances with ever-smaller dimensions and more-demanding materials requirements. Selected areas are summarized in Section C of this chapter, and more than 90 are discussed in the remainder of the report. These needs are diverse, complex, and involve many traditional disciplines, including physics, chemistry, materials science, computer science, mathematics, and several engineering fields.

3. *The Panel recommends that the research programs recommended above comprise a coordinated set of activities encompassing new and expanded activities in various selected areas primarily at universities, with additional efforts devoted to strengthening cooperative efforts between universities and industry and to nonproprietary research and development programs in industry.* Many of the needs for new basic research and the education of scientists and engineers in basic and applied microstructure science and engineering can be met by activities in universities. Interactions between certain universities and the semiconductor industry have been highly productive. Effective methods of encouraging such interactions are important and should be pursued.

4. *The Panel recommends that three complementary types of activities or organizational modes be established to meet national needs in microstructure science, engineering, and technology*:

- *Regional Resource Centers*
- *Specialized Area Thrusts*
- *Individual Research Grant Programs*

Organizational descriptions and rationale for these follow.

Regional Resource Centers should typically involve several complementary and interdisciplinary activities, be oriented to a combination of internal and external users, have five to ten internal principal investigators and permanent support staff, and receive initial capitalization of about $2.5 million and annual funding of about $1.5 million for equipment and operations. Certain needs in MSET are best met by large and coordinated centers, which are envisaged to be comparable in scope with the Materials Research Laboratories and the Cornell Submicron Facility. Such centers are needed to provide certain sophisticated and costly facilities and support personnel for a wide range of external and internal users. These centers would be for exploratory research rather than extensive development, which would be carried out in industry. Possible centers include, among others, an exploratory very-large-scale-integration (VLSI) center, a major submicrometer lithography center, and an exploratory device/circuit fabrication center.

Specialized Area Thrusts should be oriented mainly toward internal users, have from two to four principal investigators and permanent support staff, and receive total funding of about $200,000–600,000 per year. Many microstructure scientific and engineering research programs require multidisciplinary and costly skills and techniques. Rarely have such programs been supported, because their size places them outside the scale of the normal individual research grant program. An example is microstructure materials synthesis and characterization involving expensive

equipment (such as a scanning transmission electron microscope or a scanning Auger microscope).

Individual Research Grant Programs should be directed toward advancing the leading edge of basic research in specific areas of microstructure science and engineering, have one or two principal investigators and permanent support staff, and receive funds up to about $250,000 per year. Many important needs discussed in Chapters 3–6 and the Appendix can be addressed by well-focused individual research grant programs.

5. *The Panel recommends that the coordinated long-range commitments described above be made immediately to meet national needs in microstructure science and engineering.* As a response to these needs, we recommend that (a) two or three Regional Resource Centers, (b) about 10–15 Specialized Area Thrusts, and (c) about 20–30 Individual Research Grant Programs be established over the next three years. The Panel concluded that this level of funding is a minimum response to permit the pursuit of only the most promising of the diverse opportunities and needs summarized in this report. The specific number and nature of these activities will be determined by the scientific scope and quality of the proposed research. There are many possible regional sites for the establishment of resource centers. There are also numerous programs suitable for area thrusts and individual grants, as summarized in Section C of this chapter and discussed in Chapters 3–6 and the Appendix. The approximate cost of this recommended program, for the first three years, based on two new resource centers, about 12 area thrusts (average cost of each about $400,000 per year), and about 24 individual grants (average cost of each about $125,000 per year) would be about $30 million. Fulfillment of the many needs summarized in this report would require comparable additional growth in subsequent years.

C. SUMMARY OF RESEARCH NEEDS

An essential feature of this report is identification in detail of the research needs and opportunities in microstructure science and engineering (Chapters 3–6 and the Appendix). Seven areas are indicated in the Conclusions and Recommendations; here, we provide a summary of the research needs in each of these. Although there is substantial activity in these areas in industry, there are many research needs that must be addressed as characteristic dimensions shrink into the submicrometer regime.

1. Configured Materials

(a) A detailed understanding of size- and surface-dependent transport phenomena is needed at the micrometer and submicrometer scale of dimensions.

(b) Important deposition, growth, and etching processes must be understood and developed to permit the fabrication of microstructures in a controlled and predictable manner.

(c) Certain processes involving the interaction of radiation (photons, electrons, and ions) with matter must be understood to permit the fabrication of microstructures in a controlled and predictable manner.

(d) Various chemical, electronic, and structural aspects of interfaces and surfaces must be further explored, since they often govern physical effects in the submicrometer domain.

(e) New materials configurations and their applications should be explored.

2. Materials Characterization and Analysis

(a) Existing techniques and instruments for characterization and analysis of materials need to be extended for use at micrometer and submicrometer dimensions.

(b) New techniques and instruments for characterization and analysis of materials need to be developed to study interiors of solid composites.

3. Device Physics and Electronics

(a) Improved electronic and magnetic device modeling is necessary to understand phenomena that become important in the submicrometer domain.

4. System Architecture and Design

(a) A unified approach to very-large-scale integration (VLSI) that combines materials science, physics, engineering, and computer science with systems and device design is needed to obtain new architectural and organizational concepts for integrated systems.

(b) Specific attention must be paid to the increasingly important roles of interconnections and packaging.

5. Pattern Generation and Transfer

(a) Instrumentation

(1) Relatively low-cost instruments (about $100,000) for pattern writing must be available for experiments on resist sensitivity and resolution, small-structure research, and small-device fabrication.

(2) Development of generally available, high-throughput, direct-writing electron-beam systems and lithography for VLSI production at the submicrometer scale is needed.

(3) Metrology instrumentation should be developed for wafer distortion measurements and control.

(4) Development of ion-beam instruments for serial writing, resist exposure, direct milling of materials, implantation, and damage writing is needed.

(b) Resists

(1) Efforts are required to improve the resolution, sensitivity, and contrast of electron-beam polymer resists.

(2) Further development and understanding of inorganic resists should be undertaken.

(3) Development, evaluation, and understanding of resists for dry processing should be undertaken.

(c) Resistless processing: Directed, particle-beam-assisted etching and implantation techniques for maskless microfabrication should be explored.

(d) Low-temperature processing, oxidation, and impurity incorporation techniques should be studied to achieve improved device designs and minimize process-generated defects.

6. New Scientific Phenomena and Materials

Microstructure fabrication capabilities are needed to construct submicrometer structures and materials configurations that will permit new studies of important phenomena.

(a) Electronic quantization: As the size of a structure decreases, the discreteness of its energy levels becomes controllable and measurable. Devices that take advantage of this discreteness may follow.

(b) Many diverse systems have characteristic lengths that are in the thousand-angstrom scale, and submicrometer fabrication will enable exploration of such phenomena.

7. New Instruments

Submicrometer fabrication capability will make possible a variety of novel instruments of unique value to scientific research in a number of diverse fields.

(a) Astrophysics: Submicrometer devices are needed to study celestial objects at high frequencies in the far infrared or with increased contrast imaging arrays in the visible.

(b) Medical science and biology: There is a clear need for ultrasmall monitoring instruments for use *in vivo*.

3
Materials Aspects of Microfabrication

A. INTRODUCTION

The materials aspects of the science and technology of microfabrication should be considered in the context of nonequilibrium composite structures. Such a conceptual view applies to microminiaturized structures that form the basis of the semiconductor, magnetic integrated optics, and display areas. Because geometric microminiaturization involves the scaling of size in three dimensions, surface-to-volume ratios increase, and eventually, surface properties begin to dominate the properties of a composite constituent. Consequently, interface and defect phenomena become paramount concerns. The behavior of microminiaturized structures, as a result, reflects second-order effects rather than the first-order effects we normally associate with bulk materials, even when they occur in composite form. For example, surface electromigration may become more important than bulk electromigration, interface resistivity in contact openings becomes as important or more important than the resistivity of the metal forming the contact, and defects in insulators become more important than the bulk dielectric properties of the insulators. Fabrication within prescribed tolerances becomes more demanding, and we frequently require detailed knowledge of structures or interfaces buried within the overall structure.

Our basic understanding of scaling-associated changes in the properties of materials is primitive. The consequences of the interactions of ionizing and nonionizing radiation (electrons, photons, and ions) with such composites are not well understood, nor are the chemistry and physics of etching, deposition, and growth of very small structures. We understand surfaces, interfaces, and defects in only a few materials, and not in any depth even in these. Further, tools for characterization and analysis are not sensitive enough, or are nonexistent. We offer the following broad generalizations.

- The context of nonequilibrium composite structures is central.
- Properties of microminiaturized structures are not generally deducible from the bulk properties of their composite constituents.
- Properties frequently must be assessed on the configured structure.
- Interface properties are frequently as important as bulk characteristics.
- Interfaces are, in effect, a "new material."
- Scaling causes so-called second-order effects to become more important than so-called first-order effects.
- Surface-to-volume ratios are large.
- Surfaces are, in effect, a "new material."
- The device frequently must be used as a material probe.
- Defects play an important role.
- Model systems often have little value.
- Reliability issues are paramount for microminiaturized structures.

In this chapter, we deal with the needs in several important areas. We attempt to highlight key issues rather than present a comprehensive treatment.

Section B consists of three parts: in Part I we provide a broad outline of major areas requiring attention; in Part II we offer a more detailed outline; Part III is a preview of Sections C and D, in which we emphasize specific needs in materials applications.

In Section C we discuss materials needs somewhat differently and in greater depth than in Section B. We focus on selected subjects such as interconnections, contacts, techniques for film growth, characterization of small structures, and attempts to tie these fields together.

In Section D we address the needs defined in Section C more broadly in five representative areas of applications.

The Appendix at the end of the book is made up of detailed papers on the topics considered in Section C.

B. GENERAL SUMMARY OF NEEDS

I. Broad Outline of Major Areas Requiring Attention

1. Configured Composites

(a) Scaling of structures and processes

(b) Consequences of the interactions of ionizing and nonionizing radiation with matter

(c) Chemistry and physics of etching

(d) Chemistry and physics of deposition and growth

(e) Surfaces and interfaces

(f) Chemical, electronic, and structural aspects of defects

(g) New materials, techniques, and applications

(h) Reliability studies

2. Materials Characterization and Analysis

(a) Extension of known techniques to microdimensions

(b) Development of new techniques to study interiors of solid composites

II. More Detailed Outline of Major Areas Requiring Attention

1. Configured Materials

(a) Scaling of structures and processes
- Surface properties versus bulk properties
- Electromigration at surfaces and interfaces
- Current density effects
- Tunneling through insulators and across interfaces
- Fluctuation phenomena
- Process modeling

(b) Consequences of the interaction of ionizing and nonionizing radiation (electrons, photons, and ions) with matter
- Localized energy absorption mechanisms
- Process-induced radiation damage
- Interactions of radiation with lithographic materials
- Use of radiation techniques for analytical purposes
- Ion implantation

(c) Chemistry and physics of etching
- Wet and dry etching
- Isotropic and nonisotropic etching
- The etching of single-crystal, polycrystalline, and amorphous materials
- Phase and/or dopant sensitive etching
- Etching kinetics

(d) Chemistry and physics of deposition and growth
- Molecular-beam, plasma-assisted, liquid-phase, electrochemical, and physical deposition
- Controlled-area deposition and ablation
- Low-pressure and conventional chemical vapor deposition
- High-pressure oxidation and growth of materials
- Incorporation of desired electrical and mechanical processes
- Kinetics of growth
- Role of contamination by process gases

(e) Surfaces and interfaces
- Adhesion of composites and nature of binding
- Electrical properties of interfaces and surfaces
- Diffusion and alloy structure of interfaces
- Interface defects
- Chemical and physical modification of surfaces and interfaces
- Passivation of surfaces

(f) Chemical, electronic, and structural aspects of defects
- Single-crystal, polycrystalline, and amorphous materials
- Distribution, number, size, clustering
- Electrically active or neutral
- Process- and geometry-induced defects
- Role of defects in dielectric breakdown
- Deactivation and removal

(g) New materials, techniques, and applications
- Polymeric conductors, semiconductors, insulators
- Inorganic and organic photosensitive materials
- Self-passivating conductors
- Contact barriers and materials
- Surface film control of electromigration
- Submicrometer magnetic bubble materials
- Compatible composites for nonsilicon semiconductors
- Locally modifiable optical materials for projection displays and integrated optics
- Modeling of processes involving composites
- Formation of arrays of electrodes over large areas
- New doping techniques such as those involving the use of organometallics
- Self-passivating high-conductivity materials

(h) Reliability studies
- Long-term stability of devices
- Long-term stability of composites
- Electrical and physical stress and reliability

2. Materials Characterization and Analysis

(a) Extension of known techniques to microdimensions

- Scanning Auger microprobe
- High-voltage scanning transmission electron microscope
- Rutherford backscattering
- Scanning electron microscope
- Scanning energy-dispersive spectroscopy

(b) Development of new techniques to study interiors of solid composites

- Microwave acoustics
- Nondestructive techniques
- X-ray Fresnel zone plates
- Local diagnostics derived from nonlocal measurements
- Low- and high-pressure gas diagnostics
- Solid–liquid interface probes

III. Proposals for Study in Selected Areas

1. Inorganic Resists and their Radiative Patterning

(a) Studies of the radiation sensitivity of glassy inorganic materials, and study of etching kinetics for differential methods of etching exposed and unexposed regions of these to understand their etching anisotropy using wet and dry etchants

(b) Studies of the technique for forming films of such materials, controlling their sensitivity to radiation, quantifying their resist properties (etch rate, solubility, resolution), and other properties (electrical, magnetic, and mechanical)

(c) Studies to determine whether ion beams for resist exposure offer any potential in terms of resolution, exposure time, and cost

2. Plasma Etching

(a) Development of plasma gases capable of anisotropically and selectively etching a variety of metallic films, e.g., permalloy, materials other than silicon, such as garnets, III–V's, and ternary alloys of these, niobates, zinc oxide

(b) Study of the chemistry and physics of the interaction of reactive plasmas with semiconductors and their dependence on control variables such as power input, pressure, flow rate, and reactor design

(c) Understanding of plasma-etch radiation-induced damage

(d) Study of the surface chemistry and physics of systems subjected to reactive gas plasmas, e.g., to understand specific chemical interactions in etching, the role of additives, the kinetics and energetics of nonequilibrium processes, the role of surface roughness, and stoichiometry

3. Conventional Interconnections

(a) Studies of chemical systems possessing high conductivity and the ability to withstand elevated temperatures

(b) Studies of the ability of such systems to form low-defect density passivating insulators on their surfaces

(c) Studies of methods of forming and patterning such systems, removing defects introduced during patterning, and controlling grain size during growth and heat treatment

(d) Studies of ways to incorporate such technologies into device-fabrication procedures to achieve pinhole-free, leak-free, multilayered devices, with good adhesion between layers

4. Unconventional Interconnections

(a) Extensive further study of $(SN)_x$, polythiazyl, and derivatives of it, including studies of halogen partially oxidized $(SN)_x$ polymers, to understand better the range of conductivity of such polymers, their reproducibility, and the effect of structural variations on the physical, mechanical, and electrical properties of these materials

(b) Similar studies of another class of polymeric conductors $(CH)_x$, polyacetylene, whose conductivity can be varied over 11 orders of magnitude from nominally metallic values to nominally insulating values, and which may be doped *n*- or *p*-type, a property that has hardly been explored

(c) Similar studies of graphite intercalation compounds that offer the potential of being useful as anisotropic conductors, which in one direction conduct like metals, and which behave as insulators in a direction perpendicular to this "in-plane" conduction direction

5. Electromigration Phenomena

(a) Studies of the relation (proportionality) of the electron "wind force" to the magnitude of the electric current in grain boundaries

(b) Studies of the effects of defects, impurities, and grain boundaries on electromigration in thin films of the order of 0.1 μm or less

(c) Studies of electromigration on surfaces and in contacts, and of the effects of dielectric-layer overcoats and various gaseous ambient atmospheres and contaminants on surface and grain-boundary electromigration

6. Insulators

(a) Investigation of the relationship of processing to defect formation, and of reduction of the latter by postprocessing treatments and/or developing techniques for forming trap- and defect-free oxides

(b) Determination of the nature of defects and traps and annealing mechanisms, the behavior of surface and interface traps, and the phenomenon of dielectric breakdown, especially as it relates to defect state

(c) Study of the properties of ultrathin oxides, the effects of impurities on oxidation rates, the effects of competitive reactions on oxidation rates, and the properties of the resulting insulators, e.g., the competitive $Si + SiO_2 \rightleftharpoons 2SiO$ reaction

(d) Study the role of oxide/insulator formation, interfacial reactions, and growth kinetics in materials other than Si

(e) Development of new processes for formation of insulator systems, e.g., plasma oxidation and high-pressure oxidation

(f) Development of techniques for low-loss coupling of optical microelements, e.g., optical fibers to thin-film waveguides

(g) Study of new insulator systems for use in multilayer electronic devices and in integrated optical devices

7. Contacts

(a) Quantification of the exact limitations of Al–Si alloy systems in small-contact, shallow-junction applications

(b) Study of the effect of stresses on aluminum penetration through silicides or into silicon directly

(c) Study of the fundamental properties of interfaces, e.g., growth kinetics, intermediate compounds, equilibrium compounds, and electronic structure and transport, resistivity, the effect of ambient atmosphere treatments, and the specific properties of the metallurgical system

(d) Study of new contact metallurgies, which must be examined in the context of providing ohmic contacts, preferably with barrier-layer properties, to enable contacts to be made to shallow junctions in Si and other semiconductors

(e) Study of the effect of defects on contact behavior

(f) Development of high-temperature contact metallurgies

8. Defect Removal and Laser Annealing

(a) Development of techniques for control of laser pulse size (energy) and spatial homogeneity and development of tunable lasers in the 1–4 eV range

(b) Investigation of the optical properties of ion-implanted materials subjected to intense radiation, and the thermal properties of materials near their melting points, e.g., the variation of conductivity with temperature

(c) Investigation of the diffusion coefficients of dopants in liquids

(d) Investigation of segregation coefficients in high-velocity recrystallization processes

(e) Study of heteroepitaxial growth processes using laser melting techniques, e.g., silicon on sapphire, and the potential for removing defects in such layers, which limit the quality of devices

9. Formation of Thin Films

(a) Study of low-temperature techniques for film formation, e.g., plasma-assisted processes, in the context of obtaining films with characteristics normally associated with high-temperature film-formation process, especially the kinetics of growth and nucleation

(b) Development of techniques for controlling grain size and enhancing adhesion in metal films in the context of specific materials systems in which they are to be used, including questions relating to defect structure and doping

(c) Further study of differences seen between vapor- and liquid-phase grown films

10. Microstructure Formation

(a) Study of the kinetics of etching of single-crystal materials in known etchants and evolution of new etchants

(b) Development of etch masks to control the structure to be delineated, which involves the definition of suitable mask systems, study of their adhesion to the structure they are masking, and study of their resistance to the etchants

(c) Exploration of novel anisotropic approaches, e.g., deep crystallization of glassy materials through inorganic resist concepts, and development of techniques to achieve selective etching (here the potential is huge, for one can envision extremely high aspect ratios resulting)

(d) Study of electrochemical techniques for building the third dimension, which might involve evolution of catalytic approaches

(e) Exploration of selective area deposition of thick and thin films, including the possibility of radiation-enhanced deposition at desired sites

(f) Exploration of techniques of impurity incorporation in three-dimensional microstructure, e.g., focused ion beams

11. Characterization of Microminiaturized Structures

(a) Evolution of technologies for analysis with enhanced sensitivity (enhanced signal/noise ratios) at smaller dimensions

(b) Development of less-expensive and perhaps specialized tools, to make their availability greater

(c) Development of depth-imaging tools for examination of the interior of composites

(d) Development of techniques for examination of interfaces

IV. Applications

1. Semiconductor Electronics

(a) Investigation of the effects of wafer-preparation techniques on finished device properties

(b) Lower-temperature processing

(c) Improved control of tolerances, both geometrical and chemical

(d) Study of parameters that affect and control polycrystalline film grain size

(e) Study of contact metallurgies, and the effect of different metallurgy processes on the control of contact resistance

(f) Control of lithographic resist properties, e.g., sensitivity.

2. Magnetic Bubbles

(a) Device forms that do not require proportionately large drive fields

(b) Chip organizations that yield shorter access times

(c) Methods for increasing domain motion to speeds >10 m/sec

(d) Development of new bubble materials systems that can support small bubbles (<0.4 μm) at low drive fields, which may include more complex double- and triple-layer systems, amorphous bubble systems, and surface-modified structures in which bulk and surface properties are intentionally made different

(e) Study of metallurgical resistance to electromigration at high current densities

(f) Study of new ways to manipulate domain structures without direct access to each bit position

(g) Study of the mechanisms that induce and control magnetic anisotropy

(h) Study of methods for depositing and/or forming films that can sustain bubble structures

3. Integrated Optics

The needs of semiconductor electronics and magnetic bubbles, modified by the applications and materials needs of integrated optics, are fully applicable

4. Implantable Medical Electronic Devices

(a) Studies of biocompatible microinsulation techniques

(b) Studies of biocompatible micrometallurgical techniques

(c) Studies of interfacing and interconnecting in hostile environments, and passivation of the overall structures on a microscale

(d) Development of microelectrode array fabrication techniques in the context of items (a)–(c) above

5. Displays

(a) Studies of array fabrication of LED's and lasers at densities of 40 or more/cm

(b) Studies of mixed-array fabrication to provide multicolor capability

(c) Studies of novel array electrode fabrication techniques for use in electroluminescent and discharge-type displays

(d) Studies of fast-switching liquid crystal and electrochromic materials for displays

(e) Studies of techniques for fabricating arrays of deformable elements or elements optically different from the surroundings for use with reflection optics (projection displays)

(f) Studies of techniques for fabricating arrays of electrodes over large areas

C. SPECIFIC AREAS OF RESEARCH

I. Introduction

Materials science and technology of microfabrication is an extremely broad subject. Although in principle one can speculate that generalized approaches can satisfy the needs of many unrelated materials systems, experience shows that such is not generally the case. Each specific materials requirement must generally be investigated in the context of a given "materials system" comprising one or more interfaces, one or more sandwiches of thick and thin films, and, frequently, a substrate that might not exhibit bulk properties. Further, because of the end results desired, it is quite possible that each of the structural components of the materials system will be in a state of metastable equilibrium. For example, the impurity distribution in a semiconductor device often is intentionally tailored so that it is in a distinctly nonequilibrium state. The different adjacent nonequilibrium regions exhibit notably different properties that might be useful in achieving a desired end result. For example, the conductivity and the type of conduction are different, the resistance to etchants is different, and the rate of oxidation is different in the various *n*-type and *p*-type regions of such a metastable device.

Between each of the components of chemically different films is an interface with its own structure and chemical composition. For the case of very thin films, the surface-to-volume ratio is large, and, even in an ideal case, the properties of the interface often dominate the bulk characteristics of the films. Although the semiconductor materials that appear promising for device applications include gallium arsenide, indium phosphide, and ternary and quaternary III–V alloys, for purposes of illustrating some research relevant to microminiaturization, we will focus primarily on silicon-based devices in this section.

Consider the metal-oxide-semiconductor field-effect transistor (MOSFET), a cross section of which is depicted in Figure 3.1. It is a rather uncomplicated structure in its simplest form. We see that the bulk material, here *p*-type silicon, has buried within it two heavily doped regions referred to as source and drain. The source and drain are connected to an electrical supply and must not pass current between them (from the negative source to the positive drain) until a field is applied across the gate oxide by the gate electrode causing the *p*-type interface to invert to *n*-type, thus creating a continuous channel between the *n*-type source and drain. The gate voltage at which such conduction takes place is termed the threshold voltage, V_t. For large numbers of such devices to be connected to one another, their electrical characteristics must be controllable and stable; that is, they must exhibit the design threshold voltages, and the amount of current passed between the source and drain, with given voltage levels applied to each of them and with the application of a given voltage to the gate electrode, must be controllable within required tolerances. The amount of current for a given voltage is the electrical attribute known as the transconductance of the device.

As might be anticipated, the gate oxide (SiO_2) is not perfect. It contains varying amounts of traps, positively charged centers, that produce potentials that add to the positive applied gate voltage and therefore can cause unwanted changes in the threshold voltage of the device. If electrons (the majority carrier in such *n*-channel MOSFET's) manage to surmount the energy barrier of the interface between the

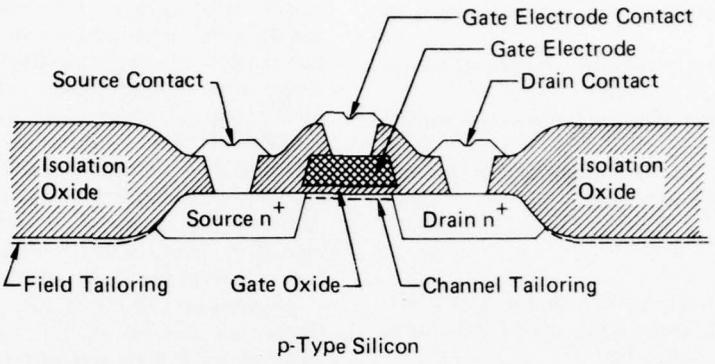

FIGURE 3.1 Schematic diagram of a metal-oxide-semiconductor field-effect transistor (MOSFET).

silicon and the gate oxide, they can create two effects: they can cause damage to the interface, creating so-called interface states that can degrade the transconductance with time; and they can become trapped at positively charged centers, neutralizing them, thereby increasing the threshold voltage at which the device turns on. Such electron penetration effects are results of "hot electron phenomena," of which two distinct types have been identified as smaller devices have been fabricated. One of these, the "channel" hot-electron effect, occurs as electrons move from the source to the drain when the device is turned on by applying sufficient voltage to the gate electrode, and results in nonohmic current transports as well as charge injection. The second is the leakage-induced threshold hot-electron effect. It arises because leakage electrons generated in the bulk of the silicon are accelerated perpendicular to the channel across the so-called depletion region existing below it during operation and plough across the silicon–silicon dioxide interface. The effects then become similar to those produced by channel hot electrons, interface damage, and neutralization of traps in the glassy oxide area.

We have discussed superficially only two of the interfaces in this simple device, those in its active regions. The properties of these two interfaces depend critically on the way in which they are fabricated, and their characteristics can be altered dramatically by subtle variations in the methods of fabrication. For example, it is now known that even such steps as the preoxidation cleaning of the silicon prior to growing an oxide can affect surface-state (interface-state) density. Stress levels at these interfaces can be altered by the manner in which they are formed, for example, the specific chemical process employed, and by the generalized processes used, for example, radiative or nonradiative. Thus, if electron beams are used to expose photoresists in preparation for delineating diffusion and/or metal contact aperatures in the several oxide regions, these beams cause, upon impact with the surface in question, the generation of x rays. X rays, which have considerable penetration power, generate positive charge in the oxides, which complicates control of the device electrical characteristics. In addition, they generate so-called neutral traps; this phenomenon was discovered as recently as 1976. These neutral traps, which are capable of trapping hot electrons, do not affect the properties of the "as made" devices, but they do affect the long-term stability (or reliability) of the devices. As they become filled by the so-called "lucky electrons," which penetrate the interface and become trapped, they too result in observed threshold voltage shifts. Development of methods for dealing with these process-induced radiative effects poses a major challenge in achieving a microminiaturization capability. Novel approaches to processing involve the use of plasmas to speed chemical reactions. Such methods are useful for lowering processing temperatures and achieving greater height-to-width anisotropy ratios in the structure, to better compliment the smaller wavelengths and greater depth of field when using electron-beam lithographic techniques. Another radiation problem that became evident in 1978 concerns the effects of low-level α-particle emissions from ceramics that serve as chip package substrates. These emissions can cause so-called "soft fails" in dynamic serial- and random-access memories as the devices comprising them become smaller. These α-particle emission rates, which are difficult to measure, are of the order of only a fraction to a few emissions/cm^2/hour from these ceramics.

Yet in a densely packed memory chip, they can cause large percentage-error failure rates/thousand hours of chip operation, because the stored charge in such small devices is measured in femtocoulombs (as low as 7–10 fC). Therefore, as we move further into the realm of microminiaturization, second- and third-order effects become first-order points of contention and must be dealt with accordingly.

Let us also consider one general area—contacts—that becomes increasingly important as the level of microminiaturization advances. Because of our greater understanding, the case is best made with reference to small semiconductor devices. The electrical characteristics of a semiconductor–metal contact interface system (or any other one) can be described in terms of its interface resistivity. For the aluminum–silicon interface, the interface resistivity has been reported as ranging between 10^{-5} Ω-cm^2 and 10^{-7} Ω-cm^2 attesting to the difficulty of making and interpreting the measurement. The relatively high value of this interface resistivity stems from the imperfect nature of interfaces (stress levels, disrupted crystallographic structure, nonabruptness of the chemical junctions, normal crystallographic defects, etc.). For the sake of discussion let us assume an interface resistivity of 10^{-6} Ω-cm^2 and a contact hole opening of 10 μm on an edge. The area of this opening is 10^{-6} cm^2, and the resistance of the contact is 1 Ω, a value that is hardly noticeable, since contamination in the contact hole opening causes greater variations in observed contact resistance than this more fundamentally determined value. Consider now a contact hole only 1 μm on an edge. The resistance is 100 Ω. If the interfacial resistivity is, in fact, 10^{-5} Ω-cm^2, the contact resistance is 1000 Ω.

For a 0.5-μm contact hole, the contact resistance in our nominal case is 400 Ω, and in the extreme case 4000 Ω. If these numbers were really fundamental, there would be a great question as to whether bipolar transistor circuits would be, in fact, designable or worthwhile at very small dimensions, since resistance–capacitance time constants would far outweigh the advantage of minimizing base widths to achieve an increased level of performance. The trouble is that we do not understand what part of the reported interface resistivity is fundamental, what part is due to the fabrication of the test structures, and what part results from the inadvertent formation of a contaminating interfacial film between the aluminum and the silicon. We must also question whether it is valid to extrapolate the bulk approximations for resistivity to microstructures. The entire formalism of transport theory in bulk materials may be invalid at these ultrasmall dimensions. That is, the time scales involved in small devices inherently require more detailed theories of transport, taking into account the spatial and temporal nonlocality. Even dielectric response on this time scale is not well understood.

Materials cannot generally be treated in the abstract but must be examined on an individual basis in the context of a materials system in which not only the nominal compositions must be quantified but properties must be specified in the context of the method of fabrication and precise structure of the system. The techniques we might apply to form the different microstructures and to characterize thin films, bulk, and interfaces cut across many disciplines. In addition, we wish to alert the scientist-technologist to the concept of utilizing the microstructure (the device) as the material probe. In the science of semiconductors such an approach has evolved almost naturally, and many of the current contributions to this science are made using the device as the probe of its own internal material characteristics. An interesting example of such a use, a problem that might otherwise have defied understanding, goes back to our example of process-induced radiation defects. Once the effects were catalogued, the next step was to see whether the several types of positively charged and neutral traps could be removed by thermal treatments in varying ambient atmospheres. With the use of capacitor structures, it was discovered that the positive charges could be removed by postprocess annealing in forming gas (nitrogen–hydrogen noncombustible mixtures). Process people then attempted such process anneals and, notwithstanding the body of data that predicted success, were repeatedly disappointed. What was discovered subsequently was a subtle difference between the prototype scientific study with capacitors and the device-process experiment, which better than any hypothetical case showed the necessity of treating the same materials system in precisely the same configuration and of utilizing the precise device as the materials probe. In the case of the capacitor materials system, the metal contact, of necessity, directly overlayed the thin oxide analog of the gate oxide in a MOSFET. In a conventional silicon-gate MOSFET, however, the metal contact to the gate electrode (the latter a thin polycrystalline silicon layer) does not lie superimposed over the gate oxide but rather lies removed at a distance from it. It was shown then that the removal of such traps requires the presence of aluminum directly over the region from which the traps are to be removed. The mechanism, which has yet to be elucidated unequivocally, probably involves a reaction between aluminum and entrained hydroxyl atoms in the oxide to form nascent hydrogen, which in some unknown way annihilates positive traps.

II. Research Needs and Opportunities

In this section we focus on selected subjects such as interconnections, contacts, techniques for film growth, characterization of small structures, and attempts to tie these fields together. The treatment of materials for microminiaturization is shown in Table 3.1. The columns indicate several major applications, and the rows represent activities that are important to some or all of the applications represented by the vertical rows with respect to progress toward microminiaturization (as indicated by an X mark at intersections).

We shall draw some general conclusions for these activities from the technical papers of Appendix 2. At best, these conclusions are pointers, for the needs are too specific to be

TABLE 3.1 Materials Aspects of Microfabrication

	Applications				
Aspects	Semiconductor Electronics	Magnetics, Bubbles	Integrated Optics	Medical Micro-structures	Displays
Deposition-etching	X	X	X	X	X
Formation of thin films	X	X	X	X	X
3-D microstructures	X	X	X	X	X
Electrochemical fabrication	?	?	?	?	?
Insulator phenomena	X	X	X	X	X
Plasma processes	X	X	X	X	X
Thin-film problems	X	X	X	X	X
Microcharacterization	X	X	X	X	X
Defects and annealing	X	?	?	X	?
Inorganic resists	?	?	?	?	?
Refractory interconnections	X	?X	?	X	?
Conducting polymers	?	?	?	?	?
Contacts	X	X	X	X	?
Electromigration	X	X	?	?	?
Medical applications of electronics	X	?	?	–	?
The device as a material probe	X	X	?	?	?

adequately generalized, and thus users of this document are urged to study the expert discussions.

1. Inorganic Resists and their Radiative Patterning

One of the key steps in microfabrication is the delineation or patterning of masks that serve either to block or expose underlying regions so that these can be processed subsequently. At present, the delineation of a mask involves an intermediate step in which a radiation-sensitive material is first patterned; this pattern is then used to pattern an underlying mask, which, in turn, is used to pattern underlying structures. This process is often expensive and wasteful and causes tolerance errors, because the radiation-sensitive mask, generally of organic nature, must be removed at some stage of the process, for it cannot be subjected to temperatures in excess of a few hundred degrees Celsius and, because of etch-bias considerations, it degrades the ultimate resolution of the radiative writing process. One approach to circumvent such problems is to employ inorganic films for patterning applications. A number of these have achieved some measure of success, but none is well enough understood to have achieved practical utility. Among the materials offering some potential are the arsenic and germanium chalcogenides, metallic halides, sulfides, selenides, and oxides of *titanium, iron, silicon, aluminum, and tantalum.*

What are needed to make inorganic masks, or other types of masks for that matter, pratical, taking into account the fact that the radiative technique most useful for extending microminiaturization is electron-beam exposure, are the following:

(a) Studies of the radiation sensitivity of glassy inorganic materials, and differential methods of etching exposed and unexposed regions of these to understand their etching anistropy using wet and dry etchant. The chemical kinetics of etching are not well understood in general, and in particular are not well described for these materials.

(b) Studies of the technique for forming films of such materials, controlling their sensitivity to radiation, quantifying their resist properties (etch rate, solubility, resolution), and other properties (electrical, magnetic, and mechanical). Again, the kinetics of nucleation, growth, and microstructure formation are not well characterized for these materials.

(c) Studies to determine whether ion beams for resist exposure offer any potential in terms of resolution, exposure time, and cost.

2. Plasma Etching

A second area that cuts across the discipline boundary involves the techniques for achieving patterning once the resist has become sensitized using radiative sensitization techniques. In theory, this patterning can be applied directly to the resist or to a region for which the resist serves as a mask. The patterning techniques that have received increasing attention in the past few years involve exposure of the material to be etched to a plasma-containing species that can react with this material to form volatile products. Like their wet chemical counterparts, to be useful, reactive plasmas must exhibit etch-rate anisotropies between the material to be etched and the material serving as an etch mask. To advance the state of this infant technology what are needed are the following:

(a) Development of plasma gases capable of anisotropically etching a variety of metallic films, e.g., permalloy,

materials other than silicon, such as garnets, III–V's, and ternary alloys of these, niobates, and zinc oxide. These gases must be characterized as to etch interactions and kinetics.

(b) Study of the chemistry and physics of reactive plasmas and their dependence on control variables, such as power input, pressure, flow rate, and reactor design. These studies must concentrate on not only equilibrium chemical states but also on nonequilibrium kinetics and intermediate state formation.

(c) Understanding of plasma-etch radiation-induced damage.

(d) Study of the surface chemistry and physics of systems subjected to reactive gas plasmas, e.g., to understand specific chemical interactions in etching, the role of additives, the kinetics and energetics of nonequilibrium processes, the role of surface roughness, and stoichiometry, including etchant-induced preferential decomposition of the surface in compound semiconductors.

Currently, the plasma etching has been applied most successfully, but nonetheless in a narrow range of uses, to silicon technology. Without research, the extension of such techniques to other areas is unlikely.

3. Conventional Interconnections

Another area, which for obvious reasons is important in microelectronics, is interconnections. Very-large-scale integration (VLSI) depends heavily on the interconnection of thousands of MOSFET devices of the kind we have discussed. The present MOSFET technology, using a polycrystalline film of silicon as a gate electrode, is termed silicon-gate technology. This polycrystalline silicon-gate layer is used not only as a control electrode but serves also as an additional level of wiring in densely packed structures. It can function in such a manner because it can be oxidized during processing to form an encapsulating and insulating layer of SiO_2 around itself. Conventional metal interconnections can then be passed over the polysilicon without shorting electrically to it. However, the resistivity of very heavily doped polycrystalline silicon is high compared with that of a metal, and when the area of a dense semiconductor chip is large, the resistance of long lines of polysilicon becomes too high and poses a serious problem in extending this technology. Further, the use of radiative processes in fabrication generates traps that must be removed. Processes for removal involve thermal annealing of the finished structure. However, there is a strong incompatibility between the temperatures required for trap removal and the temperature that usable materials, such as aluminum-contacting SiO_2, can withstand. This makes imperative the development of new interconnection technologies to overcome current limitations. The requirements for a useful metallization system are many: good adhesion to dielectrics, selective etchability, low electrical resistivity, good coverage of surface topography, resistance to electromigration, oxidation, corrosion, and low metal-to-semiconductor contact resistance. One such alternative involves the use of certain metal silicides the conductivity of which is 20 to 30 times that of the most conductive polycrystalline silicon and perhaps only 5 to 10 times lower in conductivity than aluminum. (The resistivity of heavily doped silicon is about 1000 $\mu\Omega$-cm, that of silicides ranges between 6 and 50 $\mu\Omega$-cm, and aluminum has a value of about 2 $\mu\Omega$-cm.) Needed are the following:

(a) Studies of chemical systems posessing high conductivity and the ability to withstand elevated temperatures.

(b) Studies of the ability of such systems to form low-defect-density passivating insulators on their surfaces.

(c) Studies of methods of forming and patterning of such systems, of removing defects introduced during patterning, and controlling grain size during growth and heat treatment.

(d) Studies of ways to incorporate such technologies into device-fabrication procedures to achieve pinhole-free, leak-free, multilayer devices with good adhesion between layers.

(e) Studies of interfacial reactions between silicides and the silicon, concentrating not only on the kinetics of silicide growth but also on intermediate compositions and equilibrium states.

4. Unconventional Interconnections

Conventional interconnections are fabricated from metals; in the previous section we discussed the needs as they affect VLSI. Unconventional interconnections refer to the class of conductors discovered recently that contain no metallic atoms. Their role in microminiaturization has not been explored, perhaps because our thinking on microminiaturization is often obscured by the immediate needs for VLSI. Upon reflection, a few potential uses come to mind, for example, the formation of flexible interconnections for medical prosthetic applications, interconnections in hostile environments such as body fluids, and interconnections in living tissues where rejection phenomena are severe.

To understand better the implications of polymeric conductors, several prototypes should be investigated in detail. Needed are the following:

(a) Extensive further study of $(SN)_x$, polythiazyl, and derivatives of it, including studies of halogen partially oxidized $(SN)_x$ polymers, to understand better the range of conductivity of such polymers, their reproducibility, their modifications, and the effect of structural variations on the physical, mechanical, and electrical properties of these materials.

(b) Similar studies of another class of polymeric conductors, $(CH)_x$, polyacetylene, whose conductivity can be varied over 11 orders of magnitude from nominally metallic values to nominally insulating values, and which may be doped *n*- or *p*-type. (This latter property has hardly been explored.)

(c) Similar studies of graphite intercalation compounds, which offer the potential of being useful as anisotropic conductors; in one direction they conduct like metals and in a direction perpendicular to this "in-plane" conduction direction they behave as insulators, particularly in regard to stability of the intercalate.

5. Electromigration Phenomena

In the 1960's, the impact of a known phenomenon, previously only a scientific curiosity, was felt in the semiconductor industry. The effect rose to prominence because, even in the gross microminiaturization of that day, it had made the transition from a second-order to a first-order effect. It was called electromigration and referred to the physical transport of metal atoms under the influence of the continuous bombardment of the metal atoms in aluminum thin-film conducting interconnections by the electrons moving through these interconnections. Although this problem has been dealt with successfully by restricting current densities in interconnections and incorporating impurities in the interconnections that make them more resistant to atomic displacement processes, future problems are anticipated. As miniaturization progresses, thicknesses decrease and contacts will become smaller. Furthermore, what were acceptable failure rates in the 1960's are intolerable today, and what is tolerable today is sure to be intolerable in the 1980's. Yet, the subject of electromigration in small contacts has received virtually no attention. Even in thin films, electromigration has been treated as a bulk phenomenon. With decreasing film thickness, as devices are scaled in the vertical as well as the horizontal direction, there will soon be primarily surface surrounding a vanishingly small bulk, and little is known about surface electromigration. In one instance it is enormous. What is not known is the impact of the metal–air interface on surface electromigration. In preparation for the next evolutionary or revolutionary thrust into the area of microminiaturization we require the following:

(a) Studies of the relation (proportionality) of the electron "wind force" to the magnitude of the electric current in grain boundaries.

(b) Studies of the effects of defects, impurities, and grain boundaries on electromigration in thin films of the order of 0.1 μm or less.

(c) Studies of electromigration on surfaces and in contacts, and of the effects of dielectric layer overcoats and various gaseous ambient atmospheres and contaminants on surface and grain-boundary electromigration.

An interesting aspect of item (c), which may include catalysis effects, is the recently discovered catalytic effect due to parts-per-million (ppm) impurities in an etchant on the etch rate of a solid. In the case of the ethylene diamine–pyrocatechol–water etchant, for example, it was found that only several ppm of pyrazine added to the solution could result in a doubling of etch rate. It is not inconceivable that minute traces of catalysts in the ambient atmosphere surrounding an ultra-thin-film interconnection could enhance or retard its susceptibility to electromigration.

6. Insulators

It is difficult to discuss microfabrication efforts without discussing insulator systems. Certainly, as with many moves toward microminiaturization, the semiconductor industry has provided the impetus for scientific and technological activity. We have spoken of certain properties of insulators used in semiconductor applications, those associated with charge trapping and interface states. We have only alluded to the effects of processing on such properties. We have not yet considered the effect of the temperature and pressure of processing on the structure as a whole. As devices shrink in size and active device regions become smaller, it becomes mandatory that lower temperatures of fabrication be developed for each process stage, since many such stages are employed serially during the process of fabrication, each of which is capable of degrading the desired attributes of the final structure. Among the most perturbing of these process stages is that involving formation of the insulators. Further, the properties of the insulator may represent the most critical design aspect of a semiconductor device. They may have to survive the highest applied fields, be tolerant of the smallest number of defects, and have to withstand the largest number of serial process steps, for example, the gate insulator in a MOSFET. We cannot think of the insulator as an isolated entity but must think of it as part of a materials system, and this materials system cannot be divorced from its method of preparation or its precise geometrical–topographical configuration. As such systems become smaller, their long-term reliability becomes a paramount concern and must be maintained, the difficulty of controlling their thinness tolerances increases, and the difficulty of reducing their trap density to counteract the increasing tendency for hot-electron injection to occur increases. In addition, it is known that oxides grown under high pressure are denser and have higher breakdown strength, but the causes are not well known.

The growth of research in integrated optics has created additional demands for well-characterized insulators of high quality. A number of the inventions in integrated optics deal with methods that restructure bulk optical systems into thin-film structures. Ultimately we can expect to produce integrated circuits consisting of electronic and optical devices on the same substrate. Indeed, microfabrication and epitaxial technologies are the foundations of both microelectronics and integrated optics. Thus, it will be necessary to develop surface features on optical materials that are of dimensions comparable with those on semiconductor materials, for example, edge definitions of about 500 Å are required to limit losses from optical scattering. Control of the index of refraction on a submicrometer scale will be essential; this requires a knowledge of the role that impurities play in the optical properties of insulators. Although pattern-generation techniques are adequate at this early stage, the choice of materials is still under intense investigation. The introduction of dopants to control optical properties has been achieved by ion implantation; however, this broadens the scope of the materials problems to include radiation damage, as well as the interaction of radiation damage and impurities. For example, it has been found that implantation of ZnTe to a depth of 1 μm influences its refractive index to a depth of about 7 μm, but the reasons are not well understood.

Many of the research problems stimulated by the efforts to develop integrated optical devices overlap those generated by the microelectronics industry. Opportunities for study exist in a number of fundamental areas, a few of which are as follows:

(a) Investigation of the relationship of processing to defect formation, and reducing the latter by postprocessing treatments and/or developing techniques for forming trap-free and defect-free oxides.

(b) Determination of the nature, both physical and chemical, and the size extent of defects and traps and annealing mechanisms, the behavior of surface and interface traps, and the phenomenon of dielectric breakdown, especially as it relates to defect states.

(c) Studying the properties of ultrathin oxides, the effects of impurities on oxidation rates, the effects of competitive reactions on oxidation rates, and the properties of the resulting insulators, for example, the competitive $Si + SiO_2 \rightleftharpoons 2SiO$ reaction, while much has been done on Si, little information exists on the compound semiconductors.

(d) Development of new processes for formation of insulator systems, for example, plasma oxidation and high-pressure oxidation and characterization of the growth kinetics and interface properties of the resultant oxides.

(e) Development of techniques for low-loss coupling of optical microelements, for example, optical fibers to thin-film waveguides.

(f) Study of new insulator systems for use in systems other than Si, in multilayer electronic devices, and in integrated optical devices.

7. *Contacts*

In a discussion of contacts, i.e., contact systems, one must consider the mode of fabrication of the contact windows as a key part of the contacting process. Simply fabricating the contact is inadequate, and one must be able to characterize its initial behavior as well as its long-term stability. In integrated circuit design, contact window size, to a considerable extent due to the tolerances, is a primary limitation on the level of integration achievable. For example, when the term "1-μm ground rules" is specified in integrated circuit design, it is generally meant that the smallest dimension used in lithographic resist exposure is 1 μm, and frequently this minimum exposure feature is applied quite selectively. The vast majority of exposure features may be 1.5 to 2 times the minimum size, and, generally, the minimum exposure feature refers to contact hole openings. In random-access-memory (RAM) design, a 1-μm minimum exposure feature enables packing of 256K bits of one device cell memory, and 0.2-μm ground rules imply more than 10^6 bits of memory, both in an area of 1 cm^2. We have mentioned tolerances; specification of minimum exposure feature without specification of tolerances is meaningless. Further, when one scales a minimum exposure feature, one must at the same time scale tolerances. To complicate matters further, to achieve usable yields, a simple statement of a minimum feature size and a root-mean-square deviation, e.g., a 1-sigma tolerance, is inadequate, particularly as dimensions decrease. A more meaningful tolerance is the 3-sigma value. At the 1-μm ground-rule level, to achieve adequate yields, a 3-sigma tolerance of ± 0.2–0.3 μm is required, and at the 0.5-μm ground-rule level this 3-sigma value scales to ± 0.1–0.15 μm, a rather formidable goal. At ground-rule dimensions greater than 2–3 μm, isotropic wet chemical etching of contact windows provides adequate tolerance and ground-rules control. At smaller dimensions, wet chemical etchant procedures are inadequate and dry (plasma) etching techniques are mandatory, for especially in reactive ion etching approaches, a high degree of vertical to horizontal anisotropy is attainable. Such anisotropy, which permits tighter ground rules to be applied, has a problem in that step coverage of contact openings becomes more difficult. Contact resistance problems also become more difficult, and perimeter defect structures in the contacts will become a problem in contact systems. Further increasing the difficulty in semiconductor technology, for example, where aluminum is a primary contacting and interconnection metallization medium, dissolution of the underlying silicon poses a problem because of the tendency of the silicon to saturate the aluminum. This problem of silicon "pumping" is aggravated at small contact-hole dimensions. Moreover, temperature cycling can result in Al contamination of the underlying Si. Silicide barriers are employed extensively to reduce contact resistances and act as a contact dissolution barrier, but at very small dimensions their utility is marginal. Furthermore, the kinetics of silicide formation and intermediate compound formation are not well understood. While the interface between Si and the silicides is generally less than 0.01 μm, it can become more significant as device size is reduced. However, it may be that this interface dominates the contact resistivity. Many contacts depend on tunneling through thin barriers. The dynamics of tunneling on the time scale appropriate for small devices is not understood. Improved theories for contact/tunneling behavior are required for small structures.

Although this discussion has been based on the needs of silicon chip microelectronics technology, new substrates such as GaAs and InP are being developed. Compatible contact materials will be required for the fabrication of non-silicon devices from these compound semiconductors. All the problems associated with Al metallization of Si will have to be addressed for these new materials systems.

Specific problems requiring attention include the following:

(a) Quantification of the exact limitations of Al–Si alloy systems in small-contact, shallow-junction applications.

(b) Study of the effect of stresses on aluminum penetration through silicides or into silicon directly.

(c) Study of the fundamental properties of interfaces, e.g., transport properties, growth kinetics, chemical composition, and interface states, interface resistivity, the effect of ambient atmosphere treatments on these properties, and the specific properties of the equilibrium metallurgical system apart from the interface.

(d) Study of new contact metallurgies, which must be

examined in the context of providing ohmic contacts, preferably with barrier-layer properties to enable contacts to be made to shallow junctions in Si and other semiconductors.

(e) Study of the effect of defects on contact behavior.

(f) Development of high-temperature contact metallurgies.

Such studies, to provide the basis for work in other fields, must be coupled with methods for forming contact openings, depositing contact metallurgies, and patterning these. Related questions such as electromigration phenomena in contacts, as discussed in the section on electromigration, must also be addressed. It is critical that contact interface phenomena be studied in the context of the precise materials system involved, as well as the configurations and dimensions in which they will be functioning.

8. Defect Removal and Laser Annealing

We have discussed defect phenomena, primarily in the context of insulators, and even more specifically in the context of the insulators in MOSFET's. Again, the impetus for discussing a new approach to defect removal has its origins in silicon-based technology, and we consider now the bulk material, silicon, rather than the various other device parts. Damage to the silicon substrate can occur in many ways during processing. Adjacent layers of SiO_2, because of lattice mismatch and temperature inhomogeneities, can cause slip to occur; the oxidation process can generate oxidation-induced stacking faults, as can growth of epitaxial layers. Ion-implantation processes can cause severe disruption of the crystalline lattice. Damage reduces device yield, results frequently in intolerably high bulk and/or junction leakage, and may affect long-term reliability. Thermal annealing is of marginal utility for removing the bulk damage in processed or partially processed device systems because of the high temperatures needed, although it is useful for defect removal in insulators. Two techniques for eliminating or masking bulk defects involve defect "gettering," whereby a damage layer is introduced on the back of a silicon wafer prior to processing; this damaged layer acts as a sink for mobile contaminants and mobile defects. For example, leakage in wafers gettered by backside argon-ion implantation is extremely low, as is the formation of oxidation-induced stacking faults. This approach is widely used in the semiconductor industry. However, thermal annealing is known to leave residual microstructure in the material. The nature and extent of these microstructures are not well characterized.

Another technique, which has other possibilities than damage removal, has been considered recently. This is laser annealing, which involves illumination of the surface of a semiconductor with an intense, heavily absorbed micro-laser beam. This exposure is believed to raise the temperature sufficiently for either solid-state diffusion or localized melting to occur, without raising the temperature of adjacent regions significantly, although the details of the kinetics processes are still not well understood and are controversial. During this treatment, defects are believed to be annealed. The implications, if they can be realized, are enormous. Process-induced defects can be postprocess annealed; the annealing can be carried out in air because of the rapidity with which it can be effected and one can visualize the "writing" of regions of localized electrical activity, i.e., to form active device regions. Because the process is so rapid, one can incorporate metastably large amounts of desired impurities in active regions or otherwise modify dopant profiles.

For the potential of this technique to be fully exploited much remains to be done. Required studies include the following:

(a) Development of techniques for control of laser pulse size (energy) and spatial homogeneity and development of tunable lasers in the 1–4 eV range.

(b) Investigation of the photon interactions in ion-implanted materials subjected to intense radiation, and the thermal properties of such materials near their melting points, e.g., the variation of conductivity with temperature.

(c) Investigation of the diffusion coefficients of dopants dimensionally constrained in liquids.

(d) Investigation of segregation coefficients in high-velocity recrystallization processes.

(e) Study of heteroepitaxial growth processes using laser melting techniques, e.g., silicon on sapphire, and the potential for removing defects in such layers, which limit the quality of devices.

(f) Investigation of defects and microstructure remaining after annealing.

9. The Formation of Thin Films

There are a variety of techniques available for the formation of single-crystal and polycrystalline thin films. These include chemical-vapor-deposition techniques, physical techniques (sputtering, evaporation, ion plating, and variants of these such as molecular-beam approaches), plasma-assisted decomposition, electroplating, liquid-phase epitaxial techniques, and, recently, solid-phase epitaxial techniques. The silicon industry is built around the formation via oxidation of the silicon–silicon dioxide system and utilizes the other methods of film formation to varying degrees. Although the literature dealing with film-forming techniques is huge, there are currently few films that can be deposited, in a practical way, epitaxially from the vapor, and these are restricted to a few semiconductors and magnetic garnet materials. We have considerable difficulty in modulating the grain size of even such common polycrystalline films as aluminum, and the measurement and control of interfacial properties have been accomplished nominally in only a few materials systems. Selective area deposition of films has been successful in only a few instances, and often there is incompatibility between temperature of deposition, temperature at which the underlying structure becomes disturbed, and the normal or desired properties of the interface, e.g., chemical homogeneity, sharpness, defect states, and intrinsic stress. Liquid-phase epitaxy is an interesting technique that has become useful only in the past decade,

but its range of utility is limited and it becomes difficult to control in ultra-thin-film (<0.05 μm) formation. Although chemical-vapor-deposition techniques can be applied more readily to the formation of very thin films, frequently the properties of such films, e.g., laser materials and bubble materials, do not possess the same properties that are obtained with liquid-phase epitaxial techniques. Further, the temperatures required are too high to maintain existing impurity profiles and to prevent autodoping of the epitaxially deposited films.

The requirements for research in film formation cannot be adequately defined in a few sentences, but a few generalizations can be attempted. These are

(a) Low-temperature techniques for film formation, e.g., plasma-assisted processes, must be studied in the context of obtaining films with characteristics normally associated with high-temperature film-formation processes.

(b) Techniques for grain-size control and enhancing adhesion in metal films must be developed in the context of specific materials systems in which they are to be used. Questions relating to their defect structure and doping must be included in such studies.

(c) Greater understanding is needed to explain and control differences between films grown from various epitaxial techniques.

(d) Greater understanding of the various epitaxial techniques themselves is needed, not only in the kinetics of film growth under nonequilibrium conditions but also in the interactions of constituent gases with containment vessels, which may result in contamination of the grown layer.

(e) Greater understanding of the interface between layers is needed, particularly in the compound semiconductors, where the high temperature of processing can create interfacial defects.

10. Microstructure Formation

Plasma patterning processes represent one technique for microstructure formation, but at present this technique is useful primarily as a technique for patterning of thin films and not for patterning of the bulk. Bulk in our definition can mean thicknesses as little as a millimeter, but thin-film thicknesses are in the range of fractions of a micrometer up to 1 or 2 μm. As yet, electronic microminiaturization is primarily a two-dimensional approach to a three-dimensional world. Recently, attempts have been made to move into the realm of three dimensionality, e.g., vertical FET's (vertical-metal-oxide-semiconductor, or VMOS) arrays of ink-jet nozzles, microrefrigerator systems, and arrays of deformographic storage elements for displays. These involve development of anisotropic solution etchants, when milling of bulk materials is involved, or plating of structures by electrochemical processes. This latter approach falls between thin-film and bulk-structure making.

We know best how to micromill silicon by chemical means as shown by the work on the fabrication of microrefrigerators. But even here the work is at an early stage, and means are needed not only to control the anisotropic etching of the semiconductor but to impart anisotropic thermal conduction properties to it. Alternatively, a material like pyrolytic boron nitride exhibits anisotropy in thermal conductivity, but we have no technology for etching it anisotropically. We know how to selectively etch n^+-type, n-type, and p-type silicon without etching p^+-type silicon or how to etch selectively n^+-type and p^+-type silicon without etching n- and p-type, but we cannot differentiate n- from p-type. We have no such control, crude as it might be, with other chemical systems, although the activity in inorganic resists suggests that there may be an extension of the concepts introduced there into the region of three dimensionality. Similarly, with sufficient study, the concept of selective area deposition might accord with the concept of selective area or anisotropic etching to provide a complete set of tools.

We have mentioned anisotropic etching as it relates in silicon to impurity-determined anisotropy. A second type of anisotropy, which has been applied not only to silicon but is usable with single-crystal sapphire, involves crystallographic anisotropy. Here, etch-rate anisotropy is determined by the difference in the kinetics of etching of different crystallographic planes, and it is not improbable that similar control of structure is possible in most single-crystal materials. What are needed to advance the state of microfabrication processes are the following:

(a) Study of the kinetics of etching of single-crystal materials in known etchants and evolution of new etchants.

(b) Development of etch masks to control the structure to be delineated, which involves the definition of suitable mask systems, study of their adhesion to the structure they are masking, and study of their resistance to the etchants.

(c) Exploration of novel anisotropic approaches, e.g., deep crystallization of glassy materials such as inorganic resist concepts, and development of techniques to achieve selective etching. Here the potential is huge, for one can envisage extremely high-aspect ratios resulting.

(d) Study of electrochemical techniques for building the third dimension, which might involve evolution of catalytic approaches.

(e) Exploration of selective-area deposition of thick and thin films, including the possibility of radiation-enhanced deposition at desired sites.

(f) Exploration of techniques of impurity incorporation in three-dimensional structures, e.g., focused ion beams.

11. Characterization of Microminiaturized Structures

Throughout this analysis of microminiaturization, characterization of the properties of the materials system being developed has arisen. The problem is magnified because the structures are physically small, the properties are often configuration-dependent and frequently are controlled by shielded interfaces, and finally our interest is often focused on nonequilibrium materials systems (composites) rather than on a single material. As tools we have electrical techniques that make use of the device as a probe. For oxides, for example, these include measurement of insulator traps,

their distribution and size, bulk-leakage phenomena, and internal photoemission techniques. However, these often identify a problem but do not define the cause or indicate a cure.

Here we must rely on old and new analytical techniques adapted for use at microdimensions. These techniques involve elucidation of chemical, structural, and topographic aspects of the microstructure in question and are impeded by noise problems when the probe used becomes very small. Consequently, we must evolve better sensing techniques and system component matching to enhance signal levels while not increasing noise levels. Frequently, the technique is destructive in nature. In medicine, where microanalysis is becoming more pervasive, considerable progress is being made in nondestructive three-dimensional analysis on living organisms, where both of these requirements are paramount. One might cite the use of advanced imaging systems or of computer-aided tomography (CAT) for the real-time imaging of buried structures. Such procedures should be developed for this field, permitting three-dimensional study of materials systems without destructive interference. Needs include the following:

(a) Evolution of technologies for analysis with enhanced sensitivity (enhanced signal/noise ratios) at smaller dimensions.

(b) Development of less expensive, perhaps specialized, tools to make their availability greater.

(c) Development of depth-imaging tools for examination of the interior of composites.

(d) Development of techniques for examination of interfaces.

We have attempted to draw some conclusions about some general needs in a number of the more pervasive science–technology areas that influence materials aspects of microstructure fabrication. Next, we will consider some of the major fields that require such materials system control and understanding. We have selected only five such fields. For the areas excluded, either the needs are not clear or the information involved is proprietary, e.g., Josephson technology and packaging of microelectronics.

In the above we have characterized only the technological aspects of the microminiaturized structures. It is expected that the device performance at these small scales depends strongly on the environment, such as other devices, boundaries, and oxides. New theoretical bases must be established to describe the operation of these microminiaturized structures, especially if such structures are to be utilized as probes of the materials themselves.

D. APPLICATIONS

I. Semiconductor Electronics

This field has provided the stimulus for miniaturization, LSI and VLSI, and is the one we understand best; therefore, it provides the most examples of needs. Although we understand much about this field and its needs, we hardly understand it at all. The variety of materials employed is wide, including different semiconductors and alloys, associated insulators, metals, impurities, and encapsulants. The only semiconductor material that has been extensively exploited to date for microminiaturization is silicon. Microminiaturization in semiconductor technology is at least partially cost driven, and this means that the materials and processes used must show a productivity advantage.

Concomitant with microminiaturization processes, two things occur: (1) the number of devices packed into a given area increases, nominally by the square of the decrease in device dimension; (2) the unit device performance increases more or less linearly. Microminiaturization involves shrinking of horizontal dimensions and a simultaneous shrinking of the vertical dimension, although for operational or practical reasons shrinkage in the third dimension may not be scaled with shrinkage in the horizontal direction. Thus, as thin films are made thinner, they may become less reliable, and as diffusions become shallower, they may also become more difficult to contact. Further, if a film interconnection, for example, is shrunk in width and thickness by a factor α, and the current is also decreased by α, the current density is increased by α. This can result in decreased electromigration, which, as discussed, is a current flux phenomenon. Also as mentioned earlier, surface electromigration may start to dominate. As semiconductor devices become smaller, they become less tolerant of elevated temperatures. Power dissipation is not necessarily a problem as device dimensions scale down, since current and voltage also scale. Thus, the density increases by α^2, the power/device decreases by α^2, and the chip power dissipation remains constant.

Base widths of bipolar devices are moving toward the 0.1-μm level and smaller, and, in double-diffusion processes, subsequent high-temperature processes would tend to disrupt profiles. In addition, as base widths become smaller, statistical fluctuations begin to dominate the thermodynamics of materials behavior. For example, little is known about the mobility in heavily doped semiconductors, and less is known when statistical behavior is "noisy," as in very thin base regions. As junctions, in general, become shallower, second-order effects make process modeling imprecise. For example, diffusions are enhanced during oxidations, and segregation between the diffused bulk and the growing oxide becomes important. In general, process modeling is difficult at larger dimensions, and highly imperfect at smaller dimensions (1 μm or less), because of the increasing and eventually dominating influence of interfaces, defects, etc. We may expect concepts based on bulk properties to lose validity and new ideas to be necessary.

Reliability of very small or very thin structures becomes more difficult to control, and for this reason, in both FET and bipolar technologies, much thinking has been given to the use of low temperatures to enhance reliability and/or performance.

The feasibility of low-temperature operation has been shown in MOSFET's and in germanium bipolars. However, the performance of silicon bipolars is degraded at tempera-

tures much below room temperature, perhaps because of carrier freezeout effects, or state quantization in the ultra-thin-base region. From a practical view, freezeout theory is not fully understood in heavily doped ($>10^{15}$ cm^{-3}) materials, and what is understood applies only to the more commonly employed dopants in relatively light concentrations. Much of the problem is tied to the lack of detailed understanding of localization and impurity-bonding and multiple-scattering effects.

A seemingly less important aspect of VLSI is chip attachment techniques in packages. At present, these are two dimensional, e.g., around the periphery. However, as chips become more densely populated, power distribution problems become more difficult because of resistance-induced voltage drops and transient, inductance-induced voltage excursions. These voltage excursions arise because of the rapid change of current levels as a function of time in higher-performance devices and the translation of these into voltage transients when acted on by ever-present inductances. On the other hand, parasitic and interconnection capacitances cause a delay in performance on packaged structures. If we assumed, as a rule of thumb, that inductance–capacitance products are constant, these two effects oppose each other. Thus, we would like small capacitances to reduce RC time constants and high capacitances to reduce inductive ($L di/dt$) voltage noise effects.

The net result is that to realize fully the potential of VLSI, much additional thought must be given to the packaging of semiconductor chips, namely, design and materials considerations must be treated together rather than separately. A systems approach to materials engineering may be essential. Packaging materials problems have not been addressed in a sophisticated manner, for the package must be evolved specifically for what it will package. However, certain general concerns can be identified, notably problems associated with power dissipation, particularly in bipolar technology, power-distribution techniques, reduction of inductance-induced voltage excursions at interfaces, and reduction of capacitance-induced, time-of-flight delays, all of which are largely materials-related questions. Further, as VLSI becomes more sophisticated, techniques for interconnection pattern fabrication will have to keep pace, which may preclude the use of sintered ceramics as a substrate material, since their surface topography may be incompatible with fine-line patterning of thin films. Finally, the problem of α-particle emissions must be attacked at either the package or chip level, probably through a materials solution, e.g., overcoating with α-particle absorbers or elimination of radioactive contaminants from the ceramic.

These comments represent a cursory overview and an attempt to provide some sense of the directions that must be taken. To define more specific needs, let us focus on the materials aspects of VLSI as these apply generally to MOSFET's and minority carrier devices as typified by bipolar transistors. The starting point is the substrate semiconductor materials that must be obtained by slicing wafers from a bulk ingot. Alternatively, the substrate might be obtained by cutting up a long ribbon of silicon formed by some capillary shaping technique; however, this is not yet a practical alternative, although much improvement has been realized in the quality of bulk material, and it represents perhaps the least of the problems today. As microminiaturization progresses, the substrate material probably will have to be improved in terms of its freedom from defects, its uniformity of doping, the presence of occlusions, the control of oxygen and carbon contamination, and the degree of gross and microscopic planarity of its surfaces. In addition, for further cost reduction, an increase in wafer diameter to 12 cm or more might be needed. Control of the materials parameters will require not only advanced studies of crystal-growth processes, wafer slicing, and wafer surface preparation but must include development of rapid techniques for measuring the bulk properties of the substrates. A specific problem requiring study is the effect of surface preparation on properties of interfaces grown upon substrates and elucidation of the nature of such differences, especially as they affect the growth kinetics and defects of grown overlayers.

From the substrate up, the processes used to build microminiaturized composite structures above the substrate surface and/or to construct structures beneath the surface will require some or all the following:

(a) Investigation of the effects of wafer-preparation techniques on finished device properties.

(b) Lower-temperature processing.

(c) Improved control of tolerances, both geometric and chemical.

(d) Study of parameters that affect and control polycrystalline film grain size.

(e) Study of contact metallurgies, and the effect of different metallurgical processes on the control of contact parameters.

(f) Control of lithographic resist properties, e.g., sensitivity.

Lower temperatures are required for a variety of reasons. These include minimization of thermally induced defect structures, such as slip dislocations. Aside from the deleterious electrical aspects of defect formation on the initial characteristics of devices, long-term reliability must be considered. Defects such as oxidation-induced stacking faults (OSF's) might not form in low-temperature processes. Other processes, such as those involving ion implantation, start out as low-temperature processes but require high-temperature postprocess treatment to remove crystallographic damage introduced by the low-temperature process and to make the species electrically active. Since ion implantation is a critical part of advanced semiconductor fabrication, a key area of study is low-temperature techniques for removing such damage, and, in the process, activating the implanted species. These techniques might include high-pressure annealing or the development of refractory high-conductivity metallurgies. A quasi-approach has been discussed in the section on laser annealing; as pointed out, laser pulse techniques have the potential for localized heating. Another possible approach involves temperature biasing of the substrate during implantation, a technique that has not been examined in any depth but has been shown to

be important for nucleating the growth of the damaged area. These might represent practically useful approaches to addressing low-temperature processes for impurity incorporation and damage removal. Clearly, study is required. Other areas relating to low-temperature processes that require study include oxidation processes, such as plasma-enhanced, pressure-enhanced, and possibly catalytically enhanced annealing processes for insulators and interfaces, and film deposition processes.

The many interfaces and materials present in semiconductor structures cannot be considered here, nor can the many unknowns relating to the construction of devices. What is clear is that the number of steps is so large, and the turnaround time for a complete experiment so long, that much greater emphasis will have to be placed on process simulation (modeling). With the dearth of hard data, such simulations will initially have to be piecemeal, and the major component parts will have to be combined to provide a total picture; and refinement will follow as data become available. This task is difficult; we are at the stage where, without intensive activity, the time lag between conception and implementation will increase.

II. Magnetic Bubbles

Micromagnetic devices are synonymous with bubble devices. These magnetic integrated circuit devices are most akin to charge-coupled devices (CCD's) in the semiconductor electronics field, and there is much similarity in chip layout and information handling. The use of cylindrical magnetic domains (bubbles) and CCD's is in delay line fashion; therefore, information access is serial rather than random, thus data access is slower. The motivation for bubbles and CCD's, as a consequence, is also heavily cost-driven. The shift-rate capability of bubbles relative to CCD's is much lower, e.g., kilohertz versus megahertz, but bubbles have a feature not possessed by CCD's, namely, involatility of stored information. In addition, bubble processes may be cheaper, although this is less clear. Packaging of bubble structures may be a significant cost disadvantage unless the scale of integration on the chip is extremely high so that the final packaged cost/bit accommodates the possibly more expensive package. Reliability of bubble structures is less quantified than semiconductor electronics, and, for example, electromigration may be a major problem, since employed current densities are large. On the plus side, the presence of fewer interfaces may increase reliability; and, from a process point of view, mass-production techniques based on x-ray lithography look much more attractive for bubble use than for semiconductor electronics, because the number of process mask levels is fewer.

From the purely materials point of view, the raw bubble substrate material is more complicated, more expensive, and less understood than silicon. Lithography and scaling alone cannot be used for microminiaturization, since associated materials inventions have yet to be made. Thus, in addition to many of the problems associated with the geometric scaling of semiconductor electronics, we must provide new materials systems for each scaling stage. Whether process simplicity, if it is real, outweighs the more difficult materials tasks is not known. Thus, this infant, promising technology will find extensive use if its potential for low cost, coupled with its limited performance, provides a significant cost-performance advantage over semiconductors. As with semiconductors, higher levels of integration tend to reduce speed, but unlike semiconductors bubbles can ill afford speed degradation. Unlike semiconductor electronics, as bubble size decreases, required drive fields necessary to avoid performance degradation and associated problems in heat dissipation do not scale.

To enhance the attractiveness of bubble technology, research is needed on the following:

(a) Device forms that do not require proportionately large drive fields.

(b) Chip organizations that yield shorter access times.

(c) Methods for increasing domain motion to speeds >10 m/sec.

A number of techniques offer some potential for increasing the level of VLSI in bubble technology. These involve lithographic reduction of the propagating permalloy structures and/or configuring them differently, overall structure scaling, and invoking the concept of bubble lattices in which bubble devices completely populate close-packed arrays. The latter technique no longer requires drive rails at the same spacing as the bubble arrays. Bubble lattices for a given lithographic minimum dimension can increase circuit density by 4 to 16 times. Since bubble–bubble magnetic interactions assist external drive fields, lower drive fields result. Another technique for forming "gapless" bubble arrays utilizes the contiguous disk (CD), in which guide rails are replaced by ion-implanted confining regions.

Much work has to be done to achieve the potentials offered in these concepts including:

(d) Development of new bubble materials systems that can support small bubbles (<0.4 μm) at low drive fields, which may include more complex double- and triple-layer systems, amorphous bubble systems, and surface-modified structures in which bulk and surface properties are intentionally made different.

(e) Study of metallurgical resistance to electromigration at high current densities.

(f) Study of new ways to manipulate domain structures without direct access to each bit position.

(g) Study of the mechanisms that induce and control magnetic anisotropy.

(h) Study of methods for depositing and/or forming films can sustain bubble structures.

III. Integrated Optics

Integrated optics involves application of thin-film technology to the fabrication of microminiaturized optical devices, including lasers, modulators, switches, detectors, prisms,

lenses, polarizers, and directional couplers, and attempts to integrate a large number of such devices on a single substrate. Signal propagation is by optical waveguides. The objective of much of the work in this area has been to scale down structural size and "shape" thin films to provide the same functions as their thick-film analogs. This has drawn attention to the materials and materials-scaling aspects as surface-to-volume ratios become large. Basic materials used are $LiNbO_3$, III-V alloys, and various insulating and conducting films. The techniques of semiconductor electronics find extensive application, e.g., fine-line lithography, controlled etching, and film deposition. A host of other materials not normally employed in semiconductor electronics are also used, including sputtered glasses, organic polymers, amorphous Ta_2O_5, ZnO, ZnS, CdSe, CdS, Nb_2O_3, and TiO_2, and rare earth garnets. In general, the materials problems of integrated optics are the same as for semiconductor electronics and magnetic bubbles, but the problems of integrated optics are more serious because of the myriad materials systems and interfaces involved. Consequently, the needs of semiconductor electronics and magnetic bubbles, modified by the applications and materials needs of integrated optics are fully applicable.

IV. Implantable Medical Electronic Devices

Aside from the technical aspects of the design and fabrication of implantable microelectronic circuits, for which the material problems are basically the same as in nonimplanted applications, there are unique materials aspects for implant applications centering around interconnections and passivation. The fluid environment in the body is quite hostile, and passivation of the most commonly implanted device is at the expense of an increase in size of the device, e.g., hermetically sealed cans, massive polymeric shields. Biotelemetric devices that monitor physiological parameters are also containable through these brute-force passivation methods. In both instances, however, although the electronics are enclosed, transducers are, of necessity, in contact with the hostile environment, which limits their longevity.

As we become more aggressive in the use of implantable microelectronics, brute-force methods become insufficient. For example, when multipoint contact with the nervous system is intended, for either multielectrode stimulation or multielectrode sensing, bulk space may not be available and electrode size must be greatly reduced to match the neural grid with which it is to communicate. The latter may require an electrode periodicity in the fractional micrometer range, which, in turn, requires the application of state-of-the-art sophisticated lithographic techniques. Unfortunately, the normal metallurgies available for conventional semiconductor electronics applications are either corrodable or both corrodable and toxic. Available insulation techniques are at best marginal and do not generally possess the degree of flexibility required. Perhaps conducting polymers of the type discussed in Section B.4 would offer an approach to meeting these needs. In any event, little work has been or is being done. In the semiconductor industry, the market does not appear large enough to warrant significant expenditure of research and development dollars, which places the burden on federal willingness to support such activities.

Needed are the following:

(a) Studies of biocompatible microinsulation techniques.

(b) Studies of biocompatible micrometallurgical techniques.

(c) Studies of interfacing and interconnecting in hostile environments, and passivation of the overall structures on a microscale.

(d) Development of microelectrode array fabrication techniques in the context of items (a)-(c) above.

V. Displays

Displays are usually life size, and questions of microminiaturization seem out of place. A little reflection shows that while the display as a whole is often life size, its individual parts may require microminiaturization techniques, sometimes to a level beyond the state of the art. For example, matrix-addressed displays such as the ac gas-discharge panel require fixed-position arrays of electrodes. To achieve high-quality image resolution (where image may mean coded and noncoded information being displayed), such electrode arrays may have to be made at densities of 80/cm or more (> 200 lines/inch). In a 30 cm × 30 cm display (12 in. × 12 in.), the length of electrode "wire" at such packing densities, all of which must be electrically continuous, is prodigious, and no such *tour de force* has yet been achieved. A third of this line density in a third of the area mentioned is about the state of manufacturing art. A somewhat parallel case exists in light-emitting diode (LED) or laser room-temperature-array technology, where the fabrication of reproducible, long-lived structures has not yet been achieved. In the instances of both high-resolution electrode and light-emitting arrays, yield problems are so great that costs are unacceptable. In the second of these, power dissipation and removal are also serious problems.

One general type of display does involve microminiaturization of the entire active part of the display and projection of the display to provide readability. A specific implementation of such a projection display is the deformographic storage display tube (DSDT). In principle, the device consists of a matrix of deformable microminiaturized picture elements (pels). This matrix may be as large as 1000 × 1000 or more, with each element consisting of a thin deformable membrane (50-100 nm thick) supported on a post. Reflection optics is used to project and display the "deformation" image of the written microdisplay. The problem here is akin to the fabrication of electrodes, and to date a reliable cost-competitive structure has not been achieved.

Many of the techniques of semiconductor electronics are applicable to the microminiaturization of life-size or projection displays, e.g., film formation, lithography, diffusion, patterning, and semiconductor processing, but the problems

are often unique in that different materials are needed and dimensions on which such techniques are employed may be very large.

Needed are the following:

(a) Studies of array fabrication of LED's and lasers at densities of 40 or more/cm.

(b) Studies of mixed-array fabrication to provide multicolor capability.

(c) Studies of novel array electrode fabrication techniques for use in electroluminescent and discharge-type displays.

(d) Studies of fast-switching liquid crystal and electrochromic materials for displays.

(e) Studies of techniques for fabricating arrays of deformable elements or elements optically different from the surroundings for use with reflection optics (projection displays).

(f) Studies of techniques for fabricating arrays of electrodes over large areas.

4
Pattern Generation and Transfer

A. INTRODUCTION AND GENERAL CONCLUSIONS

Pattern generation and transfer for microfabrication can be accomplished directly using scanning-charged-particle beams or by using masks to delineate the pattern exposed by radiation (such as visible, ultraviolet, or x-ray photons, electrons, or ions). The masks can be in contact with, in close proximity to, or imaged on the surface to be exposed. Much fabrication of electronic structures requires that patterns be accurately registered with previous structure on the substrate. As fabrication area increases and device feature size decreases, the relative distortion between the mask and previously fabricated structures on the substrate becomes increasingly important. This relative distortion determines how large an area can be exposed on a substrate before unacceptable loss of registration occurs. Fundamental measurements of substrate distortion as a function of processing steps, and of mask distortion as a function of exposure dosage, are needed to determine the optimum area for high-yield pattern transfer using masks. The results of these measurements are likely to determine which of several potential strategies will be adopted for pattern exposure on future generations of complex very-large-scale-integration (VLSI) circuits, a multibillion dollar, high-technology field in which the United States at present holds a lead. The strategy adopted will determine what high-throughput equipment will be needed by commercial manufacturers of VLSI circuits and, accordingly, will encourage the timely development of such equipment, be it higher-resolution, step-and-repeat optical projection equipment, x-ray equipment, computer-controlled, serial-exposure, electron-beam equipment, or some other alternative. The metrology measurements needed today for commercial production equipment are at the 0.1–0.5 μm level, but as different types of devices are designed and produced, even higher precision may well be needed—possibly even an order of magnitude higher.

The fundamentals of pattern resolution, distortion, registration, and accuracy are important in both research and commercial production. The parameters of speed, throughput, and cost are critical in commercial production. At present, not enough information exists to choose with certainty which method of pattern transfer will be best at 1 μm and smaller dimensions for commercial production of integrated circuits and other electronic devices. Optical systems, which currently are preferred for production, have a distinct cost advantage and have demonstrated adequate resolution on flat substrates for 1-μm linewidths. Depth of field for optical projection cameras is small ($\sim$2 μm), however, which may restrict their usefulness in manufacturing processes. Full-complexity large-scale-integration (LSI) devices with minimum dimensions close to 1 μm must be fabricated for the importance of this problem to be fully understood. Fundamental studies of the effect of partial coherence on image contrast will also help to determine the limits of optical projection for image transfer.

Scanning-electron-beam systems have been used to fabricate full-complexity LSI devices at 1-μm dimensions, but at present such systems are not fast enough to be economically viable, except for specialized applications where customization is important. Mask making is such an application. Methods and equipment for improving throughput and reducing cost are being studied in several industrial laboratories. These improvements are expected to come from

new electron-optical concepts, from increases in control-system speed, and from computer architectural changes that will allow overhead functions, such as mechanical sample stepping and registration, to be carried out during beam writing.

In the next few years it is likely that hybrid approaches, employing both electron-beam and optical projection, will be used. A clearer understanding of the resolution limits of optical lithography and the throughput/cost limitations of scanning-electron-beam systems is essential if optimum combinations are to be developed for given applications.

X-ray lithography holds substantial promise as a simple parallel replication method for very-high-resolution patterns. The major uncertainties at this time are mask-to-substrate distortion (mask distortion with use and substrate distortion with processing) and sufficient source intensity for rapid and economical exposure. Work to resolve these uncertainties is critically important, for a mistake in the choice of lithographic strategies could have major economic consequences.

Recent developments in high-intensity sources for submicrometer ion beams have increased the speed of direct ion-beam machining and resist exposure by several orders of magnitude. Methods that previously were impractically slow have suddenly become potentially important. Consequently, fundamental understanding of ion-beam interactions with resists; high-resolution, direct ion-beam machining; direct-writing ion implantation at the micrometer and submicrometer scale; and substrate damage by ion beams should be improved substantially—and quickly.

Most methods of exposing patterns rely on a resist. Each type of radiation has different characteristics; therefore, the resist resolution, contrast, and sensitivity can be optimized for the radiation to be used. Although some desirable resist parameters, such as adherence, are universal, others vary with the process chosen: wet chemical etching versus plasma etching versus directed ion-beam etching, and the like. New resists for specific new dry-processing technologies that avoid resist swelling, for example, thus offering higher resolution, should be developed. To do this effectively, a better understanding of present dry-etching methods, and possibly development of improved etching methods that are anisotropic, is needed for electronic and other microstructure fabrication.

Commercial production of current electronic devices requires a knowledge of lithographic patterning. Research and development of future electronic devices will require new knowledge about patterning of these devices. Yet little research or teaching of this subject is taking place in universities. The subject is both difficult and broad; it encompasses the interaction of finely focused radiation with matter; the dynamics of resist development; chemical etching of devices using liquids, gases, plasmas, and directed ion beams; patterned material deposition; diffusion; annealing; electrical properties of matter; oxidation; and other aspects. Physics, chemistry, materials science, and electrical engineering all enter in; when design of devices is included, more engineering and computer science must be included.

The successful university teaching of such a broad subject runs counter to the trend toward increasing specialization. Yet such teaching and research are increasingly important if graduates are to have the background that a technology-oriented society requires. One significant result of increased funding for universities in microlithography should be interdisciplinary activities within a university, as well as increased interaction between universities and industry, where, by economic necessity, more broadly based research and development take place. Certain topics deserve greater emphasis in U.S. universities; these include electron and ion optics, the interaction of radiation with matter (including transverse effects related to edge definition), and the applications of physics and chemistry to microstructure formation on solid and thin substrates.

B. BASIC RESEARCH NEEDS IN PATTERN WRITING AND REPLICATION

Instrumentation

Pattern-writing instruments of modest cost ($100,000–200,000) are needed for experiments on resist sensitivity and resolution, small-structure research, small-device fabrication, radiation effects on devices, and other fields. These might be university-modified scanning electron microscopes or industry-furnished instruments.

High-throughput, automatic-alignment exposure systems should be developed for VLSI production at feature sizes of the order of 1 μm. This expensive equipment will be needed to keep integrated-circuit production in the United States fully competitive worldwide. Variable-aperture or patterned-aperture electron-beam equipment, or high-throughput x-ray exposure equipment, seem the best candidates, but research in both is necessary (see Sections C and D). Proprietary industrial prototypes (e.g., IBM EL1) exist, but details of design and performance limitations are not available to the industry that would build such equipment for semiconductor companies. The development of such equipment is, in short, a matter of serious concern for industry.

Additional sources of soft x rays are needed. These range from less costly synchrotron sources for production to tabletop sources for laboratory experimentation.

Ion-beam sources for microfabrication writing are needed in more laboratories to explore resist exposure, resolution, sensitivity, direct milling of materials, implantation, damage, and the like.

Metrology standards and instrumentation will become increasingly important, especially for wafer distortion measurement and control. These measurements, as a function of processes used in fabrication, may determine the choice between electron, ion, x-ray, and ultraviolet lithography for the next generation of production. This effort will require inputs from the university, industrial, and government communities.

Microscopes capable of "seeing" patterns with greater than fabrication resolution must be available. For structures

down to about 500 Å, the scanning electron microscope (SEM) suffices; for structures <100 Å, a scanning transmission electron microscope (STEM) is probably needed, because these structures are likely to be made by directed STEM beams.

Resists

Polymer resists need to be improved in resolution, sensitivity, and contrast. Inorganic resists need to be developed and understood on a fundamental basis. There is also need for development, evaluation, and understanding of resists for dry processing.

Resistless Processing

Fundamental aspects of directed particle-beam-assisted etching, implantation, and the like should be studied to ascertain whether masking can be eliminated from the microfabrication procedures. This work is exploratory and highly fundamental.

C. ELECTRON-BEAM LITHOGRAPHY

Thin-film electronic devices, such as semiconductor integrated circuits and magnetic-bubble devices, are fabricated by a series of processes that use patterned resist layers to mask selected areas of the sample surface. Images are usually formed in the resist layers by ultraviolet (uv) exposure through a mask held in contact with or in close proximity to the resist surface. This contact printing process has two major drawbacks. First, diffraction effects between mask and wafer limit the minimum linewidths to 2–3 μm, and, second, damage can result from contact between the mask and wafer, which reduces the yield and reliability. Ultraviolet, x-ray, and electron-beam methods are being explored to overcome these two disadvantages. In this section we discuss scanning-electron-beam systems but not the resists and processes used in conjunction with the exposure tools, although in many cases they are of great importance in determining the overall resolution and speed of a given technique.

In scanning-electron-beam systems, the pattern is written with a small electron beam that is generally controlled (deflected and turned on and off) by a computer. It is the only method so far used successfully to make full-complexity silicon devices with a capability that exceeds conventional contact printing in terms of linewidth and overlay tolerance. Masks made by a scanning electron beam are also needed for replication methods, such as x-ray lithography and deep-uv conformal printing. The ability of scanning-electron-beam systems to generate patterns at very high speed can also be used to advantage in the fabrication of masks with dimensions above 1 μm. Such masks are replicated using uv reduction projection printing.

In cases where chips are written by pure electronic scanning, two basic methods have been employed: raster and vector scanning. With raster scanning, the beam scans the entire pattern area and is turned on where required. In vector writing, the beam is directed only to points where exposure is required. Vector scanning is more efficient, because no time is wasted scanning areas not requiring exposure, although it places more stringent requirements on the deflection system, such as dynamic accuracy and, in particular, eddy-current errors. Raster scanning makes it easier to apply corrections for deflection aberrations and pattern distortion. Vector scanning allows more efficient data compaction and is more suitable when proximity corrections have to be applied.

For electron-beam writing on full wafers, the beam cannot scan the whole sample. Thus electronic scanning has to be combined with mechanical movement to cover the sample, and methods must be provided to maintain the position of the beam accurately with respect to the wafer.

The throughput of scanning-electron-beam systems was originally limited by electron-optical performance, that is, by the beam current/resist sensitivity criterion. However, this situation has been significantly improved by the discovery of resists with greater sensitivity and by the following electron-optical advances:

1. Improved electron gun design and new cathode materials, in particular LaB_6, have resulted in increased intensity. Field-emission cathodes may yield a further increase for systems with beam currents below 10^{-7} Å, provided a method is found for reducing noise in the emitted current.
2. Computer-aided design of the final lens/deflection system unit has led to significant increases in field size.
3. Shaped-beam systems, which increase the number of pattern elements exposed by the beam at each beam position, have been developed.

Overall throughput for scanning-electron-beam systems is complex and, in addition to electron-optical performance and resist sensitivity, depends on the noise–bandwidth characteristics of the deflection system, digital-to-analog conversion rates, data-transfer rates, switching speeds for digital pattern-generation hardware, alignment time, mechanical movement of the sample, and time taken to load the samples into the vacuum. The relative importance of these different factors depends on the overall system configuration.

Electron-beam systems (e.g., based on scanning electron microscopes) can be configured as pattern-writing instruments of modest cost ($100,000–200,000) for experiments on resist sensitivity and resolution, small-structure research, small-device fabrication, radiation effects on devices, and the like. For mask making, scanning-electron-beam systems offer better resolution and low defect levels. Also, state-of-the-art systems offer shorter turnaround than conventional contact-printing techniques.

For direct device fabrication, scanning-electron-beam systems are not yet competitive in cost with contact printing or optical projection, but their performance in this respect is improving rapidly as a result of the introduction of advanced electron-optical design methods and concepts, higher-speed control electronics, and large reductions in the

cost of the digital processing electronics needed to supply pattern data and control the systems. The attainment of electron-beam systems with improved cost performance is significant for LSI manufacture, because direct electron-beam fabrication offers great opportunities for automation, in addition to its fundamental advantage of higher resolution. Such expensive equipment is needed to keep integrated-circuit production in the United States competitive worldwide.

D. X-RAY LITHOGRAPHY

X-ray lithography has a number of significant advantages. The chief ones are high resolution (linewidths from 100 Å to several micrometers) and simplicity (~$5000 for simple benchtop laboratory system). As a consequence, researchers can have access to patterning in the 100-Å to 1-μm range. X-ray lithography is, of course, a mask replication technique; therefore, it depends on electron-beam, holographic, and other means of mask generation. These means should be made available either through commercial or governmental sources.

As with any mask replication approach, multilevel alignment is required in some applications. Superposition precision of the order of 100 Å has been demonstrated but not yet implemented in a commercial system. Alignment systems should be developed.

The areas of patterns (or, more precisely, the number of resolution elements) that can be replicated and superimposed is constrained by mechanical distortion, either in the mask or in the substrate. It is highly unlikely that substrates or masks can be as stable as 1 part in 10^6. It is critically important to the strategy of microlithography that substrate and mask mechanical stability be carefully studied as a function of processing and lifetime. Simple moire overlayer methods may be suitable here. It is an open question whether distortion studies that relate to a specific process can be used to derive a general understanding of distortion and to work out guidelines that are independent of specific processes. We believe that there are fundamental materials-science issues here. In the commercially important applications to integrated semiconductor devices, substrate diameters are 10 cm. Superposition to 0.1 μm will almost certainly require step-and-repeat exposure.

For high-throughput production of multilevel devices, intense x-ray sources are required. Electron bombardment x-ray sources have an efficiency of only 10^{-4}. Rotating anode sources are commercially available at a power level of 10 kW, delivering about 1 W of soft x rays. The throughput of an x-ray system with such a source depends on many parameters (linewidth, wafer size, overlay accuracy); however, more efficient sources are desirable. High-temperature plasma sources can have conversion efficiencies of ~10 percent and might provide cheap benchtop sources in the future.

Synchrotron radiation sources, which will provide powerful, well-collimated beams of soft x rays for research, are now being built (at Stanford University, Brookhaven National Laboratory, University of Wisconsin, and Cornell University). The cost of these sources, however, is a severe limitation, especially for small industrial firms. It would be highly desirable to explore the feasibility of developing inexpensive (~$100,000) sources of soft x rays based on acceleration of relativistic electrons. Included in this category are storage rings, helical wigglers, crystal channeling, and other novel means.

E. MICROFOCUSED ION BEAMS

Microfocused ion beams can be used, in principle, to expose resist, machine materials, and alter the conductivity of semiconductors by implantation. All of these ends can be accomplished directly, without masks. The latter two uses are examples of resistless processing. Until recently, the limited intensity of ion-beam sources made these possibilities impractical. In 1972, examples of focused-beam processes, including implantation of lateral doping profiles and exposure of resist, were demonstrated with a low-current system. Recently, new focusing results have been obtained with a high-intensity liquid metal (LM) gallium-ion source that is imaged at unit magnification by a single-gap accelerating lens. With this system, ion-beam machining of gold and ion-beam exposure of resist have been demonstrated for linewidths down to 400 Å (= 40 nm).

Focused spot sizes and currents have been measured for the LM-gallium source operating at an extraction voltage of 6 kV. A total extracted current of 10 μA was obtained at a final beam energy of 55 keV. Spot sizes have been measured by scanning the focused beam with a postlens electrostatic deflector and either measuring the spot current risetime across an edge or machining (sputtering) a line pattern into a chosen target. For a beam half-angle of $\alpha_0 = 6$ mrad, a 0.5-μm-diameter spot at 1×10^{-9} to 3×10^{-9} A spot current has been demonstrated. At $\alpha_0 = 3$ mrad, lines ranging from 0.17- to 0.5-μm width have been machined in a film of 2000 Å Au on Al using a beam current of 7×10^{-10} A.

Also, with α_0 reduced to 1.2 mrad, and a beam current of 1.2×10^{-10} A, a series of lines has been machined in 400-Å-thick Au; the resulting linewidths were 1000 Å.

A series of lines in polymethyl methacrylate (PMMA) resist, ranging in width from 400 Å to 5000 Å, have been exposed by a focused 59-kV gallium-ion beam. The lines were generated by single passes of the beam at deflection speeds of 2.5 cm/sec to 8.0 cm/sec. The resist film was sufficiently thin, 600 Å, to allow complete penetration by the 59-kV gallium ions. Before the resist was applied, the silicon substrate was coated with 400 Å of gold for pattern transfer. After normal resist development, the gold film was rf-sputtered using the patterned PMMA resist as a mask. The widths of the resulting lines in the gold were then measured with a scanning electron microscope. The narrowest lines were obtained at higher deflection speeds (corresponding to about 7×10^{-7} C/cm^2). Intersecting lines were also exposed to evaluate proximity effects; reasonably sharp corners resulted without employing dose correction.

The high intensity and excellent stability of LM-gallium sources are highly encouraging for the future applications of focused ion beams. Finding liquid metal sources of dop-

ant ions for use in microcircuit fabrication will be the next big challenge. In view of the very small spot sizes obtained, the role of focused ion beams in diagnostics should also be reconsidered.

F. INORGANIC RESISTS AND PHOTOFORMABLE DOPANTS

Planar semiconductor fabrication began by utilizing the well-established organic polymer photoresist (OPPR) technology developed initially for the photolithography industry. Its success is well known to the solid-state electronics industry. To date this success has precluded the consideration of other alternatives to OPPR by industry on the grounds that OPPR could be modified to meet all requirements. As the complexity of materials and processes evolved, it became increasingly clear that the case for OPPR was overstated. If any significant reduction in process steps or utilization of new semiconductor material or processes is to be expected, a more innovative approach to device fabrication will be needed. Electron- and ion-beam processing and x-ray and synchrotron radiation sources are examples of new processing technologies that are resist-dependent. Organic materials tend to have low Z numbers and low stopping cross sections for electrons and x rays. Inorganic materials are far more flexible and are used extensively as additives in OPPR. Experiments on materials such as As–S and Ge–Se alloys and compounds have demonstrated a sensitivity to uv radiation that is within 2 orders of magnitude of conventional OPPR. Similar sensitivities have been observed in electron-beam writing on As_2S_3 both in the United States and in Japan. Work in both countries on Ag photodoping indicates that it is possible to improve the sensitivity of both the As–S and Ge–Se resists significantly. Furthermore, recent experiments indicate that As–S materials can be fully processed using plasma-etching techniques. The use of dry-processing techniques with these materials is attractive.

An alternative to forming a pattern in the inorganic material is to use materials like As_2S_3 as doping sources in a process technique that eliminates the oxidation-window-opening procedures required when OPPR is employed. Overcoating of the photoformed or electron-beam-formed structure by SiO_2 or Si_3N_4 and a subsequent drive-in could reduce the number of process steps for the initial n^+ diffusion in n-channel technology by a factor of 2. The resulting improvement in cost, turnaround time, and yield makes this approach potentially attractive.

Extended studies of inorganic amorphous layers are clearly indicated, for most of these show marked changes in their electrochemical properties after localized exposure to various forms of radiation.

G. RESISTLESS PROCESSING

Fundamental aspects of directed energy beams (e.g., electron, ion, and photon) for etching, implantation doping, annealing, selected-area condensation, and film growth (epitaxy) should be studied to ascertain whether masking can be eliminated from "normal" lithography and pattern-transfer processes that are used at present to make microelectronic devices and integrated circuits. In Section E the discussion on focused-ion-beam applications is one example of a potentially powerful technique for resistless processing (i.e., ion-beam sputtering and impurity doping).

Other techniques with rudimentary existence proofs include electron-beam-bombardment-enhanced etch rates of SiO_2, electron- and laser-beam annealing of ion-implanted and/or amorphous film overlaying single-crystal substrates, and electron-beam-induced condensation of films caused by local modification of the surface free energy.

Laser-beam and, more recently, electron-beam annealing, both in pulsed and cw scanning modes, have demonstrated unique surface modifications of ion-implanted and amorphous thin films. In some instances defect-free regrowth has been obtained and materials that lose stoichiometry at high temperatures have been annealed without loss of stoichiometry.

These and other beam-induced surface or near-surface effects offer tremendous opportunities for thin-film modification and patterning (i.e., etching/deposition)—all eventually without the aid of resist masking for local lateral dimensional control. However, these opportunities require considerable study and optimization to bring them into the future mainstream of microstructure fabrication. Elimination of resist materials from the processing procedure would eliminate many process-induced errors (yield losses), simplify the process, and make it more adaptable to automation and control.

H. METROLOGY FOR SUBMICROMETER STRUCTURES

Submicrometer structures are near or below the linewidth measurement and displacement measurement limits of conventional light microscopy. Because the tolerance of linewidth uncertainty scales directly with linewidth, new methods of linewidth and line-displacement measurements must be developed. The latter are crucial to the measurement of level-to-level registration in a multilevel lithography process.

The two approaches suggested here, scanning-electron-beam metrology and electrical test patterns, have already received preliminary investigation and implementation by industrial laboratories and the National Bureau of Standards. However, both methods require further development and characterization to provide the needed techniques and standards.

Scanning-electron-beam metrology utilizes scanning electron microscopy and precision laser interferometry for correlation of line-image profile signals from the electron detector with the fringe patterns from the laser interferometer. The correlation of this information with the material line edge requires a model of electron-beam interaction with the line edge. In general, this method is applicable only to lines with sloping edges that result from a structure with a base that is wider than its top. The line profiles in microstructures range from those with near-vertical edges to those that

are undercut. The undercut profile presents a situation in which normal viewing from the top is unlikely to reveal where the base of the structure contacts the substrate.

Electrical test patterns, with which pattern displacement from an underlying structure can be measured, are desirable and should be developed further. These techniques scale linearly with linewidth to dimensions as small as 0.1 μm and thus can be extended into the micrometer range.

Both methods are best implemented through close collaboration among the university, industrial, and government communities.

5

Devices, Integrated Circuits, and Integrated Systems Design

A. INTRODUCTION

Over the last two decades the complexity of individual integrated circuits has approximately doubled each year, as shown in Figure 5.1. Several factors have contributed to this increase, including increased die size, reduced device dimensions, and increased circuit cleverness. Based on Figure 5.1, it has been suggested that a slowing down of the drive of the last two decades toward very-large-scale integration (VLSI) could be expected because of the difficulty of achieving further significant increases in circuit design cleverness. However, the announcement by several suppliers of 64K random-access-memory (RAM) products in full manufacturing mode indicates that this is not necessarily so. Moreover, we appear to be entering a new era in microminiaturization employing more sophisticated technology than ever before, for example, direct-writing electron-beam exposure, total ion-implantation impurity incorporation, and high-aspect-ratio dry etching. The current trend of extrapolation of technology and design techniques can be expected to pose great technical challenges as we enter the VLSI era, and a thorough effort is essential to provide the scientific base necessary for this entry.

The motivation for moving toward VLSI is *not*, to the first order, simply improved performance, nor is it, *per se*, greater functionality or capability. Rather a combination of these factors and cost is the driving force and might most appropriately be expressed as a sort of performance-capability-to-cost ratio. The current device technology bases for application in VLSI are the metal-oxide-semiconductor field-effect transistor (MOSFET) or insulated-gate field-effect transistor (IGFET) in electronics and the magnetic domain (bubble) in magnetics. None of these technologies is intrinsically as fast as one based on bipolar devices; however, these technologies appear to be compatible with huge arrays of 10^5 to 10^6 memory bits and 10^4 or more logic gates, while the bipolar type does not. The key to VLSI is to achieve the cost objective, while, at the same time, preserving or even enhancing the potential for performance and capability inherent in an IGFET or magnetic-bubble circuit design. Of course, as the scale of integration increases, improvements in performance and capability are possible; as the individual devices are made smaller, interconnection lengths and, concomitantly, time-of-flight delays generally also become smaller. If we could integrate bipolar devices to the same scale as IGFET's or bubbles, *at about the same costs*, bipolar device technology might well be the preferred base for VLSI.

Although, in theory, VLSI leads to lower costs and greater performance capability, it also leads to a host of problems that must be confronted. Global custom design of integrated systems is perhaps the most formidable of these. But not far behind are the problems associated with power-supply distribution, testing, packaging, and fabrication. Thus, it is clear that new approaches are needed for integrated system design, approaches in which the overall problem is viewed as a continuum extending from materials-processing science through device physics to systems science. From the systems-science viewpoint, what is required is more effort devoted to improvements in the architecture

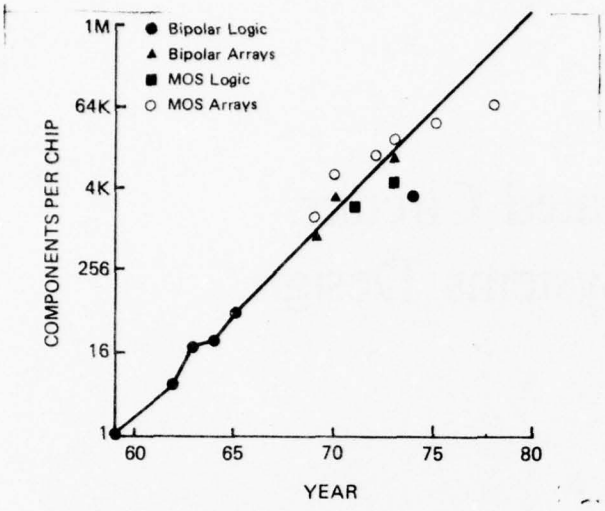

FIGURE 5.1 Approximate component count for complex integrated circuits versus year of introduction (MOS, metal-oxide semiconductor).

of circuitry, for example, macro-organization, to obtain the most effective use of silicon area at the maximum level of performance. Although knowledge of such basic processes as ion implantation, thermal oxidation, diffusion, and epitaxy is continually growing, it is limited, and the device implications and the technological applications of VLSI are so dramatic that the need for further research in these areas is paramount. We expect that the advent of complete process simulations and the coupling of process physics with device physics by means of powerful analytical tools will be key steps toward achievement of VLSI designs. Through automation of processing, the fluctuating human variable is being removed from the fabrication sequence. As concepts of design regularity (macrodesign) become paramount and process physics becomes better understood, more automated design should occur in VLSI technology.

Yet, as we approach the VLSI era we must also face the fact that the basic physics of small semiconductor devices is not well developed. As device dimensions continue to shrink, many problems existent in small-device physics must be faced. For example, MOS device models can readily be reduced via a scaling theory; however, this approach, which requires that the voltage, for example, scale as V/N when the channel length L is reduced to L/N, does not normally accommodate the required temperature scaling, which is imperative if, e.g., a dynamic RAM is to be symbiotic with static logic design to achieve greatest device density on a chip. Although there is current concern about "higher-order effects" modifying device behavior, it is reasonable to ask: When do these "higher-order effects" cease to be perturbative in nature and begin to alter severely or even dominate the operation of devices? The move toward VLSI and the recent demonstration of the use of photoresist to fabricate linewidths of 250 Å suggest that these problems must be addressed in the near future.

What then are the specific materials properties and defects that are germane to semiconductor devices? The university, industry, and government communities are currently engrossed with the technology of Si and certain compound semiconductors. Nevertheless, the understanding of process-related and process-induced defects is generally primitive, although these are usually the dominant defects. As a consequence, it is often most useful to use the semiconductor device as a probe of material properties and to study materials properties in configured states. In the study of materials science for VLSI, the opportunities to apply devices as probes of the material must be pursued. Principal barriers to this use of devices are often the lack of access by the materials scientist to device-fabrication facilities and lack of knowledge of the complexities of device technology. These barriers must be overcome, for if past history is a guide, materials progress will be most rapid with a synergetic approach. Without significant materials progress, entry into the VLSI era will be impeded significantly.

In Section B we present a brief summary of the research needs in semiconductor devices, circuits, and systems. Section C is a concise presentation of our conclusions. In the following three sections, we discuss the major aspects of integrated systems to facilitate study of the problems and the limitations of current understanding. These are taken in order: first, in Section D materials and processes, then in Section E devices and circuits, and then circuits and systems in Section F. Although these three aspects are treated separately, they are *not* really separable but are parts of a synergetic whole that must be treated *in toto* if VLSI is to achieve its fullest promise.

B. GENERAL SUMMARY OF NEEDS

1. Research in semiconductor devices and circuits

(a) It is imperative to develop nonlocal, transient analysis modeling approaches that take full account of the two- or three-dimensional nature of devices and temporal and spatial relaxation effects.

(b) The fundamental aspects of contacts, interconnections, and the reliability of small devices in an integrated systems environment must be investigated.

(c) Modeling of processes must be developed to enable the fabrication of logic and memory elements on a given wafer and to make possible the transformation of the "computer on a chip" concept into reality.

2. Research on circuits and systems

(a) Research in new system organizations and in design for these organizations is required to meld system, circuit, and device design.

(b) Research in macroarchitecture of systems designs that are amenable to VLSI must be pursued.

C. CONCLUSIONS

1. Additional facilities are needed for the fabrication of prototype devices and systems, especially within the university environment.

2. The collaboration of university and industrial laboratories to produce structures, devices, and systems for study that are close to industrial standards should be encouraged in every way possible.

3. A major funding program in microstructure research is needed.

4. A broader research program in the "speculative new science" aspects of the development and utilization of semiconductor devices and integrated systems is highly desirable.

The first three conclusions are obviously linked. Additional fabrication facilities are necessary to accommodate an increased number of researchers and a generally increased research effort in microstructure science, engineering, and technology. The few university-based research programs and the even fewer cooperative university–industry programs in this field are generally supported as fragmented portions of larger, more diversified programs. A major, intense push into the physics and technology of submicrometer devices requires a coordinated funding program. Such a program should be directed toward explicit study of the device physics on the submicrometer scale, as well as the modeling of system architecture and custom design of componentry, testability and testing of VLSI, power supply distribution, and wireability and packaging aspects to minimize voltage-transient phenomena associated with short risetimes.

The fourth conclusion results from the disappointing tendency of university research on semiconductor materials and devices and integrated systems to emulate industrial efforts, rather than to explore in new, high-risk directions.

D. MATERIALS AND PROCESSES

The materials most critical to future integrated systems are elemental and compound semiconductors. The most widely used material is silicon, which we shall briefly discuss from a device viewpoint. (An extensive discussion from a materials systems viewpoint is given in Chapter 3.) GaAs and other III–V semiconductors find use at present in light-emitting detecting and microwave devices and in high-speed logic and will be discussed next. We then consider two other classes of compounds that are important in the fabrication of cryogenic, focal-plane, infrared detecting arrays. Finally, we offer a broader picture of the tasks ahead.

Silicon

There are two major categories of silicon properties that affect device performances:

(a) Electrical properties
- Resistivity uniformity
- Net dopant concentration and degree of compensation
- Minority carrier lifetime
- Carrier mobility

(b) Physical properties
- Crystallographic microdefects and dislocations
- Point defects and clusters of point defects
- Deep-level centers and metal impurities
- Carbon and oxygen precipitates and clusters
- Epitaxial defects

In bipolar devices, crystallographic microdefects, diffusion pipes, inclusions, precipitates, clusters, deep-level traps, and the like cause the following device problems:

(a) Degraded *p-n* junction breakdown
(b) Microplasma and junction leakage
(c) Current channeling (changes in local electric field)
(d) Nonuniform heating (hot spots)
(e) Degraded transistor gain

Taken in combination, (a)–(e) introduce a limiting effect on the array size (or chip yield) that can be obtained.

In MOS devices, structural defects, stacking faults, dislocations, and microdefects act as generation–recombination centers and leakage current sources. Leakage currents affect the following MOS parameters:

(a) Refresh time in dynamic RAM
(b) Switching threshold voltage drift in static RAM's
(c) Dark current spikes in charge-coupled device (CCD) imagers and leakages in CCD memories
(d) Standby power in complimentary MOS's (CMOS's)
(e) Maximum operating temperature in static and dynamic RAM's

Czochralski silicon will continue to be employed throughout the semiconductor industry for VLSI in MOS, and possibly bipolar, production through the 1980's. However, Czochralski silicon slices will need to be tailored to the specific requirements of each device. At present, it is known that the oxygen in Czochralski silicon serves a complex but vital function, especially in bipolar processing. When uniformly distributed throughout the slice at the correct concentration and microprecipitated in the proper manner, it protects the slice *throughout* the entire front-end process. It performs this function by internal gettering of impurities and preventing the formation of defects during thermal cycling. It is important to understand that the electrically active defects that degrade device performance and adversely affect yield are not in the starting slice but are introduced during device processing. *Silicon materials produced by U.S. manufacturers have not shown the correct properties to perform this protective function during device processing.* Certain Japanese silicon manufacturers can produce silicon of this quality. Silicon materials research and development in all major companies in the United States, West Germany, and Japan are directed toward understanding the role of oxygen in Czochralski silicon. The attainment of this fundamental understanding is one of the keys to the future success in VLSI.

At present, the prospects for the use of float-zone silicon for VLSI devices are limited by the extreme difficulty in

TABLE 5.1 Current Industrial Capabilities for Single-Crystal Silicon

Property	Czochralski	Float Zone	Requirements for VLSI
Resistivity (phosphorus) *n*-type	1–40 Ω-cm	1–300 Ω-cm	100–400 Ω-cm
Resistivity (antimony) *n*-type	0.005–10 Ω-cm		0.0002–0.02 Ω-cm
Resistivity (boron) *p*-type	0.005 –50 Ω-cm	1–300 Ω-cm	100–400 Ω-cm
Resistivity gradient (four-point probe)	5–10%	20%	<1%
Resistivity microsegregation	10–15%	20–50%	<1%
Minority carrier lifetime	30–300 μsec	50–500 μsec	300–1000 μsec
Oxygen	5–25 ppma	Not detected	Uniform and controlled
Carbon	1–5 ppma	0.1–1 ppma	<0.1 ppma
Dislocation (before processing)	≤500/cm²	≤500/cm²	≤1/cm²
Swirl (before processing)	None	Present	None
Dislocation (after 1100°C)	Haze	Stacking faults	None
Swirl (after 1100°C)	High	Present	None
Diameter	Up to 100 mm	Up to 90 mm	Up to 150 mm
Slice bow	≤25 μm	≤25 μm	<5 μm
Slice taper	≤15 μm	<15 μm	<5 μm
Surface flatness	≤5 μm	<5 μm	<1 μm
Backside surface finish	Uncontrolled	Uncontrolled	Controlled
Heavy-metal impurities	≤1 ppba	≤0.01 ppba	<0.001 ppba
Epitaxial film thickness	≥2 μm	≥2 μm	0.2–1.0 μm
Epitaxial film thickness uniformity	±20%	±20%	±1%
Epitaxial film resistivity	≤20 Ω-cm	≤20 Ω-cm	10–100 Ω-cm
Epitaxial film dislocation	≤500/cm²	≤500/cm²	<1/cm²

front-end processing of this material for shallow-junction high-speed devices. However, we can expect efforts on the part of industry to solve this problem.

A summary of current industrial capabilities for single crystal silicon and the requirements for VLSI is given in Table 5.1.

GaAs and Related Materials

The present status of research in III–V materials is encouraging. Certainly the scope of university research on these materials is extensive, possibly more extensive than it has ever been for silicon. *However, a disappointing aspect of university research is the tendency to emulate industrial efforts rather than to strike out into new high-risk areas and the failure in large measure to develop theoretical tools to predict new phenomena.*

Opportunities for new discoveries lie in the application of molecular-beam epitaxy and related techniques for producing controlled compositional variations on an atomic scale. Superlattices, heterojunctions, and artificially layered compounds are likely to reveal new properties.

Quaternary alloys, which can provide new degrees of freedom in the simultaneous achievement of desired band structures and lattice constants, will probably lead to new phenomena and device opportunities.

Interface problems, such as gate insulators and metal–semiconductor contacts, have presented barriers to device development and must be pursued; III–V epitaxial insulators or contacts may be a possibility in this field.

The final realization of the potential impact of III–V materials for high-speed integrated circuits may involve merging these materials with silicon in such a way that the chemical, metallurgical, and electronic properties of the III–V/silicon interface come into play. Basic research on these interactions must pave the way for a successful marriage of these two technologies.

Narrow-Gap Semiconductors

The study of narrow-gap semiconductors offers opportunities for the extension of semiconductor materials science and the technology of device fabrication. The narrow-gap alloy semiconductor, $Hg_{1-x}Cd_xTe$, is widely used in infrared sensors in thermal imaging systems. The lead salts, such as $Pb_{1-x}Sn_xTe$, are also under development for this application and as infrared diode emitters. Extensive high-quality physics research on band structure and electro-optical properties of these semiconductors has been carried out over the last 10–15 years. The limit on application of these materials now appears to be set by materials quality, device fabrication processes, and *the lack of knowledge of basic materials parameters*. For example, little basic research has been done on phase diagrams, dislocations, and impurity diffusion constants in $Hg_{1-x}Cd_xTe$. The substantial industrial effort on these materials over the last 10 years has depended somewhat on empirical approaches, and very little fundamental information is available on materials parameters.

In the last few years, the output of fundamental or basic-research results on narrow-bandgap materials has increased in eastern and western Europe but has decreased in the United States. This is in spite of substantial industrial activity on $Hg_{1-x}Cd_xTe$ and is perhaps due primarily to *an unfortunate* lack of coupling between the industrial and academic communities.

The basic need is for several strong basic research efforts centered on narrow-bandgap semiconductor materials sci-

ence. Although the activity should center on materials science, major contributions on device physics and defect physics are essential. The results of increased basic research activity would be the creation of a literature base on critical materials parameters, as well as the training of materials scientists for opportunities in a growing field.

In materials growth, new technologies and data are required on epitaxial deposition of semiconductors with low melting points and high vapor pressures. Careful, well-documented studies of point defects and dislocations and of their role in determining materials properties would have an important technological impact. Results on impurity diffusion, ion implantation, and the techniques for junction formation should be obtained and published in the open literature. Although much of the work should center on $Hg_{1-x}Cd_xTe$, related work can be carried out on a wide variety of other semiconductors. One of the major opportunities from the academic viewpoint, is a variety of thesis projects on related materials in a field that is not overworked and that can be used to train scientists and engineers for wider opportunities in semiconductor technology.

General Comments

The emergence over the past several years of powerful techniques for determining the structure and composition of surfaces and interfaces provides for the first time an opportunity to correlate the electrical properties of interfaces with structural models. This approach should be applied to interfaces of technological interest to provide an increased scientific basis for semiconductor processing.

Increased attention should be devoted to the enhanced role of imperfections in reducing yield when device dimensions are decreased and greater numbers of devices are interconnected on the same chip. The limitations imposed by statistical and process-induced fluctuations in composition should be clarified.

Some attention should be paid to the question of engineering new materials with desired properties. These properties would range from band structure and carrier scattering to process tolerance and amenability to low-temperature and/or dry processing.

E. SEMICONDUCTOR DEVICES AND CIRCUITS

As noted, a continuing decrease in semiconductor device size can be expected. The complexity of integrated circuits has approximately doubled each year for the past two decades. There are several factors that contribute to this trend, but a major one is the reduction in device dimensions. Two other major factors are increased circuit cleverness and larger die size. If, as has been suggested, the increases resulting from circuit cleverness do not continue at the same rate, then reduction of device dimensions will assume a larger role in progress toward VLSI. Yet, many problems that must be addressed hinder efforts to reduce further the sizes of the various semiconductor devices. In principle, models of MOS devices can be reduced readily via scaling theory. As dimensions decrease, high field effects in the devices become more important, for example, if the voltages are not scaled. Punch-through effects and impact ionization in the channel occur. Moreover, scaling is not complete unless operating temperature is also scaled.

Device Status and Specific Problems

LSI/VLSI Silicon Devices

Current high-density MOS technology has taken three major approaches to increased packing density for LSI. These are high-density MOS (HMOS), a polysilicon gate version of MOS, vertical channel (VMOS), and double-diffused MOS (DMOS). The latter two approaches employ double-diffused or epitaxial layers to define gate lengths, and VMOS also utilizes anisotropic etching for shaping V-grooves. In this case, the devices are essentially nonplanar, with the resulting gate lying along the face of the groove. For HMOS, channel lengths of 3–4 μm are now standard, with 2-μm channel lengths in development. Some extensive 1-μm channel device and circuit exercises have been reported for MOS from several research laboratories, for example, the 1-μm channel IBM work described at the 1978 International Electron Devices Meeting in Washington, D.C. Bipolar technology for increased packing density largely centers around integrated-injection logic (I^2L). Such devices offer higher speeds and power-delay products than MOS. At this point, however, I^2L circuits cannot be packed as densely as dynamic RAM, nor has the possibility of manufacturing them in the VLSI context been demonstrated.

Other effects that have become important and will be discussed, are edge effects and fringing fields. Hot electron injection into the oxide, nonlocal effects arising from the carrier transit time being a significant fraction of relaxation times, and subchannel current transport are also of importance. Modeling of the devices can no longer be constrained to simple one-dimensional approaches; detailed two-dimensional, or even three-dimensional, treatments are required to evaluate device operation. Surface and interface effects become increasingly important as device dimensions shrink.

High-Speed Devices

Recently, planar technology in the III-V's, primarily GaAs, has been developed for integrated-circuit and microwave-device fabrication. To a large extent, this technology uses ion implantation and is based on the Schottky-gate FET (MESFET, metal–semiconductor FET). Gate lengths, defined by the Schottky gate, are typically 1.0 μm, but gates as small as 0.25 μm have been fabricated. Although in a relatively primitive state, this technology appears to be the definitive one for microwave applications and to hold considerable promise for LSI digital applications.

The basic instability of the material resulting from inherent tendencies to form high-electric-field instabilities (Gunn effect) has led to early use of fully dynamic two-dimensional modeling to understand device performance

and to control unwanted domain nucleation. Other applications of these materials have led to many heterojunction-based devices, arising from the relative ease of fabrication of thin layers by molecular beam epitaxy (MBE) and organometallic chemical vapor deposition (CVD) growth. In particular, MBE has allowed growth of structures of alternating monolayers of GaAs and AlAs, a result that has challenged understanding of electronic energy-band structure. Contact problems and nonlocal transport effects are important in these devices. Moreover, these compounds do not possess the inherent native oxide of Si; therefore, they entail formidable surface and interface problems, both of characterization and of understanding.

Scientific Needs and Opportunities

As devices become smaller, the attendant problems are expected to become more severe, especially those that have already been encountered. However, university researchers should not concentrate on just the problems of extrapolation of current technology; industry expects to solve these problems. They should rather anticipate the needs at least 10–20 years ahead, especially those of the inherent device physics.

The special nature of the environment to which materials are exposed in solid-state devices has been accentuated by the advance of miniaturization in electronics. As device sizes are reduced, the dimensions of significant regions of solid-state devices become comparable to the fundamental lengths, for example, optical wavelengths, electron wavelengths, screening lengths in electronic systems, and widths of depletion regions in semiconductors. Solid-state devices permit the study of the properties of materials under the specialized constraints produced by miniaturization. The unique conditions to which materials are exposed in solid-state devices have led to the discovery or recognition of the importance of many new effects in solids and furnish a valuable tool with which the scientist can investigate various properties of matter. However, as devices are developed to perform useful functions, their application as materials probes cannot be fully anticipated. That is, the deviations of devices from their predicted performance that led to the discovery of novel phenomena cannot be programmed. In certain instances, however, it may be possible to invent devices to probe specific materials properties. To take advantage of the application of devices as material probes one must be alert to the possibilities that occur during device development. Unusual features of device performance that may represent unexpected materials phenomena should thus be vigorously pursued.

Oxides

Dielectric films play a central role in today's semiconductor device technologies. In many instances, however, the insulating electrical properties of these films are no more important than their structural or chemical properties. Insulators are most commonly associated with MOS gate dielectrics, dielectric insulation, or semiconductor surface passivation, but they also are used as hermetic seals, ion-diffusion barriers, and interlevel insulation layers. Further, they can serve as intermediate processing structures by functioning as masks for etching, oxidation, or diffusion or serving as diffusion sources or as contaminant gettering layers. Each of these different applications places different requirements on insulator properties, especially in the fabrication of very small devices. Perhaps the greatest demands are placed on functionally active insulators in devices. Typical of such active insulators is an MOS gate insulator, usually the thinnest insulator in a device; it is required to withstand the highest electric fields and is the least tolerant of mobile oxide charge, interface states, and electron traps. This gate insulator must have very-low-defect densities and very high reliability and must be capable of withstanding the high temperatures and stresses associated with subsequent device processing. Although defects may not provide a fundamental limit to reducing device dimensions, they are crucial in determining the rate of progress to higher levels of integration in devices.

Research that could lead to alleviation of some of these defect-related problems would deal with high-dielectric-constant insulators. Their use would allow thinner insulators for the same surface-carrier density. It is well known that individual defects are not so important for breakdown strengths in thin films.

The use of a III–V semiconductor rather than Si presents even greater challenges to the materials scientist in producing acceptable insulator films. Despite considerable effort, no one has yet found an analog to the thermal oxide on Si for compound semiconductors. Thus, these devices have been used in optoelectronics or with Schottky gates and not as inversion channel devices for VLSI. Although III–V MOS devices may ultimately give higher performance than silicon MOSFET's in a VLSI technology, this III–V development has lagged behind silicon by a decade, and the gap seems to be widening, although a few laboratory devices have been produced in InP and InAs.

The trend to smaller device and insulator dimensions presents many challenges. First, the reliability of the insulator must be improved, as the insulator thickness is reduced. As the size of a critical defect is reduced, the number of such defects increases dramatically, which is the opposite of the desired direction. Second, an accompanying trend is to operate these very small devices at the maximum possible voltage where hot electron injection occurs; hence, it becomes increasingly important to control and reduce insulator traps, especially neutral traps, which tend to trap the injected electrons. Third, the fabrication of very fine dimensions generally requires high-energy radiation, as in electron-beam and x-ray lithography, plasma and reactive-ion etching, ion implantation, and plasma deposition of films, all of which tend to generate oxide traps. Thus the generation and annealing of radiation-induced trapping in insulators becomes exceedingly important. Finally, a decrease in device or insulator dimensions requires a corresponding decrease in tolerances. Not only must the insulator tolerances scale down, but other device parameters must also be better

controlled; often this means that the range and/or number of the thermal cycles used to prepare the insulator must be reduced. Before small-dimensional devices become widely used, it will be necessary to improve the understanding of insulator properties, to enhance control over insulator parameters, and to increase yield.

Metallization

The continuing trend toward higher density and the resultant very-large-scale integration levels are placing severe demands on metallization techniques. The problem is particularly acute in semiconductor integrated-circuit technology in which metal-to-semiconductor contacts impose additional constraints. The requirements for a useful metallization system are multiple: good adhesion to dielectrics, selective etchability, low electrical resistivity, good coverage of surface topography, high electromigration resistance, resistance to oxidation and corrosion, and, for semiconductor applications, low metal-to-semiconductor contact resistance and good contact stability. The requirements for large-scale integration are currently being met by the use of proper aluminum alloys (e.g., Al/Cu/Si) and contact metallurgies such as Pt_2Si. It should be noted that LSI MOS structures with polycrystalline silicon gates employ either diffused regions in crystalline silicon or the heavily doped polycrystalline silicon as one level of interconnection. *The limited conductivity of such layers will not allow such applications when device geometries decrease much below present dimensions.* Replacing these materials by using multilevel metallization requires the formation of tens of thousands of very small metal-to-semiconductor contacts, which is a challenging problem aggravated by the decrease in junction depth imposed by decreasing device dimensions.

An alternative to multilevel metallization may be provided by refractory metal silicides such as tungsten disilicide and molybdenum disilicide. Recent investigations have demonstrated that the conductivity limitations posed by polycrystalline silicon can be substantially reduced by replacing or supplementing the polycrystalline silicon by metal silicide. A particularly attractive property of such silicides is that oxidizing ambients produce an insulating and passivating layer of silicon dioxide so that these new materials can be incorporated into polycrystalline silicon gate technology with minor process changes. Some empirical descriptions exist for the metal–semiconductor interactions. However, the problems of the metal-to-semiconductor contact are further aggravated by lack of knowledge of the interfacial reaction kinetics during the formation of the silicide. While some information is available, from equilibrium phase diagrams, on the initial silicide formed, the details of subsequent compound formation and on the Si–silicide interface are still not understood. Now the emphasis must shift to the study of the underlying fundamental mechanisms governing the behavior of these systems. Properties of the metal–semiconductor interface must be studied intensively. Advances in electron microscopy and MeV ion-channeling techniques may provide new insights into the properties of such interface layers. An additional problem associated with VLSI is the dissolution of silicon into the metallization layer and the resultant edge effects around the periphery of the active devices.

Other possible candidates to solve metallization problems are synthetic metals, many of which contain no atoms of any metallic element. The motivation for producing new conductors is in part a desire to achieve unusual or even unprecedented materials properties of technological importance. Metallic conductors are based on open-shell atoms, whereas nonmetallic compounds typically exhibit covalent or polar bonding based on closed shells. Since open-shell electronic bands are a prerequisite for any conductor, molecular or polymeric conductors will almost certainly be chemically unusual. The stabilization of interacting open-shell nonmetals in a solid, to prevent the exclusive formation of polar-covalent bonds, is an enormously challenging task, but recent developments with doped polythiazyl $(SN)_x$ and polyacetylene (CH) suggest that the judicious incorporation of electron donating and withdrawing groups may yet provide a fairly general scheme for achieving incompletely filled bands, as required for conductors. In fact materials such as $(SN)_x$ have been used to form metallic Schottky barriers on semiconductors.

Surfaces

Dry processing and the chemical interactions at the surface are important. Moreover, the chemistry and physics of the surfaces and interfaces become crucial for processing and operation of these devices, particularly in the case of the compound semiconductors. As discussed in other chapters, the physics of the interface can completely dominate the device performance.

Ion Implantation

Ion implantation is conventionally used in low-dose applications in fabrication of MOS structures because of the uniformity and reproducibility inherent in the ion-beam techniques. Further investigation of the higher ion-dose levels used in bipolar emitter regions is required. It is commonly acknowledged that there are edge effects around the periphery of the implanted regions produced by recoil implantation or atom mixing by knock-on of the mask material and due to the requirement for extensive annealing to move the active junction region away from the implanted region. During thermal annealing, defects can propagate laterally, leading to side-wall penetration. In commercial systems with high device throughputs, the high dose rate leads to sample heating and lateral nonuniformities in defect structures across the implanted wafer. Most of these problems can be overcome in LSI structures by diffusing the implanted dopants beyond the range of the implanted region. With the dimensional constraints imposed by VLSI, the conventional thermal annealing approach may not be applicable.

Basic research in ion implantation requires studies of defect structures, gettering of fast-moving impurities, defect

propagation, and influence of ambient effects during annealing.

Device Modeling

In recent years, numerical large-scale simulation has begun to fill the gap between simple models that allow closed-form solutions and the sophisticated structures of technologically modern devices. These efforts have led to the development of full two-dimensional solutions for the device potentials and currents that reflect the effects arising from the geometrical inhomogeneity. These techniques have been utilized to probe the operation of ever smaller devices. However, in all but a few cases, these techniques have employed a local, quasi-static relationship between the electron dynamics and the electric field. By "local" and "quasi-static" we mean that the drift velocity is equivalent to what would be obtained in a large sample if the electric field were uniform through the sample and time-dependent. One should not expect this approach to be applicable to small devices.

Transport is characterized by several characteristic times; for example, the scattering time τ, the momentum relaxation time τ_m, and the energy relaxation time τ_E. The momentum relaxation time characterizes the momentum response of the free carriers; the energy relaxation time describes the manner in which the mean kinetic energy of the carrier gas relaxes to equilibrium with the lattice. When these relaxation times become comparable with the transit time of carriers through the device, as in small devices, then the velocity becomes a nonlocal, non-quasi-static function of the electric field. In this case, the velocity response becomes a retarded function of the electric field and effects such as overshoot velocity become important. Thus, static velocity–field curves can be expected to become meaningless as device dimensions shrink into the submicrometer range.

If large fields are present, then large field gradients can also be expected. Concomitantly, spatial relaxation effects are likely in the local charge density and the resultant fields. If the velocity–field relationship is nonlinear, as would generally be expected, then these spatial relaxation effects determine the existence and growth of space-charge domains. As a consequence, self-consistent solutions must be sought for the fields and potentials in the device. The large field gradients can also lead to large gradients in the effective carrier kinetic temperature. These effects in turn lead to thermally induced currents in the device. In many cases, these spatial relaxation effects and thermal gradient effects can be expected to play far larger roles than diffusion effects in majority-carrier devices.

Although device modeling has progressed, experimentation on small devices has not advanced so rapidly. Although the National Research and Resource Facility for Submicron Structures at Cornell University will help to meet this problem, there is continuing need for several regionally distributed, small, special-purpose, electron-beam systems capable of submicrometer resolution but designed for fabrication of a single device rather than the exposure of an entire chip.

Device Physics

As device size continues to shrink, typical dimensions will soon be in the range where we will have to question our concepts of transport theory and of device behavior. It is difficult to predict what new phenomena and effects might appear, but current knowledge of transport theory can be applied to the achievement of an understanding of the effects, resulting from short transit times, which arise primarily because of the small distances and high local fields.

The concept of short transit times in small devices was discussed in connection with the characteristic relaxation times and the nonlocality of the velocity–electric field relation. When, in addition, the collision time becomes comparable with the transit time through the device, one must question the applicability of the concepts of mean free path and mobility. Edge, interface, and surface effects dominate the transport, and the resultant additional scattering processes reduce the effective time between collisions so that the time duration of a collision begins to be of the same order as the mean time between collisions. The usefulness of perturbative approaches then becomes questionable, and the scattering-induced self-energy shifts lead to severe limitations on the applicability of the one-electron energy band and density-of-states concepts. As a result, the entire Boltzmann transport equation approach begins to break down and must be replaced by more appropriate quantum transport approaches.

There are many characteristic lengths that are important for small devices. Spatial relaxation and large gradient effects in field and carrier kinetic temperature were mentioned previously. Device dimensions are more nearly comparable to the electron wavelength, the carrier screening length, the mean free path, and perhaps even the mean impurity spacing. Two-dimensional quantization is observed in devices in which the channel thickness is comparable to the electron wavelength; this occurs in MOS devices and in Schottky gate FET's, where the minimum channel thickness is set by the interimpurity spacing. As devices become smaller, device dimensions could become comparable with the classical screening lengths, requiring a rethinking of our concepts of screening. If scaling theories, as currently used, are extended to smaller devices, considerably larger doping densities and carrier densities are expected. These in turn will probably lead to considerable band renormalization and phonon-softening contributions to deviations from one-electron band structures, as well as strong spatial relaxation effects in the energy gap. The small device size can lead to reduction in impact ionization effects and increased impact of tunneling effects. Microstatistical problems will become more important. Whether from ion implantation or diffusion, the statistical variation of impurity location can become significant as device dimensions shrink. Moreover, in ion implantation, small-scale microstructures remain from the implant/anneal process; and these can become important. And, of course, surface unevenness, even on the 5–10 Å scale, can be expected to become critical in very small devices.

Because of the expected high electric fields in small de-

vices, we expect all transport to be of the so-called hot-electron type. Energetic carriers are readily injected from an MOS channel into the oxide in very high electric fields, and impact ionization is currently a limitation in such devices. Other, more physically oriented effects should result from the high fields. The accelerating field and the scattering potential can no longer be treated as separate perturbations, and modifications of the scattering times from acceleration by the field *during* the collision become important for transport, as has been shown for transport in silicon dioxide. Moreover, for very small devices and very large fields, quantization of the electron energy levels due to the field is likely to be important.

F. CIRCUITS AND SYSTEMS

The complexity of the problems that we can now consider solving at the single-chip level through VLSI call for a new approach to integrated circuit (IC) chip design. We suggest that an appropriate approach may be one in which the entire set of problems from materials-processing science through the physics of microstructure devices to information systems science is viewed as a continuum. It is highly desirable to adopt a holistic approach to the design of VLSI to consolidate detailed understanding of IC process physics with innovative top-down systems design. At the same time, the feasibility of VLSI can best be assured by these developments:

1. Basic process models
2. Process and device simulation
3. Automated process equipment and data logging
4. Automated testing
5. Structured design
6. A variety of design automation aids

Although knowledge of the relevant basic processes such as ion implantation, thermal oxidation, diffusion, and epitaxy is primitive, but growing continually, the device implications are so profound that the need for further research is obvious. The advent of complete process simulations and the coupling of process physics with device physics by means of powerful analytic tools, are key steps toward achieving VLSI.

Moreover, through automation of process equipment, the most wildly fluctuating variable, the human operator, can be removed from increasingly larger and more sensitive segments of the VLSI fabrication sequence. In addition, automated data logging and subsequent convenient data access via remote computer terminals can provide much more accurate and timely information regarding the fabrication sequence to which a given wafer or chip was exposed. Combining this information with that generated through automated electrical testing of wafers will allow much more effective feedback to a fabrication line. The final two listed items indicate that the inherent structure of the system-design process, as well as the automation of its implementation, are essential in guaranteeing VLSI chips that work and can be fabricated with acceptable yields.

Based on the arguments of the preceding paragraph, we believe that competitive domestic and foreign pressures alone necessitate increasing use of VLSI process models. Current and projected product goals also clearly indicate the increasing necessity for VLSI process models. For example:

1. The development of complex monolithic chips to perform in a large focal plane array including more than 10^6 CCD image-sensing elements with onboard high-speed bipolar digital signal processing entails a complex fabrication technology that requires full exploitation of available process and device models.
2. The development of semiconductor dynamic RAM chips with more than 10^6 bits of storage, minimum feature sizes under 1 μm (approaching the fundamental room-temperature limits of MOSFET's), superior reliability, and a selling price less than $20 places a burden on fabrication technology that also demands full exploitation of available process and device models.
3. The development of true single-chip "microsystems" —following microcomputers, which in turn followed microprocessors—with, for example, only one external power supply, all internal clocks, latches, and buffers, on-chip memory, and compatible integrated analog-to-digital and digital-to-analog converters, as well as analog preprocessors and output drivers, will place perhaps the ultimate burden on semiconductor fabrication technology and clearly will require extensive reliance on process models.

In designing the semiconductor products—the integrated systems or single-chip microsystems—suggested in the previous paragraph, the ultimate utility of VLSI process models will be measured by reductions in development time for a complex new chip, development cost (from time and labor savings), and production cost (from higher yields) in higher product reliability resulting from tighter process control and in improved system performance due to the richer set of trade-offs available to chip designers.

Much of the improvement of the functional characteristics of VLSI systems over the next decade is expected to result from better circuit organization. When many thousands of components are deployed to perform some function, the organization of those components becomes a major factor in their collective performance; this is especially important when the ultimate computation speed in a system approaches the level where it is limited by the rate at which information can be transmitted from one component to another. Heretofore, we have designed LSI systems with a clear-cut separation between memory and computing functions; such a separation is no longer warranted.

To begin the linking of materials-processing science with information-systems science, investigation of a structured approach to VLSI is needed. Historically, the design of digital systems has followed a four-phase, bottom-up procedure.

First, the process/device engineer, forecasting the requirements of the circuit engineer, developed a compatible sequence of semiconductor fabrication processes for a new family of integrated circuits. Second, the circuit designer, anticipating the needs of the system designer, provided a set of components capable of performing various logical functions. Then, the system designer, anticipating the needs of the software programmer, assembled the hardware into a digital system for solving a class of problems of interest. Finally, the programmer implemented an algorithm to solve a problem of immediate concern. Limited feedback ensued, and after the functional and physical separation had been established, the problem was rarely viewed as a whole, except at the final stage.

With the introduction of VLSI, this traditional evolution will no longer effectively solve many problems of interest. The complexity of the problems at the level of a single chip, the blurring of the distinction between hardware and software, and the comparable complexity of hardware and software call for a new organization of the design process that is more synergetic than past approaches and in which a careful study of the required machine organization must be included.

This alternative methodology separates the design of VLSI into two phases: an initial, theoretical and a final, practical phase. The initial phase begins with the collection of a set of problems for solution. These problems are then abstracted, and solution methods are proposed in which the form of the solution follows the form of the problem. The second phase begins by grouping these algorithms to isolate a compatible set of problems requiring a common method of solution. In this way, only those parts of the problem that are truly separable are in fact separated. A solution for a specific problem class can then be specified in terms of hardware and software, and a logical partitioning into constituent modules can be made. As the final stage of the practical phase, a physical partitioning is made, and implementation proceeds.

This approach, structured about organizational concepts, is valuable for several reasons. As the distinction between hardware and software becomes increasingly blurred, the complexity available with VLSI will undoubtedly lead to the same type and magnitude of problems that have plagued the development of large software projects in the past. The key element in such a project is a proper, logical partitioning of the solution into self-contained modules with clean, general, extensible interfaces. Within this framework, the physical partitioning required at an early phase by the bottom-up design is unclear; the early division into fabrication process sequence, circuit chips, circuit boards, and software modules may prove deleterious for complex systems.

For example, consider the evolution of a large computer operating system. Segmented into modules at its inception, any repartitioning after its release to customers is an expensive but feasible endeavor. However, after the customers develop applications software that depends on that operating system, repartitioning quickly becomes prohibitively costly. With VLSI, repartitioning will presumably be as expensive, and errors will be as hard to correct.

These problems are rarely seen at the small- and medium-scale integration level when chips consist of latches, gates, registers, counters, and the like. Even today, on the verge of VLSI, industry focuses on implementing standard, well-understood, logical structures and processors. This approach, however, will become less feasible as VLSI is used for implementing specialized hardware designed to meet specific requirements.

Implantable telemetry systems for use in biomedical research provide an interesting and unusual, yet simple, example of a top-down design approach. For ethical, legal, scientific, and economic reasons, animal models of human disease are generally regarded as indispensable tools in biomedical research. Totally implantable telemetry systems using automated techniques for continuous data collection provide invaluable appendages to animal models of human disease because they make it possible to acquire data that are inaccessible from the body surface of the animal under conditions when the animal is not anesthetized or restrained in any way over prolonged periods of its normal life. For example, because 20 percent of the male population of the United States reaching age 65 will have suffered from a coronary attack, means of preventing and treating coronary disease, such as new drugs, are extremely important. Research on such drugs benefits greatly from the use of animal models for which cardiovascular behavior can be accurately observed over a prolonged period of normal life. Consequently, totally implantable blood flowmeters that are capable of measuring the volume of flow in a coronary artery are needed. These devices obviously must be extremely small and consume very little power to serve the intended purpose.

The design of telemetry systems for coronary flow and pressure, as well as cardiac electrograms, begins with the statement of the medical problem, proceeds to optimal partitioning of the total instrument system between external and internal subsystems, and then turns to definition of their architectures. Focusing on the internal subsystem, one must devise particular circuit functions to achieve the required performance. These functions must be implemented with an optimal, silicon, monolithic device technology. Among the important requirements of this technology are the ability to provide circuits that operate reliably when energized at the extremely low currents furnished by a single lithium cell with a terminal voltage of 2.7 V. Thus the design of custom, micropower, monolithic circuits, typically combining analog and digital functions, is a key optimization feature in the top-down design approach. Ion implantation to achieve very-high-value resistors is particularly important, as is the fabrication of linear, compatible, I^2L digital electronics that will operate effectively at collector currents as low as 10^{-9} A. Although this example deals with an extremely simple system, it illustrates a holistic top-down approach to design of specialized hardware to meet specific and urgent needs. At each level of the design hierarchy—that is, the system level, the circuit level, the device level, and process levels—quantitative models that permit accurate simulation can reduce the cost of designing such specialized hardware.

In summary, the advent of VLSI with extremely fine-geometry devices virtually precludes the conventional cut-and-try approaches to process and device design. Ongoing efforts in process and device modeling bring many of the VLSI bottom-up issues clearly into perspective. Consequently, it appears that holistic top-down approaches (Table 5.2) to the design of information systems hold the major promise for resolving the complex problems posed by requirements for processing of millions to billions of logical operations per second.

The objectives of future research should be the following:

1. To identify the nature of information-processing strategies that lend themselves to VLSI; for example, minimizing and regularizing component connections (an important consideration now that wires and information transfer times dominate the cost of computing equipment) begins with the specification of the solution.
2. To define the approach for achieving a facility for VLSI design automation. This capability necessarily merges top-down structure architectures with the recent developments in computer aids for process and device modeling.

TABLE 5.2 VLSI Design: A Holistic Structured Approach

- Statement of Generic Problem
- Expression of Algorithm
- System Architecture
- Logic Design
- Circuit, Device, and Process Definition

The scope of these two objectives is oversimplified. The first goal stresses the importance of novel algorithms, now with an emphasis on hardware opportunities. We must consider VLSI interconnections as communications networks, and, conversely, systems approaches must be applied vigorously to IC design. The second objective encompasses the full range of design automation starting with functional simulation and extends down to module design, interconnection, testing, and reliability. Since the final IC hardware is to be built with VLSI device-processing technologies, the ultimate need for the process and device-modeling efforts discussed earlier is implicit.

6
Science Opportunities

A. INTRODUCTION AND CONCLUSIONS

In considering the possibilities for new science opportunities that might come from the development of submicrometer technology, it is important to appreciate the nature of the industry involved. The semiconductor industry, to a larger extent than any other, has been based on advances in, and a strong interplay with, basic research, particularly in the electronic properties of solids and the associated materials science. This coupling is directly responsible for many of the semiconductor industry's major advances, derived largely from scientific knowledge developed in the 1950's and 1960's. These advances will continue until device sizes become such that scaling of the present devices ceases to be valid. As discussed in this report, this size is surely in the few tenths of a micrometer range. Thus, as a basis for new technology on the submicrometer scale, a renewed and enhanced basic research effort in solid-state physics and materials science is required.

We cannot overemphasize the importance of this interplay between semiconductor technology and basic research in solid-state physics and materials science. For the sake of concreteness, we illustrate this interplay by two examples.

When *p-n* junctions were first made, it turned out that above certain voltages applied in the reverse- or low-current direction, the current was orders of magnitude higher than predicted by simple theory. This effect, which is termed dielectric breakdown, had been known for many years. The very high fields existing in the depletion region of a *p-n* junction, however, made breakdown a commonly encountered phenomenon and a practical problem in that it limited the range of application of devices. Because of the ease with which high electric fields could be produced in *p-n* junctions, the junctions themselves became the primary vehicle for the study of breakdown. Thus a new area of solid-state physics was opened to exploration by the unique environment of the depletion region of a *p-n* junction.

The study of breakdown in junctions soon revealed that two effects were involved: tunneling, or "Zener" breakdown, and avalanche breakdown, in which electrons acquire enough kinetic energy to excite another electron across the gap from the valence band to the conduction band. It was found that tunneling could be enhanced to create a new kind of device, the tunnel diode. Although the tunnel diode has not gained an important place in technology, it has been realized in many semiconductors and has been employed at low temperatures as a probe of the phonon and electron energy band structures of semiconductors. Investigations of the mechanism of avalanche breakdown led to the concept of hot electrons, and eventually to the discovery of the Gunn effect, and extensive research into scattering mechanisms for hot electrons in a great variety of semiconductors.

Field-effect transistors (FET's) also provide a unique environment, in that conduction in the semiconductor occurs in a thin layer less than 5 nm in thickness. This layer is so thin that motion of electrons confined in it is quantized in the direction normal to the surface; the quantum energy spacings are much larger than kT (where k is the Boltzmann constant and T is the absolute temperature) at cryogenic

temperatures. The electrons in the layer thus constitute a two-dimensional Fermi gas. There is a large amount of flexibility in the FET environment, which makes it extraordinarily useful; the thickness of the layer can be changed by varying the electrical potentials applied to the device, and the scattering can be altered by introducing charged impurities in the SiO_2 and by otherwise doping the silicon. It should be noted that, although the quantization effects could be predicted from physical theory, their experimental discovery was stimulated by the observation of anomalies in FET device characteristics.

In developing submicrometer technology, this kind of interplay will remain important. For example, to make wires that are several hundred angstroms in diameter, their edge definition would have to be on the scale of a few angstroms. Thus polycrystalline material and amorphous metals would no longer be suitable; new ways of growing epitaxial metals, or possibly conducting polymers, would be necessay. However, current understanding of such materials is insufficient to permit their use in such applications. Thus, the impetus for new research will come from the technological implications, and in turn, the technology will advance. Thus, *our main conclusion is that a high level of long-range research activity closely related to integrated circuit technology is essential for continued progress.*

Although the interplay among solid-state physics, materials science, and submicrometer technology is extremely important, experimental science also advances through new technology. For example, radar developed during World War II led to radio receivers, which in turn led to the development of radioastronomy, and to, what is regarded by many as, convincing support for the big-bang concept of the origin of the universe. Advances in computers have now taken us to the point where data acquisition and analysis for many experiments are controlled by minicomputers and microprocessors, thereby revealing new horizons in data handling and analysis. The recent work by W. A. Little at Stanford University in producing refrigerators small enough to fit on silicon wafers is an example of near conventional approaches to solve problems in ultraminiaturization, which will have import not only for integrated circuit technology but for other areas of technology and basic research as well. In a similar way, submicrometer technology is going to have wide-ranging impacts in virtually all fields of science. However, although science will benefit from the new technology developed *primarily* for other purposes, there are possibilities for many specialized devices that will not have wide applicability but will be of considerable use in various fields of scientific research. Examples are solid-state detectors for astrophysics, elementary-particle physics, x-ray and electron-scattering physics, and biology; submillimeter-wave detectors for astrophysics and far-infrared spectroscopy; and a variety of miniaturized devices for solid-state physics, which will allow the probing of systems at scales of distance comparable with the characteristic lengths of the system. Therefore, *our second conclusion is that it is important to provide access for scientists to facilities where special-purpose, miniaturized electronic devices can be designed and fabricated. Funds should be made available to stimulate and facilitate the development of such advanced specialized devices.*

In this chapter we cite selected examples of the types of scientific opportunities that are made possible by microstructure science and technology. These are representative of ideas close to current realities. Any imaginative scientist could add examples. Undoubtedly, developments in the future will far exceed what we expect on the basis of our limited present-day imagination.

B. FUNDAMENTAL LIMITS

In all present semiconductor devices, there are certain characteristic lengths, such as the Debye screening length and the electron mean free path, that are related to the dimensions of the device. Attempts to scale down current devices to the submicrometer regime frequently fail because the relationships between the dimensions of the device and the relevant characteristic lengths change. At the same time, devices already depend on manipulating a variety of fairly fundamental lengths, and the breakdown of scaling emphasizes the need to learn to manipulate other, perhaps more fundamental, characteristic lengths.

This need will stimulate many new ideas in basic solid-state physics and materials science. To illustrate this point, we list in Table 6.1 a variety of lengths, some of which are manipulated in present devices and others that are currently considered as fundamental limits.

As mentioned earlier, interconnections using metal stripes will soon involve dimensions that are small compared with grain sizes. To obtain adequate line definition, it will be necessary to develop epitaxial growth of metals or learn to use amorphous metals or perhaps highly conducting polymers. If, for example, we could develop epitaxial metal lines with lateral dimensions of 100 Å controlled to the atomic level, electron waveguides might be possible. If it turns out that this is not possible, the increased understanding of epitaxial growth or amorphous metals or highly conducting polymers will be a fundamental advance. It may be that the localized states that occur in amorphous semiconductor materials will become important for storing charge in small devices. If so, considerable knowledge of the spatial extent of these states would be a prerequisite and would enhance understanding of their nature. At present, almost nothing is known regarding this matter, which is fundamental to all theories of localization.

The situation is similar for deep-trap levels in semiconductors. Eventually, perhaps, these levels can be used rather than regarded as defects to be avoided, but a much better understanding of their nature will first be necessary. The same is true of surface bands. Efforts to characterize these bands and attempts to change their carrier density, for example, are only beginning.

Another fundamental limitation is the discreteness of electron charge, which, since it is necessary to use an integral number of electrons to represent a signal, results in statistical noise. The voltage across a capacitor 100 Å × 100 Å × 100 Å changes by about 0.5 V for a change of one

TABLE 6.1 New Phenomena Found in Silicon Configured to Dimensions Comparable with Characteristic Lengths and the Resulting Device Concepts

Achievable Linewidths	Characteristic Length	Physical Phenomenon	Resulting Device
Production (>3 μm)	• Minority carrier diffusion length	• Minority carrier injection/collection	• Bipolar transistor
	• Depletion length	• Punch-through	• JFET, IGFET, CCD
	• Tunneling length	• Tunneling	• MOS, tunnel diodes, ohmic contacts
Developmental (0.2–3 μm)	• Debye screening length	• Field shielding	• Accumulation-mode CCD
	• Mean free path, energy loss	• Velocity overshoot	• Microwave transistors
Exploratory (<0.2 μm)	• Mean free path, momentum loss	• Ballistic transport	?
	• Bloch wavelength	• Quantization/tunneling	?
	• Grain size	• Metallization	?
	• Lattice constant	• Breakdown of effective mass approximation	?

electronic charge in the charge on the capacitor. Perhaps new techniques, such as the "proofreading" techniques nature uses in biological systems, can be employed in solid-state devices to overcome this problem.

The problem of excess noise at low frequencies, commonly called $1/f$ noise or flicker noise, may well be a serious problem. The fundamental cause of this noise is not understood, so one cannot reliably predict the consequent limitations. However, from a phenomenological point of view, we know that a small number of electrons, a small conducting region in which there is a bottleneck in current flow, and the relatively larger thermal fluctuations associated with smaller volumes can all be expected to increase greatly this excess low-frequency noise in small structures.

Although these specific examples may not, in fact, turn out to be important, past history suggests that the probability of such activity leading to the discovery of new phenomena and new inventions is high.

C. CONDENSED-MATTER PHYSICS

The ability to prepare structures at the micrometer and submicrometer level offers the opportunity for novel experimental studies in condensed-matter physics. We give a few selected examples of the applications of microstructure technology to basic research to show kinds of problems that might profit from use of future developments in semiconductor technology.

Maximum Metallic Resistance in Thin Wires

It has been argued that electronic states should be localized in any wire with impurity resistance greater than about 10 kΩ. At sufficiently low temperatures this could lead to a T^{-2} dependence on the absolute temperature, T, because phonons are needed to assist electronic transitions between localized states. The condition for the localization to be apparent depends on the cross-sectional area of the wire; for 10^2-Å wire, such effects should be easily observable at liquid helium temperatures. This problem is of fundamental scientific interest and cannot be approached by "conventional" techniques—submicrometer fabrication alone can make it possible.

Metal-Insulator Transition at High Pressure

Studies of the insulator-to-metal transition have been scientifically important for many years; however, because of the need for very high pressures in some cases, such experiments represent a major undertaking with conventional techniques. An ultra-high-pressure (possibly 3 Mbars or more) research project utilizing microfabrication techniques is being carried out at Cornell University.

At present, the electrical leads are 10 μm apart. Photoetch techniques are used. Preliminary work with electroetch methods, and also ion etching, to reduce the separation of electrical leads to 0.1 μm, is beginning.

To obtain the needed pressures it is necessary to use

1. The hardest substance known
2. The smallest contact radius possible
3. Specially profiled shapes
4. Superb surface finishes

Of necessity, microfabrication technology must be used, and extremely small samples (0.1 μm thick and only a few micrometers in diameter) must be carefully characterized.

Such high pressures can also be used to synthesize new materials and to study their properties.

Electron–Phonon Interaction Spectroscopy Using Metal–Metal Contacts

Yanson (Kharkov, U.S.S.R.) is doing electron–phonon interaction spectroscopy using randomly fabricated metal–metal

contacts with dimensions on the order of 100 Å. The contacts arise from "pinholes" through an insulating film between two metal films. Electron flow through the contact can be ballistic, with electrons dropping through about 1 V within one mean free path, then emitting phonons in an interesting nonlinear fashion. Yanson claims to have seen electron de Broglie waveguide modes in some contacts. The concepts are almost like vacuum electronics inside a solid. With better control and definition in the fabrication of such contacts, using microstructure fabrication techniques, a variety of interesting and important phenomena involving the electron–phonon system could be probed.

Quasi-particle Diffusion Length in Superconductors

On both sides of a weak link in a tunnel junction, the quasi-particle chemical potential is out of equilibrium with the superconductor chemical potential for pairs, for a distance that is called the quasi-particle diffusion length. This length was measured by G. J. Dolan and L. D. Jackel of Bell Laboratories by placing normal and superconducting electrodes 1–2 μm apart downstream from a weak link. This experiment was made possible by the development of offset masks for liftoff photoprocessing. The measurement is the first direct one of the quasi-particle diffusion length in superconductors.

Planar Tunnel Junctions

These thin-film junctions are made by fabricating two metal films in close proximity on an insulating substrate. The edges of the films must be close enough to permit tunneling, that is, 25 to 100 Å. This requirement introduces a new critical length, that over which tunneling occurs or the width at the tunnel barrier. In this case, this dimension is determined by the separation of the planar metal films not by the thickness of a growing oxide, which presents interface problems. Very thin substrates, which allow transmission electron microscopy (TEM) studies to be made, are preferred. Only TEM has the necessary resolution for studying such samples. Work on high-resolution electron-beam lithography has indicated that such samples are possible.

A variety of physical studies could be made with such junctions. With barrier materials deposited between the metals, potential barriers could be measured by tunneling, since the barrier thickness would be predetermined. Tunneling spectroscopy could also be used on these deposited materials. As the interfaces would be comparatively sharp, scattering processes at this small dimension could be better understood. Study of chain-like organics could determine whether there is a difference in potential barrier or tunneling probability when the chains are perpendicular or parallel to the tunnel current. For low-potential barrier materials, wider gaps could be used. For high-potential barrier materials, tunneling through the substrate might occur, which would also be interesting; however, this could be reduced by etching the substrate so that the metal films would be free standing. In this way, vacuum tunneling could be studied.

System-Environment Interaction

With miniaturization, the total system—system of interest plus environment—is of the scale of the characteristic lengths and wavelengths. It would thus become impossible to separate phenomena associated with the system of interest from phenomena stemming from the interaction of the system of interest with the environment. This problem is already important, for example, in intercalated systems as well as in biological systems. We have cited one example for which such inhomogeneity can be turned to advantage—the two-dimensional Fermi gas in FET's, which was discussed in Section A, and there are doubtless others.

Spatial Spectroscopy

Using microstructures as spatially limited sources of electric fields and heat, one could, in effect, construct a fine spatial probe for observing desorption from thin films. Similar studies using optical techniques with lasers (limited in size to λ^2) or electron-beam techniques (10^2 Å^2) would also be possible. However, certain physical systems may have to be studied by other excitation methods and may require microstructures for higher resolution. A thin system could be created by constructing conducting parallel lines separated by a thin resistive material from another set of conducting parallel lines oriented at right angles to the first; the resultant structure could be employed as an addressable heater array.

Three-Dimensional Microstructures

Mechanical deflecting devices of submicrometer lateral dimensions are possible with present techniques. Such a device has been constructed by taking advantage of differential etching rates for different dopings of Si. This device was utilized to deflect light. It is possible to make submicrometer devices with which to modify reflection of electromagnetic radiation by modifying the interference of different portions of the array, for example, the grating strength. This particular example is included to show that mechanical structures with varying dimensions should also be envisioned as an area in which one can do speculative new science.

With sizes of devices and interconnections comparable to electron wavelengths, perhaps we should think of transport as guided by waves. Hence concepts of waveguide technology would be appropriate. It should be possible to fabricate waveguide devices for electrons, phonons, and other types of waves in condensed matter, as well as photons (e.g., soft x rays). With the control that would thus become possible, a variety of wave-interaction experiments would be feasible. It might even be possible to construct the analogs of electromagnetic traveling-wave amplifiers and oscillators for other types of waves in condensed matter.

As device sizes decrease and the number of devices in VLSI systems becomes very large, phenomena similar to those in condensed-matter systems might be expected to occur, for example, cooperative phenomena and perhaps phase transitions. What concepts and techniques from condensed-matter theory and experiment and biology can be adopted to help us understand VLSI systems? For example,

cooperative phenomena in condensed-matter systems are quite tolerant of defects and depend crucially on dimensionality. Will the same be true of VLSI systems? Can such general and powerful theoretical tools as renormalized group techniques be applied to VLSI systems?

Low-Temperature Physics

To date, the production of very low temperatures (T less than 1 mK) has been expensive because of the scale of the cryogenic equipment required. Many of the experiments could be performed much more rapidly and cheaply if the whole scale of the sample and refrigerant mass could be reduced. For such purposes, microstructure instrumentation would be needed. For example, perhaps superconducting strain gauges and magnetic thermometers used with superconducting quantum interference devices (SQUID's) could be made on the submicrometer scale.

Examples of fields of physics that might benefit from such an approach are superconductors and superfluids at the scale of their respective coherence lengths. The study of the various phases of solid ^{3}He could also be facilitated in this way.

D. MATERIALS SCIENCE

One can foresee a potential coupling between materials research and microstructure fabrication technology in two ways:

1. New materials may possess new and previously unavailable properties of particular use in submicrometer devices.
2. Submicrometer fabrication techniques may open the way to important experimental studies of the intrinsic properties of new systems and materials.

Materials research is broad and underlies much of this report (see Chapter 3). We select some examples because of their special relation to basic research.

Semiconducting and Metallic Polymers

Principal examples of such polymer systems are polythiazyl $(SN)_x$ and its derivatives and polyacetylene $(CH)_x$ and its derivatives. Polythiazyl and its halogen derivatives [e.g., $(SNBr_{0.4})_x$] are anisotropic metallic polymers. Polyacetylene is the simplest possible conjugated organic polymer and is therefore of special fundamental interest. Through chemical doping, the electrical conductivity of films of $(CH)_x$ can be varied over 13 orders of magnitude, ranging from insulator ($\sigma < 10^{-10}\ \Omega^{-1}\ cm^{-1}$) to semiconductor to metal ($\sigma > 2000\ \Omega^{-1}\ cm^{-1}$). Both donors and acceptors can be used to yield n-type and p-type material, respectively.

Currently available $(SN)_x$ crystals consist of microfibrils that are fully oriented in a common-chain direction but are poorly coupled electronically. Gross twinning occurs and about 20 percent of the chains in each microfibril are in defect positions. Polythiazyl can be sublimed and will form thin films on a variety of substrates. Submicrometer film thicknesses are readily achieved. Use of prepared substrates results in aligned (oriented, expitaxial) $(SN)_x$ films with anisotropic optical and electronic properties.

Polyacetylene may be prepared as silvery polycrystalline films by the polymerization of acetylene, C_2H_2, using a Ziegler catalyst. The films may be either free-standing (flexible) or on a variety of substrates. Films have been prepared with thicknesses of less than 10^3 Å. Polyacetylene films consist of randomly oriented fibrils (typical fibril diameter of 200 Å) that are relatively loosely packed; the polymer fibrils fill only about one third of the total volume. The $(CH)_x$ films can be partially chain-aligned by mechanical stretching and may also be doped. Such films exhibit anisotropic electrical and optical properties, with an increase in conductivity in the direction of alignment of up to one order of magnitude. For dopant levels below 1 percent, $(CH)_x$ behaves as a semiconductor; the semiconductor-to-metal transition occurs at a few percent dopant concentration (i.e., at a dopant concentration of a few times 10^{20} per cm^3).

These polymers have unusual electronic properties that may provide specially attractive features for microstructure fabrication. Two of these features are (1) anisotropic optical and electronic properties, that is, quasi-one-dimensional properties, and (2) compatibility with thin-film geometry.

Further, $(SN)_x$ can be sublimed to form oriented films and has highest electronegativity of *any known metal* [$(SN)_x$ halides may be even more electronegative].

For $(CH)_x$, compensation and p-n junction formation have been demonstrated, and the microfibril morphology is, in essence, a synthetic submicrometer array

This list is not comprehensive; however, it does point to some of the special features that may be technologically relevant. For example, the high electronegativity of $(SN)_x$ leads to excellent Schottky barrier formation with large potential barrier heights on simple semiconductors. The large barrier heights lead to small reverse-bias currents, large photovoltaic open-circuit voltages, and the like. Polyacetylene is similarly attractive. It behaves as a semiconductor to relatively high dopant concentrations (approximately 2 orders of magnitude above Si). Thus some of the problems of very small devices (e.g., nonstatistical behavior) can possibly be avoided. The control of electrical conductivity over such a wide range coupled with the unique aspects of polymer processing make this an attractive class of materials.

Although the optical and electronic properties are attractive, detailed experimental studies are hampered by the morphology of these polymers. The microfibrilar structure makes evaluation and subsequent understanding of *intrinsic* properties difficult. Submicrometer structures can potentially offer a great deal in this regard; for example, it may be possible to study the transport on individual fibrils of $(SN)_x$, $(CH)_x$, and other materials as a function of temperature, dopant concentration, and pressure.

Such utilization of microstructures can be more widely applied in materials science. Progress in quasi-one-dimen-

sional conductors is often limited by the difficulties of crystal growth. In particular, the efforts of a lengthy synthesis program may result in a new compound to be evaluated and characterized by a variety of techniques. The current status of the field is such that basic knowledge and intuition do not guarantee that such a newly synthesized compound will be of special interest. Submicrometer structures offer a possible set of tools for making measurements on extremely small crystals. The resulting information would provide guidance for further synthesis, ultimately leading to new materials with more desirable properties.

Molecular-Beam Epitaxy

The increasing use of molecular-beam epitaxy (MBE) for fabrication of optical devices is well known and is illustrated by the Au–GaAs Schottky diodes discussed in Section F. However, the latest efforts have produced materials with extremely high electron mobilities by modulated doping of semiconductor heterojunction superlattices of GaAs–$Al_xGa_{1-x}As$. The Si donors are placed in the wider bandgap material, $Al_xGa_{1-x}As$, while the electrons move in the GaAs layers, thus greatly reducing impurity scattering. With this technique, room-temperature mobilities a factor of 2 higher than for bulk GaAs have been obtained; several orders of magnitude can be gained at low temperatures. This work illustrates the importance of exploring further MBE as a means of preparing novel materials for microstructure work.

Interface Problems and Solid-State Reactions

The interfaces in MOS structures play a critical role. The shrinking of some of the dimensions but not others in such structures aggravates some problems and creates new ones.

Although recent work indicates the possibility of producing thin oxides that have "normal" characteristics, as deduced from tunneling and conductance measurements, it is not certain what failure mechanisms will dominate and, hence, what failure rate will ensue for thin oxides.

One particular class of problems that is magnified at small dimensions is contact effects. One always has the problem of voltage drops across contacts, which will become more critical as device size decreases. However, the most critical problem will probably be associated with strain. The strain region between a doped/implanted region and a "pure" region does not scale down. Strain-aided solid-state diffusion is a potential problem.

Normal scaling considerations point out the critical need for control of interface charge, which controls threshold. One cannot have such variations in magnitude as are tolerated in devices operating at higher voltages. The effect of thin oxides on threshold variation has not been studied.

Surface-Related Phenomena

The ability to control structure and composition on a scale of 50–100 Å would make possible studies of some important problems in catalysis.

1. One such problem is that of structure-sensitive reactions. The activity of some catalysts, with respect to certain reactions, depends only on the total number of sites. These reactions are called "structure insensitive" or "facile." Other reactions, termed "structure-sensitive" or "demanding," depend on the structure of the catalyst, as revealed by studies of the influence of particle size.
2. A second problem is the role of catalyst support. The choice of catalyst support is known to affect catalytic activity, but the reasons are not understood.

Surface diffusion is a basic step in a number of surface processes, such as surface chemical reactions, segregation, and oxidation. Hardly any quantitative measurements of diffusion rates have been made (except for some metal–metal studies). A surface with a known initial concentration profile (e.g., "sawtooth") would permit investigations of these rates.

Microfabrication may also have a wide impact in the science of crystal growth. Two examples are: it can supply a means of probing the electrical properties of small crystallites; it can be used to establish small lateral dimensions, which can be used to probe the detailed nature of the growth mechanisms themselves.

E. SHORT-WAVELENGTH SPECTROSCOPY AND MICROSCOPY

The use of electron and x-ray beams for lithography is discussed in Chapter 4. Here we address only the interplay between electron microscopy and x-ray techniques and microfabrication.

Electron microscopes are reaching the level of individual-atom resolution; the development of these microscopes served as the basis for the development of the lithographic machines currently in use and those anticipated. With such microscopes, one would like to do a wide variety of elastic and inelastic experiments that involve energy loss, Auger spectroscopy, or simply small-angle scattering. For this purpose, there is a definite need for solid-state detectors of the type discussed in Section F. Electron scattering requires a large dynamic range, which currently available detectors do not have. Whether such detectors could be used with a phosphor depends on their damage characteristics, but, if possible, they would offer advantages in resolution and readout. There is essentially no major effort in the United States to develop such detectors for this purpose.

Such detectors are also applicable in x-ray physics. More importantly, microfabrication is necessary for the development of grating monochromators and focusing Fresnel zone plates. Considerable effort is going into the development of zone plates for imaging of laser fusion implosions, with the goal of attaining the 0.1-μm scale with extremely high-aspect ratios for a good lens. In designing gratings particularly for the soft x-ray regime, the wavelength and grating scales should be comparable.

With the development of synchrotron-radiation sources, these x-ray devices will become more important. At the

same time, such sources make possible investigations in lithography, topography, holography, and the many conventional techniques that will have a major impact on microstructure technology.

F. ASTROPHYSICS

Starting with optical astronomy and proceeding into the modern era with radio and x-ray astronomy, astrophysics has advanced through the introduction of new types of detection systems. Advances have been made by improving substantially on resolution and sensitivity in those regions of the spectrum previously explored or by developing new capabilities for observation at previously unexplored wavelengths. Currently, microfabrication techniques are contributing to both types of improvements through the development of charge-coupled device (CCD) imaging arrays for the visible region of the spectrum and advances in fabrication of small Schottky diodes and superconducting tunnel junctions.

The current status of detection systems in the visible region of the spectrum has been reviewed recently. For the past several years, integrated linear silicon diode arrays have been available. These arrays are geometrically stable and simple to use, have high-resistive quantum efficiency and good dynamic range, and are almost free of "cross-talk" between adjacent elements. The amplifier noise limit is about 1000 electrons, which limits the use of the arrays to relatively bright objects or long integration times.

A CCD detector with 400 x 400 pixels, in which the silicon chip is thinned to a 10-μm thickness and illuminated from the reverse side, has been developed. In tests, the on-chip amplifier achieved a readout noise of 15 electrons per pixel. These detectors have a dynamic range of approximately 2500 and excellent linearity. They are likely to create a new area in optical astronomy because their sensitivity and range will allow the observation of faint objects previously inaccessible.

The development of such detectors, regarded as "ultimate astrophysics detectors," has come about through Department of Defense and National Aeronautics and Space Administration contracts, thus progress in this field has been dependent on government contracts to private industry. Further developments should lead to 800 x 800 and even larger arrays in the next few years.

In the submillimeter region of the spectrum, good detectors are not currently available, since the RC of most detectors limits the frequency to less than 10^{11} Hz. Since the capacitance is directly proportional to the area, microstructure fabrication offers an opportunity to reduce the capacitance of such devices. The current state-of-the-art devices are GaAs-Au Schottky diodes with ~1-μm dimensions, operating near 10^{11} Hz, with noise temperatures in the range of 300–500 K, and superconducting tunnel junctions, ~0.4 μm^2, used as mixers at 110 GHz, with noise temperatures of about 230 K. Much work needs to be done to improve the stability of these devices and to increase the operating frequency by reducing their area. Few or no astronomical observations have been carried out in this region of the spectrum because of the lack of such detectors. In the past, the opening of previously unexplored regions of the spectrum led to major advances in understanding of the universe. There is every reason to expect that this will be true of the submillimeter region.

G. BIOPHYSICS AND MEDICINE

To accomplish something directly beneficial to human beings is often a stronger motivation than attempting to roll back the frontiers of science or develop a technology that will eventually improve life for mankind. Thus it is somewhat easier to consider applications of microstructures in biophysics and medicine than in physical and materials sciences. The following examples are more speculative than the suggestions offered in previous sections.

Microstructures and Nerves

When we consider that normal human nerve cell size is many cubic micrometers, and that individual memory cells can be packed on a scale that is small compared to nerve cells, we begin to feel that perhaps we can develop means to improve local nerve behavior or even to replace defective nerve tissue. There is still an interface problem, of course. In all likelihood, we can find an algorithm to do the logic for the interfacing, to determine what kind of stimulation is necessary as well as where it is necessary. Obviously, we must ensure that the physical structure remains operable within the body.

Internal Monitors

With the decrease in size of circuits, it might be possible to make sensors and transmitters so small that not only could they be swallowed without problems but they might be inserted in particular portions of the circulatory system, with provision for readout of information. More generally, we can contemplate using such ultraminiaturized devices to do more testing and monitoring for individuals. This development would probably come about not so much from smaller devices as from decreases in cost, so that health care could be made more nearly universal.

Appendix:
Technical Contributions

This Appendix of technical contributions follows the general format of Sections C and D of Chapter 3 and provides in-depth discussion of several topics shown in Table 3.1 of Section C. These technical contributions were prepared by experts selected from university, government, and industrial laboratories. Their contributions, together with those of the members of the Subpanel on Materials Aspects of Microfabrication, underlie the conclusions stated in Sections B and C of Chapter 3.

CONTENTS

Etching and Deposition of Very Small Structures

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Microstructure Fabrication

Etching and Deposition of Very Small Structures

1.0 Introduction and Status

Future designs in microfabrication for semiconductor circuits will require etching and/or deposition of very small structures In today's technology we can etch and deposit in submicron geometries[1,,5] however, the controlling mechanisms are not well understood, if at all. Anisotropic or orientation dependent etching (ODE) is being widely used in today's processing of Dielectric Isolation structures[2] CMOS and VMOS structures[3], vertical MOSFET structures[4], etc., Vertical Multiple Junction solar cells have also been produced by ODE and ODD (orientation dependent deposition) having over one thousand junction per centimeter[5]. ODE is also used in the processing of electronic printerheads[6] which must be electrically, thermally and mechanically stable, and in the ink jet printer heads[7]. Etch ratios of over six hundred to one (600 to 1) have been reported in ODE of (110) silicon, that is >600 times faster in the <110> direction than in the <111> direction[1]. Very high packing densities can also be achieved by use on dielectric isolation in (100) silicon. Submicron structures have been etched in (110) silicon with excellent reproduction[1]. Figure 1 is a 5000 x 80° SEM showing a crosssectioned (110) silicon slice with 0.6 μm ridges on 1.2 μm centers. The sidewalls of these ridges are (111) orientation. These (111) sidewall surfaces can be diffused by conventional diffusion techniques, and oxidized by conventional oxidation processes. However, patterning in these structures has not yet been developed to any degree.

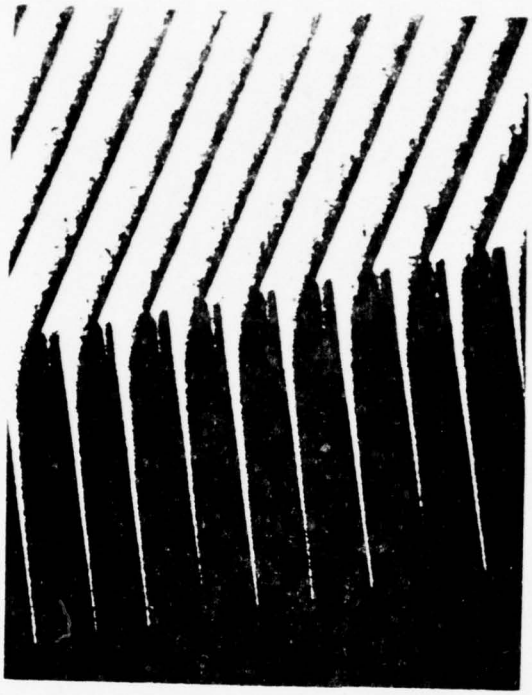

Figure 1. 5000X SEM 80° of 0.6 μm ridges on 1.2 μm centers etched in (110) silicon

The ridges can be pointed to form a black body structure (see Figure 2) and of course, they can be tilted with respect to the surface. Tilting as much as 16° off has been achieved. Figure 3 is a 250X SEM cross-sectional view of a (110) ODE structure. The surface is tilted 10° off the <110> direction.

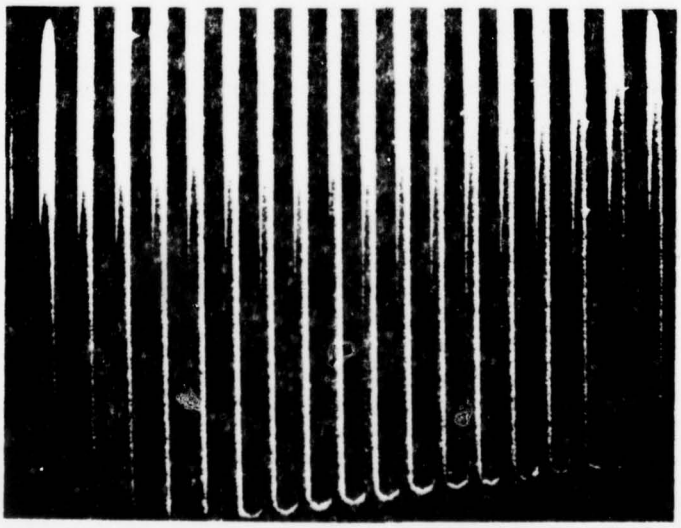

Figure 2. 600X 68° SEM pointed ridges

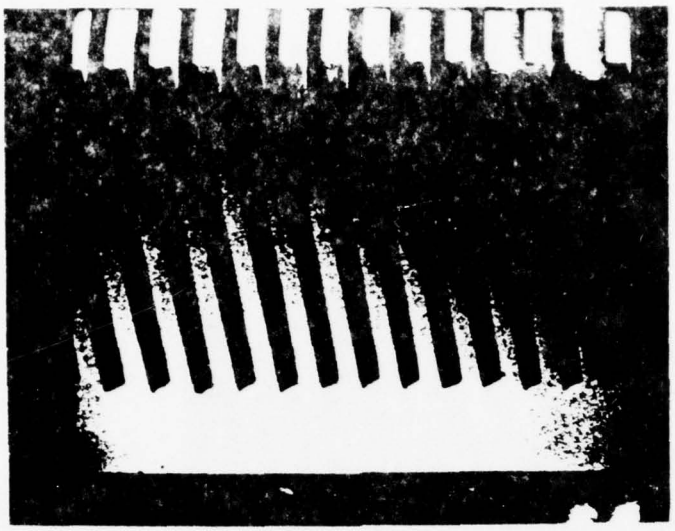

Figure 3. 250 SEM cross-sectional view of (110) off orientation ODE 160 μm deep

The very large gain in surface (available device) area is readily evident from these photographs. For example, if one opens up a 1 μm wide line in the mask and etches 200 μm (8 mils) deep into the slice one obtains a 400 to 1 gain in surface area. (110) silicon slices can readily be etched completely through from one side or with simultaneous etching from both sides to form lines of moats and ridges or X-Y grids. See Reference (1) for details. The moats and ridges offer many possibilities in large area capacitors, high voltage diode arrays, solar cells, optical gratings, etc., while the X-Y grid offers potential in addressing structures very fine sieves, shadow masks, etc.

Another emerging technology is that of concentration dependent etching (CDE). Some etches, for example 1-3-8 [1 part HF, (hydrofluoric) 3 parts HNO_3 (nitric) and 8 parts CH_3COOH(Acetic)] etch P+ or N+ ($\gtrsim 5 \times 10^{18}$) but practically stop etching at an abrupt P-, or N- junction, or interface. The opposite effect is observed, and used, in the case of the ODE used for (100) silicon. This

CHEMICAL ETCHING OF SILICON

ETCHES	CHARACTERISTICS	COMPOSITION	RATE AND REMARKS
Planar Etch	Etch Uniformity	HF - HNO_3 - HAc ~8% ~75% ~17%	~5 μ/min (111) RT
Dash Etch 1-3-8 1-3-10	Etches P^+ or N^+ Silicon "Stops" at P- or N-	HF HNO_3 HAc 1 3 8	~3 μ/min (100) RT
ODE (100)	Etches [100]~100 x [111] direction	KOH - Normal Propanol H_2O	~1 μ/min at 80°C in (100) silicon stops at P^{++} interface
ODE (110)	Etches [110]600 x [111] direction	KOH - H_2O	~.8 μ/min at 80°C in (110) silicon
ODE Ethylenediamine	Orientation dependent and concentration dependent	Ethylenediamine -Catechol - H_2O (Hydrazine)	~1.1 μ/min at 100°C in [100]. Stops etching at P^{++} interface. Very slow etching of SiO_2

Table 1. Chemical Etching of Silicon

etch (KOH, normal propanol and H_2O) stops etching at a P+ interface. Table 1 lists some of the orientation dependent etches, and some concentration dependent etches as well as planar etch.

The deep grooves, as shown in Figure 1 can be filled to a planar surface by selective epitaxial deposition[5]. Selective epitaxial deposition can be accomplished by using the proper masking materials and mask to open silicon geometries. See references 1 and 2 and Figure 4. Figure 4 shows selective deposition of (100) silicon.

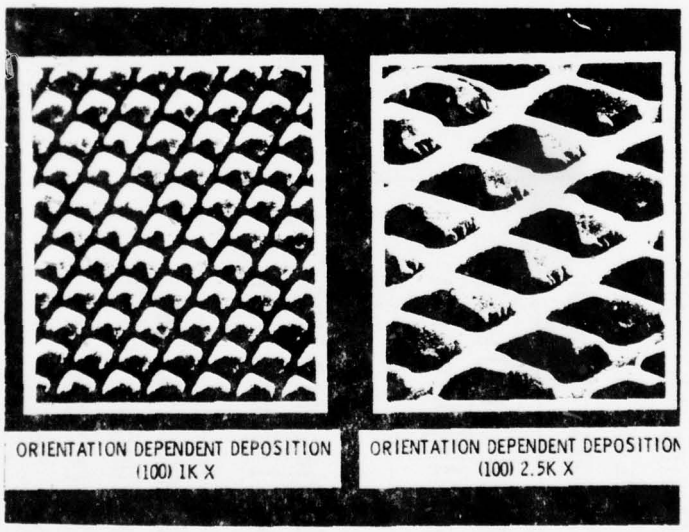

Figure 4

The mask is 5 μm diameter opening on 20 μm centers. Note the (100) square fourfold symmetry development through the round mask opening. The "epi tops" have grown laterally over the mask from the original 5 μm diameter to 13 μm x 13 μm squares. In this device there can be no spurious nucleation of silicon on the mask, which would bridge the structures.

Figure 5 is a 3000X magnification, SEM of selective epitaxial deposition of (111) silicon using the same mask as in Figure 4. Note the oxide mask and "Epi Top" breakage along the cleaved edge. The original unmasked diameter is evident as is the mask thickness. Also note the area of silicon-oxide interface reaction under the silicon overgrowth. This can be eliminated or altered by use of silicon nitride masking.

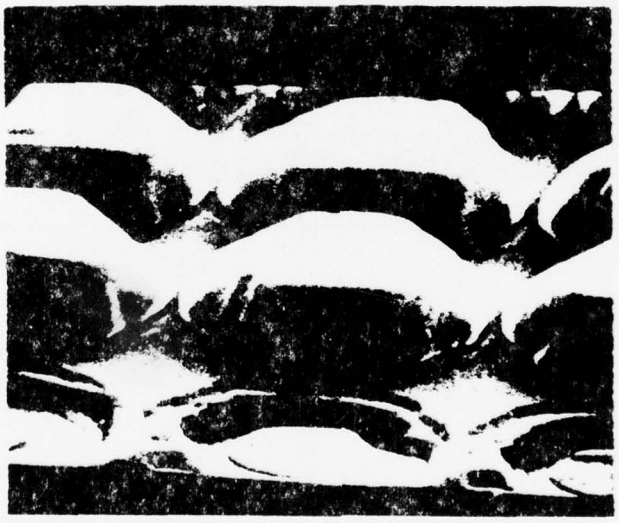

Figure 5. 3000X SEM. (111) Preferential Orientation Dependent Epitaxial Deposition of Silicon

Figure 6 is a 3000X cross-sectional view of such a structure as in Figure 5 above, after oxide etch to remove the mask.

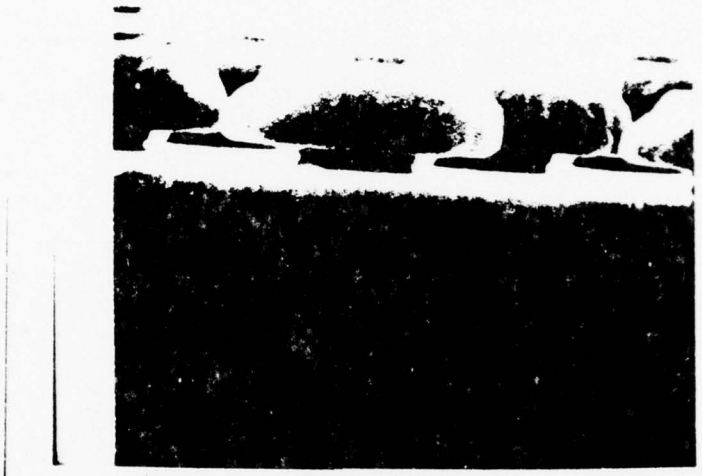

Figure 6. 3000X SEM. (111) Preferential Orientation Dependent Epitaxial Deposition of Silicon

2.0 Technological Needs

A thorough understanding of the mechanics of silicon etching is required for orietnation dependent etching and for concentration and/or type dependent etching. Some of these are related to ionic properties while others may be related to lattice packing densities and some may be effected by atomic or lattice stress or damage (due to doping concentration). At present it is difficult if not impossible to predict the effect a particular etch solution will have at a silicon crystal interface concentration gradient or P-N junction.

Studies need to be made to understand (1) the etching mechanisms, (2) the byproduct of etching reactions, (3) the effects of these byproducts on etch rate, (4) the possible process contaminations in device processing, and (5) the effect on masking materials.

3.0 Potential Impact

The potential impact is very diverse in not only the Electronic Semiconductor field but in the fields of energy converters; biomedical instruments; body fluid, chemical, gaseous and solid sieves; dangerous gas or pollution detectors; micromachining and others.

4.0 Opportunities to University, Government and Industry

- The above technology requirements offer many new, challenging and potentially revolutionary studies for graduate student thesis programs.
- These technology programs offer areas wherein support can be offered from industry or government to universities for potentially revolutionary but high-risk programs.

- o The opportunity for government, industrial and university working agreement are presented in these technology requirements.
- o New technology fields are offered to universities , industrial and government laboratories.
- o New and advanced product fields are offered to industry.
- o New instrumentation and products are potentially available for biomedical fields merging university, industrial and governmental interests.

4.1 Specific Topics for Investigation

I. (1) Define etching mechanism for 1-3-8 etch on silicon.

(2) Is the mechanism controlled by ionic or damage properties?

(3) Why does it attack N+ or P+ silicon and stop at N- or P- interface or junction?

(4) What is the effect of a P+, N- junction over that of a P+ P- interface or N+ N- interface?

II. (1) Define etching mechanism of KoH propanol and water edch.

(2) Why is it anisotropic with respect to crystal orientation?

(3) Why does it etch P- or N- and stop at a P+ interface or junction?

(4) Why is this etch both orientation and type concentration dependent?

III. (1) What is the etch mechanism of the Ethylenediamin-Pyrocatechol-H_2O etch?

(2) Why does the addition of hydrozine speed the etching rate so drastically?

(3) Why is the etch orientation dependent?

(4) Why is the etch concentration dependent?

IV. (1) What is the etching mechanism of KOH-H_2O?

(2) Why is it so highly orientation dependent, for example 650 to 1 in the <110> direction vs the <111> direction?

(3) Why is it not concentration dependent as the KOH-Propanol and H_2O is?

V. (1) What is the mechanism for silicon atom mobility in preferential or selective epitaxial deposition? What is the optimum silicon halide to use? It is known that $SiCHl_3$ is better than SiH_2Cl_2 or $SiCl_4$. Why? It is also known that even SiH4 has some degree of silicon mobility even though literature reports none.

(2) What is the optimum mask material?

(3) What are the optimum deposition conditions?

(4) What is the optimum mask area to open silicon area and geometries?

(5) What is the effect of the chlorine molecule on silicon atom mobility or transport?

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TECHNIQUES FOR GROWTH AND CHARACTERIZATION OF THIN FILMS

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1. INTRODUCTION (SCOPE)

The preparation and characterization of thin epitaxial semiconductor layers and thin metallic and insulating films is a very important aspect of the development and extension of the limits of ultraminiaturization. This is true especially for the future utilization of compound semiconductors which are already achieving dominance in the field of low noise microwave FET amplifiers. Further extension of submicron technology in these materials will require more development of the various growth techniques as well as development of the methods of characterizing the very thin layers required for some submicron device applications. This report

summarizes the current status of the work in academic, governmental and industrial research laboratories and attempts to point out the areas where additional research is essential for continued progress towards ultraminiaturization. Finally, the possible impact of the anticipated research results on other fields of work is discussed and research areas particularly suitable to university and industrial study are suggested. The needs relative to silicon and silicon integrated circuits are not considered because (1) the wide industrial and commercial interest in this area insure adequate--at least much more than can be provided by governmental agencies--support for applied research, and (2) university laboratories are not generally equipped to contribute to state-of-the-art silicon technology. The long term potential of compound semiconductors justifies governmental support of research, with uncertain but possibly great rewards, that would not be adequately supported by industry.

2. EPITAXIAL GROWTH TECHNIQUES

2.0 Introduction

The primary techniques used in the growth of epitaxial semiconductor layers are liquid phase epitaxial (LPE) growth, vapor phase epitaxial (VPE) growth, molecular beam epitaxial (MBE) growth, and metalorganic chemical vapor deposition (MO-CVD). Although the last two growth methods can technically be classed as VPE, they are so much different from earlier methods of VPE growth it is best to retain the special terms MBE and MO-CVD. In this section the current status of the various growth techniques will be briefly summarized. A final topic is the importance and status of the substrates required for the growth of high quality epitaxial layers.

2.1 Liquid Phase Epitaxy

2.1.0 Current Status. The prototype of the LPE method of crystal growth was the system described by Nelson[1] for the growth of GaAs. In the application of the LPE growth technique to GaAs, a Ga solution at an elevated temperature is saturated with GaAs. The epitaxial growth occurs when the growth solution is moved over a GaAs substrate and the temperature of the growth solution is lowered to induce supersaturation of the solution and epitaxial growth on the substrate. If Al is introduced into the growth solution, the epitaxial layer that is grown is $Al_xGa_{1-x}As$,[2] and a heterostructure results between the $Al_xGa_{1-x}As$ and the GaAs substrate. Until recently, LPE has been the best technique for the growth of $Al_xGa_{1-x}As$-GaAs heterostructures, and it has been particularly important for the fabrication of diode lasers in this materials system. This growth technique and its application to simiconductor lasers utilizaing multiple-well graphite slider boats for the growth of complex device structures has been reviewed in detail by Kressel and Butler[3] and Casey and Panish.[4] The LPE growth technique has been used for many materials besides $Al_xGa_{1-x}As$ and GaAs, and an extensive list of references is given in References 3 and 4. The LPE growth technique has also been used for the growth of variable-bandgap lattice-matched heterojunctions of the quaternary alloy $In_{1-x}Ga_xAs_{1-y}P_y$. Further developments of this growth technique for applications of InGaAsP in emitters and detectors for optical fiber transmission system and microwave devices will be important. (Note: The quaternary InGaPAs is used also for visible spectrum emitters.)

Compared to the other methods of epitaxial growth LPE has certain disadvantages, such as poorer control of layer thickness, problems with poorer surface

morphology including growth terraces and meniscus lines and less flexible control of crystal composition in the growth of alloys. However, there are particular advantages associated with the LPE growth technique that make it an attractive technique for further study. It is relatively inexpensive to set up an LPE growth system and this makes it ideal for laboratory scale experiments, but it is also capable of some results that cannot be obtained with the other growth techniques. An example of this is the use of the amphoteric dopants Si and Ge to obtain p-n junctions with both p and n sides of the junction doped with the same impurity. Under most growth conditions, both Si and Ge tend to preferentially locate on the Column III sites (Ga) and act as shallow donors. However, in the LPE growth technique because of the large concentration of Ga atoms in the growth solutions there is a tendency for more As vacancies and thus, for certain growth conditions (temperatures) the dopants Si and Ge will occupy the Column V lattice sites and act as acceptors.[5] It is probable that the Column IV atoms acting as acceptors may be incorporated both in a vacancy complex, and as a simple substitutional acceptor.[6] In fact, Si introduces at least two acceptor levels, with the shallower level presumably due to a simple substitutional acceptor and the deeper level due to a vacancy complex. So far, it has not been possible to obtain p-type doping with Ge and Si using the other VPE growth techniques. (P-type doping can be obtained with Ge in MBE growth, but the minority carrier diffusion lengths are much lower than in p-type Ge-doped LPE material.)

Relatively high-purity GaAs has been prepared by LPE growth techniques (see Wolfe and Stillman, Ref.7, for a review of results for high purity GaAs) and more recently, Morkoç and Eastman[8] have shown that the multiple-well slider boat growth technique that is so important for the growth of multiple layer heterostructures can also be used for the LPE growth of high purity GaAs. More recently, Ip, Eastman, and Wrick[9] have shown that similar techniques can be used for the growth of high purity InP.

2.1.1 Major Problems. The major problems related to the LPE growth of thin films in general are the accurate control of thickness, the control of surface morphology, and the uniformity and control of doping in the epitaxial layers. All of these problems are related to the transport rates of the minority components from the bulk of the growth solution to the substrates - growth solution interface. It is now well known that for accurate control of layer thickness and for layer uniformity it is essential that this transport occur only by diffusion. Any convection in the growth solution will produce generally thick and non-uniform layers, and must therefore be avoided. This places severe requirements on the temperature uniformity, boat design, melt height, etc.

In particular applications of LPE growth, such as to the quaternary alloy InGaAsP there are additional problems that need to be resolved. With this material, any change in the composition of the epitaxial layer will result in a lattice mismatch heterojunction, instead of just a slightly different bandgap that would result for AlGaAs, and the mismatch will certainly cause poor device reliability and/or performance.

2.2 Vapor Phase Epitaxy

2.2.0 Current Status. The vapor phase epitaxial growth technique is the most widely used method for the growth of GaAs, GaAsP, GaP, InP, and Si epitaxial layers. This process generally provides layers with good surface morphology and few surface defects compared to LPE layers. The melt wipe-off problems and meniscus line defects and terraces that pose some of the major problems in LPE are non-existent

in VPE growth. The thickness of the layers can be accurately controlled and the doping can be easily adjusted in comparison with LPE techniques. In the growth of alloys using VPE it is much easier to grade or change the alloy compositions than in LPE and thus for applications where heterojunction effects (i.e., abrupt transitions) are not utilized, the requirement of accurate lattice matching between the substrate and the ternary of the desired composition can be bypassed. For example, good quality $GaAs_{0.6}P_{0.4}$ layers for LED applications can be grown by grading either from GaAs or GaP to the desired composition for growth on GaAs or GaP substrates respectively.

There are two different vapor phase growth process that are widely used. These are generally described as the "chloride process", which utilizes $AsCl_3$ or PCl_3 as the As and P sources for the growth of III-V compounds incorporating these elements, and the "hydride process" which utilizes AsH_3 and PH_3 as the As and P sources. In both growth techniques, the column III elements, such as Ga and In are transported by an HCl reaction. In the chloride process the HCl is generated from the $AsCl_3$ or PCl_3 while for the hydride process, high purity HCl must be separately supplied.

The status of the chloride or $AsCl_3$-Ga-H_2 VPE technique for high purity GaAs as of 1970 is reviewed in Ref.7, and the current status relative to purity is essentially unchanged. However, there have been significant developments in this growth technique relative to the control of doping profiles, abrupt substrate-epitaxial layer interfaces, etc. All of these developments have resulted because of their importance for particular device applications. This growth technique is also the one that has been most effective in the growth of high purity InP, but it has recently been pointed out[10] that the standard chloride process does not permit wide variation of the growth parameters that which may be essential to obtain material with the best electrical properties.

The hydride growth technique which was first described by Ruehrwein[11] is the system most widely used for the large scale commercial growth of $GaAs_{1-x}P_x$ for LED applications[12,13] and is also the one developed by RCA for the growth of a large number of III-V compounds and alloys.[14] The chemical processes in the hydride growth technique are described in detail in Ref.15. This growth technique is particularly well suited to the growth of alloys, and RCA has recently reported CW lasers in VPE InGaAsP grown using this process.[16] The purity of GaAs and InP epitaxial layers grown with this technique is not as high as that of similar layers grown using the chloride process, however. Although reasonably high purity has been achieved in the growth of GaAs,[17] these results were not generally reproducible, and in spite of "rumors" of high purity GaAs (i.e., $\mu_{77} \geq 200{,}000$ $cm^2/V\text{-sec}$) from several industrial laboratories using this process there has been no published report of these results. There are very few published results for InP grown with the hydride system, and in fact very complicated modifications have been made to the chloride system to attain the capability of wide variation of the growth conditions while retaining the advantage of the higher purity starting materials in the chloride process.[10] Thus it is clear that the current status of the purity of materials grown by the hydride growth technique is not as good as that of the chloride process. However, the purity may be adequate for many applications and the hydride system makes it relatively easy to vary the growth conditions. Also, it should be remembered that not nearly as much effort has been expended in growth of high purity material with the hydride system.

2.2.1 Major Problems. There are several problems in the VPE growth process that, if solved, could make material grown by this method very suitable for appli-

cations in submicron ultraminiaturized devices. The chloride growth system is adequate for many applications, but the possibility of controlling the growth conditions by simply controlling the gas flows makes the hydride system of particular interest for ternary and quaternary applications and for the VPE growth of heterojunctions. For many applications, the purity that can be obtained with the presently available starting materials and gases is adequate, but for others, such as FET buffer layers or buffer layer for integrated circuits much better control of the purity is needed. Not only do higher purity gases need to be developed, but also, the best means of cleaning the storage tanks and keeping the gases pure needs to be developed. For applications in high speed ultra-miniaturized integrated circuits, the best developed compound semiconductor material is GaAs. However, there are indications that InP could hold the potential of even higher speeds of operation in these circuits, and development of InP should be continued in parallel with GaAs. It is not to late for InP to be considered for the basic ultra high speed microminiaturized integrated circuit material if discrete results indicate that InP has superior properties.

2.3. Molecular Beam Epitaxy

2.3.0 Current Status. Another type of VPE has been studied extensively since about 1970. This technique is essentially the evaporation of elemental components onto a heated single crystal substrate, but to emphasize the control of the crystal composition this growth method has been called molecular beam epitaxy (MBE). This technique consists of directing controlled "beams" of the required atoms from effusion-cell ovens, that can be shuttered to change from the growth of one type of crystal to another, toward the heated substrate in a vacuum of ~10^{-10}Torr. The technology of this technique has recently been extensively reviewed.[18,19] The MBE growth rate is relatively low (~60-600 Å/min) and this permits precise control of the thickness of the epitaxial layers. This capability may be the most important feature of MBE. In fact, it is possible to grow AlAs and GaAs in alternate monolayers and this capability may permit the growth of structures with particular transport properties. MBE systems are commercially marketed by several companies, Varian and Physical Electronics (in the U.S.), Riber (France), Vacuum Generator (England), and Niva (Japan). Probably the most important advantage of the MBE growth technique is that it is possible to do many different types of *in situ* analyses during the actual growth of the epitaxial layers, and most of the commercial MBE growth systems include reflection electron diffraction equipment, a mass spectrometer, and an Auger spectrometer with ion sputtering capability. Although ultra-high vacuum is required, most of the commercial systems also incorporate a sample-exchange interlock so that atmospheric contamination of the growth chamber is prevented and rapid sample exchange can be accomplished. Most of the work on MBE has been directed toward GaAs and AlGaAs and good electrical properties have been obtained. However, although room temperature CW lasers have been fabricated from MBE material, the radiative efficiency of MBE material does not seem to be as high as that of LPE and VPE material, possibly because of nonradiative recombination at native defects. There have been some reported MBE results for InP but P is generally much more difficult to work with in MBE systems because of the low sticking coefficient of this material and the resulting necessity for high P fluxes.

Because of the capability of the accurate control of extremely thin epitaxial layers, including the fabrication of new structures involving monolayers, and because of the capability of studying the crystal as it grows *in situ*, it is likely that this growth technique will become more and more important, especially for applications in submicron ultraminiaturization when extremely good surface morphology will be required.

2.3.1 Major Problems. Although the general techniques for MBE growth of GaAs and AlGaAs have been developed over the past few years, many fundamental areas that will be important for applications of MBE material in submicron circuits and devices need to examined. Fundamental basic research needs to be done on the atomic nucleation process, on the elemental sticking probabilities of the primary atomic species as well as of dopant impurities, and on the actual atomic crystal growth process. The interdiffusion effects of the primary atoms as well as of the dopant impurities need to be studied because small amounts of diffusion could be very critical in submicron (10-100 Å) layers that can be controllably grown using MBE. The defects that are introduced during growth also need to be characterized since little is known about the defects that, for example, are responsible for the low radiative recombination efficiency characteristic of most MBE material.

It has been demonstrated that alternate monolayers of GaAs-AlAs can be grown using the MBE technique, so this growth technique should permit the study of really abrupt heterojunctions of these materials. The energy band discontinuities and interface recombination velocities of this material should be thoroughly characterized for their effect on possible device applications, particularly with regard to ultraminiaturization.

In addition to these problems related to GaAs and AlGaAs, the same problems need to be considered for other important compound semiconductor alloys--particularly those containing P. The kinetics and energetics of P incorporation during growth of both GaAs and InP substrates should be examined in detail.

2.4. Metalorganic Chemical Vapor Deposition

2.4.0 Current Status. The most recently developed technique for the growth of epitaxial films is the metalorganic chemical vapor deposition (MO-CVD) technique, and for many applications it is potentially the most useful. This growth technique is the one that is most successful for the growth of III-V compounds on sapphire and spinel oxide substrates and was initially developed for this purpose, but even more importantly, it permits the VPE growth of $Al_xGa_{1-x}As$. This material cannot be grown by any of the other VPE techniques, except MBE, and because of its usefulness for many lattice-matched heterojunction devices, MO-CVD will be particularly important for the growth of this material for submicron ultraminaturization applications where the surface morphology and uniformity obtainable by LPE, at present at least, is not adequate.

The MO-CVD growth technique uses the volatile metalorganic compounds such as triethylgallium, trimethylgallium and trimethylaluminum as the source of Ga and Al and AsH_3 as the source of As. Although early results using MO-CVD were not particularly promising because of heavy compensation and poor minority carrier properties,[20] relatively uncompensated material with good optical properties can now be grown, and CW room temperature AlGaAs-GaAs double heterostructure lasers with thresholds and efficiences as good or better than those obtained by LPE techniques have been reported.[21] Other results by Dupuis and Dapkus and Holonyak and coworkers[22] indicate that very uniform, thin (~50 Å), single and multiple (up to ~50) epitaxial layers can be grown using this technique, and these structures may be particularly useful in submicron ultraminiaturized circuits and devices. Relatively high purity GaAs has been obtained with the MO-CVD technique using specially purified triethylgallium. The carrier concentrations were in the $<10^{14}cm^{-3}$ range and the maximum liquid nitrogen mobility was $120{,}000 cm^2/V\text{-}sec$.[23] With ordinary sources of trimethylgallium the purity is not as high, and there is also the possibility that the carbon which is part of the metalorganic sources may also be a

source of compensation since photoluminescence studies have identified C-acceptors in MO-CVD GaAs. Although the purity of MO-CVD material is primarily limited by the purity of the source materials, it is possible to adjust the growth conditions, such as the III-V ratio, so that quite high resistivity, low carrier concentration material is obtained.

2.4.1 Major Problems. The recent outstanding results of MO-CVD AlGaAs-GaAs heterojunction diode lasers by Dupuis are proof of the potential of this growth technique for AlGaAs, but there are many details in the growth process and in the materials characterization that need to be studied. The MO-CVD growth system is particularly well suited to varying the gas composition in the growth zone, the the effects on the various material properties need to be determined. The minority carrier diffusion lengths, the majority carrier mobility, and the compensation may be considerably influenced by the growth conditions, and the optimum parameters should be determined to obtain material with the best electrical as well as optical properties. The possibility of using structures consisting of undoped quantum well layers bounded by doped AlGaAs layers grown by MO-CVD for obtaining higher conductivity material has been suggested by Dapkus (and recently reported for MBE layers) and this possibility should be thoroughly investigated. Although the purity of presently available metalorganic compounds appears to be adequate for laser diode photocell and similar applications, better control of purity may be required for FET and other microwave devices and it is important that work be done to purify the metalorganic sources.

Other areas that need to be studied further in much more detail include the MO-CVD of phosphorous compounds. There is some industrial work on this topic in France as well as in this country, and the capability of growing InP, and in particular the quaternary alloy InGaAsP, could have far reaching implications for many optical and microwave devices and for applications in ultraminiaturization.

2.5 Substrate Material

2.5.0 Current Status. For all of the epitaxial growth techniques described in the previous sections, suitable substrates are essential. Low dislocation density, uniformly doped low resistivity epitaxial material is required for many device applications such as lasers and detectors, and high quality semi-insulating substrates, also with low dislocation densities are required for FET and planar integrated circuit applications. Satisfactory conducting GaAs substrate material can generally be obtained from several suppliers in this country. Although there can be considerable ingot to ingot variation. The availability of satisfactory semi-insulating GaAs material is not so good however, and the properties of each ingot must be evaluated to determine whether it is satisfactory or not. Even when the general properties, such as resistivity, thermal stability, etc., of semi-insulating substrate are satisfactory, there are often problems related to the influence of the Cr-dopant and other impurities on the electrical properties of thin epitaxial layers grown on these substrates.[24] However, the feasibility of growing essentially intrinsic VPE ($AsCl_3$-Ga-H_2 technique) GaAs layers on specially qualified Cr-doped substrates has recently been demonstrated by R.D. Fairman of Rockwell International.[25] In a recent potentially very important development, E.N. Swiggard and H. Lessoff of the Naval Research Laboratory[26] have grown unintentionally doped semi-insulating GaAs crystals using the LEC crystal pulling technique and GaAs starting material compounded in pyrolytic boron nitride. This semi-insulating single crystal material has a resistivity greater than 10^7 and is thermally stable. For MSI and LSI GaAs integrated circuits it would be desirable to have substrates of sufficient quality that the devices could be formed directly on the substrate without having to grow an epitaxial layer at all, and this NRL material may be suitable for these applications.

The availability of InP substrate material is not nearly as good as for GaAs, and what is available is very expensive (≥$80 per gram). This limits the research on materials using these substrates, and if the potential of InP and related materials is to be realized, considerable work will have to be done on increasing the quality and availability of InP substrates. In this country, the main work on bulk InP is at Varian Associates (G. Antypas)[27] and the Naval Research Laboratory (R. Henry),[28] and there have been considerable advances in the purity and quality of this material. Fe-doped semi-insulating InP substrates can be grown and the main effort in both conducting and insulating material needs to be directed toward reducing dislocation density, elimination of precipitates, and increasing the purity.

2.5.1 Major Problems. The major problems in GaAs substrates are concerned with semi-insulating material, particularly with the thermal type conversion of this material and with the influence of impurities in the substrate, including Cr, on the properties of epitaxial layers grown on these substrates. The achievement of reliable, semi-insulating substrates without Cr-doping could have important consequences for MSI LSI, and ultraminiaturization possibilities of GaAs. With InP substrates, in addition to the quality of the substrates related to dislocations, precipitates, and other defect, there is the problem of ready availability of reasonably priced material. The development of a ready supply of satisfactory InP material will be of primary importance in realizing the potential of this and related materials such as InGaAsP in optical, microwave, and ultraminiaturization applications.

3. CHARACTERIZATION TECHNIQUES

3.0 Current Status

The characterization techniques for semiconductors are well developed and generally quite well understood. There are numerous review articles on each of the measurements within a general type of characterization technique and often there are reviews of applications of particular techniques to specific semiconductors. In general, for the characterization of thin films for device applications results of several of these techniques will have to be correlated and the actual device performance may also have to be used to characterize the material. A good example of this is the measurements of the noise figure of GaAs FET's to determine the presence and influence traps in the substrates and/or epitaxial buffer layers. The characterization techniques can arbitrarily be divided into the following measurements:

3.0.1 Structural Measurements. These measurements include x-ray determination of crystal structure, lattice mismatch, stress and defects, and SEM (scanning electron microscopy) and TEM (transmission electron microscopy).

3.0.2 Compositional and Chemical Measurements. There are many different instrumental methods that are available for these measurements and the depth to be examined including the resolution required, the number and type of elements to be detected, the required sensitivity, and the cost of the equipment vary widely. The various methods include ESCA(electron spectroscopy for chemical analysis), XPS(x-ray photoelectron spectroscopy), USP (vacuum ultraviolet photoelectron spectroscopy), AES (Auger electron spectroscopy), SAM (scanning Auger microanalysis), SIMS (secondary ion mass spectrometry), IPM (ion-probe microanalysis), EPM (electron-probe microanalysis), ISS (ion scattering spectrometry), SSMS (spark source mass spectrometry), and RBS (Rutherford backscattering spectrometry), and each has particular applications for which it is most useful.[29,30]

3.0.3 Electrical Measurements. The most important electrical characterization method historically is the measurement and analysis of Hall coefficient and resistivity data over a large temperature range. For GaAs, the characterization has been complete enough that it is possible to make an accurate estimate of the donor and acceptor concentrations from a single measurement of the Hall mobility at 77 K.[31] Similar characterization has not been done for InP however. Other methods of electrical characterization suitable for analyzing epitaxial layers include capacitance voltage measurements and analyses, various forms of deep level transient capacitance, thermally stimulated capacitance and current, and finally the measurement of minority carrier diffusion lengths and lifetime. These electrical characterization methods have recently been reviewed by Blood and Orton.[32]

3.0.4 Optical Measurements. Optical methods of semiconductor characterization include simple absorption or transmission measurements for energy gap determination, photoluminescence measurements for acceptor identifications,[33] far-infrared photoconductivity measurements for identification of residual donors,[34] and reflectance measurements for the determination of thin layer thickness and carrier concentrations.[35]

3.1 Major Problems

Most of these characterization techniques described above are very well understood, but there can still be considerable uncertainty and ambiguity in applying them to particular semiconductors. The techniques will need to be refined if they are to be of value in characterizing the very thin layers that will be important in ultraminiaturization where it will be essential to determine not only the structural and electrical properties of ~1000 Å layers and also to evaluate the influence of the substrate-epitaxial layer interface on these properties. Most of these experimental problems are not fundamental however, and they will undoubtedly be solved in the process of characterizing these thin layers. There are some problems that require more theoretical attention, particularly those relating to the interpretation of deep level measurements such as DLTS. The influence of internal electric fields on the properties of the traps and the effects on the experimental data need to be considered. The effect of the deep levels on the minority carrier lifetimes and diffusion lenghts also need to be considered.

4. SCIENTIFIC AND TECHNOLOGICAL NEEDS

The scientific and technological needs in the growth and characterization of thin films have been discussed under the headings "major problems" in the preceding sections. These needs and others outlined in the appropriate references are summarized in terms of basic, applied, and developmental research opportunities in Table 1 on page 10.

5. IMPACT ON OTHER FIELDS

Although the problems and needs discussed above are all directly related to improving our capabilities for microstructure fabrication, the solution of these problems would also have a direct impact on discrete electron devices in microwave systems, fiber-optic transmission systems, high-speed computer systems, and many others.

Table 1. Scientific and Technical Needs in the Growth and Characterization of Thin Films for Microstructure Fabrication

	Basic Research	Applied Research	Development
Crystal growth			
LPE	Kinetic, non-equilibrium effects during growth (substrate orientation effects, doping effects)	Determination of best techniques for growth of constant composition lattice matched quaternary and ternary epitaxial layers High-purity growth techniques for alloys Slow diffusing p-type dopant for abrupt junctions in very thin layers in ternary and quaternary materials other than AlGaAs.	Large area uniform thin layer growth
VPE	Influence of gas composition (III-V ratio, unreacted HCl, etc) on crystal properties	High-purity hydride grown GaAs, InP, and alloys Residual impurities in hydride and chloride growth processes	High-purity source and transport gases- AsH_3, PH_3, HCl. Methods of handling gases to maintain purity
MBE	Atomic nucleation processes Sticking probabilities of primary atomic species and dopant atoms	Interdiffusion effects in submicron layers Origin and type of defects limiting radiative efficiency, and effect of growth parameters on these defects. Effectiveness of special structures such as super-lattices, alternate doped and undoped layers, on transport and optical properties Study of atomically abrupt interfaces Growth of phosphorous compounds such as InP, InGaAsP	Evaluation of optical and microwave devices, reliability, noise, etc., as a means of characterizing MBE material
MO-CVD	Determination of thermodynamics of MO-CVD system	Influence of growth conditions on minority carrier diffusion lengths, mobility, etc. Residual impurities in MO-CVD material Mobility in special structures such as alternate doped and undoped layers Optical properties and potential of multiple quantum well structures Influence, if any, of carbon on electrical and optical properties Abruptness of n-n and p-n heterojunctions Evaluation of low pressure growth techniques for phosphorous compounds, InP and InGaAsP	High-purity metalorganic sources Reliability of MO-CVD room temperature CW lasers as a means of material characterization
Characterization			
	Relationship between deep levels and traps and other electrical properties Influence of high electric fields on transport properties and device performance Device modeling for use of device measurement in materials characterization	Correlation of theory and experimental work for proper interpretation of deep level measurements such as DLTS Utilization of photothermo ionization of shallow donor and acceptor states to help characterize impurities and growth techniques High-field transport measurements, velocity-field characteristics, saturated drift velocity measurements	

6. RESEARCH OPPORTUNITIES FOR UNIVERSITIES AND INDUSTRY

The scientific and technical needs listed in Table 1 offer research opportunities to both university and industrial laboratories. The primary requirement in what ever reserach is supported should be tha a wide range of techniques be applied to the characterization of state-of-the-art epitaxial material. Most of the basic and applied research opportunities apply to both university and industrial laboratories, while most of the development opportunities apply primarily to industrial laboratories. The recent results obtained with the MO-CVD of AlGaAs-GaAs materials justify a thorough examination of this growth technique for applications in microstructure fabrication and also for the growth of other materials and compounds. The other epitaxial growth techniques should be studied in more detail.

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FABRICATION OF MICROMINIATURE GAS REFRIGERATORS using SILICON TECHNOLOGY

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FABRICATION OF MICROMINIATURE GAS REFRIGERATORS USING SILICON TECHNOLOGY.

1. Status of Current Work.

During the past decade a large number of new electronic devices have been developed which are based on the Josephson effect in superconductors. These include supersensitive magnetometers, gradiometers, voltage standards, bolometers and logic elements. For their operation these devices require a cryogenic environment. Traditionally the low temperature environment has been provided by a bath of liquid helium. For many applications this is inconvenient and an effort has been made in recent years to use small closed cycle gas refrigerators for this purpose. However, these refrigerators have a capacity on the order of watts while the power dissipated by the devices is typically in the microwatt range. The refrigerators are thus poorly matched to the devices. In response to this problem studies have been directed in recent years to the development of scaling laws for the design of smaller refrigerators. (1)

In 1978 the design of a new class of microminiature refrigerator with a capacity more closely matched to the needs of these devices was reported. (2) Its small size required new construction methods. Photolithographic fabrication techniques were used to etch the gas lines, heat exchangers and expansion valves into the face of a 2" wafer of Silicon. These were then sealed with a cover plate of pyrex glass anodically bonded to the Silicon. This development, if successful, would herald a new era in cryogenic electronics and small scale cryogenic devices. It is dependent, however, on the resolution of several remaining technical and materials related problems. Work on these problems is underway at present in one*university laboratory with strong support from a small private company.†

2. Areas Requiring Scientific and Technological Research and Development

The miniature refrigerators require close thermal coupling between the in-coming and out-going gas streams in the heat exchangers and at the same time good thermal isolation between the low- and high-temperature ends of the device. Single crystal silicon has a very high thermal conductivity, comparable to that of copper at room temperature. It can thus provide the high heat transfer between the gas lines. However, this high conductivity results in a serious heat leak along the length of the exchanger. It would be extremely valuable if the thermal conductivity of

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2. Continued

the Silicon could be modified in a controlled manner so as to make it an anisotropic thermal conductor. Fundamental studies are needed here as to the effects on the thermal characteristics and etching behaviors of silicon of heavy doping by chemical diffusion and, radiation damage with very energetic heavy ions. In addition studies are needed on ways to selectively anneal and cause local recrystallization of amorphous silicon to yield regions of high thermal conductivity in the amorphous matrix. If these problems can be solved, a substantial improvement in the efficiency of these devices can be expected.

The only refrigerator of this general type described to date uses a Joule-Thomson open cycle. It is the simplest cycle but one of low efficiency. It has been pointed out (3) that similar fabrication techniques could be used for the construction of other refrigerator designs using the more efficient Stirling and Gifford-McMahon cycles. Further work is required on these designs. These cycles would require miniature valves and miniature fluidic engines to absorb energy from the working fluid. Some of these have been developed in other ultra-miniature fabrication work notably that of Stephen Terry on the development of a miniature gas chromatograph(4) upon whose work the J-T refrigerator fabrication was also modeled and Kurt Peterson(5) on the development of a micromechanical light modulator.

At the present time the use of silicon appears to be the most useful material for these devices. This is due to the vast amount of work done on it in the semiconductor industry and the ready availability of materials. However, the same microstructure techniques could also be used for the fabrication of similar devices on metal, alumina or plastic substrates. Very little work has been done on this to date but several interesting possibilities exist for the fabrication of very low cost devices with these materials provided problems involving bonding and etching tolerance control can be solved.

3. Impact of Microminiature Fabrication on Cryogenics.

The major limitation to the large scale utilization of superconducting electronics is the lack of a convenient low cost cryogenic refrigerator system. With recent developments in the field of superconducting electronics(6) particularly in the area of ultra high speed data processing using microminiature Josephson devices the need for such refrigerators is the major bottle neck to technological advance in this area. The successful development of a cryogenic refrigerator closely matched to the refrigerator requirements of the superconducting devices would bring a significant number of these devices into large scale use. A superconducting magnetometer, gradiometer, voltage standard or precision attenuator together with its refrigeration system, thermal shroud and vacuum enclosure is envisioned as being contained in a package the shape and size of a miniature vacuum tube.

3. Continued

Other applications are the following. For electron microscopy and x-ray diffraction studies a similar need exists for a miniature refrigerator to enable structural studies to be done on samples as a function of temperature. In many other applications a closed cycle microminiature refrigerator built along the above lines could replace thermoelectric coolers and provide cooling at substantially lower temperatures. Microstructure fabrication of such gas refrigerators would reduce the cost of miniature cryogenic refrigeration systems by two or three orders of magnitude and make superconducting devices available for general use in instrumentation, data processing and medical applications.

4. Opportunities for Research and Development.

As indicated in (2) a need exists for fundamental and applied studies of the thermal conductivity of silicon and of modification of this by chemical and physical means. This could best be done at the Universities. Likewise studies should be made of the fabrication problems of microminiature fluidic devices using silicon, metal, alumina and plastics.

Studies should be made of means for implementing refrigeration cycles other than the Joule-Thomson cycle and the development of microstructure fabrication of pneumatic valves, engines and thermal compressors. Exploratory studies should be made to determine what factors set a lower limit on the size that a refrigerator can be made. For example, could one provide efficient local cooling in regions less than a square micron in size using gas refrigeration?

Funding of the development of specific prototype devices would bring to the fore any remaining problems which are not immediately obvious and would encourage work in the commercial sector. It is important that once these devices are shown to be technically feasible, that commercial development be encouraged so as to bring the fruits of their development to the scientific and technical community as soon as possible. A close working association between Industry and the Universities would make this possible.

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THE ROLE OF ELECTROCHEMISTRY IN THE DEVELOPMENT AND INVESTIGATION OF VERY SMALL STRUCTURES

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CONTENTS

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Section 1 A. CURRENT APPLICATIONS OF ELECTROCHEMISTRY AND PRESENT DAY TECHNOLOGICAL OBJECTIVES

In recent years there has been a considerable number of applications of electrochemistry to the production of materials to be used in the electronics industry and a number of relevant fields are also currently being actively investigated. We can classify some of these applications as follows:

(a) Structures large in 2-dimensions and small in 1-dimension

One of the most wide-spread applications of electrochemistry has been in the production of thin layers of a variety of materials, that is of structures which are large in 2-dimensions but small in the 3rd dimension. These applications include the plating of thin foils such as of copper and gold for printed circuit conductors and contacts and for active devices; the plating of magnetic materials for example on wires; the deposition of oxide films on metals to be used in capacitors.

(b) Structures of intermediate dimensions

The best known application in this area is probably the etching of metals and semi-conductors to produce structures which are of intermediate size in at least 2-dimensions. Etching is in essence a controlled corrosion process in which two electrochemical reactions are maintained in balance. There is also currently considerable renewed interest in the direct plating of arrays to be used in magnetic bubble memories as well as of electrodes for use in liquid crystal or in electrochemical displays. The latter include electrochromic displays and the initiation of colour changes in materials such as viologens and tungsten bronzes.

(c) Structures small or very small in at least 2-dimensions

Structures in the size range 10-100 nm (very fine metal probes) have so far only been investigated and used in the fields of pure electrochemistry and physiology. Arrays of such small structures have not yet been developed although their application in research and technology would be immediate.

(d) Structures large in 2-dimensions and extremely small in 1-dimension

These structures having dimensions down to unit lattice repeat in one dimension again have only so far been investigated in the field of pure electrochemistry.

B. RESEARCH INTO ELECTRODEPOSITION AND DISSOLUTION

Research in this field can be described under the following headings: the fundamental aspects of electrodeposition; the basic aspects of dissolution; current technology; current research on small structures.

(a) The fundamental study of electrocrystallisation

There has been extensive research in this field of work and the increase of present day interest is shown by papers presented at two conferences[1,2]. The study of electrocrystallisation in itself covers a very wide area of work since it includes the deposition of metals, semi-conductors and insulators and each of these topics is sub-divided into deposition on a substrate of the same material and deposition onto a substrate of a foreign material.

The kinetics of these processes are partly established for some systems; thus 3-dimensional nucleation and crystal growth has been observed for some materials while in other cases it has been found that crystal growth takes place via nucleation and growth of individual lattice layers. In many cases the formation of a 2-dimensional layer is followed by the nucleation and growth of a 3-dimensional deposit. The kinetics of nucleation and of lattice formation have been investigated in several systems. In other examples the growth of steps generated by screw dislocations has been observed and in several instances it has been shown that surface diffusion of intermediate species has to be taken into account.

(b) Dissolution processes

Electrodissolution has been investigated mainly in the context of corrosion. A major objective here is the inhibition of dissolution and the work has therefore inevitably concentrated on aspects such as the control of corrosion by using appropriate inhibitors. The basic aspects are not as well established as for electrodeposition.

(c) Technological aspects

The major body of published information in this field relates to the deposition of thick deposits and much of the research has been devoted to the parametric study of practical systems. Thus the conditions for the formation of bright deposits, for the levelling out of recesses for the control of adhesion and stress and the incidence of imperfections have been established and there have been many investigations of epitaxy. There has been success in classifying the effects but at the same time it is evident that many aspects

are not understood on a fundamental level: the search for addition agents to modify deposits remains an empirical art. The major technological objective has been the deposition of uniform deposits and one aim has therefore been to develop plating baths having a high "throwing power". This demands the use of highly conducting solutions while maintaining a high impedance of the interfacial reaction, for example by using complexants. There have also been numerous studies of the conditions which lead to the formation of other types of deposits such as of dendrites (structures small in 2-dimensions) but, as has already been implied, the major objective has been the elimination of the conditions leading to these growth forms.

It will be apparent that much of this work, and especially the topics listed in Section 1A, has been investigated in industry and published information probably only covers a small part of the work actually carried out.

(d) Small structures

Research on deposits of small dimensions has already been referred to in Sections 1A(c) and (d). There has been considerable effort in recent years to investigate the deposition of monolayers at potentials positive to the reversible thermodynamic potential of the bulk material, the so-called "underpotential" deposition. In this way it is possible to form a deposit consisting of one or at the most two layers of the metal. The deposition of thin layers of metals on semi conductors and insulators has also been investigated.

SECTION 2 SCIENTIFIC AND TECHNOLOGICAL NEEDS

The scientific and technological needs will be discussed under the following headings: the fundamentals of electrodeposition processes; the fundamentals of electrodissolution; the development of existing and new technologies; the development of new materials.

(a) The fundamentals of electrodeposition

In future programmes it will be important to investigate the properties of small structures produced by a variety of techniques. These techniques may well include electrodeposition and electrodissolution (see also sections (b) and (c)).

It has already been pointed out that current research has established the mechanism of a variety of electrocrystallisation reactions and, in particular, the role of nucleation and of crystal growth in the initial stages. In order to facilitate the use of electrochemical methods in the production of small structures it is now necessary to study electrodeposition onto very small areas (for example microelectrodes, section 1A(c)). It is known that many electrodeposits are microcrystalline (and in some cases approach the amorphous state) and it is evident that there must be processes causing the "death" of

crystal growth. Studies of the nucleation, growth and death of individual crystallites on micro structures should serve to elucidate these mechanisms. These studies should include the influence of technological variables (such as the use of additives) on the individual steps. It is necessary for work of this type to embrace the deposition of metals, semi-conductors and insulators.

Means are now available which permit the ex situ and in situ study of electrical, magnetic and mechanical properties of electrodeposits; the properties of very thin films will be of particular interest.

It is important now to establish the relationship of the dependence of the properties of electrodeposits on the method of preparation and it here may be noted that electrocrystallisation has so far been approached from one of two points of view: either the kinetics of crystal growth have been investigated on surfaces with known patterns of imperfections or else the development of imperfections under stated conditions has been studied. These two aspects are linked: the kinetics are determined by the pattern of imperfections and in turn determine the pattern of imperfections. It is important that this loop be now closed.

It should also be noted that the study of electrocrystallisation has been dominated by theoretical considerations and that observation of the "classical" mechanisms of growth following nucleation and of growth perpetuated by dislocations has been due in part to the search for systems which follow the predicted kinetic laws. It is highly likely that there will be other mechanisms at work and there is therefore an urgent need to develop methods which may be used to investigate the basic aspects of practical systems and to define the mechanisms which are of particular relevance to the technological needs. These studies may well serve to provide novel means of controlling the complex processes.

(b) The fundamentals of electrodissolution

It is important to establish the basic aspects of electrodissolution to achieve a level of understanding comparable to that which has been reached in the case of electrocrystallisation. It will be necessary to investigate the dissolution of very small structures and a substantial part of these investigations should be carried out in conjunction with (a).

(c) Technological aspects

The technology of depositing and of etching small structures will certainly require the investigation of new classes of additives which will give these structures the required properties. It has already been pointed out in section 1B(c) that the practical objectives of plating have usually been the production of uniform deposits. However, these objectives are not necessarily relevant to the development of small structures. For example, in the field of

electronics one will certainly wish to develop the means for plating and etching sharply defined small areas and it is therefore necessary to develop baths and conditions for achieving low throwing powers.

The development of electrodes of very small dimensions (both dots and lines) is itself relevant to the production of small areas. Thus it may well prove possible to use such electrodes in turn in order to plate or dissolve deposits on the sub-micron scale (using solutions of low throwing power). For example, it may be possible to plate a raster of lines or an array of dots or, indeed, more complex patterns. Direct methods of deposition may well permit higher precision and a reduction in the number of process steps as compared to conventional technology. It may also prove possible to photo-initiate nucleation in electrodeposition processes and indeed to investigate the general question of the role of catalysis in electrodeposition and electrodissolution. It is possible to deposit thin films of semi-conductors and insulators in addition to thin films of metals. It would be useful therefore at this time to reconsider whether the direct deposition and dissolution of new phases should not be integrated into present and future production schemes. Furthermore, the deposition of organic polymers may also be feasible. It should be noted that inorganic and organic materials could be deposited by electrophoresis and that polymerisation may be initiated electrochemically.

Electrodeposition and electrodissolution involves a complex sequence of steps and it should therefore be possible to modify the overall performance by using pulse techniques, that is, by introducing time as a variable. For example, it is known that the dimensions of the crystallites of an electrodeposit may be reduced by initiating nucleation with a short pulse of high overpotential and continuing growth at a low potential. Equally the throwing power during non-steady state deposition or dissolution must be a function of time.

(d) *The development of new materials*

The deposition of thin films (including monolayers) of metals has already been referred to in section 1A(c). It should be possible to devise electrochemical means of forming layer lattices of controlled dimensions.

SECTION 3 THE POSSIBLE IMPACT OF THIS RESEARCH ON RELATED FIELDS

One of the aspects we have emphasised in this article is the role which electrochemistry may play in the formation of small structures. The availability of such small structures would, however, in turn have a consider-

able impact on electrochemistry, biology, physiology and medicine. For example, in the case of the investigation of electrode kinetics the enhanced mass flows to systems of small dimensions (due to the nature of the cylindical or spherical diffusion fields as compared to a planar field) will permit the study of fast electrode reactions on a long time scale and, indeed, in the case of spherical diffusion fields, in the steady state. Reduction in the size of the electrode enhances the "noise" due to the random nature of the chemical processes as compared to the mean reaction rate. It should therefore become possible to interpret the higher moments of the rates of reaction and especially of the quantities related to the second moment such as the standard deviation, the auto covariance function or the power spectral density of the rates. It may be noted that electrodeposition processes themselves generate appreciable noise so that measurements of such stochastic quantities may well be integrated into research in electrodeposition and dissolution, Sections 2(a) and (b).

The production of closely spaced arrays of micro electrodes or of rasters would also prove valuable in the study of electrochemical kinetics since the fate of intermediates generated at one location may be monitored at other points. Such arrays would also prove useful in investigating the spatial and temporal distribution both of electrochemical (e.g. electrodeposition and corrosion) and of bioelectrochemical processes. The arrays could be passive or active; thus an array of gates could be used to probe the distribution of potential while an array of current followers could be used to probe the distribution of current over appropriate surfaces.

Deposition of small structures of metals, semi-conductors and insulators will permit novel studies of catalysis for example by relating the rate of catalysis to the dimensions of the clusters. The deposition of monolayers of metals on substrates also affords new opportunities for investigating the role of defined lattice sites (the edges and tops of the layer planes) on catalytic reactions. The study of these materials may well lead to the production of novel catalysts.

SECTION 4 RESEARCH OPPORTUNITIES IN UNIVERSITIES AND INDUSTRY

The areas of work outlined in Sections 2(a)-(d) could well be pursued either in university or in industrial laborstories. It is likely, however, that the basic aspects, namely the fundamentals of electrodeposition and electrodissolution will be best suited for investigation in an academic environment. The technological aspects and the development of new materials which has to meet stated objectives is, on the other hand, probably best carried out in industry with appropriate underpinning of the research in academic

institutions. All these fields of research will require extensive structural measurements as well as electron optical investigations. They will, therefore, be best carried out in those institutions which have a background in the fields of electrochemistry and/or crystal growth, as well as in materials research.

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PROPERTIES OF INSULATOR MATERIALS AT VERY SMALL DIMENSIONS

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PROPERTIES OF INSULATOR MATERIALS AT VERY SMALL DIMENSIONS

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I. CURRENT STATUS

Dielectric films play a central role in today's semiconductor device technologies. In many instances, the insulating electrical properties of these films is less important than their structural or chemical properties. Kern's recent review[1] lists nearly two dozen different applications of dielectric films in Semiconductor Technology. Insulators are most commonly associated with MOS gate dielectrics, dielectric insulation, or semiconductor surface passivation. However, they also are used as hermetic seals, ion-diffusion barriers and interlevel insulation layers. Furthermore, they can also serve as temporary processing structures by functioning as masks for etching, oxidation, or diffusion, or serving as diffusion sources, or as contaminant gettering layers. Each of these different applications place different requirements on insulator properties, especially in the fabrication of very small dimension devices.

Despite the varied applications of insulating materials in microstructure fabrication, their use as surface passivation layers is probably the most demanding application and should be the focus of the most attention. The passivating insulator as typified by an MOS gate insulator is typically the thinnest insulator in a device, is required to withstand the highest electric fields, and is the least tolerant of oxide charge mobile charge, interface states, or electron traps. This gate insulator must have very low defect densities and very high reliability, and must be

capable of withstanding the high temperature and stresses associated with subsequent device processing.

Because of these strenuous requirements, thermally-grown silicon dioxide has been the almost universally chosen dielectric for use as a gate insulator in silicon device technology. Balk's review[2] of alternate insulators concludes that it is unlikely that SiO_2 will be replaced by other insulators in single insulator film MIS gates in the near future, and that any layered dielectric system will be fundamentally unstable. As a result of this choice, SiO_2 grown on Si has been very extensively studied over the last two decades. Recent review articles discuss correlations of preparation properties[3], charge effects [4], dielectric breakdown[5,6], and charge trapping[7,8] in SiO_2

In an attempt to precisely define the status of the current understanding of charge effects in SiO_2, Deal[4] surveyed seventy scientists in 12 countries from industrial, government, and university laboratories. The survey showed reasonable agreement on general items, such as classifying charges, the problems and technologies associated with controlling and minimizing these charges, and the effect of charge on device parameters. However, there are substantial questions and differences of opinion regarding the origin and nature of these charges and of the structure of the Si-SiO_2 interface.

In addition to charge levels, technological interest has focused on insulator defect levels[1,5] and dielectric integrity[5,6] under long term stressing. Yield and reliability are not simple properties of an insulator; they are usually dependent on insulator preparation[3], electrode materials[9], and subsequent processing, and one has to think in the context of an insulator system rather than in terms of the pure insulator film itself. Wafer cleaning, oxidation temperature and atmosphere, and the use of additives, especially Cl, during oxidation are some

of the key variables. Often a specific device technology will result in insulator defects that are unique to the process or topography associated with that technology. For instance, the dielectric breakdown voltage of SiO_2 in a VMOS device may be only 1/3 of that in a planar device. The local oxidation process is known to produce defects at pattern edges. High levels of perimeter defects have also been observed in overlapping double poly-Si devices. Although defects may not provide a fundamental limit to reducing device dimensions, they certainly are key in determining the rate of progress to higher levels of integration in devices.

The use of a III-V semiconductor rather than Si presents even greater challenges to the material scientist in producing acceptable insulator films. Despite considerable effort, no one has yet found an analog to thermal oxide on Si for compound semiconductors. Thus, these devices have been used in opto-electronics or with Schottky gates, and not as inversion channel devices for VLSI. While it cannot be denied that III-V MIS devices may ultimately give higher performance than Silicon MOSFET's in a VLSI technology, the III-V development has lagged silicon by a decade and the gap seems to be widening. Furthermore, alternate silicon devices such as high performance npn bipolars are likely to exceed the speed of III-V MIS devices.

II. FUTURE NEEDS

The trend to smaller device and insulator dimensions presents many challenges. First, the yield and reliability of these insulators must be at least maintained, if not improved, while reducing the insulator thickness; as the size of a critical defect is reduced, the number of critical defects increases dramatically. The yield problem is aggravated by the fact that thin oxides require very little oxidation time at low temperatures; under these conditions it is more difficult to control oxide thickness, and the beneficial effects of Cl containing oxidation additives is diminished. Second, the corresponding trend is to operate these very small devices

at the maximum possible voltage where hot electron injection occurs; hence insulator traps, especially neutral traps, become increasingly important tc control and reduce. Third, the fabrication of very fine dimensions generally requires high energy radiation: electron-beam or X-ray lithography, plasma or reactive-ion etching, ion implantation, and plasma deposition of films, all of which processes generate oxide traps. Thus, the generation and annealing of radiation-induced trapping in insulators becomes very important[8]. Finally, a decrease in device or insulator dimension really requires a corresponding decrease in tolerances (thickness, charges, etc.). Not only must the insulator tolerances scale down, but other device parameters must also be better controlled; often this means that the thermal cycles used to prepare the insulator must be reduced.

These general needs are translated into more specific scientific and technological needs in Table I. This table makes extensive use of the survey results of Deal[4]. It should be kept in mind also that no revolutionary new requirements are envisioned, and that, in fact, devices having very small dimensions have already been fabricated in laboratories. It will be necessary to improve our understanding of insulator properties, to enhance control over insulator parameters, and to increase yield before small-dimensional devices become important; nevertheless, only evolutionary improvements will be needed. The rate of progress of devices will be limited by the rate of progress in controlling insulators.

III. ADDITIONAL IMPACT OF INSULATOR RESEARCH

Increased study of insulators used for small dimension semiconductor devices could reasonably be expected to benefit other microelectronics technologies. Magnetic Bubbles, Josephson Junctions, thin film capacitors, and solar cells, to name a few, all use thin-insulating layers. In the past, these technologies have benefited from advances in silicon technology, and

it is likely they will benefit from future advances in reliability, control, characterization and preparation.

The additional impact of insulator research on unrelated areas is quite speculative. Currently the use of MIS devices for medical or chemical sensors is an active area of research. The use of insulators as corrosion or thermal barriers is also important. However, it is very difficult to pinpoint synergisms. Certainly it seems reasonable to hope that advances in insulator research will benefit other areas in three ways: 1) from the use advanced semiconductor devices in instrumentation and analysis, 2) from advances in materials characterization techniques, and 3) from the development of alternate insulators and alternate deposition techniques.

IV. OPPORTUNITY FOR RESEARCH

The needs of future insulators as outlined in Table I present many opportunities for industrial, university and government research laboratories. Because of the evolutionary and technological nature of these needs, it is most logical to expect most actual progress to come from industrial laboratories. Because of the large resource requirement, it seems unrealistic to expect university studies on yield or process optimization. However, there are many fundamental areas from Table I that are especially suitable for academic address. The subset of research areas that should be most amenable to university research is summarized in Table II under three headings: 1) Improved Understanding, 2) New Processes for SiO_2, and 3) Novel Insulators and Materials. University research to improve our fundamental understanding of oxide properties should receive the highest priority. Technological progress in industry does not ensure adequate fundamental understanding, and additional university work could be very beneficial in supplementing industrial work. Second priority should go to studies of new or

novel processes for SiO_2. While ordinarily one would expect most progress in this area by industry, creativity and invention know no bounds, and good ideas should be pursued wherever they occur. The lowest priority goes to the study of novel insulators and materials. In the context of Microstructure Fabrication at small dimensions, the current body of knowledge indicates that other materials have only a remote possibility of being useful. Nevertheless, it seems shortsighted to totally abandon alternates - especially since they may find other applications. For example, in medical electronics applications one can envision a need for microprobes which are flexible and which require passivation against hostile environments. University laboratories seem like an ideal place to conduct some of these high risk studies.

TABLE I

Areas of Scientific and Technological Needs for Insulator Materials

I. Yield and Reliability

Relationship of substrate and substrate cleaning to defects.

Effect of processing conditions and subsequent thermal cycles on defects.

New methods to reduce defects.

II. Insulator Traps

Oxide trap origins, trapping and annealing mechanisms, and relationship of traps to impurities and defects.

Trapping in thin oxides and/or under high fields; also hot carrier trapping.

Production of trap free oxides.

Effect of process parameters and annealing on insulator traps.

III. Radiation Induced Traps

Relationship of radiation-induced charge to other trapped charges.

Effect of process parameters and impurities on radiation-induced traps.

Techniques to reduce radiation sensitivity.

IV. Tolerance Reduction

A. Oxidation

-- Properties and control of ultra-thin oxides.

-- Effects of impurities on oxidation of thin oxides.

-- Evaluation of new techniques to reduce thermal cycles - high pressure oxidation, plasma oxidation, CVD.

B. Charge Control

-- Nature of Si-SiO_2 interface region. Better analytical techniques.

-- Relationship of oxide charges to oxidation and other processes.

TABLE I (continued)

-- Relationship among chemical, physical, and electrical properties of oxide.

-- Interrelationship among device parameters and charges.

-- Effects at metal-oxide interface. Effects due to poly-Si gates.

-- Experimental results to back up opinions; scientific rather than empirical process control.

-- Origin and physical/chemical structure of fixed oxide charge and interface states.

-- Nature of negative bias trapping.

-- Minimize oxide charge and interface states.
-- Relationship of Q_{ss} to other charges.

-- Effect of dopants and impurity ions on oxide charge and interface states.

-- Relationship of oxide charge to interface states and traps.

-- Improved purity of processing materials.
-- Gettering mechanisms, including chlorine.
-- Nature of impurity ion "chemistry" in oxides. Also role of hydrogen.

-- Relationship of mobile charge to other charges.

TABLE II

Opportunities for University Research on Insulator Materials

I. Improved Understanding of Insultors

Models for long-time dependent dielectric breakdown.

Origin of oxide charge.

Origin and nature of interface states.

Origin of insulator traps.

Origin of radiation-induced traps.

Effect of impurities on oxide charge and traps.

Relationship, if any, between different charges and traps.

Nature of the Si-SiO_2 interface region.

Nature of negative bias trapping.

II. New or Novel Processes for SiO_2

Techniques to reduce charge or traps.

New oxide preparation techniques - high pressure oxidation, plasma processing, Cl oxidation.

III. Novel Insulators and Materials

Alternate Dielectrics

Insulators for III-V's.

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PLASMA PATTERNING OF MATERIALS AT VERY SMALL DIMENSIONS

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PLASMA PATTERNING OF MATERIALS AT VERY SMALL DIMENSIONS

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I. Introduction and Status of Current Work

INTRODUCTION

Recent improvements in lithographic techniques have permitted a reduction in feature size in photo and electron sensitive organic resist masks into a range where conventional liquid phase chemical etching is no longer a viable means of transfer of the resist pattern into an underlying inorganic film. Accordingly, there has been a growing emphasis on the use of gas phase, plasma-assisted etching methods which offer the potential for very high resolution pattern transfer. This potential is linked to the ability to direct charged particles from the plasma onto the surface being etched in such a manner that the vertical etch rate (through the film thickness) can be made to greatly exceed the lateral etch rate; that is, anisotropic etching is possible. Indeed, recent work in this area has demonstrated the capability to perform anisotropic etching of all of the materials currently used for silicon integrated circuit fabrication under conditions producing essentially no lateral etching.

Under the generic title "plasma-assisted etching" we include ion milling, sputter etching, reactive ion etching (reactive sputter etching) and plasma etching. Although these techniques

all utilize plasma activated species, the mechanisms involved in the etching processes differ. Ion etching (ion milling or sputter etching) is a strictly physical process in which high energy (several hundred to several thousand eV) noble gas ions are directed at the film surface and etching occurs by momentum transfer ejection (i.e., by physical sputtering). Since ions can be directed normal to the film surface, anisotropic etching is possible.

At the other extreme of plasma patterning techniques a molecular gas plasma serves as a source of reactive radicals capable of chemically combining with film material to result in a volatile product readily removed by pumping. Silicon, for example, is easily etched in a CF discharge via SiF formation. This chemically based technique is generally called plasma etching.

Ion etching and plasma etching are parametically as well as mechanistically different. The former process is most effective at low pressure (< 0.1 torr) and relatively high electron and ion energies, while the latter has typically been found to produce practical etch rates at higher pressure ($\gtrsim 0.1$ torr) and substantially lower energy.

Between these two extremes is a parameter space referred to as reactive ion etching. In this mode, reactive gases are used and substrates are exposed to ion energies of several hundred eV. Ion energies are sufficient to produce anisotropic etching but are not high enough to produce significant physical sputtering rates. The interaction between ions and radicals in reactive ion etching is not completely understood. It is not necessary to operate in the ion etching or reactive ion etching modes to obtain anisotropic etching. Under suitable conditions, anisotropic etching is readily demonstrated under the higher pressure (lower energy) conditions typical of plasma etching. This is of particular interest for silicon integrated

circuit fabrication where it is desirable not to exceed energy thresholds for device radiation damage.

An additional benefit of "reactive" plasma techniques (plasma etching and reactive ion etching) is the ability to achieve a high degree of etch selectivity with respect to etch mask and underlying materials exposed at the end of etching. Consequently, these techniques are preferable to the "physical" plasma methods which inherently lack substantial selectivity. Additionally, the reactive techniques are free from redeposition phenomena[3,4] which ultimately limit the resolution of ion etching.

STATUS OF CURRENT WORK

Research and development activity directed toward plasma patterning of materials has been and continues to be concentrated in the semiconductor industry. The obvious implications of very high resolution pattern transfer in emerging semiconductor technologies such as very-large scale silicon integrated circuits have been recognized for several years and development efforts by major semiconductor manufacturers have been in progress for nearly as long a time. However, comparatively little information has been disseminated by industrial sources reluctant to release any "art" which might provide an "edge" in development of very fine feature circuits. Academic and government laboratories have had relatively little involvement in this area. This is not surprising in light of the motivating factors for developing high resolution pattern transfer processes and the somewhat prohibitive costs of equipment needed to produce device structures and masking patterns appropriate to exploratory work.

Noble gas ion etching techniques are older and far better understood than the newer reactive methods and consequently, an ample literature exists for them which is adequately referenced in several recent review articles.[3-6] The reactive techniques which are favored for

silicon device applications have been reviewed less extensively.[6-9] In particular, there has not been an adequate discussion of the methods or processes essential to anisotropic etching. Since the capability to routinely achieve high resolution pattern transfer, with high selectivity, is probably limited to a few laboratories at present, this situation may persist for some time. Despite this, it is known, for example, that all of the pattern transfer needs peculiar to state-of-the-art silicon IC fabrication can be accomplished with high resolution (anisotropic) reactive plasma processes and that these processes are either being used in production or are considered to be production ready.

Use of reactive plasma methods for *high resolution* pattern transfer in non-silicon device technologies (e.g., III-V compound semiconductors, magnetic bubbles, integrated optics ...) has been almost nil judging from the dearth of published information on the subject. This results, in part, from the difficulty in finding suitable gaseous reactants for materials such as GaAs, permalloy, LiNbO, etc. and also because there has been considerably less effort expended.

Noble ion etching techniques have been employed in the fabrication of GaAs and magnetic bubble devices, however, as noted earlier redeposition ultimately limits the resolution of these techniques and it is unlikely that submicron geometries could be achieved using current processing methods.

II - Scientific and Technological Needs

There are both scientific and technological needs which must be satisfied for optimum progress in the development of plasma patterning of materials. As already mentioned, the ion etching techniques based on sputtering are reasonably well understood and further scientific advances which would have a significant impact on the use of these techniques for pattern transfer seems remote. In contrast, for the reactive techniques the technology has clearly

advanced far beyond any detailed understanding of basic mechanisms. Specific areas of interest here include: (1) plasma chemistry and physics; better understanding of the chemical reactions occurring in the plasma and the influence of physical parameters such as fields, field gradients, and ion and electron energy distributions on these reactions is needed. Further, the relationship of these factors to control variables such as pressure, power density, frequency and reactor geometry requires further study. (2) Surface chemistry; details of the actual etching process are required such as identification of the active species and its site of origin, a kinetic desciption of the surface processes involved in the etching reaction, identification of primary product species and further understanding of the importance of ion and/or electron bombardment in enhancing chemical reaction rates. (3) Thermochemical and kinetic studies applied to prediction of suitable gases for etching of new materials and optimizing selectivity. (4) Better understanding of the mechanisms of device radiation damage in cold plasmas particularly as regards type and importance of damaging particles (ions, electrons, photons), threshold energies for damage, damage as a function of feature size and means for elimination or suppression of damage.

Technological needs to be met for progress in applying reactive plasma techniques are:

1. Refinement of existing high resolution processes (mainly for silicon technology) to improve selectivity, uniformity and reproducibility.

2. Development of high throughput, automated reactors capable of high uniformity, high resolution etching.

3. Development of processes or improvement of existing processes for etching metallization, particularly metals such as Al-Cu, Al-Si, Au, Pt, Pd and permalloy.

4. Improvements in plasma tolerance of organic resist masks, particularly those materials appropriate to submicron lithographies. Improvements in reactor design and tooling may also be needed in this regard.

5. Development of etching processes for III-V and II-VI compounds and materials pertinent to fabrication of devices based on these compounds.

6. Development of etching processes for materials pertinent to integrated optics.

III. Possible Impact on Non-related Fields

Technologies other than those based on silicon that would benefit from advances in reactive plasma techniques include bubble memory, integrated optics and display. Bubble memory and integrated optics are moving to submicron dimension line widths and so will require the patterning capability of these techniques. An important prerequisite is that etching gases must be found to etch the materials that are used.

Bubble Memory

State of the art bubble memory products employ permalloy as the magnetic material and AlCu or Au as the conductor.[10] At the present time, the permalloy is delineated using ion

milling. Reactive plasma techniques are not possible because a suitable etching gas has not been found. The gases used in silicon device fabrication do not chemically attack permalloy to form volatile products. Etching of the conductor is at a more advanced stage because it is known that AlCu and Au form volatile chlorides at elevated substrate temperatures. If a suitable etching gas for the magnetic material were found, reactive plasma techniques could be used in the fabrication of bubble memory. The advantage would be one of greater etch resolution and so a higher storage density in the bubble memory chip. The substrate material used for bubble devices is a doped GdGa garnet. At present bubble devices are planar and so it is not necessary to pattern the substrate. However, there may be additional bubble device applications if it were possible to pattern the garnet.

Integrated Optics

The goal in integrated optics is to combine a number of optical components in a single structure in order to perform complex functions for optical communication applications.[11,12] The components include sources, single mode wave guides, switches and associated circuitry. GaAs-GaAlAs is the material most commonly used for the injection laser. With the goal of integration in mind, GaAs has also been used to fabricate other optical components. Electro-optic and acoustooptic materials are important in the fabrication of thin film modulators.[13,14] These materials include GaAs, LiNbO, ZnO and some organic films. Micron to submicron patterning capability is required to fabricate the single mode wave guides, high resolution optical gratings and other structures for thin film optical devices. The dimension of optical wave guides, for example, must be comparable to the wavelength of the light, approximately one micron. The edge definition of the wave guide should be better than 0.5 μm in order to minimize scattering. Reactive plasma techniques could be used to fabricate these structures if an etching gas can be found for a suitable combination of materials.

Display

The displays that are available now are ones in which the primary image is created in the viewing plane. Displays in this category are the CRT, a continuous display, and the matrix addressable gas panel display. In a matrix addressable display of this type, the smallest desirable writing spot is determined by the optical characteristics of the eye. A reasonable dimension is of the order of 10 mils, well within the patterning capability of conventional photolithographic and plating techniques. Displays that are well along in the development process include matrix addressable electroluminescent displays and continuous liquid crystal displays. Conventional patterning techniques appear adequate for these displays as well. Conventional lithography does not appear to be taxed until matrix addressable projected displays are considered. These large area displays are at a less developed stage.[15,16] They involve the fabrication of structured targets for addressability. If a reasonable magnification of the order of 10 is considered, a target dimension of about 25 μm with a spacing between targets of about 2.5 μm is obtained. The use of reactive plasma techniques in the fabrication of these displays is highly desirable for two reasons. First, the aspect ratio of the targets is $\gtrsim 1$. Thus, directional etching is required even though the lateral dimensions are in the range of optical lithography. Secondly, directional etching is required for edge definition. Edge rounding leads to scattering of light in unwanted directions with a consequent loss of contrast.

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IV - Academic and Industrial Research Opportunities

Areas that require further investigation can be divided into three categories. The first category is basic research devoted to developing an understanding of the details of the reaction between the plasma and the solid surface. The second category is the development of processes by which VLSI circuits can be fabricated. The third category is the development of processes by which devices and circuits based on technologies other than silicon can be fabricated. This category is not considered with work in silicon processing because the two areas differ so greatly in their level of development.

Basic Research

It is the opinion of the authors that a weak point exists in the development by industry of reactive plasma techniques for fine patterning. There is an increasing reliance on these techniques that is not matched by advances in our understanding of the basic mechanisms involved in the etching process. While only a few industrial research labs are able to devote resources to basic work, the university is especially suited to meet this important need. Some important areas under the category of basic research include:

1. Chemistry and physics of reactive plasmas and their dependence on control variables such as power, pressure, flow rate, and reactor design.

2. Surface chemistry, specifically, study of reaction to form volatile product and possible alteration of substrate surface by the etching process.

3. development of diagnostic tools to study plasma during etching, possibly leading to development of process control tools.

Silicon Device Process Development

Work under this heading tends to require substantial support in that realistic (submicron line width, gate quality oxides, etc.) test structures must be supplied and extensive electrical and material testing facilities must be available. For this reason, the industrial lab or the university with the support of the industrial lab is best able to carry out this activity. Some pressing technological needs are:

1. Selective etching of films relative to mask materials and the underlying substrate

2. delineation of Al, Al alloys, Au, Pt, Pd etc. for metallization

3. improved reactor designs for higher throughput, better uniformity

4. understanding of radiation damage, for example, sources of damage, shielding effect of gate electrode, methods to avoid or remove damage

Process Development for Devices Based on Technologies Other than Silicon

Reactive plasma techniques have not been widely investigated for use in technologies such as bubble memory, integrated optics and display. As a result, important contributions can be made with relatively little support in the way of test structures. The first technological advance required to apply these technqiues in most of these areas is simply the development of a suitable etching gas or gas mixture. For example, etching gases for permalloy, garnet, AlO

and electrooptic materials such as LiNbO are not now known. Once suitable etches gases are found, questions concerning mask materials and selective etching can be addressed.

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INTERFACES AND ION BEAMS

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INTERFACES AND ION BEAMS

1.0 INTRODUCTION

In principle, an interface is a transition in the structural and/or the chemical uniformity of a material which is confined to few atomic distances. In practice, our ability to study interfaces is restricted by the limitations of the analytical tools that are applied to investigate interfaces. These limitations are particularly confining in the case of interfaces because they are basically two dimensional boundaries of three dimensional objects. The number of potential sites or atoms available for detection and characterization of an interface is smaller than those of the surrounding bulk by orders of magnitude. Experimental limits are thus faced simultaneously with signal-to-noise ratio and with spacial resolution. To achieve the required sensitivity and resolution inevitably leads to increased doses of exposure and energy levels of the physical processes involved in the measurement. The trade-off between gain in information and loss of interface integrity ultimately sets a limit to the precision with which an interface can be characterized. In one particular instance, namely in the case of ion beam interactions with solids, the experimental sophistication is nearing the points where these trade-off's can be perceived in some of their rough outlines. This is the subject of the first part of this report.

The second part treats the same subject of interfaces

and interactions of ion beams with solids from a diametrically opposite point of view. The aim there is to maximize the affect of an experiment on an interface in an attempt to exploit the unique conditions that exist there and obtain results not achievable by other means. Limitations then became assets, and they transform analysis into synthesis.

2.0 STATUS OF CURRENT WORK

2.1 Profiling of Interfaces by Ion Beams and Backscattering Spectrometry

The depth resolution obtained by backscattering of 1 - 3 MeV ^{4}He ions is limited by practical as well as by basic factors[1]. In standard types of measurement with near-normal path of the incident and detected particles and Si surface barrier detectors, the energy resolution is limited by the detector-preamplifier system to about 15 - 20 keV, which translates to 100 to 300 Å of depth resolution, depending on the nature of the sample investigated. This value applies to the near-surface region only. At a depth, the equivalent depth resolution deteriorates because of energy straggling of the He beam. For example, the resolution at 1μm depth deteriorates to about 3 - 5 times its near-surface value, depending on beam and sample parameters. That deterioration is of fundamental origin and cannot be eliminated by improvements of the detection system.

In the near-surface region, however, the resolution can be improved very substantially by various experimental means. Glancing angles of incidence or exit of the particles increases the effective path length to a given depth and correspondingly increases the effective depth resolution for the same detection system. A resolution of 25 Å has been reported[2], and values of 40 Å are typical in this mode of backscattering analysis. Energy straggling again deteriorates the resolution with depth. A degradation by a factor of two was observed at a glancing angle of 5° for a depth of 700 Å in Si[2]. Electrostatic and magnetic analyzers are much superior to Si surface barrier detectors in their ultimate energy resolution, but they can only analyze a small energy interval at a time and so require much larger exposures for the same spectrum. Equivalent depth resolutions at the sample surface of 5 Å have been reported with an electrostatic analyzer combined with glancing beam angles[3].

A drawback of the glancing angle technique is the increased area that the beam illuminates on the sample. Stringent requirements must be met in the integrity and lateral uniformity of a sample if a real improvement in resolution is to be obtained. It is also necessary to increase the energy stability of the beam and the quality of the vacuum appropriately. It must be noted too that depth resolution values can be claimed only to the extent that it is established by independent means that the samples used in the test possessed the requisite integrity. For backscat-

tering spectrometry, where lateral beam dimensions of 1 mm are typical, this requirement is extremely stringent and particularly difficult to meet when samples of thicknesses below a few 100 Å have to be prepared. Most data on reported depth resolutions in that thickness range rely on theoretical estimates of energy straggling which await confirmation.

Channeling is a refinement of backscattering spectrometry which can determine atomic displacements at surfaces and at interfaces. For example, the relaxation of the outer-most layer of atoms of a Pt single-crystal on a (111) surface has been measured by channeling as consisting of an outward displacement of 0.03 Å with an estimated probable error of $\pm$ 0.01 Å[4]. The channeling method has also been applied to the study of the SiO_2-Si interface below thin SiO_2 layers by admitting the channeled analyzing beam from the backside of sufficiently thin (< 3000 Å) substrates[5]. The resolution of fractional monolayers in this method is obtained by shadowing the atoms of a surface or an interfacial layer against the atomic rows or planes of a single-crystal substrate. The detector resolution does not enter as a limiting factor for the accuracy with which the shadowing can be detected, but the presence of a single-crystal as the substrate is essential and so is the geometrical precision of the beam collimation and the goniometer.

2.1.1 Layer Removal by Sputtering

The question on the accuracy of a measured profile obtained by ion bombardment and sputtering in combination

with a surface sensitive analysis technique (SIMS, AES, ESCA) cannot be answered unambiguously[6,7]. The complexity of the sputtering process itself and of the phenomena associated with the detection method are the main reasons. Obvious causes of errors in the accuracy with which an interface can be measured are due to instrumental factors, information depth, original surface roughness, knock-on and ion mixing, preferential sputtering, atomic transport and chemical reactions, crystal orientation and crystal imperfection, and the basic sputtering process.

The analysis techniques, such as AES or SIMS are highly surface sensitive because the escape depth of Auger electrons and secondary (or sputtered ions are generally less than ten to twenty angstroms. Experiments have shown that ions used for sputtering can mix atoms over depths comparable to the ion range[8,9]. Since the depths ($\sim$ 50 Å/ keV for Ar ions) are greater than escape depths of Auger electrons and secondary ions, AES and SIMS techniques are essentially analyzing "mixed" layers. When analyzing interfaces, the ion beam used to sputter remove the layer above the interface will reach and alter the interface before the analysis technique can sense the presence of the interface.

For an optimum setup of the sputtering experiment and favorable sample conditions, all these effects might be minimized and negligble compared to the uncertainty introduced by the fundamental process of sputtering. An explicit

expression for this contribution has been derived on the basis of simple probabilistic sequatial layer removal model[10]. The depth resolution predicted by this model has been verified for a number of cases[11]. For example, a sharp interface located 10 Å below a plane surface can be located only with a depth resolution of 10 Å ($\Delta x/x$ = 100%) while that same interface at 1000 Å depth can be located within about 100 Å only ($\Delta x/x$ = 10%). Processes which adversely affect the resolution in a mainly depth independent fashion (e.g. knock-on effects, ion mixing, chemical reactions) will worsen this ultimate resolution for shallow depths, while thickness - (or sputtering time-) dependent processes (like matrix effects, and presumably also original surface roughness and impurity effects) deteriorate the resolution at increasing depths.

In conclusion, neither backscattering spectrometry nor layer-removal methods based on sputtering are found to have a depth resolution adequate to depth profile interfaces located several hundred angstroms or more below the surface. Under special conditions, channeling measurements can provide information on atomic displacements at the surface or the interface.

2.2 Alteration of Interfaces by Ion Beam

The passage of an energetic ion through an interfacial layer will influence the properties of the interface. One example is the formation of silicide layers at the metal-silicon interface as a result of bombardment with energetic ions. For example, several hundred angstroms of Pt_2Si can be formed by 10^{15} Ar ions/cm^2[12]. The growth of the silicide layer is due

to an atomic mixing or enhanced diffusion within the volume of the collision cascade around the ion track rather than to recoil of knocked-on atoms or sample heating.

The use of ion beams to trigger interfacial reactions differs from direct implantation of ions, a process where high doses, $> 10^{17}$ ions/cm^2, are required to achieve atomic concentrations greater than ten atomic percent[13]. In the present case, atomic mixing within the collision cascade leads to displacements of orders of magnitude more atoms than the number of incident ions. The process is efficient in altering the properties of materials as compared to direct implantation.

As in the case of sputtering of compound materials[8,9], the changes in the atomic composition of the material extend over distances of the order of the ion range. The energy of the ion must be sufficient to penetrate to the interface. For films of about a thousand angstrom thickness, ion energies of several hundred keV are required. Implantation systems with this energy are in commercial use.

The extent to which the interface undergoes a transformation appears to be related to the thermodynamic properties of the system, activation energies and diffusion constants. For example, silicides which form at low temperatures are more easily reacted by ion beams than those which form at higher temperatures. At present, however, there have not been systematic studies to predict in advance the ion specie or dose required to cause significant mixing or interfacial reaction of an

arbitrary system.

It had early been established that the penetration of energetic ions would improve the adhesion of metal layers[14] and that high-dose implantation could change the corrosion resistance of metals[15]. The thrust of this discussion is that reactions can be induced by ion beams penetrating the interface. Recent experiments have indicated that phases can be produced that cannot be formed by conventional near equilibrium processes.

3. TECHNOLOGY NEEDS

Interfaces play a dominant role in technology whether related to adherence of films, the inter-penetration of metal and semiconductor in device contacts, or the composition of the transition layer between Si and SiO_2. The present methods of depth profiling the interface composition are not adequate. There have been advances in transmission electron microscopy which provide valuable information on the structure and uniformity of metal/semiconductor and Si/SiO_2 interface. However, they have not revealed the atomic composition. The interface problem becomes all the more acute as one considers VLSI technology where dimensional control must be achieved.

The need for use of ion-induced interfacial reactions is not as well established as the requirement to minimize these reactions in sputter sectioning. However, the widespread availability of ion implantation systems with energies sufficiently high so that ions can penetrate through the interface suggests an obvious

area of study.

4. OPPORTUNITIES TO INDUSTRY/UNIVERSIY

Studies of the interface provide an ideal opportunity for interaction between universities and Industry. On one hand, Industry can delineate the requirements for interface properties and identify classes of structure that are of primary importance. Universities can proceed in the detailed study in collaboration with industrial groups.

The influence of ion beams on depth profiles and interfacial reactions requires studies of particle-solid interactions. The extent of atomic mixing within the collision cascade has not been extensively studied. Use of glancing angle incidence or lower ion energies has not been applied in ion sputtering or backscattering to establish the limits of depth resolution at a buried interface. Channeling techniques have only been applied to study the Si/SiO_2 interface.

The situation is reversed with the use of ion-induced interfacial reactions. The mechanism has been established, but not the application. Further studies are required to determine the properties that would be useful in industrial applications.

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CHARACTERIZATION OF MATERIALS AT SMALL DIMENSIONS

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CHARACTERIZATION OF MATERIALS AT SMALL DIMENSIONS

1.0 INTRODUCTION

The characterization of materials at small dimensions requires the concerted measurement of chemical, structural and functional (e.g., electrical, magnetic) properties concomitant with sufficient understanding of their interaction to enable reproduction of the material. The measurement of these properties becomes increasingly difficult as: (i) the form of the material changes from bulk to film to surface, (ii) the physical size decreases from crystal or slice to chip to individual device element, and (iii) the elemental concentration decreases from major component (> 0.1%) to dopant (1 to 1000 ppm) to trace (< 1 ppm). With the emergence of sub-micron technologies the three trends just described are happening simultaneously. The question that arises is "What is the current status of sub-micron materials characterization technology?". Larrabee,[1] Evans[2,3] and Wittry[4] have reported comprehensive reviews of the capabilities of materials characterization techniques for surface, thin film and microvolume analysis.

2.0 STATUS OF CURRENT WORK

2.1 CHEMICAL ANALYSIS

When surface (X-Y plane) or in-depth profiling (Z) analysis (< 100 Å thick sections) or microvolume analysis (< 10μm x 10μm x 10μm) are required, the number of applicable characterization techniques become highly restricted. These are generally electron or ion beam techniques with electron beam techniques being the ones employed for high spatial resolution, < 1μm. This is graphically illustrated in Figure I which shows the detection limit for the major characterization techniques as a function of the diameter of the analyzed area. The line for each characterization technique starts at the top of the chart and is the minimum analytical diameter for that technique. Following the line down shows that for each technique there is a mutual exclusiveness of analyzing trace amounts of elements (microanalysis) and analyzing elements in extremely small (microanalysis) volumes. Notice the lack of techniques in the lower left quadrant of the figure.

Electron beam characterization techniques are inherently insensitive. Auger spectroscopy has 0.1% - 1% detection limits for all elements while the electron microprobe has 100-1000 ppma. Obviously these techniques cannot be used to analyze for dopants or trace impurities. There are no known electron beam techniques nor any under development that have this capability. The basic limitation is getting enough electrons for excitation yet not vaporizing or destroying the sample. The field emission electron gun has provided the best spatial resolution capability for major component (> 0.1%) analysis. Venables, et al,[5] presents convincing data supporting 300 Å resolution using a scanning Auger microprobe. This data is supported by the Monte Carlo calculations of El Gomati and Prutton.[6] Goldstein and Williams[7] have reported < 200 Å resolution using a scanning transmission electron microscope (STEM) with a field emission gun and a Si(Li) x-ray detector. Issacson and Johnson[8] using a STEM with an electron energy loss analyzer have reported detection limits of 10^{-18} gram with spatial resolutions of 100 Å.

Ion beam techniques do not have the high spatial resolution normally associated with electron beam techniques. The best that the ion microprobe can achieve (see Figure 1) is 2.5 μm and this is accomplished at a 1000 fold penalty in sensitivity. Thus while the ion microprobe has good elemental sensitivities ($\geq$ 1 ppma) it requires areas as large as 100 x 100 μm and this makes it of limited use for microvolume analysis. Since the ion microprobe is a secondary ion mass spectrometer, the technique has mass interferences from the matrix species, e.g., SiH^+, Si_2O^+, in the case of silicon. These interferences limit the elemental sensitivity for certain elements in each matrix, e.g., phosphorus, arsenic, iron, cobalt, nickel, in silicon. These mass interferences limit sensitivities for such elements to > 20 ppma and this is a serious limitation for in-depth profiling of ion implanted and diffused materials. Improvements in vacuum would appear to be useful in decreasing the species which contribute to mass interference. Using a cesium ion source for excitation has improved the sensitivity for certain elements, e.g., As in Si,[9] Se in GaAs.[10] Where there are no mass interferences this technique performs exceptionally well for in-depth profiling for both dopants and impuri-

ties, but not at sub-micron dimensions. Ion beams of gallium as small as 0.2 μm have been reported[11] but not applied to the characterization of materials.

Rutherford backscattering of 1-3 MeV helium ion particles can provide in-depth (or Z) concentration profiles with 50 Å resolution.[12] Sensitivity is in the 10-50 ppma range. This is obviously not as good as the ion microprobe and is not applicable to dopants. However, Rutherford scattering is readily quantitated directly from the physics of the scattering process. This is a powerful asset for this technique. This technique has a spatial resolution of only 1-2 mm and thus its applicability in the context of this paper would be for quantitative in-depth profiling.

Photoelectron spectroscopy utilizes x-ray and ultra-violet radiation to determine the chemical composition (as opposed to elemental composition) of a surface. Photoelectron spectroscopy is a surface technique with elemental sensitivities in the 0.1 to 1% range. When used with ion sputtering, in-depth profiling with 20-30 Å resolution is possible. Spatial resolutions are limited to 1-2 mm. Synchrotron radiation has been receiving increasing attention[13] as a versatile excitation source for this technique because of its high intensity and continuous available energy range from the visible to hard x-rays.

In summary, for in-depth profiling, all characterization techniques except the ion microprobe have inadequate sensitivity for dopants and trace impurities. The mass interferences associated with the ion microprobe prevent achieving adequate sensitivity for some elements in every matrix.

2.2 SURFACE IMAGING

Secondary electron microscope (SEM) has matured[1] to the point where spatial resolutions of 20 Å are possible when field emission electron sources are used. Most conventional tungsten filament electron sources provide 70-100 Å resolution. These will be adequate for all characterization work at small dimensions.

2.3 PHYSICAL DEFECT CHARACTERIZATION

Physical defects are detected and imaged by the deflection or absorption of x-rays, electrons or ions. X-ray diffraction and topography are effective tools for examining crystals, slices and devices. However the physical defect, or strain field generated by the defect must be larger than 1 μm in size. The detectability or sensitivity of x-ray techniques to defects are controlled by signal (defect) to noise (fluctuations in Bragg angle deflected) and improvements are only possible by using double crystal techniques. Double crystal techniques are not widely employed because of difficult experimental problems. Computer control could circumvent many of these problems but has not been attempted.

For sub-micron defects, as with sub-micron chemical characterization, only electron beam techniques can be used. The transmission electron microscope and its more recent evolution, the scanning transmission electron microscope (STEM) are capable of imaging defects with resolutions in the 2-5 Å range. The use of field emission electron sources in these instruments has greatly expanded their applicability because of the very fine (1-2 Å) and highly intense electron beams. The addition of other detectors to the STEM system to measure x-rays, secondary electrons and "energy-loss" electrons has made these instruments truly state-of-the-art for characterization of physical defects.[14]

Rutherford backscattering of 1-3 MeV helium ions has recently been extensively applied to the measurement of crystallographic perfection in the near surface (top 300 Å) and at depth (up to 5000 Å) for laser annealed silicon[15] and GaAs.[16] As described earlier, this technique can also measure the ion implanted impurity distribution. This represents the best technique for measuring physical defects in the outer few thousand angstroms of a material.

The establishment of electrical behavior of physical defects continues to be a problem. Electron beam techniques can be used to detect electrically active centers with spatial resolutions in the order of one micron.[17] Resolution is limited by carrier diffusion length and not by the diameter of the electron beam.

In summary, electron beam techniques are available to image and to establish electrical activity of many physical defects in materials.

2.4 FUNCTIONAL PROPERTIES

The measurement of the functional properties, e.g., electrical, magnetic or display at sub-micron dimensions is not readily achievable. Normally the integrated or system function of the device/material is measured and then correlation with chemical and physical defects and properties is attempted. Even in the case of the more established technologies such as silicon, gallium arsenide and magnetic bubbles, the signal to noise problem virtually precludes this type of measurement. Considerable success has been achieved for silicon and the III-V compounds in measuring trace levels (as low as 2×10^{-7} ppma) and establishing their electrical behavior using deep level transient capacitance spectroscopy (DTLS).[18] Petroff, et al,[17] used the scanning transmission electron microscope coupled with a DTLS system to obtain DLTS images with resolutions of less than 10 μm. It is not clear that sub-micron resolutions will be attainable.

3.0 TECHNOLOGY NEEDS

The technology needs for the characterization of materials at small geometries is clear. Better sensitivities at small geometries for chemical analysis is vital. This is readily apparent in Figure 1 where the lower left quadrant is void of characterization techniques. Field emission guns have provided the required brightness for electron sources. Now, more efficient detection systems are required. Electron energy loss spectroscopy appears particularly exciting both with regard to spatial resolution and detectability. Other similar advances in new detection systems are needed.

Ion beam techniques need to have enhanced resolution; going from the current 2.5 μm to $\sim$ 100 Å. When this occurs brighter ion sources will be required to even maintain current sensitivities. More efficient detection systems are also required. Improved mass resolution (current 300 going to 10,000) better vacuums at the sample (current 10^{-7} torr going to 10^{-10}) and new ion sources (e.g., iodine, gallium, etc.) will alleviate much of the mass

interference problem in ion microprobe work.

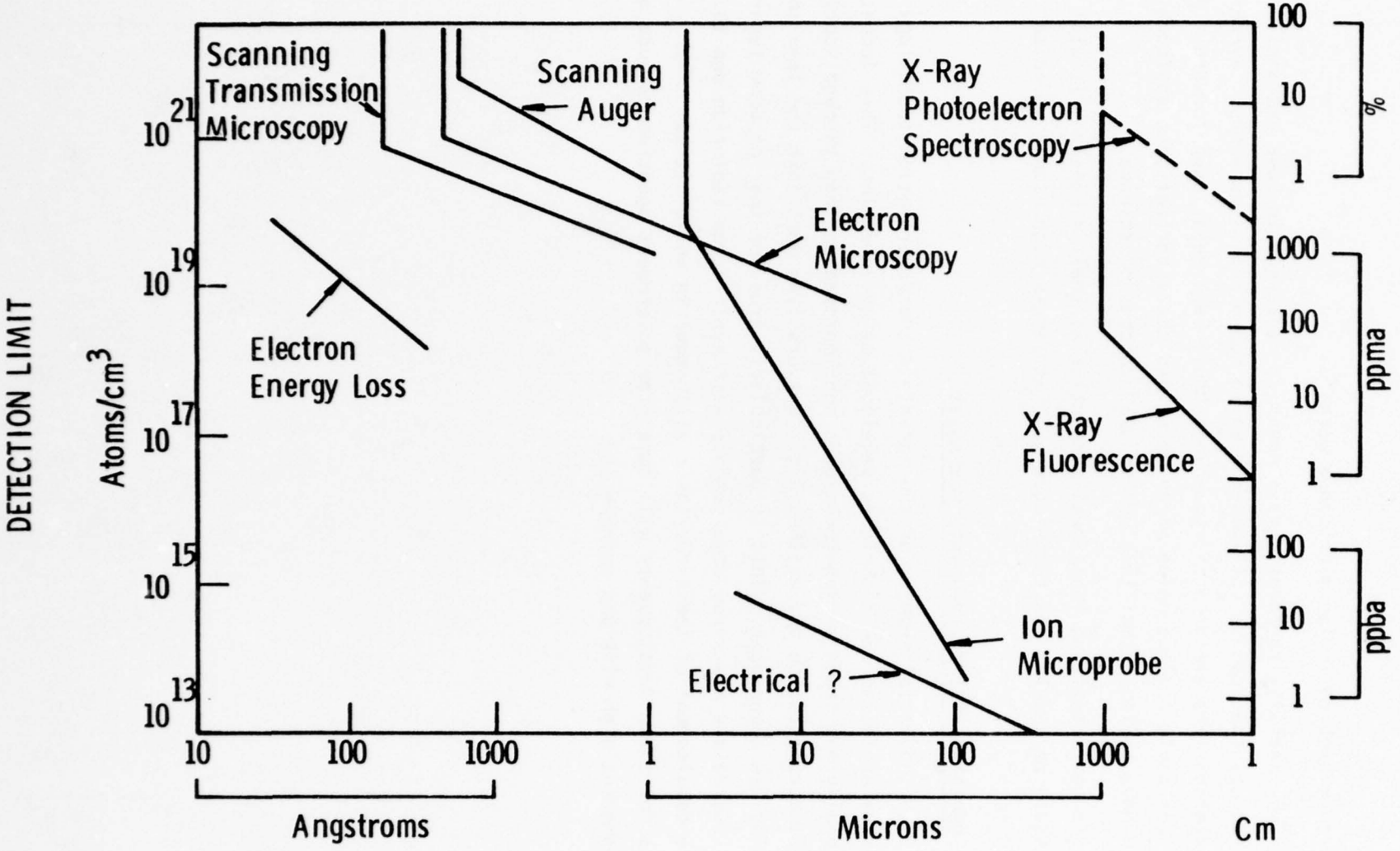
The inability to focus x-rays makes it necessary to have extremely bright sources that can be collimated down to sub-micron dimensions. Synchrotron radiation from electron storage rings could be a major step forward. An x-ray laser would revolutionize x-ray materials characterization techniques. It would have obvious rammifications in all branches of science.

In characterizing functional properties at small dimensions it will be necessary to develop new techniques with extremely high signal to noise ratios.

4.0 OPPORTUNITIES TO INDUSTRY/UNIVERSITY

The industrial segment of the materials characterization technology have always exploited new techniques developed at universities. This industry traditionally has taken proven techniques and improved on them through sophisticated instrumentation and engineering. Universities must take the lead in developing new techniques. This is particularly true for the ion beam techniques. Certainly new x-ray developments with synchrotron radiation and the ultimate development of the x-ray laser will occur in universities. The stimulus for these developments will come from government agencies because of their inherent high risk and expense.

EFFECT OF DIAMETER OF ANALYZED AREA
ON DETECTION LIMIT



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MICROCHARACTERIZATION

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INTRODUCTION.

As we consider the drive to smaller dimensions, microcharacterization takes on considerable importance. We must not only devise pattern and mask making capability, materials processing and safe handling procedures at the small dimensional limits, we must also develop chemical and electronic structural diagnosic capability at this level also. These notes will be concerned with a projection into the future and represent an attempt to identify gaps in our existing understanding, techniques and technology and make recommendations as to how these gaps might be rectified.

A preliminary task is to identify some of the base assumptions. In the immediate future, development of semiconductor technology will continue to reduce size scales of structures laid down on the surface of bulk chips. Surface probes (SEM, SAM etc.) will continue to be of crucial importance and work will continue to be necessary to develop the diagnostic imaging techniques that tell us what is there, chemically and electronically, and where it is. Equally, looking to the long term future, the physics of the scattering process indicates that the most direct path to 'nano lithography' is the use of thin films on which the structures are written. Thin films will also be easier (though not 'easy') to characterize at the small lateral dimensions. Chemical and electronic characterization of thin films at a spatial resolution sufficiently below the lithographic scale therefore becomes an important factor in extending limits into the submicron region. Finally, much of the science in this region will involve the physics and chemistry of surfaces, edges and line structures. A knowledge of the chemical and electronic morphology

of defects and interface structures will be badly needed.

Since electrons are readily focussed and handled, many of the existing techniques and the prospects for the future are centered around the exploration of small, intense electron beams. This document will focus in that area since small electron probes are at the heart of both many of the observational tools (e.g. SEM, SAM and STEM) and the electron beam lithography systems. Some developments are of value in both types of systems. Nevertheless, the prospects of development of small probes of X-rays, ions and other particles do exist and should not be overlooked.

CURRENT-STATE-OF-THE-ART.

Larrabee[1] has surveyed the current instruments available for characterization. I would like to inject a projection of the future giving a somewhat different perspective on the techniques and the steps necessary to push back the existing limits. When an electron interacts with the sample, a wide variety of effects occur. Utilization of a wide variety of these effects gives the wide variety of acronymic probes we currently use. One can ask the question what are the ultimate limits of detectability--in chemical constitution, spatial resolution, spacings of electronic energy levels etc. that can be identified? Thus with a SAM system detection of surface structures down to 300Å has been achieved with a field emission gun,[2] use of 'low-loss' imaging techniques gives a SEM resolution of 30Å[3] and X-ray microprobe (for high Z elements[4]) and electron energy loss techniques (for low Z elements such as Al, Si, O, C etc.)[5] in transmission in thin films give a chemical analysis capability down to the 30Å region. Microdiffraction techniques give an area limit of ~ 20Å.[6] These achievements represent chemical detection in the order of

10^{-18} to 10^{-19} gm or ~ 5,000 atoms. Similarly, use of cathodoluminescence and scanning deep level transient spectroscopy resulting from the scanning beam also is leading to the study of electrical activity on a scale down to ~ 200 Å[7]. The procedure limits identified above are by no means routine and represent achievements in particular laboratories and particular systems that are not necessarily readily duplicated. They demonstrate that characterization in the submicron range can be achieved but the experiments also identify and epitomize some of the real problems that need to be attacked and solved.

SCIENTIFIC AND TECHNOLOGICAL NEEDS AND OPPORTUNITIES.

The achievements listed in the previous paragraph were achieved in many cases in somewhat unique situations with some difficulty. In all cases, ultimate limits will be governed by signal/noise considerations and attention has to be paid to both enhancing and optimizing the signal and minimizing the noise. In some of the situations described above, the techniques are so sensitive that some problems are accentuated. In the particular area of analytical electron microscopy using techniques such as STEM energy loss, X-ray fluorescence in transmission, recent workshop at Cornell University[8] offer some guidance. Somewhat similar comments can be made about some of the areas but space does not permit such assessment here.

Three relatively major problems can be identified

(a) contamination of the specimen either inside the instrument or by preparative techniques

(b) radiation induced effects in the specimen

(c) interference with the desired signal of either instrumental or specimen origin (i.e. background).

Procedures to alleviate the difficulties caused by these can be developed. Thus, very clean vacuum systems are needed along with considerable care and specimen preparation. Specimen transfer stages in which specimens can be transferred from one UHV system to another are necessary. Radiation damage limits need to be explored to insure that the optimum lifetime is attained. For example, lower temperature apparently gives longer lifetimes. Perhaps, low current densities permitting dynamic recovery of damage may also permit improvements. System data collection efficiencies need attention to ensure that all possible contributions to the useful signal are obtained. Background problems have to be solved by careful design of the apparatus to minimize experimental contributions, precise measurements (e.g. use of counting techniques to avoid noise contributions from electronics) and well understood subtraction techniques. Precise measurements imply high mechanical and electrical stabilities and control of the incident probe current and voltage. There is some evidence and opinion that for transmission techniques in the thicker samples, advantages are obtained by operation at higher voltages such as 300keV[8,9]. Multiple scattering effects are reduced, thus improving the signal beam spreading can be reduced and thus higher oxidation can be achieved or thicker samples can be studied. Finally, achievement of sensitivity limits implies that efficient use is made of every available electron or signal from the specimen. Thus efficient detectors that collect over the optimum detection angle in parallel could enhance sensitivities by a considerable factor.

Based on the above, general areas of research opportunities and needs can be identified as follows:

(a) Many of the instruments used in characterization rely on the use of electron beams in a wide variety of forms. Electron optics is not a dead subject and is crucial to many of these systems. There have been a number of developments over the past twenty years that attest to the health of this area. These include development of scanning techniques, field emission gun, high excitation lenses and so forth. There is every reason to expect that continued attention to new sources, and detection systems will pay off immensely. Improving the stability of the field emission gun, increasing the collection efficiencies of spectrometers, higher performance lenses at both the high and the low voltage ends of the specturm, parallel detection systems and so forth are just a few of the items needed to enhance the efficiency of the detection processes and which can be described under the general term electron optics.

(b) A second major need and opportunity is in the area of electron interaction with the specimen. In developing the optimum methods of probing the sample, i.e. to develope truly quantitative methods, we need to know how best to set the parameters--beam intensity, voltage, collection efficiencies and so forth. We need to know how to subtract background and how the background might be modified by interaction with the sample. Radiation damage limits must be understood. All of these items call for a deepened understanding of electron scattering. The new techniques are precise to a point not previously met. Scattering differential cross-sections are needed at a level not currently available in the literature and efforts should now be made to enchance the precision with which experimental and theoretical values for cross-sections are known. Multiple scattering and the interaction of elastic with inelastic cross-sections are factors that could cause

problems if not mastered. An understanding of electron scattering is an important basic underpinning to such studies.

(c) A third comment which will not be expanded much in these pages is that somewhat similar remarks can be made concerning the use of optical and other particle probes. Such probes are very valuable in determining average surface physics and chemistry but have so far not extended dramatically into lateral microcharacterization. The successful development of Fresnel zone plates may dramatically change this and effort should be devoted to development of this.

OPPORTUNITIES FOR UNIVERSITIES, INDUSTRY AND GOVERNMENT.

In general, we may expect industry to use the characterization techniques available at the commercial state-of-the-art. Innovation of new techniques is carried on at a few industrial laboratories but an overwhelming case usually has to be made. Historically, instrumental and technique innovation has developed in the laboratory of an innovative user[10] often in Universities. It is then picked up by an instrumental manufacturing company on the basis of a perceived or demonstrated demand, engineered and sold. Universities, in particular, are suitable places to undertake high risk innovative work that an industrial company cannot undertake and it is important that this be recognized as an appropriate avenue for instrumental innovation. In the past eight years or so, it has been extremely difficult to undertake such efforts. I urge that methods be sought for the adequate support and encouragement of innovative instrumental efforts of a suitable quality. Adequate support would have to include provision of suitable engineering support (including machinist, digital and electronic hardware etc. as needed).

As indicated in the text above, many techniques appear to be of value using light optical or particle probes. In many of these areas, the United States has a strong base of skilled scientists and technologists and no particular problem is encountered. In one area, however, electron optics and to some degree electron scattering, a gap does exist. Not many individuals are trained in this country in these areas and most efforts of significant quality in industry rely on individuals trained overseas. We emphasize that we are not including the substantial effort in the application of electron optical instrumentation per se. Significant and highly skilled use of electron optical instrumentation is made for the solution of problems in materials science and biology but the efforts devoted to extending the limits of the techniques, development

In contrast, Japan and Western Europe have had extensive university based programs along with large professional laboratory efforts in these areas. Efforts of any quality seen in this country reflect in cases a part-time program of individual faculty members. Instead of a sustained group effort, making possible adequate support resources at an economic level and a large enough group of individuals to make formal classes and seminar speakers welcome, only fractions of faculty time are devoted to these topics with the help of postdoctorals trained overseas. U.S. efforts have been innovative and effective. However, the typical pattern is for the response to the innovation to appear overseas and after a period of several years to filter back to the large user community in this country.

Electron optics and electron scattering are likely to play an important role in the submicron region. It appears particularly dangerous to rely on overseas sources of trained personnel. Thus, it appears important for at least a few Universities to develope active groups capable of providing the trained individuals in this area and of attacking the high rise, speculative work that industry usually does not attempt.

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LASER ANNEALING

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I. INTRODUCTION

The use of high-power lasers in a variety of materials processing steps is a rapidly growing technology.[1] Well-developed applications include drilling, cutting, and welding, while other applications such as surface alloying, laser shock hardening, and laser glazing are still under development.

Very recently, there has been a sharp increase of interest[2] in the use of laser radiation for annealing the lattice damage due to ion implantation of dopants into semiconductors. Pioneering work[3-6] on laser annealing by Soviet scientists, has stimulated research activities throughout the world,[7-16] primarily because laser annealing appears to offer distinct advantages over thermal annealing for processing implanted materials. For example, because the laser light is heavily absorbed in the near-surface region of the sample, the very high temperatures necessary for annealing the lattice damage are created. The absorbed photon energy, however, is not great enough to raise the temperature of the undamaged substrate significantly and thus undesirable side effects of high temperatures in this region are avoided. Another advantage is that laser annealing can be carried out in air because the annealed region cools so quickly that pick-up of significant amounts of impurities from the atmosphere is circumvented. A third, and potentially very important, advantage of laser annealing is the capability it provides for performing extremely well localized annealing[10] of selected areas of an implanted sample. Finally, laser annealing is a very simple process since the annealing can be accomplished merely by illuminating the implanted material with laser radiation of appropriate wave lengths and energy densities.

Two other processes closely related to laser annealing of ion-implant damage are laser-induced diffusion of surface-deposited films and laser breakup of dopant precipitates in thermally-diffused materials. These three processes have so many characteristics in common that "laser annealing" will often be used to refer to all three.

The remainder of this report is divided into five sections. In the next section, the types of lasers which have been used for annealing and their similarities and differences will be briefly discussed. In Section III, several of the better-established and understood experimental and theoretical results of work on laser-annealed silicon will be reviewed. In Section IV, problems which have been encountered with certain aspects of laser annealing, desired laser characteristics, and important areas where more information on materials properties is needed will be discussed. Possible implications of laser annealing for the fabrication of microstructures and possible impacts on a number of fields are given in Section V. Finally, in Section VI some obvious opportunities for research and development in the area of laser annealing and its extensions will be mentioned.

II. TYPES OF LASERS USED FOR ANNEALING

Lasers used for annealing are of both the continuous wave (CW) and pulsed type. Most of the reported work has employed either Q-switched ruby[4,7,13] and Nd:Yag lasers[5,9] or CW argon-ion lasers operated in a scanning mode.[6,12] The pulse duration of a Q-switched laser can be varied between approximately 20 and 100 nsec and annealing can be achieved by choosing an appropriate combination of photon energy density and pulse duration time. Depending on a number of factors, particularly the application and the available laser power, annealing with a single pulse may give satisfactory results. However, pulsed lasers can also be operated in a quasi-scanning mode in which annealing is accomplished by overlapping many pulses of small spatial extent but high energy density. Annealing has been reported in the literature with beams as large as 2 cm in diameter and as small as 40 μm, but privately the author has been told of effective annealing with beams as large as 5 cm in diameter and as small as 1.5 μm. Small beam sizes are of obvious importance for microstructure fabrication. Annealing can be achieved with a CW laser by varying the output of the laser and the rate at which the photon beam is scanned across the sample. Annealing with CW lasers of 40 μm beam diameter has been reported but presumably the beam could have been focussed to smaller dimensions. The mechanisms giving rise to annealing with the two different types of lasers appear to be quite different and this will be discussed briefly later in this report.

III. REVIEW OF SELECTED EXPERIMENTAL AND THEORETICAL WORK

Most of the results reported in this section were obtained using a Q-switched ruby laser operated with a pulse duration time of approximately 50 nsec and an energy density incident on the sample which was varied between 0.6 and 3.0 J/cm^2. Annealing was usually accomplished with a single pulse but larger samples required a few overlapping pulses. Semiconductor-grade, single-crystal silicon was used as the substrate material and the implanted dopants included B, P, As and Sb in doses ranging from 10^{14} to 10^{17} ions/cm^2. Implanting was done at room temperature under high vacuum conditions (2×10^{-8} Torr) and at energies that ranged from 35 keV to 100 keV.

A. Annealing of Lattice Damage Induced by Ion-Implantation

The removal of implantation-induced lattice damage by laser and thermal annealing was studied by transmission electron microscopy for the cases of B, P and As ions implanted into silicon.[7,17,18] The results showed that no damage remained in the laser-annealed specimens down to the resolution of the microscope which was approximately 10 Å. In contrast, after thermal annealing, significant damage remained in the form of dislocation loops. The total lack of irregularities in electron diffraction patterns from laser annealed samples showed that the implanted region had annealed with

the same lattice orientation (001) as the substrate. The results of measurements on P, As and Sb implanted Si crystals[19] with Rutherford ion backscattering and ion channeling techniques showed directly that the long-range, crystalline order had been restored to the implanted region by laser annealing, thus verifying the transmission electron microscope results. Together these measurements show that laser annealing is much more effective in removing displacement damage and restoring crystalline order than is conventional thermal annealing.

B. Dopant Profile Changes During Laser Annealing

Pulsed-laser annealing produces a redistribution of dopant profiles; this is shown in Fig. 1 for the case of B, P, and As implanted into silicon.[20,21] The profiles for B and P were measured by secondary ion mass spectroscopy (SIMS) and that for As was measured by Rutherford backscattering. Diffusion coefficients in the solid state are far too small to explain the redistribution of these dopants. Recognition of this fact led to speculation in the earliest Russian literature that the near-surface region actually melted during annealing with pulsed lasers. Annealing with scanned CW lasers is seldom accompanied by dopant redistribution and it is currently believed that this implies that the implanted region does not melt.

C. Macroscopic Theory of Laser Annealing

Recent calculations,[22] give convincing evidence that the near-surface region of silicon samples can be melted by pulsed-laser radiation. The same calculations show further that, because diffusion coefficients in molten silicon are almost seven orders of magnitude higher than in the solid, the spreading of dopant profiles during laser annealing is readily explained. Thus, the beginnings of a macroscopic theory of laser annealing with pulsed lasers has been well established. The most significant results of these calculations are given in Figs. 2 and 3. Figure 2a shows calculated temperature profiles at the termination of the laser pulse. The upper curve is a typical temperature distribution obtained from an analytical solution of the one-dimensional heat conduction equation when melting is not allowed and the thermal conductivity and specific heat are assumed to be constant with temperature. The lower curve was obtained from numerical solution of the same equation generalized to allow for the possibility of a phase change (melting) and for temperature-dependent thermal conductivity and specific heat. As shown by this curve, at the termination of the laser pulse the crystal was melted to a depth of almost 0.85 μm.

From a series of curves such as the lower one in Fig. 2a, the position of the melt front as a function of time can be determined; typical results are shown in Fig. 2b. The melt front very rapidly penetrates to a depth of about 0.95 μm in the solid, before receding back to the surface with an average velocity of approximately 270 cm/sec. While this occurs, a region that is almost 5000 Å thick remains in the molten state for a few

hundred nanoseconds during which time the dopants can diffuse in liquid silicon where diffusion coefficients are so much higher than in the solid. Figures 3a and 3b compare experimental profiles for B and As after laser annealing with profiles calculated by assuming that the implanted ions diffuse in liquid silicon; the agreement is obviously very good. From the calculated profiles, values of the square of the diffusion length ($D\tau$) can be obtained. Using these results and literature values for the diffusion coefficients in liquid silicon, values for the diffusion time (τ) can be extracted. The resulting times of 180 nsec for boron and 270 nsec for arsenic are in good agreement with the melt front predictions of Fig. 2b.

Based on the above results, the pulsed laser annealing process can be pictured as follows. The incident laser light melts the crystal to a depth greater than that of the implanted profile. The melted region then recrystallizes from the underlying substrate by means of liquid phase epitaxial regrowth, resulting in defect-free single crystal material with dopants in substitutional sites in the silicon lattice. During the time the implanted region is molten, dopants can diffuse in the liquid where diffusion rates are much higher than in the solid. Similar conclusions regarding melting of the sample in the case of Q-switched laser annealing have been reported recently by others.[15]

Redistribution of dopants during pulsed-laser annealing contrasts sharply with results which have been obtained using a scanned CW Argon laser for annealing.[12] As stated earlier, annealing of lattice damage and incorporation of dopants into substitutional lattice sites was found to occur in the absence of dopant redistribution. It was suggested in reference 12 that the mechanism for annealing with the scanned CW laser is solid phase epitaxial regrowth. More recent experimental work tends to further validate this suggestion. Calculations of temperature distributions during scanned laser annealing tend to confirm that melting does not occur, but the temperature-time regime required to achieve annealing is still the subject of debate.

D. Change in Lattice Symmetry Induced by Laser Annealing

The silicon lattice undergoes a significant one-dimensional contraction or expansion in the implanted region during laser annealing[24] and as a result, the symmetry of the lattice in this region is lowered from cubic to tetragonal. The physical size (ionic radius) of the dopant atom relative to that of the silicon atom it displaces in the lattice determines whether the lattice will expand or contract. For example, the atomic radii of B and P are less than that of Si, and these ions produce a net contraction in the implanted region; Sb which is larger than Si causes the lattice to expand; and As which is very nearly equal in size to Si produces no change. The one dimensional lattice changes produced by laser annealing at these dopant concentrations of approximately one atomic percent appears to be a unique property of laser annealing. It should be noted that the concentrations far exceed the limits of conventional solid solubility. In thermal annealing, misfit dislocations destroying the one-dimensional

nature of the lattice change would be expected at such high concentrations, if they could even be obtained without precipitation. The one-dimensional aspect of the change arises from the fact that the adherance to the underlying crystal planes of the substrate prevents changes in the plane of the sample, thus leaving lattice parameter changes only along the surface normal. The time scale associated with annealing apparently is too short for the introduction of misfit dislocations which would tend to relieve the strain and destroy the one-dimensional nature of the lattice parameter change.

There is a large body of both experimental and theoretical literature on the effects of uniaxial stress on the electronic properties of semiconductors. It will be interesting to see how some of the results of this work will correlate with the results of similar work on laser annealed samples.

E. Improved Electrical Properties

We have already seen that laser annealing is more effective than thermal annealing in incorporating the dopant ions into the lattice at substitutional sites and hence it should also be more effective in electrically activating the dopant. Measurements[7,19] of the electrical carrier concentration after laser and thermal annealing for a wide range of implanted doses and atomic species confirm this. In fact, since the equilibrium solubility limit cannot be greatly exceeded in conventional thermal annealing, the carrier concentration as a function of implanted dose saturates, whereas in laser-annealed material it continues to increase linearly up to the highest doses used to date.

In the earliest Soviet literature on the subject, it was noted that laser annealing did not significantly reduce the minority carrier lifetime (MCL) in the substrate. Extensive measurements[7] at Oak Ridge confirm that values of the MCL in the base region before and after laser annealing are very nearly equal, whereas thermal annealing at 1100°C for 30 minutes reduces the MCL by a factor of about 10. A comparison of the quantum efficiency of laser- and thermally-annealed ion-implanted silicon cells shows that the response of the laser annealed cell is superior throughout the entire solar spectrum. The superior response in the red region correlates very well with the retention of a long MCL in the laser-annealed sample. The improvement in the blue region can be attributed to the almost complete absence in the laser-annealed cell of any lattice damage which might give rise to trapping and excessive electron-hole recombination. If this interpretation is indeed correct, then it shows once again the ability of laser annealing to remove the lattice damage in the implanted region while retaining the electrical properties of the substrate.

F. Laser-Induced Melting and Diffusion

The very fast melting and recrystallization characteristic of annealing with pulsed lasers may also find applications in materials processing not directly related to ion implantation. For example, thermal

diffusion results in the formation of a surface layer several hundred angstroms deep containing a very high concentration of electrically inactive dopant atoms in the form of precipitates. It has been shown[25] that after irradiation of a boron-diffused sample with a single laser pulse, the dopant profile is significantly redistributed and the boron contained in the precipitates is dissolved into solid solution, with an order of magnitude increase in the electrical activity. Laser treatment of these diffused crystals has also been found to improve the p-n junction characteristics as determined from measurements on mesa diodes.

Laser radiation has been used recently to form large area p-n junctions in silicon by a process of laser-induced diffusion.[26] For this application, the dopant (B or Al) is evaporated onto the sample surface as a film approximately 100 Å thick and the sample is then irradiated with pulsed-laser light. The dopant diffuses into the near surface region of the silicon and becomes electrically active. The technique of laser-induced diffusion has been applied to the fabrication of solar cells and efficiencies comparable to those of laser-annealed, ion-implanted cells have been obtained. This type of processing may become especially important for the formation of large area p-n devices such as solar cells because it by-passes the ion-implantation step and, with slight modifications, it can probably be carried out completely at room temperature. This appears to be an attractive method for fabricating a variety of devices which require shallow p-n junctions.

Laser-induced melting may also find application as a method for purifying the near-surface region of materials during processing. Recent results obtained for Cu-implanted silicon after laser annealing, show that all of the implanted Cu was segregated to a region within the first few hundred angstroms of the surface where it could be removed by etching. Segregation of Cu to the surface is apparently the result of its very low segregation coefficient from the melt. Segregation of Fe and Pb to the surface of silicon samples has also been observed after pulsed laser irradiation.

IV. PROBLEM AREAS IN THE UNDERSTANDING AND DEVELOPMENT OF LASER ANNEALING

The discovery that lasers could be used to very effectively anneal the lattice damage due to ion-implantation of silicon and gallium arsenide has occurred so recently that is is difficult to foresee what even the short developments will be. Clearly, laser annealing will be tried for p-n junction formation and device fabrication in a variety of semiconducting materials. However, it seems likely that the combination of ion-implantation and laser-annealing will have much wider applications and some of these will be mentioned later in this report. Here, some problem areas in which increased knowledge would greatly enhance our understanding of laser annealing will be briefly discussed.

Control of energy deposition. Laser annealing is a technique which is sufficiently sensitive to the energy deposition process that good control of this process is essential for understanding the technique and, to a lesser

extent, for applying it. For pulsed lasers this implies a high degree of control of pulse size (energy), spatial homogeneity, temporal shape, and duration time. Of somewhat lesser importance, but still highly desirable, would be a tunable laser with wavelengths in the 1-4 eV range. For applications to solar cell fabrication where low cost and a high degree of automation are especially important, laser efficiency, reliability, and lifetime are important considerations. Hence, the development of special lasers for laser annealing seems almost inevitable.

Absorption and reflectivity data for materials subjected to intense laser irradiation. In order to thoroughly understand the mechanisms by which the laser energy is deposited in the material, it will be necessary to greatly expand the meager body of data which now exists on the optical properties of ion-implanted materials subjected to high-intensity irradiation. Ion implantation creates a high degree of disorder in the near-surface region of the implanted material and in some cases this region may be driven completely amorphous. Undoped amorphous silicon has an absorption coefficient at 0.694 μm, approximately an order of magnitude higher than undoped single crystal silicon. High doping levels such as those encountered in ion implantation can produce very large changes in the absorption coefficients. Also pseudo-two photon processes may become important at high light intensities. Thus, the absorption coefficient, which determines how the laser energy is deposited into the crystal, is expected to be a complex function of the lattice damage, the doping level, laser wavelength, laser intensity, temperature, phase changes, and probably other parameters. The reflectivity of the material also depends on many of the same parameters, especially the transition from solid to liquid phase.

Thermal properties of materials at high temperatures. During laser annealing the material undergoes extremely large temperature changes in very short times. To obtain reliable theoretical modelling of the annealing process it is necessary to know the temperature dependence of any parameters entering into the calculations. For example, the thermal conductivity of most materials varies greatly with temperature. Although the thermal conductivity of silicon has been measured over a wide temperature range below the melting point, this is not true for most semiconductors. Measurements above the melting point are needed for all materials.

Mass transport in the liquid phase. There is little doubt that dopant profile broadening during laser annealing involves mass diffusion in the liquid. In order to calculate this broadening, it is necessary to have an accurate value of the diffusion coefficient D for the particular dopant-host combination under consideration. To illustrate how unsatisfactory the situation is with respect to reliable values of D, let us consider the case of silicon for which there is more data than almost any other semiconductor. Values of D for several impurities in molten silicon were reported in 1963 by Kodera[27] and by Shaskkov and Gurevich[28] in 1968. Kodera shows uncertainties in his values of roughly ± 30% whereas Shaskov and Gurevich show substantially smaller uncertainties. However, for those impurities common to the two studies, the ratios of the reported values range from

approximately 1.5 for boron to about 40 for indium. In fact, the situation is so bad that if a few of the other parameters in laser annealing could be pinned down, fitting of the profiles could be used to determine diffusion coefficients.

Rapid recrystallization and segregation coefficients. The calculated velocity of the melt front as it returns to the surface during laser annealing of silicon is of the order of a few hundred centimeters per second. This ultrarapid refreezing is a highly non-equilibrium thermodynamic process and conventional theories of recrystallization may not apply. Some work in this area has been done on metals but more is needed and the work must be extended to semiconductors. For those impurities such as copper in silicon for which the effective segregation coefficient is low, one finds that the implanted profile is completely changed because the impurities are swept back to the surface by the melt front. Much more study of this process is needed and methods of estimating and measuring effective segregation coefficients during rapid freezing must be developed.

V. IMPLICATIONS FOR MICROMINIATURIZATION OF STRUCTURES

The use of lasers to modify the near-surface properties of materials, especially metals and alloys, is an active area of research undergoing rapid development. The modifications may entail a variety of microstructural changes which are of considerable interest in themselves but which will not be discussed here. It should be remembered that the terminology "laser annealing" as used in this report implies that impurities have been ion implanted into or deposited on the surface of the material before the material is subjected to the laser irradiation. This type of materials modification is so new that it is much too early to predict in any detail how it can be used in the microminiaturization of structures. However, laser annealing has a number of characteristics which might make it useful in microstructure fabrication.

The most obvious characteristic is that the laser beam can be focussed to very small dimensions to deliver high power densities. An entire sample can be ion-implanted and areas as small as 1 μm in diameter can be annealed to create regions of electrical activity. In these microareas, other properties such as optical reflectivity and absorptivity, thermal conductivity, etc. are also changed from their values in the surrounding material. The laser beam can be scanned across the surface in any pattern to "write" regions of modified materials properties. Quite similar effects should be obtained with laser-induced diffusion of surface-deposited layers. An obvious alternative to "writing" in microstructures would be to photograph them into the surface by laser annealing through suitably chosen photolithographically-deposited masks.

In Section III, it was shown that with laser annealing it is possible to incorporate impurities into semiconductors at concentrations which far exceed the equlibrium solid solubility limits. One result of this is that there is a one-dimensional expansion or contraction of the lattice and

hence a change of its symmetry properties in the near-surface region. The laser annealing has led to the creation of a new structure by alteration of the lattice on the level of the unit cell.

In those cases where the solubility limit has been exceeded, it is possible to cause precipitation of the impurities by conventional thermal treatment at 900°C for a few minutes. However, the precipitates can again be broken up and the impurities placed in substitutional sites. Apparently, this cycling between formation and destruction of this type of microstructure can be carried on indefinitely.

The growth of epitaxial and polycrystalline layers of semiconductors a few microns thick on suitably chosen substrates (e.g. silicon-on-sapphire) is a common requirement for the fabrication of a number of electronic devices. Non-uniformities in the doping concentrations of these layers is a common problem when the dimensions of the samples exceed about two inches in diameter. Laser annealing may prove useful in the growth and doping of these thin layers and in the removal of dopant inhomogeneities.

VI. OPPORTUNITIES FOR UNIVERSITY AND INDUSTRY STUDIES

There is a multitude of opportunities for both university and industry studies of laser annealing and its applications. At the present, there is a virtual explosion of interest in laser annealing. Almost every group working with ion implantation is either already involved or rapidly becoming so. Research on laser annealing need not be particularly expensive and most reasonably well-equipped university and industrial laboratories should be able to make contributions to the field while it is rapidly developing.

As the field becomes more mature, it is likely that some basic questions will emerge which are best tackled in a highly research-oriented university environment. For example, the physics underlying extremely rapid solidification phenomena and the incorporation of ion-implanted impurities into lattices at concentrations far above the solubility limit requires much further development. What new materials can be formed in this way? What are their properties? How stable are they? A whole host of questions come to mind.

On a somewhat less fundamental level, research in university physics and electrical engineering departments should be encouraged. For example, the development of lasers especially designed for annealing should be pursued. Commercial suppliers of lasers may rapidly push laser development to the limits of the present state of the art and still not have reached the desired goal. For economic reasons, further investment of manpower and financial resources would not be feasible. Advancement of the state of the art would then be up to the universities and larger industrial research laboratories, if they were interested.

It seems to this author that much of the near-term development and application of laser annealing will go on at industrial laboratories and

universities with very strong departments in electrical and electronic engineering and/or well-developed programs in ion implantation. Much of the work will be motivated by the potential usefulness in semiconductor device applications. If the potential is realized, the motivation for work by this type of organization will continue. On a longer term basis, however, some of the more fundamental aspects of laser annealing must be thoroughly investigated, and physics and engineering departments in smaller universities not specializing in device work should then have a great deal to contribute.

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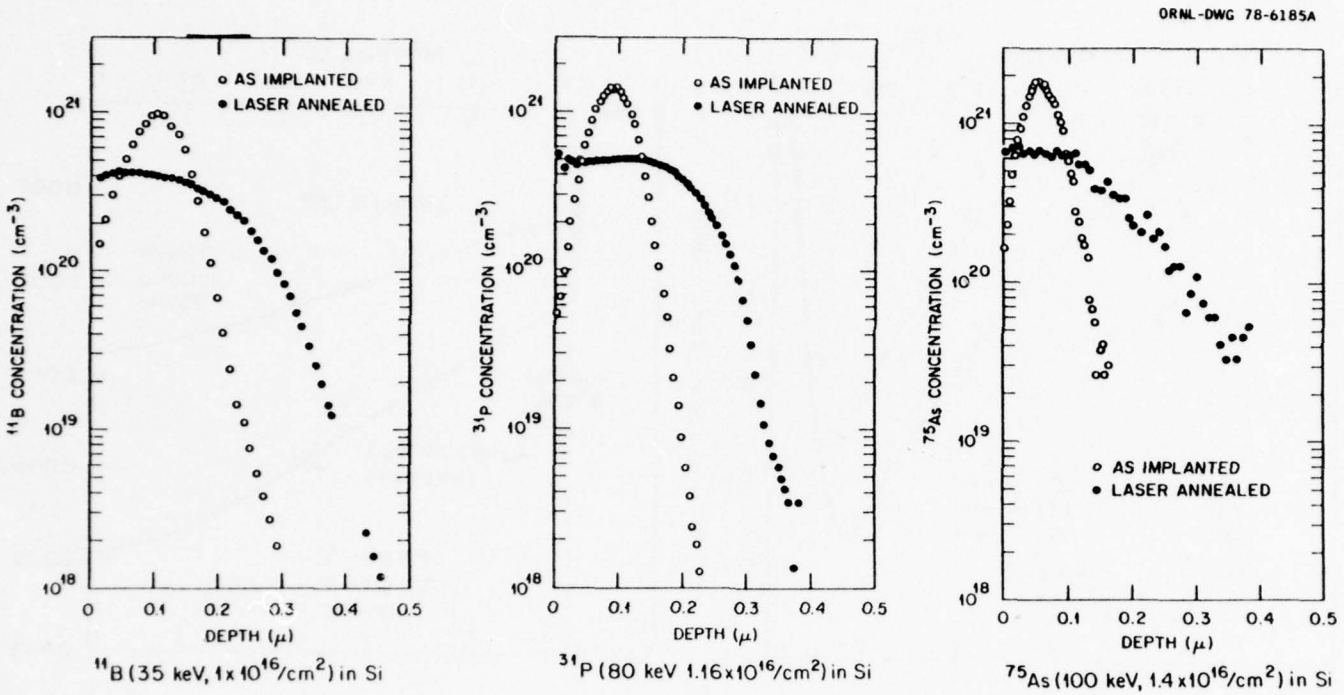

Fig. 1. Profiles of ^{11}B, ^{31}P, and ^{75}As implanted silicon.

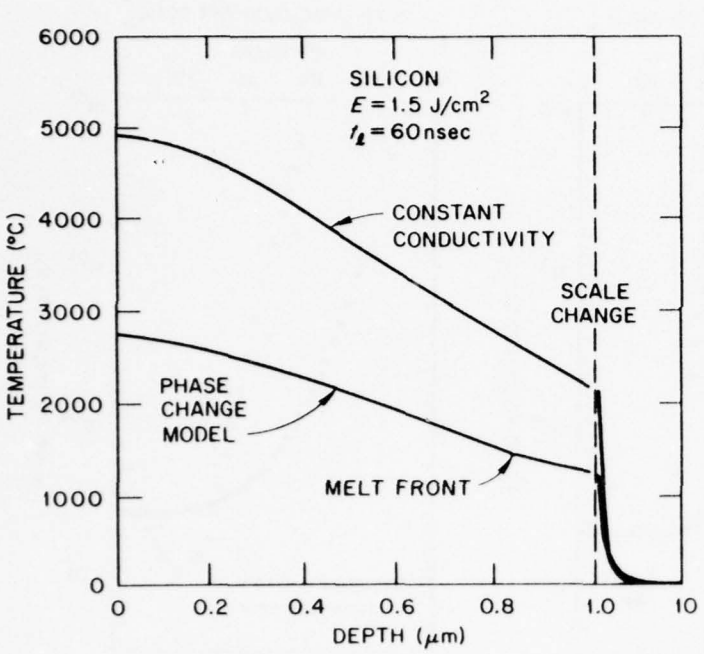

Fig. 2a. Calculated temperature distribution at the termination of the laser pulse.

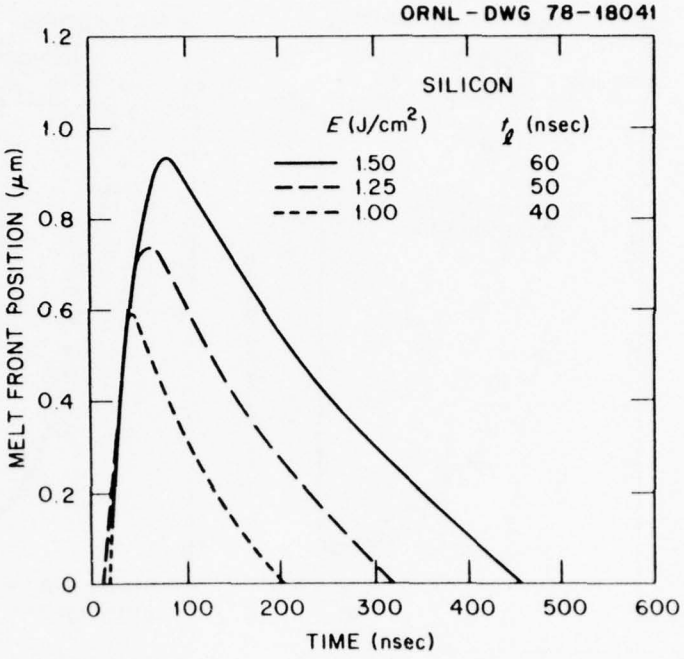

Fig. 2b. Calculated melt front penetration during and after the laser pulse.

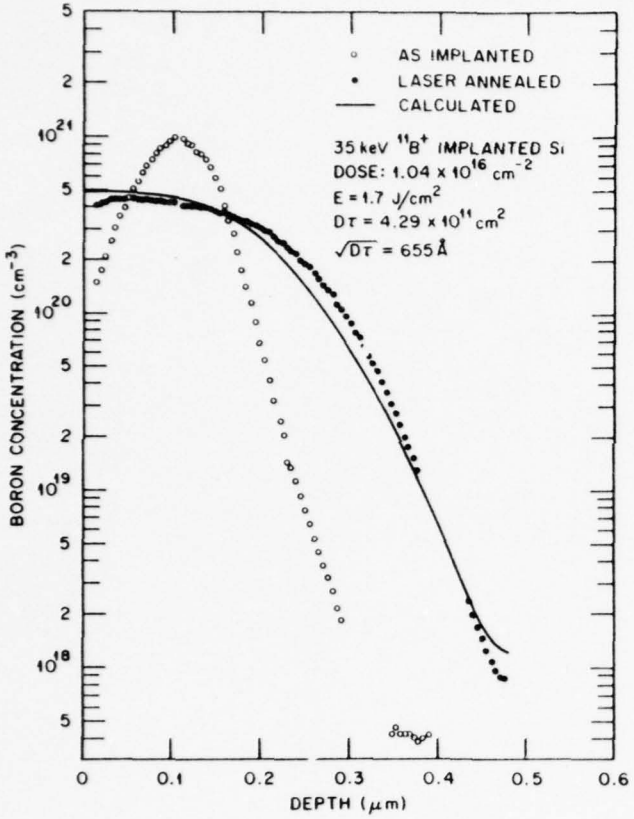

Fig. 3a. Comparison of experimental and calculated ^{11}B profiles after laser annealing.

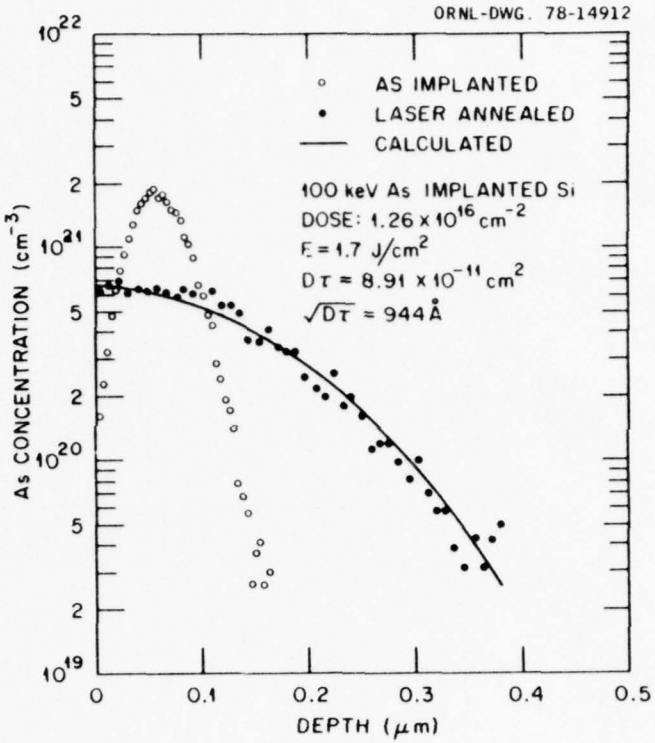

Fig. 3b. Comparison of experimental and calculated ^{75}As profiles after laser annealing.

PATTERNING APPLICATIONS OF INORGANIC FILMS

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INORGANIC RESISTS

Alexander M. Voshchenkov

I. Status of Current Work in Patterning Applications Inorganic Films

Patterning applications in lithography of inorganic films have been studied on the following materials: a broad class of As and Ge chalcogenides, metallic halides, Fe_2O_3, TiO_2, SiO_2, Al_2O_3, and Ta_2O_5. The work has not been systematic and no clear program has evolved. Fundamental mechanisms for the radiation sensitivity of these materials have not been well characterized. At the current level of understanding, some of the mechanisms involved include: (1) photostructural changes due to bandgap irradiation, (2) thermal processes which initiate crystalline phase transformation, (3) thermal processes which anneal defect structure, (4) metallurgical transformation by Ag doping, (5) light enhanced vaporization, (6) radiation induced defect structure.

Inorganic materials have been demonstrated to behave as negative and positive resists. In addition, certain patterning techniques have been demonstrated that are not possible with organic resists. For example, the irradiation of SiO_2, Al_2O_3, and Ta_2O_5 creates a defect structure which allows selective etching without the use of a resist film. In combination with direct pattern generation, the resulting patterned inorganic film could be used as part of the device or circuit structure. Since no mask layer is required, undercutting is avoided and the number of processing steps is significantly reduced. The potential of inorganic films to "synthesize" a device structure and avoid replication transfer of patterns may have significant impact on submicron fabrication technology.

To date, application of inorganic materials to patterning techniques have been studies in at least the following countries: Britain, Bulgaria, Germany, Hungary, Israel, Japan, Russia and the United States.

Details of the materials investigated follow.

A. As and Ge Chalcogenides

Most of the chalcogenide materials appear to experience photostructural changes upon exposure to bandgap irradiation. As a result, the refractive index changes upon exposure to argon-ion laser irradiation. Thermal processes may be dominant in films which undergo crystalline phase transformation or change in density.

As_2S_3

In response to irradiation of 1.5-3.0 eV, structural changes such as crystallization, polymerization, and changes in local

structural order take place.[1] As a result, the refractive index increases while the etch rate decreases.

The change in refractive index has been used to form volume phase holographic gratings 20-60 μm wide with no development or etching required.[2] This is analogous to a negative image formation process. Similar results have been obtained in $As_{1-x}S_x$[3] and As_2Se_3[4].

As grown films (vacuum evaporated) have an etch rate in alkaline solutions 1.6-1.8 times that of an area exposed to a mercury-pressure lamp (acts as a negative resist). Surface relief-type holograms with 1 μm pitch have been achieved by etching the exposed films in NaOH.[5] These films dissolve in aqueous solutions of NaOH, KCN, NH_4OH, and KOH. The rather low etch selectivity of 1.8 is an order of magnitude less than routinely achieved in current silicon integrated circuit (IC) processes. Also, the films have a low exposure sensitivity so that exposure times as long as 2-4 hours have been used. The exposure time could probably be reduced significantly.

Recently, it has been shown that a CF_4 plasma can be used to etch a grating pattern with 12.5 μm pitch.[6] Improved etch selectively in a CF_4 plasma can be achieved by Ag-photodoping the film.

Light enhanced vaporization of As_2S_3 takes place if the exposure is conducted in an oxygen enriched atmosphere at a temperature about 200°C (acts as positive resist).[7] Patterns have been replicated on substrates of organic polymers, quartz, and aluminum.

As-Se-Ge

Argon-ion laser irradiated films dissolve more rapidly in alkaline solutions (acts as positive resist).[8]

As-Se-S-Ge

Argon-ion laser irradiated films dissolve more slowly (acts as negative resist). Relief diffraction gratings have been made with a pitch of 0.86 μm and a diffraction efficiency of 15.8 percent by etching in a 0.33N solution of NaOH at 25°C.[8]

Se-S-Ge, Se-Te-Ge, Se-Sn-Ge

Upon irradiation, these glasses have been shown to exhibit selective etching in alkaline solutions.[9]

Se_xGe_{1-x}

Electron beam irradiation or photo exposure of a thin Ag layer can be used to dope the underlying Se_xGe_{1-x} film.[10] This gives rise to an almost insoluable film to alkaline solutions (acts as negative resist). The sensitivity is comparable to PMMA while the contrast, $\gamma \sim 8$, is appreciably higher than organic

resists ($\gamma \sim 1$). Linewidths of 0.3 μm have been made with 1.5 μm spaces in 1500Å thick films using an electron beam current of 1×10^{-10} A at 20 KV.[10] It is estimated that the resolution limit will be determined by the diffusion length of the excited carriers which is ~100Å. These films resist etching in aqueous solutions of H_2SO_4, HF, H_3PO_4, and HCl.

Undoped films exhibit an 18 percent increase in etch rate upon irradiation (acts as positive resist).[9] Contrast is lower $\gamma \sim 4.5$.[11] Linewidths of 1 μm and 1.5 μm have been fabricated in SiO_2[11] and Si_3N_4[9], respectively, using $Se_{75}Ge_{25}$ as the resist. The sensitivity can be increased by increasing the Se content.

B. Metallic Halides, Sulphides, Selenides

Photographic effects have been observed in PbI_2, CuI, CuCl, SbI_3, As_2Se_3, Sb_2S_3, PbS, and CdS.[12-14] The small dimensions of the grains (several hundred angstrom) make it possible to increase the resolution of photographic materials.

C. TiO_2

Low temperature CVD TiO_2 films have been produced in an amorphous form on substrates such as glass, Si, fused quartz. Annealing at temperatures higher than 300°C leads to crystallization and variation in grain size. This can also be achieved by electron bombardment at 2-35 KV. The rutile phase is highly etch resistant even to 49 percent HF and hot H_2SO_4 (acts as negative resist). Electron fluxes of ~1coul/cm^2 and a power density of 2.8×10^3 watts/cm^2 were used to pattern 3 μm lines with edge definition of less than 0.5 μm.[15] The sensitivity is low because this is a predominantly thermal process requiring crystallization.

These films do not seem to have great potential because it is difficult to achieve stoichiometric material due to the trivalency of Ti. Typically a reoxidizing heat treatment is necessary to produce a stoichiometric film. This is not feasible for TiO_2 because of the mixing of crystallographic phases and changes in grain size.

D. Fe_2O_3

The etch rate of films prepared at 160°C can be reduced by 25 times upon Ar-ion laser irradiation (acts as negative resist). Linewidths of 1 μm were obtained with writing speeds of 2000 cm/sec and power densities of 10^7 W/cm^2.[16] Electron beam irradiation can produce similar effects and 0.8 μm linewidths

were fabricated in 2500Å thick films with a beam current of $3\text{-}4 \times 10^{-7}$ A at 10 KV.[17] The reduction in etch rate has been attributed to differences in grain size caused by local heating.

At high irradiation power densities, the film is completely vaporized. Such a patterning technique is analogous to a positive resist.

E. SiO_2

Electron bombardment of SiO_2 results in an increase in etch rate of 3-4 times. Etch rate enhancement saturates at a dose of 1 coul/cm^2. Using this technique, windows 0.6 μm × 5 μm have been made in a 6,000Å thick SiO_2 film. Device structures have been fabricated without use of conventional lithography, i.e., no resist films. An array of 8 resistor-transistor-logic elements were fabricated with 25 μm wide contact windows and resistor diffusion windows. The resulting bipolar transistors had low leakage but also low gain, $\beta \sim 5$.

Bombardment of SiO_2 with Ar, N, Cl, P, B or Ne ions will enhance the etch rate in buffered HF.[19,20] Argon implants have been used to taper windows in silicon ICs.[21]

An organic film polymethylcyclosiloxane (PMCS) can be exposed in an e-beam at 15 KV with a dose of 85-300μ coul/cm^2. It behaves as a negative resist and can be developed in acetone. When annealed in wet oxygen at 650°C and densified in nitrogen at 1000°C, the resulting film exhibits the same refractive index and etch rate in HF as amorphous silica.[22] Such siliceous films have been used as barriers against diffusion of As, B, P. Bipolar transistors have been fabricated with diffusion barriers and passivating layers defined by e-beam exposure of PMCS.[22] The emitter stripes were 5 μm wide and the gain $\beta \sim 100$.

F. Al_2O_3 (evaporated), Ta_2,O_5(anodic)

Exposure of these films to an e-beam at 15 KV with a dose of 2 coul/cm^2 reduces the etch rate by a factor of 2.[23]

II. Areas of Scientific and Technological Needs for Microfabrication

1. The relatively constant sensitivity - resolution - contrast product associated with organic resists must be increased. Specifically, an overall improvement in contrast is needed to achieve better edge definition.
2. The chemical, plasma, and thermal resistance of resists during patterning must be improved.
3. After patterning, dry processes must be developed for easy removal of the resist.
4. Improvement of resist wettability and/or adhesion to various surfaces is needed.

5. Resist undercutting phenomena as a result of etching must be reduced.
6. To achieve thinner resist films new resist application techniques are needed to improve control of thickness deposition rate and uniformity.
7. In order to utilize thinner resists, the increase in pinhole density as resist films get thinner must be overcome.
8. Resist conformability to topographical fluctuations needs to be improved.
9. The distortion of resist patterns during replication processes must be reduced.
10. Resists are preferable whose effective contrast and sensitivity are developer independent.
11. Resolution degradation due to interference fringe back reflectance of radiation or substrate backscattering of primary electrons needs to be reduced.
12. An increased aspect ratio (thickness to width ratio) of resist and underlying thin film is desirable.
13. A high contrast-resolution negative resist which does not distort during development would be useful.
14. For direct e-beam exposure, an electrically conducting resist would alleviate pattern distortion due to charging effects.
15. The adverse effect on the integrity of a resist film caused by dust particles on a substrate surface must be minimized.

III. Possible Impact on Related or Unrelated Fields if Successful

1. Replication of ~1000Å minimum feature size would impact integrated circuit technology by increasing the device density, increasing switching speed, decreasing noise-equivalent power, possibly allowing use of lower logic levels, and decreasing power consumption. It would also improve high frequency performance of discrete devices (Si, GaAs, etc). Submicron lithography would have applications in the fabrication of piezoelectric, pyroelectric, ferroelectric, Josephson junction, and magnetic domain devices, as well as in SAWs, integrated optics, integrated heterojunction lasers, and display technology.
2. A high contrast-resolution negative resist with no replication distortion could increase the efficiency of direct e-beam pattern generation. This applies to integrated circuit lithography levels requiring small feature sizes with relatively large separations between them.

3. An inorganic resist would reduce the number of processing steps thereby increasing cosmetic yield and decreasing cost.

4. Inorganic resists would be amenable to an all dry processing technology.

5. Improved resolution would have application for technical photography (medical, military, etc.).

6. Evaporation deposition of inorganic resists could be useful in engraving of contoured surfaces. This could have both commercial and artistic applications.

7. Improved replication of submicron structures could lead to microminiature transducers. Such devices could be implanted in various organs to provide sensory outputs. There are obvious applications to space medical experiments. Conceivably a submicron sensor could be implanted in a cancer cell or a large bacterium (~1 μm minimum dimension). Or, perhaps more realistically, cells could be induced to grow on a suitable sensor structure. Such applications could lead to new understanding of pathogenic functions on a microscopic level.

IV. Opportunities for Research that Current Needs Present to Universities and Industry

Although it is difficult on an item-by-item basis to separate research topics for universities and industry, the emphasis for universities should be on long-term objectives, fundamental understanding of mechanisms, new device concepts, and process and device modeling.

A sample listing of specific topics for universities and industry is shown below. It is to be expected that some overlap will occur naturally between the two categories.

A. University Opportunities

1. A systematic investigation of structureless, amorphous-like inorganic materials which are radiation sensitive to exposure with lasers, electron or ion beams. This should be compatible with a pattern generation exposure scheme, i.e., a maskless noncontact exposure process.

2. Materials should be investigated that exhibit abrupt phase transition phenomena either thermally, optically, or electrostatically activated.

3. Phase transition phenomena should be investigated from the perspective of influencing the following "macroscopic" material properties: etch rate and solubility (useful for pattern replication), index of refraction (useful for integrated optics), piezoelectricity (surface acoustic transducer applications, medical sensors, etc.), ferroelectricity, and ferromagnetism.

4. Understanding of radiation sensitive mechanisms should address the sensitivity-resolution-contrast product of a resist material. Therefore, the work should try to define the following: resolution limit (backscattering phenomena or reflectance of primary radiation beam), edge definition (contrast, grain structure, diffusion length of excited carriers), sensitivity (radiation absorption mechanisms, crystallographic phase transformations).
5. Investigate doping in inorganics as a technique for improving radiation sensitivity and/or dissolution selectivity.
6. Studies are needed of stress cracking in inorganic films.
7. Synthesis of glasses with large atomic number which could be used as ion implant or ion beam milling masks.

B. Industrial Opportunities

1. Development and evaluation of alternate resist deposition techniques: plasma assisted deposition, surface catalysis of resist films on a substrate, vacuum evaporation, low pressure chemical vapor deposition, enhanced surface molecular migration for improved step coverage, other nonspin-on approaches. Particular emphasis should be on thinner films, better uniformity and conformability, fewer pinholes, voids, and occlusions.
2. Development of an all dry lithographic process including resist deposition and stripping, thin film etching, and direct pattern generation exposure.
3. Develop a high contrast-sensitive negative resist with low distortion during patterning.
4. Determine limitations to shelf life of inorganic resists.
5. The potential for resistless lithographic processes should be investigated. Such processes could be based on radiation enhanced dissolution of such films as SiO_2 and Si_3N_4.
6. Investigate the ability of a continuously variable composition profile in a multicomponent alloy resist to control edge profiles. Variable composition with thickness could be achieved with techniques similar to molecular beam epitaxy perhaps with in situ ion implantation.
7. Study the usefulness of laminate resist films consisting of two or more layers in controlling edge profiles.
8. Investigate the possibilities of synthesizing organic films containing Si-O, Si-OH, Si-N bonds or metallic complexes which upon appropriate radiation could be converted into inorganic films compatible with device structural needs (SiO_2, Si_3N_4, Si, Al_2O_3, Al, etc.)

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METAL INTERCONNECTIONS AND VERY LARGE SCALE INTEGRATION

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METAL INTERCONNECTIONS AND VERY LARGE SCALE INTEGRATION

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1. Introduction and Current Status

The continuing trend toward higher density and the resultant very large scale integration levels is placing severe demands upon metallization techniques. The problem is particularly acute in semiconductor integrated circuit technology in which metal to semiconductor contacts impose additional constraints. The current status of metallization in silicon microelectronics at medium and large scale integration levels has been recently reviewed.[1,2] The requirements for a useful metallization system are multiple; good adhesion to dielectrics, selective etchability, low electrical resistivity, good coverage of surface topography, high electromigration resistance, resistance to oxidation and corrosion, and (for semiconductor applications) low metal to semiconductor contact resistance and good contact stability. The requirements for large scale integration are being met currently by the use of proper aluminum alloys (e.g., Al/Cu/Si) and contact metallurgies such as PtSi. Practical metal linewidths and spacings between adjacent lines are about 2.5 micrometers at present.[2] It should be noted that large scale integrated metal oxide semiconductor structures with polycrystalline silicon gates employ either diffused regions in crystalline silicon or the heavily doped polycrystalline silicon as one level of interconnection. The relatively high resistance of such layers will not allow their use as interconnections if device geometries decrease much below present dimensions (e.g., heavily doped polycrystalline silicon has a resistivity of 1000 micro-ohm-cm as compared to 3 micro-ohm-cm for aluminum alloys at 300°K). Replacing these materials by using multilevel

metallization requires the formation of tens of thousands of very small metal to semiconductor contacts, which is a challenging problem aggravated by a decrease in junction depth imposed by decreasing device dimensions.

The insulator is an important part of the overall metallization system and must provide reliable crossovers (where one metal passes over another separated by the insulator) and vias in which metal to metal contacts between levels are fabricated. Surface topography is quite important and sharp steps must be avoided - the ideal would be to maintain a planar top surface on the insulator for deposition of the next metal level. Selective etchability of the insulator relative to the underlying layers (e.g. metal) is a must for obtaining a viable process. Silicon dioxide, silicon nitride, aluminum oxide, and polyimide have been employed as the insulator in multilevel metallization applications.[1,2] The defect density in silicon dioxide (the most commonly employed insulator) as deposited by present techniques is likely to limit yield at very large scale integration levels because of interlevel metal to metal shorts at crossovers.

The use of electron beam (or X-ray) patterning, which is required to achieve micrometer and sub-micrometer dimensions, will require a careful re-evaluation of present metallization practices. This is particularly true for device structures which are sensitive to ionizing radiation. Multilevel metallization systems which would allow for moderately high post metal anneal temperatures (e.g. 600 to 700°C would be a very desirable goal). Refractory metals such as molybdenum and tungsten allow for high temperature anneals and represent potential alternatives to the more reactive aluminum alloys.[3,4] The poor resistance of these materials to oxidation and corrosion pose reliability problems. Japanese laboratories are continuing to investigate molybdenum for multilevel applications in high density integrated circuits.[5] An alternative to multilevel metallization may be provided by refractory metal silicides such as tungsten disilicide and molybdenum disilicide. Recent investigations have demonstrated that

the conductivity limitations imposed by polycrystalline silicon can be substantially reduced by replacing or supplementing the polycrystalline silicon by metal silicide[6,7] A particularly attractive property of such silicides is that oxidizing ambients produce an insulating and passivating layer of silicon dioxide so that these new materials can be incorporated into polycrystalline silicon gate technology with minor process changes. It should be noted that the advent of dry processing techniques (e.g. reactive plasma etching) made the use of these materials practicable - selective wet chemical etches compatible with silicon dioxide and silicon are not known.[7]

2. Scientific and Technological Needs

"New" materials may be required to realize the requirements imposed by ultraminiaturization and consequent very large scale integration. There are many "metallic" compounds which are known to have oxidation resistance and corrosion resistance in bulk form. Material science studies of such materials in thin film form (50 to 500 nm) could provide candidates suitable for more detailed evaluation. Materials with a low dielectric constant, good insulating behavior, high temperature stability, and capable of "planarizing" surface topographical features are very desirable as insulators in multilevel metallization. Materials science research directed toward finding such materials is necessary.

Technological needs include (1) development of techniques for contacting shallow junctions which allow for annealing at temperatures sufficient to remove radiation damage induced by energetic patterning techniques (electron beam, X-ray), (2) developing procedures for fabricating large numbers of very small vias with low resistance contacts, and (3) refinement of existing insulators or combinations thereof in order to achieve low defect densities. Implementation of refractory metal silicides requires a better understanding of the relationship

between processing parameters and the quality of the silicon dioxide grown over these materials. An understanding of the parameters which control grain size and grain growth during high temperature processing in these materials is also necessary for the applications requiring very fine lines.

3. Possible Impact on Non-Related Fields

Benefits derived from advances in interconnection technology for ultraminiaturization in silicon technology would be applicable to other silicon device areas. In addition, benefits may be derived from other areas requiring multilevel metallization. However, the constraints imposed by the metal-semiconductor contact may be overly restrictive for other applications. It should be noted that contact procedures are material related - e.g. contacts to GaAs are made quite differently than contacts to silicon. The development of better insulators could have wider application (e.g. integrated optics, amorphous bubble materials fabrication technology).

4. Academic and Industrial Research Opportunities

Future research in industry will focus mainly on extensions of aluminum alloy multilevel metallization with refinements of existing insulator systems. Few industrial laboratories have the resources or the inclination to explore radical alternatives. However, university laboratories can engage in materials science studies of thin films of materials which possess high conductivity and oxidation resistance in order to identify promising candidates for more exhaustive study. The latter studies must be conducted at industrial laboratories or in conjunction with industrial laboratories because they would entail actual device fabrication at small dimensions - a task that most universities are not able to adequately handle.

Thin film studies in this area would provide a wide range of research problems for universities because of the variety of materials which might be suitable - e. g. metal silicides or intermetallic compounds such as AlNi. Since many different deposition techniques are available (co-evaporation, sputtering, reaction from the elements, chemical vapor deposition), the number of permutations is quite large. Further opportunities for university research are provided by the multiple constraints imposed on a good metallurgy for VLSI applications. For example, the requirement of oxidation and corrosion resistance could form the basis for quite fundamental studies of oxidation and corrosion kinetics of thin films of high conductivity materials. The necessity for controlling surface morphology could generate research into the mechanisms of grain growth during thermal processing of such materials. The materials science understanding necessary for developing high temperature, high conductivity interconnections provides university research with a fertile area for exploration which is both challenging and potentially very important.

An examination of organic and inorganic thin films which are both insulators and have a low dielectric constant could also provide candidates for better insulators. Again, it is unlikely that industrial laboratories will conduct a broad based search for such materials.

Emphasis in industrial laboratories will focus on the problems of contacting very shallow junctions and on the patterning of fine metal lines and very small vias. Combinations of insulators will most likely be employed to achieve low defect densities. Research in refractory metal silicides will focus on obtaining good silicon dioxide over such silicides and upon achieving fine line structures, which implies control over grain size.

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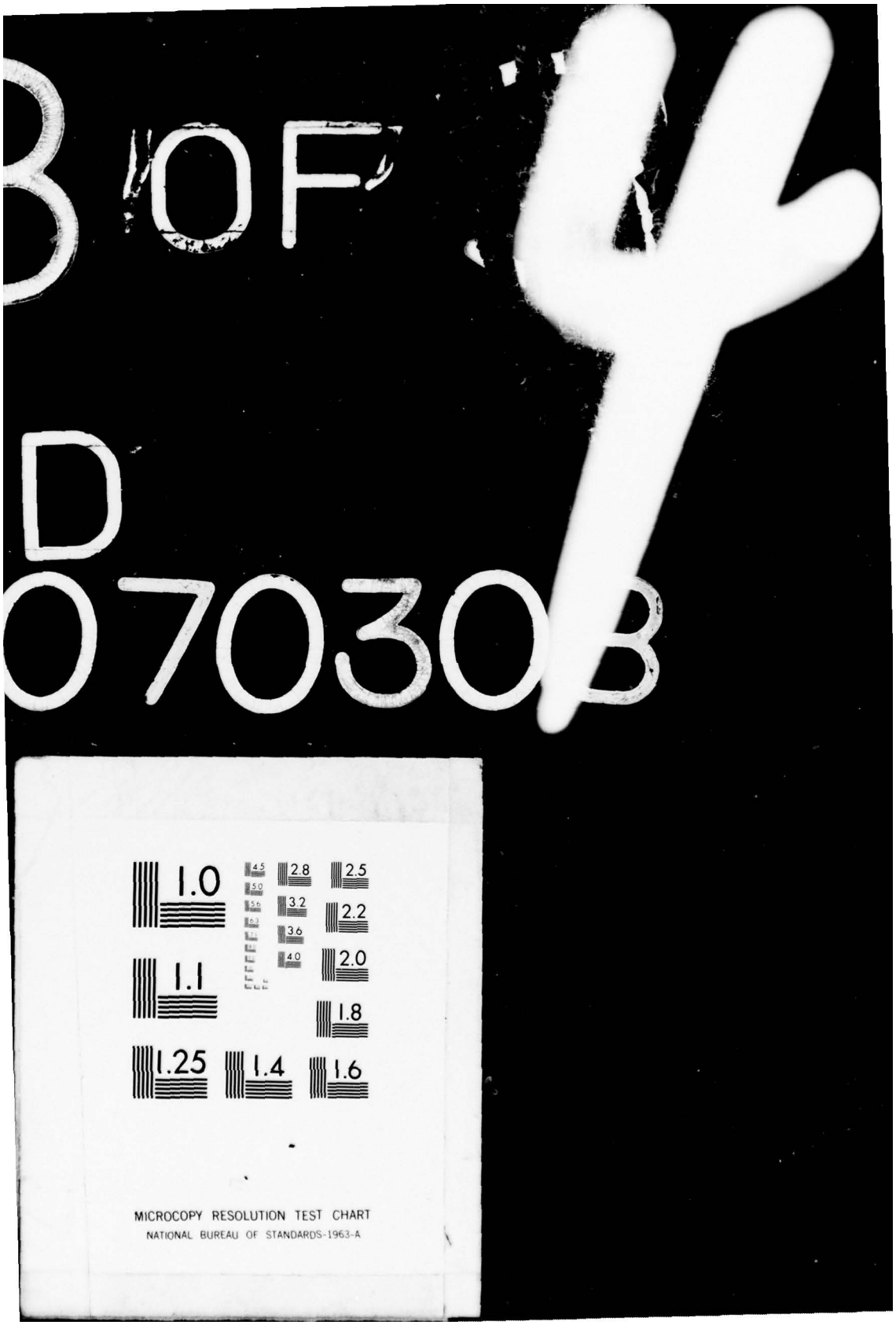
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METALLIC AND SEMICONDUCTING MATERIALS DERIVED FROM NON-METALLIC ELEMENTS

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I. Introduction

This report is directed towards the very new area of materials science which is concerned with the preparation and characterization of synthetic metals, many of which contain no atoms of any metallic element in their chemical constitution. The three main presently known classes and their potential technological significance will be described. One of the classes also encompasses a series of p- and n- semiconductors.

Although there is no immediate obvious application of these systems to ultraminiaturization of electronic devices, it would appear they warrant considerable further investigation and evaluation by specialists in the field of electronic devices.

The motivation for producing new conductors is in part a desire to achieve unusual, or even unprecedented, materials properties of technological importance. Metallic conductors are based on open-shell atoms, while non-metallic compounds typically exhibit covalent or polar bonding based on closed shells. Since open-shell electronic bands are a prerequisite for any conductor, molecular or polymeric conductors will almost certainly be unusual chemically. The stabilization of interacting open-shell non-metals in a solid, so as to prevent the exclusive formation of polar-covalent bonds, is an enormously challenging task. On the other hand, recent developments with doped polythiazyl, $(SN)_x$, and polyacetylene, $(CH)_x$ suggest that the judicious incorporation of electron donating and withdrawing groups may yet provide a fairly general scheme for achieving incompletely filled bands, as required for conductors.

The stabilization of partly-filled bands in nonmetallic conductors is primarily a chemical and structural problem. The synthesis, characterization, optimization and exploitation of conducting systems provides many opportunities for both experimental and theoretical studies. When nonmetallic open-shell systems are available, traditional chemical ideas about crystal packing, about isoelectronic substitutions, or about analogous reactions have generated essentially all of the currently known "families" of molecular metals. These have been derived from a few conductors that were originally prepared for other reasons. Finding new conductors among nonmetallic elements or compounds will consequently demand great ingenuity, with only very modest theoretical suggestions. On the other hand, the theoretical appreciation of the role of dimensionality in phase transitions and in magnetic phenomena has greatly increased interest in model compounds, whose experimental study has further enriched theory.

The bulk properties of most known conducting polymers are quite different from their intrinsic crystal properties. These bulk properties typically reflect the state of crystallite aggregation as much as the crystallite properties. For example, a variety of indirect measurements indicate metallic conductivity for $(SN)_x$ and for doped $(CH)_x$ in directions in which d.c. conductivity measurements indicate a non-metallic temperature dependence. This difference between bulk and intrinsic properties, which includes everything from mechanical strength and environmental stability to superconductivity, is a consequence of gross structural inhomogeneity in these materials. As a result, basic uncertainties exist in our knowledge of their fundamental

materials properties, which limit our ability to understand their polymer physics and to optimize their properties for possible applications.

This report concentrates on three presently known classes of metallic compounds derived from non-metals, namely those based on $(SN)_x$, $(CH)_x$ and graphite.

II. Critical Assessment of Existing Knowledge in the Field

A. $(SN)_x$ and Derivatives[1]

Polythiazyl, "polymeric sulfur nitride," is the first example of a covalent polymer containing no metal atoms which has been shown to be a conducting ($\sigma_{RT} \approx 5 \times 10^3$ ohm^{-1} cm^{-1})* and a superconducting polymer ($T_c \approx 0.3$K). Electrical contacts can be made with metal clips or by silver paint. These unique electronic properties have opened up new vistas for the scientific investigation of potentially conducting polymers. Currently available $(SN)_x$ consists of golden crystals made up of crystalline microfibrils which are fully oriented in a common chain direction, but poorly coupled together electronically. Gross twinning occurs and about 20% of the chains in each microfibril are in defect positions. However, band structure calculations based on the ideal $(SN)_x$ structure have led to a semi-quantitative understanding of its properties; in particular $(SN)_x$ has been shown to be an anisotropic semi-metal, stabilized against the Peierls distortion by interchain interactions. $(SN)_x$ crystals may be conveniently sublimed at *ca* 150°C and cohesive golden films may be condensed on room-temperature substrates of plastics, metals, glass, etc. These films are also highly conducting. Completely aligned epitaxial films can be deposited on appropriately "scratched" plastic or glass surfaces. These show highly anisotropic electrical and optical properties. The films on flexible substrates are also completely flexible and may be bent without cracking. $(SN)_x$ crystals and films are stable in air for extended periods.

Presently, the only known conducting derivatives of $(SN)_x$ are obtained by partial oxidation with halogens and interhalogens. Of these compounds $(SNBr_{0.4})_x$ has been the most thoroughly investigated. This material exhibits an order of magnitude higher conductivity than $(SN)_x$ and other interesting electronic properties. However, details of the crystal structure and the role of bromine are not yet entirely clear. Halogen derivatives of $(SN)_x$ have been obtained also by halogenation of S_4N_4 which eliminates the intermediate synthesis of $(SN)_x$.

B. $(CH)_x$ and Derivatives[2]

Polyacetylene, $(CH)_x$, is the simplest possible conjugated organic polymer and is therefore of special fundamental interest. It may be prepared in *cis*- or *trans*-isomeric forms as silvery, polycrystalline, flexible films by the polymerization of acetylene gas, C_2H_2, at *ca* 1 atm. pressure using a Ziegler catalyst at temperatures ranging from -78°C to *ca* 150°C. Low temp-

*For comparison, the conductivity, σ, of mercury at room temperature is *ca* 1×10^4 ohm^{-1} cm^{-1} and that of copper is *ca* 6×10^5 ohm^{-1} cm^{-1}.

erature polymerization conditions favor the formation of films of the cis-isomer which can be subsequently isomerized to films of the trans-isomer by heating at ca 200°C for 2 hours in an inert atmosphere or in vacuo. Cis-rich films have a tensile strength of ca 3 kg/mm^2 and can be stretched to 3-4 times their original length at room temperature. Electron microscopy studies show that the as-formed $(CH)_x$ films consist of randomly oriented fibrils (typical fibril diameter of a few hundred angstroms). The bulk density is ca 0.4 gm/cm^3 compared with 1.2 gm/cm^3 as obtained by flotation techniques. This shows that the polymer fibrils fill only about one-third of the total volume. In the absence of added deoxidant the films slowly undergo oxidation in air during several days. Oxidation may be prevented by covering with appropriate polymer lacquers, etc. Both isomeric forms are semiconductors; however, through chemical doping, their electrical conductivity may be controllably varied over an extraordinary 13 orders of magnitude with properties ranging from semiconducting ($\sigma<10^{-10}$ ohm^{-1} cm^{-1}) to metallic ($\sigma>1 \times 10^3$ ohm^{-1} cm^{-1})*. Electrical contacts to the films may be made by metal clips or by "Electrodag" (graphite dispersed in a polymer "cement"). The metallic state is preserved down to at least 40 mK. Studies of the chemical stability and electrical conductivity of the doped films at room temperature are presently being undertaken. The semiconductor to metal transition occurs at a few mole percent dopant concentration. Both electron acceptors (e.g. I_2, Br_2, AsF_5, $AgClO_4$, etc.) and electron donors (e.g. Li, Na, K, etc.) can be used to yield p-type or n-type material respectively. The $(CH)_x$ films can be partially chain-aligned by mechanical stretching and may also be doped. Such films exhibit anisotropic electrical and optical properties with an increase in conductivity in the direction of alignment of up to one order of magnitude. Preliminary band structure calculations suggest that $(CH)_x$ is an anisotropic semiconductor with a small band gap (~1eV) but with wide conduction and valence bands (5-10eV in the chain direction). Presently available $(CH)_x$ is morphologically complex and is not well understood.

C. Graphite Intercalation Compounds[3]

Graphite can be readily intercalated with a variety of electron acceptor or donor species to give solid materials which are generally unstable in air unless surrounded by a protective material. Graphite and its intercalates exhibit interesting anisotropic two dimensional properties in contrast to the more one-dimensional properties of $(SN)_x$ and $(CH)_x$. The electronic properties of intrinsic graphite crystals are reasonably well established with one main exception: the specific effects of crystal defects on the scattering mechanism. Both donor and acceptor intercalation compounds of graphite with a wide variety of interesting electronic properties have been made. Three general properties of these compounds which are of particular interest are mentioned below.

(1) Acceptor (e.g. HNO_3, SbF_5, AsF_5, Br_2) compounds have higher in-plane electrical conductivity ($\sigma_{RT} \simeq 10^6$ ohm^{-1} cm^{-1}) than the donor (e.g. K, Cs, Rb) compounds ($\sigma_{RT} \simeq 10^5$ ohm^{-1} cm^{-1}).

(2) The maximum in-plane conductivity occurs at a stage higher than one in acceptor compounds.

*For comparison, the conductivity, σ, of mercury at room temperature is ca 1×10^4 ohm^{-1} cm^{-1} and that of copper is ca 6×10^5 ohm^{-1} cm^{-1}.

(3) There is an increase in anisotropy (ratio of in-plane conductivity to conductivity normal to the planes) which accompanies increased in-plane conductivity. For example, with AsF_5 doping, an exceedingly large anisotropy of $\sim 10^6$ is observed.

In general, the donor (group I) compounds are better understood than the acceptor compounds but the acceptor compounds appear to have the potentially more interesting properties, e.g. high electrical conductivity and anisotropy.

III. Scientific and Technological Potential

A. $(SN)_x$ and Derivatives[1]

$(SN)_x$ is a unique material and has served as a model compound for understanding the metallic and superconducting properties of polymers. $(SN)_x$ and its derivatives have scientific and possible technological potential. It does not appear likely that high superconducting transition temperatures will be achieved with polymers unless novel methods for increasing the electronic density of states are discovered. $(SN)_x$ films have been used in the formation of Schottky barrier photovoltaic devices. Other potential technological applications are under investigation.

B. $(CH)_x$ and Derivatives[2]

The scientific potential of doped $(CH)_x$ derives from the fact that this new class of materials has by far the highest conductivity of any known organic polymer. It may also be doped (either p- or n-) to give semiconducting films. An understanding of the conduction and doping mechanism and the effect of alignment on the electrical and optical properties presents fundamental scientific challenges. p-n junctions having typical rectifier diode characteristics have been prepared by pressing together films of p-$(CH)_x$ and n-$(CH)_x$. A photovoltaic effect has been observed with an n-Si/p-$(CH)_x$ heterojunction. Furthermore, the ease of fabricating large sheets of p-n junction $(CH)_x$ films suggests possible use for terrestrial solar cells, etc.

C. Graphite Intercalation Compounds[3]

On the scientific level these compounds have significant potential for improving our understanding of anisotropic two dimensional systems in which electrical conductivity and anisotropy can be controlled over wide ranges. Stage 3 graphite-SbF_5 has a conductivity comparable to the best elemental metal at room temperature. As far as technological potential is concerned, three areas can be mentioned:

(1) Stage 3 graphite-SbF_5 can be swaged into a practical wire form, when protected with a thin sheath of copper, having a room temperature conductivity of 6.5×10^5 ohm^{-1} cm^{-1}. For comparison, the room temperature conductivity of copper is ca 6×10^5 ohm^{-1} cm^{-1}. In addition, the conductivity decreases less rapidly with increasing temperatures than for the best elemental metals. The stage 3 compound has density less than 3 grams/cm^3 so that considerable weight saving is possible compared to copper.

(2) The electrical conductivity of graphite fibers of the kind used to reinforce epoxy composites can also be increased by intercalation, while maintaining their high strength and elastic modulus. Conductivities of 1×10^5 ohm^{-1} cm^{-1} have been obtained and values as high as that of copper are forecast. These high conductivity fibers have been incorporated into epoxy composites which then demonstrate an increase of conductivity of about a factor of ten. The electrical conduction of the composite suggest increases applications that require high strength, light weight and conductivity such as aircraft structural members, large antennae and others.

(3) On intercalation with acceptors, the reflectivity of graphite on the c face - the outside surface of graphite fibers - is increased to substantially 100% in the infrared (specifically at the 10.6 μ laser wavelength).

IV. Useful Research Directions for Universities and Industry

From past experience it has been observed that technology advances by quantum jumps when either new materials or new techniques have become available. In the previous sections, it has been shown that completely new types of metallic conductors and semiconductors are becoming available and several potential applications based on laboratory studies have been presented. What is now required is further basic research on these materials to explore the breadth of the field while at the same time carrying out in-depth research on carefully-chosen aspects which appear to be of particular importance.

Academic institutions should be encouraged to do what they can do best (basic research) and industry should be encouraged to do what it can do best (application of new knowledge to technology). A faculty member at an academic institution can do first class fundamental research in a field which has no apparent relevance to any technological problem or objective or he can do first-class research in a field which may have relevance to some technological problem or objective. The fields mentioned in the previous sections of this report clearly fall into the second category.

It is proposed that the areas of research described be studied at least in part by government research contracts involving collaborative work by an academic institution and industry. For example, a joint contract might be given to an academic institution and to industry to evaluate the possibility of fabricating commercial solar cells for terrestrial use from $(CH)_x$ p-n junctions. The academic institution could be primarily responsible for ascertaining methods for making p-$(CH)_x$ and n-$(CH)_x$ while an industrial collaborator skilled in classical semiconductor technology could attempt the fabrication of photovoltaic devices, etc.

Specific areas for research in the systems mentioned in this report are described below.

A. $(SN)_x$ and Derivatives

There are several directions for significant research on this polymeric system: the chemistry of halogen derivatives and its relationship to the electronic properties needs further study; demonstration of donor intercalation; separation of the $(SN)_x$ chains to change the dimensionality; attempted synthesis of isoelectronic analogues; a better understanding of the "S_4N_4-halogen route" to conducting polymers, which may provide the key to obtaining a much wider class of materials based on the $(SN)_x$ polymer.

B. $(CH)_x$ and Derivatives

There are a number of important directions in which research should proceed. Essentially only one set of polymerization conditions for the synthesis of $(CH)_x$ have been investigated to date. Undoubtedly $(CH)_x$ films with considerably different electronic, optical, mechanical, etc. properties will be prepared using different conditions. Only a very few different types of dopants, which give widely different conductivities, have been investigated so far. The chemical properties of the doped and undoped $(CH)_x$ need to be studied, particularly those related to stability to heat, air and light. It is extremely important to devise methods of synthesizing completely aligned $(CH)_x$ in order to ascertain its intrinsic conductivity parallel to the $(CH)_x$ chains. Much more theoretical work needs to be done in order to gain an understanding of the conduction process.

An almost unlimited number of chemical derivatives of $(CH)_x$ are potentially available in which the hydrogen atoms of $(CH)_x$ have been replaced in whole or in part by organic, inorganic or organometallic groups. It therefore appears that it may be possible to synthesize a very large number of semiconducting and metallic polymers based on $(CH)_x$ whose electronic, optical, mechanical, etc. properties may be controlled and pre-determined by chemical fine tuning of the system.

C. Graphite Intercalation Compounds

Several significant scientific problems for these materials are briefly outlined below.

(1) Identification of the chemical species and the state of ionization in acceptor compounds.

(2) Determination of role of defects and defect-intercalant interactions in transport scattering mechanisms.

(3) Examination of other systems with a) intercalants of high electron affinities, b) donor systems other than Group I, and c) intercalate into boron nitride, $(BN)_x$, an isoelectronic system, to compare with the conductivity properties of graphite intercalates.

D. Structural Characterization

Future research on A., B., C. should fully characterize the relationship between defect structure and electronic properties. No comprehensive studies of this sort exist for $(SN)_x$, $(CH)_x$ and graphite intercalation compounds. This probably reflects the scarcity of research facilities which are equipped to accomplish all of the following: (1) prepare new materials under carefully controlled experimental conditions (2) fully characterize defect structure and (3) evaluate electronic properties. In this light, collaboration between researchers in different facilities and countries should be encouraged. Major effort should be devoted to the development of methods for producing conductive materials as high-perfection single crystals suitable for electronic and structural measurements.

V. Conclusions

It appears that the new field of polymeric conductors and the closely related area of graphite intercalation compounds are both advancing at an

extraordinarily rapid rate. However, the synthesis of new chemical systems is absolutely fundamental for the continued growth of the field. The potential for increasing the scientific knowledge in these fields by the synthesis of new compounds, by better characterization of presently-known materials, and by theoretical analysis of the new phenomena is extremely high. It presents a challenge and opportunity for collaborative interaction between chemists, physicists and materials scientists. These materials have important technological potential in electronic devices. Present knowledge suggests that we are seeing only the tip of the iceberg and that the next few years will bring forth important new materials with unusual properties.

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Report on "Contacts at Very Small Dimensions"

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Report on "Contacts at Very Small Dimensions" (Definitions and Introduction)

by T. E. Seidel and D. B. Fraser

Topics will be discussed in regard to successful fabrication of "contact systems" at very small dimensions.

By "contact system" we mean: (i) A dielectric(s) with a topologically adequate opening, and surfaces suitable for metallization inside and outside the opening. (ii) A contact, formed by deposition and reaction of thin film(s) with the material primarily inside but also outside the opening. For example, in applications to semiconductor contacts for integrated circuits (IC), Al reacts with Si, and Si with Al, Al also reacts and bonds well with SiO_2 which results in good adhesion to the dielectric.

After contact formation, the characterization of the performance must also be made: contact resistance, body resistance, capacitance, stability under aging, (electromigration and corrosion effects), depth of reaction-penetration, contact yield, for example as determined by reverse bias leakage of p-n junctions underneath the contact.

Formation of the window is now a <u>necessary</u> part of a useful study for a contact system. Thus the emerging disciplines of lithography for large scale integration and dry etching are the domain of this topic. We will discuss the relevant aspects of lithography as it pertains to window formation.

Finally, the scale of IC design can be used to organize the various aspects of the report. Design considerations for IC layout show that the scale of integration is $\sim$50% limited by lines and spaces and $\sim$50% by contact window size - which in turn sets up the rules for the layout of the active devices. Roughly speaking: 5-3 μm design rules imply 16-64K bit RAM, this

represents the current status; ∿1 μm rules imply 256K bit, and ∿0.2 μm rules imply 10^6 bits for a 1 cm^2 chip. The latter two scales of integration are where we wish to be in the near and more distant future, respectively.

(1) Current Status of Window Technology

Today, in industry, window sizes of 3 to 5 μm are in manufacture.[1] Projection printing lithographic techniques have replaced contact printing. This reduces (nearly eliminates) mask damage.

X-ray lithography is still in the development stage but 1 μm and 0.25 μm features have been obtained.[2,3] X-ray lithographic techniques can be a high volume process. In addition, the resolution due to Compton scattered electrons is better than that afforded by electron-electron scattering using electron-beam techniques.[3] Utilization of X-rays for 1 μm lithography requires the achievement of "error budgets" of ±0.15 to ±0.2 μm for: pattern generation, alignment, processed edge position, pattern replication, wafer bending and thermal expansion.[2]

Electron-beam techniques have utilized direct writing[4] (direct e-beam exposure of resist on chip) to produce 0.5 μm features. This procedure eliminates the use of masks and mask fabrication. The resolution is primarily limited by the thickness of the resist. If thick layers are used to reduce pin-holes and promote coverage, then lateral electron scattering limits the resolution. If one wishes to use more planar structures, and very highly filtered thin resists, smaller features could be obtained by e-beam writing. The data rate or resist sensitivity must also be increased before direct e-beam writing can be a high volume process.

For 5 μm technologies, windows are etched using wet chemical methods (isotropic), this partly characterizes the

present technology. However, plasma etching and reactive ion etching are also currently being used, and will be adopted for windows of 3 μm and smaller.[5] Dry processes incorporating reactive ion and sputter phenomena are being combined with plasma processes to develop anisotropic etching, and "degrees" of anisotropic etching.[5] In wet etching a major problem has been resist lifting, while in dry processing the resist may etch away at a rate comparable to the substrate. The latter partly controls and limits the topology of the window cut.

There is a conflict between obtaining very small feature size which implies well defined, almost vertical window walls and good step coverage of the metal running between the contact-surface and the rails on the IC chip. This conflict will be discussed below.

2. Specific Areas of Scientific and Technological Need for Window and Substrate Definitions

It is likely that industry (e.g., Perkin Elmer) will provide advances in optical lithography which result in window sizes of $\lesssim$1.5 μm by use of ultraviolet wavelengths.[1] To achieve this, improvements are needed in: (1) ultraviolet sources, (2) the mechanical stability of the projection printer system, (3) optical surfaces, wafer and mask flatness (in combination with more planar technologies), (4) better linewidth control, and (5) improvement in alignment and registration techniques for nonvisible wavelengths.[1]

Advances in X-ray lithography[6] require the above same generic improvements, and in addition need improved resists (i.e., those with higher sensitivity to X-rays, high resolution and good resistance to chemical, ion and/or plasma etching), improved life and compatibility of sources with filter-window and mask, and the development of large area, stable, low defect-density masks, and improvements in mask-to-layer registration capability.

Electron-beam techniques are limited by data rates (an engineering job), electron optics performance (the fundamental limits need study), and by electron scattering effects.

Both X-ray and electron-beam systems exist as laboratory tools today.[7,8] Although they are now not manufacturing tools, one should take advantage of their capabilities for the fabrication of ∿1 μm window sizes for tester structures. It is the position of this report that window-size effects cannot be usefully studied unless contact reactions of interest are studied on scaled down - real size windows.

It will be desirable to control topology of the small window cuts such that steep angles are achieved in a controllable manner. Vertical or reentrant features are undesirable for step coverage, and so are very gradually tapered window cuts as they limit the packing density. Window topology work should be pursued which develops a capability to make controllable steep angles for the window cuts.[9]

It would be interesting to pursue new metal deposition techniques such as CVD or plating which may improve step coverage at steep window cuts.[10] For the purpose of contact performance, doping of the window region should be carried out in a manner which (i) gives low contact resistance or controlled barrier heights and (ii) limits the defect density - by limiting the doping[11] or controlling the ambient during contact doping. It is known that very high impurity concentrations and oxygen ambients[12] promote defect expansion. It would be interesting to see work appear which introduces variations on the defect characteristics in windows and around their edges and answer the question as to what role the defects play in subsequent contact formation.

There is also a need to further characterize and understand redistribution of impurities during silicide formation.[13]

Laser annealing of implanted layers has recently resulted in the formation of very high (nonequilibrium) substitutional concentrations of dopant impurities in semiconductors.[14] It is possible that lower contact resistance may be achieved with such layers. Any such exploratory contact study should include the effects of thermal history following the laser annealing as well as the variation of sintering and/or reaction temperatures upon the nonequilibrium dopant concentrations.

(1) Current Status of Contact Formation

Aluminum metallization has been the mainstay of the industry for contacts to integrated circuit windows.[15] Dissolution of Si in Al and Al in Si has resulted in the use of Al-Si alloys of up to 2% Si in Al.[16] Too little Si in Al results in Al penetration into the underlying Si, too much Si results in precipitation of Si, extending above the plane of the Al-Si alloy/Si interface.

The situation of "too little Si" in Al is aggravated by smaller window sizes because all the Si required to satisfy solubility requirements in the Al is "pumped" from the small window region, making the interpenetration of the Al into the contact very deep. Of course, it is intended that shallower junctions are to go with smaller windows, so a situation develops which is aggravated by smaller windows.

The situation of "too much Si" may also be aggravated by smaller window sizes because the precipitate size may be a substantial fraction of the window[17] size and this could result in high resistance contacts.

In summary, Al metallization and Si-Al alloy metallization is currently being used for some window sizes and junction depths but problems may be anticipated at smaller windows and junction depths.

Silicides (e.g., PtSi, Pd_2Si, NiSi, etc.) form a class of contacts to silicon which have been used for IC and discrete device fabrication. Silicide formation may, in principle, give completed reactions which give very shallow stable metal contacts.[18]

There are a very large number of metal layered systems which could be used on silicides, Ti-Pt-Au is one example of such.[19] With silicides (e.g., PtSi) multilayer metallization schemes are used since Pt does not give good adherence to SiO_2.

It seems that contact formation can be classified into two broad areas: (1) Al (alloy) single metal, and (2) silicide with multilayer: adherence promoter layer and inter-diffusion barrier layer. Barrier diffusion layers (Ti, Cr, V) can be used between reacted silicides and Al.[18]

These two broad areas will be discussed below for future work.

Present technologies use doped polysilicon for gate and rail material in MOS devices. However, for dimensions smaller than 1.5 μm widths, increasing rail resistance limits the performance of high-speed circuits. The use of silicides on polysilicon[20] or refractory metals such as Mo or W becomes needed. There is a need to explore contacts to lower resistance materials, to characterize the interfaces between these "rails" and the primary metallization from the point of view of stability against intermetallic diffusion and interface resistance. Contacts between W, Mo, PtSi, Pd_2Si and Al should be explored in more detail.

Electromigration effects have been studied in considerable detail for Al, Au and assorted pure metals and alloys.[21] Typically, homogeneous test structures are used which have massive contact areas. For use in integrated circuits a metal-alloy, such as

Al-Cu, will terminate at the interface of a contact. The system is not homogeneous at the contact (by definition) and for a 1.0 μm window diameter and a current of 1.0 mA, the current density is $10^5 A/cm^2$, a value for which electromigration effects are observed in thin films. It is possible that stability effects associated with electromigration may be observed in very small windows at moderate currents.

(2) Specific Areas of Scientific and Technological Need for Contact Formation

Al is widely used for metallization of IC, thus an extensive effort should be made to quantify its limitations for use at small window size. The difficulties mentioned above have not been quantified in the literature. It is not clear if a range of alloy compositions exists which gives no Al penetration (Si rich alloy) and simultaneously no yield limiting precipitates (dilute Si alloy). It should be the objective of current research to define and determine the exact limitations of Al-Si in small windows.

The question of window edge stresses and doping induced stresses as they relate to contact formation (Al or silicide) should be examined. What effect do stresses have on the penetration of silicides or Al?

The effect of ambients on the interface between silicon and metal should be systematically studied in the context of contaminated interfaces.

The effect of the presence of extended defects such as stacking faults and dislocations upon Al and silicide contacts should be documented. Stacking faults and dislocations can now be intentionally introduced in a rather controlled manner. Exploratory research could well make use of this fact and form contacts in the presence of the intentionally introduced defects.

(3) Areas of Impact of Contact Research on Other Fields

Many of the fields addressed by the Subcommittee on Materials for Fabrication of Small Structures will either directly affect the topic of contacts or vice-versa. "Contact Studies" include deposition processes, all classes of thin film studies, lithography (sources, masks and resists), etching processes and fabrication of functioning device test structures to characterize the contact as well as the study of electro-migration and corrosion.

Contact layer film studies will have a continued impact on the fields of optics, superconductor devices, solar cell devices, display devices, medical microstructures and magnetic bubble devices. Implicit in the quest for smaller contact structures will be the development of commercial equipment to provide production capability.

(4) Opportunities for Industry and Universities

Industry will continue their major role where either large capital investments for equipment are needed, or the technological driving force is very strong. Universities may consider studying continuous layers or patterned gross features, i.e., undertake fundamental generic studies. Industry on the other hand may concentrate more on the technology of getting such layers into device test structures, i.e., methods of deposition, patterning and device testing. However, there may be considerable overlap and cooperative programs between universities and industry should be encouraged.

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ELECTROMIGRATION

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ELECTROMIGRATION

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STATUS OF CURRENT WORK

About ten to twelve years ago it was discovered that electromigration, the transport of metal atoms by an electric current, was the cause of failure in the aluminum thin film conductors used in microelectronic devices.[1] This caused a flurry of activity, mostly in industrial laboratories (Fairchild, Motorola, IBM), reflected by numerous publications, which went on for several years. A review published in 1973[2] summarizes the work done in this early and most active period in the history of electromigration in thin films. With the adoption of various palliative measures, which shall be briefly discussed later, the interest of industry in electromigration decreased considerably, resulting in a markedly reduced rate of publication. A relatively small output of articles from two centers of academic interest (Stevens Institute of Technology, and the University of Florida, Gainesville) overlaps the early and more recent periods. A fair idea of the work which has appeared in the open literature up to the present can be obtained from a quite recent publication[3]. Apparently quite fortuitously the decrease in the concern regarding electromigration in thin films, parallels a simultaneous decline in the interest in electromigration phenomena in general, A recent monograph [4] provides a convenient source of information about the current situation with respect to various aspects of electromigration (theory, purification of metals, liquids). It may be noted here that although electromigration phenomena in thin films have been the almost exclusive object of attention, thin films are not the only material related to the electronic technology where electromigration

is manifest. One of the early references to electromigration problems was concerned with soft solders[5] (where the related question of thermomigration[6] may be also significant); quite recently attention has been drawn to the effect of electromigration in liquids on the crystallization of III-V and II-VI compounds[7-9] (which may become of greater importance considering current activities in GaAs devices). Although many of the published studies on thin films have immediate and obvious applications to very small dimensions (width of the order of 1 μm), with a very few exceptions (e.g., ref. 10,11) authors have been concerned with conductors of normal size (width of ~10 μm).

NEEDS

In considering the work to be done in establishing a solid basis for future technology, one may start with an examination of unresolved problems and follow with an analysis of new problems anticipated to arise specifically as a result of the use of conductors with smaller geometries.

1. Problems Remaining to be Solved

a) It is recognized that electromigration in thin film is a grain boundary transport phenomenon. Yet there exist no theoretical work on the electromigration force in grain boundaries, and only very few measurements of this force: on Sb atoms in Ag[12], on Cu atoms in Al [13], for the most technologically important aspect of self transport one can quote only one study of Al in Al[14], and the value obtained there appears suspiciously too low. More work is needed here which should not be limited to thin film studies but should include boundaries between bicrystal samples.

b) Of the three techniques which are used to increase the resistance of thin film conductors to electromigration failure: large grain size, alloying, and dielectric overcoating, only the first one may be said to be thoroughly understood.

Considerable amount of work, probably on bicrystals, is needed to arrive at a realistic atomistic model of the role of impurity absorption in grain boundaries on decreasing the rate of self-diffusion along these boundaries.

The analysis of one aspect of the effect of dielectric overlayers, that of the creation of pressure and stresses and the result therefrom on grain boundary diffusion rates, has led to the paradoxical situation that if a reasonable value of the electromigration force is assumed there should be no effect of dielectric overlays on electromigration lifetimes[15], while the experimental measurement of stress effects led to the derivation of a very low electromigration force [14]. The question deserves clarification; it is conceivable that overlayers effects are not only due to pressure and stress but also to modifications of the role of the free surfaces of conductors as a sources and drains for vacancies, the behavior of which are thought to be important in electromigration failures.

2. Anticipated New Problems

In analysing the effects of decreasing geometries, it is natural to consider direct effects, resulting from a simple consideration of geometrical scaling factors (a, below), and indirect effects resulting from the increasing importance of phenomena which play only a minor role in conductors with sizes prevalent today (b, below).

a) The design of reliable electronic devices requires the knowledge not only of median failure times, but also of the distribution of failure times including the width of such distributions. A

realistic model for the effect of grain size and conductor width on electromigration failure exists [16]; however, discontinuities may be anticipated when the width of the conductors become smaller or commensurate with the grain size. The model needs to be extended and data on failure distributions need to be obtained for such conditions.

Electromigration failure at contacts have received little attention[17] presumably because they are not important with the prevalent existing geometries. It is quite conceivable that with smaller geometries contact problems may become more acute, because contact areas may not scale as other factors, e.g., the cross section of the conductors.

b) With decreasing dimensions it is anticipated that surface phenomena will play more important roles. There are a few references to electromigration at surfaces in W filaments[18] and on Au samples[19]. With thin films one may refer only one bonafide surface phenomena related to electromigration[20]. It is on Ag, and one is uncertain about possible connection to environmental corrosion effects. Of course these too are surface effects and the correlation between electromigration and environmental factors deserve attention. The beneficial effect of an H_2 environment on the electromigration behavior of Al thin film conductors[21] should be mentioned in this context.

3. Other Problems

Other problem areas shall be listed briefly: Pulse effects, largely studied in the context of magnetic bubble devices[22,23] are hardly understood, require much work. There has been very little work done on electromigration in semiconductors, much of it is quite dated [24], some applies to materials for bistable elements[25]. With shallow devices, obtained for example by ion implantation techniques, or with Schottky diodes, one may anticipate problems with electromigration, especially of fast diffusion elements, Au, Li, etc. Work needs to be done to

establish on a firm basis the electromigration rates in semiconductors, not only in the lattice but along short-circuit paths, such as dislocations, and hence to determine the limits at which electromigration phenomena can become a source of device problems.

RELATED SUPPORT

Much of the material discussed above touches upon areas of interest which are distinct from the narrower concerns of the electronic engineer. Electromigration along grain boundaries and effects thereon of alloying additions is a matter of interest to all those concerned with the properties and behavior of grain boundaries. It is a question for the more general physical and matallurgical disciplines. This is also true of course of electromigration phenomena at surfaces. The extension of systematic electromigration work to semiconductors should elicit the interest of theoreticians who attempt to define the fundamental forces at work in electromigration. The problem of migration of Li in Li drifted detectors, in the forward and reverse direction appears intriguing in this respect. The effect of electromigration on the crystallization of GaAs, and other compounds, should interest not only crystal growers but all those concerned with our understanding of the liquid state.

SPECIFIC RESEARCH

At the present time electromigration is a well known, although not universally well understood, phenomenon to the people involved in electronic technology. Industry can be counted on to carry on with the tedious lifetime tests which will continue to be required with the design of new circuits. This is at least true for thin film conductors, and may be less true for semiconductor effects per se, which have been of no concern up to now. However, in order for the technology to evolve in a meaningful fashion an understanding of the basic phenomena need to be provided. By necessity the list of suggested work below will be

somewhat repetitious of what has already been written above, and may be thought of as something of a summary.

Grain Boundaries:

In the lattice the electron "wind force" is proportional to the electric current. How can this concept be extended to grain boundaries in a meaningful way?

Experiments should be directed at a measure of the electron wind force in grain boundaries, possibly in bicrystals. The effects thereon of alloying additions, separation of the effects on the electromigration force, and on the grain boundary mobility should be investigated. How do alloying additions affect the structure of grain boundaries? Relate structural effects to mobility and force terms (above).

Surfaces

Extend work on electromigration on surfaces. The work on Ag thin films was not well controlled and needs to be repeated, and the contributions of ambient effects analysed. The possibility of surface transport effects should be looked for in very thin Au films, possibly also Pt films. However, this surface work should by no means be limited to thin films, but should include whatever type of samples is judged likely to provide information. A critical experiment on the effect of a dielectric overlayer on electromigration in thin films, separating stress effects from other (if any) effects is badly wanting.

Pulse Effects

The problem there remains ill defined and it appears difficult to provide suggestions for experiments. Apparently, once the duty cycle has been factored out the lifetimes of thin film conductors undergoing pulse testing remain longer than would be anticipated on the basis of

the results obtained under pure dc testing. This is all the more surprising, since under pulse testing one would anticipate accelerated failures due to the contributions of thermal fatigue. These latter effects have not been separately analysed. This should be done, either under ordinary ac current, or preferably with reverse square wave pulses. Beyond this one should look at possible time effects in the nucleation and growth of holes.

Liquids and Semiconductors

Experiments should be done on the electromigration of fast diffusing impurities in semiconductors, e.g., Au, Cu, Li, etc. The forces at work should be defined, the contributions of short circuit diffusion paths measured. To limit oneself to GaAs, the electromigration of Ga and As atoms in liquid GaAs should be measured, as well as the electromigration of doping additions in the medium.

Solders

Experiments on electromigration and thermomigration effects in soft solders, including possible atmosphere interactions, would contribute to the general fund of knowledge upon which a successful technology can be built.

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APPLICATIONS OF ELECTRONICS TO MEDICINE

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ABSTRACT

Due to their revolutionary rate of advance for nearly two decades, integrated electron devices can be applied in medical instruments with outstanding advantages to the quality and availability of health care. To provide an overview of activities in this field, various types of medical electronic instruments are classified in a matrix format according to their orientation relative to the patient and the generic function which they perform. Explicit examples which illustrate the utility of custom integrated electron devices are: i) totally implantable blood flow telemetry for use in research animals, ii) noninvasive ultrasonic imaging systems for diagnostic and monitoring functions, and iii) a prosthetic optical-to-tactile reading aid for the blind.

INTRODUCTION

Health care presents a singular opportunity to improve the quality of life in our society through electronics. In modern medical research a myriad of electronic instruments ranging from pinpoint-size implantable microelectrodes to 1 MeV electron microscopes contribute immeasurably to the identification, treatment, and prevention of disease. In current medical practice the premier diagnostic and monitoring tools are electronic instruments, as illustrated by the computerized x-ray tomograph, ultrasonic echograph and electrocardiograph. The electrical defibrillator commonly provides life-saving therapy for patients under cardiac arrest, while an electronic reading aid for the blind is a prosthetic instrument which offers significant social and economic benefits to the visually handicapped. Due to their revolutionary rate of advance for nearly two decades, integrated electron devices can be applied in medical instruments with outstanding advantages to the quality and availability of health care [1].

ORIENTATION AND FUNCTION MATRIX

To provide an overview of the field, various types of medical electronic instruments can be classified according to their orientation relative to the patient and the generic function which they perform, as illustrated by Fig. 1. In this representation each matrix element is a specific example of a particular type of instrument. In most instances a matrix element can be described by a rudimentary block diagram, as shown in Fig. 2, which consists of input sensor, central processor, and output or display blocks. Frequently, commercially available general purpose integrated electron devices, such as silicon microprocessors and custom software, are used to meet the peculiar requirements of a central

processor. The resulting "smart" instruments can have a remarkable impact on medicine. This is most profoundly demonstrated by the computerized x-ray tomograph which has revolutionized diagnostic radiology [2].

Moreover, output or display hardware may vary from a general purpose television monitor to quite special purpose tactile displays for the blind depending on the orientation and function of an instrument. It is the input sensor, however, which most frequently benefits from special purpose integrated electron devices. Design and fabrication of custom transducers and preprocessor circuits are often necessary to satisfy the unique requirements of hardware which must acquire data from biological systems. Consequently, the keys to many promising new medical instruments tend to be the custom integrated electron devices directly associated with the input and output interfaces. The following discussion deals with these key devices. More explicitly, examples are described of custom integrated electron devices in i) totally implantable telemetry for use in research animals, ii) noninvasive imaging systems for diagnostic and monitoring functions, and iii) a prosthetic reading aid which allows immediate access by the blind to all printed material normally used by sighted people.

IMPLANTABLE TELEMETRY IN RESEARCH

In science and engineering the contributions of models to the process of discovery and invention can hardly be overestimated. Clearly, computer-aided modeling of integrated electron devices has been a crucial factor in their rapid advance. For compelling ethical, legal, scientific and economic reasons animal models which simulate human behavior are indispensable tools in medical research. Using animals, otherwise impossible experiments can be conducted which contribute immeasurably to improved health care for man. In countless instances, the value derived from animal experiments can be enormously enhanced by acquisition of data which: i) cannot be collected from the surface of the body, ii) is available only if the animal is neither anesthetized nor restrained, and iii) must be gathered throughout the course of a study extending over many months. For such chronic animal investigations miniature telemetry units which are surgically implanted in the host animal represent a unique tool.

Because the vitality of every organ in the body depends upon the flow of blood to it, the capability for accurate estimation of blood flow is extremely valuable in many chronic animal studies. A block diagram of a recently developed implantable pulsed Doppler ultrasonic blood flowmeter is illustrated in Fig. 3. In this instrument the gated oscillator provides a short 1 μsec burst of 6 MHz high frequency excitation to a piezoelectric transducer immediately adjacent to a blood vessel. During a relatively long 50 μsec interval following each transmit burst, the associated ultrasonic pulse traverses the vessel diameter producing back-scattered signals, emanating from moving erythrocytes, which are amplified, detected and telemetered by the internal electronics. At any instant the Doppler frequency shift in the back-scattered signals is proportional to blood velocity (v) at a particular location within the lumen defined by the corresponding ultrasonic transit time of a

transmit burst. The range gated external electronics provides many spatially discrete samples of a blood velocity profile whose electronically derived integral over the lumen area is an accurate estimate of instantaneous bidirectional volume flow.

Two special purpose monolithic integrated circuits have been demonstrated to provide the high performance, small size, low power drain and reliability required in the implantable unit [3,4]. Without these custom electron devices this implantable flowmeter would be unfeasible. Application of the unit in heretofore impossible investigations of cardiac pharmacology, fetal and neonatal physiology and hepatic hemodynamics in cirrhosis is in progress [3,4].

NONINVASIVE ULTRASONIC IMAGING FOR DIAGNOSIS AND MONITORING

The ideal diagnostic instrument provides definitive data on a patient's condition, causes him no harm or discomfort, and is convenient, reliable and economical for a physician or his medical associates to operate. A monitoring instrument imposes the additional stringent objective of virtually total freedom from the need for human intervention during prolonged periods of operation. Because of its apparently harmless and noninvasive character, transcutaneous ultrasonic imaging offers great potential for fulfilling these idealized specifications. In contrast to x-rays, two principal features of ultrasonic instruments are i) their capability for real-time imaging of moving targets such as the heart, and ii) their complete avoidance of tissue damage by ionizing radiation.

A block diagram of a new electronically scanned and focused phased array system is illustrated in Fig. 4. In this instrument a short coherent burst of 2.25 MHz ultrasonic energy is emitted by a 32-element piezoelectric transducer array contained in a hand-held probe in contact with the patient. As the packet of ultrasonic energy propagates through the body, most of it is lost through tissue absorption, but a small amount is reflected or scattered at boundaries between materials of differing acoustic impedance. It is the reflected or scattered component, which returns to the transducer array, that provides useful information. Following preamplification by a matched array of 32 low noise, wide dynamic range, voltage variable gain circuits, returning signals are time delayed and summed by a 32-input four-element cascade charge coupled device (C3D) lens [5]. Through appropriate control of clock frequencies f_3 and f_4 the two linearly tapered elements of the lens provide electronic scanning in a 60°-80° sector pattern for a large field of view. Control of clock frequencies f_1 and f_2 of the quadratically tapered elements permits electronic focusing for high resolution.

Noninvasive ultrasonic instruments are very widely used in medical practice for cerebral, ophthalmic, thoracic, abdominal and fetal imaging. Extremely promising opportunities for improved capabilities are in the offing through the application of custom integrated electron devices in i) the piezoelectric transducer array [6], ii) the preamplifier array [7] where analog LSI is most desirable, iii) the high voltage transmitter array [8], and iv) the C3D electronic lens [5].

A PROSTHETIC READING AID FOR THE BLIND

For many humans the quality of life is greatly diminished by loss of some natural function. Blindness, deafness, paralysis, and loss of limbs are afflictions suffered by many. The powerful and compact sensory, computational and display capabilities of integrated electron devices make possible promising new avenues for prostheses to remedy these functional deficiencies. Sensory prostheses frequently operate transmodally, mapping information normally gathered by an impaired sense onto an intact one. The Optacon optical-to-tactile reading aid for the blind is such a prosthesis [9].

In principle the Optacon is a direct translation reading aid for the blind which converts an optical image of a printed character on a page of an ordinary book, magazine or newspaper to a vibrating tactile facsimile. A block diagram of the instrument is illustrated in Fig. 5. By means of a simple optical system contained in a hand-held camera, an image of a printed character is focused on a custom 6 X 24 monolithic array of phototransistors. Output signals from the phototransistor image sensor array are processed in a simple electronic system, and then used to control a corresponding 6 X 24 array of piezoelectric tactile stimulators or bimorphs. The bimorphs are excited by custom monolithic arrays of high voltage (100V) MOS circuits. Tiny pins cemented to the bimorph tips protrude slightly through perforations in a rectangular plastic plate. A blind reader whose fingertip is resting over the perforations can then feel an accurate tactile facsimile or vibrating image of the original printed character. Several thousand Optacons are now in daily use by blind individuals in many countries [10].

CONCLUSION

In many instances the projected market for a custom integrated electron device required in a particular medical instrument does not provide economic justification for its development by private industry. Both the small size of the market for such a custom device and the extended lead time required for its research and development, which must be followed by thorough medical evaluation of the instrument itself, mitigate against private investment. However, the overall social and economic benefits of such investments may outweigh many of those which are economically feasible for a particular private enterprise. In addition, the strong interdisciplinary teams of engineering and medical investigators which typically are required to research a radically new instrument concept are very infrequent in private industry. Considering the foregoing statements, one is led to the hypothesis that public support of research dealing with integrated electronics in medicine which is conducted in a university environment may offer a viable approach to many problems in the field of advanced medical instrumentation. From a university viewpoint such research provides both the highly stimulating intellectual challenge necessary for effective graduate education and research as well as the prospect of an important and unique benefit to the society which the institution serves.

In summary, the initial impact of integrated electron devices on health care is now visible, and consequently, it is postulated that we

are beginning a new era of revolutionary advances in medical instrumentation. Health care may indeed present the most promising opportunity to improve the quality of life in our society through electronics [11,12].

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BIOMEDICAL INSTRUMENT MATRIX - ORIENTATION VS FUNCTION

	RESEARCH	DIAGNOSTIC	MONITORING	THERAPEUTIC	PROSTHETIC
SUBCUTANEOUS	TOTALLY IMPLANTABLE TELEMETRY		CEREBRAL PRESSURE TELEMETRY	NERVE BLOCK FOR PAIN RELIEF	CARDIAC PACEMAKER
SUPERCUTANEOUS	ANIMAL BACKPACK TELEMETRY	INGESTIBLE pH TELEMETRY CAPSULE	AMBULATORY CARE ECG TELEMETRY	NERVE BLOCK FOR PAIN RELIEF	HEARING AID
PERCUTANEOUS	IMPLANTABLE TRANSDUCER WITH EXTERNAL LEADS	CATHETER-TIP BLOOD GAS SENSOR	CATHETER-TIP PRESSURE SENSOR	THERAPEUTIC MUSCLE STIMULATION WITH PERCUTANEOUS ELECTRODE	FUNCTIONAL MUSCLE STIMULATION WITH PERCUTANEOUS ELECTRODE
TRANSCUTANEOUS	X-RAY	COMPUTERIZED X-RAY TOMOGRAPHY	ULTRASONIC IMAGING	DEFIBRILLATOR	ELECTRONIC READING AID FOR THE BLIND
EXTRACUTANEOUS	ELECTRON MICROSCOPE	MASS SPECTROMETER	GAS CHROMATOGRAPH		

Fig. 1. Biomedical Instrument Matrix - Orientation versus Function

RUDIMENTARY SYSTEM BLOCK DIAGRAM

Fig. 2. Rudimentary System Block Diagram

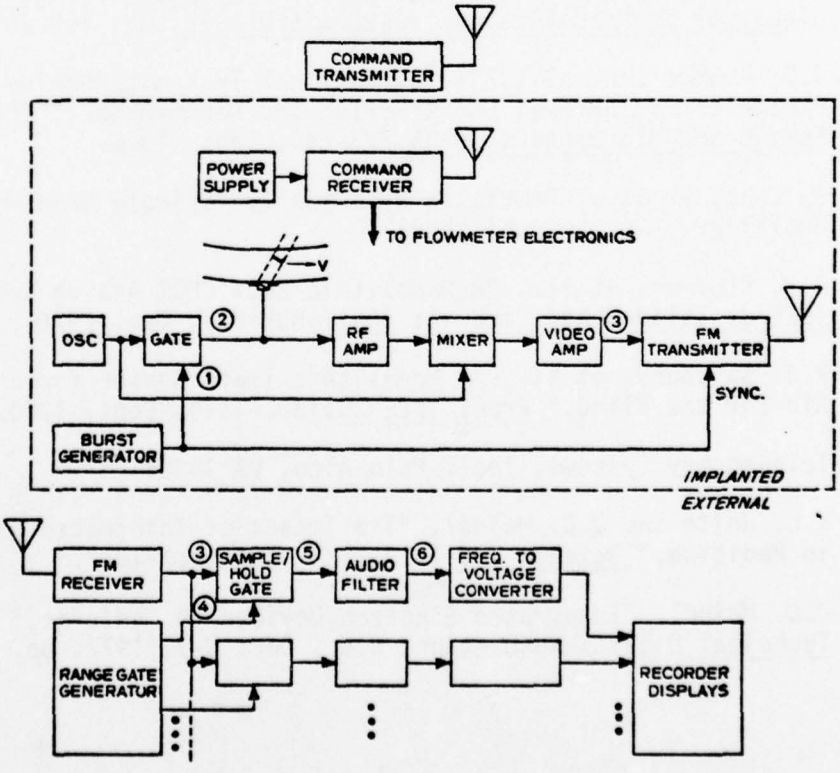

Fig. 3. Implantable Flowmeter Block Diagram

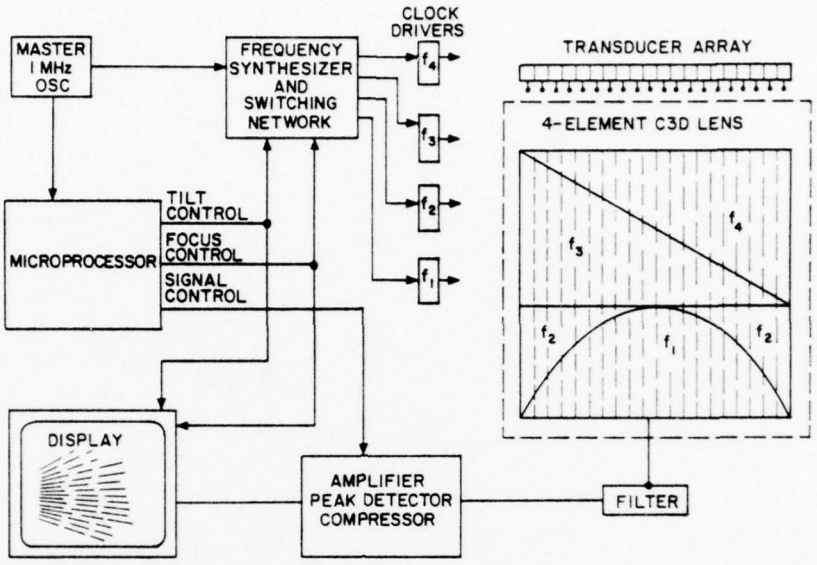

Fig. 4. C3D System Block Diagram

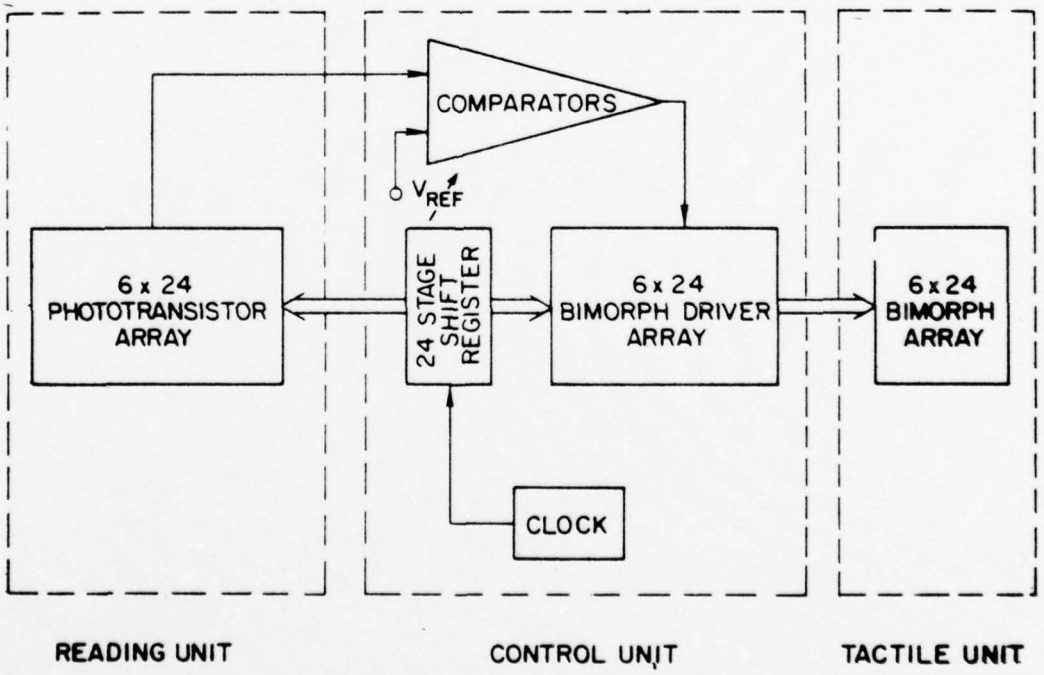

Fig. 5. Optacon Reading Aid Block Diagram

Solid State Devices as Material Probes

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I. Status

Initial device concepts usually depend on a view of a solid state device as composed of interacting regions of materials, each region having properties that have been established for the materials in bulk form. The exploitation of devices for technological purposes, however, often leads to the production of unique environments in the solids involved, in which known bulk properties do not provide a guide to the behavior of materials. Novel phenomena occur in the unusual environment created, phenomena unfamiliar and unexplored in the bulk material or involving unanticipated interactions between various parts of the material system.

The special nature of the environment to which materials are exposed in solid state devices has been accentuated by the advance of miniaturization in electronics. The dimensions of significant regions of solid state devices have become comparable to the fundamental length parameters that enter into the theory of solid state phenomena, such as optical wave lengths, electron wave lengths, screening lengths in electronic systems, widths of depleted regions in semiconductors, and thickness of magnetic domain walls. Solid state devices permit the properties of materials under the specialized constraints produced by miniaturization to be studied. The unique conditions to which materials are exposed in solid state devices have led to the discovery of, or, at least, the recognition of the importance of, many new effects in solids and furnish a valuable tool with which the scientist can investigate various properties of matter. The new phenomena discovered in devices have stimulated a large body of research in solid state science and the techniques of device fabrication have played an important role in making various avenues of research feasible.

The course of events is best illustrated by examples. Consider the p-n junction in a semiconductor. The simplest view of a junction regards it as adjacent p and n regions separated by a thin region depleted of carriers by the potential difference between n and p type semiconductors. Current flow is decribed by Shockley's model, which perturbs the concentrations of electrons and holes in the vicinity of the junction.

When junctions are made, however, it turns out that above certain voltages applied in the reverse, or low current, direction the current is orders of magnitude higher than predicted by simple theory. The effect is called dielectric breakdown, and had been known for many years. The very high fields existing in the depletion region of p-n junction, however, made breakdown a commonly encountered phenomenon, and, also, an important practical problem in that it limited the range or application of devices. Moreover, because of the ease with which high electric fields can be produced in p-n junctions, the junctions themselves became the primary vehicle for the study of the breakdown. Thus a new area of solid state physics was opened to exploration by the unique environment in the depletion region of a p-n junction.

The study of breakdown in junctions soon revealed that two effects were involved: Tunneling on "Zener" breakdown and avalanche breakdown, in which electrons acquire enough kinetic energy to excite another electron across the gap from the valence band to the conduction band. It was found that tunneling could be intentionally enhanced to create a new kind of device, the tunnel diode. The tunnel diode has not gained an important place in technology but has been realized in many semiconductors and exploited at low temperatures as a probe of the phonon and electronic energy band structures of semiconductors. Investigations of the mechanisms of avalanche breakdown led to the concept of hot electrons and eventually to the discovery of the Gunn effect and a vast field of research into scattering mechanisms of hot electrons in many semiconductors.

Electric fields high enough to produce hot electrons also occur in field effect transistors. The hot electrons are produced in close proximity to an SiO_2 layer in insulated gate FETs. A few electrons attain enough energy to surmount the potential barrier confining them to the semiconductor and escape into the SiO_2. Here they may be trapped, creating fixed charges in the SiO_2. The presence and distribution of this trapped charge affects the device characteristics, which characteristics can therefore be used a a probe of such material properties as the cross section and concentration of the traps, the motion of electrons in the SiO_2, and the effects of modifying the SiO_2 on the traps. The insulated gate FET thus constitutes an unusual materials system in which the capability of silicon to produce controlled quantities of hot electrons and its intimate contact with SiO_2 provides a means for probing the electronic properties of SiO_2.

Field effect transistors also provide a unique environment in that conduction in the semiconductor occurs in a thin layer, a layer less than 50A in thickness. The layer is so thin that motion of electrons confined in the layer is quantized in the direction normal to the surface; the quantum is much larger than kT in the cryogenic regime. The electrons in the layer thus constitute a system in which the properties of electrons with freedom to move in only two dimensions can be probed. There is a large amount of flexibility in the FET environment which makes it extraordinarily useful; the thickness of the layer can be varied by varying the electrical potentials applied to the device, and the scattering can be varied by introducing charged impurities in the SiO_2 and by doping the silicon. It is worth noting that, although the quantization effects could be predicted from physical theory, their experimental discovery was stimulated by the observation of anomalies in FET device characteristics.

The above examples all concern electronic properties of solids. This is a consequence of the fact that the exploitation of miniaturization has been most intense in the area of electron devices. However, other areas that have been invaded by miniaturization have also brought obscure phenomena into prominence. For example, Bloch lines in domain walls affect the properties of magnetic bubbles. At the high light intensities in semiconductor lasers photons can assist atomic motions, causing degradation of the lasers. There is potential for studying novel solid state phenomena with such devices.

II. Needs

Although the effects that are unexpectedly encountered in solid state devices are most often intensively investigated to achieve a more complete understanding of their role in devices, they can also often be used as a deliberate probe of material properties, a tool of material science. The use of oxide-gate FETs to study the two dimensional electron system and quantization normal to the surface, and the properties of SiO_2 have been mentioned, as has the use of tunnel diodes to locate energy levels in solids. The characteristics of bipolar transistors have been used to measure the energy gap of silicon, in particular, the dependence of the energy gap on doping, an experiment that depends on the ability of device technology to fabricate n-p-n structures in which the thickness of the p region that separates the n regions is small compared to the diffusion length of electrons.

There is a large element of accident or luck in the use of devices to probe material properties. It is infrequent that, given a material property, a device will be found that is sensitive to that property. Somewhat more often it turns out that a characteristic of a device provides a useful measure of a material property. Thus, exploitation of devices as material probes would most profitably start with a view that asks: What materials properties can be examined with a known device type? Most experimental studies that use devices to reveal the basic properties of solids have been performed with silicon, because the technology of fabricating devices in silicon is so far ahead of that in other materials. There appear to be possibilities for extending the applications of devices that have been demonstrated in silicon to other semiconductors. Furthermore, device technology can frequently be used to fabricate structures intended as materials probes, that is, devices that are not optimized to perform some useful function, but designed to extend the range of environments in which a phenomenon is studied. Thus, the field effect transistors used to study quantization in the surface layer would not be the FET's that one would use in a semiconductor memory. Some of the bipolar transistors used to measure the energy gap of silicon would have doping levels that are not very suitable for useful devices. Even further away from application are larger n-p-n devices that can be used as DC transformers but found their principal use as probes of phonon properties by means of the transmitted phonon drag effect. There are many opportunities to apply devices and device technology to problems in material science.

III. Opportunities

The fortuitous nature of the application of devices as materials probes has been pointed out. Consequently, it is not possible to manage this application in the same way as areas which are oriented towards fulfilling a recognized technological need may be managed. Devices are developed to perform useful functions and their development to serve as materials probes cannot be anticipated. The deviations of devices from their predicted performance that leads to the discovery of novel phenomena cannot be programmed nor can the inventions devices to probe specific materials properties. Thus the orientation of research towards the application of devices as probes of material properties in a general way would be fruitless.

The opportunities for the management of research and development to take advantage of the application of devices as material probes must be through an alertness to possibilities that may evolve in the course of device development. Unusual features of device performance that may represent an unexpected material phenomenon should be vigorously pursued. The conformity of device characteristics to theoretical predictions ordinarily conveys no new information. Rather, it is the failure of devices to perform as expected that may hint at the novel and unusual phenomena that can be the key to new device invention or to additional tools for the exploration of the properties of the solid-state.

The principal barrier to the use of devices as tools in the study of materials is lack of access by the materials scientist to device fabrication facilities and lack of knowledge of the complexities of device technology. Successful application of devices to the study of materials requires the participation of those skilled in the technology of device manufacture. Organization and funding of developmental and pilot device production lines should be structured to insure their availability to materials scientists. For example, since device fabrication facilities are relatively rarely found in universities, device production facilities assisted by Federal funding should be obligated to provide access to the facilities by academic research workers and partially measured by the success of the research. Funding of joint university-industry research, as in certain recent NSF programs, provides another means to increase the availability of fabrication facilities to university workers.

SEMICONDUCTOR ELECTRONICS

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ON THE OPPORTUNITIES FOR UNIVERSITY RESEARCH CONTRIBUTIONS IN VLSI RESEARCH

It is widely recognized that a turning point in the continued development of integrated circuits has been or soon will be reached. This is largely a result of two factors.

- Continued skrinking of lateral and vertical geometries in integrated circuit structures is now dependent not only on better lithographic techniques for defining such patterns but also on better understanding of the fundamental limits of device size and on a better understanding of the physical processes used to fabricate the devices.
- Continued increases in the number of components fabricated and interconnected in a single integrated circuit make detailed interaction between system architecture and integrated circuit topology essential.

Essentially these points imply that close interaction between integrated circuit engineers and material scientists on the one hand and between integrated circuit engineers and computer scientists on the other hand are essential for continued progress. Universities with their interdisciplinary environments, make such interactions potentially easier than most industrial environments currently engaged in integrated circuit manufacturing. Thus the opportunity exists for substantial university impact in both the areas outlined above.

The remainder of this report pursues this theme discussing heavily upon a number of reports and proposals prepared in the Department of Electrical Engineering at Stanford University through the contributions of J.G. Linvill, J.D. Meindl and J.D. Plummer of the Integrated Circuits Laboratory, J.F. Gibbons of the Solid State Laboratory and M.J. Flynn of the Digital Systems Laboratory.

The IC/Solid-State/Materials Science Opportunity

The rapidly increasing use of microprocessors in a wide variety of commercial and military applications has brought with it the need to increase the "functional density" on a silicon wafer by an order of magnitude or more, if possible. Such a goal is of commercial significance, since an increase in functional density will reduce the size and, hence, the cost of an integrated system with given capability. The military interest in such a development is not so much in cost as in substantially increased computational capability on a larger chip.

In either case, the integrated circuit designer is faced with the problem of designing and fabricating devices with a minimum feature size that is about an order of magnitude smaller than that presently used. This decrease in size implies that most of the important device action will be occurring in regions of the semiconductor that are within 0.5 to 1 μ of the surface and, as a result, "surface" doping and analysis techniques will be of substantially greater importance in the next decade than they have been in the past. Substantial progress in understanding surface related phenomena should be possible through an organized effort involving scientists in materials science, solid state and integrated circuit technology areas.

Although our knowledge of basic processes such as ion implantation, thermal oxidation, diffusion and epitaxy has increased dramatically in recent years, it is still in a relatively primitive state. The device implications of this are so dramatic that the need for further research is paramount. The advent of complete process simulation techniques and the coupling of process physics with device physics by means of powerful computer tools mark key steps toward achieving VLSI. Moreover, through

automation of process equipment the most widely fluctuating variable -- the human operator -- is removed from increasingly larger and more sensitive segments of the VLSI fabrication sequence. In addition, automated data logging and subsequent convenient data access via remote computer terminals provide much more accurate and timely information regarding the fabrication sequence to which a given wafer or chip was exposed. Combining this information with that generated through automated electrical testing of wafers allows much more effective feedback to the fabrication line.

Considering the arguments of the preceding paragraph, competitive pressures alone -- both domestic and foreign -- necessitate increasing use of VLSI process models. However, from another aspect, current and projected product goals clearly indicate the increasing necessity for VLSI process models. For example:

- The development of complex monolithic chips to perform in a large focal plane array including more than 10^5-10^6 IR CCD image sensing elements with on-board high speed ECL digital signal processing, entails a complex fabrication technology which demands full exploitation of available process and device models.

- The development of semiconductor RAM chips with more than 10^6 bits of storage, minimum feature sizes under 1.0 μ (approaching the fundamental physical limits of MOSFETs), superior reliability taken for granted, and a selling price less than $20, places a burden on fabrication technology which also demands full exploitation of available process and device models.

- The development of true single chip "microsystems" -- following microcomputers which in turn followed microprocessors -- with, for example, only one external power supply, all internal clocks, latches and buffers, on-chip EPROM and RAM and compatible integrated A/D and D/A converters, as well as analog preprocessors and output drivers, will place perhaps the ultimate burden on semiconductor fabrication technology and clearly will require extensive reliance on process models.

In designing the semiconductor products -- the integrated systems or single chip microsystems -- suggested in the previous paragraph, the

ultimate utility of VLSI process models will be measured in the reduced development time for a complex new chip, in reduced development cost due to time and labor savings, in reduced production costs due to higher yields, in higher product reliability resulting from tighter process control and in improved system performance due to the richer set of trade-offs available to chip designers.

In summary, better understanding of the processes used in integrated circuit fabrication (oxidation, ion implantation, diffusion and epitaxy) and their interactions are essential to the successful fabrication of very small geometry devices. Such understanding is best utilized in computer process simulation programs which permit accurate two-dimensional simulation of device structures resulting from arbitrary fabrication sequences. Understanding of these physical processes on a microscope level requires the coordinated efforts of materials scientists, solid state physicists and integrated circuit technologists. Such a combination of people might best be found in an interdisciplinary university environment although substantial contributions to these problems are to be expected from the industry as well.

The IC/Digital Systems/Computer Science Opportunity

Man's intelligence through electronics/computers has already had a profound effect on current society and human understanding. There is every indication that present technology is accelerating its capability to produce complex programmable structures. This acceleration is both a problem and a challenge.

Human organizations reflect our understanding of their mission and its decomposability; disciplinary boundaries are defined at points of

minimum contact. Representations, techniques, and solutions are constructed within a discipline, assuming that the disciplinary boundary is unchanged. Communication across boundaries is done in static terms that simplify disciplinary understanding.

Possibly nowhere is the above more true than in the computer area and its relationship to modern developments in integrated electronics; for example,

- Algorithms are still treated independent of topology interconnections while the latter dominate physical implementations.
- The microprocessor strongly resembles computer structures of a decade ago -- largely implemented on the basis of textbook tradition.
- System complexity -- both hardware and software -- becomes a pre-eminent issue: first design costs, design verification, development time are the problem; yet automated assistance tools remain primitive.

To pass beyond this stage of limited interaction requires, essentially, the restructuring of a discipline. Examples of the problem areas that need attention are:

- Programming systems: verification and design of large and complex systems.
- Computer-aided design of both hardware and software systems, including testing, testability, verification, fault-tolerant design, simulation, automated interconnection.
- Issues related directly to integrated circuit technology such as signal propagation research and low-energy switching phenomena.

In order to begin a program of holistically linking materials processing science with information systems science, a "top-down" approach to VLSI is needed. Historically the design of a digital system has often followed a four-phase, bottom up procedure. First, the process/device engineer, forecasting the requirements of the circuit engineer, developed

a compatible sequence of semiconductor fabrication processes for a new family of integrated circuits. Second, the circuit designer, anticipating the needs of the system designer, provided a set of components capable of performing various logical functions. Then the system designer, anticipating the needs of the software programmer, assembled the hardware into a digital system for solving a class of problems of interest. Finally, the programmer implemented an algorithm to solve a problem of immediate concern. Limited feedback ensued, but after the functional and physical separation had been established, the partitioning of the problem was rarely viewed as a whole, except at the final stage.

With the introduction of VLSI, this traditional evolution may no longer effectively solve many problems of interest. The complexity of the problems we can now consider solving at the level of a single chip, the blurring of the distinction between hardware and software, and their comparable complexity, call for a new segmentation of the design process which is more holistic than past approaches.

The alternative methodology, a top-down approach, separates the design of a VLSI application into two phases: an initial theoretical phase and a final practical phase. The initial phase begins with the collection of a set of problems for solution. These problems are then abstracted, and solution methods are proposed.

The second phase begins by grouping these algorithms to isolate a compatible set of problems requiring a common method of solution. A solution for a specific problem class can then be specified in terms of hardware and software, and a logical partitioning into constituent modules can be made. As the last phase of the practical design, a physical

partitioning is made, and implementation proceeds.

This top-down approach is valuable for several reasons. As the distinction between hardware and software becomes increasingly blurred, the complexity available with VLSI will undoubtedly lead to the same type and magnitude of problems that have plagued the development of large software projects in the past. The key element in such a project is a proper logical partitioning of the solution into self-contained modules with clean, general, extensible interfaces. Within this framework the physical partitioning required at an early phase by the bottom-up design is unclear; the early division into fabrication process sequence, circuit chips, circuit boards, and software modules may prove deleterious with complex systems.

For example, consider the evolution of a large computer operating system. Segmented into modules at its inception, any repartitioning after its release to customers is an expensive but feasible endeavor. However, after the customers develop applications software dependent upon that operating system, repartitioning quickly becomes prohibitively costly. With VLSI, repartitioning will presumably be as expensive, and errors will be as hard to correct.

These problems are rarely seen at the SSI and MSI circuit level when chips consist of just latches, gates, registers, counters, etc. Even today, on the eve of VLSI, industry focuses on implementing standard, well-understood logical structures and processors. This approach, however, should become decreasingly viable as VLSI is used for implementing specialized hardware designed to meet specific requirements.

The top-down approach to system partitioning problems described above, clearly requires close interaction between computer scientists, digital system designers and integrated circuit technologists. Such an

interdisciplinary team may again be effectively organized in a univeristy environment to attack these problems. As in the IC/Solid State/Materials Science opportunities previously described, however, substantial contributions come from industrial organizations where the requisite team of people exists or can be gathered.

MICROMAGNETIC DEVICES

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I. INTRODUCTION

Micromagnetic devices are an important new category of microelectronics in the steady improvement in cost/performance of electronic systems. So far micromagnetic devices have been used almost exclusively for information storage but they have properties that offer possibilities for logic or display, especially in conjunction with storage. The storage devices have a cost and speed intermediate between the lowest cost semiconductors and magnetic recording. At the same time they provide a unique combination of the best features of those other technologies (electronic speeds, modularity, non-volatility) plus a stop/wait/restart on demand capability that neither of the others have and are fabricated by an integrated circuit process, simpler even than for semiconductor devices, allowing low cost. These devices have already been used for such diverse applications as storage in a portable terminal (e.g., Texas Instruments [1]) and telephone answer-back (Bell Telephone [2]). Other applications will undoubtedly be forthcoming (e.g., storage with micro- and mini-computers [3], storage hierarchies for large computer systems in conjunction with semiconductors and disks [4], flight recorders [5], text-editing [6], etc.), especially as further microminiaturization leads to even lower costs. Thus progess toward such microminiaturization should result in a substantial payoff.

Micromagnetic devices involve the manipulation of small magnetic domains in a thin film of appropriate material. Most of the progress has been in a variety of forms using cylindrical magnetic domains, called "bubbles," but there has also been effort to develop alternate approaches such as the "crosstie" memory [7] and the domain tip, "DOT" [8,9]. Suffice

it to say that micromagnetics is not limited to a single embodiment and more variations may be invented with additional research. We will limit our discussion to the various forms of bubble storage because this is the main stream of activity and progress, is diversified enough to show the various dimensions for further progress and is sufficient to illustrate the type of fundamental work that should be fruitful in micromagnetics and the relevant materials.

There is a main thrust in magnetic bubbles that a host of companies are following and then there are variations on the theme which are being pursued in order to achieve greater circuit density and lower cost. We will first discuss the current main thrust, then the factors which hinder the achievement of greater density in this main thrust, then the variations that are already being explored to avoid these hindrances and, finally, areas of research which our current knowledge suggests as important for future progress. This discussion can be only a summary and references are included that allow the interested reader to obtain more information on any of the various items mentioned.

II. THE MAIN THRUST IN BUBBLES

As with semiconductor technology, the bubble technology involves circuit chips mounted in modules which in turn are mounted on circuit boards. The chips are fabricated with optical photoresist lithography wherein patterns of magnetic permalloy and conductors are defined on top of a thin single crystal magnetic film which has been grown by liquid phase epitaxy on a wafer of single crystal non-magnetic garnet. The

magnetic film will support small cylindrical domains, bubbles, as long as a constant bias field, H_B, is maintained perpendicular to the film. H_B is provided by permanent magnets built into the module. The bubbles move along tracks, defined by the permalloy pattern, under the influence of a rotating, in-plane magnetic field, H_{xy}. H_{xy} is generated by two out-of-phase currents in a pair of coils built into the module. The bubbles are shifted from one track to another by switches controlled by the magnetic field due to a current in a conductor line. The bubbles are detected by the voltage pulse they produce in a magnetoresistive sensor. Thus there are a few conductors on the chip which must connect to the module pins to provide for bubble generation, track switching and bubble detection. However, no physical access is needed to each bit position, in contrast to semiconductors; propagation at all bit locations is induced simultaneously by the overall rotating field.

A typical chip has the following parameters: 64-256 Kbits; 2 μm magnetic film; 0.5 μm permalloy, conductor and SiO_2 spacer layers; 3 μm diameter bubbles; permalloy patterns with 1.5-2.0 μm minimum features that repeat on a 14-16 μm scale, defining the unit bit cell; $H_B \simeq 150$ Oe, $H_{xy} \simeq 50$ Oe at 100-250 KHz; current pulses ≃150 MA to generate, 20 MA to switch, 5 MA to detect; detector output ≃3 MV.

A module contains sometimes one chip (e.g., TI), sometimes a few (e.g., BTL packages four in a module), sometimes many (e.g., Hitachi packaged 32 chips in one module).

If a complete chip with ~100 Kb is pictured, it is not possible to see the detail. Figure 1 is a pattern for a smaller experimental chip that shows the overall pattern. The storage loops are in the center, the input loop is on the left and the detector at the right. Bubbles are generated when conductor G is pulsed. These bubbles flow down the chevron input loop to an inverse generator, or annihilator, unless the write conductor, W, is pulsed, in which case they transfer to the storage loops. In this small chip the storage loops have only 40 chevrons each vs the 500-1000 that are typical of product chips. The bubbles continue to circulate in the storage loops under the influence of H_{xy} unless the read conductor, R, is pulsed, in which case they transfer to the output loop and proceed to the chevron expander. The expanding chevron pattern expands the bubble into a strip which then propagates to the right past the detector, D. The detector is a column of interconnected chevrons. Because this permalloy chevron column is magnetoresistive a change in IR drop is observed across the column when the magnetic strip passes. The detector column has to be long to increase the sensitivity and the bubble must be expanded to cover the detector and make it efficient. A shorter detector of equivalent resistance can be achieved by making it narrower and thinner and then the bubble does not require so much expansion at the cost of chip real estate. The "thin" detector, however, requires an additional fabrication step.

The permalloy elements in Fig. 1 define the bubble positions and information is coded by the presence or absence of a bubble in each bit position. When using this method of coding the bubbles must be kept 4-5 bubble spaces apart to minimize their magnetic interference. In addition,

the bubbles must be larger than the gap between elements by a certain multiple or the barrier to transfer is too great. The main influence of the design of the permalloy elements is on the ratio of bubble size, d, to gap dimension, g, that will allow propagation with good operating margins. Obviously that pattern is preferred which permits the smallest d/g because it will provide the largest circuit density for a given lithographic process capability. The resolution and reproducibility capability of the lithographic process determines the g that can be used. The circuit density is inversely proportional to the unit cell dimension or pattern repetition period, P, and P=4-5d=4-5(d/g)g. With the asymmetric chevron element, "AC", used in Fig. 1, d/g can be two or even somewhat less. With older propagation elements, such as the "TI" elements, d/g had to be greater than three and preferably four. This discussion is important because it shows first of all that circuit density can be improved by the invention of better element shapes as well as by refining the lithographic process. In addition, it shows that circuit density can be improved even more fundamentally by finding a coding scheme that allows bubbles to interact so they can be less than 4-5 spaces apart or by finding a different propagation technique that would remove the restriction that bubbles be larger than the minimum feature. Indeed, approaches are being worked on to accomplish each of these and we will discuss these after we finish reviewing the present situation.

Many companies by now are working on magnetic bubble technology: some are in an exploratory phase, some are developing commercial products and some have been engaged in the manufacture of qualified products for over

a year (e.g., Western Electric, Texas Instruments). Most of these companies have publicly disucssed the configuration and properties of their chips and modules; others, like IBM, have published technical results of their bubble research but have not yet disclosed whatever product configurations they may be working on. The following list indicates the progress that has been achieved in the main thrust of the technology, as revealed by the published literature in the summer of 1978:

1) Bell Telephone Laboratories/Western Electric:
   - 68 Kb chips with 16 μm circuit period AC elements packaged four to a module being manufactured and used for record-message playback [10].

2) Texas Instruments:
   - 92 Kb chips packaged one to a module being manufactured and available for purchase [11]. At first used TI bar propagation elements (22 μm period), but has now been phased over to AC elements (16 μm period). Application in portable terminal (TI Model 765) was announced in early 1977 [1].
   - 256 Kb chips with the 16 μm period are in development and product announcement expected [12].
   - 1000 Kb chip with 8 μm period operated in the laboratory and described at 1977 Intermag Conference [13].

3) Rockwell International:
   - 100 Kb chips with 16μm period delivered for evaluation [14]. This chip has been incorporated in a recorder for a point-of-scale terminal (POS-8) with eight chips packaged

in a module [15]. It has also been packaged 16 to a module for a NASA flight recorder [16].

- 1000 Kb chip with an 8 μm period has been operated in the laboratory and described at the 1977 Intermag Conference [17].

4) Hitachi:

- 64 Kb chips using 20 μm period TI bar elements have been produced and used in a 2 Mb memory by NTT in portable switching systems [18].
- 256 Kb chips using a smaller period have been operated and built into a 16 Mb memory [19].

5) Fujitsu:

- 73 Kb chips using a 14 μm period have been packaged four to a module to provide a removeable cassette that is interchangeable with floppy disks and paper tapes for terminals [20].
- 294 Kb chips using newer elements have been described at the 1977 MMM Conference [21].

Other companies known to be working on similar chips include Univac, Plessey, Siemans, Philips, National Semiconductor, Fairchild and Intel.

There are at least two major government programs. One is with Texas Instruments contracted by Air Force Avionics Laboratory to demonstrate the feasibility of several configurations of airborne mass memories, e.g., 16 Mb disc/drum type systems and 100 Mb recorder type systems [22]. The other is with Rockwell International contracted by NASA for a 100 Mb

satellite recorder [23]. These same agencies are sponsoring other work intended to advance bubble technology and make possible higher levels of integration and lower costs.

All of this establishes a substantial basis for the technology at a particular circuit density (and corresponding cost/bit) and performance level. Let us now discuss the opportunities for further improving cost/performance.

III. THE PATH TO IMPROVED COST/PERFORMANCE

There appear to be ample opportunities to lower the cost/bit of bubbles through increased circuit density. At the same time it is hard to see ways to increase the speed of the devices and, in fact, we have to be careful to keep the speed from deteriorating as we increase the level of integration. Fortunately, increased payoff from bubble technology will flow much more from cost reduction than speed improvement. We will explain these points a little further.

The speed parameters that are important are operating frequency, data rate and access time to the specific data desired. The operating frequency determines the rate at which the data moves in the device, as the bubbles step from cell to cell. Operating frequencies are 0.1-1.0 MHz. The data rate is this operating frequency times the number of storage registers that are operated in parallel. Thus typical data rates are 0.1 to ~10 Mbs (megabits per second). The access time depends on the length of the storage loops and are in the range 1-10 ms. The operating frequency is

limited by two different considerations. First of all the frequency is limited to that which the bubbles can follow, i.e., propagate successfully from step to step. Secondly, increased frequency increases the drive power required, the driver cost, heat generation, etc. Therefore, to increase the frequency appreciably we must find ways to propagate the bubbles faster (>10 m/sec) and circumvent the limitations of the H_{xy} drive. Increased levels of integration, allowed by further reduction in bubble and pattern size, aggravate the speed problem in two ways. In the normal approach, which we have described, the magnitude of the drive field, H_{xy}, must increase as the bubbles become smaller (should we decrease coil volume or frequency to compensate?) and the length of the storage loops increase leading to an increased access time for the same frequency (if we can't increase frequency should we reduce the size of the chip or segment the storage on the chip?). Obviously, this subject involves an elaborate discussion. Suffice it to say that we can probably sustain operating speeds, that it is very difficult to find hope for substantially increased speeds and that factors that would help in this regard are:

a) device forms for which the drive field is reduced and/or does not increase as much as the bubble size becomes smaller,

b) chip organizations that yield shorter access times and/or larger data rates for a given operating frequency, and

c) conditions under which bubbles will move at speeds above 10 m/sec.

All of these are proper areas for research and some progress has been achieved on each already.

Fortunately, speed improvement is not required to expand the utility of magnetic bubble devices. For those applications where increased speed is necessary, there are semiconductor devices. But for the applications visualized for magnetic bubbles, the important characteristics are: non-volality, modularity, stop/wait/restart, ≤10 ms access time, ≥100 KHz, ≤$0.0002 cost/bit and once these are satisfied, the applications appear to expand exponentially with lower cost/bit. Thus our major emphasis is on cost/bit.

Obviously, the most direct way to substantially decrease cost/bit is to increase the capacity on the chip. For each factor of two reduction in the device period we quadruple the chip capacity and reduce the cost/bit by 75%, if we don't aggravate any of the other cost factors. In judging which of the approaches to reduced device period is best we must take into account its impact on chip processing cost, auxilliary circuit costs (e.g., drivers, detectors), heat generation and cooling requirements, etc.

There are several ways we could achieve smaller device periods:

a) changes in the permalloy bar device form that allows a smaller d/g (as already accomplished by a factor of two in replacing the TI elements by AC type elements),

b) refined lithographic processes that would allow smaller minimum feature (gap) size,

c) change in the method of representing data that would allow bubbles to interact and the device period to be less than 4d, and

d) elimination of the gap in the propagation pattern so that the bubble size can be less than the minimum feature, not greater than, as at present.

We will now discuss some of the efforts that are underway to accomplish these improvements.

1) There is continuous effort to reduce the d/g requirement by revising the design of the permalloy propagation element. A variety of different shapes have been made and tested. None so far published are significantly better than the asymmetric chevron. This element can be designed with d/g=2 to yield the widest operating margins or with d/g reduced to 1.5 or even a little smaller if we can be satisfied with narrower margins [10]. Other designs may be found that are even more tolerant of d/g but it can be argued that no design can be achieved where $d/g \leq 1$ if the bubble position is defined by a gap. Placing alternate propagation elements on two different layers separated by a SiO_2 layer allows the "gap" to be defined by the thickness of the SiO_2 layer and the horizontal separation of the elements can be reduced to zero. The minimum feature of the horizontal pattern, W_o, is then the width of the leg of the element, W, not the gap, g. However, it is also necessary that d>W. Usually $d \simeq 2W$ but experiments with this configuration showed that 1.5 μm bubbles could be propagated successfully with 1.0 μm legs [24]. Thus $d/W_o \simeq 1.5$ or greater and this approach does not appear to give

significant relief from the d/W_o requirement of the more usual single level propagation pattern.

2) Many organizations are trying to develop a lithographic capability that would produce much smaller minimum pattern features, W_o. Currently, W_o=1.0-2.0 μm with visible optics. Somewhat finer patterns can be achieved with a given lithographic process in bubble devices than in semiconductor devices because the bubble devices don't have the severe mask allignment requirement that semiconductor devices do. In fact, some bubble device designs do not require any precise allignment [25]. This means that X-ray [26] and deep UV [27] lithographies can be used to reduce W_o, as well as electron beams [28]. While all of these are being worked on it may be some time before they can be applied successfully in a manufacturing environment. However, in the laboratory, bubble devices with 0.3 μm gaps have been made and tested [25].

3) "Bubble-lattice" devices utilize completely populated, close-packed arrays of bubbles in order to permit bubble spacings ≤2d instead of the 4-5d of "isolated" bubble devices. In such arrays, each bubble feels the magnetic presence of its neighbors as a component of bias field so that the array is stable in an applied bias field, H_B, of lower magnitude than for the isolated bubble devices. Because each bubble position must be occupied, data cannot be represented by the presence and absence of bubbles in the bit positions, as in isolated bubble devices. Instead, data is represented by the bubble "wall-state." This requires

methods of generating and detecting these wall states as well as establishing the conditions under which the wall states themselves will be stable, without converting from one to the other with resulting errors in the data. These methods and conditions have been extensively investigated [29]. Since the bubbles interact, it is not necessary to drive every bubble - the driven bubbles will push the undriven bubbles. It is thus possible to translate a lattice of bubbles with an overlay of conductors [30] or permalloy elements [31] that is less dense than the bubble lattice. The stability of bubble states under conductor drive [32] and under permalloy drive elements [33] has also been investigated. Almost all of the work on such devices has been done by IBM and they have reported on a 1 Kb bubble lattice device using the conductor drive with all the required functions [34]. Such a device certainly has more complications than an isolated bubble device but its advantages can be:

a) increased circuit density by 4-16X for a given lithography W_o over even the best AC isolated bubble device. This is because $P \simeq 2d$ (vs 4d) and in addition d can be $\simeq W_o$ (vs $2W_o$) for drive patterns that are less dense than the lattice,

b) lower drive fields since the bubble interaction helps. In addition, the conductor drive can be used to completely eliminate the need for the rotating field coils in the module. In either case we can expect alleviation of the problems due to the high drive coil power of conventional bubble devices when density is increased, and

c) wider operating margins. The lattice is stable over a greater range of H_B than are isolated bubbles. It is conceivable that the other required functions can also be designed to give a wider overall operating margin than for isolated bubble devices.

Reference [31] reviews some of the complexities of lattice devices that must be provided for. Surely, there has been impressive progress made on such devices but whether the complexities can be managed and the advantages eventually realized will only be revealed by more research.

4) Significant progress has been made also on "gapless" devices such as the "contiguous disk" (CD). In this device a pattern similar to rows of slightly overlapping disks is ion-implanted in the surface of the bubble film. An impressed drive field then produces a "charged wall" magnetic structure in that surface extending out from the disks in the pattern. The charged walls move around the disk pattern as the drive field, H_{xy}, rotates and they will trap and carry bubbles with them. Thus these charged walls provide a different mechanism for positioning and propelling bubbles. This device is too complicated to describe here but ref. [35] provides a good background as well as a review of recent progess. In these devices the bubble size can be several times smaller than the minimum feature of the pattern so that this is another approach to higher density. If $d \simeq W_o/2$, instead of $d \simeq 2W_o$ as for AC devices, the density improvement is 16X while still using "isolated" bubbles spaced 4d apart. This

device does not then have the complications of the lattice devices but it does have some other complications associated with the charged wall phenomena. The chip fits directly into the AC chip environment with H_B and H_{xy} but the magnitude of H_{xy} required is less for charged wall propagation. Thus CD offers the desired relief on more than one of the AC constraints. More work on these devices and the process for making them is needed before they can displace AC devices in products.

5) Other on-going efforts are devoted to improvements in bubble materials: new compositions, multiple layer films, different techniques for depositing films, etc. This is such a multifaceted category that only a few items will be mentioned. Garnet compositions which will support bubbles of 0.4 μm diameter have been developed [36]. This is the apparent limit for garnets due to the requirement that $K \gtrsim 4\pi M_s^2$, where M_s is the saturation magnetization and K is the anisotropy energy that holds the magnetization perpendicular to the plane of the film, a necessary condition for bubbles. Smaller bubbles require larger M_s and larger M_s requires larger K. The mechanisms of K have been studied in garnets and the limit has apparently been reached in 111 oriented films for $d \simeq 0.4$ μm. There is some indication that larger values can be obtained in 100 films [37] and then there is the possibility of other compositions such as hexaferrites [38]. Work has also been done on amorphous films such as GdCo alloys which can have large K introduced by the sputter or vapor

deposition process [39]. Bubbles smaller than 0.4 μm will require substantial innovation in materials. Double layer films where the magnetic properties of the two layers are different are already in use and the virtues of three layer films are being explored. Alternation of the magnetic properties of the top surface of a bubble film by ion implantation is used to inhibit "hard" bubbles [40] and to fabricate "charged-wall" devices [41]. The different surface layer can also be obtained by depositing a film of different composition. The surface layer has also been shown to raise the maximum velocity of bubbles [42] and now the benefits to the dynamic properties of triple layer films is being investigated [43]. An in-plane field or a built-in in-plane anisotropy has also been shown to substantially raise the maximum bubble velocity [44]. The point of these diverse remarks is that the study of the physical mechanisms controlling bubble properties (especially the dynamics and anisotropy), the relation of material composition and deposition technique to these, and the exploration of new materials can lead to innovations that will extend the utility of bubbles.

IV. AREAS FOR RESEARCH

There has been significant progress in bubbles in recent years: physical phenomena, materials, devices and fabrication techniques. However, the application of bubbles has barely begun with devices having ~14 μm cells and operating at ~100 KHz. Enough work has been done already, as illustrated by the foregoing discussion, to show that additional

research can lead to substantially higher device densities and perhaps greater device speeds. This, in turn, should increase the utilization of bubble devices, bringing economic benefits.

The most obvious route to higher density is through the development of finer lithography. This is also true for semiconductor devices so the research needs in this area will be adequately covered elsewhere and need not be repeated here. It is worth repeating, however, that refinements in lithographic technique may find application to bubbles sooner than semiconductors because of the comparative simplicity of bubble devices.

Before new lithographic techniques are available significant increases in density may be produced by novel device forms that remove the constraints of the AC device forms, e.g., bubble lattice devices that allow bubbles to be closer together or contiguous disk devices that allow the bubble size to be smaller than the lithographic resolution or others that remain to be invented. Such device innovation can derive from research into new ways to propagate bubbles such as via charged walls or perhaps the newer phenomenon of "automotion" [45].

Hopefully, the relevance of the following areas for future fundamental research is now somewhat evident:

1) the mechanisms underlying both old and new methods of propagating bubbles, e.g., permalloy bars [46], charged walls [35], conductors [47] and automotion [45],

2) the dynamic properties of bubbles and ways to postpone the saturation of velocity, e.g., orthorhombic anisotropy [44], multiple layer films [43],

3) micromagnetic configurations: their static and dynamic properties, and especially how the configurations change with ambient conditions and motion. Included are isolated bubbles [48], bubble lattices [30], cross-ties [7], charged walls [35], surface domains [49], domain tips [8], exchange coupled bubbles in double layers [50] and others,

4) the equilibrium configuration, dynamic conversion and control of the variety of bubble states [29],

5) the mechanisms that induce and control anisotropy, especially how it can be controlled and even enhanced by the growth process [51][39] or composition variation [44],

6) other classes of materials which may offer better properties and/or extend the utility to smaller dimensions or higher speeds (crystalline materials, such as hexaferrites [38] or amorphous materials [52]), and

7) novel ways to manipulate domain structures, such as bubbles, without direct access to each bit position and especially where the minimum feature that needs to be defined lithographically is larger than the relevant domain structure.

V. CONCLUSION

The rate of discovery of new phenomena, understanding of fundamental mechanisms and ideas for improving the properties and extending the utility

of micromagnetic domain structures indicates that additional research will bear good fruit. Progress will come from a blend of applied and basic research and there are a variety of avenues to pursue.

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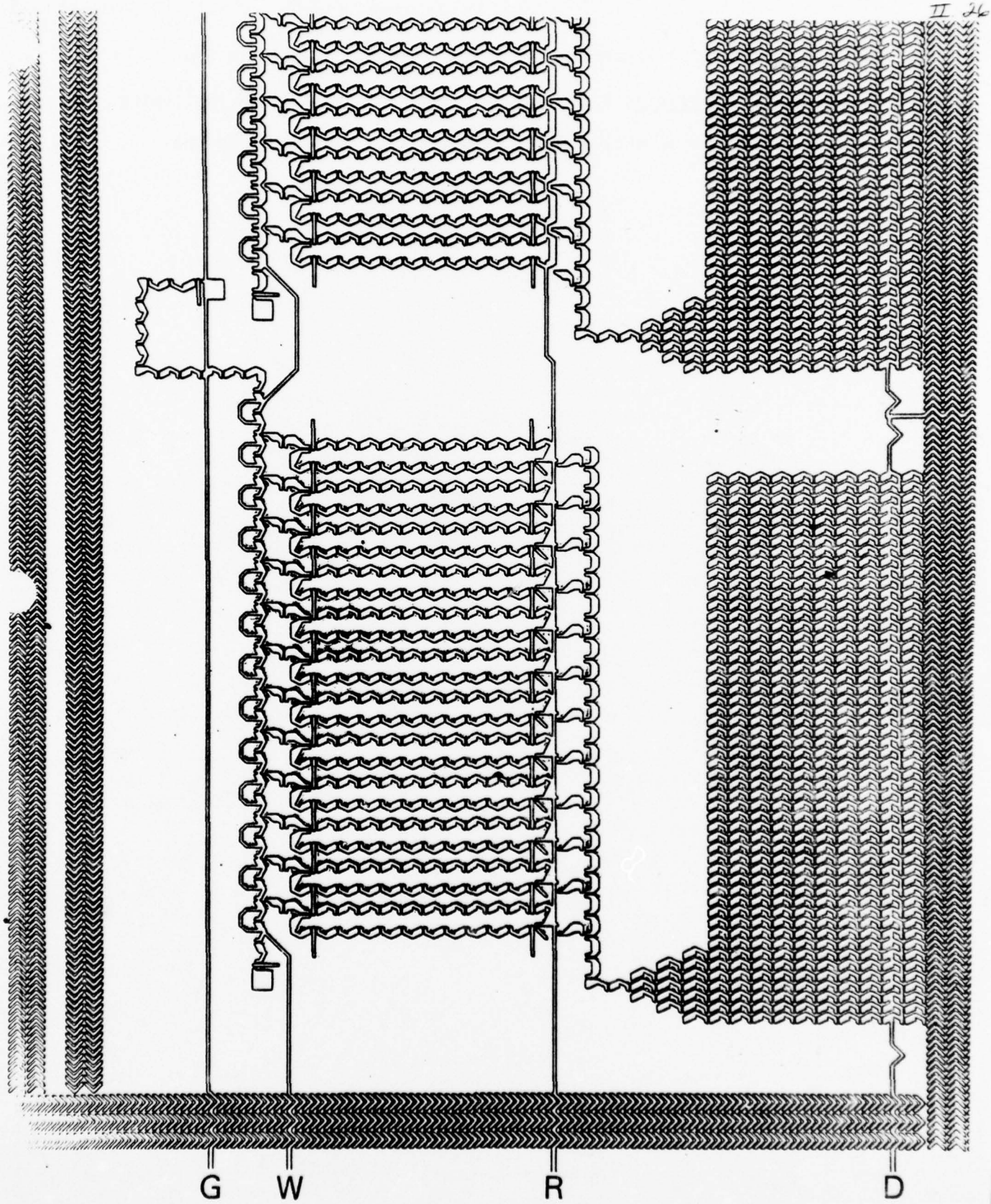

Fig. 1. Experimental Bubble Chip

Material Aspects of Integrated Optics at Very Small Dimensions

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Introduction

The basic ideas of integrated optics[1-11] were conceived in 1969-1972, at the time when the availability of low-loss optical fibers had already brought optical communication close to reality and there are definite needs to form compact optical systems. Research in integrated optics may be catalogued into two parts: one is to apply thin-film technology to the fabrication of miniature optical devices including lasers, modulators, switches, detectors, prisms, lenses, polarizers and directional couplers. The other is the integration of a large number of these devices on a single substrate. It is well known that a layer of thin dielectric film with a refractive index larger than its surroundings is a perfect optical waveguide. We may use these thin-film waveguides as the basic structures of all the optical devices which are then interconnected forming optical circuits. Typically, thin-film optical devices have one dimension ranging from hundreds of microns to a few millimeters and other two dimensions ranging from a fraction of a micron to several microns. The optical wavelength of interest is about 10^6 times smaller than ultra-high frequency radio waves and the devices should have an edge definition of about 500 Å in order to avoid excessive optical scattering. Integrated optics thus demands the finest microfabrication technology. There are a variety of materials[12] one can use to form integrated optical circuits. For passive devices such as prisms, lenses, polarizers, waveguides and grating filters and reflectors, the materials commonly used are sputtered glass, SiNO, organic polymers and amorphous Ta_2O_5, ZnO, ZnS, CdSe, CdS, Nb_2O_3 and TiO_2.[12] For modulators and switches, single-crystalline electro-optic,[13-15] acoustooptic and magnetooptic[16] films such as $LiNbO_3$, $LiTaO_3$, Bi_2O_3:TiO_2, III-V semiconductor compounds,[17,18] and rare earth

iron-garnets may be used. A great deal of the effort in the past has been concentrated to Al-Ga-As system[3,5] to form monolithic integrated optics.[11] Lately, however, the interest in the optical communication system at the wavelength near 1.3 microns has directed the attention to InP, and In-Ga-As-P related ternaries and quaternaries.[19-21] As devices are made smaller in sizes, the optical density in the devices has to increase and may reach MW/cm^2. Optical damage, optical losses, heat generated in the optical circuits, methods to form better epitaxial layers are a few of many material problems which demand most of our efforts in integrated optics.

Status of Current Work

Most of the inventions in integrated optics deal with methods which restructure bulk optical systems into thin-film forms. They include tapered-film[22] and grating couplers[23,24] thin-film prisms and lenses,[25,26] Bragg modulators[27] and directional-coupler switches,[28] distributed feedback[29] and Bragg-reflector lasers[30] and methods of forming interconnections between devices.[31] In the past seven years, research in integrated optics have involved, in U.S.A., about 150 scientists mainly from Bell Laboratories, IBM, Xerox Palo Alto, Rockwell International Science Center, RCA, Westinghouse, Hughes Research Laboratories, Lincoln Laboratory, United Technologies Research Center, Texas Instruments, University of California, Berkeley, Caltech, Cornell University, Carnegie-Mellon University, Washington University, University of Washington, Polytechnic Institute of New York, and Navy Research Laboratories in Washington D.C. and in San Diego. In spite of the scarcity of the research funds for exploring new science, the accomplishment of integrated optics has been spectacular: Research of propagating modes in waveguides has made single-mode kink-free laser-diodes[32] possible, waveguide modulators have a figure of merit of several orders of magnitude better than those in bulk forms,[33] diffused-$LiNbO_3$ directional-coupler switches have a crosstalk of about -32 dB,[34] and thin-film geodesic lenses are capable of focusing a light beam to the diffraction limit and of resolving light beams with an angular separation as small as 3.3 mrad.[35] More importantly, prism coupler and m-line spectroscopy enable one to determine refractive index and mode spectrum in waveguides better than 1 part in 10,000.[1,9,36] Gratings of period as small as 1200 Å have been fabricated[37] and their uses for band-rejection filters,[38] reflectors and distributed feedback and Bragg reflector lasers[39,40] have been demonstrated.

As of today, simple integrated optical circuits can be readily developed in $LiNbO_3$, on silicon substrates, or in III-V alloy-semiconductor compounds. A multipurpose spectrum analyzer involving a geodesic lens, an acoustooptic deflector and hundreds

of silicon detectors is being pursued at Rockwell International Science Center, Air Force Avionics Laboratory and Battelle Columbus Laboratories. A $LiNbO_3$ circuit containing 4 x 4 directional-coupler switches has been built at Bell Laboratories.[41] GaAs circuits containing lasers and modulators have been constructed at Bell Laboratories,[42] University of California, Berkeley,[43] and Tokyo Institute of Technology.[44] A circuit composed of six GaAs laser diodes and six waveguides for wavelength multiplexing is developed by Hitachi Central Research Laboratory.[45] In general, because of more ambitious policy and more liberal funding by the Japanese government toward technological advancement, integrated optics in Japan is just as good as, or even better than that of the United States, in spite of the fact that we have contributed most of the original research!

Specific Scientific and Technology Needs

Although simple integrated optical circuits have been demonstrated with existing technology, to produce them reliably and economically faces a multitude of difficult material and technology problems. In general, the areas needing extensive support may be summarized below.

(1) To form monolithic integrated optical circuits in the Al-Ga-As system, the present epitaxial layers have a loss[46] from 1 to 10 cm^{-1} which should be reduced by about a factor of 10 in order to satisfy the system requirement.

(2) Techniques of fabricating optical gratings either on deposited films or on epitaxially grown layers have to be improved. The present optical circuits containing grating filters, distributed feedback lasers, and Bragg-reflector lasers have poor quality and are generally not reliable.

(3) Research in orientation-dependent epitaxial growth[48] and etching[49] has to be carried out to form atomically flat facets for reflecting or deflecting light in optical circuits. Such techniques are also needed for forming blazed gratings structures in waveguides.

(4) It is generally recognized that to achieve long lifetimes, semiconductor lasers have to be grown on dislocation-free substrates. Methods to grow dislocation-free GaAs or InP substrates and the kinetics involved should be investigated.

(5) Typical semiconductor laser-diodes have sizes hundreds of microns long and 1 to 10 microns wide. They produce 1 to 10 mW of light and are excellent light sources. For signal processing and for performing logic operation in optical circuits, however, a large number of the lasers are required. These lasers must have much smaller sizes in order to improve packing density and need only to produce a fraction of microwatt of light to cut total power consumption. Such microlasers have yet to be developed.

(6) Switches with a speed in the subnanosecond range may be formed in Ti-diffused $LiNbO_3$ waveguides. However, $LiNbO_3$ is susceptible to optical damage. Moreover, impurity ions in the diffused waveguides may move under an intense switching electric field and thus short-circuits the field needed for switching. Research for better electrooptical and acousto-optical materials is in order.

(7) It is likely that optical circuits will be formed on $LiNbO_3$, GaAs, InP, or Si substrates. Fortunately GaAs, InP and Si are also excellent material for high speed electronics. Methods of fabrication so that optical circuits and electronics may be formed on a same substrate have yet to be developed.

(8) For a single optical fiber to carry two-way communication, the incoming and outgoing signals have to be separated and processed in different optical circuits. The device which separates the incoming and outgoing signals is a circulator or an isolator which has to be formed of magnetooptical materials such as rare earth Garnets. The present magnetooptical material has a Faraday rotation constant of 200°/cm. Materials of Faraday constant more than 1000°/cm could be developed by adding Bi or Pr into the composition of the Garnets.

One realizes that the technology needed in integrated optics is also needed in other industries. Therefore, carried with the research of integrated optics are a more refined semi-conductor industry, better methods for epitaxy and for film-deposition, and a better understanding in solid state physics regarding interfaces and dislocations.

Possible Impacts of Research

With commercially available optical fibers, lasers and detectors, it is already possible to design a communication system, 50 MHz in bandwidth and 7 to 8 kilometers in distance, for a cost comparable to that of a similar system using coaxial cables. There is no doubt in the mind of the telecommunication industry that optical fiber systems will grow for short-haul services. For long-distance telecommunication, although intensive research has reduced losses in single-mode optical fibers comparable to those of the multi-mode fibers, the commercial deployment of such long-distance single-mode systems will not be forthcoming until about the middle of the 1980's.

Integrated optical circuits serve best for multiplexing of optical signals. Such applications must, however, wait for the maturity of the optical communication. Even then, the optical communication systems must be standardized before integrated optical circuits can be designed. More immediate applications of integrated optics

are in military communication services, signal processing for warfare operations, local communication and signal-sensing in ships and airplanes. There,light weight and small volume of the fiber system are often dominant factors for the choice. The optical-fiber system has also a unique advantage as being immune to the electromagnetic interference. Optical systems have also been found to be economical for cable televisions. Japan has already used optical systems for data collection and signal processing in large electric power plants where stray magnetic fields produced by the electric cables are found to be harmful to the electronic devices. There are also increasing uses of optical systems in nuclear power plants and high-energy research facilities. Optical systems are also invaluable as a data link between two large computers or two large switching stations in order to avoid mutual electronic interferences or a common ground-current loop. For each of the above applications, there is a need of integrated optical circuits.

The real impact of integrated optics will come when high speed electronics is incorporated into the optical circuits. In fact, a chip containing a bank of the laser-diodes including the driving electronic circuits can be readily developed with the existing technology. Such chips may be used for the transmitters in the optical communication systems. They may also be designed for printing, for survey, and for controls of various industrious processes. Optical beams have the advantages that they may be pulsed in rapid sequences, can scan over wide angles and may be transmitted over any transparent space with a minimum of interference. If visible semiconductor lasers can be developed into practice, a chip containing the visible lasers with their associated electronics has many medical applications. Work to form electronic and optical devices on a same GaAs substrate has already begun.[49,50]

The development of the first practical medium-scale integrated optical circuit can be very costly. However, once the technology is established, optical circuits should not be more expansive than IC chips used in wristwatches or pocket calculators. Heavy investment from the industries is not likely since the present market for the optical circuits does not justify their initial cost. On the other hand, without actively pursuing advanced technologies such as those associated with the integrated optics, we will quickly lose the leadership in this general field of opto-electronics.

University Opportunities

Integrated optics does not compete with the present microelectronics, but rather complements it. In fact, integrated circuits containing both optical and electronic devices opens up new opportunities for

the electronics industry. To develop such circuits to their full potential, research and development should not be confined only to the fabrication of thin-film devices and circuits, but they should be directed to the exploration for new ideas of circuit designs as well as novel device-physics which combines optics to electronics. In that sense, there are plenty of the opportunities for the universities to participate in the research and development, since such studies carry as much as academic value as industrial. In particular, integrated optics is one of the few fields where fundamental science and discoveries can be made.

Microfabrication and epitaxial technologies are the foundations of the modern electronics. Both microelectronics and integrated optics demand the excellence of these technologies. Indeed, the research of integrated electronic circuits and integrated optical circuits should be carried out side-by-side. In particular, InP and GaAs used for the fabrication of the lasers are also the materials for high speed electronics. For micro-fabrication, one requires: electron-beam exposure system (EBES) for computer controlled mask fabrication and electron-beam writing, electron-resist and photo-resist facilities, a mask aligner for both contact and project printing, photo and x-ray lithography, scanning electron microscope for viewing small structures, ion-beam etch and dry plasma etch facilities, and equipments for depositing SiO_2 and Si_3N_4. The equipment required for laser research involves scanning electron microscope coupled to x-ray energy dispersive and wavelength analysis, Auger electron spectrometer with depth profiling, SIMS, mass spectrometer, diffusion furnaces, evaporation and sputtering stations, and liquid-phase and vapor-phase epitaxial growth facilities. Unfortunately, even the best universities in the United States are not equipped with all these facilities. On the other hand, both Osaka University and Tokyo Institute of Technology in Japan have the best of these equipments.

One microfabrication center is being set up in Cornell University by NSF. We believe other similar centers should be, perhaps, in Stanford University and in University of Illinois where a large pool of human resources and technical know-how are readily available. It is believed that these centers will have far-reaching consequences to maintain the momentum of our science and technology in general, and the competitive position of our electronics industry in particular.

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MATERIALS PROBLEMS IN IMPLANTABLE MEDICAL ELECTRONIC DEVICES

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TABLE OF CONTENTS

INTRODUCTION

The focus of this article can be quickly set by examination of Fig. 1 which shows a photomicrograph of human brain cells (from the motor cortex) superimposed on a photomicrograph, to the same scale, of a commercially available (Intel) four kilobit random access memory. Note that the bit density of the semiconductor memory is two orders of magnitude higher than that of the human brain. With the further shrinkage of semiconductor structures now in progress the dimensional advantage of electronic intelligence over natural nervous tissue can only increase. It is now possible to contemplate the replacement of defective nervous tissue (e.g., inoperative sensory organs such as the eye or ear, stroke-damaged brain tissue) by synthetic intelligence in approximately the same volume and at approximately the same energy cost per transaction. The realization of such remarkable substitutions is now limited primarily by materials problems, in the long-term insulation and protection from attack by body fluids of the integrated circuits and by materials problems at the neural-electronic interface. This review will focus primarily on these problems.

The continuing shrinkage in size and cost of computational power affects medical electronics profoundly in many other ways, in all cases where computational power can be brought to bear on diagnosis or treatment. Cases in point would be computer-aided x-ray tomography and the various applications of microprocessors to "smart" medical instruments. This article will not deal with such cases, since they are covered elsewhere in this series of reports where the main stream of computer-oriented programs are considered. This article will also not deal with the numerous materials problems in bioengineering associated with bone, tooth, tendon, etc. implants, as not being relevant to the main theme of these reports, materials problems in microstructure fabrication.

STATUS OF CURRENT WORK

The focus of this report, as indicated above, is the development of materials and techniques for the fabrication, passivation, and protection of implantable active microelectronic circuits, active prosthetic or monitoring electronic devices. This section of the report, describing current work in industry, academia, and government, will delineate the exceedingly limited spectrum of active groups.

The largest and most active class of research and development groups in this area exist in the cardiac pacemaker companies. The cardiac pacemaker is, at present, the only widely accepted commercially important neural prosthesis. It is a relatively simple device functionally. Its output is a single pulse to a single electrode at about a one Hertz rate. Its logical function centers on the need to sense the presence of natural heartbeat signals and to suspend stimulation output when satisfactory natural signals are present. Circuits of very modest complexity can achieve these functions, without taxing even the current state of the art

in integrated circuits, in adequately small volume and at adequately small power demand. The pacemakers are relevant to this discussion because they have had to confront seriously for the first time long-term protection of electronic circuits in a biologic environment[1,2]. Early devices were constructed of discrete components potted in an epoxy resin chosen for biocompatibility and minimum permeability to body fluids; Hysol A, manufactured by the Dexter Corp., was the common choice. The lifetime of such systems against ultimate penetration by body fluids was on the order of two years, similar to the life of the batteries incorporated into such systems. Current devices place their active circuits, and batteries when possible, into a hermetically sealed can typically titanium, achieving excellent protection, but at a volume increase factor on the order of 10^5 as compared to the volume of active circuitry. Further, external to the hermetic package is only one massive electrode and its fairly massive lead elements. Since the dimensional constraints are relatively relaxed, insulation of these elements is usually achieved using thick plastic (silastic or epoxy) jacketing. The pacemaker companies have not been forced to confront the problem of insulating and protecting an array of closely spaced elements, as we will see must be confronted by more complex neural prostheses. Some pacemaker companies, however, notably VITATRON in the Netherlands, have made significant progress in developing viable long-term implantable insulation schemes other than a plastic wrapping of the sensitive elements; they have in particular been developing anodic oxidized layers as a class of tightly bonded insulation coatings, and have been particularly successful with anodized tantalum. This work is probably seminal for the micro-insulation needed for implantable microcircuitry.

A second class of research and development groups active in solving problems inherent in implantable electronics are those engaged in biotelemetry[3]. Typically biotelemetry units monitor a few (often one) physiologic parameters (body temperature or blood flow or blood pressure, for instance) and transmit to an external receiver this information. Again for this set of applications, the standard current solutions are hermetically sealed containers for as much of the circuitry as possible, with plastic coating for the elements, such as sensors or antennae, which must be external to the hermetic container. The applicability of these techniques to true microminiaturization is small.

Recently an important class of applications has been emerging which makes technical demands not satisfiable by current materials technology. These applications mostly involve multipoint contact with the nervous system[4]. This multipoint contact is required either for multielectrode stimulation of the nervous system, such as is required for sensory (ear, eye) and muscular (lung, bladder, leg) prostheses, or for multipoint recording of the nervous system such as is desired for research in many areas of neurophysiology (learning, brain disfunction, multiple sclerosis, auditory and visual physiology, etc). For these applications a multiplicity of contact elements (typically platinum microelectrodes for survival against electrolysis) are required, with spacings on the order of the size of the basic neural elements, microns to tens of microns. There is

no sensible way to make such arrays other than with the photolithographic techniques characteristic of the semiconductor industry. The materials currently used in the semiconductor industry are, however, not adequate or appropriate to the implantable application. The metals typically used, gold and aluminum, are in the one case not optimum and in the other not acceptable (toxic). The commonest current insulation material, SiO_2, does not survive protracted saline exposure. A second emerging insulation and passivation material, silicon nitride, Si_3N_4, shows promise as an impermeable insulation but has not been extensively tested. Also a possibility, but with even less documentation, is silicon carbide, SiC. No materials have been evolved for conductors or insulation in situations where a flexible structure is required. If the potential of artificial intelligence for neural prostheses and neural characterization is to be fully realized, truly multiple interface points - microelectrodes - will be necessary, perhaps hundreds or thousands of contact points, not possible without multiplexing or interspersing of passive interface elements with active logic elements. One is therefore led to the necessity of passivating active elements against multiyear saline immersion, utilizing protective coatings whose dimensions must be on the order of microns or less, compatible with the scale of the semiconductor logic elements or the neurons they excite or record. Though the value and potential of such multi-electrode stimulation and recording arrays has been appreciated for some years, especially by neurophysiologists and neurosurgeons, very little progress has been made on the generation of the appropriate hardware, and very little work is, in fact, in progress. The commercial possibilities of such devices are sufficiently modest that the semiconductor industry, wherein resides most of the appropriate talent, has not been motivated to pursue the key problems. Funding to support such materials research in universities has been almost totally lacking because its medical orientation causes all Federal agencies except the NIH to regard the NIH as the appropriate support agency, and the NIH is strongly disinclined to support the development of technology of medical potential unless tied to a specific disease or disability. Recently the NIH has commenced support of the development of such materials and technology pursuant to the development of an "artificial ear," a cochlear prosthesis which works by direct electrical stimulation of the auditory nerve[5]. Such work, at Stanford University, is in its early stages but shows promise. The NIH also has had some in-house work on microminiature electrode arrays, also pursuant to neurophysiology, but with very limited resources committed to the project. The NIH has also been supporting, in recent work, small but important projects aimed at understanding the electrolysis of metals in electrolytes such as body fluids.

In summary, the current state of relevant research is that a number of pacemaker companies are working on related but mostly not directly applicable problems, there is one substantive University project directly aimed at such problems, and a small amount of work in-house at the NIH, but no substantive activity by the effervescent semiconductor industry whose experience is most relevant to the problems involved, for the good and continuing reason the overt commercial markets for the resulting devices is small.

SPECIFIC SCIENTIFIC AND TECHNOLOGICAL NEEDS

The scientific and technological needs for high-intelligence-density implantable electronics are several. The leading need is for the development of insulation materials such that insulation a few microns, or perhaps even a few hundred Angstroms thick, will provide long-term insulation in a saline fluid environment. The structures to be protected are of similar dimensions to the insulation thickness, so the separation and protection of closely spaced elements is required. Since the performance of semiconductor devices is determined by the density and distribution of dopant ions, the protective layers must resist penetration by unwanted dopant ions, such as sodium.

It is exceedingly unlikely that the required technology will be achieved within the conceptual framework of present-day insulation technology, which basically relies on wrapping the active elements tightly with plastic or some other insulating material which is chemically and physically unrelated to the element to be protected. For all such insulation techniques, saline penetration between the insulation and the protected element is inevitable, and if penetration on the order of microns is damaging, the useful lifetime of the protection is short. The successful technology will be one in which the insulation layer is chemically bonded to the substructure. A first step in this direction has been made in certain passive (electrode lead and array) systems using tantalum as a conductor and anodically formed tantalum oxide as an insulation. Such a system shows promise for a number of applications. Shortcomings of the tantalum-tantalum pentoxide system are the unipolar nature of the insulation (the oxide reduces for the "wrong" sign of voltage) the brittle nature of the insulation, and the inapplicability of this particular system to active (i.e. silicon) electronic components. Research is required to define the parameters which make a material, particularly a thin film of material whose volume is essentially all surface volume, impermeable to a number of biologically relevant ions and molecules.

Implantable systems must be biocompatible, which usually translates into being fabricated out of materials which are chemically very inert. Yet the lithographic fabrication characteristic of integrated circuits in general and microstructure circuits in particular invariably involve multilayer structures where successive layers must bond physically and chemically to one another. Research is needed in the science of adhesion as applied to metal, semiconductor and insulating (oxide or nitride) interfaces. How does one form multilayer structures out of chemically inert (biocompatible) materials without having delamination, and failure, a major problem? A good deal of surface physics and surface chemistry must be explored before we can resolve the essential paradox of constructing active electronic microstructures which will not delaminate out of biocompatible, relatively inert, materials.

A second class of problems arising in implantable active electronic devices arises from the phenomenon of electrolysis, the dissolution of metals placed in an electrolytic solution, especially in the presence of

electrical currents. Though the electrochemistry of metal-electrolyte solutions is the subject of an extensive literature, so many of the results are compound-specific or configuration-specific that it is hard to draw generally useful and extrapolatable conclusions, except in broadest terms. Studies specific to the metals most likely to be used in implantable devices, and in situations resembling the complex environment of body fluids, need implementation.

In summary some science and technology areas needing exploration are

(1) The surface chemistry and physics of adhesion especially as applied to biocompatible materials such as may be useful in implantable devices.

(2) The physics of impermeability, especially of oxide, nitride,etc. layers.

(3) The physics and technology of various metal-metal oxide or metal-metal nitride or metal-unknown layers as "permanent" passivation layers. This study should include investigation of the technology of deposition and patterning and of practical feasibility of such passivation schemes.

(4) Studies of plastic-metal interfaces to generate biocompatible flexible systems operable in a hostile electrolytic environment.

(5) A study of electrolysis of metals in a biologic environment, with attention also to the toxicity of by-products.

POSSIBLE IMPACTS OF THE RESEARCH

The direct impact of the successful development of materials making possible long-term electronic implants of high intelligence density is upon the medical world. Successful work would make possible neural prosthesis for a variety of motor and sensory handicaps. Successful work would make possible sophisticated investigations of the operations of the neural system, especially the brain, of how it functions, and of how it is affected in such diseases as cerebral palsy. A secondary area of impact is broader and harder to define - it is the general area of passivation of semiconductor devices. Certainly the techniques which might be developed to ensure circuit survival in the hostile environment of the body, with its fluids, salts, enzymes, and invading fibrosis growths, are extensible to give greater reliability and lifetime to circuits operating in less hostile, yet still threatening environments, such as hot and humid climates. Finally, the information gained in studying the physics and chemistry of surfaces, and of the bonding mechanism of one class of materials to another, is of more general applicability than to microstructure fabrication alone, though the exact ultimate utilization of such information is difficult to identify.

To give specific examples of impact in the areas outlined above: An auditory prosthesis for the profoundly deaf which operates by direct electrical stimulation of the auditory nerve to replace the function of

a defective inner ear (cochlea) is under development in several laboratories throughout the world. It is necessary for such a prosthesis to excite differentially a number of small subsets of the nerve bundle comprising the auditory nerve. A major technological obstacle to this artificial ear is the difficulty of fabricating microelectrode arrays small enough and complex enough to achieve this stimulation, yet capable of surviving in the biological environment. Similarly, electrical stimulation of the optical nerve or the optical cortex produces bright spots in the visual field, from which a representation of the visible world can, in principle, be constructed.One obstacle to this project is, again, suitable electrode arrays and electronics. Electronic bladder control for paraplegics and others with lower body neural disfunction is an important area of neural prostheses also under development. Electronic bladder control is important not only for the obvious convenience and social advantages but is life-prolonging because it eliminates the infection risk of an indwelling catheter, now the only viable solution to bladder dysfunction. Electronic stimulation of leg muscles for gate improvement in hemiplegics is making headway, but again is obstructed by electronic technological obstacles. The operation of prosthetic limbs through the neural signals still naturally available to control the missing limb is only crudely possible at present, but could, in principle, be achieved. The list of neural prosthetic devices which might be conceived, given implementation possibilities, is mind-boggling.

In addition to playing dramatic roles of "bionic man" variety, implantable intelligence with complex high-density sensing electrodes could play a valuable role in extending our knowledge of how the nervous system, especially the brain, works. The applications extend from understanding the mechanisms of learning and memory, through the role of various chemicals on brain functions (e.g. chemical control of schizophrenia), to understanding the architecture in space, and the distribution in space and time, of the signals which characterize and govern our capabilities and behavior. The author has a thick bundle of letters from neurophysiologists of all stripe, inquiring about the availability of microelectrode arrays for studying brain function from a variety of points of view.

Proceeding to the second impact area, the passivation of semiconductor circuits has been an ongoing problem since the earliest days of the semiconductor business, since performance characteristics can be severely damaged by relatively small numbers of impurity ions reaching and infiltrating the active areas. Surfaces are currently passivated with insulating layers such as SiO_2 or Si_3N_4, and sensitive elements further encapsulated in epoxy or in hermetically sealed containers. Even so, failure due to environmental factors is still common, and a serious cause of effort and concern in the semiconductor industry. The informational gain from material studies directed in a more searching way at this problem will certainly impact the semiconductor world generally. Such impact has, in fact, already occurred through the needs of the pacemaker industry. The careful life-test and failure-mode analysis of pacemakers has produced results challenging the military-specification procedures for hermetically sealed devices,and has resulted in a major reexamination

and reevaluation of both the materials used and the procedures allowed in the high reliability circuits of our military and space programs. Such impact will undoubtedly continue if more sophisticated and penetrating results or material parameters can be generated.

Finally one is left with the unpredictable nature of the impact of scientific advances which allows major impacts to occur in areas not foreseen As a stand-alone argument for a scientific research project, such justification is inadequate. It should not be overlooked, however, as a potential benefit of a scientific program, especially one focussed so closely on real materials obstacles in a real applications environment.

UNIVERSITY AND INDUSTRY OPPORTUNITIES

The applications area of first order relevance of this class of programs is of insufficient commercial promise to attract the attention of the industrial laboratories whose facilities and manpower make them optimal for attacking the problems involved. The commercial potential of neural prosthesis or neurophysiological investigative tools is insignificant compared to that of microprocessors or central processing units or generalized memory. The role of the industrial laboratories in attacking the materials problems of implantable electronics is destined, therefore, to remain a supportive and peripheral one, not a central one. The key work must and should be done in university laboratories, and represents a major opportunity area for university laboratories, especially in those situations where a strong materials science group, a strong electronics group (with integrated circuit process capabilities) and an interested medical school exist together. The overwhelming depressant on work of this kind has been the lack of governmental funding available. The medical flavor of the problems moves them - or in the past has strongly tended to move them - outside the charter interest area of all Federal agencies other than the NIH. The NIH, on the other hand, is not set up organizationally or philosophically to support technology of relevance to medical problems until and unless that technology has reached the stage of applicability where its impact on a specific disease or disability can be demonstrated. The review procedures of the NIH involve personnel who are generally non-technical and materials and engineering grants proposals have small chance of support. If the material and technological studies described in this report are to be implemented, it is vital that funds be designated, and an agency mission assigned, to bring about the implementation. It is also clear that these funds should be directed at university laboratories, though a collaborative effort between a university and industrial laboratory would have real virtue if the industrial participation were genuine. The area of materials technology for implantable electronics represents at present a genuine, largely unrealized, scientific opportunity, in which some attention should be focussed.

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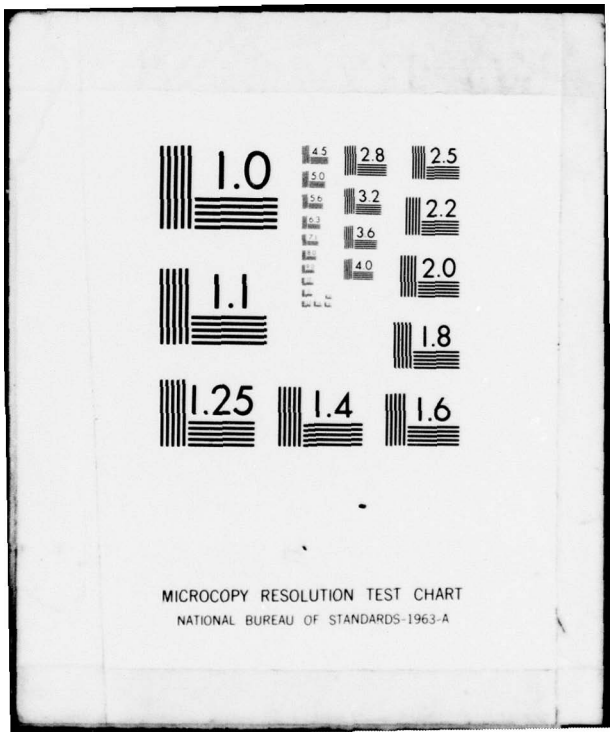
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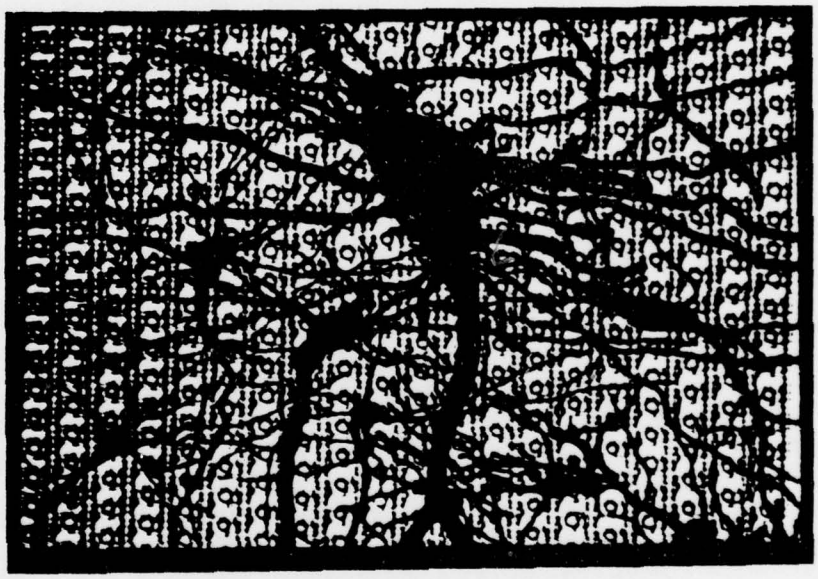

Fig. 1 Photomicrograph of stained neurons from motor cortex, superimposed on photomicrograph (to same scale) of Intel 4 Kilobit random access memory.

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MATERIALS FOR DISPLAYS

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MATERIALS FOR DISPLAYS

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1. Status of Current Work

1.1 Cathode Ray Tubes (CRT's)

The present state of CRT's as display devices is quite advanced, as befits a class of devices with over 70 years of development. There is a wide range of types and performance characteristics available, and in the materials area new phosphors continue to be developed and registered, thus ensuring at least some improvements on a constant basis. Higher efficiencies and luminances are some of the improvements that have come about, largely in response to the insatiable appetite of entertainment television, but also most recently as a result of the needs of information display systems. In addition, new gun designs, such as the Laminarflo, and improved cathode materials have permitted reductions of spot size at cathode loadings approaching the theoretical limits. Further development may bring performance closer to this limit, but present performance, at least where monochromatic CRT's are concerned, suffices for the large majority of applications.

In spite of a plethora of types, color CRT's are still largely restricted to two structures, those represented by the shadow mask and the Trinitron. The in-line-gun shadow mask is in most respects equivalent in performance to the Trinitron, and either one may be used effectively, particularly where standard 525 line television is involved. However, when higher resolution is required, as is the case in many non-entertainment applications found in industry, government and military, high resolution versions are needed, and have been developed to the point of commercial availability with twice the resolution of the standard types, but at many times twice the price. The limited market for these high resolution types will keep the price high unless simpler manufacturing processes are developed.

Other approaches to high resolution color CRT's have tended to concentrate on the beam penetration technique, with moderate success. Tubes with two phosphors are commercially available and have been incorporated in several monitors. However, the full potential of this approach has not been realized since two phosphors offer only a limited number of discrete colors and the high switching voltages needed to penetrate the selected phosphor result in severe operating limitations.

cont'd.

1.1 Cathode Ray Tubes (CRT's) cont'd.

Little work is being done to develop thin film phosphor deposition techniques so that lower switching voltages may be used. This technique offers great promise for attaining very high performance full color displays, but the market impetus appears to be lacking, although the need exists and is growing. A three gun approach has been proposed as another solution to the high voltage switching problem, but no significant work has been done.

Another approach to color which has been resurrected is the scanning beam technique that has achieved demonstrable success, at least in relation to what may be done with the standard shadow mask type. Its advantages are moot for entertainment television, but it could be a candidate for high resolution color since it is a single beam tube without a mask.

The third area of importance is the direct view storage tube, primarily represented by the devices produced by Tektronic. This type of CRT has created a revolution in computer graphics, causing costs to be reduced drastically so that the applications of computer graphics have been extended to many areas that previously' found it too expensive to be useful. Although continued development of the CRT has overcome some of the early deficiencies, such as small size and low luminance and contrast ratio, and the initial impetus for its invention, which was to eliminate the need for large, expensive memories, has not proved to be valid due to the rapid decline in memory costs, the concept has remained viable and further improvements should allow it to maintain its position as a balancing factor in the cost of computer graphics systems. However, the essentially sole source condition needs to be changed to permit more widespread use.

Another approach to storage systems is the electrical in-electrical out type coupled to standard CRT monitors. This technique has been rather restricted in its use and warrants some further consideration since it is a well-developed technology and can be improved with relatively little effort.

A last type worthy of consideration is the flat matrix CRT, using matrix addressing rather than beam deflection techniques. This has been the object of considerable development effort, and has resulted in a viable device for limited density displays. The prime area for improvement lies in the large area cathode required for this type of CRT. The flat matrix CRT is a possible alternative for the non-CRT flat panel matrix devices discussed next, especially when it is desireable to obtain the high luminances of CRT's combined with a flat structure and the simplified matrix addressing possible with this structure. Cost and manufacturing complexity

cont'd.

1.1. Cathode Ray Tubes (CRT's) cont'd.

remain serious deterrents to large scale acceptance of this device.

In summary, standard monochrome CRT's are in a very advanced state of development, but color CRT's for special high density applications are in need of further effort. Storage CRT's have many useful features and should be further developed. Some special gun designs also need attention to achieve best performance and the flat matrix CRT is a promising design.

1.2. Flat Panel Matrix

Turning from the various CRT display devices to the flat panel matrix devices requiring no election beam, there are three major and a number of minor technologies that have been investigated and brought to various levels of development. The three major technologies, so termed because they have achieved the highest levels of development, are those represented by the light emitting diodes (LED's), gas discharge (Plasma), and liquid crystal (LC) display devices. All of these have resulted in some forms of commercially available units, and development continues to satisfy the needs of the various applications that have found these devices practical. LED's are largely restricted to small assemblies of numerics and alphanumerics, and usage as simple indicators is probably the most extensive single application of this technology. Improvements in luminous efficiencies and peak luminance capability are the prime areas for further development, although applications for large monolithic arrays remain to be satisfied. Here material cost and high power consumption are important limitations.

One very important area for development that impacts on all forms of matrix displays is the fabrication of the electrode patterns required for driving the data points. Present technology can readily achieve about 25 lines/cm, and up to 40 lines/cm without undue effort. There are also some examples of as high as 200 lines/cm, but these are laboratory results, and have been done on small panels of about 3 cm on a side. The technology is available for producing high resolution panels of larger size, but has not been developed to the point of commercial feasibility.

DC gas discharge devices have continued to improve, based on a long background of experience, and have found a market where medium information density is adequate and moderate levels of luminance are sufficient. Attempts to include a multicolor capability and adapt them to television inputs remain as laboratory efforts, although the results to date offer

cont'd.

1.2. Flat Panel Matrix, cont'd.

some promise of ultimate success. The commercial market is large enough to insure continued development of at least the monochromatic versions without additional incentives, but the situation is quite different for the color types. Also, high resolution devices are subject to the electrode patterning difficulties previously mentioned.

AC gas discharge devices are the most fully developed matrix devices, with capabilities close to that of CRT's for both alphanumeric and full graphics displays. However, limitations in size and relatively high cost have limited their acceptance for large scale applications. The capillary tube structure seems to allow the size limitation to be overcome, but it is much less advanced than the more common flat plate structure. Color versions are still in the laboratory stage, and increase the electrode patterning problems since the three color dots required for each data point triple the number of electrodes needed in at least one dimension. The present situation is that while much development work has been expended on ac gas discharge types, in the hope of ultimate success in replacing the CRT for many applications, success has been limited and further work is being curtailed.

Liquid crystal displays have exhibited a continuing growth, but primarily for applications requiring small assemblies of numerics where low power is important, such as watches, calculators and other battery operated instruments. Improved materials and fabrication techniques have resulted in devices that appear to be satisfactory for at least these applications. Improvements in switching time, temperature range, and angle of view should expand this usage, and all are being investigated. However, larger panels with data densities competitive with CRTs or even gas discharge panels are much less advanced. There are several developments that begin to approach this goal, using either special materials or unique addressing techniques. In particular, two techniques that combine large scale integration of solid state switches and thin film transistors with more or less standard liquid crystal material and panel structure have achieved considerable success in producing panels with true high density data capabilities and compatibility with television inputs, at least in black and white. One or more of these techniques may produce the successful flat panel display of the future.

Finally, among the most promising techniques are the ac and dc thin film electroluminescent (EL) panels that have shown considerable promise, in particular the ac thin film devices that exhibit high luminance and long operating life, both of which features have been lacking in the powder EL panels developed in the past. The new thin film technologies are strong contenders for effective high data density flat panel displays that may be used for full graphic and television displays, albeit with the same problem in the electrode patterning that is characteristic of all these types of matrix displays. True commercial availability is still not here, but given the rapid pace of development may not be far in the future, at least in the monochromatic versions, although color remains a problem.

cont'd.

1.2. Flat Panel Matrix, cont'd.

Among the minor technologies we may include ferroelectrics (FE), electrochromics (EC), and electrophoretics (EP) techniques. FE displays offer characteristics that appear ideal for flat panel matrix displays, being solid state with fast switching times and potentially long operating lifetime. Inherent memory and low material cost are the other advantages of this technology, as well as low power and moderate drive voltages. Little has been done with this approach because of fabrication problems, especially in producing the very thin discs that are necessary for best performance, and because the demand remains low.

EC displays have been fabricated using both the solid state and liquid forms, although the solid state is the more advanced of the two. They have a number of interesting features similar to those of the FE devices, having inherent memory and being solid state in one of the forms. To these can be added the very low voltage and sustaining power requirements, although the slow switching speed and difficulty in multiplexing have militated against acceptance of this approach for the watch application to which it appears most suited. Considerable development effort has been expended without overcoming these limitations or insuring long enough operating life.

Last among this group, EP displays have excellent appearance but require relatively high switching voltages, although the sustaining power is low due to the inherent memory. In addition, slow response and difficulty in multiplexing are disadvantages, although the addition of a control element to the structure has improved the multiplexing capability. This technique appears well suited to large displays, but requires more development, particularly in the colloidal solutions used.

1.3. Large Screen

Another aspect of displays that has attracted a great deal of attention perhaps with little justification as to actual need, is the provision of large screen displays for group viewing. A large number of technologies have been used or attempted in the apparently never ending search for the ultimate solution to television on the wall. The most successful results have been achieved with CRT projection and with the combination of electron beam modulated oil film and Schlieren optics as embodied in the well known Eidophor. Both of these techniques have been embodied in commercial systems and have seen considerable acceptance.

In addition to these two well established approaches, there are several others worthy of some consideration, in particular as they may involve microstructures. These include the use of either a laser or CRT to optically address a liquid crystal panel by means of a photosensitive layer. The photosensitive layer is made up of an assembly of microstructures

cont'd.

1.3. Large Screen, cont'd.

so as to avoid cross talk when one area is addressed. A similar system has been developed using FE instead of liquid crystal. The optically addressed cell acts as a light valve in the path of projection light sources.

Another approach uses the electron beam in a CRT to selectively charge and cause to rotate individual metal foil elements that act as a reflective surface and may be used to project the image that is created onto a large screen. The elements that make up this surface must be microstructures if reasonable resolution and surface size are maintained.

2. Scientific and Technological Needs

2.1. Requirements

We may best establish what improvements are needed in display devices by presenting a set of specifications for an ideal display device, and comparing this set with what is attained or can be attained by existing devices and technology. This specification is given in Table 1 in terms of a standard set of parameters. The extent to which each technology meets these requirements is indicated by the matrix given in Table 2 where a rating range of 0-10 is used, with 10 designating the closest conformance to the specification for the parameter listed in the row, to the technology listed in the column, and a question mark indicates insufficient data.

It is interesting to note that a single, unweighted sum puts CRTs at the top with LEDs close behind, followed by ac plasma, thin film EL and dc plasma, with FE at the bottom of the list. However, this is somewhat misleading due to the absence of data for some of the parameters, leading to perhaps undeservedly low scores in some cases. More significantly, the sum is weighted against the reflective types, since they receive a zero for luminance, and against those technologies that are too new for reliable information to be available as to life, cost and maximum size. More importantly, if we eliminate structure, power, and maximum size, the CRT is by far the best, and if we make favorable assumptions for ac EL then it approaches the CRT, with the plasma displays not far behind. Of course, this kind of evaluation is limited in its utility, and it is necessary to decide on the relative importance of each parameter to the application in order to arrive at a realistic evaluation of the state of the technology. In any event, we may use the matrix shown in Table 2 as a guide to the capabilities and lacks of each technology, and as an indication of what improvements are necessary.

cont'd.

2.2. Research and Development Needs

2.2.1. CRTs

a) Penetration Color-
One primary area for CRT development is the penetration color device. Here the most important need is the investigation of thin film, transparent phosphors that will reduce the switching voltages required to go from one color to another. Fabrication techniques to allow three different color phosphors to be combined in one envelope are the ultimate goal.

b) Matrix CRT-
Another important program is the development of improved large area cathode structures for the matrix CRT, combined with fabrication techniques for producing the multi-aperture grids used as the switching elements. Microstructures might be one approach to this problem.

2.2.2. Matrix Panels

a) LEDs-
Monolithic LED structures with densities of over 40 to the cm and substrate sizes of 5 to 8 cm on a side would permit high resolution panels of useful size to be constructed, when combined with electrode patterns of high density. In addition, if improved efficiencies were achieved, this would permit multiplexing of larger numbers of pixels than is now feasible. Multicolor could be included if multiple LEDs were used, in which case the electrode problem is truly formidable. Alternatively, LEDs with multicolor capabilities could be used.

b) Thin Film EL-
Thin film technology to allow fabrication of large structures which can be matrix addressed and scanned would lead to assemblies that could be used for many purposes, such as information and entertainment displays. This appears to be a high potential area, especially if multicolor can be achieved. Multicolor requires the development of phosphors that can produce the various colors in the thin film variety, or a phosphor that can emit sufficient energy to activate standard color phosphors. In either case, the number of pixels to be addressed is tripled over the monochromatic version, with the consequent increase in pattern complexity.

c) Gas Discharge-
Some improvements in fabrication techniques may result in lower cost, but the only area that appears to warrant some additional effort, at least insofar as the monochromatic versions are concerned, is the use of capillary tubes to build large panels, although the application of self-shift to the ac plasma is a useful development. Two problems that remain unsolved are the addition of multi-color capability and the inclusion of gray scale in some simple fashion. Experimental multi-color panels have been built, using the plasma output to activate color phosphors, but while some feasibility has been established it is still a long way from demonstrated success. Gray scale has been

cont'd.

2.2.2. Matrix Panels cont'd.

achieved in the ac plasma by pulse duration modulation but better techniques are needed. One other approach has been to use a multi-layer panel for gray scale and might repay further investigation. Here microstructures might be used to facilitate the construction of such a device.

d) Liquid Crystal-

Material investigation to develop materials with fast switching times and wide temperature ranges are the most significant areas. In this respect, polarizers appear to introduce a problem in achieving wide temperature ranges, and microstructures might permit improvement of polarizer performance, or else development of other LC display techniques, structures and materials that operate without polarizers, but without the deficiencies of dynamic scattering are the possible approaches. In addition, the attainment of multi-color through the use of the DAP effect needs further investigation.

e) Ferroelectrics-

Ferroelectrics require thinner crystal structures to allow lower switching voltages and faster switching speeds. Very little is known about operating life and ultimate cost, which may determine the usefulness of this technology. If these improvements can be achieved, ferroelectrics may be very important for displays.

f) Electrochromics-

Unless switching time is reduced and a multiplexing capability achieved, electrochromics will not fulfill their indicated promise. New materials and a better comprehension of the exact chemical processes involved may lead to such improvements.

g) Electrophoretics-

Slow switching, high drive voltages, and uncertainty as to the exact mechanisms of performance degradation limit the usefulness of this technology. More detailed theory should lead to materials and microstructures whose performance can be better predicted and controlled so that satisfactory performance for various applications can be reached.

2.2.3. Large Screen Displays

The major area for development in large screen displays is the microstructures used in the beam addressed liquid crystal and ferroelectric systems. A similar need exists in the electron beam addressed metal foil CRT that has been used for large screen projection.

3. Impact

3.1. CRTs

The development of improved thin film phosphors for penetration CRTs

3.1. CRTs cont'd.

may have a major impact on entertainment displays if the results are compatible with television signals, although this is a somewhat remote possibility. However, computer graphics will definitely be impacted by the addition of a versatile color capability to the vector graphics systems already in wide use. This will have a very wide spread effect, since color is being used at present in only a limited number of such installations, and the resultant expansion could be significant.

The matrix CRT is of lesser significance, since a flat CRT will find few applications not met by standard CRTs or the matrix panels available or promised. However, here too the use of penetration color will expand the value of this device, especially as the circuit corrections required for the single gun penetration CRT are not required for the matrix version, and the multiplication of electrodes found in the color panels is not necessary.

3.2. Matrix Panels

Any work in thin films or monolithic assemblies should develop technologies that are applicable to microcircuits and memories. Also, if flat panel assemblies in any of the technologies become practical at competitive costs, they may be used in large scale applications such as automobile speedometers and other indicators, which should considerably expand the market.

Liquid crystal and ferroelectric panels may also be used for printing, and create something of a revolution in the field of typography. Here microstructures will be very important.

4. Opportunities

4.1. Universities

Thin film phosphors, both for CRTs and matrix panels, should benefit from good theoretical and experimental work, so that a better understanding of the exact mechanisms is achieved. There is still too much black art in making phosphors, in spite of the many years of experience. In addition, research into cathode materials and structures, and theoretical analysis of new and improved guns should be beneficial.

In matrix technologies, higher efficiency LEDs, especially towards the blue, and better gas discharge mixtures would be useful, especially with higher uv emissions that can activate color phosphors for multicolor displays. Improved liquid crystal materials with fast switching times and wide temperature range, preferably not requiring polarizers, are very necessary for this technology to advance. The same holds true for ferroelectric material, although the main problem is to produce thin discs. As to electrochromics and electrophoretics, theoretical studies of the chemical reactions in the former and charged particle motion in fluids for the latter should aid in the design of viable displays.

cont'd.

4.1. Universities, cont'd.

Finally, the application of microstructures to electrode patterning is a basic requirement for all matrix displays.

4.2. Industry

Industry should continue to be active in the development of penetration color and matrix CRT devices, drawing on fundamental research in phosphors and large cathode structures by the Universities. The significance of microstructures to these developments has been noted previously.

For matrix devices, all the technologies discussed previously can be used to achieve better performance of the devices using these technologies. Microminiaturization and microstructures are important for the switching devices and the electrode patterning, as described, and further development of the microcircuits should greatly benefit matrix panel displays, especially those using EL and LC technologies. Since two of the dimensions of a display device are controlled by the needs of the human observer, the only direction for size reduction lies in the depth or thickness of the device. Some improvements are possible in this dimension, but the main emphasis should be on developing flat panel matrix displays with the circuit elements as an integral part of the display assembly. These elements can be microstructures, and increased densities will permit a larger proportion of the total electronics to be included on the display panel.

****

Materials for Displays

Table 1

Parameter	Value
Peak Luminance	> 30,000 nits
Peak Contrast Ratio	> 100
Device Resolution	> 1000x1000 shrinking raster lines or addressable elements
Response Time	< 100 nanoseconds per pixel
Minimum Element Size	.025 mm
Maximum Element Size	2.5 mm
Minimum Display Size	25 cm
Maximum Display Size	2.5 m
Power	< 100 μW per element
Structure	Flat Panel
Material	Solid State
Angle of View	> $\pm$ 70°
Life	> 30,000 hrs
Cost	< 0.1 c per pixel
Number of Colors	4 - 7
Memory	Intrinsic to element or panel

Par / Tech	Lum	CR	Res	Res T	Element Size Min	Element Size Max	Dis Size Min	Dis Size Max	Pow	Structure Panel	Structure Solid	No Vac	Angle	Life	Cost	Color	Mem	Sum
CRT	10	10	10	10	10	10	10	3	3	3	0	0	8	10	8	10	0	115
DC Plasma	1	5	10	7	7	7	10	2	4	10	0	10	8	10	5	1	10	107
AC Plasma	1	5	10	7	7	7	10	2	4	10	0	10	8	10	5	1	10	107
Dyn Scat LC	NA	2	5	1	10	10	10	4	10	10	0	10	5	10	8	1	0	96
TN LC	NA	2	5	1	10	5	10	2	10	10	0	10	3	10	8	1	0	87
FE	NA	8	5	8	10	?	10	?	10	10	10	10	3	?	?	1	0	85
EL Chrom	NA	5	5	1	10	?	10	?	10	10	10	10	8	?	?	3	10	92
EP ID	NA	5	5	3	10	?	10	?	10	10	3	10	8	?	?	3	10	87
TF DCEL	2	5	10	5	10	?	10	?	5	10	10	10	8	3	?	1	0	89
TF ACEL	10	10	10	6	10	?	10	?	5	10	10	10	8	8	?	1	0	108
LED	10	10	3	10	10	?	10	?	2	10	10	10	8	8	5	5	0	111

Table 2

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