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MANUFACTURING METHODS AND TECHNOLOGY PROGRAM FOR BEAM LEAD SEAL--ETC(U)
SEP 77 B ARMBRUSTER, G ZENNER, D BUHANAN DAAB07-75-C-0033

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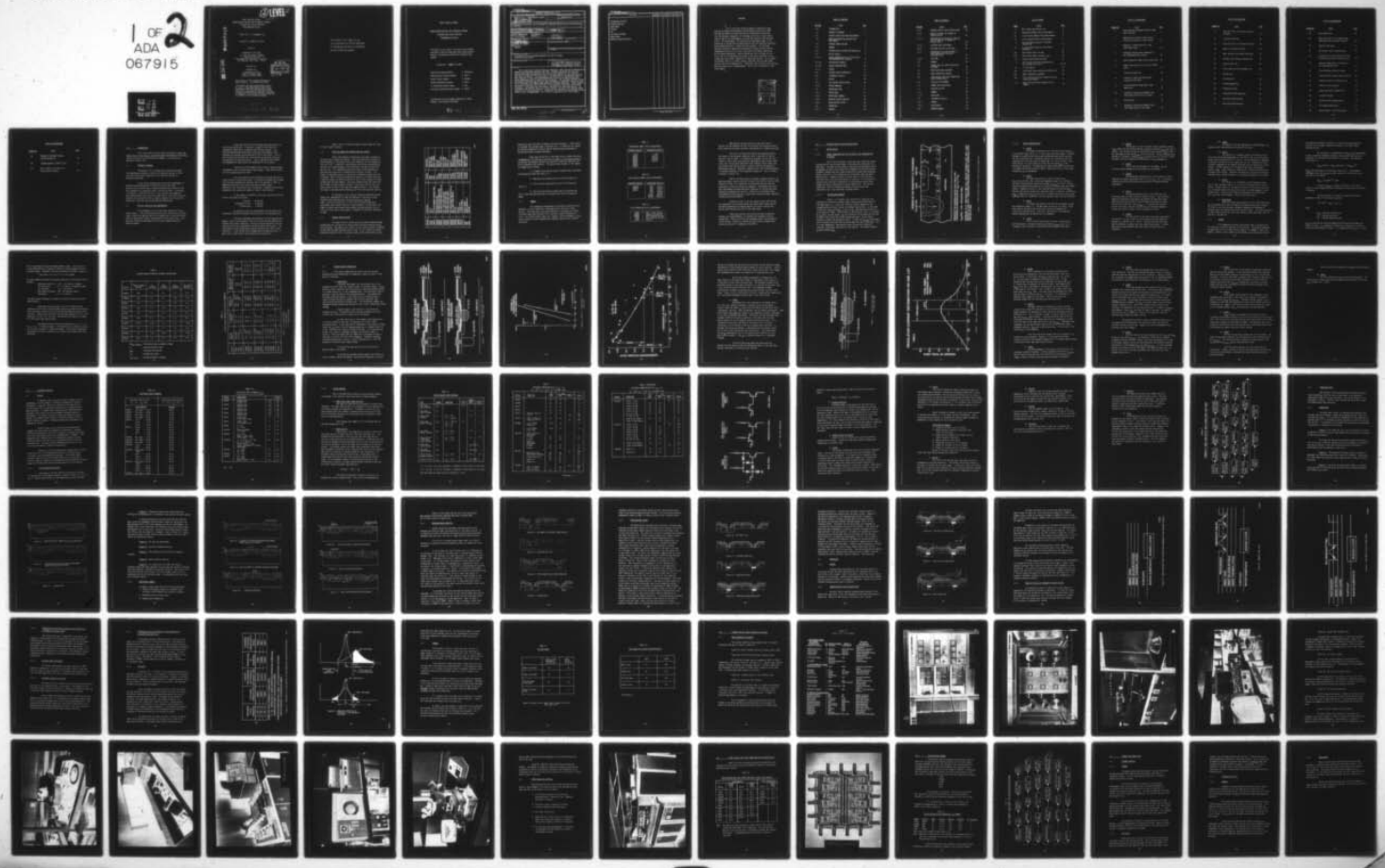

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FINAL TECHNICAL REPORT

MANUFACTURING METHODS AND TECHNOLOGY PROGRAM

FOR BEAM LEAD SEALED JUNCTION

SEMICONDUCTOR DEVICES

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21 MAY 1975 - 21 SEPTEMBER 1977

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FINAL TECHNICAL REPORT

MANUFACTURING METHODS AND TECHNOLOGY PROGRAM FOR BEAM LEAD SEALED JUNCTION SEMICONDUCTOR DEVICES

The object of this study is to refine the processes required to fabricate beam beam lead sealed junction devices in production quantities by manufacturing methods.

Contract No. DAAB07-75-C-0033

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13. ABSTRACT

This is the Final Technical Report on Motorola's Beam Lead Device Manufacturing Methods and Technology contract with ECOM. Although the market for beam lead devices unfortunately diminished over the two-year timespan of this program, resulting in later cancelling of some of the requirements, the work was certainly well worth the effort. The technologies initiated and the improvements made in the processing of the devices provided Motorola with the necessary experience which proved beneficial on other military programs. The low power Schottky process was employed and developed on these junction-isolated integrated circuits for the first time within the Federal High Reliability Products Operation. Master masking was also initiated for the first time in this Operation and proved to be highly successful in providing very high yields, especially for beam lead devices. As an example, the 54LS197, which is a binary counter, achieved a 40.6 percent probe yield on the first processing lot. Conversely, the results on the discrete devices proved to be a disappointment. All of this is detailed in this final report.

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ABSTRACT

This is the Final Technical Report on Motorola's Beam Lead Device Manufacturing Methods and Technology contract with ECOM. Although the market for beam lead devices unfortunately diminished over the two-year timespan of this program, resulting in later cancelling of some of the requirements, the work was certainly well worth the effort. The technologies initiated and the improvements made in the processing of the devices provided Motorola with the necessary experience which proved beneficial on other military programs. The low power Schottky process was employed and developed on these junction-isolated integrated circuits for the first time within the Federal High Reliability Products Operation. Master masking was also initiated for the first time in this Operation and proved to be highly successful in providing very high yields, especially for beam lead devices. As an example, the 54LS197, which is a binary counter, achieved a 40.6 percent probe yield on the first processing lot. Conversely, the results on the discrete devices proved to be a disappointment. All of this is detailed in this final report.

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1.0 INTRODUCTION

This is the final technical report on Motorola's Beam Lead Sealed Junction Semiconductor Devices Manufacturing Methods and Technology contract with the U.S. Army Electronics Command. The contract was awarded on 21 May, 1975.

1.1 PURPOSE OF PROGRAM

The purpose of this program was to perform the production engineering necessary to refine the processes required to fabricate both discrete and integrated circuit beam lead devices in production quantities.

It was further expected that through the improvements in manufacturing techniques and in yields the cost of beam lead devices could be significantly reduced and become more attractive from that standpoint for widespread usage in military systems. Furthermore, if successful in lowering the cost, it was believed that commercial hybrid manufacturers would also find these devices to be more attractive. Certainly the improved reliability aspects compared with chip-and-wire devices has long since been established and demonstrated.

1.2 SPECIFIC OBJECTIVES AND REQUIREMENTS

The requirements of this effort were comprised of three primary phases. First was engineering over which time period the designs, layouts, masks and redesigns were to be accomplished in delivering three groups of engineering samples representative of each device type. Progress and processing improvements must have been demonstrated from sample-to-sample.

Second was the First Article Phase requiring delivery of 100 of each device type. In addition, a sample of each had to be packaged and submitted to a complete qualification program. This required designing and developing of new beam lead packages, since they were not available with exception of TO-5's and TO-18's. Also, a qualification specification had to be written and approved since none was available for beam lead devices. Thus a combination MIL-M-38510 and ECOM/Motorola specification was generated for this purpose.

These first article samples had to have all design changes incorporated, and no further designs were allowed. There was one exception later authorized on the 5404.

The final phase was Pilot Production requiring delivery of 1,000 of each of the 35 device types. No processing changes were allowed since the same equipment and processes had to be employed in order to demonstrate and verify that these lots were as nearly representative of the first article lots as possible. A complete qualification program was also required on samples of each of these devices.

In this phase, furthermore, each device type had to achieve certain yield goals as follows:

Discretes	-	20 percent
Integrated Circuits	-	10 percent
60 Gate Array	-	5 percent

An incentive clause was incorporated into the contract for successfully achieving 20 percent yields on the IC's and 60-gate array.

The yield requirement was different from the industry-norm, however, since it was effective from initial oxide through probe and on through final visual inspection. Electrical testing and burn-in did not count since this was a requirement for qualification testing only. The 1,000 devices to be shipped were therefore selected after final visual inspection. If any lot had to be scrapped due to processing errors, it would count in the overall yield along with the back-up lot.

Table I lists all 35 device types required under the terms of this original contract.

1.3 BEAM LEAD MARKETING PRESENTATIONS AND SURVEYS

During 1976 numerous presentations were made to potential and past users of beam lead devices. One such presentation was made at the Proceedings of the Hybrid Microcircuit Symposium at Fort Monmouth on June 8 of 1976. In addition, questionnaires and surveys were generated and sent out to approximately 15,000 individuals who were on Motorola's mailing list. This represented possibly as many as 500 companies who were believed to be users or manufacturers of hybrid circuits. The number of respondees asking for additional information totaled only 250. In general, most of those who answered the question of whether there was a potential usage for beam lead devices in any of their present or future systems made the same comment: they were concerned about the relatively small number of device types available on the market, and the lack of a second source on most of the types which were available. This problem has always discouraged hybrid manufacturers from using beam lead devices.

At the outset of this contract, Motorola marketing surveys showed that requirements for beam lead devices on two major military programs alone totalled nearly 10 million devices of some 68 types. During the latter half of 1976, all of the beam lead device requirements were deleted from one of these programs. On the other, the number of device types required was reduced from approximately 38 to 5. Since the latter was an Army program, it became of significant importance to ECOM.

1.4 CONTRACT MODIFICATIONS

In January of 1977, during the Sixth Technical Motorola/ECOM Exchange meeting, the results of these surveys and other marketing inputs were presented. The question was raised, is the original forecast of weapons systems need for beam lead parts still valid? If not, should the present program be modified? How? In addition, some of the discrete device types

TABLE I

MM & T BEAM LEAD DEVICE LIST

DEVICE	FUNCTION	DEVICE	FUNCTION
1N746	3.3V Z	5405	HEX INV O.C.
1N748	3.9V Z	5410	TRIP 3 NAND
1N5314	5.14 ma CURRENT SOURCE REG.	5440	DUAL 4 NAND
2N2484	NPN HIGH GAIN (100)	5473	DUAL JK
2N2907	PNP SWITCH AND AMPLIFIER	54LS04	HEX INV
2N3251	PNP HIGH SPEED SWITCH (200 ns)	54LS08	QUAD 2 AND
2N3467	PNP 1 AMP CORE DRIVER	54LS21	DUAL 4 AND
2N3501	NPN HIGH VOLTAGE (150V)	54LS32	QUAD 2 OR
2N3635	PNP HIGH VOLTAGE (140V)	54LS73	DUAL JK
2N3639	PNP HIGH SPEED SWITCH (20 ns)	54LS74	DUAL D
2N3725	NPN 1 AMP CORE DRIVER	54LS86	QUAD 2 EX OR
2N3960	NPN RF	54LS138	DECODE-DEMUX
2N4260	PNP RF	54LS193	UP-DOWN COUNTER
2N5115	P CHAN JFET	54LS194	4 BIT S.R.
RA108	60 GATE ARRAY	54LS196	DECADE COUNTER
5400	QUAD 2 NAND	54LS197	BINARY COUNTER
5401	QUAD 2 NAND O.C.	54LS253	DUAL 4-1 MUX
5404	HEX INV		

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proved to be most difficult to process with any consistency. (These technical problems are reviewed later in Section 2.0.) It simply was not logical to continue attempting to resolve some of these processing problems on devices which were no longer marketable.

After many discussions in the months which followed regarding recommendations for deleting or modifying a number of the hardware/software and testing requirements, Motorola was advised by ECOM that they were partially terminating the contract. The overall major changes to the program are summarized as follows:

1) A number of the devices would be deleted after satisfying the Engineering Phase (see Table II).)

2) Some would be deleted after First Article (Table III).

3) Only five part types would go into Pilot Production (Table IV).

4) Only one qualification program would be required and only on those devices which were to continue into the Pilot Production phase.

1.5 SUMMARY

This program was undertaken by the Federal High Reliability Operation, a part of Motorola's Integrated Circuit Division in Mesa, Arizona. This group had no previous experience in designing and processing either beam lead discrete or 54LS junction isolated integrated circuits. This latter process (54LS) was, however, under development at that time on another military program which required dielectrically isolated substrates.

TABLE II

ENGINEERING SAMPLE DEVICE REQUIREMENTS

DISCRETE DEVICES	INTEGRATED CIRCUITS
1N748	5440
1N5314	54LS193
2N2484	54LS194
2N3251	54LS196
2N3467	54LS197
2N3501	
2N3635	
2N3639	

TABLE III

FIRST ARTICLE SAMPLE DEVICE REQUIREMENTS

DISCRETE DEVICES	INTEGRATED CIRCUITS	
2N2907A	5400	54LS21
2N3725	5401	54LS32
2N5115	5405	54LS73
	5410	54LS74
	5473	54LS86
	54LS04	54LS138
	54LS08	54LS253

TABLE IV

PILOT PRODUCTION DEVICE REQUIREMENTS

1N746 2N3960 2N4260 5404 RA108	NOTE: First article samples and complete qualification testing also required on these devices.

Additionally, master masking (as described later in Section 3.0) was employed for the first time by this processing group, which proved to be highly successful and beneficial in improving yields.

The only IC JIC beam lead devices being manufactured at the outset of this program, therefore, were in the 5400 TTL family, and only a few of those. In designing of the 5400 circuits for this contract, since yields and processing improvements were of major importance, the circuits were redesigned using Schottky diodes rather than the standard gold doping process in order to achieve the necessary speed-power products. Additional redesigns were later required because of threshold problems at high temperature operation. This is further discussed in Section 3.0.

Despite the many technical problems, downward trend of the beam lead market, and the deletion of most of the devices from the Pilot Production Phase, this program has provided Motorola with technical experience in areas not previously attempted. Furthermore, the yield goal requirements provided additional incentive for instituting better processing procedures and controls. Some of this technology and/or improvements has been applied in other wafer processing areas, therefore, providing additional benefits.

Sections 2.0 and 3.0 of this report reviews the discrete and integrated circuit device design and layout phase, detailing the problems encountered and changes required in order to satisfy the device specifications over the full MIL temp range.

These same sections also discuss the wafer processing problems and accomplishments of discretes and integrated circuits respectively. Section 4.0 lists the equipment used in the processing of the devices. Section 6.0 reviews the qualification program test results and Section 7.0 summarizes the effort.

2.0 DISCRETE DEVICE DESIGN AND PROCESSING

2.1 DEVICE DESIGN

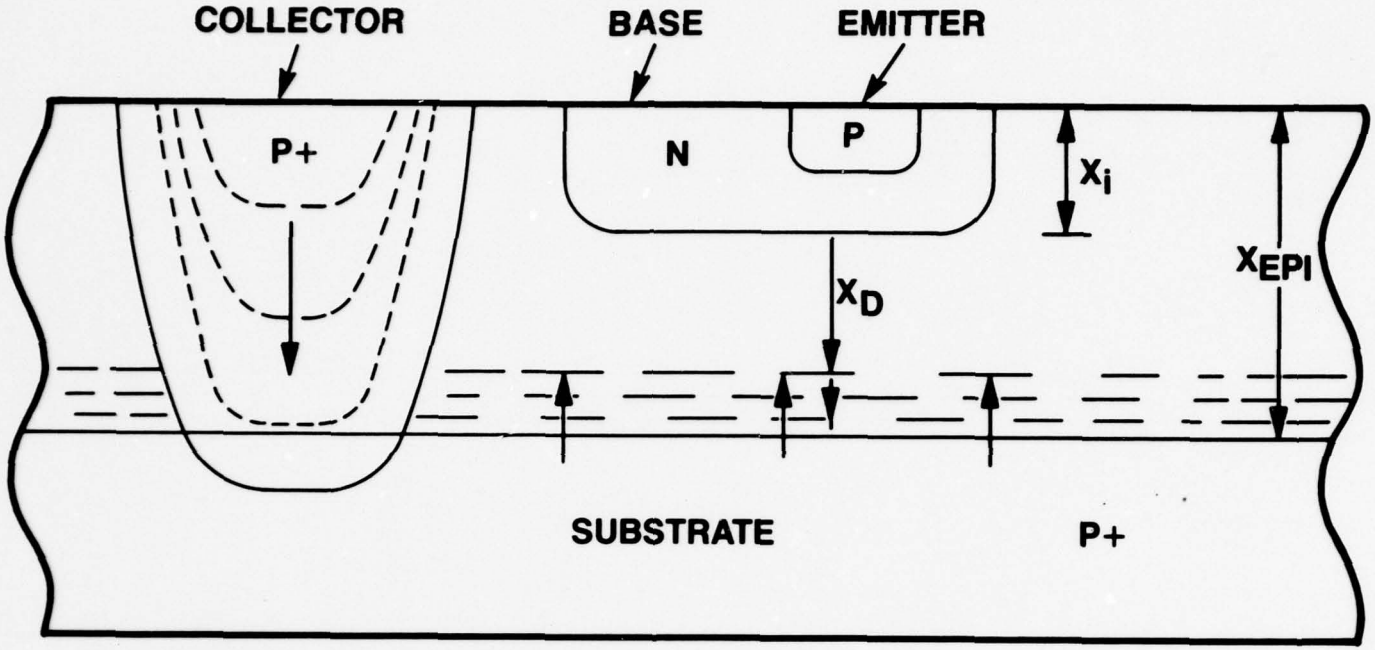
2.1.2 UNIQUE CHARACTERISTICS OF THE DEVICES FOR CONSIDERATION IN DESIGN

Each of the transistors, J-FET and zener diodes had unique characteristics providing challenges in designing and processing with beam leads. The same starting material and processing procedures cannot be employed as used in the production of standard chip-and-wire devices. Parameters change drastically when processing with beam lead technology making it difficult if not impossible to consistently meet the device specifications. Probably the most critical step is in the collector diffusion since a top collector contact is required. It is during this long diffusion time that outdiffusion of the substrate occurs which changes the device characteristics quite dramatically. This was the single most difficult problem encountered in processing of the transistors, and is now explained in greater detail.

2.1.2.1 OUTDIFFUSION PROBLEM

Figure 1 is a typical cross section of a transistor and indicates the continuous problems faced in processing discrete devices with beam leads, i.e., with a top collector contact compared to the standard bottom collector contact on non-beam lead devices. In designing a transistor, BV_{CEO} and BV_{CBO}, as well as H_{FE}, determine the resistivity of the epitaxial layer. The thickness of the epitaxial layer is calculated by X_{jb} (base junction depth), X_{BC} (out diffusion of the substrate into the epitaxial layer during the various processing steps), and X_D (space required to support the depletion layer). To meet the $V_{CE(sat)}$ requirement, the P+ collector diffusion must be driven deep into the P+ substrate. This is a high temperature, long duration cycle during which time the P+ substrate outdiffuses substantially into the Epi. This effect reduces X_D which affects BV_{CEO}.

DESIGN OF EPI RESISTIVITY & THICKNESS



RESISTIVITY IS CONTROLLED BY CEO, CBO & HFE
THICKNESS IS CONTROLLED BY X_{JB}, X_D & X_{BL}

V_{CE}(SAT) = F(P+ DIFFUSION TIME)

INCREASE IN P+ DIFFUSION TIME WILL REDUCE VCE(SAT), BUT WILL ALSO REDUCE X_D DUE TO P+ SUBSTRATE DIFFUSION AND WILL EVENTUALLY FAIL FOR CEO & CBO.

Figure 1 CROSS-SECTIONAL DRAWING OF TYPICAL BEAM LEAD TRANSISTOR

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2.1.2.2 DESIGN CONSIDERATIONS

1) 2N2484

The unique characteristics of this device are high gain at low current (H_{FE} >30 at I_C = 1.0 μA), and a low noise figure. The major problems in producing this device were maintaining good surface quality for low current gain and in basewidth control for a relatively flat gain characteristic over four orders of magnitude in collector current. Basewidth control is critical because of the high gain and BV_{CEO} of 60V required of the device. No downgrade to a more relaxed gain specification is allowed, necessitating emitter home-in (basewidth) within a tight band dictated by H_{FE} and breakdown.

2) 2N2907

This PNP transistor has a high dc current gain (H_{FE} >50 at 500 mA), high current gain bandwidth product (f_t >200 MHz), and low collector-emitter saturation voltage ($V_{CE(sat)}$<0.4 Vdc at 150 mA). Controlling basewidth and keeping the collector resistance down was a major concern. Basewidth control is very important because of the high BV_{CEO} (60 Vdc) and high DC current gain specified from 0.1 to 500 mA. Controlling BV_{CEO} is made more difficult since this is a PNP device with a boron doped substrate that will outdiffuse into the epitaxial layer with any diffusion.

3) 2N3251

This device has higher dc current gain and higher current gain bandwidth product (f_t = 300 MHz) than the rest of its family. Basewidth control determines the device gain at certain breakdown and resistivity characteristics. The size of the emitter is an important design consideration for making the "f_t" parameter.

4) 2N3467

This is a high current device (Ic max = 1A) with fast switching speeds. Collector saturation voltage ($V_{CE(sat)}$<1V at 1A) is increased by any resistance in the emitter-to-collector current path.

5) 2N3501

The device has a high collector-emitter breakdown voltage (V_{CEO} >150V) and low collector-emitter saturation voltage ($V_{CE(sat)}$<0.4 Vdc at 150 mA). Epi resistivity must be sufficiently high to obtain V_{CEO} of 150V, yet low enough so that the $V_{CE(sat)}$ limit can be met. The epi thickness must be kept to a minimum to reduce $V_{CE(sat)}$ and must not be so thin as to cause thickness limiting of depletion which results in BV_{CEO} degradation.

6) 2N3635

This is the PNP complement of the 2N3501, and the critical process parameters are the same as for the 2N3501.

7) 2N3639

The outstanding characteristics of this device are high speed and low output capacitance (Cob <3.5 pF at V_{CB} = 5V). High speed is achieved by minimizing the emitter area which will reduce the output capacitance.

8) 2N3725

The unique characteristics of the 2N3725 are fast switching speeds and high collector current (1A max). Fast switching speeds are obtained by gold doping and keeping the base width small. Resistance must be minimized in the collector and emitter to reduce heating and to maintain a low $V_{CE(sat)}$. To achieve low collector-emitter resistance, the deep collector must be diffused completely through the epitaxial layer, and the basewidth minimized.

9) 2N3960

This NPN device has low input and output capacitances (Cib and Cob <2.5 pF) as well as a very high current gain-bandwidth product (f_t >1600 MHz at Ic = 10 mA). The base area and base metal must be minimized to reduce input and output capacitances. To obtain high current gain bandwidth the emitter width and depth must be minimized.

10) 2N4260

This device is the PNP complement of the NPN 2N3960, and process control considerations are basically the same.

11) 2N5115

This device is a P-Channel junction field-effect transistor with low "on resistance" (RDS on = 100 ohms at VGS = 0) and low gate-source cutoff voltage (VGS off = 3 to 6V). The on resistance is dependent on the bulk resistivity of the channel and its size. Gate-source cutoff voltage is dependent on the channel width and the bulk resistivity of the channel. Thinner channels will increase on-resistance and decrease cutoff voltage. Lower resistivity material will reduce on-resistance and increase cutoff voltage. Therefore, the best way to reduce on-resistance and keep cutoff voltage the same is to increase the amount of the channel.

12) 1N5314

This device is a field-effect current regulator diode with a tight regulator current (I_p = 4.7 mA $\pm$ 10 percent at 25V) specification. Process control of the regulator current is difficult to maintain to $\pm$ 10 percent because the regulator current is greatly dependent on the channel width. Even with very tight epi tolerances, the channel width will vary with slight changes in diffusion characteristics.

13) 1N746/1N748

These low voltage zener diodes (3.3V and 3.9V respectively) use an aluminum (Al) alloy to produce low voltage zener action. Because Al alloy is very fast and zener voltage is dependent on the method of alloying used, the time must be controlled very closely. The close tolerances on these diodes and the fact that they overlap slightly make them ideal for running in the same lot.

2.1.3 DESIGN

This summarizes the basic calculations made in designing the 10 transistors originally required on this program. The equations employed are applicable to all of these devices; however, the 2N2484 is used as an example. Tables V and VI summarize the thickness calculations and material

and processing parameter information as derived from these equations (Table VI also includes information pertinent to the other three discrete devices.)

Epi resistivity is determined from BV_{CEO} (min) requirements. To meet a specified breakdown voltage at some required current gain, a particular epi thickness and resistivity is required. The governing relationship is:

$$BV_{CBO} \text{ (planar)} = BV_{CEO} \text{ (required)} \times (Beta_{max})^{1/4}$$

BV_{CBO} then determines the required epi resistivity. The breakdown requirements are that BV_{CEO} be greater than 60V at current gains less than 800 for the 2N2484.

$$BV_{CBO} = 60\ (800)^{1/4} = 320V$$

To obtain a BV_{CEO} in excess of 320 volts, from Irvins curves, it can be determined that an epitaxial resistivity of 5.5 ohms-cm is required.

The total epitaxial thickness is determined by three parameters as seen in the following equation:

$$T \text{ epi (min)} = X_{ODS} + X_{jb} + X_D$$

where:

X_{ODS} = Substrate outdiffusion
X_{jb} = Maximum base depth
X_D = Minimum depletion width

X_{ODS} is calculated by using the appropriate diffusion coefficients and diffusion times. X_{jb} is generally determined by experience in order to obtain the maximum base efficiency. X_D is determined by C_{EO} max = 60 volts

and is calculated by using the Lawrence Warner curves. This results in a total base width of 9.0 microns of which 7.5 microns extends into the collector region. Therefore, the total minimum epi thickness is equal to:

$$T\ epi\ (min) = 2.5 + 2.2 + 7.5 = 12.2\ microns$$

The other essential material and process parameters for this device are as follows:

Substrate resistivity:	.005 - .013 ohm-cm. As doped
Epi resistivity:	5.5 - 7.4 ohm-cm. Phosphorus doped
Epi thickness:	12.2 - 20 microns
Base sheet resistance:	180 - 220 ohms-per-square
Base depth:	2.0 - 2.4 microns

The other process parameters are homed in to meet the device electrical specifications.

Based upon the above design, two lots of material were processed and the results indicated that processing changes were necessary. Prior to emitter diffusion the collector-base breakdown was greater than 130 volts. After emitter diffusion, this voltage dropped to 40 - 60 volts resulting in a CEO $\sim$ 20 - 30 volts. Both CBO and CEO require a voltage of > 65 volts to meet specification.

The emitter diffusion cycle was changed from ρ_s = 2.8 - 3.0 to ρ_s = 6.5 - 7.3 ohms-per-square. This combined with an emitter junction of 1.7 micron resulted in a pipe-free process. Calculations showed that the present cycle with a junction of 2.2 microns could reveal high spike densities.

TABLE V

DISCRETE DEVICE EPITAXIAL THICKNESS CALCULATIONS

DEVICE	BV_{CBO} (PLANAR) (VOLTS)	X_D (MICRONS)	X_{ODS} (MICRONS)	X_{jb} (MICRONS)	T_{epi} (min) (MICRONS)
2N2484	320	7.5	2.5	2.2	12.2
2N2907A	250	5.9	4.0	2.84	12.74
2N3251	166	3.6	3.2	2.5	9.3
2N3467	160	3.7	2.47	3.0	8.5
2N3501	624	15.0	4.0	4.0	23.0
2N3635	583	17.0	5.0	3.5	25.5
2N3639	19.85	0.85	1.5	1.5	3.85
2N3725	175	4.7	1.0	3.3	9.0
2N3960	54	0.64	2.85	1.0	4.49
2N4260	52.5	1.3	2.5	1.0	4.8

BV_{CBO} (PLANAR) = Calculated planar breakdown voltage

X_D = maximum depletion width

X_{ODS} = substrate outdiffusion

X_{jb} = maximum base depth

T_{epi} (min) = minimum epitaxial thickness

TABLE VI

DISCRETE DEVICE MATERIAL AND PROCESS PARAMETERS

DEVICE	EPI RHO (Ohm-cm)	EPI THICKNESS (Microns)	SUBSTRATE RHO (Ohm-cm)	BASE SHEET RHO (Ohms/square)	BASE DEPTH (Microns)
1N746	Intrinsic	2.8 - 3.2	.0031 - .005 (3)	N.A.	N.A.
1N748	Intrinsic	2.8 - 3.7	.0031 - .005 (3)	N.A.	N.A.
1N5314	1.3 - 2.0 (3)	3.8 - 4.8	3 - 4 (2)	N.A.	N.A.
2N2484	5.5 - 7.4 (3)	12 - 20	.005 - .013 (1)	180 - 220	2.0 - 2.4
2N2907A	7 - 9 (2)	14 - 16	.001 - .008 (2)	90 - 110	2.6 - 2.8
2N3251	8.5 - 10 (2)	9 - 11	.001 - .008 (2)	84 - 98	2.0 - 2.5
2N3467	3.3 - 6.7 (2)	12.5 - 15.5	.001 - .008 (2)	90 - 110	1.9 - 2.4
2N3501	19 - 35 (3)	34 - 41	.005 - .013 (1)	240 - 280	3.7 - 4.2
2N3635	19 - 35 (2)	30 - 40	.008 - .020 (2)	90 - 110	2.8 - 3.2
2N3639	0.3 - 0.7 (2)	5 - 7	.001 - .008 (2)	110 - 140	1.0 - 1.5
2N3725	4.2 - 6.3 (3)	11.5 - 13	.001 - .005 (1)	180 - 230	3.0 - 3.3
2N3960	0.4 - 0.8 (3)	3.6 - 5.6	.001 - .005 (1)	235 - 335	Approx. .75
2N4260	0.8 - 1.2 (2)	4.5 - 6	.001 - .008 (2)	260 - 285	Approx. .80
2N5115	1.2 - 1.3 (2)	4 - 5	.07 - .15 (3)	N.A.	N.A.

NOTES: (1) Arsenic dopant
(2) Boron dopant
(3) Phosphorus dopant

2.2 DISCRETE DEVICE PROCESSING

2.2.1 This section summarizes and details some of the major problems which were experienced in attempting to meet the overall yield goals of 20 percent.

1) 1N746/1N748

A possible improvement was investigated late in the program which would lower the leakage current of the Zener diodes. Rather than use a boron diffusion into the substrate to make the surface intrinsic or of high resistivity, it was recommended that a 3-micron-thick intrinsic epitaxial layer be grown on the substrate material. The problem with the boron diffusion process is that there is not an effective way to control surface resistivity, whereas, the intrinsic epitaxial layer can be controlled during the growth cycle. This effectively removes the breakdown from the surface into the bulk of the silicon, eliminating surface leakage.

Figure 2 shows a cross section of the old and the proposed structure. Confirmatory wafer lots were processed using the intrinsic epi structure with a probe yield of 24 percent.

As seen from Figure 3, the leakage current measured at 1 volt was improved by one order of magnitude, and is well within the specification. It was noted that a considerably large number of diodes failed for Z_{ZT} which is the AC impedance measured at a reverse current of 20 mA. Specifications require a maximum of 28 ohms. To investigate this further, Z_{ZT} versus V_Z (breakdown voltage) was plotted as shown in Figure 4. This curve shows that the 1N746, with a breakdown voltage of less than 3.2 volts, will fail for AC impedance. Therefore, reducing the diode characteristic from $V_Z = 3.3V \pm 10$ percent to $V_Z = 3.3V\ ^{+10}_{-2}$ percent will provide a much tighter window.

It can also be seen that this kind of restriction does not apply to the 1N748.

To utilize the complete voltage range of the 1N746, the curve in Figure 4 had to be lowered. There were two potential solutions:

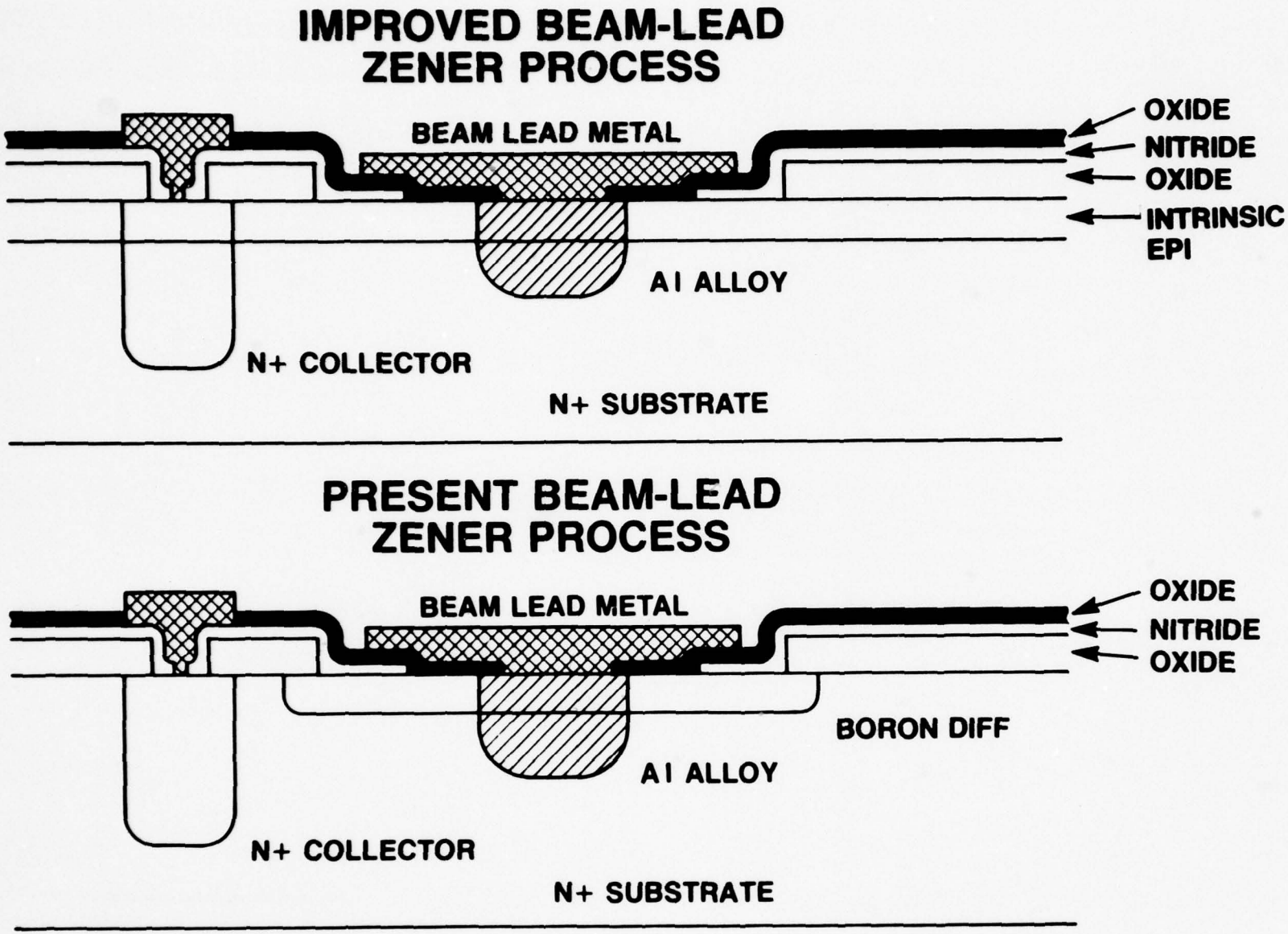


Figure 2 COMPARISON OF EPITAXIAL VERSUS BORON DIFFUSION PROCESSING OF ZENER DIODES

D8449-1

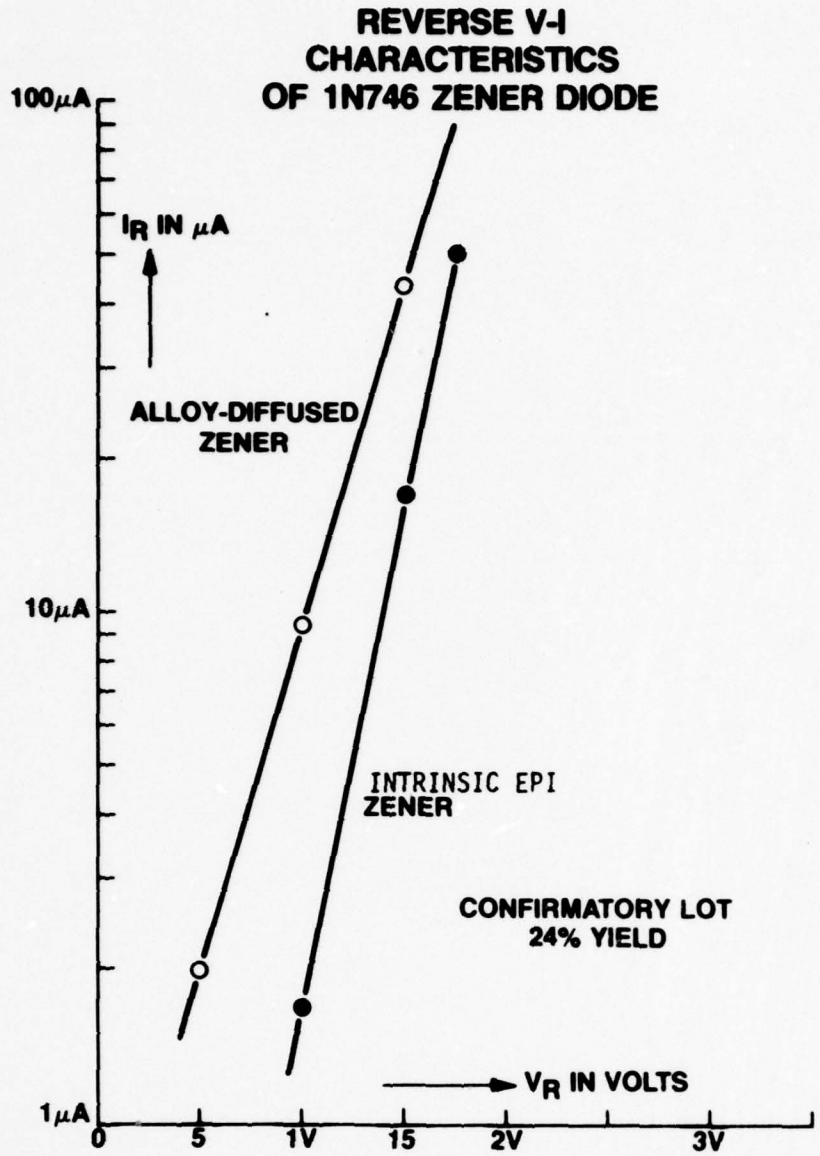


Figure 3 REVERSE V-I CHARACTERISTICS OF 1N746 ZENER DIODE

D8449-B

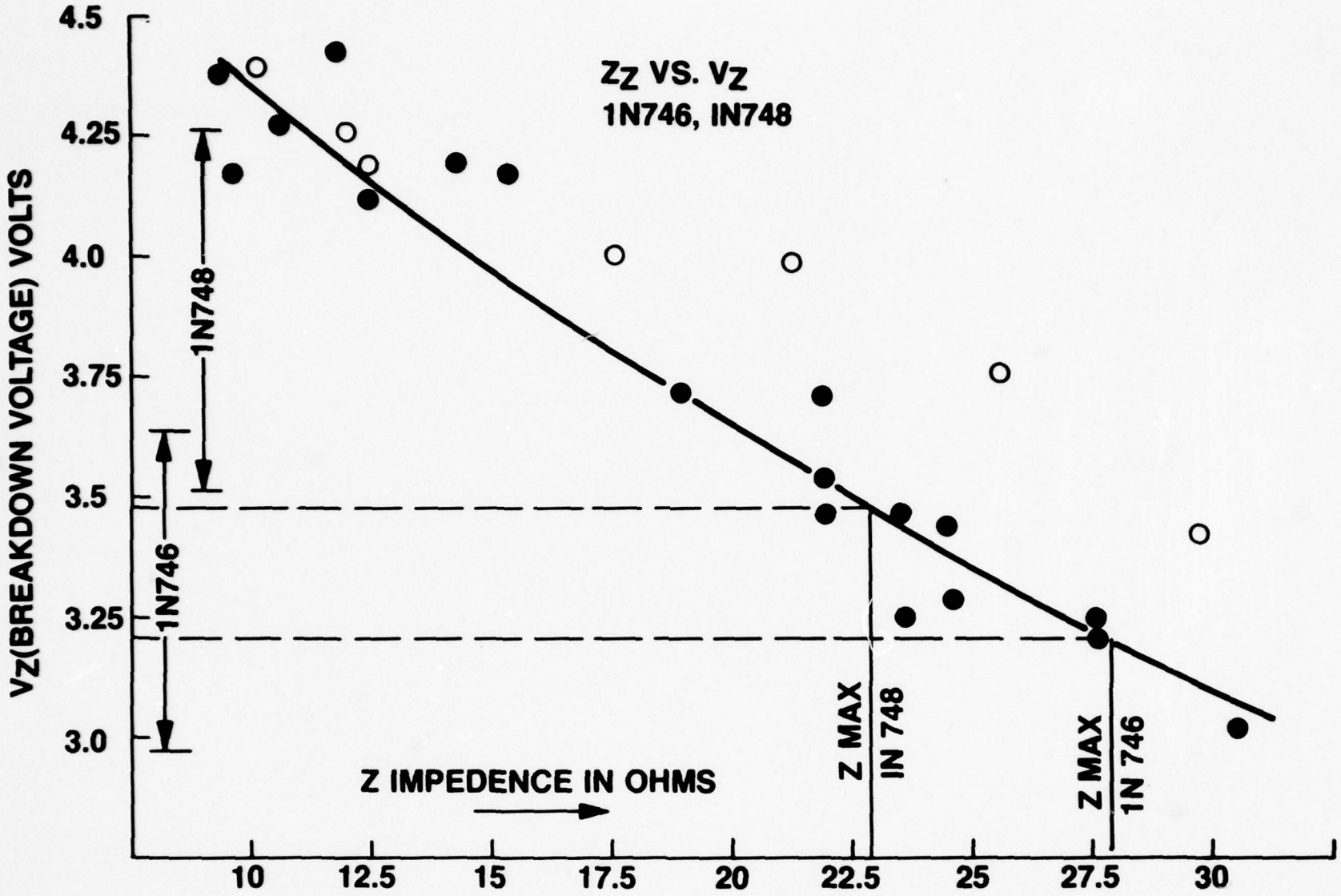


Figure 4 BREAKDOWN VOLTAGE VERSUS IMPEDANCE ON 1N746/1N748 ZENER DIODES

D8449-E

one was to increase the active area of the diode; and the second to change the gradient of the alloyed-diffused gradient of the PN junction. Figure 5 shows a cross section of the 1N746 with a larger active area. This change was implemented and proved to be beneficial in improving the yield.

One of the problems encountered in processing of the Zener diodes (to the specified voltage), as mentioned in past reports, is in the very critical alloy diffusion time. The breakdown voltage at the specified current in the reverse direction is a function of the dwell time in the furnace as well as the pull rate. The breakdown voltages can either be increased or decreased by varying the dwell and pull rate times. There is only a slight margin for error, otherwise the diodes would fall into another breakdown voltage range in this diode family.

2) 1N5314

Considerable work was conducted on the 1N5314, which is a FET, with identical problems in process control as the 2N5115. Figure 6 shows the sample I_p probe yield distribution of the total family (76 percent), the 5310 - 5314 (42 percent), and the 1N5314 (20 percent). These yield figures were only with respect to I_p (regulator current), since none of the other parameters were tested. This yield curve was obtained under extremely difficult processing conditions since there was no process control pattern to use in tweaking during the diffusion cycles. It is interesting to note that the shape of this yield curve is a direct indication of the uniformity of the epi thickness and resistivity. To overcome the processing problems, a new processing aid located on each die in the grid was incorporated into the mask set. This would permit making V_{BR} measurements prior to the source-drain diffusion for final gate diffusion home-in. The V_{BR} is directly related to V_T (threshold voltage).

Since this device was among the group which was deleted from the contract after the engineering phase, it was not known how much improvement in processing was realized.

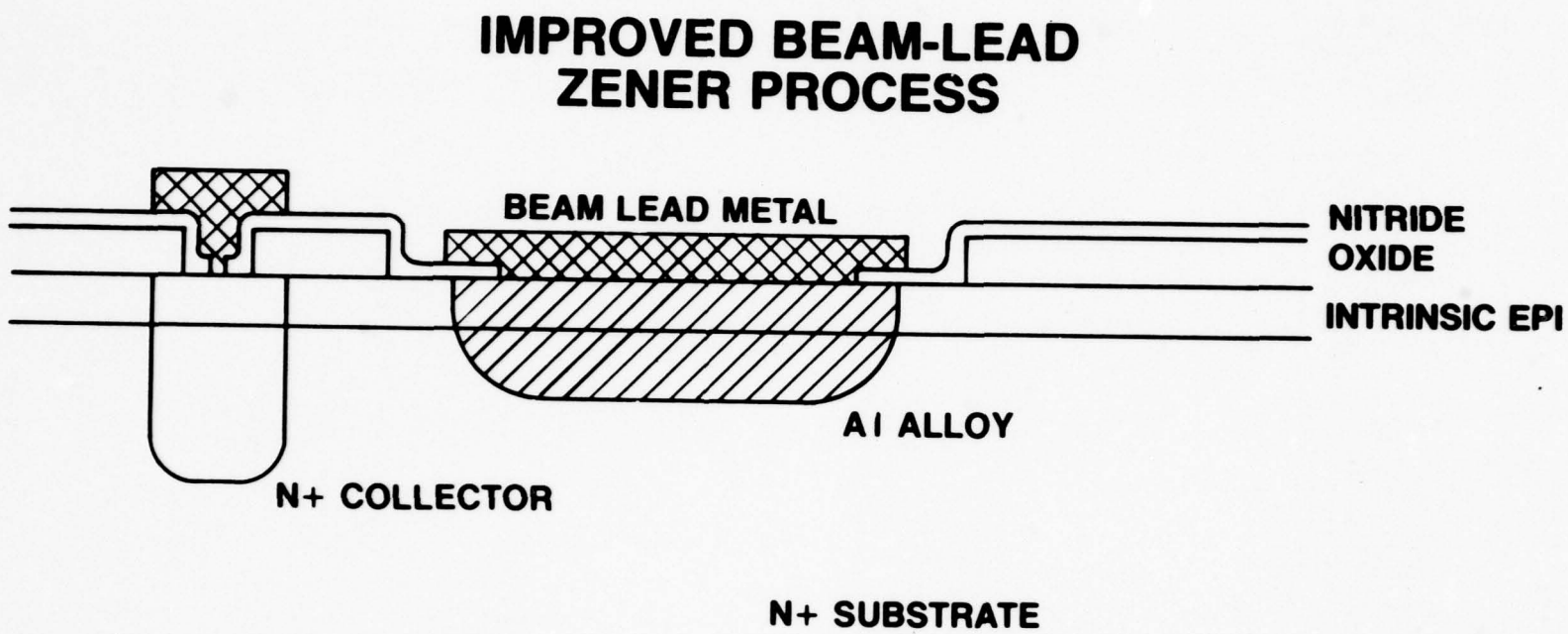


Figure 5 ZENER DIODE WITH LARGER ACTIVE DIODE AREA

D8449-D

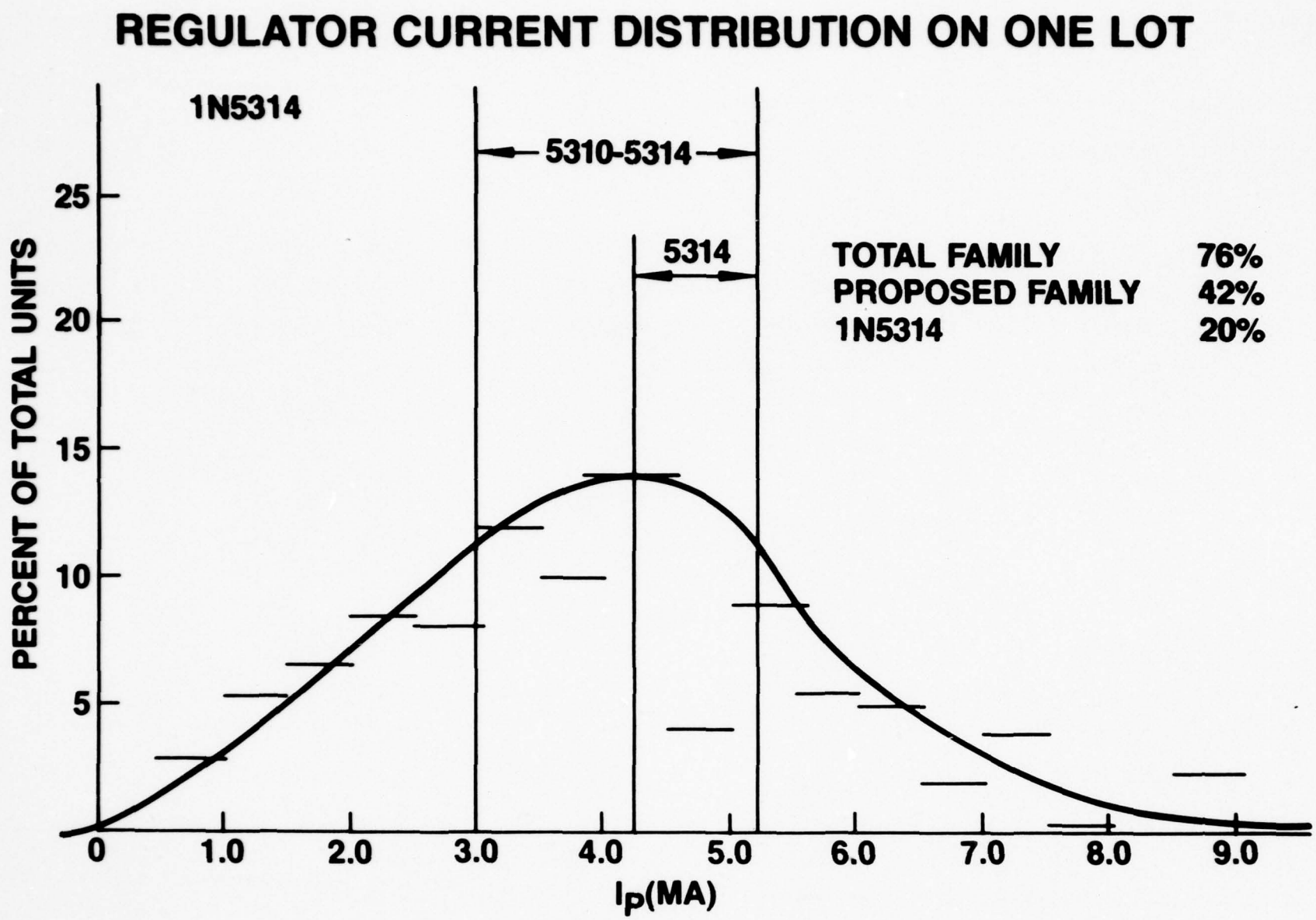


Figure 6 SAMPLE PROBE RESULTS FOR I_p ON 1N5314 FAMILY

D8449-K

3) 2N2484

Prior to deletion of this device from both first article and pilot production, five lots were processed in the first article phase. In each case, the BV_{CEO}'s were too low, i.e. in the 20 - 30 volt range as compared to the required 65 volts. It was determined that the base resistivity of 300 ohms per square and X_{jb} of 3.1 microns was not adequate for high efficiency. When supporting a BV_{CBO} of 65 volts, the spread of the depletion layer into the base is of the order of 0.95 microns. This is equal to or greater than a base width requiring an h_{fe} >200. A new base cycle was designed with a 200 ohms per square resistivity and X_{jb} = 2 microns. This resulted in a depletion layer spread of 0.54 micron. The sixth and final lot processed showed that this new base cycle was successful.

4) 2N2907A

The major problem in processing this device (a high current, high voltage PNP transistor) is the outdiffusion of the heavily doped substrate into the epitaxial layer during the long deep collector diffusion cycle. This is required in order to satisfy the high current beta and $V_{CE(sat)}$ specifications. Collector diffusion times of 60 and 90 minutes on different lots showed that this was inadequate to provide sufficient high current beta hold up and a low $V_{CE(sat)}$. Although on two subsequent lots having diffusion times of 170 and 200 minutes, these parameters were met, BV_{CEO} was slightly below spec. This was due to the outdiffusion of the substrate.

Since this device was deleted from pilot production, no further lots were processed. However, it is believed that a deep collector diffusion time somewhere between 90 and 170 minutes would provide a device which would meet these specifications.

5) 2N3251

During development of this device one of the last lots processed, yielded 4.5 percent. The main parameter failure was $V_{CE(sat)}$. Had this device continued into first article and pilot production, a longer collector diffusion time would have corrected this problem.

6) 2N3467

This device was also deleted from first article and pilot production. The last lot processed achieved a yield of 7 percent, which was down from the previous lot of 13.6 percent. The major problem was in meeting the leakage specification and it was not determined whether this was due to the diffusion of the platinum or to a surface problem.

7) 2N3501

All of the engineering lots yielded low due to $V_{CE(sat)}$ problems, high current beta and beta kink. Calculations later showed that the emitter area of this device was too small to avoid operating in the region of non-linear mobility and conductivity modulation. This caused the so-called beta kink, which resulted in a failure of high current $V_{CE(sat)}$ and beta. The non-beam lead device uses the same area and has the same beta kink; however, the R_{sat} is so much lower, due to collector contact to bottom of die. Even with a 10 hour diffusion time in the collector, the penetration is only about 20 microns. To meet all $V_{CE(sat)}$ requirements, a total R_{sat} less than 2.6 ohms is required. Increasing the diffusion time in excess of 10 hours is not practical since the substrate doping begins to affect the epi.

One potential solution is having a phosphorus doped plug in the substrate which outdiffuses into the epi and meets the collector diffusion from the top half way. However, this was not attempted since the device was later deleted.

8) 2N3635

Two first article lots were rejected for low BV_{CEO} and BV_{CBO} as well as very high $V_{CE(sat)}$. The second lot, which had an increased collector diffusion time still failed. Both lots looked good prior to the Pt diffusion; however, the Pt diffusion destroyed the collector properties reflecting in a high leakage BV_{CEO} and high $V_{CE(sat)}$. A similar argument applies to this device as with the 2N3501 with respect to beta kink. No further first article lots were processed since this device was later deleted from the list.

9) 2N3639

One first article lot was almost through wafer processing when this device was canceled. It was continued through to DC probe and proved to be the highest yielding lot (82 percent) of all of the devices processed. Five and a half wafers yielded a total of about 15,000 good die. The collector diffusion time had been increased from 35 to 60 minutes, thereby overcoming slight $V_{CE(sat)}$ problems which occurred in the past. Probe yield was quite consistent and uniform from wafer-to-wafer which reflected a mature process.

10) 2N3725

After several engineering lots were processed, it was determined that the epitaxial layer had to be increased in thickness in order to satisfy BV_{CEO} and $V_{CE(sat)}$. The major problem, however, was in attempting to meet the tight H_{FE} window of 60 to 160 at 100 mA. as well as minimum beta at 1 ampere. This device was later deleted from the program so it is unknown whether the H_{FE} specification could have been met.

11) 2N3960

BV_{CBO} problems on engineering lots were corrected by increasing the epitaxial thickness on the first article and pilot production lots. The first article lot probe yield was 63.9 percent and this lot later successfully passed the qualification program. Unfortunately, the pilot production lot failed to yield any good die due to the emitter being driven into the base too deeply resulting in punch through.

12) 2N4260

The first article had a probe yield of 40.1 percent. The major failure mode on previous lots (including one with 15 percent yield) was $V_{CE(sat)}$. The collector diffusion time was increased from 20 to 60 minutes and the $V_{CE(sat)}$ specification was easily met.

The first pilot production lot had a probe yield of 18.8 percent. However, the entire lot was later destroyed during back lap. A back-up lot only yielded 3.3 percent which meant that the yield goal was not achieved.

The first article lot successfully passed the qualification program.

13) 2N5115

All lots processed failed to yield any good devices. The first article lot most nearly met the complete specification, failing only I_{GSS} (0.5 mA) at 10 - 20 mA.

3.0 INTEGRATED CIRCUITS

3.1 DESIGN

In general, when a new circuit family concept is being implemented, a certain amount of trimming and tweaking to optimize performance is required. Motorola's approach to the 5400 and 54LS circuit families was to provide the industry with a state-of-the-art beam lead logic, i.e. master mask, sealed junction technology (both described later) as well as one with somewhat improved electrical performance. The concept in doing this was that ECOM would realize greater value added from the contract, and Motorola would realize a superior family of devices. Although problems were encountered, the approach was correct.

Motorola used a gate structure which improved upon standard 54LS noise margin and threshold at temperature. Although electrical performance of this gate is superior to standard 54LS gates, the silicon real-estate required for implementation is greater. This presented layout problems since it required more complex circuitry (requiring more silicon area) into a pre-determined chip size with fixed beam outs. This was a rather formidable task but all of the circuits were eventually layed out successfully.

Material for the 54LS devices was designed with an arsenic buried layer of 13 to 18 ohms/square resistivity diffused into an 8-12 ohm-cm <100> boron doped starting wafer. The arsenic doped epitaxial layer was 3.5 to 4.5 microns thick with a resistivity of 0.6 to 0.8 ohm-cm. Material for the 5400 devices was designed similarly except for the epitaxial resistivity which was 0.27 to 0.33 ohm-cm.

3.1.1 54LS DESIGN SPECIFICATION

The design of the 54LS family of devices was initiated in consideration of the specifications as listed in Tables VII, VIII, IX, and X. Similar specifications for the 5400 devices are not included.

TABLE VII

54LS DEVICE INPUT CURRENTS

Low-Level Input Current V_1 = .4V V_{cc} = 5.5V		High Level Input Current V_1 = 2.7V V_{cc} = 5.5V
	Input Maximum	Maximum
54LS04	Any Input - .36 mA	20 nA
54LS08	Any Input - .36 mA	20 nA
54LS21	Any Input - .36 mA	20 nA
54LS32	Any Input - .36 mA	20 nA
54LS73	J or K - .36 mA	20 nA
	Clear - .8 mA	60 nA
	Clock - .72 mA	80 nA
54LS74	Preset - .8 mA	40 nA
	Clear - 1.2 mA	60 nA
	Clock - .8 mA	40 nA
	D - .4 mA	20 nA
54LS86	Any Input - .6 mA	40 nA
54LS138	Any Input - .36 mA	20 nA
54LS193	Any Input - .4 mA	20 nA
54LS194	Clock - .44 mA	20 nA
	Other - .36 mA	20 nA
54LS196	Data Count- Board .36 mA	20 nA
	Clear - .72 mA	40 nA
	Clock 1 - .24 mA	40 nA
	Clock 2 - 2.8 mA	80 nA
54LS197	Data Count- Board .36 mA	20 nA
	Clear - .72 mA	40 nA
	Clock 1 - .24 mA	40 nA
	Clock 2 - 1.3 mA	40 nA
54LS253	Any Input - .36 mA	20 nA

TABLE VIII

54LS DEVICE SUPPLY CURRENTS (I_{cc})

DEVICE	CONDITIONS*		UNITS
54LS04	Outputs High Outputs Low	2.4 6.6	mA mA
54LS08	Outputs High Outputs Low	4.4 8.8	mA mA
54LS21	Outputs High Outputs Low	2.4 4.4	mA mA
54LS32	Outputs High Outputs Low	6.2 9.8	mA mA
54LS73	Clock = gnd Q & $\overline{Q}$ High or Low	8	mA
54LS74	Clock = gnd Q & $\overline{Q}$ High or Low	8	mA
54LS86	V_1 = nd I_v = 0 mA	10	mA
54LS138	Outputs Enabled I_o = 0 mA	10	mA
54LS193	I_o = 0 mA Clear = load = gnd Other Inputs = 4.5V	31	mA
54LS194	I_o = 0 mA V_A...V_o = gnd S_1 = S_o = Clear = Serial Inputs = 4.5V Clock = gnd then 4.5 driving measurement	20	mA
54LS196	I_o = 0 mA V_{in} = gnd	20	mA
54LS197	I_o = 0 mA	20	mA
54LS253	V_{in} = gnd V_{in} = gnd Output Control = 4.5V	12 14	mA mA

*V_{cc} = 5.5V

3.1.2 DESIGN PROBLEMS

Most of the 5400 and 54LS devices required design changes, as outlined in this section, after one or more lots were processed.

1) 5400, 5401, 5404, 5405, and 5410

The input PN diodes had to be changed to increase input threshold. The output devices were also increased in size to decrease the VOL (output voltage) over temperature. Crossunders in series with the output devices were also removed to prevent forward biasing and turning on of a Darlington transistor pair which would lead to excessive current drain at high temperatures.

These changes were common to all of the above devices and were implemented on all.

2) 5440 and 5473

These circuits also required an increase in the size of the output devices to reduce the VCE(s) and lower the output VOL. This problem was encountered due to the fact that the output devices were initially sized correctly for gold doped processing. As Motorola made the decision to implement Schottky technology for this family of devices, this size proved inadequate due to the higher offset voltage of the Schottky devices. The Schottky devices are faster than conventional gold doped devices because no minority carrier injection ever occurs at the collector-base junction, therefore, no stored charge can ever accumulate in the collector region and slow down turn-off time. Excess base drive is shunted away from injection and flows externally through the Schottky diode. As a consequence, however, since no injection occurs at the collector-base junction, the alpha inverse becomes vanishingly small and the offset voltage increases logarithmically.

$$V(\text{offset}) \simeq \frac{KT}{q} \ln \frac{1}{\alpha_i}$$

This offset voltage term is added to the VCE(s) and degrades the output voltage minimum. This can only be compensated by

TABLE IX

DIGITAL DEVICE SPECIFICATIONS

TEST	SYMBOL	CONDITION	LIMITS		
			MIN.	MAX.	UNITS
High Level Input Voltage	V_{IH}		2.0		V
Low Level Input Voltage	V_{IL}			0.7	V
Input Clamp Voltage	V_I	V_{CC} = 4.5V I = = -18 mA		-1.5	V
High Level Output Voltage	V_{OH}	I_{OH} = -400 μA V_{CC} = 4.5V $V_I = V_1^+$	2.5		V
Low Level Output Voltage	V_{OL}	V_{CC} = 4.5V $V_I = V_1^{++}$		0.4	V
Input Current At Maximum Input Voltage	I_1	V_{CC} = 5.5V V_1 = 5.5V		0.1	mA
High Level Input Current	I_{1H}			SEE TABLE I	
Low Level Input Current	I_{1L}			SEE TABLE I	
Short Circuit Output Current*	I_{OS}	V_{CC} = 5.5V	-6	-40	mA
Supply Current	I_{CC}	V_{CC} = 5.5V		SEE TABLE II	

$+V_1 = V_{1L}$ max. or V_{1H} min. whichever is necessary to get output to high state.

$++V_1 = V_{1L}$ max. or V_{1H} min. whichever is necessary to get output to low state.

*Not more than one output should be shorted at a time.

TABLE X

SWITCHING CHARACTERISTICS AT V_{CC} = 5V

T_A = 25°C C_L = 15 pF R_L = 2K OHMS f MAX.

DEVICE	CONDITION	T_{PLH} MAX.	T_{PHL} MAX.	T_{PHL} MIN.	UNITS
54LS04		20	20		nS
54LS08		24	24		nS
54LS21		24	24		nS
54LS32		22	22		nS
54LS73	Clear or Clock to Q or $\overline{Q}$	20	30		nS
				30	MHz
54LS74	Clear, Preset, or Clock to Q or $\overline{Q}$	25	40		nS
				25	MHz
54LS86	A or B Other Input Low	10.5	10		nS
	A or B Other Input High	10.5	10		nS
54LS138	Binary Select to Any Output				
	2-Level	20	41		nS
	3 Level	27	39		nS
	Enable to Any Output				
	2-Level	18	32		nS
	3-Level	26	38		nS
54LS193				25	MHz
	Count-up to Coy	26	38		nS
	Count-down to Borrow	24	24		nS
	Either Count to Q	38	47		nS
	Load to Q	40	40		nS
	Clear to Q		35		nS
54LS194				20	MHz
	Clear to Output		54		nS
	Clock to Output	41	47		nS

Continued.....

TABLE X (CONTINUED)

SWITCHING CHARACTERISTICS AT V_{CC} = 5V

$T_A = 25^oC$ C_L = 15 pF R_L = 2K OHMS f MAX.

DEVICE	CONDITION	T_{PLH} MAX.	T_{PHL} MAX.	T_{PHL} MIN.	UNITS
54LS196	Clock 1 to Q_A			30	MHz
	Clock 1 to Q_A	15	20		nS
	Clock 2 to Q_B	24	33		nS
	Clock 2 to Q_C	57	62		nS
	Clock 2 to Q_D	18	45		nS
	A, B, C, D to Q_A, Q_B, Q_C, Q_D	30	44		nS
	Load to any Output	41	45		nS
	Clear to any Output		51		nS
54LS197	Clock 1 to Q_A			30	MHz
	Clock 1 to Q_A	15	21		nS
	Clock 2 to Q_B	19	35		nS
	Clock 2 to Q_C	51	63		nS
	Clock 2 to Q_D	78	95		nS
	A, B, C, D to Q_A, Q_B, Q_C, Q_D	27	44		nS
	Load to any Output	39	45		nS
	Clear to any Output			51	nS
54LS253	Data to Y	18	20		nS
	Select to Y	30	32		nS

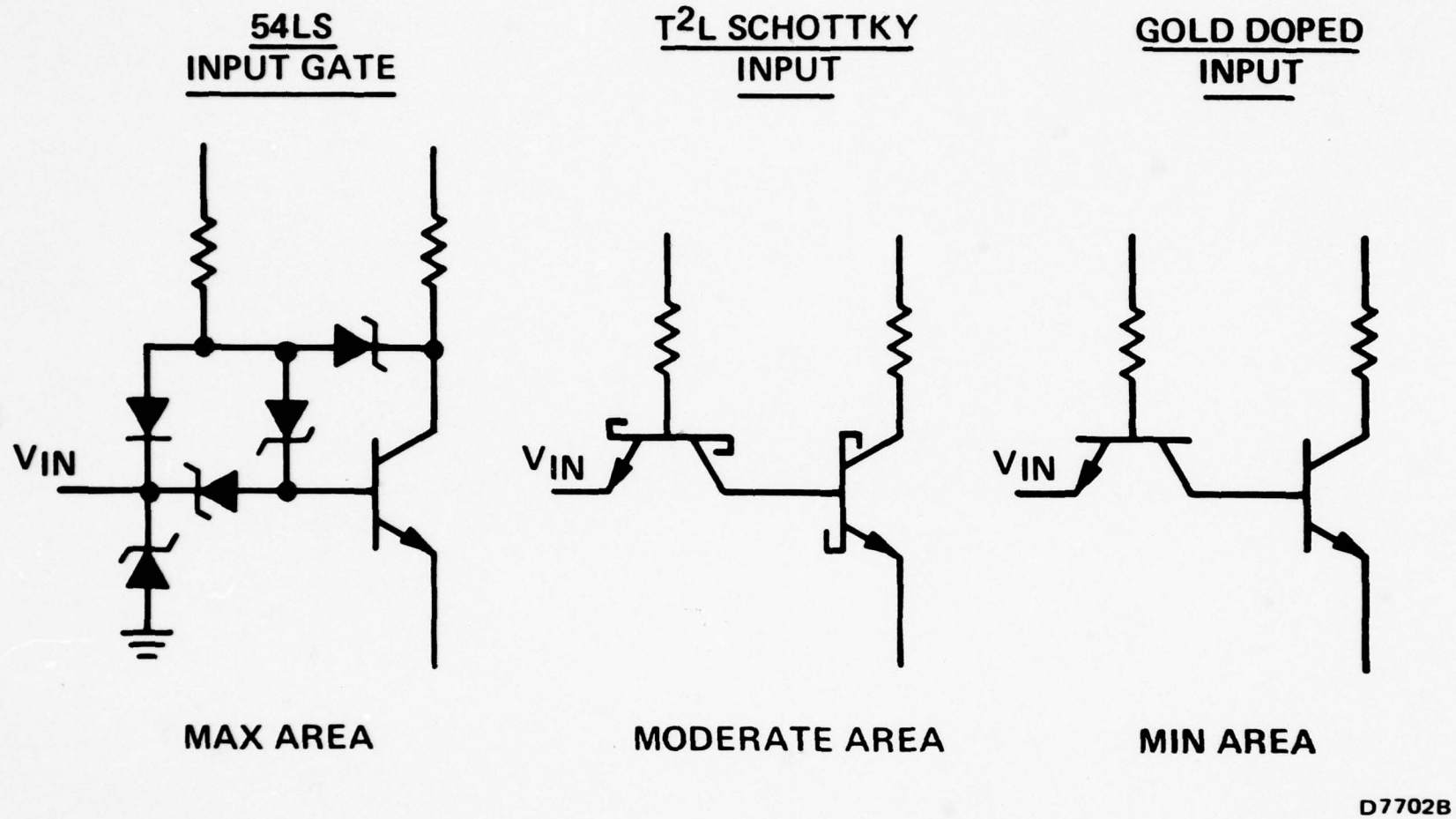


Figure 7 - INPUT GATE COMPARISON

creating a larger output device with a lower IR drop in the collector region.

$$VCE(s) = V(offset) + I_C (R_1+R_2+R_3)$$

3) 54LS04 and 54LS05

A problem common to the majority of the 54LS family of circuits (as was the conversion to Schottky technology) was believed to be an inadequate input threshold to insure noise immunity over the full temperature range. Motorola had gone to considerable effort to increase the input threshold level to 0.8 volt at room temperature to insure that the input threshold would still be greater than 0.7 volts at high temperatures. This noise immunity was achieved at the price of additional space requirements per gate, plus a need to increase gate speed to compensate for each gate triggering higher (and later) on the input waveform. The 54LS input gate structure shown in Figure 7, may be compared with other approaches.

4) 54LS08, 54LS21 and 54LS32

These circuits all required the input gate threshold changes detailed above. In addition, some minor beam-out changes were implemented to the metals mask.

5) 54LS86

The primary problem with the initial lots was inadequate speed. Functionally the design was correct and most performance (DC) characteristics were acceptable. To increase circuit throughput speed, a Schottky diode in the input structure was changed to a PN type diode. In the off-going mode the stored charge in the PN diode's diffusion capacitance acted to remove base charge from the gate transistor to be switched. This increased speed with no sacrifice in power. Additionally, two PN type clamping diodes on the input lines were removed, so that their additional capacitance would not excessively load the circuit. These corrections were successful.

6) 54LS73

This circuit exhibited a speed problem associated with the maximum toggle frequency, although the propagation speeds were in spec. This problem was particularly serious and quite difficult to fix, since it was controlled by an internal race condition between different logic elements. Considerable analysis was performed to determine if the circuit could be used adequately in its present configuration, or if a different logic realization would have to be employed which would require a complete redesign and re-layout.

Several engineering changes to the circuit were proposed to optimize performance, as listed below, and were implemented. These corrections were sufficient in increasing the nominal toggle frequency as determined in later testing of the first article units.

54LS73 Design Changes

1) Change 8K resistors to 6K (4 places)
2) Remove negative transient transistors from clock line (4 places)
3) Change Schottky diodes to PN diodes on Q & $\overline{Q}$ output to master (4 places)
4) Same as above on clock inputs
5) Change 25K resistors to 17K (4 places)
6) Change 12K resistors to 10K (4 places)
7) Change 17K resistors to 12K (4 places)

Results of testing on the first article group of devices proved that these design changes were successful.

7) 54LS138

This circuit also had the input gate diode conversion implemented as explained previously. The Schottky diodes were changed to PN diodes to increase the switching speed. In addition to these corrections, some pull-up resistors were increased in value to decrease the power consumption. One of the internal gates was also completely redesigned to achieve a lower device count.

8) 54LS193

Samples of this circuit were packaged and tested over temperature, which indicated that the present design, although functionally correct, would not pass the AC spec. requirements. Since this device was one among the group which was deleted from both first article and pilot production phases, no redesign was accomplished.

9) 54LS194

The same comments apply as to the 54LS193. This device had good DC probe yields, however, especially for one of the more complex functions. The first lot processed achieved a yield of 20 percent and the third 49 percent. The second lot was much lower (12 percent) due to experimenting with the base cycle.

10) 54LS196/7

These circuits were so large, and so complex that each required considerable changes in design and/or layout in order to fit into the predetermined chip size.

11) 54LS253

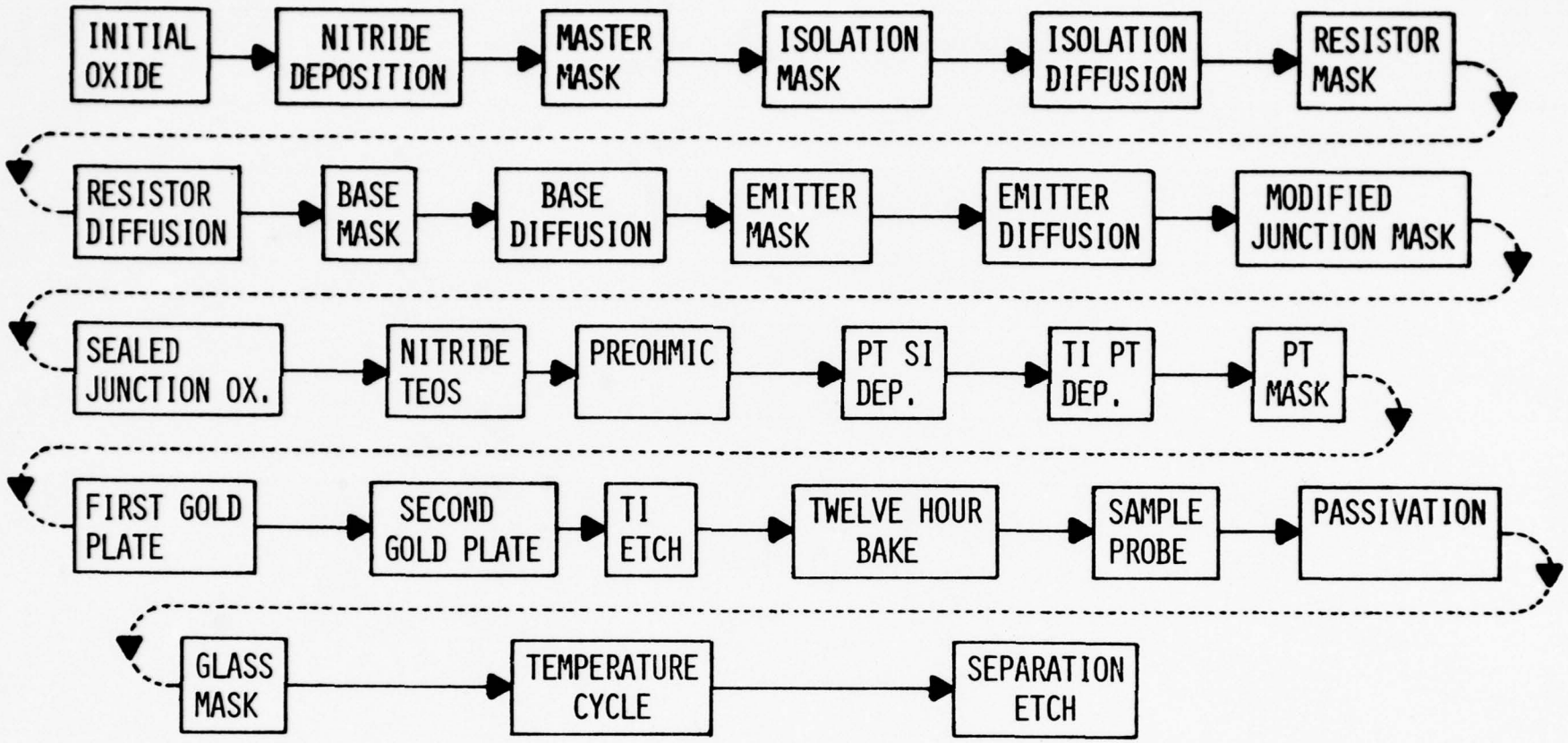
The speed-up resistors were changed from 8K to 5.5K to increase the switching speed with more current. One node was particularly slow due to excessive capacitance. Four separate transistors were incorporated into one tub to reduce the overall parasitic capacitance and thus speed-up that node. In addition, several of the internal gate output devices were enlarged to improve the driving capability.

12) RA108

The RA108 60 gate array, designed originally by Raytheon for the Patriot (SAM-D) system, provided the major challenge of the integrated circuits. The original circuit was gold doped, but Motorola elected to employ Schottky devices to achieve the necessary speed-power products, and, hopefully increase yields. However, this presented a problem in that the Schottky devices required more silicon real estate which in turn meant that metal line widths and spacings had to be reduced. Because of this, metal shorts occurred on the first article and pilot lots, although functional units were found and tested on earlier engineering lots. One minor redesign was required in changing of resistor values only, as a result of these tests.

Figure 8

STANDARD IC BEAM LEAD DEVICE WAFER PROCESSING FLOW CHART



3.2 PROCESSING STEPS

Upon delivery of the starting material having the buried layer and epitaxy, the first step in the process is the growth of approximately 5KÅ of SiO_2 over the wafers. The overall process flow is presented in Figure 8. The next step initiates the first step in what was termed master mask processing.

3.2.1 MASTER MASK

The master mask concept is a manufacturing technique that provides precision alignment, reduced device geometries and a relatively pin-hole-free process. This concept was implemented in the production of the beam lead IC's in the Federal High Rel operation for the first time on this contract. A description of the master mask process and its associated illustrations is discussed in this section.

Figure 9 - This shows the first step in the process in which a 2000 Å-thick layer of Si_3N_4 has been deposited on the initial oxide grown on the starting material.

The reason for the pin-hole protection should be evident at this first step; it would be necessary to have coincidence in pin holes in the precise location in both the nitride and oxide for diffusion or metallization shorting problems to later occur.

Figure 10 - The photoresist has been applied, exposed and developed from those areas where the nitride will be etched. These areas will later become the isolation region, deep collector, base and resistor diffusions.

Figure 11 - The Si_3N_4 has been etched through to the underlying SiO_2 which is not affected by the nitride etch (different etchants and different etch rates).

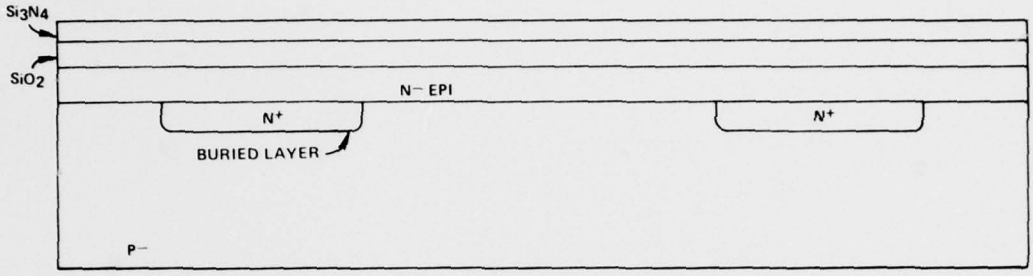


Figure 9 - STARTING MATERIAL SHOWN AFTER SI_3N_4 DEPOSITION

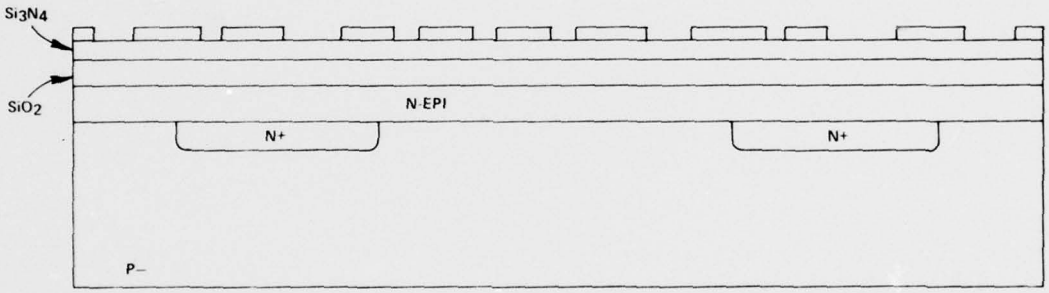


Figure 10 - PHOTORESIST EXPOSED AND REMOVED FROM AREAS WHERE NITRIDE WILL BE ETCHED

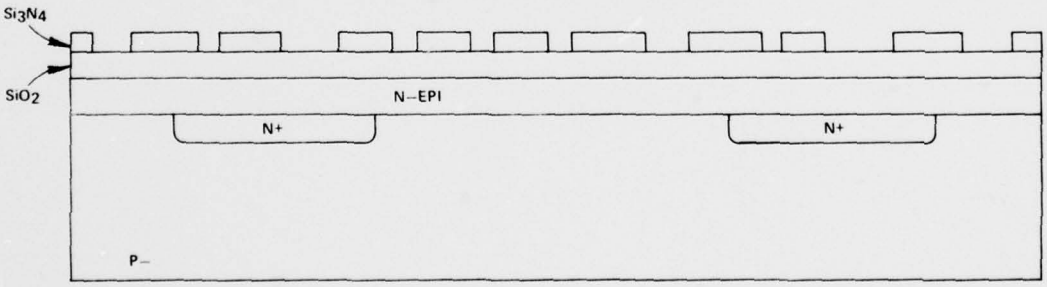


Figure 11 - NITRIDE ETCH

E1019

Figure 12 - Photoresist removed from those areas where the SiO_2 will be etched prior to diffusion of the junction isolation regions.

It should be pointed out at this point that the isolation mask, as well as subsequent diffusion masks, except for the emitter, has been designed with 0.2 mil wider openings to allow for misalignment. For example, note in this figure that the isolation (SiO_2 etch) mask has been misaligned 0.2 mil to the right. Since the oxide etchant does not attack the nitride, only the oxide will be removed. Later, (Figure 15) it can be seen that the deep collector mask has been misaligned to the left, again without any deleterious effects.

Figure 13 - The SiO_2 has been etched.

Figure 14 - Junction isolation diffusion.

Figure 15 - SiO_2 etched prior to diffusion of deep N+ collector.

Figure 16 - Deep collector diffusion.

Figure 17 - For simplicity, this shows that several processing steps have been combined; first the base and resistor diffusions have been completed, followed by the emitter diffusion. The latter is the only diffusion mask which requires critical alignment since it is not associated with the nitride master mask. This represents the final step prior to metallization.

3.2.2 MASTER MASK SUMMARY

In summary, master mask offers the following advantages:

1) Precision alignment of masks for isolation, deep collector, base diffusions and resistor diffusions.
2) Relatively pin-hole free process.
3) Reduced device geometries.

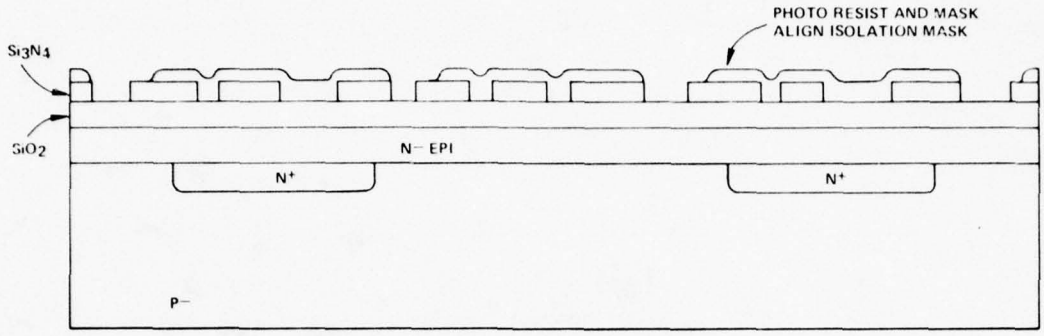


Figure 12 - PHOTORESIST EXPOSED AND REMOVED FROM AREAS WHERE SIO_2 WILL BE ETCHED

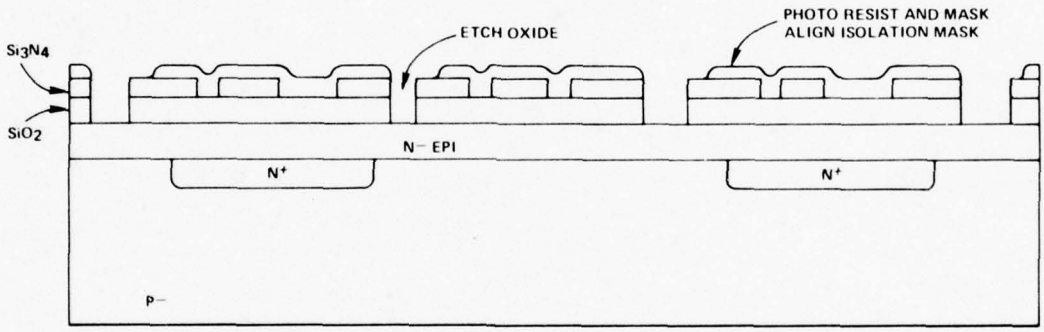


Figure 13 - SIO_2 ETCH PRIOR TO JUNCTION ISOLATION DIFFUSION

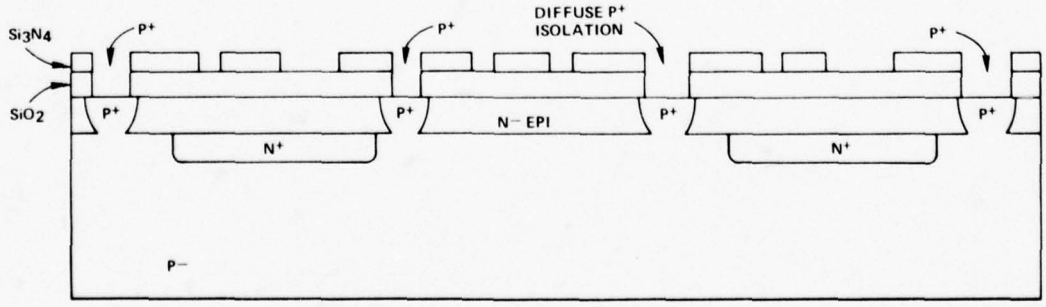


Figure 14 - ISOLATION DIFFUSION

E1021

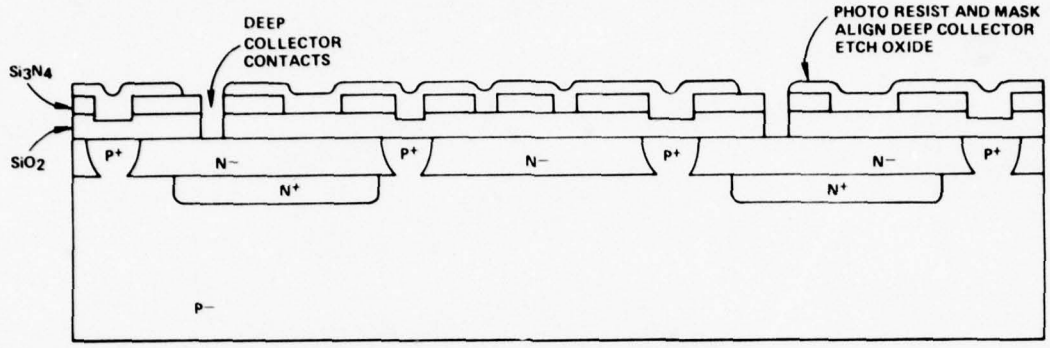


Figure 15 - SIO_2 ETCH PRIOR TO COLLECTOR DIFFUSION

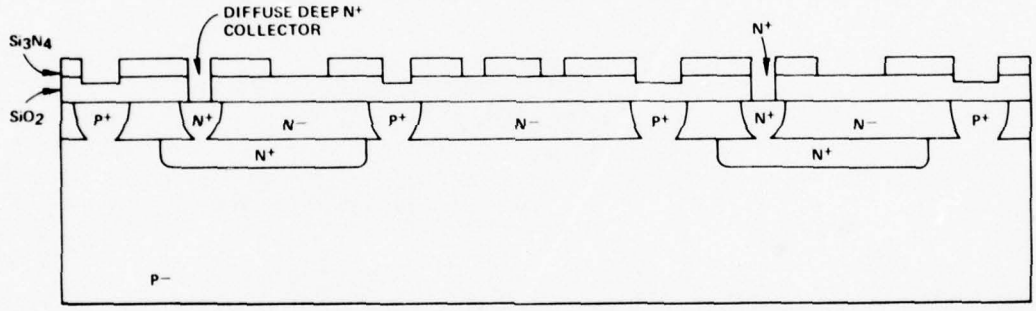


Figure 16 - DEEP N+ COLLECTOR DIFFUSION

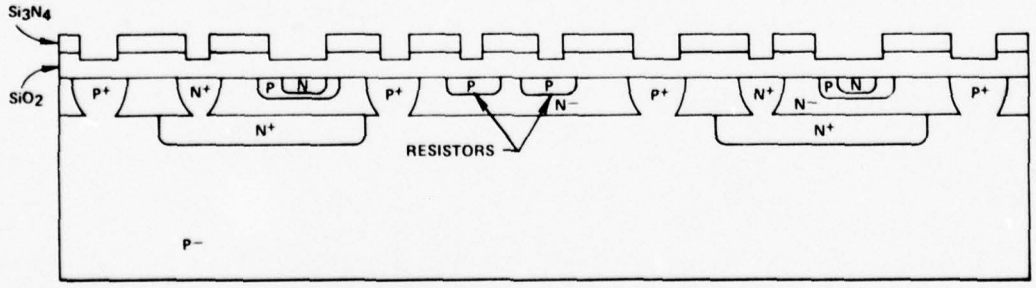


Figure 17 - BASE, RESISTOR AND EMITTER DIFFUSION

E1023

There is little doubt that the use of the Si_3N_4 master mask approach significantly improved the yields although there was no other process to compare with.

3.2.3 MODIFIED SEALED JUNCTION

Another processing improvement developed earlier which improved the yields for beam lead devices was in the sealed junction. It is important to review and compare the standard sealed junction approach, developed some years ago, with that of todays modified sealed junction.

First of all, a sealed junction means that all of the PN junctions are protected from the deleterious effects of charged ions such as sodium.

It can be seen from Figure 18 that there is a difference in the thickness of the oxide at the point where it has been etched from the preohmic vias. This variation can range from emitter or implanted resistor oxides of 3K - 5KÅ, shown on the left, to >10KÅ used as initial oxides shown on the right. It is quite evident that etching of these various oxide thicknesses will either result in underetching or overetching or both. In the case of the thicker oxides, if insufficient or underetching has occurred, a marginal or no preohmic metal will result. In the case of thin oxides a severe undercut can result. This undercut will provide a protruding nitride which can shadow the deposited metal or can in some cases uncover P-N junctions under the nitride lip. (This results in severe etching of the oxide in the horizontal plane beneath the nitride. This nitride lip can later cause problems such as breaking off. In some cases metal shorts will result at the junction of the base diffusion and epitaxial layer due to the horizontal etching of the oxide.)

To overcome this problem the modified sealed junction was developed. As can be seen from Figure 19, the original master mask nitride has been removed and the oxide has been etched from the areas where metal contact is to be made <u>prior</u> to nitride deposition. Next, as shown in Figure 20, a thin layer (500Å - 700Å) of oxide is regrown in these areas followed by a 2000Å nitride deposition.) Since this oxide is so thin,

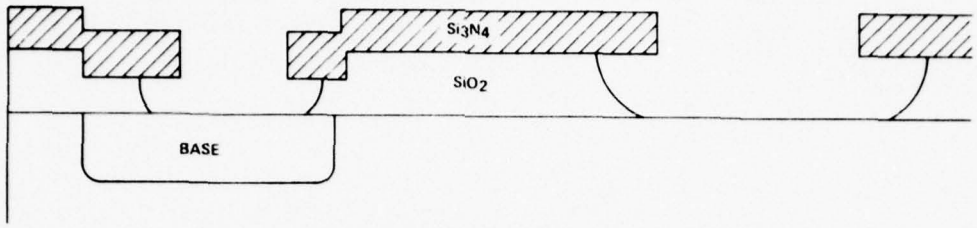


Figure 18 - PRE-OHMIC ETCH WITHOUT JUNCTION SEAL

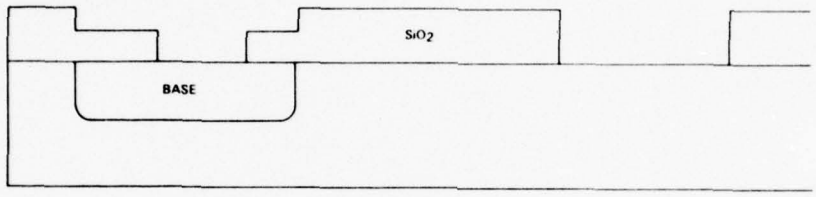


Figure 19 - JUNCTION SEAL ETCH

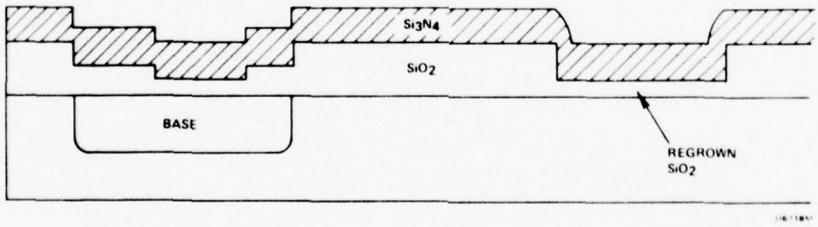


Figure 20 - OXIDE GROWTH AND NITRIDE DEPOSITION

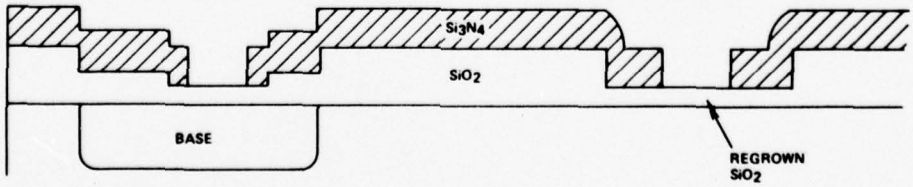


Figure 21 - NITRIDE ETCH

subsequent etching will be uniform across the wafer thus eliminating any voids in the platinum deposition which follows. The nitride and oxides are subsequently etched as shown in Figures 21 and 22 prior to metallization.

3.2.4 METALLIZATION SYSTEM

The metallization processes used by Motorola to produce beam lead devices essentially begins with the deposition of platinum to form the platinum silicide ohmic contact material within the active areas of the silicon (see Figure 23). This operation is typically conducted by processing the wafers through an R.F. sputter system equipped with a special sputter etch platen to permit in-situ sputter cleaning immediately prior to deposition of metal. Once this sputter etch has been accomplished, the exposed silicon surface areas are now as clean as possible and remain under vacuum conditions, where they are not susceptible to further contamination or oxidation. Sputter deposition of high purity platinum to a thickness of 700Å $\pm$ 300Å follows immediately after the sputter etch of each wafer platen. All wafers are subsequently removed from the vacuum system, placed into a nitrogen ambient furnace at 650°C for approximately 10 minutes. This sintering operation forms the platinum silicide as shown in Figure 24. They are then inspected for platinum silicide formation. Next the wafers are subjected to a brief chemical etch in hot aqua regia to remove unreacted platinum where it was deposited in contact with the nitride. It should be noted here that, because the platinum silicide has a protective oxide on the surface as a result of the 650°C temperature, the chemical solution does not attack the silicide material; therefore, an etch mask is not required for this operation. Further visual and electrical inspections are then performed to insure the integrity of the ohmic contact material. The wafers are then placed into a dual-target sputtering system where they receive sequential sputter-depositions of titanium to a thickness of approximately 1300Å, followed by approximately 1800Å of high purity platinum as shown in Figure 25. The wafers are inspected at this point for metallization thickness and visual quality. The surface is then covered with a positive photoresist for masking to allow further chemical processing. The masking operation defines the metal interconnect and beam pattern on the surface of the platinum unique to each part type. Again, an aqua regia solution is used to chemically remove (etch) all unwanted platinum exposed as a result of the

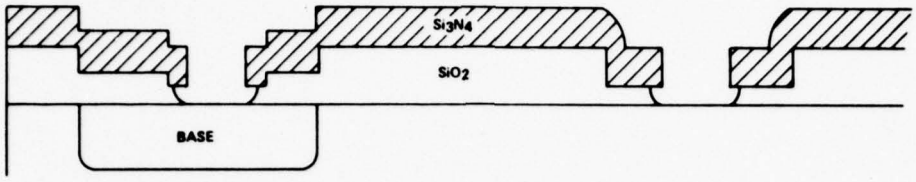


Figure 22 - TOP OXIDE ETCH

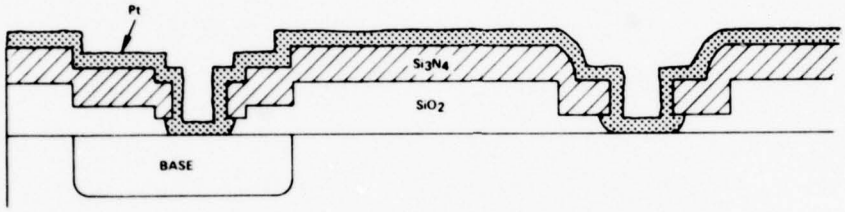


Figure 23 - PLATINUM DEPOSITION

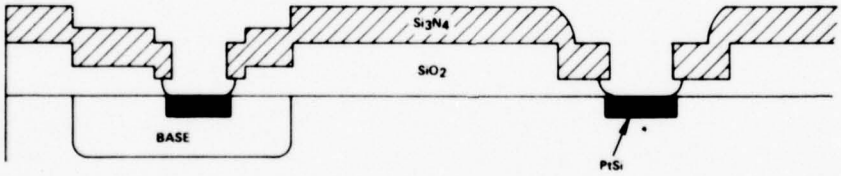


Figure 24 - PLATINUM SILICIDE

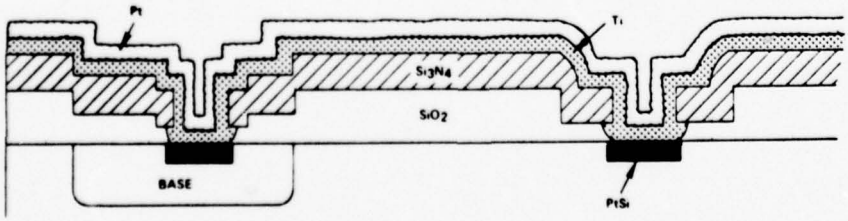


Figure 25 - TITANIUM-PLATINUM DEPOSITION

the masking operation. At this point, the wafer surface consists of patterned platinum with titanium over the entire surface. Removal of the positive photoresist, and subsequent application of negative photoresist material to define the same metal interconnect pattern now leaves the previously defined platinum exposed, and all of the titanium covered. The wafers are next gold plated to a thickness of 2-3 microns by electroplating directly on the platinum. (See Figure 26) Additional photolithographic processing is applied to expose only the beam locations in the gold pattern. The wafers are returned to the gold plating solution and the beam locations are plated with the same gold metallization to a thickness of approximately 0.5 mil. This is shown in Figure 27. Following this operation, the beam gold plating hardness is measured, and the continuous layer of titanium is removed from all areas between the interconnects and beams. Further processing operations include a 12 hour bake at 325°C in wet nitrogen, sample probe, mount and lap, separation etch, and finally glassivation. The glassivation process applies approximately 12KÅ of chemical vapor deposited glass at 450°C to provide increased reliability and metallization integrity. (See Figure 28)

3.3 PROCESSING

3.3.1 GENERAL

Processes were established for both the 5400 standard TTL series and the 54LS low power Schottky series of integrated circuits by early 1976 on this program. Some of the wafers in the first lots processed yielded up to 28 percent. Several process problems were discovered, however, and are discussed in detail in subsequent paragraphs. Overall, most of the problems encountered were easily corrected.

3.3.2 UNDERCUTTING OF TEOS ON MASTER MASK

The early lots of material processed were undercut at the master mask step, which is the first photoresist step after the epitaxial deposition. Details of the process at this point are as follows:

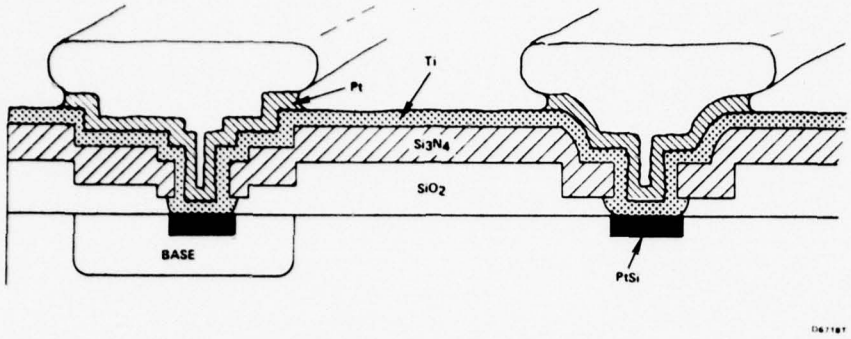


Figure 26 - THIN GOLD ELECTROPLATING

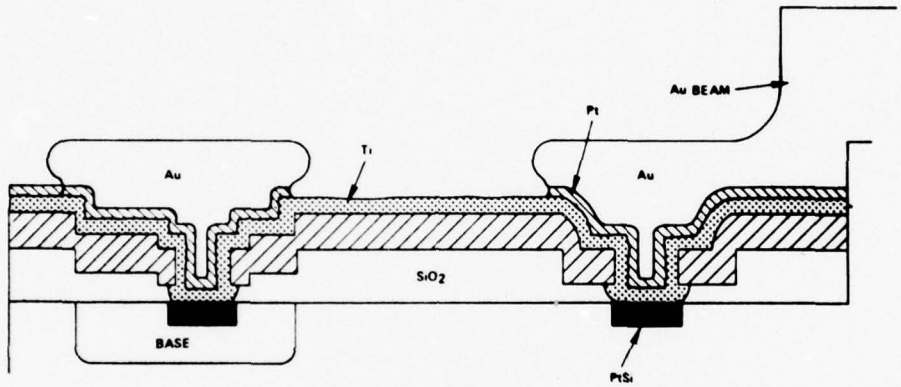


Figure 27 - THICK GOLD ELECTROPLATING

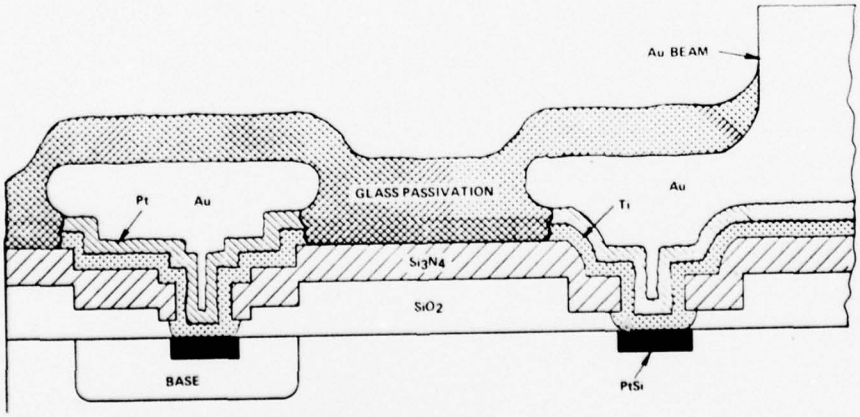


Figure 28 - GLASS DEPOSITION

The wafer structure prior to the master mask photoresist step is shown in Figure 29. After the epitaxial deposition, 3500Å of thermal oxide is grown on the wafers followed by 2000Å of silicon nitride. Next, in the original process, 3000Å of TEOS (tetraethylorthosilicate glass) was deposited.

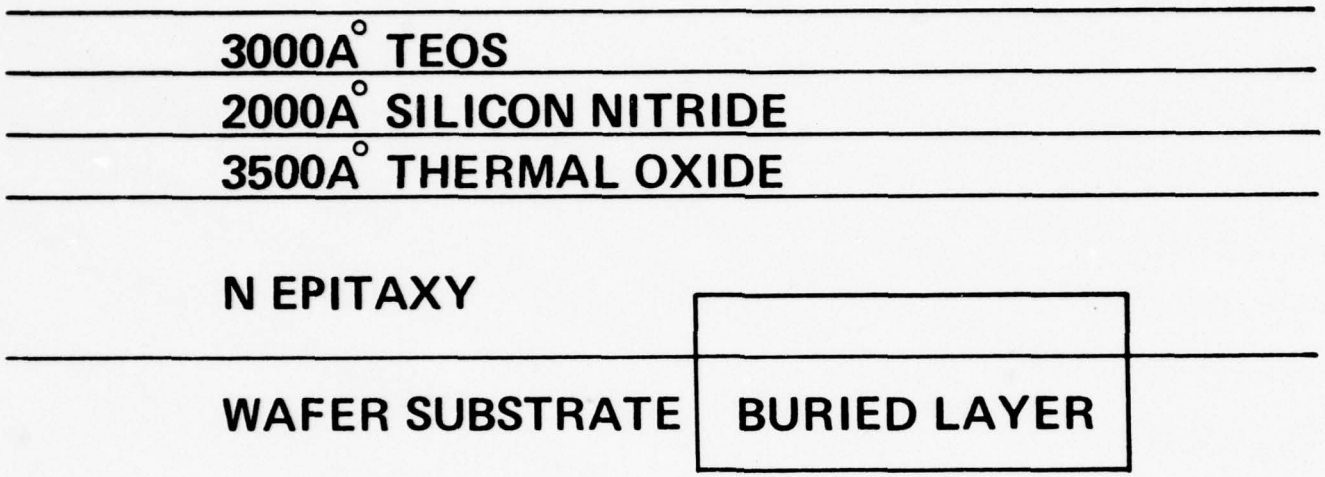
Photoresist is then applied to the wafer and patterned with the master mask, which, as discussed in Section 3.2, is a combination mask of the isolation, deep collector, base, and resistor patterns. This master mask pattern is then etched into the TEOS as shown in Figure 30. On the first lots of material, the TEOS layer undercut approximately 0.05 - 0.07 mil on each pattern edge, which reduced the isolation-to-base pattern spacing from the original design spacing of 0.4 mil to 0.25 - 0.3 mil.

The isolation-to-base spacing was further reduced by additional slight undercutting at the base pattern etch step. The space between the two patterns was sufficiently reduced so that the base and isolation diffusions touched, causing base-to-isolation leakage and non-functional devices.

The TEOS undercutting problem was resolved by the implementation of a plasma dry etcher to etch the silicon nitride layer. Normal liquid chemical etching of the silicon nitride requires 180°C phosphoric acid as the etchant. This etching corrodes and destroys the photoresist, and as a result, the TEOS layer is required as an etch mask. However, etching with a fluorine plasma eliminated the need for the TEOS (see Figure 31). This process is extremely resistant to undercutting and was implemented as a standard production practice.

3.3.3 AREAS OF NITRIDE NOT REMOVED BY PLASMA ETCHING

The plasma etch process is sensitive to small amounts of photoresist film that may be present on the wafers. In a few lots there were areas where the nitride was not removed in the plasma etcher, which was caused by a thin photoresist film. An improved photoresist develop cycle, in which the xylene spray time was increased from four seconds to five seconds, eliminated this problem.



D7076

Figure 29 - WAFER STRUCTURE PRIOR TO MASTER MASK PHOTORESIST STEP (ORIGINAL PROCESS)

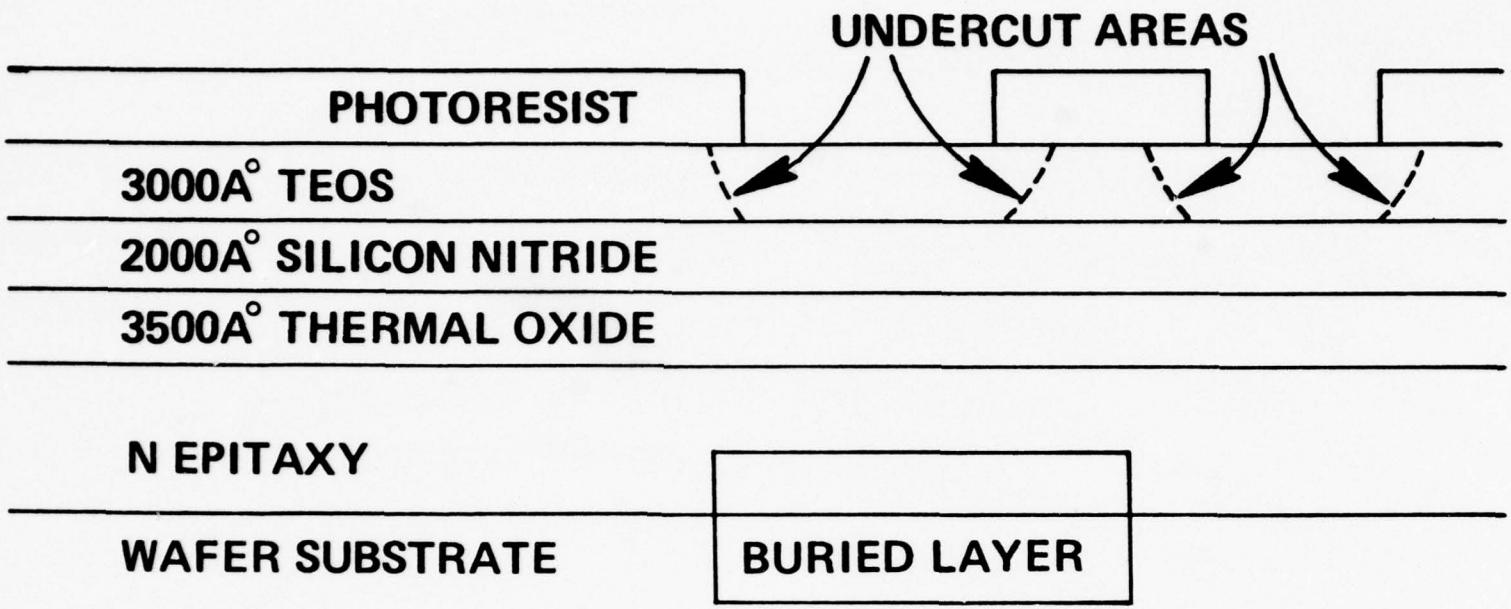


Figure 30 - UNDERCUT TEOS LAYER

D7077

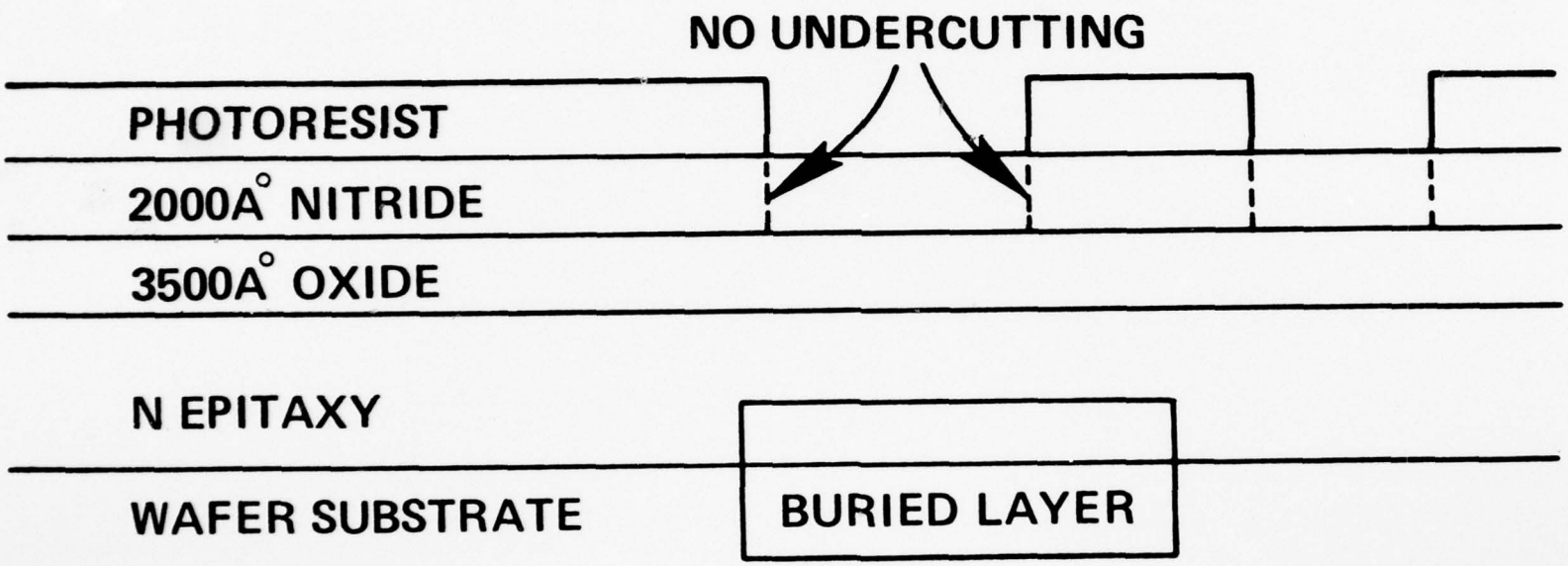


Figure 31 - NEW PROCESS USING A PLASMA ETCHER

D7078

3.3.4 UNDERCUTTING OF EMITTER OR JUNCTION SEAL PATTERN DUE TO REMOVAL OF NITRIDE LAYER

The nitride layer that is deposited for the master mask sequence is removed later in the process after the base and emitter diffusion steps. On the first four lots processed, the nitride removal etch created a wafer surface condition which caused the subsequent photoresist layer to have poor adhesion and severe undercutting. This poor wafer surface condition was corrected by immersing the wafers in a dilute hydrofluoric solution for five seconds. The additional surface preparation almost completely eliminated any subsequent photoresist undercutting.

3.3.5 LOW BASE SHEET RESISTANCE

The original base process was established with a 920°C deposition temperature. This cycle gave sporadic results, since some lots had a low base sheet resistance. The problem was corrected by the use of a 970°C deposition cycle, which provided quite uniform results.

3.3.6 PLATINUM SILICIDE IN THE GRID

Platinum silicide is formed in the grid area during sputtering when there is no protective oxide in that region. The presence of the platinum silicide in the grid resulted in incomplete die separation when the silicon was later removed from the grid area to expose the beams.

Several wafers had platinum silicide in the grid due to the removal of grid oxide from: (1) an overetch at the preohmic masking step, and (2) on excessive sputter etch prior to the platinum deposition. This second problem was largely caused by a non-uniform plasma field in the sputtering system and was subsequently corrected. The first problem of the overetch was corrected by specifying a maximum etch time.

3.3.7 CONVERSION OF SILICON NITRIDE TO OXIDE DURING DEEP COLLECTOR DIFFUSION CYCLE

It has been previously established that a silicon nitride layer will be converted into a silicon dioxide layer in the presence of phosphine during a diffusion cycle, such as the deep collector diffusion. The rate of conversion is strongly dependent on the percentage of phosphine that is present. Figure 32 summarizes the results of an experiment that was conducted to determine the proper deep collector cycle. It can be seen that the cycle that was used converts approximately 200Å of silicon nitride to oxide. This amount is only 10 percent of the original thickness of 2000Å, and the remaining nitride of 1800Å is sufficient for all subsequent steps.

3.3.8 RESISTORS

Previously, all of the 54LS circuits were designed assuming a ±50 percent resistor variation. This presented no problems on the gates or small MSI functions such as flip-flops and decoders. However, as the 54LS family grew in complexity, it became necessary to tighten the design values for the resistors. This was accomplished by converting to ion implanted resistors with ±30 percent tolerances.

Figure 33 graphically shows the affect of this new tighter resistor tolerance. The first curve (A) reflects the affect of shifting the resistor resistivity to a more optimum design center such that DC parametric conditions remain in spec. The shaded portion shows the variation no longer experienced with the tighter tolerance. AC characteristics are largely due to resistor values. The ±50 percent shift can result in as much as a 2-to-1 change in speed (reduction in prop delay or increase in toggle frequency). It can readily be seen that if Motorola had not converted to the ion implanted resistor more than 50 percent of the devices would have failed specifications.

The second curve (B) shows the affect of moving the design center of the ±50 percent resistors to the same place as that of the ±30 percent resistors. The shaded areas reflect that portion which

DIFFUSION CYCLE (MINUTES)	DIFFUSION TEMPERATURE	FLOW OF 10% PHOSPHINE GAS THROUGH DIFFUSION TUBE	PERCENTAGE OF PHOSPHINE	THICKNESS OF NITRIDE CONVERTED TO OXIDE
0 – 30 – 10	1050°C	90 cc/min	0.34%	1240 A°
0 – 30 – 10	1100°C	8 cc/min	0.032%	330A°
3 – 20 – 10	1100°C	8 cc/min	0.032%	200A°

COMPLETE CYCLE PRESENTLY BEING USED –

3 – 20 – 3 MINUTES AT 1100°C PHOSPHINE DEPOSITION (0.032% PH_3)

40 MINUTES STEAM, 10 MINUTES O_2 at 900°C.

CONVERTS APPROXIMATELY 200A° OF SILICON NITRIDE TO OXIDE

(10% OF ORIGINAL THICKNESS OF 2000A°)

Figure 32 - CONVERSION OF SILICON NITRIDE TO OXIDE DURING DEEP COLLECTOR DIFFUSION CYCLE

7073

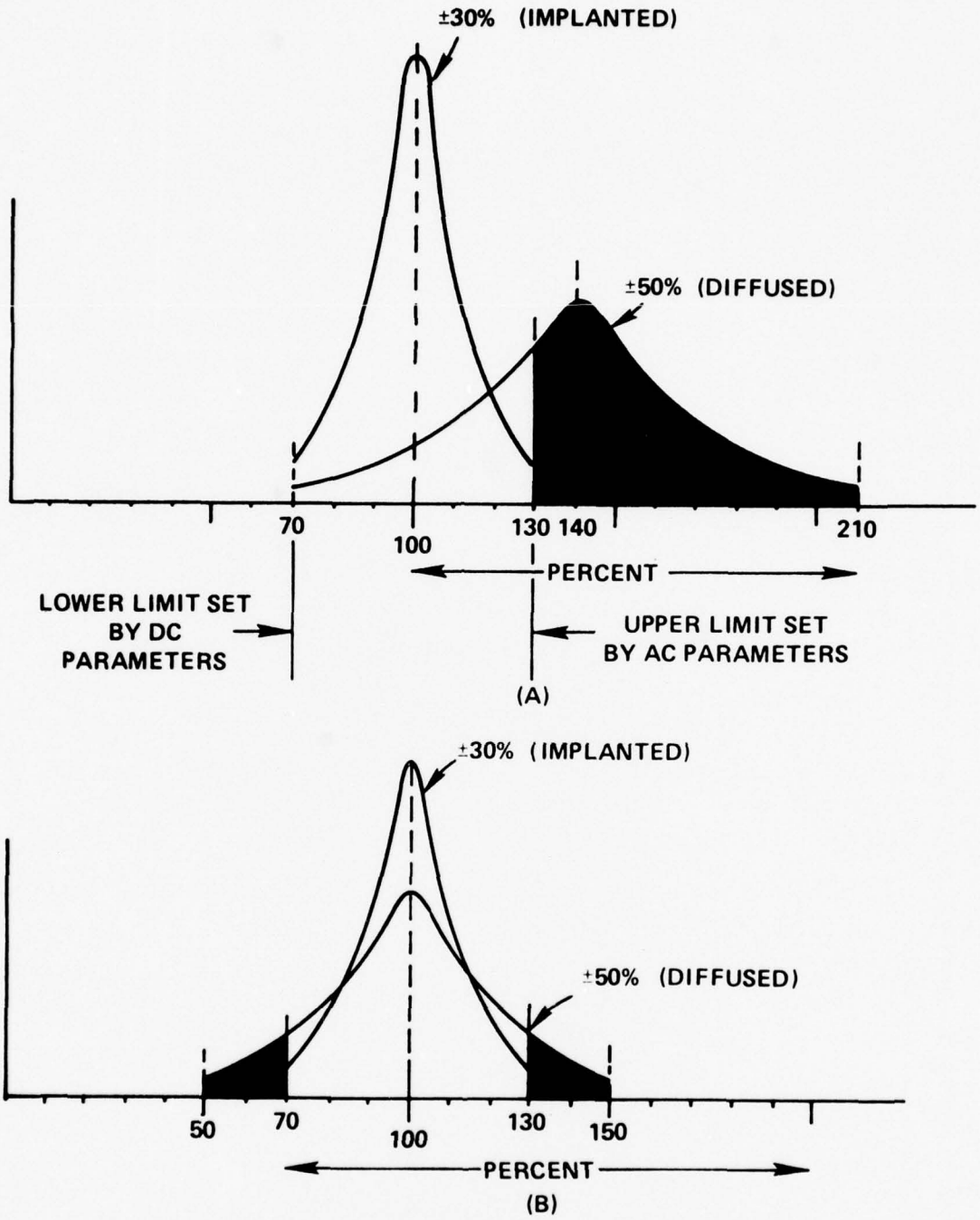


Figure 33 - GRAPHICAL COMPARISON OF DIFFUSED VS. ION IMPLANTED RESISTORS

D7982B

D7982B

would be out of spec either DC or AC. As can be seen, about 10 percent would fail DC and 10 percent would fail AC, representing a 20 percent yield loss compared to a greater than 50 percent yield loss for the first case.

3.4 SUMMARY

As discussed in Section 1.0 the yield goal for the IC's and RA108 was 10 percent and 5 percent respectively, but there was an added incentive for achieving a 20 percent overall yield. This included wafer breakage, wafer losses through processing errors, DC probing and die high power visual screening. All of these counted toward yield losses.

To be successful, wafer yield goals, probe yield goals and die high power yield goals were established early in the program as shown in Table XI. All of these yield goals (wafer throughput, probe and visual inspection) when multiplied together equal the overall contract yield objectives.

As also discussed in Section 1.0, the contract was modified deleting all but the 5404 and RA108 IC's from pilot production. Therefore, it will never be known whether the contractual yield goals would have been met. Certainly there would have been little trouble on most of the IC's provided no major processing errors occurred, since the 5400 and 54LS processes had been well established.

It is doubtful that the higher yield incentive of 20 percent would have been achieved on some of the more complex functions. However, the 10 percent goal probably would have been met.

As stated, the only standard IC required for pilot production was the 5404, and the results are as shown in Table XII. It can be seen that even the incentive yield goal of 20 percent was exceeded. Also previously mentioned was the fact that the RA108 yielded no good die due to metallization shorts.

TABLE XI

IC YIELD GOALS

	5400 and 54LS Integrated Circuits (%)	RA108 60 Gate Array (%)
Wafer Yield Goals	70	70
Probe Yield Goals	26	15
Die High Power Yield Goals	55	48
Overall Contract Yield	10	5

Overall Contract Yield = Wafer Yield X Probe Yield X Die High Power Yield

TABLE XII

YIELD GOALS VS. ACTUALS ON 5404 DEVICES

	GOAL*	ACTUAL
Wafer Yield	70	100
Probe Yield	26	47.3
Die High Power	55	82.7
Overall Yield	10	39.1

*From Table XI

4.0 FEDERAL HIGH REL WAFER PROCESSING EQUIPMENT

4.1 WAFER PROCESSING EQUIPMENT

This section identifies the equipment used in the wafer processing area and is listed in Table XIII.

Figure 34 - Brute flatzone diffusion furnace control panel.

Figure 35 - Brute diffusion furnace loading station.

The diffusion furnaces used are capable of 450°C to 1250°C temperatures with control limits of less than ± 1°C. Typical gases used are oxygen, nitrogen, hydrogen, and hydrogen chloride. Diffusion impurities are introduced into the furnace in either vapor, gaseous or solid state form. In specialized cases vacuums are utilized.

Figure 36 - Cleaning station in the diffusion area.

Figure 37 - Electrical test stations.

The type 576 curve tracer shown is a dynamic semiconductor tester which allows display and measurement of characteristic curves of a variety of two- and three-terminal devices. This includes bipolar transistors, MOS FET's, SCR's and unijunction devices. A number of possible measurements is available.

The C-V equipment is used to determine both the fixed charges in the oxides produced during processing, and the amount of mobile ions which may be introduced during cleaning or diffusion steps.

TABLE XIII

WAFER PROCESSING EQUIPMENT

EQUIPMENT DESCRIPTION	QTY	MANUFACTURER	MODEL #	PROCESS APPLICATION
I. DIFFUSION AREA				
Diffusion Furnaces	22	Thermco	Pacesetter III	Various Diffusions & Oxidations
Diffusion Furnaces	6	Thermco	Brute American	Diffusion & Oxidations
Rinser Dryers	2	Corotek	Cor II-D	Wafer Rinser-dryer
4-point probe	2	Veeco	FPP-100	Resistivity Measurements
Ellipsometer	1	Applied Materials	AME-500	Oxide Thickness Measurements
In-Process Probes	4	Motorola/ Tektronix	576	In-Process electrical probing
CV Plotter	1	Princeton Applied Research	410	Oxide stability
II. PHOTORESIST AREA				
Photoresist Coater	1	GCA	6605	Automatic photoresist coater
Developer	1	GCA	7405	Develop photoresist
Scrubber	1	Kasper	CII-1WS-2-1	Wafer Scrub Clean
Bake Ovens	4	Pacific Combustion	PCE-100	Photoresist bake
Plasma Asher	1	Tegal	200	Plasma Photoresist removal
Plasma Etcher	1	Tegal	200	Oxide & Nitride etcher
Plasma Etcher	1	I.P.C.	4005T-1813SCT	Metal, oxide & nitride etcher
Plasma Asher	1	Ionized Gas Tech.	1500	Plasma Photoresist removal
Alignment systems	5	Kasper	2001	Mask — wafer alignment systems
III. METALLIZATION AREA				
Sputtering System	1	MRC	902	Metals sputtering
Sputtering System	1	MRC	903	Metals sputtering
Rinser Dryer	4	Fluoroware	K-10	Wafer Spin Dryer
Alloy Tubes	4	Lindberg	59754	Alloy and sintering
Sputtering System	1	MRC	S3007B-RF	Metal Sputtering
Sputtering System	1	Perkin-Elmer	3038	Metal Sputtering
Sputtering System	1	Perkin-Elmer	2038	Metal Sputtering
Evaporator	1	NRC	3110	Gold evap. E-gun
Evaporator	1	Edwards	E19E	Alum. evap. 2 E-guns
Evaporator	1	NRC	2759	Gold evap. Fil.
Plating Bath	1	Motorola	—	Gold plating
Passivator	2	Applied Materials	Silox 1200	Deposit passivation glass

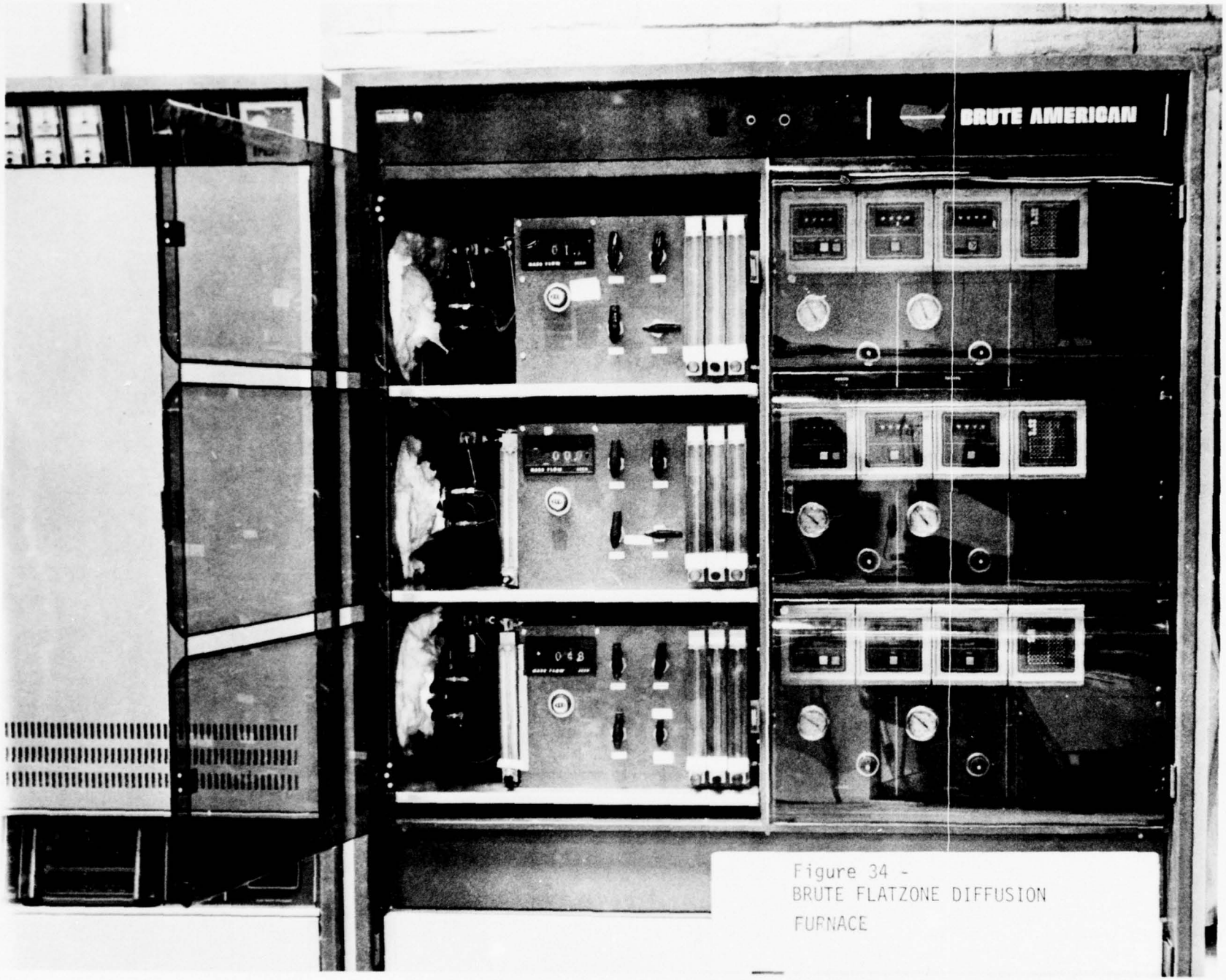


Figure 34 -
BRUTE FLATZONE DIFFUSION
FURNACE

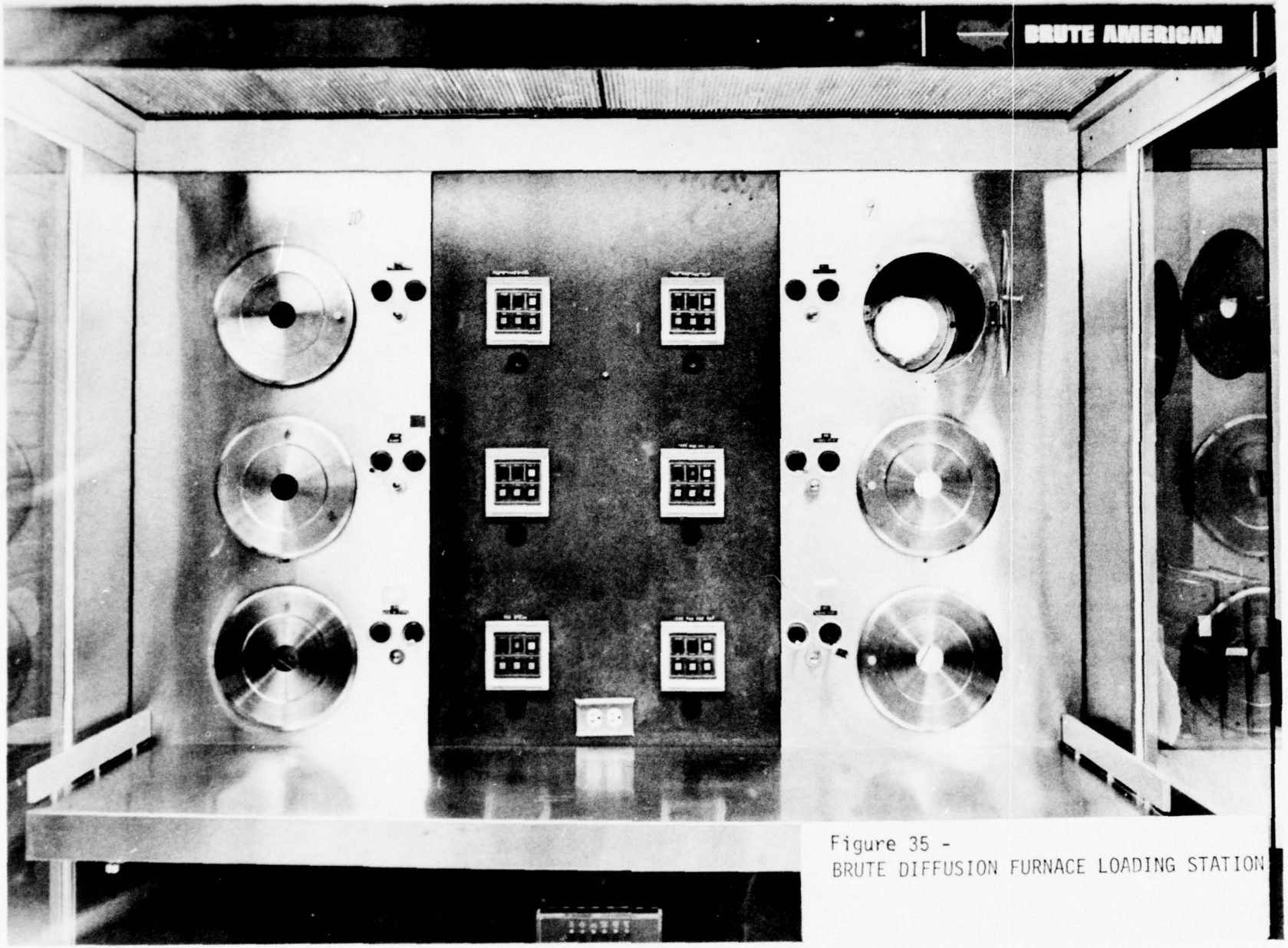


Figure 35 -
BRUTE DIFFUSION FURNACE LOADING STATION

Figure 36 -
CLEANING STATION IN DIFFUSION AREA

Figure 37 -
ELECTRICAL TEST STATIONS

Figure 38 - Kasper 2001 alignment tool.

The Kasper 2001 alignment tool is a precision instrument for the alignment and exposure of photoresist patterns. Wafers are automatically loaded from a casette. Alignment tolerances to a previous pattern of less than 0.1 mil are routinely attained. The lens system is capable of exposing a three-inch diameter wafer with a light intensity variation of less than 5 percent.

Figure 39 - III wafer scrubber.

The III wafer scrubber employs a rotating brush to mechanically remove particulate contamination from the wafer surface. The wafer is then rinsed and spun dry. The operation is fully automatic, with casette loading and unloading.

Figure 40 - GCA four-track coater/spinner.

The GCA coater/spinner is presently set up to spin both positive and negative photoresists. The operation is completely automatic, with casette loading and unloading, and all machine functions such as spin speeds, times and acceleration rates are computer controlled.

Figure 41 - IPC plasma etcher/asher.

The IPC plasma etcher/asher is capable of etching silicon nitride, silicon dioxide, platinum, and silicon in an RF-induced plasma gas. It is also used to remove photoresist. The plasma etcher employs a heater and temperature controller for an accelerated and uniform etch rate.

Figure 42 - Nikon surface-finish microscope.

The Nikon surface-finish microscope, equipped with a micrometer and digital readout, is used for the precision measurement and control of wafer pattern geometries. The instrument is capable of measuring within $\pm$ 10 millionths of an inch. Critical dimensions on any

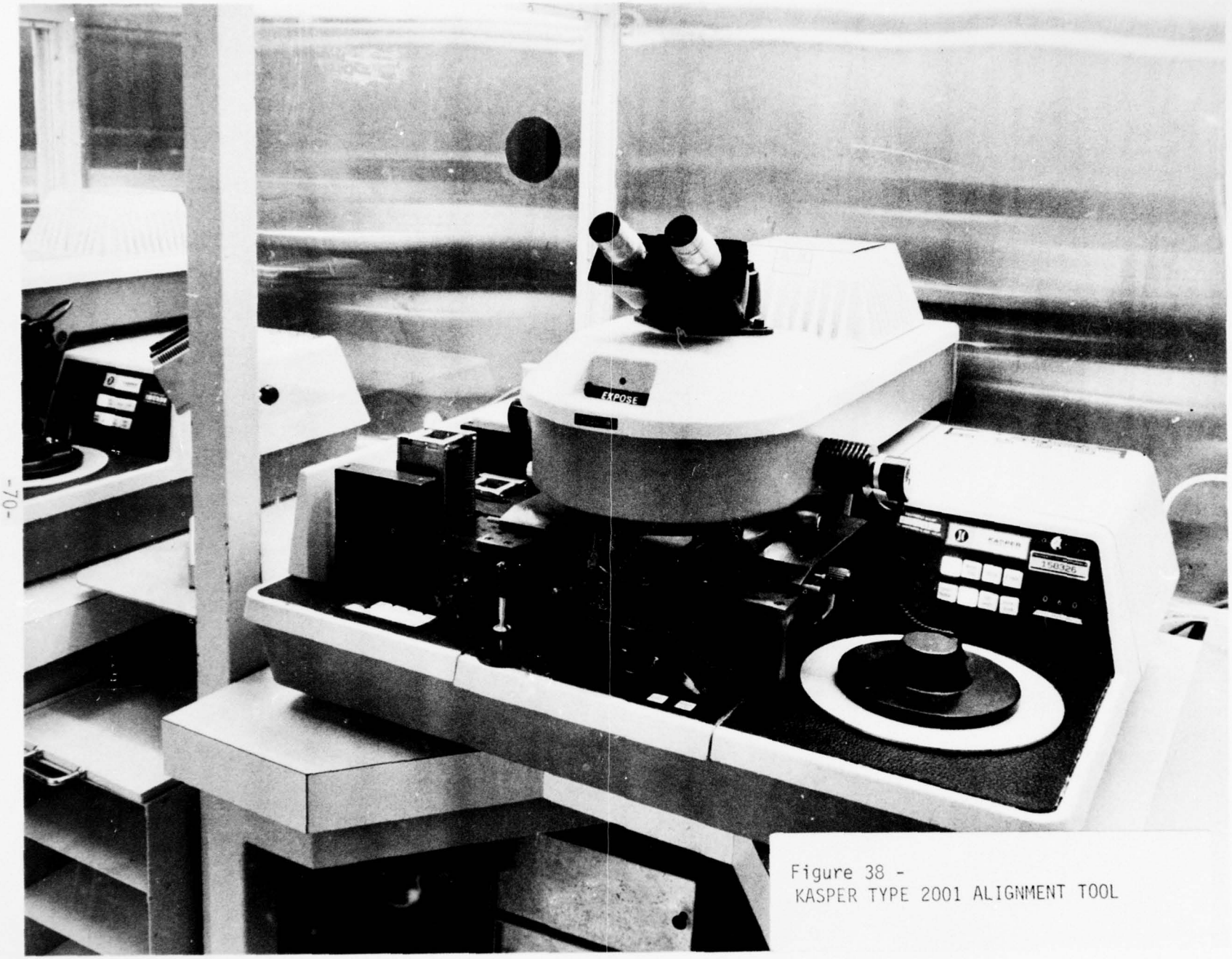


Figure 38 -
KASPER TYPE 2001 ALIGNMENT TOOL

Figure 39 -
III WAFER SCRUBBER

Figure 40 -
GCA FOUR-TRACK COATER/SPINNER

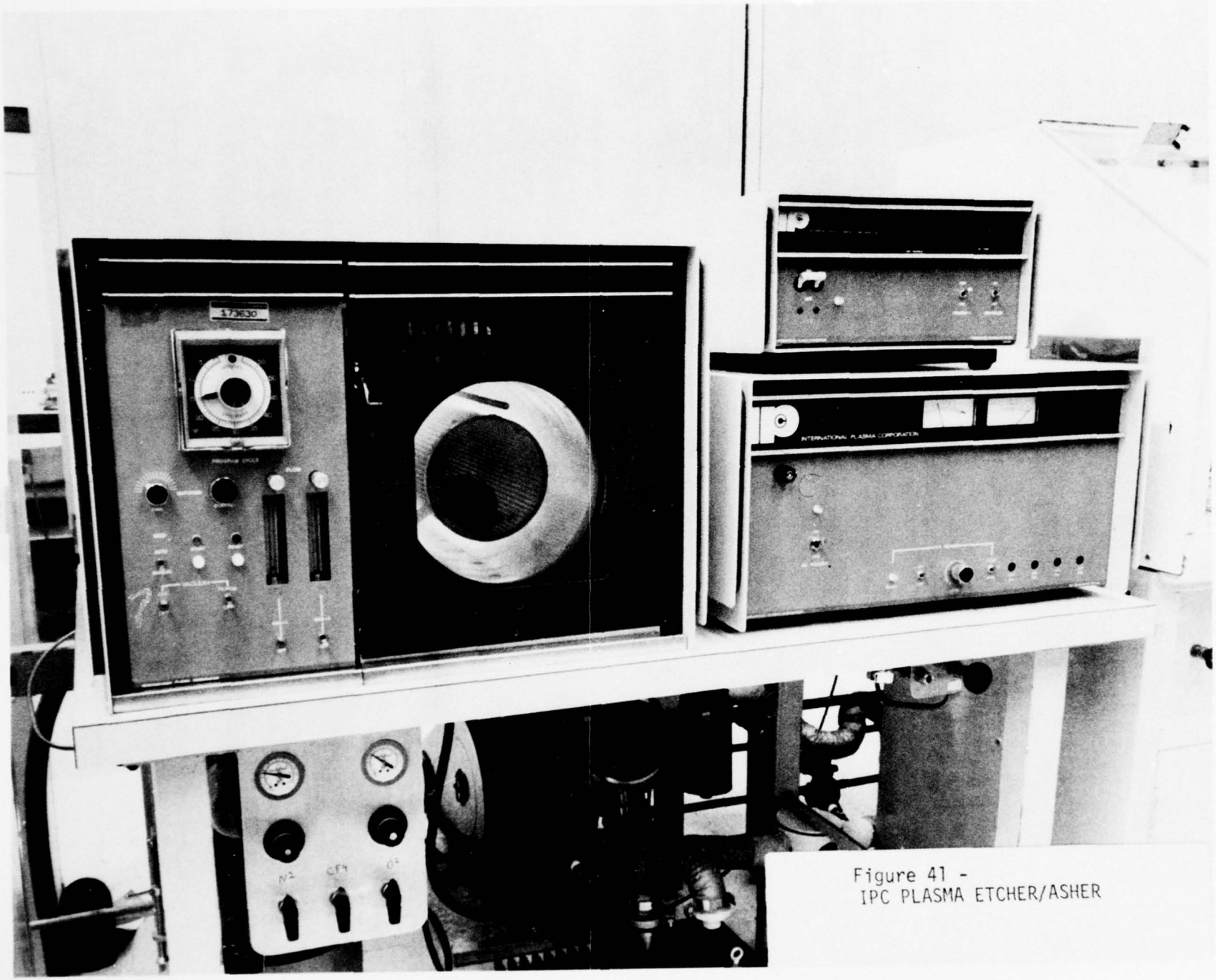


Figure 41 -
IPC PLASMA ETCHER/ASHER

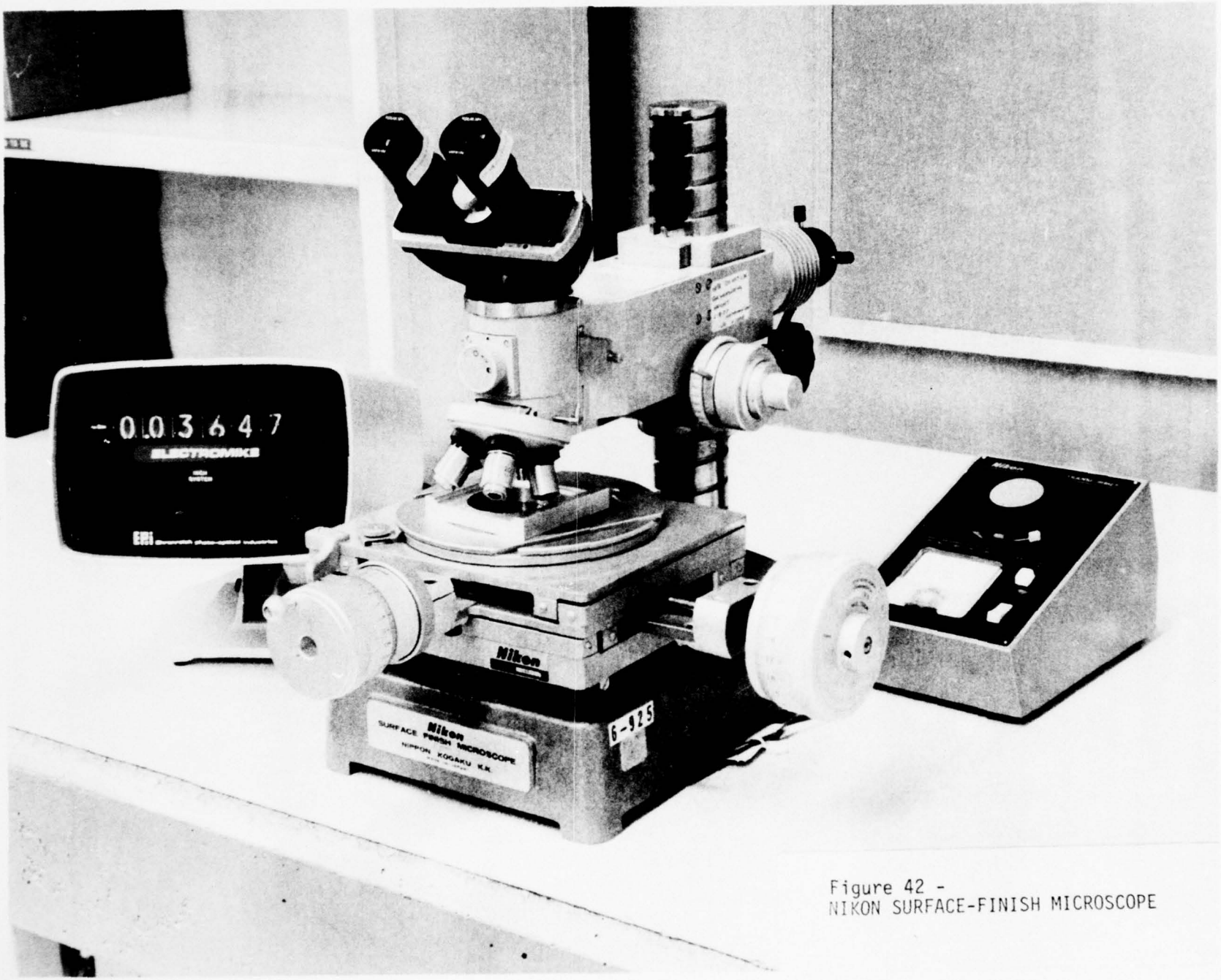


Figure 42 -
NIKON SURFACE-FINISH MICROSCOPE

mask or wafer pattern are easily measured and controlled through the use of this tool.

Figure 43 - MRC-903 inline metallization sputtering machine. The MRC-903 is capable of high rate sputtering with excellent concentration control of ±5 percent uniformity, and reproducibility of thicknesses from run to run and across the pallet of thirty-two 2 1/4-inch wafers, every 15 minutes.

4.2 WAFER PROCESSING CONTROLS

Detailed below are the various steps and controls which ensure a rapid feedback of information alerting the engineering group when any step in the process is out of control.

1) All diffusion furnaces are profiled and documented weekly; some more often, depending upon specific process.

2) Diffusion furnaces cleaned at different intervals depending upon application.

3) Gas flows checked daily.

4) Deionized water initial purity is 18 meg-ohms; wafers are rinsed after chemical processing until purity reaches a minimum of 12 meg-ohms.

5) All test and measuring equipment is calibrated in accordance with MIL-M-38510 by a special instrumentation group.

Figure 43 -
MRC-903 INLINE METALLIZATION
SPUTTERING MACHINE

5.0 FIRST ARTICLE AND PILOT PRODUCTION DEVICE PROBE RESULTS

Table XIV lists the devices required (as modified by the contract) for first article and pilot production phases of the contract along with yield results.

TABLE XIV

FIRST ARTICLE AND PILOT PRODUCTION DEVICE PROBE YIELD RESULTS

FIRST ARTICLE				PILOT PRODUCTION	
DEVICE	PERCENT PROBE YIELD	DEVICE	PERCENT PROBE YIELD	DEVICE	PERCENT PROBE YIELD
1N746	20.0	LS04	60.1	1N746	10.0
2N3725	10.2	LS08	46.0	2N3960	0.0
2N3960	63.9	LS21	52.8	2N4260	3.3
2N4260	40.1	LS32	66.5	5404	47.3
2N5115	0.0	LS73	57.6	RA108	0.0
5400	52.8	LS74	39.4		
5401	39.7	LS86	65.4		
5404	61.3	LS138	22.4		
5405	59.9	LS253	59.9		
5410	60.5	RA108	0.0		
5473	55.0				

NOTE: The 5404 pilot group yielded an overall total of 39.1 percent through Die High Power Visual Inspection. This was the only device of the five required to successfully achieve the programs yield goals. A photomicrograph of this device is shown in Figure 44.

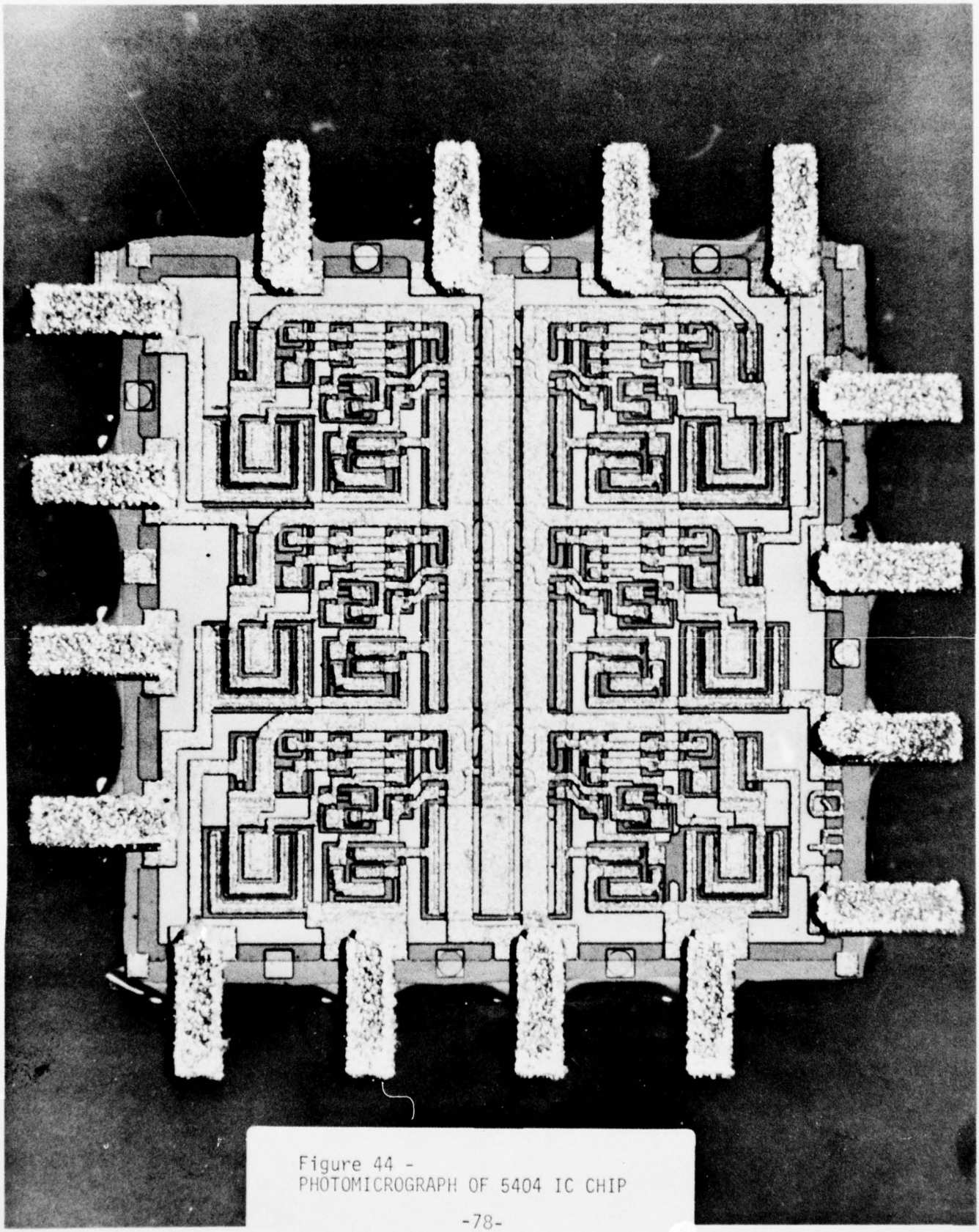


Figure 44 -
PHOTOMICROGRAPH OF 5404 IC CHIP

6.0 QUALIFICATION PROGRAM

The original contract required qualification testing of both first article and pilot procution devices on all 35 part types. By mutual agreement this was later changed so that testing would only be required once, and it was optional whether the samples would be selected from the first article or pilot groups of devices. Furthermore, only five device types were required for qualification testing; those which were to continue on into the pilot production phase are as follows:

1N746
2N3960
2N4260
5404
RA108

As discussed in previously, there were no good RA108 die from either the first article group or from pilot production. Therefore, no qualification program was conducted on this device type.

All of the devices in the four qualification lots successfully passed Groups A, B and C-1 testing and subsequently Group C-2 as listed in Table XV.

TABLE XV

QUALIFICATION TESTING OPERATING LIFE SUMMARY

Device	Lot No.	Quan.	Time On	Date On	Date Off	No. Failures
1N746	FM108	80	4:00 P	8/1	9/4	1
2N3960	FM87	80	11:37 A	8/3	9/16	0
2N4260	FM63	82	12:41 P	7/28	9/10	0
5404	915A0	82	2:40 P	8/10	9/21	0

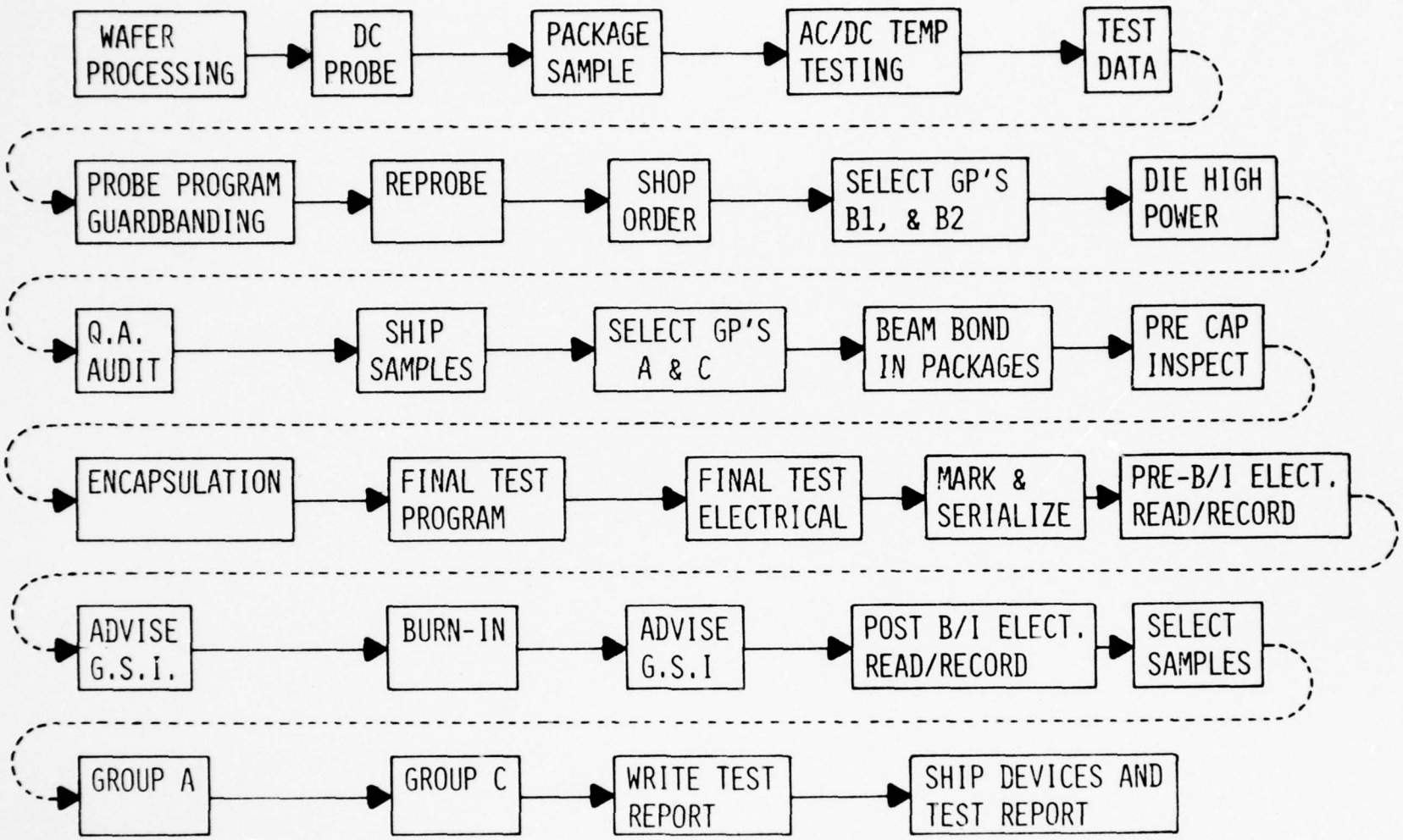
One failure was allowed for each Group C lot.

NOTE: Because of a malfunction to the furnace on one weekend, the first four lots, which were in that oven, were retained on life test two additional days.

Figure 45 shows the flow of material, after leaving wafer processing, required to successfully conduct a qualification program.

Figure 45

MM&T OVERALL FLOW CHART FOR QUALIFICATION TESTING



7.0 SUMMARY AND CONCLUSIONS

7.1 DISCRETE DEVICES

7.1.1 SUMMARY

It became evident soon after some of the discrete devices had been processed that these offered the greatest challenge to a successful program. This has been mentioned previously in numerous reports and contract reviews.

Each discrete device is unique in its processing requirements; each must be targeted (from a processing standpoint) for selection from what would normally be a family of devices in a standard chip-and-wire production line. One prime example was the 1N5314, which is only one of some thirty regulators, and falls at the end of the distribution curve.

Any variation in diffusion times, temperatures or other processing variables on any of the discrete devices meant that the specific device type might yield low, whereas some other device in the family might yield quite high. Furthermore, this occurs on the same wafer, i.e. many device types from the family will yield on every good wafer. This happened many times on many of the device types, but did not count toward total yield.

As discussed in Section 2.0, manufacture of all of these devices is further agggravated by the beam lead process, especially where the deep collector diffusion causes outdiffusion of the substrate which results in parameter characteristic changes.

7.1.2 Conclusion

Motorola was not successful in achieving the (20 percent) yield goal on any of the discrete devices. Quite possibly some of them could and would have met and even exceeded this goal (the 2N3960 first article lot probed to a 63.9 percent), but this would have been as much

through luck as through rigid process controls. Although the results were disappointing, certainly a lesson was learned: it is not practical to expect to consistently achieve high yields on a specific beam lead discrete device from a family of devices. Furthermore, it is most impractical to expect this of one single processing lot (pilot production) with all of the variables that can and do change the device characteristics.

7.2 INTEGRATED CIRCUITS

7.2.1 SUMMARY

Although a few good RA108 60 Gate Array devices yielded from the third engineering lot, none were good on either the first article or pilot production groups. Most of these latter two lots failed due to metallization shorts, because of the very narrow line widths and spacings.

The original design/process employed gold doping to reduce lifetime whereas Motorola elected to design with Schottky devices. This required additional devices for each cell and obviously increased the cell size. Since the chip size was already established, in order to fit all of the circuitry on the chip, the metal line widths and spacings had to be limited. This resulted in the metal problems which caused the zero yields.

In most cases the 5400 and 54LS devices achieved very respectable yields, (refer to Table XIV) even on the more complex functions. One reason for the high yields, when compared with the discretes, is that integrated circuit processing is, for the most part, more forgiving. Variations in diffusion times and temperatures are not as critical since most of the electrical parameters have much broader ranges than the discretes.

7.2.2 CONCLUSIONS

There is little doubt that Motorola would have been successful in achieving the yield goal of 10 percent on most, if not all, of the IC's and in most cases would have exceeded the 20 percent yield incentive. The primary reasons are (again compared to the discretes): (1) The 5400 and 54LS processes were well established since so many lots of material were processed and, (2) the IC processes are more forgiving.

Whether the RA108 would have been successful remains in doubt; however, the metal problems most probably would have been resolved had a few more lots been processed.

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8.0 PROGRAM SUMMARY

Although there were some disappointments on this program, especially with the discrete devices, in the final analysis there were more positive results than negative.

Processes and controls were established on the IC's after only some twenty lots of material had been processed, although this represented the first 54LS junction isolated material ever processed by the Federal High Rel operation. Yields were significantly higher than first thought possible.

Although this effort was, for the most part, terminated, and the requirements for beam lead devices all but disappeared, much was learned from this program. Some of the technologies advanced were adopted by other production groups of Motorola thereby enhancing their capabilities and yields. In final summary, Motorola believes this was a most beneficial program.