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INTERFACE DESIGN OF VIDEO TERMINALS

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This Interim Technical Report describes the progress for the 1 April 1976 to March 1977 period of Phase I of the Interface Doping of MNOS program.

Use of Cr, W, Pt, Ni, Pd and Ir as interface dopant in monolayer quantities between an oxide layer of Fowler-Nordheim tunneling thickness and 300-500A of Si_3N_4 gives MNOS memory retention of electrons of many centuries even at elevated temperatures, while retaining high write speed. Endurance is limited to 10^3 write/erase cycles.

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SECTION I

INTRODUCTION

Interface doping of dual dielectric charge storage cells of the IGFET types was introduced by Kahng et al.[1] and Thornber et al.[2] in 1974. In this method, a layer of metal, such as tungsten, usually less than a monolayer thick, is placed between a thin silicon dioxide film (first dielectric), which is grown to a thickness of the order of 100A thick on silicon, and an alumina or silicon nitride film (second dielectric), which is of the order of 400A thick. This was followed by an aluminum film, to make up the MAOS or MNOS structure. It was established by Kahng et al. that the dopants act as trapping sites for charge injected from the silicon. Charge is injected into these sites from the silicon under the influence of a high applied field. Here the charge motion mechanism is by Fowler-Nordheim tunneling, rather than by direct tunneling, which is the mechanism which operates for the conventional, thin oxide dual dielectric storage cells (Fig. 1). The principal differences between the conventional and the interface doped device are:

1) The stored charge is separated from the silicon by a much thicker oxide film,
2) The stored charge resides principally at the dopant sites, and not 100-200A inside the nitride film, as it does in the conventional MNOS.

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[1] D. Kahng, W. J. Sundburg, D. M. Boulin, and J. R. Ligenza, Bell System Technical Journal, Vol. 53, 1974, p. 1723.

[2] K. K. Thornber, D. Kahng, and C. T. Neppell, Bell System Technical Journal Vol. 53, 1974, p. 1741.

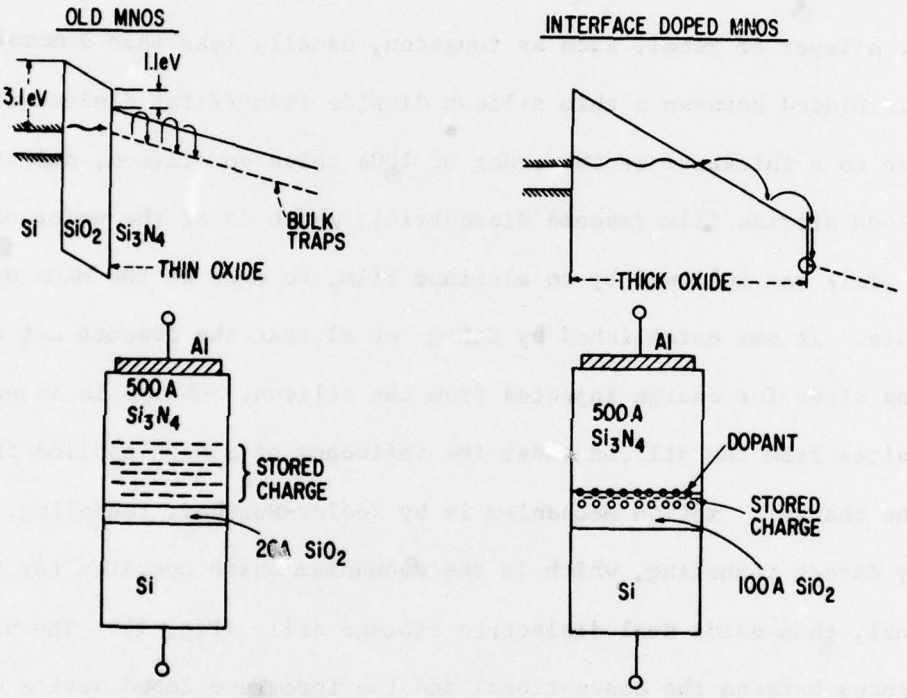

Figure 1. Conventional vs. Interface-Doped MNOS

This has the following important consequences:

1) The stored charge is retained for very long times.

2) The cell is very insensitive to read-disturb.

3) Device degradation mechanisms associated with charge motion in the nitride are less important.

The charge retention in interface-doped MAOS devices has been studied extensively by Thornber et al[2]. It was found by them that charge loss could be accelerated at elevated temperatures and applied bias voltages; the extrapolated charge retention was 500 years at 80°C. The charge decay mechanism at temperatures between 150 to 300°C was found to be by activated conduction through the alumina to the gate electrode.

In this previous work, emphasis was placed on tungsten as the interface dopant and alumina as the second dielectric, although other dopants such as Pt, Ta, Ir, and silicon nitride as the second dielectric were also explored. A lower limit of the doping concentration of 10^{14} cm^{-2} and an upper limit of $5 \cdot 10^{15}$ cm^{-2} was identified. Device endurance toward write/erase cycling was not reported.

Since the dopant deposition is an easily controllable step, the interface-doped memory device represents an advance in the state-of-the-art. In this report, we describe the use of ten different interface dopant metals in MNOS memory cells. Included are the write/erase characteristics as a function of the dopant concentration and oxide thickness, memory window as a function of dopant concentration and oxide thickness, write speeds as a function of write pulse width and amplitude, the charge retention as a function of doping concentration and oxide thickness, and finally, the endurance. The goal of this investigation is to enable an optimum choice to be made among types of dopants, deposition method, range of doping concentrations, and oxide thicknesses.

SECTION II

APPROACH

In order to survey as many dopant concentrations and oxide thicknesses as quickly as possible and without interfence from processing artifacts, a large number of varactor cells of varying concentrations and oxide thicknesses were prepared on a single silicon wafer. This was accomplished by preparing 5 to 6 oxide stripes across the wafer of increasing thickness (usually from 50 to 140A) by alternate thermal growth and subsequent partial removal of the oxide film by etching. This gives rise to a step pattern in the oxide thickness. The interface dopant is now deposited in such a way that its concentration varies from zero on one end of the wafer to a pre-determined level such as 10^{15} or 10^{16} cm^{-2} on the other, giving a wedge-like thickness distribution in between. The dopant concentration *gradient is perpendicular to the oxide thickness* gradient, thus giving a full range of dopant concentrations with each oxide thickness. In practice, this method is applicable if the variation in the doping concentration does not greatly exceed one order of magnitude. As a result, a concentration range of about one order of magnitude and six oxide thicknesses can be evaluated on one wafer. This is illustrated in Fig. 2.

For transistors, only the dopant concentration was varied over the wafer, at a constant oxide thickness.

The nitride thickness was between 300 and 600A.

Accelerated test methods were used wherever possible. Thus, to measure charge retention after writing, high gate bias voltages were applied to force an observable charge decay within several minutes. Extrapolation to zero bias voltage gives the expected retention under real use conditions. Since the endurances measured in this program have not exceeded 10^7 cycles so far, accelerated measurements have not been necessary.

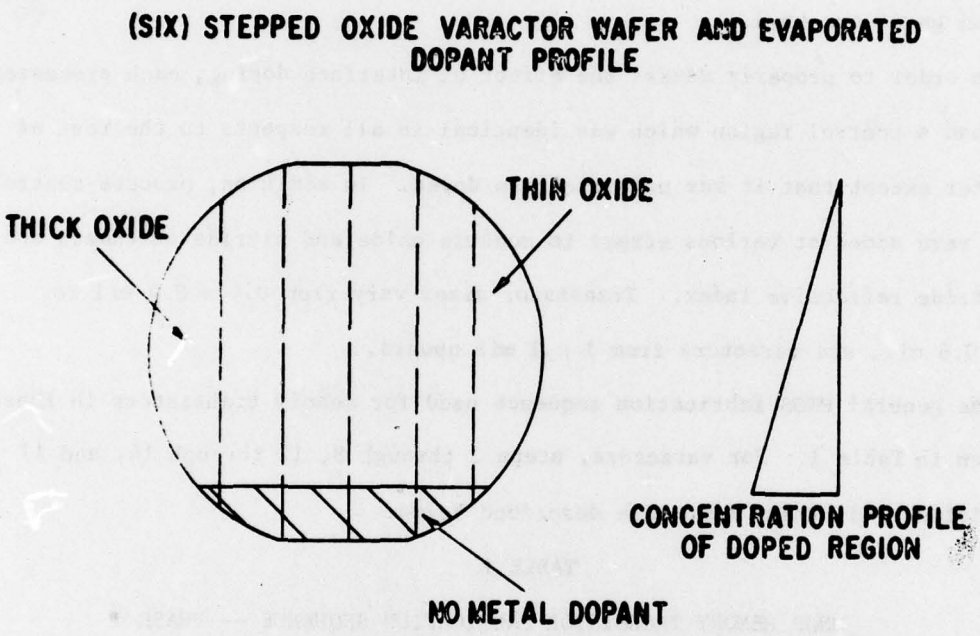

Figure 2. Stepped Oxide Varactor Wafer and Evaporated Dopant Profile

SECTION III

INTERFACE-DOPED MNOS DEVICE FABRICATION

In this section, the MNOS process which was used to fabricate devices for Phase I of this program is described. During Phase I, only varactors and discrete memory transistors were fabricated. The devices are p-channel, on 2" (100) silicon wafers of 3 to 8 ohm-cm n-type resistivity (phosphorus). Aluminum gates are used.

In order to properly assess the effect of interface doping, each processed wafer had a control region which was identical in all respects to the rest of the wafer except that it was not interface doped. In addition, process control wafers were added at various stages to measure oxide and nitride thickness and the nitride refractive index. Transistor sizes vary from 0.4 x 0.4 mil to 12 x 0.6 mil, and varactors from 1 x 1 mil upward.

The general MNOS fabrication sequence used for memory transistors in Phase I is shown in Table 1. For varactors, steps 2 through 8, 12 through 14, and 17 are omitted. All these steps are described below.

TABLE 1

MNOS MEMORY TRANSISTOR FABRICATION SEQUENCE -- PHASE I

Step No.	Description
1	Initial cleaning
2	Wafer oxidation
3	Source drain mask
4	Source drain predeposition
5	Source drain drive-in
6	Stable gate mask
7	Stable gate oxide
8	Memory gate mask
9	Memory gate oxidation

No.	Description (contd.)
10	Interface doping
11	Nitride deposition
12	Oxide deposition (SiO_2)
13	Contact mask (SiO_2)
14	Nitride oxide etch
15	Metal deposition
16	Interconnection mask
17	Interconnection sinter

(1) Initial cleaning

The initial cleaning process removes any surface contaminants that may remain on the wafers in the as-received condition.

The silicon wafers are first immersed in a 50/50 mixture of hydrofluoric acid (HF) and deionized water. They are next rinsed with deionized water and blown dry with nitrogen. In a quartz tube furnace at 1050°C, a thermal oxide is grown on the wafers. With pure oxygen flowing at 1 cubic ft./hr., 30 minutes is sufficient to grow a layer 180 Å thick. At this point, the dilute hydrofluoric acid bath is repeated. The oxide layer and any trapped impurities are stripped away. The cleaning step ends with a final rinse in deionized water and drying with nitrogen.

(2) Wafer oxidation

Wafer oxidation occurs in two parts. First a layer of thermal oxide 1100 Å thick is grown on the wafers in the manner described in step 1. At 1050°C and an oxygen flow rate of 1 cubic ft/hr, three hours are needed.

Second, 5200 Å of SiO_2 are deposited on the wafers by chemical vapor deposition in a silox reactor. The silox reactor is purged for 15 minutes with

line nitrogen. During this time, the heater block in the furnace is heated to 450°C. After the purge, the line nitrogen is turned off. Bottled nitrogen, oxygen and silane (SiH_4) diluted in argon flow through the reactor tube at the rates listed below:

Oxygen	0.211 liters/min.
Nitrogen	0.066 "
5.4% SiH_4 in Argon	0.45 "

After thus clearing the gas feed lines, the silane-in-argon is vented directly to the exhaust, and the oxygen is turned off. At this time, the wafers are inserted into the reactor. During a two-minute nitrogen purge, the wafers heat to the reaction temperature. The furnace now automatically begins a deposition run. Twelve minutes at the specified flow rates is sufficient to deposit 5200 Å of SiO_2. Thickness is determined by referring to a color/thickness table.

The 6300 Å (total thickness) of SiO_2 will act as a diffusion stop during the source/drain diffusion.

One of the by-products of the silox reaction is water vapor. Because of the harmful effect of water on photoresist, the wafers are baked for 30 minutes at 175°C in a nitrogen atmosphere prior to the next step.

(3) Source drain mask

The diffusion stop SiO_2 layer must be etched in this step to expose the source drain regions of the wafers. Photoresist is spun on to the wafers at 5000 rpm with a photoresist spinner. The resist is dried for 30 minutes in a nitrogen atmosphere at 80°C. The source-drain mask is then aligned on the wafers and the wafers are exposed to ultraviolet light. Resist developer is now used to wash away the photoresist that was not exposed to the UV light at the source and drain regions. The wafers are now baked for 30 minutes in a

nitrogen atmosphere at 175°C in preparation for the oxide etching step. The etchant is composed of 1 part hydrofluoric acid and 9 parts NH_4F. Three minutes are sufficient to remove the oxide above the source and drain without appreciable undercutting of the photoresist. After rinsing in deionized water, the remaining photoresist is removed in microstrip heated to 95°C (5 minutes) and boiling deionized water (3 minutes). Finally, the wafers are cleaned in a vapor degreaser with a solvent mixture of equal parts of isopropyl alcohol, acetone and trichlorethylene and blown dry with nitrogen.

Periodic microscope checks are made during this step to insure correct alignment and proper etching.

(4) Source drain predeposition

The p-dopant which we use is boron. The wafers to be doped are arranged vertically in a quartz rack, interspersed with wafers of boron nitride. The rack is then inserted into a tube furnace (1000°C) with a nitrogen atmosphere for 15 minutes. Boron is transferred to the silicon wafers, where a thin layer of silicon at the source and drain regions becomes very highly doped.

(5) Source drain drive-in

Before the boron dopant is driven into the silicon surface, the silicon dioxide and boron residing on wafer surfaces are stripped away in 50/50 HF. The wafers are then inserted into the 1000°C tube furnace for 3 hours in oxygen. The junction depth is about 1.5 microns. Simultaneously, 1100 Å of thermal oxide are grown on the wafers.

(6) Stable gate mask

Fifty-two hundred Å of SiO_2 are again deposited on top of the thermal oxide layer. This oxide layer, which totals 6300 Å, is masked and etched to give the stable gate mask pattern.

(7) Stable gate oxidation

The stable gate oxide, which is 500 Å thick, is a thermal oxide grown at 1000°C for 1½ hrs with an oxygen flow of 1 cu.ft/hr.

(8) Memory gate mask

In the great majority of our devices, the stable gate oxide was not used. In these cases, the stable gate mask served to expose the memory region. Those wafers which had stable gates, however, employed a memory gate mask for the thinner memory oxide.

(9) Memory gate oxide

The memory gate oxides ranged in thickness from 30 Å to 134 Å. They were grown in a tube furnace at 1050°C. To more closely control the growth process, the flow gas is 1% oxygen in argon. Figure 3 shows the relationship between oxide thickness and time.

(9a) The use of varactors

For much of the initial survey of interfacial dopants, varactors were used instead of transistors because of their much more rapid producibility. The use of varactors enables us to vary the gate oxide thickness within a single wafer, further minimizing the effect of wafer-to-wafer differences, as illustrated in Fig. 2. It required oxidizing the wafers 6 separate times. After each oxidation, the wafers were partly immersed in 50/50 HF and water to remove a portion of the oxide layer. For instance, after the first gate oxidation, all but the leftmost strip of the wafer would remain. Table 2 contains the thickness vs. total oxidation time data for one particular six step oxide run.

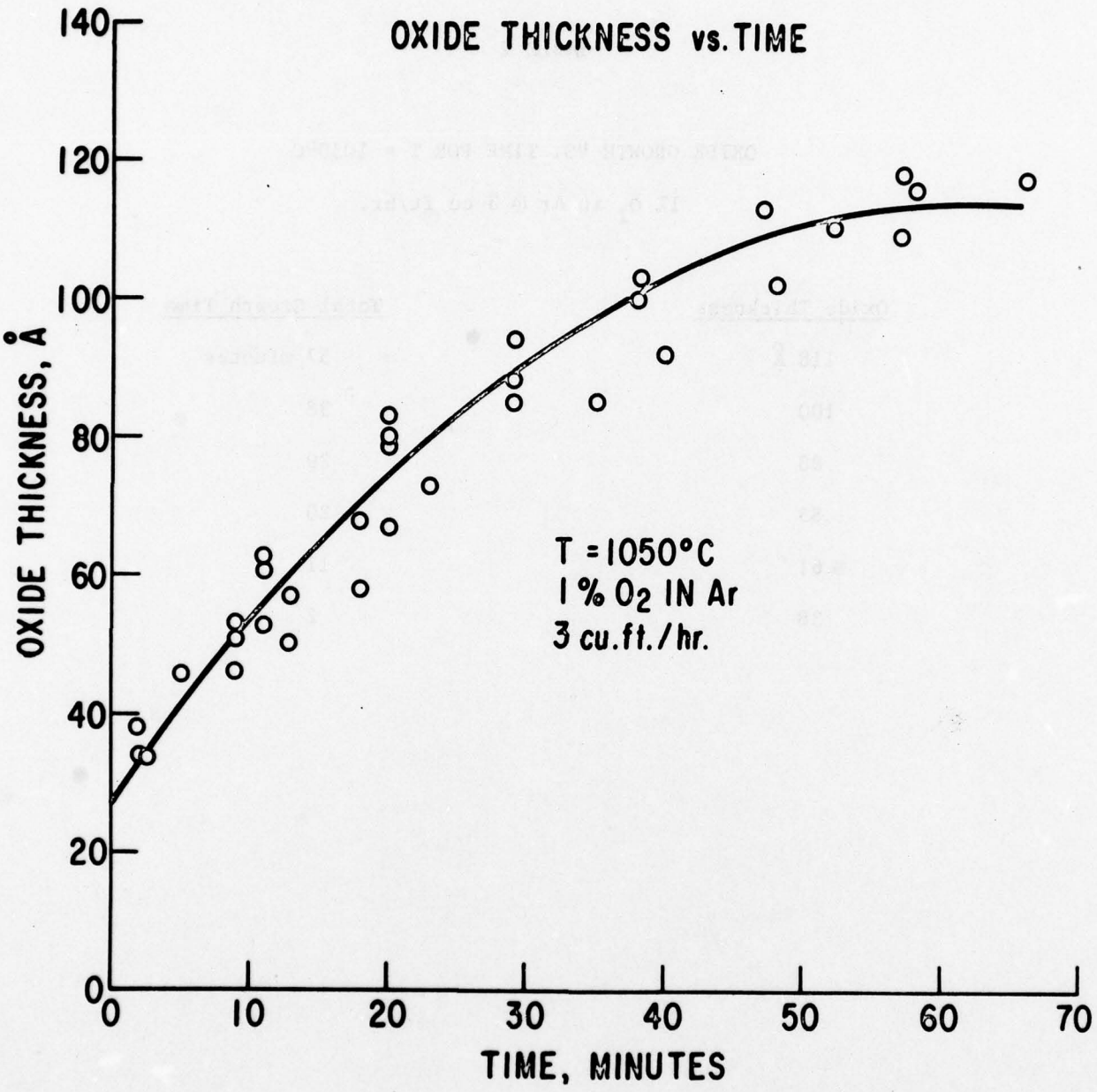

Figure 3. Oxide Thickness vs. Time

TABLE 2

OXIDE GROWTH VS. TIME FOR T = 1050°C

1% O_2 in Ar @ 3 cu.ft/hr.

Oxide Thickness	Total Growth Time
118 Å	57 minutes
100	38
88	29
83	20
61	11
38	2

(10) Interface doping

This important process step is covered in section IV.

(11) Nitride deposition

Silicon nitride is deposited in an epitaxial reactor by the SiH_4/NH_3 reaction at a wafer temperature of 850°C. The reactor is first given a 10 minute nitrogen purge. During this time, the silane, ammonia and hydrogen flow rates are set. The ratio of silane to ammonia is 1/1000. After the purge, the wafers are inserted into the reactor and brought to temperature in the presence of the hydrogen flow gas. Fast write devices have a nitride thickness in the neighborhood of 300 Å, and most slow write devices have 450 - 600 Å nitride layers. Deposition times are from 1/2 min. to 1 min. long.

(12) Oxide deposition (SiO_2)

For a third time, 5200 Å of SiO_2 are deposited by the chemical vapor method. This oxide will remain on the wafers as a field oxide.

(13) Contact mask

This mask allows windows to be etched down to sources and drains, so that they can be contacted with aluminum, which will be deposited in a later step.

(14) Nitride oxide etch

The 5200 Å of oxide are first etched by immersing the wafers for three minutes in buffered HF (NH_4F/HF:9/1) as described earlier. The photoresist is removed and wafers cleaned, degreased and dried. The wafers are then boiled for 45 minutes in phosphoric acid to etch the nitride layer

(15) Metal deposition

Au aluminum layer is deposited by electron beam evaporation. The wafers are placed in a bell jar which is evacuated to 10^{-6} torr. An aluminum slug is melted with an electron beam and the wafers are coated to a thickness of 1 to 1.5 μm. The thickness is monitored by quartz crystals.

(16) Interconnection mask

Photoresist is patterned on the wafers as before, using the interconnection mask. The aluminum is etched in a solution of 76% phosphoric acid, 15% acetic acid, 5% water, and 4% nitric acid heated to 45°C. Etching time is 1 to 2 minutes. The photoresist is stripped and the wafers are again boiled in deionized water and vapor degreased.

(17) Interconnection sinter

Processed wafers are annealed at 500°C for 25 minutes in an annealing oven. Nitrogen and hydrogen are used at the following flow rates:

Nitrogen - 2 cubic ft/hr.

Hydrogen - 0.1 cubic ft/hr.

SECTION IV

INTERFACE DOPING

The interfacial doping step is carried out after the memory gate oxidation. In this section the selection of dopants, dopant concentration, and doping conditions are given.

SELECTION OF DOPANTS

In the selection of dopants, the following criteria were applied:

- The vapor pressure of the element or its oxide must be negligible at 850°C.
- The diffusion coefficient of the dopant at 850°C in SiO_2 or Si_3N_4 must be low.
- The dopant must not be subject to ionic motion in SiO_2 or Si_3N_4 under bias temperature stress.
- The melting point of the deposited species must be above 900°C.
- Depositing reproducibly must not be too difficult.

These criteria eliminate the alkali and alkaline earth metals because of their high ionic mobility, Au, Ag, and Cu, which have high diffusivities in SiO_2, Zn, Cd, Hg, Ga, and In, because of high vapor pressures or low melting points. Primarily the elements in group VII, I-VIIB, the rare earth elements and perhaps Al remain. The reactivities of some of those elements are given in Table 3. They fall into four classes, according to their oxide-free energy of formation:

- Elements that will not oxidize on exposure to air (Ru, Rh, Pd, Os, Ir and Pt).
- Elements that oxidize in air but can be readily reduced by hydrogen at 850°C (V, Cr, Mo, W, Fe, Co, and Ni).

- Elements that oxidize in air and are not reducible by hydrogen at 850°C (Nb and Ta).
- Elements that react with SiO_2 to form the oxide, reduce the SiO_2 to form Si (Y, Ti, Zr, and La), and are not reducible by hydrogen at 850°C.

TABLE 3

REACTIVITIES OF POTENTIAL DOPANTS

Element	Group	Oxidizes in Air	Oxide Reducible in H_2	Reduces SiO_2
La	III B	Yes	No	Yes
Ti	IV B	Yes	No	Yes
Zr		Yes	No	Yes
V	V B	Yes	Yes	No
Nb		Yes	No	No
Ta		Yes	No	No
Cr	VI B	Yes	Yes	No
Mo		Yes	Yes	No
W		Yes	Yes	No
Fe	VII	Yes	Yes	No
Co		Yes	Yes	No
Ni		Yes	Yes	No
Ru		No	--	--
Rh		No	--	--
Pd		No	--	--
Os		No	--	--
Ir		No	--	--
Pt		No	--	--

At least one metal was included from each of these classes. The metals in the fourth class will react to give a layer of metal oxide. For the initial survey, the following elements were selected: Ir, Pd, Pt, Nb, Ta, W, Mo, Cr, Ni, and Ti.

DOPANT CONCENTRATION

It is of interest to calculate the charge stored in a MNOS device to give a threshold shift of ΔV_T, if the charge is located near the silicon/insulator interface. This situation is given by:

$$Q_{stored} \simeq C_o \Delta V_T$$

where C_o is the gate insulator capacitance. For ΔV_T = 10 volts, $Q_{stored} \simeq$ 1.6×10^{-10} C/cm^2, or about 10^9 electronic charges/cm^2.

Kahng et al.[1] have indicated that the effective doping range for tungsten in thick oxide MNOS devices was between 10^{14} to $5 \cdot 10^{15}$/cm^2. There are then 10^5 to 10^6 available dopant sites for each stored charge.

In Phase I of this program, dopant concentrations ranged between 0 and 5×10^{16} cm^{-2}.

DOPING CONDITIONS

Methods that have the potential of introducing precise amounts of dopant are:

a. Vacuum deposition by evaporation or sputtering.

b. Adsorption of metal ions from solution.

c. Electroplating by current flow through the thin oxide.

d. Exposure to a gas bearing the dopant at high temperature or in electrical discharge.

e. Growing the last portion of the oxide film in the presence of small additions of dopants to the flow gas.

f. Ion implantation.

Doping by vacuum deposition, sputtering, and adsorption from solution were employed in this investigation.

VACUUM DEPOSITION OF METAL DOPANTS BY EVAPORATION

Vacuum deposition of the metal dopants is the most generally applicable technique available. Evaporation by electron gun is readily controlled and the use of quartz crystal monitors provides a reliable relative thickness standard.

Figures 4 and 5 are schematics of the deposition equipment. Figure 4 indicates the relationship between the wafer holder, the Sloan 180° electron gun, the flying shutter, and the two quartz crystal monitors. Figure 5 is a top view of the wafer holder. The open and closed shutter positions are shown by the dotted lines.

The wafer holder has a capacity of four-two inch wafers. However, only during the deposition of aluminum does it hold more than 2 wafers. During a dopant evaporation only two wafers are placed at the points marked A and B in Figure 5. The darkened areas indicate the position of shields used to prevent deposition on those portions of the wafers. A small slug of the dopant metal is placed in the electron gun and the system evacuated to below 10^{-5} torr. The shutter covers the wafers and the inner oscillator.

The dopant metal is slowly heated to its melting point by the magnetically focused electron beam. The water cooled outer oscillator monitors the gradually increasing rate of evaporation.

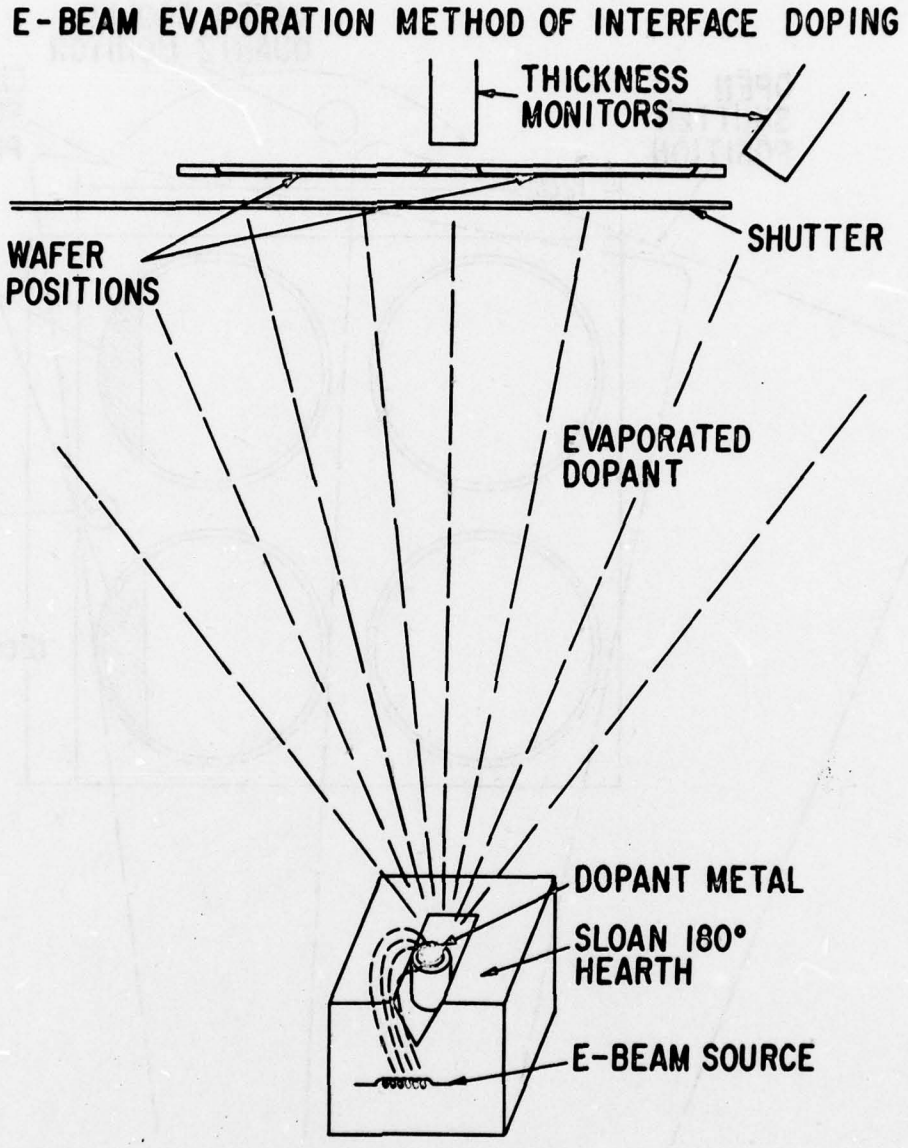

Figure 4. E-Beam Evaporation Method of Interface Doping

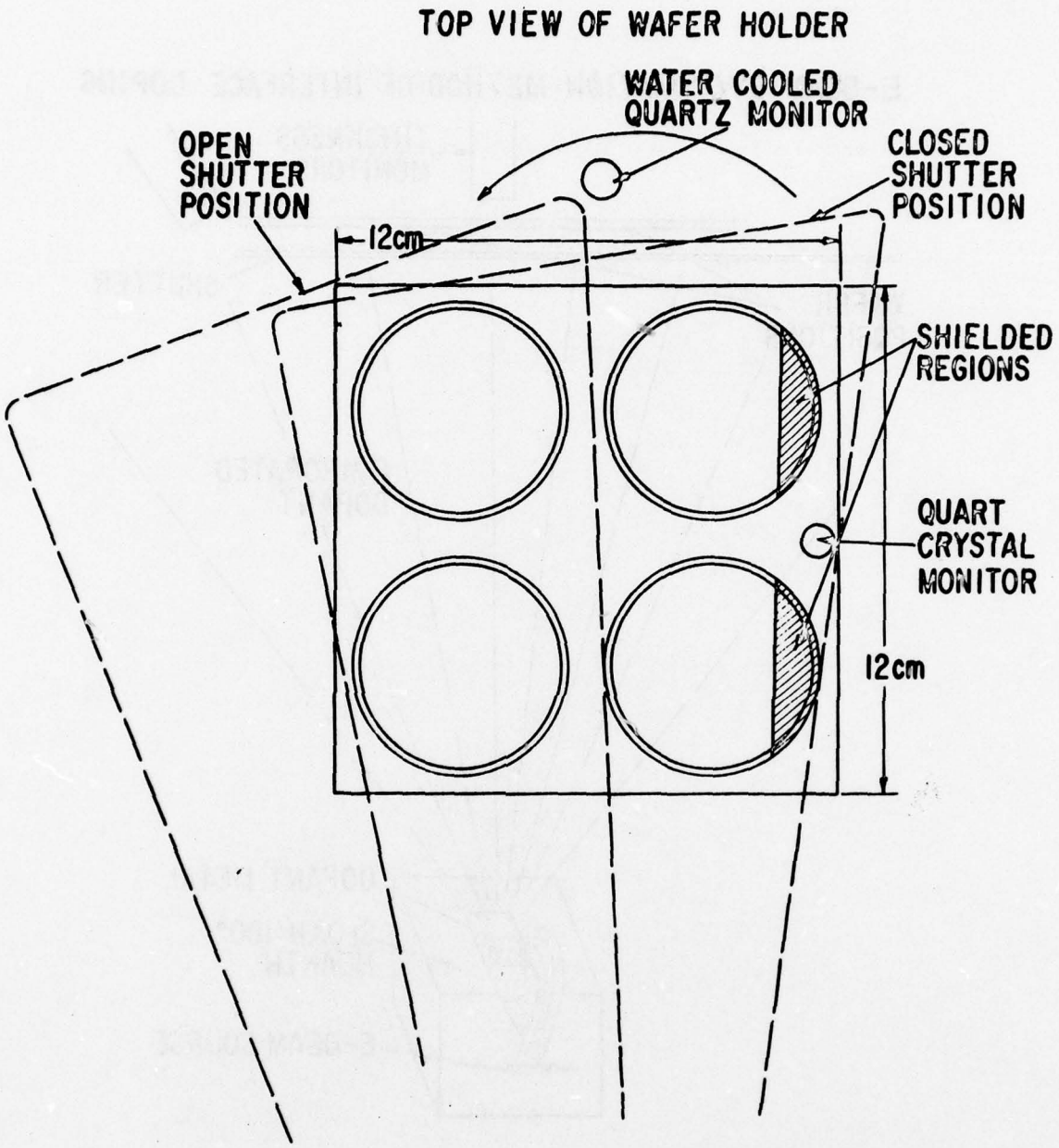

Figure 5. Top View of Wafer Holder

Once this rate has stabilized at a predetermined level, the shutter begins to open. If the rate of evaporation of a metal is high or a low dopant concentration is desired, the shutter is set to turn through the 27 degrees necessary to expose the wafers completely in 1 second. For lower evaporation rates, the shutter is allowed 5 seconds to rotate through this angle. As the shutter opens, the inner oscillator measures the evaporated metal thickness. By noting the oscillator frequency before the shutter opens and after it closes again, we can calculate the amount of dopant on those parts of the wafers exposed for the longest time.

When the wafers have been fully exposed (save for the shielded regions), the shutter is released from motor control and swings shut instantly.

Table 4 shows the multipliers necessary to calculate dopant concentration from the frequency change of the oscillator recorded during the evaporation.

TABLE 4

MULTIPLIERS TO CALCULATE DOPANT CONCENTRATION

Dopant	Maximum Dopant Concentration, x 10^{15} cm^{-2}
Tungsten	0.0717 x Δf
Iridium	0.0686 x Δf
Palladium	0.1236 x Δf
Platinum	0.0674 x Δf
Niobium	0.1416 x Δf
Tantalum	0.0724 x Δf
Molybdenum	0.1369 x Δf
Chromium	0.2536 x Δf
Nickel	0.2252 x Δf
Titanium	0.2740 x Δf

TUNGSTEN OXIDE EVAPORATION

Of the six most promising dopants, tungsten proved to be the most difficult one to deposit by electron beam evaporation. It was difficult to maintain a constant rate of evaporation for the required length of time. As a result, we investigated the possibility of evaporating tungsten trioxide from a ribbon of the metal.

A tungsten ribbon of dimensions .003" x 3/8" x 5" is clamped between two current leads from a step-down current transformer. The strip is oxidized in air by passing a large current through it. By observing the colors on the ribbon, the resulting oxide thickness can be controlled and is highly reproducible. The system is then evacuated and the oxide flashed off and deposited on the wafers by resistance heating the strip.

DOPANT DEPOSITION BY SPUTTERING

Sputtering was carried out in a vacuum system filled with argon to a pressure of $1.8 \cdot 10^{-2}$ torr., after having been previously evacuated to 10^{-6} torr. Sputtering targets were 6 in. in diameter, and the distance between targets and substrates was 1.5 inches. A sputtering power of 50 watts was used. This resulted in a deposition rate of 6 A/min. Only Cr and Ni were sputtered.

DOPANT DEPOSITION BY SOLUTION DOPING

Very dilute solutions (0.00018M) of Cr or Ni were prepared. From 1 to 3 cm^3 of solution were then metered out and the solvent evaporated on the wafer surface. The resulting dopant concentration was not uniform over the wafer, however, the dopant concentration being higher at the wafer edges due to the accumulation of solute at the edges where the solvent evaporated last.

ANALYTICAL PROCEDURES

When the dopant was evaporated, the deposited dopant concentration was monitored by the frequency change of a 4 MHz quartz crystal. The quartz crystal, in turn, was calibrated in blank runs in which metal was deposited on an oxidized Si wafer to a coverage of about 100 monolayers, which was accurately determined by atomic absorption measurements. This was then compared to the corresponding frequency change. The sensitivity of the quartz crystal used was .0078 microgram/Hz.

When the dopant was sputtered, the dopant concentrations were determined from the sputtering time at a sputtering voltage and current for which the sputtering rate has been previously determined in blank experiments using dopant thicknesses of 500 to 1000 A.

In experiments involving solution doping, very dilute (0.00018M) solutions of the dopants (Cr and Ni only) were prepared. From 1 to 3 cm^3 of solution were then metered out and the solvent evaporated on the wafer surface. The average dopant concentration was then calculated from the quantity of solute contained in the solution, which was known to three significant figures.

Auger analysis of the wafer surface after dopant deposition clearly shows the presence of the dopant. This is illustrated in Fig. 6 for tungsten. In addition to the expected elements, a strong carbon peak is always visible, probably due to the long storage time before analysis. The Auger peak-to-peak distance for the various W lines obtained for a number of W concentrations corresponds reasonably well to the surface concentration calculated from the quartz crystal frequency change. This is illustrated in Fig. 7 for tungsten

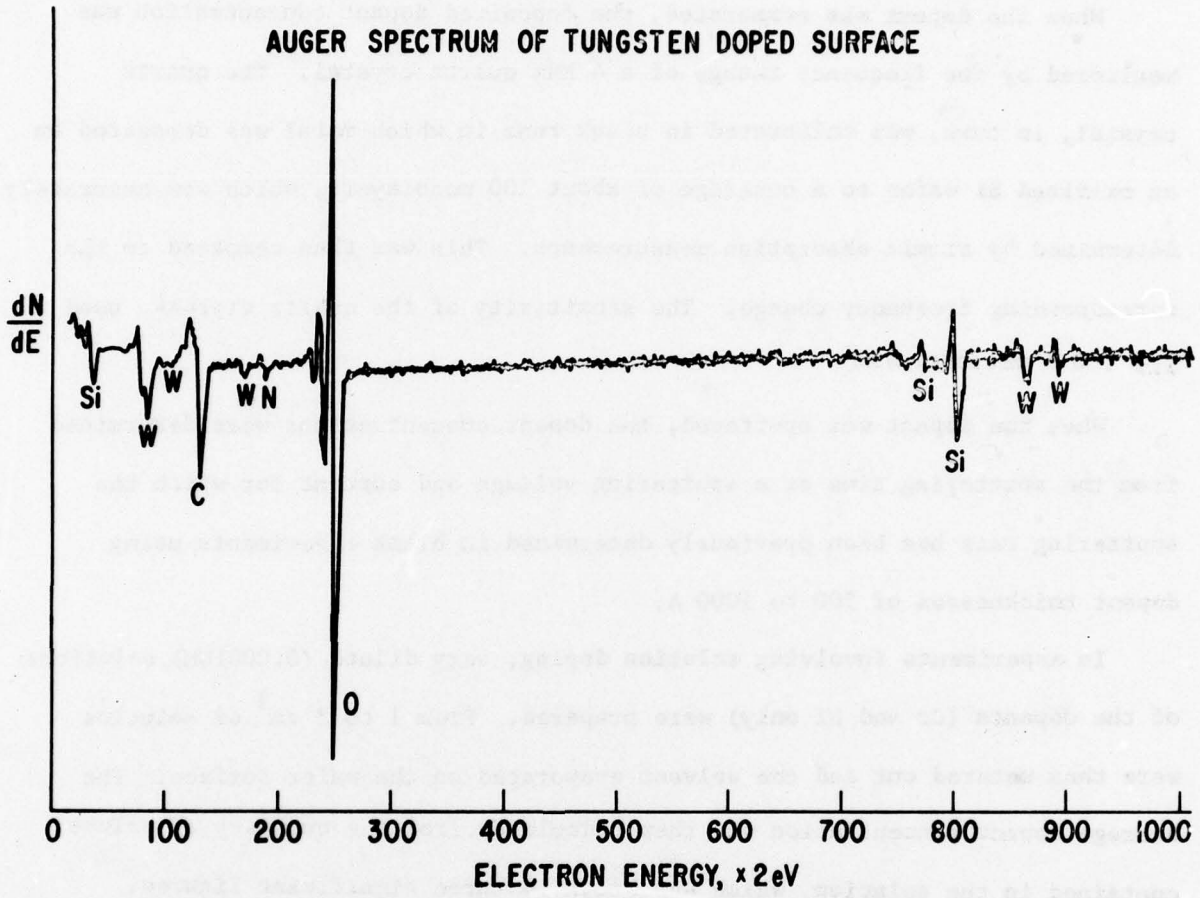

Figure 6. Auger Spectrum of Tungsten Doped Surface

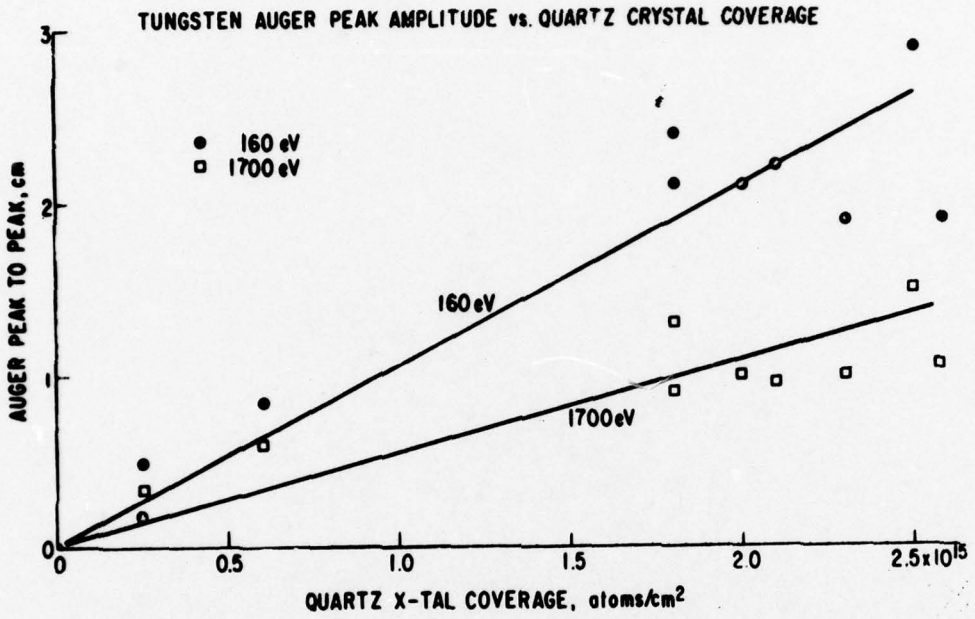

Figure 7. Tungsten Auger Peak Amplitude vs. Quartz Crystal Coverage

as the dopant, for the tungsten lines corresponding to 160 and 1700 ev Auger electron energy.

SECTION V

WRITE CHARACTERISTICS

WRITE MECHANISMS AND WRITE CURVES

The three mechanisms by which the threshold voltage in interface doped MNOS devices can be changed are illustrated in Figure 8. First, charge can be transferred through the thin oxide by a tunneling process (direct tunneling if the oxide is thin, and F-N tunneling if thick). Application of a positive write voltage on the gate will shift the threshold voltage in a positive direction (forward shift). Second, charge can be transferred from the gate electrode through the Si_3N_4 to the storage sites, probably by Poole-Frenkel conduction. Here, application of a positive voltage to the gate electrode shifts the threshold voltage in a negative direction (reverse shift). Third, the threshold voltage can change irreversibly due to effects associated with wear-out (lack of endurance) which is caused by the prolonged application of a high write voltage of either polarity, and is normally associated with the generation of a large number of fast surface states.

The first mechanism is responsible for writing the two memory states. It is essentially temperature independent. The second mechanism, which is strongly temperature dependent, has not been found to be the predominant one in this investigation. Note, however, that Thornber[2] et.al.have reported that the second mechanism is important in determining retention.

To write, a sufficiently high write voltage must be applied for a sufficient length of time. The lower the write voltage, the longer the time required to transfer the charge to the storage sites and change the threshold voltage. This is schematically indicated in Fig. 9, where the expected threshold voltage shift is shown as a function of the write pulse width for various write pulse amplitudes (full lines). The expected behavior is shown for initial memory

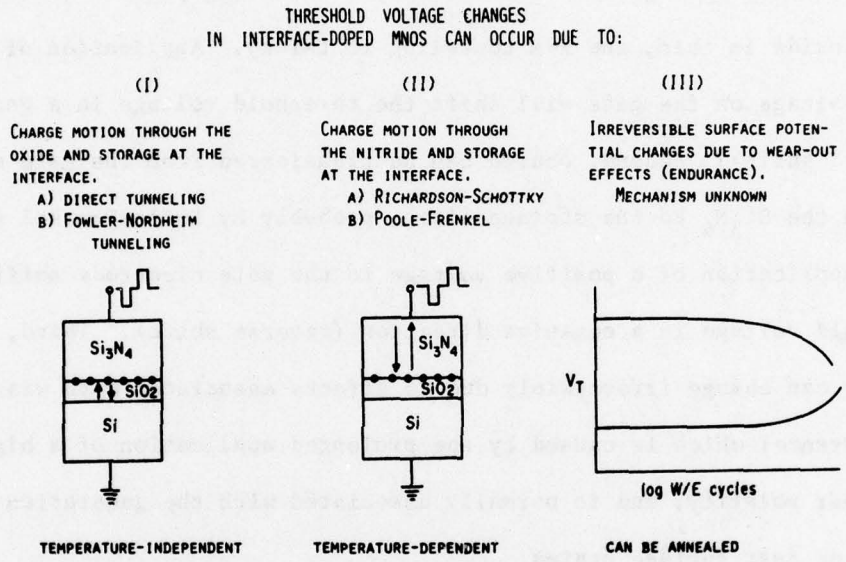

Figure 8. Threshold Voltage Changes in Interface-Doped MNOS

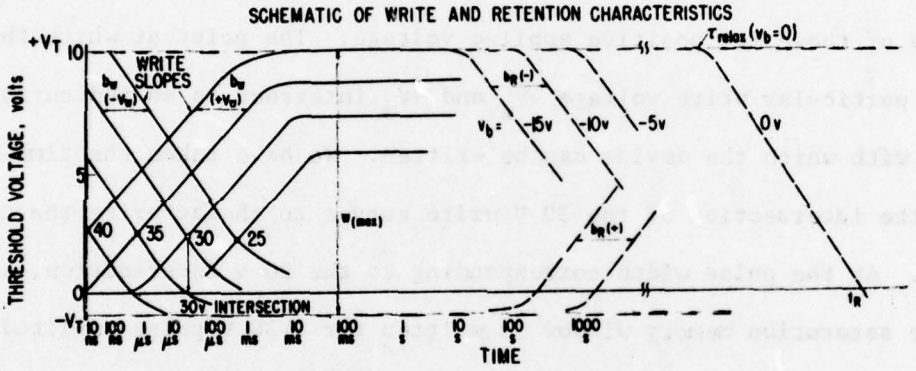

Figure 9. Schematic of Write Characteristics

states for which the threshold voltage is -1 V and also + 10 V, and to which a positive and negative write voltage is applied, respectively. When the write voltage is first applied, the threshold voltage changes rapidly due to the high field across the thin oxide. However, the threshold voltage must be expected to saturate soon as more and more charge is stored at the dopant sites and the field is reduced. The time at which the threshold voltage levels out with time depends on the write pulse amplitude.

The write curves for negative applied write voltages are roughly mirror images of those for positive applied voltage. The point at which the curves for a particular write voltage $-V_w$ and $+V_w$ intersect is an indication of the speed with which the device can be written. We have taken the time associated with the intersection of the 30 V write curves to characterize the device write speed. At the pulse width corresponding to the 30 V intersection, about half of the saturation memory window is written for a 30 V pulse amplitude.

It is found experimentally that the spacings, b_w on the log time axis, between write characteristic curves expressed in decades of write time per volt of write voltage are approximately equal in the range of voltages from 20 to 40 V, which were normally used for writing. Also, the slopes of the write curves, expressed in volts of threshold voltage change per decade of applied write pulse time, are approximately equal for all write voltages of the same polarity. The same is true for both polarities, except that the sign of the slopes are changed.

The schematic behavior indicated in Fig. 9 is actually followed quite well, as indicated in Fig. 10 where actual experimental write curves are plotted for a chromium interface doped varactor for write voltages of $\pm$ 25V to $\pm$ 40V and

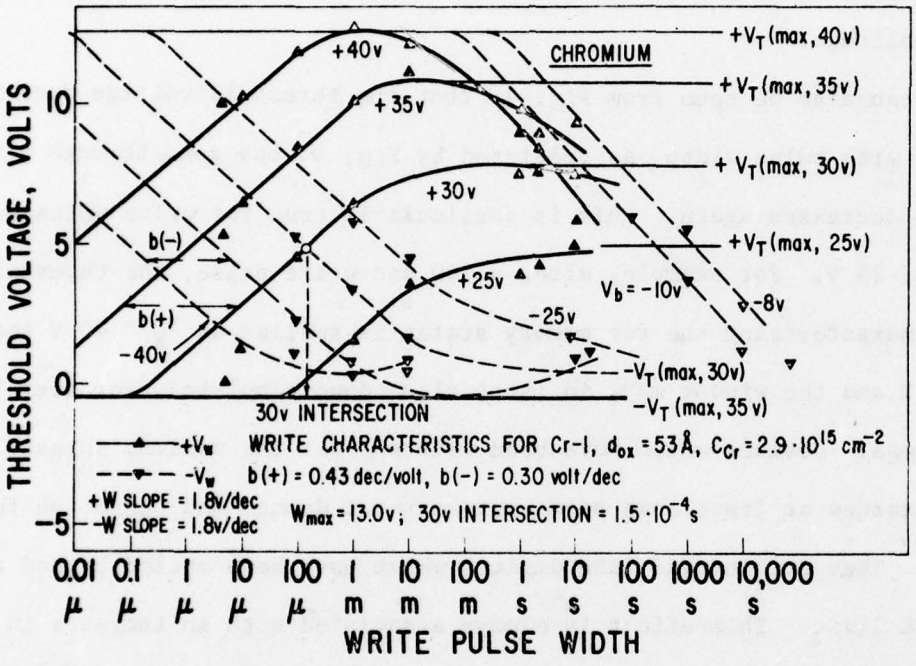

Figure 10. Write Characteristics of Chromium Doped Varactors

pulse widths between 5μs and 10s. The write behavior of this device can be characterized by a write slope of 1.8 V/dec, a spacing b_w between write curves of 0.43 dec/volt for positive write voltages and -0.30 dec/volt for negative write voltages, and a "30 V intersection" of 100 μs, meaning that approximately a 5 V window can be written at a 100 μs write pulse width and a 30 V write pulse amplitude.

It can also be seen from Fig. 10 that the threshold voltage does not saturate with pulse width, as predicted by Fig. 9, but goes through a maximum and then decreases again. This is particularly true for write voltages in excess of 25 V. For example, after a 100 sec write pulse, the threshold voltage window characterizing the two memory states is smaller at V_W = 40 V than it is at 30 V,and the window may, in fact, close down completely for very long write times. Devices which have been written past the maximum threshold window have sustained at least some permanent wear-out damage and cannot be fully re-written. They act instead like devices which have been cycled beyond their endurance limit. This effect is always associated with an increase in the surface state density. We have taken the maximum memory window achievable for any write pulse width or amplitude (up to 40V) as the "saturation memory window." The saturation memory window of the device in Fig. 10, for instance, is from +12.5 to -0.5, for a maximum window of 13 V, at $V_w = \pm 40$ V.

COMPARISON WITH UNDOPED DEVICES

It is in the write characteristics where the beneficial role of interface doping can be demonstrated best. Figure 11 illustrates the write characteristic curves of two devices which differed from each other only in that one was doped with $1.1 \cdot 10^{15}$ cm^{-2} of Pt, and the other was undoped. (They were adjacent on the same wafer.) Writing with both polarities gives the curves shown in Fig. 11,

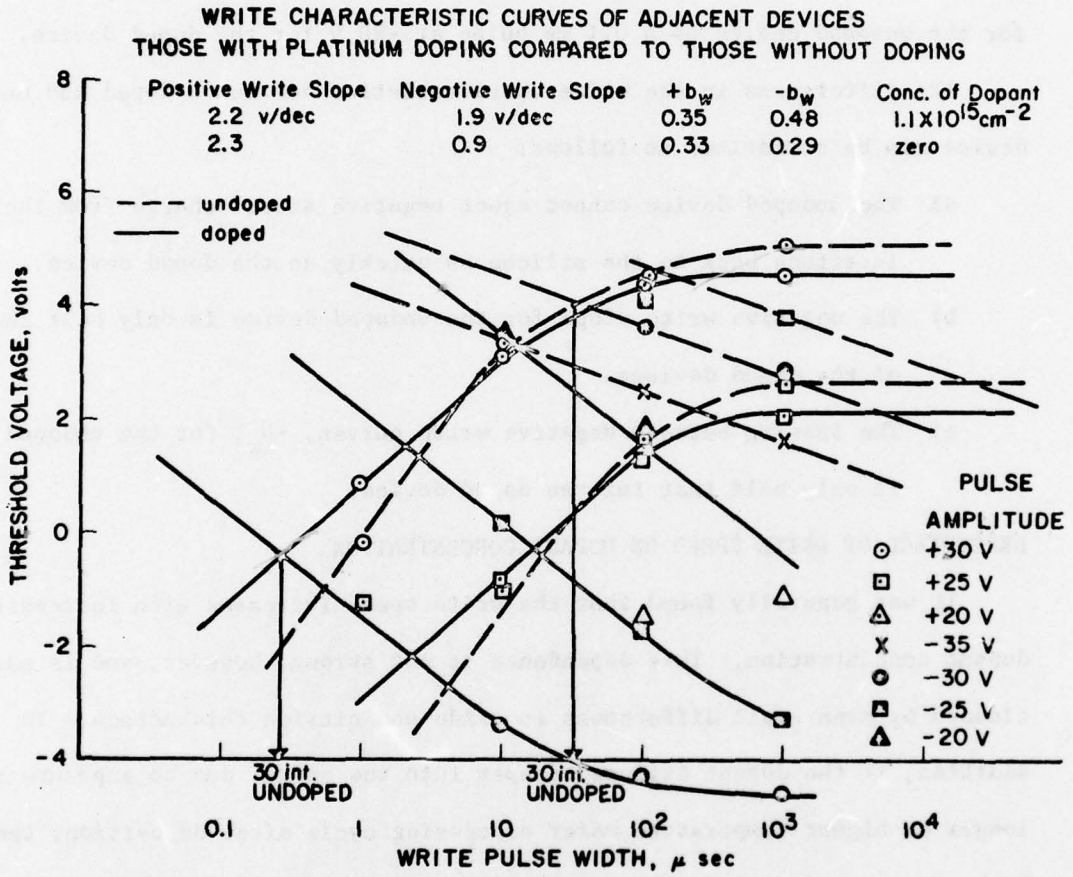

Figure 11. Write Characteristic Curves of Doped and Undoped Devices

starting from the opposite saturated memory state. It can be seen that the write curves are essentially identical for the doped and undoped devices when the write voltage is positive. However, for negative write voltages, the undoped device needed much longer pulse widths to bring about the same threshold voltage change which was obtained for much shorter pulse widths in the doped device. Thus, a 1 ms pulse at -35 V gives the same threshold voltage change for the undoped device as a 0.1 ms pulse at -20 V for the doped device.

The differences in the write characteristics between a doped and undoped device can be summarized as follows:

a) The undoped device cannot eject negative stored charge from the interface back to the silicon as quickly as the doped device.

b) The negative write slope for the undoped device is only half that of the doped devices.

c) The spacing between negative write curves, $-b_w$, for the undoped device is only half that for the doped device.

DEPENDENCE OF WRITE SPEED ON DOPANT CONCENTRATION

It was generally found that the write speed increased with increasing dopant concentration. This dependence is not strong, however, and is easily clouded by even small differences in oxide and nitride thicknesses. In addition, if the dopant diffused deeper into the oxide, due to exposure to a longer or higher temperature wafer processing cycle after deposition, then high write speeds can be observed even at relatively low concentrations.

Fig. 12 shows the normally observed behavior. Here the 25 volt intersection is plotted as a function of the chromium dopant concentration for a set of increasing oxide/nitride thicknesses. The write speed increases by about two orders of magnitude for an increase in the doping by one order of magnitude.

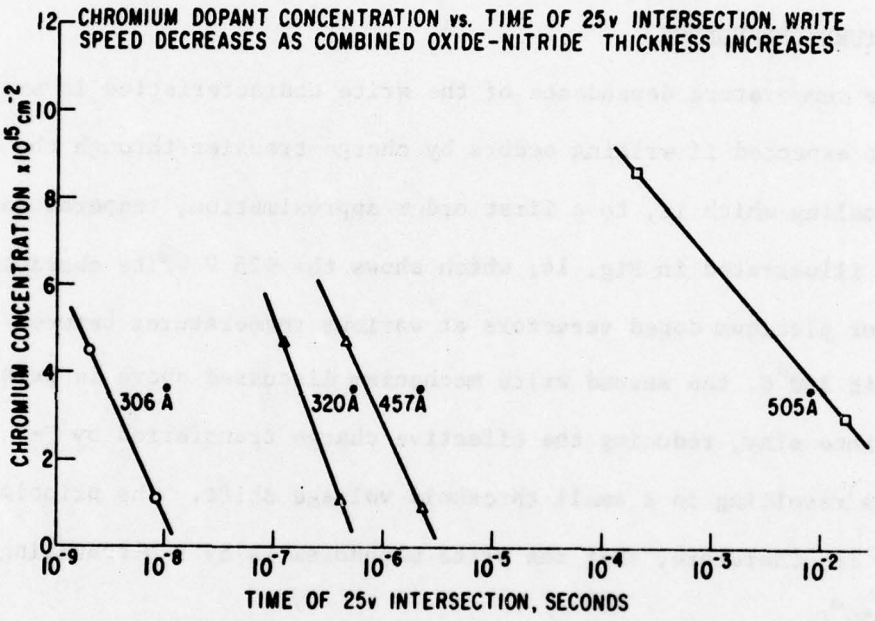

Figure 12. Cr Dopant Concentration vs. Time of 25V Intersection

DEPENDENCE OF WRITE SPEED ON OXIDE THICKNESS

The oxide thickness has a strong influence on write speed. Although this influence is again clouded somewhat by the varying degrees of diffusion of the dopant in the oxide, the dependence of write speed on oxide thickness is generally as shown in Fig. 13, which displays the dependence for fast-write devices. An increase in the oxide thickness of 20 A decreases the write speed by about 3 orders of magnitude.

TEMPERATURE DEPENDENCE

The temperature dependence of the write characteristics is small. This is to be expected if writing occurs by charge transfer through the oxide by F-N tunneling which is, to a first order approximation, temperature independent. This is illustrated in Fig. 14, which shows the +25 V write characteristic curve for platinum doped varactors at various temperatures between 25°C and 300°C. At 300°C, the second write mechanism discussed above is perhaps coming into play, reducing the effective charge transferred by F-N tunneling, and thus resulting in a small threshold voltage shift. The principal conclusion is, therefore, that the write mechanism is by F-N tunneling at least up to 250°C.

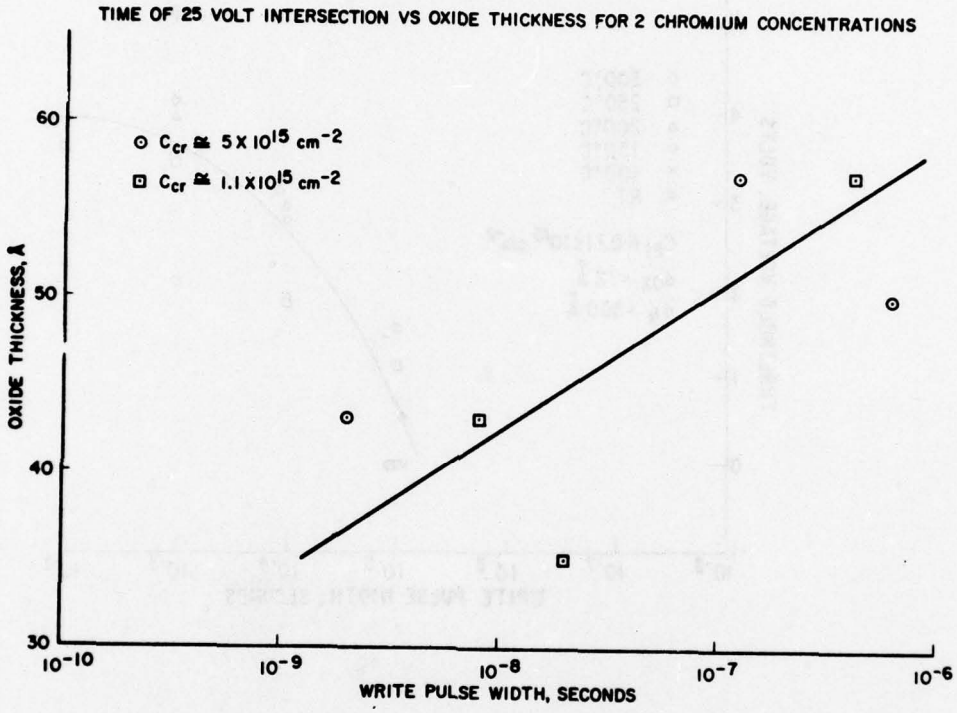

Figure 13. Time of 25V Intersection vs. Oxide Thickness

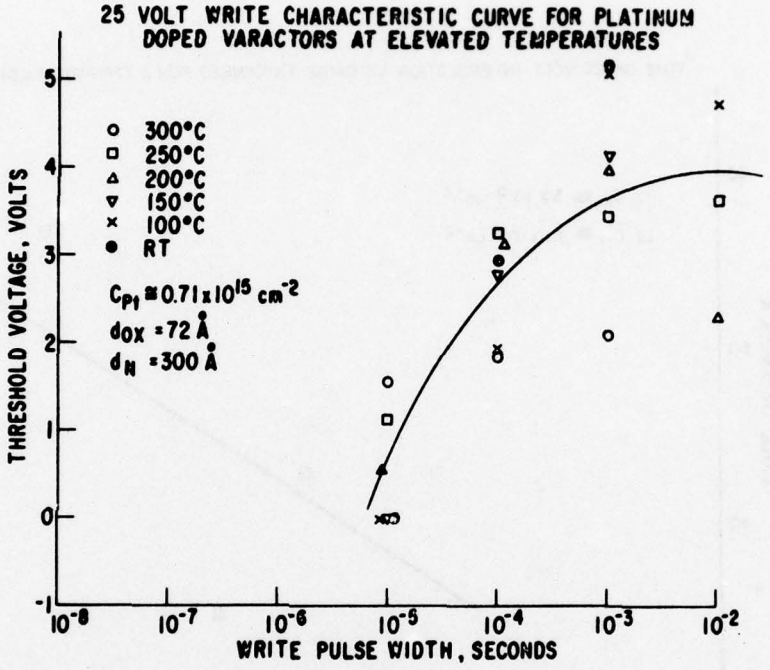

Figure 14. 25V Write Characteristic Curve at Elevated Temperatures

WRITE CHARACTERISTICS OF DEVICES DOPED BY SPUTTERING

Devices doped by sputtered Cr or Ni generally behaved similarly to those doped by evaporation, with the possible exception that writing with negative write voltages was more difficult. This is illustrated in Fig. 15 for Ni doped varactors, and in Fig. 16 for Cr doped varactors.

SUMMARY OF WRITE CHARACTERISTICS

The write characteristics for Pt, W, Ni, Cr, Ir, and Pt doped devices are summarized in Table 5. It should be noted that there is a considerable degree of similarity between the write parameters of all devices for all dopants, concentrations, and oxide thicknesses. Thus, over the entire dopant concentration (10^{14} to 10^{16} cm^{-2}) and oxide thickness range (40 to 140A) studied, and all of the six most promising dopants, the write slope was always 2.0 ± 0.5 V/dec, and the spacing b_w was always 0.40 ± 0.10 dec/volt. The saturation (maximum) memory window was generally around 10 V. The parameter which does differ the most between devices is the "30 V intersection." The shortest "30 V intersections" are obtained for the thinnest oxide films and the highest dopant concentrations. The lowest value is $2 \cdot 10^{-9}$ sec, obtained for a 48 A oxide film and a Cr dopant level of $4.5 \cdot 10^{15}$ cm^{-2}, and a 58 A oxide film and a WO_3 concentration of $1.94 \cdot 10^{15}$ cm^{-2}. For the thicker oxide films and lower dopant concentrations, values as long as 100 msec have been obtained. This covers the range of write speeds required for fast and slow write devices.

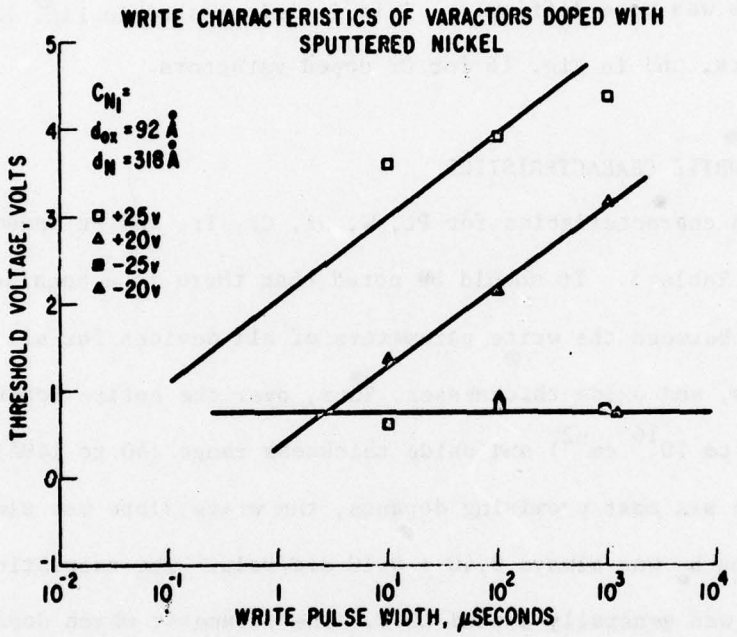

Figure 15. Write Characteristics of Varactors Doped with Sputtered Nickel

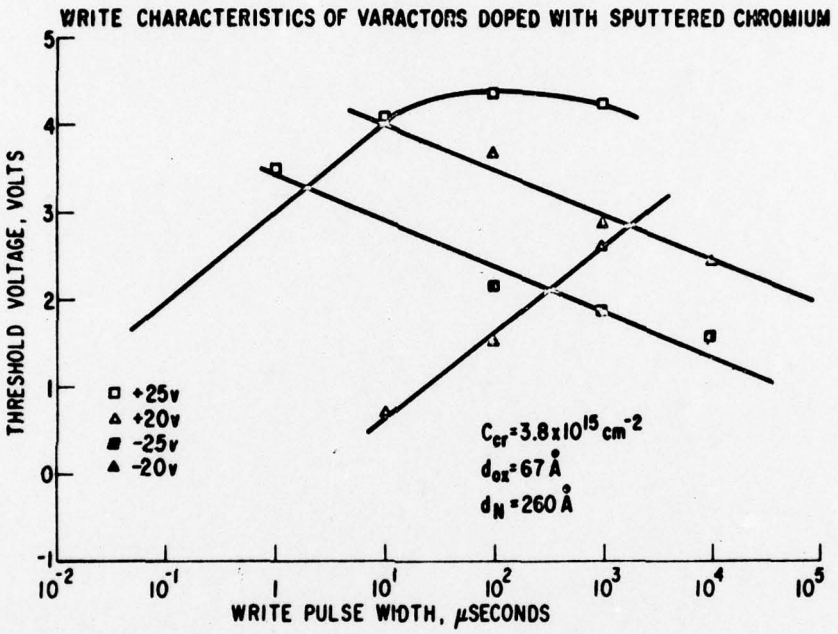

Figure 16. Write Characteristics of Varactors Doped with Sputtered Chromium

TABLE 5

Write Parameters

Dopant	Var. or Transistor	Dopant conc. x 10^{15} cm^{-2}	d_{ox}' A	d_{Nit}' A	Write slope V/dec + V_w	b_w' dec/volt + V_w	+ $V_{T,max}$ volts	W_{max}' volts	30 volt intersect. sec.	Fast Write
Chromium	V	2.95	53	452	1.80	0.43	12.5	13.0	1.5×10^{-4}	
	V	2.95	134	452	1.80	0.43	8.8	9.1	1.1×10^{-4}	
	V	8.6	53	452	1.70	0.43	10.4	10.7	1.8×10^{-6}	
	V	8.6	134	452	1.80	0.27	5.9	6.3	4.0×10^{-4}	
	V	1.32	88	372	1.80	0.31	10.5		3.1×10^{-4}	
	T	1.59	85	372	1.80	0.31	5.0	6.4	3.2×10^{-6}	
	T	1.1	43	263	1.45	0.43	3.8	5.8	8.0×10^{-9}*	F
	T	1.1	35	263	1.62	0.36	3.9	5.8	2.0×10^{-8}*	F
	T	1.1	57	263	1.72	0.53	> 4.1	> 6.4	4.0×10^{-7}*	F
	T	4.5	43	"	1.65	0.35	4.1	6.0	2.0×10^{-9}*	F
	T	5.4	50	"	2.55	0.36	5.4	8.6	3.5×10^{-7}*	F
	T	4.7	57	"	2.0	0.37	4.6	6.7	1.2×10^{-7}*	F
	T	1.59	85	372	1.8	0.31	5.0	6.4	3.2×10^{-6}	
	T	0.81	"	"	1.5	0.38	4.1	5.8	7×10^{-8}	
	T	3.9	"	"	1.48	0.36	5.4	7.1	1.4×10^{-8}	
Platinum	V	0.51	70	452	1.95	0.37	8.0	11.0	4.0×10^{-5}	
	V	0.42	113	452	1.95	0.35	8.5	11.5	8.0×10^{-4}	
	V	2.28	70	452	1.95	0.41	10.0	13.0	5.6×10^{-5}	
	V	2.10	134	452	1.95	0.34	9.6	12.1	4.0×10^{-3}	
	V	0.40	88	372	1.80	0.32	8.0	11.0	4.0×10^{-5}	
	T	0.27	85	372	1.3	0.48	3.2	5.4	2.5×10^{-6}	
	T	0	85	372	2.27	0.33	5.2	3.6	3.5×10^{-5}	
	T	1.1	85	372	2.2	0.35	4.6	9.2	2.5×10^{-7}	
	T	0.98	85	372	1.8	0.32	5.0	6.2	2.0×10^{-5}	
	T	0.12	58	320	1.3	0.48	4.4		1.5×10^{-7}*	F
Iridium	V	0.081	53	468	2.6	0.33	9.0	9.6	4.5×10^{-4}	
	V	0.081	80	"	2.3	0.44	9.0	9.3	1.8×10^{-3}	

	V	0.40	88	372	1.80	0.32	8.0	11.0	4.0 x 10	
	T	0.27	85	372	1.3	0.48	3.2	5.4	2.5×10^{-6}	
	T	0	85	372	2.27	0.33	5.2	3.6	3.5×10^{-5}	
	T	1.1	85	372	2.2	0.35	4.6	9.2	2.5×10^{-7}	
	T	0.98	85	372	1.8	0.32	5.0	6.2	2.0×10^{-5}	
	T	0.12	58	320	1.3	0.48	4.4		1.5×10^{-7}*	F
Iridium	V	0.081	53	468	2.6	0.33	9.0	9.6	4.5×10^{-4}	
	V	0.081	80	"	2.3	0.44	9.0	9.3	1.8×10^{-3}	
	V	1.09	80	"	2.1	0.50	9.0	14.0	1.1×10^{-3}	
	V	0.49	53	"	2.2	0.30	6.8	7.8	1.0×10^{-5}	
	V	0.21	58	320	1.6	0.48	6.2		4.0×10^{-7}	F
Tungsten		0.60	85	372	2.2	0.32	5.5	6.7	2.0×10^{-5}	
	V	0.55	63	450	1.3	0.43	8.0	9.0	8.0×10^{-2}	
	V	2.52	63	"	1.25	0.45	7.0	7.5	1.0×10^{-1}	
	V	2.52	94	"	1.0	0.41	6.5	7.3	2.0×10^{-1}	
	V	0.363	85	468	2.8	0.32	8.8	9.8	2.0×10^{-4}	
	V	0.363	53	"	2.7	0.36	8.8	9.1	3.0×10^{-5}	
WO_3	T	1.79	84	280	1.12	0.40	4.6	9.5	6.0×10^{-7}	
WO_3	V	1.94	58	320	0.9	0.92	7.7		2.0×10^{-9}	F
Palladium	V	0.47	70	452	1.93	0.32	7.5	9.5	1.0×10^{-3}	
	V	0.47	134	452	1.93	0.34	5.5	7.5	4.0×10^{-3}	
	V	4.2	70	452	1.93	0.40	7.0	7.0	4.0×10^{-5}	
	V	4.2	134	452	1.75	0.33	4.0	4.0	1.0×10^{-2}	
	T	0.86	85	372	1.63	0.33	3.3	5.3	1.7×10^{-5}*	F
	T	1.58	85	372	1.6	0.4	2.4	4.3	6.5×10^{-8}	
Nickel	V	0.266	53	468	2.0	0.49	9.5	5.0	10^{-3}	
	V	0.266	85	468	2.6	0.464	8.0	10.0	4.0×10^{-4}	
	V	1.22	53	468	2.5	0.33	9.5	12.0	2.0×10^{-4}	
	V	1.22	85	468	3.4	0.34	7.5	-	10^{-3}	
	V	0.66	58	320	1.8	0.34	6.1		2.0×10^{-8}	F

* Time of 25 V intersection instead of 30V intersection.

SECTION VI

DOPANT CONCENTRATION DEPENDENCE OF MEMORY WINDOW

Dopants were selected in accordance to their reactivity with oxygen. One metal, Ti, has an oxide more stable than SiO_2. Nb and Ta have oxides which are not reducible by hydrogen, while Cr, Mo, W, and Ni have oxides which are reducible by hydrogen. Three metals were chosen for their inertness toward oxidation: Pd, Ir, and Pt.

We have investigated the saturation memory window for 10 different dopants, namely, Pt, W, Ni, Cr, Ir, Pd, Nb, Ta, Mo, and Ti at various dopant surface concentrations between 10^{14} to 10^{16} cm^{-2} and in the oxide thickness range from 40 to 140 A. Reasonably large saturation memory windows were obtained in this range for six dopants: Pt, W, Ni, Cr, Ir and Pd.

The behavior displayed by Pt in Fig. 17 is somewhat typical for these six dopants. The saturation memory window is located principally at positive threshold voltages. The window tends to become smaller at dopant concentrations lower than 10^{14} cm^{-2}, and in some cases, but not always, a closing trend is observed beyond 10^{15} cm^{-2}. It should be noted that the oxide thickness has relatively little effect on the saturation memory window. The write voltage required to achieve the saturation window is higher for the thicker oxide devices, of course, but the maximum achievable window is not.

Behavior similar to Pt was found for W (Fig. 18), Ni (Fig. 19), Cr (Fig. 20), Ir (Fig. 21), and Pd (Fig. 22). An especially detailed picture was obtained for chromium at dopant concentrations between 10^{14} and 10^{15} cm^{-2}. It was found that in this range, somewhat surprisingly, the thinner oxide windows close faster with decreasing dopant concentration than the thicker oxides.

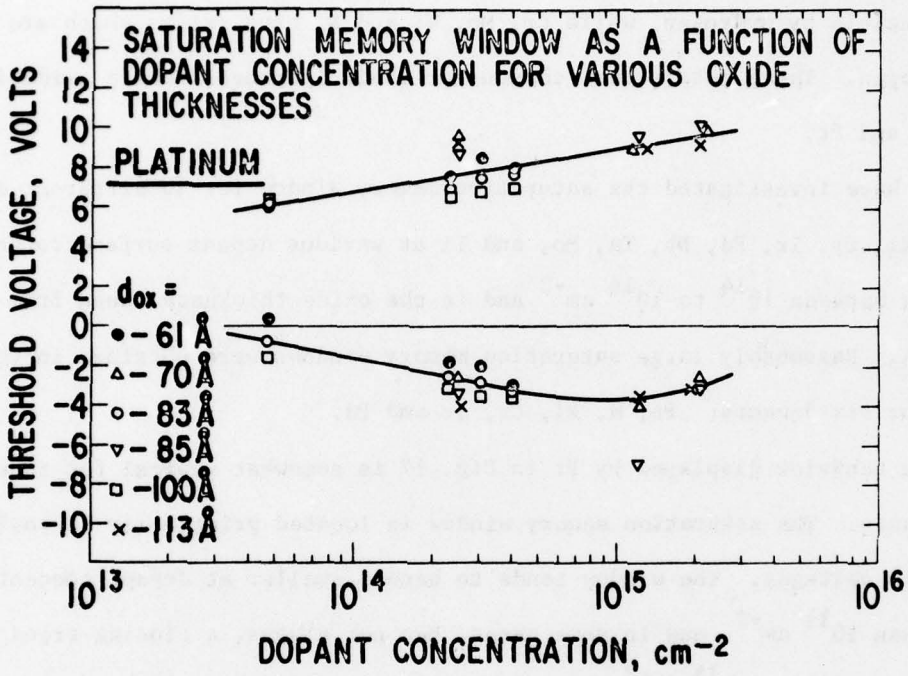

Figure 17. Platinum Saturation Memory Window vs. Dopant Concentration

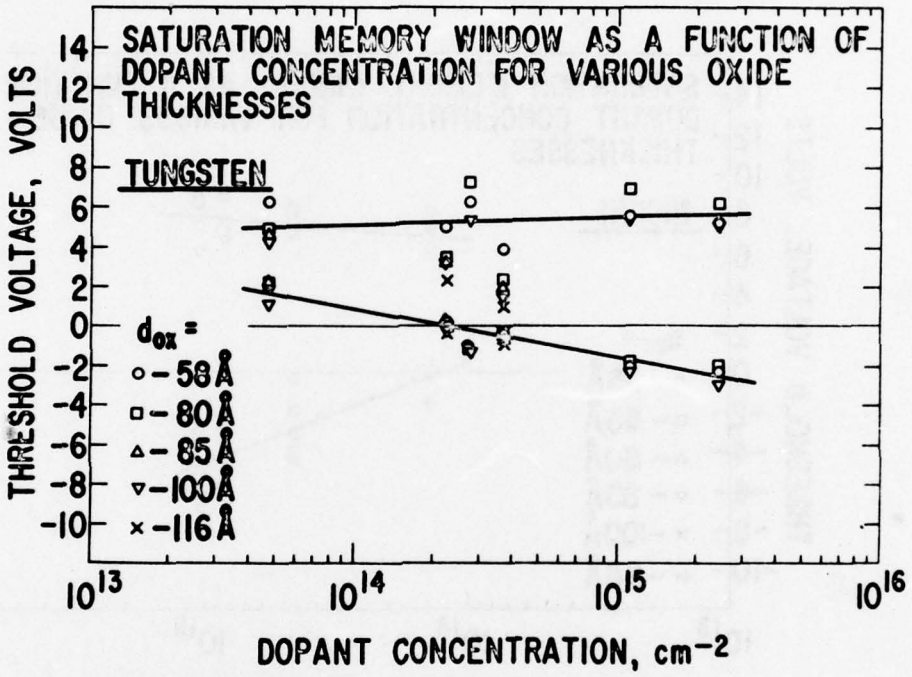

Figure 18. Tungsten Saturation Memory Window vs. Dopant Concentration

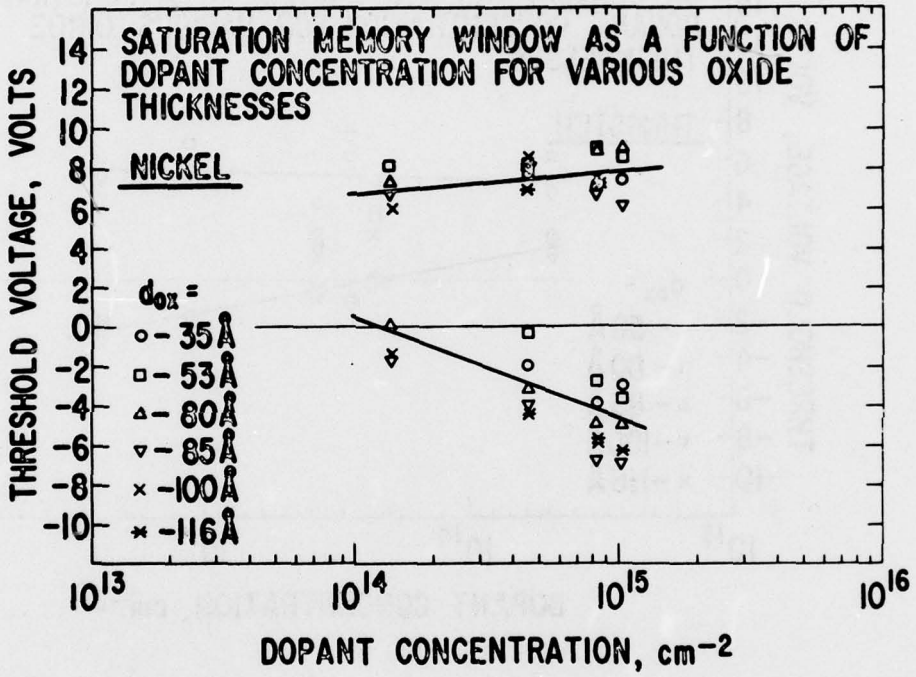

Figure 19. Nickel Saturation Memory Window vs. Dopant Concentration

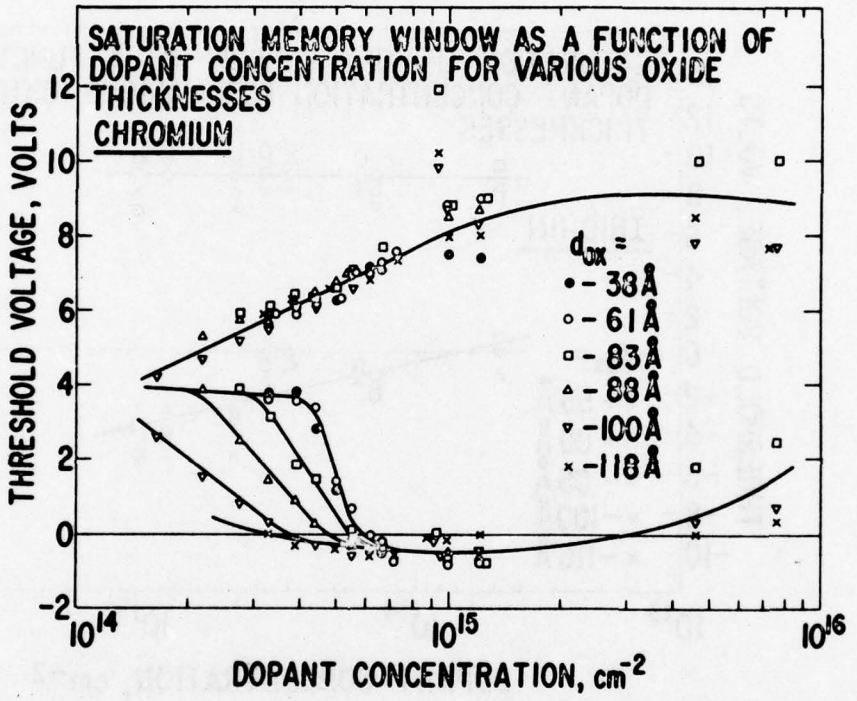

Figure 20. Chromium Saturation Memory Window vs. Dopant Concentration

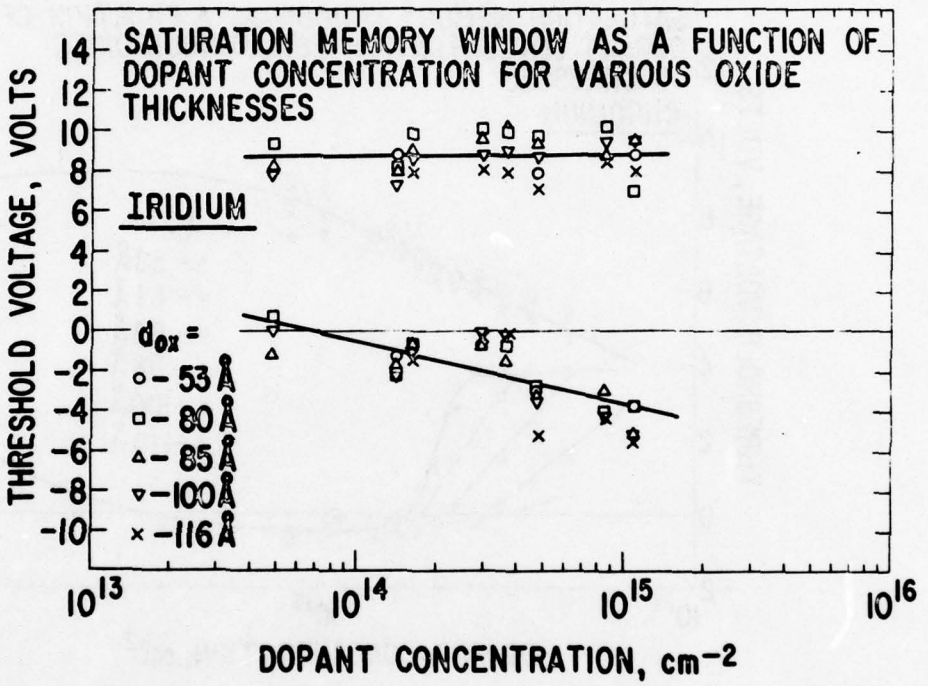

Figure 21. Iridium Saturation Memory Window vs. Dopant Concentration

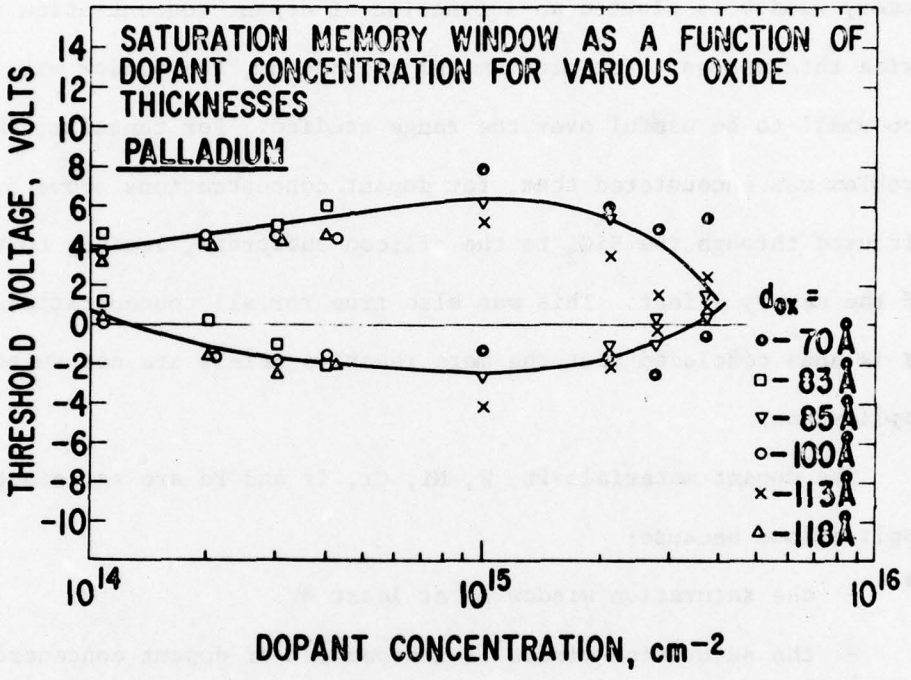

Figure 22. Palladium Saturation Memory Window vs. Dopant Concentration

These dopants give satisfactory memory windows for applications in arrays. It should be noted that the center voltage of the window indicates that they should be most useful as N-channel devices.

The use of niobium, tantalum, and molybdenum did not lead to satisfactory results. This is shown in Figs. 23, 24, and 25, respectively, in which the memory window is plotted as a function of dopant concentration for various oxide thicknesses. For niobium and molybdenum, the window was judged to be too small to be useful over the range studied. For tantalum, the additional problem was encountered that, for dopant concentrations above 5×10^{14} cm^{-2}, Ta diffused through the SiO_2 to the silicon substrate, leading to the disappearance of the memory effect. This was also true for all concentrations of Ti used. It is thus concluded that the more reactive metals are not suitable for memory application.

The dopant materials Pt, W, Ni, Cr, Ir and Pd are satisfactory for memory applications because:

- the saturation window is at least 8V
- the saturation window is independent of dopant concentration over at least a decade.
- there is minimum diffusion through the oxide
- there is no reaction with the oxide.

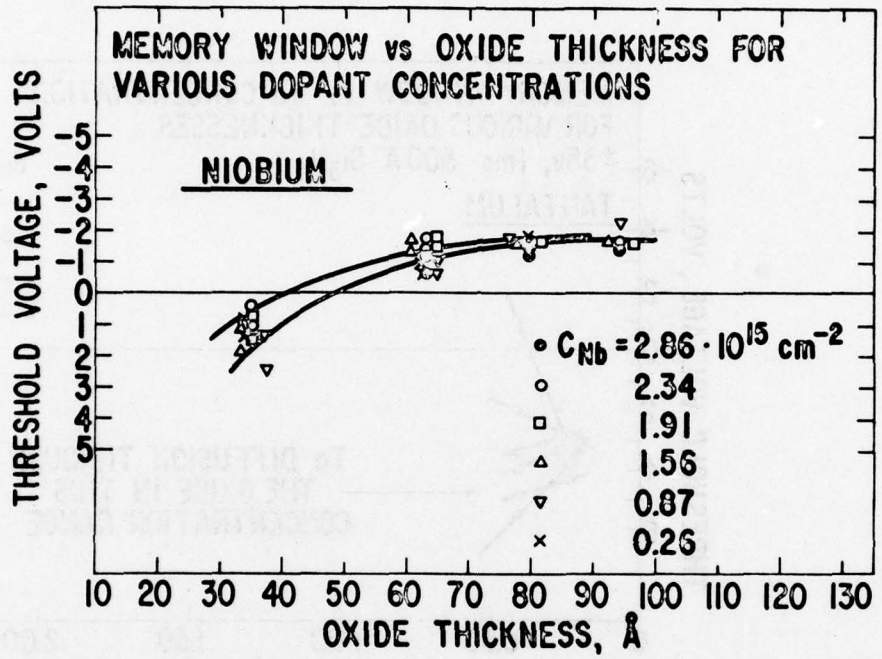

Figure 23. Niobium Memory Windows vs. Oxide Thickness

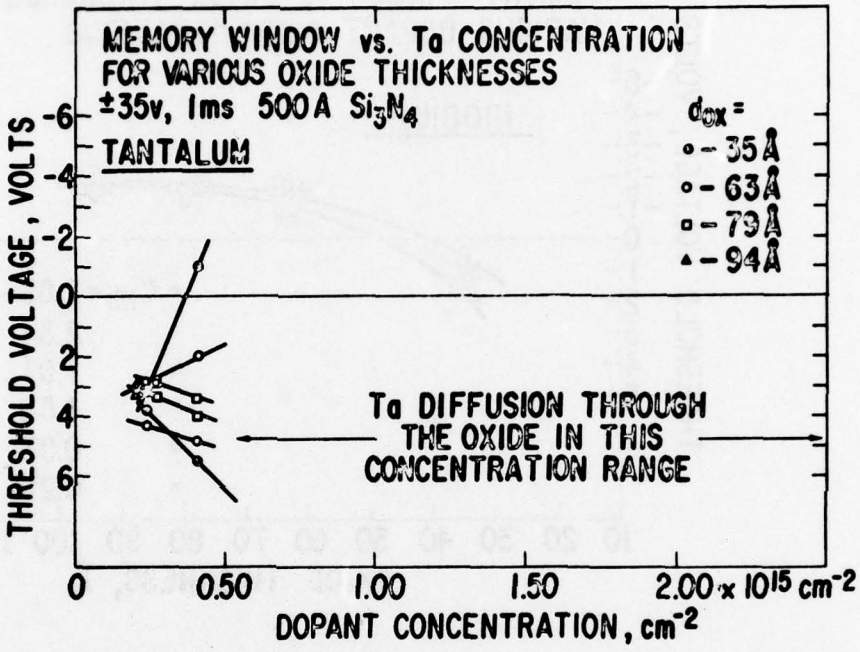

Figure 24. Memory Window vs. Tantalum Concentration

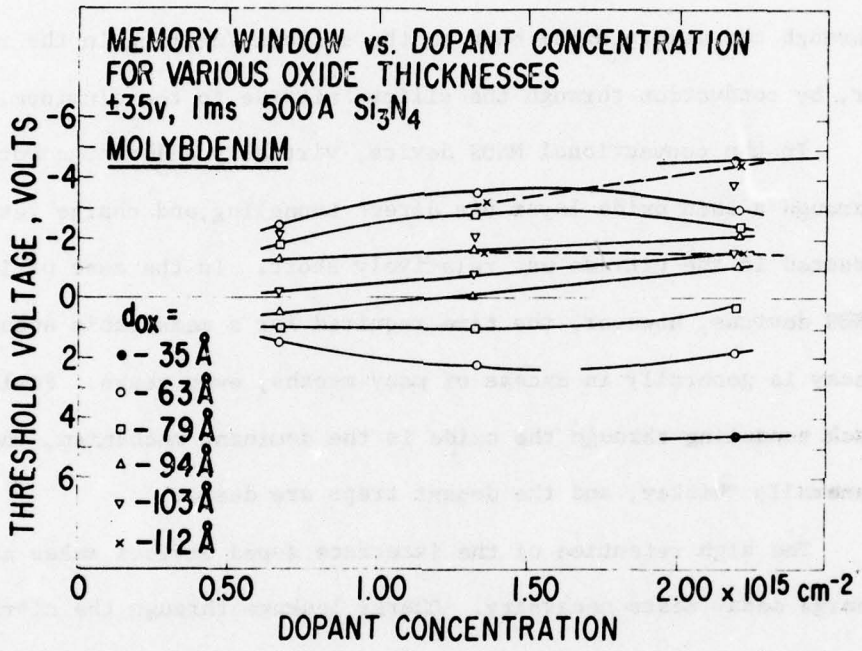

Figure 25. Molybdenum Memory Window vs. Dopant Concentration

SECTION VII

MEMORY RETENTION

After writing, the charge stored at the dopant sites tends to leak away from the oxide nitride interface in order to decrease the field created by its presence. Charge decay at the dopant sites can occur either by conduction through the memory oxide back to the silicon (writing in the reverse direction) or, by conduction through the silicon nitride to the aluminum.

In the conventional MNOS device, virtually all charge motion occurred through a thin oxide layer via direct tunneling,and charge retention in traps located in the nitride was relatively short. In the case of interface doped MNOS devices, however, the time required for a measurable amount of charge to decay is generally in excess of many months, even years. Fowler-Nordheim back tunneling through the oxide is the dominant mechanism, the oxide is generally thicker, and the dopant traps are deeper.

The high retention of the interface doped devices makes accelerated charge decay tests necessary. Charge leakage through the nitride or oxide, or both, can be accelerated by applying a gate bias voltage to increase the electric field. Conduction through the nitride alone can be accelerated by raising the temperature since it is an activated mechanism.

STORED CHARGE DECAY AS A FUNCTION OF TIME

In general, retention behavior parallels write behavior. It is characterized by a set of curves describing the decay of the threshold voltage as a function of time. The curves are linear on a log time plot over a considerable portion of the memory window. The following parameters are used to describe retention behavior. First there is the decay slope measured in volts/decade, which is analogous to the write slope, and which describes the rate at which the memory states change from one into the other with time for a specific accelerating bias. A second parameter is the spacing between the linear regions

of the characteristic curves, b_R, measured in decades of time per applied bias voltage difference. Thus b_R is quite analogous to b_w, the spacing between the write characteristic curves described earlier. Retention is further characterized by τ_{relax}, the extrapolated charge relaxation time for zero applied bias. The retention time itself, t_R, is the time after writing when memory is finally lost, i.e., the window is closed.

The procedure to estimate τ_{relax}, the time beyond which noticeable charge decay is observed, and also t_R, is as follows. After writing into a device to give a certain threshold voltage shift, normally 6 to 10 volts, an accelerating bias is applied to the gate. The bias is of a polarity opposite that of the writing voltage. In most cases, the retention of the positive threshold voltage state only was studied, since here the negative applied bias voltage adds to the internal field in the oxide due to the electrons stored at the interface. The positive memory state is then the most vulnerable to decay.

Under the applied bias, the threshold voltage decay is recorded as a function of time. When a decay of approximately 5 V has been observed, the measurement is repeated on a similar, neighboring device with a different bias voltage. One such measurement will yield the decay slope, but two are necessary to measure b_R. This procedure is illustrated in Fig. 26. The decay of the threshold voltage was followed for bias voltages of -21 V, -18 V and -16 V. It can be seen that τ_{relax} moves rapidly towards longer times as the bias voltage becomes smaller. Assuming that b_R remains constant down to $V_b = 0$, an extrapolated τ_{relax} ($V_b = 0$) is obtained by displacing τ_{relax} ($V_b = 16$)

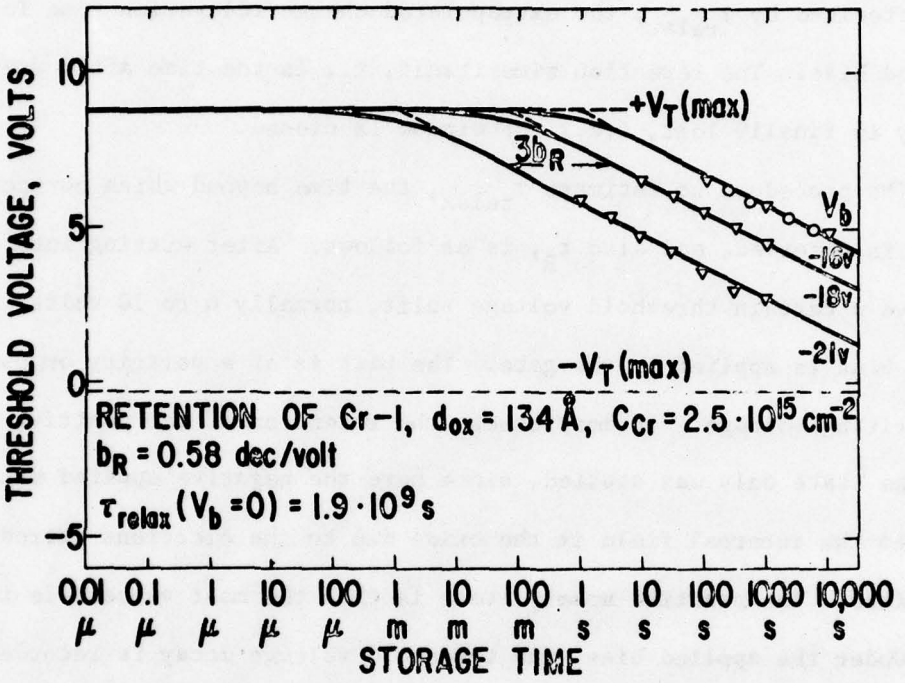

Figure 26. Retention of Chromium

to the right on the log time scale by the amount 16 x b_R. If it is also assumed that the decay slope is the same between 0 and -21 V, t_R can be estimated by drawing a line of the same decay slope from τ_{relax} (V_b = 0) to the V_T = 0 axis. The time marked by that intersection is taken to be t_R.

It should be noted that several of the measurements in Fig. 7-1 were carried out at 100°C instead of room temperature. These points coincide with the room temperature measurements indicating that at 100°C activated charge conduction through the nitride does not yet play a major role in these devices. As was found for the write characteristics curves, the decay slopes and spacings do not differ greatly from device to device over the range of dopants, concentrations, and oxide thicknesses investigated. Thus, the decay slopes are of the order of 2V/dec for poorly retaining devices and 1 V/dec for highly retaining ones. The spacing b_R varies from about 0.30 dec/volt for the less retentive devices to about 0.60 dec/volt for the more retentive ones. By far the most sensitive parameter is τ_{relax} (V_b = 0), which has been found to vary over nearly 20 orders of magnitude depending on doping and oxide thickness.

THE EFFECT OF OXIDE THICKNESS

τ_{relax} (V_b = 0) for the chromium doped device described in Fig. 7-1 is 1.9×10^9 seconds, or 60 years. This is not an uncommonly high value. Table 7-1 contains a list of the four important retention parameters, including τ_{relax} (V_b = 0), for devices studied in the course of Phase I of this program. τ_{relax} ranges from a low of 5.3 seconds to 8.5×10^9 years. This extreme variation in charge retention is largely a function of oxide thickness. If devices are compared in Table 7-1 which have the same dopant and concentration, there are many examples where the device with the thicker oxide has the higher retention.

TABLE 6

Retention Parameters for the Six Promising Dopants

Dopant	Dop. conc. $\times 10^{15}$ cm^{-2}	d_{ox}, Å	b_R, dec/volt	Decay slope volt/dec	Retention		
					τ_{relax}, secs	V_T initial*	t_R, sec
Cr-1	8.6	53	0.18	2.1	3×10^{1}	10V	3.2×10^{5}
"	2.95	53	0.36	2.7	3.5×10^{4}	10V	4.2×10^{7}
"	8.6	134	0.48	1.1	3.0×10^{5}	10V	5.7×10^{14}
"	2.95	134	0.58	1.1	5.0×10^{8}	10V	4.7×10^{17}
Cr-2	0.77	61	0.62	1.2	1.0×10^{10}	7V	1.2×10^{15}
"	0.77	134	0.50	1.2	5.0×10^{9}	7V	3.2×10^{14}
Cr-14 in	5.2	36	-	1.18	8×10^{1}	~ 4V	4.0×10^{5}
-14 in	1.1	36	-	1.18	5.3	3.5V	5.0×10^{3}
-15 in	1.1	50	0.45	1.13	8.7×10^{5}	5.3V	4.0×10^{10}
-15 in	5.4	50	0.45	1.4	1.0×10^{7}	5.2V	4.6×10^{10}
-14 out	5.2	43	-	1.0	8.5×10^{1}	5.4V	1.1×10^{8}
-14 out	1.1	43	0.38	1.34	3.1×10^{3}	5.15V	1.2×10^{7}
-15 out	1.1	57	1.0	0.68	8.0×10^{10}	5.2V	4.0×10^{18}
-15 out	5.4	57	1.0	0.72	3.0×10^{9}	5.7V	4.1×10^{17}
W-17	1.4	59	0.15	3.8	8.3×10^{2}	6.5V	4.0×10^{4}
"	0.23	59	0.13	3.8	3.2×10^{3}	6.5V	1.7×10^{5}
W-39	0.55	63	0.60	1.0	3.1×10^{12}	6.0V	1.0×10^{18}
"	2.5	63	0.34	1.8	7.6×10^{6}	6.0V	6.3×10^{9}
"	0.77	103	0.703	1.3	2.7×10^{17}	6.0V	4.5×10^{21}
"	2.5	103	0.46	2.1	6.3×10^{9}	6.0V	6.3×10^{12}
W-40	0.22	85	0.725	1.1	2.0×10^{11}	3.7V	8.8×10^{19}
-44 in	1.08	68	0.59	1.34	1.0×10^{9}	8.0V	3.0×10^{13}
-45 in	2.8	68	0.775	1.1	6.0×10^{14}	8.2V	1.1×10^{20}
-47	1.8	84	0.47	0.9	1.7×10^{7}	5.05V	2.2×10^{12}
-48	1.94	72	0.83	1.0	6.0×10^{11}	6.4V	2.9×10^{13}
"	1.94	58	0.64	1.27	4.8×10^{8}	6.35V	7.8×10^{13}
Ir-2	0.081	53	0.30	1.9	2.5×10^{4}	8V	4.0×10^{8}

"	0.77	103	0.703	1.3	2.7×10^{17}	6.0V	4.5×10^{21}
"	2.5	103	0.46	2.1	6.3×10^{9}	6.0V	6.3×10^{12}
W-40	0.22	85	0.725	1.1	2.0×10^{11}	3.7V	8.8×10^{19}
-44 in	1.08	68	0.59	1.34	1.0×10^{9}	8.0V	3.0×10^{13}
-45 in	2.8	68	0.775	1.1	6.0×10^{14}	8.2V	1.1×10^{20}
-47	1.8	84	0.47	0.9	1.7×10^{7}	5.05V	2.2×10^{12}
-48	1.94	72	0.83	1.0	6.0×10^{11}	6.4V	2.9×10^{13}
"	1.94	58	0.64	1.27	4.8×10^{8}	6.35V	7.8×10^{13}
Ir-2	0.081	53	0.30	1.9	2.5×10^{4}	8V	4.0×10^{8}
"	0.081	80	0.67	1.1	2.3×10^{12}	8V	1.0×10^{19}
Ir-1	1.09	80	0.39	1.6	1.8×10^{6}	8V	6.0×10^{11}
"	1.09	53	-	1.7	5×10^{-2}	8V	2.0×10^{3}
Ir-7	0.15	72	0.73	0.88	6.8×10^{9}	4.85V	6.3×10^{12}
"	0.15	58	0.63	0.65	1.4×10^{6}	4.05V	1.2×10^{14}
Ni-4	0.266	53	0.31	1.3	1.7×10^{5}	8V	1.7×10^{11}
"	1.22	53	0.35	1.6	2.1×10^{4}	8V	2.1×10^{9}
"	0.266	85	0.77	0.7	1.3×10^{10}	8V	1.0×10^{19}
"	1.22	85	0.91	0.8	1.2×10^{12}	8V	1.0×10^{21}
Ni-10	2.37	72	0.75	0.94	9.0×10^{7}	4.7V	7.3×10^{12}
"	0.53	58	0.88	0.63	5.8×10^{8}	4.05V	1.2×10^{15}
Pd-1	1.85	70	0.16	2.1	1.0×10^{2}	7.5V	1.0×10^{6}
"	3.5	70	0.41	1.6	5.0×10^{3}	7.5V	1.0×10^{8}
"	1.85	100	0.26	1.3	1.6×10^{4}	4V	1.6×10^{8}
"	3.5	100	0.33	0.73	6.0×10^{5}	4V	6.0×10^{9}
Pt-10	0.37	61	0.33	1.71	3.0×10^{3}	7V	3.0×10^{7}
"	0.37	88	0.86	0.80	2.4×10^{12}	7V	2.0×10^{20}
"	1.94	70	0.69	0.90	6.5×10^{11}	7V	1.0×10^{18}
"	1.94	100	0.57	1.11	3.5×10^{9}	7V	3.5×10^{15}

TABLE 6 Concluded

Dopant	Dop. conc. $\times 10^{15}$ cm^{-2}	d_{ox}, Å	b_R, dec/volt	Decay slope volt/dec	Retention		
					τ_{relax}, secs	V_T initial*	t_R, sec
Pt-11	1.1	85	1.0	0.67	2.2×10^{14}	5.2V	1.3×10^{21}
"	0.27	85	0.95	1.7	1.7×10^{13}	4.8V	6.0×10^{19}
Pt-16	0.16	72	1.18	0.52	1.2×10^{11}	4.4V	2.6×10^{14}
"	0.12	58	0.7	0.65	3.0×10^{6}	3.8V	2.4×10^{12}
Pd-3	0.18	85	1.13	0.42	2.6×10^{12}	3.8V	8.0×10^{20}
"	1.58	85	1.1	0.4	4.0×10^{13}	3.5V	1.1×10^{22}
Cr-4	0.81	85	0.87	0.77	5.1×10^{11}	5.1V	2.0×10^{18}
"	3.9	85	0.76	1.0	3.5×10^{10}	5.5V	9.0×10^{15}

* Positive threshold voltage from which decay is measured.

Figure 27 illustrates the relationship between oxide thickness and τ_{relax} and t_R for chromium doped devices. It can be seen that they depend strongly on oxide thickness.

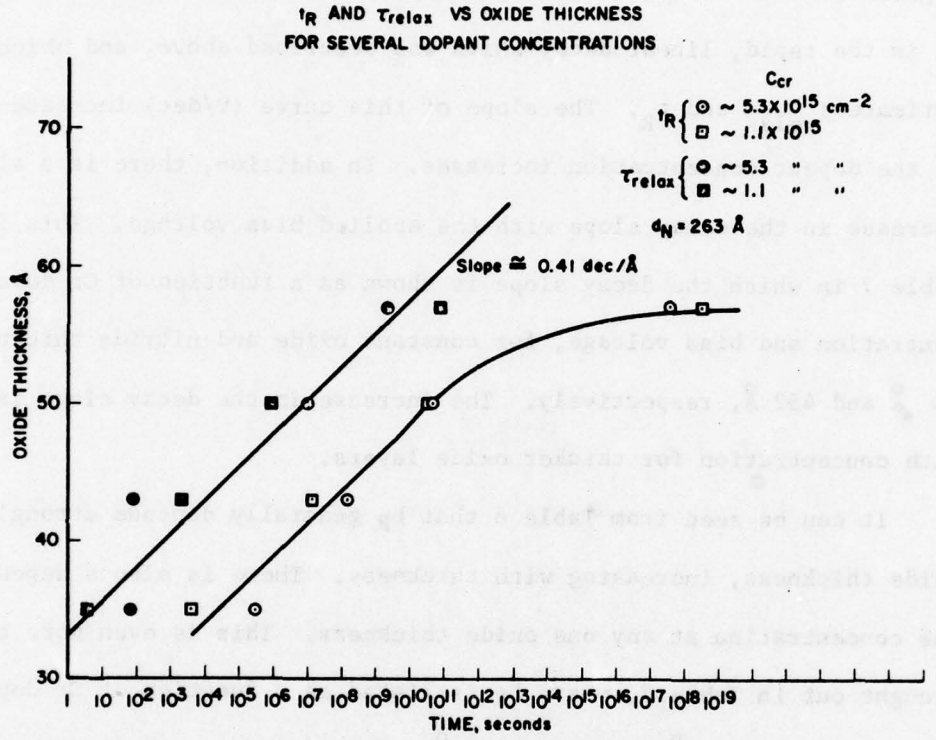

Figure 27. t_R and τ_{relax} vs. Oxide Thickness

THE EFFECT OF DOPANT CONCENTRATION

The decay of a written threshold voltage at some applied gate bias is at first quite rapid(linear portion on the log time plot), but then, as it approaches zero volts, the decay becomes much slower (nonlinear in log time). It is the rapid, linear decay which was described above, and which is used to estimate τ_{relax} and t_R. The slope of this curve (V/dec) increases slightly as the dopant concentration increases. In addition, there is a slight increase in the decay slope with the applied bias voltage. This is shown in Table 7 in which the decay slope is shown as a function of Cr dopant concentration and bias voltage, for constant oxide and nitride thicknesses of 70 Å and 452 Å, respectively. The increase in the decay slope is more rapid with concentration for thicker oxide layers.

It can be seen from Table 6 that b_R generally depends strongly on the oxide thickness, increasing with thickness. There is also a dependence on the concentration at any one oxide thickness. This is even more clearly brought out in Table 8, where b_R is listed as a function of Cr dopant concentration for 100 Å oxide and 452 Å nitride devices. It is seen that between 1.8 and $5.9 \cdot 10^{15}$ cm^{-2}, b_R decreases only slowly, but it decreases rapidly as the concentration increases above $5.9 \cdot 10^{15}$ cm^{-2}. It is also seen in Table 8 that b_R is a slow function of the bias voltage applied during the accelerated retention measurement, increasing with decreasing bias. This means that the estimates made in Table 6 to obtain τ_{relax} ($V_b = 0$) and t_R are conservative.

TABLE 7

VARIATION OF DECAY SLOPE WITH CONCENTRATION

OF DOPANT AT 70A OXIDE THICKNESS

Decay Slope	Bias Voltage	Dopant Concentration
0.75V/dec	-19V	3.3×10^{15} cm^{-2}
0.92	-19	5.9
1.07	-19	8.8

TABLE 8

VARIATION OF "b_R" WITH DOPANT CONCENTRATION

AT 100A OXIDE THICKNESS

Dopant Concentration	-19V & -21V	-19V & -25V	-21V & -25V
1.8×10^{15} cm^{-2}	0.75 dec/V	0.64 dec/V	0.59 dec/V
5.9	0.53	0.54	0.55
8.8	0.22	0.11	0.27

The effect of dopant concentration on decay slope and b_R is illustrated in Fig. 28. As the dopant concentration increases, τ_{relax} decreases for several oxide thicknesses and applied voltages, as a result of a decreasing b_R and increasing decay slope.

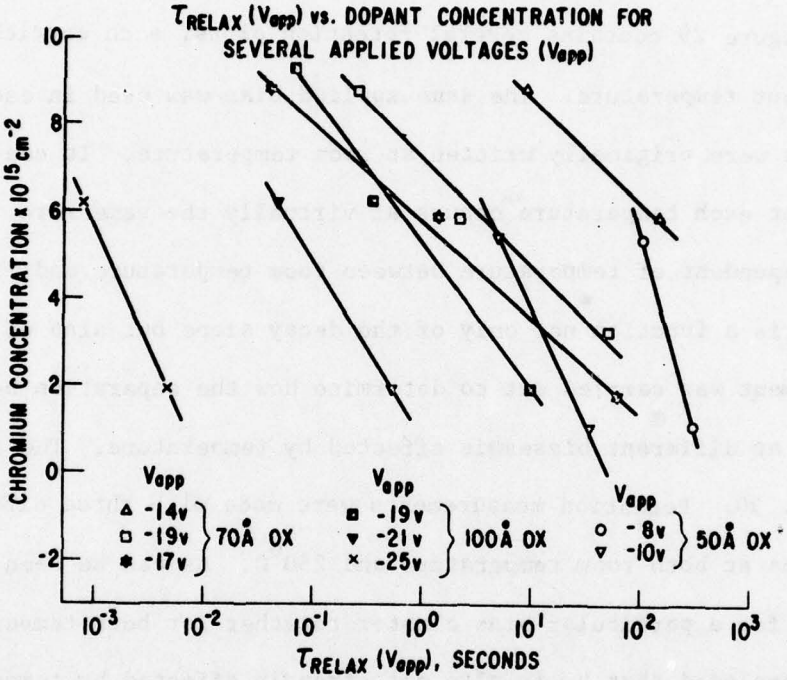

Figure 28. τ_{relax} (V_{app}) vs. Dopant Concentration

TEMPERATURE DEPENDENCE

As pointed out above, one possible charge decay mechanism, namely conduction through the nitride, is strongly temperature dependent. However, it was found here that within the temperature range studied, -196°C to 250°C, back tunneling is the dominant mechanism.

Figure 29 contains several retention plots, each carried out at a different temperature. The same applied bias was used in each case and all devices were originally written at room temperature. It can be seen that decay at each temperature occurs at virtually the same rate. The decay slope is independent of temperature between room temperature and 200°C. Since τ_{relax} is a function not only of the decay slope but also of b_R, another experiment was carried out to determine how the separation between decay curves at different biases is affected by temperature. The results are shown in Fig. 30. Retention measurements were made with three different bias voltages at both room temperature and 250°C. As can be seen, threshold voltage values for a particular bias cluster together for both temperatures. It is thus concluded that b_R is also not strongly affected by temperature, at least to a first order approximation.

To further test the temperature dependence, retention tests were made at liquid nitrogen temperature. Figure 31 contains the results of two retention tests. In one test the bias voltage was applied at room temperature. In the second test, bias was applied at 77°K. This curve was corrected for a voltage shift due to fast surface state generation (see below). Even at 77°K therefore, charge decay does not occur at a significantly different rate than at room temperature, indicating charge decay due to back tunneling only.

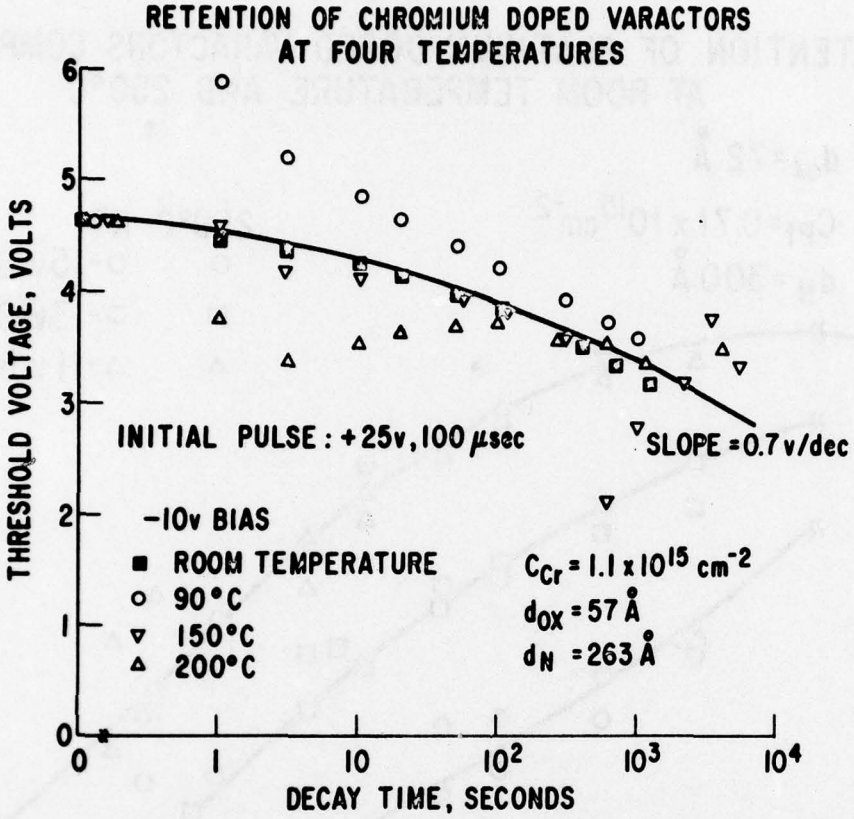

Figure 29. Chromium Retention at Four Temperatures

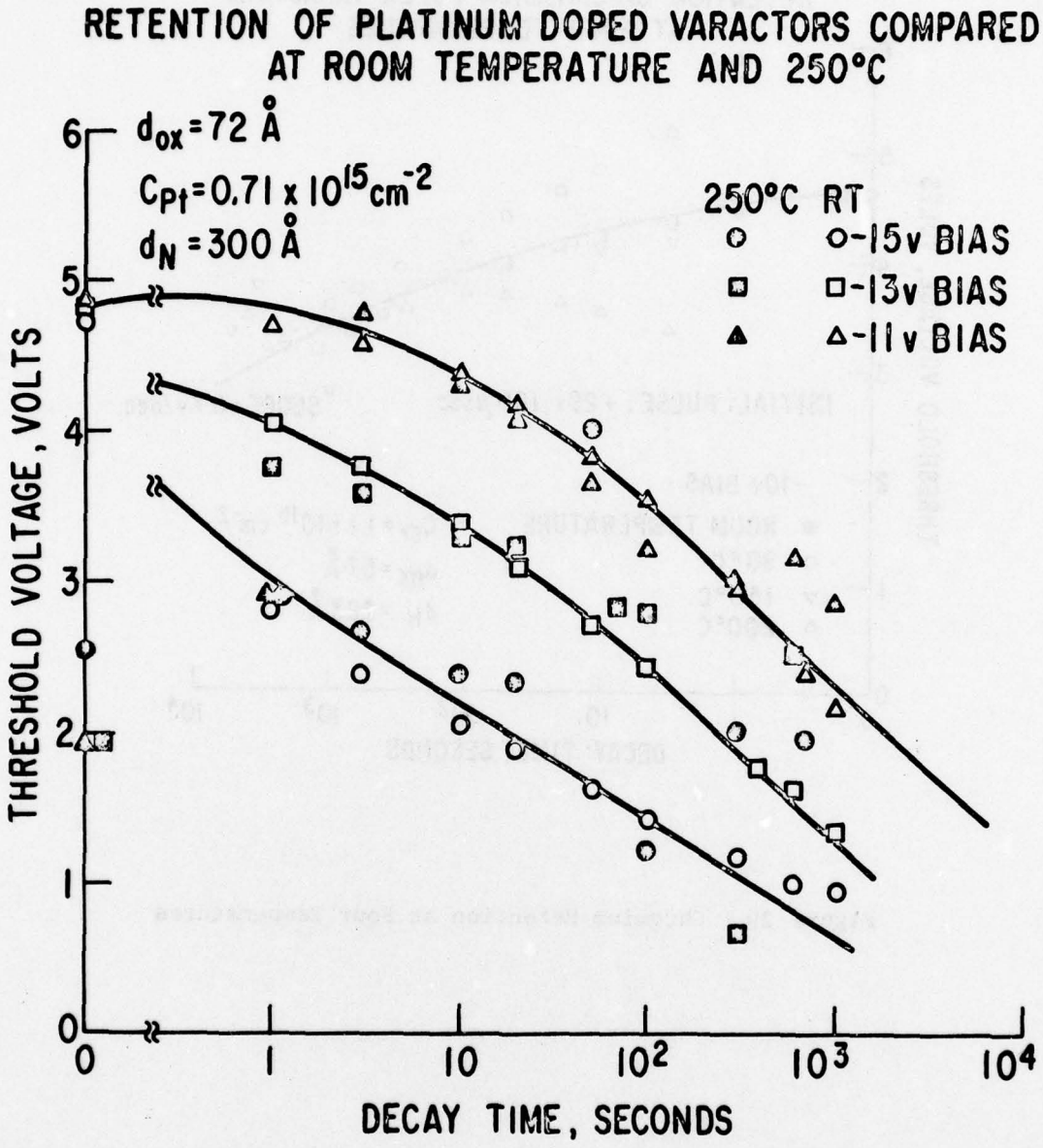

Figure 30. Platinum Retention at Room Temperature and 250°C

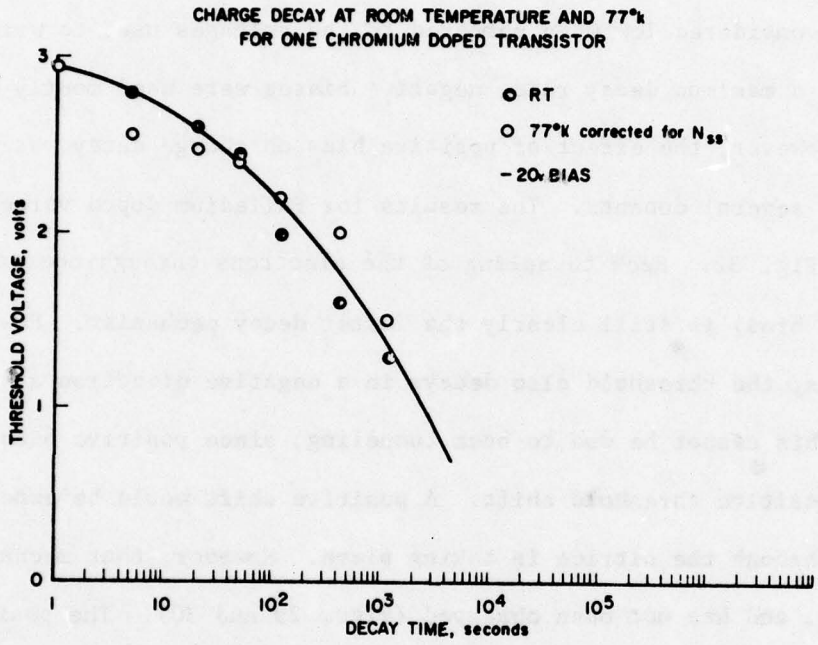

Figure 31. Charge Decay at Room Temperature and 77°K

In conclusion, the retention of metal doped MNOS devices is independent of temperature between -196°C and 250°C, at least to a first order approximation.

THE EFFECT OF HIGH POSITIVE APPLIED VOLTAGES

Most retention tests are made at room temperature and with applied biases that are considered low when compared to the voltages used to write the devices. To obtain a maximum decay rate, negative biases were used mostly for retention tests. However, the effect of positive bias on charge decay was also investigated for several dopants. The results for Palladium doped varactors are shown in Fig. 32. Back tunneling of the electrons through the oxide (negative bias) is still clearly the faster decay mechanism. However, at +20 volts bias, the threshold also decays in a negative direction at room temperature. This cannot be due to back tunneling, since positive bias should yield a positive threshold shift. A positive shift would be expected if conduction through the nitride is taking place. However, that mechanism is highly activated, and has not been observed (Figs. 29 and 30). The positive shift is thus believed to be caused by the third threshold shift mechanism, which is always characterized by the formation of large numbers of fast surface states. As shown in Fig. 32, measurements at room temperature and 77°K show the generation of such surface states with time. Indeed, after 100 seconds of applied bias, surface states are increasing at a rapid rate.

Platinum doped varactors showed similar results. In Fig. 33, note again that back tunneling is the fastest decay mechanism. At positive bias, more and more surface states are generated with time. No surface state formation occurs for comparable negative biases.

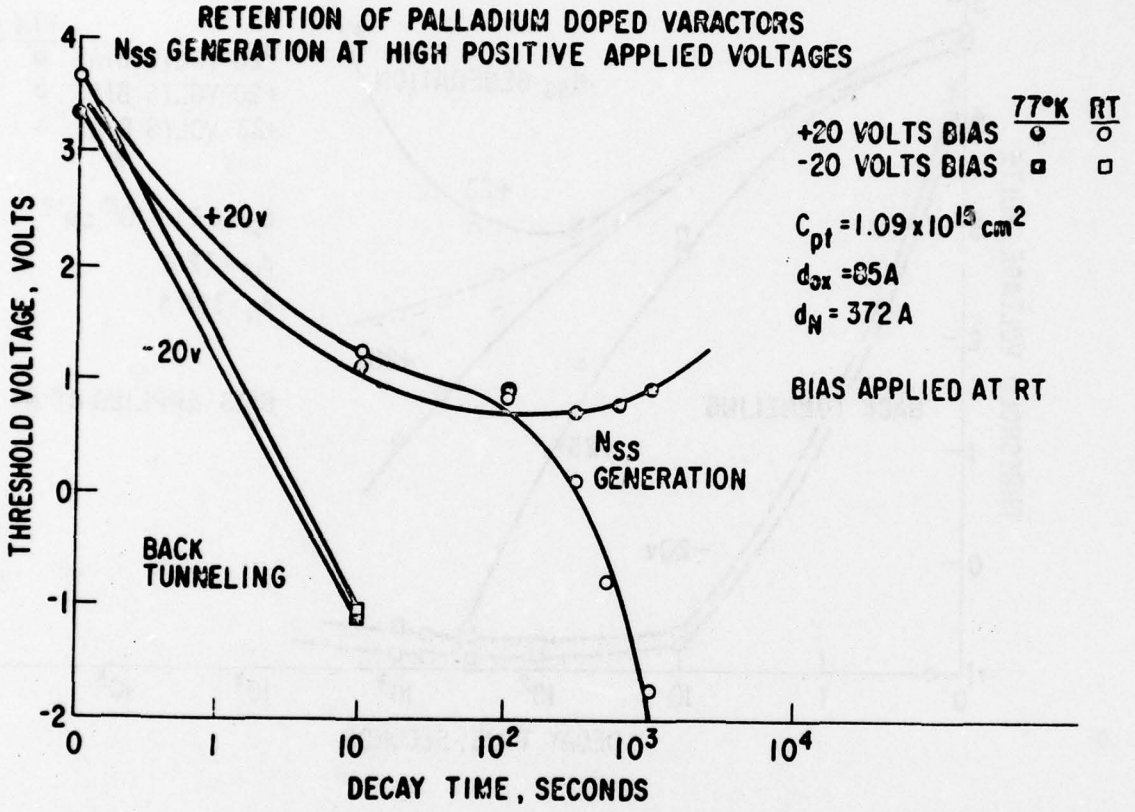

Figure 32. Palladium Retention at High Positive Applied Voltages

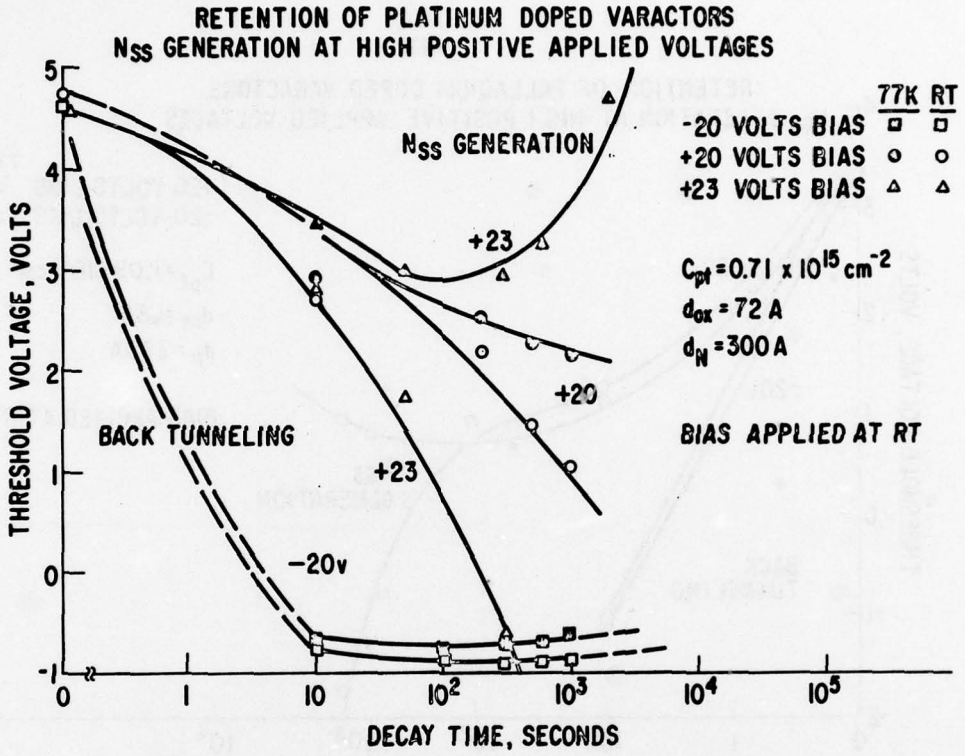

Figure 33. Platinum Retention at High Positive Applied Voltages

THE EFFECT OF ENDURANCE CYCLING

The retention of conventional, undoped MNOS devices is strongly reduced by write/erase cycling. To determine the impact of endurance cycling on interface doped devices, a retention test was made on a varactor before and after cycling 1000 times. That number was chosen because it approximated the effective endurance of the device (see below). The results are shown in Fig. 34. There is a distinct difference between the retention curve made before cycling and the one made after cycling. The latter is shifted by an almost constant amount in the negative direction. However, when the threshold voltage measurement on the cycled device was repeated at $77^{o}K$, it was found that practically the entire negative shift was the result of surface state generation. Thus it appears that charge decay is independent of write/erase cycling to 1000 cycles, but the formation of surface states during cycling causes the room temperature threshold voltage to be reduced. Fast surface state generation in relation to write/erase cycling is discussed in a later section.

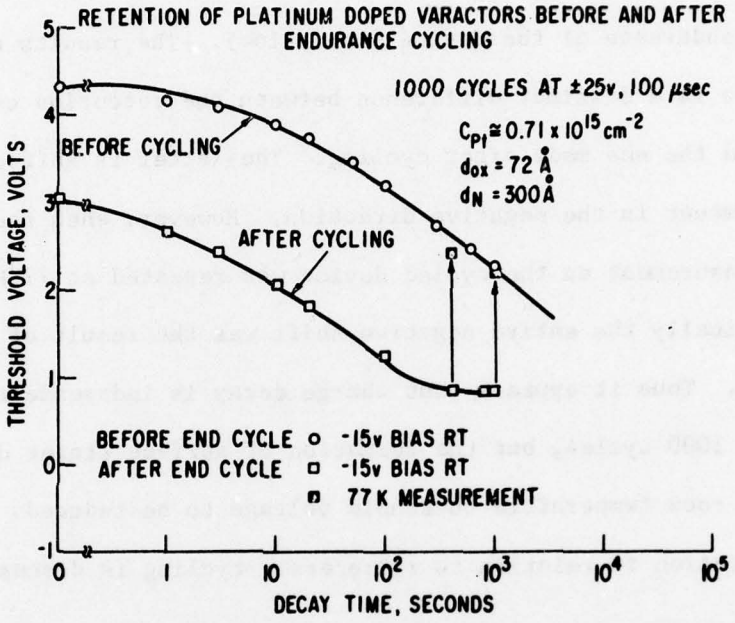

Figure 34. Platinum Retention Before and After Endurance Cycling

SECTION VIII

FAST SURFACE STATE GENERATION

It was found in the course of this study that fast surface states could be generated in interface doped devices by two methods: Prolonged application of high positive voltages, and write/erase cycling. These are now described.

SURFACE STATE GENERATION UNDER PROLONGED BIAS

Up to a voltage on the gate of about 20 V, fast surface state generation is generally negligible, except if the bias is applied for very long times ($>$ 1000 sec). This is illustrated in Fig. 35, where the threshold voltage is plotted as a function of time with the applied biases shown. The measurement of V_T was carried out at room temperature and liquid nitrogen temperature, but the bias was applied only at room temperature. It can be seen that at least to 1000 sec, the room temperature and liquid nitrogen threshold roughly coincide for each bias, except for +19V, where they begin to diverge from 100 sec on, indicating an increasing rate of surface state generation at that bias. We use here the method of Brown and Gray [3], which relates the density of fast states to the flat band voltage shift between room and liquid nitrogen temperature.

Devices on the same wafer were subjected to even higher bias, as shown in Fig. 36. Here a definite divergence of the liquid nitrogen and room temperature threshold voltages can be observed after about 30 sec, for positive voltages above +20V, indicating the generation of a very large number of fast surface states, rising to about 10^{13} cm^{-2} at 1000 sec. Note that no surface states are generated at -20V.

Figure 37 shows fast surface states generated at +25 in tungsten doped varactors.

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[3] P.V. Gray and D.M. Brown, Applied Physics Letters, Vol. 7, 108 (1965).

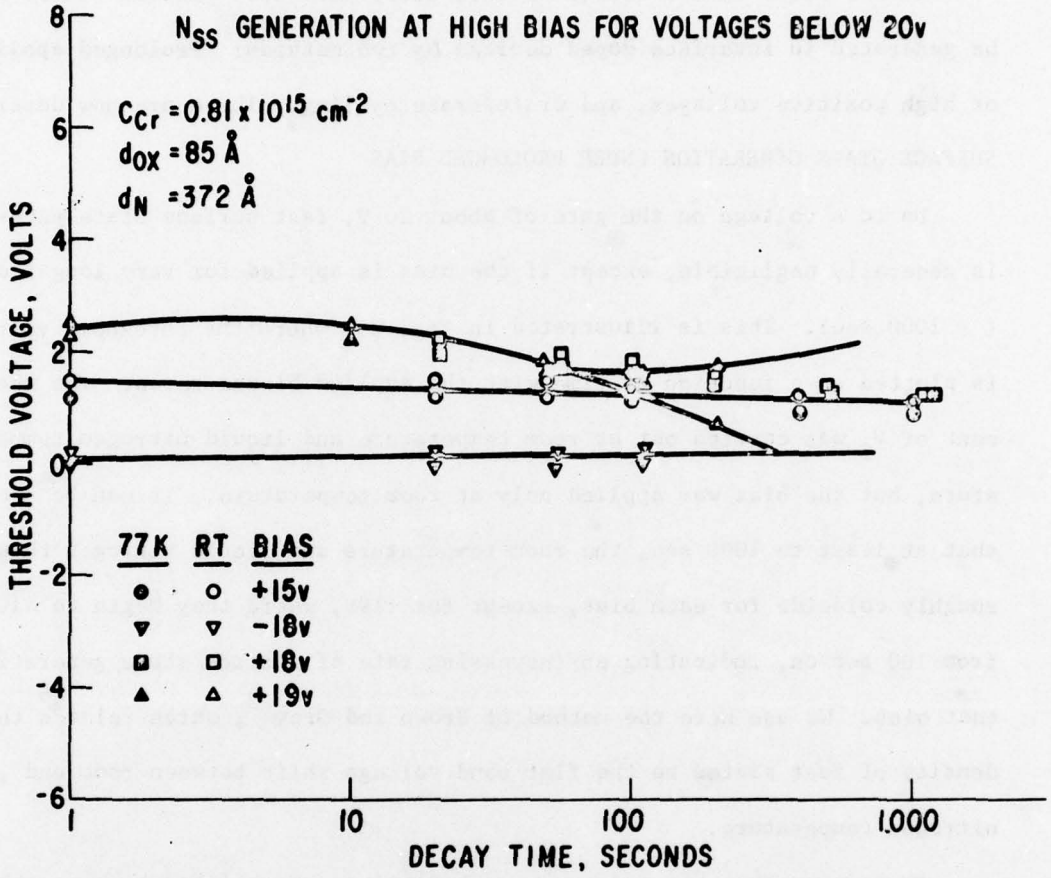

Figure 35. N_{ss} Generation at High Bias for Voltages Below 20V

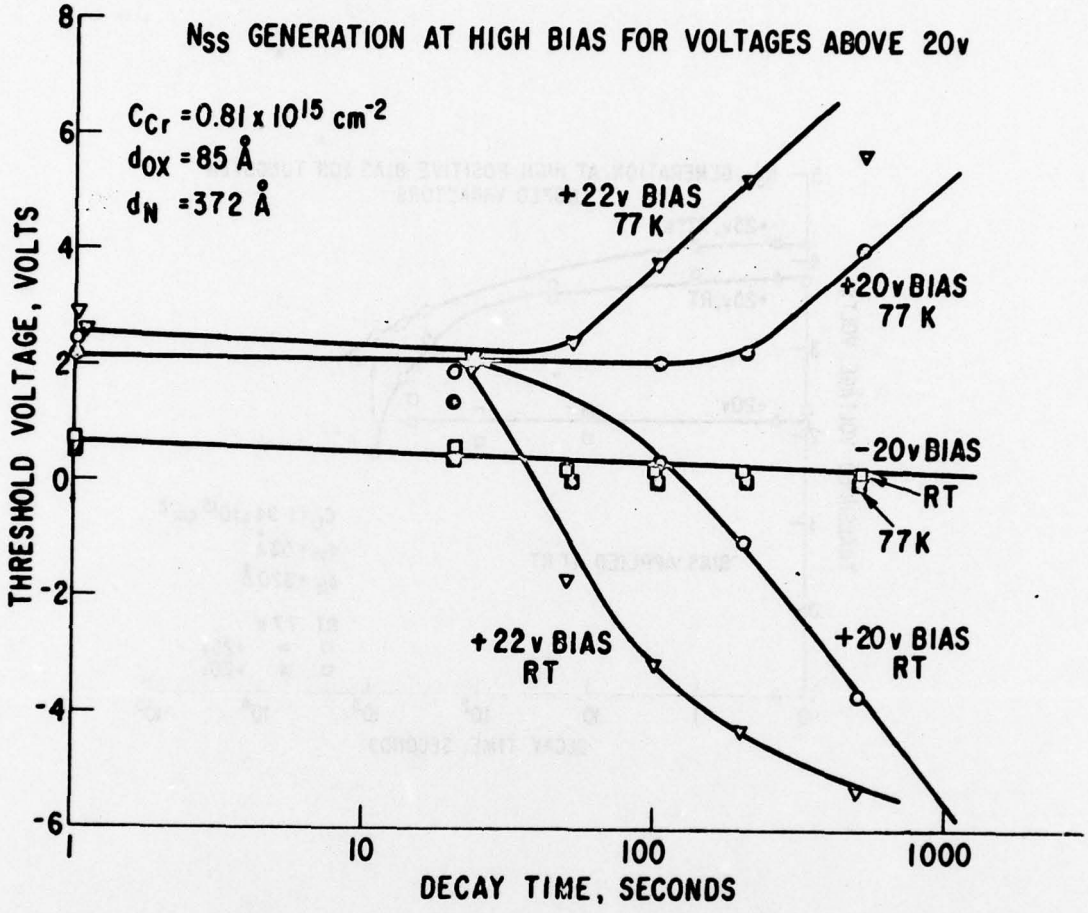

Figure 36. N_{ss} Generation at High Bias for Voltages Above 20V

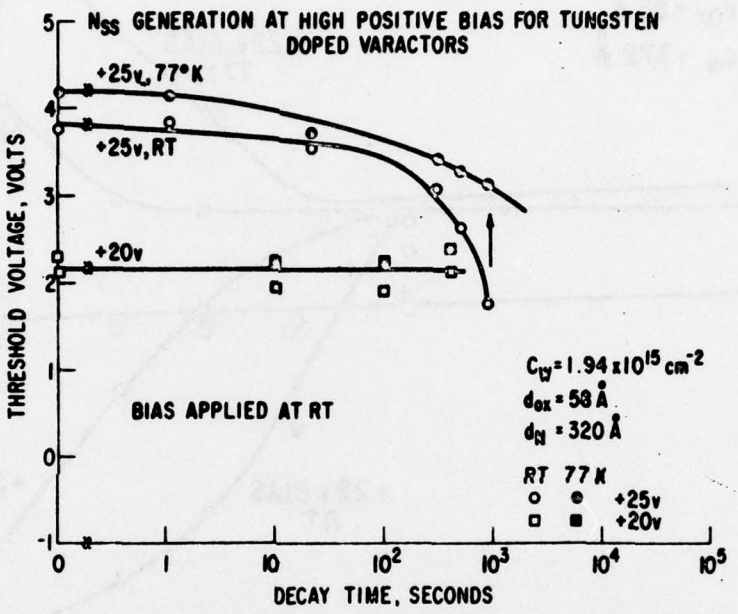

Figure 37. N_{ss} Generation at High Positive Bias for Tungsten Doped Varactors

SURFACE STATE GENERATION DUE TO WRITE/ERASE CYCLING

In write/erase cycling above 1000 cycles, severe distortion of the C-V curve is observed, indicating a large number of surface states. The surface state density of a chromium doped device is shown in Fig. 38 as a function of write/erase cycling. It can be seen that the surface state density increases sharply after 1000 cycles, increasing from $3 \cdot 10^{11}$ for the original device before cycling to $11.2 \cdot 10^{12}$ after 5000 cycles, and it increases at the same rate for both memory states.

In Fig. 39, the two memory states are plotted after they were measured at room temperature and liquid nitrogen temperature, as a function of the write/erase dose. It is observed that while the center voltage as measured at room temperature decreases with write/erase cycling, the center voltage as measured at liquid nitrogen temperature increases. However, the memory window is identical for the two temperatures up to at least 100 cycles. The number of write/erase cycles required for significant deviation of the center voltage and significant window closure coincides with the number of cycles at which the surface state density begins to increase sharply.

In Fig. 39, it can be seen that the behavior of the $-V_T$ memory state is quite different from that of the $+V_T$ state. At room temperature the $-V_T$ state remains about constant at -1V as write/erase cycling proceeds to 10^4 cycles. However, the same state remeasured at $77^{\circ}K$, shows increasingly more positive values beyond 100 cycles. The corresponding band diagram showing the introduction of surface states in the band gap is shown to the left in Fig. 40.

The behavior is just reversed for the $+V_T$ memory state in Fig. 39. Here the room temperature value drops sharply with cycling beyond 100 cycles, while the $77^{\circ}K$ value remains about constant at +7V. This situation requires a more complicated explanation than the $-V_T$ behavior. An attempt is made in

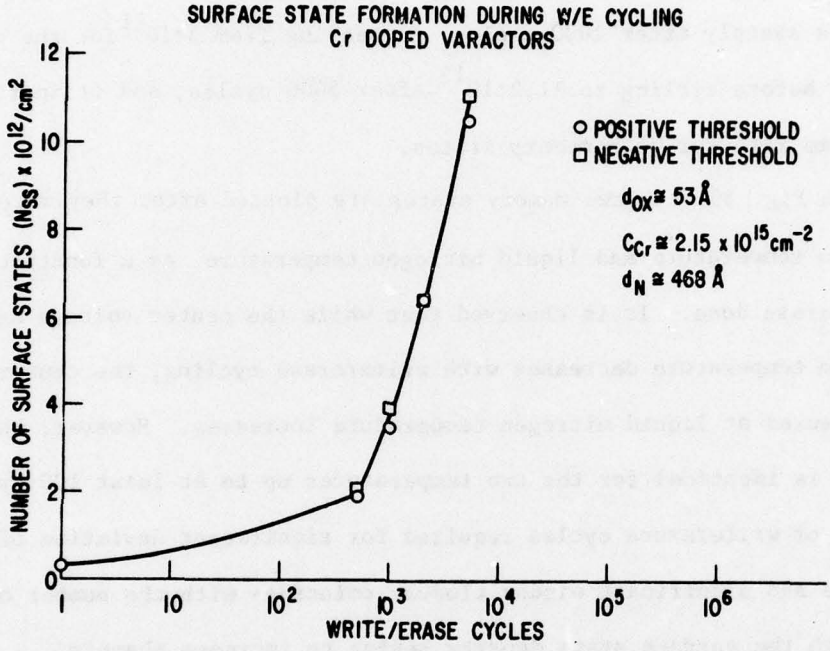

Figure 38. Surface State Formation During Write Erase Cycling

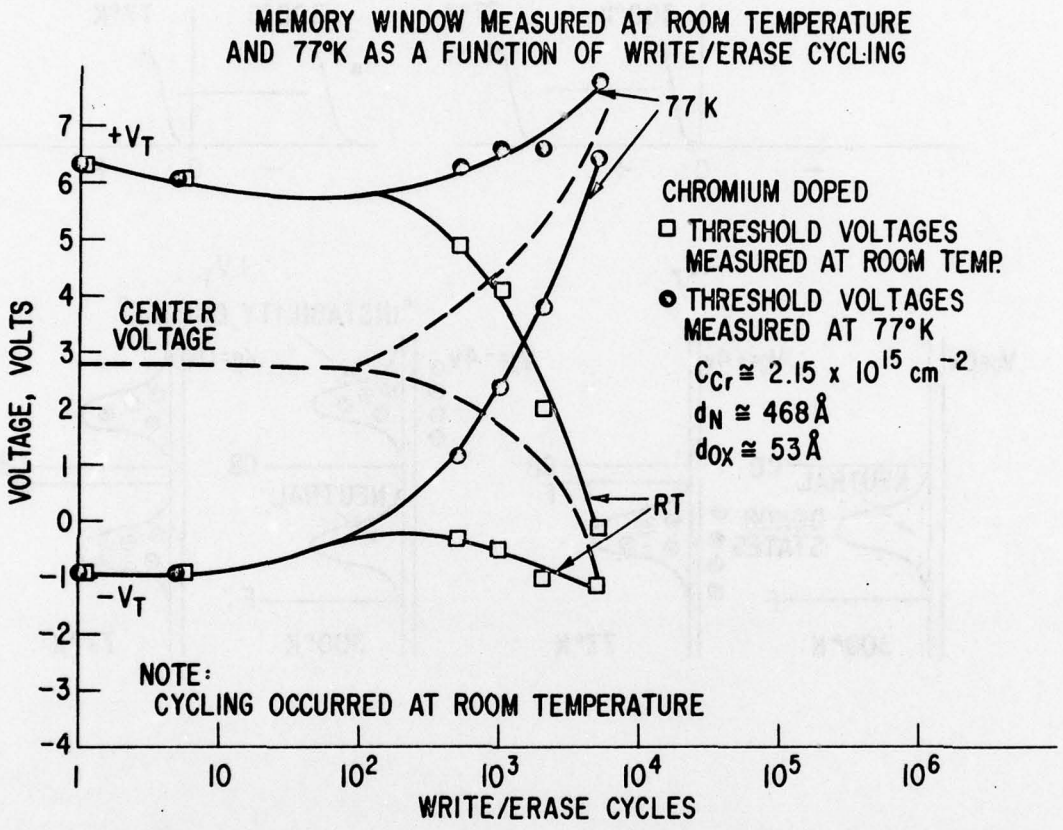

Figure 39. Memory Window Measured at Room Temperature and 77°K vs. Write/Erase Cycles

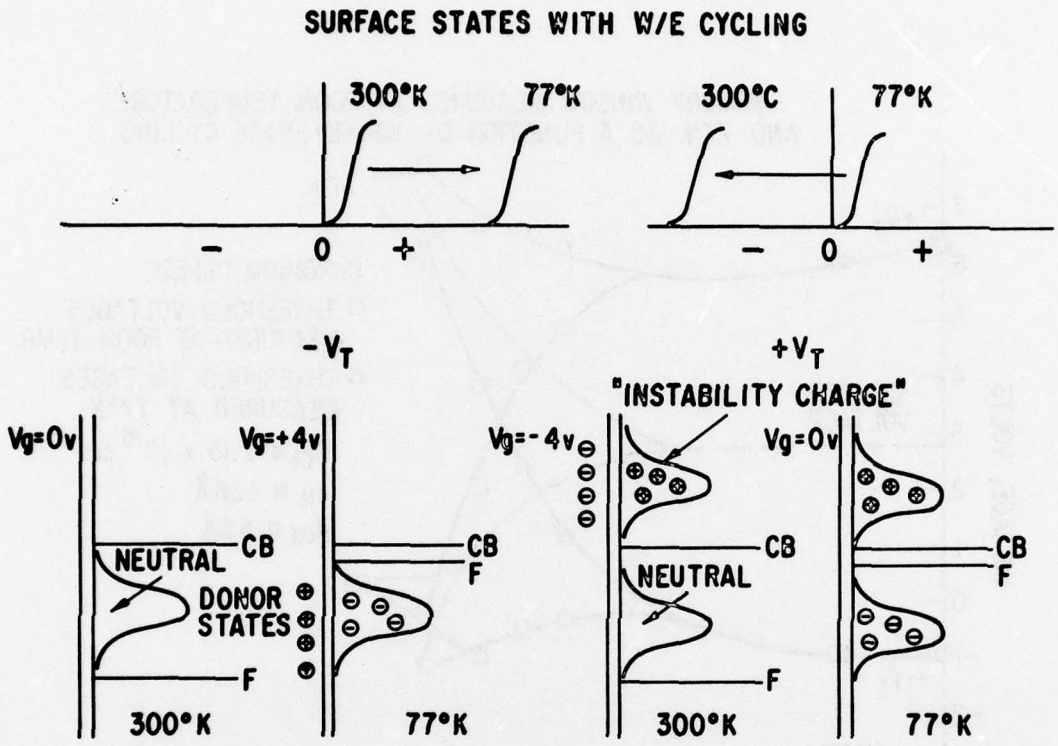

Figure 40. Surface States vs. Write/Erase Cycling

the right half of Fig. 40. Here the surface states introduced in the band gap are accompanied by another set of positively charge states, which is perhaps similar in nature to "instability charge" postulated by others[4].

[4] See for instance, S.M. Sze, Physics of Semiconductor Devices, Wiley-Interscience, NY, 1969, p. 444.

SECTION IX

ENDURANCE

Excessive write/erase cycling can cause window closure, changes in the center voltage, and an increase in the surface state density. Either of these alone, or together, can cause the device to fail. Endurance is the number of write/erase cycles which a device can withstand before it fails. We define endurance here as either the number of cycles needed to make one of the threshold voltages associated with the two memory states equal to the center voltage of the original device before extensive cycling, or the number of cycles at which the threshold window has narrowed to 1V, whichever occurs first. This is illustrated in Fig. 41, which shows the two threshold voltages with write/erase cycling for devices doped with Platinum for two oxide thicknesses. It can be seen that, although total window closure may not occur even at 10^6 cycles, the endurance is generally limited to values smaller than this by the excursions of the center voltage.

DEPENDENCE OF ENDURANCE ON WINDOW BEING CYCLED

The endurance of a device which was cycled at relatively low write voltages or short write times, thus giving small windows, was generally not much greater than the endurance for a similar device cycled at high write voltages and times to give large windows. This is illustrated in Fig. 42, in which the window decay of two similar devices is shown for two different original windows. The smaller window was cycled at $\pm$ 30.5V, 1 ms, and the larger one at $\pm$ 35V, 1 ms. The endurance in both cases is seen to be of the order of 1000 cycles, although complete window closure occurs well beyond that.

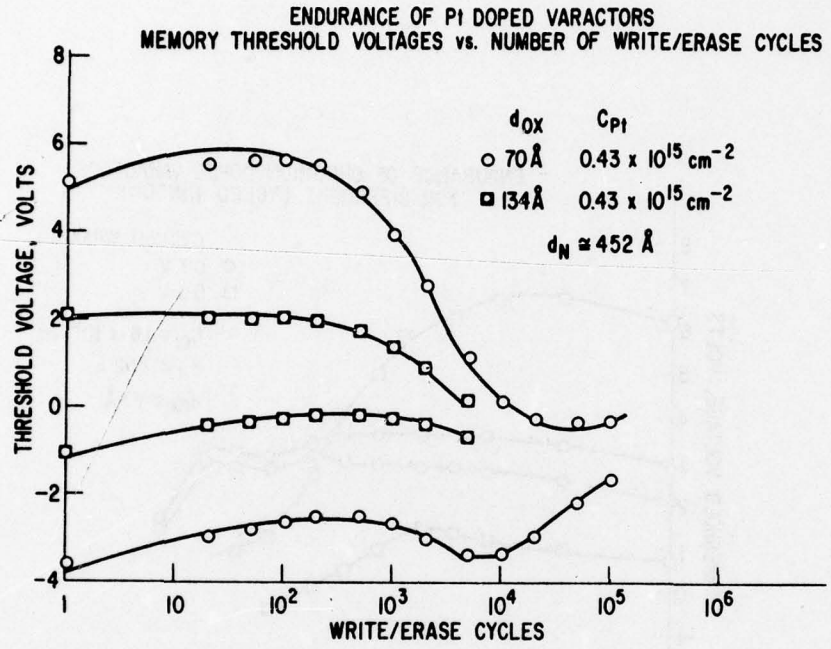

Figure 41. Endurance of Platinum Doped Varactors

AD-A067 857 GENERAL ELECTRIC CORPORATE RESEARCH AND DEVELOPMENT --ETC F/G 20/12
INTERFACE DOPING OF MNOS TRANSISTORS.(U)
JUN 77 C A NEUGEBAUER, M M BARNICLE F33615-76-C-1035
UNCLASSIFIED SRD-77-108 AFAL-TR-77-111 NL

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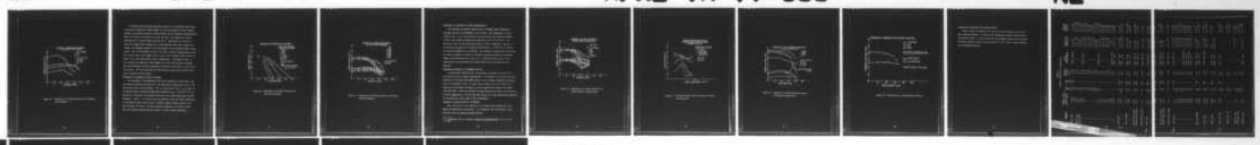

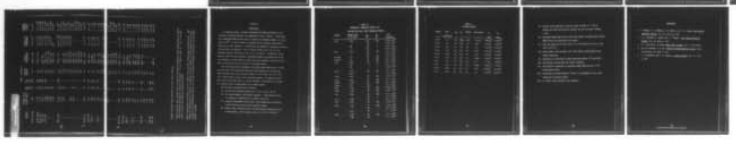

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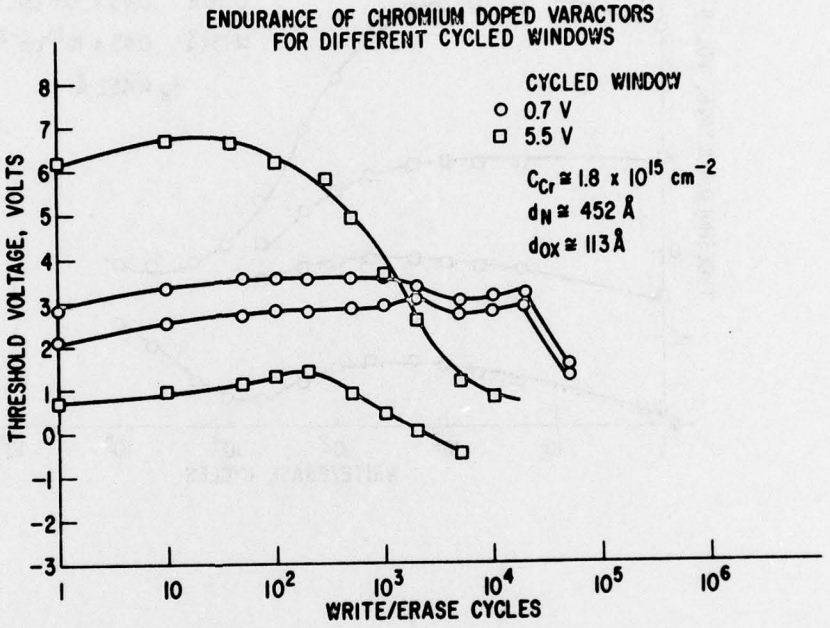

Figure 42. Endurance of Cr Doped Varactors for Different Cycled Windows

If a device which has been previously cycled to its endurance limit using a low write voltage and a small window, is now cycled again but with a higher voltage, the previous endurance cycling affects the new endurance proportionally. Thus, if at first a 1V window is cycled, and then a 10V window, the second endurance test is hardly affected by the first. Conversely, if a device is cycled with small write voltage, but is then rewritten once with a high write voltage, the endurance appears to be much greater for the smaller windows being cycled. This is illustrated in Fig. 43 in which 4 similar (neighboring) devices were cycled using a 3.5V window ($\pm$ 30V, 1 ms), 5.75 V window ($\pm$ 30V, 10 ms), 8V ($\pm$35V, 1 ms), and 8.25V ($\pm$35V, 10 ms), respectively. The points in Fig. 43 were obtained by cycling to a given number of cycles using the write voltages and times indicated, but then rewriting at the end of this with a $\pm$ 35V, 10 ms write pulse. The less rapid decay of the window at lower write voltages indicates a smaller wear-out effect.

DEPENDENCE OF ENDURANCE ON OXIDE THICKNESS

The dependence of the endurance on the oxide thickness is quite small, and the measured endurances of devices at the same dopant concentration are all the same within about one half decade. This is illustrated in Fig. 44, in which the two memory states of varactors doped with chromium at $C_{Cr} = 1.83 \cdot 10^{15}$ cm^{-2} are plotted as a function of write/erase cycling for six oxide thicknesses (nitride thickness = 452 A). It is seen that the endurance, using the above definition, is from 1000 to about 10,000 cycles, although complete window closure occurs only at about 10^5 cycles. No clear thickness dependence is evident, except that the thinnest oxides generally display a slightly higher endurance.

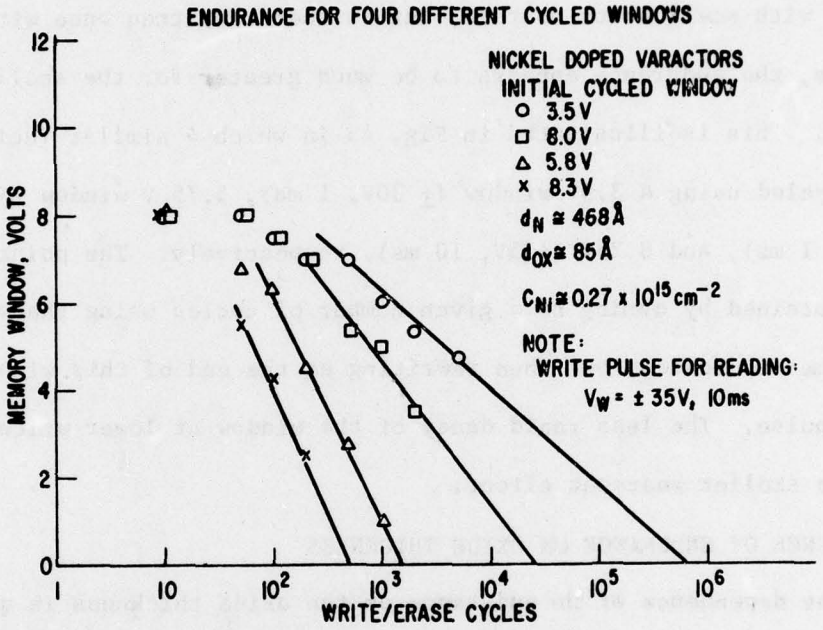

Figure 43. Endurance of Ni Doped Varactors for Four Cycled Windows

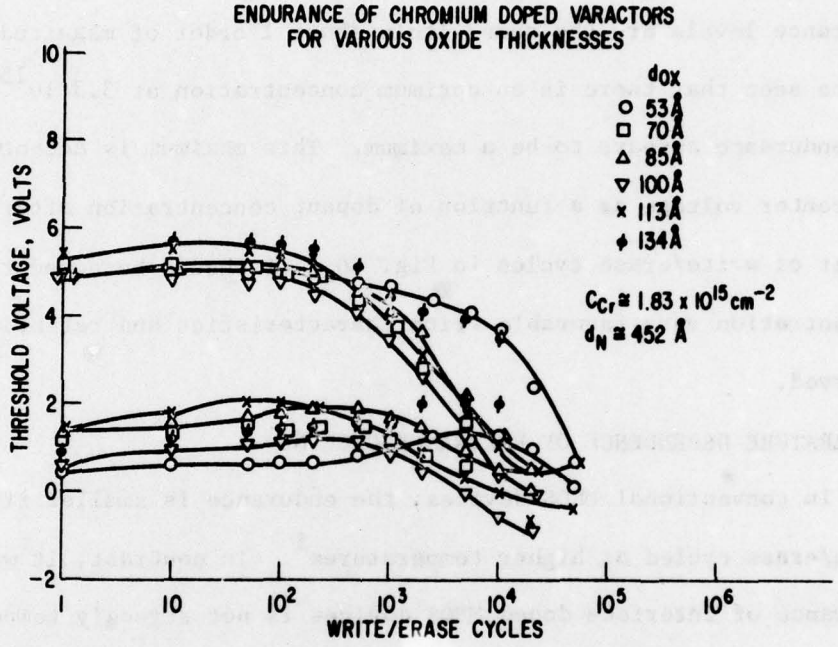

Figure 44. Endurance of Cr Doped Varactors for Various Oxide Thicknesses

DEPENDENCE OF ENDURANCE ON DOPANT CONCENTRATION

The dependence on dopant concentration is somewhat more complicated, although even here the dependence is not strong. This dependency is illustrated in Fig. 45 for chromium doped varactors which have an oxide thickness of 113A, and a dopant concentration range from 1.8 to $7.7 \cdot 10^{15}$ cm^{-2}. The endurance levels are the same within about 1 order of magnitude. However, it can be seen that there is an optimum concentration at $3.3 \cdot 10^{15}$ cm^{-2} at which the endurance appears to be a maximum. This maximum is accentuated by plotting the center voltage as a function of dopant concentration after an increasing number of write/erase cycles in Fig. 46. It should be noted that at this concentration very favorable write characteristics and retention are also observed.

TEMPERATURE DEPENDENCE OF ENDURANCE CYCLING

In conventional MNOS devices, the endurance is smaller if the device is write/erase cycled at higher temperatures[5]. In contrast, it was found that the endurance of interface doped MNOS devices is not strongly temperature dependent. This is illustrated in Fig. 47, where the two memory states are plotted as a function of write/erase cycling for various temperatures between room temperature and 200°C. While the threshold voltage decay with cycling is not identical for each temperature, it can be seen that there is no clear temperature dependence of the endurance in the range of these experiments.

ENDURANCE OF DEVICES DOPED BY SPUTTERING

Fig. 48 illustrates the endurance of a chromium doped device where the dopant was deposited by sputtering. It is apparent that the behavior closely parallels that of evaporation-doped devices.

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[5] C.A. Neugebauer and J.F. Burgess, Journal of Applied Physics, Vol. 47, 1976, p. 3182.

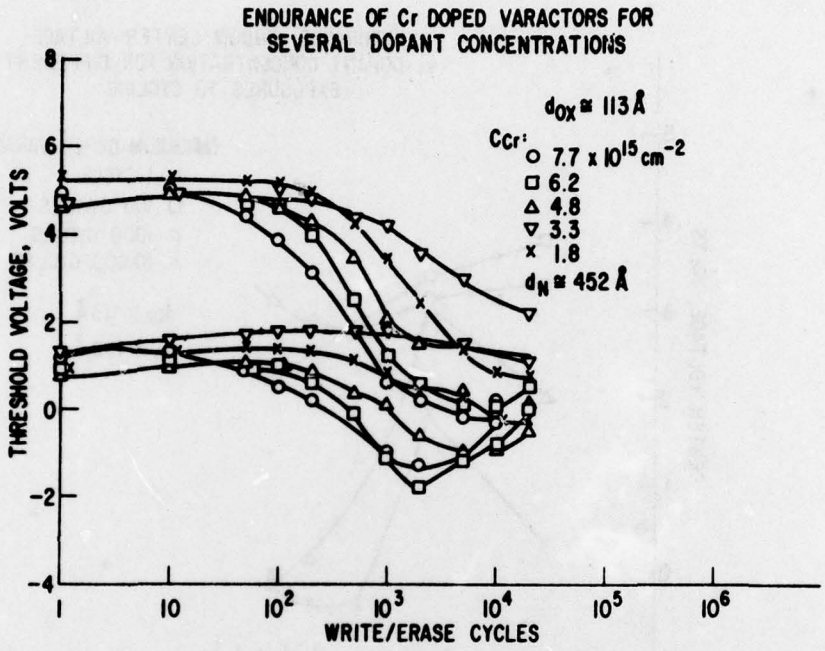

Figure 45. Endurance of Cr Doped Varactors for Several Dopant Concentrations

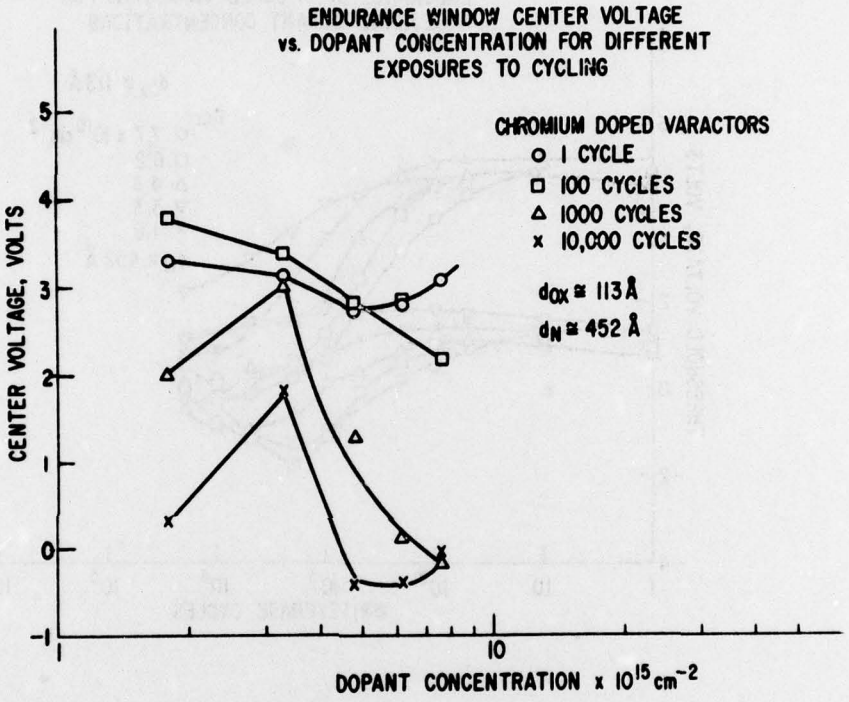

Figure 46. Endurance Window Center Voltage vs. Dopant Concentration

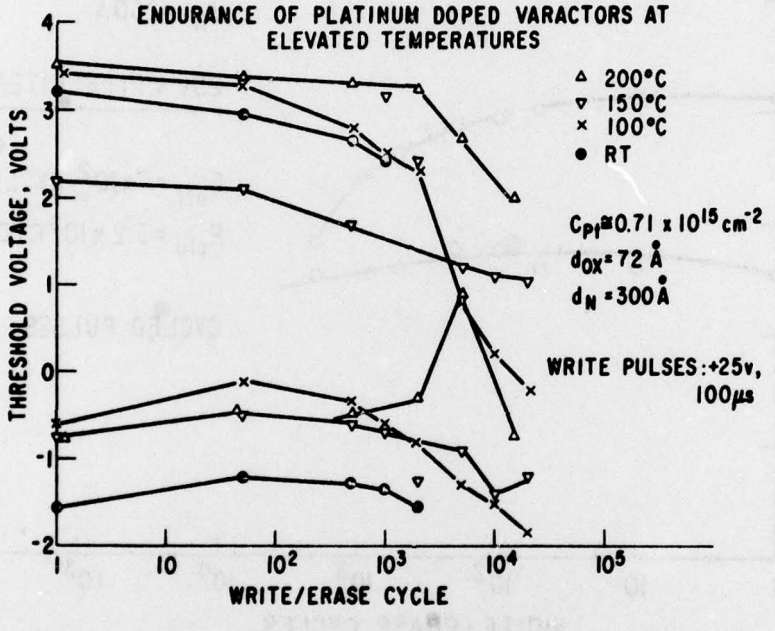

Figure 47. Endurance of Platinum Doped Varactors at Elevated Temperatures

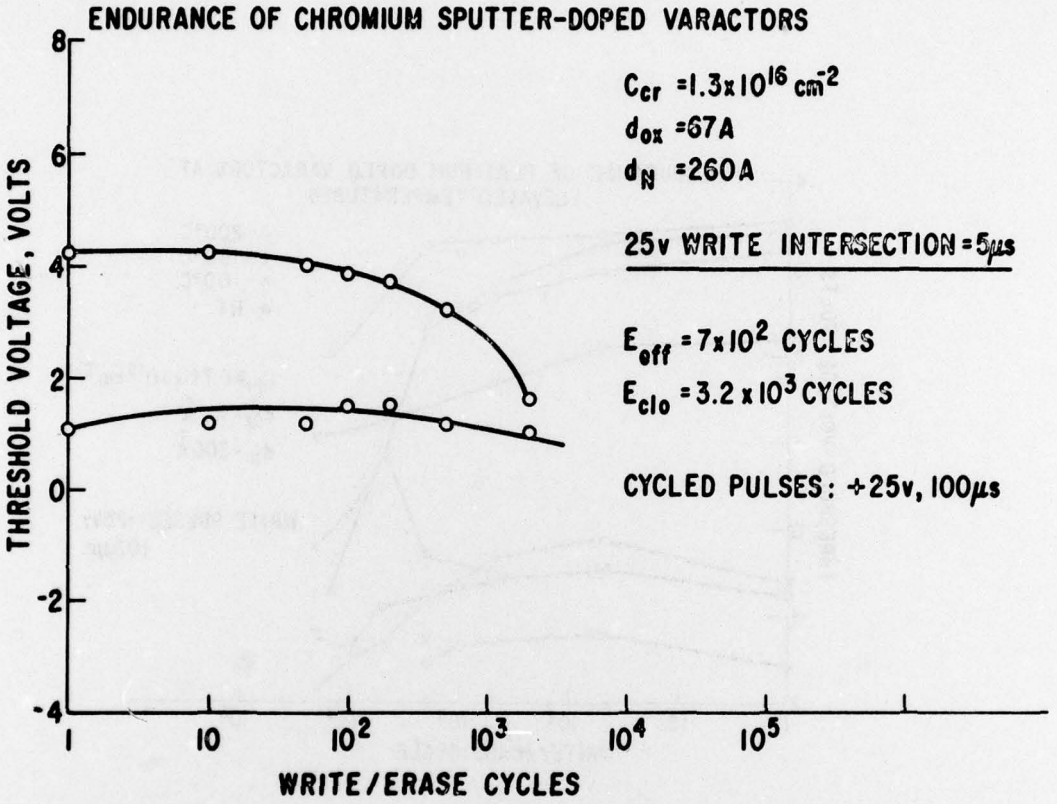

Figure 48. Endurance of Cr Sputter-Doped Varactors

COMPARISON OF ENDURANCE FOR VARIOUS DOPANTS

Table 9 shows the endurance for varactors and transistors for the six most promising dopants, at various oxide thicknesses, dopant concentrations, and windows cycled. It can be seen that the endurance values are not greatly different from each other, and vary from 10^3 to 10^5. This is quite adequate for an EAROM application.

TABLE 9

Typical Endurance Parameters

Device	Dopant conc. x 10^{15} cm^{-2}	d_{ox} Å	d_N Å	Window cycled V	Pulse dimensions	Effective endurance	Window closure (est.)
Cr-1 var	2.95	134	452	3.05	±35V, 100 µs	6×10^2	7×10^4
"	2.95	53	"	3.17	"	7.5×10^4	2.5×10^5
†Cr-1 var	8.6	53	"	5.7	"	2.5×10^3	1.5×10^4
Cr-1 var	8.6	134	"	3.0	"	8×10^2	1.5×10^4
"	1.83	53	"	4.55	±33V, 1 ms	1.7×10^4	9×10^4
"	"	70	"	3.75	"	1.7×10^3	1.5×10^4
"	"	85	"	3.65	"	3.1×10^3	5×10^4
"	"	100	"	4.35	"	1.8×10^3	2×10^5
"	"	113	"	4.0	"	1.6×10^3	8×10^4
"	"	134	"	4.15	"	$\sim 5 \times 10^4$	1.5×10^5
"	7.7	113	"	3.7	±32V, 1 ms	2×10^2	2.5×10^4
"	6.2	"	"	3.8	"	5.0×10^2	6×10^4
"	4.8	"	"	3.8	"	8.0×10^2	7×10^4
"	3.3	"	"	3.4	"	4.3×10^3	6×10^5
"	1.8	"	"	4.35	"	1.4×10^3	2×10^6
"	1.85	"	"	0.7	±30.5V, 1 ms	10^1	1×10^5
"	1.85	"	"	5.5	±35V, 1 ms	1.4×10^3	3×10^5
Cr-2 var	0.77	61	372	5.5	±30V, 1 ms	$3.0 \times 10^{3*}$	2×10^4
"	0.77	134	372	4.9	±30V, 1 ms	$6.6 \times 10^{2*}$	1.6×10^3
Cr-7 trans	1.95	53	468	9.2	±30V, 1 ms	6.4×10^2	1.5×10^4
"	1.95	53	468	10.8	±35V, 1 ms	2×10^1	3×10^2
†Cr-14 in trans	2.47	35	263	3.85	±25V, 400 ns	4×10^3	1.6×10^5
†Cr-14 out trans	5.2	43	263	3.6	±20V, 10 µs	2×10^4	7×10^6
†Cr-15 out trans	1.1	57	263	1.34	±25V, 500 ns	1.6×10^2	2×10^5
Pt-7 var	2.3	70	452	8.5	±35V, 100 µs	1.3×10^4	9×10^4
"	2.3	134	"	3.4	"	3.0×10^3	1×10^4

"	1.95	53	468	10.8	±35V, 1 ms	2 x 10^{-}	3 x $10^{}$
†Cr-14 in trans	2.47	35	263	3.85	±25V, 400 ns	4 x 10^{3}	1.6 x 10^{5}
†Cr-14 out trans	5.2	43	263	3.6	±20V, 10 µs	2 x 10^{4}	7 x 10^{6}
†Cr-15 out trans	1.1	57	263	1.34	±25V, 500 ns	1.6 x 10^{2}	2 x 10^{5}
Pt-7 var	2.3	70	452	8.5	±35V, 100 µs	1.3 x 10^{4}	9 x 10^{4}
"	2.3	134	"	3.4	"	3.0 x 10^{3}	1 x 10^{4}
"	0.51	70	"	8.7	"	6.0 x 10^{3}	6 x 10^{5}
"	0.51	134	"	3.2	"	3.6 x 10^{3}	2.5 x 10^{4}
"	0.51	70	"	3.1	±28V, 100 µsec	1.0 x 10^{4}	4 x 10^{4}
"	0.51	70	"	5.3	±25V, 10 ms	1.1 x 10^{4}	8 x 10^{5}
"	0.51	70	"	2.8	±35V, 1.75 µs	1.6 x 10^{2}	4 x 10^{4}
"	0.51	70	"	6.8	±35V, 10 µs	5.2 x 10^{4}*	6 x 10^{7}
†Pt-11 trans	1.12	85	372	2.3	±25V, 100 µs	1.5 x 10^{3}	6 x 10^{4}
† "	0.27	85	"	4.6	±25V, 1 ms	4 x 10^{1}	2.0 x 10^{4}
W-17 var	1.65	59	468	5.45	±35V, 100 µsec	2.1 x 10^{2}	8 x 10^{2}
"	0.06	59	"	4.5	"	8.0 x 10^{3}	2.3 x 10^{4}
W-39 var	0.55	63	450	1.2	±35V, 1 ms	∿10^{1}	8 x 10^{4}
"	2.5	63	"	2.0	±35V, 1 ms	>1.4 x 10^{4}	-
W-44 in var	1.08	68	439	10.2	±35V, 1 ms	-	1.1 x 10^{3}
"	"	100	"	7.6	"	-	5 x 10^{3}
W-44 out var	"	68	"	8.1	"	-	2 x 10^{4}
"	"	100	"	5.0	"	-	3.2 x 10^{7}
W-45 in var	2.8	68	"	8.2	"	4.0 x 10^{3}	4 x 10^{4}
W-45 out var	"	68	"	7.1	"	-	7 x 10^{4}
"	"	100	"	4.2	"	-	3.5 x 10^{5}
W-45 in var	2.8	68	"	6.35	±35V, 1 ms	6.0 x 10^{3}	1.4 x 10^{6}

TABLE 9 (Cont'd.)

Device	Dopant conc. x 10^{15} cm^{-2}	d_{ox} Å	D_N Å	Window cycled	Pulse dimensions	Effective endurance	Window closure (est.)
W-44 in var	1.08	68	439	8.4	±35V, 1 ms	4.0×10^2	2×10^3
W-47 trans	1.79	84	280	5.6	±25V, 1 ms	1.0×10^3	2.3×10^4
†W-47 var	1.79	84	280	4.3	"	2.0×10^3	1.6×10^4
W-48 var	1.94	58	320	5.5	±30V, 10µs	1.1×10^4	8.4×10^4
Ir-2 var	0.081	53	468	6.5	±35V, 1 ms	3.2×10^3	5.5×10^3
"	0.081	80	"	5.8	±32.5V, 1 ms	$1.3 \times 10^{3*}$	2×10^4
"	0.081	85	"	6.6	±35V, 1 ms	1.1×10^3	3.6×10^3
"	1.09	80	"	6.6	±30V, 1 ms	$>10^5$	7×10^5
Ni-4 var	1.22	53	468	4.9	±30V, 1 ms	$>2.0 \times 10^{4*}$	6×10^6
"	0.27	85	"	6.9	"	$>1.0 \times 10^{4*}$	1×10^5
"	1.22	53	"	7.75	±35V, 1 ms	3.5×10^4	1.6×10^4
"	"	"	"	4.0	±30V, 1 ms	$6.0 \times 10^{6*}$	5×10^6
"	"	"	"	7.0	±30V, 10 ms	$1.0 \times 10^{5*}$	1.1×10^5
"	1.22	"	"	9.2	±35V, 10 ms	$1.5 \times 10^{3*}$	1×10^4
"	0.27	85	"	3.5	±30V, 1 ms	-	7×10^5
"	"	"	"	8.0	±35V, 1 ms	-	1.6×10^3
"	"	"	"	5.8	±30V, 10 ms	-	2.5×10^4
"	"	"	"	8.3	±35V, 10 ms	-	5×10^2
Ni-10 var	0.39	58	320	6.2	±30V, 10 µs	3.1×10^2	2.3×10^3
Pt-16 var	0.12	58	320	5.2	±30V, 10 µs	2.1×10^2	4.8×10^2
Pd-3 tr	0.86	85	372	4.7	±25V, 100µs	3.6×10^2	2×10^4
"	1.58	85	372	5.2	±25V, 1 ms	2.2×10^1	7×10^3
Cr-4 tr	0.81	85	372	3.0	±25V, 1 ms	1.6×10^2	4×10^2
"	3.9	"	"	5.2	±25V, 1 ms	-	6×10^1
"	3.9	"	"	3.95	±25V, 100 µs	5.7×10^2	1.7×10^3

	"	0.27	85	"	3.5	±30V, 1 ms	-	7×10^5
	"	"	"	"	8.0	±35V, 1 ms	-	1.6×10^3
	"	"	"	"	5.8	±30V, 10 ms	-	2.5×10^4
	"	"	"	"	8.3	±35V, 10 ms	-	5×10^2
	Ni-10 var	0.39	58	320	6.2	±30V, 10 μs	3.1×10^2	2.3×10^3
	Pt-16 var	0.12	58	320	5.2	±30V, 10 μs	2.1×10^2	4.8×10^2
	Pd-3 tr	0.86	85	372	4.7	±25V, 100μs	3.6×10^2	2×10^4
	"	1.58	85	372	5.2	±25V, 1 ms	2.2×10^1	7×10^3
	Cr-4 tr	0.81	85	372	3.0	±25V, 1 ms	1.6×10^2	4×10^2
	"	3.9	"	"	5.2	±25V, 1 ms	-	6×10^1
	"	3.9	"	"	3.95	±25V, 100 μs	5.7×10^2	1.7×10^3
	Pt-4 var	0.17	65	564	4.9	±35V, 1 ms	4.5×10^3	4.5×10^3
	"	1.55	"	"	4.5	" "	6.6×10^3	1.0×10^4
	"	2.76	"	"	4.3	" "	3.8×10^3	6.0×10^3
	W-38 var	1.01	65*	~590	5.7	" "	7.6×10^2	2.5×10^3
	Ir-7 var	0.15	58	320	5.5	±30V, μs	5.6×10^2	1.8×10^3

2

†These devices could qualify as fast write devices.

*These devices were cycled with pulses of different dimension from those used to write the threshold voltages we actually measured. In all cases, pulse of 35V, 1 ms was used to write the actually observed window.

NOTE: Comparison of figures in this table with earlier version may be deceiving. The effective endurance of a device is defined as that number of write-erase cycles that a device can accommodate before one of the threshold voltages intersects the original center voltage.

SECTION X

CONCLUSIONS

An important figure of merit established for MNOS performance is the retention x endurance product, with dimensions of sec x cycles. It was found for conventional MNOS devices that the retention x endurance product is of the order of 10^{16}. If this criterion is applied to the interface doped devices fabricated in this program, it is found that this product is frequently exceeded by many orders of magnitude. This is shown in Table 10 for the six most promising dopants, which are Cr, Pt, W, Ir, Ni, and Pd. It should be noted, however, that this high retention x endurance product is entirely due to the long retention of these devices, rather than their endurance, which was of the order of 1000 cycles for all devices, as discussed above.

The surprising feature displayed by interface doped MNOS devices is that they can show a very high write speed and long retention at the same time. These "optimum" devices are listed in Table 11, which gives the write speed (30 V intersection) as well as the retention obtained. It should be noted that write speeds well below 1 μs can be obtained. This speed can be traded for a smaller write voltage applied for a longer period.

The principal conclusions are as follows:

(1) The six most promising dopants are: Pt, W, Cr, Ni, Pd, Ir.

(2) The stored charge is principally negative. A one-transistor cell is, therefore, compatible with n-channel circuitry.

(3) Interface doped MNOS devices differ from undoped ones principally in their ability to eject stored negative charge.

(4) Thinner oxide, thinner nitride, and high dopant concentration give a faster device. Write times as short as 2 nsec are possible.

TABLE 10

ENDURANCE X RETENTION PRODUCT FOR

DEVICES WITH THE 6 MOST PROMISING DOPANTS

DEVICE	DOPANT CONC. $\times 10^{15}$ CM^{-2}	d_{ox} Å	d_N Å	ExR CYCLE-SEC
Cr-1	2.95	134	452	3.29×10^{22}
	"	53	"	1.05×10^{12}
	8.6	53	"	4.8×10^{9}
	"	134	"	8.55×10^{18}
Cr-2	0.77	61	372	2.4×10^{19}
	"	134	"	5.12×10^{17}
Cr-14-o	5.2	43	263	7.7×10^{14}
Cr-15-o	1.1	57	263	8.0×10^{23}
Cr-4	0.81	85	372	8.0×10^{20}
	3.9	"	"	5.4×10^{17}
	3.9	"	"	1.53×10^{19}
Pt-11	1.12	85	372	7.8×10^{25}
	0.27	"	"	1.2×10^{24}
Pt-16	0.12	58	320	1.15×10^{15}
W-39	0.55	63	450	8.0×10^{22}
W-44-i	1.08	68	439	3.3×10^{16}
W-45-i	2.8	68	"	4.4×10^{24}
W-47	1.79	84	280	5.06×10^{16}
W-48	1.94	58	320	6.55×10^{18}
Ir-2	0.08	53	468	2.2×10^{12}
	"	80	"	2.0×10^{23}
Ir-1	1.09	80	"	4.2×10^{12}
Ir-7	0.15	58	320	2.16×10^{17}
Ni-4	1.22	53	468	1.26×10^{16}
	"	85	"	3.4×10^{13}
	0.27	85	"	1×10^{24}
Pd-3	0.86	85	372	1.6×10^{25}
	1.58	85	"	7.7×10^{25}

TABLE 11

OPTIMUM DEVICES

Dopant	Conc.	d_{ox}	d_N	Window	Write Speed	τ_r	t_R
	$\times 10^{15}$ cm^{-2}					sec	sec
Cr-15	1.1	57A	263A	6.4V	0.4 μs	8.0×10^{10}	4.0×10^{18}
Cr-15	5.4	50	263	5.4	0.35	1.0×10^{7}	4.6×10^{10}
Pt-11	0.27	85	372	5.4	2.5	1.7×10^{13}	6.0×10^{19}
Pt-11	0.27	85	372	9.2	0.25	2.2×10^{14}	1.3×10^{21}
Pt-16	0.12	58	320	4.4	0.15	3.0×10^{6}	2.4×10^{12}
W-48	1.94	58	320	7.7	0.002	4.8×10^{8}	7.8×10^{13}
W-47	1.8	84	280	9.5	0.6	1.7×10^{7}	2.2×10^{12}
Pd-3	1.58	85	372	4.3	0.065	4.0×10^{13}	1.1×10^{22}
Ni-10	0.66	58	320	6.1	0.02	5.8×10^{8}	1.2×10^{15}
Cr-4	1.59	85	372	6.4	3.2	3.5×10^{10}	9.0×10^{15}

(5) Surface state generation occurs at gate voltages of $> +20V$ if applied for more than several seconds, but not for gate voltages $< -20V$.

(6) Interface doped MNOS devices have much higher retention than undoped MNOS devices of equivalent write speed.

(7) Even the retention of fast write ($< 1\ \mu s$) devices can be very long (10^5 to 10^{17} s).

(8) Thick oxide, thick nitride, and a low dopant concentration favor higher retention.

(9) Retention is controlled by back-tunneling between $77^{\circ}K$ and $300^{\circ}C$.

(10) Write/erase cycling does not affect retention.

(11) The effective endurance of interface doped MNOS devices is 10^3 write/erase cycles.

(12) Write/erase cycling beyond 10^3 cycles is accompanied by the rapid formation of surface states.

(13) We cannot trade retention for endurance.

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