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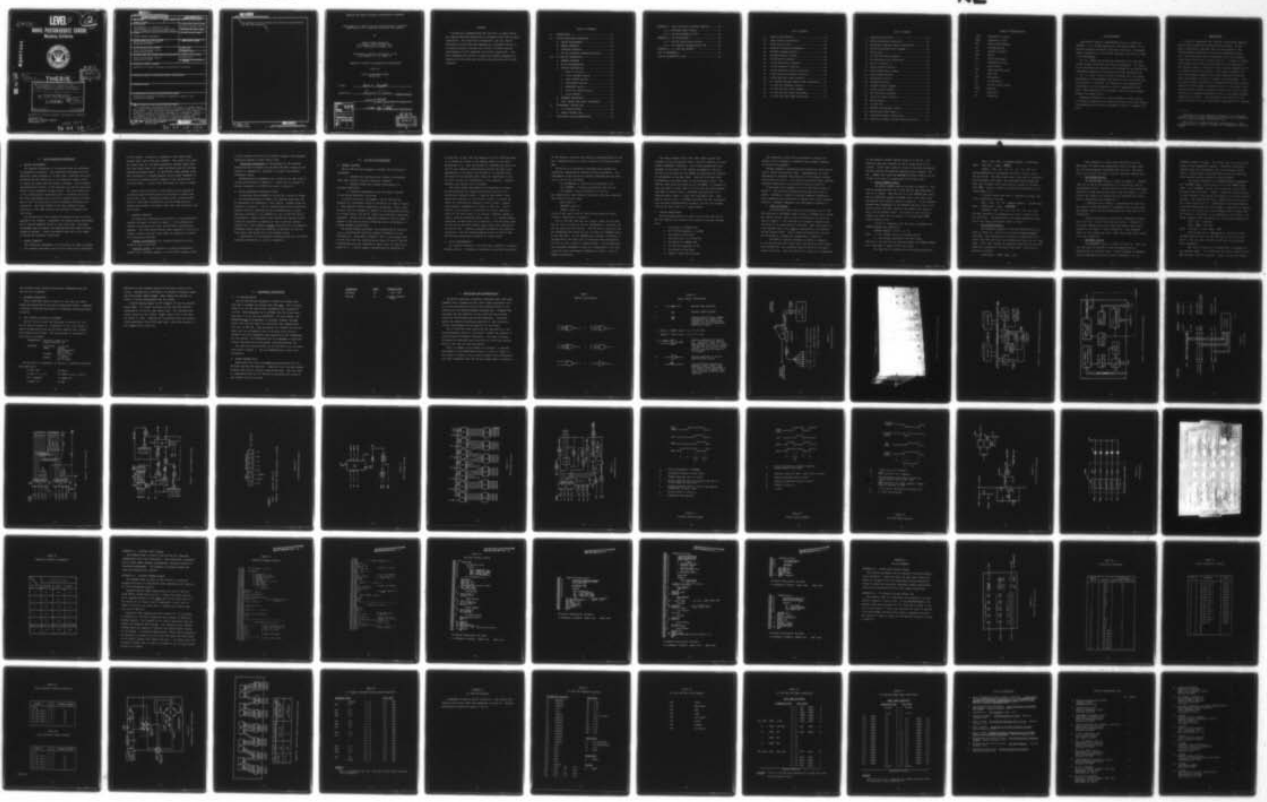

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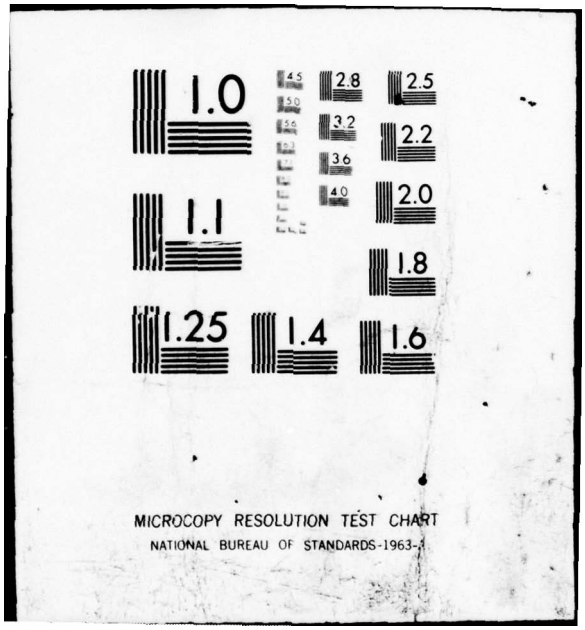
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NAVAL POSTGRADUATE SCHOOL

Monterey, California

(9) Master's THESIS

(6) Development of a Device for the Incorporation of Multiple Scanivalves into a Computer-Controlled Data System

by

(10) Robert Neldon Geopfarth

(11) March 1979

(12) 83 p.

Thesis Advisor: R.P. Shreeve

Prepared for:
Naval Air Systems Command
Washington, DC

251 450

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SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER NPS67-79-002	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) Development of a Device for the Incorporation of Multiple Scanivalves into a Computer-Controlled Data System		5. TYPE OF REPORT & PERIOD COVERED Master's Thesis: Mar 79 6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) Robert Neldon Geopfarth		8. CONTRACT OR GRANT NUMBER(s)
9. PERFORMING ORGANIZATION NAME AND ADDRESS Naval Postgraduate School Monterey CA 93940		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS Naval Postgraduate School Monterey CA 93940		12. REPORT DATE March 1979 13. NUMBER OF PAGES
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office) Naval Postgraduate School Monterey CA 93940		15. SECURITY CLASS. (of this report) Unclassified 15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Scanivalve-computer interface; pneumatic scanner; data acquisition system.

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

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Development of a Device for the Incorporation of Multiple Scanivalves into a Computer-Controlled Data System

by

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Lieutenant, United States Navy
B.S., University of Kansas, 1972

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN AERONAUTICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
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ABSTRACT

A controller (designated HG-78K) was built to permit manual and computer-directed acquisition of pneumatic data from multiple Scanivalves. The controller incorporated a low cost digital electronic circuit which was designed as a peripheral device on the Hewlett-Packard Interface Bus (HP-IB) to enable computer interrogation of port addresses of multiple Scanivalves. Computer programs were written in BASIC and FORTRAN languages and operation of the system was verified using HP-9830A and HP-21MX computers.

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TABLE OF ABBREVIATIONS

ADR_L	Addressed to Listen
ADR_T	Addressed to Talk
BCD	Binary Coded Decimal
CR	Carriage Return
DVM	Digital Voltmeter
DVR	Driver
EOI	End-of-Information
IC	Integrated Circuit
I/O	Input/Output
LED	Light Emitting Diode
LF	Line Feed
MUX	Multiplexer
NC	No Connection
PCB	Printed Circuit Board
RCVR	Receiver
S/V	Scanivalve
TX	Transducer

ACKNOWLEDGEMENT

Significant technical achievements occur as a result of teamwork. It is richly rewarding to have been a member of the team who produced the HG-78K Scanivalve Controller. The alpha-numeric designation of this device represents the pride we share in its development.

Mr. J.E. Hammer was principally responsible for the major design concept formulation and device requirements. His extensive instrumentation experience and knowledge of data acquisition requirements produced concise physical design specifications.

Mr. J.C. King, a man of infinite resource, was principally responsible for the hardware fabrication of both the HG-78K and the intricate S/V MUX PCB. His experience and competence in electronics, plus his ability to acquire impossible-to-find parts, were responsible for the rapid transition from schematic design to physical reality.

Associate Professor R.P. Shreeve guided the team's effort. His attentive support and his faith and trust in his team created a professional and fertile environment in which to complete this work.

I. INTRODUCTION

In tests of compressors and turbines, simultaneous measurements of many steady-state pressures are required. In past years, Scanivalves[1] have been used for this purpose at the Turbopropulsion Laboratory at the Naval Postgraduate School. Up to four Scanivalves were incorporated into a data logging system which output data on paper tape [1]. In order to replace this system with on-line data acquisition to the Laboratory's new computer system, a Scanivalve control device compatible with the computer system was required. This report documents the logic and hardware design of the HG-78K Scanivalve Controller which was designed and built to answer this requirement. The new device permits acquisition of steady-state data from multiple Scanivalves under manual or computer control. The design incorporates low-cost digital electronic circuits and the unit itself functions as a computer peripheral device on the Hewlett-Packard Interface Bus (HP-IB)[2]. The development was carried out primarily to satisfy the data acquisition requirements of a transonic

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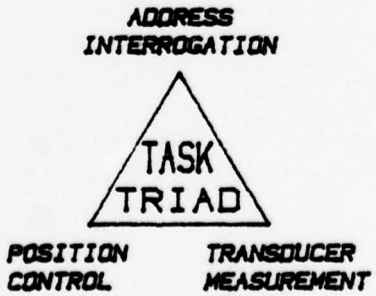
[1]"Scanivalve" is the registered trademark for a mechanical pneumatic selector switch manufactured by Scanivalve Corporation, P.O. Box 20005, San Diego, California 92120.

[2]The HP-IB is the Hewlett-Packard implementation of IEEE Standard 488-1975, "Digital Interface for Programmable Instrumentation".

compressor research program sponsored by Naval Air Systems Command, Code 310A.

The Scanivalve (S/V) is a device having multiple pneumatic input ports and a single pressure-measuring transducer. A mechanical rotor, driven by an electric motor, pneumatically connects one input port at a time to the transducer. Rotor position is controlled electronically. The transducer output is a voltage which, after proper conditioning, can be measured using a precision voltmeter and, through calibration, interpreted as pressure.

Operation of a Scanivalve involves three essential tasks: Address interrogation, position control and transducer measurement. Address interrogation is the process by which the Scanivalve port address is identified. Position control involves the process by which the Scanivalve is positioned to a specified input port. Transducer measurement involves the process by which the electrical output of the pressure transducer is transformed and sampled. These three tasks are completely independent, yet are involved each time Scanivalve data is taken. In this report the concept of these essential tasks is referred to as the "Task Triad":



In the following section the operation and description is given for the HG-78K Scanivalve Controller which was designed to perform the above tasks. The device is a single control station which features digital port address display, manual S/V control functions, signal conditioning, transducer outputs and computer address interrogation of each of the five laboratory Scanivalves. In Section III, a detailed description is given of the Scanivalve multiplexer printed circuit board (S/V MUX PCB). This digital electronic device was designed to perform the address interrogation task for multiple Scanivalves under computer control. Section IV contains programming instructions necessary to accomplish data transfer between the computer and the S/V MUX PCB. Conclusions and a recommended design improvement for the S/V MUX PCB are given in Section V. Sample computer programs which demonstrate the BASIC and FORTRAN code necessary to obtain steady-state data using the HP-21MX and the HP-9830A computers are given in Appendix A. Appendices B and C contain complete hardware documentation of the HG-78K Scanivalve Controller and the S/V MUX PCB, respectively.

II. HG-78K SCANIVALVE CONTROLLER

A. DESIGN REQUIREMENTS

The pressure transducer in a Scanivalve must be calibrated and checked at intervals. The calibration procedure involves applying a known pressure to an input port, selecting that port, and adjusting the resistance in the transducer bridge circuit to obtain the proper span and balance voltages. This procedure requires position control of the Scanivalve as well as electrical access to the transducer bridge circuit. The five Scanivalves in the Turbopropulsion Laboratory were at different locations. The first requirement was to provide a single location at which each of the five Scanivalves could be manually controlled and calibrated. Real-time display of the port address of each Scanivalve at the same location was required to complete the task triad.

The acquisition of data using the Scanivalves was to be programmed on the computer. Therefore, the second design requirement was to provide computer control of the task triad. The final requirement was that manual and computer-directed tasks be simultaneously operable. These requirements were met in the design of the HG-78K Scanivalve Controller.

B. MANUAL OPERATION

The electrical arrangement of a Scanivalve is shown in Figure 1. The elements associated with the task triad can be identified

in this figure. Attention is directed to the binary coded decimal (BCD) form of the port address. Four lines (0-3) carry the binary code for the least significant decimal digit while the other three lines (4-6) carry the binary code for the most significant decimal digit. In the HG-78K, these address lines were connected to a decoder/display circuit board (Appendix B) to provide continuous digital display of the selected port on the front panel. A view of the front panel is shown in Figure 2.

Manual position control of the Scanivalve was enabled by connecting panel-mounted push-button switches in series with the control lines. Transducer bridge circuit junctions were wired to front panel receptacles, and the bridge span and balance potentiometer adjustment knobs were also mounted on the front panel.

C. COMPUTER OPERATION

The Scanivalve installation in relation to the laboratory's computer equipment is shown in Figure 3. The interface bus (HP-IB) is controlled by either the HP-21MX or the HP-9830A computer. The other three devices shown connected to the bus in Figure 3 execute the task triad under the direction of either bus controller as follows:

·Address interrogation of a selected Scanivalve is performed by the S/V MUX PCB.

·Position control is obtained by closing predetermined relays (via a software command) in the HP-3495A Scanner, which

in turn connects the 24-Vdc S/V control voltage to the selected Scanivalve advance or home control line.

Transducer measurement of the pressure on the selected Scanivalve port is made by the HP-3455A DVM when a relay in the Scanner is commanded (in software) to connect the selected transducer output.

Representative programming code to execute the task triad is listed and described in Appendix A. Codes used to address the devices connected on the HP-IB are given in Table A1.

D. HG-78K SCANIVALVE CONTROLLER LAYOUT

A functional block diagram of the HG-78K is shown in Figure 4. The non-interference of manual and computer operations can be understood with reference to this figure. Address lines are connected in parallel. The S/V decoder/display PCB continuously displays the port addresses while the address data is simultaneously available to the computer by the S/V MUX PCB without interference. Manual control line switches and Scanner control relays are connected in parallel so that a position control function will occur whenever either electrical path is completed. Transducer output lines are connected in parallel to both the front panel test points and to the Scanner relays.

A description of the hardware and wiring plans for the HG-78K Scanivalve Controller is given in Appendix B.

III. S/V MUX PCB DESCRIPTION

A. GENERAL FEATURES

The S/V MUX PCB was designed to satisfy the following requirements:

1. Perform the Scanivalve port address interrogation task under control of either laboratory computer.

2. Perform random port address interrogation of multiple Scanivalves.

3. Function independently from the manual features of the HG-78K Scanivalve Controller.

To satisfy the first requirement, the S/V MUX PCB was designed as a peripheral device on the HP-IB, as shown in Figure 3. This approach offered significant advantages. First, logic circuits could be designed to respond to the established protocol of a single device, the HP-IB, rather than individual laboratory computers. Second, HP-IB compatible computers could be added or changed in the future without affecting circuit performance or causing hardware alterations.

The second design requirement was accomplished by electronically selecting the Scanivalve address information in the following way. Referring to Figures 1 and 3, port address data (7-bits) from the five Scanivalves are input to the S/V MUX PCB. Corresponding bits are connected to input ports of seven multiplexer IC's. A binary number, representing the Scanivalve to

be selected, is sent from the computer to the S/V MUX PCB where it is stored and routed to the address inputs of the seven multiplexer IC's. Each multiplexer IC, representing one bit of the S/V port address, electronically selects the input line represented by the binary code latched on its address input. The state of the selected input lines are transferred to the bus line drivers for transmission to the computer. Computer software then decodes the S/V address.

The third design requirement was accomplished by simply connecting manual and computer-controlled functions into electrically parallel paths. A special high-current relay module was installed in the HP-3495A Scanner to provide ten relays for handling the Scanivalve control lines. Scanner relay/channel assignments are listed in Table A2. Control current can be routed to a Scanivalve by either pressing a button on the front panel or by issuing a computer command to close a parallel-connected Scanner relay. In a similar manner, transducer voltage lines were connected to both the front panel outlets and to HP-3495A Scanner relays which were connected to the HP-3455 DVM. Scanivalve address information was parallel-connected to both the Decoder/Display PCB and to the S/V MUX PCB and was continuously available to either device.

B. HP-IB CONSIDERATIONS

All devices connected to the HP-IB must conform to a rigidly-defined protocol. Reference 2 presents an excellent description

of the features, protocol and electrical characteristics of the bus. Presented here is a brief overview of the HP-IB environment.

The HP-IB is a serial-byte interface which permits bi-directional communication between multiple instruments. All instruments on the bus can be uniquely addressed and can function as one of the following:

bus CONTROLLER -- controls bus information flow

bus LISTENER -- receives information from the bus

bus TALKER -- sends information to the bus

Bus communication uses sixteen lines which have been organized into three functional types:

DATA lines (8)

TRANSFER lines (3)

CONTROL lines (5)

The bus lines used by the S/V MUX PCB are shown with their mnemonic definitions in Figure 5.

The S/V MUX PCB uses only two control lines; IFC and ATN. The IFC line is driven by the bus CONTROLLER to initialize the bus and clear any bus activity. The ATN line is driven by the bus CONTROLLER and places the bus in either the COMMAND mode or in the DATA mode. In the COMMAND mode, address information is transmitted on the data lines to establish those instruments that are to talk, listen or remain dormant. In the DATA mode, the instrument addressed to talk will communicate on the data lines with those instruments addressed to listen. Only one TALKER is permitted.

The three transfer lines (DAV, NRFD, NDAC) execute the transfer of each information byte on the data lines by an interlocked "handshake" technique. This allows asynchronous data transfer at the speed of the slowest instrument on the bus. The DAV line is driven by the TALKER and indicates the validity of information on the data lines. When DAV is driven true, information on the DATA lines is unconditionally valid. The NRFD and NDAC lines are driven by all LISTENERs to indicate if they are ready to accept data or if the data has been accepted. When NRFD is driven false, a LISTENER indicates that it is unconditionally ready to accept one information byte. When NDAC is driven false, a LISTENER indicates that the information byte has been unconditionally accepted, and that the information on the data lines is no longer needed.

C. CIRCUIT DESCRIPTION

The following sequence of events occurs each time the S/V MUX PCB supplies the computer with Scanivalve address information:

1. Bus placed in COMMAND mode.
2. S/V MUX PCB addressed to LISTEN.
3. Bus placed in DATA mode.
4. Data byte sent to S/V MUX PCB.
5. Bus placed in COMMAND mode.
6. S/V MUX PCB addressed to TALK.
7. Bus placed in DATA mode.
8. Computer reads one data byte.

The remainder of this section describes in detail the digital circuit designed to implement this transfer sequence in the HP-IB environment.

Boolean algebraic expressions were written for each circuit line to define the required logic. Implementation of these expressions in hardware often made use of the logical equivalences shown in Table I. The circuit conventions which identify component labeling and line states are given in Table II.

A functional block diagram of the S/V MUX PCB is shown in Figure 6. The following discussion describes each block in detail. Reference is made to detailed schematic diagrams in which components are identified by numbers that follow standard practice. Hardware components are identified in Appendix C.

1. DATA I/O Section

Bi-directional data lines are used because the S/V MUX PCB functions at different times as both a LISTENER and a TALKER. The logical devices used to form bi-directional bus lines are shown in Figure 7. The receiver is a standard inverter while the driver is an open-collector NAND gate. Each individual bus line, whether used or not, must be terminated in the resistor divider network shown. Four of these bi-directional circuits are contained in a single bus transceiver IC (MC3441P).

The DATA I/O section schematic is shown in Figure 8. In this section the ATN control line and the seven data lines, DI01 through DI07, are connected from the HP-IB to bus transceivers U1 and U2. Data line DI08 is not used and is terminated

by the resistor divider network formed by R1 and R2. All received lines are inverted for use in other parts of the circuit. Driver input lines to U1 and U2 from the multiplexer section identify the selected Scanivalve port address. The DRIVE ENABLE line (from the HANDSHAKE section) enables the bus drivers in U1 and U2 to place data on the data lines.

2. DEVICE ADDRESS Section

The DEVICE ADDRESS section is shown in Figure 9. This section determines when the S/V MUX PCB has been addressed to talk or to listen. When the bus is in the COMMAND mode (ATN), the bus CONTROLLER places an address word on the data lines. The address word format is shown in Figure 10. If the received address word corresponds to the address physically set on the circuit board, the logic state of one address line (ADR_T or ADR_L) will be defined "true". The state of this line will remain valid after the bus returns to the DATA mode ($\overline{ATN}$), unless cleared by IFC.

A five bit comparator (U6) was used to implement the ADDRESS ENABLE line defined as:

ADDRESS ENABLE = (DAV) • (B = A)

where A = bit pattern set by the address switch

B = bit pattern received on the data lines.

When DAV is true and the bit patterns match, the ADDRESS ENABLE line goes high to enable U27(a) and U27(b).

The ADR_T line is defined by the following expression:

ADR_T = (ATN • $\overline{B6}$ • B7•ADDRESS ENABLE) + (TALK HOLD)

where TALK HOLD = (ADR_T • $\overline{UNTALK}$)

UNTALK = (ATN • B1 • B2 • B3 • B4 • B5 • $\overline{B6}$ • B7)

The ADR_T expression is implemented by U27(a), U30(c), U7(c), U26 and U30(d). The ADR_T output line is set when U7 receives a positive-edged clock pulse. The TALK HOLD logic allows the ADR_T line to remain valid after the bus returns to the DATA mode ($\overline{ATN}$). ADR_T is cleared by making TALK HOLD false or by a CLEAR signal to U7.

A similar circuit was used to implement the ADR_L line which is defined as follows:

ADR_L = (ATN • B6 • $\overline{B7}$ • ADDRESS ENABLE) + (LISTEN HOLD)

where LISTEN HOLD = (ADR_L • $\overline{UNLISTEN}$) ,

• UNLISTEN = (ATN • B1 • B2 • B3 • B4 • B5 • B6 • $\overline{B7}$)

The ADR_L expression is implemented by U27(b), U30(b), U7(b), U25 and U30(a). Implementation of the above expressions made use of the logical equivalence shown in Table I.

3. DATA STORAGE Section

The schematic diagram for the DATA STORAGE section is shown in Figure 11. Device U9 is a positive-edge-triggered flip-flop. Data appearing on its input is transferred to its output only when the clock line transitions from a low to a high state. Thus, data storage is completely controlled by the DATA STORE line connected to the clock input gate. This line is defined as follows:

(DATA STORE) = ($\overline{ATN}$ • ADR_L • DAV)

When addressed to listen while the HP-IB is in the DATA mode, the three least significant bits on the data lines will be stored whenever the TALKER sets DAV true. The three bits, A1, A2 and A3 are used to select Scanivalve address data.

4. MULTIPLEXER Section

The MULTIPLEXER circuit is shown in Figure 12. Address lines A1, A2 and A3 are connected to the data select pins of multiplexers U10-U16. The bit pattern on these lines determines which one of eight multiplexer input lines is selected. In this circuit only inputs one through five are connected and correspond to Scanivalves one through five.

A Scanivalve port address is represented by seven bits. The output of each multiplexer IC represents one of these bits. Multiplexer inputs are the corresponding bits from each of five Scanivalves.

Scanivalves physically define port addresses by grounding "true" bits; "false" bits are open circuit. Buffers U17-U22 invert address data bits to make multiplexer input logic conform to the "high" = "true" convention. Thus, grounded inputs to the buffers are output "high" while open inputs result in a "low" output [3].

5. HANDSHAKE Section

The HANDSHAKE circuit is shown in Figure 13. This section executes the transfer of each information byte by manipulating the transfer lines. Circuit response is dependent upon the designated function of the S/V MUX PCB; i.e., as

LISTENER, TALKER or dormant. The driver circuits in bus transceiver U3 were permanently enabled. Therefore, line driver - enabling logic was incorporated into the individual driver inputs. Unused control lines REN, SRQ and EOI are shown with their required terminal resistor divider networks.

The circuit responds as a LISTENER whenever designated as a LISTENER (ADR_L) or when the bus is in the COMMAND mode (ATN). As a LISTENER, the DAV line is received and the NRFD and NDAC lines are driven. Figure 14 shows the timing sequence of these transfer lines during the transfer of one byte from the computer. The received DAV line is sampled every 100-nsecs by the clocked flip-flop U7(a). Depending on the synchronization of the DAV signal with the clock signal, a time delay of approximately zero to 100-nsec will occur between time of receipt and the time DAV is available to the remainder of the circuit. The driven transfer lines are defined by the following expressions:

$$NRFD = DAV \cdot (LSN\ RDY)$$

$$NDAC = \overline{NRFD} \cdot (LSN\ RDY)$$

where $(LSN\ RDY) = (ATN + ADR_L) \cdot \overline{IFC}$

The LSN RDY line is implemented by U29(a) and U29(b), the NRFD line by U28(c) and the NDAC line by U5, U31(c) and U31(d). (U31 was used to create an AND gate from available logic components.)

The circuit responds as a TALKER when so designated by the computer (ADR_T). As a TALKER the DAV line is driven and the NRFD and NDAC lines are received. Figure 15 shows the timing

sequence of the transfer lines during the transfer of one data byte to the computer. Information is placed on the data lines whenever the DRIVE ENABLE line is true:

$$\text{DRIVE ENABLE} = (\overline{\text{ATN}} \overset{U28(d)}{\downarrow} \text{ADR}_T \overset{U32(a)}{\downarrow} \overline{\text{NRFD}})$$

Whenever this condition exists, Scanivalve address information is unconditionally present on the data lines. An end-of-record (EOR) signal is not provided by this circuit; therefore, the computer must be programmed not to expect or to require one. The driven DAV line is defined as:

$$\text{DAV} = (\text{DAV ENABLE}) \cdot \overset{U31(a)}{\overset{\downarrow}{\overline{\text{NRFD}}}}_{\text{DELAYED}} \cdot (\text{NDAC} \overset{U29(d)}{\overset{\downarrow}{\cdot}} \overline{\text{CLEAR}})$$

When using open-collector bus drivers, a 2 μsec delay is required to allow line ringing and signal transients to decay [2]. The delay was provided by U24, a retriggerable one-shot multivibrator, and U23, a positive-edge-triggered flip-flop. These components provide a pre-set delay between receipt of $\overline{\text{NRFD}}$ and driving the DAV line "true". Figure 16 describes the time delay sequence. Adjustment of the time delay circuit is described in Section III-E.

6. CLOCK and CLEAR Sections

The CLOCK and CLEAR circuit diagrams are shown in Figure 17. The CLOCK consists of multivibrator U8 and crystal Y1. The CLOCK output is a 10MHz sinusoidal signal and is available to the circuit sections shown in Figure 6.

The CLEAR section sets the initial operating state of the circuit when power is first applied and also monitors the IFC control line. Whenever the IFC or the PRE-CLEAR lines are "true", the following circuit state is set:

ADR_L set false

ADR_T set false

All HANDSHAKE driver lines disabled

DRIVE ENABLE set false

The pre-clear circuit provides an 8-msec "high" pulse to U29(c). When power is first applied, capacitor C2 charges through resistor R5. This develops a voltage which biases transistor Q1 into saturation and lowers the collector to nearly ground potential. The collector state is inverted by U5 to create the PRE-CLEAR pulse. When C2 is charged, no current flows through R5 and Q1 is cut-off. The collector potential then is at the supply voltage, and the inverted PRE-CLEAR signal is set "false". After the pre-clear sequence is complete, the CLEAR lines respond only to IFC.

7. HP-IB Display

It is useful to the programmer to monitor circuit response to computer-issued commands. The HP-IB display circuit was added to provide front panel display of the ADR_L, ADR_T and stored data lines A1, A2, A3. The circuit is shown in Figure 18. The selected lines were input to open-collector inverters. When input lines are "true", the inverters sink enough current to allow the LED's to illuminate. When input lines are "false",

the inverter output becomes electrically transparent and the LED's do not illuminate.

D. HARDWARE DESCRIPTION

The S/V MUX PCB, shown in Figure 19, was laid out, photo etched and fabricated at the Naval Postgraduate School. Appendix C contains a complete description of components and wiring specifications.

E. "DAV" DRIVER LINE DELAY ADJUSTMENT

The DAV driver circuit was discussed in Section III (C5) and is shown in Figure 13. Adjustment of the 2 μsec delay is easily accomplished using the HP-9830A computer and a single-trace memory oscilloscope. The oscilloscope is connected to the circuit as follows:

CONNECTIONS:	External Trigger to TP7	
	Signal Input to TP8	
SETTINGS:	Time Sweep:	1 μsec/div
	Sweep:	Single
		Max persistence
		Write mode
	Trigger:	Ext (-) slope
		DC input
	Signal:	1 volt/div
		DC (+) input

The HP-9830A is programmed, as follows, to perform successive read operations:

```
10 CMD "?G$"                    50 NEXT I
20 FOR I = 1 to 75              60 OUTPUT (13,70) 256,95;
30 A = RBYTE13                  70 FORMAT 2B
40 WAIT 750                     80 END
```

Execution of this program causes the DAV drive circuit to be active. Program line 40 provides 0.75 seconds to manually reset the oscilloscope sweep trigger. Many traces are required to "burn" a visible presentation onto the screen.

A negative-going signal on TP7 triggers U24 and the oscilloscope sweep. U24 output is driven low for the time interval determined by C4 and R6, then resets high. The low-high transition clocks the DAV ENABLE (high) state on U23 to the DAV bus driver U3 (TP8). Resistor R6 is adjusted until the oscilloscope presentation (from TP8) goes high 2 μsec after receipt of the trigger pulse (from TP7).

IV. PROGRAMMING INSTRUCTIONS

A. I/O SPECIFICATIONS

The S/V MUX PCB was designed to receive one binary data byte and to transmit one binary data byte only. End of record codes (EOI, CR, LF) are neither transmitted nor processed by the PCB. When designated as a LISTENER, the PCB stores every byte sent to it by the bus CONTROLLER. For this reason, the CONTROLLER must be programmed to suppress terminal carriage return (CR) and line feed (LF) characters when communicating with the S/V MUX PCB. When designated as a TALKER the PCB can place only one information byte on the data lines and will transmit this byte repeatedly when requested by the CONTROLLER. For this reason, the CONTROLLER must be programmed to read data without requiring any end-of-record indication from the PCB.

The data byte received from the S/V MUX PCB is in the binary form shown in Figure 1. The bus CONTROLLER must decode this information.

B. SAMPLE PROGRAM CODE

References 4-8 contain programming specifications for the HP-9830A and HP-21MX computers. Tables A3 and A4 contain example program codes used to acquire steady-state data. The code used to communicate with the S/V MUX PCB is annotated and listed in the program lines as follows:

CONTROLLER	TABLE	PROGRAM LINES
HP-9830A	A3	295 - 360
HP-21MX	A4	INTEGER FUNCTION IPORT

V. CONCLUSIONS AND RECOMMENDATIONS

The HG-78K Scanivalve Controller described here, when used together with a Scanner and DVM, allows data acquisition from up to five Scanivalves on-line to any computer which is compatible with the Hewlett-Packard Interface Bus. Programs were developed and the operation of the controller was verified using both the HP-9830A and HP-21MX computers. Concurrent manual and computer-controlled operation of each Scanivalve without interference was provided for in the design.

The S/V MUX PCB in the controller was developed as a computer-peripheral device on the HP-IB to enable the computer to obtain Scanivalve address information. The logic circuitry developed and described here satisfied all functional requirements at low cost and high reliability.

While no changes in the design are necessary, a possible improvement in the MULTIPLEXER section is shown in Figure 20. The design in Figure 20 would provide greater input flexibility and fewer components than the initial design shown in Figure 12.

Table I

Logical Equivalences

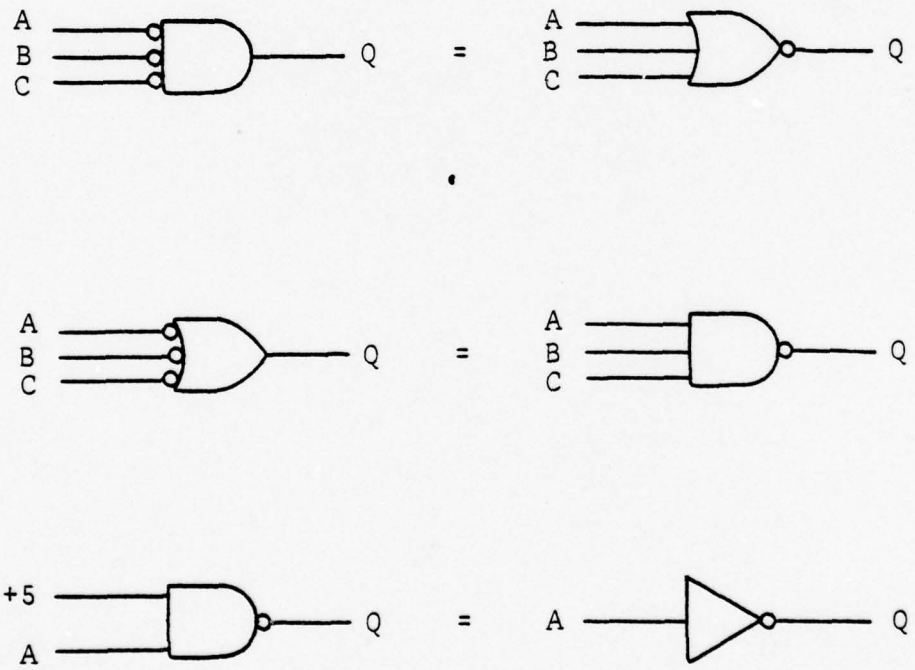


Table II

Logic Circuit Conventions

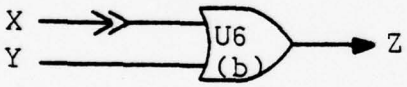
1.  Denotes edge connector

2.  Denotes chassis ground

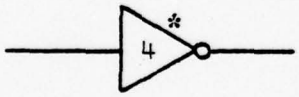
3.  Denotes positive edge trigger. (Information on inputs will transfer to the outputs when trigger line state transitions from low to high.)

4. "TRUE" = "HIGH" level = +2.4 to +5.0 Vdc

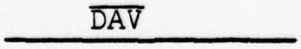
   "FALSE" = "LOW" level = 0.0 to +0.4 Vdc

5. 

Denotes component U6, section (b). Input "x" comes from an edge connector; input "y" comes from another part of the circuit; variable "z" is routed to other circuit sections not shown on the diagram.

6. 

Denotes component U4 has an open-collector output.

7. 

Line identifiers denote the mnemonic logic "high" state. The example shown represents a line that will be "high" when logic dictates a $\overline{\text{DAV}}$ (not DAV) condition.

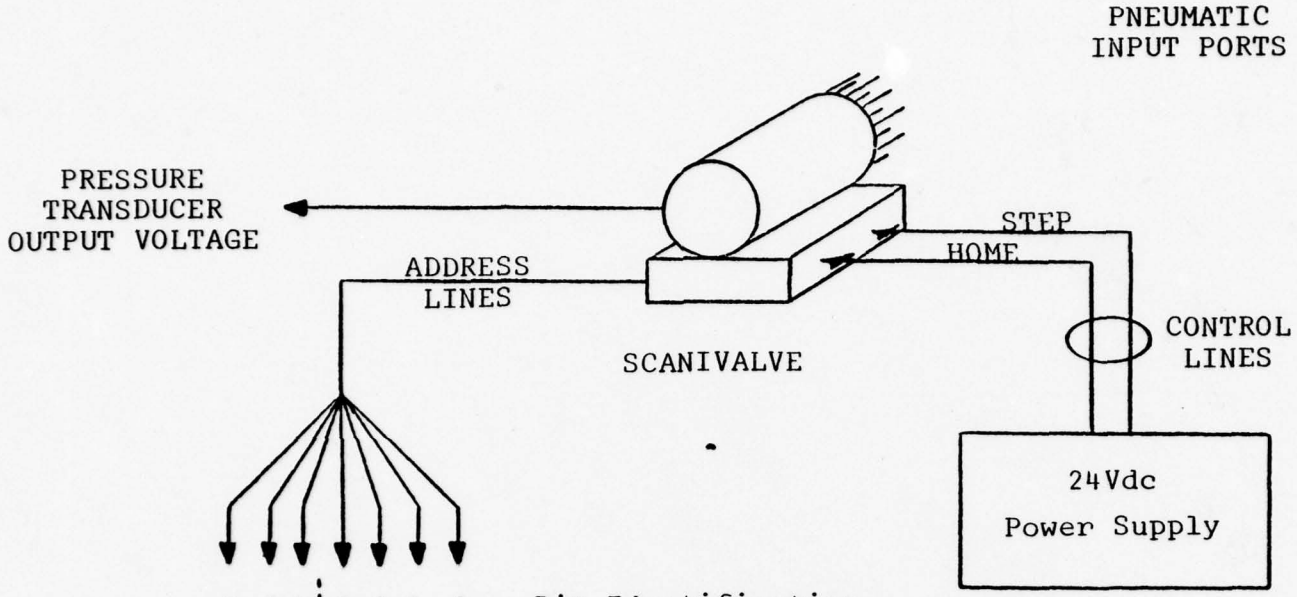


Figure 1

Scanivalve Functions

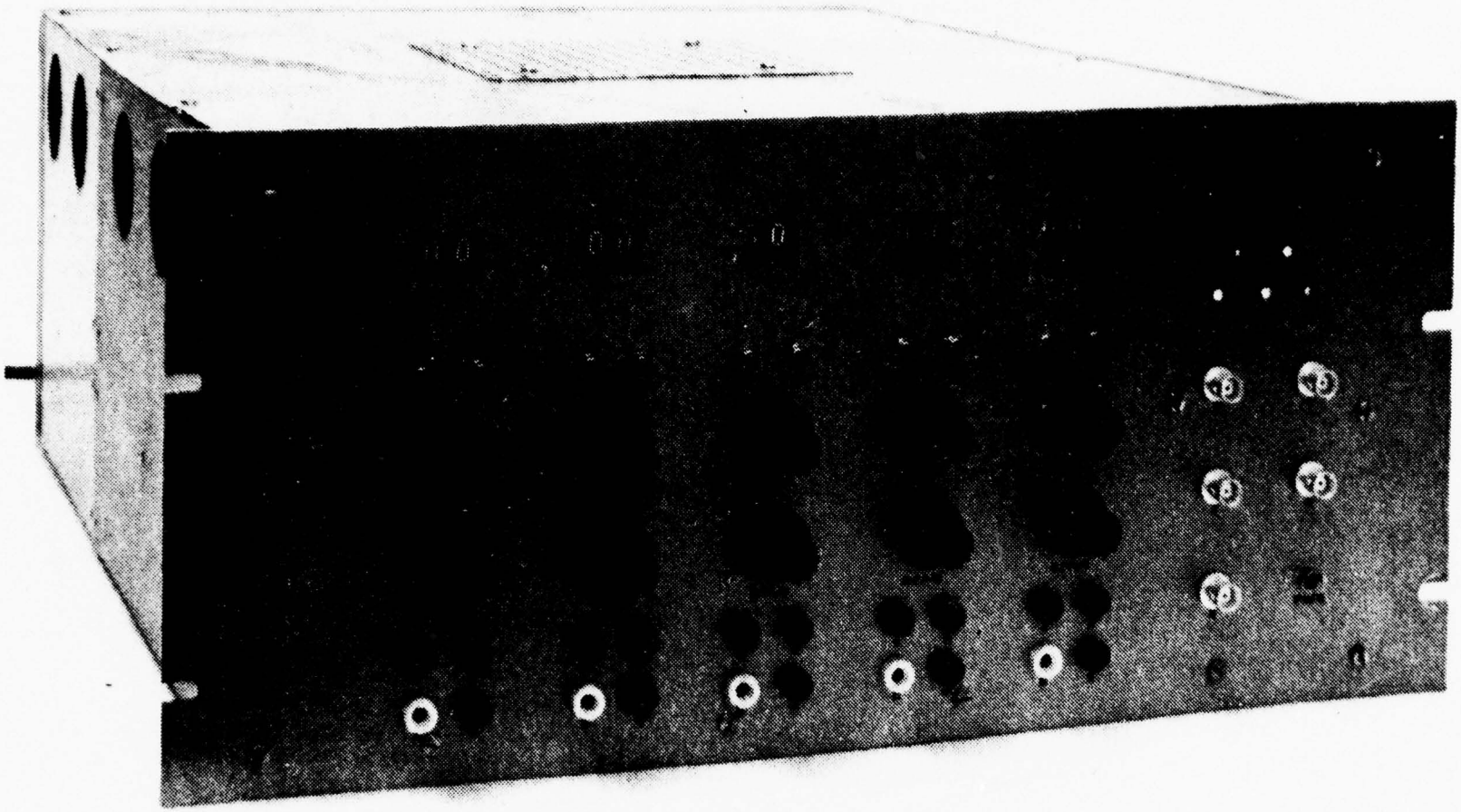


Figure 2: HG-78K Scanivalve Controller

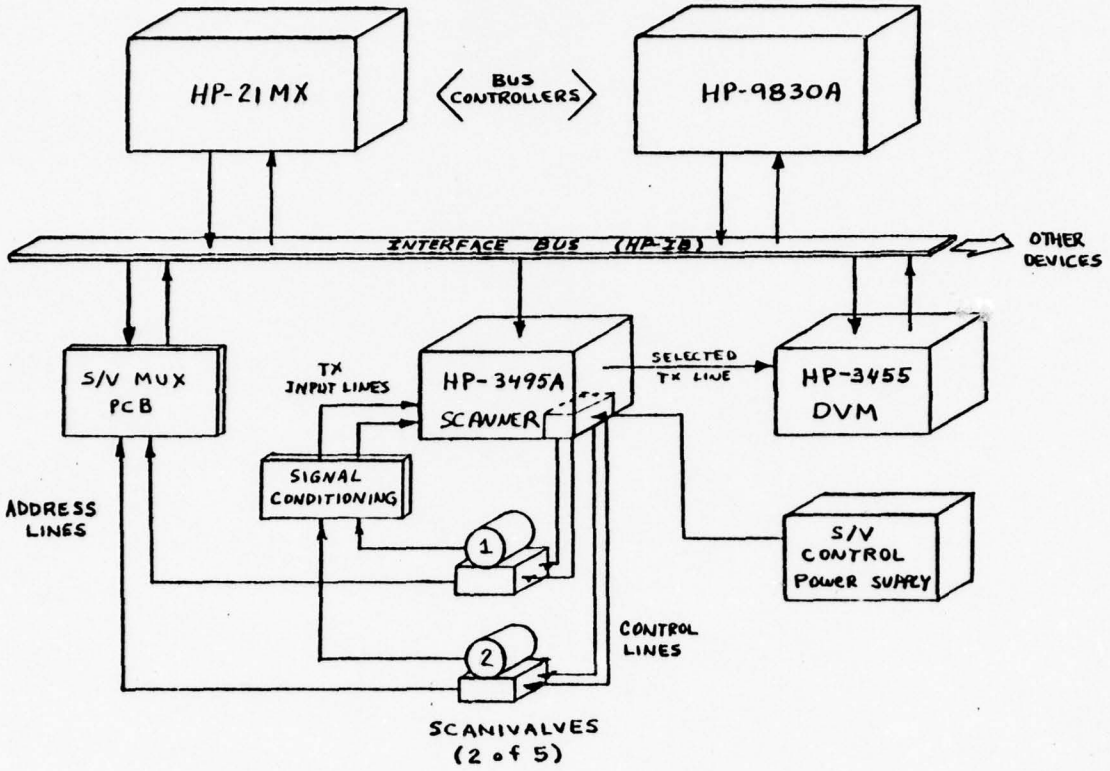


Figure 3: Scanivalve-Computer System Installation

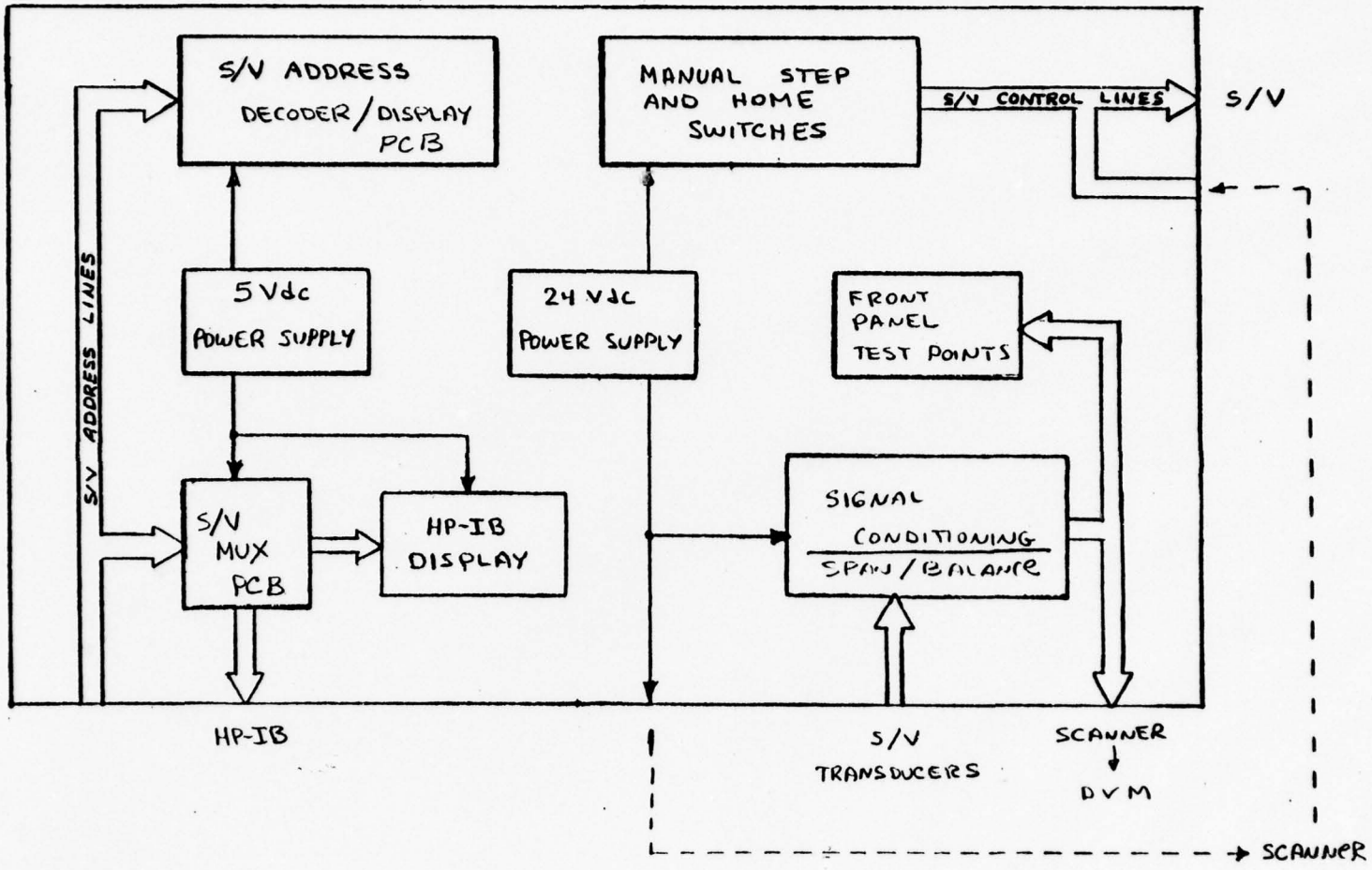


Figure 4: HG-78K Functional Block Diagram

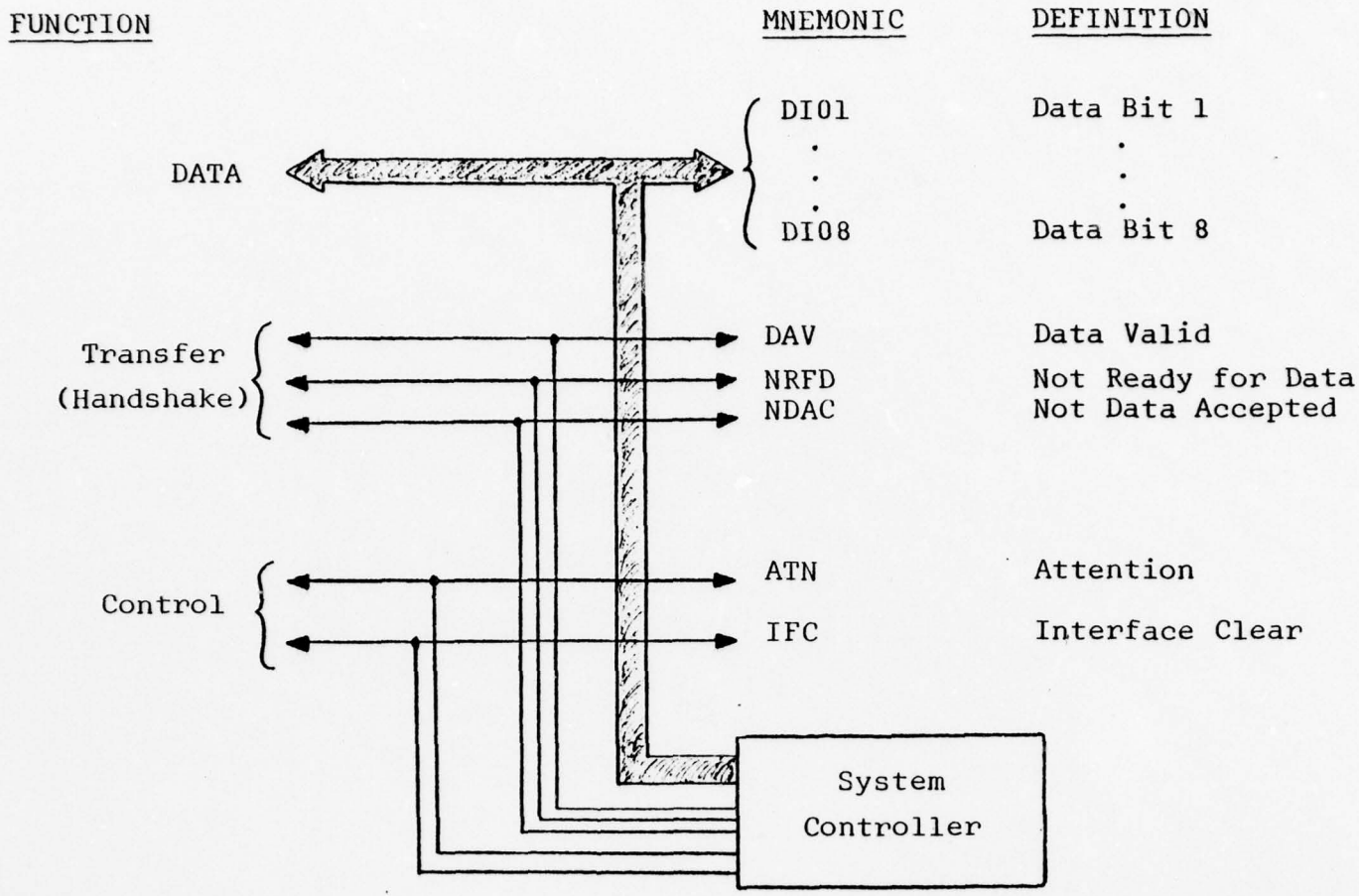


Figure 5

HP-IB Lines

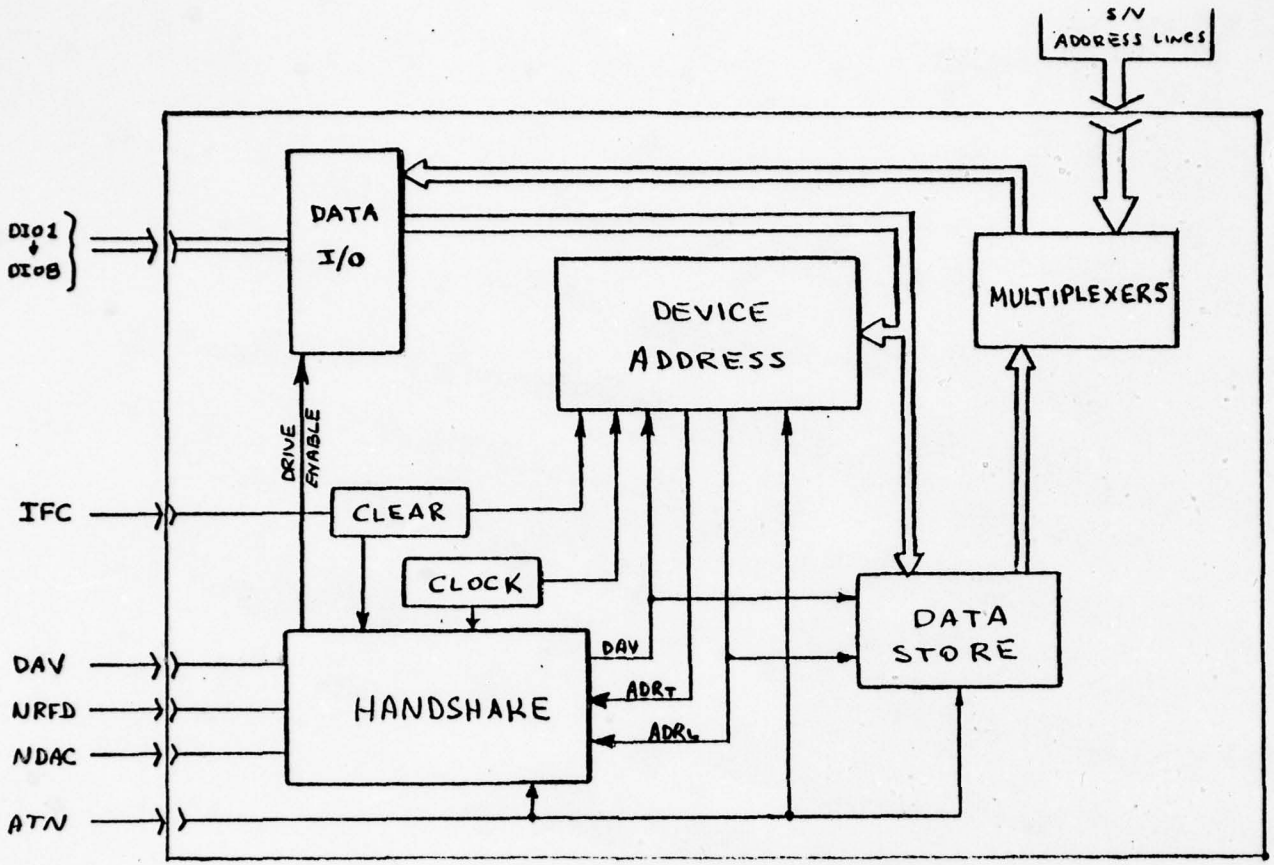


Figure 6

S/V MUX PCB Block Diagram

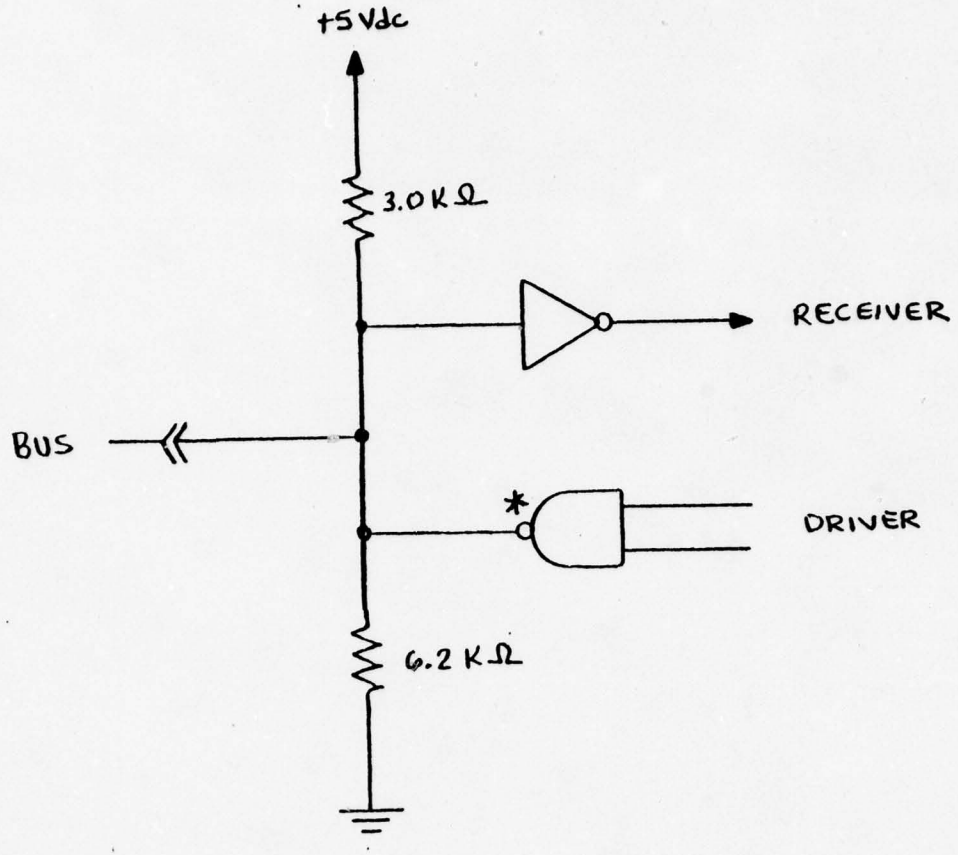


Figure 7

Bi-Directional Bus Connections

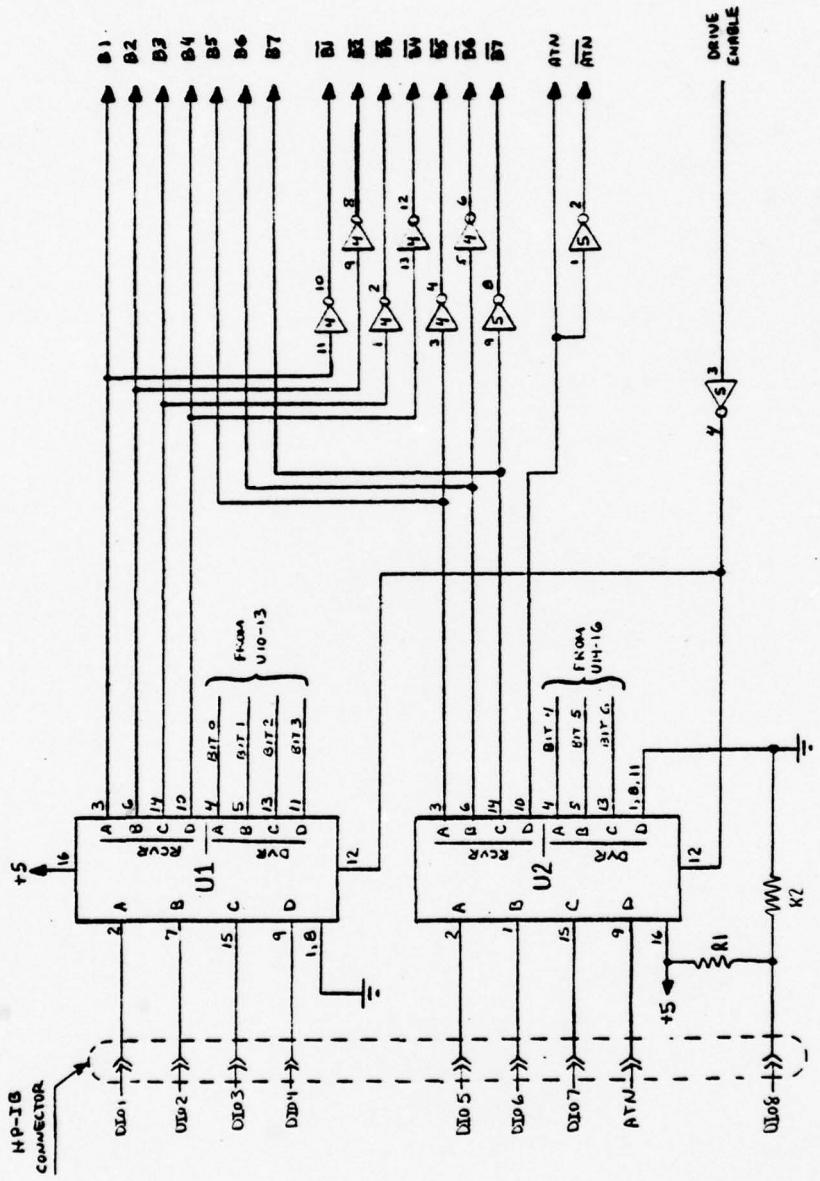


Figure 8: Data I/O Section

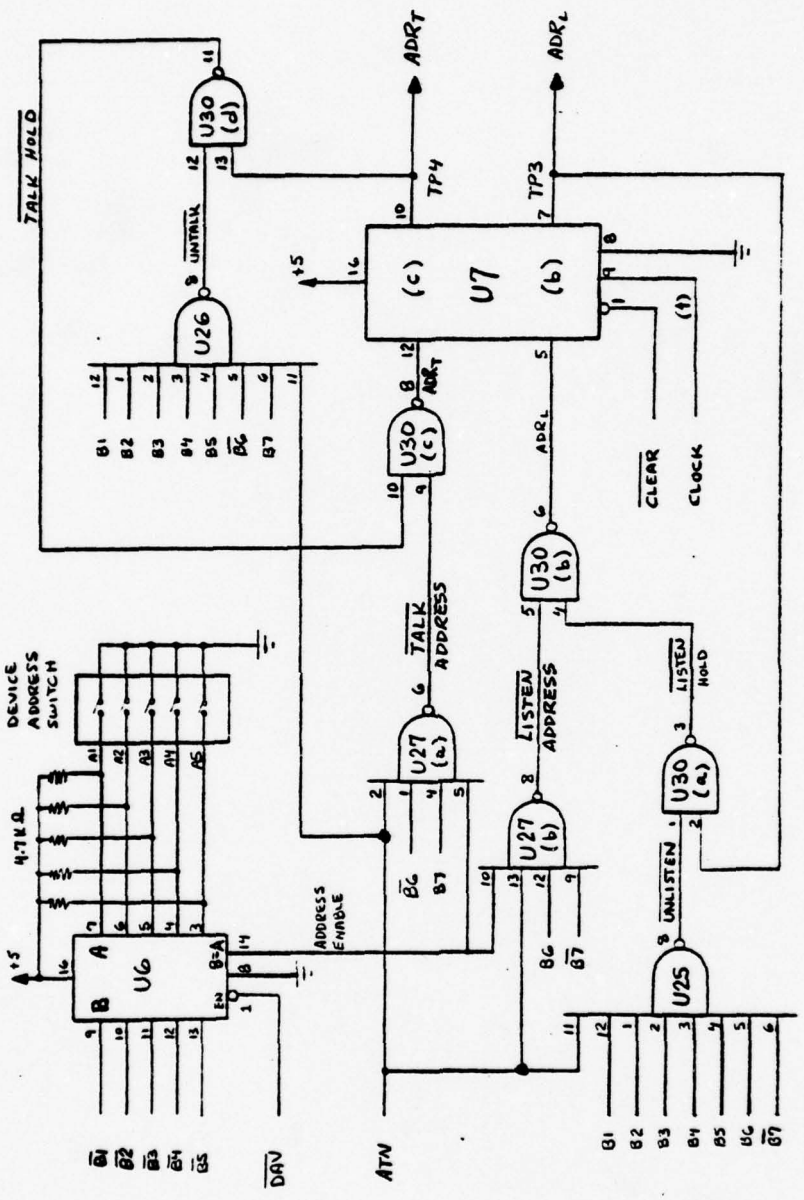
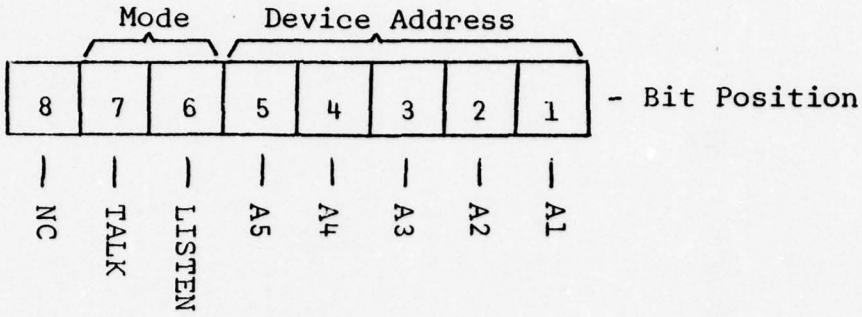


Figure 9: Device Address Section



EXAMPLE

Word: 0100101 (ASCII %)

Meaning: Device with address decimal 5 to LISTEN

Figure 10

HP-IB Address Word Format

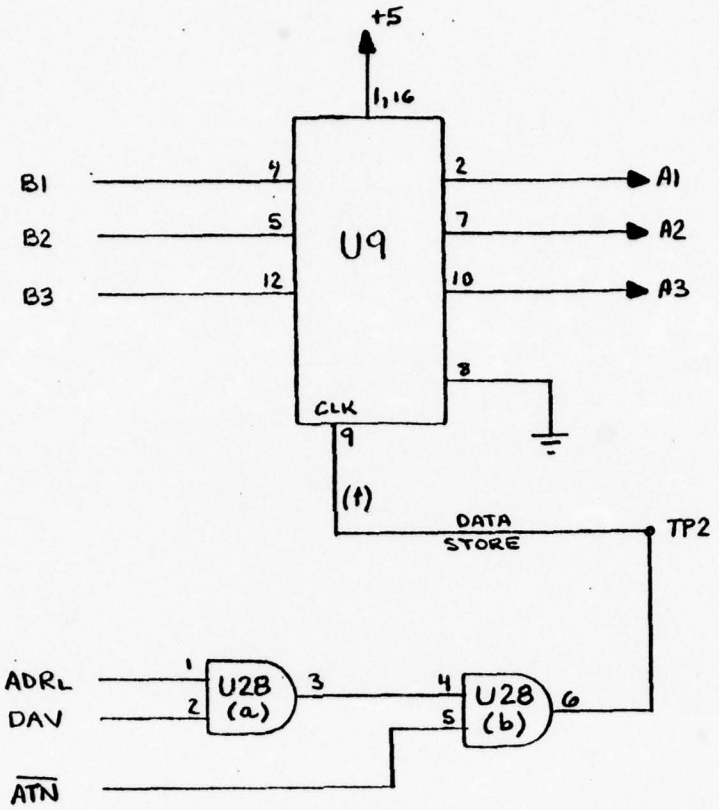


Figure 11

Data Storage Section

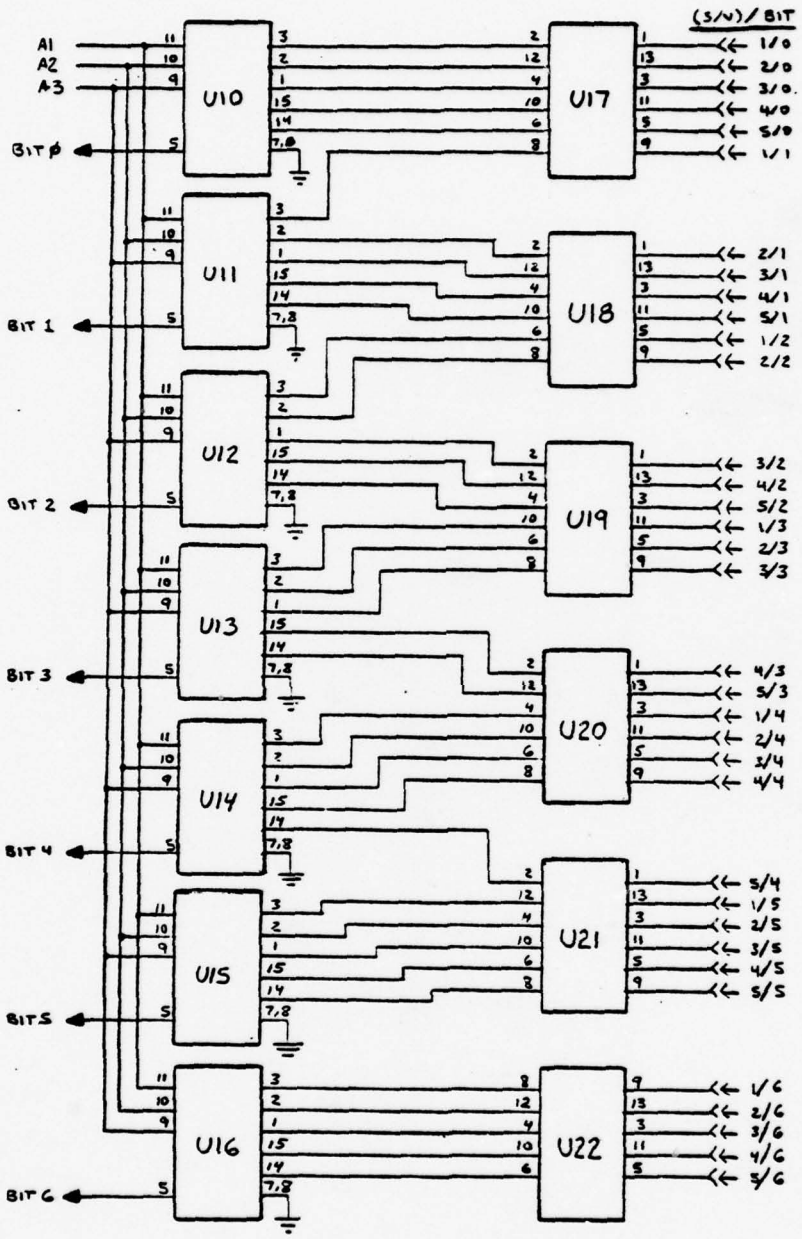


Figure 12

Multiplexer Section

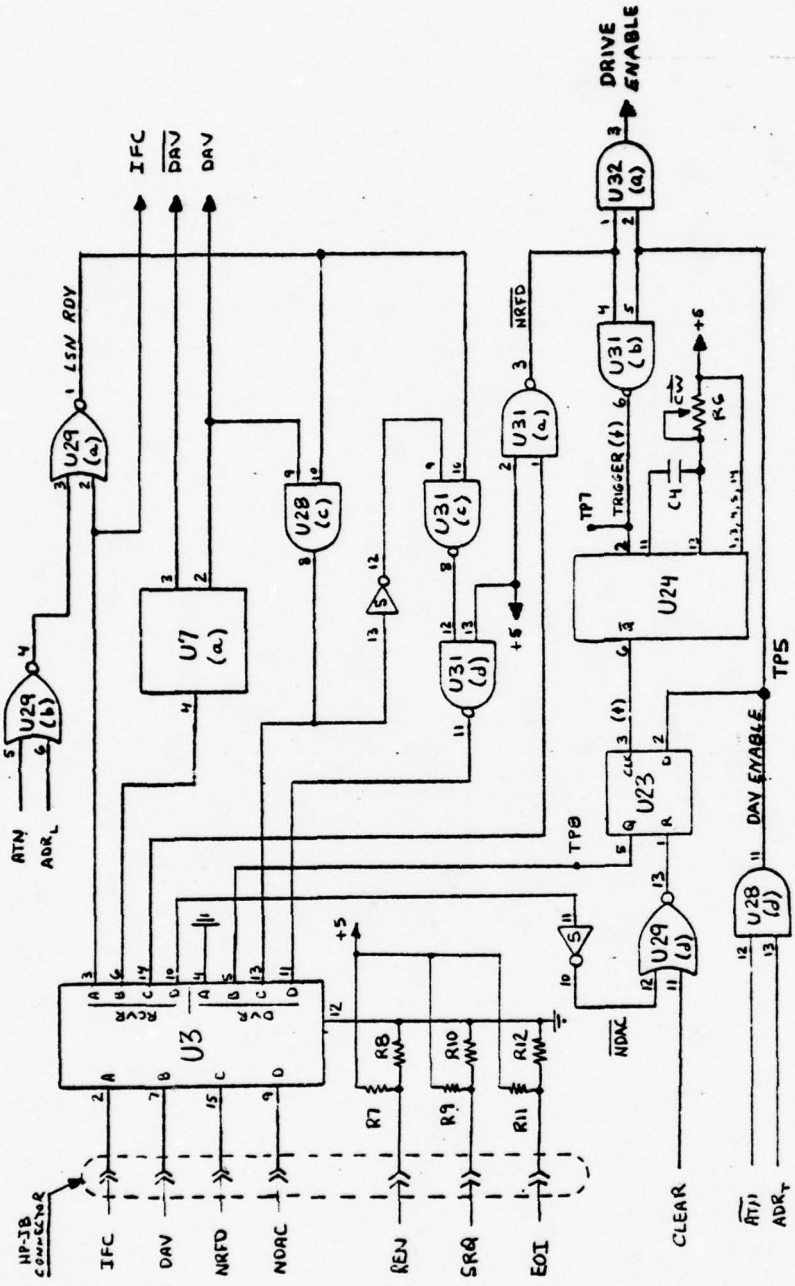
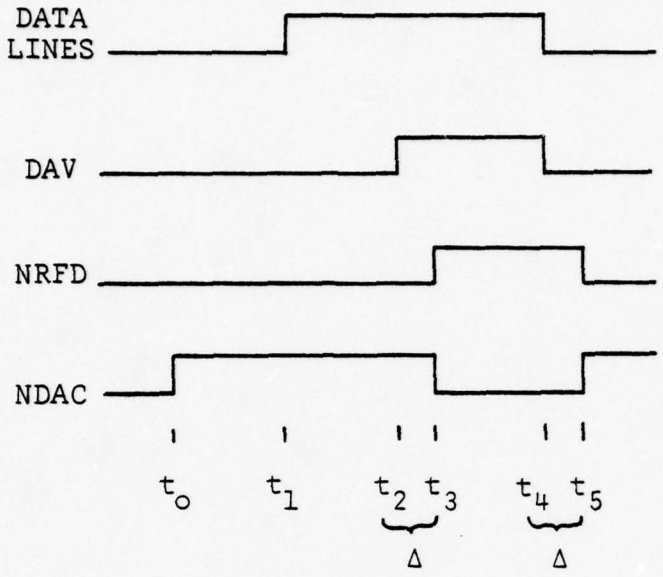


Figure 13

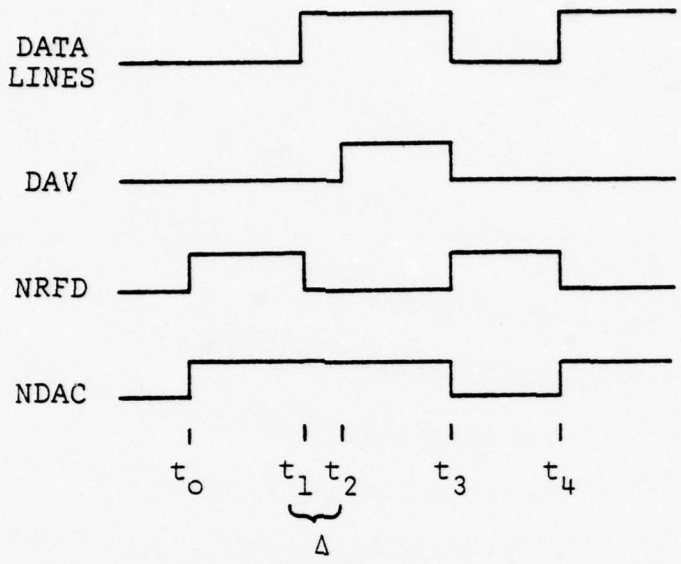
Handshake Section



t_o	Device designated a LISTENER.
t_1	Information placed on data lines.
t_2	TALKER indicates data is valid.
t_3	Device indicates data is accepted and that it is not ready for more data.
t_4	TALKER indicates data is invalid and removes information on data lines.
t_5	Device return to state t_o.
Δ	Variable, 0-100 nano-sec.

Figure 14

Listener Timing Diagram



t_o Device designated a TALKER; computer returns bus to data mode.

t_1 Computer ready for data. Valid data on lines.

t_2 Device indicates data is valid.

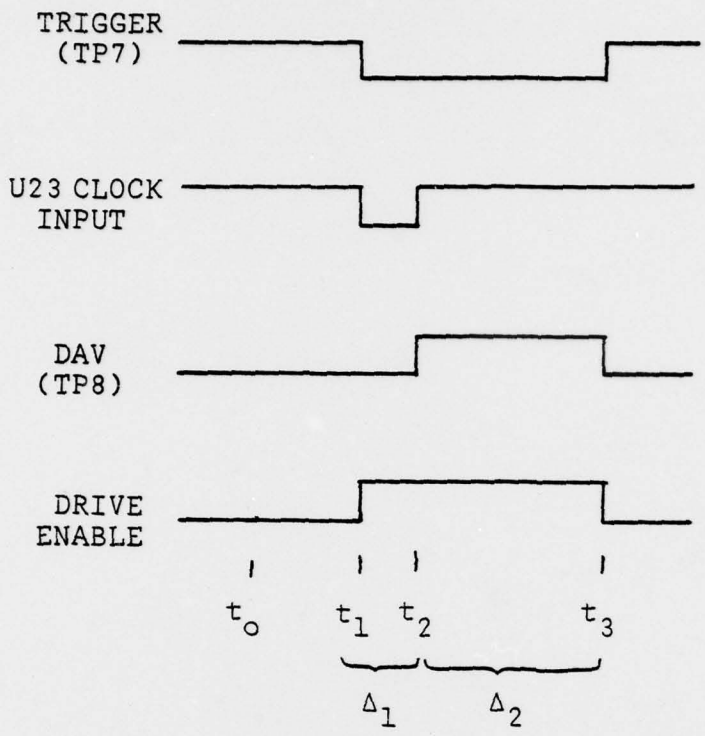
t_3 Computer indicates receipt of data.

t_4 Return to state t_1.

Δ 2 μsec

Figure 15

Talker Timing Diagram



t_o U31(b) and U32(a) enabled.

t_1 $\overline{\text{NRFD}}$ received; U24 triggered.

t_2 Positive-edged clock pulse latches DAV enable state to DAV driver line.

t_3 $\overline{\text{NDAC}}$ received; U23 (DAV) cleared; trigger reset by receipt of NRFD.

Δ_1 2 µsec delay; adjustable by resistor R6.

Δ_2 7.2 µsec for HP-9830A.

Figure 16

DAV Time Delay Sequence

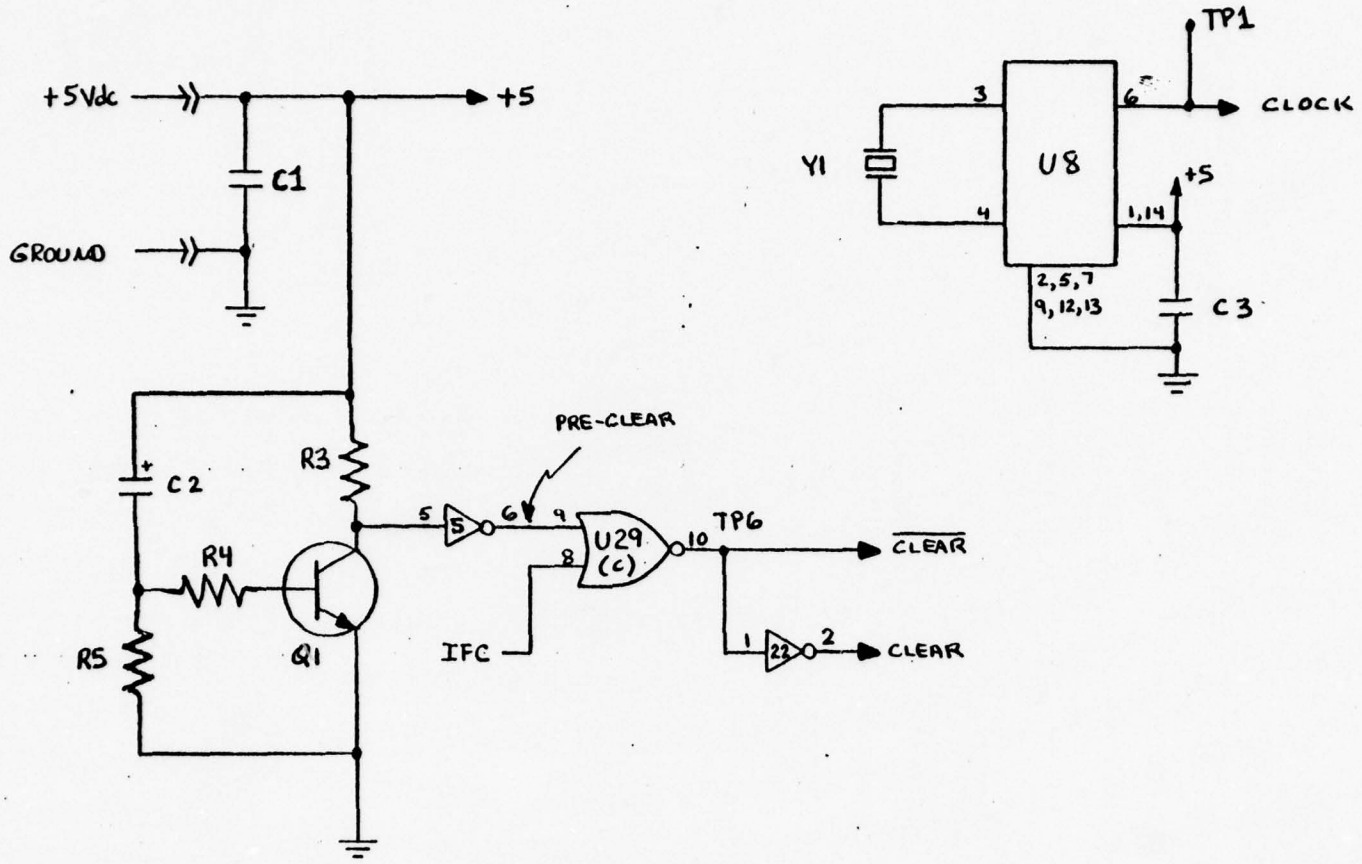


Figure 17

Clock and Clear Sections

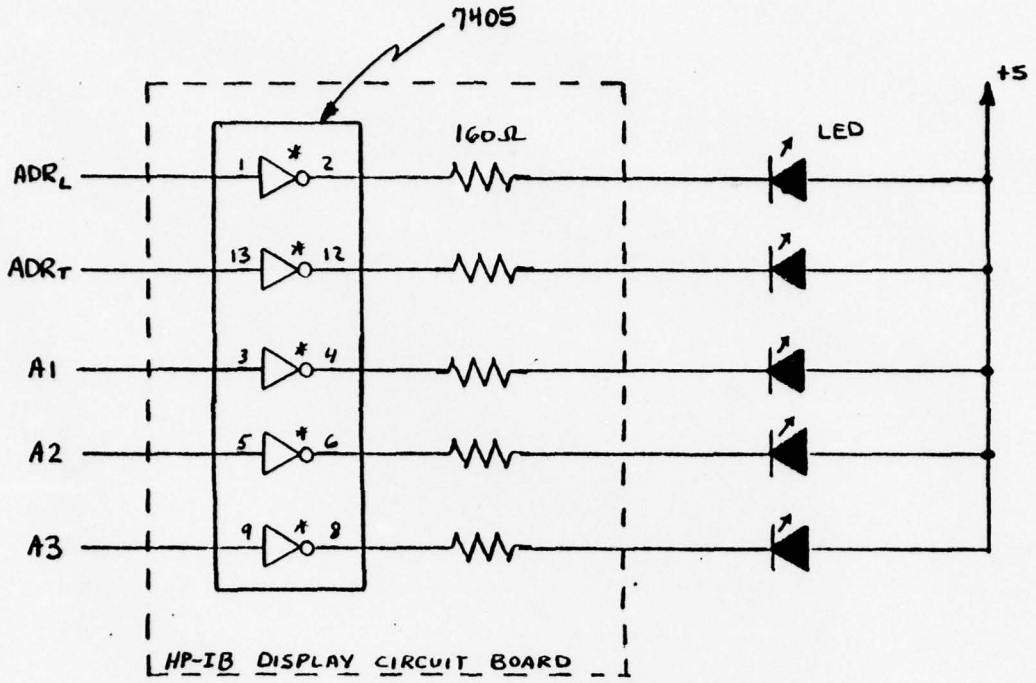


Figure 18

HP-IB Display

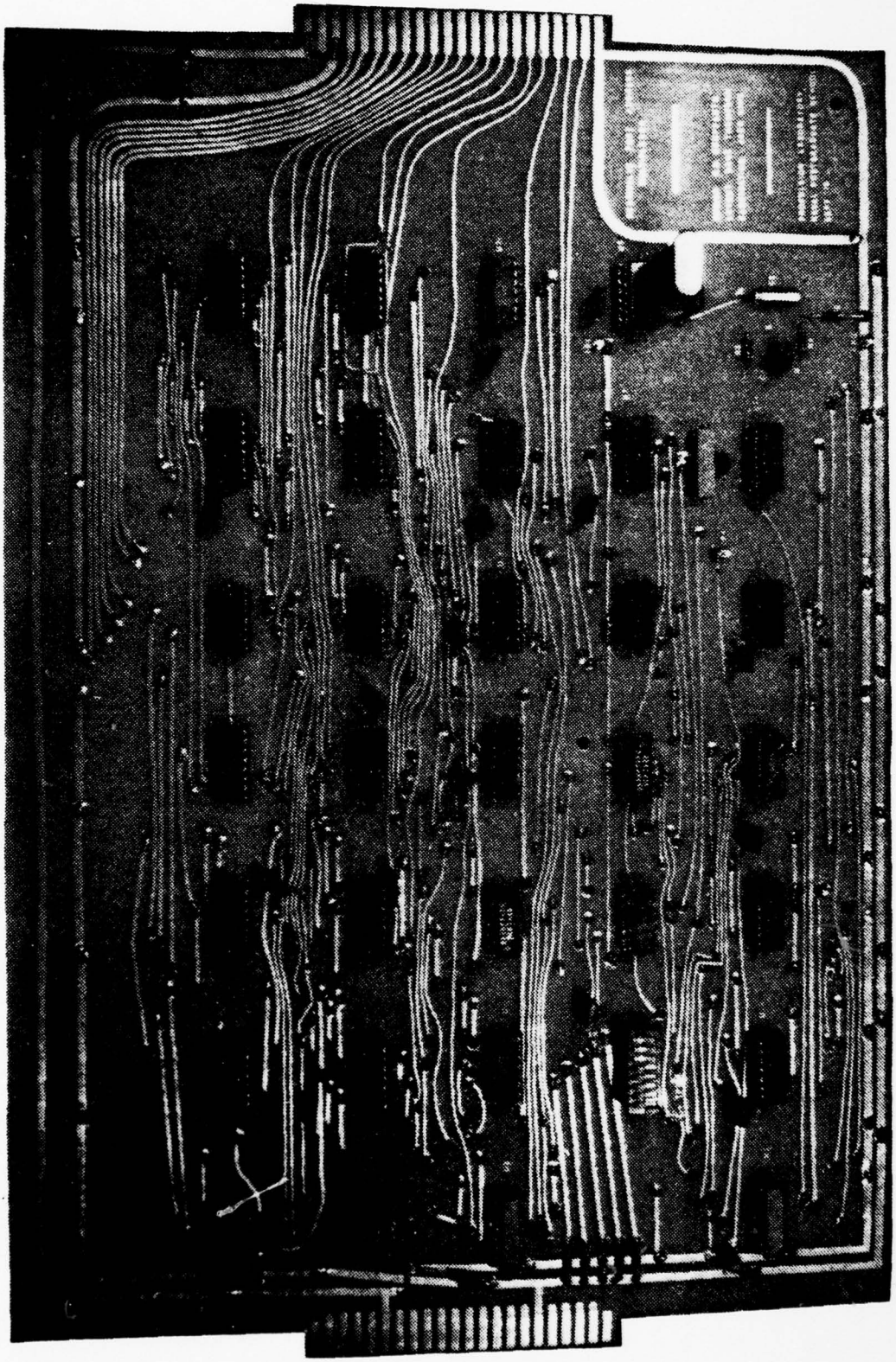


Figure 19: S/V MUX PCB

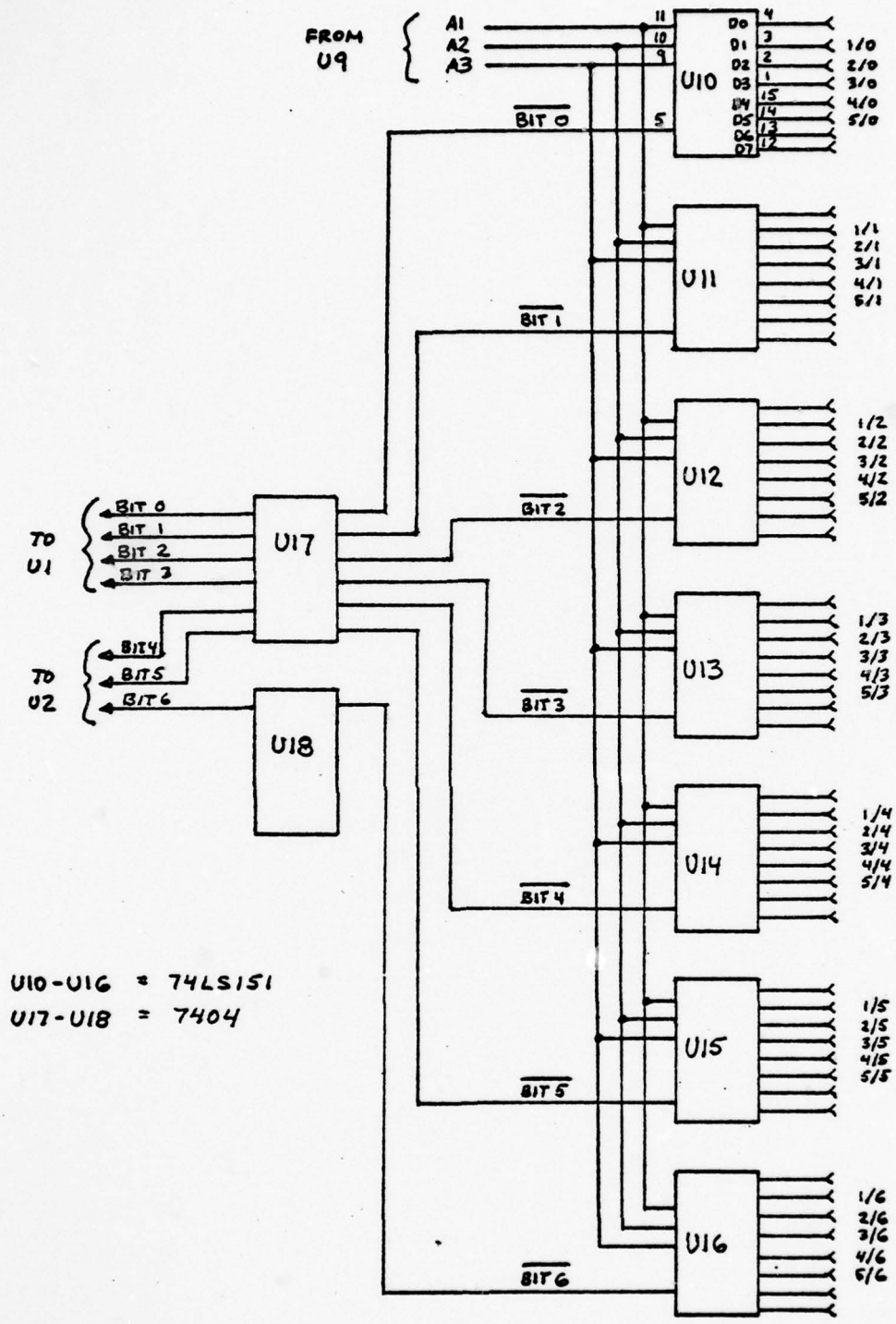


Figure 20

Modified Multiplexer Section

APPENDIX A

DATA ACQUISITION PROGRAM EXAMPLES

This section contains two programs which illustrate the code required to acquire steady-state data using the HP-9830A and HP-21MX computers. The programs were written in modular form to illustrate separately the codes used for each task. Except for INTEGER FUNCTION IPORT , programming efficiency was not intended. In both programs, HP-IB device codes were obtained from Table A1 and Scanner channel assignments were obtained from Table A2.

Table A1

HP-IB Device Codes

Device	21-MX LU#	9830 Talk	9830 Listen
21-MX HPIB PCB	7	@	[SP]
Scanner #1	8		!
DVM	10	C	#
HP-9830	11	D	$
S/V MUX PCB	14	G	'

Table A2

Scanner #1 Channel Assignments

S/V #	FUNCTION		
	Advance	Home	Read
1	00	05	10
2	01	06	11
3	02	07	12
4	03	08	13
5	04	09	14
I	I-1	I+4	I+9

APPENDIX A.1: HP-9830A BASIC Program

The program shown in Table A? was written as a mainline program that calls task subroutines. Each subroutine completes one of three tasks; address interrogation, position control or transducer measurement. The program is straight forward and steps are annotated for clarity.

APPENDIX A.2: HP-21MX FORTRAN Program

The program shown in Table A4 was written as a mainline program with calls to subroutines which communicate with particular HP-IB peripheral devices.

Integer Function IPORT communicates with the S/V MUX PCB using RTE-IV system EXEC calls [5]. Single byte EXEC read and write commands operate on the upper half of the 16-bit word [2]. The factor 256 in lines 76 and 78 represents a shift left or right of 8-bits in the word used to transmit and receive data from the S/V MUX PCB.

Subroutine CNTL communicates with Scanner #1. As discussed in Reference 9, two ASCII characters are required to identify a Scanner channel. For channels ten or above, subroutine CODE can create the necessary ASCII string. For channels 00-09, however, leading zeros are ignored by CODE and the required ASCII string is not formed. To preserve leading zeros, direct ASCII conversion was achieved by adding octal 60 to both the upper and lower bytes of the 16-bit integer word ICHAN (line #124). In either case, the converted integer word is output to Scanner #1 as a two-byte ASCII string in A2 format.

Table A3

HP-9830A Program Listing

```
100 REM     BUS CONTROLLER:  HP-9830A
105 REM
110 REM     VARIABLES:
115 REM
120 REM          I = DESIRED S/V (1-5)
125 REM          A = PRESENT PORT ADDRESS
130 REM          P = DESIRED PORT ADDRESS
135 REM          C = SCANNER CHANNEL
140 REM          V = VOLTAGE
145 REM          Z = S/V DOUBLE BCD PORT CODE
150 REM          T = TEN'S DIGIT
155 REM          U = ONE'S DIGIT
160 REM          J = DUMMY VARIABLE
165 REM
170 REM             * * * MAINLINE * * *
175 REM
180 DIM B$[12]
185 DISP "ENTER S/V IDENT";
190 INPUT I
195 DISP "ENTER DESIRED PORT";
200 INPUT P
205 REM  DEFINE DVM FUNCTION CODES
210 B$="F1R2M3H1T3A1"                    <-- "T3" MUST BE SPECIFIED
215 N2=2                                     [REF. 10]
220 IF I=2 OR I=3 THEN 230
225 N2=1
230 REM
235 REM   INTERROGATE S/V "I"
240 GOSUB 295
245 REM
250 REM   POSITION S/V "I" TO PORT "P"
255 GOSUB 370
260 REM
265 REM   READ AND PRINT PRESSURE
270 GOSUB 530
275 STOP
280 GOTO 185
285 REM ------------------------------------------------
290 REM
295 REM       * * * INTERROGATION SUBROUTINE * * *
300 REM
305 CMD "^D"                    } SEND 1 DATA BYTE TO MUX
310 OUTPUT (13,310)I;           } PCB (SUPPRESS CR/LF) [REF. 4]
315 FORMAT B
320 CMD "^G#"                   } READ 1 DATA BYTE
325 Z=FBYTE(3
330 U=BIAND(Z,15)               }
335 P=POT(Z,4)                  } DECODE S/V ADDRESS
340 T=BIAND(P,7)                }
345 A=10*T+U
350 OUTPUT (13,305,256,95;      } UNTALK S/V MUX PCB
355 FORMAT 3A
360 RETURN
```

```
365 REM
370 REM          * * * CONTROL SUBROUTINE * * *
375 REM
380 FORMAT F3.0
385 D=P-A
390 IF D=0 THEN 515
395 CMD "?D!"                          - SCANNER TO LISTEN
400 IF D>0 THEN 450
405 REM
410 REM   HOME S/V "I"
415 REM
420 C=I+4                              - "HOME" CODE (TABLE A2)
425 OUTPUT (13,380)C                   } CLOSE, OPEN RELAY AND
430 OUTPUT (13,*)"C"                   }   PAUSE 4-SEC
435 WAIT 4000                          }
440 GOTO 495
445 REM
450 REM   ADVANCE S/V "I" TO PORT "P"
455 REM
460 C=I-1                              - "ADVANCE" CODE (TABLE A2)
465 FOR J=1 TO D STEP N2
470 OUTPUT (13,380)C
475 OUTPUT (13,*)"C"
480 WAIT 50                            - ALLOW S/V MECHANISM TO
485 NEXT J                                 RESET
490 REM
495 REM   VERIFY ADDRESS & RETURN
500 REM
505 GOSUB 295
510 GOTO 385
515 RETURN
520 REM ------------------------------------------------
525 REM
530 REM        * * * MEASUREMENT SUBROUTINE * * *
535 REM
540 FORMAT B
545 FORMAT 3B
550 FORMAT F3.0
555 CMD "?D!"                          } CLOSE "READ" RELAY
560 C=I+9                              }   (TABLE A2)
565 OUTPUT (13,550)C                   }
570 CMD "?D"
575 OUTPUT (13,540)768                 - REMOTE ENABLE BUS
580 CMD "?D#",B$                       - PROGRAM DVM FUNCTIONS
585 OUTPUT (13,540)256,B,512;          - TRIGGER DVM
590 CMD "?C$"                          } READ VOLTAGE
595 ENTER (13,*)V                      }
600 WRITE (15,605)I,A,V
605 FORMAT "S/V",F2.0,"  PORT",F3.0," = ",F9.6," PSI"
610 CMD "?D!","C"                      - CLEAR SCANNER
615 RETURN
620 END
```

Table A4

HP-21MX Program Listing

```
0001  FTN4,L
0002        PROGRAM HG78K
0003  C
0004  C             BUS CONTROLLER: HP-21MX
0005  C
0006  C             VARIABLES:
0007  C
0008  C                 IVALVE = DESIRED S/V (1-5)
0009  C                 IAPR   = PRESENT PORT NUMBER
0010  C                 IADES  = DESIRED PORT NUMBER
0011  C                 ICHAN  = SCANNER CHANNEL
0012  C                 VOLTS  = DVM VOLTAGE READING
0013  C
0014  C           * * * * * MAINLINE * * * * *
0015  C
0016        DATA ISTEP /1/
0017        WRITE(1,60)
0018        READ (1,50) IVALVE
0019        WRITE(1,62)
0020        READ (1,52) IADES
0021        IF(IVALVE.EQ.2 .OR. IVALVE.EQ.3) ISTEP=2
0022    10  IAPR = IPORT(IVALVE)
0023        IDEL = IADES - IAPR
0024        IF (IDEL) 100,300,200
0025  C
0026  C             HOME SCANIVALVE
0027  C
0028   100  ICHAN = IVALVE + 4
0029        CALL CNTL(ICHAN,2)
0030        GO TO 10
0031  C
0032  C             ADVANCE SCANIVALVE
0033  C
0034   200  ICHAN = IVALVE - 1
0035        DO 210 J=1,IDEL,ISTEP
0036   210  CALL CNTL(ICHAN,1)
0037        GO TO 10
0038  C
0039  C             MEASURE TRANSDUCER
0040  C
0041   300  ICHAN = IVALVE + 9
0042        CALL CNTL(ICHAN,3)
0043        CALL DVM(VOLTS)
0044  C
0045  C             LIST STEADY-STATE DATA
0046  C
0047        WRITE(1,64)IVALVE,IAPR,VOLTS
0048        WRITE(8,66)
0049        STOP
0050  C
0051    50  FORMAT(I1)
0052    52  FORMAT(I2)
0053    60  FORMAT("S/V #:")
0054    62  FORMAT("DESIRED PORT #:")
0055    64  FORMAT("S/V    PORT    VOLTS"/1X,I1,6X,I2,3X,F9.6)
0056    66  FORMAT("C")
0057        END


 FTN4 COMPILER: HP92060-16092 REV. 1805 (780310)

 **  NO WARNINGS **  NO ERRORS **   PROGRAM = 00176      COMMON = 00000
```

```
0058          INTEGER FUNCTION IPORT (IVALVE)
0059    C
0060    C               THIS PROGRAM INTERROGATES SCANIVALVE
0061    C               "IVALVE" AND CONVERTS PORT ADDRESS
0062    C               INTO A DECIMAL VALUE.
0063    C
0064    C               S/V MUX PCB = LU#14
0065    C               HPIB BUS PCA = LU#7
0066    C
0067    C               VARIABLES:
0068    C
0069    C                 IVALVE = DESIRED S/V
0070    C                 IP     = S/V INPUT BUFFER
0071    C                 MSD    = MOST  SIGNIF. DIGIT
0072    C                 LSD    = LEAST SIGNIF. DIGIT
0073    C                 IPORT  = DECIMAL S/V ADDRESS
0074    C
0075          LU = 14 + 2100B                  — CONFIGURE DRIVER WORD
0076          CALL EXEC(2,LU,IVALVE*256,-1)      [REF 5  P. 3-3]
0077          CALL EXEC(1,LU,IP,-1)
0078          IP=IP/256
0079          MSD = IAND(IP/16,7B)
0080          LSD = IAND(IP,17B)
0081          IPORT = 10*MSD + LSD
0082          CALL ABRT(7,1)
0083          RETURN
0084          END

 FTN4 COMPILER: HP92060-16092 REV. 1805 (780310)

 ** NO WARNINGS ** NO ERRORS **   PROGRAM = 00068      COMMON = 00000
```

```
0085          SUBROUTINE CNTL (ICHAN,K)
0086    C
0087    C             THIS PROGRAM CONTROLS THE
0088    C             CLOSING OF SCANNER RELAYS.
0089    C             PROGRAM OPTIONS ARE INPUT
0090    C             THROUGH VARIABLE "K" AS:
0091    C
0092    C             K          FUNCTION
0093    C            --- -------------------------
0094    C             1   CLOSE RELAY FOR 10-MS,
0095    C                 OPEN RELAY, RETURN
0096    C
0097    C             2   SAME AS K=1 EXCEPT
0098    C                 DELAY 4-SEC PRIOR TO RTN.
0099    C
0100    C             3   CLOSE RELAY, RETURN.
0101    C            --- -------------------------
0102    C
0103    C             SCANNER LU#=8
0104    C
0105    C             VARIABLES:
0106    C
0107    C                 ICHAN = SCANNER CHANNEL
0108    C                 J     = ASCII STRING
0109    C
0110          IF(ICHAN.LT.0 .OR. ICHAN.GT.14) GO TO 900
0111          IF(ICHAN.LT.10) GO TO 100
0112    C
0113    C             ASCII CONVERSION
0114    C             ICHAN >= 10
0115    C
0116          CALL CODE
0117          WRITE(J,60) ICHAN
0118     60   FORMAT(I2)
0119          GO TO 200
0120    C
0121    C             ASCII CONVERSION
0122    C             ICHAN < 10
0123    C
0124    100   J = ICHAN + 30060B        - ADD 60B TO UPPER & LOWER BYTES
0125    C
0126    C             CLOSE RELAY
0127    C
0128    200   WRITE(8,65)J              } SEND INTEGER "J" AS
0129     65   FORMAT(A2)                } 2-BYTE ASCII STRING
0130          IF(K .EQ. 3) RETURN
0131    C
0132    C             10-MS TIME DELAY
0133    C
0134          CALL WAIT(1)
0135    C
0136    C             OPEN RELAY
0137    C
0138          WRITE(8,68)
0139     68   FORMAT("C")
0140    C
0141    C             150-MS TIME DELAY
0142    C
0143          CALL WAIT(15)
0144          IF(K .EQ. 1) RETURN
0145    C
0146    C             4-SEC TIME DELAY
0147    C
0148          CALL WAIT(400)
0149          RETURN
0150    900   WRITE(1,90)ICHAN
0151     90   FORMAT("ILLEGAL SCANNER CHAN INPUT TO SUBR CNTL: ",I4)
0152          RETURN
0153          END


 FTN4 COMPILER: HP92060-16092 REV. 1805 (780310)

 **  NO WARNINGS **  NO ERRORS **   PROGRAM = 00127      COMMON = 00000
```

```
0154          SUBROUTINE DVM (VOLTS)
0155    C
0156    C             THIS PROGRAM CONTROLS
0157    C             THE HP-3455A DVM.
0158    C
0159    C             DVM LU#=10
0160    C             HPIB LU#=7
0161    C
0162          CALL RMOTE (10)
0163          CALL CLEAR (10,1)
0164          WRITE (10,60)
0165          CALL TRIGR (10)
0166          READ (10,*) VOLTS
0167          RETURN
0168     60   FORMAT ("F1R2M3A0T3")
0169          END
```

FTN4 COMPILER: HP92060-16092 REV. 1805 (780310)

** NO WARNINGS ** NO ERRORS ** PROGRAM = 00039 COMMON = 00000

```
0170          SUBROUTINE WAIT (N)
0171    C
0172    C             THIS PROGRAM USES THE HP-21MX
0173    C             SYSTEM CLOCK TO PRODUCE A
0174    C             DELAY OF (N*10)-MILLISECONDS.
0175    C
0176    C             VARIABLES:
0177    C
0178    C                 NM   = # OF MINUTES
0179    C                 IT   = INPUT TIME BUFFER
0180    C                 ITF  = COMPUTED FINAL TIME
0181    C                 INOW = PRESENT TIME
0182    C
0183    C
0184          DIMENSION IT(5)
0185          CALL EXEC (11,IT,IY)
0186          NM=IT(3)
0187          ITF=IT(1) + 100*IT(2) + N
0188     10   IF(ITF.LE.5999) GO TO 20
0189          NM=NM + 1
0190          ITF=ITF - 6000
0191          GO TO 10
0192     20   CALL EXEC (11,IT,IY)
0193          INOW=IT(1) + 100*IT(2)
0194          IF(ITF-INOW)30,30,20
0195     30   IF(NM-IT(3))99,99,20
0196     99   RETURN
0197          END
```

FTN4 COMPILER: HP92060-16092 REV. 1805 (780310)

** NO WARNINGS ** NO ERRORS ** PROGRAM = 00092 COMMON = 00000

APPENDIX B

HG-78K HARDWARE

APPENDIX B.1: HG-78K Input/Output Wiring

This section documents the I/O wiring of the HG-78K Scanivalve Controller. Figure B1 shows the back panel layout and Tables B1 through B6 list the associated wiring connections. Figure B2 shows the Scanivalve transducer signal conditioning circuit with associated back and front panel connections.

APPENDIX B.2: S/V Address Decoder/Display PCB

The address lines in a Scanivalve are connected to circuit ground to define a "true" state. In the DECODER/DISPLAY, the address lines were connected to 7404 inverters in order to convert to the "high" = "true" logic required for input to HP-5082-7300 BCD-DECIMAL decoder/driver display integrated circuits. The circuit is shown in Figure B3 and external wiring is listed in Table B7.

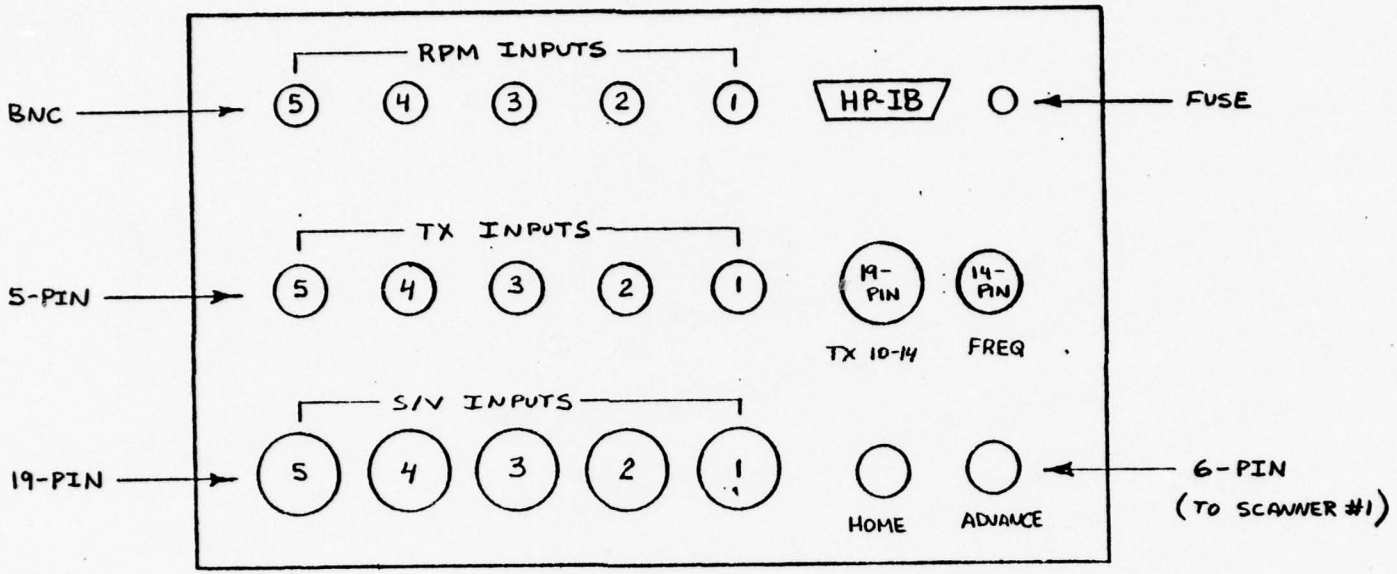


Figure B1

HG-78K Back Panel Layout

Table B1

24-Pin HP-IB Connector

HP-IB PIN #	FUNCTION	S/V MUX PCB LEFT EDGE CONNECTOR
1	DI01	19
2	DI02	20
3	DI03	22
4	DI04	21
5	EOI	N
6	DAV	2
7	NRFD	4
8	NDAC	3
9	IFC	1
10	SRQ	L
11	ATN	8
12	NC	
13	DI05	5
14	DI06	6
15	DI07	10
16	DI08	17
17	REN	R
18	CKT GND	J
19	CKT GND	J
20	CKT GND	J
21	CKT GND	J
22	CKT GND	J
23	CKT GND	J
24	CKT GND	J

Table B2

19-Pin Transducer Connector

PIN	FUNCTION	WIRE
A	TX #1; Pin B	White
B	TX #1; Pin C	Green
C	Shield #1	Black
D	TX #2; Pin B	White
E	TX #2; Pin C	Green
F	Shield #2	Black
G	TX #3; Pin B	White
H	TX #3; Pin C	Green
J	Shield #3	Black
K	TX #4; Pin B	White
L	TX #4; Pin C	Green
M	Shield #4	Black
N	TX #5; Pin B	White
P	TX #5; Pin C	Green
R	Shield #5	Black
S	NC	
T	NC	
U	NC	
V	NC	

Table B3

14-Pin Frequency Connector

PIN	FUNCTION	WIRE
A	BNC #1	OR
B	GND	BL
C	BNC #2	OR
D	GND	BL
E	BNC #3	OR
F	GND	BL
G	BNC #4	OR
H	GND	BL
I	BNC #5	OR
J	GND	BL

Table B4

19-Pin Scanivalve Input Connectors

PIN	S/V Connector #					FUNCTION
	1	2	3	4	5	
A						Chassis ground
B						Logic ground
C						+24 VDC
D						Advance
E						Home
F	1/0	2/0	3/0	4/0	5/0	Address bit 0
G	1/1	2/1	3/1	4/1	5/1	Address bit 1
H	1/2	2/2	3/2	4/2	5/2	Address bit 2
J	1/3	2/3	3/3	4/3	5/3	Address bit 3
K	1/4	2/4	3/4	4/4	5/4	Address bit 4
L	1/5	2/5	3/5	4/5	5/5	Address bit 5
M	1/6	2/6	3/6	4/6	5/6	Address bit 6
N						Address common (ground)

Table B5

6-Pin Scanivalve Advance Connector

SOURCE *	PIN	SCANNER CHANNEL
Pin B	A	
S/V #1; Pin D	B	00
S/V #2; Pin D	C	01
S/V #3; Pin D	D	02
S/V #4; Pin D	E	03
S/V #5; Pin D	F	04

Table B6

6-Pin Scanivalve Home Connector

SOURCE *	PIN	SCANNER CHANNEL
Pin B	A	
S/V #1; Pin E	B	05
S/V #2; Pin E	C	06
S/V #3; Pin E	D	07
S/V #4; Pin E	E	08
S/V #5; Pin E	F	09

*Table B4

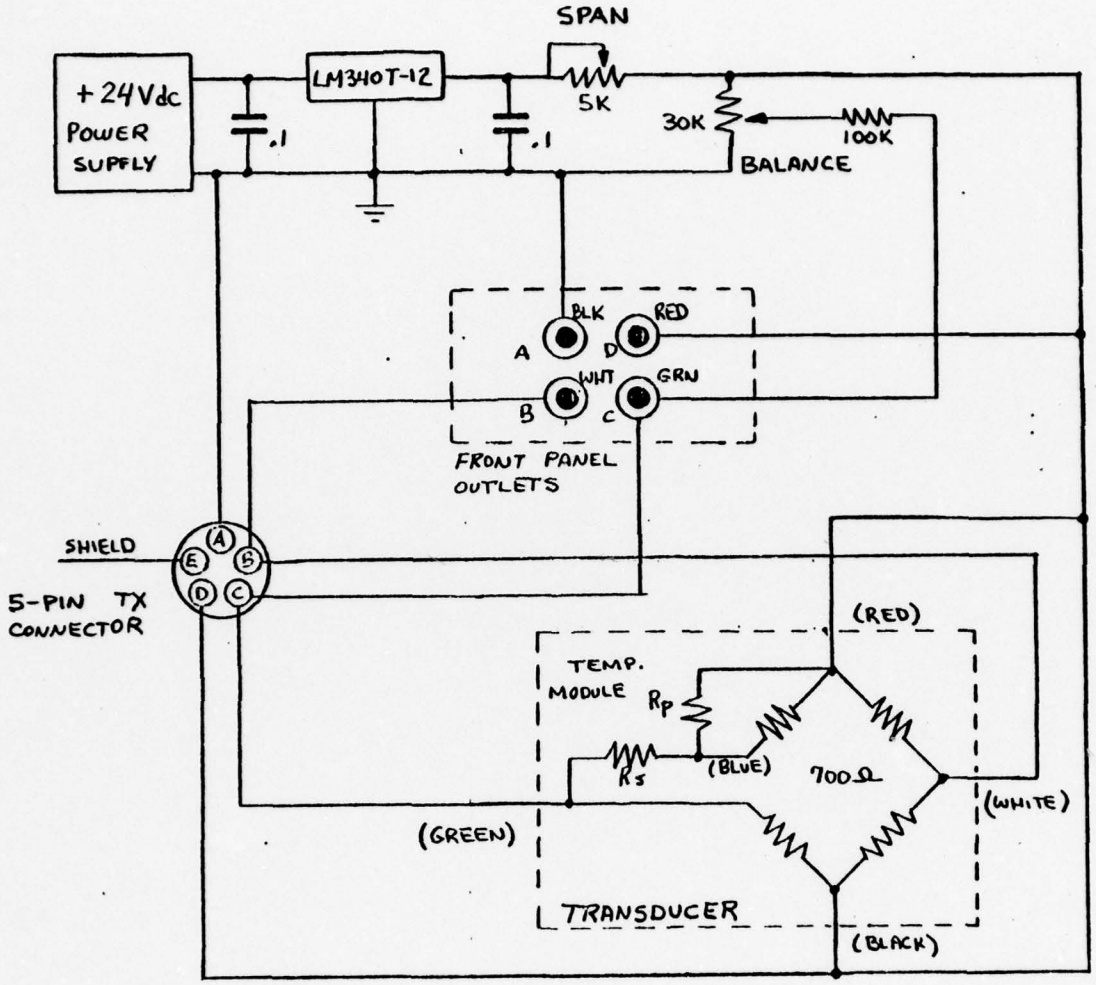
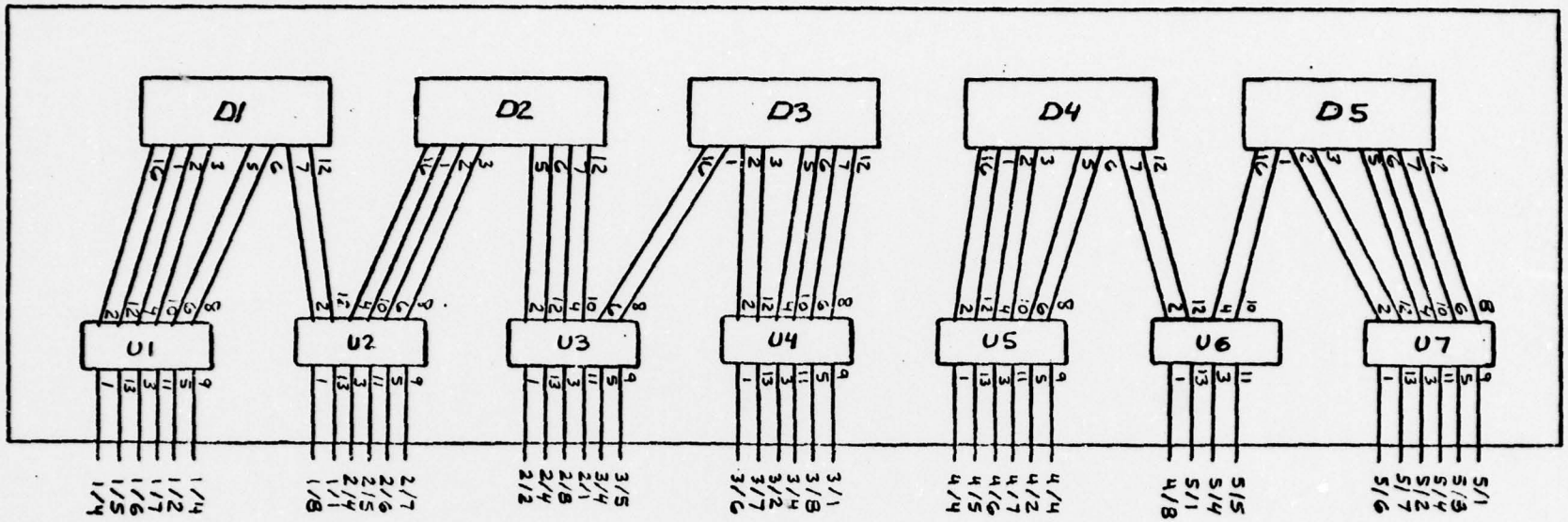


Figure B2

Transducer Signal Conditioning



IC	INPUT	PIN CONNECTIONS	COMPONENT TYPE
D1 - D5	+5 GND	4, 8, 11, 15 9, 10, 13, 14	NUMERIC DISPLAY HP-5082-7300 (2 ea/SOCKET)
U1 - U7	+5 GND	14 7	7404 HEX INVERTER

Figure B3: Scanivalve Address Decoder/Display Circuit

Table B7

S/V Address Decoder/Display Edge Connections

Component Side			Foil Side	
	Ground	1 - A	1/4	Wht
Red	1/5	2 - B	1/6	Red
		3 - C	1/1	Blk
Blk	1/2	4 - D	1/3	Grn
Wht	1/0	5 - E	2/4	Grn
Red	2/5	6 - F	2/6	Wht
		7 - H	2/1	Grn
Wht	2/2	8 - J	2/3	Blk
Grn	2/0	9 - K	3/4	Grn
Blk	3/5	10 - L	3/6	Blk
		11 - M	3/1	Red
Grn	3/2	12 - N	3/3	Red
Grn	3/0	13 - P	4/4	Red
		14 - R	4/5	Grn
		15 - S	4/6	Grn
		16 - T	4/1	Wht
Red	4/2	17 - U	4/3	Blk
Red	4/0	18 - V	5/4	Blk
Wht	5/5	19 - W	5/6	Wht
		20 - X	5/1	Blk
Wht	5/2	21 - Y	5/3	Wht
	+5Vdc	22 - Z	5/0	Red

EXAMPLE

PIN F is Scanivalve #2, bit 6 and has a white wire connected to its terminal.

APPENDIX C

S/V MUX PCB HARDWARE

A component listing is given in Table C1. Test points provided on the circuit board are summarized in Table C2. External connections are given in Tables C3 and C4.

Table C1

S/V MUX PCB Component Listing

Integrated Circuits

U1	MC3441P		
U2	MC3441P		
U3	MC3441P		
U4	7404		
U5	7404		
U6	9324DC		
U7	74LS175		
U8	MC4024P		
U9	74LS175		
U10	74LS151		
U11	74LS151		
U12	74LS151		
U13	74LS151		
U14	74LS151		
U15	74LS151		
U16	74LS151		
U17	7404		
U18	7404		
U19	7404		
U20	7404		
U21	7404		
U22	7404		
U23	7474		
U24	74LS122		
U25	7430	U29	7402
U26	7430	U30	7400
U27	7420	U31	7400
U28	7408	U32	7408

Resistors

R1	3.0K
R2	6.2K
R3	4.7K
R4	4.7K
R5	4.7K
R6	50K (10-turn)
R7	3.0K
R8	6.2K
R9	3.0K
R10	6.2K
R11	3.0K
R12	6.2K

Capacitors

C1	10µF TANTALUM
C2	5µF ELECTROLYTIC
C3	.1µF
C4	360pF

Transistor

Q1	2N3904

Crystal

Y1	56MHZ

Table C2

S/V MUX PCB Test Point Summary

TP1	Clock
TP2	Data Store
TP3	ADR_L
TP4	ADR_T
TP5	DAV Enable
TP6	Clear
TP7	Trigger
TP8	DAV Driver

Table C3

S/V MUX PCB Left Edge Connections

Left Edge Connector

Component Side				Foil Side		
			A - 1	IFC	(BLK)	9
			B - 2	DAV	(WHT)	6
			C - 3	NDAC	(GRN)	8
			D - 4	NRFD	(RED)	7
			E - 5	DI05	(BLK)	13
Pwr supp	(RED)	+5Vdc	F - 6	DI06	(WHT)	14
			H - 7			
24	(BLK)	CKT GND	J - 8	ATN	(GRN)	11
			K - 9			
10	(WHT)	SRQ	L - 10	DI07	(RED)	15
			M - 11			
5	(RED)	EOI	N - 12			
			P - 13			
17	(GRN)	REN	R - 14			
			S - 15			
			T - 16			
Pwr supp	(BLK)	Supp GND	U - 17	DI08	(BLK)	16
			V - 18			
			W - 19	DI01	(WHT)	1
			X - 20	DI02	(GRN)	2
			Y - 21	DI04	(RED)	4
			Z - 22	DI03	(BLK)	3

HP-IB Connector

EXAMPLE: PIN 8 is the ATN line connected by a green wire from HP-IB connector PIN 11.

Table C4

S/V MUX PCB Right Edge Connections

Component Side			Right Edge Connector ↓		Foil Side		
		Ground	A - 1		Ground		
			B - 2				
		+5 Vdc	C - 3		+5 Vdc		
G/2	(GRN)	2/1	D - 4				
G/3	(RED)	3/1	E - 5		5/3	(WHT)	J/5
G/5	(BLK)	5/1	F - 6		2/4	(GRN)	K/2
H/2	(WHT)	2/2	H - 7		4/4	(RED)	K/4
J/1	(GRN)	1/3	J - 8		4/3	(BLK)	J/3
J/3	(RED)	3/3	K - 9		1/4	(WHT)	K/1
H/1	(BLK)	1/2	L - 10		3/4	(GRN)	K/3
G/4	(WHT)	4/1	M - 11		1/5	(RED)	L/1
F/2	(GRN)	2/0	N - 12		3/5	(BLK)	L/3
F/4	(RED)	4/0	P - 13		5/5	(WHT)	L/5
G/1	(BLK)	1/1	R - 14		4/5	(GRN)	L/4
F/1	(WHT)	1/0	S - 15		2/5	(RED)	L/2
F/3	(GRN)	3/0	T - 16		5/4	(BLK)	K/5
F/5	(RED)	5/0	U - 17		2/6	(WHT)	M/2
J/2	(BLK)	2/3	V - 18		4/6	(GRN)	M/4
H/5	(WHT)	5/2	W - 19		1/6	(RED)	M/1
H/3	(GRN)	3/2	X - 20		3/6	(BLK)	M/3
H/4	(RED)	4/2	Y - 21		5/6	(WHT)	M/5
		Ground	Z - 22		Ground		

↑ ↑

Scanivalve 19-Pin

EXAMPLE

PIN 10 is S/V3, bit 4 connected by a green wire from PIN K of Scanivalve 19-Pin connector #3.

LIST OF REFERENCES

1. Naval Postgraduate School Report 57Va72091A, A Description of the Turbopropulsion Laboratory in the Aeronautics Department at the Naval Postgraduate School, by M.H. Vavra and R.P. Shreeve, September 1972.

2. Operating and Service Manual, Bus Input/Output Interface Kit 59310A, Hewlett-Packard, 1975.

3. Lancaster, D., TTL Cookbook, Sams, 1976.

4. Operating Manual, 11272B Extended I/O ROM, Hewlett-Packard, 1972.

5. User's Guide, HP 59310A/B Interface Bus I/O Kit, Hewlett-Packard, 1977.

6. User's Manual, The HP-IB in HP 1000 Computer Systems, Hewlett-Packard, 1978.

7. User's Guide, Hewlett-Packard Interface Bus for Systems Based on the HP-9830A Calculator, Hewlett-Packard, 1974.

8. Programming and Service Manual, HP-IB Calculator Interface 59405A, Hewlett-Packard, 1974.

9. Programming and Service Manual, HP-3495A Scanner, Hewlett-Packard, 1977.

10. Operating Information, HP-3455A Digital Voltmeter, Hewlett-Packard, 1976.

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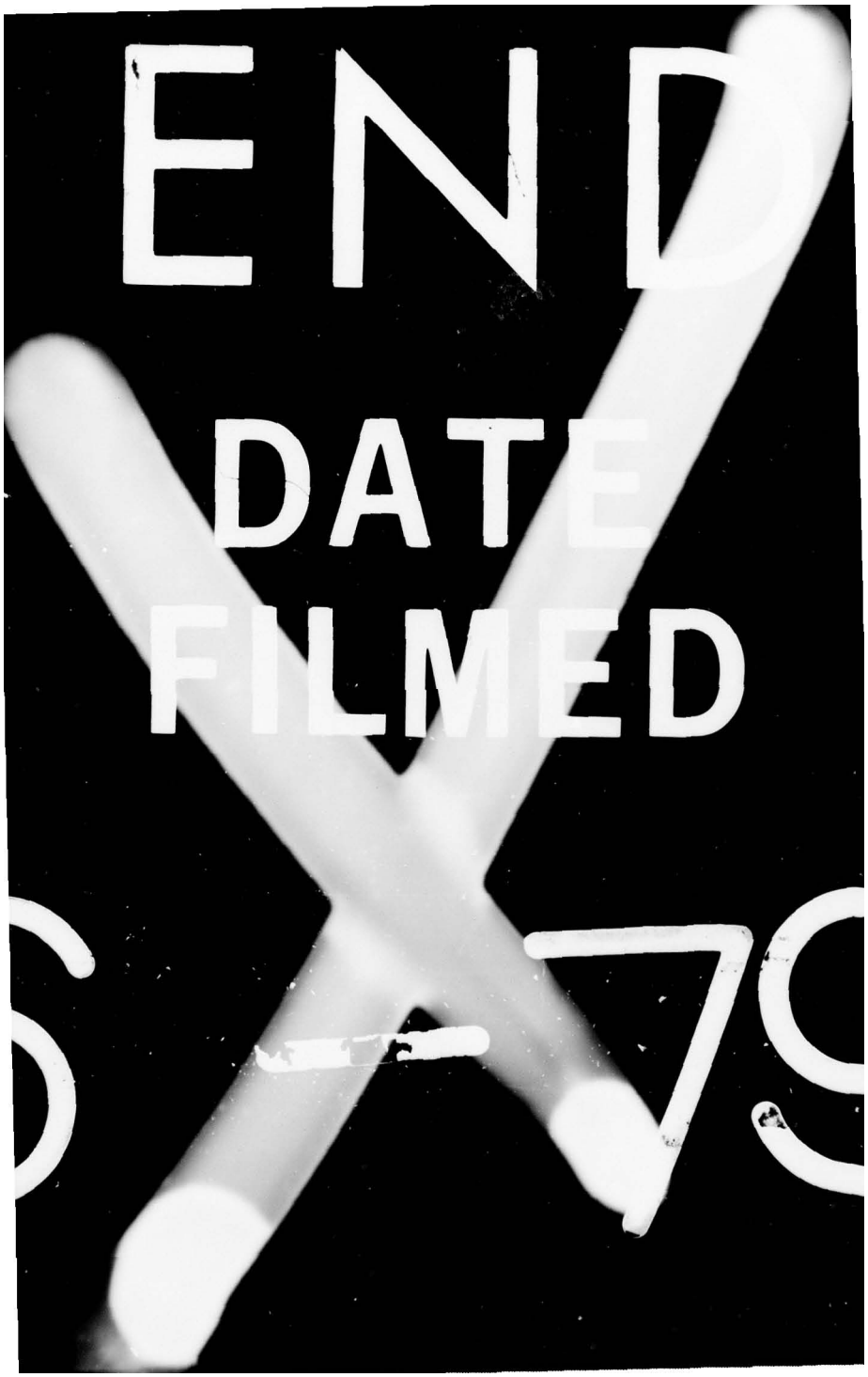
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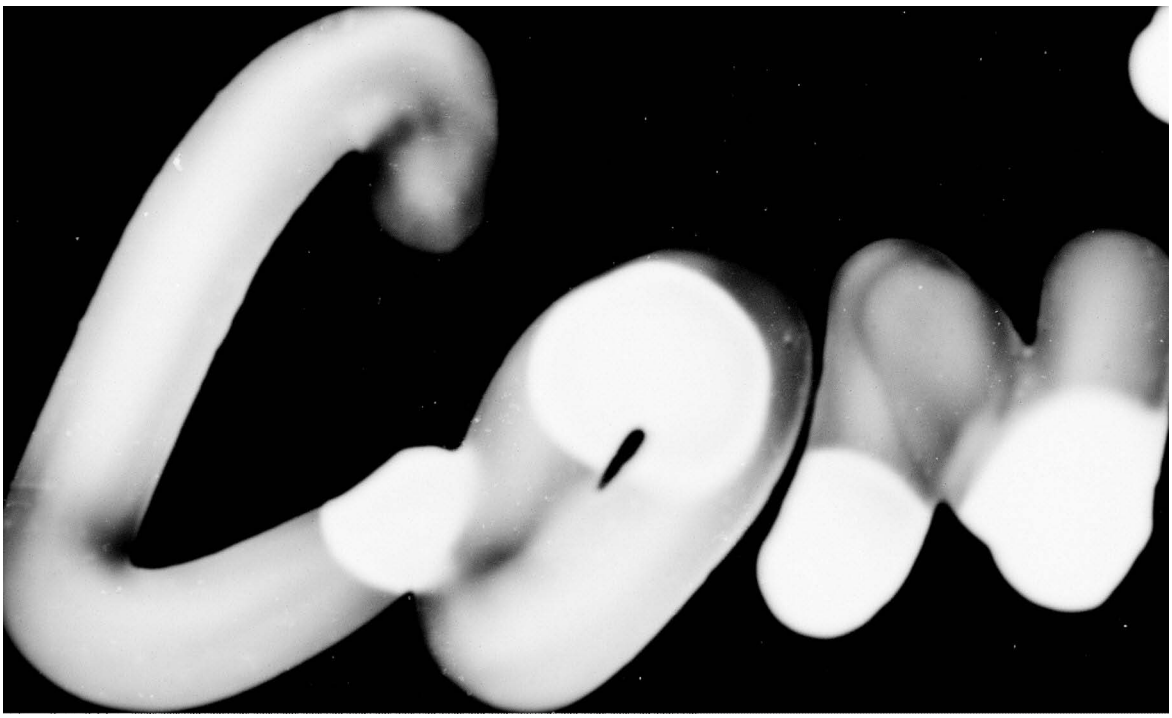

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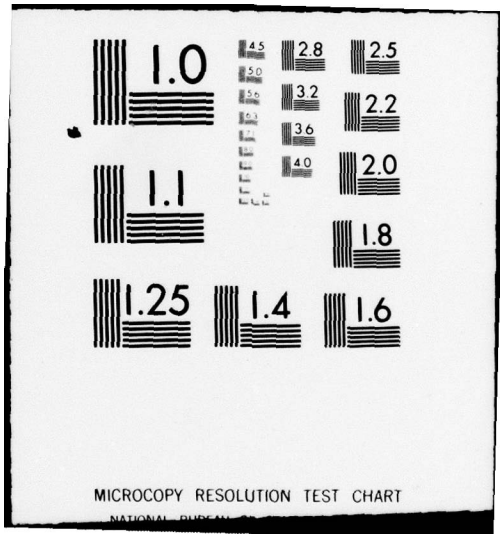
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Dear Sir,

Enclosed are revisions to the publication "Development of a Device for the Incorporation of Multiple Scanivalves into a Computer-Controlled Data System" by Robert Neldon Geopfarth, Naval Postgraduate School Technical Report NPS67-79-002 and M.S. Thesis, March 1979.

Revisions have been made to pages 26, 47, 49 and 50. The enclosed revised pages should be inserted in place of the original pages in your copy, or copies, of this document.

Sincerely,

Raymond P Shreeve

Dr. R. P. Shreeve
Director, Turbopropulsion
Laboratory

sequence of the transfer lines during the transfer of one data byte to the computer. Information is placed on the data lines whenever the DRIVE ENABLE line is true:

$$\text{DRIVE ENABLE} = (\overline{\text{ATN}} \overset{\text{U28(d)}}{\downarrow} \text{ADR}_T \overset{\text{U32(a)}}{\downarrow} \overline{\text{NRFD}}); \text{ LATCHED BY U23(b)}$$

Once this condition exists, Scanivalve address information is unconditionally present on the data lines until cleared by receipt of $\overline{\text{NDAC}}$. An end-of-record (EOR) signal is not provided by this circuit; therefore, the computer must be programmed not to expect or to require one. The driven DAV line is defined as:

$$\text{DAV} = (\text{DAV ENABLE}) \cdot \overset{\text{U31(a)}}{\downarrow} \overline{\text{NRFD}}_{\text{DELAYED}} \cdot (\text{NDAC} \overset{\text{U29(d)}}{\downarrow} \cdot \overline{\text{CLEAR}})$$

When using open-collector bus drivers, a 2 μsec delay is required to allow line ringing and signal transients to decay [2]. The delay was provided by U24, a retriggerable one-shot multi-vibrator, and U23(a), a positive-edge-triggered flip-flop. These components provide a pre-set delay between receipt of $\overline{\text{NRFD}}$ and driving the DAV line "true". Figure 16 describes the time delay sequence. Adjustment of the time delay circuit is described in Section III-E.

6. CLOCK and CLEAR Sections

The CLOCK and CLEAR circuit diagrams are shown in Figure 17. The CLOCK consists of multi-vibrator U8 and crystal Y1. The CLOCK output is a 10MHz sinusoidal signal and is available to the circuit sections shown in Figure 6.

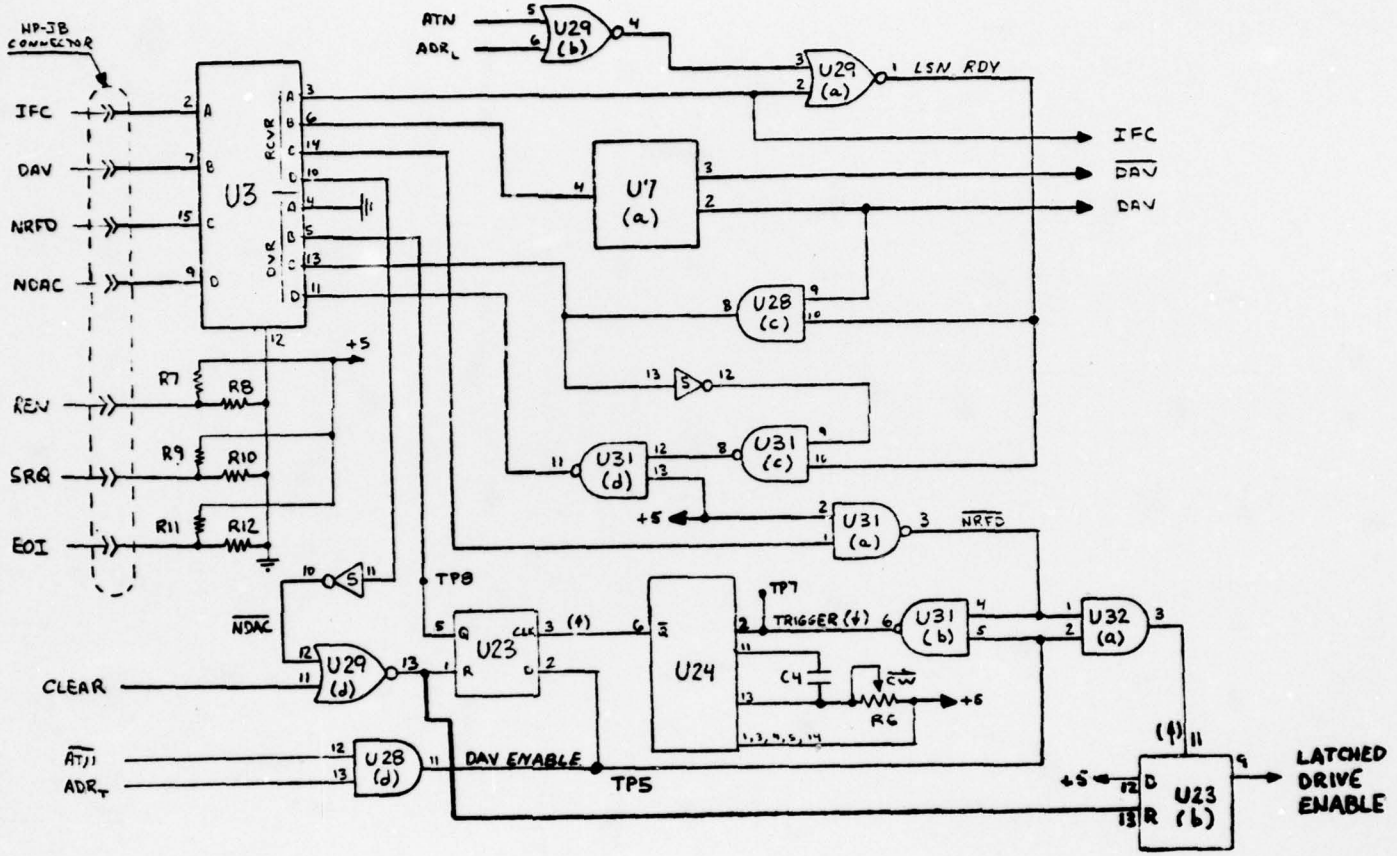
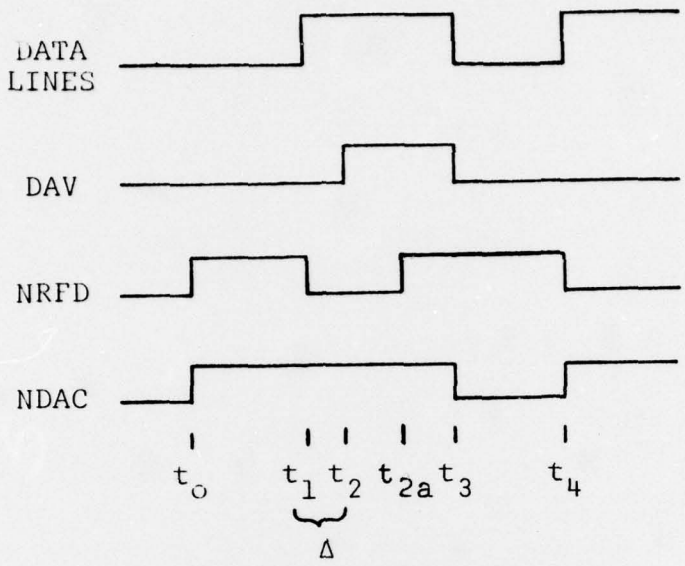


Figure 13

Handshake Section



t_o Device designated a TALKER; computer returns bus to data mode.

t_1 Computer ready for data. Valid data on lines.

t_2 Device indicates data is valid.

t_{2_a} Computer arbitrarily resets NRFD.

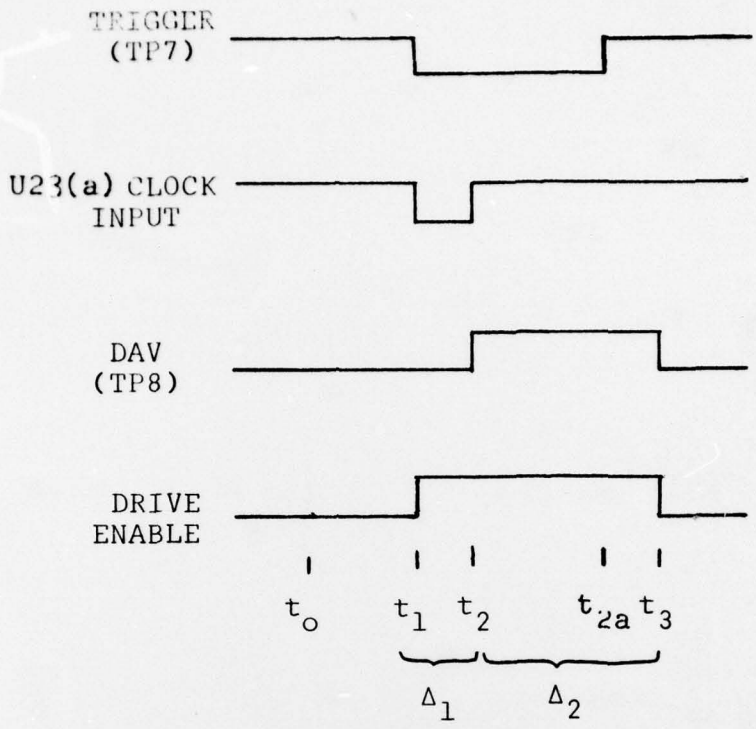
t_3 Computer indicates receipt of data.

t_4 Return to state t_1.

Δ 2 μsec

Figure 15

Talker Timing Diagram



t_o U31(b) and U32(a) enabled.

t_1 $\overline{\text{NRFD}}$ received; U24 triggered, U23(b) Drive enable clocked latching logic true on output line.

t_2 Positive-edged clock pulse latches DAV enable state to DAV driver line.

t_{2a} Trigger reset by receipt of NRFD.

t_3 $\overline{\text{NDAC}}$ received; U23(a) (DAV) and U23(b) (Drive enable) cleared. Data is removed from bus lines.

Δ_1 2 µsec delay; adjustable by resistor R6.

Δ_2 7.2 µsec for HP-9830A.

Figure 16

DAV Time Delay Sequence