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DELTA MODULATION CONFERENCING SYSTEM.(U)
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LERNER TECHNOLOGY, INC.
195 North Long St. Williamsville, N.Y. 14221

DELTA MODULATION CONFERENCING SYSTEM,

FINAL REPORT.

Contract No. N00173-77-C-0216

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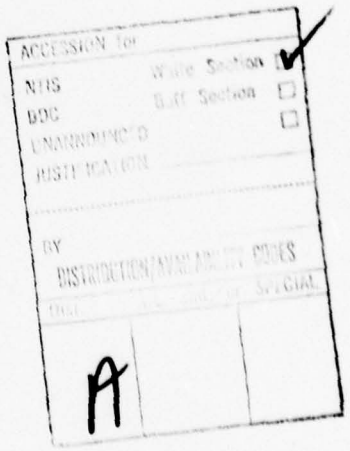


LIST OF ILLUSTRATIONS

1.0 Introduction

This report describes a Delta Modulation Conferencing unit and Delta Modulator-Demodulator units which were constructed under this contract No. N00173-77-C-0216. The conferencing unit is based on a technique for combining a number of delta modulation speech signals into a single bit stream which, in effect, represents the sum of all the input speech signals. Thus any participant can hear all the participants even when a number are speaking at the same time. The system is a relatively simple one in which the processing can be completely digital, and does not involve recovery of the original speech signal. The technique takes advantage of the statistical property of a delta modulation voice signal that adjacent bits differ about 90% of the time and are the same only about 10% of the time.

Section 2.0 presents a description of the principles of operation of the conferencing technique. A review of delta modulation and its characteristics is included. A description of the circuitry in the Delta Modulator-Demodulator units and the Delta Modulation Conferencing unit is presented in Section 3.0.

2.0 Principle of Operation

2.1 Review of Delta Modulation Techniques

This section presents a review of the conventional and adaptive delta modulation techniques.

A block diagram of a conventional delta modulation system is shown in Figure 2-1. The output of the integrator, g(t), is compared against the voice input signal, f(t). If g(t) is less than f(t), a positive pulse is generated by the pulse modulator, and if g(t) is greater than f(t) a negative pulse is generated by the pulse modulator. The integrator integrates these positive and negative pulses to yield a step like signal, g(t), which attempts to follow the input voice signal, f(t), as shown in Figure 2-1. At the receiver the pulses are also integrated, so that the signal g(t) also appears at the output of the receiver integrator. At the receiver, the signal g(t) is passed through a low pass filter to remove frequency components outside the desired band. The sequence of bipolar pulses is normally PSK modulated onto a carrier for transmission over the communication link.

In Figure 2-1, it is seen that the signal g(t) differs from the analog input signal in two important ways. First, the signal g(t) tracks f(t) in discrete steps, which, despite low pass filtering at the receiver, leads to quantization noise in the output signal.

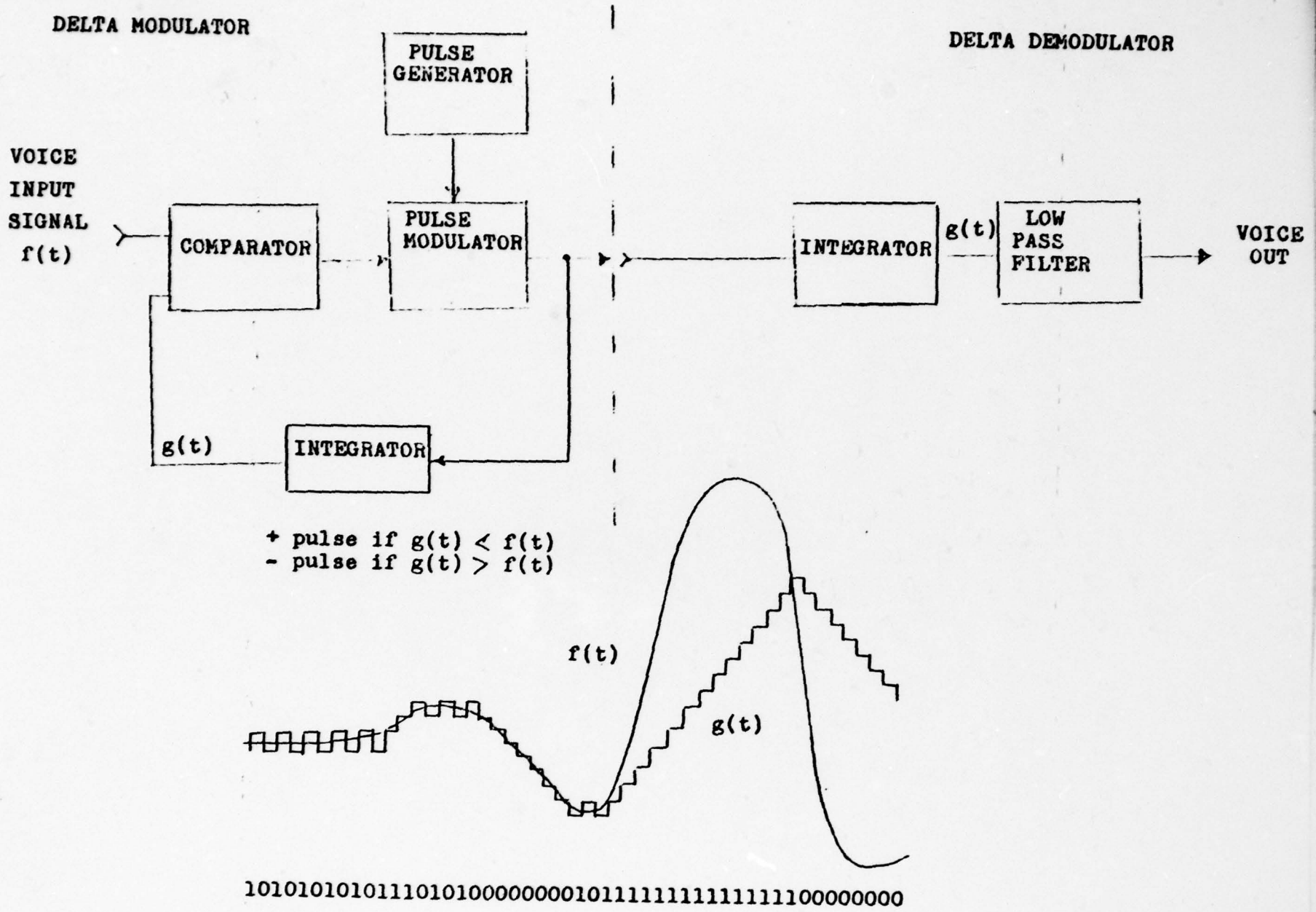


Figure 2-1 Conventional Delta Modulation System

Secondly, when f(t) changes rapidly, the signal g(t) cannot follow and the detail is lost. This condition is known as slope overload. If the step size of g(t) is decreased to reduce quantization noise, then g(t) will be less capable of following rapid changes. If step size is increased to permit g(t) to follow rapid changes, the quantization noise will increase. The step size in conventional delta modulation systems is adjusted as a compomise between these two factors.

Adaptive delta modulation (ADM) is a technique in which the step size adjusts automatically in accordance with the slope requirements. A block diagram of a relatively simple adaptive delta modulation system is shown in Figure 2-2, and associated waveforms are shown in Fig. 2-3. The system stores the previously transmitted symbol, δ, and compares it with the present output. If the symbols are alike, the step size is increased one increment; if the successive symbols do not match, the step size is decreased one increment. The output of the sequence detector is fed to an integrator, which generates a multiplying constant, K. Long alternating sequences into the integrator reduce K to a minimum such that the step size is the smallest increment. Long constant sequences into the integrator increase K to a maximum such that the step size is the largest increment. The polarity of the step is

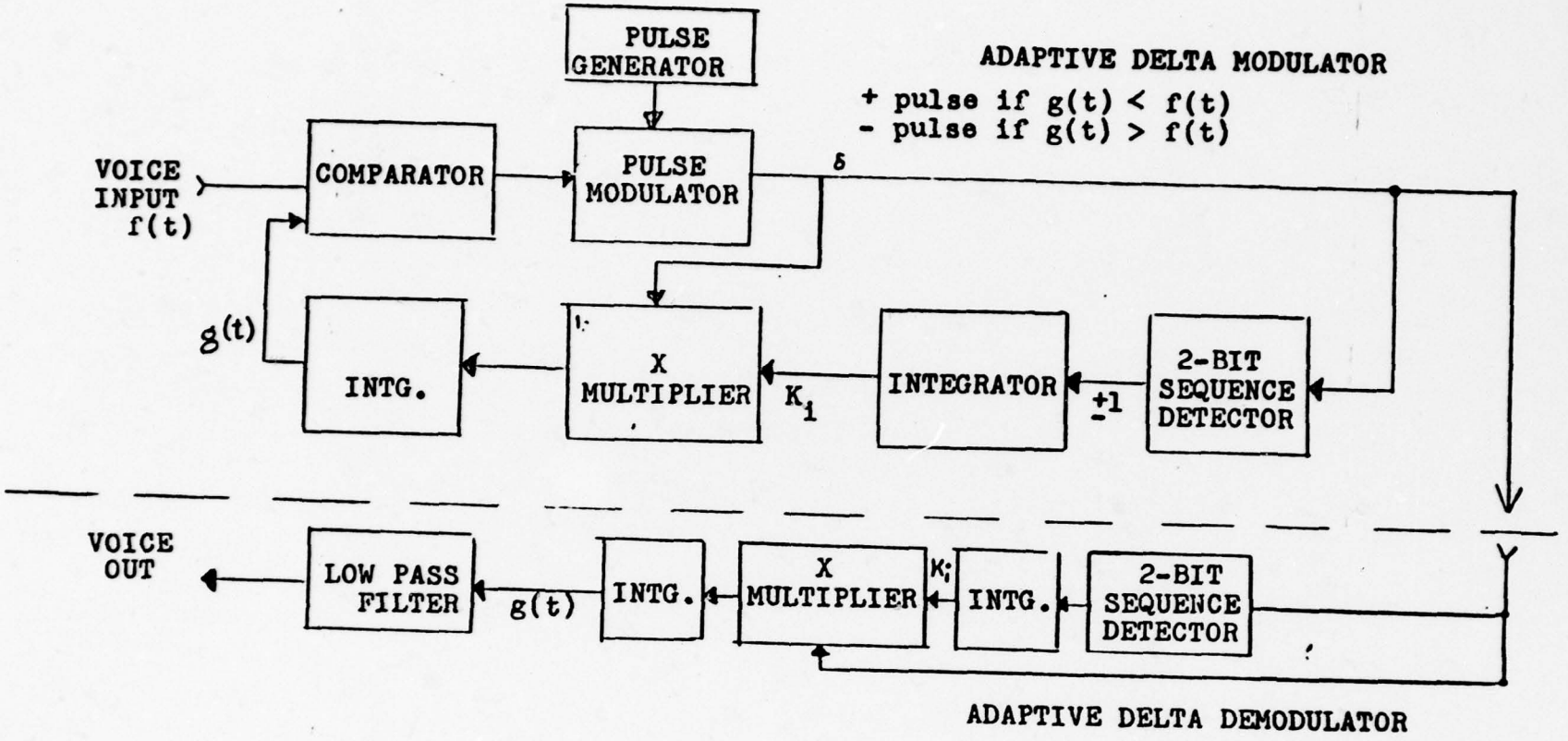
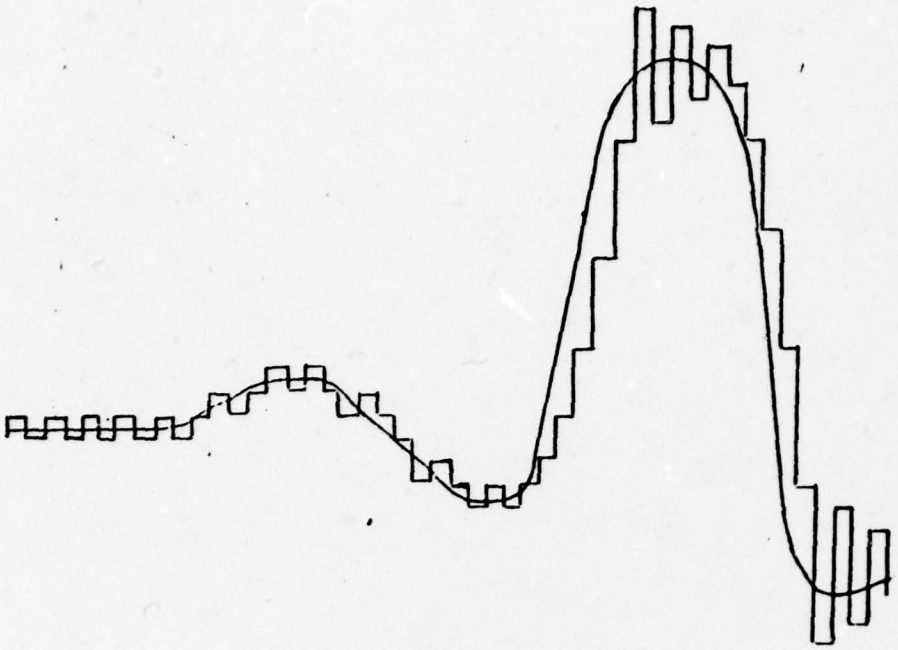


Figure 2-2 Adaptive Delta Modulation System



10101010101101101001000100101111111010100000001010

Figure 2-3 Waveform for Adaptive Delta Modulation

determined by the present output symbol. The steps from the multiplier are integrated to form g(t), the predicted signal. At the receiver, a sequence detector, integrator, multiplier, and second integrator are used to reconstruct the predicted signal, g(t). This signal, g(t), is fed through a low pass filter and provided as the voice output. Other more complex adaptation techniques have been developed, but the principle is similar to that used in the system described. In general, in ADM systems of this type, the step size adaptation can be considered as a variable multiplier operating on the step size with the actual multiplier constant being dependent on the past history of the transmitted signal.

2.2 Encoding Delta Modulation Signal Into Ternary Alphabet

In order to understand the principle of operation of the conferencing system, it is useful to consider the delta modulation signal represented as a ternary sequence rather than a binary sequence. The method for converting the binary sequence from the delta modulator into a ternary sequence is illustrated in Figure 2-4. As shown, a ternary symbol (0, +1, or -1) is generated for each binary symbol in accordance with the following rule: the current binary symbol is compared with the previous symbol; if the two symbols are different a 0 is generated; if the two symbols are 1's a +1 is generated; if the two symbols are 0's a -1 is generated.

Using these rules, the ternary sequence shown in the illustration can easily be derived from the binary sequence. It is also evident, that, if desired, the binary sequence can be derived from the ternary sequence.

Let the ternary sequence be represented electrically in the following way: +1 is represented by a positive voltage pulse; -1 is represented by a negative voltage pulse; 0 is represented by a zero voltage. Now consider the output from a delta demodulation integrator if a ternary sequence is applied, and compare it with the output if the corresponding binary sequence is applied.

TO CONVERT BINARY DELTA MODULATION SIGNAL TO
TERNARY DELTA MODULATION SIGNAL

IF SUCCESSIVE SYMBOLS ARE:

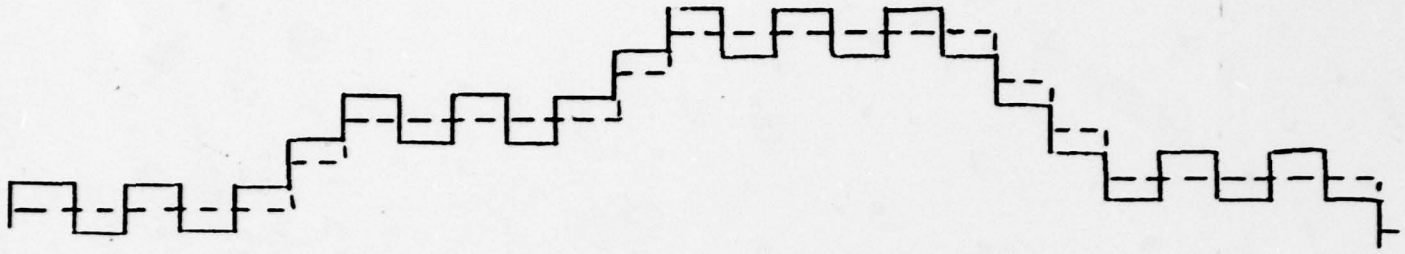
DIFFERENT (01 OR 10) ——→ 0
TWO 1's (11) ——→ +1
TWO 0's (00) ——→ -1

BINARY SEQUENCE	1	0	1	0	1	1	1	0	1	0	1	1	1	0	1	0	1	0	0	0	0	1	0	1	0	0
TERNARY SEQUENCE		0	0	0	0	+1	+1	0	0	0	0	+1	+1	0	0	0	0	0	-1	-1	-1	0	0	0	0	-1

Figure 2-4 Conversion of Binary Sequence to Ternary Sequence

A little thought will show that the two outputs are essentially the same. The only difference is the alternating increase and decrease in voltage for a conventional binary signal when there is no net change in output voltage. These alternations would normally be filtered by the low pass filter following the delta modulator. These ideas are illustrated in Figure 2-5 for the binary and ternary sequence shown in Figure 2-4. It is also evident that the ternary sequence can be used in an adaptive delta demodulator in a way similar to that for a conventional binary sequence; the $\pm$ 1's will increase the step size; the 0's will decrease the step size.

These ideas have been verified experimentally by alternately applying a binary and ternary signal to a delta demodulator. The outputs resulting from the two input signals were indistinguishable.



BINARY SEQUENCE	1	0	1	0	1	1	1	0	1	0	1	1	1	0	1	0	1	0	0	0	0	1	0	1	0	0
TERNARY SEQUENCE	0	0	0	0	+1	+1	0	0	0	0	+1	+1	0	0	0	0	0	-1	-1	-1	0	0	0	0	-1	

Output from Binary Sequence Shown Solid

Output from Ternary Sequence Shown Dotted

Figure 2-5 Output Signals from Binary and Ternary Delta Modulation Signal Input

2.3 Statistics of Delta Modulation Voice Signal

A speech signal has the property that most of the time there is silence. This results from pauses between phrases, words, and phonemes. Even when there is activity this activity is more often low level than high level. In a conventional binary delta modulation signal the periods of silence are represented by alternating 0's and 1's. Similarly signal periods in which there are small changes in voltage have occasional sequences of identical symbols to represent the changes but are represented primarily by alternating 0's and 1's. It is evident, therefore, that alternating 0's and 1's will be more probable than identical symbol pairs. Tests have been conducted on both conventional and adaptive delta modulation systems with normal two way conversations to determine the relative frequency of alternating symbol pairs and identical symbol pairs. It was found that alternating symbol pairs occurred about 90% of the time, and identical symbol pairs occurred about 10% of the time. Equivalently, in the ternary system, 0's occurred about 90% of the time, and $\pm$ 1's occurred about 10% of the time.

2.4 A Conferencing Technique Based On A Ternary Representation

It is evident that if two ternary delta modulation voice signals on separate wires are connected to a common integrator, the output will be the sum of the two voice signals. The two signals can be combined on a common wire, except for the problem that arises when a +1 (or -1) occurs at the same time in both signal streams. When this occurs, the sum signal should be +2 (or -2), but since a ternary alphabet is to be used, it must be represented by a +1 (or -1). Since, however $\pm$ 1's occur only about 10% of the time, the probability that they will occur in two streams at the same time is only about 1%. Thus, since the effect on performance of a simultaneous occurrence is small, and the probability of such occurrence is small the overall effect is negligible.

It is seen, therefore, that two or more ternary delta modulation voice signals can be combined into a single ternary signal which, when fed to a delta demodulator, will yield an output signal which is the composite of all the input signals.

As has been pointed out in Section 2.2, a ternary delta mod signal can be converted back to a binary delta mod signal. A problem can arise, however, when the ternary signal has been derived from two or more binary delta mod signals. This problem is illustrated by considering the situation where a +1 is immediately followed by a -1, as shown in Figure 2-6. (This situation cannot arise

if the ternary signal derived from a single binary delta mod signal.)

Original Delta Mod Signal #1	0 1 0 1 0 1 1 0 1 0
Original Delta Mod Signal #2	0 1 0 1 0 1 0 0 1 0
Ternary Signal #1	0 0 0 0 0+1 0 0 0
Ternary Signal #2	0 0 0 0 0 0-1 0 0
Composite Ternary Signal	0 0 0 0 0+1-1 0 0
Proposed Compromise Composite Binary Signal	0 1 0 1 0 1 0 0 1 0

Figure 2-6 Adjacent +1 and -1

A little thought will show that we cannot recover both the pair of 1's and the pair of 0's from the original signals in the original locations. Some compromise is needed, and the one chosen and illustrated in Figure 2-6 is to give priority to the last occurring event. As shown, the -1 is represented, but not the +1. Because of the statistics of the delta mod signals, these occurrances are rare, and should not seriously affect the performance of the system.

2.5 A Conferencing Technique Based On A Binary Representation

The discussion heretofore has been based on the use of ternary signals as an intermediate step. Since, however, the information for generating the ternary signals is contained in the original binary signals, the output binary stream can be derived directly from the input binary streams. An algorithm for doing so is presented below:

> For each of the input binary streams observe the current symbol and preceding symbol.
>
> If for each of the input binary streams the current symbol differs from the preceding symbol, make the current output symbol differ from the preceding output symbol.
>
> If for one or more of the input binary streams the current symbol and the preceding symbol are both 1's, make the current output symbol and the preceding output symbol 1's. If for one or more of the input binary streams the current symbol and the preceding symbol are both 0's, make the current output symbol and the preceding output symbol 0's.
>
> If for some of the input binary streams the current symbol and the preceding symbol are both 0's, and for other input binary streams, the current symbol and the preceding symbol are both 1's, make the current and preceding output symbols correspond to the majority. If there are an equal number with pairs of 0's and pairs of 1's, make the current output symbol differ from the preceding output symbol.

The algorithm can be stated more simply as follows:

For all of the input delta modulation bit streams observe the current bits and preceding bits.

If there are an equal number of 1's and 0's make the current output differ from the preceding output bit.

If there are more 1's than 0's make the current output bit and the preceding output bit 1's.

If there are more 0's than 1's make the current output bit and the preceding output bit 0's.

Two examples illustrating the algorithm are shown in Figure 2-7. As shown, when only one chanel is active, the output signal duplicates the active chanel; when two channels are active the output signal is a composite.

Three Input Signals	10101010101010101010101010101010
One Channel Active	01010101010101010101010101010101
	01010110101110100010101001010101
Output Signal	01010110101110100010101001010101
Three Input Signals	10100101010010101010100100010101 0
Two Channels Active	01010101010101010101010101010101 0
	01010110101010010010101011010110 1
Output Signal	01000110100010010010100100010110 1

Figure 2-7 Examples of Conferencing Signals

3.0 Circuit Description

3.1 Delta Modulator - Demodulator Unit

The delta modulator and demodulator are contained in a single unit. Power and clock signals for the unit are generated in the Conferencing unit and are supplied over a cable. The Delta Modulator-Demodulator units have been designed to operate with sound powered phones which have been modified to provide four wire operation. A suitable jack is provided for the phone. In addition separate jacks are provided to permit the unit to be driven from a tape recorder, and for the output of the unit to drive a speaker or tape recorder.

3.1.1 Delta Modulator

Figure 3-1 is a schematic diagram of the delta modulator. The circuit is on a single card in the Delta Modulator-Demodulator unit.

The dual operational amplifier A-1 serves as a high gain amplifier and low pass filter. The low pass filter is designed to provide a 3 db cut off at 3.0 KHz. The resistor shown in dotted lines at the input to the operational amplifier is not mounted on the card, but at the input jack. It provides lower gain to permit a tape recorder to drive the unit with normal gain settings on the tape recorder.

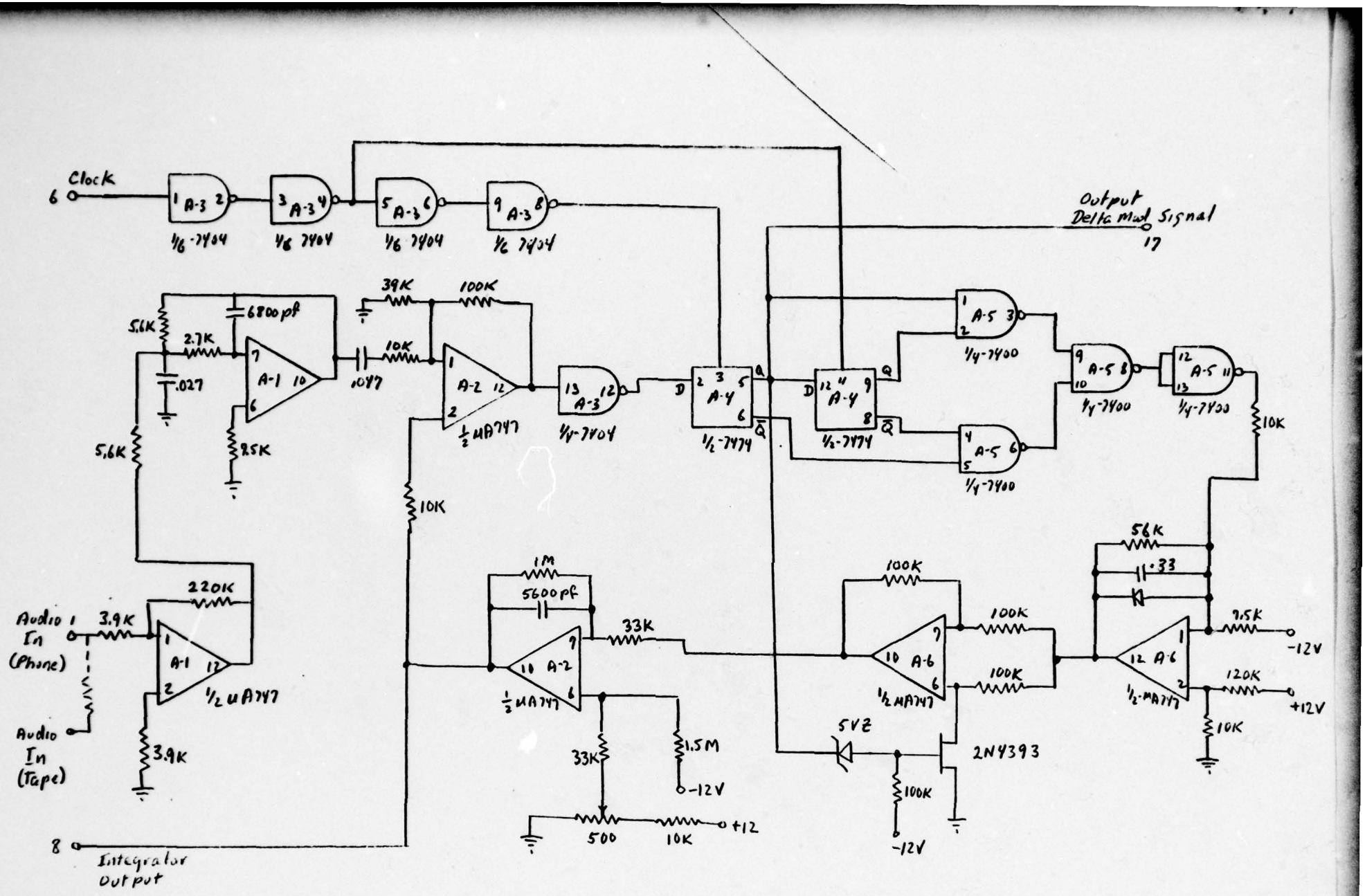


Figure 3-1 Delta Modulator

One half of the dual operational amplifier, A-2, is used as the delta modulation integrator. The other half together with one section of a 7404 hex inverter is used as a comparator; it puts out a 0 if the input signal is less than the output from the delta modulation integrator and a 1 if it is greater.

The dual flip-flop, A-4 serves as a shift register to permit a comparison between the current bit and the previous bit for adaptation purposes. As shown, the clock signal to the first flip-flop is delayed with respect to that for the second flip-flop to insure proper shift register operation.

The 7400, A-5 is connected as an exclusive - or. When the current bit and the previous bit are the same the output is a 0; when the two bits differ the output is a 1.

The first half of the dual operational amplifier A-6 integrates the output from the exclusive -or circuit. When there are 0's at the input to the integrator (i.e. when there is a sequence with bits the same in the delta mod signals) the output will go positive. When 1's are fed to the integrator, the output is driven in a negative direction. The diode shown prevents the output from going any more negative than about +200mv as controlled by the bias on the operational amplifier.

The second half of the dual operational amplifier A-6 provides an output signal whose magnitude is the same as the input, but the polarity of which is capable of being reversed in accordance with the current bit of the delta modulation signal. The polarity reversal is accomplished by the FET connected to the non-inverting input of the operational amplifier. When a 1 occurs theFET shorts the non-inverting input leading to a polarity reversal at the output. When a 0 occurs the FET is an open circuit, and since the gain through the non-inverting input is 2 compared to a gain of -1 through the inverting input, there is a net gain of 1. The polarity at the output is therefore not reversed.

This signal, whose polarity reflects the current bit of the delta modulation signal, and whose magnitude is a function of the number of times bit pairs have been the same, drives the delta modulation integrator, A-2. As shown a balance potentiometer is provided for a bias adjustment. This potentiometer is adjusted to give a steady stream of alternate 1's and 0's in the absence of an input signal.

3.1.2 Delta Demodulator

Figure 3-2 is a schematic diagram of the delta demodulator. This circuit is on a single card in the Delta Modulator-Demodulator unit.

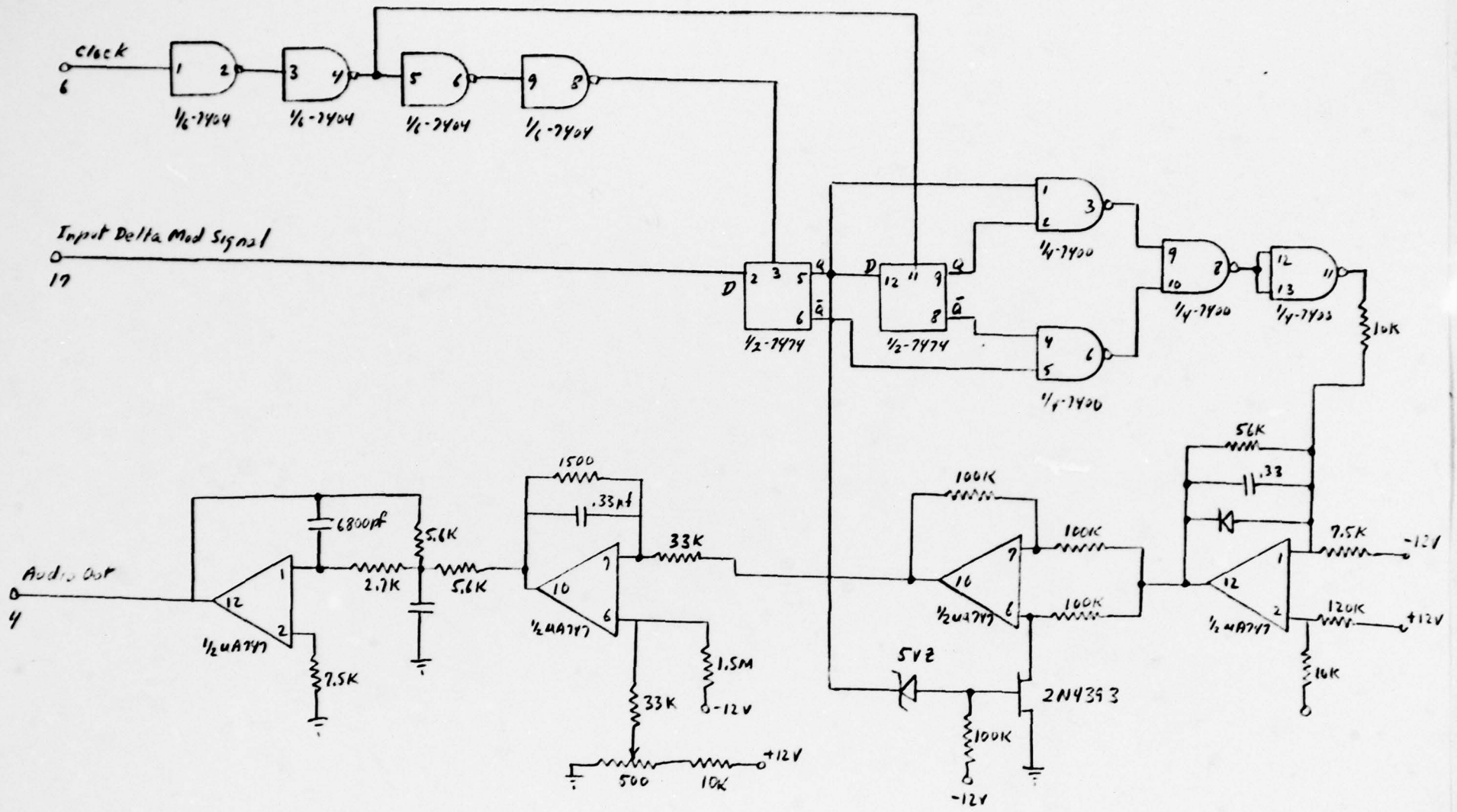


Figure 3-2 Delta Demodulator

The adaptation circuitry in the demodulator is identical to that in the modulator. As shown, a low pass filter with a 3 db cut-off at about 3.0 KHz. is provided for the audio output signal.

3.2 Conferencing Unit

The conferencing unit contains a single card on which is mounted the conferencing circuit and clock generator. Power supplies for the conferencing circuitry as well as the Delta Modulator-Demodulator units are also contained in the conferencing unit.

A schematic diagram of the conferencing circuit and the clock signal generator is shown in Figure 3-3. Detailed schematics and descriptive material concerning the sign and magnitude generating part of the circuit and the logic circuitry are given in Figures 3-4 and 3-5.

Each of the input delta mod signals is fed to a section of a 7474 flip-flop which serves as a shift register stage. This makes available for each delta mod signal the current bit and previous bit. When all three delta mod signals are connected the jumpers shown dotted between pins 3 and 6, pins 4 and 6, and pins 5 and 6 are connected. These jumpers are in the connectors from the Delta Modulator-Demodulator units, and are connected when the associated Delta Modulator-Demodulator

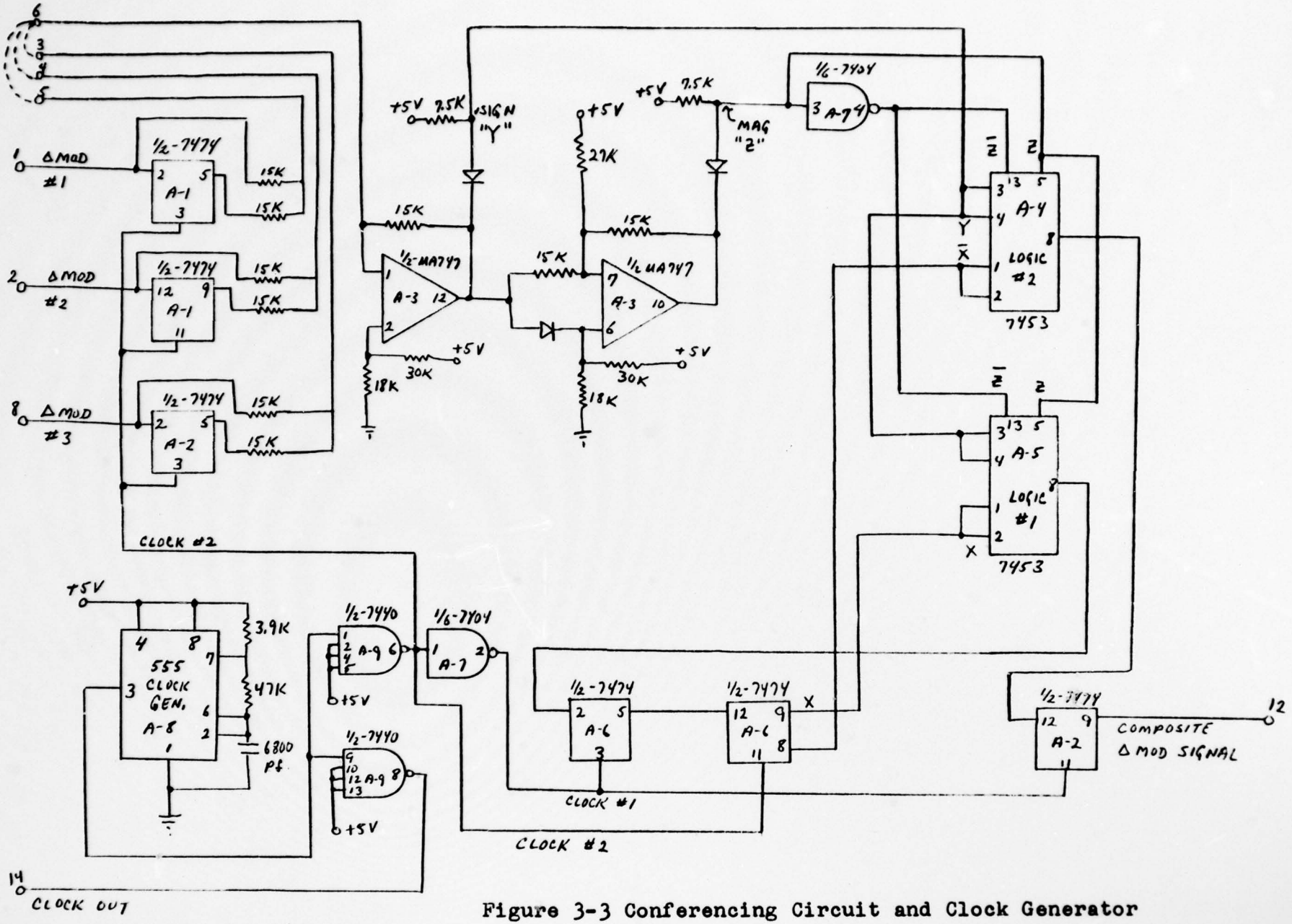
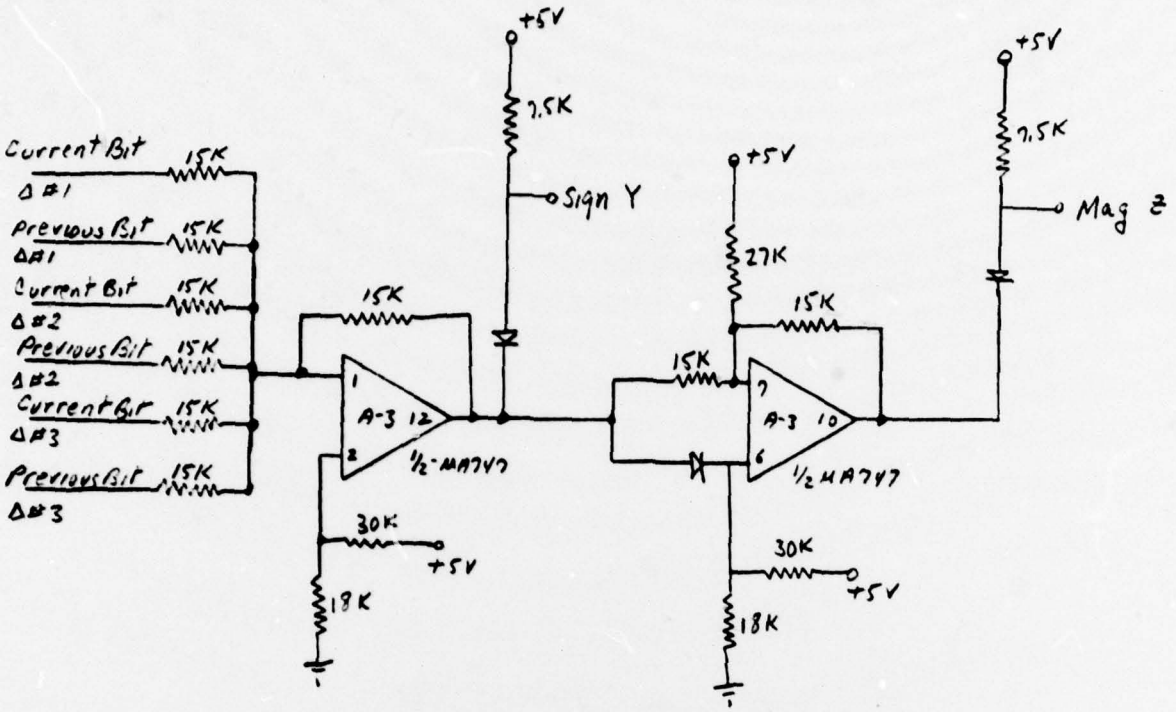


Figure 3-3 Conferencing Circuit and Clock Generator

unit is connected. Thus for each Delta Modulator-Demodulator unit that is connected the voltage for the current bit and the previous bit are summed in the first operational amplifier of the pair A-3.

The operational amplifier A-3 is connected to generate two logic signals which are called respectively "sign" (Y) and "magnitude" (Z). The details are shown in figure 3-4. As shown, the "magnitude" (Z) and "sign" (Y) are functions of the current and previous bits for each of the delta mod signals that are connected. If there are more 1's than 0's at the input, the sign signal is 0; if there are more 0's than 1's the sign signal is 1; if there are an equal number of 0's and 1's the magnitude signal is 0; if there are more 1's than 0's or 0's than 1's the magnitude signal is 1.

The sign and magnitude logic signals are fed to a pair of logic circuits along with a signal, X, which represents a temporary estimate of the output bit. The signal, X (& and $\bar{X}$) is obtained from the shift register A-6. The details of the logic circuits are shown in Figure 3-5. Logic circuit #1 outputs a bit which is opposite to the previous estimate bit, X, if the magnitude signal Z, is a 0. (This is the situation that exists when there are an equal number of 0's and 1's at the input to the sign and magnitude circuit.) Logic circuit #1 outputs a bit which is the same as the sign signal, Y, if the magnitude signal, Z, is 1. (This is the situation that exists



If there are an equal number of 0's and 1's at input Sign = ? Mag = 0
If there are more 1's than 0's at input Sign = 0 Mag = 1
If there are more 0's than 1's at input Sign = 1 Mag = 1

Note: In delta modulation polarity doesn't matter, so the fact that sign is opposite input majority doesn't matter.

Figure 3-4 Sign and Magnitude Circuit

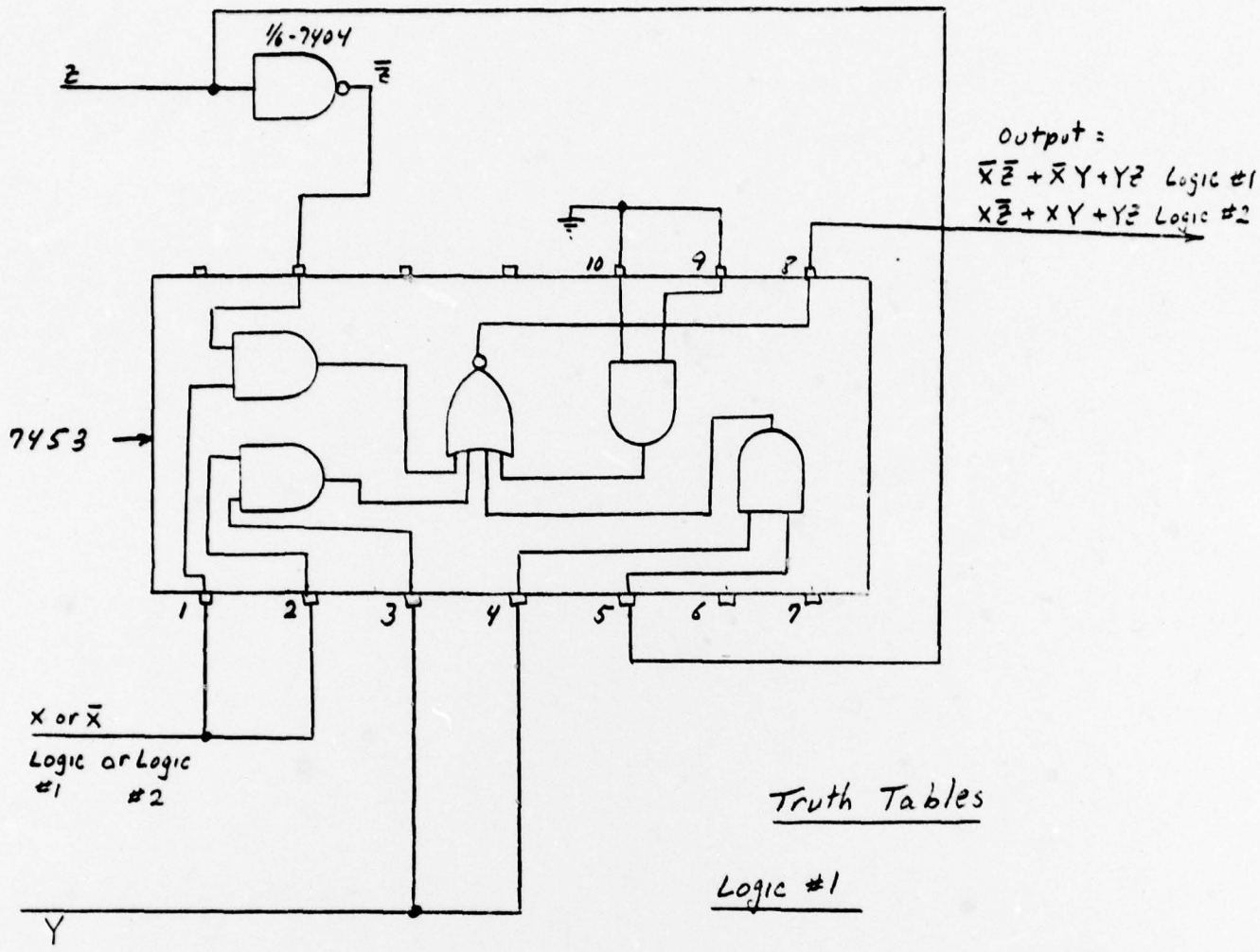


Figure 3-5 Logic Circuit

Truth Tables

Logic #1

Prev. Bit	Sign	Mag.	Output
X	Y	Z	
0	?	0	1
1	?	0	0
?	0	1	0
?	1	1	1

Logic #2

Prev Bit	Sign	Mag	Output
X	Y	Z	
0	?	0	0
1	?	0	1
?	0	1	0
?	1	1	1

when there are more 1's than 0's or more 0's than 1's at the input to the sign and magnitde circuit.)

The output from logic circuit #1 is a temporary estimate of the output bit. The output from logic circuit #2 is the final output composite delta mod signal. The output from logic circuit #2 is the same as the previous estimate, X , if the magnitude signal, Z , is a 0. The output from logic circuit #2 is the same as the sign signal, Y , if the magnitude signal, Z , is a 1.

3.3 System Cabling

Figure 3-6 shows the cabling between the conferencing unit and the three Delta Modulator-Demodulator units. It also shows the connections to the circuit boards. In the case of the Delta Modulator-Demodulator unit an "M" subscript refers to a connection to the modulator board; a "D" refers to a connection to the demodulator board; where no subscript appears the connection is to both boards.

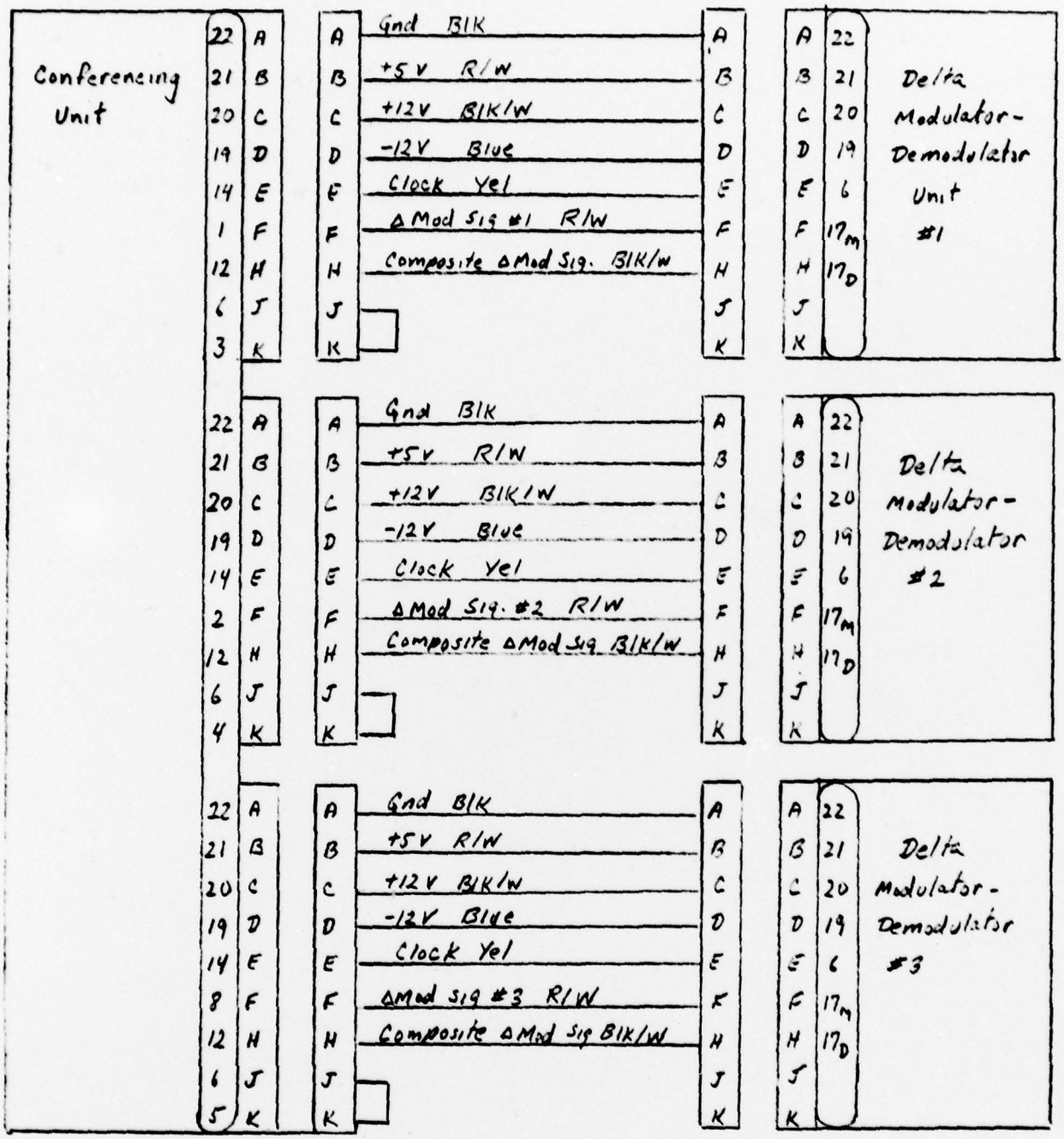


Figure 3-6 Cabling Diagram