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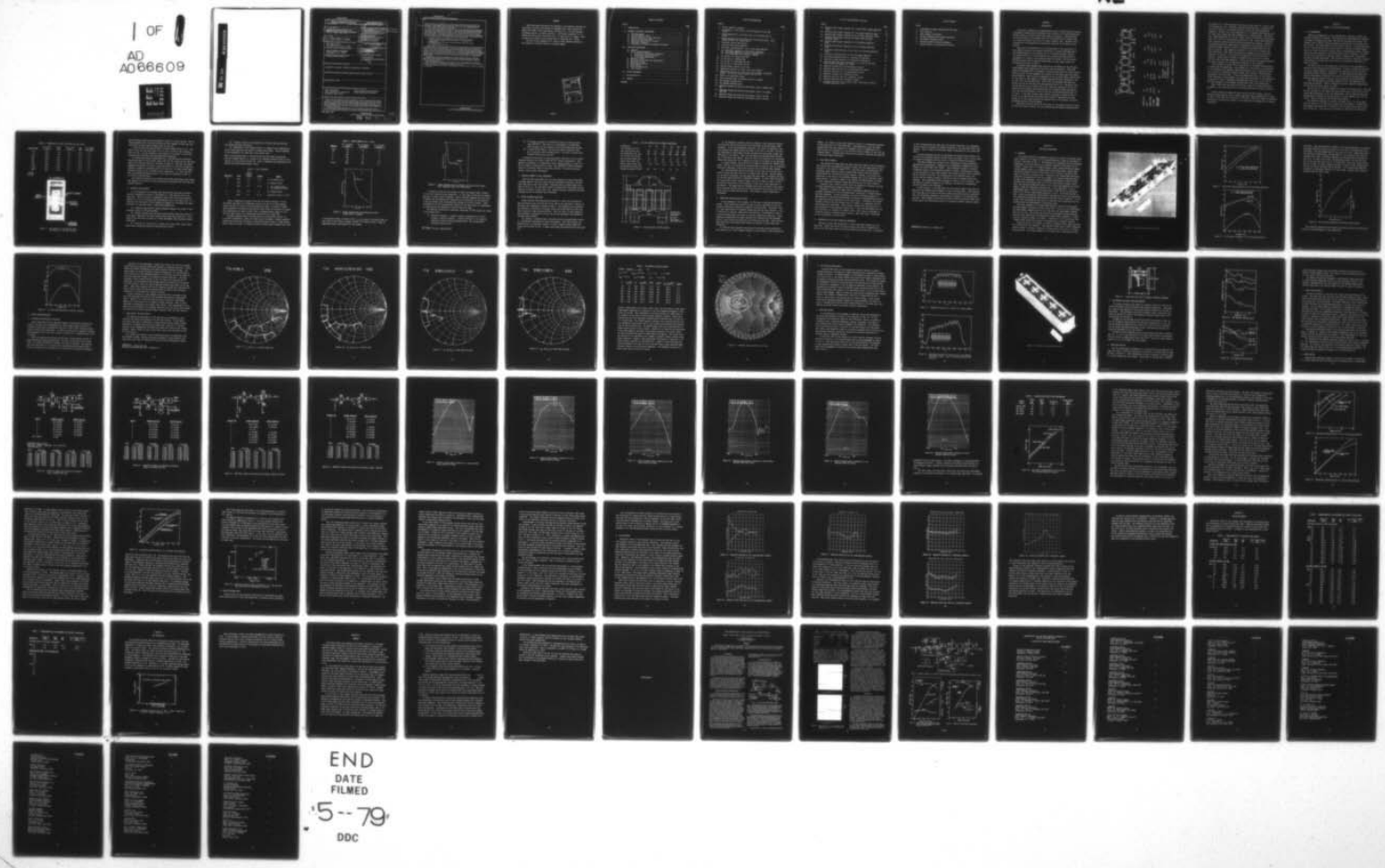

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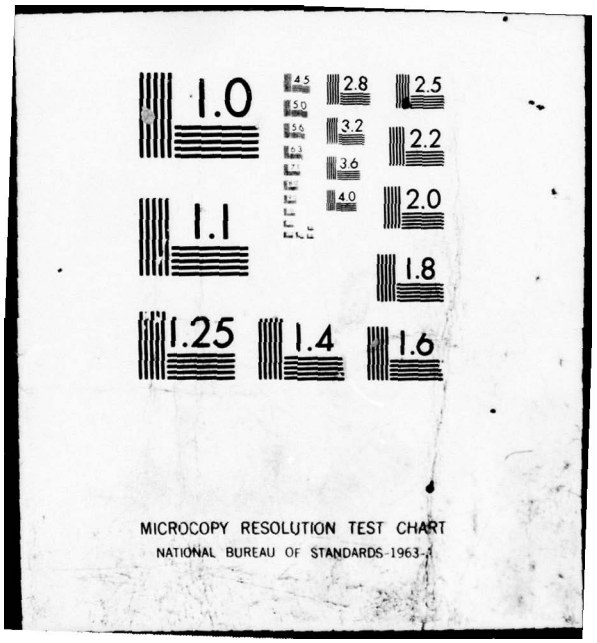
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This final report summarizes the results achieved in a 21-month research program (including a 3-month no-cost extension) to develop an amplifier module suited to airborne active array radar applications. During the course of this program, advances have been made in the areas of GaAs substrate preparation, design of new FET types having improved performance, fabrication of amplifiers having greater than 1-W output over the 9- to 10-GHz frequency range, and development of pulsed phase characterization techniques which demonstrate the suitability of power FET amplifiers for a pulsed phased array.

RCA now has three $AsH_3/Ga/HCl/H_2$ (hydride) and one $AsCl_3/Ga/H_2$ (trichloride) reactors. These reactors have been used extensively in a program to develop improved buffer layers on GaAs

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substrates suitable for FET fabrication. Cr-doped buffer layers have been developed with excellent surface morphology, voltage breakdowns in excess of 1500 V and resistivities of about 10^7 ohm-cm. Undoped buffer layers have been grown using the two-buffer $AsCl_3$ system, and resistivities of about 10^4 ohm-cm have been achieved.

In the course of this program, new power FET types have been developed which achieve greater power levels than had previously been available. A unit having eight parallel gates, designated as an 8G type, has achieved a power of 854 mW at 10 GHz with over 28% power-added efficiency. Two 8G units connected in parallel on the same carrier have achieved greater than 1.3 W. Power levels greater than 1 W have also been achieved in a single device by a 16G and an 18G design. At lower frequencies, a 32G design has achieved 1.8 W at 8 GHz and a large 48G FET has demonstrated over 4 W of output at 4 GHz. This improved performance is also the result of developments during the course of this program in the following areas of device fabrication:

- An innovative continuous gate geometry utilized in the 8G and 18G devices.
- A Ti/Pt/Au refractory metallization system results in a considerably more reliable device.
- An Ni/AuGe/Ni sintered ohmic contact technology permits good quality source and drain contacts.
- A new automatic flip-chip system.

Balanced amplifier stages have been fabricated which can be cascaded to form a four-stage amplifier having greater than 1-W output power. The lowest level stage utilizes Dexcel 3501 FETs to generate 83 mW, a 4G stage generates 398 mW, an 8G stage generates 589 mW and a 16G stage generates 1.55 W, all at 9.5 GHz. The first three stages have been cascaded in a single package to achieve an output of 590 mW with an associated gain of 15.7 dB. A separately packaged fourth stage developed toward the end of the program has been cascaded with the three-stage module resulting in an amplifier having an output of 1.38 W at 19.4-dB gain and 10.1% efficiency. The response of this four-stage amplifier falls off 1.25 dB over the 9- to 10-GHz band so that greater than 1 W is obtained over this full band.

The phase characteristics of pulsed-gate GaAs FET power amplifiers have been extensively characterized using a phase bridge developed with standard waveguide components. It has been found that the phase characteristics of FETs are superior to miniature traveling-wave tubes used in phased array applications.

Six 8G FETs have been subjected to dc-biased life test at an effective channel temperature of 250°C. The MTTF has been determined to be 2000 hours under these conditions. This is equivalent to an MTTF of 10^6 hours at a normal operating temperature of 130°C.

Fifty-five power FETs of the 4G, 8G, and 16G varieties have been delivered to NRL for evaluation by the customer.

PREFACE

This Final Report describes the progress of the research performed for the period 1 October 1976 through 30 September 1978, under Contract No. N00173-76-C-0383 at RCA Laboratories, Princeton, N.J., in the Microwave Technology Center, F. Sterzer, Director. The Project Supervisor is S. Y. Narayan and the Project Scientists are R. L. Ernst and H. C. Huang. Other personnel who worked on this program were A. Mikelsons and P. Pelka.

The Navy Project Engineer is E. Cohen of Naval Research Laboratory. This program is funded by Naval Air Systems Command.

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SECTION I

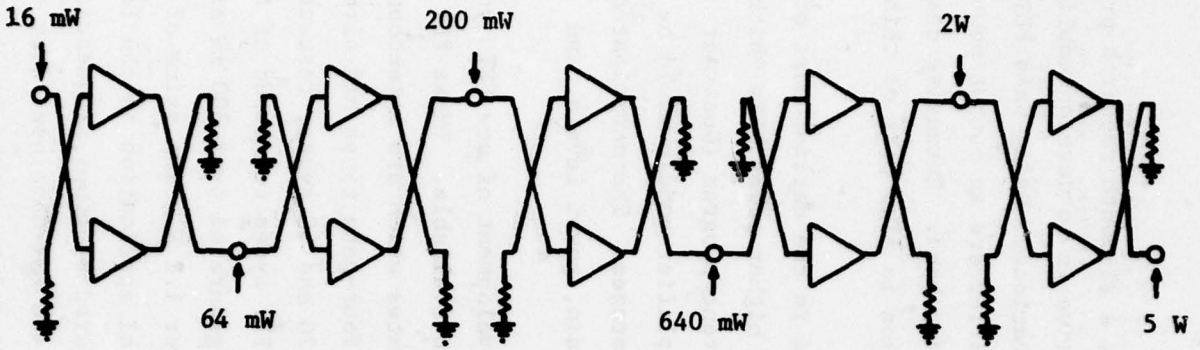
INTRODUCTION

This report summarizes the progress made during a 21-month research program (including a 3-month no-cost extension) whose objective is to develop amplifier modules suited to airborne active array radar applications. Using GaAs FETs as the active device, the design goals for the amplifier are an output power of 5 W with 25-dB gain over the 9- to 10-GHz frequency band. Extensive characterization of FET amplifiers during pulsed operation is also part of this program.

Based upon the performance of devices developed in the earlier part of this program, and upon the predicted performance of higher power FETs which were being designed in this program and in a concurrent program (Contract No. F33615-76-C-1144), it was projected that the amplifier module would be configured as a cascade of five balanced amplifier stages. The anticipated FET device types and the stage-by-stage budget of gain, power levels, and efficiencies are shown in Fig. 1.

To satisfy these program goals required the development of new FET types having higher power outputs than previously had been available. These FET types are distinguished by the number of parallel gates which are interconnected. Before the start of this program, the two-gate and four-gate types had already been developed. These units are designated as the 2G and 4G types, respectively. In the course of this program, the newly developed FET types consisted of the 8G, 16G, 18G, 32G, and 48G units. The 8G unit has generated over 800 mW at 10 GHz, and the 16G and 18G units have generated over 1.2 W. The gains of the 32G and 48G units are currently too low for practical application in the frequency band of interest, and therefore had to be tested at lower frequencies. Thus, the 32G FET developed 1.8 W at 8 GHz and the 48G FET developed over 4 W at 4 GHz. If the gain of these units could be increased to usable levels at 10 GHz, it is expected that the power output would be essentially the same. Section II of this report details the progress made in the material and device development portion of this program.

Using FETs available within the time frame of this program from both within RCA and from outside sources, the best single-stage performance achieved within



DEVICE TYPE	2G	4G	16G	16G	48G
GAIN	6 dB	5 dB	5 dB	5 dB	4 dB
ADDED POWER	48 mW	136 mW	440 mW	1.36 W	3.0 W
DC POWER	267 mW	680 mW	2.2 W	5.44 W	12.0 W
POWER ADDED EFFICIENCY	18%	20%	20%	25%	25%

Total Gain : 25 dB
DC Power : 20.6 W
PA Efficiency: 24.3%

Figure 1. Overall amplifier approach.

the desired 9- to 10-GHz frequency band was an output level of 1 W with a gain of approximately 4 dB. Therefore, only amplifiers sufficient to populate the first four stages of the proposed amplifier module have been designed and assembled. Because of the late availability of the highest power devices, only the first three stages have been assembled into a single module. This module has a small-signal gain of 18.8 dB, a power output of 590 mW with an associated gain of 15.7 dB, and a power-added efficiency of 8.9%. After some difficulty with premature saturation when utilizing interdigitated couplers, a balanced fourth-stage module was fabricated by combining two 16G amplifiers with two Wilkinson couplers offset to achieve a quadrature combiner effect over the band of interest. This stage has an output of 1.48 W with 2.7-dB gain and 10.1% efficiency. When these two modules are cascaded to form a four-stage amplifier, an output of 1.38 W with 19.4-dB gain and 10.1% efficiency is obtained. Greater than 1-W output is achieved over the full 9- to 10-GHz band with this four-stage amplifier. Section III details the design procedures and results obtained for the amplifiers developed in this program.

Also included in Section III are discussions on the phase characteristics of pulsed gate FET amplifiers. This program has concentrated on the evaluation of the intrapulse and interpulse phase sensitivities of the various FET types as a function of variations in gate voltage, drain voltage, load mismatches, temperature, and drive level. It has been demonstrated that up to the power levels developed in this program, the pulsed phase performance of FET amplifiers is superior to that of comparable traveling-wave tubes, and as such, FETs are entirely suitable for the intended airborne phase array radar application.

Some 55 FETs have been delivered directly to NRL for customer evaluation. A summary of the characteristics of these delivered devices is given in Section IV.

An FET reliability program has been started with RCA funding. The preliminary results indicate that at normal operating channel temperatures of 130°C, the MTTF for RCA FETs is of the order of 10^6 hours. These data, which are detailed in Section V, confirms the validity of the fabrication techniques used to enhance reliability.

SECTION II

MATERIAL AND DEVICE DEVELOPMENT

A. FET PERFORMANCE

Before the commencement of this program, RCA's repertoire of FETs consisted principally of two types. RCA FET types are distinguished by counting the number of parallel gates where each gate is typically 150 μm wide. The simplest type of FET has 2 gates connected in parallel and is referred to as the 2G type. Its power output is of the order of 150 mW. A more sophisticated type is a multicell structure in which each of 5 cells has 4 parallel gates. One cell of this 4G type has an output power of approximately 250 mW. Greater powers have been achieved by connecting several cells in parallel. Thus with all five cells connected in parallel, powers of greater than 1 W have been achieved at X-band frequencies. This multicell approach is difficult to fabricate because of its many electrical contacts and relatively complicated assembly procedure.

The device part of this program has concentrated on the development of single-cell FETs having improved performance. By using a single-cell approach, the device becomes simpler to incorporate into amplifier circuits and has a potentially higher frequency capability. To obtain improved performance has required development of advances in the areas of material epitaxial growth, device processing, metallic contacts, device geometry, and FET evaluation.

This FET development program has resulted in five new geometries with high power performance. Table 1 summarizes the power capability demonstrated by these new FET types, mostly at 10 GHz.

The 8G type was initially designed to produce 0.5-W output power. This type has been perfected to the degree that power levels greater than 0.75 W are obtained and efficiencies of over 40% demonstrated. Two of these 8G types have been mounted in parallel on the same carrier to obtain greater than 1.3 W at 10 GHz. Figure 2 shows how these devices are mounted.

The 16G FET is designed to achieve a 1-W power level. At 10-GHz power levels as high as 1.2 W have been achieved with this geometry. Variations in this geometry have been made to incorporate the features that worked so well with the 8G type. These variations were made to incorporate the continuous

TABLE 1. PERFORMANCE OF NEWLY DEVELOPED RCA FET TYPES

Device Type	Gate Width (μm)	Power (mW)	Assoc. Gain (dB)	η_{PA} (%)	Sm. Signal Gain (dB)
8G	1200	854	5.2	28.4	9.4
8G	1200	590	5.3	42.3	7.8
2(8G)	2400	1372	4.3	27.4	6.6
16G	2400	1206	5.3	22.2	6.6
18G	3150	1262	3.9	11.8	5.0
32G*	4800	1800	3.3	14.0	5.0
48G**	9600	3000	4.7	32.0	6.5
48G**	9600	4100	3.4	12.6	5.3

*8 GHz
**4 GHz

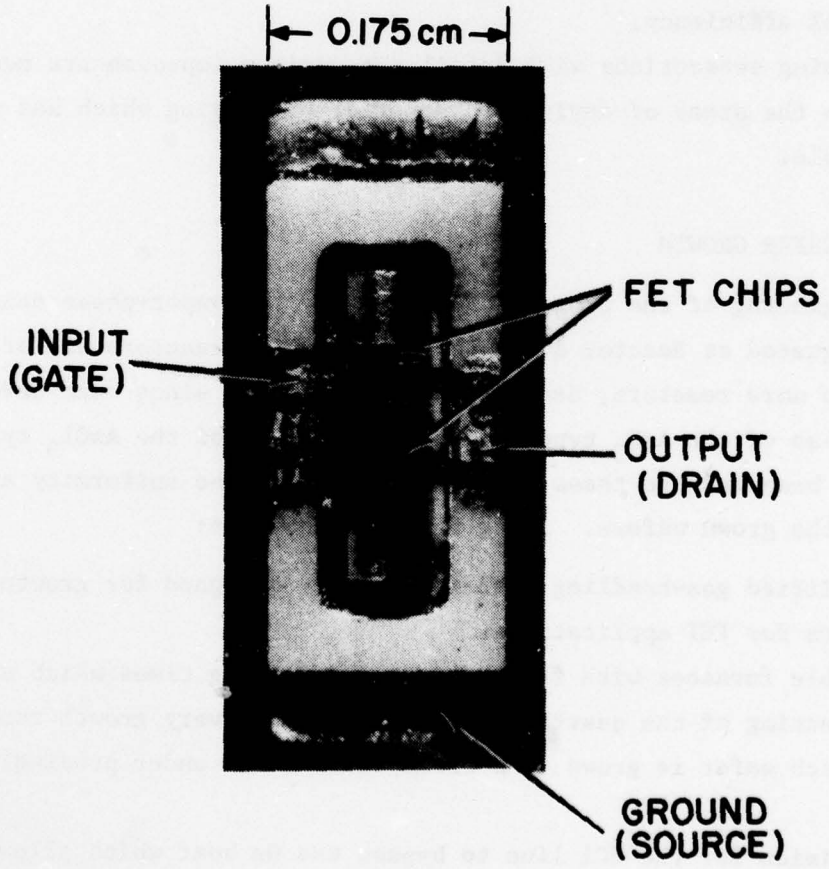


Figure 2. Photograph of 2 FET pellets flip-chip mounted on the same carrier.

gate structure, which will be described in detail in a later section. The resulting geometry has 18 continuous gates and early samples of this type have shown power levels slightly greater than the 16G type.

A 32G structure has been developed to achieve power levels of 2 W. The gain of this unit has been found to be too low at 10 GHz so that testing is done at 8 GHz. At this frequency, power levels of just under 2 W have been achieved with 3.9-dB gain and 14% power-added efficiency.

To achieve power levels approaching 4 W, a 48G FET has been developed. Because each gate is 200 μm wide, rather than the 150 μm used for all the other types, the total gate width for the device is 9600 μm. The input and output impedances associated with such a large area device are very low at high frequencies, causing the achievable gain to be very low. To obtain useful gains requires testing of this type FET at lower frequencies. At 4 GHz, this FET type has demonstrated power outputs of 3.0 W with an efficiency of 32%, or 4.1 W with 12.6% efficiency.

The following subsections will detail the various improvements made during this program in the areas of device and material processing which has made this progress possible.

B. EPITAXIAL WAFER GROWTH

At the beginning of the program, RCA had only two vapor-phase epitaxial reactors, designated as Reactor A and Reactor B. Both reactors are of the AsH_3 type. Two more reactors, designated C and D, have since been developed. Reactor C is also of the AsH_3 type, which Reactor D is of the $AsCl_3$ type. Innovations have been made to these reactors to improve the uniformity and reproducibility of the grown wafers. Among these changes are:

(1) Simplified gas-handling system expressly designed for growth of thin epitaxial layers for FET applications.

(2) Movable furnaces with fast heat-up and cooling times which allow for vapor phase cleaning of the quartz reactor tube after every growth run. This ensures that each wafer is grown in a clean environment under precisely similar conditions.

(3) Provision for the HCl line to bypass the Ga boat which allows vapor-phase wafer etching and excess HCl mole-fraction control.

(4) A baffle in front of the deposition zone which ensures efficient gas mixing and wafer uniformity.

(5) Elimination of the "history effect" or change in the background impurity level produced after growth of highly doped layers. This is achieved by the elimination of a side arm on the reactor tube.

Many of the features made on these reactors have since been incorporated into the original Reactor A. Because of the complete renovation done to this reactor, it is now called reactor A^+. Table 2 summarizes the properties of the various RCA vapor-phase epitaxial wafers.

TABLE 2. RCA's REACTORS

Reactor #	Type	Bore Diameter (cm)	Dopant	Remark
A^+	AsH_3	2.5	S, Cr	for Cr buffer layer
B	AsH_3	5.0	S	for undoped buffer
C	AsH_3	2.5	S, Si	1. for undoped buffer 2. for Si-doped n^+ layer
D	$AsCl_3$	4.0	S	for undoped buffer
A	AsH_3	2.5	S, Se	completely rebuilt to be A^+

Table 3 summarizes the wafer yield from the various reactors. Of the 510 wafers processed in the different reactors for all of our FET programs during the last two years, 80 were processed into FETs. Of these, 11 wafers were successfully processed in good quality FETs, where the criteria for acceptable performance is a gain of about 7 dB, a normalized power output of 0.5 W per mm of gate width, and a power-added efficiency of at least 15%.

The major material effort has been aimed at growing buffer layers 4 to 6 μm thick consistently. When 1-μm buffer layers are grown, a sharp transition between the n-layer and the buffer is observed as seen in Fig. 3. When thicker buffer layers are grown, an anomalous region of high carrier concentration close

TABLE 3. WAFER SUMMARY (1976 - 1978)

Reactor	No. of Wafers Grown	No. of Wafers Processed	No. of Useful Wafers
Old A	123	26	5
A^+	28	3	--
B	182	23	1
C	112	20	4
D	65	8	1
Total	510	80	11

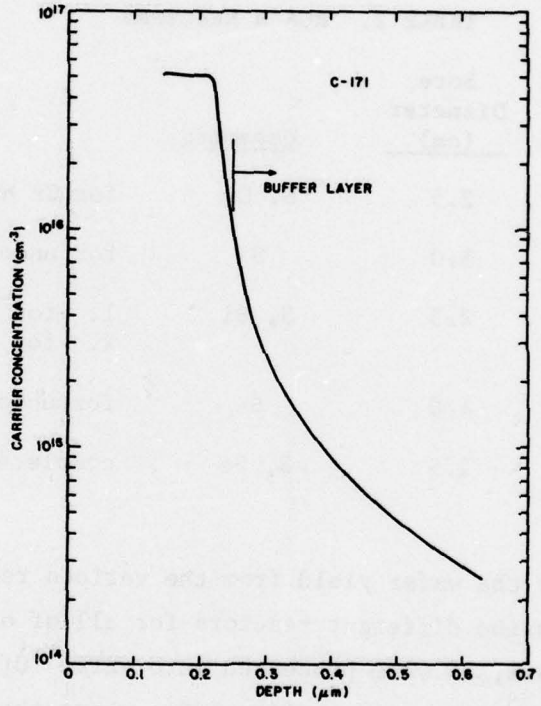


Figure 3. Growth adjusted for 1-μm buffer and 0.3-μm n-layer with no anomaly.

to the n-layer occurs, as shown in Fig. 4. As a result, the buffer layer region close to the n-layer is doped to 2×10^{15} cm^{-3} which is over 1 order of magnitude greater than desired for this region.

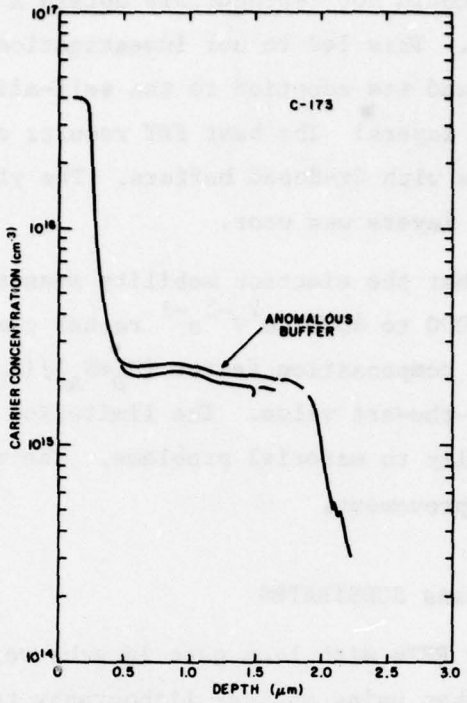


Figure 4. Growth adjusted for 4-μm buffer and 0.3-μm active layer. Note anomalous 2×10^{15} cm^{-3} doped layer.

It should be noted that our ability to grow very highly doped n^+-layers in the old A reactor was not understood. At that time, no one else in industry was able to obtain these n^+-dopings. Recent research* suggests that such high n^+-doping can be obtained under conditions of Ga deficiency at the substrate. It may be possible that such conditions existed in our old A reactor. After conversion to the new configuration, Reactor A^+ was used mostly for experiments on Cr-doping for the generation of buffer layers for FETs.

The problems encountered in materials technology for FETs during the course of the program were:

(1) Substrate flatness: A special polishing technique had to be developed to improve flatness. A slight concavity in the substrate drastically reduced photolithography yield. The new procedure developed improved yield.

*M. Yoder, (Private Communication).

(2) n^+-Doping: We could not reproducibly obtain n^+-doping greater than $5 \times 10^{18} cm^{-3}$. This led to our investigation of AuGe-based ohmic contacts and its adoption to the self-aligned gate process.

(3) Cr-doped buffer layers: The best FET results obtained by RCA were from wafers with Cr-doped buffers. The yield of wafers with Cr-doped buffer layers was poor.

It should be noted that the electron mobility measured on thin n-layers indicated values in the 4000 to 4500 $cm^2 V^{-1} s^{-1}$ rather consistently. This mobility corresponds to a compensation factor $(N_D+N_A)/(N_D-N_A)$ of close to 2. This is almost a state-of-the-art value. The limitation of FET performance cannot be attributed totally to material problems. The material quality, however, needs further improvement.

C. SURFACE FLATNESS OF GaAs SUBSTRATES

When the first power FETs with 1-μm gate lengths were being fabricated, it became apparent that when using optical lithography techniques, the GaAs wafer must have a very flat surface. Realizing that the mask aligner has a depth of focus of 1 μm, the wafer cannot be concave with a difference between high and low points of more than 2 μm. Special polishing techniques have been developed at RCA to eliminate this difficulty.

D. DEVICE PATTERN VARIATIONS

Using classical FET metallization patterns, in which all the gates are open-circuited at the drain pad end of the device, RCA developed a variety of FET types with dimensions as shown in Table 4. This geometry was dictated by the inability to fabricate a 1-μm gate stripe with bends which was free from short circuits or major discontinuities. Since the start of this program we have perfected a technique to do this and can now experiment with distinctly different gate patterns.

As a result, a continuous-gate structure has been developed which results in a significant improvement in device performance. With this pattern, two adjacent gates are connected together to form a U-shape pattern around the source pad, as shown in Fig. 5, rather than being open-circuited near the drain pad.

TABLE 4. RCA FET GEOMETRIES AND THERMAL RESISTANCE

Designation	2G	4G	8G	16G	32G	48G
Gate Stripes Per Cell	2	4	8	16	32	48
Gate Stripe Width (μm)	150	150	150	150	150	200
Gate Width Per Cell (μm)	300	600	1200	2400	4800	9600
No. of Cells Per Pellet	1	5	1	1	1	1
Drain Contact Width (μm)	25	25	25	12	12	12
Source Post Width (μm)	50	50	50	30	30	30
Design Output Power (μm)	0.15	0.25	0.5	1.0	2.0	4.0
Calculated Flip-Chip Cell Thermal Resistance (°C/W)	153	80	43	24	13	7

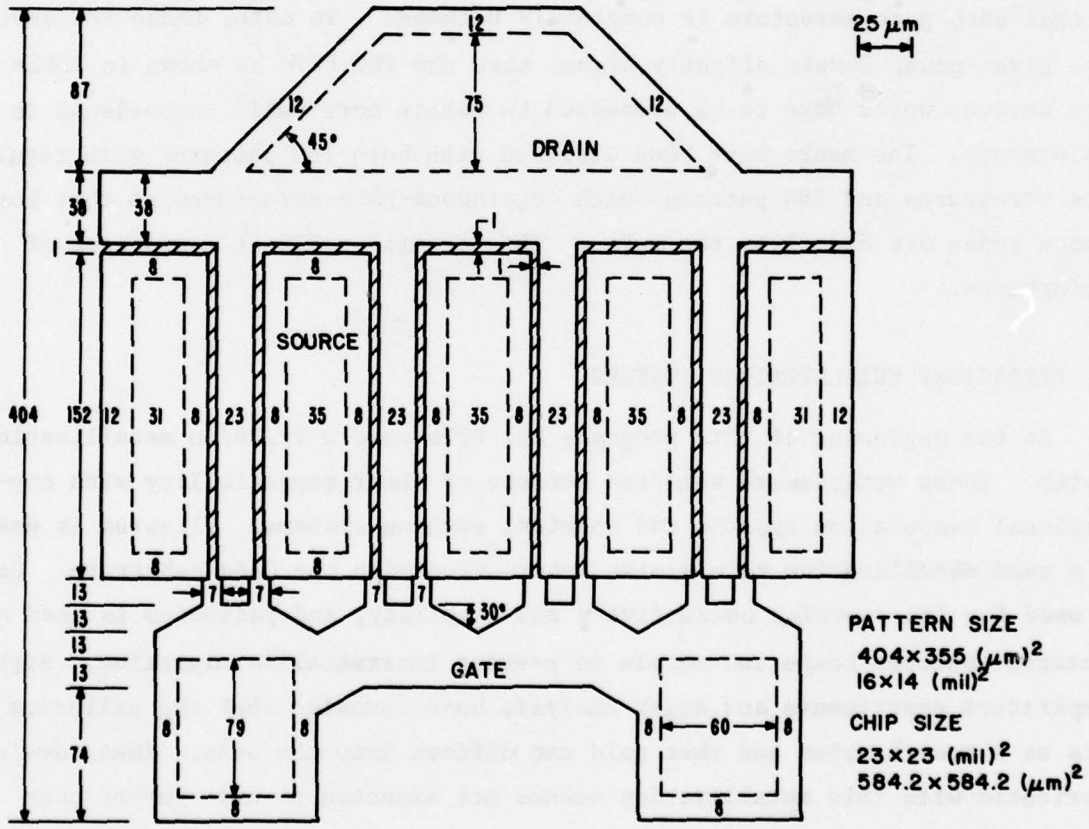


Figure 5. Continuous-gate 8G FET pattern.

In the open-gate structure, there is normally a wide separation between the drain pad and the source posts to provide high isolation between these terminals. In the continuous-gate structure, this cutout is replaced by the 4-μm spacing used between source and drain in the rest of the FET. The area now contributes to FET action and thus increases the gain, power output, and efficiency of the device. Thus, the continuous gate provides more effective use of the device real estate. Since the ends of the gates are now continuous rather than being open, the rf phase at the ends of the gates is now equalized.

As stated earlier, the 8G device was originally designed for 500-mW output power. However, by utilizing the continuous-gate structure, with its inherently lower-gate resistance, power levels greater than 750 mW have been obtained.

The continuous-gate pattern has worked so well with the 8G device that a similar concept has been tried for the higher power 16G FET. Besides making all the gates continuous, two more gates have been added in designing the mask so that each gate structure is completely U-shaped. To date, these 18G devices have given power levels slightly higher than the 16G FETs as shown in Table 1. More devices would have to be processed to obtain more valid comparisons in performance. The masks have been designed with both 16G patterns with regular gate structures and 18G patterns with continuous-gate structures so that both device types are made from the wafer. This permits a direct comparison of performance.

E. REFRACTORY METALLIZATION SYSTEMS

At the beginning of this program, all FETs used a Ti/Pd/Au metallization system. These metals were selected because of their compatibility with conventional evaporation systems and chemical etching systems. Titanium is used as a seed metallization to minimize interaction with the GaAs substrate. Gold is used for its superior conductivity and stability, and palladium is used as a barrier between these two metals to prevent intermetallic migration. High-temperature experiments and Auger analysis have revealed that the palladium acts as a poor barrier and that gold can diffuse into the GaAs. Thus, devices fabricated with this metallization scheme are expected to have rather poor reliability.

An electron beam evaporation system and an ion-beam etching system have since been set up so that complete freedom of choice exists in the selection of

metals. As a result, a multilayer conductor contact of titanium-platinum-gold is now being used on all RCA power FETs. High-temperature tests and Auger analysis show that this approach is extremely stable at temperatures up to 300°C because the platinum is a very effective barrier between the gold and the titanium layers. Therefore FETs using this metallization approach are expected to have much higher reliability.

F. AuGe OHMIC CONTACTS

The earliest RCA power FETs were made from wafers grown in the old Reactor A. This reactor had the capability to grow n^+-layer with very high-carrier concentrations, of the order of $4\text{-}6 \times 10^{18}$ cm^{-3}. With this high a concentration, low resistance ohmic contacts could be readily made directly with the Ti/Pt/Au metallization for the source and drain contacts. However, this carrier concentration is very close to the absolute maximum that can be achieved by vapor-phase epitaxy. As Reactor A aged, it was rebuilt and modifications were made to give it desirable features already incorporated into our newer reactors.

Presently, none of RCA's reactors have the capability to generate the high n^+-layer concentrations needed for good ohmic contacts.

Therefore, to achieve an ohmic contact technology compatible with the stringent constraints of the self-aligned gate technology, an AuGe/Ni process has been developed. In this technology, the source and drain contacts are processed with a multilayer metallization consisting of Ni/AuGe/Ti/Pt/Au, which for simplicity will be referred to as an AuGe contact. Initially, the surface finishes achieved with AuGe contacts were too rough to be compatible with the self-aligned gate technology. These surface finishes have been found to be a strong function of the sintering process used. It has been determined that the best procedure is to deposit the AuGe/Ni film at 90°C, sinter in hydrogen in a separate furnace, followed by rapid cooling. This AuGe contact technology is now incorporated in all RCA FETs.

G. AUTOMATION OF FLIP-CHIP PACKAGING TECHNIQUES

RCA was the first FET manufacturer to mount power FETs flipped onto the heat sink. Rather than mount the device face up, the device is mounted face down so that the source pads are directly bonded onto the heat sink. An analysis

of both configurations has shown that the thermal resistance of an up-mounted device is more than double the thermal resistance of the same device when flip-mounted. Table 4 shows the calculated thermal resistances for the various RCA FETs.

Flip-chip mounting also has the advantage of minimizing the parasitic inductance and resistance between the FET source and ground. This, in turn, gives the maximum performance from the device at X-band and KU-band frequencies.

Flip-chip bonding has previously been accomplished by manual methods of applying heat and pressure. Bonding is now accomplished automatically with a Kulicke and Soffa* Model 578-2 bonder. This instrument utilizes a partially transparent prism in its microscope assembly to permit a simultaneous viewing of the top surface of the copper pedestal onto which the device will be mounted, and the surface of the FET. The bonding pads on the standoff ring of the carrier and the ribbons attached to the FET can also be aligned during this sighting. This instrument permits alignment to within a few μm accuracy. Once the device is properly aligned to the pedestal, the device is automatically flip-chip bonded by the instrument.

In this section, it has been shown how with partial support from this program, RCA has advanced the performance of power microwave FETs. These advances have been made in the areas of material growth and characterization, metallization, and processing techniques, and geometrical changes in the metallization patterns. These changes have resulted in many new FET types having higher power levels, gains, and efficiencies within the X-band and KU-band frequency ranges.

*Kulicke and Soffa Inc., Horsham, PA.

SECTION III

AMPLIFIER DEVELOPMENT

A. APPROACH

The overall amplifier configuration proposed to satisfy the program design goals consists of a cascade of five balanced amplifier stages as discussed in Section I and shown in Fig. 1. This approach was predicated upon the successful development of new FET types with consistent repeatable high levels of performance. Within the 9- to 10-GHz frequency range, using both RCA and commercially supplied devices, the highest power level single-stage, single-ended amplifier developed during the time frame of this contract, utilized a 16G device to achieve a 1-W power level. Therefore, only single-ended amplifiers sufficient to populate the first four stages of the proposed amplifier shown in Fig. 1 were developed. The most dependable performance to date has been achieved from those devices used in the first three balanced stages; therefore, the three-stage amplifier shown in Fig. 6 has been assembled and tested. Figure 7 shows the saturation characteristic of this amplifier. It has a small-signal gain of 18.8 dB, and power output of 590 mW with an associated gain of 15.7 dB and a power-added efficiency of 8.9%. The dotted contour in Fig. 7 shows the saturation characteristic obtained when these three amplifiers were separately mounted and interconnected with SMA coaxial connectors. It can be seen that eliminating the two pairs of connectors and integrating into one package results in approximately 1.5-dB greater gain.

The swept response of the three-stage amplifier under both small-signal and large-signal conditions is shown in Fig. 8(a). Over the 9- to 10-GHz band, the small-signal response falls off by 2 dB, while the large-signal response falls off by 1 dB. The dotted line shows the large-signal response obtained when the three stages were interconnected through coaxial connectors. A small change in frequency response is evident. Integration of the three stages into a single module causes the frequency of maximum gain to slightly increase.

Toward the end of the program, a separately packaged fourth stage utilizing two 1-W amplifiers was completed. This amplifier stage uses an offset Wilkinson combiner design to achieve a quadrature coupling effect over the 9- to 10-GHz frequency band. This stage achieves a 1.5-W output with 2.7-dB gain and 10.1%

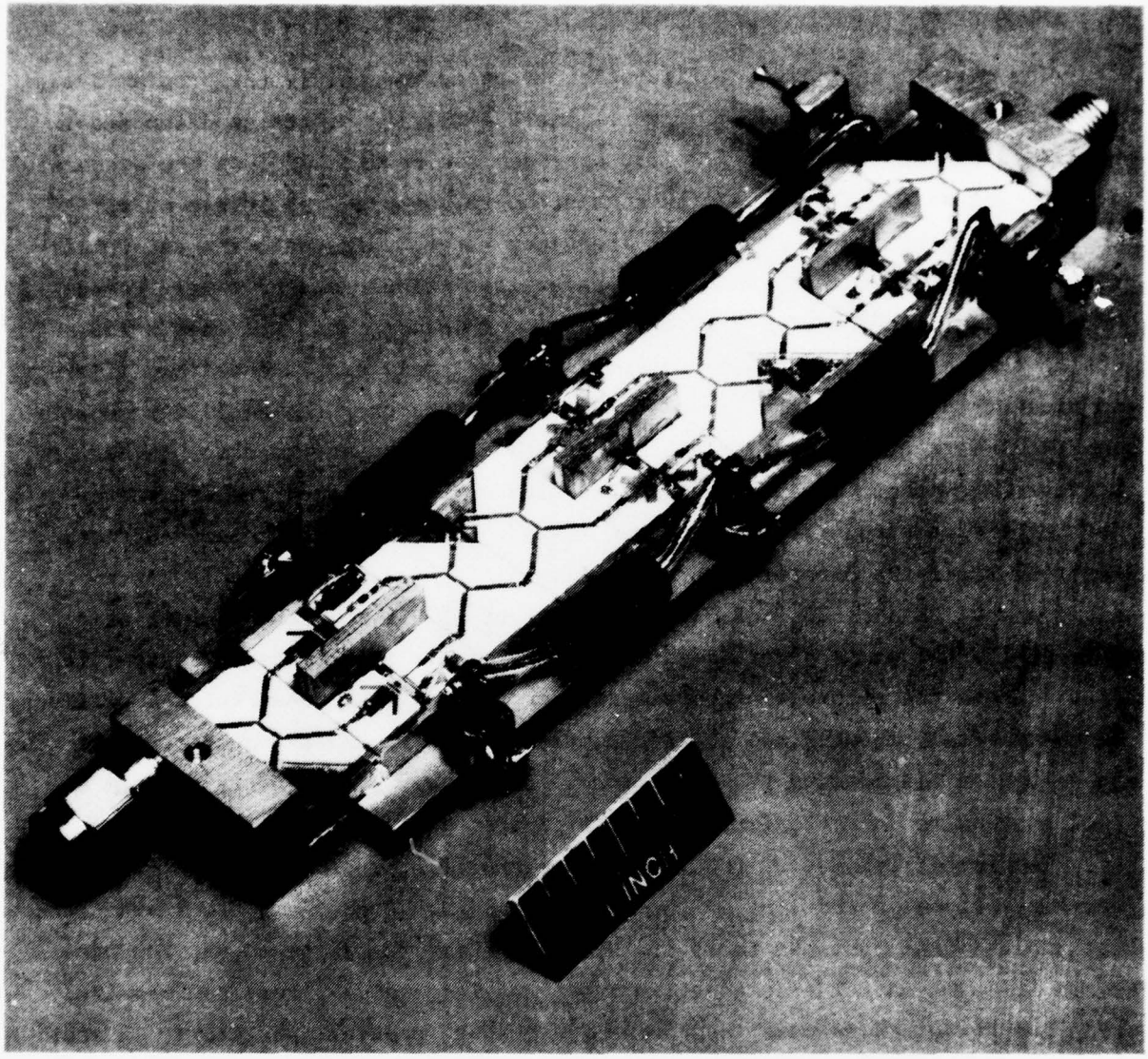


Figure 6. Prototype three-stage amplifier.

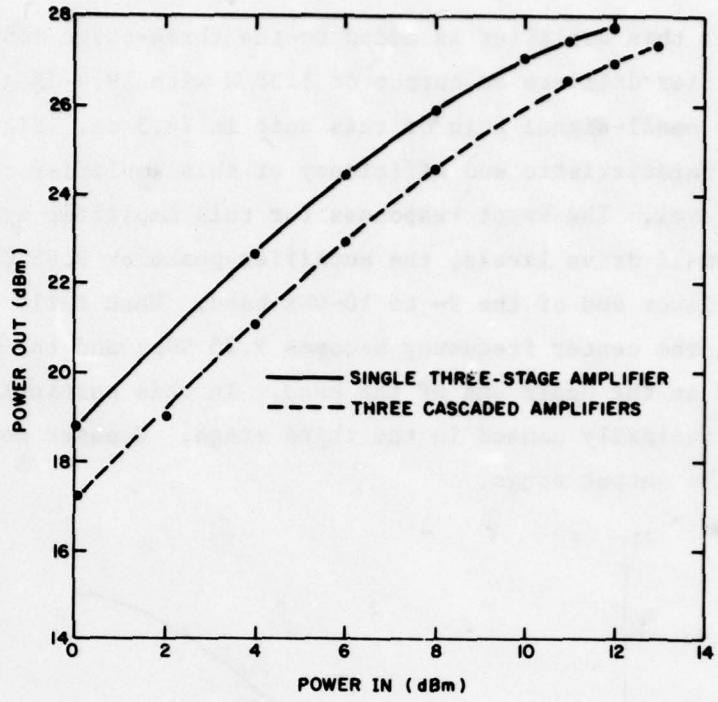


Figure 7. Saturation characteristics of the three-stage amplifier.

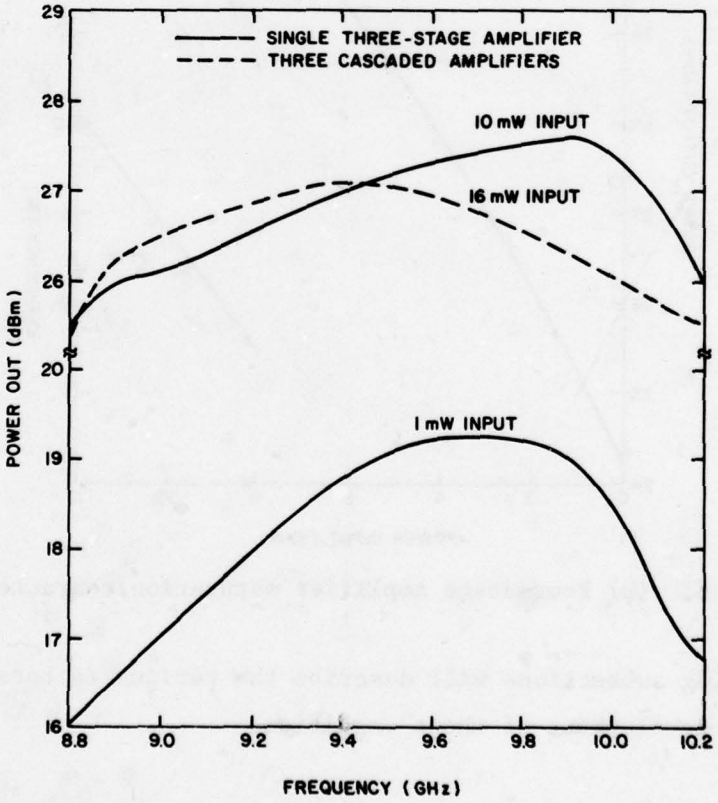


Figure 8. (a) Frequency response for three-stage amplifiers.

efficiency. When this amplifier is added to the three-stage module, the overall four-stage amplifier delivers an output of 1.38 W with 19.4-dB gain and 10.1% efficiency. The small-signal gain of this unit is 24.3 dB. Figure 8(b) shows the saturation characteristic and efficiency of this amplifier chain with increasing drive level. The swept responses for this amplifier are detailed in Fig. 8(c). At small drive levels, the amplifier peaks at 9.65 GHz and falls off 3 dB at the lower end of the 9- to 10-GHz band. When fully driven with an input of 12 dBm, the center frequency becomes 9.35 GHz, and the response falls off only 1.25 dB at the upper end of the band. In this particular amplifier, saturation is principally caused in the third stage. Greater power output is available from the output stage.

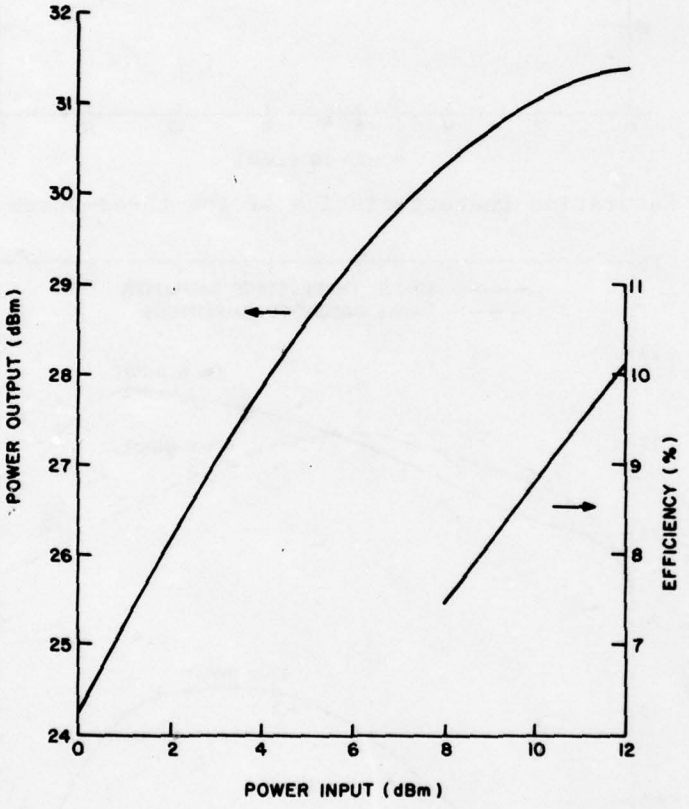


Figure 8. (b) Four-stage amplifier saturation characteristic.

The following subsections will describe the various factors that have been utilized in the development of these amplifiers.

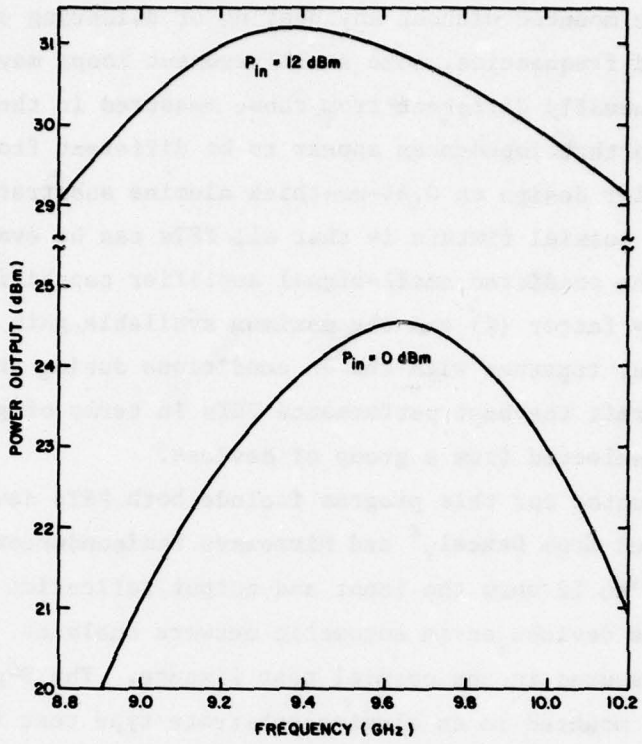


Figure 8. (c) Four-stage amplifier frequency response.

B. DEVICE CHARACTERIZATION

1. S-Parameter Measurement Techniques

When evaluating a FET for amplifier design on 0.64-mm-thick alumina substrates, the most usable S-parameters for small-signal design purposes are obtained by mounting a representative FET into a test fixture utilizing 50-ohm lines on similar type substrates. To improve accuracy and to suppress radiation and waveguide effects, this test fixture is placed into a waveguide below cutoff enclosure.

While this approach does give accurate data, it does subject the FET to extra heating and soldering operations. To reduce the failure rate of these FETs, it is highly desirable to minimize this type of handling. One approach which has been used is to evaluate only a representative few devices from a wafer and assume that the remainder of the wafer will have similar performance.

Recently, we have developed a coaxial test fixture into which a flip-chip mounted FET can be mounted without any heating or soldering operations. Within X-band and KU-band frequencies, some small resonant loops may be seen. The phase angles are usually different from those measured in the enclosed microstrip structure so that impedances appear to be different from those needed for microstrip amplifier design on 0.64-mm-thick alumina substrates. The major advantage of this coaxial fixture is that all FETs can be evaluated for S-parameters, and the predicted small-signal amplifier capability as calculated from the stability factor (K) and the maximum available gain (MAG) can be compared. These data, together with the dc conditions during test, especially the drain current, permit the best performance FETs in terms of gain and power capability to be selected from a group of devices.

Devices evaluated for this program include both FETs developed by RCA and units purchased from Dexcel,* and Microwave Semiconductor Corporation** (MSC). Figures 9 to 12 show the input and output reflection coefficients measured for these devices on an automatic network analyzer. Most of these parameters are measured in the coaxial test fixture. The S-parameters for the same type devices mounted in an alumina substrate type test fixture have already been shown in the second Semiannual Report (January, 1978) for this contract.

2. Large-Signal Characterization

The high-power performance of power FETs has been determined by chip tuning of the device when mounted in an open test fixture. It has usually been found that this is preferable to using external tuning elements because matching at a distance from the device causes some losses due to the high currents in the transmission line sections between the device and the tuning element. Table 5 shows the type of data which result from this kind of test for an 8G device.

The coaxial test fixture is also finding application in high-power characterization of FETs. RCA has previously developed a C-band load-pull test setup which, when used in conjunction with our in-house minicomputer system,

*Dexcel Inc., Santa Clara CA.
**Microwave Semiconductor Corp., Somerset NJ.

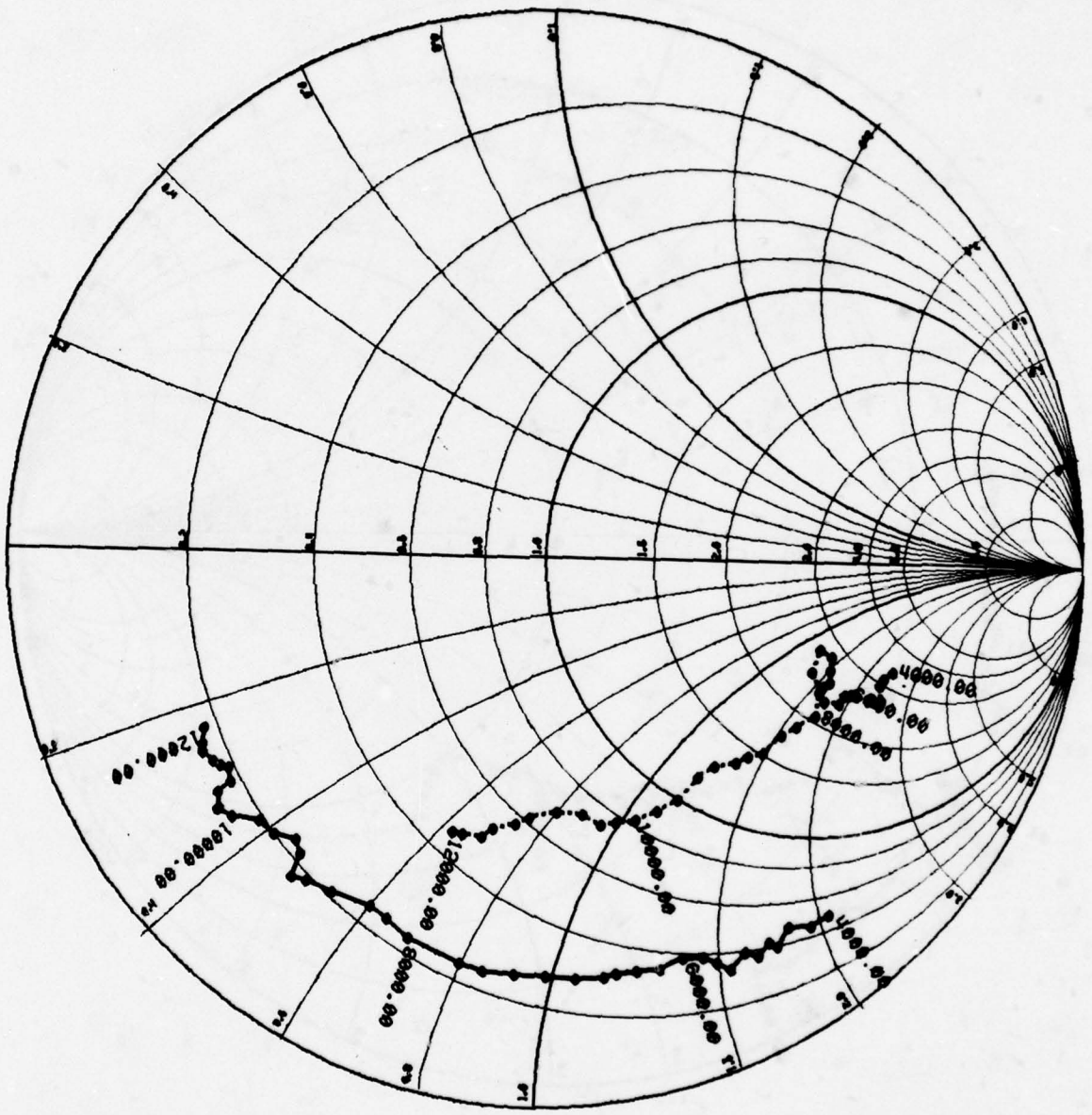


Figure 9. S_{11} and S_{22} of a Dexcel-3501A FET.

S11 - C182-2 8G RG -2V, 275MA @ 8V, COAX MT ZO= 50.00
S22 - C182-2 8G RG -2V, 275MA @ 8V, COAX MT ZO= 50.00

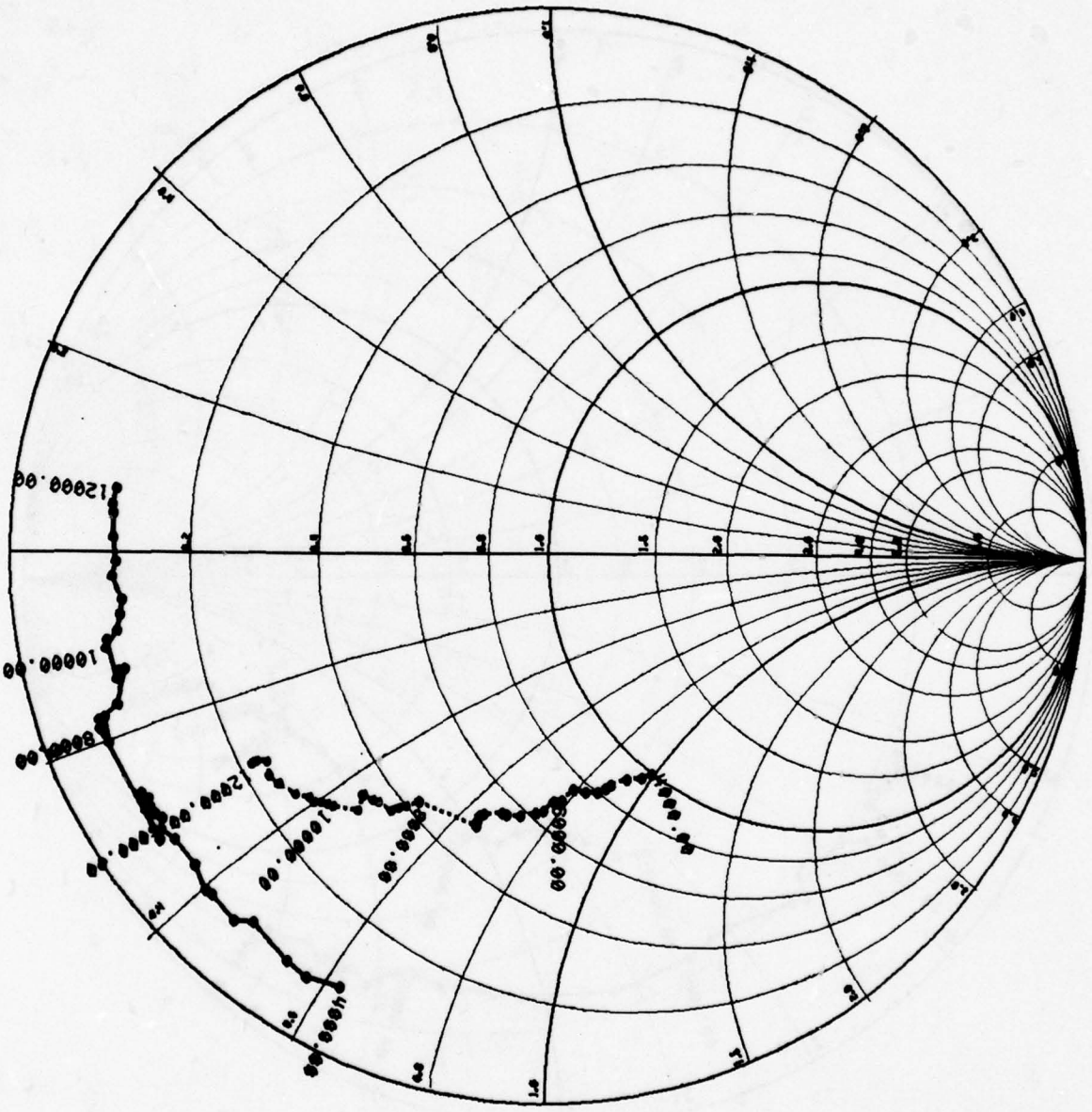


Figure 10. S_{11} and S_{22} of a C182B 8G FET.

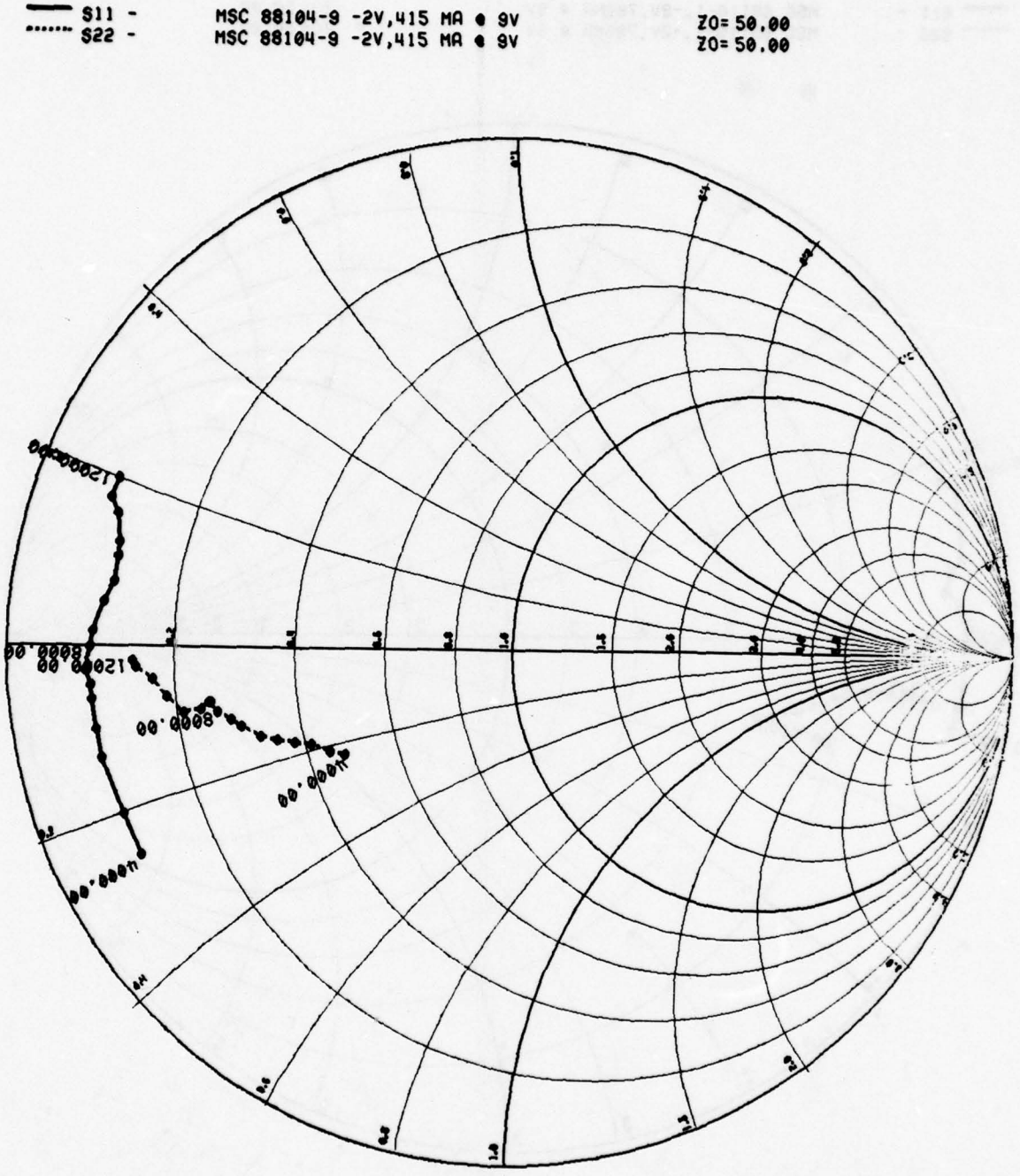


Figure 11. S_{11} and S_{22} of a MSC 88104 16G FET.

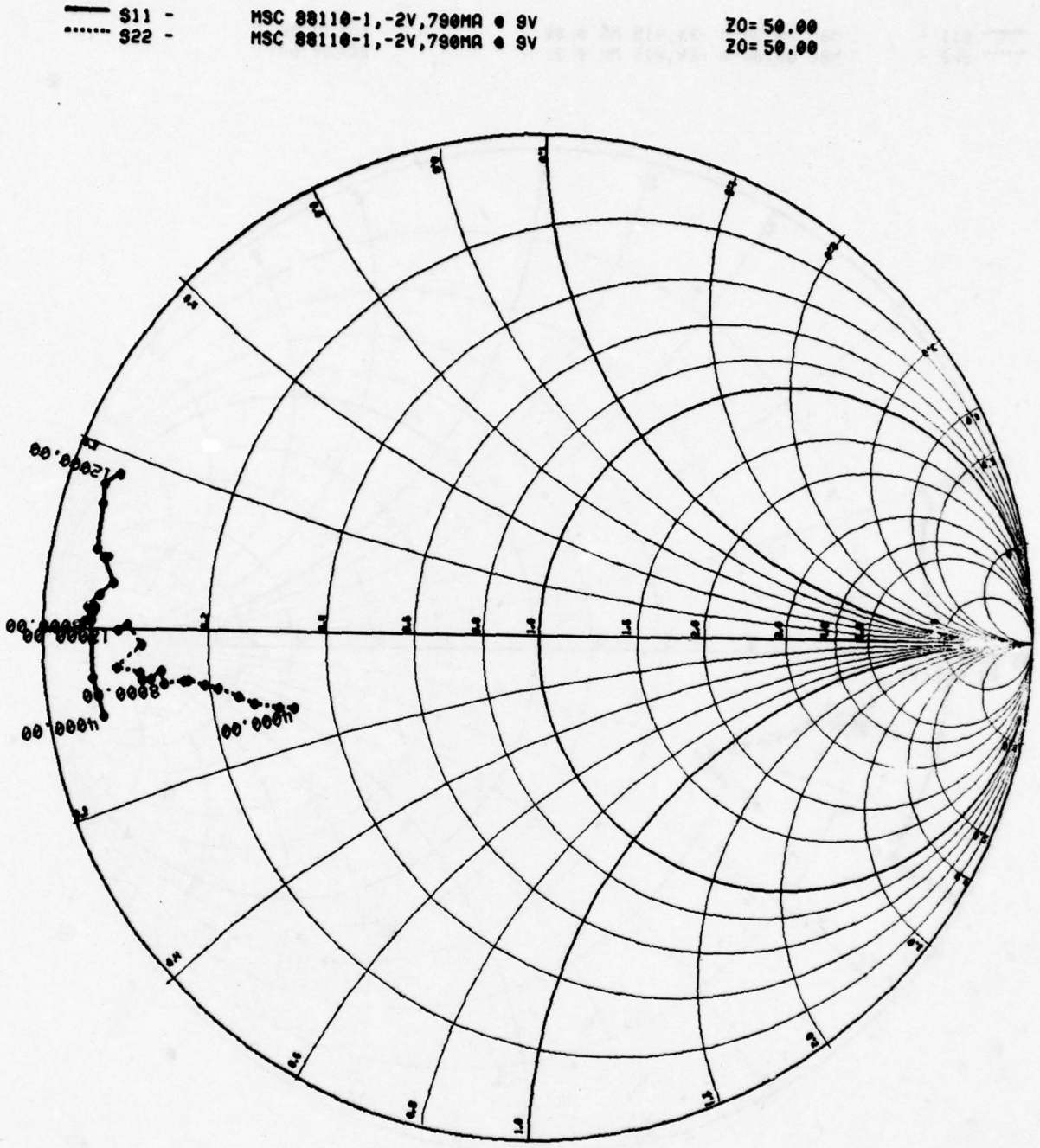


Figure 12. S_{11} and S_{22} of a MSC 88110 40G FET.

TABLE 5. RCA MESFET EVALUATION SHEET

DEVICE: 3172A-9 9G CG

V_D = 10 V, I_{DSSO} = 442 mA, V_G = -2 V, f = 10 GHz

V_{SAT} = 2.5 V, G_M = 62 mmho, V_B = V at 1 mA

P_i	P_{in}(mW)	P_o	P_{out}(mW)	G(dB)	I_D(mA)	$P_{out}-P_{in}$(mW)	η_{PA}(%)
50	45	160	214.4	6.78	329	169.4	5.1
100	90	295	395.3	6.427	334	305.3	9.1
200	180	520	696.8	5.878	338	516.8	15.2
300	270	610	817.4	4.810	322	547.4	17.0
400	360	655	877.7	3.870	309	517.7	16.75
500	450	670	897.8	2.99	303	447.8	14.77
600	540	680	911.2	2.272	301	371.2	12.37

permits a measurement of the power output, gain, and efficiency of a FET under large-signal conditions as a function of the load impedance presented to the output of the FET. This information is plotted directly on a Smith chart by the computer in the form of constant power impedance contours. During this program period we have developed a high-frequency load-pull unit to cover the 8- to 18-GHz band. This high-frequency load-pull unit required much more precise mechanical construction, and it also required some software modifications from the low-frequency unit. The high-frequency unit was constructed and debugged toward the end of this program. Because of the delay in the development of the high-frequency load-pull, the matching networks of the power stages initially designed were based on small-signal S-parameters. The output matching networks of the amplifiers were trimmed to provide a nearly optimum large-signal operation. However, some large-signal S-parameters as measured by our high-frequency load-pull are presented here. Figure 13 shows representative contours obtained at 9.5 GHz for an 8G type FET using a newly developed high-frequency version of this load pull apparatus. The impedance contours for a given output power are nearly circular.

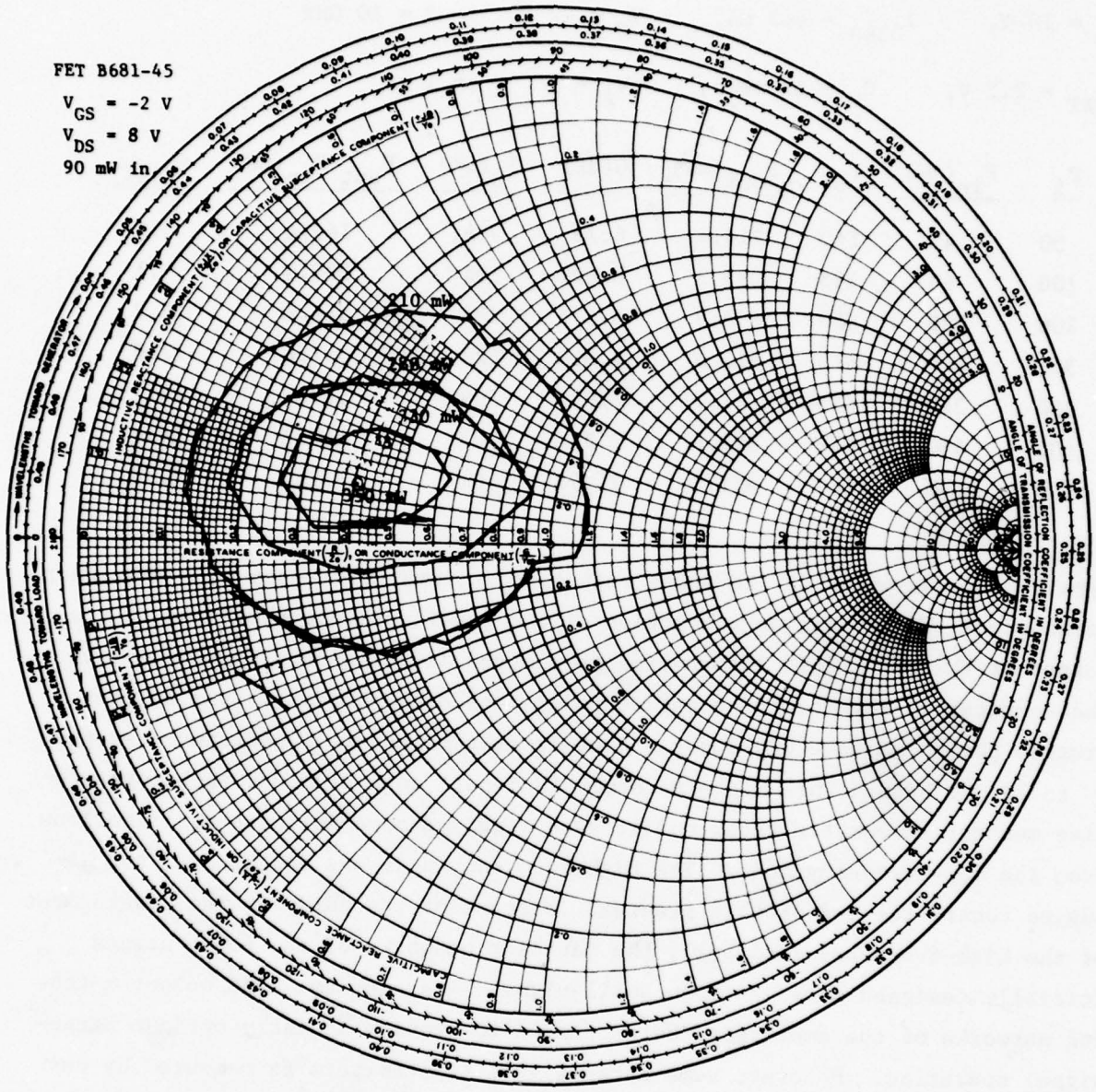


Figure 13. Constant power contours at 9.5 GHz.

3. IR Scanning Measurements

The power FETs used in this program are flip-chip mounted to achieve optimum electrical performance at these frequencies and to guarantee a minimum thermal resistance. The effectiveness of the flipping process in firmly bonding all source posts to the copper pedestal heat sink can be readily determined with an infrared scanning microscope system developed at RCA. This system can measure the temperature variation across the face of the FET because the GaAs material is effectively transparent to the IR radiation generated at this surface. The microscope can therefore read the radiated energy through the back side of the FET, provided that this surface is not metallized, which is true for the devices used in this program. Figure 14 shows the resulting plot generated under computer control for a properly flipped device, while Fig. 15 shows the plot for a device in which some of the source posts are poorly bonded. Poorly bonded source posts sometimes manifest themselves through abnormally low drain currents or through drain currents which change abruptly as the normal power dissipated in the FET causes an increase in device temperature.

C. AMPLIFIER LAYOUT

In the beginning of this program, an amplifier layout was developed for the five-stage amplifier as shown in the photograph of Fig. 16. In this arrangement, each amplifier stage and each directional coupler is mounted on a separate block, permitting individual testing, adjustment, and repair of each component part before overall assembly and integration. The amplifier blocks are fabricated with a side wall so that when placed into the chassis and covered, each amplifier stage is an isolated waveguide below cutoff section. This approach minimizes interaction between the individual amplifiers in a balanced stage to negligible amounts.

On the other side of the chassis is a cutout area for placement of pulse modulation circuitry. The cross-sectional view of this arrangement is shown in Fig. 17. Bias wires which carry the dc and pulse modulation are designed to pass through holes placed on either side of the FET carrier. This same bias layout arrangement is utilized in the three-stage demonstration unit shown in Fig. 6.

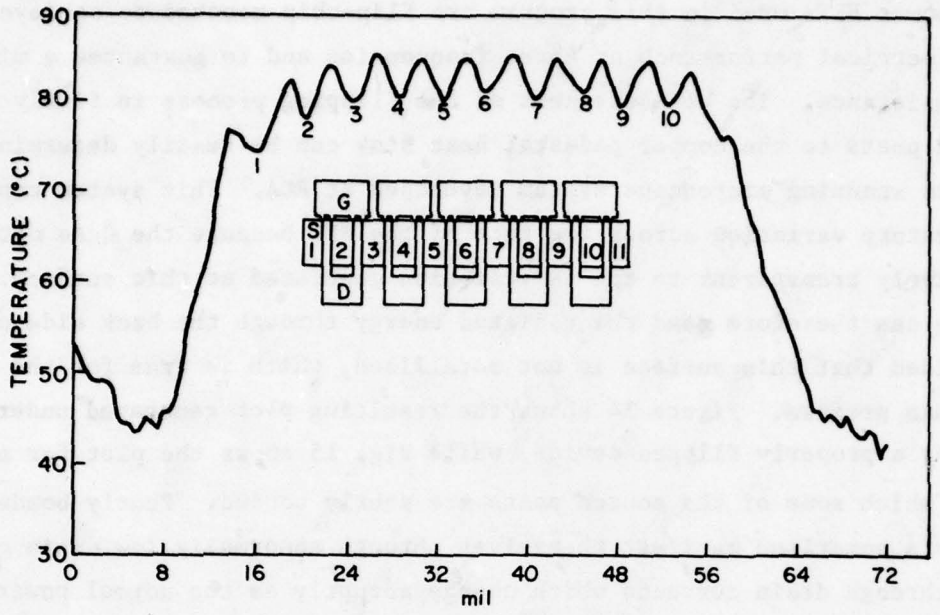


Figure 14. Temperature profile of an RCA 5-cell power MESFET.

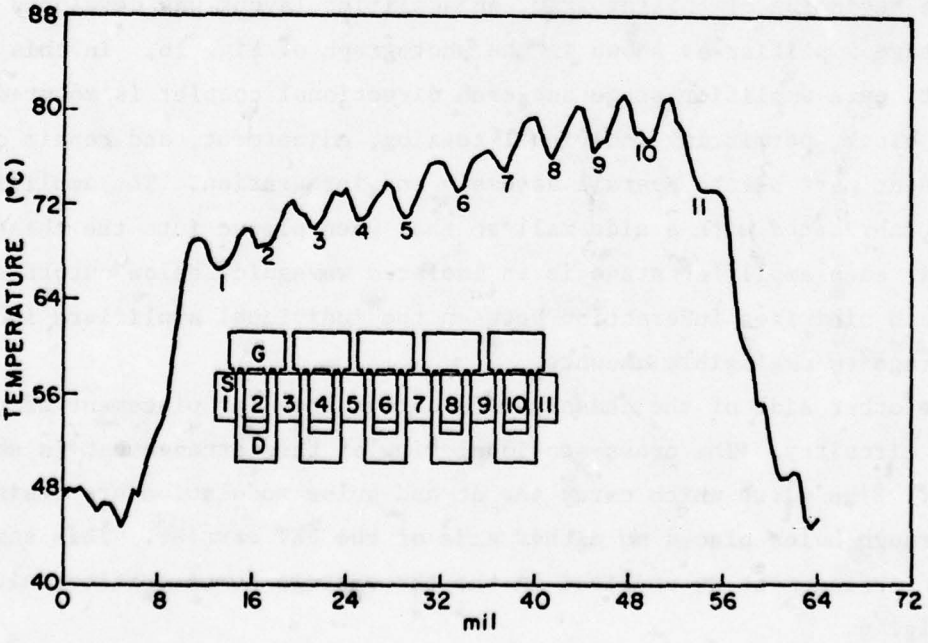


Figure 15. Temperature profile of an RCA 5-cell power MESFET, improperly bonded. Cell #1 was better bonded than cell #11.

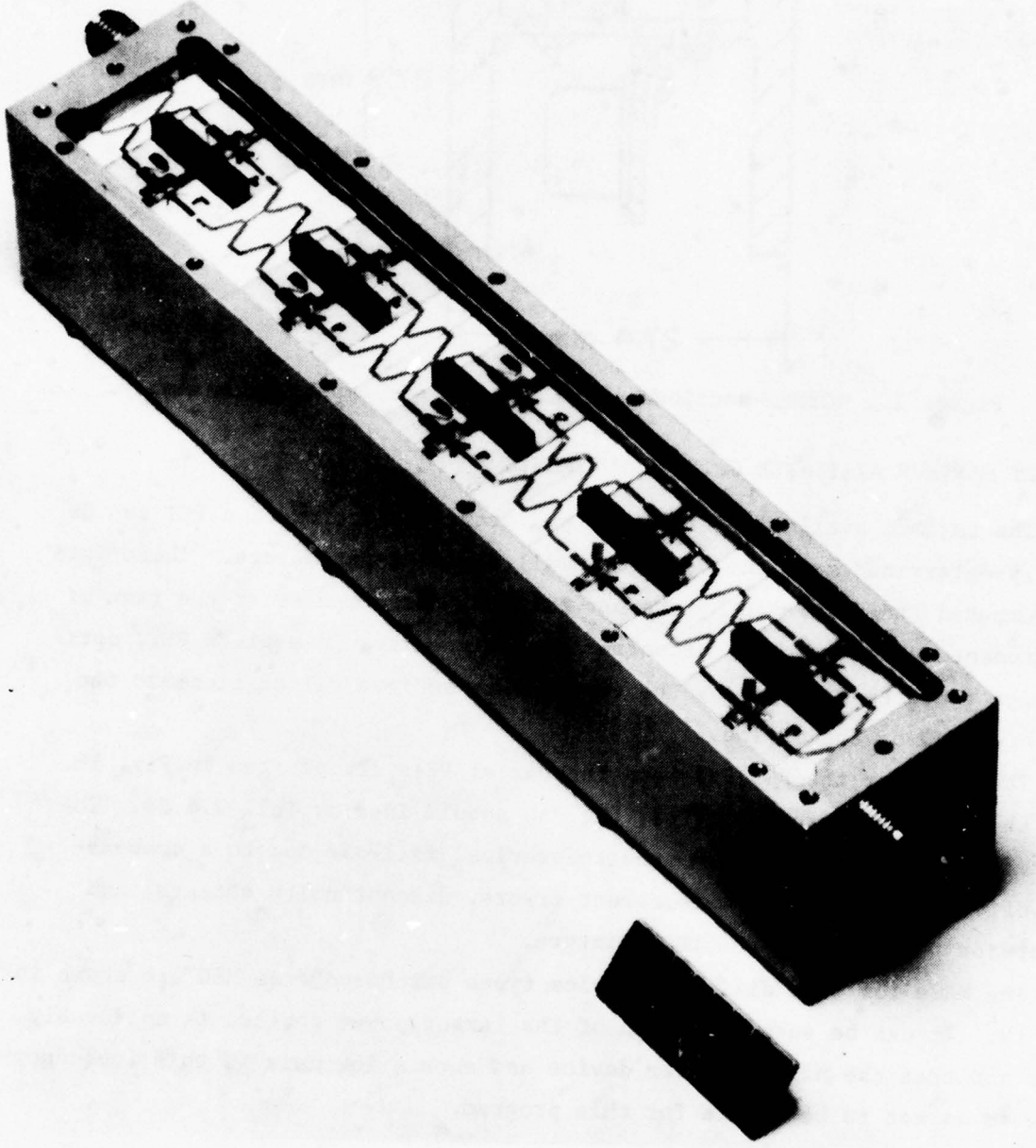


Figure 16. Model of the amplifier module.

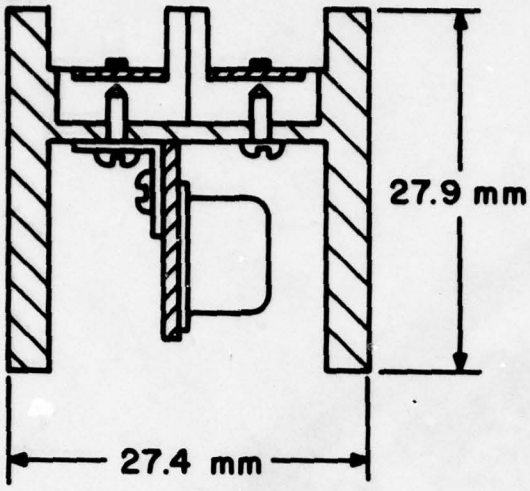


Figure 17. Cross-sectional view of complete amplifier assembly.

D. FET MAXIMUM AVAILABLE GAIN MEASUREMENTS

The maximum available gain (MAG) and stability factor of a FET can be readily determined from the measured small-signal S-parameters. These data are computed and displayed by the network analyzer computer at the time of measurement. When matching networks are designed around a given FET, optimization routines are used by the computer to achieve values close to the predicted MAG of the device.

The MAGs for the RCA FETs and the Dexcel FETs are plotted in Fig. 18. Over the frequency range plotted, the MAG should ideally fall 2.4 dB. The plotted variations differ from the theoretical fall-off due to a combination of effects including measurement errors, discontinuity effects, and dispersion phenomena in the test fixture.

The MAGs for five different device types purchased from MSC are shown in Fig. 19. It can be seen that gain of the larger power devices is noticeably lower and that the highest power device has such a low gain in this frequency range so as not to be usable for this program.

E. AMPLIFIER DESIGNS

Once the small-signal S-parameters of a given FET have been measured, the input and output reflection coefficients are plotted on a Smith chart as shown in Figs. 9 through 12. These impedances are used to generate an initial guess for a small-signal amplifier design. This design is verified with a computer

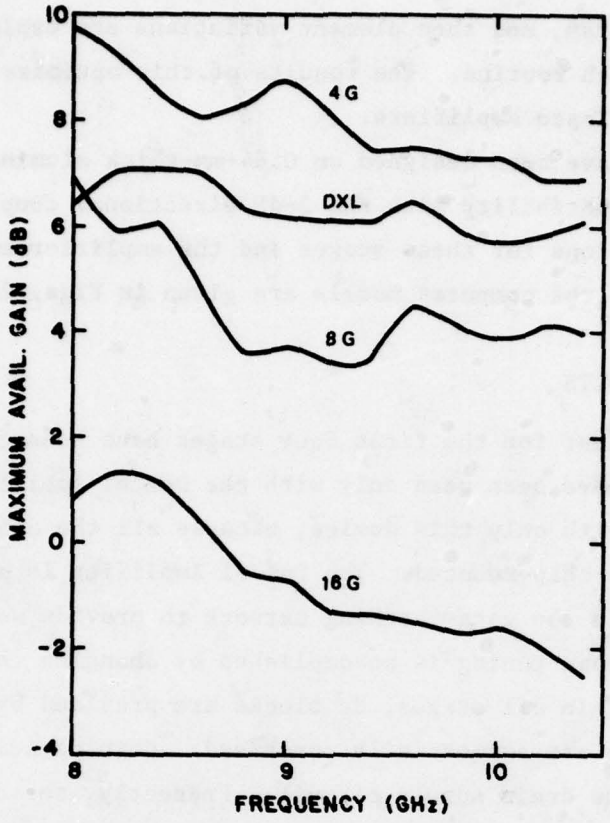


Figure 18. FET maximum available gain.

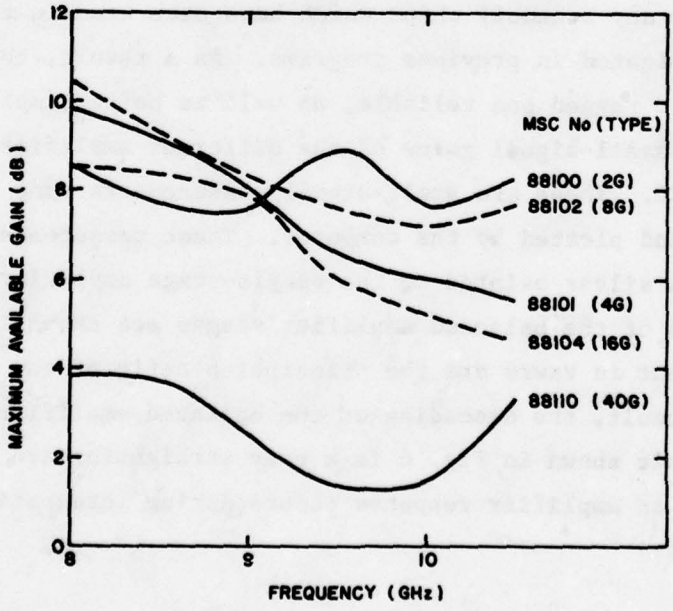


Figure 19. FET maximum available gain.

network analysis program, and then element variations are explored with a computer optimal search routine. The results of this optimization procedure are then used to fabricate amplifiers.

All amplifiers have been designed on 0.64-mm-thick alumina substrates to assure maximum compatibility with the 3-dB directional couplers. The schematic representations for these stages and the amplifier small-signal response predicted by the computer models are given in Figs. 20 through 23.

F. SMALL-SIGNAL RESULTS

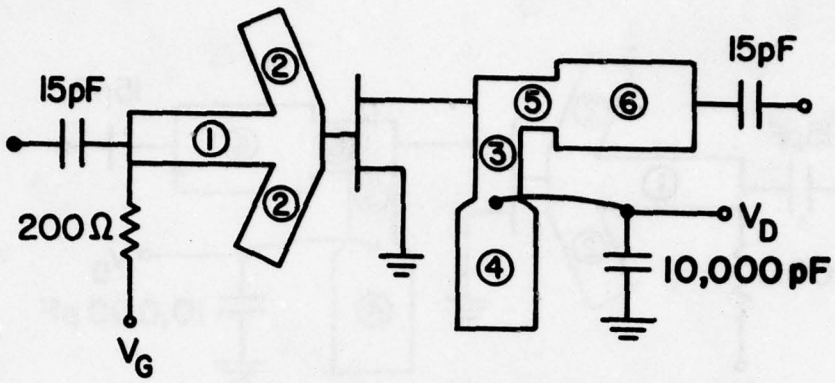
Circuits sufficient for the first four stages have been fabricated and tested. Wire bonds have been used only with the Dexcel amplifier stage. These bonds are necessary with only this device, because all the other FETs used in this program are flip-chip-mounted. The Dexcel amplifier is also designed with a series inductance in the gate-matching network to provide some circuit adjustment. In this stage tuning is accomplished by changing the number of parallel wire bonds. In all stages, dc blocks are provided by 15-pF beam lead capacitors which are commercially purchased. Chip capacitors of 10,000 pF are used to bypass the drain supply circuit. Presently, the amplifiers are configured for pulsing at the gate by using a 200-ohm chip resistor for dc and pulse injection into the gate-matching network. These circuits have not used any wire bonds nor any standoff chips which have been used in the bias circuits of amplifiers fabricated in previous programs. As a result, these circuits are expected to be more rugged and reliable, as well as being simple to fabricate.

The measured small-signal gains of the different amplifiers are plotted in Figs. 24 through 26. These are small-signal measurements done on the automatic network analyzer and plotted by the computer. These measurements are done with coaxial connectors silver painted to the single-stage amplifiers.

The responses of the balanced amplifier stages are shown in Figs. 27 through 29. The improvement in vswrs are the principal benefit of the balanced amplifier approach. As a result, the cascading of the balanced amplifier stages to form the three-stage unit shown in Fig. 6 is a very straightforward procedure. No unexpected change in amplifier response occurs during integration.

G. POWER RESULTS

Balanced power amplifier stages for the first four stages of the desired 9- to 10-GHz amplifier have been fabricated by combining pairs of single-ended

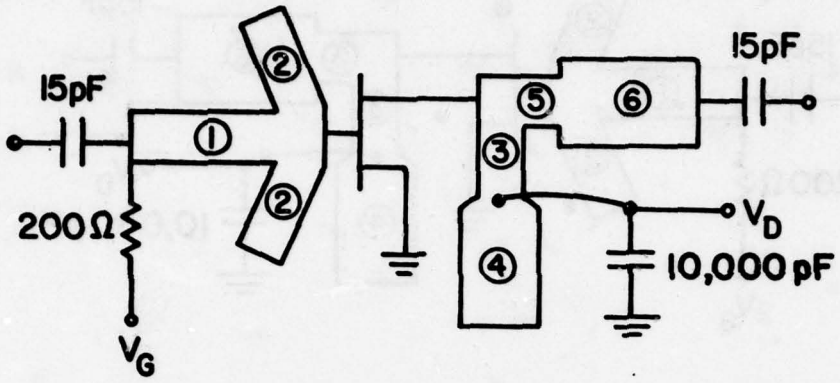


LINE #	LENGTH (mil/cm)	WIDTH (mil/cm)
1	145 (0.368)	75 (0.191)
2	86 (0.218)	16 (0.041)
3	76 (0.193)	5 (0.013)
4	117 (0.297)	50 (0.127)
5	90 (0.229)	10 (0.025)
6	53 (0.135)	23 (0.058)
Gate Induct.	0.44nH	

COSMIC(RTE) RUN: 8/22/77
DATA FILE: $.RLE4: DXL3501A, -1V, 42 MA @ 8V.
ANALYSIS ONLY!...

FREQ	FGAIN PH		FLATNESS		S11,I.RC		S22,0.RC	
	X	1.000DB	X	1.000DB	X	1.000*	X	1.000*
8.800	8.542	-159.63	0.000	0.00	0.326	-51.95	0.531	-137.93
9.000	8.706	-176.57	0.164	0.16	0.294	-79.14	0.458	-153.79
9.200	8.660	167.24	0.164	-0.05	0.253	-99.00	0.386	-172.89
9.400	8.506	150.54	0.201	-0.15	0.211	-122.69	0.319	163.84
9.600	9.025	133.36	0.519	0.52	0.254	-148.78	0.309	132.15
9.800	8.815	116.97	0.519	-0.21	0.213	-168.63	0.290	100.62
10.000	8.778	95.94	0.519	-0.04	0.205	150.24	0.323	67.76
10.200	8.145	76.32	0.880	-0.63	0.167	95.02	0.387	42.42

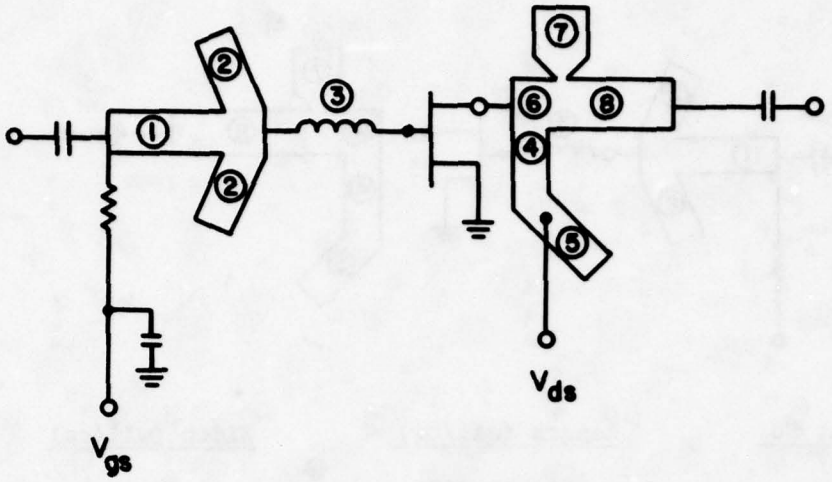
Figure 20. Amplifier design and predicted performance using a DEXCEL-3501A FET.



LINE #	LENGTH (mil/cm)	WIDTH (mil/cm)
1	133 (0.338)	75 (0.191)
2	70 (0.178)	40 (0.102)
3	30 (0.076)	6 (0.015)
4	117 (0.297)	50 (0.127)
5	30 (0.076)	30 (0.076)
6	80 (0.203)	40 (0.102)

FREQ	FGAIN PH		FLATNESS		S11,I.RC		S22,0.RC	
	X	1.000DB	X	1.000DB	X	1.000*	X	1.000*
8.800	6.405	-126.72	0.000	0.00	0.308	-82.40	0.641	-85.33
9.000	6.651	-142.04	0.247	0.25	0.319	-104.44	0.582	-98.65
9.200	6.721	-156.61	0.316	0.07	0.320	-124.20	0.504	-113.22
9.400	6.951	-175.47	0.546	0.23	0.376	-153.39	0.418	-126.66
9.600	7.205	168.65	0.801	0.25	0.438	-173.61	0.361	-143.53
9.800	6.704	155.17	0.801	-0.50	0.379	166.78	0.303	-160.11
10.000	6.405	140.45	0.801	-0.30	0.360	147.29	0.255	-177.96
10.200	6.052	128.05	1.153	-0.35	0.336	125.76	0.234	161.08

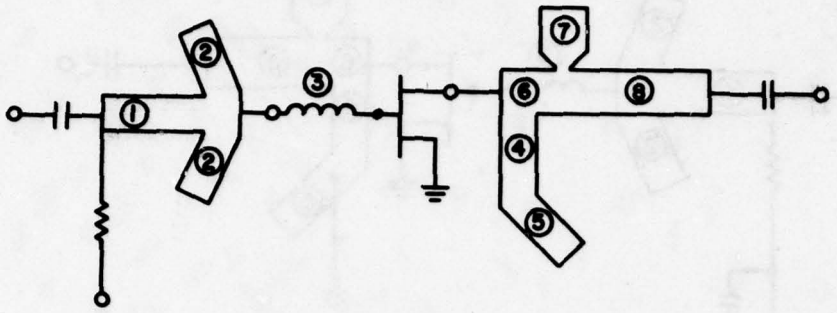
Figure 21. Amplifier design and predicted performance using a 4G single-cell FET.



Element No.	Length (mil/cm)	Width (mil/cm)
1	110 (0.279)	42 (0.107)
2	66 (0.168)	50 (0.127)
3	0.17 nH	
4	21 (0.053)	6 (0.015)
5	117 (0.297)	50 (0.127)
6	35 (0.089)	39 (0.099)
7	65 (0.165)	45 (0.114)
8	110 (0.279)	39 (0.099)

FREQ	FGAIN PH		I VSWR O		FLATNESS	
	X	1.000DB	X	1.000	X	1.000DB
8.600	7.508	167.54	4.198	1.09	0.000	.00
8.800	7.449	153.66	3.332	1.05	0.059	-.06
9.000	7.569	144.57	3.430	1.13	0.121	.12
9.200	7.208	130.92	2.428	1.14	0.362	-.36
9.400	7.590	118.48	2.116	1.24	0.382	.38
9.600	7.325	107.75	1.836	1.22	0.382	-.26
9.800	7.092	92.53	1.319	1.19	0.498	-.23
10.000	7.590	75.26	1.440	1.22	0.498	.50
10.200	7.186	58.47	1.710	1.30	0.498	-.40
10.400	7.214	41.14	2.398	1.41	0.498	.03

Figure 22. Amplifier design and predicted performance using an 8G FET.



Element No.	Length (mil/cm)	Width (mil/cm)
1	109 (0.277)	47 (0.119)
2	77 (0.196)	30 (0.076)
3	0.135 nH	-
4	113 (0.287)	5 (0.013)
5	117 (0.297)	50 (0.127)
6	25 (0.064)	47 (0.119)
7	77 (0.196)	40 (0.102)
8	109 (0.277)	47 (0.119)

FREQ	FGAIN PH		I VSWR O		FLATNESS	
	X	1.000DB	X	1.000	X	1.000DB
9.400	4.368	127.87	2.424	1.73	0.000	0.00
9.600	5.631	117.91	2.337	1.77	1.263	1.26
9.800	7.264	106.87	2.746	1.70	2.896	1.63
10.000	7.357	79.31	1.720	1.33	2.989	0.09
10.200	7.229	63.51	1.559	1.17	2.989	-.13
10.400	5.503	44.04	1.445	1.15	2.989	-1.73
10.600	5.095	24.76	1.944	1.35	2.989	-.41

Figure 23. Amplifier design and predicted performance using a 16G FET.

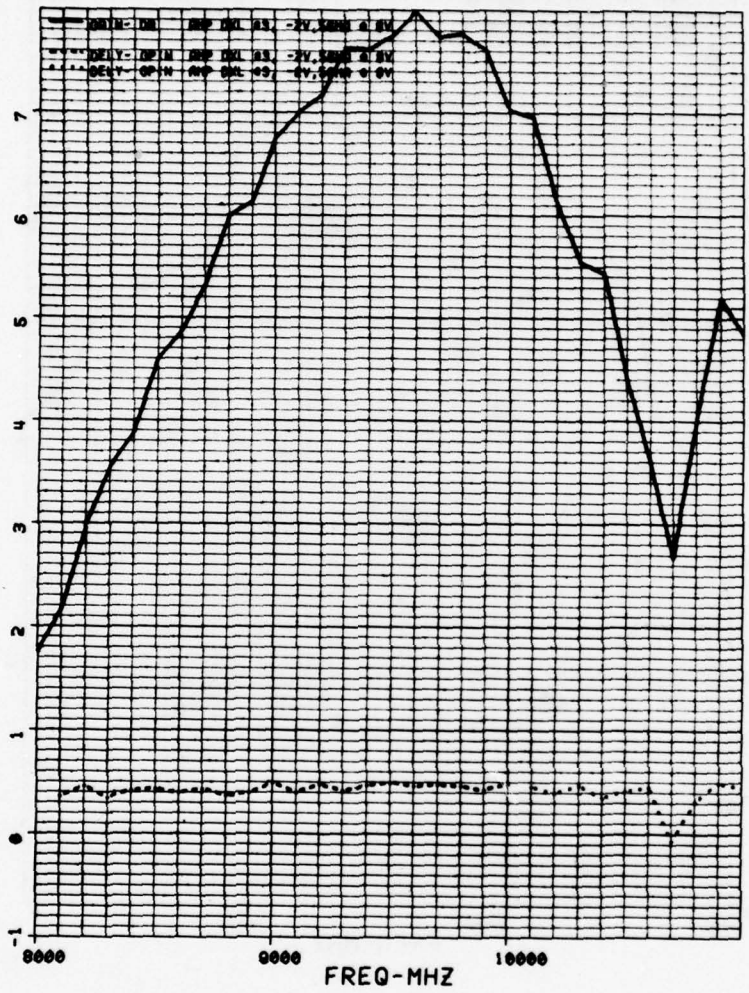


Figure 24. Measured small-signal response for a Dexcel-3501A single amplifier stage.

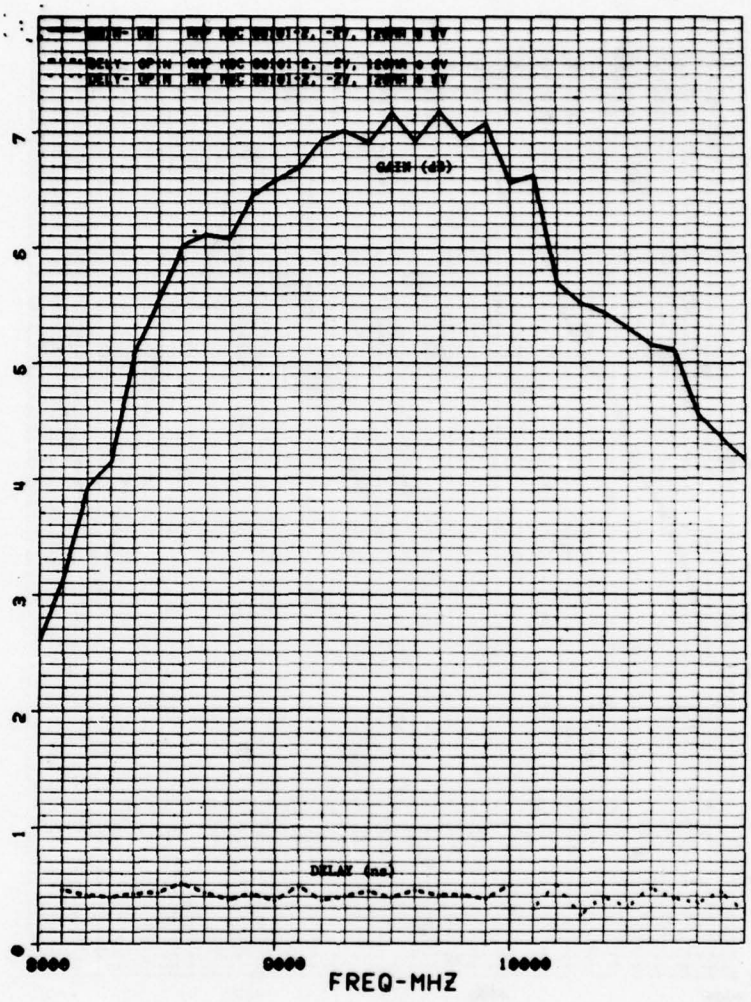


Figure 25. Measured small-signal response for a 4G single amplifier stage.

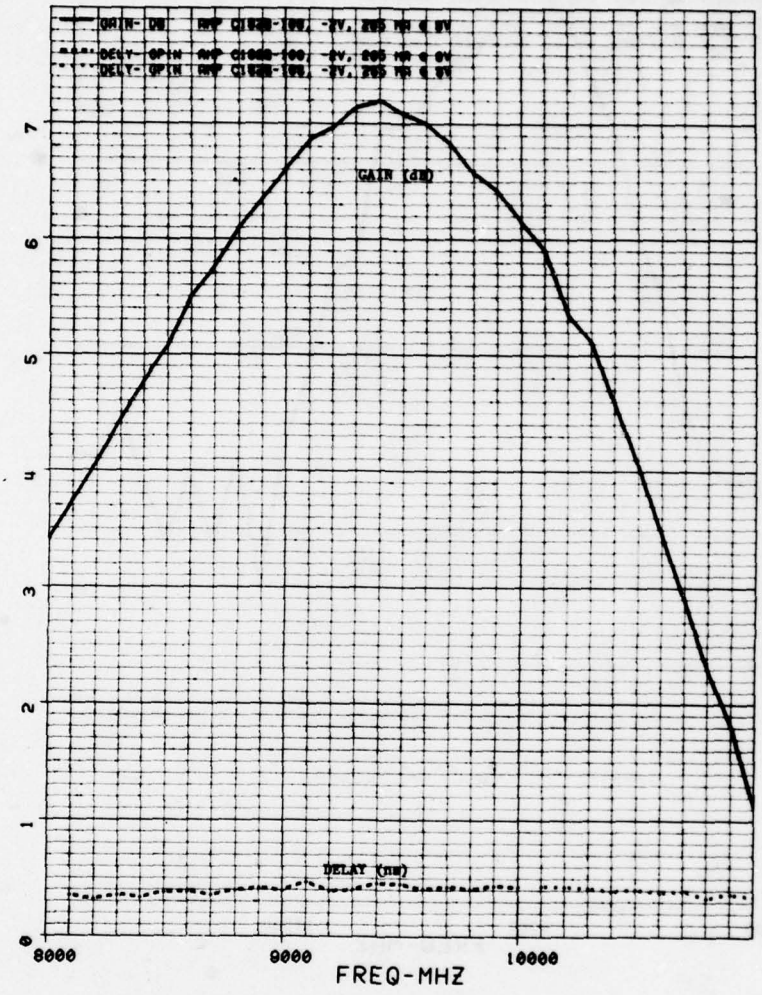


Figure 26. Measured small-signal response for an 8G single amplifier stage.

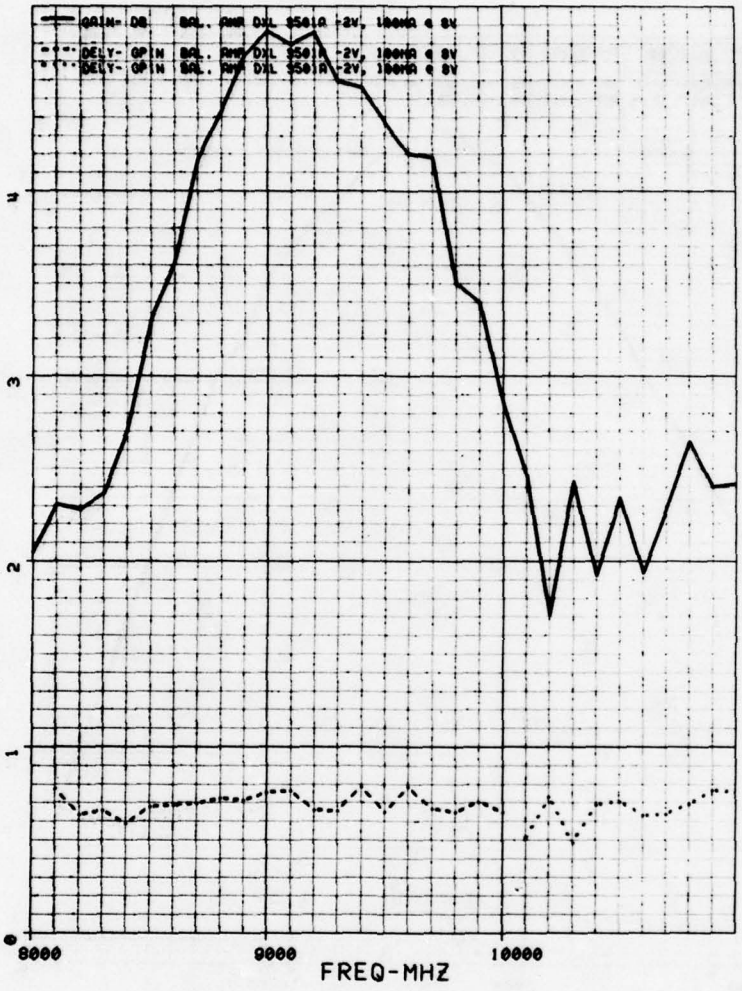


Figure 27. Measured small-signal response for Dexcel-3501A balanced amplifier stage.

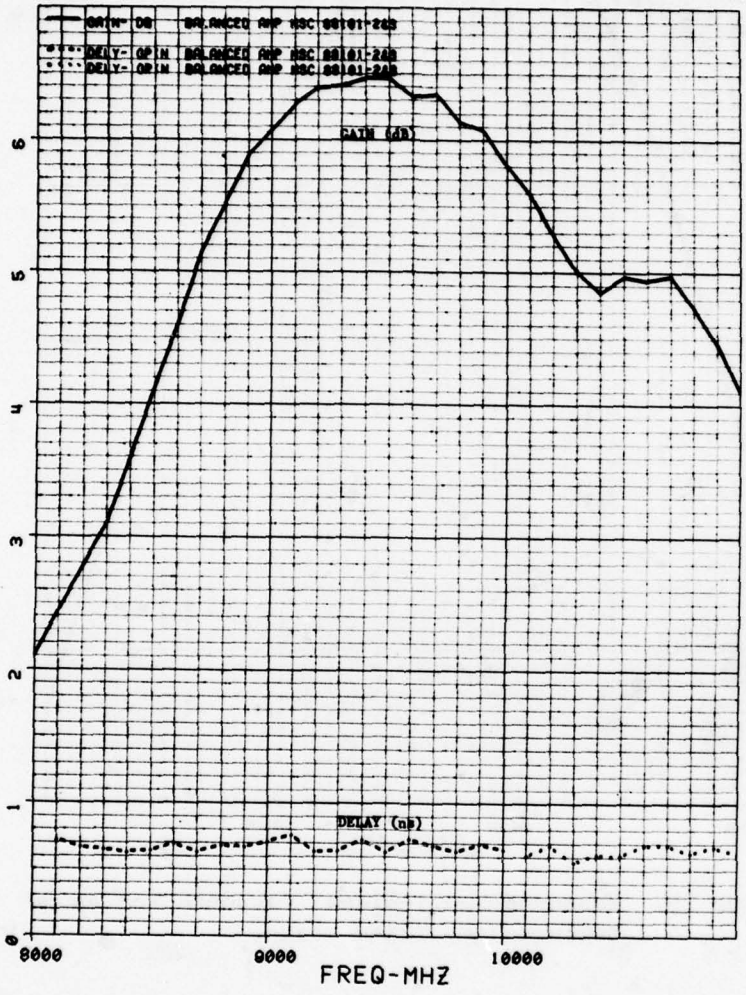


Figure 28. Measured small-signal response for a 4G balanced amplifier stage.

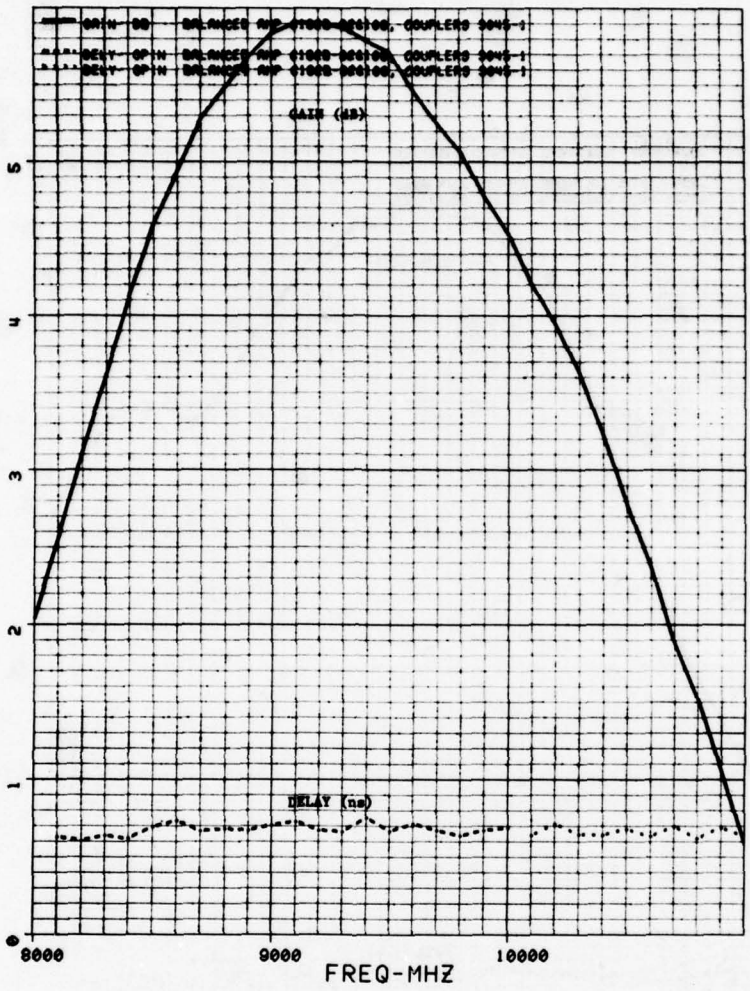


Figure 29. Measured small-signal response for an 8G balanced amplifier stage.

amplifiers with two 3-dB couplers. The power performance of these amplifiers is summarized in Table 6. Figure 30 shows the saturation characteristics of these balanced stages compared with the desired operating point as given in Fig. 1.

The first stage, utilizing Dexcel 3501A FETs, has rather poor performance compared to the original performance of the single-stage amplifiers. As reported

TABLE 6. BALANCED AMPLIFIER POWER PERFORMANCE

Device Type	Power Out (mW)	Assoc. Gain (dB)	Efficiency (%)	Small-Signal Gain (dB)
Dexcel 3501	83	4.2	7.6	5.2
MSC 88101	398	5.0	15.8	6.2
RCA C182B	589	3.7	8.0	6.4
MSC 88104	1549	1.9	7.8	4.0

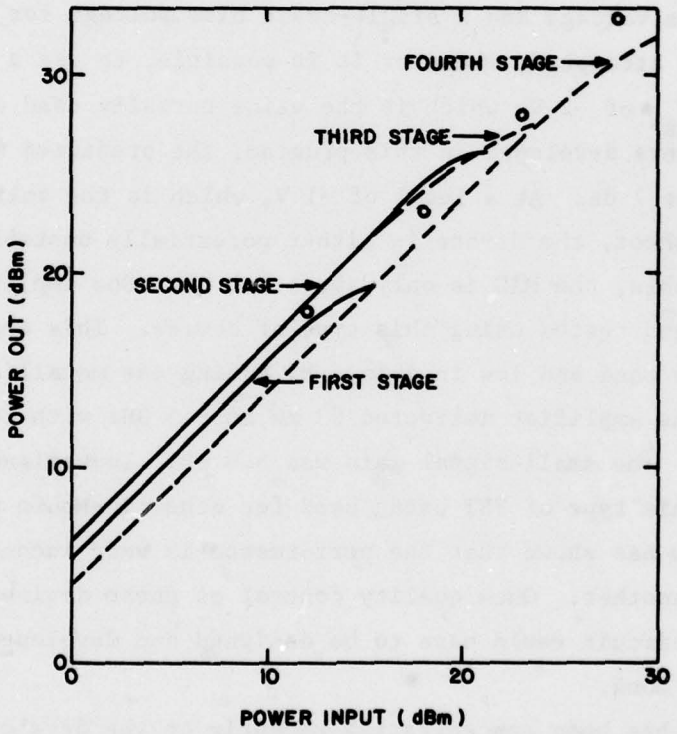


Figure 30. Saturation characteristics of the first four balanced amplifier stages.

in the Semiannual Report dated January 1978, these amplifiers had power outputs greater than 50 mW each with gains greater than 6.5 dB and efficiencies greater than 15%. However, when these amplifiers were retested several months later, it was found that they had degraded in performance, were prone to bias circuit oscillations and eventually died during testing. More amplifier units were fabricated using newer shipments of the same devices. Performance of these devices was found to be very inconsistent and unstable. Therefore, the fabricated balanced amplifier uses single-ended stages which do not have the performance of the originally developed units.

As a replacement for the Dexcel FETs, 2G FETs from MSC, type 88100, have been ordered and tested. According to the manufacturer's data sheet, these devices should have an output of 65 mW with 8-dB gain at 10 GHz. When tested for small-signal parameters, these devices were found to be unusually sensitive to gate bias voltage. In actual system applications it is desirable to use a single-gate bias voltage and a single-drain bias voltage for all the stages. Therefore we have attempted, whenever it is possible, to use a uniform bias voltage. At a V_{gs} of -2 V, which is the value normally used on all the other FET amplifiers developed in this program, the predicted maximum available gain is about 7 dB. At a level of -1 V, which is the value specified on the MSC data sheet, the device is either potentially unstable, or is unconditionally stable, the MAG is only about 7.5 dB. One amplifier stage has been fabricated and tested using this type of device. This amplifier was found to be very narrow band and low in gain. By adding one metallic chip on the drain circuit, the amplifier delivered 93 mW at 9.5 GHz with 16.9% efficiency and 4.7-dB gain. The small-signal gain was 6.0 dB. Investigation of the performance of this type of FET being used for other in-house programs at lower frequencies has shown that the performance is very inconsistent from one delivery to another. Once quality control of these devices has improved, a new amplifier circuit would have to be designed and developed for the 9- to 10-GHz frequency band.

Because RCA has been concentrating recently on the development of 8G and 18G FETs, 4G devices from MSC are now being used in the second-stage amplifiers. The units have been found to be very consistent in performance, with a typical amplifier having an output of over 200 mW with 6.5-dB gain and 20% efficiency. The performance of a balanced amplifier using these devices is an output of

400 mW with 5-dB gain and 16% efficiency. One minor shortcoming of these amplifiers is that it has been found difficult to trim the center frequency by adjusting dimensions of the interconnecting ribbons or the lengths of the stubs. A redesign of the matching networks, utilizing a different topology should overcome this difficulty.

The third stage uses RCA 8G devices from wafer C182B. The amplifiers fabricated from these devices have shown output powers of about 350 mW with about 5-dB gain and 15 to 20% efficiency. These amplifiers have been found to be very reproducible and are easily adjusted to any center frequency within the band 8.5 to 10.5 GHz.

Figure 31 summarizes the performance obtained with successive degrees of integration of the three-stage balanced amplifier shown in Fig. 6. It can be seen that, as expected, the power output remains essentially constant and the gain increases as the additional stages are placed ahead of the output stage. When this is done, no unexpected changes in frequency response occur. This is one of the principal benefits of the all-balanced amplifier approach using quadrature couplers. Each balanced stage has a vswr better than 1.7:1 across the band. With this low a vswr, the stages can be cascaded with a minimum amount of interstage interaction and detuning effects. Figure 32 shows two contours for the complete three stages. The solid contour is the response obtained with all three stages directly interconnected as shown in Fig. 6 and is the same as shown in Fig. 7. The dotted contour is for the same three stages when separately mounted as single-stage balanced amplifiers and interconnected through coaxial connectors. This shows that the effect of the two pairs of connectors amounts to about 1.5-dB loss at these frequencies.

Various other FET types have been investigated to determine their usefulness to this program at this time. For the first stage, a two-gate unit from MSC, type 88100, has been investigated. As already described, this unit has been found to give inconsistent performance from one unit to another.

Amplifiers designed for the RCA 8G FET have been found to also work well with the equivalent unit from MSC, type 88102. With a V_{ds} of 9 V, power levels of 540 mW with gains of 4.5 dB are obtained fairly consistently. Center frequencies of the responses can be shifted fairly easily.

When two 8G amplifiers using the MSC 88102 are paired with interdigitated couplers to form a balanced amplifier, a lower power level than expected is obtained. With lossless couplers, a power level of greater than 1 W should be

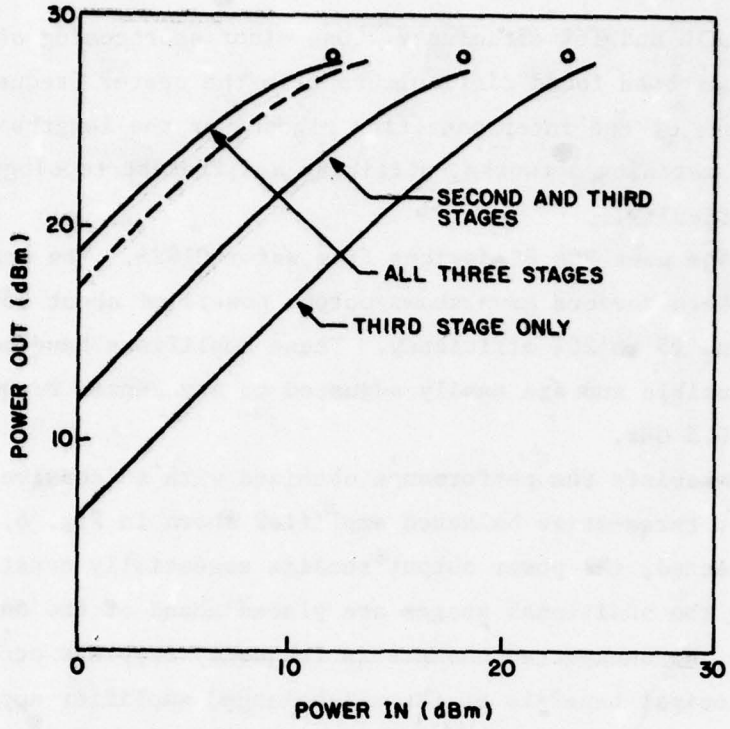


Figure 31. Saturation characteristics of the three-stage amplifier.

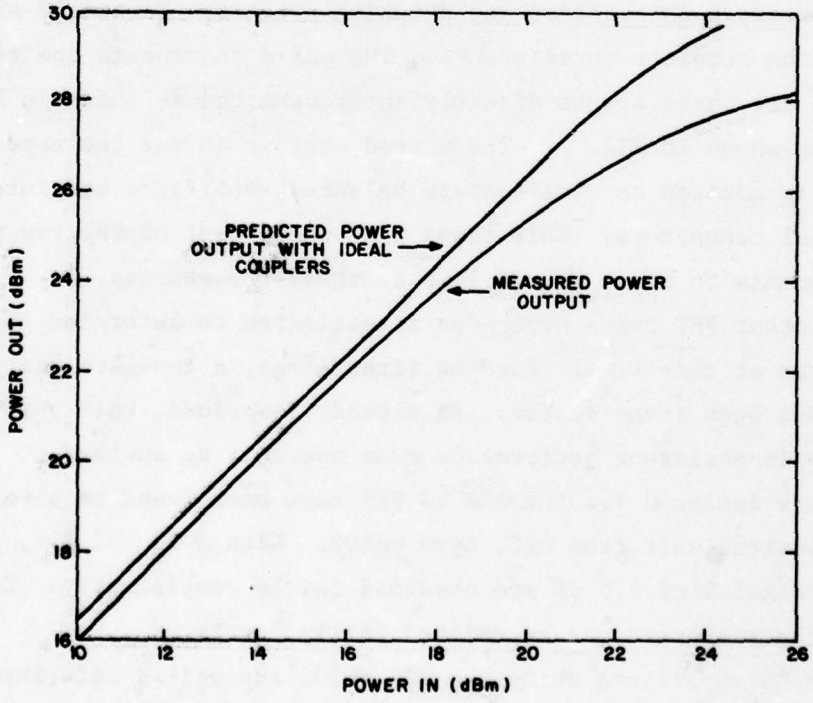


Figure 32. Saturation characteristics of a balanced 8G amplifier.

generated at 9.5 GHz. At small-signal levels, the gain of the balanced amplifier is about 0.5-dB lower than expected, indicating that each directional coupler is contributing about 0.25-dB loss. At high power levels, the gain is about 2-dB lower than expected with ideal lossless couplers as shown in the saturation characteristic in Fig. 32. This is caused evidently by the vswrs of the couplers, which at 9- to 10-GHz can be as high as 1.6:1. Apparently, what happens is that at high levels the amplifiers want to see load impedances which are different from the small-signal impedances and considerably different from the impedances presented by the directional couplers. Modifications to the directional couplers are being tried to obtain lower vswrs.

To obtain power levels of 1 W, amplifiers have been designed and fabricated using the MSC 16G FET, type 88104. These devices are specified as having a typical power output of 1 W at 12 GHz, with a minimum of 800 mW. By inspecting the measured S-parameters of several samples of this type FET, and noting the associated dc drain current with a V_{gs} of -2 V and a V_{ds} of 9 V, it is felt that most of the delivered units will meet the minimum power specification, but not the typical power of 1 W. By selecting high current devices of this type, three amplifier stages having output levels of approximately 1 W have been fabricated. It has been observed that this type of amplifier, which has essentially the same type of topology as the 8G amplifier, can be shifted in frequency fairly easily. The dress of gate bias lead has been found to be very important to the rf response of the circuit, and if improperly positioned, the swept rf response tends to break up and low-frequency oscillations occur in the gate circuit.

FETs which are rated for 2.5-W typical output at 8 GHz (MCS 88110) have also been evaluated at 10 GHz. The measured MAG is only about 1.5 dB at 10 GHz, as shown in Fig. 19, and the S_{21} gain is approximately -10 dB. Therefore, this type FET does not appear to be a suitable candidate for use in 10-GHz amplifiers at its present state of development. Higher power levels required in the immediate future would dictate that more than two amplifiers utilizing lower power devices would have to be combined. Thus, to achieve 5W at 10 GHz would require combining six 1-W amplifiers, allowing for power lost in the combining process.

Two 1-W amplifiers have been combined using interdigitated couplers. Figure 33 shows the difference between the measured saturation curve and the power output expected with lossless couplers. It can be seen that in this case, almost 1.5 dB of loss occurs even at small-signal levels, and that at higher

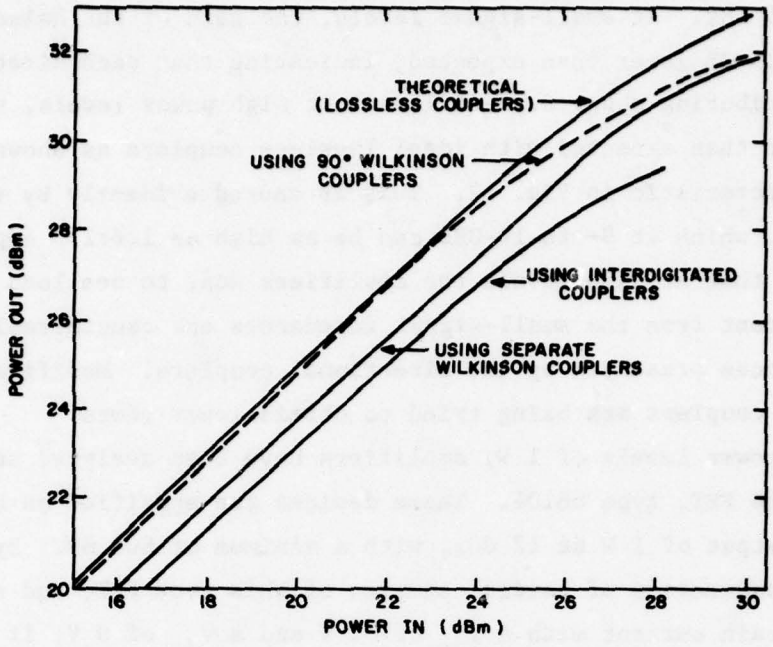


Figure 33. Saturation characteristics of a balanced 16G amplifier.

levels the loss is greater than 2 dB. The maximum output power from the combined units is only 1 W, which is the power delivered by either one of the two amplifiers. Suspecting that the directional coupler mismatches are the major cause of this premature saturation, combining with Wilkinson-type combiners has been tried. These combiners are packaged with SMA type connectors, and thus the individual single-ended amplifiers also had SMA connectors attached for this test. Figure 33 shows the measured saturation response. The gain is now approximately 1-dB less than expected from ideal lossless couplers, and a power level of 1.6 W is now achieved from this balanced amplifier. The Wilkinson combiners used have vswrs less than 1.2, isolation greater than 25 dB, and losses less than 0.3 dB when measured separately. An integrated package for the fourth stage has been made combining two 1-W amplifiers with Wilkinson combiners which are offset to achieve a quadrature coupling effect over the band of interst. These couplers have minimal effect on the small-signal loss as shown in Fig. 33. The 1.5-W level is now reached with 2.7-dB gain and 10.1% efficiency.

This fourth stage has been added to the three-stage module to achieve a power output of 1.38 W with 19.4-dB gain as detailed in the introduction of this Section.

The measured amplifier performance at 9.5 GHz for four different FET types from MSC is summarized in Fig. 34. The solid symbols indicate the typical performance at 10 GHz given on the manufacturer's data sheet, while the clear symbols show the measured amplifier performance for a number of units. A general trend is seen in that amplifiers which have power outputs close to the expected values, have gains which are lower than specified. Units which have high gain, have much lower powers. In the case of one 16G amplifier, and one 8G amplifier, the performance is so poor that they respectively look like an 8G and a 4G device, respectively. Of course, the efficiencies are very poor in these cases.

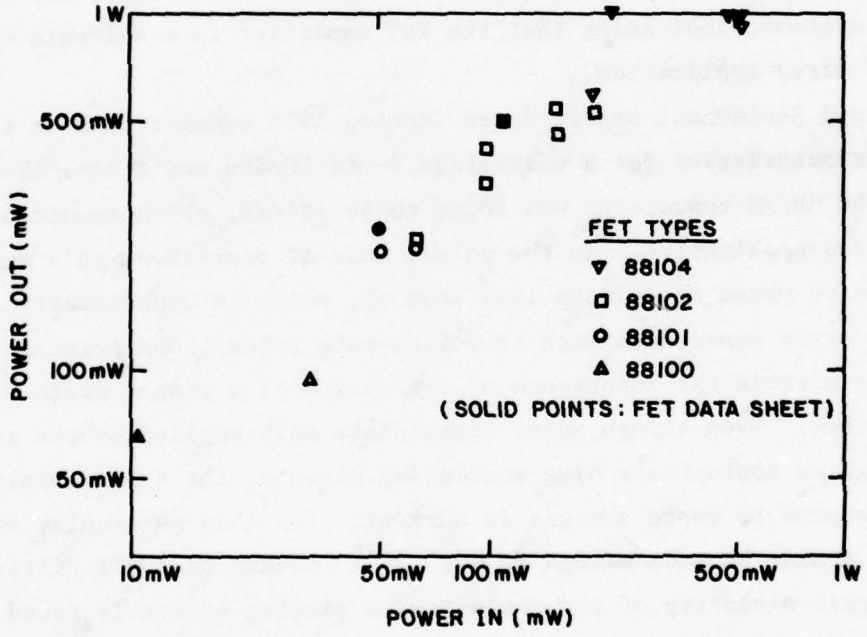


Figure 34. Measured amplifier power performance at 9.5 GHz and FET data sheet typical performance at 10 GHz.

H. PHASE CONSIDERATIONS

A major portion of this program concentrated on determining the pulsed phase characteristics of FET power amplifiers to determine their suitability

to an airborne phased array radar application. This entailed the fabrication of amplifiers suitable for efficient pulsed operation, the development of an accurate phase transient characterization technique, and the evaluation of both single-ended and single-stage amplifiers and of a complete amplifier module.

The first Semiannual Report dated May 1977 details the results obtained with single-stage amplifiers of various types. A phase measurement bridge was developed which permits the evaluation of FETs in both the cw and pulsed mode of operation. The sensitivities of amplifier phase responses were determined as a function of drain voltages, gate voltages, load mismatches, temperature, and drive level for various FET types in both cw and pulsed modes. This same phase bridge was also used to accurately determine the phase transient of the various amplifier types with both gate voltages and rf voltages simultaneously pulsed, and the rf only pulsed. In all cases, the rf phase responses were found to be better than miniature traveling-wave tubes currently used in phased array systems, indicating that the FET amplifier is a suitable candidate for the phase array application.

The second Semiannual Report dated January 1978 concentrated on the AM/PM conversion characteristics for a multistage 9- to 10-GHz amplifier. In the worst case, the AM/PM conversion was found to be $\pm 3°$/dB, which is acceptable for the intended application. In the pulsed mode of operation, this amplifier was found to have phase transients less than 5°, which is considerably less than the $\pm 10°$ error associated with traveling-wave tubes. One principal discovery of this work is the importance of the design of a proper drain bias filtering network. Even though pulse signals are only applied to the gate bias network through an appropriate bias modulating circuit, the drain supply is required to respond to rapid changes in current. For this particular amplifier, a change of 1 A must be made within 20 ns. If a conventional RFI filter is used in the drain circuitry of the amplifier, a ringing effect is found in both the drain current and phase response of the amplifier. This ringing occurs at approximately 400 kHz which is the resonant frequency of the RFI filter. The series inductance associated with the filter resists the rapid change in current demanded by pulsed operation of the FET. To eliminate this ringing effect, the drain filtering network must be designed with no series inductance. Thus, a better filter network would consist principally of capacitive standoffs. The

charge stored in these capacitors would thus provide the sudden increase in current needed when the FETs are pulsed on. Experiments with a single-stage amplifier have demonstrated the superior effectiveness of this type filtering network in suppressing ringing effects.

In the final months of this program, initial turn-on and turn-off transients which appeared to be caused by the amplifiers being tested, were identified as phase bridge measurement errors. The turn-on transients have been determined to be caused by slight differences in the lengths of the two arms of the bridge. During the 40-ns rise-time of the incident rf pulse, the rf levels in the two arms are at slightly different levels, so that a voltage appears at the differential amplifier output of the bridge. After the rf pulse is fully turned on, both are at the final rf level so that the transient disappears. Sharp transients which appear at the turn-off edge of the pulse have been determined to be characteristic of the detectors used at the bridge output.

This phase investigation has shown that up to the 0.5-W levels, FETs are suitable devices for the intended phased array application. Although the measured phase sensitivities and phase transients are sufficiently low, further investigation is still needed in certain areas. More amplifiers should be built so that unit-to-unit variations can be accurately determined. Assuming that the phase properties are found to be reproducible, all amplifiers in a given array could then be operated from common voltage supplies and on a common heat sink. Thus, as voltages and temperatures vary, all the amplifiers in the array would have an identical phase variation, and the beam would continue to be aimed in the same direction. With this technique, uncorrelated phase shifts of the component amplifiers would become correlated.

In this program, it was learned that the phase sensitivities to gate voltage variations decrease and the sensitivities to drain voltage variations increase as larger-area, higher-power devices are used. This phenomenon is not understood at the present time. Determining the cause of these effects could lead to criteria for the design of FETs optimized for best phase performance.

The relative merits of gate pulsing and drain pulsing are better understood as a result of this program. At the beginning of this program, gate-pulsing techniques were selected as the apparently better technique. Because essentially no current is required by the gate of an FET, a pulse modulator

circuit can utilize simple compact circuitry and have potentially high speed. A drain-pulsing approach would require a modulator circuit having high current capability. The overall efficiency would be degraded because it would be the product of the modulator efficiency and the rf amplifier efficiency.

Disadvantages of the gate pulse-modulating approach became apparent during this program. In gate pulsing, the FETs are switched between a low negative voltage in the "on" state and a higher negative voltage in the "off" state. This higher voltage does place an electrical stress on the gates of the FETs. During the "off" state, the FET might typically have a drain voltage of 8 to 10 V, and gate voltage of -6 V. With a high-level rf signal superimposed onto this, the FET is required to have a gate-to-drain breakdown voltage in excess of 20 V. This device restraint must be satisfied without compromise to rf performance. To satisfy these requirements during this program, devices having both high breakdown voltages and good rf performance were selected. This resulted in some sacrifice in power-added efficiency. In general, however, these simultaneous requirements are not conflicting, and it should be possible to consistently fabricate FETs which can have both good rf performance and high breakdown voltage.

For gate pulsing to be effective, the FET must have a good pinchoff when the "off" state voltage is applied. This is necessary to maintain a good overall efficiency.

It has become apparent that the principal advantages of a drain-pulsing technique would be that it does not have the disadvantages of gate pulsing. In drain pulsing, the "on" condition occurs when the drain voltage is at its normal 8- to 10-V range. The "off" condition is obtained by switching the drain supply off to a 0-V condition. With this mode of operation, no extraordinary breakdown voltage restriction is imposed on the FET, and there is no stress in the "off" state. Drain pulsing also has the advantage of consistently providing a high on/off ratio and a high rf amplifier efficiency independent of the pinchoff characteristics of the FET.

Therefore, this program has shown that gate pulsing requires tight controls on FET parameters in order to simultaneously satisfy the requirements of good rf performance and efficient pulse operation. At first, it seemed clear that gate pulsing is the more desirable approach, but now a more careful examination of the merits of both approaches is required.

This investigation of pulsed operation of FET amplifiers has resulted in the publication of a paper entitled, "Phase Characteristics of I-Band Pulsed Gate GaAs FET Power Amplifiers," (see the Appendix) at the 1978 IEEE International Microwave Symposium held in Ottawa, Canada. This paper was so well received that it was reviewed in a special article in MICROWAVE MAGAZINE in the July 1978 issue, and by special invitation, it was presented to an informal workshop at the 1978 European Microwave Conference held in Paris, France.

I. 3-dB COUPLERS

During the course of this program, much attention has been paid to the 3-dB couplers required to form balanced amplifiers. The principal coupler type examined is the interdigitated type. Such couplers had been designed for this frequency band before the start of this program. These couplers were, however, fabricated on rather large substrates of 20.3 mm x 12.7 mm x 0.64 mm. Extensive modifications have been made to the layout of the 50-ohm microstrip lines which interconnect the coupler to other circuits to reduce overall coupler size. Compared to the Wilkinson couplers, the interdigitated types we fabricated are more sensitive to the angle between the 50-ohm lines and coupling section, to the placement of any bends in the lines relative to the coupler and the connectors, and to the location of the 50-ohm lines relative to the edge of the substrate. The performance of the current version of interdigitated couplers designed for the 9- to 10-GHz frequency range is summarized in Figs. 35 to 37. These units, when tested with an internal high-power cermet resistor developed and fabricated by RCA, have measured insertion losses better than 0.5 dB, maximum vswrs of approximately 1.6:1, and isolations greater than 18 dB.

When these couplers are used with a pair of amplifiers to form a balanced amplifier stage, several effects are noted. The overall small-signal gain is approximately 0.6-dB less than what would be expected with ideal lossless couplers, indicating that the true loss of each coupler is only about 0.3 dB. However, as discussed in previous sections, some balanced amplifiers saturate sooner than expected as larger drive levels are applied. This is apparently caused by the 1.6:1 vswr associated with the terminated coupler. Continued modifications should be made to the coupler to improve its vswr.

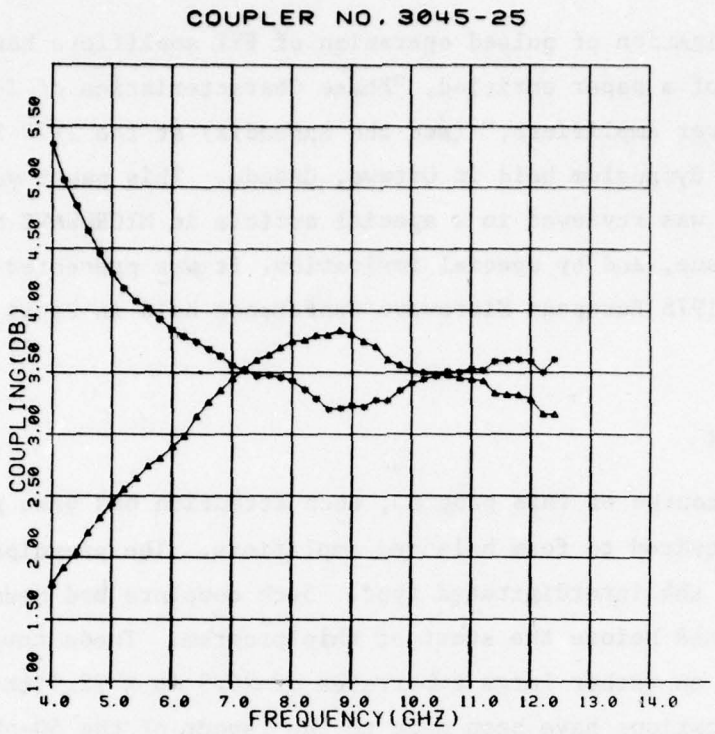


Figure 35. Measured coupling for an interdigitated coupler.

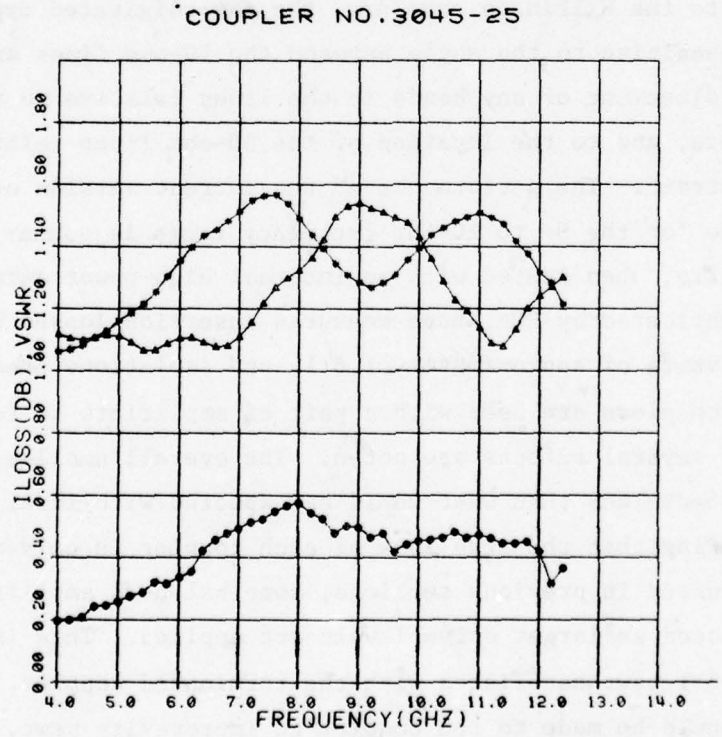


Figure 36. Measured vswrs and loss for an interdigitated coupler.

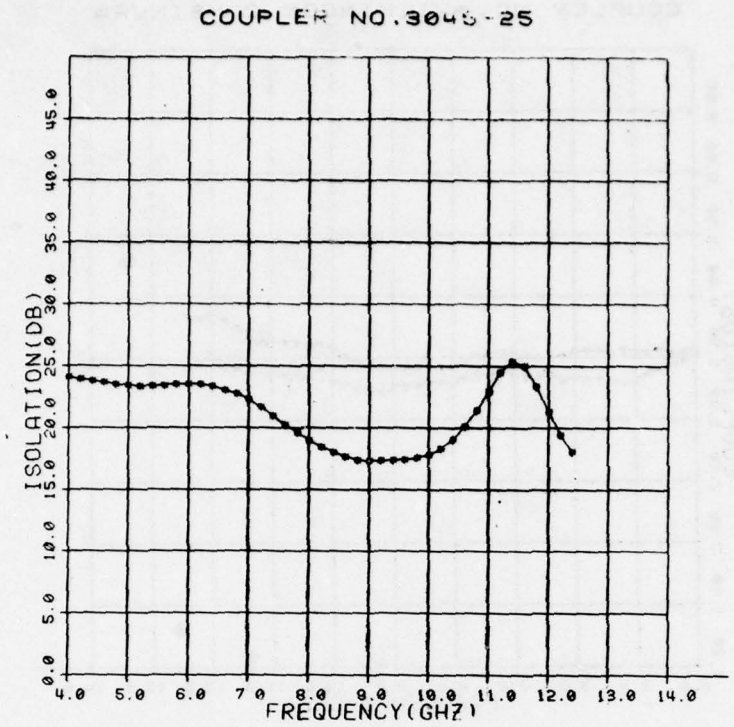


Figure 37. Measured isolation for an interdigitated coupler.

The Wilkinson-type 3-dB coupler has been developed with good performance in the band of interest. Figures 38 through 40 show the measured data for a unit designed for 9.5-GHz operation. It can be seen that although these combiners are designed for the 9- to 10-GHz band, they are usable over the full 4- to 12-GHz frequency band of measurement. Over the band of interest, the loss is less than 0.4 dB, the vswrs less than 1.2:1, and the isolation greater than 25 dB. When two such combiners are cascaded into a divider-combiner configuration, the overall loss is approximately 0.75 dB.

Normally, the interdigitated coupler is the preferred type for fabrication of balanced amplifiers. This type coupler is a quadrature type, which ensures low interstage mismatches when identical amplifiers are combined. This minimizes any interstage interaction and detuning effects which might occur when several stages are cascaded. The interdigitated coupler also has very low vswrs and very high isolation at lower frequencies. This is a very desirable feature when combining amplifiers which may have very high gain at these lower frequencies. When using combiners which do not have these features, it is possible

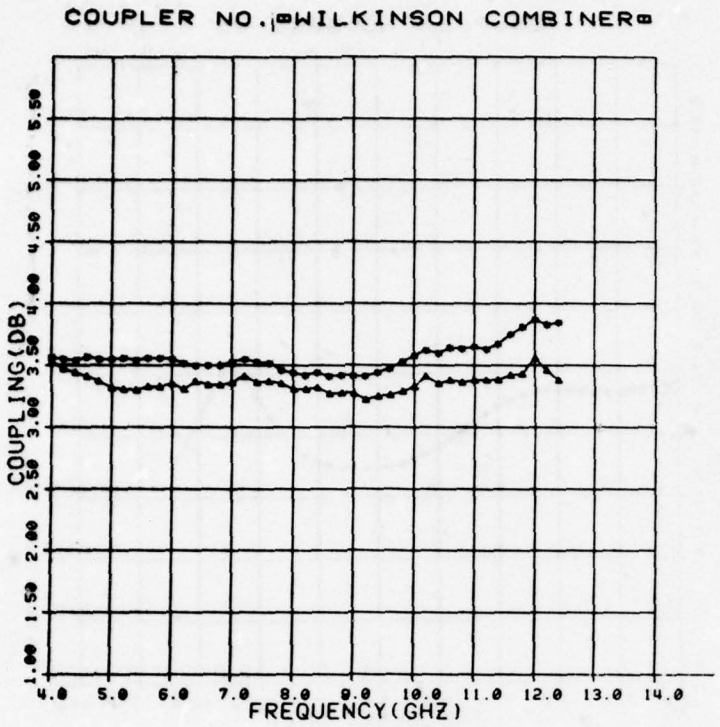


Figure 38. Measured coupling for a Wilkinson coupler.

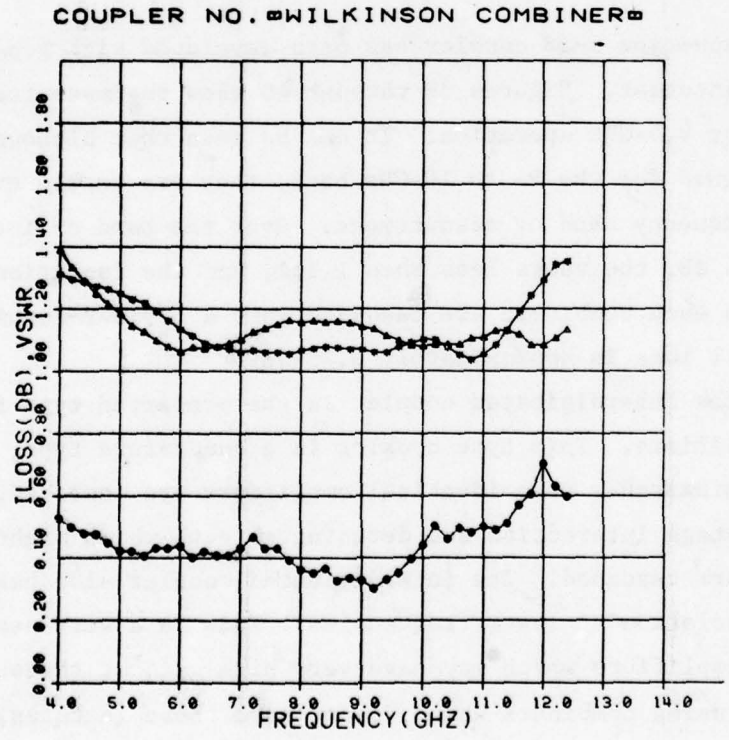


Figure 39. Measured vswrs and loss for a Wilkinson coupler.

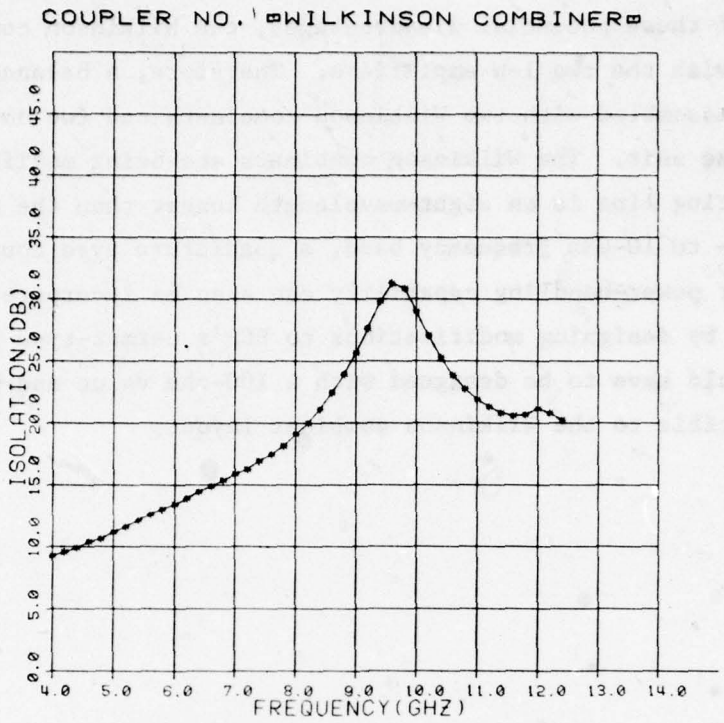


Figure 40. Measured isolation for a Wilkinson coupler.

that amplifiers which are stable when tested in a 50-ohm system, may oscillate at lower frequencies when combined to form a balanced amplifier.

Because of the premature saturation problems which may be caused by the higher mismatch problems of the interdigitated couplers, amplifiers have been combined utilizing two Wilkinson combiners. As shown earlier in Fig. 34, greater power output at higher drive levels has been obtained in this way. However, one of the disadvantages of this approach is that the Wilkinson combiner is normally an in-phase type. Therefore, mismatches associated with the component amplifiers of a balanced amplifier are not directed to the internal termination, but instead appear at the overall input and output of the amplifier. Another potential disadvantage of the Wilkinson combiner is that its internal termination is connected between two microstrip lines rather than having one end attached directly to ground. This means that the termination is not as well heat-sinked, and thus may have a significantly lower power dissipation capability.

In spite of these potential disadvantages, the Wilkinson combiner has performed well with the two 1-W amplifiers. Therefore, a balanced amplifier stage is being assembled with two Wilkinson combiners and two amplifiers packaged into one unit. The Wilkinson combiners are being modified so that one interconnecting line is an eight-wavelength longer than the other, so that over the 9- to 10-GHz frequency band, a quadrature type coupler is obtained. Greater power-handling capability can also be incorporated into future versions by designing modifications to RCA's cermet-type resistor. The resistor would have to be designed with a 100-ohm value and with dimensions which are compatible to the Wilkinson combiner layout.

SECTION IV

DEVICE DELIVERIES

During the course of this program, four deliveries of ten devices each and one delivery of fifteen devices were made. Complete data sheets showing the rf performance of the mounted devices as function of drive level have been delivered with the devices. A summary of the characteristics is tabulated in Table 7.

TABLE 7. CHARACTERISTICS OF DELIVERED FET DEVICES

Device No.	Power Out (mW)	Gain (dB)	η_{PA} (%)	Gain (Small Signal) (dB)
4G Two-cell FETs tested at 8 GHZ				
B327B-112	209.4	4.5	6.7	6.0
-113	243.9	5.2	8.2	6.3
-147	211.8	4.6	5.2	5.7
-294	327	5.0	16.8	5.9
-33	256	3.9	15.7	5.95
16G FETs tested at 8 GHz				
B642 -20	540	3.26	7.9	6.32
-22	580.5	2.32	6.2	6.07
-23	621	6.62	7.5	6.40
-26	594	2.42	8.33	6.48
-30	600.75	2.47	9.16	6.48
3147 -1	1490	3.4	14.6	4.6
-4	1282.5	2.8	12.05	5.0
-6	783.0	2.7	26.27	5.2
-7	1039.5	3.09	9.79	4.18
-8	1053	3.15	11.11	5.43

TABLE 7. CHARACTERISTICS OF DELIVERED FET DEVICES (Continued)

Device No.	Power Out (mW)	Gain (dB)	η_{PA} (%)	Gain (Small Signal) (dB)
16G FETs tested at 8 GHz (Continued)				
B390-11	417	5.0	7.2	5.4
-29	315	4.3	15.2	4.7
-30	220	3.3	3.7	3.3
-32	298	4.0	9.3	4.1
2975-72	393	4.7	9.75	5.4
B620-5	761.6	3.14	10.6	5.07
-9	654.5	2.48	6.43	4.62
-11	737.8	3.00	12.1	4.96
-17	714.0	2.85	11.88	3.68
-18	821.1	3.46	15.16	5.18
-26	642.6	2.40	6.48	4.66
-32	773.5	3.20	11.36	4.97
-33	654.5	2.48	9.05	3.97
-34	749.7	3.07	12.10	4.96
-40	690.2	2.71	7.38	4.85
8G FETs tested at 10 GHz				
3172A-8	670	2.69	10.0	4.28
-21	562.8	1.93	10.9	4.28
-23	549.4	1.81	8.9	5.35
-27	623.1	2.38	18.1	5.05
-42	589.6	2.12	10.6	3.6
-55	623.1	2.38	14.6	3.76
3149-1	602	3.68	18.9	4.76
-3	504	2.91	22.2	5.58
-4	588	3.58	24.6	6.27
-11	385	1.74	7.3	2.91
-15	504	2.91	15.6	3.93
-25	434	2.26	10.3	4.32
-26	462	2.53	11.4	4.16
-28	420	2.12	9.1	3.05

TABLE 7. CHARACTERISTICS OF DELIVERED FET DEVICES (Continued)

Device No.	Power Out (mW)	Gain (dB)	η_{PA} (%)	Gain (Small Signal) (dB)
8G FETs tested at 10 GHz (Continued)				
B642-24	770	3.50	10.5	6.43
-41	644	2.72	7.56	5.92
Unmounted 8G FETs - dc testing only				
3172A-41				
-50				
-53				
-75				
C131-6				
-7				
-8				
-9				
-10				

SECTION V

FET RELIABILITY

Six 8G FETs from wafer B681 and utilizing AuGe contacts and a Ti/Pt/Au metallization system have been put on accelerated life tests. In these high-temperature, dc-only life tests, each transistor dissipates 2 W of dc power while in an oven at 165°C. The resulting transistor channel temperatures are 250°C. The failure times for these six units are shown in Fig. 41. Two transistors failed relatively early, and thus their significance is discounted as being premature. The remaining four transistors failed due to the same mechanism, namely a decrease in the drain current. The MTTF for this failure mechanism is therefore 2000 hours at a channel temperature of 250°C. The standard deviation is 0.26. Therefore, at a normal operating channel temperature for the transistor of approximately 130°C, the MTTF becomes 10^6 hours, assuming a conservative value of 1 eV for the activation energy.

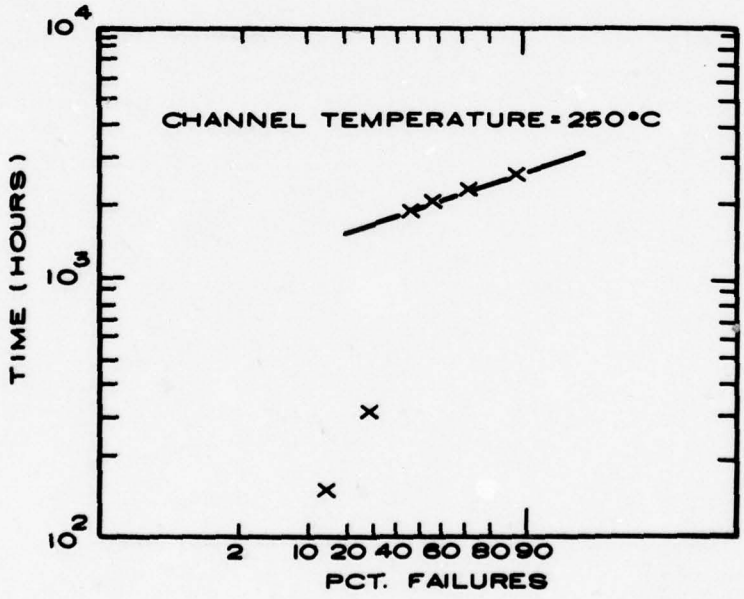


Figure 41. dc-Biased life-test data at 250°C. MTTF = 2000 hours at 250°C/ standard deviation = 0.26.

These preliminary results are being supplemented by an RCA in-house program. In this program, a computer-controlled life-test system is being set up which controls the dc-bias voltages and measures the dc I-V data of many devices automatically. Life-test stations have also been established for the determination of failure rates in the presence of simultaneous application of both dc and high-power rf drive.

SECTION VI

SUMMARY

This final report has summarized the results achieved in a 21-month research program (including a 3-month no-cost extension) to develop an amplifier module suited to airborne active array radar applications. During the course of this program, advances have been made in the areas of GaAs substrate preparation, design of new FET types having improved performance, fabrication of amplifiers having greater than 1-W output over the 9- to 10-GHz frequency range, and development of pulse-phase characterization techniques which demonstrate the suitability of power FET amplifiers for a pulsed phased array.

In the preparation of GaAs wafers, two new reactors have been designed and fabricated under company sponsorship. RCA now has three $AsH_3/Ga/HCl/H_2$ (hydride), and one $AsCl_3/Ga/H_2$ (trichloride) reactors. Improvements incorporated in the newer reactors proved to be so beneficial that the original reactors have been modified to include these same modifications. These reactors have been used extensively in a program to develop improved buffer layers on GaAs substrates suitable for FET fabrication. Cr-doped buffer layers have been developed with excellent surface morphology, voltage breakdowns in excess of 1500 V and resistivities of about 10^7 ohm-cm. Undoped buffer layers have been grown using the two-buffer $AsCl_3$ system and resistivities of about 10^5 ohm-cm have been achieved.

In the course of this program, new power FET types have been developed which achieve greater power levels than had previously been available. FET designs are designated by the number of parallel interconnected gates. Thus, a unit having eight parallel gates, designated as an 8G type, has achieved a power of 854 mW at 10 GHz with over 28% power-added efficiency. Two 8G units connected in parallel on the same carrier have achieved greater than 1.3 W. Power levels greater than 1 W have also been achieved in a single device by a 16G and an 18G design. At lower frequencies, a 32G design has achieved 1.8 W at 8 GHz and a large 48G FET has demonstrated over 4 W of output at

4 GHz. These two larger power devices have to be evaluated at lower frequencies because the gain at 10 GHz is too low. This improved performance is also the result of developments during the course of this program in the following areas of device fabrication:

- An innovative continuous gate geometry having greater power output, gain, and efficiency, and utilized in the 8G and 18G devices.
- A Ti/Pt/Au refractory metallization system is now possible because of our incorporating new compatible evaporation and etching techniques. This results in a considerably more reliable device.
- An Ni/AuGe/Ni sintered ohmic contact technology has been developed which permits good quality source and drain contacts to be realized with wafers from all four reactor systems.
- A new automatic flip-chip system which permits the rapid mounting of many FETs onto the copper pedestals in a reliable, consistent manner.

Balanced amplifier stages have been fabricated which can be cascaded to form a four-stage amplifier having greater than 1-W output power. The lowest level stage utilizes Dexcel 3501 FETs to generate 83 mW, a 4G stage generates 398 mW, an 8G stage generates 589 mW and a 16G stage generates 1.55 W, all at 9.5 GHz. The first three stages have been cascaded in a single package to achieve an output of 590 mW with an associated gain of 15.7 dB. When the separately packaged fourth stage is connected after this three-stage module, an output of 1.38 W with a gain of 19.4 dB and an overall efficiency of 10.1 % is obtained.

The phase characteristics of pulsed gate GaAs FET power amplifiers have been extensively characterized using a phase bridge developed with standard waveguide components. The sensitivities of different FET types to changes in gate voltage, drain voltage, load mismatches, temperature, and drive level have been measured. Intrapulse and interpulse phase variations have been evaluated with the rf only being pulsed, and with both rf and gate voltages being pulsed. In all cases, it has been found that the phase characteristics of FETs are superior to miniature traveling-wave tubes used in phased array

applications. It has therefore been demonstrated that the power FETs usable in the 9- to 10-GHz frequency band are suitable for the intended airborne phased array radar application.

Six 8G FETs have been subjected to dc-biased-only life test at an effective channel temperature of 250°C. The MTTF has been determined to be 2000 hours under these conditions. This is equivalent to an MTTF of 10^6 hours at a normal operating temperature of 130°C.

Fifty-five power FETs of the 4G, 8G, and 16G varieties have been delivered to NRL for evaluation by the customer. Complete data sheets showing the rf performance of the mounted devices as a function of drive level have been included in the deliveries.

APPENDIX

PHASE CHARACTERISTICS OF I-BAND PULSED GATE GaAs FET POWER AMPLIFIERS*

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ABSTRACT

The measured phase sensitivities and transients of FET power amplifiers having pulsed gate voltages are very low and are suitable for phased array applications. Gate pulsing requires that the FETs have good rf performance and a drain-to-gate breakdown voltage large enough to support the sum of the gate voltage, drain voltage, and maximum rf voltage swing.

Introduction

In pulsed phase array applications, such as airborne radar, both amplitude and phase characteristics of microwave amplifiers must be precisely known under pulsed conditions. Moreover, the differential phase shift obtained between amplifiers must be held within controlled limits to ensure minimum error in a phased array. Power FET amplifiers, which have recently become available for application at I-band frequencies (8-10 GHz), and which have significant advantages in terms of potential reliability, low voltage operation, low noise, and size and weight, have not previously been considered for these applications because suitable techniques for pulsing such amplifiers had not been developed. Furthermore, the intrapulse and interpulse phase properties of such amplifiers have not been studied.

This paper will present the phase sensitivities of several amplifier stages using different FET geometries as a function of gate voltage, drain voltage, VSWR, temperature, and rf input level under both cw and pulse conditions. The amplitude and phase characteristics of a complete five-stage amplifier including special pulse modulation biasing circuitry will be described. It will thus be shown that the microwave power FET amplifier is suitable for pulsed phased array systems.

Pulsing Techniques of FET Amplifiers

To maintain high efficiency during pulsed rf conditions, the dc power supplied to the amplifier must be pulsed on only when rf signal is present. This is achieved in a FET amplifier by pulsing the drain current.

The FET drain current can be controlled by changes in either the gate or drain voltage. In gate pulsing, the gate voltage is switched between a low negative voltage which results in efficient rf power amplification and a higher negative voltage near the pinchoff voltage of the FET which effectively turns off the drain current. In drain pulsing, the drain voltage is switched between the level needed for efficient power amplification and zero volts. Drain pulse bias modulation circuitry must handle large currents and because losses of drain modulation degrade overall amplifier efficiency, amplifiers were fabricated using gate pulsing. It was found however that gate pulsing requires that the FET meet dc voltage breakdown limits and rf performance levels which are difficult to satisfy simultaneously. The drain-to-gate breakdown voltage must be large enough to support the sum of the drain voltage, the gate voltage, and the peak rf voltage; this sum can be as high as 15 to 20 volts. The tradeoffs between gate and drain pulsing must be investigated further.

*This work has been partially supported by the Air Force Aeronautical Systems Division under Contract F33615-76-C-1122 and by the Naval Research Laboratory under Contract N00173-76-C-0383.

Phase Sensitivities

It is necessary to determine the variation in phase shift of pulsed FET amplifiers as a function of gate voltage, drain voltage, temperature, load variations, and drive levels. Under cw conditions, these can readily be determined with a special automatic network analyzer system which incorporates a system of step attenuators under computer control to permit vector measurements under varying high power levels. To permit similar measurements during both pulsed and cw conditions, a special phase measurement bridge was set up using standard waveguide components as shown in Fig. 1. The output of this bridge is provided by a

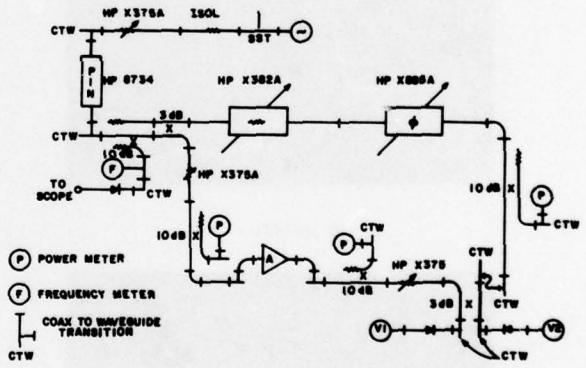


Figure 1. Pulsed phase measurement bridge.

pair of hybrid-coupled detectors driving a differential amplifier oscilloscope plug-in. This arrangement provides a well-defined high sensitivity null which does not require equal power levels in each arm of the bridge. Nulls are achieved and vertical sensitivities in degrees/division are determined by adjustment of the calibrated waveguide phase shifter.

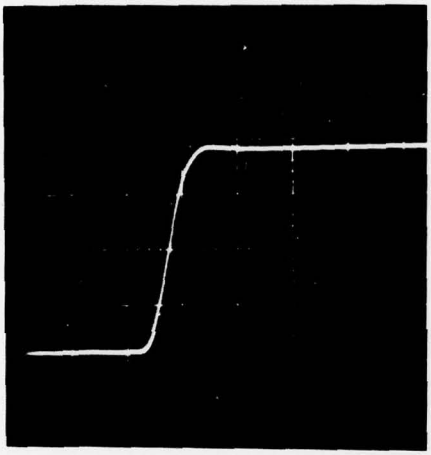
The phase sensitivities of single stage amplifiers using different type FETs have been measured with the phase bridge. The pertinent characteristics are summarized in Table 1. It is seen that the phase sensitivity to the gate potential is greatest for small signal devices while the sensitivity to drain voltages is greatest for the large signal devices. These data show that the greatest amount of voltage regulation is needed at the gate.

Transient data can readily be determined even when

TABLE 1. FET Amplifier Stage Phase Sensitivities

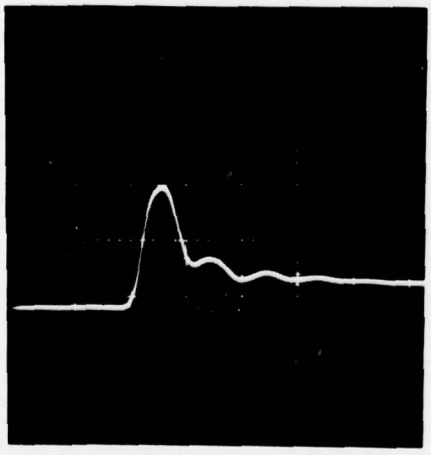
	Number of Parallel Gates		
	2	4	16
Gate Width (μm)	300	600	2400
$\Delta\phi/\Delta V_{drain}$	± 1°/V	- 2°/V	- 3°/V
$\Delta\phi/\Delta V_{gate}$	12°/V	8°/V	6°/V
$\Delta\phi/\Delta$VSWR		6°	
$\Delta\phi/\Delta T$		0.66°/°C	

both rf and gate voltages are pulsed. Typical turn-on responses are shown in Fig. 2. Figure 2a shows the amplitude response with the rf pulse and gate voltage turned on simultaneously. The amplitude reaches its final response within 40 nsec. This response is identical to that of the input rf pulse. The phase transient response is shown in Fig. 2b when the trailing edge of the pulse (not shown) is set to zero degrees. After an initial overshoot of 7° (caused by small length differences in the arms of the phase bridge) the phase shift 60 nsec after pulse turn-on is 1.5°.



20 mV/ div.

(a) 40 ns/div.



2.5°/ div.

(b) 40 ns/div.

Figure 2. Pulse responses of a 4-gate single cell amplifier: (a) amplitude response; (b) phase response.

Multi-Stage Amplifier Phase Responses

A five-stage FET amplifier including pulse modulators in the gate bias circuitry has been fabricated. This amplifier has an output of 500 mW with over 27 dB gain covering the 9-10 GHz band. A schematic representation of the overall FET amplifier bias and video pulse circuitry is shown in Fig. 3. Only the last two stages are pulsed; in the absence of rf drive, this reduces dissipation by 70%. These two stages are cut off with -4 V applied to the gates. The output stage is turned on with a -1.5 V gate bias while the preceding stage requires 0 V. These different voltages are generated by the pulse modulation circuitry.

To determine the amplifier suitability to phase array applications, extensive testing has been done under three different modes of operation, namely, cw, pulsed rf, and pulsed rf during pulsed gate bias. The cw performance of the amplifier at the center frequency of 9.5 GHz is summarized in Fig. 4. The FET amplifier shows virtually identical performance under pulsed rf conditions as shown in Fig. 5. These measurements are made with an rf pulse width of 100 μsec at a duty cycle of 50%. The AM/PM ranges from +3.5°/dB to -2°/dB at 9.5 GHz. At 9.0 GHz, the AM/PM conversion is ±2°/dB and at 10 GHz the AM/PM conversion is negligible. When operated with pulsed gate voltages and pulsed rf, even lower AM/PM conversion is obtained.

Phase transients during pulsed rf-pulsed gate voltage operation were evaluated with the following test conditions: (1) gate and rf pulses turned on simultaneously; (2) 100 μsec pulse width for both gate and rf; (3) 50% duty cycle; and (4) the phase bridge balanced for a null at the turn-off edge of the rf pulse permitting intrapulse incremental phase shifts to be accurately measured. The drain current to the complete amplifier during the on-time is slightly less than 1 A. Because this must be provided within 20 nsec rise time of the amplifier, the drain supply circuitry must be able to tolerate a switching current transient of 50 A/μsec. It was found that the EMI filter type of feedthroughs typically used at bias circuit connection points are not suitable for pulsed applications because they resist rapid current changes and cause drain current ringing at a 400 kHz rate. When this ringing is removed from the measurements, the intrapulse phase shift is found to be under 5°.

Conclusions

The measured phase sensitivities and transients of FET power amplifiers with pulsed gate voltages are very low. FET amplifiers are thus suitable for phased array radar applications. These measurements indicate that the low level of phase sensitivities apparently inherent in the FET amplifiers will also result in low uncorrelated RMS phase shift due to external power supply, temperature, drive, and load pulling effects. Although pulsed gate operation results in simpler bias circuit requirements than pulsed drain operation, tighter restrictions are placed upon the FET. Besides providing good rf performance, tight controls on the device dc characteristics must be maintained. All devices must pinch off or the overall efficiency of the amplifier will be degraded. The drain-to-gate breakdown must be great enough to withstand the sum of the drain voltage, the gate voltage required for device pinchoff, and the maximum rf voltage swing. This can be as high as 15-20 volts. The devices selected in this program satisfied these breakdown requirements at the expense of power added efficiency.

In using a pulsed gate system, the drain supply circuitry must be designed to permit very rapid changes in drain current. Special attention must be given to the feedthrough filters to ensure that no distortion of the pulsed drain current occurs.

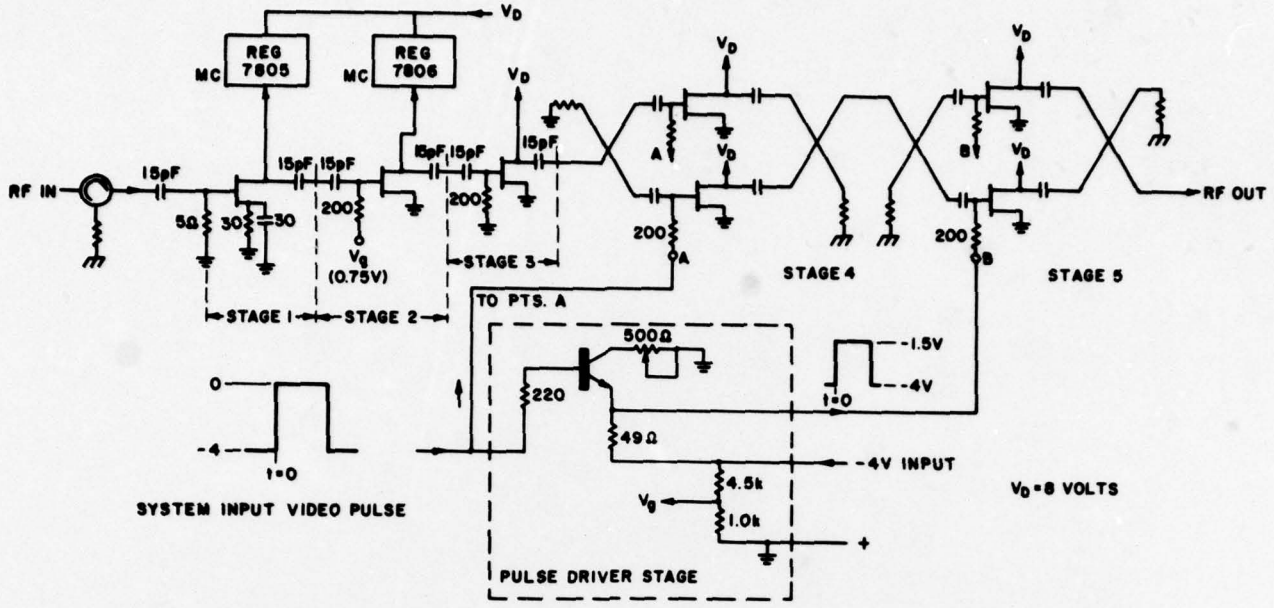


Figure 3. Composite schematic of overall FET amplifier bias (gate-drain potentials) and video pulse circuitry.

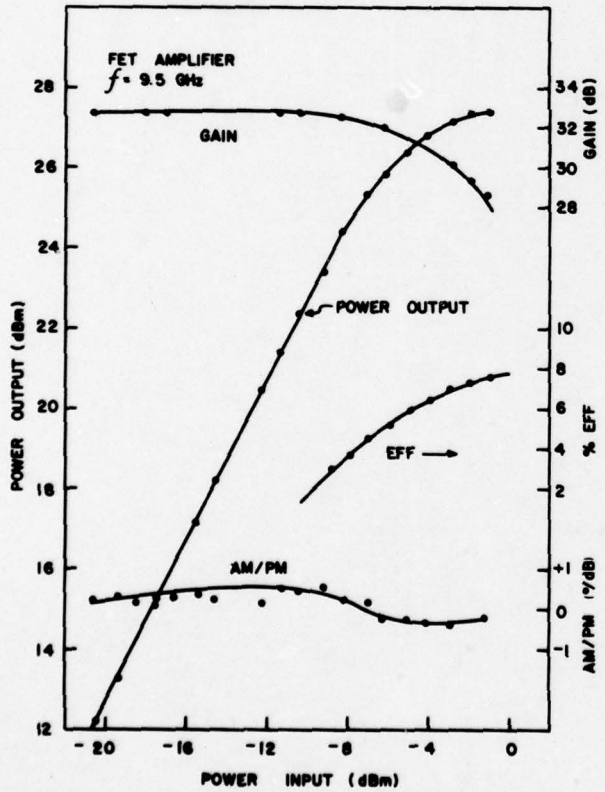


Figure 4. Output power, power added efficiency, gain, and AM/PM conversion vs. input power at 9.5 GHz (cw).

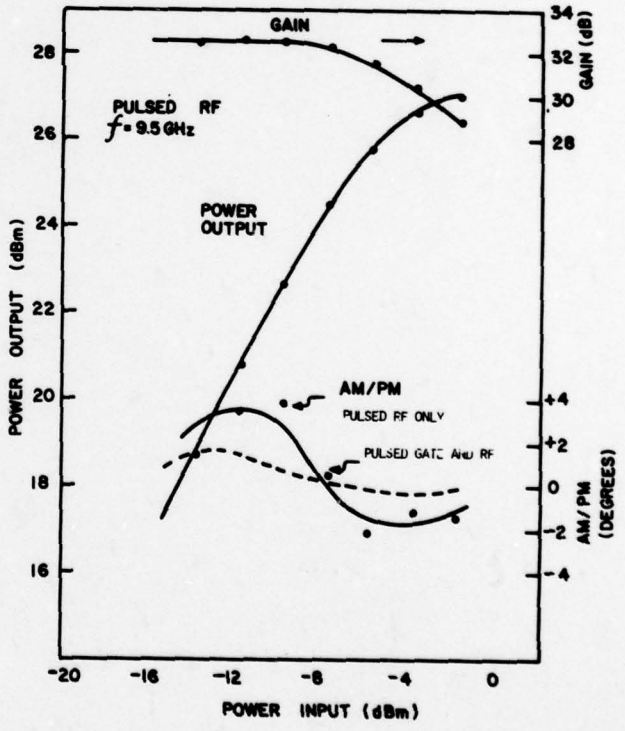


Figure 5. Midband (9.5 GHz) pulsed measurements.

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