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AAES LABORATORY SIMULATOR REQUIREMENTS

(A-7 AIRCRAFT)

FINAL REPORT
DECEMBER 1978

Ву

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For

Naval Air Development Center Department of the Navy

By

VOUGHT CORPORATION An LTV Company

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This program was conducted for establishing specific design data for a hot bench mockup (sime system being developed is based on the MAES Proto Vought Corporation under contract N62269-75-C-03 will ultimately be used by NADC to provide a labor operation and performance of the AAES in an aircoment. The evolved simulation design is formulated.	ulator). The simulator type Design evolved by the 91. The simulator system oratory verification of the raft weapon system environ-
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relectrical and avionic systems and the general physical/installation constraints of the TA-7C forward and mid fuselage sections. The designs developed under this contract were limited to electrical-avionic system definition and design. Simulator structural, system installation and wire harness designs will be developed under a follow-on contract. The designs developed under this contract include the full application of the AAES technologies to the TA-7C electrical and avionic subsystem and systems. The AAES technologies include HVDC (High Voltage DC) power generation, SOSTEL (Solid State Electric Logic) power distribution and management, and AMUX (Avionic Multiplexing).





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1.0 INTRODUCTION

The purpose of this program was to establish system requirements and develop specific design data leading to the full development and construction of the AAES TA-7C Simulator. This simulator will in essence be a hot bench mock up of the AAES technologies designed to operate and control the TA-7C electrical and avionic systems. The hot bench mock up configuration, the ADM equipment installation and system interconnect wiring closely simulates an actual TA-7C. Thus it will allow laboratory verification of the AAES technologies in an environment that closely approximates an actual aircraft weapon system.

The work performed under this program consisted of two major items, these being:

- o completing specific design tasks relative to the AAES TA-7C Laboratory Simulator Design and,
- o performing technical services for NADC relative to the AAES development and ADM hardware procurements.

The design tasks included evolving a modular system implementation concept for the simulator; developing system designs, interconnection data and wire diagrams for the TA-7C systems and circuits using the AAES technologies; establishing requirements for system control including a methodology for automatic load management; and identifying the use and requirements for the ADM hardware. The technical services consisted of participating in and assisting NADC in AAES Program and ADM Hardware Development design reviews, assisting NADC in establishing AAES system and hardware requirements, and providing NADC with planning information and data for definition and implementation of the AAES Laboratory Simulator and the AAES Flight Test System.

A modular system design concept for the simulator was developed to allow test and checkout of the complete TA-7C systems and circuits on a "group" basis. A modular design is necessary because the simulator will encompass the full complement of TA-7C systems; however, due to resource limitation, only a partial set of AAES ADM equipment is being developed for the simulator. The modular design developed allows reassignment of the ADM equipment for operating and controlling the TA-7C systems in four functional groups. These four groups are characterized as (1) weapon control and release, (2) flight control, (3) navigation and (4) communications subsystems. Interspersed among these groups are the various airframe utility subsystems. Assignments of the utility subsystems was based on enabling most of the ADM components to be functional during each of the four test configurations. The modular concept therefore provides a realistic simulation of aircraft electrical/electronic system integration as well as intersystem EMI (Electromagnetic Interference) environments. The final aspect of the modular design evolved is that it will allow updating the simulator to a "full-up" system with minimal changes to the basic simulator other than adding the full complement of ADM hardware and incorporating the full-up system operational software.

As an overview, this report identifies the functional areas, systems and circuits of the simulator design which were completed under this contract. The level of design addressed and completed by this program is in the area of the electrical/electronic system and circuit designs. The simulator structure, equipment

installation, and wire harness designs are to be evolved under a subsequent Full Scale Simulator Development Program. The design data and documentation developed under this contract will therefore form the starting base of the Simulator Development Program. The level of design and documentation completed under this program is summarized herein and examples of the data and drawings are provided. The bulk documentation (data and drawings) will be delivered along with the AAES Simulator System.

2.0 SYSTEM DESIGN

Discussed in the following paragraphs are the design tasks performed toward the development of the AAES TA-7C Simulator. Tasks performed include:

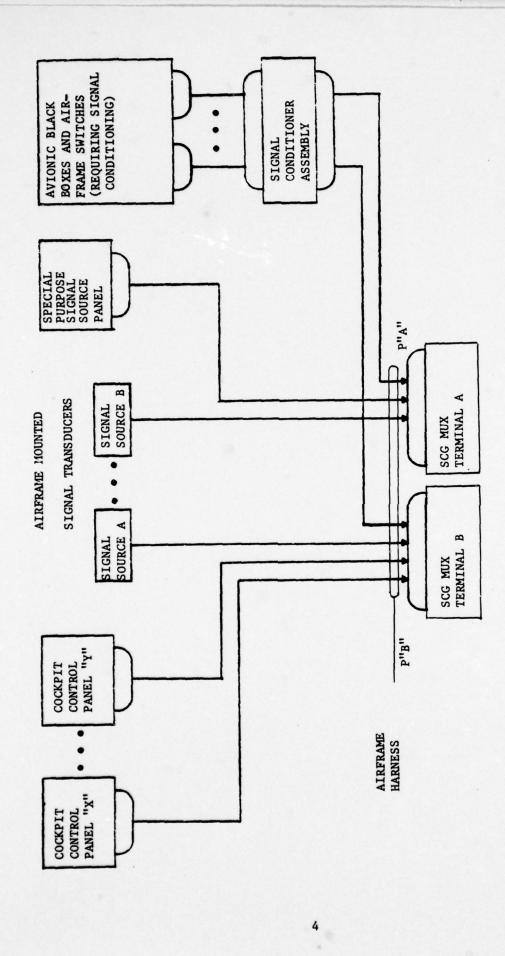
- o Development of modular design concept
- Design of TA-7C systems, circuits and control panels using AAES concepts
- o Establishment of PGS design requirements
- o Development of system control and I/O interface requirements
- o Establishment of avionic multiplex system scope and requirements
- o Definition of AAES ADM hardware utilization and
- o Establishment of system implementation/checkout priorities

These and related tasks are discussed in the following paragraphs.

2.1 Modular Design Concept

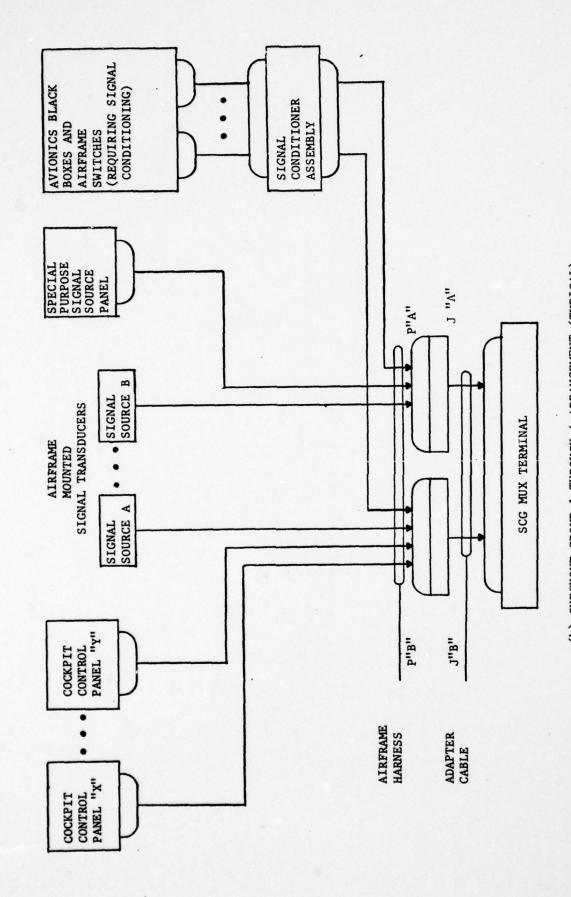
The simulator design is based on allowing operation and checkout of each circuit or subsystem on the TA-7C using a partial set of AAES ADM hardware (approximately 50 percent of that required for a full up system). The design was further evolved based on allowing growth to a full up system with minimal impact to the simulator in terms of design, hardware, wiring and installation details. Based on the ADM hardware available and the specific hardware required to implement the TA-7C Simulator, four checkout groups were established. These functional groups are characterized as weapon control and release, flight control, navigation and communication subsystems. Interspersed among these are the various airframe utility subsystems.

Figures 1 and 2 reflect the basic approach used for accomplishing the modular design. Figure 1 is illustrative of the modular concept in the area of system input control and related interfaces. Figure 1-a illustrates the signal source multiplexer interfaces and associated wire harnesses for a full-up simulator implementation. This interface primarily involves the multiplex terminals, signal sources, signal conditioning, system wiring harnesses, and special adapter cables. Of this equipment, the multiplex terminals and solid state signal sources are being developed (ADM equipment) in limited quantities for application on the simulator. It is expected that the signal sources being developed will not initially be available for installation on the simulator. Therefore, simulated signal sources of the various types needed will be mechanized for the simulator using a "standard" switch with resistors added to achieve the switched impedance function. To complete the input signal category a full complement of signal conditioning will be provided for interfacing miscellaneous "black box" and "inaccessable" switch function types to the SOSTEL Control Group. As a result, the only input related ADM hardware lacking sufficient quantity for full simulator mechanization is the SCG multiplex terminals. As shown in Figure 1-b, special adapter cables are therefore used to route signals from equipment/circuits to the "available" multiplex terminal. An appropriate set of adapter cables are thus used to select the required set of input signals for each of the four modular checkout groups. Since the multiplex terminal inputs change in terms of signal source function and equation variable for the load to be controlled, a unique set of software is used for each checkout group.



(a) FULL-UP SYSTEM ARRANGEMENT

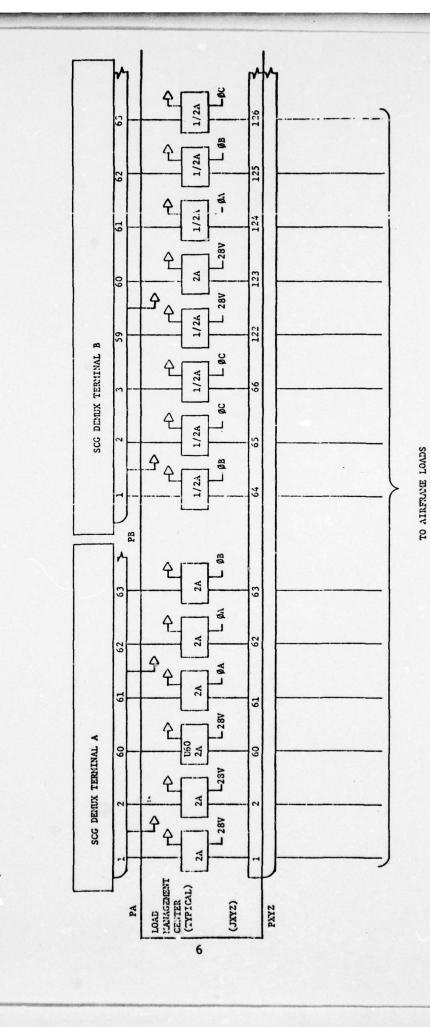
FIGURE 1 - MODULAR CONCEPT, INPUT CONTROL



(b) CHECKOUT GROUP 1 THROUGH 4 ARRANGEMENT (TYPICAL)

FIGURE 1 - MODULAR CONCEPT, INPUT CONTROL

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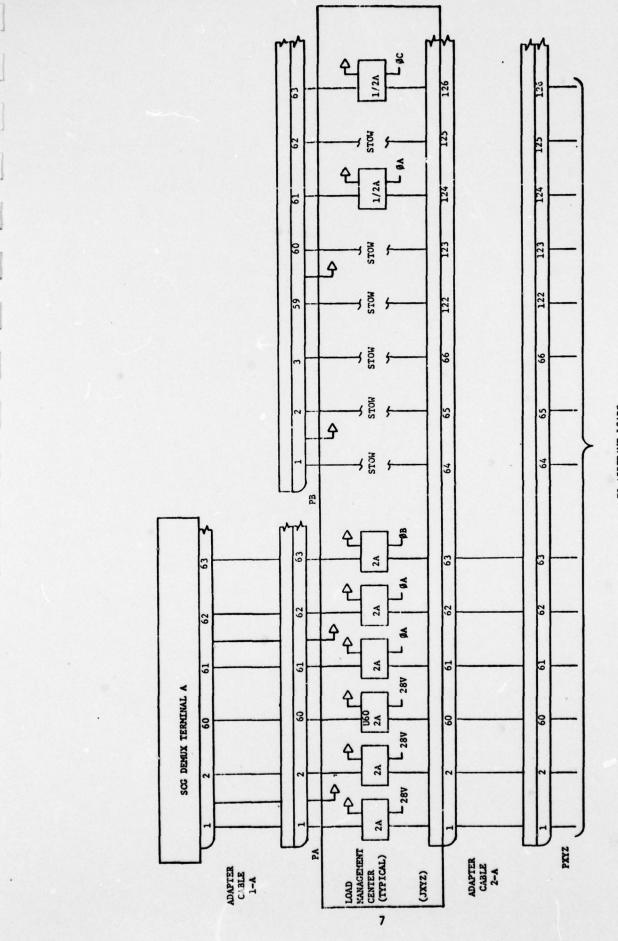


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FIGURE 2 - MODULAN CONCEPT, OUTPUT CONTROL

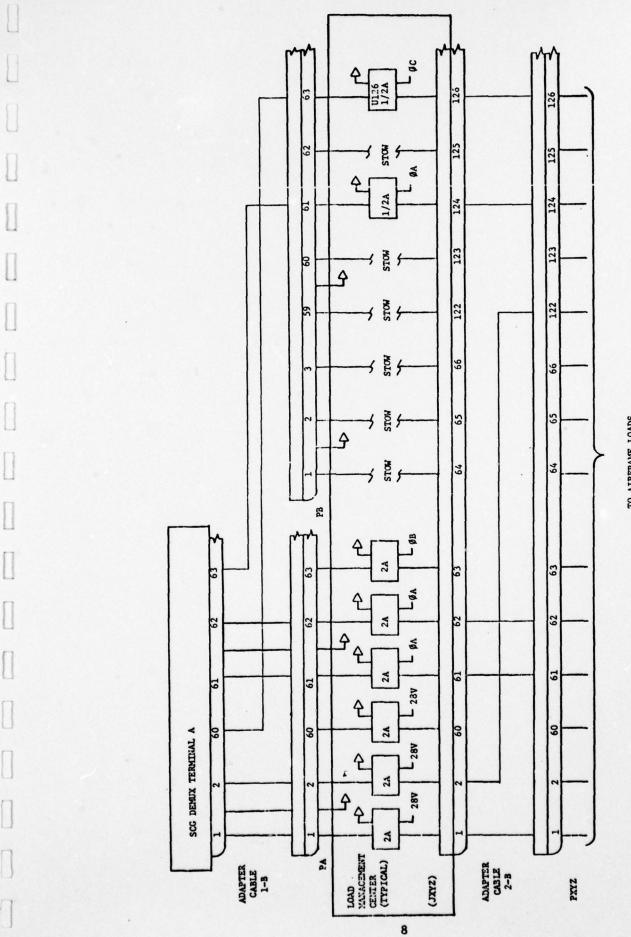
(a) FULL-UP SYSTEM ARRANGEMENT



TO AIRFRATE LOADS

(b) CHECKOUT GROUP 1 ARRANGEMENT

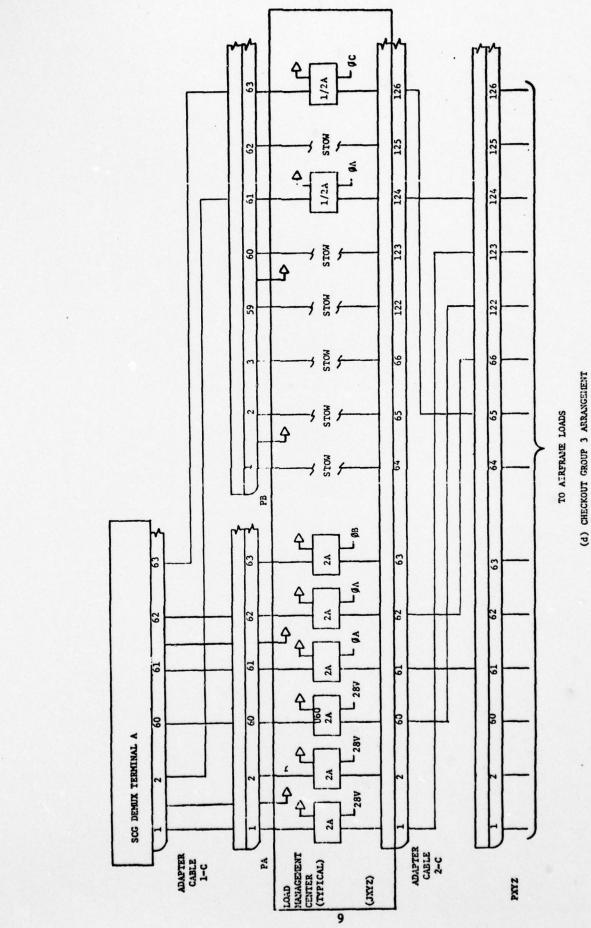
FIGURE 2 - HODULAR CONCEPT, OUTPUT CONTROL



TO AIRFRAME LOADS

(c) CHECKOUT GROUP 2 ARRANGEMENT

FIGURE 2 - HODULAR CONCEPT, OUTPUT CONTROL



0

(d) CHECKOOL GROUP 3 ARRANGEMENT

FIGURE 2 - HODULAR CONCEPT, OUTPUT CONTROL

Figure 2 is illustrative of the modular design as related to the system output control and associated interfaces. Similar to the case described for the multiplex terminals and signal sources, limited quantities of demultiplex terminals and power controllers will be initially available for application on the simulator. One notable difference is that it is not practical to simulate the power controller. Therefore in addition to change out of the "demux to controller" adapter harnesses and software, the power controllers must be reinterfaced to different loads. The controllers are contained in Load Management Centers which are configured as subassemblies for production line producibility. Because of the connector subassembly interface, it is feasible to use adapter cables for establishing the desired controller to load interfaces.

The load controller interface with SCG demultiplex terminals and with the airframe harnessing (and hence airframe loads) is shown in Figure 2-a for the full-up simulator. This figure depicts a typical Load Management Center (LMC) electrical configuration to be used on the full-up simulator. The only difference between this configuration and one which would be used on a production aircraft lies in the demultiplex terminal/load controller interface. In a production configuration, the demultiplex terminal size would be sufficiently smaller (due to MSI/LSI terminal construction) to permit the terminal to be installed within the LMC. Installation within the LMC reduces the control harness length between the demultiplex terminals and the load controllers.

Since the simulator initially will have less controllers and demultiplex terminals than are required for the full-up configuration, adapter cables will be added between (a) the load controllers and the demultiplex terminal, and (b) the load controllers and the airframe harnessing (loads). Figure 2-b through 2-d illustrates these adapter cables. The three figures also show the variation in adapter cables end-to-end terminations. These variations permit limited demultiplex channels to control the "available" load controller complement for powering all simulator loads.

The variation in signal/power paths between checkout groups can be seen by examining the interconnection paths from channel 60 of demultiplex terminal "A". In Figure 2-b (checkout Group 1) channel 60 signal routes through adapter cable 1-A to the input of a 2 ampere, 28 VDC controller. Power is then switched by this controller (designated U60) through adapter cable 2-A to the load associated with airframe harness contact 60 of plug designated P "XYZ". To transition from checkout group 1 to group 2, adapter cables 1-A and 2-A are replaced by cables 1-B and 2-B respectively. This second interconnect configuration (shown in Figure 2-c) permits demultiplex terminal channel 60 to be routed through adapter cable 1-B to a 1/2 ampere, 115 VAC controller (designated U126). Power switched by this controller is routed through adapter cable 2-B to the load associated with P "XYZ" contact 126.

In a similar manner, transitioning from set B switching adapter cables to set C adapter cables reconfigures the LMC to the interface shown in Figure 2-d for checkout group 3. In this group 3 arrangement, channel 60 again controls the 28 VDC, 2 ampere controller designated U60 as occurred in checkout group 1. In group 3, however, U60 controller switches dc power through the 2-c adapter cable to a 28 VDC load associated with P "XYZ" contact 122.

In summary, the modular concept implementation shown for load controllers facilitates sharing the limited output related ADM equipment. However, in addition to load controllers, solid state output drivers are required to provide the full set of SCG output signals. A full set of these output drivers are defined for the simulator system to allow it to be easily expanded to a full-up system. Of particular significance is that this modular checkout concept allows

the simulator basic wiring to remain intact for the full-up case. Also in the interim case, the systems/equipment operated in each of the four functional groups are basically equivalent to those operational at any given time in a full-up system. And lastly, the group assignments result in a maximum usage of the available ADM equipment.

The ADM equipment usage versus that available is described in paragraph 2.4.4 as are the various special equipments (signal conditioners, simulated signal sources and adapter harnesses) needed for the simulator.

2.2 TA-7C Subsystem Designs

A total of 121 TA-7C subsystems and circuits were designed using the AAES technologies, hardware and control techniques. These subsystems are listed in Table 1. Documentation was prepared for the designs using CAD (Computer Aided Design) techniques. Figures 3 and 4 are representative of the designs evolved and the level of completeness and detail contained in the prepared documentation. These representative designs are for the Liquid Oxygen Gauging and the Emergency Accumulator Test systems. The documentation for each system will be expanded to include appropriate harness and termination assignment upon their completion as a part of the Full Simulator Development Program.

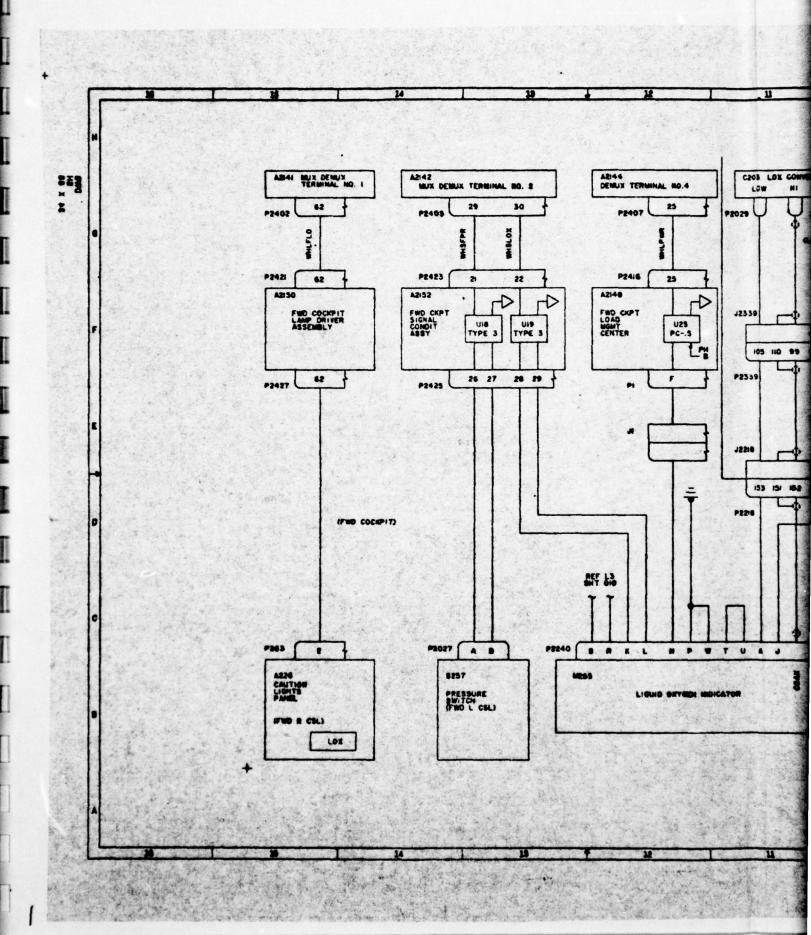
2.3 Power Generating System (PGS) Design Requirements

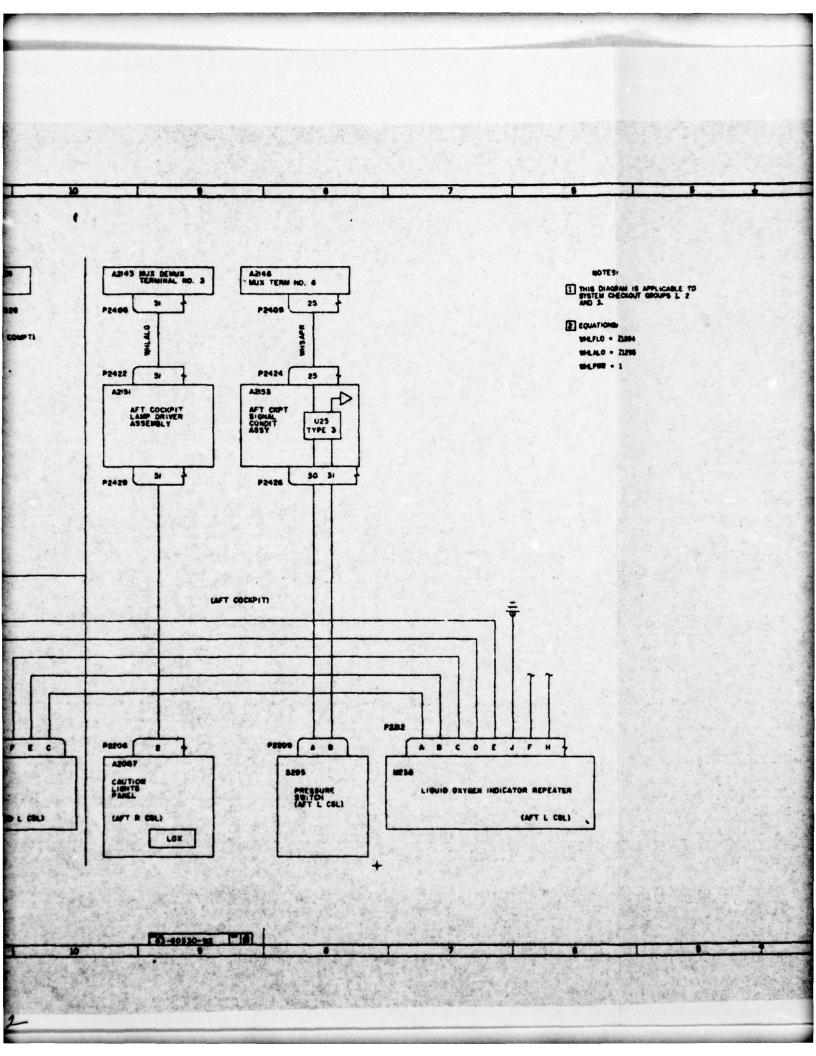
A number of related tasks were performed concerning the PGS. These included preparing a PGS system definition and description, establishing a method for supplementary loading of the ADM 45 KW generator with the simulator system, establishing a preliminary grounding philosophy for the simulator, and defining the A-7 engine pad-generator mounting interface. These are discussed in the subsequent paragraphs.

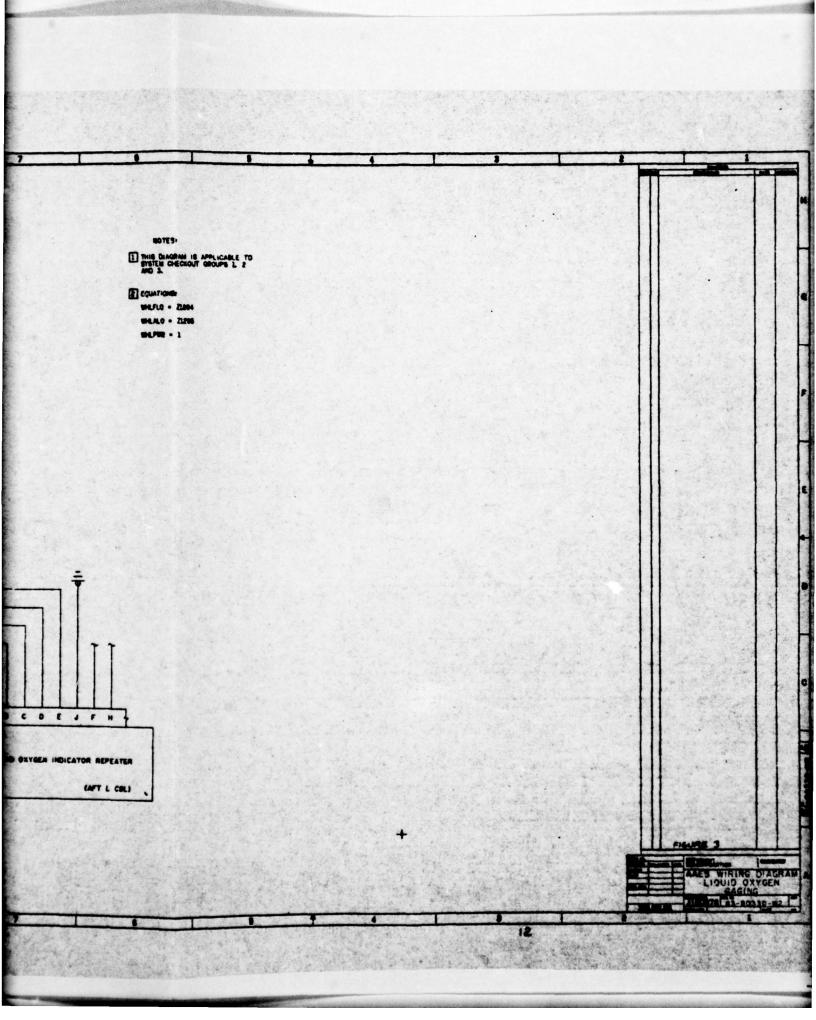
2.3.1 PGS Definition and Description

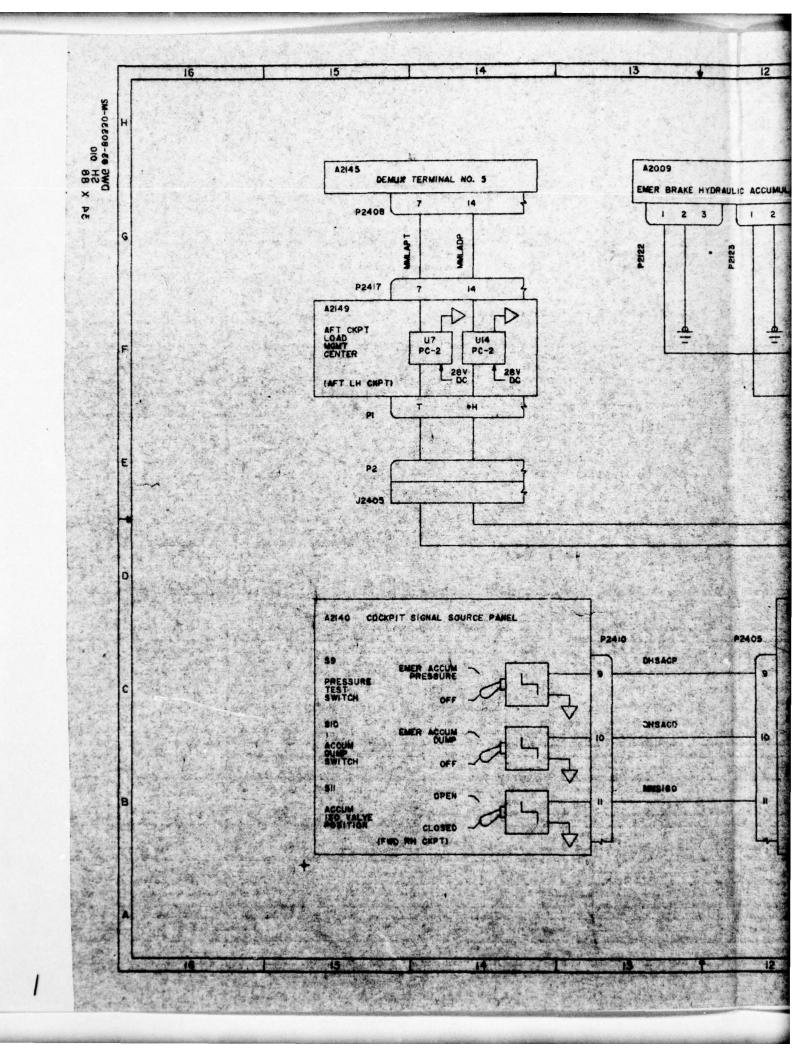
The power generation subsystem design for the AAES simulator is based upon performance requirements defined in procurement specifications for the generator (NADC-VT-TS-7502 dated 13 June 1975) and the power conditioner units (NADC-VT-TS-7503 dated 8 July 1975). The primary electric power source for the simulator consists of two 45 KW, 270 volt DC generators as defined by the NADC procurement specification. The generators will not be an integral part of the simulator but will be operated from a "generator drive stand" in the NADC AAES Laboratory. Power feeders will route the power to the simulator. The point of regulation will be located on the simulator as will all equipment except the generators. A portion of the 270 VDC power will be used to power 270 VDC "dummy" loads located external to the simulator and a limited number of loads (the SCG and AMUX WRAs) mounted in the simulator. The remainder of the power will be converted to 28 volts DC by two 100 ampere converters and to 115/200 volt AC by two 10 KVA inverters. The generation and conversion equipment will be connected to provide primary buses as shown in Figure 5.

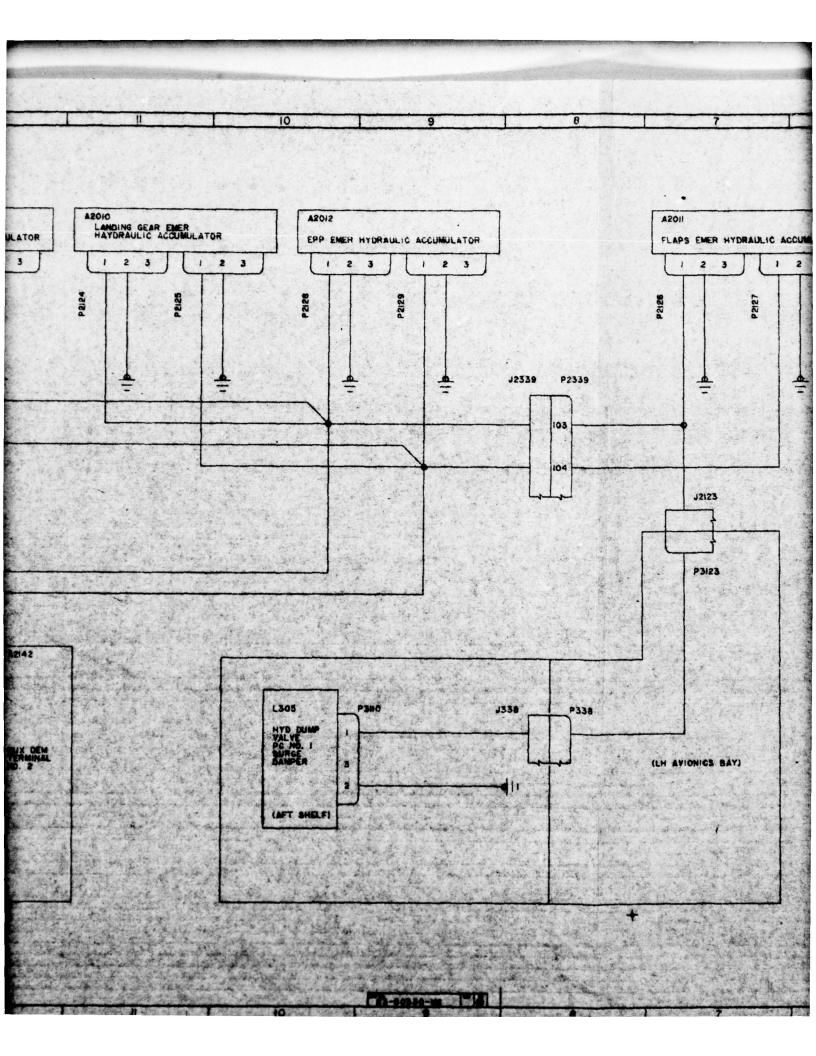
System operation is as follows: When one generator is brought up to rated speed and the output voltage at the point of regulation (located on the simulator) is at rated voltage (270 \pm 5 VDC), the HVDC bus controller (BC) and the HVDC bus tie controller (BTC) will automatically close. The generator now











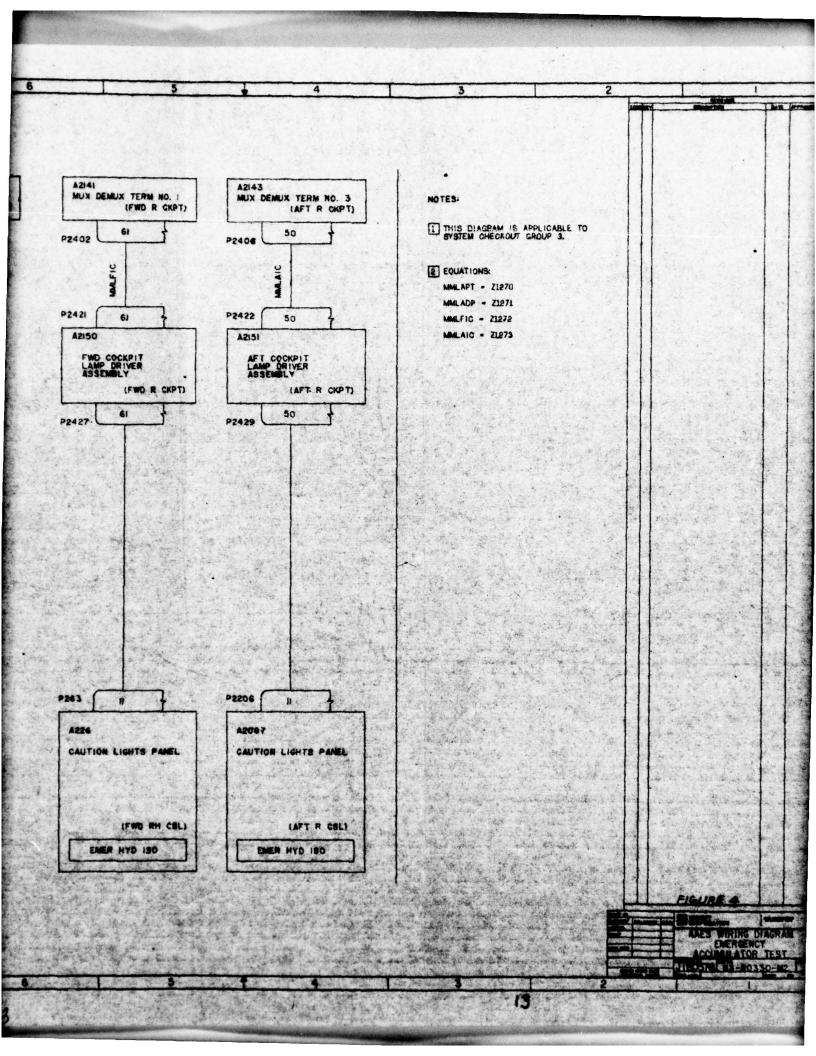


TABLE 1

TA-7C SUBSYSTEM/CIRCUIT DESIGNS

TA-7C SUBSYSTEMS

*A1	Shrike Improved Display System
*A2	Armament Station Control- Jettison
*A3	Weapon Station 1 Stores Management
*A4	Weapon Station 2 Stores Management
*A5	Weapon Station 3 and 4 Stores Management
*A6	Armament Advisory-Forward Cockpit
*A7	M61-Internal Gun System
* 48	Armament Advisory-Aft Cockpit
~ AQ	Nay/Won Del ContreRelease Control
~ 410	Electric Fuzing System
*A11	Weapon Station 5 and 6 Stores Management
* A12	Weapon Station 7 Stores Management
* A13	Weapon Station 8 Stores Management
B1	KB-18 Camera
C1	Speed Brake Control
C2	Wheels Flaps Warning
C3	Approach Power Compensator
C4	Pitch and Roll Trim System
C5	Automatic Flight Control System - Roll Channel
C6	AFCS-Pitch Channel
C7	AFCS-Yaw Channel
C8	Variable Flaps Control
C9	Emergency Flaps Control
D1	Landing Gear Position Indication
D2	Hydraulic Pressure Indication and Warning
D3	Weight-on-gear and Deck Compression Sensing
D4	Pitch and Roll Trim Indication
D5	Leading Edge Flaps Position Indication
D6	Trailing Edge Flaps Position Indication
D7	Speed Brake Flaps Position Indication
υ,	Speed Brake Fraps Position Indication
E1	Pressure Ratio Indication
E2	Engine Oil Pressure Indication and Warning
E3	Fuel Quantity Indication and Warning
E5	Engine Fuel Control
E6	Engine Fuel Flowmeter Indication
E7	Fuel Filter Bypass Indication
E8	Turbine Inlet Temperature
. F1	Doppler Radar
F2	Pitot Heater/Engine Anti-Icing
F3	Counting Accelerometer System
F4	Standby Attitude Indication
F5	IMS Control
F6	Inertial Measurement Set

(Continued)

TA-7C SUBSYSTEM/CIRCUIT DESIGNS

TA-7C SUBSYSTEMS

F7	Inertial Measurement System
F8	Angle of Attack
F9	Horizontal Situation Indicator
F10	Heading Mode
F11	Flight Mode Control - Fwd. Cockpit
F12	Flight Mode Control - Aft Cockpit
F13	Head Up Display
F14	Projected Map Display
F15	Nav/Weapon Delivery Computer
F16	Nav/Weapon Delivery Computer
F17	HUD Monitor
F18	ARA-63 Appraoch Control System
F19	
	HUD & ADI Landing Select Control
F20	Command Transfer Control
F21	Horizontal Situation Indicators
G1	Windfold Control
G2	Landing Gear Safety/Position Detent
G3	Arresting Gear Control
G4	Nose Gear Steering
G5	Launch Bar Control
G6	Anti-Skid Brakes
G7	Parabrake Control
H1	Temperature Control/Rain Repellant
H2	Hydraulic Accumulator Heaters
113	Electronic Compartment Cooling
K1	Engine Crank and Ignite
K2	Engine Bleed
L1	Flood Lighting-Forward Cockpit
L2	Instrument Board Lighting-Forward Cockpit
L3	Console Lighting-Forward Cockpit
L4	Exterior Lighting
L5	Warning and Advisory Lighting-Forward Cockpit
L6	Flood Lighting-Aft Cockpit
L7	Instrument Board Lighting-Aft Cockpit
L8	Console Lighting-Aft Cockpit
L9	Warning and Advisory Lighting-Aft Cockpit
	and included and accurate
M1	Seat Adjust
M2	Emergency Accumulator Test
M3	Emergency Power Package Actuator
M4	Canopy Actuation Control and Warning
114	campy Accuation control and warning

TABLE 1

(Continued)

TA-7C SUBSYSTEM/CIRCUIT DESIGNS

TA-7C SUBSYSTEMS

*XA1

*XB1

*XB2

*PA1 *PB1 *PC1 *PC2 *PC3 *PC4	Primary Power Generation, Conversion and Control External Power Control Primary 270 VDC Load Bus System Emergency 270 VDC Load Bus System Primary 28 VDC Load Bus System Emergency 28 VDC Load Bus System
Q1	In-Flight Refueling and Ground Fueling
Q2	Fuel Transfer and Dump
Q3	Low Level Fuel Warning
*RD1	UHF-ADF System (ARA-50)
*RL1	Auxiliary Radio Receiver Set (ARR-60)
*RN1	TACAN Navigation System (ARN-52)
RP1	ASW-25 Data Link (Display Control)
RP2	ASW-25 Data Link (Forward/Aft Control)
*RU1	UHF Communication System (ARC-51A)
*RZ1	Audio System
*RZ2	Weapon Release and Low Altitude Tone Generator
*SA1	Radar Height Indication System
SN1	Altitude Indicator
SS1	Forward Looking Radar (Dig. Scan Conv.)
SS2	Forward Looking Radar (NWDC Interface)
SS3	Forward Looking Radar (Power Control)
SX1	IFF System (APX-72)
SX2	IFF Aft Control
TE1	Interference Blanker Set
TE2	ALR-50 Radar Homing and Warning
TE3	ALR-45 Radar Homing and Warning
TM1	ALE-29 Chaff Dispenser
TN1	True Airspeed Indicator
TN2	Air Data Computer
TQ1	Radar Beacon (APN-154)
U1-U3	AMUX System
W1	Fire Detection System
W2	Liquid Oxygen Gauging and Warning
W3	Rain Removal Overheat Warning

Emergency Power Generation, Conversion and Control

Primary AC Load Bus System

Emergency AC Load Bus System

^{*} Systems Requiring Additional Circuit Definition and Design which are to be completed on Full Simulation Development contract.

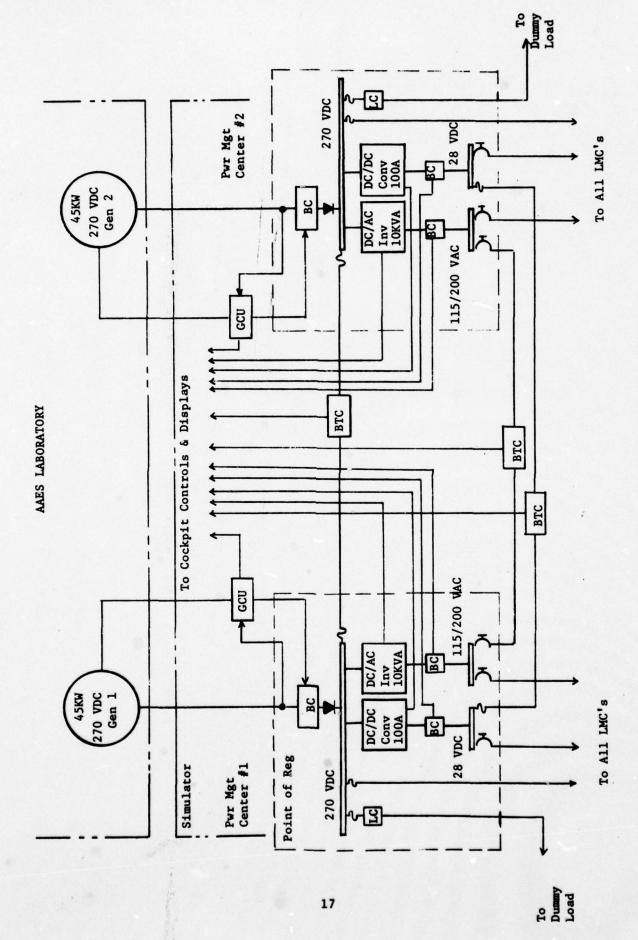


FIGURE 5, AAES Laboratory Simulator Power Generation Subsystem

supplies power to both 270 VDC buses. When the other generator is brought up to rated speed and its output voltage is less than 5.0 volts above the main bus voltage, its HVDC bus controller closes automatically and the two generators now supply power to the simulator system loads. The two generators are now operating in parallel which is the normal mode of operation for the system. The main buses are regulated to 270 ± 5 volts BC by each of the generator GCUs which ensures the load on each generator is equally divided. Isolated mode of operation is provided by manually commanding the HVDC BTC to open. In the event a generator becomes inoperative (generator, GCU or drive failure), the failed generator will be automatically disconnected from the bus.

The bus controllers for the converter and inverter are automatically closed (with manual override) when the output voltage characteristics of the inverter and converter are within prescribed limits. The AC bus controller closes when the two inverters are synchronized and voltage levels are within prescribed limits to ensure equal load division. The normal mode of operation for the two converters and inverters is parallel. Isolated mode of operation is provided by manually commanding the 28 VDC BTC and 115/200 VAC BTC to open. The converters and inverters contain overload and fault protection. MIL-STD-704 power at the main buses is maintained by automatic opening of the respective bus controller should MIL-STD-704 limits be exceeded.

It is noted that all control of power to the main buses is independent of SOSTEL. Data, however, can be supplied to SOSTEL to effect the control of loads (i.e., load management) by SOSTEL. Useful data includes generator temperature, converter temperature, inverter temperature, bus voltage (270 VDC, 28 VDC, 115/200 VAC), AC bus frequency and ripple content on DC buses. SOSTEL can be programmed to remove loads when data indicates the removal of loads might avert shutdown of the complete system.

2.3.1.1 Emergency System

An emergency power source as defined by SD-24K is not provided. The emergency operation will be simulated by having one generator operate as the primary source and the other generator serve as an emergency source. The non-essential loads will be removed from the buses via SOSTEL control during the simulated emergency condition.

2.3.1.2 External Power

The Vought AAES Simulator Design is presently based on not including "External Power" provisions. In the event that NADC wants "external power" provisions included on the simulator, this requirement should be established prior to award of the simulator development contract. Design data and interface requirements for the power monitor, external power receptacle and bus controller hardware must be established by NADC to enable adequate design of the External Power interface on the simulator if required.

2.3.1.3 Bus Controller

The bus controller function can be implemented with either an electromechanical, solid state or hybrid (electromechanical and solid state) device. The DC bus controller can be either a directional or a bi-directional device. If it is a directional device, it must have reverse voltage blocking capability. The controller must be capable of conducting and switching the maximum power source output current without affecting the normal operation of the power source protective circuitry. That is, the bus controller must not impede the flow of current. The minimum current level is 150 percent of generator rating for the inverter and converter bus controllers (specification NADC-VT-TS-7503 dated 8 July 1975). The HVDC bus controller must also have a minimum blocking voltage rating of 500 VDC. The Hartman contactor, part no. A-751RG, meets the HVDC bus controller requirements for the laboratory environment. Vought will establish the installation and connection requirements for the converter and inverter bus controller based on the Hartman contactor unless notified to the contrary by NADC prior to award of the Simulator Development Contract.

2.3.1.4 Bus Tie Controller

The bus tie function can be implemented with an electromechanical, solid state or a hybrid device. The DC devices must be capable of conducting and switching bi-directional current. Bus tie controllers must be compatible with the opening characteristics of feeder protectors (fuses or circuit breakers), that is, it must not impede the flow of current to the extent that the protector will not open. The Hartman bus tie controller, part no. A-751RG, meets the HVDC bus tie requirements for the laboratory environment. The AAES simulator designs, installation and electrical interface will be based on this device unless Vought is advised to the contrary prior to award of the Simulator Development Contract.

2.3.1.5 Protective Circuitry and System Coordination

To provide compatibility with the power source (generator, converter, inverter) equipment, it is necessary that the feeder protector opening characteristics (fuse or circuit breaker) not cause interference with the normal operation of the power source protective circuitry i.e., the feeder protector device must open before the power source trips off the bus. System design requires the capability of supplying full system load from either generator. Therefore, the HVDC bus tie feeder and associated feeder protectors must be rated for 100% generator capacity. This creates a problem because the trip characteristics of available feeder protectors (high voltage fuses) can allow the generator to trip before the feeder protector opens, i.e., clears the fault. This results in the generator protecting the feeder in some load conditions rather than the fuse providing the feeder protection.

Additionally, available feeder protectors that are needed for protecting feeders to some of the LMCs are not compatible with the converter and/or inverter protective circuitry. That is, the LMC feeder protector (fuse or circuit breaker) can allow the converter and/or inverter to trip before the feeder protector opens. These problems are primarily due to the tight trip limits established for the generator, converter and inverter. This is not a serious problem for the simulator since feeder faults will be an unlikely occurrence due to the simulator environment. Should a feeder fault occur, the worst thing that could happen would be a nuisance power source (generator, converter or inverter) trip. Vought will therefore select feeder protectors based upon feeder current ratings. Possible solutions exist for actual aircraft applications which include changing the power source trip limits, or paralleling feeders to allow use of current protectors that have lower trip ratings.

The generator, power converter, feeder protector coordination conditions as they exist for the AAES TA-7C Simulator are highlighted in Figures 6 through 10. Figure 6 identifies the trip coordination for the generator 270 VDC protection and the PCU feeder protector. This shows that the generator will trip off-line rather than the fuse opening to isolate PCU feeder faults for overload conditions in excess of 120 percent of generator rating, i.e., 200 amperes. Also shown is the compatibility between the generator with respect to the TA-7C composite overload as imposed by an overloaded PCU. Figure 7 indicates the incompatibility between the PCU trip protection and the worst case LMC feeder circuit breaker. In this case the PCU will trip rather than the circuit breaker for 28 VDC overloads exceeding 150 amperes. Also the PCU will not carry the full simulator composite load under a feeder fault condition. The PCU will however, marginally carry the full simulator 28 VDC composite load under normal conditions. Figures 8, 9 and 10 indicate the coordination conditions for 115 VAC for cases of using MIL-C-5809 circuit breakers, MIL-F-5372 fuses and MIL-F-15160 fuses, respectively. Proper coordination is obtained using the circuit breaker and the 5372 fuse. The 15160 fuse is not compatible with the PCU trip protection limits.

2.3.1.6 PGS Installation

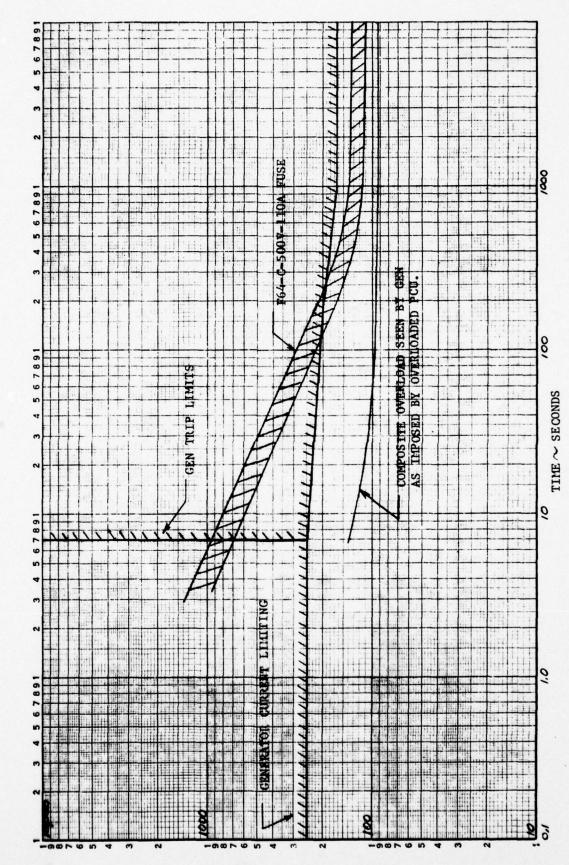
The bus controllers, inverter, converter and feeder protectors will be installed in close proximity to each other and physically protected to form a "power management center" as shown in Figure 5. This will negate the need for feeder protectors between the HVDC bus and the inverter/converter. Detailed installation data/design will be generated as part of the Full Simulator Development contract.

2.3.1.7 PGS Equipment Responsibility

The power generation and bus network equipment requirements for the AAES simulator are summarized in Table 2. Identified are equipment types, quantities, and procurement responsibility as presently understood by Vought.

2.3.2 PGS Supplementary Loading

The HVDC generator and power converter/inverter equipment procured for the simulator requires supplementary loading in order to provide equipment evaluation at full capacity. This is required because limited ADM equipment is being initially procured and the TA-7C electrical load is less than the ADM generator 45 KW rating.



46 7522

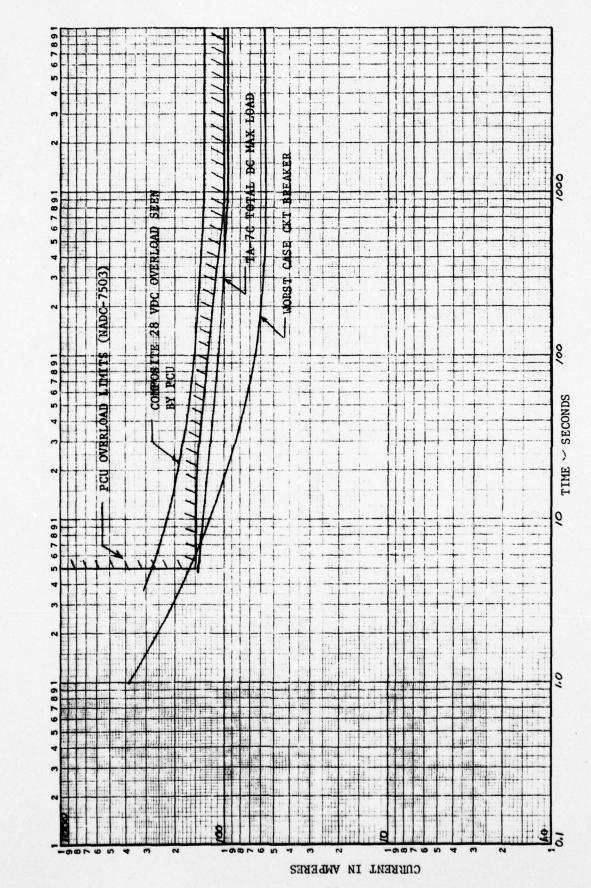
KOEARITHMIC 4

GENERATOR-PCU 270 VDC FEEDER PROTECTION COORDINATION

(HIL-F-15160 FUSES)

FIGURE 6

CURRENT IN AMPERES



10 . 522 100 in U S.A. .

KON 3 X S CYCLES
KEUFFEL & ESSER CO.

PCU-LMC 28 VDC FEEDER PROTECTION COORDINATION

FIGURE 7

(MIL-C-27715 CIRCUIT BREAKERS)

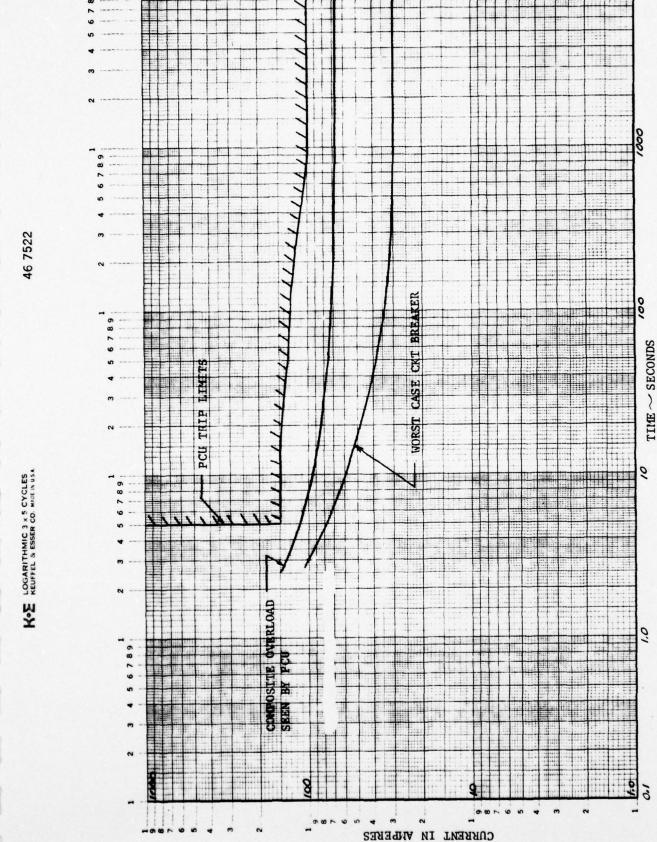
22

TIME ~ SECONDS 0.1

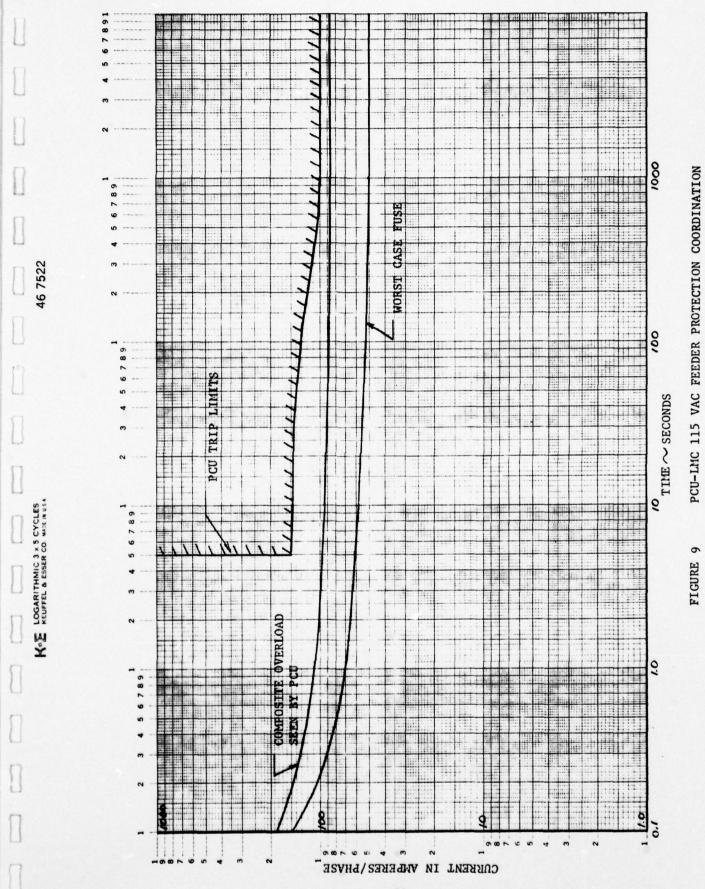
PCU-LMC 115 VAC FEEDER PROTECTION COORDINATION

FIGURE

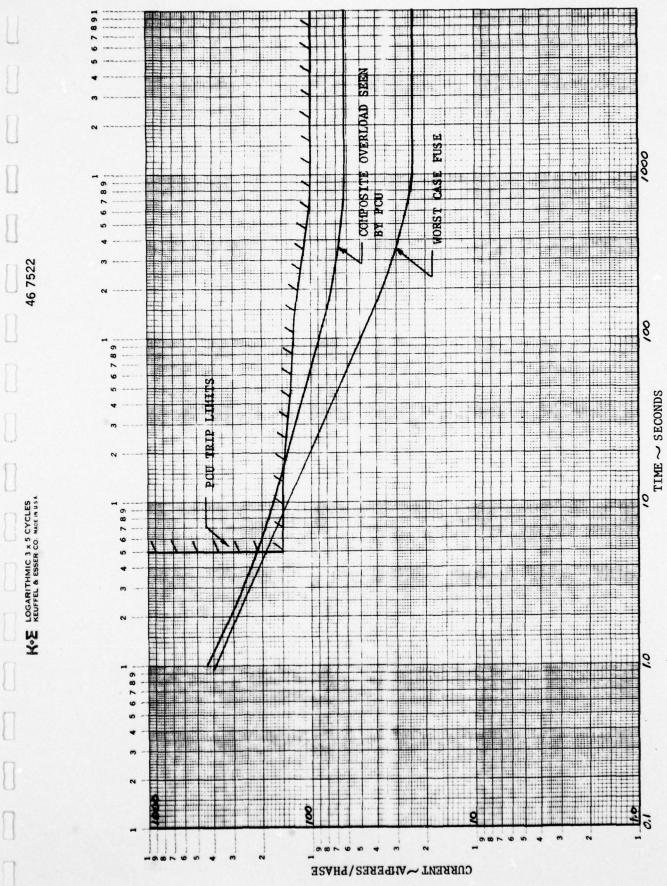
(HIL-C-5809 CIRCUIT BREAKERS)



23



(MIL-F-5372 FEEDER PROTECTORS)



PCU-LMC FEEDER PROTECTION COORDINATION

FIGURE 10

(HIL-F-15160 FEEDER PROTECTORS)

25

TABLE 2.

POWER GENERATION SUBSYSTEM AND BUS NETWORK EQUIPMENT REQUIREMENTS

ITEM	NOMENCLATURE	PART NO.	QTY	FURNISHED BY
1	45KW, 270VDC Generator Sys	NADC-VT-TS-7502	2	NADC
2	100A, 28VDC Pwr Conditioner	NADC-VT-TS-7503	2	NADC
3	200A, 270VDC Bus Controller	A-751RG or Equiv	2	NADC
4	200A, 270VDC Bus Tie Controller	A-751RG or Equiv	1	NADC
5	100A, 270VDC Load Controller	A-754R or Equiv	8	NADC
6	HVDC Feeder Fuse	Type F64-C-500	24	Vought
7	100A, 28VDC Bus Controller	MS24141-D1 or Equiv	2	NADC
8	50A, 115/200 VAC Bus Controller	MS24168-D1 or Equiv	2	NADC
9	100A, 28VDC Bus Tie Contr	MS24141-D1 or Equiv	1	NADC
10	50A, 115/200VAC Bus Tie Contr	MS24168-D1 or Equiv	1	NADC
11	28VDC Feeder Fuse	MS28937-XXXX	2	Vought
12	28VDC Feeder Circuit Bkrs	MS24571-XXXX	14	Vought
13	115/200 VAC Feeder Circuit Bkrs	MS14153-XXXX	16	Vought
14	Cockpit Controls & Displays	TBD	-	Vought
15	10KVA, 115/200VAC Pwr Cond.	NADC-VT-TS- 7503	2	NADC
16	Diodes, Reverse Current Protection	TBD	2	Vought
	External Power Provisions if Requi	red		
17	External Power Receptacle	TBD	1	NADC
18	External Power Monitor	TBD	1	NADC
19	200A, 270VDC Bus Controller	A-751RG, or Equiv	1	NADC
20	Diode, Reverse Current Protection	TBD	1	Vought

The discussion which follows describes a recommended design for artifically loading the AAES simulator power system.

2.3.2.1 Supplementary Loading Design

Design provisions for artificial (or dummy) loads are provided on the simulator to allow the power system capacity to be fully exercised. These loads are connected to the main power buses (270 VDC, 28 VDC and 115/200 VAC) through electromechanical contactors. The contactors are controlled by the SCG terminal located in the aft equipment shelf LMC.

Figure 11 provides a block diagram overview of the dummy load circuitry. Figures 12 through 14 depict the load interconnection at each main bus and identify the recommended hardware and load current requirements. The figures also show the division between simulator installed hardware and provisions versus external simulator hardware.

As shown in the figures, the contactors are controlled by the SCG via relay drivers. Ideally, this relay driver function would be provided by ADM load controllers. However, due to the limited initial load controller quantities being procured for the simulator, the contactors may be energized by solid state custom designed relay drivers controlled by an SCG terminal. The estimated load requirements for these drivers are:

- 3.5 amperes at 28 VDC for 500 milliseconds
- 0.4 amperes at 28 VDC continuously

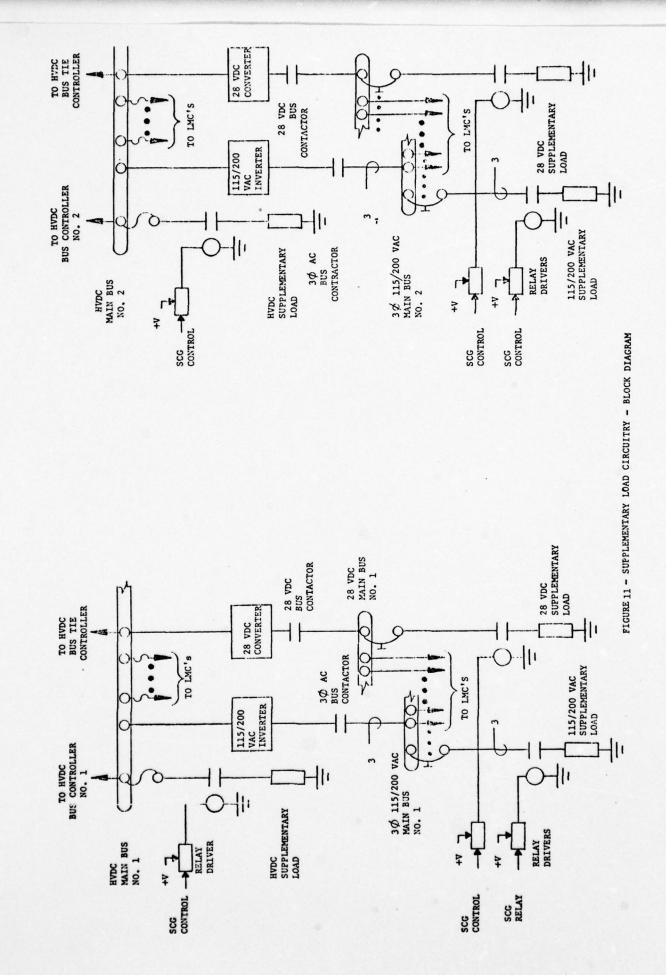
Provisions are included in the design to allow connection of the dummy loads to the main power buses via SCG control. The dummy load control via the SCG will be derived by:

- o The state of various signal sources installed in the General Purpose Signal Source Panel located on the aft equipment shelf
- o The operational mode of SCG Load Management system software routine.

This method of control permits dummy loading of the power system by manual (signal source panel) or automatic (load management) operations. The Boolean logic for this control will be integrated into the power distribution software of the SCG Processors to be delivered by Vought with the simulator.

As shown in Figures 12 through 14, a total dummy load requirement of 135 to 270 kilowatts is required to adequately evaluate the simulator power system. Since the required mounting space for the dummy loads is somewhat excessive, mounting of dummy loads external to the simulator is recommended. In addition, to keep the simulator relatively "clean" of power system "test" hardware, the power contactors and wire harnessing associated with dummy load control should also be located in mounting racks located external to the simulator. Figure 15 schematically depicts this external rack configuration. It is anticipated that existing generator load banks at NADC can be used for the dummy loads to reduce hardware costs.

Interconnection points are provided on the simulator for interfacing the load rack (Figure 15) to the main power buses and to the appropriate SCG demultiplex terminal channels. The power bus terminations (identified as Point A in Figures 12 through 14) are downstream of the feeder protectors but within the associated Main Power Center to maintain physical protection of the power bus.



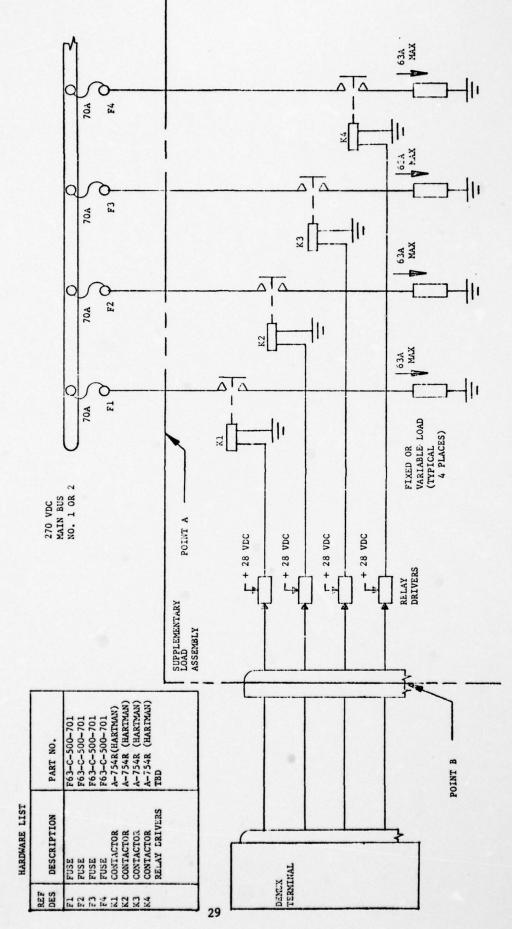
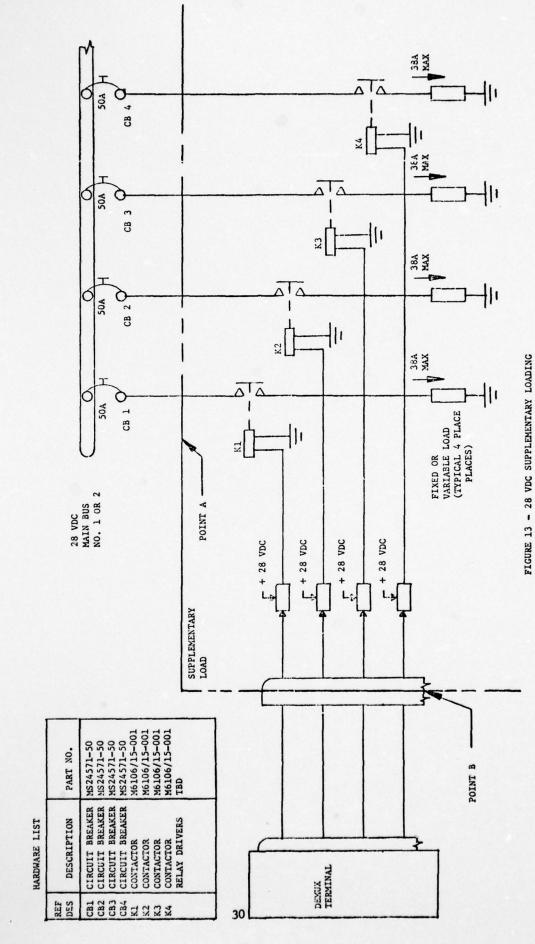
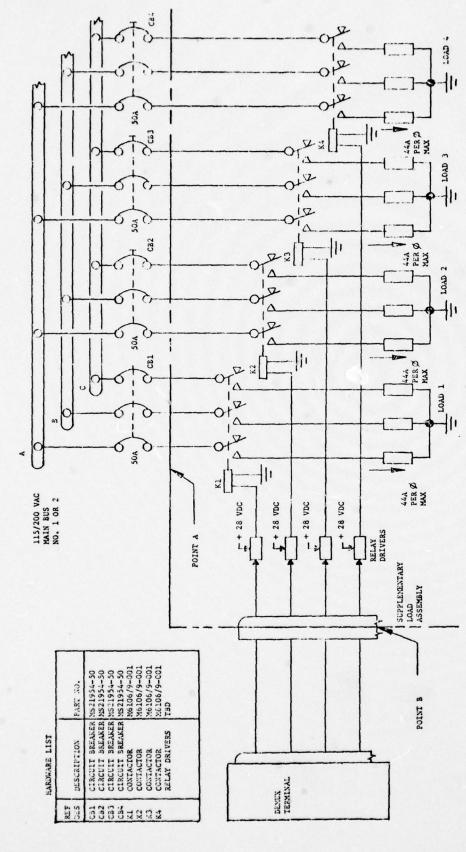


FIGURE 12 - HVDC SUPPLEMENTARY LOADING





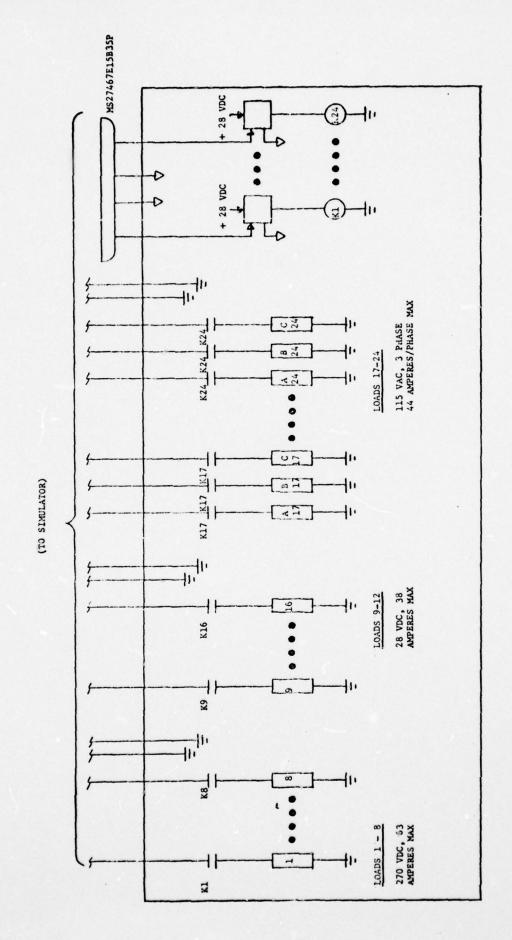


FIGURE 15 - SUPPLEMENTARY LOAD ASSEMBLY

The termination location reduces personnel hazards by eliminating exposed "hot" points on the simulator. The SCG demultiplex terminal channel interface is provided by a connector break at the simulator aft equipment shelves (Point B of Figures 12 through 14). A jumper plug will be provided with the simulator to maintain proper terminal channel loading (for SCG BIT) on these channels when the external dummy loading racks are not connected.

2.3.2.2 Hardware Requirements and Considerations

Hardware requirements and considerations for implementing and demonstrating the PGS supplementary loading involve the HVDC power contactors rated at 100 amperes, relay drivers for contactor control, and load banks having the required wattage ratings. These are discussed in the subsequent paragraphs.

1. HVDC Power Contactors

Due to the apparent lack of hybrid or solid state HVDC bus controller availability, large electromechanical contactors will likely be required for switching power to HVDC dummy loads. An "off-the-shelf" contactor has been identified for use as the main HVDC bus controller. This contactor, rated at 400 amperes at 270 VDC, requires considerable mounting space (at least 144 cubic inches per contactor) for the eight HVDC dummy load contactors required for the simulator implementation. A preferred approach is to use a contactor rated closer to the 75 ampere requirement. The manufacturer (Hartman) providing the 400 ampere contactor is presently investigating the adequacy and availability of an A-754-R series contactor for this application, i.e., a rating of 100 amperes at 270 VDC for the laboratory environment application. The coil voltage would remain at 28 VDC as currently used in the present A-754 contactor design.

2. Relay Driver

A device which provides the relay driver function is required. This device is certainly within the state-of-the-art, but requires design and fabrication. As previously stated, estimated driver load requirements are to switch 3.5 amperes at 28 VDC for 500 milliseconds and 0.4 amperes at 28 VDC continuous. The input control circuitry of the driver must be compatible with SCG terminal interface.

3. Load Bank

Figure 15 depicts the approximate load requirements needed for the supplementary loading of the PGS. Variable loads are desirable but not mandatory. Load power factors should be comparable to those used for testing the ADM generator and converter/inverter equipment. Use of existing NADC load banks is recommended to the extent of their availability and adequacy.

2.3.3 Simulator Grounding Requirements

Grounding philosophy to be employed on the AAES Simulator should include provisions for personnel safety and proper operation of equipment. To provide optimum safety to personnel, the simulator structure should be connected to earth ground or to some conducting body which serves in place of the earth. It is expected commercial Power (110/220 VAC, 60 Hz) operated equipment such as drills, lamps, power supplies, etc., will be used in the vicinity and on the simulator. A faulty equipment could result in the simulator being at commercial power potential if the simulator is not connected to earth.

All equipment enclosures should be electrically connected to the simulator structure. This is to preclude the housing being at some high potential due to an internal power-to-case fault. All equipment circuit grounds should be connected to the simulator structure. Equipment circuit grounds having isolated (different) power supplies should use separate ground terminals. For example, the 28 VDC ground and 115/200 VAC ground should not share the same ground terminal. Single point grounds should be used in applications where equipment operation is sensitive to EMI. Grounds isolated from the structure is permissible (from a personnel safety view point) in systems operating at not more than 30 volts (AC or DC) between conductors.

The use of a "shock hazard detection system" needs to be investigated. A shock hazard monitor would automatically disconnect the power source from the simulator in the event that the simulator structure is above ground potential.

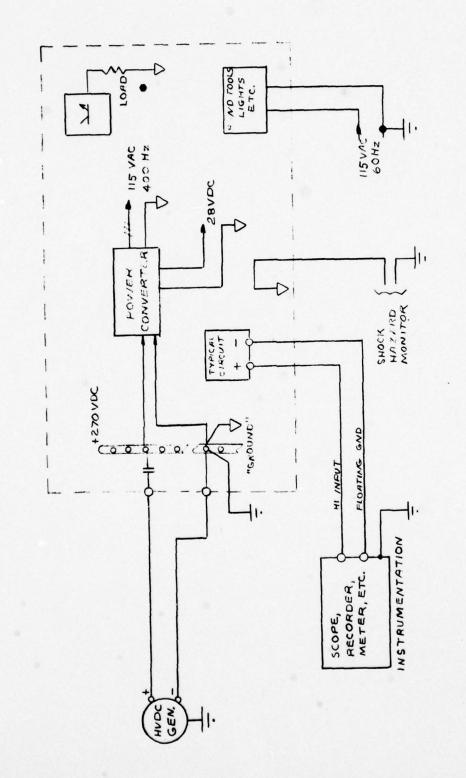
It is recommended that the PGS (270 VDC) power ground not be tied to the earth ground at the generator but at the earth ground point on the simulator. It is further recommended that the simulator structure not be used as the ground return for signal and HVDC power circuits. Instrumentation equipment should use a floating ground that is tied to the simulator common earth ground point with a sufficiently large conductor to minimize instrumentation error (based on instrumentation impedance circuit). The instrumentation equipment enclosure(s) should be tied to earth ground for safety. The grounding concept and requirements are schematically depicted in Figure 16.

2.3.4 A-7 Engine Pad Requirements

An assessment was made concerning the mounting drive requirements for the HVDC generator for application on the A-7. Interface and performance requirements were established for TA-7C (TF30-P-408 Engine) and the A-7E (TF41-A-2 Engine). These requirements are contained in Appendix A. Additionally, data was obtained on a gear box which has the potential for being used for interfacing the HVDC generator to the A-7 pad. The candidate gear box will provide the approximate required speed range; however, availability and torque requirements were not fully established. The gear box was used in conjunction with the 20 KVA VSCF Generator, General Electric Model No. 2CM38 and is illustrated in Figure 17. Availability and full compliance to AAES TA-7C system requirements should be established upon solidifying of the Flight Test Program Plans.

2.4 System Control and I/O Interface Requirements

The control logic in the form of Boolean combinational and sequential equations was prepared in conjunction with design of the AAES TA-7C subsystems and circuits. The formats and form in which these control equations were prepared are discussed in the subsequent paragraphs. Examples of methods for implementing and solving these equations using a one-bit processor and a more general purpose type processor are also provided. In addition, techniques were established for accomplishing the signal source function in the absence of a full complement of ADM solid state devices. Simulated signal sources, signal adapters and general purpose signal source panels, and airframe signal sources are defined for these purposes. Special purpose power output switches and lamp driver circuits are used for achieving the required interface between the demultiplexer and various aircraft "low power" loads. These devices and applications are described in the following paragraphs.



• Structure Return vs Conductor Ground Return to be Established on Circuit by Circuit Basis.

Simulator Ground

-0

___ Earth Ground

(Structure)

FIGURE 16 - SIMULATOR GROUNDING REQUIREMENTS

20KVA VSCF GENERATOR (MODEL NO. 2CM381) FIGURE 17 -

GEZ-5206A-2

TABLE 3
AAES SIMULATOR TYPICAL CONTROL EQUATIONS

[].

VETENBEIS SOLUTIONS	SHOILMING TOBLEGO	
	PRESENT FORMT	TAMBOT TERRAD
	MACART = (0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0), Z1270/ Z1250 = DHEACP/	
Carolina ca	MACADP = (0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0), Z1271/ Z1271 = DHSACD * "(PASDC1 + PASDC2)"/	MIAPT = DESACP, M(NOODCOODCOODCOO)/ MOIADP = DESACP + (PASTC) + PASTC) M(NOODCOODCOOL)
ENERGENCY ACCIMILATOR TEST	MALFIC - 21272/	NOTFIC = MOSISO + ICSELT/
	21272 - MISISO + LCSTLT/	MOTAIC = MOSISO + ICSALT/
	NOTAIC = 21273/	
	21273 = MASISO + LOSAII/	
	/46212 (N.O.N.N.N.O.N.N.O.N.N.O.N.N.O.) = OIEIHW	
	212301 + WISPR + WISCX + LOSFLZ/	WHEELO = WHSTPR + WHSLOX + LCSFLT, M(HOWSHOCHCHRA)/
83-80330-42	WHIALO = (N,N,N,O,N,N,O,N,N,O,N,N,N,N,O,N), 21295/	WHIALO = WHSAPR + WHSLOX + LOSALE, M(NOTOWNOWNOWNOWN)/
LIQUID OXIGEN GAGING	Z1295 = WHSAPR + WHSLOX + LCSALT/	WHIEMR = M(101110110111)/
	WHIFWR = (1,1,1,0,1,1,0,1,1,0,1,1,1,1,1,0,1)/	•
	FWIEAY = (M,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0,0	FALRAY = YACSEL * -LOSPLE + -YACSEL * LOSFLE, M(TOCCOCCOCCTICCON)/
	Z1006 - MACSEL * "LOSFLT" + "MACSEL" * LOSFLT/	YACSEL = (YACLEN + YACLAF) * -YACSEL + -(YACLEN + YACLAF) * YACSEL/
63-80330-720	YACSEL = (YACIF# + TACIAF) * "YACSEL" + "(YACIF# + YACIAF)" * YACSEL/	YACIEW = PWSPAC * -YACP/
CCMAND TRANSFER - AUTO CARRIER LANDING	YACLEW = FWSFAC * "YACF"/	YACIAF - FASAAC * -YACA/
	YACIAF = FWSAAC * "YACA"/	YACF = FASFAC, T:1(0.01)/
	II(1), YACF = FASFAC /	YACA = FASAAC, T:1(0.01)/
	TI(1), YACA = FVSAAC /	

2.4.1 System Control Equations

The control requirements were developed for each of the TA-7C subsystems designed for the AAES Simulator. This design information was prepared on keypunch coding forms. Table 3 contains typical Boolean equations which are used for control of the AAES TA-7C Simulator subsystems and circuits. Shown in the table are the form of the equations as currently written and the format to which they will be modified on the Full Simulator Development Contract. The change in format is required for achieving compatibility with the SCG hardware currently under development by the Garrett Corporation. Upon being updated to the required format and checked for completeness/correctness, the equations will be key-punched for listing. Both the listings and punched cards will be delivered on the Full Simulator Development contract. The basic control equations will also be shown on the wiring diagram drawings which are described in paragraph 2.2.

In addition to the basic system control equations SCG modifier equations were prepared for providing the load management control capability. These are also written on key-punch coding forms. These, like the basic Boolean control equations, will be revised to the Powertran format required by the SCG ADM hardware and key-punched. Listings will be prepared and the punched cards delivered under the Full Simulator Development contract.

Since four different (nonsimultaneous) checkout groups will be used to verify operation of all simulator subsystems, four separate sets of software are used for the SCG processor. In addition, one processor software set is used for the full-up simulator configuration. In that the basic Boolean equation for any specific load does not change between checkout groups (or full-up configuration), the difference between the five software sets is:

- a) the correlation between SCG terminal channels and input/output variable names, and
- b) activation or use of the applicable Boolean equations of the full complement.

The software "interface" data to be delivered with the simulator basically consists of the Boolean equations, equation modifiers, terminal bus address assignments and terminal channel assignments. This data will allow compilation of the operational software for the SCG processors using the POWERTRAN programming language. The control data to be delivered with the simulator will also define:

- a) the applicable checkout groups for each Boolean equation and equation modifier,
- the variable name assigned to each terminal channel for each of the four checkout groups; and
- c) the terminal bus address assignment for each checkout group.

It is noted that definition of terminal bus addresses and channel assignments for the full-up configuration cannot be completed until the final configuration and procured quantities of the SCG hardware are defined. Specifically, the SCG configuration variations yet to be fully established are the universal terminal concept versus the present dedicated multiplex or demultiplex terminal concept and subsequently the mix of dedicated multiplex, demultiplex, and multiplex/demultiplex terminals versus universal terminals.

As a means for more specifically establishing the computational capability and memory requirements needed by the SCG Processor for solving combinational/sequential logic control equations an analysis was conducted. The Z80 instruction set and the ICU one bit processor instruction set were compared for two different approaches for solving a typical sequential logic problem. These two approaches are: (1) a flow chart implementation and (2) a Boolean next state equation implementation.. The flow chart method proved to be the most efficient approach for solving the sequential logic problem for both processor instruction set implementations as is illustrated in Table 4.

SUMMARY OF MEMORY REQUIREMENTS AND EXECUTION TIMES FOR SEQUENTIAL EQUATION SOLUTION

TABLE 4

		BOOLEAN EQUATION METHOD			
MEMORY (BITS)	EXECUTION TIME µs	HEHORY (BITS)	EXECUTION TIME µs		
496	34-70	1280	.112–150		
360	20	450	25		
	(BITS) 496	(BITS) TIME µs 496 34-70	(BITS) TIME (BITS) 496 34-70 1280		

The memory requirements are given in terms of total bits since the word length is not the same for the Z80 and ICU. The Z80 memory is organized as an 8 bit byte, however, the ICU would be organized as an 18 bit word.

The ICU one bit processor proved to be much more efficient in terms of memory required and execution time; 20 microseconds execution time compared to 34 to 70 microseconds for the Z80, and 360 bits compared to 496 bits for the Z80 memory. There was even greater improvement in the ICU over the Z80 for the Boolean equation approach; 25 microseconds compared to 112 to 150 microseconds for the Z80, and 450 bits compared to 1280 bits of memory for the Z80.

It is noted that the Boolean equation approach requires six temporary scratch pad locations for implementation of software flip-flops and partial results. Only one temporary memory location was used in the flow diagram approach.

If a microprocessor is used for equation solutions, it is recommended that a one bit processor be used or an optimized Boolean solution instruction set be micro coded in a general processor for solving Boolean equations whether combinational or sequential.

In solving sequential Boolean equations, the flow chart approach proved to be more efficient than the Boolean logic method (20 words and 20 microseconds versus 25 words and 25 microseconds, respectively). This approach although more efficient, differs from the current equation solution approach where the computer compiler program takes the control equations and automatically generates the equation solution instructions. If the flow diagram approach is used, the flow diagram must be made for each sequential function and the program coded based on the flow diagram. A new compiler program could be written to do the compiling of the sequential equation functions based on the flow diagram algorithms, however, because of the limited number of sequential equations, the cost of this compiler would be difficult to justify. Standard combinational logic equations are generally solved as simply using the Boolean equation flow approach as compared to the flow chart method.

Sequential equations are basically ones that depend on memory elements. The memory elements can be provided by the scratch pad memory. Since the SCG specification requires a capability for 20 percent of the equations to be sequential with or without time delays, and one memory element per equation is assumed, then the processor requires about 200 locations in the scratch pad memory for the sequential circuits. When the requirement for time delays, partial solution to combinational logic, etc., are added, the processor scratch pad memory requirement is about 500 bits.

2.4.1.1 Sequential Circuit Implementation Example

The Automatic Carrier Landing System (ACLS) in the two-place TA-7C is controlled by either the Forward or Aft control panels. A push button switch is provided in both cockpits for alternately selecting either the Forward or Aft control panel for control of the Automatic Carrier Landing System. Each push button switch may be used to select or de-select control of the ACLS. Control is always given to either the Forward or Aft control panels. The push button switch is used to toggle this control from forward to aft or vise versa. Transfer of control is not allowed until the command - transfer pushbutton switch is released after having been activated.

The input and output variables for the sequential logic problem are defined below.

FWSFAC - Forward ACLS Command Transfer Switch

FWSAAC - Aft ACLS Command Transfer Switch

YACSEL - ACLS Control - Cockpit Select Transfer Command

The flow chart for the sequential circuit is shown in Table 5. Note that dummy variables FLG1 and FLG2 are used for implementing the sequential function. FLG1 is used to remember that FWSFAC has been activated. The transfer of control is initiated only after FWSFAC is deactivated provided that FLG1 was previously set by having activated FWSFAC. FLG2 serves the same purpose as FLG1 for the FWSAAC AFT ACLS command transfer switch.

Programming of this flow diagram for the 280 microcomputer is shown in Table 5a, and for the 1-bit ICU processor in Table 5b.

The programming with the Z80 instruction set makes use of the bit set, reset and bit test instructions for an eight bit byte while the ICU

instruction set addresses each bit directly. Note that the ICU has a unique output enable (OEN) instruction which disables output store commands if the output enable variable is false. This enables the ICU to efficiently implement flow diagrams without branch on condition instructions.

The Boolean equation approach for the sequential circuit design is shown in Table 6. The equations, when implemented with software, perform the same seq ential logic function as the flow diagram described previously.

Dummy variables FLG1, FLG2, S1, S2, and R1, R2 are used to control the sequential operation. The FLG1 and FLG2 equations are RS flip-flops which remember that the command transfer switches (FWSFAC and FWSAAC) have been activated. Equations S1 and S2 are partial solutions used in the toggle flip-flop equation YACSEL. Variables R1 and R2 are used to reset the FLG1 and FLG2 RS flip-flops after the command transfer switches have been released and control transfer has been completed.

TABLE 5

FLOW CHART SOLUTION
FOR SEQUENTIAL CIRCUIT

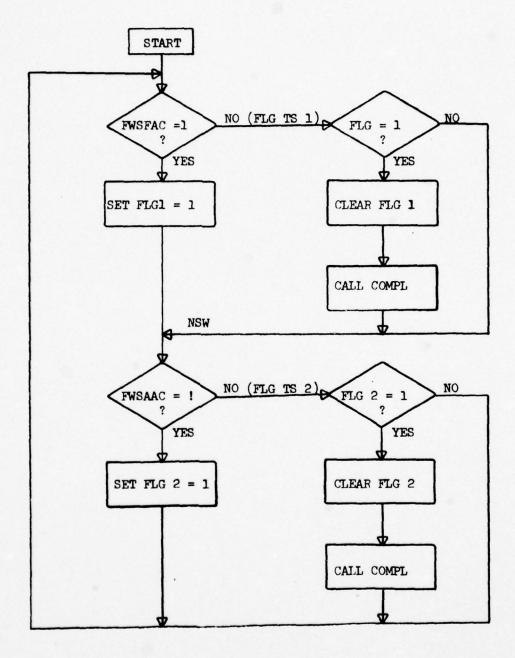


TABLE 5 (Continued)

FLOW CHART SOLUTION FOR SEQUENTIAL CIRCUIT

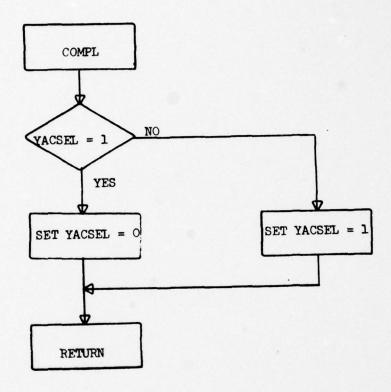


TABLE 5a

FLOW CHART SOLUTION USING Z80 INSTRUCTION SET

0	BYTE ADDR.	BYTE 0			T BYTES/STATES
	START	LD A, (STATUS) LD HL, DABYTI	;	Get status byte Get SWI Byte Address	3/13 3/16
In		BIT FWSFAC, (HL)	;	Is FWSFAC on?	2/12
111		JR Z, FLGTS1	;	Jump if no	2/7
14		SET FLG1, A		Set FLG1 in status byte	2/8
0		JR NSW	•	Jump to next switch	2/12
Ш	FLGTS1	BIT FLG1, A	;	FLG1 Bit Set?	2/8
		JR Z, NSW	;	Jump if no	2/7
10	(28 Total Instructions	RES, FLG1, A	;	Clear FLG1	2/8
II	for Sequential Circuit)	CALL COMPL	;	Complement control bit	3/17
	NSW	LD HL, DABYTZ		Get SW2 byte address	3/16
П		BIT FWSAAC, (HL)		Is FWSAAC on?	2/12
Ш		JR Z, FLGTS2		Jump if no	2/7
		SET FLG2, A	;	Set FLG2 in status word	2/8
177	SAVE:	LD (STATUS), A		Save status word	3/13
2.4		JR START	;	Repeat	2/12
П	FLGTS2	BIT FLG2, A		FLG2 bit set?	2/8
L		JR Z, SAVE		Jump if no	2/7
		RES FLG2, A		Clear FLC?	2/8
17		CALL COMPL		Complement Bit control	3/17
U		JR SAVE	;	Return	2/12
-	COMPL	LD HL, OUTBYT 1		Get contl bit byte addre	ss 3/16
		BIT YACSEL, (HL)		Is bit set?	2/12
U		JR Z SET		Jump if no	2/7
		RES YACSEL, (HL)		Clear contl bit	2/8
1		RET			1/10
n	SET	SET YACSEL, (HL) RET	;	Set contl bit	2/15 1/10
U	STATUS	PEFB 1		Flag byte location	1/0
-	DABYT1	EQU ADDSW1		Address of byte containi	
11	FWSFAC	EQU BITSW1		Bit containing FWSFAC	
U	FLG1	EQU O		Bit O equal FLG1	
	FLG2	EQU 1		Bit 1 equal FLG2	
17	DABYT2	EQU ADDSW2		Address of byte containi	ng SW2
U	FWSAAC	EQU BITSW2		Bit containing FWSAAC	
	OUTBYT1	EQU ADDCTL		Address of byte containi	ng YACSEL
П	YACSEL	EQU BITCTL	i	Bit containing YACSEL Fu	nction .
17					

TABLE 5a (Continued)

FLOW CHART SOLUTION USING Z80 INSTRUCTION SET

Assumption made for this program:

- Input variables FWSFAC and FWSAAC are bits located in ITRAM, but not in same byte.
- 2. Output function YACSEL is a bit in the ORAM.
- 3. FLG1 and FLG2 bits are located in the same status byte in temporary RAM.
- 4. T State = 1 clock cycle = 0.25 µsec

TOTAL MEMORY = 62 BYTES

Longest exec time = (281×0.25) = $70.25 \mu s$

Shortest exec time = $(136 \times 0.25) = 34 \mu s$

TABLE 5b

FLOW CHART SOLUTION USING ICU ONE BIT PROCESSOR INSTRUCTION SET

START	LD FWSFAC	; Load	FWSFAC
	STOC TEMP	; Save	FWSFAC
	OEN RR	; Enab	le output 1F RR = 1
	STO FLG1		
	LD TEMP	; Load	FWSFAC
	AND FLG1	; And	FLG1
	OEN RR	; Enab	le output if RR = 1
	STOC FLG1		
	LD YACSEL	; Load	YACSEL
	STOC YACSEL	; Comp	olement YACSEL
	LD FWSAAC	; Load	1 FWSAAC
	STOC TEMP	; Save	FWSAAC
	OEN RR	; En al	ole output if RR = 1
	STO FLG2		
	LD TEMP	; Load	1 FWSAAC
	AND FLG2	; And	FLG2
	OEN RR	; En al	ole output if RR = 1
	STOC FLAG2		
	LD YACSEL	; Load	d YACSEL
	STOC YACSEL	; Com	plement YACSEL
	JMP START		

Total Memory = 20 Words Execution Time = 20 μ s

18 bit words for 16K bit address field and 4 bit OPT code

TABLE 6

BOOLEAN EQUATION SOLUTION FOR SEQUENTIAL CIRCUIT

 $FLG1 = FWSFAC + \overline{R1} * FLG1$

 $FLG2 = FWSAAC + \overline{R2} * FLG2$

S1 = FLG1 * FWSFAC

S2 = FLG2 * FWSAAC

YACSEL = $(S1 + S2) * \overline{YACSEL} + \overline{(S1 + S2)} * YACSEL$

R1 = FWSFAC

R2 = FWSAAC

TABLE 6a

BOOLEAN EQUATION SOLUTION USING
Z80 INSTRUCTION SET

-					_
n					T BYTES/STATES
2-2	1	START	LD A, (STATUS)	; Get status	3/13
F)			LD HL, DATBYT1	; Get byte addr.	3/16
11			BIT FWSFAC, (HL)	: Is FWSFAC on?	2/12
U			JR Z, NXT1	; Jump if no	2/7
		SET1	SET FLG1, A	; Set FLG1	2/8
17		OUT1	LD (STATUS), A	; Save status	3/13
U	(a)		JR FLG2EQ	; Solve next equation	2/12
	FLG1	NXT1	BIT R1, A	; Is R1 set?	2/8
n	(14 instructions)		JR NZ, ZRO1	; Jump if yes	2/7
11	EXEC TIME		BIT FLG1, A	; Is FLG1 set?	2/8
No. of	EXEC TIME		JR Z, ZRO1	; Jump if no	2/7
-	20,25 -		JR SET1	; Set FLG1	2/12
11	27.7 µs	ZRO1	RES FLG1, A	; Clear FLG1	2/8
U	27.7 μs		JR OUT1	; Save status and return	2/12
0		FLG2EQ	LD HL, DATBYT2	; Get byte addr.	3/16
11			BIT FWSAAC, (HL)	: Is FWSAAC set?	2/12
-			JR. Z, NXT2	; Jump if no	2/7
0		SET2	SET FLG2, A	: Set FLG2	2/8
11		OUT2	LD (STATUS), A	: Save status	3/13
11	FLG2		JR S2EQ	; Solve next equation	2/12
	(13 instructions)	NXT2	BIT R2, A	Test R2	2/8
11			JR NZ, ZRO2	; Jump if not zero	2/12
U	EXEC TIME		BIT FIG2, A	; Test FLG2	2/8
	=		JR Z, ZRO2	; Jump if zero	2/7
0	17 -		JR SET 2,	; Set FLG2	2/12
	28.75 µs	ZRO2	RES FLG2, A	; Clear FLG2	2/8
			JR OUT2	; Save and return	2/12
		S2EQ	BIT FLG2, A	: Test FLG2	2/8
	S2		JR Z, ZRO3	; Jump if zero	2/7
	(9 instructions)		BIT FWSAAC, (HL)	; Test FWSAAC	2/12
0	EXEC TIME		JR NZ, ZRO3	; Jump if not zero	2/7
U	-		SET S2, A	; Set S2	2/8
	15 -	OUT3	LD (STATUS), A	; Save status and	3/13
1	16.75 µs		JR S1EQ	; Next Equation	2/12
		ZRO3	RES S2, A	; Zero answer	2/8
			JR OUT3	;	2/12
0		SIEQ	BIT FLG1, A	; Test FLG1	2/8
	S1		JR Z, ZRO4	; Jump if zero	2/7
	(10 instructions)		LD HL, DATBYT1	; Get Byte address	3/16
0	EXEC TIME		BIT FWSFAC, (HL)	; Is FWSFAC on?	2/12
11	EAEC IIME		JR NZ, ZRO4	; Jump if on	2/7
-	15 -		SET S1, A	; One answer	2/8
-	23.75 μs	OUT4	LD (STATUS), A	; Save status	3/13
11	23.75 μο	ano.	JR YACEQ	; Next equation	2/12
C		ZRO4	RES S1, A	; Zero answer	2/9
			JR OUT4		2/12

TABLE 6a (Continued)

BOOLEAN EQUATION SOLUTION USING Z80 INSTRUCTION SET

		TOO INDINCOTION BEI			
D e					T BYTES/STATES
					DITES/STATES
G .	YACEQ	LD HL, OUTBYT1		Get byte address	3/16
n		BIT YACSEL, (HL)	•	Is YACSEL set?	2/12
YACSEL		JR Z, NXT3		Jump if no	2/7
(14 instructions)		BIT S1, A		Test S1	2/8
		JR NZ, NXT3		Jump if not zero	2/7
EXEC TIME		BIT S2, A		Is S2 set?	2/8
_		JR NZ, NXT3		Jump if yes	2/7
21.25 -	OUT5	SET YACSEL, (HL)	•	Set ORAM Bit	2/8
27.5 μs		JR EQR1		Next equation	2/12
	NXT3	BIT S1, A	•	Is S1 set?	2/8
		JR NZ, OUT5	•	Jump if yes	2/7
		BIT S2, A		Is S2 set?	2/8
14		JR NZ, OUT5	•	Jump if yes	2/7
U		RES YACSEL, (HL)	:	Clear ORAM Bit	2/15
p.1	EQR1	LD HL, DATBYT1	;	Get byte address	3/16
R1		BIT FWSFAC, (HL)	;	Test FWSFAC	2/8
(6 instructions) EXEC TIME		JR NZ, ZRO5	;	Jump if not zero	2/7
EXEC TIME		SET R1, A	;	Set R1	2/8
		JR EQ R2	;	Next equation	2/12
12.75 µs	ZRO5	RES R1, A	;	Clear R1	2/8
9.75 µs					
	1				
U	EQR2	LD HL, DATBYT2	;	Get byte address	3/16
		BIT FWSAAC, (HL)	;	Test FWSAAC	2/12
7		JR NZ, ZRO6	;	Jump if set	2/7
		SET R2, A	;	Set R2	2/8
		JP START	;	Repeat	3/10
П	ZRO6	RES R2, A	;	Clear R2	2/8
		JP START	;	Repeat	3/10
D 8	STATUS	DEFB 0	;	Status location	1/0
	DATBYT1	EQU ADDSW1	;	Address of byte conta	
U	FWSFAC	EQU BITSW1	;	Bit containing FWSFA	0
	FLG1	EQU 1	;	Bit 1	
	FLG2	EQU 2	;	Bit 2	
	S1	EQU 3			
	S2	EQU 4			
	R1	EQU 5			
	R2	EQU 6			
	YACSEL	EQU BITCTL	;	Bit in ORAM for cont	
6	OUTBYT1	EQU ADDCTL	;	Address of byte conta	aining YACSEL
	DATBYT2	EQU ADDSW2			
			TO	TAL BYTES - 160 BYTES	

Longest Exec time = 150.45 μs Shortest Exec time = 111.5 μs

TABLE 6b

BOOLEAN EQUATION SOLUTION USING MOTOROLA ICU ONE-BIT PROCESSOR

FLG1	START	LDC R1	;	Load Complement R1
4 instructions		AND FLG1	;	and FLG1
$ET = 4 \mu s$		OR FWSFAC	;	Or FWSFAC
		STO FLG1	;	Store in FLG1
FLG2		LDC R2	,	Load complement R2
4 instructions		AND FLG2	;	And with FLG2
		OR FWSAAC	;	Or with FWSAAC
$ET = 4 \mu s$		STO FLG2	;	Store in FLG2
S1		LDC FWSFAC	:	Load Complement FWSFAC
3 instructions		AND FLG1		And with FLG1
$ET = 3 \mu s$		STO S1	i	Store in S1
S2		LDC FWSAAC	;	Load complement FWSAAC
31 instructions		AND FLG2	•	And with FLG2
$ET = 3 \mu s$		STO S2	;	Store in S2
VACCET		LD S1	;	Load S1
YACSEL		OR S2		Or with S2
6 instructions		STO TEM		Store in tem
$ET = 6 \mu s$		LD YACSEL		Load YACSEL
		XNOR TEM		Exclusive or with YACSEL
		STO YACSEL	i	Store in YACSEL
R1		LDC FWSFAC	,	Load complement FWSFAC
2 instructions ET = 2 μs		STO R1	í	Store in R1
R2		LDC FWSAAC	,	Load complement FWSAAC
3 instructions		STO R1		Store in R1
ET = 3 μs		JMP START	;	Repeat
			TOT	TAL MEMORY = 25 WORDS
			EXE	ECUTION TIME = 25 µs

2.4.2 Signal Source Implementation Methods

A wide variety of signal source types and installation designs are used in the TA-7C. As identified in Table 7, several design alternatives exist for the AAES signal source implementation. These include replacement of the conventional switch function with a solid state signal source, adding resistors to the existing contact type switch to provide the signal source function, and using external signal conditioning. The advantages and disadvantages of each design approach are listed in Table 7. The use of solid state transducers are preferred. However, due to the limited quantities of signal sources and also because of retrofit difficulty in some equipments, either the simulated signal source or external conditioning approaches are used. Retrofit difficulty is typically a result of unique switch physical configuration or inaccessibility of the switch, i.e., in an actuator, avionic subsystem, etc. Figure 18 is representative of both of these cases. Table 8 provides a summary of the switch types needed for this representative application and the implementation alternatives.

Because of the limited types, quantities and initial inavailability of ADM signal sources being procured for the simulator, simulated signals sources and "existing switches" buffered with signal conditioning circuits will be used on the simulator. The evolved system designs described in paragraph 2.2 are based on using these methods to achieve a "full-up" implementation of signal sources in the simulator. A total of 152 signal sources consisting of 5 types are used in the simulator system.

2.4.2.1 General Purpose Signal Source Panels

The transducers associated with airframe actuated functions cannot feasibly be implemented on the simulator. Typical of these functions are landing gear and control surface position sensing transducers. The simulator design uses toggle and rotary signal sources mounted on three special purpose panels to provide the input signals to the SCG for these type functions. This allows representative system operation without the need for the large, complex and costly mechanization of the moving surfaces and pressurized fluid subsystems. However, the general purpose panels are minimally used since their application is restricted to functions which are not an integral part of the simulator.

2.4.2.2 Signal Conditioners

Signal conditioner cards were defined for achieving compatibility between the SCG and signals eminating from various avionic "black boxes". The subsystem and circuit designs were developed based on use of five signal conditioner assemblies. A total of 137 conditioner channels consisting of five types of conditioners are required for the "full-up" simulator. The system design and adapter harness assemblies are based on a full set of signal conditioners and simulated signal sources being supplied with the simulator. Thus, the only factor which requires use of the modular concept (in the input control area) is the reduced quantity of multiplex terminals needed for simultaneous operation of all simulator subsystems. Use of the signal conditioners in conjunction with the modular concept is depicted in Figure 19.

TABLE 7 COMPARISON OF CONVERSION APPROACHES

АРРКОАСН	ADVANTAGE	DISADVANTAGE
REPLACE WITH SOLID STATE TRANSDUCER	o BIT UP TO (& INCLUDING) SIGNAL SOURCE O REPRESENTATIVE OF FUTURE IMPLEMENTATION O AIRFRAME WIRING LESS COMPLEX O OVERALL SYSTEM MORE RELIABLE	o NON-STANDARD SIGNAL TRANSDUCERS o REWORK OF EQUIPMENT REQUIRED o HIGHEST INITIAL COST (RELATIVE COST = 50C) o REQUIRES EQUIPMENT TO BE AVAILABLE DURING SIMULATOR CONSTRUCTION
ADD RESISTOR NETWORK INTO EQUIPMENT	O BIT UP TO EQUIPMENT O AIRFRAME WIRING LESS COMPLEX O USE EXISTING EM SWITCHES O AIRFRAME PART OF SYSTEM REPRESENTATIVE OF FUTURE IMPLEMENTATION	o REMORK OF EQUIPMENT REQUIRED o MEDIUM INITIAL COST (RELATIVE COST = 5C) o RELIABILITY IMPACT OF SWITCHING LOW LEVEL SIGNALS o REQUIRES EQUIPMENT TO BE AVAILABLE DURING SIMULATOR CONSTRUCTION
USE EXTERNAL SIGNAL CONDITIONING	o LOW COST (RELATIVE COST = 1C) o USE EXISTING EQUIPMENT WITHOUT MODIFICATION o DOES NOT REQUIRE EQUIPMENT TO BE AVAILABLE DURING SIMULATOR CONSTRUCTION	O MORE COMPLEX AIRFRAME WIRING O LEAST RELIABLE O LIMITED BIT O NOT REPRESENTATIVE OF FUTURE IMPLEMENTATION

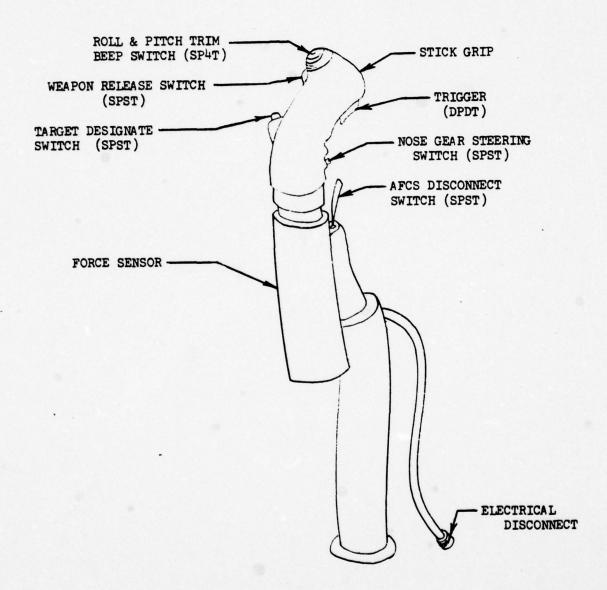


FIGURE 18
CONTROL STICK ASSEMBLY

TABLE 8 SIGNAL SOURCE CONVERSION EXAMPLE

CONTROL STICK ASSEMBLY

- O SIGNAL SOURCES TO INTERFACE WITH AAES
 - ROLL & PITCH TRIM SWITCH (SP4T) (MS27708-3)
 - WEAPON RELEASE SWITCH (SPST) (MS25089-4aR)
 - TARGET DESIGNATE SWITCH (SPST) (MS25089-5AR)
 - NOSE GEAR STEERING ENABLE SWITCH (SPST) (MS25089-4AR)
 - TRIGGER SWITCH (DPDT) (SPECIAL)
 - AFCS DISCONNECT SWITCH (SPST) (SPECIAL)
- o TECHNIQUES OF ADAPTION TO AAES
 - REPLACE EM SWITCH WITH SOLID STATE TRANSDUCER
 - ADD RESISTOR DIVIDER NETWORK IN STICK GRIP ASSEMBLY OR IN FORCE SENSOR
 - WIRE CONTROL STICK TO MUX TERMINAL VIA SIGNAL CONDITIONER CARD

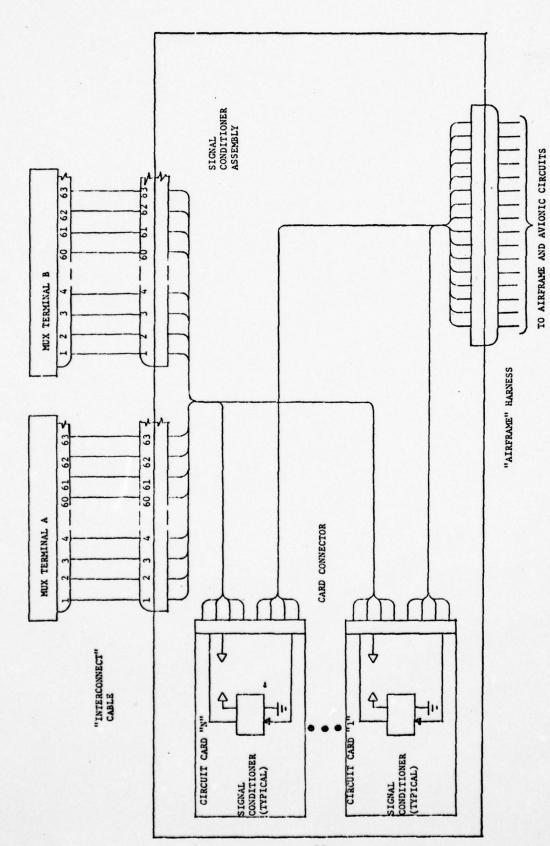
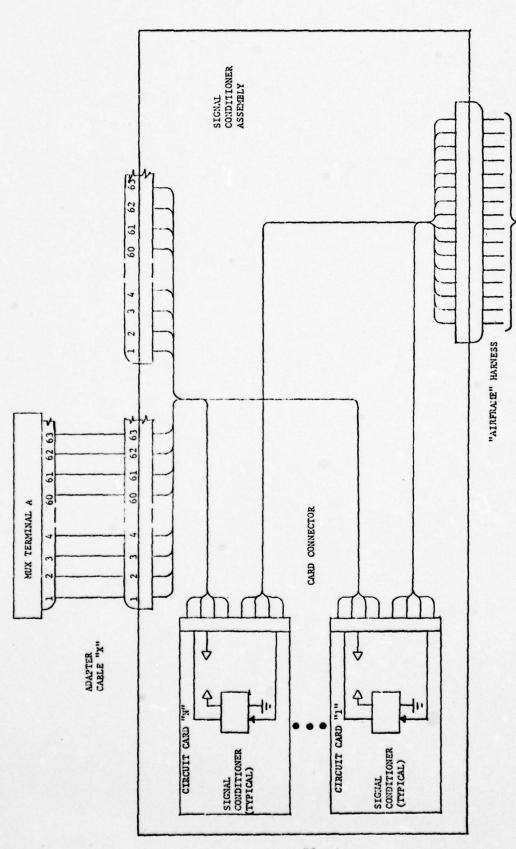


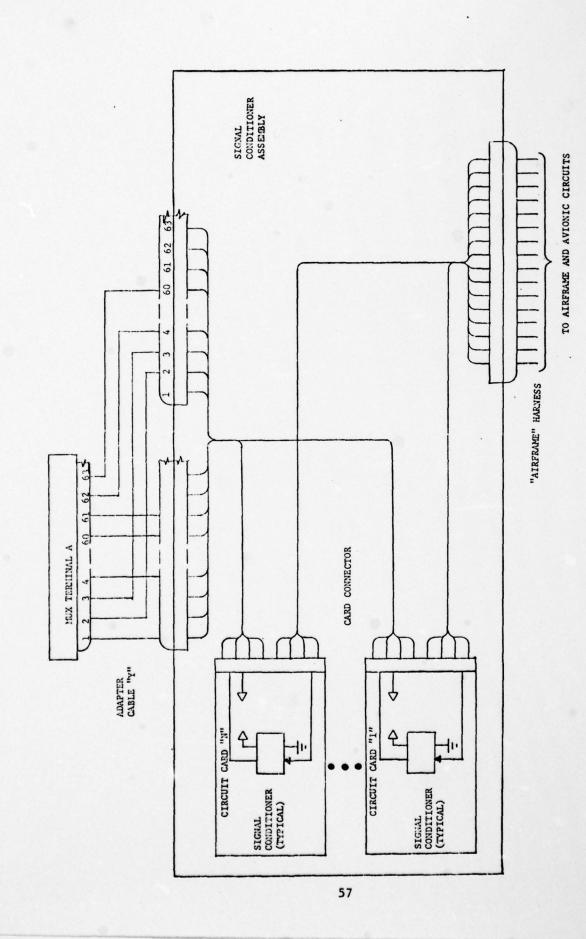
FIGURE 19 - SIGNAL CONDITIONER IMPLEMENTATION

(a) FULL-UP SIMULATOR



TO AIRFRAME AND AVIONIC CIRCUITS





(c) CHECKOUT GROUP Y FIGURE 19 - SIGNAL CONDITIONER IMPLEMENTATION

Figure 19a depicts the signal conditioner interface with the multiplex terminals and airframe harnessing for a full-up simulator configuration. As shown in the figure, the airframe harness connects directly to the signal conditioner assembly. The multiplex terminals, however, connect to the signal conditioner assembly through an interconnect cable. The primary factors requiring use of the interconnect cable is that the multiplex terminals must interface both the signal conditioner assembly and airframe harnesses for access to signal transducers mounted in various assemblies. This airframe harness interface eliminates the ability to connect the signal conditioner assembly harness directly to the multiplex terminals.

For the simulator interim configuration, the multiplex terminal-to-signal conditioner interconnect cable will be replaced by a series of adapter cables which connect the limited multiplex terminal channels to selected signal conditioners. Figures 19-b and 19-c illustrate use of adapter harnesses for reassignment of the available multiplex terminal channels for two representative checkout groups. Thus, by using adapter cables between the multiplex terminals and signal conditioner assemblies, all AAES Simulator subsystems can be operated and evaluated with the limited number of SCG multiplex terminals. The full-up simulator configuration is achieved (in the input control area) by inserting the "full-up" interconnect harness.

2.4.3 Load Controllers

The load controllers cannot be feasibly simulated as could the signal sources. Therefore, the simulator system and wire harness designs are based on sharing the available quantities of load controllers. This design approach was discussed in paragraph 2.1 under the modular design concept. To achieve the full-up system (in the output power and control areas) requires that full quantities of controllers be installed in the LMCs and removal of the two adapter harness associated with each LMC. A total of 342 controllers are required for the full-up simulator, however, a total of only 200 controllers (28VDC, 270VDC, 26VAC, and 115VAC) are required with the modular concept.

2.4.3.1 Power Output Switches

Application of the modular concept to the low level power output switches is comparable to the implementation concept used for signal conditioners. In both cases sufficient low-level power output devices will be fabricated to service the full-up simulator configuration. The limitation forcing use of the modular implementation is the limited number of demultiplex terminals. However, since the power output card assemblies are installed within the LMCs, the modular implementation is the same as that used for load controllers in paragraph 2.1.

The circuit interconnection for the low level power output switches corresponds to that shown in Figure 2-b through 2-d except a full quantity of drivers are provided. The only hardware sharing required is for terminal channels. For this reason, conversion between checkout groups in the initial simulator configuration is accomplished by changing adapter cables between the LMC (low level power output devices) and the demultiplex terminals and between the LMC and "airframe" harness. Rework of the initial simulator to the full-up arrangement only

requires removing the adapter cables associated with the LMC and reconnecting the associated SCG terminal, LMC and airframe harness connectors.

A quantity of 122 output drivers consisting of five basic types are used in the simulator design.

2.4.3.2 Solid State Lamp Drivers

The simulator system design is based on using a full set of lamp driver assemblies. The interconnect technique for the lamp drivers is the same as that used for the signal conditioning modules described in paragraph 2.4.2.2, Figures 19-a though 19-b. Conversion between the four checkout groups and the full-up simulator is achieved through interchanging the adapter harnesses. A total of 265 lamp drivers consisting of 3 types are used in the simulator.

2.4.4 Simulator Equipment Utilization

In order to provide an overview of the equipment requirements for both the full-up and the interim modular implementations, summary tables were prepared, Tables 9 and 10. Table 9 lists the ADM hardware requirements. Shown are the quantities of hardware being procured for each device and rating. Also shown are the quantity of hardware for the full-up and modular arrangements. Since the modular arrangement contains four checkout groups, the quantity of hardware "active" during each group is shown. It is further noted that the full-up and interim quantity of SCG terminals is based on the ADM "types" of hardware. If Universal Terminals are used in transitioning to the full-up system, a total of 19 will be required. Also, in the area of signal sources, the simulator will be initially implemented with a full set of Vought furnished simulated signal sources. The table does not reflect requirements that may occur in order to fully accommodate integration of the AAS (Advanced Armament System) capability.

Table 10 identifies the quantity of supplementary hardware required for the simulator. The supplementary equipment consists of the signal conditioners (5 types as shown), power output switches (5 types as shown), lamp drivers (3 types as shown) and the adapter cables. Since Vought is to supply a full-up set of the supplementary equipment items, the full-up and modular implementation quantities are the same. Since in most of the simulator system areas, the full-up arrangement is derived by removing adapter cables and connecting up the basic system wire harness connectors, only 6 interconnect harnesses are required for the full-up implementation.

Appendix B contains the list of GFE required for the simulator. Table B-1 is the baseline GFE recommended for inclusion on the simulator. These GFE items will allow checkout and evaluation of the systems and circuits which can be operated in a meaningful manner. Table B-2 contains a list of additional GFE that is relevant to the TA-7C simulator. However, these equipments cannot be "fully operated" or would be difficult to "adequately evaluate" as a result of basic limitations of the simulator. As an example, M61 gun clearing solenoid can be operated but should be loaded and checked for force and actuation time to fully determine if degradation of performance occurs as a result of the AAES implementation.

TABLE 9
ADM HARDWARE UTILIZATION

		Qty	Used				
	Qty		Modular	Syste	m Che	ckout	Group
Item	Procured	Full-Up	Checkout	1	2	3	4
SCG Equipment							
o Processors	2	2	2	2	2	2	2
o Maintenance Panel	1	1	1	1	1	1	1
o Pilot Control							
Panel	1	1	1	1	1	1	1
o Multiplexer	6	5	5 5	5 5 3	5	. 5	5 5
o Demultiplexer	6	11	5	5	5	5	5
o Mux/Demux	4	5	3	_	3	3	3
o Data Bus Couplers	AR	50	34	34	34	34	34
Power Controllers 28VDC Load Control							
o 1/2 Amp	25	38	22	10	20	13	13
o 2 Amp	45	83	41	17	35	25	25
o 5 Amp	15	29	15	4	5	8	7
o 10 Amp	15	20	10	8	0	0	2
115 VAC Load Control					1		
o 1/2 Amp	25	29	21	8	10	16	5
o 2 Amp	45	66	38	19	31	29	19
o 5 Amp	15	31	15	3	4	9	7
26 VAC Load Control							
o 1 Amp	15	16	13	1	5	10	6
270 VDC Load Control							
o 2 Amp	40	30	30	30	30	30	30
Signal Sources							
o Toggle (SPST)	65	51	51	17	29	27	31
o Toggle (SPDT)	0	27	27	5	7	11	16
o Pushbutton Ltd	65	45	45	17	0	27	16
o Rotary	35	18	18	18	0	0	0
o Proximity	35	14	14	6	6	13	12

Alternate total quantity is 19 universal terminals.

TABLE 10 SUPPLEMENTARY HARDWARE UTILIZATION

			Qty	Used				
		Qty		Modular	Syste	em Check	out Gr	oup
_	Item	Procured	Full-Up	Checkout	1	2	3	4
Si	gnal Conditioners							
0	Type 1 - Ground or Open/28VDC	43	43	43	6	18	14	14
0	Type 2 - Open/Ground	36	36	36	11	6	10	8
0	Type 3 - Open/Con- tinuity	44	44	44	11	23	9	11
0	Type 4 - Open/28VDC or Ground	12	12	12	12	0	0	0
5	Type 5 - Ground or Open/5VDC	2	2	2	2	0	2	0
Po	wer Output							
0	Type 1 - 28V, 400 ma	69	69	69	24	19	28	12
0	Type 2 - Grd, 250 ma	43	43	43	23	, 9	9	19
0	Type 3 - Grd, 2.5 a	3	3	3	1	0	1	1
0	Type 4 - SPDT, 100 m	a 2	2	2 5	0	0	2	0
0	Type 5 - 6V, 100 ma	5	5	5	0	0	5	0
La	mp Drivers							
0	Type 1 - 28V at 80 m	a 120	120	120	32	40	45	34
0	Type 2 - 6V at 400 m	a 133	133	133	75	0	58	23
0	Type 3 - 28V at 340	ma 6	6	6	0	6	2	0
Ad	apter Cables	AR	6	67	24	20	20	20

2.4.5 Load Management System

SOSTEL provides a capability for automatically adjusting power bus loading to match the generating system capacity. The load management capability greatly simplifies the bus management hardware requirements while providing a more sensitive bus loading control than can be feasibly implemented with conventional techniques. Reference 1 provides a discussion of the load management concept and identifies the benefits that it provides. The load management operation uses the inherent computerized control of SOSTEL for controlling the flow of power to individual loads. This allows loads to be powered-up or powered-down as a function of the power system capacity by providing the proper control equations in the SCG processors. Two sets of control data have been defined.

The first data set consists of the load management modifiers and are in accordance with the format of the Powertran Reference Manual². A load management modifier has been defined for essentially all of the SCG output control equations. The primary exceptions are the output terms which are always enabled. These are for the critical emergency loads that are energized if any power is available.

The load management modifier format is illustrated in Figure 20. As shown, sixteen management states are provided for load control. One of the sixteen states is active at all times and control the load action during that state by the following criteria:

- o Management character = N: Output equation is solved normally and the associated load controller state is set based on the equation solution.
- o Management character = S: Solution of output equation is skipped and the last state of the output is maintained. The load controller state is set based on the previous output state.
- o Management character = 0: The output equation is forced to a logic "0".

 The associated load controller is turned off and the load deenergized.
- o Management character = 1: The output equation is forced to a logic "1".

 The associated load controller is turned on and the load energized.

As previously stated each load (i.e., load controller) has an associated load management modifier. The total load connected to the power generating_conversion equipment is therefore limited to the sum of all loads which have a management character of N, S or l in the specific management level or state in effect. This is illustrated by the following example for four loads which have control equations of:

15 14 13 12 MANAGEMENT STATE LEVELS

			12	14	13	12		PIE	MAG	EFIENI STATE LEVELS	_
W =	Α,	M(N	0	1	0	•		•)	(load = 2KW)	
W =	В,	M(N	0	0	0		•)	(load = 1KW)	
W =	С,	M(0	N	1	0)	(load = .6KW)	
W =	D,	M(N	N	0	1)	(load = .2KW)	

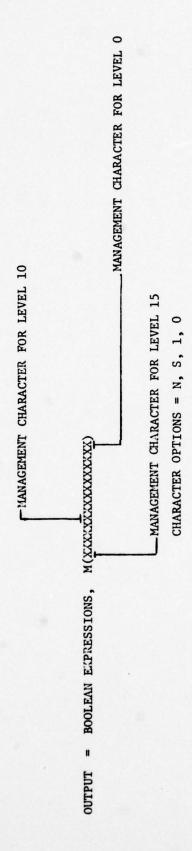


FIGURE 20 LOAD MANAGEMENT MODIFIER FORMAT

If management level 15 is selected and Λ , B, C and D are a logic 1, then the total load connected is 3.2 kilowatts; should the management state shift from level 15 to level 14, the connected load is reduced from 3.2 kW to 0.2 kW. If Λ , B, C and D are a logic 0, the connected load is zero for management levels 15 and 14, 2.6kW for level 13, and 0.2kW for level 12. In this manner, the total power demand on the main power buses can be adjusted by changing management states.

The second load management data set consists of equations which define management level selection.

Appendix C contains the preliminary equations which will be used to establish the management levels. Contained in the equations are terms which are functions of the aircraft flight mode, the PGS operational "health" state and the bus priority level. These equations will require refinement as more detailed or complete definition of the PGS health status functions and response characteristics become available. However, the equations as defined are illustrative of the control variables, time constants and management level operation. To the extent that PGS health signals are not available for automatically indicating the generator-power conditioner operational status, manually activated signal sources installed on the General Purpose Signal Source Panels can be used to simulate status. This will exercise the load management "load shedding" and "load addition" operation of the SCG but will not provide an effective evaluation-demonstration of the use of PGS sensed health parameters and associated PGS response characteristics.

Exercise of the load management operation will be somewhat limited during the initial simulator evaluation phase because of the lack of sufficient ADM hardware (SCG terminals and power controllers). The supplementary loading concept described in paragraph 2.3.2 however, minimizes this limitation. This can be accomplished by assigning load management modifiers to the supplementary loads. In this manner sufficient load changes can be made to occur during management level transitions to noticeably impact the generator-converter loading and consequently their level of performance.

Another factor which limits or perhaps complicates the load management operation on the simulator results from the power generation/conversion subsystem design. The PGS subsystem is being designed as basically a 45 kilowatt, dual channel, main system with no emergency power sources. In addition, the generators and converters can be operated in either a split synchronized or parallel mode. In either of these modes, load management will not typically initiate load shedding until the sum of the "present generating capacity" of both generators is less than the connected load. Since a dual channel system is typically designed so that either channel can power all connected loads, both generators would have to degrade to the point where the total generating capacity is less than 45 kilowatts. Therefore, load management will be exercised on the simulator only to the extent that supplementary loading on the main buses can increase the system load above 45 kilowatts.

The simulator design also includes provisions for a second PGS operational mode. In the second mode or alternate configuration, one channel serves as the main power source while the second channel serves as the emergency generator. Although this arrangement distorts the ratio of emergency power capacity to main power capacity, the impact and operation of power source switchover and load management can be evaluated for the single engine implementation. It is noted that for a"typical" single channel system having load management, the main power source load is reduced as a function of its "capacity to generate power". At the point where the degraded capacity of the main channel drops below the capacity available from the emergency source, the main source is disconnected (tripped) and the emergency source is brought

on line. The single channel system load centers (LMC) also typically contain an essential bus and a non-essential bus. The essential sub-bus is powered from the main and the emergency sources. However, the non-essential bus is powered only from the main source. When the main source trips and the emergency source is activated, the connected load drops by virtue of only the LMC essential bus being powered. In this case, the load management software will sense an underload on the emergency generator (main generator tripped). This will result in loads being added until the underload condition load is removed or until all emergency loads are enabled. The number of effective load management levels is doubled as a result of powering only the loads connected to the hardwired essential buses. Since the simulator is being designed for a limited quantity of load controllers and for dual channel operation, it is not practical to split the LMC buses between essential and non-essential. Therefore, the initial simulator design will in effect not employ a split (essential and non-essential) bus.

In order to address both the single channel and dual channel power system operating modes, the management level selection equations in Appendix C contain terms which modify the load management operation as a function of system operation mode. These terms appear in the overload and underload equations of Tables C-2 and C-3 and in the level modifier equations of Table C-5. These additional terms are derived from three cockpit mounted signal sources:

- (a) Load Management Enable,
- (b) Emergency Generator, and
- (c) Single/Dual Channel Mode

Table 11 contains a matrix which illustrates the load management operating mode for the various states of the three signal sources. This enables the load management routine to be exercised with the available simulator loads for both the dual channel and the single channel power system arrangement.

2.5 Avionic Multiplex System Definition

The Avionic Multiplex System (AMUX) provides data communication between the six avionic primary subsystems and seven secondary subsystems as listed in Tables 12-a and 12-b. The signals selected for multiplexing on the data bus represent a cross section of signal types and characteristics. Table 13 indicates the assignment of these signals to the four area multiplex terminals (AMTs). Given in Table 12 are the subsystem name, nomenclature and part numbers, and the location of equipment used in the signal list. The signal assignment list identifies the signal name and identification number, orgin and destination, and the general characteristics of each signal. Tables 13-a through 13-d are the assignments for the forward cockpit, aft cockpit, right avionics and left avionics terminals respectively. The candidate signals to be multiplexed are made up of 154 inputs and 178 outputs. Table 14 identifies the signal counts assigned to each terminal.

TABLE 11

LOAD MANAGEMENT OPERATING MODES

EL TRANSDUCER DUAL CHANNEL	FLIGHT PROFILE LEVEL AND THE	LOAD MANAGEMENT LEVEL 15 IS SELECTED FOR NORMAL OPERATION (I.E., ALL LOADS ENABLED.)
SINGLE/DUEL CHANNEL TRANSDUCER SINGLE CHANNEL DUA	BUS PRIORITY SELECTION AND FLIGHT PROFILE DETERMINES THE MANAGEMENT LEVEL AND THE ASSOCIATED CONNECTED LOAD.	MANAGEMENT LEVEL 1 SELECT MANAGEMENT LEVEL FORCED TO LEVEL 4 OR 8. MANAGEMENT LEVEL FORCED TO LEVEL 9.
EMERGENCY GENERATOR TRANS DUCER	OFF CRUISE TAKE-OFF OR LANDING	OFF CRUISE TAKE-OFF OR LANDING
LOAD MANAGEMENT TRANSDUCER	NO	OFF

TABLE 12

AVIONIC SYSTEMS MULTIPLEXED

(a) Primary Subsystems Interfaced

NO. OF			
UNITS	SUBSYSTEM NAME	PART NUMBER	LOCATION
	RADAR ALTINETER (APN-194)		
1	Receiver Transmitter	RT-1042/APN-194	RC
2	Indicator	ID-1760A/APN-194	INST (Fwd and Aft)
1	Interference Blanker	MX-9132A/APN-194	RC
	DIGITAL DATA COMMUNICATION (ASW-25)		
1	SINS/Waypoints Receptacle	MS3120E16-8S	LWW
1	Converter Receiver	CV-2230/ASW-25	RME
1	Coupler Converter	CU-1923/ASW-25	AMO
2	SINS/Waypoint Switch	215-21209-3	LCSL (Fwd and Aft)
2	Control	C-7100A/ASW-25	LCSL (Fwd and Aft)
	TACAN (ARN-84)		
1	Receiver Transmitter	RT-1022/ARN-84	RA
2	Control	C-9054/ARN-84	RCSL (Fwd and Aft)
1	Mount	MT-4354/ARN-84	RA
1	Antenna Switching Unit	SA-521A/A	RA
	IFF TRANSPONDER (APX-72)		
i	Receiver Transmitter	RT-859A/APX-72	RA
1*	Control	C6200A/APX	LCSL (Fwd and Aft)
i	MK XII Computer	KIT-1A/TSEC	RA
ī	Tester	TS-1843B/APX	RA
	UHF RADIO SET (ARC-159)		
2	Receiver Transmitter	RT-1150/ARC-159	RA
2	Control	C-9577/ARC-159	LCSL (Fwd and Aft)
2	Frequency Indicator	ID-1972/ARC-159	INST (Fwd and Aft)
	AUTOMATIC DIRECTION FINDER (ARA-50)		
2	Control	C-1457/ARR-40	LCSL
1	Antenna	AS-909/ARA-48	CD
1	Amplifier Relay	AM-3624/ARA-50	RA ·
1	Receiver	R-1286/ARR-69	RA

^{*} IFF Control will not be incorporated in aft cockpit.

TABLE 12

AVIONIC SYSTEMS MULTIPLEXED

(b) Secondary Subsystems Interfaced

NO. OF UNITS	SUBSYSTEM NAME	PART NUMBER	LOCATION
	HEAD-UP DISPLAY (AVQ-7)		
1	Signal Data Processor	CP-915/AVQ-7	LA
	NAV/WEP DELIVERY COMPUTER (ASN-91)		
1	NWDC	CP-952/ASN	LA
	INERTIAL MEASUREMENT SYSTEM (ASN-90)		
1	Adapter Power Supply	PP-6141/ASN-90	LA
	FORWARD LOOKING RADAR		
1	Sweep Generator	SG-811/APO-126	LME
	INTERCOMMUNICATION SET (AIC-25)		
1	Tone Generator	0-1595/A	RA
	AUTOMATIC FLIGHT CONTROL SYSTEM		
1	Roll Centrol Amplifier	AM-4353/ASW-26	LA
	HEADING MODE SYSTEM		
2 2	Attitude Director Indicator Horizontal Situation Indicator	ID-1329/A ID-1013/A	INST

ASSIGNMENT OF SIGNALS TO BE MULTIPLEXED TABLE 13a FWD COCKPIT AMT 1

SIGNAL NUMBER NAME		FROM	707 H	TO TINO	. 301	1486	VOL TAGE		UPDATE	•
CAT	INDICATOR ALT SELF TEST	RA/RT RA/RT	2 2	RA/IND	INST	DC ANA 01SC	+ 25 VDC, DV GROUND/OPEN	VDC, DV OPEN		5 14
INPUTS TO HMS/HSI										
FLA	RNG FLAG CONT	TAC/HT	A A	HMS/HSI	INST	0150	GR DUND / OPEN	OPEN	2	
TANC	E UNITS	TAC/MT	RA	HMS/HSI	INST	SYNCHR	11.8	VACAOV	•	
TANC	E TENS	TAC/HT	RA	HMS/HSI	INST	SYNCHR	11.8	VAC , DV	2	1
TANC	E HUNDS	TACIMT	RA	HMS/HSI	INST	SYNCHR	11.8	VACOO	•	_
AN B	EAPING	TACIMT	P.A	HMS/HSI	INST	SYNCHE	11.8	VAC, DV	2	13
IR SE	DEVIAT	TAC/HT	RA	HMS/HSI	INST	DC ANA	+1-200	MVDC	S	-
FLA	91	TAC/HT	RA	HMS/HSI	INST	0150	+380 6	+380 MVDC , DV	•	
FROM		TAC/MT	RA	HMS/HSI	INST	DC ANA	+/-300 HVDC	MVDC	2	-
S R SL	VEP ROT	TACIMT	RA	HKS/HSI	INST	SYNCHR	92	VAC, DV	•	-
INPUTS TO HMS/ADI										
35011 EL STEE 35034 LATEPAL	TEERING PAL ERROR	00C/CR	RAE	HMS/ADI HMS/ADI	INST	DC ANA	+/- 2.2VDC	SVDC	52	• •
OUTPUTS FROM DOC/S-W										
35004 WAYPOINTS	15	4-S/200	1631	DDC /RECPT	141	0150	+ 28	VDC, OPEN	•	-

			CABLE 13	TABLE 13a (cont)						
SIGNAL	7 A 3 E	FROM	25	TINU	201	TYPE	VOLTAGE		UPDATE	1 e
OUTPUTS FROM	DOCICENT	•								
	ANTI-JAP	DOCICONT	1631	00C/CR	RFE	0150	• •	VOC. OV		5
	SELEC	DDC/CONT	1531	DDC /CR	RAE	0150	+ 28	VDC, DV		•
35019 F	FREC SEL 0.1	1007000	1001	100 VC	N W	2010	• •	VOC. 0V		
		DOCACONT	1631	000 / CR	E E	0130		VDC 20V		
	FREG SEL 0.8	DOCICONT	16.51	00C/CR	PME	0150	•	VDC, DV		•
	SEL	DOCICONT	1531	DDC /CR	RME	0150		VDC, DV		2
	SEL	DDC/CONT	rcst	DDC/CR		0180	• •	, AD . DO		S
	SEL	DOC/CONT	רכצו	DDC/CR	RME	0150	•	VDC , DV		•
	SEL	1007200	וכפו	DDC /CK	E S	0150	•	VDC , UV		
	FRED SEL 10.0	1007200	1531	27,000	E 3	2510	• •	VOC. 0V		n .
	351 6	DOCACONT	100	000,00	KE	0150	+ 28	VDC-00V		
OUTPUTS FROM	IFF/CONT									
	SENSITIVIT CNT	IFF/CONT	1631	1FF /RT	8	0150	GROUND/OPEN	EN	•	_
	MODE 3/A ENABL	IFF/CONT	1631	IFF/RT	8	0150	GROUND/OPEN	EN	•	-
46003	MODE 2 ENABLE	IFF/CONT	יכנו	1FF/RT	8 .	0150	GROUND / OPEN		6	٦.
	, -	IFF/CONT		166/01	4 4	2510	SACONOLOR SACONO	2 2	n v	٠.
90094	U	IFF/CONT	1031	IFF/RT	4	0150	GROUND/OPEN	. N		
10095	OL.	IFF/CONT	1531	IFF/RI	RA	0150	GROUND/OPEN	EN		
80095	«	IFF/CUNT	1531	IFF /RT	RA	DISC	GROUND/OPEN	EN	•	-
4000	TOENT CONTROL	IFF/CONT	וכצו	IFF /COMP	4	2510	GROUND/GPEN	EN	.	٦.
46016	_	IF F/CONT		166/1510	4 4	2510	NE ADVONOUS	2 2		٠.
46017	MODE 2 TEST	IFF/CONT	1531	IFF/TSTR	. A	0150	GROUND/OPEN			
46018	MODE 3/A TEST	IFF/CONT	1631	JFF/15TP	RA	0150	GROUND/OPEN	EN	•	
61095	MODE C TEST	IFF/CONT	1631	IFF/TSTR	8	0150	GROUND/OPEN	EN	•	-
12095	AUDIO ENABLE	IFF/CONT	1631	1FF/RT	R.A	DISC.	GROUND/OPEN	EN	s	-
77094	MCAITOR CNIPL	IFF /CONT	ICSL	1FF/TSTR	RA	0150	GROUND/OPEN	EN	•	-
42044	HODE & TEST	I F / CONI	וכצר	IFF/RT	A .	0150	GP DUND / DP EN	Z	S	-
46030		IFF/CONT	153	IFF/COAP	4 4 2 a	2510	GROUND/OPEN	Z	o «	-
46031	MODE 1 AZ ENAR	1FF/CONT	1631	IFF/RT	*	0130	GPOUND/OPEN	Z Z	, "	

TABLE 13a(cont)

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			10				UPDATE	
×	UNIT	רפכ	UNIT	201	TYPE	VOLTAGE	KAIE	•
	IFF/CONT	1631	IFF/RT	R.A.	0150	GROUND/OPEN	•	-
7	FF/CON1	1631	1FF/RT	44	0150	GROUND/DPEN	•	-
=	FF /CONT	1631	IFF/RT	RA	0150	GROUND / OPEN	•	-
-	IFF/CONT	LCSL	IFF/RT	RA	0150	GROUNDIOPEN	•	-
-	FF/CONT.	1531	IFF/RT	RA	0150	GROUND / OPEN	•	_
-	IFF/CONT	וכזר	IFF/RT	RA	0150	GROUND / OPEN	•	-
-	FF/CONT	1631	IFF/RI	RA	0150	GPOUND/OPEN	•	-
-	IFF/CONT	רכצר	IFF/RT	RA	0150	GROUND/OPEN	•	-
=	IFF/CONT	1537	IFF/RT	44	0150	GROUNDIOPEN	•	_
=	FF/CONT	1631	1FF/RT	**	0150	GROUND/OPEN	•	_
=	IFF/CONT	1631	IFF/RT	RA	0150	GROUND/OPEN	•	-
1.	I F F / CONT	1631	1FF/RT	N. A.	0150	GP DUND / DP EN	•	-
15	FF/CGN1	1631	1ff /RT	RA	0150	GROUND/OPEN	•	
1	IFF/CCNT	1631	16F/RT	RA	0150	GROUND/OPEN	•	_
15	FF/CONT	1531	IFF/RT	RA	0150	GROUND/OPEN	•	-
IFF	IFF /CONT	1631	IFF/CCMP	RA	0150	GP DUND / OPEN	•	_
IFF	FF/CUNT	1631	1FF/COMF	FA	0150	+ 28 VOC.OPEN	•	-
166	FF/CONT	1631	IFF/COMP	R A	0150	GROUND/OPEN	•	-
141	1FF/151R	4 6	1FF/CONT	1531	0150	+ 28 VOC. OPEN	•••	٠.
		!			7510	N3404004	•	•
	TAC/CONT	RCSL	TAC/HT	R.	0150	2	•	-
CMD/STATUS TAC/ SERIL DATA TAC/	TAC/CONT	RCS1 RCSL	TAC/HT TAC/HT	8 8 8 4	018C S 01G	+ 28 VOC.OPEN + 28 VOC.OV	32	32

TABLE 13a(cont)

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ŏ.	5442111115	NA 1 24	777777777777777777777777777777777777777	NA 24 1
UPDATE	v	8008	N	800
VOLTAGE	+2, -8 GROUND/OPEN GROUND/OPEN GROUND/OPEN 42, -8 +2, -8 +2, -8	+2, -8 GROUND/OPEN +2, -8	+2, -8 GROUND/OPEN GROUND/OPEN GROUND/OPEN GROUND/OPEN GROUND/OPEN +2, -8 +2, -8 +2, -8 GROUND/OPEN	+2, -8 GROUND/OPEN +2, -8
TYPE	\$ DIG DISC DISC \$ DIG \$ DIG \$ DIG	s dig disc s dig	\$ 216 2 216 2 216 3 216 5 216 5 216 5 216 5 216 5 216	s DIG DISC S DIG
TO	UHF/RT 1 RA UHF/RT 1 RA ADF/AIP RA UHF/IND 1 INST UHF/CONT 1b LCSL	UHF/CONT 1a LCSL UHF/CONT 1a LCSL UHF/CONT 1a LCSL	UHF/RT 2 RA UTE/RT ADF/ATP UHF/IND 1 INST UHF/IND 2 INST UHF/GONT 2b LCSL ANT/SW RA	UHF/CONT 2a LCSL UHF/CONT 2a LCSL UHF/CONT 2a LCSL
PROM UNIT LOC	UHF/CONT 1a LCSL	UHF/RT 1 RA SCG/PROC LA UHF/CONT 1b LCSL	UHF/CONT 2ª LCSL	UAF/RT2 RA SCG/PROC LA UHB/CONT 2b LCSL
NAME	PROM UHF/CONT 1a DATA HI/LO PWR ON/OFF GRD RCVR ON/OFF TONE XMIT CONT SQUELCH ADF ENABLE 1 DATA HI/LO DATA HI/LO DATA HI/LO	NPUTS TO UHF/CONT 1a 81002 CLOCK HI/LO 81008 TAKE CONTROL 81001 DATA HI/LO	B1011 DATA HI/LO B1013 PWR ON/OFF B1014 GRD RCVR ON/OFF B1015 GRD RCVR ON/OFF B1015 ADF ENABLE 2 B1011 DATA HI/LO	TO UHF/CONT 2a CLOCK HI/LO TAKE CONTROL DATA HI/LO
SIGNAL	0UTPUTS FROM 81001 DA 81003 PW 81004 GR 81005 TC 81005 SG 81001 DA 81001 DA 81001 DA	81002 81008 81001	81011 81013 81014 81014 81015 81017 81011 81011 81011	1NPUTS TO UHP/ 81012 CLC 81017 TAR 81011 DAT

ASSIGNMENT OF SIGNALS TO BE MULTIPLEXED

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TABLE 13b AFT COCKPIT AMT 2

SIGNAL	R NAME	H UNIT	FROM LOC	DT TINU	301	1496	VOLTAGE	UPDATE	
INPUTS TO RAZINO	RAZIND								
21001	INDICATOR ALT SELF TEST	RAIRT	22	RA/IND RA/IND	INST	DC ANA DISC	+ 25 VOC, DV GROUND/OPEN	~ ~	*-
INPUTS TO HMS/HSI	HMS/HSI								
45011	PNG FLAG CONT	TAC/NT	48	HMS/HSI	INST	D1 SC	=	•	-
45012	-	TACIMT	R.A	HPS/hSI	INST	SYNCHE		2	-
45013		TAC/HT	RA	HMS/HSI	INST	SYNCHR		2	_
45014		TACINT	RA	HMS/HSI	INST	SYNCHR		•	-
45015	-	TACIMT	44	HMS/HSI	INST	SYNCHR	11.8 VAC, DV		13
45016	CCURSE DEVIAT	TAC/HT	RA	HPS/HSI	INST	DC ANA	+/-200 MVDC		12
45017	BPG FLAG	TAC/MT	RA	HMS/HSI	INST	0150	+380 MVDC, DV	~	-
45018	TOFFROR	TAC/HT	R.A	ISH/SHH	INST	DC ANA	+/-300 HVDC	2	12
45019	CRS RSLVEP ROT	TACIMT	RA	HKS/HSI	INST	SYNCHR	26 VAC, 0V	'n	13
INPUTS TO HMS/ADI	HMS/ADI								
35011	EER	00C/CR	RME	HMS/ADI	INST	DC ANA	+1- 2.2VDC	52	6 0 0
35034	LATERAL ERROR	00C/CR	RME	HMS/ADI	INST	DC ANA	+/- 2.2VDC	62	0
OUTPUTS FROM DOC/S-N	M 00C/S-N								
35004	VAYPOINTS	00C/S-1	ונצו	DDC /RECPT	***	0150	+ 28 VDC, OPEN	S	_
OUTPUTS FROM DOCICEN	M DDC/CCNT								
15017	ANTI-IAM	DOCICONT	1631	00C/CR	PHE	2510	+ 5 VDC, 0V	•	-
15018	EXT. SELECT	DOCICONT	1651	00C/CR	RME	0150		•	
35019	SEL	DOCICENT	1631	DDC/CR	RME	0150	VDC,		_
35020		DDC/CONT	וכצר	00C/CR	RME	0150	+ 5 VOC, 0V	•	-
35021	•	DOCICONT	1631	00C/CR	RME	0180	V00	•	
35022	SEL	DDC/CONT	וכצר	00C/CR	PRE	0180	4 5 VOC. DV	•	
35023	SEL	DOC/CONT	וכצו	000 /CR		DISC			٠.
35024	SEL	DOC/CONT	רכצו	DDC /CR	T :	0150			٠.
35025	SEL	DDC/CDN1	1531	DDC /CR	X 2	0150	100 00 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	n 4	٠.
35056	SEL	100/200	1531	000 VCK	E 2	2010			
35027		100/200	153	2000	U 4	0130	* * * * * * * * * * * * * * * * * * *		
35028	35.	DOC YOUR	1631	2000	310	0150	1 28 VOC. UV	٠ ،	٠.
01067	1631 1/0	ODENEGRA			•	;			

TABLE 13b (Cont'd)

2		555111115		7 T 7 T 7 T 7 T 7 T 7 T 7 T 7 T 7 T 7 T		55777775	1 24	% T %
UTATE		N.———N N		908		v v	N W	800
70LTAGE	:	+2, -8 GROUND/OPEN GROUND/OPEN GROUND/OPEN GROUND/OPEN +2, -8 +2, -8		+2, -8 GROUND/OPEN +2, -8		+2, -8 GROUND/OPEN GROUND/OPEN GROUND/OPEN GROUND/OPEN GROUND/OPEN +2, -8 +2, -8	+2, -8 GROUND/OPEN	+2, -8 GROUND/OPEN +2, -8
TYPE	ı	s DIG DISC DISC S DIG S DIG S DIG S DIG S DIG S DIG		S DIG DISC S DIG		5 DIG DISC DISC S DIG S DIG	s dig	S DIG S DIG S DIG
TOC		RA RA INST		TCST TCST TCST		RA INST	I,CSL RA	1021 1031 1031
2		đ		222		8	2a	222
		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		TNO		THE PART OF THE PA	TNO	TNO
UNIT		UHF/RT 1 UHF/RT 1 ADF/APP UHF/IND 1 UHF/IND 2 UHF/CONT 1a		UHF/CONT 1b UHF/CONT 1b UHF/CONT 1b		UHF/RT 2 UHF/RT 2 ADF/AMP UHF/IND 1 UHF/IND 2	UHF/CONT 2a	UHF/CONT 2b UHF/CONT 2b UHF/CONT 2b
100		TCSI TCSI		233		75	TCST	Z T
FROM		a a		a		8	28	28
UNIT		TNOC		TROC CONT		UHF/CONT 2b	UHF/CONT 2b	UHF/RT 2 SCG/PROC UHF/CONT
12		UHF/CONT 1b		UHF/RT 1 SCG/PROC UHF/CONT 1a		UHF/	UHIP/	UHF/ SCG/ UHF/
×		,						
				:				
	:	ρ				E.		
	a	HI/LO ON/OFF ECVR ON/OFF X:II CONT LCH ENABLE 1 HI/LO HI/LO		00_	T 2b	DATA HI/LO FER ON/OFF GRD RCUR ON/OFF TONE XMIT CONT SQUELCH ADF ENABLE 2 DATA HI/LO DATA HI/LO	N 40	980
NAME	CONT	DATA HI/LO TWR ON/OFF GED ECVR ON TONE X:II C SQUELCH ADF ENABLE DATA HI/LO DATA HI/LO DATA HI/LO	a	CLOCK HI/LO TAKE CONTROL DATA HI/LO	/con	DATA HI/LO GRD RCVR OI TONE XMIT SQUELCH ADF ENABLE DATA HI/LO	ADF ENABLE	CLOCK HI/LO TAKE CONTROL DATA HI/LO
	OHE/	DATA HI/ CED ECVE CED ECVE TONE XII SQUELCH ADF ENAI DATA HI/ DATA HI/ DATA HI/	/con	TA KE	UHF/	ATA INTA INTA INTA INTA INTA INTA INTA I	OF E	NAKE NAKE
	OUTPUTS FROM UHP/CONT 15	DATA TUNE GEED TONE SQUEI ADF DATA DATA DATA	INPUTS TO UHP/CONT 1b	TAKE	OUTPUTS FROM UHF/CONT 2b	9225.2599	81011 DAT	5 5 5 5
-1 #	13.		8		UTS	16489711		187
SIGNAL	UTIE	81001 81003 81004 81005 81006 81007 81001 81001	NPUI	81002 81007 81001	OUTP	81011 81013 81014 81015 81017 81017 81011	81011	81012 81018 81011
2 2	. •.	∞ ∞ ∞ ∞ ∞ ∞ ∞ ∞ ∞	-	00 00 00				

TABLE 13b (cont)

Towns &

Consult A

SIGNAL	RAPE		TIND	FROM LOC	TINU	991	1496	VOL TAGE	P 6 E	UPDATE		
OUTPUTS	DUTPUTS FROM TAC/CONT											
45001 45002 45004	TOTAL CHOSTATUS		TAC/CONT TAC/CONT TAC/CONT	RCSL RCSL PCSL	TAC/HT TAC/HT	444	015C 015C 5 016	680UF + 28 + 28	GROUND/OPEN + 28 VOC,OPEN + 28 VOC,OV		32 32	
SIGNAL	344	5	FROM	201	TIND	201	1796	VOLTAGE	w	UPDATE	•	
047PUTS FROM FLR/SG 72023 ALT DATA	TS FROM FLR/SG 72023 ALT DATA XFER	3	FLR/SC		FA/RT	, s	0150	GPOUND	GP D UND / DP EN	•	-	
IMPUTS TO FLR/SG	18/36											
21005	PELIABILITY LINEAR ALT LINEAR ALT	# # # # # # # # # # # # # # # # # # #	#4/#T	222	FLR/56 FLR/56 FLR/56	335	DISC DC ANA DC ANA	23.2	VDC.0V VDC.0V	222		
DUTPUTS FROM DOC/CC	M DDC /CC						•					
35013 35014 35015	DDC DATA READY DDC DATA DDC ADDRESS	888	33/300 33/300 33/300	144	NAMO	333	\$ 010 \$ 010 \$ 010	***	V00,00V V00,00V	000	-22	
INPUTS TO ODC/CC	95/30											
11032 11064 35000 35010	ADC/ODC TEST DATA CLOCK DATA LINK DATA DATA LINK RDY	2200	NWDC NWDC DDC/CR DDC/CR	2288	33/300 33/300 33/300	4444 6444 6446	S O O O O O O O O O O O O O O O O O O O	222	00000 00000 00000 00000		3-	

ASSIGNMENT OF SIGNALS TO BE MULTIPLEXED

TABLE 13c RIGHT AVIONICS AMT 3

UPDATE PATE O		2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	11 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	22	v
VOLTAGE		+ 5 VDC, DV GROUND/OPEN 11.8 VAC, DV 11.8 VAC, DV 11.8 VAC, DV +-200 HVDC +-300 HVDC +-300 HVDC	+ 5 VOC, OV + 5 VOC, OV 11.8 VAC, OV GROUND/OPEN + 28 VOC, OPEN + 28 VOC, OPEN	GROUND/OP EN GROUND/OP EN	GROUND/OPEN
1486		S S S S S S S S S S S S S S S S S S S	S 016 S 016 S 016 SYNCHR D1SC 015C	DISC	DISC
201		NEW STATES	444444 44444	₩	\$
UNIT TO		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 ACC/M1 1 ACC/M1 1 ACC/M1 1 ACC/M1 1 ACC/M1	ANT/SW ANT/SW	ADF/AMP
FROM LOC		< < < < < < < < < < < < < < < < < < <	L LA L LA R R R S S L R R R S S L	TCST	TCST TCST TCST
T TINO		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	NUDC NUDC NUDC IHS/APS TAC/CONT TAC/CONT	UHF/CONT 2a UHF/CONT 2b	UHF/CONT 1a UHF/CONT 1b UHF/CONT 2a
. 944	TAC/HT	TAC SEPIAL DTA BISTANCE UNITS DISTANCE TENS DISTANCE HUNDS TACAN BEARING COURSE DEVIAT TO/FROP CRS RSIVER ROT	ADPESS LINE B READ ADDR LINE SHIFT CLGCK HAG HEADING TUPN ON CMD TST CMD/STATUS PUX SEPIL DATA	INPUTS TO AMT/SW \$1017 ADF ENABLE 2 \$1017 ADF ENABLE 2 INPUTS TO ADF/AMP	ADF ENABLE 1 ADF ENABLE 1 ADF ENABLE 2
STGRAL	OUTPUTS FROM TACINT	45007 45011 45011 45013 45015 45015 45016 45018	1010 ADRE 11011 READ 11012 SHIF 12063 HAG 45001 TUPN 45002 TST 45004 PUX	INPUTS TO AMI/SI 81017 ADF 1 81017 ADF 1 INPUTS TO ADF/A	81007 81007 81017

		TABI	TABLE 13c (cont)	ont)				
SIGNAL	2 2 2 2	FROM P	. 001	OT TINO	100	TYPE	VOL TAGE	UPDATE RATE 9
OUTPUTS FROM 1FF/R	JH IFF/RT							
46020	PEPLY LIGHT EN	1FF/RT	. 4	IFF/CONT	ונצו	2510	+ 28 VOC, OPEN	,
INPUTS TO I	166/81							
46001	SENSITIVIT CNT	IFF/CONT	1631	184/81	PA	0150	GROUNDIDPEN	5 1
46062	6	IFF/CONT	וכצר	IFF/RT	4	0150	GROUND/OPEN	2
46003	MODE 2 SNABLE	IFF/CONT	ונצו ניצו	1FF /RT	4 4 0	0150	GPOUND/OPEN	•
46005	, –	I F F / CONT	וכפר	1FF/RT	4 4	0150	GROUND/OPEN	
46006	0	IFF/CONT	1631	JFF/RT	RA	0150	GP DUND / DPEN	
46007	EMERCENCY CNT	IFF/CONT	וכצר	1FF/RT	A S	2510	GROUND/CPEN	5
46008	THE RELAY CNT	TEE/CONT	ונצו	156 /81	A A	0120	COULIND COREN	
46021		1 FF/CCN1	1031	IFF/RT	. A	0130	GROUND/OPEN	
46023	DOF	IFF/CONT	1631	IFF/RT	N N	0150	GPGUND/OPEN	
46030	4	IFF/CONT	וכצר	IFF /RT	P.	0150	GR DUND / CPEN	
16031	MODE 1 AZ ENAB	IFF/CONT	וכאר	1FF /RT	X 0	0180	CRUCADION	
46033		1FF/CON1	1631	IFF/RI	4 A	0150	GROUND/OFEN	
46034	1 62	IFF/CONT	1031	IFF/RT	P. A	0150	GP GUND / OPEN	
46035	3/4	IFF/CONT	וכצו	IFF/RT	RA	0180	GROUND/OPEN	
46036		IFF /CONT	1021	IFF/RT	W W	0150	CPOUND/CPEN	
46038	3/8	IFF/CON1	1631	166/81	4 4	0150	GROUND/OPEN	
46039	3/4	I+F/CCNI	1631	IFF /RT	RA	0150	GROUND/OPEN	
04094	3/4	IFF /CONT	רכצו	IFF/RT	RA	0150	GROUND/OPEN	
46041	#00F 3/A C1 EN	I F CON I	1521	144/81	4 4	0150	SADUAD/ORDEN	
25095	3/4 64	I F / CONT	1631	IFF/RT	4 4	0130	GR CUND/OPEN	
44044	3/4 01	IFF/CONT	1651	F / R	RA	0150	GROUND / OPEN	
44045	F006 3/4 02 FN	IFF CCNT	SSI	164 /81	A d	0180	GROUND/OPEN	
OUTPUTS FROM IFF	/COMP		1631		4 %	2617	U	
73026	IFF ADV SIGNAL	IFF/COMP	R A	SC G / PROC	3	0150	+ 28 VOC.OPEN	•
INPUTS TO	1FF/COMP							
46009	NO0 4	IFF/CONT	וכצו	IFF/COMP	A .	0180	GROUND/OPEN	
75034	MODE 4 COO	IFF/CONT	בנים בנים	IFF/COMP	8 8 8 8	0150	GROUND/OPEN	w. 4
46048	PCDE 4	IFF/CONT	1631	IFF/COMP	8	0150	+ 28 VOC. OPEN	
46049 MODE DUTPUTS FROM 1FF	4 ZERI	IFF/CONT	1631	IFF /COMP	8	0150	GR CUND / OP EN	
* 46015	TST LAMP ENABL	11F/15TR	RA	IFF /CONT	1631	0150	+ 28 VDC.OPEN	•
							:	

TABLE 13c (cont)

		* * * *			77.77	1771		***		
UPDATE		0 0 0 0 0 0 0 0		S	. ~ ~ ~ ~ ~ ~	างงง		80000		~~~~~~~~~~
VOLTAGE	•	+ 5, -8 +2, -8 +2, -8 +2, -8	,	0,28	0,12 0,28 0,28 0,19	+2, -8 GROUND/OPEN	,	+2, -8 +2, -8 +2, -8 +2, -8		0,28 0,28 0,12 0,12 +2,-8 0,28 0,28 0,12 0,12 +2,-8 GROUND/OPEN
TYPE		s DIG		DISC	DISC S DIG DISC	DISC S DIG DISC		s DIG s		DISC S DIG DISC DISC S DIG S DIG S DIG
700		LCSL LCSL INST		a		22		LCSL LCSL INST INST		222
OT TINU		UHF/CONT 1a UHF/CONT 1b UHF/IND 1 UHF/IND 2		UHF/RT 1		UHF/RT 1 UHF/RT 1		UHF/CONT 2a UHF/CONT 2b UHF/IND 1 UHF/IND 2		UHF/RI 2 UHF/RI 2
100		g g	:	TCST		Tcsr T		≨≨		1 CS1 CS2 A
FROM		UHF/RT 1 UHF/RT 1 UHF/RT 1		UHF/CONT 18	UHF/CONT 1a	UHF/CONT 15 UHF/SA		UHF/RT 2 UHF/RT 2 UHF/RT 2		UHF/CONT 2a UHF/CONT 2a UHF/CONT 2b UHF/CONT 2b UHF/CONT 2b
×									•	
NAME	FROM UHF/RT 1	CLOCK HI/LO CLOCK HI/LO CLOCK HI/LO CLOCK HI/LO	O UHF/RT 1	PWR ON/OFF GRD RCVR ON/OFF TONE XMIT CONT	SQUELCH DATA HI/LO PWR ON/OFF GRD RCVR ON/OFF TONE XIIT CONT	SQUELCH DATA HI/LO KEY XMIT 1	ROM UHF/RT 2	CLOCK HI/LO CLOCK HI/LO CLOCK HI/LO CLOCK HI/LO	O UHF/RT 2	PWR ON/OFF GRD RCVR ON/OFF TONE XMIT CONT SQUELCH DATA HI/LO PWR ON/OFF GRD RCVR ON/OFF TONE XMIT CONT SQUELCH DATA HI/LO KEY XMIT 2
SIGNAL	OUTPUTS FROM UNF	81002 81002 81002 81002	INPUTS TO UHF/RI	81003 81004 81005	81006 81001 81003 81004 81005	81006 81001 81009	OUTPUTS FROM UHF	81012 81012 81012 81012	INPUTS TO UHF/RI	81013 81014 81015 81016 81011 81013 81014 81016 81016 81011

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cont
13c (c
TABLE

I

•	N-880	2	. 8			******	
POATE	775551	7 5 2 2	a		****	222222	n n
VOL TAGE	+ 12 VDC, DV + 12 VDC, DV +/- 2.2VDC -/- 2.2VDC 26 VAC, DV	26 VEC. DV GROUND/OPEN GROUND/OPEN +/- 2.2VDC +/- 2.2VDC	+ 5 VDC, DV + 2 VDC, DV + 5 VDC, DV + 5 VDC, DV	20000000000000000000000000000000000000	GROUND/OPEN GROUND/OPEN GROUND/OPEN GROUND/OPEN GROUND/OPEN	GROUND/OPEN + 5 VDC, DV + 25 VDC, DV + 25 VDC, DV + 25 VDC, DV + 25 VDC, DV	GROUND/OPEN GROUND/OPEN
149E	S DIG S DIG DC ANA	O O O O O O O O O O O O O O O O O O O	8 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	2000000 200000000000000000000000000000	015C 015C 015C 015C	DOC ANA ANA DC ANA ANA DC ANA ANA DC ANA DC ANA DC ANA DC ANA DC ANA DC ANA ANA DC ANA ANA ANA ANA ANA ANA ANA ANA ANA AN	01SC 01SC
100	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	***************************************	*******		4444	INST LAE LAE LAE LAE	2 5
OT TINU	DDC/CC DDC/CC HMS/ADI HUD/SDF	AFCS/PCA AFCS/PCA AFCS/PCA HUD/SDP HMS/ADI	000C/CR 000C/CR 00C/CR	20000000000000000000000000000000000000	166/1518 166/1518 166/1518 116/1518	RAVIND RAVIND FLR/SG FLR/SG NWOC HUD/SDP FLR/SG	RA/RI SCC/PROC
91		******	1001 1001 1001 1001	25 25 25 25 25 25 25 25			LINE RC
R UNIT FROM	000C/CR 00C/CR 00C/CR	00000000000000000000000000000000000000	000C/RECPT 000C/CONT 000C/CONT 000C/CONT 000C/CONT	1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 1007/200 100	1FF/CONT 1FF/CONT 1FF/CONT 1FF/CONT 1FF/CONT	# # # # # # # # # # # # # # # # # # #	FLR/SG RA/IB
NANE	DATA LIN DATA LIN EL STEER EL STEER	0000 0 0000 0 0000 0 1 LATERA 1 LATERA	SINS/UPTS DA ANTI-LAM EXT. SELECT FPEO SEL O. FREO SEL O.	FREG FREG FREG FREG FREG	HODE 1 TEST FODE 2 TEST FODE 2 TEST FODE C TEST FONITOR CNIRL OM PA/RT	INDICATOR ALT SELF TEST RELIARILITY LINEAR ALT LINEAR ALT LINEAR ALT	ALT DATA XFER OM RA/16 TPANS BLANXER
SIGNAL		35030 35031 35032 35032 35033 35034	35007 35018 35018 35019 35020	5024 5025 5026 5026 5026 5026 5026	46016 46017 46017 46019 46022 0UTPUTS FRE	21001 21003 21005 21006 21007 21009	72023 ALT DA OUTPUTS FROM RA/18

ASSIGNMENT OF SIGNALS TO BE MULTIPLEXED

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Comments

			TABLE	13dleFT	TABLE 13dleft AVIONICS AMT 4	7 1				TANGIL	
SIGNAL	NA ME	=	TIND	FAUN LOC	TINU TO	707	TYPE	VOLTAGE	166	RATE	•
DUTPUTS FROM NVDC	N N N N N N N N N N N N N N N N N N N				*						•
	ADDESC LINE R		NEDC	14	TAC/HT	W W	S 016	+	VDC , DV	•	٠.
01011	•		200	1.4	TAC./MT	A &	S D16	•	VDC, DV	•	-
11011			200	::	TACAMT	8	5 016	+	VDC, DV	H	-
11011	SHIFT CLUCK		NADC	5			2310	1 28	VOC.00V	•	-
11032	ADC/00C TEST		NADC	LA	22/200	DHA	2510	07	200	200	
11064	DATA CLOCK		NEC	17	33/300	SH.	2 016		ADCACA	YOU THE	•
INPUTS TO NUDC	DC										
					2078	•	DC ANA	+ 25	VDC, DV	25	12
	LINEAR ALT		KAZK	,	200		2000	•	VDC . DV	100	-
35013	DOC DATA READY		22/200	AMO	JOAN	5:	200		70.707	100	20
35014	DOC DATA		22/200	AMO	JOAN	5:	200		70.707	100	20
	DOC ADDRESS		22/200	AND	NADC	3	2010		2000		20
	TAC SEPTAL DTA		TACINT	4	NAOC	5	2 016	•	*0000		2
OUTPUTS FROM INSTANT	IHS/APS									•	
12063 MAG HE	MAG HEADING		INS/APS	3	TACINT	R.A	SYNCHR	11.8	VAC, DV	•	13
INPUTS TO HUD/SOP	/ SDP										:
21008	I THE AD ALT		RA/RT	B.C.	HUD / SDP	14	DC ANA	+ 25	VOC. 0V	62	75
	EI STEFRING	i	900/08	RAE	HUD/SOP	۲,	DC ANA	1- 2	20V5.	52	20 (
	LATEGAL EPROR		. 40/000	RHE	HUD/SDP	5	DC ANA	+1- 2.2VDC	.zvoc	2	n
INPUTS. TO AFCS/RCA	/RCA										
35029 R 35032 G	ROLL DISPLACE GOOD DATA		DDC/CR DDC/CR	8 8 8 8 8 8	AFCS/RCA AFCS/RCA	11	DC ANA DISC	SROUND/OPEN	VAC. OV	7.	g - '
OUTPUTS FROM DOC/RECPT	DC/RECPT										
35007 SINS/WPTS	NS/WPTS DATA	8	DDC/RECPT	7.5	00C /CR	RHE	s 016 +	41- 5	VOC	63 80	
INPUTS TO DOC/PECPT	PECPT										
35004 WA	WAYPOINTS	8	M-S/200	רכזו	DDC/RECPT	1,4	• 2510	+ 28	VDC . OPEN	n	

TABLE 13d (cont)

Control of

			MOGA		\$		TYPE		UPDATE	
SIGNAL	NAME	×	UNIT	200	UNIT	207	ZIGNAL	VOLTAGE	RATE	o.
1			1					•		
INPUTS I	INPUTS TO UHF/IND 1								1	
81001	DATA HI/LO		THE/CONT 18	TCST	UHF/IND 1	INST	S DIG	+2, -8	· ·	24
8.001	DATA HI/LO		CHF/CONT 16	_			_	87.74	٠ ٠	37
8.011	DATA HI/LO		UHF/CONT 28		_				۰ ۳	54
81002	CLOCK HI/LO							+2, -8	800	NA
8_012	CLOCK HI/LO		UHF/RT 2	rcsr	UHF/IND 1	INST	S DIG	+2, -8	800	KA
INPUTS TO	O UHF/IND 2									
81001	DATA HI/LO		UHF/CONT 1a	TCST	UHF/IND 2	INST	s pic	+2, 08	٥-	77
81001	DATA HI/LO		UHF/CONT 1b			<u></u>		+5, 08		
81011	DATA HI/LO							+2, -8		
81011	DATA HI/LO		UHF/CONT 2b					+2, -8.	^ :	54
81002	CLOCK HI/LO		UHF/RT 1	-	-	_	_;	8- '2'	000	Z :
81012	CLOCK HI/LO		UHF/RT 2	TCST	OHE/ IND 2	INST	570 8	8- '7+	200	ž
OUTPUTS F	FROM SCG/PROC									
81008	TAKE CONTROL		2084/528	I.A	IMP/CONT 1a	TCST	DISC	GROUND/OPEN	9	-
81008	TAKE CONTROL			i	CHF/CONT 1b	-	-	-	_	_
81018	TAKE CONTROL						-	_		_
81018	TAKE CONTROL		-	_	UHF/CONT 2b	TCST	-	GROUND/OPEN	'n	-
73026	IFF ADV SIG		SCG/PROC	1	IFF/COMP	2	DISC	+28 VDC/OPEN	·	~

TABLE 14

AMUX TERMINAL-SIGNAL ASSIGNMENT

Terminal No.	Inputs	Outputs	Total
1	21	74	95
2	26	40	66
3	88	39	127
4	23	12	35
		_	
Total	158	165	323

Although the TA-7C provides for both forward and aft cockpit controls for the IFF transponder, only the forward controls will be handled over the AMUX system. This is basically in keeping with the A-7E aircraft implementation. It is also noted that switching logic is required for a group of 15 avionic discrete signals. Of these, 13 signals are used as control variables in Boolean equations and 2 signals are output controls, i.e., the results of equation solutions. All fifteen signals are transferred between the SCG and AMUX via the data bus interface. It is envisioned that the AMUX bus will be operated in the poll-contention mode, therefore, transfer of the signals will occur upon a "change of state" of the signal(s). However, the AMUX data bus operation and protocol is flexible as a result of the AMT being programmable. Consequently, a range of communication-data transfer schemes can be evaluated.

2.6 Avionic System Priority Assignment

In view of the limited quantity of AAES ADM equipment being procurred, the problem of requisitioning some of the GFE used on the TA-7C, and the difficulties and complexity of performing certain system tests and evaluations, a list was prepared for the purpose of establishing priority for the systems and equipment. The list was prepared on the basis of performing test and evaluation on a primary subsystem. Therefore, the equipments comprising that subsystem, other supporting subsystems required or desired, and test equipment needed were assembled into a list, Table 15. The table lists the pertinent part numbers for the various equipment. The table also identifies priorities for implementing and testing/evaluating the various TA-7C avionic subsystems on the AAES simulator based on such factors as complexity, equipment availability, special support equipment requirements, difficulty of testing as a result of requiring special set-up such as hydraulics, radiation, the equipment being classified, etc. The priorities range from 1 to 5 with 1 being the most desirable for implementing on the simulator.

EQUIPMENT REQUIREMENTS FOR SYSTEMS TESTS

NOTES				Radiation Required.	Classified equipment.
TEST DIFF	-		1	e .	м
TEST EQUIPMENT REQU	AN/ASN-395A Memory Loader Verifier AN/ASN-478 System Interface T/S		AN/ASN-478 System Enterface T/S	AN/ASN-478 System Interface T/S AN/APH-342A Nav T/S	TS2853C/APM-394 Radar T/S AN/ASN-478 System Interface T/S
OTHER SYS. DESIRED	IIS Almost HUD Tenucos Radar Altimeter Air Data Computer	Angle of Attack	HUD Heading Mode Sys.	None	1135 ADC Radar Altimeter
OTHER SYS. REQD.	None		Tactical Computer	Tactical Computer Inertial Measurement	Tactical Computer
FSN	2RH6605004093124GA 2RH6605004933733GA	2RH5895010258539UA	2RE660500022789 3TA 2RE4920901823006GA 2RI6605001042771 2RI6605008335087FZ	2RH5841000978741TA 2RH5841001049299GA 2RH5841001032707TA	ZRES841000017075GA ZRES841000017066G7 ZRES84100001709GB ZRES841000017109GA ZRES8410010267278 ZRES841001105379 ZRES841001105379 ZRES841001105370 ZRES841001105370 ZRES841001105370 ZRES841001105370 ZRES841001105370 ZRES841001105370 ZRES841001105370 ZRES841001105370 ZRES841001105370 ZRES841001105370 ZRES841001105370 ZRES841001105370 ZRES8414000139349 SRSS50001052148
LTV PART NO.	216-37183-14 216-21231-14	229-21203-101	216-37340-7 216-37631-9 216-21355-3 is225396-1	216-37629-1 216-21380-1 216-37325-1	11091/APQ126 AS2272/APQ126 PP6130/APQ126 CP954/APQ126 CP954/APQ126 220-27121-101 216-27877-1 216-21877-1 216-21143-7 220-21242-101 220-21143-7 220-21143-101 220-21143-101 220-21143-101 220-21143-101 220-21146-101 220-21146-101 220-21393-4 CVC6070-6
SYSTEM & EQUIPMENT	S Y R	Monitor Display Panel	INERTIAL MEASUREMENT SET (ANJASH-90) Inertial Heasurement Unit Adapter Power Supply Control Panel - Pwd. Mil Remote Compass Transmitter	Receiver-Transmitter Control Panel - Pwd. Antenna	POSMARD LOOKING RADAR (AN/APQ-126) Porward Assembly Transformer Power Supply Computer Mount Digital Scan Converter Fault Locator Range Control Panel Radar Control Panel Indicator-Fed. Indicator-F

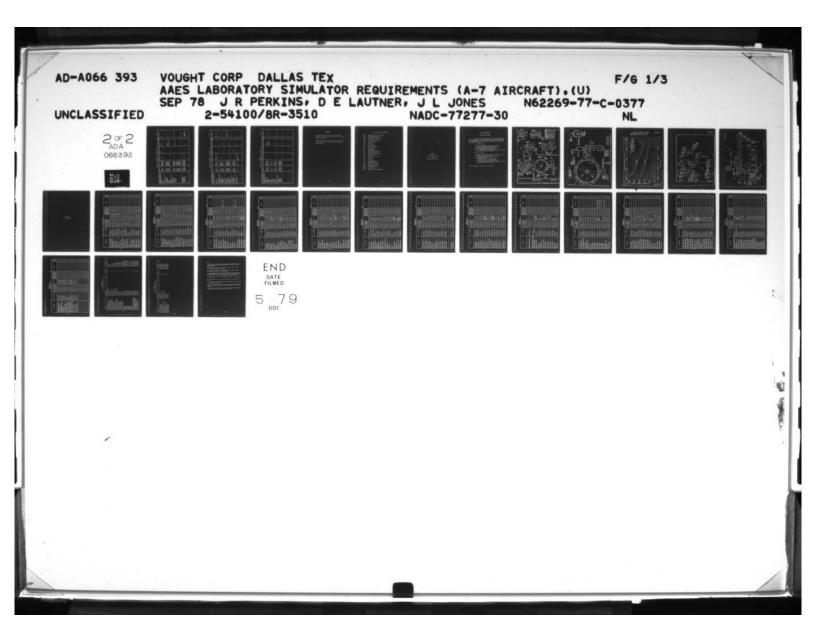
PEV. 9/8/78

EQUIPMENT REQUIREMENTS FOR SYSTEMS TESTS

П					
NOTES				Radiation Required	
TEST DIFF.	-	7	-	2	1
TEST EQUIPMENT REQU ^{TEST}	None	SN565A/ASM AIDS Input T/S AN/ASM-371A ADC System T/S	None	AN/APH-347 Altimeter T/S	None
OTHER SYS. DESIRED	ADC Angle of Attack	uUD IFF Tactical Computer	No Tactical Computer A Heads-Up Display		TACTICAL CO.PUTER
OTHER SYS. REQD.	Tactical Computer Inertial Measurement	Jone	Tactical Computer	None	ione
FSN	2RH6605001507026TA 2RE605001506499TA 2RH581101025817UA 2RH581101025853UA 2RH6615001812469GA 9G6210008746232 2RH6605004162934TA	On rt slant pnl) 2846605010298749 906685006781082 2846610000863840 2846610000853840 2746610000853840	2846605001507043CA 284660500187544CA 9N5950003508282	ZRH5841001653030WZ ZRH584100168781ZWZ (Same as above) IRM5841000198501 IRM5841000198501 IRM5841001108101	1RD6510010253196uA 2RH1680000457081cA 2RH1680000457081cA 2RQ651000620788FZ 2RQ651000620788FZ 2RQ6520009441332 9G6220009441345 9G522000941345 9G522000956311 9R6220001812542
LTV PART NO.	216-21245-32 216-37267-21 220-21201-101 220-21201-102 216-37194-1 CVC2600-7 216-21245-26	215-21127-1 220-37125-101 215-37125-1 AMU-19/A AMU-19/A 213-21124-3	ID-1665/ASN-99 218-37668-4 218-27505-1	RT-1042/APH-194 ID-1760A/APH-194 ID-1760A/APH-194 AS-1233/APN141 AS-1233/APN141 MST-1233/APN141	220-27166-101 C15302 (83326) C15302 (83326) C15302 (83326) WS28067-2 WS2818-2 WS25318-3 WS25318-4 WS25311-7
SYSTEM & EQUIPMENT	HEAD-UP DISPLAY (AN/ANQ-7) Display Unit Signal Data Processor Camera HUD Monitor Lateral Accelerometer In Range Indicator HUD Mount	AIR DAIA COMPUTER True Air Speed Ind. Air Data Computer Total Temperature Probe Airtitude Ind-Pad. Airtitude Indicator-Aft Mach Inc.	PROJECTED MAP DISPLAY SET (AN/ASN-99) Project Map Display Signal Data Converter PMDS Transformer	RADAR ALTHETER (AN/APN-194) Receiver-Transmitter Indicator-Pwd. Indicator-Aft Antenna-Transmit Interference Blanker	ANGLE OF ATTACK Transducer Rudder Pedal Shaker-Aft Rudder Pedal Shaker-Pud. Indicator-Pud. Indicator-Aft Approach Lights Indexer-Pud. Indexer-Aft.

TABLE 15 EQUIPMENT REQUIREMENTS FOR SYSTEMS TESTS

SYSTEM & EQUIPMENT	LTV PART NO.	FSN	OTHER SYS. REQD.	OTHER SYS. DESIRED	TEST EQUIPMENT REQUIPER.	TEST DIFF.	NOTES
HEADING MODE SYSTEM Attitude Direction Indicator-Pad. Attitude Direction Indicator-Afr. Horizontal Situation Indicator-Pad. Horizontal Situation Indicator-Afr. Turn Rate Gyro 1 Turn Rate Gyro 2 Electronic Switch Demodulator DC Amplifier	HS18028-1 HS18028-1 HS17869-1 HS17869-1 T751AJB3A T751AJB3A 215-27143-1 220-27105-101	2RH6610009442632FZ 2RL6610009442632FZ 2RL5610009447012GA 2RE5826009447012GA 2RH1280002210649GA 2RH1280002210649GA 2RH1580002210649GA 2RH1580002210649GA 2RH16610010241459UA	Tactical Computer Inertial Measurement	Head-Up Display TACAN Auto Direction Finder	17A383 Line Analyzer (ADI)	2	1
STANDBY ATTITUDE INDICATING SYSTEM Rate Switching Gyro Vertical Displacement Gyro Attitude Indicator-Pwd. Attitude Indicator-Aft.	MS17399-1 CN1169A(3003) MS17249-1 MS17249-1	2R16615009509736F2 2R16615009587969F2 1A6610003131407 1A6610003191407	None	ione	None	1	1
Control-Pad. Control-Aft. Pitch Control Amplifier Yaw Actuator Yaw Actuator Yaw Actuator Yaw Actuator Yaw Actuator Yaw Control Yaw Colelerometer Dual Command Coupler Rate Oyro No. 1 Rate Oyro No. 1 Rate Oyro No. 2 Roll Solenoid Valve Yaw Solenoid Valve Yaw Solenoid Valve Yaw Solenoid Valve Akt Cath Changer All-RUD Transducer Normal Accelerometer 1 Normal Accelerometer 2	215-21130-1 215-21130-2 215-37121-24 215-37121-21 215-37121-18 210-32230-20 210-32230-20 210-32230-20 210-32230-20 210-32230-20 210-32230-10 210-3230-10 215-37330-10 215-37331-1 215-32331-1 215-32331-1 215-32331-1 215-32331-1 215-38104-3 215-38104-3 215-37129-2	2816615000877443 2816615004113356 2816615004113356 287666150001108926 28766615000108926 28766150001499883 2876150001499883 2876150001499883 2876150001499883 2876150001499883 26615001812469 66615010281932 6615001817122 6615000597961 1650000597961 1650000597961 1650000597961 1650000597961 1650000597961 1650000597961 1650000597961 1650000597961 1650000597961 1650000597961	Aone	Lnertial Measurement Set Air Data Computer	AN/AS1+499 AFCS T/S	n	Hydraulic system and actuators and Loads Required.
APPROÁCH POMER COMPENSATOR (AN/ASN-54) Computer Servo Amplifier UMT Potentioneter Accelerometer APC Warning Light	215-37155-3 215-47120-1 215-37126-2 215-37176-2 215-37178-2 CVC2600-9	ZRI6615007820895GA BRH6615000899084GA BRH6615001217677GA (51mulace) IRD6615008801341 9G6210001830523	Angle of Attack	None	AN/ASH-334 APC T/S	2	1



EQUIPMENT REQUIREMENTS FOR SYSTEMS TESTS

NOTES		Radiation Required.	Classified equipment.	Radiation Required. (Alternate FSN 8R15821001401817HZ for ID-972)
DIFF.	3	m	e .	3
TEST EQUIPMENT REQU	AN/ARH-146 ACS T/S	AN/APM-230B Radar Beacon T/S SN/658/APM Radar Beacon Simulator	SM-511/ASW Digital Data Simulator	None
OTHER SYS. DESIRED	Data Link	None	ione	None .
OTHER SYS. REQD.	Heading Mode	None	Tactical Computer	Intercommunication Set
FSN	8RG5826004917513EX 8RH5826004917514EX 8RH5895001688856EX 8RH5895001688856EX	ZRIS841001687890 ZRIS841001687890 ZRIS895001108174 ZRIS895001687820 IRMS841000706135 ZRIS8410001687822 ZRIS841001687822 ZRIS841001687822 ZRIS841007635060	2815895008391404 28158950016885804 2815895001683631 2815895001683631 1805826001186221 905210001830521 905210001830522 905210001830533 905210001830533 905210001830532	8RH58210102135G3J2 (5ame as above) 8RH582101018424GJZ 6RH58210014GJ785HZ (5ame as above)
LTV PART NO.	R1 379 / ARA6 3 KY 651 / ARA6 3 C79 49 / ARA6 3 C79 49 / ARA6 3	C4419/PN154 C4419/PN154 C4419/APN154 RT623/APN AS1739/APN154 AS2406/APN ID811/APN154 CU1104/APN154	CV2230A/ASW-25 218-27590-1 C7100/ASW-25 C7100/ASW-25 C7100/ASW-25 C7100/ASW-25 C7100/ASW-25 CV2600-10 CV2600-10 CV2600-11 CV2601-46 CV2601-46 CV2601-46 CV2602-35 CV2602-35 CV2602-35 CV2602-45 CV2602-35	C9815/ARC-159 C9815/ARC-159 RT-1150/ARC-159 ID-1972/ARC-159 ID-1972/ARC-159
SYSTEM & EQUIPMENT	0	RADAR BEACON (AN/APH-154) Control Panel-Pad. Control Panel-Aft. Receiver-Transmitter KA Band Receiver Antenna 2 Antenna 2 Modulator Duplexer	DIGITAL DATA COMMUNICATION SET (MI/ASH-25) Converter-Receiver Coupler Converter Control Panel-Nd. Control Panel-Aft. Antenna Data Link Lights	UHF RADIO (AN/ARC-159) Control Panel-Nd. Control Panel-Aft. Recaiver-fransatteer Freq. Indicator-Nd. Freq. Indicator-Aft.

EQUIPMENT REQUIREMENTS FOR SYSTEMS TESTS

UNIT Part UNIT	SYSTEM & EQUIPMENT	LTV PART NO.	FSN	OTHER SYS. REQD.	OTHER SYS. DESIRED	TEST EQUIPMENT REQUIPE.	TEST DIFF.	NOTES
SET (MI/AIC-25)	AUTOWATIC DIRECTION FINDER (AN/ARA-50)							
## SET (AW/AIC-25) 220-21362-101	UHF-IFF Diplexer Antenna Amplifier-Relay Tail Cap Antenna		9N5985000694614 2RH5826008490055 2RH5826000592726 1RD1560001030573		None	None	e .	ADF Station must be available,
CS054/ARI-84 IRUSS26009480468 CS054/ARI-84 IRUSS26009480468 CS054/ARI-84 IRUSS26009480468 CS054/ARI-84 RRISS260016887972 RRIO22/ARI-84 RRISS260016887972 RRIO22/ARI-84 RRISS260016887972 RRIORDO CS054/ARI-84 RRISS2600168877072 RRISS260016877072 RRISS2600168273 RRISS2600168273 RRISS2600189727 RRISS2600189727 RRISS26001822980 RRISS26004872 RRISS260014911319AZ RRISS2604/ARX-72 RRISS260014911319AZ RRISS2604/ARX-72 RRISS260014911319AZ RRISS2604/ARX-72 RRISS26004994446 Radar Altimeter RADAR Alti	INTERCOMBUNICATIONS SET (AN/AIG-25) CONTROL Panel-Pad. Control Panel-Afr. Intercom Station Tone Generator Pilot's Service Disconnect Pilot's Headset Audio Unit		1RD1680010248762 1RD1680010248762 2RI5831008802833 2RI5821005147856 (Simulate) (Simulate) 2RH5950010274134	UHF Radio	None	15387U Handphone T/S	5	Audio Source required.
C6280/AFX 1RD5895001822980 None Air Data Computer G5280/AFX 1RD5895001822980 None Air Data Computer RT829/AFX-72 2RH5895001491319AZ T51843/AFX-72 2RH5895001491319AZ T51843/AFX-72 2RH5891001066148 Forward Looking Radar None Radar Altimeter None 1FF None TFP	TACAN (AN/AUD-84) Control Panel-Pud. Control Panel-Aft. Reciver-Transmitter Mount Antenna Switching Unit Blower Antenna Upper Antenna	C9054 / MRH-84 C9054 / MRH-84 RT1022 / MRH-84 HT-4354 / MRH-84 SA-521A SA-521A 218-77514-1 CV21-010001-4	IRD5826009480468 IRD5826009480468 8RH5826001688769T2 8RH5826001688707Z 9985008370000 IRM54140708786606 IRM582600186221 IRM5826000899727	Heading Mode System	Tactical Computer	AN-A2M-155 AN-A2M-156	2	(The C2010 panels are an acceptable alternate for C5054.)
- 216-37162-3 2RH5841001066148 Forward Looking Radar None Radar Altimeter TACAN IFP	IFF TRANSPONDER (AN/AEX-)2) Control Panel-Pad. Control Panel-Aft. Receiver-Transmitter Tester	C6280/APX C6280/APX RT859A/APX-72 TS1843/APX-72	1RD5 89 5/01 8229 80 1RD5 89 5/01 8229 80 2 RB15 89 5/01 49 1319 AZ 2 RB15 89 5/00 859 444 46	None	Air Data Computer		7	
	INTERFERENCE BLANKER Interference Blanker	216-37162-3	ZRH5841001066148	Forward Looking Radar Radar Altimeter IACAN IFF	None	None	7	

EQUIPMENT REQUIREMENTS FOR SYSTEMS TESTS

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NOTES	Classified equipment.	1.	
TEST DIFF.	2	1	
TEST EQUIPMENT REQU	AN/ASM-456, 457, 458 High Power RF Simulators. AN/ALM-140 ALR-50 T/S	None	
OTHER SYS. DESIRED	None.	vione	
OTHER SYS. REQD.	None	None	
FSN	2RH5865001275166 2RH5865000011717 8RH5865001486059 2RH5865009892107 2RH5865004345409 2RH5865004345409 1RD5895001360906 1RD5895001340900 (Simulate) 966210001830538	2RH5995004940781 2RH5995000874212 2RH5995000974212 2RH5865001773417 2RH5865000899754 2RH5865000899754	
LTV PART NO.	218-21195-3 218-37503-4 128-37503-4 123053/ALR-45 31-011203-01(15280) 31-027824-01(15280) 81764/ALR-50 AS2605/ALR45 AT-141A 01-23-03721(15280) 216-21347-11 CVC2601-44	218-21243-2 \$A1557/ALE-29A \$A1577/ALE-29A HX7718/ALE-29A HX7721/ALE-29A	
SYSTEM & EQUIPMENT	PASSIVE COUNTEDUEASURES (AN/ALR-45 and ALR-50) 45/50 Control Panel 5ignal Distribution Unit 45 Analyzer 45 Indicator Preamp-45 Preamp-45 Preamp-135 Preamp-135 Preamp-315 Antenna-315 Antenna-125 Ante	CHAFF DISPENSER (AN/ALE-29) Control Panel Left Sequencer Right Sequencer Programer Programer Left Dispenser Right Dispenser	

REFERENCES

- Advanced Aircraft Electrical System, A-7E Prototype Design,
 Final Report NADC-76193-30, dated August 1977, by J. R. Perkins,
 etal, Vought Corporation.
- POWERTRAN Reference Manual for Program Support Software Pakcage, Report No. 78-14905, dated 15 February 1978, by W. R. Sobko, Garrett Airesearch.

LIST OF ABBREVIATIONS AND ACRONYMS

Advanced Aircraft Electrical System AAES AAS Advanced Armament System ACLS Automatic Carrier Landing System ADM Advanced Development Model AMT Avionic Multiplex Terminal AMUX Avionic Multiplex BC Bus Controller BIT Built In Test BTC Bus Tie Controller CAD Computer Aided Design DT Data Terminal Electromechanical EM EMI Electromagnetic Interference GCU Generator Control Unit GFE Government Furnished Equipment HVDC High Voltage DC ICU Industrial Control Unit 1/0 Input/Output KW Kilowatt LC Load Controller LMC Load Management Center PCU Power Conditioning Unit PGS Power Generation System SCG SOSTEL Control Group SOSTEL Solid State Electric Logic TBE To be Defined VSCF Variable Speed Constant Frequency

APPENDIX A

A-7 ENGINE PAD DEFINITION
FOR
INTERFACING HVDC GENERATOR

A-7 ENGINE PAD DEFINITION

FOR

INTERFACING HVDC GENERATOR

1.0 Enclosed are drive pad definitions for the two engines used on the A-7. The HVDC generator can be suitable mounted on either in terms of available space, overhung moment, and available torque. A suitable gear box is required for attaining the desired speed/rotation for the generator. The drive pads are summarized as follows:

1.1 TA-7C (TF30-P-408 Engine)

- a. Power Take-off (CSD) Pad Special, see enclosure (1), counter clockwise rotation (looking at pad).
- b. Pad Output RPM Range 4000 to 7500 RPM (.488 N2 RPM).
- c. Max. allowable overhung moment 2,500 in-1b.
- d. Max. permissible torque, See Enclosure (2).
- e. Max. available space envelope available for generator installation: 11.0 inches diameter x 24.00 inches long.

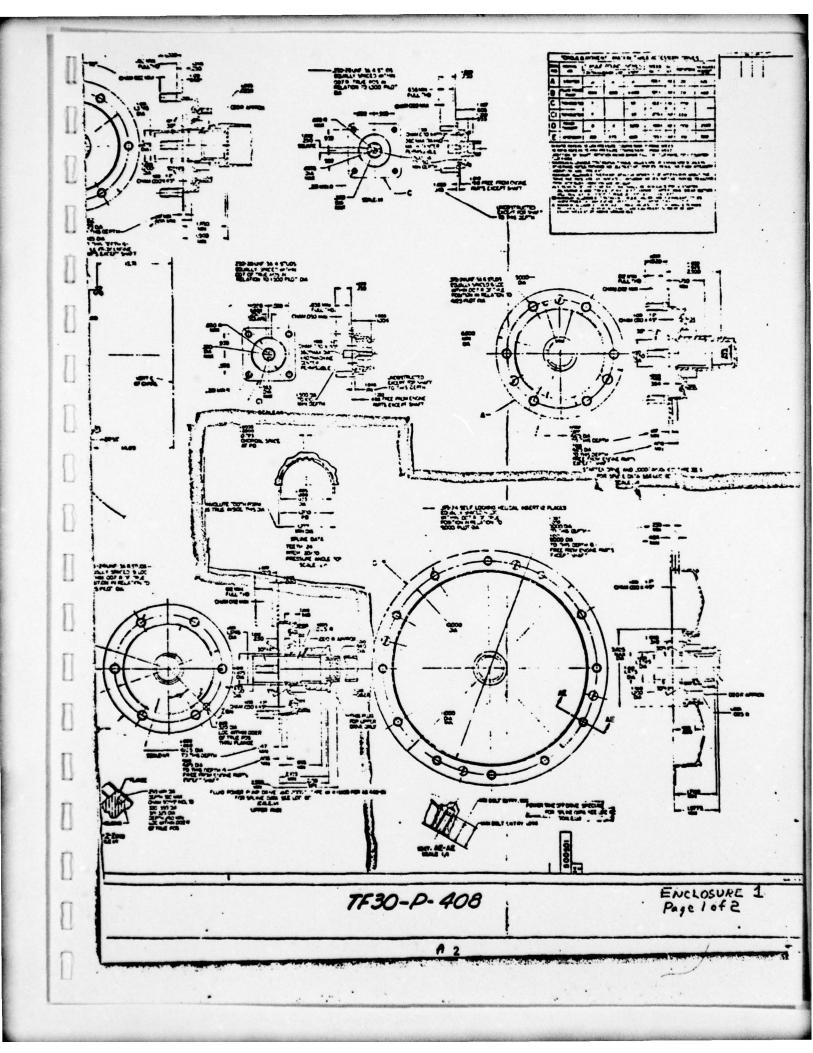
1.2 A-7E (TF41-A-2 Engine)

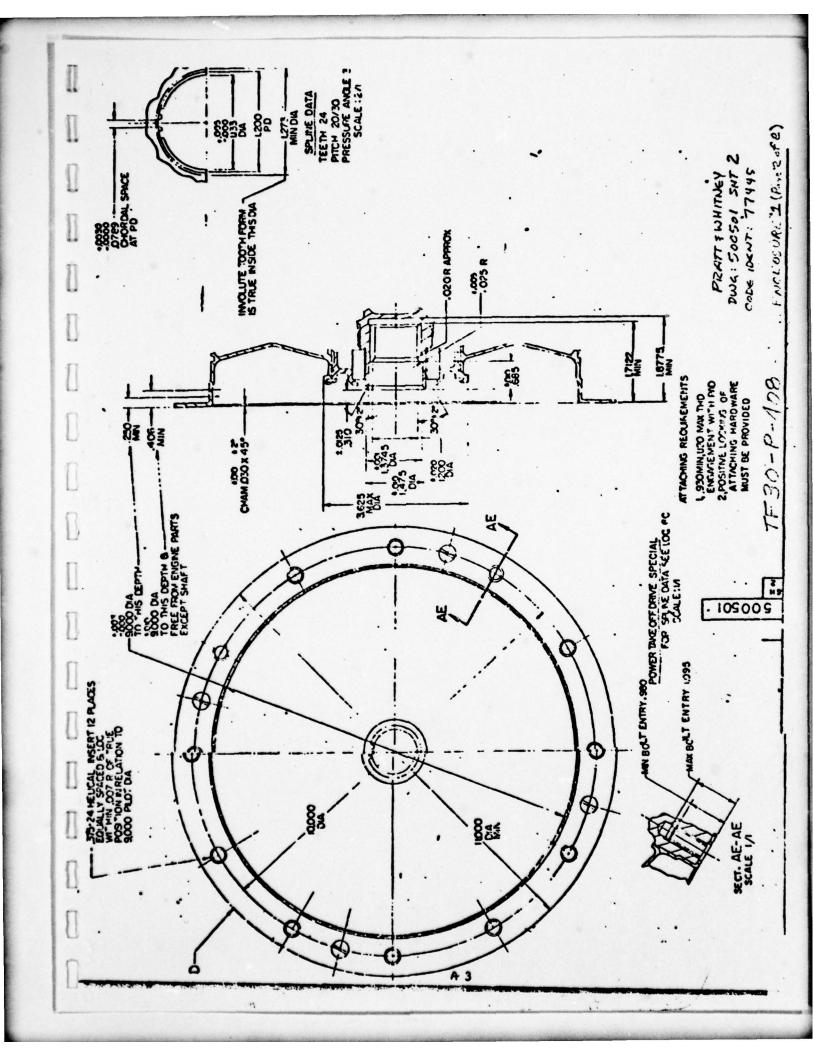
- a. Power Take-off (CSD) Pad Special, see Enclosure (3), counter clockwise rotation (looking at pad).
- b. Pad Output RPM Range 4074 to 7459 RPM (.574 N, RPM).
- c. Max. allowable overhung moment 2,500 in-1b.
- d. Max. permissible torque: Continuous 2354 lb.-in. @ 4074 RPM (152 HP),

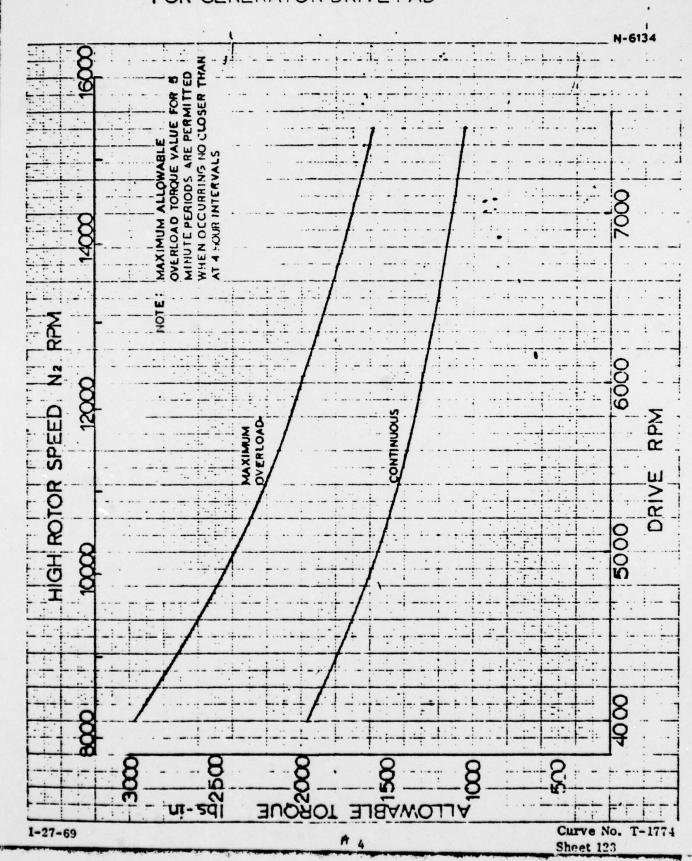
Continuous 1060 lb.-in. @ 7459 RPM (125 HP). 5 Min. Overlead 3750 lb.-in. @ 4074 RPM (242 HP).

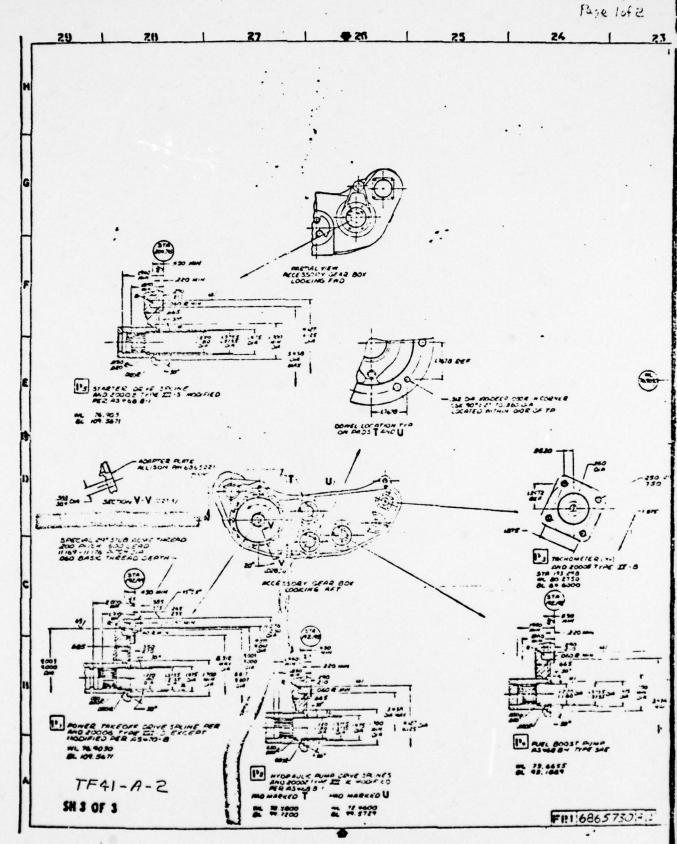
e. Max. available space envelope available for generator installation: 11.0 inches diameter x 24.0 inches long.

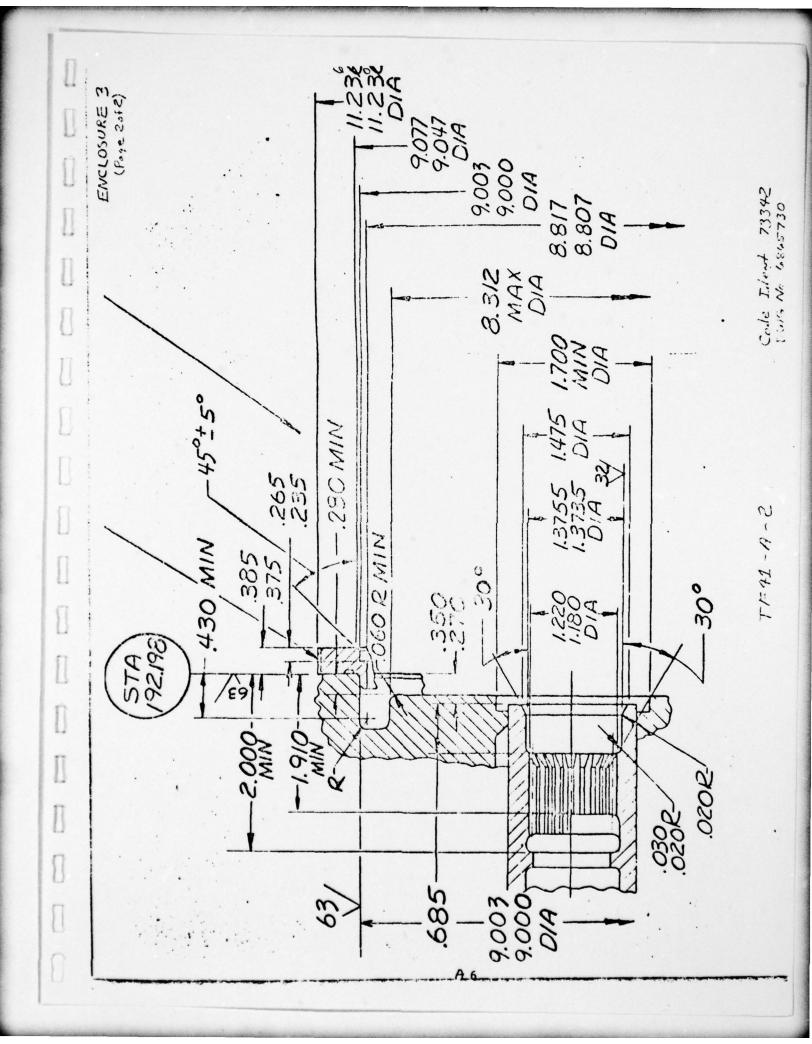
NOTE: Enlargements are provided to show details of pad.











APPENDIX B

GFE EQUIPMENT LIST

TABLE B-1: SIMULATOR GFE EQUIPMENT LIST

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1.4	IABLE B-1: SIMULATOR G	GFE	ŭ	EGUIPMENT	Z.	2	LISI								
		_			QTY				_	_	_		_		
NOMENCLATURE	PART NO. OR SIMILAR TO	CLE	GFE .	aov	HEMORK HEMONE	BEPLACE	LOCATION	DESIGN AND	SET THOUSE	SIMULATOR	EVALUATOR	WOCK NE	лэ н то	REMARKS	TEST TEST REGO
SIDS SIG CONDITIONER	CV2529/APG		×	П	-		L AVIONIC								
DIODE/RESISTOR CARD	220-27182-101	×		ㅋ			AMMO CMPT		-	×			-		
FWD STICK GRIP	215-21132-3	×		7			FWD COCKPIT			×					
AFT STICK GRIP	215-21132-3	×		٦			AFT COCKPIT			×					
ARMT ADV LTS	CVC260X SERIES	×		8			FWD INSTR B	A		×					
ARMI ADV LIS	CVC 260X SERIES	×		7	-		AFT INSTR B	A		×					
GUN CONTROL UNIT	216-27209-2	×		7			LOX CMPT								
GUN CMPT PURGE VALVE	215-26106-3	×		7			MID EQUIP								
FUZE FUNC CIL PNL	C-8213/AWW-2B		×	1			LCSI-FWD								
FUZING FWR SUPPLY	AM4708A/AWW-2A		×	1			L AVIONIC								
CAMERA CONTROL UNIT	LB-17A		×	1			L AVIONIC								
CAMERA	KB-18A		×	1			AFT SHELF								
THROTTLE QUADRANT	220-21241-101	×			-		LCSI-FWD			×					
THROTTLE QUADRANT	220-21241-102	×			-		LCSL-AFT			×					
SPEED BRAKE VALVE	215-32106-3	×		-1			AFT SHELF								
WHIS/FIAPS WARN LT	cvc2553-58	×		-1			FWD INSTR			×					
WHIS/FIAPS WARN LT	cvc2553-58	×		7		_	AFT INSTR			×					
FUEL MGMT PNL-FWD	218-21270-3	×				1	LCSI-FWD			-	×				

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Table 1

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OUAL TEST REGD REMARKS Page 2 REHTO MOCK-UP EVALUATOR × × × × × × ROTAJUMIS FLIGHT TEST TEST GNUORD DESIGN AND FWD INSTR B L MID EQUIP L AVIONIC L AVIONIC L AVIONIC AFT SHELF L AVIONIC AFT SHELF AFT SHELF LCSI-AFT ICSI-FWD LCSI-AFT LCSL-AFT LCSL FWD LCSI-FWD LCSI-AFT LOCATION DORSAL DORSAL HEPLACE 1 HEMORK REMOVE H -H 00Y CU Н GFE × × × CLE × × × × × VENDOR (*) PART NO. OR SIMILAR TO CV21-406052-6 CV21-406052-6 220-21375-101 220-21174-101 215-47120-1 215-38030-5 215-68050-3 215-77709-1 215-37178-2 215-37126-2 215-37134-4 215-22151-6 218-21261-1 215-37155-3 218-11074-4 215-22106-1 cvc2600-9 220-21269 PITCH & ROLL TRIM AMPL T.E. FLAPS CTL VALVE PITCH TRIM ACTUATOR NOMENCLATURE ROLL TRIM ACTUATOR I.E. FLAPS SYNCHRO FUEL MGMT PNI_AFT APC WARNING LIGHT EMER FLAPS VALVE ACCEL TRANSDUCER AFT GEN CTL PNL GEN CIL PNI L FWD SLANT PNL L AFT SLANT PNL FWD LDG GR HDL AFT IDG GR HDL APC AMPLIFIER APC COMPUTER APC ACTUATOR 2

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Total Control

			-	EQUIPMENT	7	E	IT LIST			1	1	1		Page 3	1
		_	_		10	>					_		_		
NOMENCLATURE	PANT NO. OR SIMILAR TO	VENDOR	GFE.	OGA	REMOVE	немонк	LOC PTION LOCATION	DESIGN AND	ST GNUORD	FLIGHT TES	TOTALLIAVE	EVALUATO	MAHTO	REMARKS	OUAL TEST REGD
SPEED BRAKE POS IND	216-21573-1	×		2			FWD & AF	E _			×	-	-		
SPD BRAKE POS SYNCHRO	215-77709-1	×		1			R CHEEK				×	-	-		
FUEL QIY IND-FWD	215-21301-1	×		1			FWD INSTR	gr.			×	-	-		
FUEL QIY IND-AFT	220-21301-101	×		٦			AFT INSTR	p4			×	-	-		
DOPPLER CIL PNL	216-21380-1		×	7			RCSI-FWD								
DOPPLER TRANSCIEVER	216-37629-1		×	-1			R AVIONIC	Ŋ					-	APN=190 System	
DOPPLER ANTENNA	216-37525-1		×	4			MID EQUIP	д			-				
RH PITOT TUBE	856W4 (O4274)		×	-1			R COCKPIT	H			×				
STBY ATT IND	MS17249-1		-	X 2			FWD & AFT COCKPIT	E			×				
RATE GYRO	MS17399-1		-^	×			L AVIONIC	Ŋ			×		-		
VERTICAL GYRO	CN1169A (30003)		-	X			R AVIONIC	D)			×		-		
INS CONTROL	216-21355-3		×	근			RCSL FWD						\dashv	_	
IM UNIT	216-37340-7		*	-=			L AVIONIC	Ŋ	_				-	ASN-90 System	
ADAPT FUR SUPPLY	216-37631-9		×	-			L AVIONIC	U	-			1	-		
REMOTE COMPASS XMTR	MS25396-1		-	X			AFT EQUIP	P.							
ANGLE OF ATTACK IND	MS28067-2		-	X Z			FWD & AFT INSTR BD	EL.			×		-		
APPROACH INDEXER	MS25317-7		×	2			FWD & AFT INSTR BD	EH _			×				
RUDDER PEDAL SHAKE'R	C15302 (83326)		×	2			FWD & AFT	FT			×				

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Section 1

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Total Section 1

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QUAL TEST REOD REMARKS Page 4 MAHTO MOCK-UP ROTAUJAVE × × × × ROTAJUMIS × × FLIGHT TEST GROUND TEST DESIGN AND AFT INSTR BD FWD & AFT INSTR BD L DUCT WALL AFT COCKPIT FWD INSTR BD AFT COCKPT FWD & AFT INSTR BD L AVIONIC L AVIONIC L COCKPIT LOCATION HEPLACE REMORK QT.Y HEMONE 3 N -N N GGA 1 --9 × × GFE CLE × × × × × × VENDOR MS25318 (-2,-3,-4) PART NO. OR SIMILAR TO 220-27105 -101 220-27166-101 220-21271-101 215-21124-3 216-17411-1 215-27143-1 MS18028-1 MS17394-1 CVC2600-7 NOMENCLATURE AFT FLT MODE PNL AOA TRANSDUCER DEMOD SWITCH APPROACH LIS ATT DIR IND

FWD INSTR BD FWD INSTR BD FWD INSTR RCSL FWD L AVION R AVION R AVION L AVION X ~ ~ × × × ID-1665/ASIN-99 216-21245-32 216-21245-26 218-37267-21 218-27505-1 216-21231-4 216-37194-1 218-37668-4 LATERAL ACCELOMETER IN RAINGE INDICATOR PROJ MAP DISP UNIT PROJ MAP ELEC UNIT HEADS-UP DISPLAY TURN RATE GYRO HUD ELEC UNIT AIRSPEED IND RELAY CARDS NAD CONTROL THO MOUNT PMDS XFMR DC AMPLR

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OUAL TEST REOD REMARKS Page 5 язнто MOCK-UP EVALUATOR × ROTAJUMIS × × × × × FLIGHT TEST TEST GNUORD DESIGN AND FWD INSTR BD AFT INSTR BD FWD INSTR BD AFT INSTR BD FWD & AFT RCSL MID EQUIP FWD & AFT INSTR BD FWD & AFT INSTR BD DUCT WALL DUCT WALL MID EQUIP MID EQUIP MID EQUIP MID EQUIP AFT SHELF L AVIONIC RCSL AFT RCSL FWD LOCATION HEPLACE HEMORK REMOVE aav a N a Н ч -Н --Н × × × × GFE × CLE × × × × × VENDOR PART NO. OR SIMILAR TO 220-21203 -101 220-21201-102 220-21366-103 220-21201-101 220-21366-104 216-37183-14 215-21222-25 218-27590-1 215-22122-2 215-27156-3 KY651/ARA63 R1379/ARA63 C7949/ARA63 215-32101-1 215-32331-1 215-32331-1 218-21680-1 MS17869-1 HYD ACCUM HTTR BLANKT NOMENCLATURE LGS SELECTOR VALVE LAUNCH BAR WARN LT DIG DATA FORMATTER WINGFOLD CTL ASSY LAUNCH BAR VALVE NATO MONITOR DISP WINGFOLD VALVE ACLS CIVIL PINI HORIZ SIT IND CMD XFER PML ACIS DECODER CMD XFER PML NAD COMPUTER HUD MONITOR HUD CAMERA ACIS RCVR ARG VALVE

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QUAL TEST REOD REMARKS Page RBHTO MOCK-UP ROTAULAVE X × × × × × × × × × × × × × × × HOTAJUMIS FLIGHT TEST GROUND TEST DEV TEST L&R AVIONIC FWD & AFT INSTR BD COCKPIT FWD & AFT COCKPIT AFT CKPT MID EQUIP MID EQUIP MID EQUIP AFT SHELF AFT SHELF AFT SHELF LOCATION COCKPIT COCKPIT COCKPIT COCKPIT COCKPIT COCKPIT COCKPIT COCKPIT FWD REPLACE HEMORK REMOVE Q 2 8 2 a 9 O Q N 2 OOV 2 GFE × CLE × × × × × × × × VENDOR (*) PART NO. OR SIMILAR TO A4950A-1 (72914) 50-0018 (72914) A9555-2 (72914) CP53B5FE504VI 220-21151-109 CV21-207503-2 CV21-407505-1 CV21-407505-1 220-21151-107 215-36320-2A 216-27383-26 216-27383-27 218-27538-1 218-27538-4 215-77300-1 210-29276-1 MS17245-5 A6331-1 36271-1 UPPER ANTI-COLLISION LT SEAT ADJUST ACTUATOR CAPACITOR ASSY BEAT ADJUST ACTIVATOR NOMENCLATURE COCKPIT UTILITY LI DINMER PWR SUPPLY MASTER CAUTION LT DIMMER PWR SUPPLY WHE FLOOD LIGHTS ELECT COMPT FAN LAND TAXT LIGHT RED FID LIGHTS LIGHTING XFMR TRIMMER PANEL TRIMMER PANEL FORMATION LT FORMATION LT TAIL LE TAIL IN

SIMULATOR GPE EQUIPMENT LIST

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QUAL TEST REOD REMARKS Page 7 RAHTO MOCK-UP ROTAUJAVE × × ROTALUMIS FLIGHT TEST TEST GNUORD DESIGN AND FWD & AFT RCSL MID EQUIP DUCT WALL R AVIONIC R AVIONIC AFT-SHELF AFT SHELF R AVION LOCATION COCKPIT COCKPIT REPLACE BEMORK HEMOVE S aav 7 -N N a ٦ Н Н Н 1 × × × × GFE × CLE × × × × × × × × VENDOR (*) PART NO. OR SIMILAR TO AM-3624/ARA-50 220-24514-102 220-27020-103 220-24515_101 220-27021-102 C9054/ARN-84 218-21675-2 216-60090-4 215-22337-1 215-22330-1 215-43301-1 215-37151-1 215-33308-1 216-60090-4 218-37530 AV16B1601 CANOPY LOCK ACTUATOR FUEL TRANSFER VALVE NOMENCLATURE EPP ACTUATOR VALVE UHF-ADF AMP-RELAY UHF-IFF DUPLEXER CANOPY ACTUATOR BATTERY CHARGER FUEL DUMP VALVE UHF-ADF ANTENNA UHF-IFF ANTENNA BAITERY, CANOPY TONE GENERATOR THERMAL SENSOR TACAN CONTROL PROBE LIGHT PROBE VALVE

SIMULATOR GFE EQUIPMENT LIST

QUAL TEST REGO REMARKS Page 8 MAHTO MOCK-UP ROTAULAVE × × ROTAJUMIS FLIGHT TEST TEST ONUORS DESIGN AND FWD & AFT INSTR BD MID EQUIP INSTR BD FWD & AFT LCSL FWD & AFT LCSL DUCT WALL FWD & AFT INSTR BD FWD & AFT INSTR BD MID EQUIP MID EQUIP MID EQUIP MID EQUIP LOCATION R AVION R AVION R AVION R AVION L AVION R AVION HEPLACE 2 HEMOHK OTY REMOVE X 7 0 N aav -H --N × × × × × × × × GFE CLE × × × × × VENDOR PART NO. OR SIMILAR TO ID-1972/ARC-159 CVC2601 SERIES ID1760/APM-194 CV2230A/ASW-25 RT1150/ARC-159 ROTR-AD-18709 CV21-010001-4 C9815/ARC-159 220-37455-101 220-21362-101 220-27416-105 C:/100/ASW-25 C6624/AIC-25 218-77514-1 RT1022/ARN84 218-77514-1 SA-521A DATA LINK RCVR- CNVTR NOMENCLATURE UHF SWITCHING UNIT DATA LINK DISC LTS DATA LINK ANTENNA AUDIO CONTROL PNL HEIGHT INDICATOR INTERCOM STATION TACAN COAXIAL SW UHF CONTROL PNL TACAN XMIR/RCVR TACAN UPPER ANT TACAN LOWER ANT UHF CHANNEL IND DATA LINK CTL UHF XMIT RCVR TACAN BLOWER TACAN MOUNT AUDIO UNIT

EQUIPMENT LIST SIMULATOR GFE

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OUAL TEST REOD REMARKS Page 9 **В**ЭНТО MOCK-UP ROTAULAVE FLIGHT TEST GROUND TEST DESIGN AND FWD & AFT INSTR BD MID EQUIP LOCATION R AVION R AVION NOSE HEPLACE HEMOHK OTY REMOVE 2 aav 1 O Н GFE CEE × VENDOR PART NO. OR SIMILAR TO HEIGHT INTERFERENCE BLANKER MX9132A/APN-194 /APN-194 RT1042/APN-194 216-27122-8 AAU-19/A IND RCVR-XMIR NOMENCLATURE HEIGHT IND ANTENNA ALTITUDE INDICATOR RADAR SET HEIGHT

× × AFT INSTR BU MID EQUIP FWD INSTR BD FWD INSTR BD FWD LCSL CAN DECK NOSE NOSE NOSE NOSE NOSE --Н ч -× × × × × × MT-4043/AP9126 220-21242-101 220-21242-102 220-27121-101 PP6130/AP9126 216-21600-10 216-21143-7 216-27877-1 216-27393-4 CVC6070-5 cvc6070-6 RADAR DIG SCAN CNVR RADAR FWR SUPPLY RADAR INDICATOR RADAR INDICATOR RADAR RANGE CTL RADAR FAULT LOC RADAR CTL PNL. RADAR BLOWER RADAR MOUNT RADAR XFMR RADAR XFMR

SIMULATOR GFE EQUIPMENT LIST

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NOMENCLATURE	PART NO. OR SIMILAR TO	CLE	GFE	PEMOVE	REMORK	REPLACE	LOCATION	DESIGN AND	GROUND TEST	ROTAJUMIS	EVALUATOR	MOCK-UP	РЕНТО	REMARKS	QUAL TEST REGD
RADAR ANT TILT CIL	220-21186-101	×		п			AFT LCSL								
IFF TRANSPONDER CTL	c-6280/AFX		×	2			FWD & AFT LCSL								
IFF TRANSPONDER TESTER	TS-1843/APX-72		X	н			R AVION		-	-					
IFF RCVR-XMIR	RT-859/APX-72		×	ㅁ			R AVION			_					
INTERFERENCE BLANKER	216-37162-3	×		-1			L AVION			-	_				
RHAW CTL PML	218-21195-3	×			_		FWD RCSL			-					
RHAW RCVR	R1764/ALR-50		×	н			R AVION			-					
RHAW ANALYZER	TS3053/ALR-45	×		7			L AVION			-	_				
RHAW INTERFACE	218-37503-4	×					L AVION			-					
RHAW ANTENNA	AT-741A	×					MID EQUIP			-	-				
RHAW ANTENNA	01-23-03721	x		1			MID EQUIP							(CODE IDENT 15280)	
RHAW INDICATOR	31-011203-01	×		н			FWD INSTR BD			-				(CODE IDENT 15280)	
RHAW PREAMP	31-027824-01	×	•	4										(CODE IDENT 15280)	
RHAW ANTERINA	AS2605/ALR45	×	•	2			DUCT WALL								
RHAW ANTENNA	21-027827	×	- 1	2	_		AFT SHELF			-	-			(CODE IDENT 15280)	
INTEGRATED ECM PNL	218-21243-2	×		-	-		FWD RCSL		1	-	-	_			
PROGRAMMER	MX7718/ALE-29A		×		_		COCKPIT			-	-	_			
CHAFF SEQUENCER	SAL557/ALE29A		×	2			AFT SHELF								

SIMULATOR GFE EQUIPMENT LIST

QUAL TEST REQD REMARKS Page 11 MAHTO MOCK-UP ROTAUJAVE × × HOTAJUMIS × FLIGHT TEST TEST GNUORD DESIGN AND DUCT EQUIP DUCT EQUIP DUCT BOUTP DUCT EQUIP DUCT EQUIP DUCT EQUIP FWD & AFT RCSL MID EQUIP AFT SHELF FWD RCSL AFT LCSL LOCATION R AVION HEPLACE --HEMOHK OTY SVOMSR dov Н Q a --Н × × × × × × GFE CFE × × × VENDOR PART NO. OR SIMILAR TO 4S-1739A/APN154 CU-1104/APM154 MD-817/APN154 220-21299-101 MX7721/ALE29A 220-37125-101 RT763/APN1.54 C4419/APM154 218-21399-3 215-37152-1 AS2406/APR R1623/APW NOMENCLATURE

× R. AFT CKPT L. AVIONIC MID EQUIP MID EQUIP MED EQUIP ERH U. 8 m -m × × 216-17411-1 216-32497-1 216-32483-1 216-17411-1 216-17411-1 216-26205 RADAR BEACON MODULATOR RADAR BEACON DUPLEXER RADAR BEACON CTL PNL RADAR BEACON ANTENNA RADAR BEACON ANTENNA INT-EXT LIS CTL PNL HYDRAULIC SOLEMOID RADAR BEACON RCVR TEMPERATURE PROBE RADAR BEACON XMTR AIR DATA COMPUTER PURSE DOOR VALVE INT LTS CTL PNL CHAFF DISPENSER GUN RATE VALVE RELAY CARDS RELAY CARDS RELAY CARDS

				-	0	EQUIPMENT	JEN		LIST					Page	7	2	1
_				_		0	,						_		_		•
	MOMENCLATURE	PART NO. OR SIMILAR TO	VENDOR	310	004	REMOVE	MEWORK	REPLACE	LOCATION	DESIGN AND	ST GNUORD	FLIGHT TES	EVALUATO	MOCK-UP	MahTO	REMARKS	OUAL TEST REGO
	ADVISORY LIGHTS PANEL	220-21353-101	X	14			П	<u>E</u>	FWD R CSL				×	-	_		
	ADVISORY LIGHTS PANEL	220-21353-102	×				Ч	4	AFT R CSL			~	×	-			
	HYDRAULIC PRESS XMITTER	216-32499-1	×	-	a			4	S.					-	!		
	PRESS RATIO INDICATOR	215-21185-1	×	- 14	2			EH	FWD & AFT INSTR BD						_		
	OIL PRESSURE INDICATOR	MS 17996-2	×		7			4	AFT INSTR BD				-	-	_		
7	OIL PRESSURE INDICATOR	218-21538-1		×	7			-	FWD INSTR BU				-				
3 12	FUEL QIY SIM ASSY	216-27361-1	×		러			Σ	ATD EQUITS								
<u> </u>	TACHOMETER INDICATOR	NS 21971-2	×	u	2			타버	FWD & AFT INSTR BD								
	FUEL FIOW INDICATOR	EFU-7/A	×		2			FH	FWD & AFT INSTR BD								
لتت	TURBINE INLET TEMP IND	215-21338-1	~	×	2			FH	FWD & AFT INSTR BD								
	PITOT HEATER	856W-1	^	×	٦			Ö	COCKPIT							•	
	ACCEL COURT INDICATOR	MS 25448-1	×		!				UT SHELF		1	-	-				
	ACCEL COUNT TRANSDUCER	MS 25447-7	×		7			4	AFT SHELF								
	ANTI-SKID CONTROL UNIT	218-34251-4	×	-	-			- 12	RH AVION			T			-		
	ANTI-SKID CONTROL VALVE	216-34251-1		×				4	AFT SHELF						_		
	ANTI-SKID SHUTOFF VALVE	216-32498-1		×	-1	_]		4	AFT SHELF			1	\neg	\neg	-		
	BATTERY RELAY ASSY	220-2725-101	^	×	7			F	COCKPIT			-	×	-	-		
	•				_				1	:				_			
j				1	ļ	1	1	I		١	1	İ	1	1	1		

			입	EQUIPMENT	Z E		. IIST	15	1231	-	-	- C			
MOMENCIATINE	PART NO. OR SIMILAR TO	CEE	340	REMOVE	PEWORK	REPLACE	LOCATION	DESIGN AND	T GHUORD	FLIGHT TE	SIMULATO	EVALUATO	MOCK-U	ACMANKS	OVAL TEST REGO
PARABRAKE CONTROL VALVE	215-22120-2	×		귀	_		AFT SHELF						-		
•	397690-1-1(99 193)	×	-	ਜ			R COCKPIT							•	
RAIN REPELIANT VALVE	MS 29527-1	×		ਜ			"RADAR COMPT"						-		
ACCUM HEATER BLANKET	215-27156-1	×		ᆔ	!		MED EQUIP						-		
ACCUM HEATER BLANKEE	215-27156-3	×		ᆔ			MID EQUIP						-		
FUEL SHUTOFF VALVE	215-43307-2	×		a			AFT SHELF				-				
ANTI-COLLISION LIGHT	216-37341-4	×		귀			BASE						-		
WING POSITION LIGHT	215-87300-1	×		ᆔ			AFT SHELF								
WING POSITION LIGHT	215-87300-2	X	-	규			AFT SHELF								
WING FORMATION LIGHT	215-87120-1	X		ਜ			AFT SHELF								
WING FORMATION LIGHT	215-87120-2	×		न			AFT SHELF								
FUSELAGE FORMATION LIGHT	CV21-408505-1	×		8			MID EQUIP								
HYD DUMP SURGE DAMPER	215-22308-1	×		ਜ			AFT SHELF								
HYD ACCUMITATION	215-22102-8	×		2			MED EQUEP					-			
HYD ACCUMITATION	215-22102-10	X		न			MED EQUEP								
HYD ACCUMULATOR	215-22102-11	×		7			MID EQUIE						_		
FUEL SHUTOFF VALVE	215-73301-1	×		#			AFT SHELF						-		
THERMAL SENSOR CIT.	215-33308-2	×		ਜ	_		AFT SHELF				-	-	\vdash		

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•					2		٠			-					
MOMENCLATURE	PART NO. OR SIMILAR TO	CEE	310	004	REMOVE	30AJ93A	LOCATION	DESIGN AND	ST GNUORD	FLIGHT TES	EVALUATOR	MOCK-UP	МЭНТО	REMARKS	TEST REGO
PRESSURE SHUTOFF VALVE	215-73302-1	×		ㅋ	-		AFT SHELF				-				
AIR PRESSURE VALVE	215-43300-2	×		П		-	AFT SHELF								
PRESSURE REGULATOR VALVE	215-43304-5	×		Ä		-	AFT SHELF					_			
FIRE DETECTOR	215-27132-1	×		П		-	MOD EQUIP								
FIRE DETECTOR SENSOR	215-47301-1	×		н			AFT SHELF					_			
LIQUID OXYGEN INDICATOR	GMJ-61A	×		п			FWD L CSL								
LIQUID OXYGEN INDICATOR	GMU-65A	×		ਜ			AFT L CSL								
LIQUID OXYGEN CONVERTER	33н1083(83533)	×		н			LOX COMPT								
LIQUID OXYGEN PRESS SWITCH	PS7000-14	×		2			FWD & AFT L CSL								
FWD RT SLANT PANEL	220-21213-101	×				ᆜ	FWD R CSL				×			•	
AFT RT SLANT PANEL	220-21313-101	×				-	AFT 'R CSL				×				
FWD ARMT RELEASE PANEL	218-21020-4	×				-	FWD INST BD				×	_			
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TABLE B-2
ADDITIONAL GFE EQUIPMENT LIST

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ITEM	PART NUMBER	FSN	NOTE	SYSTEM
CLEARING SOLENOID	11010205 (81840)		1	MG1 GUN
STICK GRIP FORCE SENSOR	215-21129-8		1	AFCS
STICK GRIP FORCE SENSOR	215-21129-8		1	AFCS
MAGNETIC PICK-UP SENSOR	114C2927 (05606)		2	MG1 GUN
FIRE VOLTAGE POINT	216-29126-1		2	MG1 GUN
LAST ROUND SWITCH	13535825 (05606)		2	MCI GUN
PRESSURE RATIO TRANSDUCER	220-45302-101		2	ENG INSTR
OIL PRESSURE TRANSDUCER	121-5/A9111L-T-25642B		5	ENG INSTR
OIL PRESSURE SWITCH	215-55312-1		5	ENG INSTR
TACHOMETER GENERATOR	GEN-7/A		5	ENG INSTR
FUEL PRESSURE SWITCH	215-53301-1		7	FUEL CONTR
FUEL FLOW TRANSMITTER	TRU-12/A		5	ENG INSTR
WAVEGUIDE	216-37188-2		7	DOPPLER RADAR
WAVEGUIDE	216-37188-1		7	DOPPLER RADAR
WAVEGUIDE	216-37188-4		7	DOPPLER RADAR
WAVEGUIDE	218-27214-2		7	APP CTL LDG
WAVEGUIDE	218-27215-1		7	APP CTL LDG
WAVEGUIDE	218-27213-2		7	APP CTL LDG
ANTENNA	218-27500-1		7	APP CTL LDG
NOSE GEAR STEERING ACTUATOR	215-22130-1	•	11	NOSE GEAR STR
NOSE GEAR STEERING TRANSDUCER	215-68131-1		11	NOSE GEAR STR
AIR CONDITIONING CONTROL	216-26102-3		14	TEMP CONTROL
CABIN TEMPERATURE SENSOR	216-26119-1		14	TEMP CONTROL
SUIT AIR CONTROL PANEL	218-21257-1		14	TEMP CONTROL

TABLE B-2
ADDITIONAL GFE EQUIPMENT LIST

ITEM	PART NUMBER	FSN	NOTE	SYSTEM	
SUIT AIR TEIT SENSOR	216–26119–1		14	TEMP CONTROL	
SUIT AIRPLOW VALVE	397420-1-1 (99193)		14	TEMP CONTROL	
SUIT AIR FLOW CONTROL PANEL	216-26118-2		14	TEMP CONTROL	
CABIN AIR VALVE	397418-1-1 (99193)		14	TEMP CONTROL	
HYDRAULIC SOLENOID VALVE	215-21067-1		11	ACCUM TEST	
FUEL PRESSURE SWITCH	215-73317-1		7	FUEL TRANSFER	
FUEL FLOAT SWITCH	215-73319-1		17	FUEL TRANSFER	

NOTES:

- 1. This equipment is required for full operation of the Automatic Flight Control System. The AFCS was assigned a System Test Difficulty of 5 (the highest difficulty).
- 2. This equipment is required for operation of the M61 20M1 gun. This system has a test difficulty rating of 5+.
- 3. Use of this equipment will be somewhat meaningless without providing the fluid pressure of which is to be monitored.
- 4. This equipment is part of the engine instrumentation set and will not be operational without the TF-30 engine which generates the measured condition or without some suitable device for simulating the measured condition.
- 5. This equipment is required if electromagnetic radiation is attempted in the lab.
- 6. This equipment will not be fully operational without a hydraulic power source.
- 7. This equipment requires complicated mechanical hardware to fully evaluate the anti-skid control function.
- 8. This item is required for operation of the temperature control system. However, air conditioner operation (or installation) is not practical in the simulator.
- 9. This equipment is required for operation of the fuel transfer system. Since fuel will not be transferred, this item is optional.