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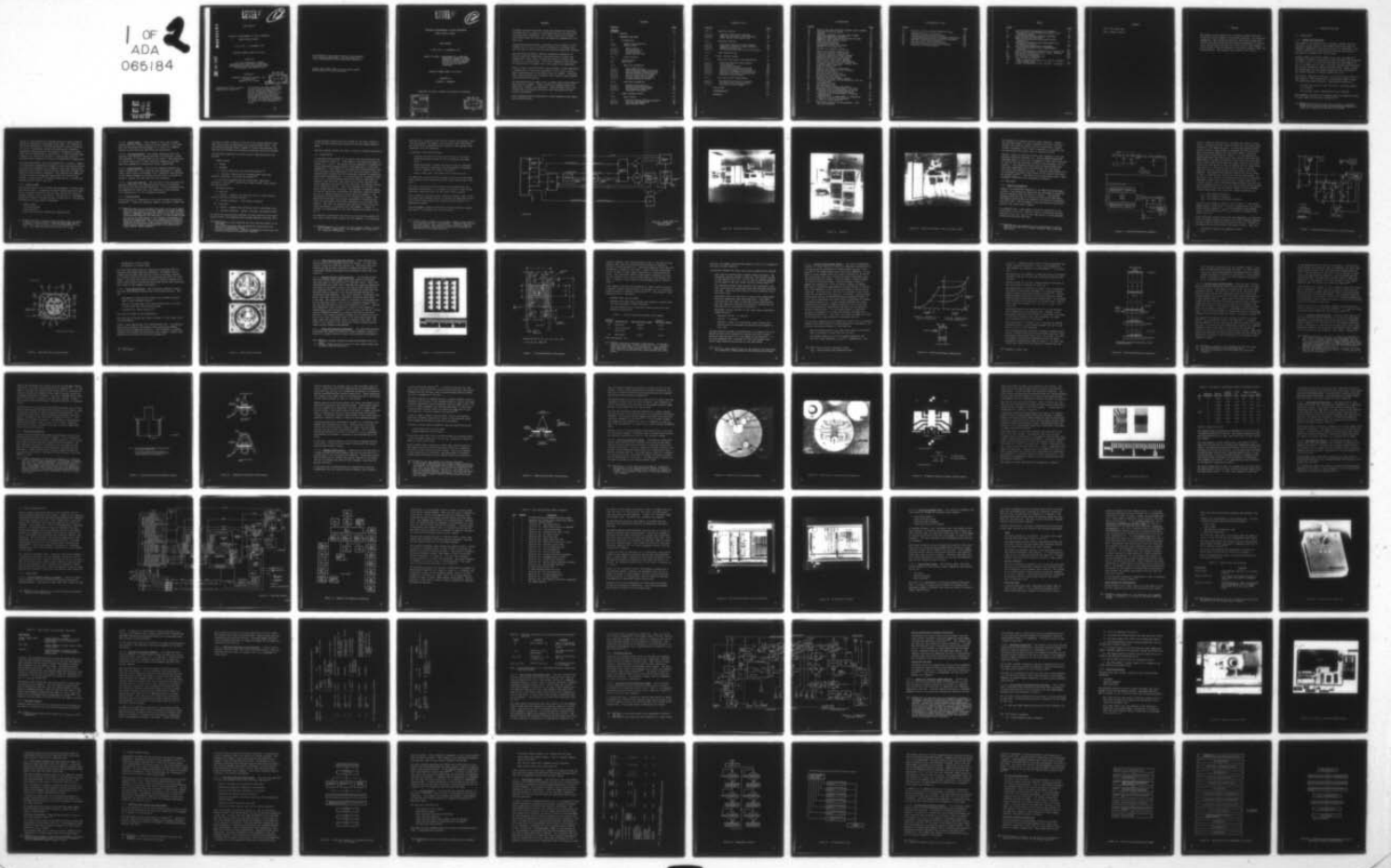

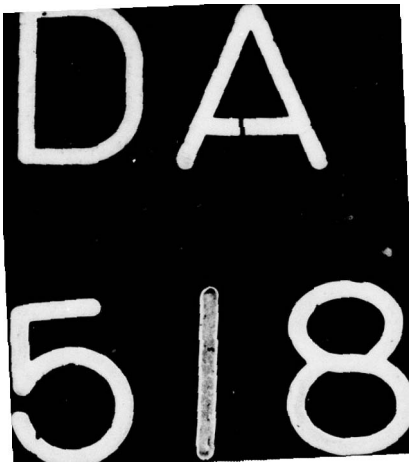
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FINAL REPORT

PRODUCTION MEASUREMENT OF FUZE COMPONENTS UNDER DYNAMIC STRESS

11 MAY 1976 - 31 DECEMBER 1978

CONTRACT NUMBER DAAB07-76-C-0032

PLACED BY

U.S. ARMY ELECTRONICS COMMAND
PROCUREMENT AND PRODUCTION DIRECTORATE
COMMUNICATION SYSTEMS PROCUREMENT BRANCH
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LEVEL II

12

PRODUCTION MEASUREMENT OF FUZE COMPONENTS UNDER DYNAMIC STRESS

FINAL REPORT

11 MAY 1976 - 31 DECEMBER 1978

OBJECT OF STUDY: DEVELOPMENT OF A COMPUTER CONTROLLED AUTOMATIC TESTER, CAPABLE OF TESTING AND TRIMMING THICK FILM ADJUSTMENT CIRCUITS AT THE RATE OF 3,000/HOUR

CONTRACT NUMBER DAAB07-76-C-0032

PREPARED BY

RICHARD F. DeMATTOS

ABSTRACT

A dynamic test and correction system was designed and partially developed which is capable of high-speed testing and laser-trimming electronic assemblies. The circuits selected for tester verification were the oscillator and amplifier assemblies of the M732 Fuze.

Program goals required that a selected critical property of each assembly be set to a ±0.5 percent tolerance at an average test and trim rate of 3000 units per hour excluding mechanical handling.

The system was designed to measure fundamental properties of modified amplifier assemblies, calculate height of burst, and automatically laser trim a thick-film resistor to adjust this property to a precise value. Oscillator assemblies were adjusted for sensitivity by trimming one of two ceramic chip capacitors.

Height of Burst (or sensitivity) was calculated in real-time using a combination of "black box" equivalent circuit and/or circuit model representations of individual test unit stages. Pre-calculated look-up tables were introduced where complex time-consuming calculations were required.

The engineering effort ended prior to system testing the program's amplifier test segment. Tester system and hardware design and fabrication, however, was completed. Three thousand (3000) amplifiers and 75 prototype oscillators were fabricated and electrically prechecked.

Basic techniques may be applicable to other assemblies with appropriate modifications.

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GLOSSARY

UUT - Unit Under Test

HOB - Height of Burst

1. PURPOSE

The purpose of this program was to develop a dynamic test and correction system, capable of high-speed operation, for electronic assemblies. The circuits selected for verification under this contract were the oscillator and amplifier assemblies of the M732 Fuze. The contract required that 3,000 units of each assembly be delivered, of which 2,900 were to have been trimmed to meet the specifications. The required test rate was 3,000 an hour.

2. NARRATIVE AND DATA

2.1 INTRODUCTION

2.1.1 Purpose and Objectives

The purpose of this program was to develop a dynamic test and correction system capable of high-speed testing and tuning inexpensive, operational electronic circuits (or assemblies). The circuits selected for tester verification were the oscillator and amplifier assemblies of the M732 fuze.

Although these circuits are unique to the fuze, the measuring techniques, hardware and computer software developed may be applied (at least in part) to other circuits requiring measurements of dc, ac or video gain (or loss), rectifier transfer characteristics and voltage thresholds, waveform analysis and/or timing, resistance measurement and the dynamic measurement and calculation of the impulse response of selected passive circuits.

The contract required the delivery of 3,000 test units (UUT's) of each assembly, 2900 of which were to have been trimmed to specific design goal specifications. These specifications are:

- Test and tune rates of 3,000 units/hour (excluding mechanical indexing).
- Trim accuracy and/or repeatability of $\pm$0.5 percent.

The parameters selected for adjustment were fuze amplifier height of burst (HOB) and oscillator sensitivity[1].

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1 Height of burst (HOB) is the fuze altitude at detonation. Sensitivity is the rms value of the oscillator detector ac output at a specified height above the ground.

Use of a "third generation" computer-controlled laser-trimming system was selected to accomplish these tasks. The computer in this case generates all the required stimulus signals (directly or via an rf modulator), selects and measures all necessary parameters, then calculates the change in resistance or capacitance for the desired HOB or sensitivity. It then controls laser trimming of a thick-film resistor or ceramic-chip capacitor, modifying their properties to obtain a desired HOB or sensitivity.

The overriding project design philosophy was to utilize a computer's calculation capability and speed to best advantage by calculating test unit responses over frequency rather than sequentially applying several analog stimulus signals (step wise or swept) and measuring point-by-point responses. This approach was essential in order to meet the test-time requirements of the M732 fuze because a single M-wave[2] stimulus signal equals or exceeds the maximum desired overall test time.

2.1.2 Scope of Work

The program scope of work included the development of tester hardware and software to accomplish the above objectives and to demonstrate technique feasibility by building, testing and tuning an adequate sample of each fuze device. The design of a high-speed, mechanical "indexer" was not included in this effort. The program was broken into four general categories:

- Tester Design
- UUT Modifications
- System Checkout
- Final Test and Tune (Feasibility) Demonstration.

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2 A fuze "amplifier" standard input stimulus signal is called an M-wave. This signal is a sinusoid whose amplitude increases as $A/(1-Bt)$, where A and B are constants and t is time. This amplitude variation is valid for $0 \leq t \leq \frac{1}{B}$.

2.1.2.1 Tester Design. Tester design in this case included system selection, design, construction and checkout of the hardware and the design and development of a "first cut" computer program to test both fuze amplifiers and oscillators.

2.1.2.2 UUT Modifications. The present production M732 fuze amplifier and oscillator assemblies were to be modified to make them adaptable to high-speed testing and tuning. This effort was to include fabrication of 3000 oscillator assemblies and 3000 amplifier assemblies to demonstrate tester capabilities.

2.1.2.3 System Checkout. The initially designed software and tester hardware were to be mated and then developed as a system using a small group of prototype UUT's. Additional modifications to the tester hardware or software and UUT's were to be made as needed to improve test and tune time and accuracies.

2.1.2.4 Final Test and Tune. The validity of the "test and tune" approach taken was to be demonstrated by tuning 3000 modified oscillators and 3000 modified amplifiers. A fully documented test and demonstration report was to be generated to show accuracy (and repeatability) of the techniques developed.

2.1.3 Goals Attained

The project was not completed as funds were limited and problems numerous[3]. Sufficient progress, however, was made to assure the

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3 These problems were principally the result of the M732 amplifier test unit effort and several computer and laser problems. Choice of the amplifier as a test vehicle was "good" in that several fundamental measurements had to be made to accurately calculate HOB enhancing the universality of the system concept.

The choice was unfortunate in that computer programming was lengthy and complicated due to the multiplicity of measurements and calculations. Further difficulties arose from the necessity of dealing with the nonlinear rectifier circuitry which requires analytic approximations that substantially effect overall system accuracy.

program's ultimate success in that the final system approach taken has a good chance of approaching the required design goals. The discussions presented herein attempt to verify this assertion and describe the problems and successes encountered during the program.

The following summarizes the work actually completed during the program:

. Tester Design

a) System

b) Hardware

1) Design (amplifier, oscillator-98 percent)[4]

2) Purchase, fabrication and assembly plus electrical checkout (amplifier, oscillator-80 percent)[5]

c) Software (excluding system integration) (amplifier, oscillator - partial[6], M-Wave final check of HOB, laser control, UUT serialization)

. UUT Modifications

a) Amplifier

1) Boards - assembly and functional test of 2900 units excluding thick-film trimming resistor.

2) Trimming Resistor - final design selection.

b) Oscillator

1) Boards - assembly and functional test of prototype units.

2) Trimming Capacitor - design finalized, prototypes tested.

The above two program areas represent the main portion of the total project effort, the remaining being system checkout and final test.

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4 Load chamber rf test probe was the only remaining effort to be completed.

5 All rf modulator parts were purchased and received but not assembled or subsystem tested.

6 Initial flowcharts only. Computer differential sensitivity and capacitance selection program was completed.

Enough hardware versatility was included in the tester design to facilitate any modifications required during the system checkout phase.

Amplifier system checkout was about to begin at program termination.

2.2 SYSTEM DESIGN

A simplified block diagram of the overall test and corrective system is shown in Figure 1a. Photographs of the system are shown in figures 1b, c, and d. The system has the capability of dynamically testing and laser-trimming modified M732 amplifier or oscillator assemblies[7]. The "heart" of the system is a Hewlett-Packard (HP) 2112A Processor which generates all UUT stimulus signals, records responses and calculates the UUT properties required to dynamically adjust these subassemblies. It also performs all controlling functions (i.e., laser positional and on-off controls, oscillator or amplifier test selection, gain selection of buffer amplifer and signal-processing circuits for both oscillator and amplifer testing and rf modulator control). Self-test features are included to assure proper system functioning. The computer, frequency counter, d/a and a/d converters, multiplexer and precision amplifier blocks are all HP subunits physically located with the computer. The multiplexer provides switching for 16 balanced-line inputs. The amplifier-electronics card, signal processing, rf modulator and power and load chamber blocks were designed and built during the program. The laser was purchased and modified to mount the UUT's signal processing, rf modulator and load chamber. Figures 1b through d are photographs of the major system blocks shown in figure 1a.

The amplifier electronics card serves as the interface between UUT test points (eight signal points) and the computer. Its principal

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7 These assemblies are similar to M732 assembly numbers 11716460 and 11718271, respectively. See paragraphs 2.3.1 and 2.3.2 for a detailed description.

purposes are to eliminate UUT loading, provide UUT/computer isolation and minimize the computer a/d converter least significant bit (LSB) error by amplifying test signals to the maximum level compatible with the converter.

In addition, this block provides:

- Buffered signals to the laser control and rf oscillator electronics cards located in the rf modulator and power block.
- Relay-controlled, low-pass filtering of the d/a converter output signals to eliminate the high-frequency components from the computer d/a output "staircase."
- Several other test- and signal-conditioning circuits.

The amplifier electronics card is physically near the UUT where signal amplification enhances converter input signal/noise (S/N) ratio.

The signal processing block provides signal conditioning for oscillator test signals. Its purpose is similar to that of the amplifier electronics card for oscillator output signals.

The rf modulator and power block samples oscillator (UUT) rf output energy and frequency shifts; it adjusts its amplitude to provide a fuze return signal that simulates ground returns at a specified altitude.

The load chamber houses an oscillator UUT and provides a pseudo-free space[8] environment for the test units.

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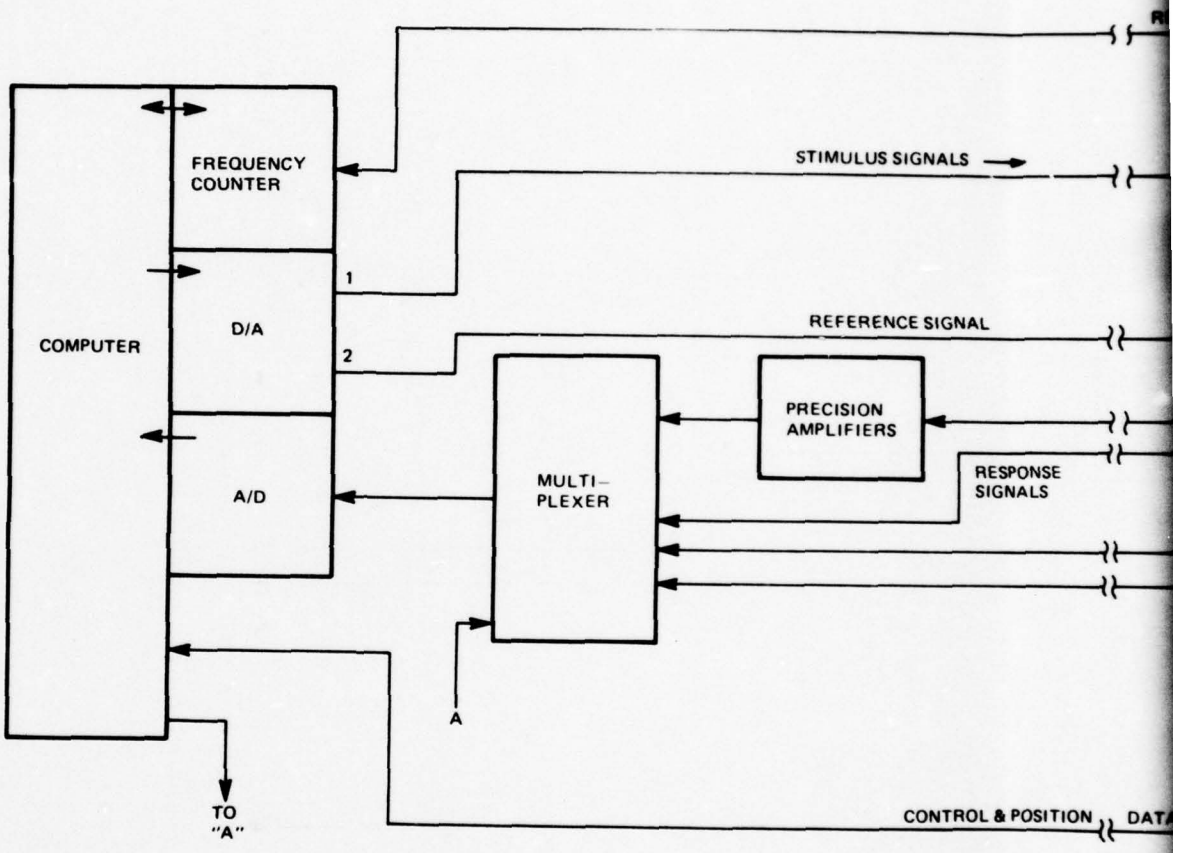
8 A true anechoic chamber is preferable; however, space restrictions mandate the use of this chamber. Absorbing material at the walls exhibit some reflection which slightly loads the test oscillators. Calibration of this unit is provided to simulate true free-space operation.



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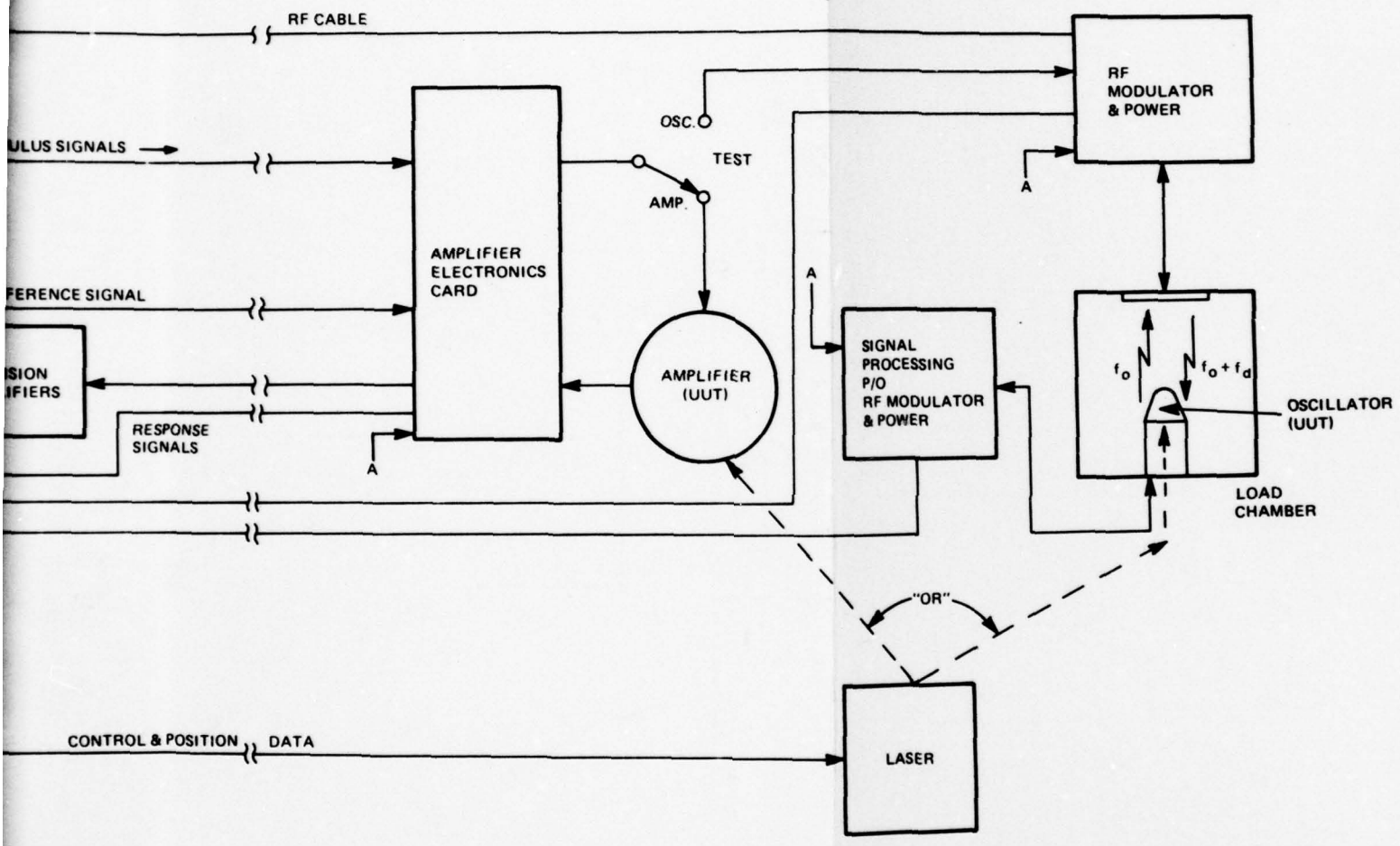

Figure 1a. Overall Test and Corrective System, Block Diagram

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Figure 1b. Test and Correction System

Figure 1c. Computer

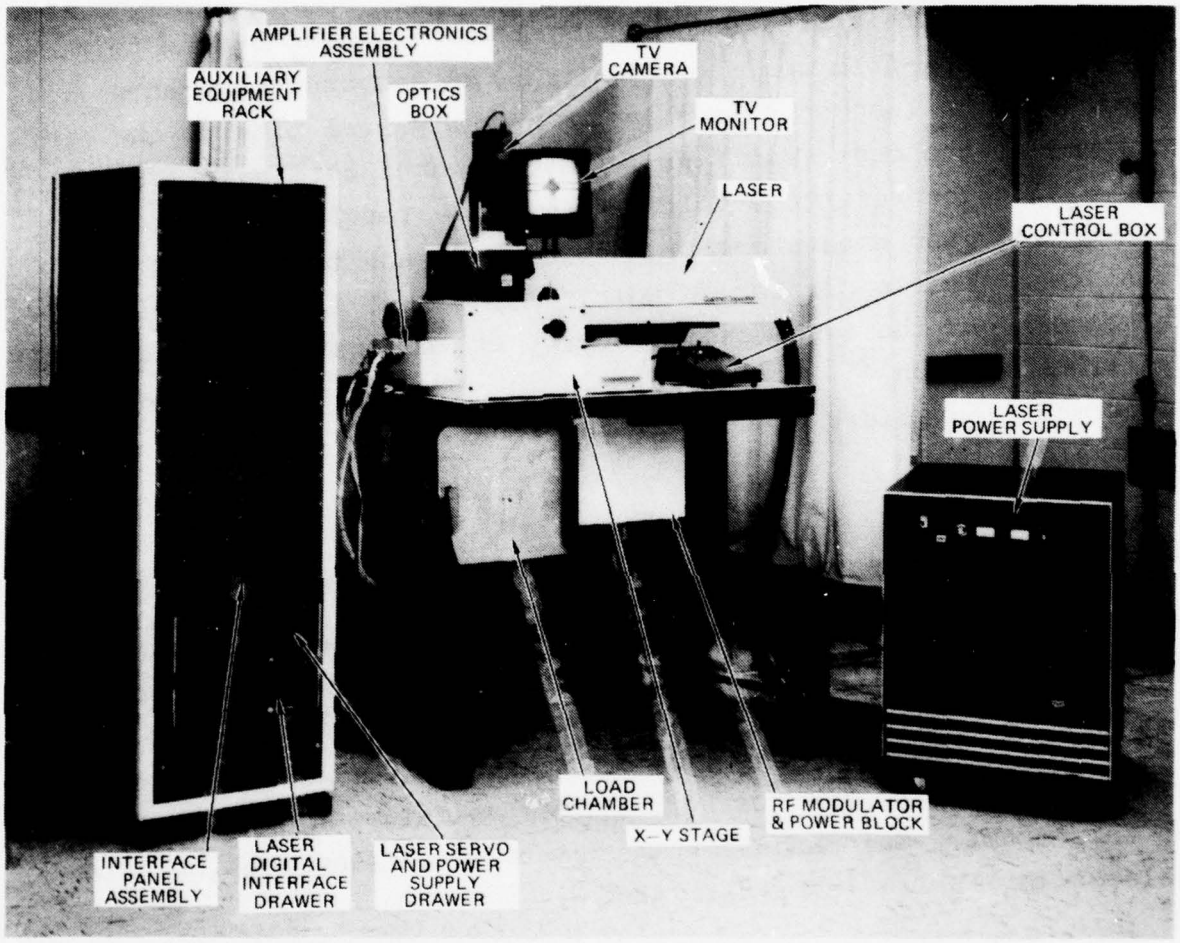

Figure 1d. Auxiliary Equipment Rack and Laser Trimmer

The computer d/a converter has two output channels. Channel 1, the principal output, is used to generate test unit "stimulus signals" for amplifier testing and for controlling a voltage variable attenuator (VVA) in the rf modulator to accurately set the amplitude-return-signal level to oscillator UUT's.

Channel 2 output is used only during laser trimming of the test amplifier thick-film resistor, R_9. The dc computer-generated reference signal on this line is compared in real time to the peak ac level at the test amplifier rectifier input terminals (V5 in figure 2). The reference-voltage level is precalculated from "pre-tune" measurements and calculated HOB, and the desired "post-tune" test amplifier ac gain. A positive laser-inhibit signal interrupts the laser output energy at the instant that these two signals match[9]. The result is an accurate post-tune ac gain adjustment regardless of R_9 resistance uniformity.

2.3 TEST UNITS

2.3.1 Amplifier Assemblies

Figure 2 is a simplified schematic of the amplifier board-signal circuits. M732 production amplifiers are individually tested for HOB by stimulating each unit with an "M-wave". This program dispenses with this test by stimulating these units with short test-signal bursts while using computer calculations to determine the unit's HOB. Gain adjustment is made by varying a thick-film resistor (R_9) using laser trimming.

To accomplish this, eight sampling points are monitored in the signal path, along with a means of rapidly initializing selected capacitors (C_{13}, C_{14}, C_{16}) so that they return to their quiescent voltage levels before each test.

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9 This approach was mandated by the nonuniformity in surface depth of the thick-film trimming resistors used in the test amplifiers.

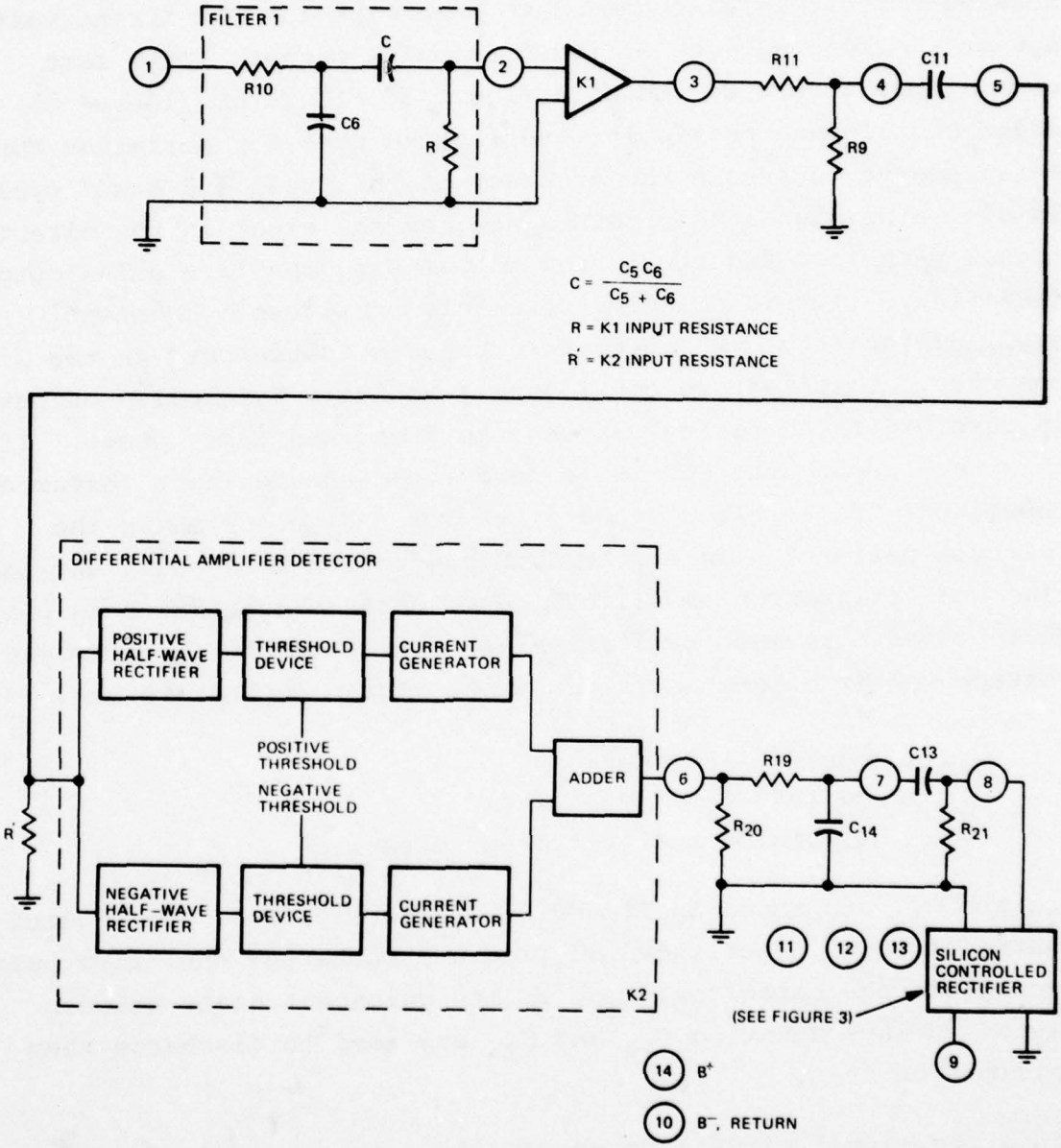

Figure 2. Simplified Amplifier Schematic

Figure 2 shows the test points in the amplifier signal circuits. Figure 3 presents the bias, energy storage, and fire pulse output circuitry on the amplifier board. A fire-pulse output-voltage-sensing circuit is also needed to determine the SCR firing voltage at the leading edge of the fire pulse output. This last sensing point is also shown in figure 3. It is considered an added signal-path test point and is also used for post-tune HOB measurements to assure the accuracy of the "test and tune" cycle. In all, nine signal test points are needed, eight in the direct signal path (see figure 2), and one sensing the fire pulse output (see figure 3). This latter point also triggers a constant amplitude one-shot, which drives the event sense card in the computer. This feature continuously monitors fire pulse output in case of "false firing" during the "test and tune" phase. If this does occur, the UUT is re-normalized and the test restarted. Subsequent "false fires" aborts the UUT. Figure 4 shows the "circuit pattern" side of the ECOM production board with the location and designation of all UUT test, quick charge and bias points. Three capacitors must be initialized rapidly to their quiescent voltage values before any given test. These capacitors are:

- C_{13} - SCR coupling capacitor
- C_{14} - The integrator capacitor
- C_{16} - Fire pulse energy-storage capacitor

C_{13} and C_{14} are shown in figure 2; C_{16} in figure 3. The "quick-charge circuit" block shown in figure 3 recharges the "fire pulse" energy-storage capacitor, C_{16}, to its quiescent state between tests. Relays shunting C_{13} and C_{14} are used to discharge them before each test.

Since the signal circuit source and load impedances are relatively high, a voltage follower is used to isolate the computer sampling circuits from the signal-path circuitry in the UUT. Several requirements must be met by these test probe circuits. They are:

- Isolation of signal from sampling circuits
- Gain

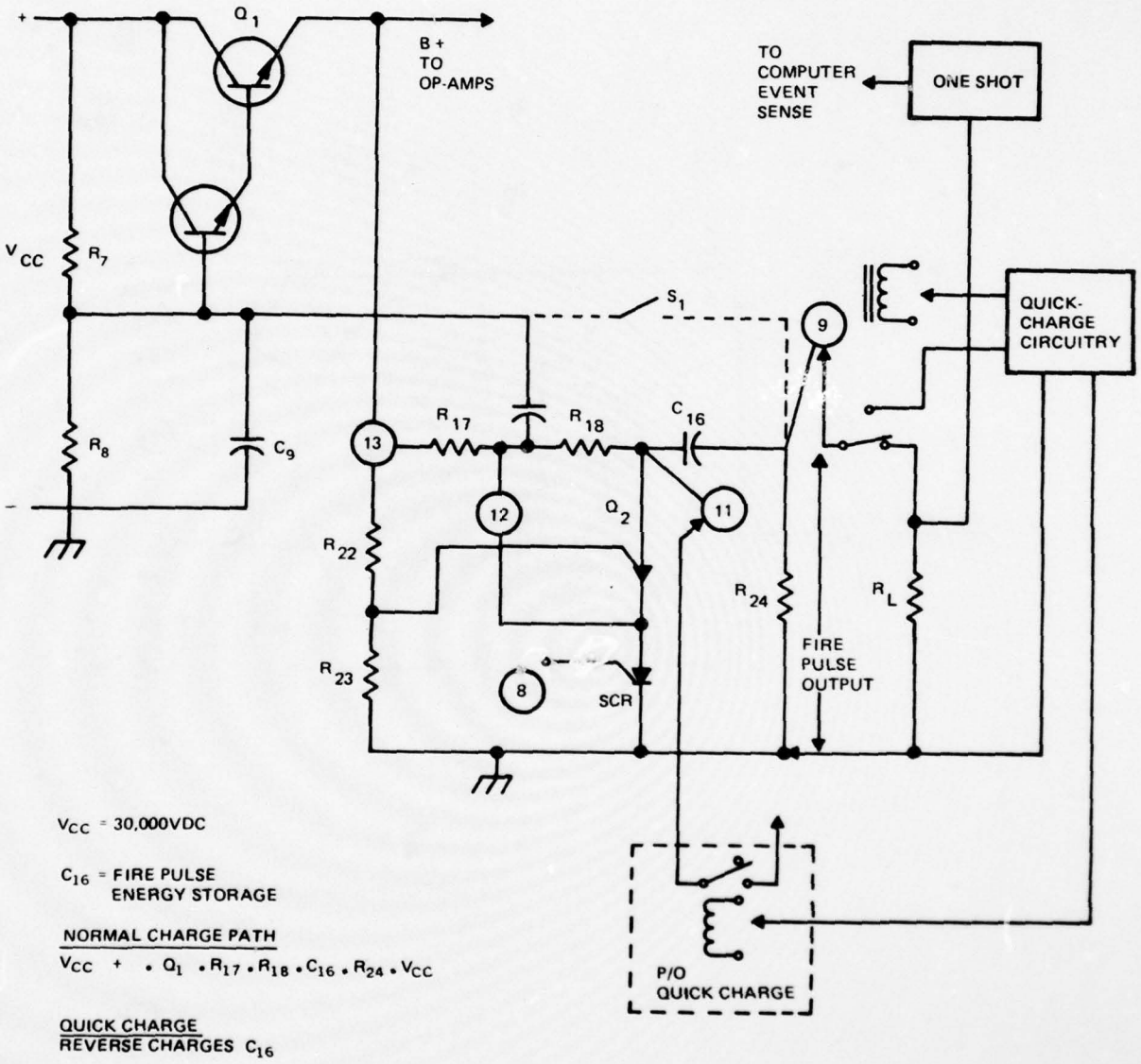

Figure 3. Amplifier Board Bias and Fire Pulse Circuits

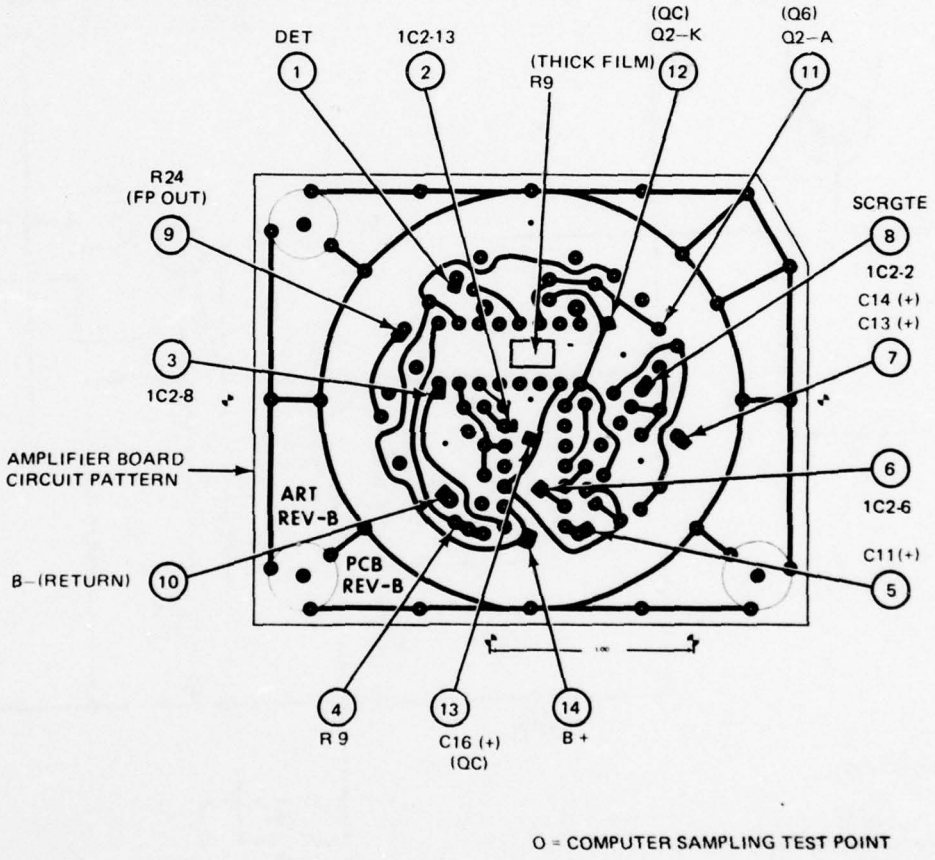

Figure 4. Amplifier Test and Bias Points

- Minimization of 60-Hz pickup
- Minimization of ground loops

The first item assures that the computer a/d converter does not interfere with normal amplifier operation. The second item increases the low-level test signals to about a 10V peak, reducing a/d converter resolution errors and minimizing the effect of 60-Hz pickup. The latter two items are needed to assure a minimum error signal which results from ground loop pickup on the lines connecting each output to the computer multiplexer.

2.3.1.1 Board Modifications. - M732 production amplifier boards had minor modifications incorporated to facilitate testing. They are:

- Replacement of M732 version resistor R_9 (an RCR07 resistor) with a laser-trimmable resistor.
- Addition of probe pads on the circuit board side of the UUT to facilitate test fixture probe pickup.
- Elimination of impact switch S_1[10].

The first two items are self-explanatory.

The third was an economy move since no plans to "fire" these units were anticipated.

Figure 5 shows photographs of an ECOM modified unit. The amplifier board shown includes a rectangular frame used by the assembly machinery during component insertion. This framework is normally removed after assembly and preliminary test; however, present ECOM production units were left with this framework on.

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10 See figure 3.

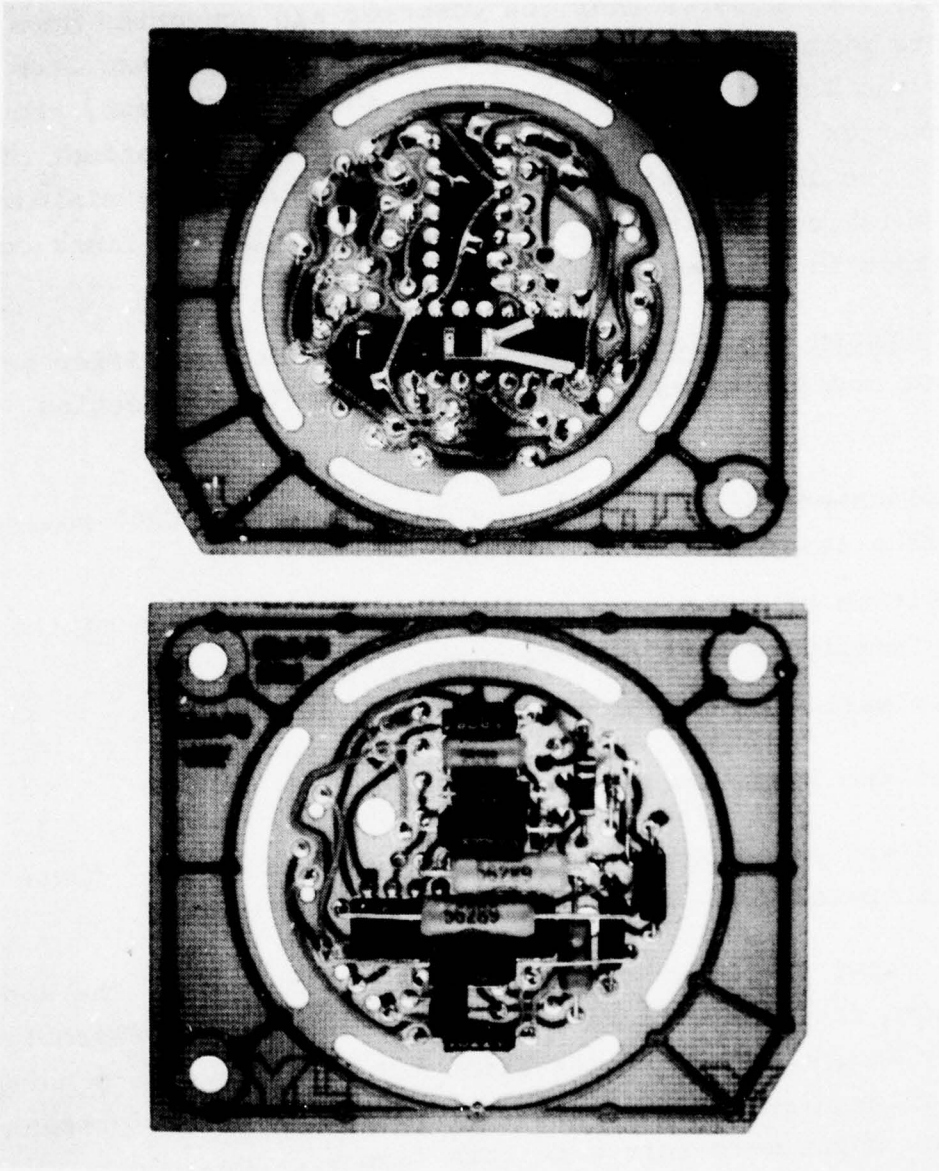


Figure 5. ECOM Production Board

2.3.1.2 ECOM Production Amplifier Boards. - Three thousand production boards were assembled during the program. All were functionally tested with 2000-ohm resistor R_9. The final thick-film resistor R_9 had not been installed in these units since only "finalized" resistor prototypes were available at this time (see figure 6).

2.3.1.3 Desired Resistor Characteristics. - The desired minimum value and cutting range needed for R_9 were based on functional test data taken on the good units[11] described above. These data (mid-band HOB) were taken with a 2000-ohm test resistor temporarily installed in the boards to obtain the range of HOB's expected for the production units. The UUT's with extreme HOB values were then retested with R_9 adjusted to the desired mid-band HOB and new resistance values measured. Five units required a resistance value below 1,400 ohms, while five required a resistance value above 2,710 ohms. This represents about 0.35 percent of the present production amplifier total. A pre-cut R_9 resistance value of 1400 $\pm$ 100 ohms was specified for the final production units[12]. Maximum room temperature power dissipation is about 0.4 mW, based on a maximum R_9/R_{11} input voltage of 3 volts dc plus 1.5V rms ac. Actual design dissipation capability is about 91 mW pre-cut and 64 mW post-cut. This latter estimate is based on a cut depth of 50 percent of the total resistance width (0.057 inch) and no more than three laser cuts equi-spaced along its length (0.080 inch). See figure 7 for a sketch of the production resistor design with the laser cut-path schedule superimposed.

2.3.1.4 Thick-Film Resistor Development. - The thick-film resistor development was geared to producing a laser trimmable, stable resistor on a ceramic substrate using "silk-screening" techniques to

11 Utilizing standard production measuring equipment and technique.

12 Figure 6 shows a pre-cut 1-inch by 1-inch ceramic plate with 24 sample 1400-ohm resistors.

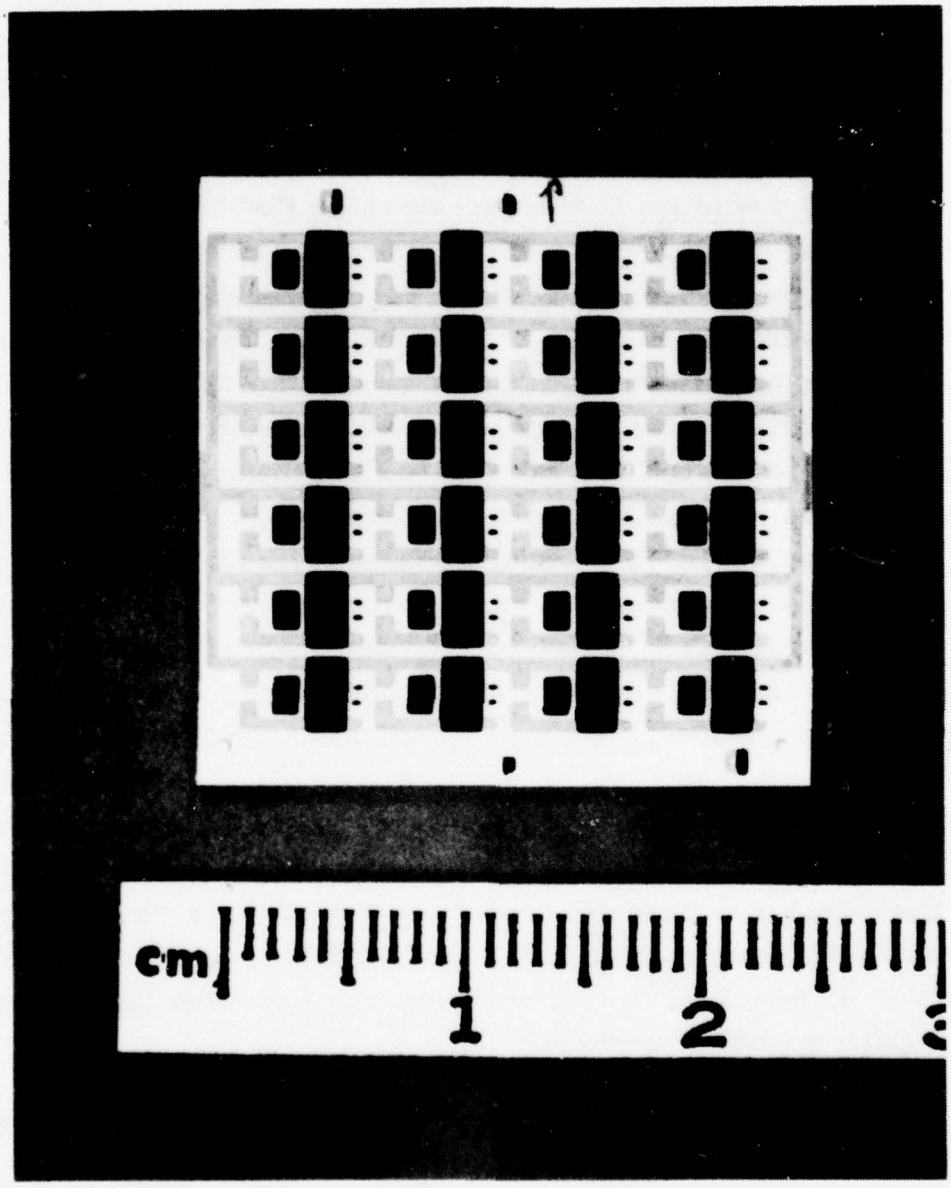
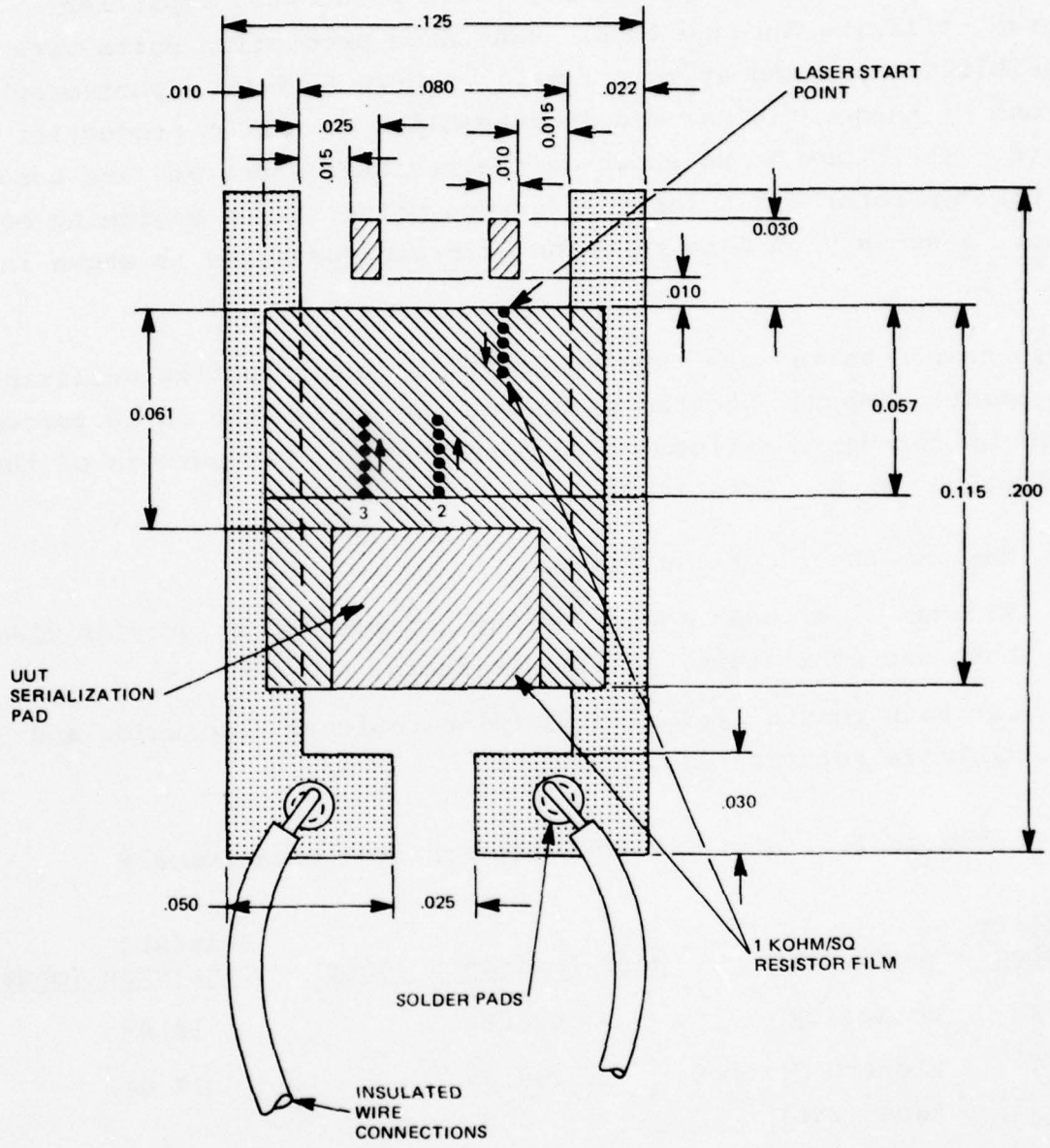


Figure 6. Final-Design Resistors



TRIMMABLE RESISTOR CHIP, R9 96% Al_2O_3 -.025"TH, (0.125" X 0.200").

R = 1400 TO 2700 OHMS $(\frac{R_{MAX}}{R_{INIT}} = 1.929)$

Figure 7. Prototype Resistor Chip Design

minimize expense. The initial design was set at 700 ohms and was based on data taken on previously built production amplifier boards utilizing Sprague IC's. (New ECOM production units were not assemblied or tested at this time.) Figure 5 shows a photograph of one of these original models assemblied to a ECOM production board. The cross hairs shown on the resistor substrate are used by the "operator" as a laser reference point at the beginning of test. A summary of data taken on 63 prototype units is shown in Table I.

These sample units were then subjected to laser cutting utilizing a separate computer program which cut the units in 5 or 10 percent steps up through a maximum of 80 percent[13]. The purpose of this evaluation was to determine:

- Maximum laser cutting range.
- Minimum laser peak power, energy and overlap to provide clean cuts and consistent, stable resistors.
- Cut path possibilities to maximize resistor resolution and minimize cutting time.

Table I. Initial Thick-Film Resistor Data Summary

Quantity Tested	Manufacturer*	Mean Resitance (ohms)	Standard Deviation (ohms)
24	Cermalloy	646.88	19.93
20	Electro Science Labs (ESL)	759.07	17.04
19	Englehardt	674.6	38.03

*1000 ohms/square, ink.

13 Initial tests were conducted in this manner. It was subsequently found that a single continuous cut on a given resistor was preferable to a step-wise cut. This resulted from inability to consistently overlap on adjacent cuts; also, start-end points had wider areas removed than other points.

Once cut, the sample resistors were baked at 150°C for a minimum of 48 hours to check stability.

Conclusions reached from these tests may be summarized as follows:

- Inks from all manufacturers produced stable resistors. The Englehardt material tended to show the "silk-screen" pattern in the resistor area (i.e., the ink did not spread uniformly and an image of the silk screen could be plainly seen)[14].

  The Cermalloy and ESL inked resistors were comparable, however, more data was accumulated using the Cermalloy resistors than ESL. Plans were being made to utilize Cermalloy ink on this basis only.

- Resistance shifts of less than 0.2 percent were experienced after the temperature bake described above. This small variation was also noted in selected control samples which were not laser cut, implying that material cracking was not the cause of the variations in resistance.

- Resistance cutting occurred for the laser-energy conditions summarized below:

  - Pump-Lamp Current - 18 amps dc.
  - Overlap - 75 percent.
  - Trim Rate - about 0.3 inch/second. These cutting conditions were not optimized for maximum cutting speed at this time.

Ink-manufacturer personnel indicated that a cut depth of 30 to 40 percent should not be exceeded to minimize the risk of crack migration from the laser cut to the edges of the resistors. It was also suggested that a minimum of 0.020 inch between cuts and/or edges should be maintained for the same reason.

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14 It is not known whether this was the result of the pre-fired ink viscosity or some problem in the manufacturing process.

2.3.1.5 Initial Laser-Cutting Scheme. - The initial programming concepts for laser cutting of thick-film resistors assumed that an accurate universal percentage cut depth versus (R_{9F}/R_{9I}) curve existed[15] for simple-aspect-ratio thick-film resistors. An example of these assumed curves are shown in figures 8a, 8b and 8c. The figures plot the ratio of final-to-initial resistance value versus percentage cut depth. Figure 8a shows a typical primary cut curve in 10 percent steps. Figure 8b shows a family of shadow cuts assuming 30, 40 or 50 percent primary cut depths. When pre-cut functional measurements are made and HOB is calculated, a new amplifier ac gain can be determined to obtain the desired HOB. From this gain, the final R_9 resistance value can be found and the desired ratio (R_{9F}/R_{9I}) calculated. Entering these curves would provide the needed cut-depth information which, in turn, can be translated into laser-cutting information to produce the desired value of R_9. It was initially planned that these curves would be placed in computer memory for use in real-time along with appropriate subroutines and logic for interpolation between primary points. (In the example shown in figure 8b, R_{9F}/R_{9I}=D corresponds to a 50 percent primary cut depth and a 45 percent shadow cut.) From this, the actual cut depth in inches can be found and laser-coordinate information derived.

The principal problem with this approach is that a set of universal curves do not exist with the accuracy needed for the program. Additional difficulties adding to inaccuracy are:

- The non-trimmed value of R_{9I} ohms is not known to any better than $\pm$ 10 percent or more from unit to unit.
- The loading effect on R_9 of the coupling capacitor and rectifier input impedance (C_{11} and R', respectively - see

15 R_{9F} - Post laser-cut resistance value.
R_{9I} - Initial thick-film resistance value.

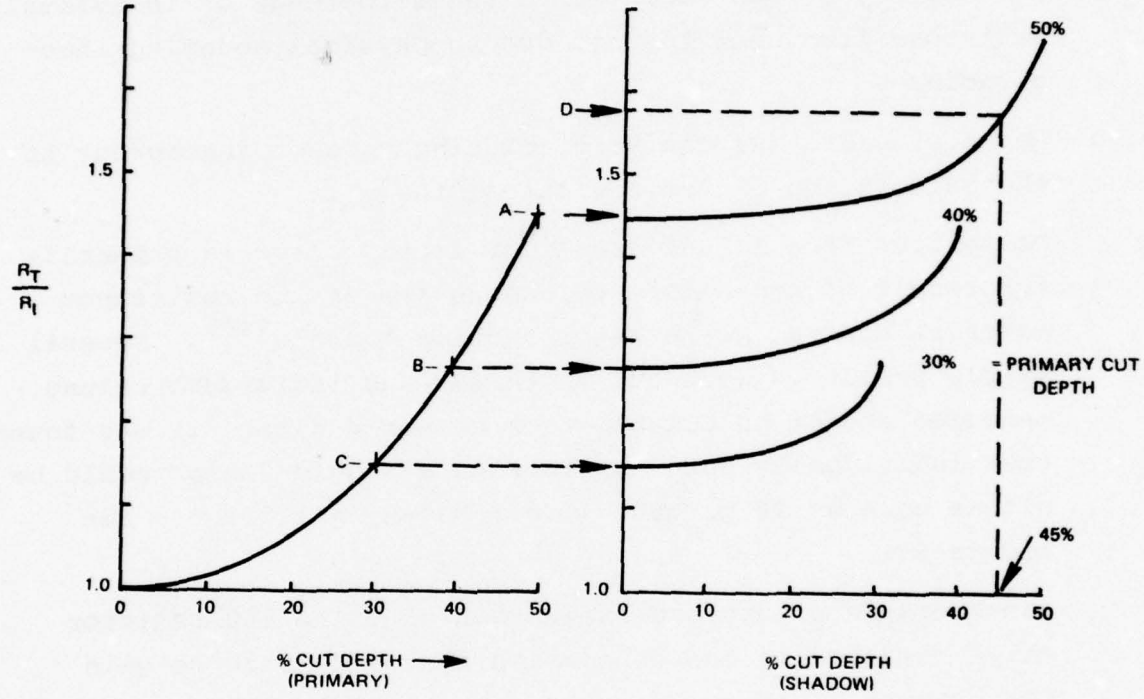


Figure 8a. RGF/RGI for a Typical Primary Cut

Figure 8b. RGF/RGI for a Typical Shadow Cut

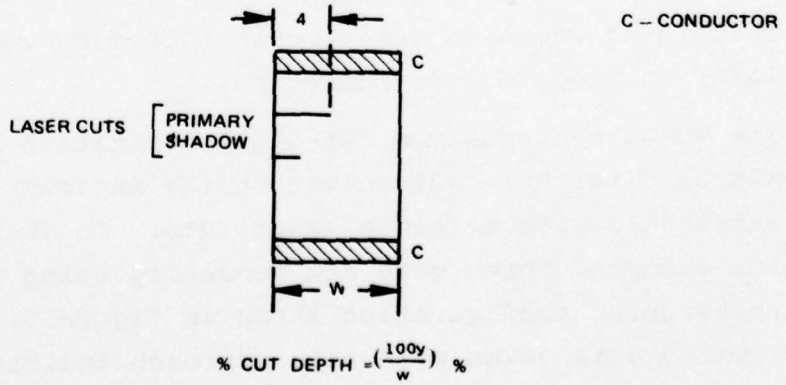


Figure 8c. Thick-Film Resistor Nomenclature

figure 2). Although nominal values of these components are known, variations from unit to unit can be substantial. (For example, C_{11} accuracy is $\pm$ 20 percent; R' is $\pm$ 25 percent.)

- The ability of the computer to sense the edge of individual resistors from unit to unit due to physical mounting inaccuracies.
- Resistor width (w) can vary, causing another inaccuracy in the calculation of desired cut depth (y).

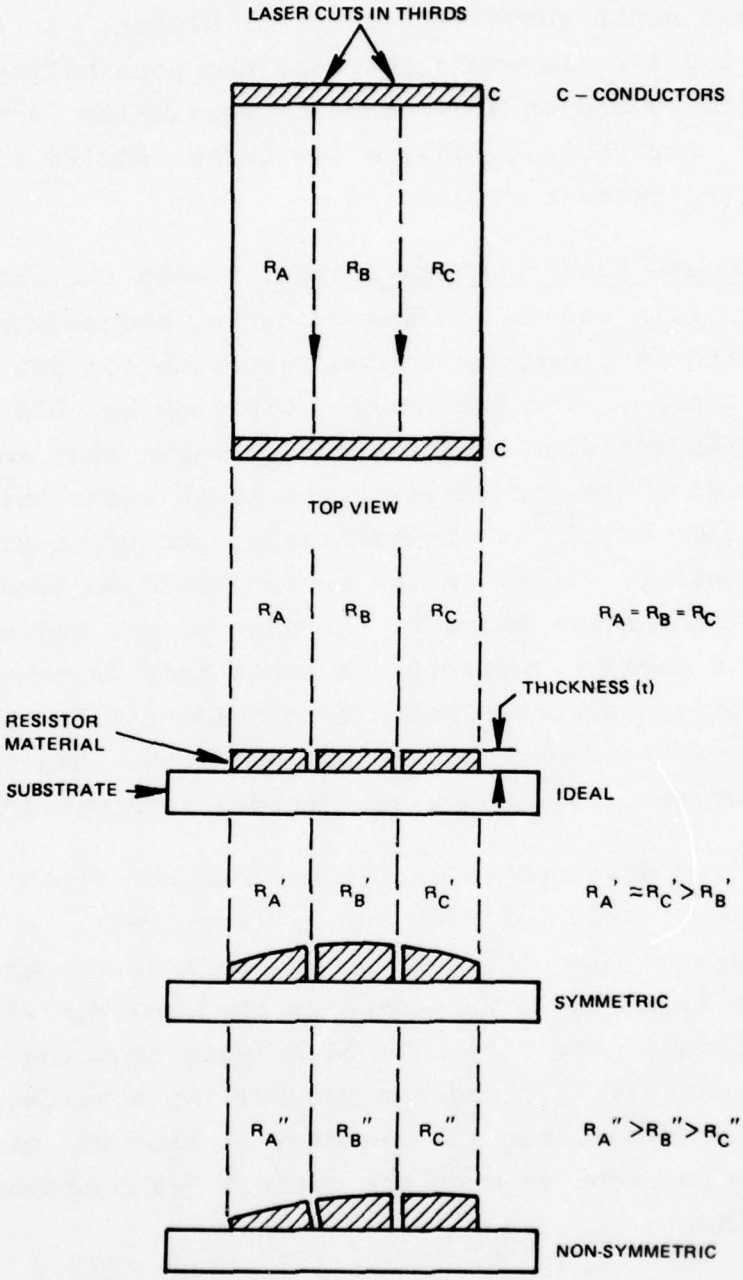
Deviations from a "universal cut depth" curve is primarily the result of nonuniform thickness (t) of the resistance material across the resistor cutting surface[16]. Several sample resistors were cut in thirds and individual values measured and/or calculated from measured data. It was found that individually cut resistors on a single "chip" could be off as much as 20 percent (i.e., $Ra' \simeq R_C' \simeq 1.2\ R_B'$ - see figure 8d).

Considerable effort and evaluation of 75 to 100 resistor chips resulted in the conclusion that a dynamic ac gain measurement (post-cut V5/V1-figure 2) would have to be made in real-time instead of using the percentage cut depth curve approach originally envisioned.

Once the measured ac voltage (V_5/V_1) equalled the desired calculated value, a laser-inhibit command was sent to the laser to stop it from radiating.

The 40-percent-maximum cut-depth limitation suggested above places a further restriction on the maximum (R_{9F}/R_{9I}) ratio attainable with multiple laser cuts. To attain a 1.9 ratio, for example, three cuts are mandatory using the simple rectangular configuration shown in figure 7. In fact, the limited data taken with this approach indicated that the

16 Nominal t=0.0005 inch.



NON-UNIFORMITY IS CAUSED BY RESISTANCE MATERIAL THICKNESS VARATIONS WITH POSITION.

Figure 8d. Thick-Film Resistor Irregularity

UUT's requiring very-high-value R_9's probably require a primary cut depth above 40 percent or higher. In short, obtaining a 1.9:1 ratio would increase the possibility of resistor instability and/or a decrease in resolution in these extreme cases. Fortunately, only a few UUT's require this value of R_9 in the present program.

2.3.1.6 Revised Laser-Cutting Scheme. - With the above in mind, the R_9 thick-film design and laser-cutting scheme shown in figure 7 was selected as a compromise configuration for use on the ECOM production boards. The two small (.010 inch by .020 inch) pads above the main resistor are orientation marks that enable the "system operator" to "initialize" the laser cross hairs manually to the resistor edge[17]. Specifically, the upper right mark (above the one) as viewed in the sketch would be used to manually preset the laser cross hairs to the edge of the resistor (just below the one mark). The vertical cross hair is centered on the mark; the horizontal cross hair is coincident with the resistor edge. The left hand mark has no purpose other than to assure the operator that the last shadow cut (three) is properly oriented[18].

The program was designed so that a maximum cut depth of 40 percent[19] will be made for each cut (if required). A separate analog-comparator circuit looks at the peak ac voltage at V_5 while the laser is trimming R_9 and compares that voltage with a computer reference voltage (see figure 1) calculated from the desired post-cut ac gain (V_5/V_1) and a given UUT input voltage. When these values are identical, the laser energy is shut off even though the laser servos continue to move the optical X-Y coordinate to the maximum cut depth.

17 A production trimmer would automatically seek this edge.
18 Cut three should be in line with this mark.
19 This may be increased to 45-50 percent for high-value resistors.

If the measured peak ac voltage is 95 percent or less than the final desired value when cut (one) is completed, the laser immediately goes to point (two) and repeats the process along cut (two). When 95 percent of the final value is reached, ac gain (V_5/V_1) is remeasured and compared to the calculated gain for the desired HOB. The remaining 5 percent change is then begun either as a continuation of cut (two) or begun at cut (three) depending upon the overall gain resolution desired[20].

Once the final cut is made, ac gain is measured again and a final HOB is calculated. This is the value used as a post-trim HOB. The use of this alternate approach eliminates the accuracy problems described in previous paragraphs. The technique relies on UUT ac gain and gain changes. Since HOB is directly proportional to first-stage ac gain, a desired change in UUT HOB can be related directly to changes in this gain.

This is not true for R_9 resistance changes since the rectifier-coupling capacitor (C_{11}) and input impedance (R') load R_9, making the problem considerably more difficult to resolve[21].

2.3.1.7 Alternate Resistor Design. - The thick-film resistor design and cutting procedure described in the previous paragraphs represents a first approximation toward providing an acceptable laser trimmable thick- film resistor for the present production boards. Stability is acceptable within specified cutting limits. Resolution, however, may or may not meet desired limits, depending upon the post-cut R_9 resistance value needed. Because the

---

20 A gain resolution of less than 0.1 percent is necessary if the overall 0.5 percent design goal requirement is to be met. The cut schedule proposed above straddles this resolution with high percentage cut depths yielding insufficient resolution and low percentage cut depths exceeding our needs. Additional development effort in this area should provide adequate resolution for all UUT's.

21 Not that the problem cannot be solved. The main difficulty here is that the actual values of C_{11}, R' and R_9, R_{11} would also have to be measured.

present UUT production lot nominal R_9 value is 1950 ohms (1400 to 2700 ohms), the laser cutting resolution is adequate[22]. If 2700 ohms is required, the resolution per stage count is inadequate because cut depths are greater and the slope of R_{9F}/R_{9I} versus the cut-depth percentage is steeper. Utilizing a second vernier shadow cut (cut three in figure 7) for the last 5 percent in gain shift should reduce the potential resolution problem to acceptable limits.

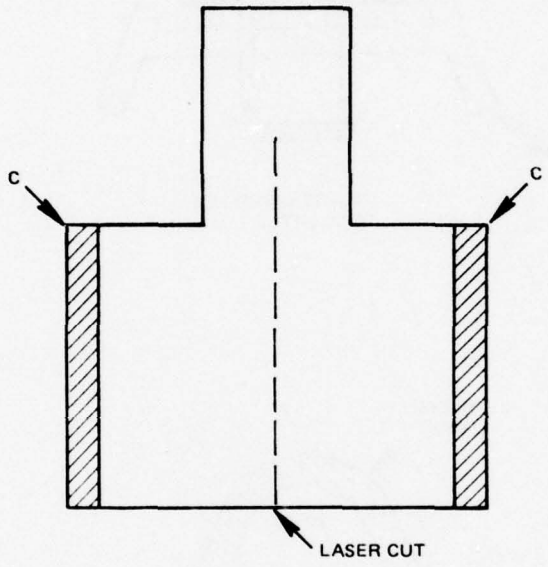
Statistical data on R_9 spread accumulated on several tens of thousands of M732 production amplifiers indicates a much broader range of resistance values is needed in high-volume situations. Providing this added range, while maintaining acceptable resolution, forces a redesign of the thick-film R_9 shown in figure 7. One possibility is shown in figure 9. It represents a configuration which could provide a range of about 4:1 or better, depending upon specific design. No plans were made to pursue these alternatives during this program.

2.3.2 Oscillator Assemblies

Figures 10a and 10b show simplified cross-sectional views of the present production M732 oscillator assembly. The fuze consists of a combined antenna/oscillator, a bypass capacitor circuit board, and a metal mounting body which holds the entire assembly. The M732 amplifier (not shown) is mounted to the underside of this body, and this assembly has leads connecting the amplifier and oscillator. These leads provide oscillator supply voltage (B+, V_{base} and Gnd) and connect the detector output voltage to the M732 amplifier board.

---

22 A laser stage shift of one count corresponds to a physical shift of 0.000488 inch representing 0.856 percent cut depth per count for a 1400-ohm resistor. This amounts to about 4.6 ohms for an R_9 value of 1950 ohms (0.24 percent change in R9). This typical resolution is that for a 43 percent by 5 percent principal and one shadow cut using the approximate data of figure 8b. The cutting procedure shown in figure 7 provides considerably better resolution (less than 0.1 percent/count).

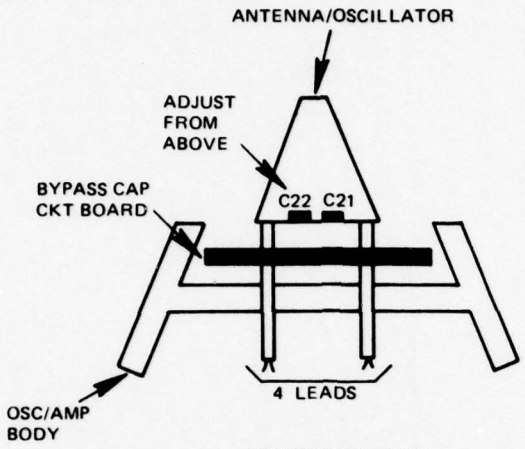


C = CONDUCTOR

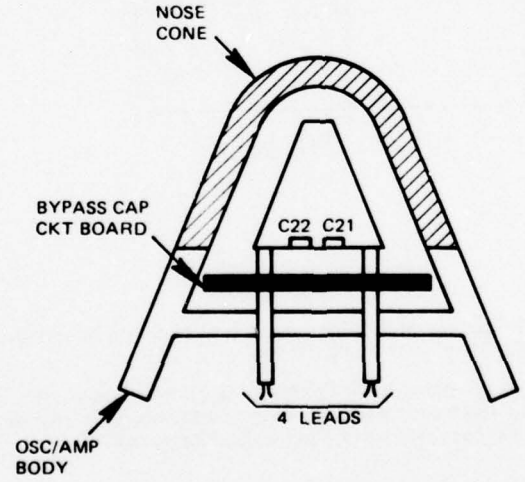
NOTES: 1) WHERE RELATIVE DIMENSIONS WOULD DETERMINE RESISTANCE CUTTING RANGE AND RESOLUTIONS.

2) A SECOND IMAGE RESISTOR CAN BE ADDED TO DOUBLE THE OVERALL RESISTANCE RANGE. THIS RESISTOR IS ELECTRICALLY CONNECTED IN SERIES WITH THE ABOVE RESISTOR.

Figure 9. Alternate Thick-Film Resistor Design



ADJUST UNPOTTED
OSCILLATOR



ADD NOSE CONE/POT AND
RETEST

Figure 10. Unmodified Oscillator Cross Section

The M732 antenna is an integral part of the oscillator tank circuitry. Shunt and series tank capacitances are supplemented by extra pads (C_{21} and C_{22}) for incremental adjustment of transistor/antenna load matching and receiver sensitivity. These capacitors are located on the upper side of the bottom portion of the antenna circuit board triangle as shown in this figure.

Bypass capacitors and series chokes (not shown) feed power to the oscillator and extract the detected M-wave. These bypass capacitors are located on an additional low-loss circuit board under the oscillator. The bottom plate of the board is copper clad with holes at appropriate points to feed through power and detector voltage. Distributed constant upper plates on this board serve as capacitors, assuring proper rf bypass at each feedthrough point.

Oscillator-sensitivity adjustments are made in a calibrated load chamber that simulates free space. Sensitivities of the prepotted units are set within a range of values such that after potting they fall within specification limits. This is accomplished by decreasing the value of either C_{21} or C_{22}, depending upon whether an increase or decrease in unit sensitivity is desired.

A nose cone is then attached to the oscillator assembly and the unit potted. Potted oscillator sensitivity should fall within required specification limits.

2.3.2.1 Assembly Modifications. - Adapting the M732 oscillator to a dynamic-tester and laser-trimming facility was much more of a problem than it was for amplifier assemblies. Minimizing program cost dictated use of unpotted oscillators instead of the potted version to eliminate the need for body assembly, nose cone and potting materials.

It was felt that a tester-feasibility demonstration could be accomplished with the unpotted antenna assembly just as easily

as with the potted version[23]. It should be pointed out, however, that a real production facility should deal with the potted assembly because the body, nose cone and potting material effect all the rf properties of the UUT.

The above approach is possible because a potted assembly could be modified to be similar to the unpotted design as long as the laser-trimmable capacitors remain accessible from the "body" side of the unit. In this technique, the unpotted oscillator is first functionally tested, potted (with the access hole kept free of potting material), and then trimmed after potting[24].

Figure 11 shows a simple cross-sectional view of the modified oscillator assembly along with a listing of the measured parameters needed for successful sensitivity adjustment.

The major original-design components requiring modification are:

- Antenna/Oscillator Circuit Board.
- Bypass Capacitor Circuit Board.

The antenna oscillator circuit board includes the principal sensitivity adjustment capacitors, C_{21} and C_{22}, originally located as shown in figure 10a or 10b.

Laser trimming these capacitors dictated that they be placed on the opposite side of the board and that they be on a substrate that will not be effected by laser energy. The circuit pattern on the bottom side of this board was redesigned to accomodate ceramic chip that holds the multi-element thick-film capacitors.

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23 As long as the test samples are handled carefully.

24 A much simpler approach would be to mate untuned (functionally tested) original-design oscillators to amplifier boards and adjust R_9 to compensate for variations in amplifier and oscillator parameters as a combination. The range of R_9 must be broadened somewhat, but not to the extent that would make the alternate approach unfeasible. The "top hat" resistor-design concept of figure 9 would provide the necessary R_9 range.

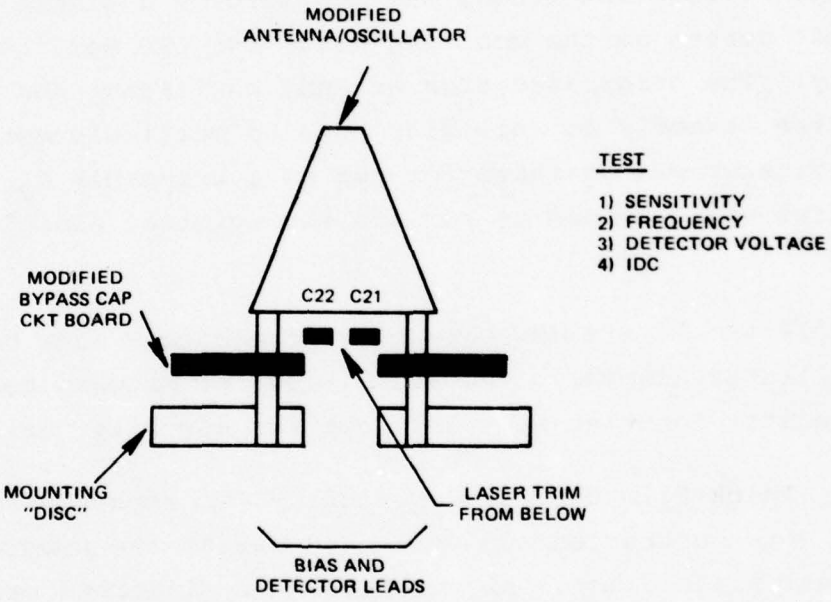

Figure 11. Modified Oscillator Cross Section

The UUT detector diode was relocated to allow room for the new design. Overall tuning capacitance values were maintained at or near their original values to minimize deviations from original-design-oscillator electrical properties.

The bypass-capacitor circuit board (oscillator PC Board) also was redesigned to add a hole for laser trimming. This redesign required rearranging of the location of the bypass-capacitor upper plates to allow space for this access hole.

The original oscillator body was replaced by a simple aluminum disc that serves as the mounting plate for the modified oscillator assembly. The original-design antenna positioner and studs hold the entire assembly to this disc[25]. A multi-element ceramic-chip capacitor was designed for use as a trimmable C_{21} and C_{22}, and a disc was designed to replace the original oscillator/antenna body.

Figures 12 and 13 are photographs of the bottom view of the overall oscillator assembly. Detailed views of antenna modifications and capacitor mounting were left out for security reasons.

2.3.2.2 Thick-Film Capacitor Design. - Two separate capacitance designs were contructed and evaluated during the program where individual plate dimensions were based on different criteria of fringing capacitance. Figure 14 shows an enlarged version of the artwork for the prototype design based on an experimental estimate of fringing capacity. The other design, based on a theoretical fringing criteria, looks similar except for slightly different pad dimensions for each "bit". The experimental fringing design was to be used in the ECOM production units.

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25 See figure 1 of the Third Quarterly Report, "Production Measurement of Fuze Components Under Dynamic Stress", 11 November 1976 to 10 February 1976, Contract No. DAAB07-76-C-0032, for a complete family tree of the modified oscillator assembly.

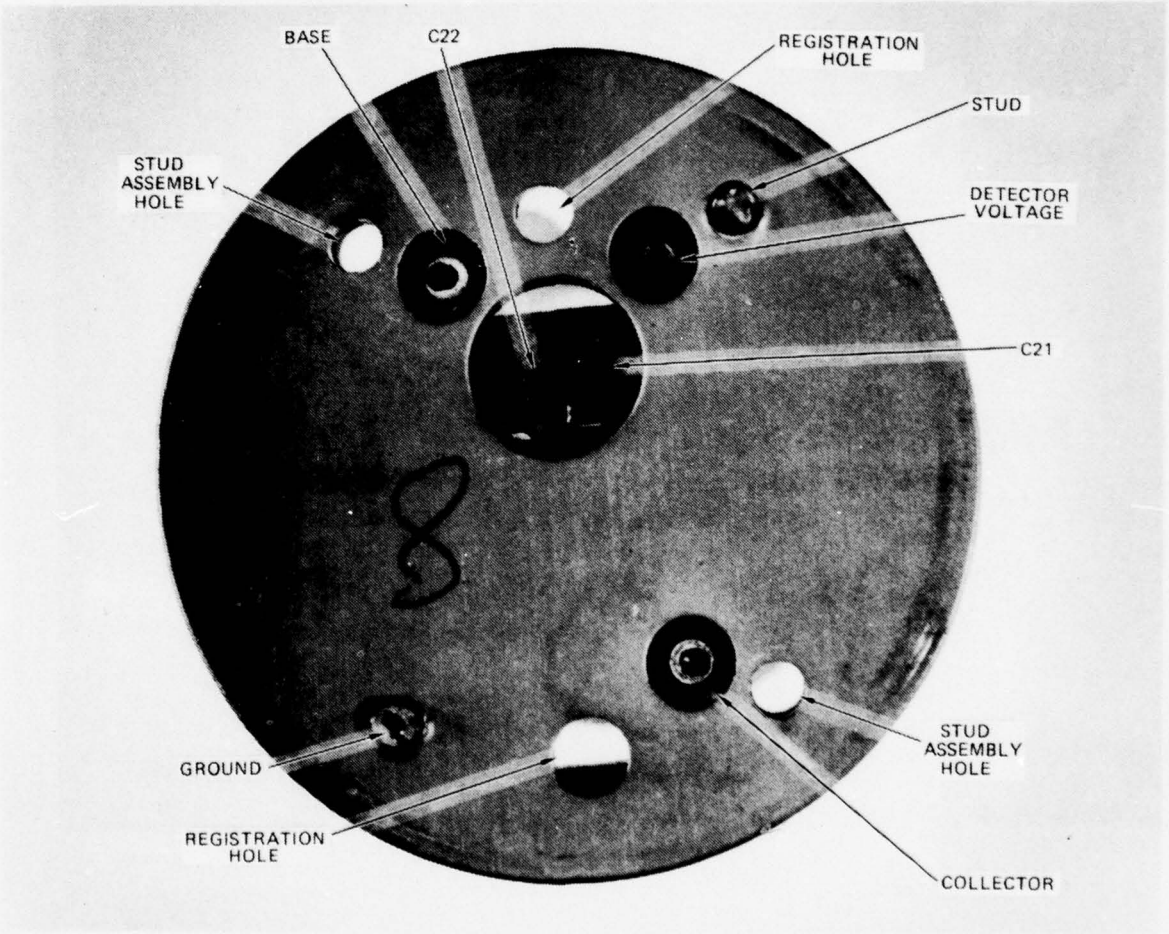


Figure 12. Bottom View of Oscillator Assembly

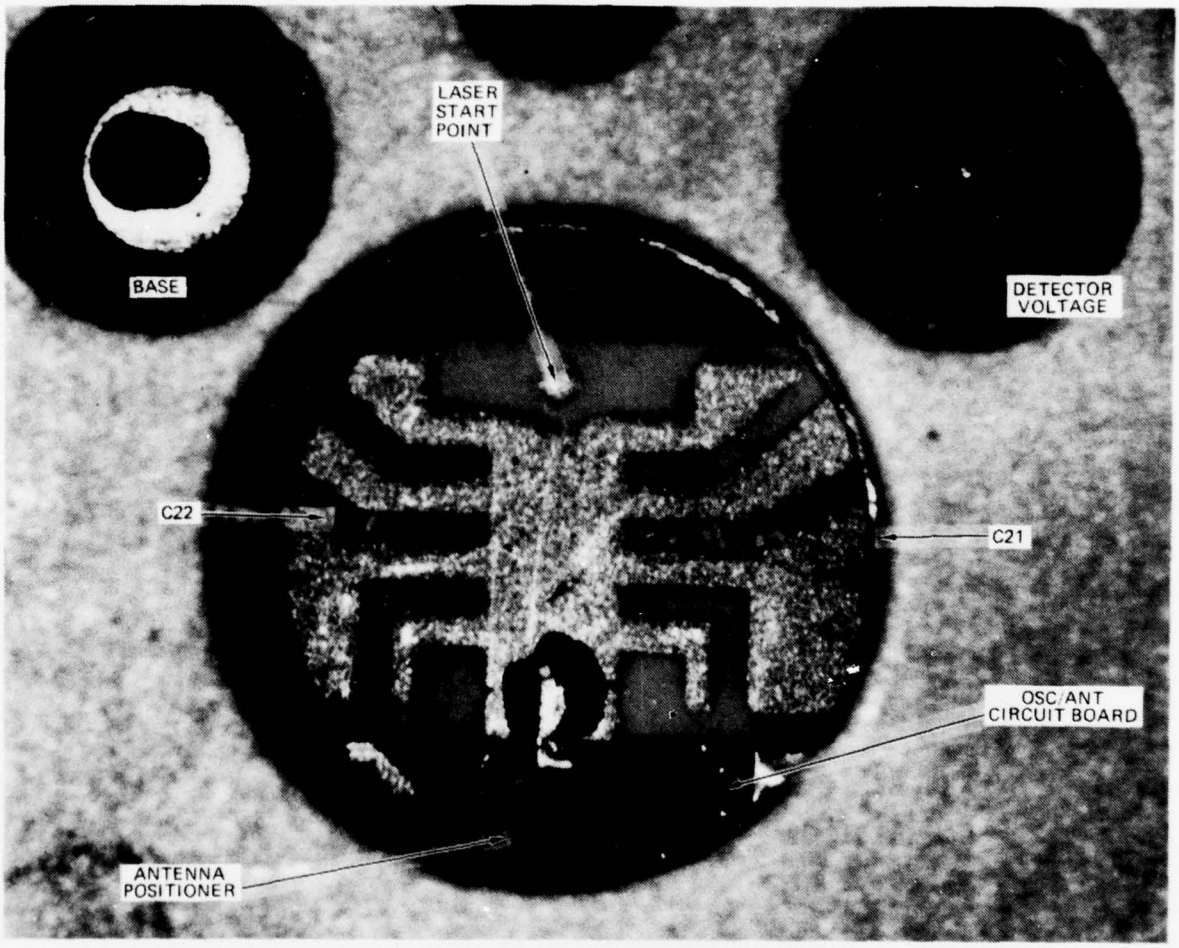
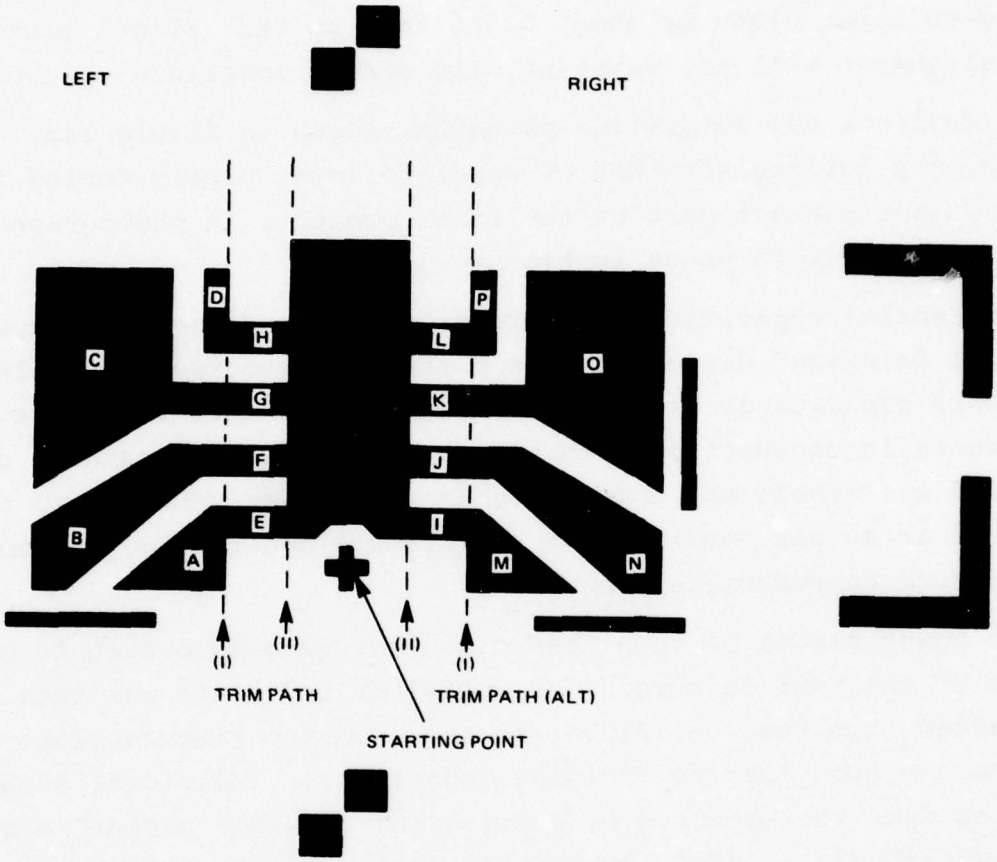
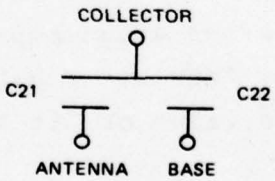


Figure 13. Laser View of Oscillator Chip Capacitor



UPPER PLATE ARTWORK



C21 = SERIES CAPACITOR

C22 = PARALLEL CAPACITOR

ELECTRICAL SCHEMATIC

Figure 14. Trimmable Capacitor Pattern (Binary Ratio)

Figure 14a shows the upper plate pattern of this design. The lower plates are located under plates (A+B+C+D) and (M+N+O+P), respectively. Figure 14b shows the electrical schematic. The lower plates are continuous and extend beyond the outside perimeter of each upper plate by about 0.015 inch so that slight pattern misalignment will not substantially effect individual bit capacity.

The dual-box and outer-line patterns, shown in figure 14a, are used only for registration of upper-to-lower plates during fabrication and are not part of the final product. A photograph of a prototype unit is shown in figure 15.

Differential capacitance measurements were made on six "experimental fringing" design samples during the program. A Hewlett-Packard capacitance bridge (Model 4270A) was used for these measurements in conjunction with a test fixture whose residual capacitance was stable and accurately known. Measurements were conducted in an air conditioned, temperature controlled, environment to assure reproducible results.

Both lower plates of each test capacitor were connected to one side of the test fixture. The capacitor top plate was then attached from its central bar to the opposite fixture plate using a short ribbon lead to minimize inductance. Individual capacitor plates were then removed by cutting the linking "street" along "trim path (I) - left", "trim path (II) - left", "trim path (alt) (I) - right" and "trim path (alt) (II) - right", respectively (as shown in figure 14a). This was done, one element at a time, so that readings before and after a cut represented the capacitance bit removed (i.e., cutting "street" E along trim path (I) - left determines the capacitance value of bit A by subtracting pre-cut and post-cut readings.

The results of these experiments are summarized in table II.

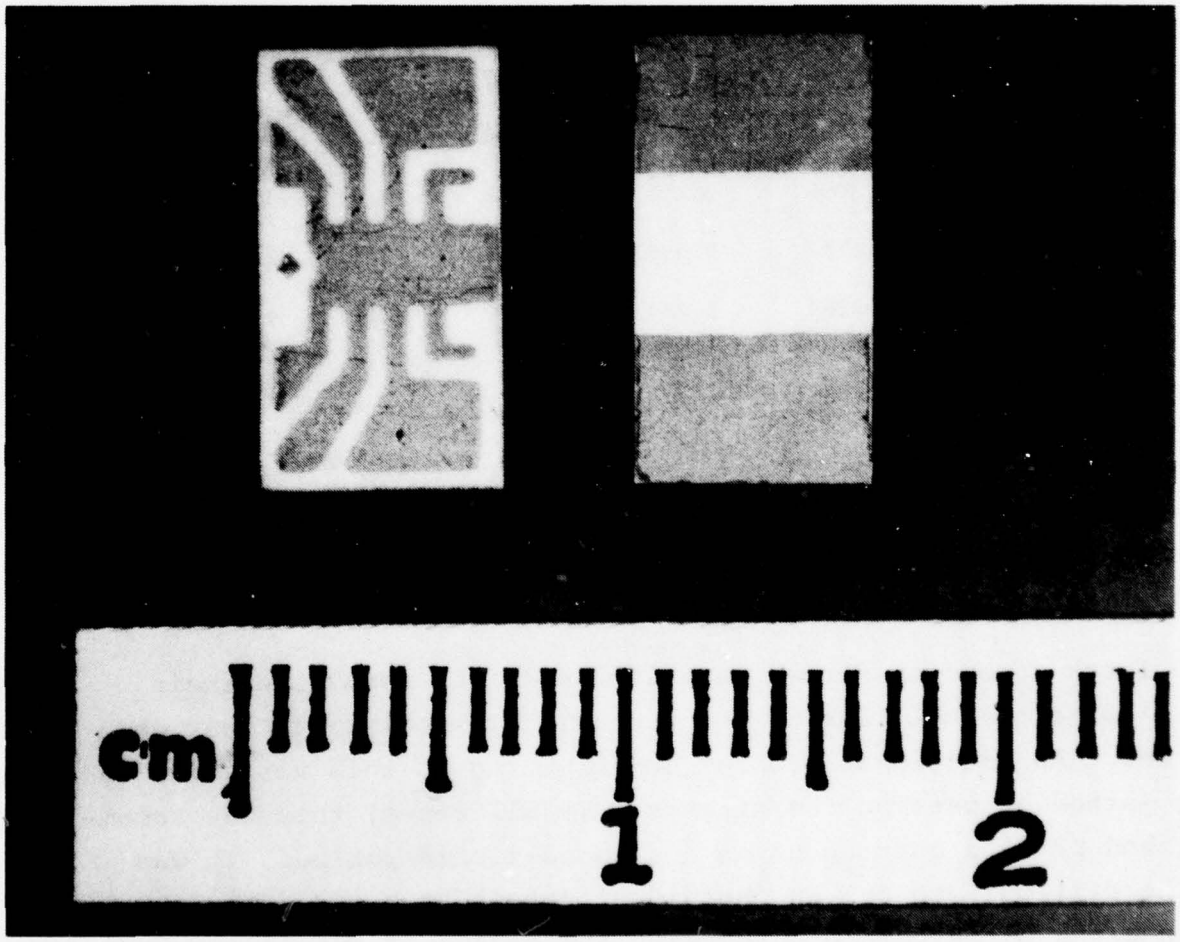


Figure 15. Laser-Trimmable Capacitor

Table II. Test Results of "Experimental-Fringing" Chip-Capacitor Design*

Side	Capacitor Designation	Desired Value (pF)	Average Measured Value (pF)	% Error of Mean	Limits - % Error		
					Maximum	Minimum	Total Spread
Left	D	0.1533	0.151	-1.50	+16.1	-10.0	26.1
	A	0.3066	0.258	-15.85	-10.0	-22.4	12.4
	B	0.6132	0.598	-2.48	+1.8	-9.0	10.8
	C	1.2264	1.280	+4.37	+7.7	-1.3	9
Right	P	0.1533	0.138	-9.98	+3.4	-22.4	27.8
	M	0.3066	0.253	-17.48	-19.8	-14.9	4.9
	N	0.6132	0.598	-2.48	+2.7	-10	12.7
	O	1.2264	1.284	+4.70	+7.0	+1.8	5.2

*Based on a sample of six units.

The average street capacitance was measured to be 0.056 pF with a standard deviation of 0.019 pF. The residual capacity of the upper plate central bar to each lower plate was 0.630 pF, including streets.

The large spread in street capacitance is the result of their small size and the lack of a bottom plate immediately under each street. An additional problem contributing to this variation is the method of cutting the streets. In all cases, this was accomplished by hand cutting using a diamond-tipped scribe. It was quite difficult to cut an individual street at a specific location along either "trim path" with any degree of consistency. This probably contributes to the comparatively large variations in the small bit capacitors (D and P).

The results summarized in table II indicate that the basic chip-capacitor design is not far from the desired values (except possibly capacitors A and M). In fact, minor changes in pad sizes

(including A and M) will shift their mean capacities to the desired values without major modification to pad sizes. This change was being accomplished when it was decided to concentrate on the amplifier-board development. Although several prototype samples were fabricated, this final design was never completed.

2.3.2.3 Chip-Capacitor Resolution. - The design goal of this program was to test and trim oscillator assemblies to a specified value ±0.5 percent. The present M732 oscillator design has a sensitivity capacity slope that is in the range of 0.024 pF/mVrms on the average. This implies a maximum least significant bit (LSB) of 0.012 pF, about an order of magnitude lower than the design LSB. To obtain this resolution, a second and possibly a third cut will be necessary that are continuous area cuts that provide the needed infinite resolution.

Program plans were to provide a stepwise cut on first tuning using the binary capacitors. The second and third trials would be continuous. If convergence is assumed, the second and third trials should have smaller differential capacitance changes that allow for removal of smaller portions of a remaining pad or street.

2.3.2.4 Prototype Oscillators. - The prototype design of the overall ECOM oscillator assembly was completed and several units assembled and tested. Figures 12 and 13 show a bottom view of one of these units in which the laser trimming "hole", the chip capacitor and the electrical connections to the load-chamber fixture can be seen.

The prototype units tested still required some minor antenna-pattern modifications to be incorporated when this portion of the program was curtailed.

The rf modulator design and interface circuitry had already been completed at this point. (See paragraph 2.4 for a more detailed description of the tester hardware effort.)

2.4 TESTER HARDWARE DESIGN

Figure 1 shows a functional sketch of the automatic test and trim system designed during the program. Figure 16 is a detailed interconnection diagram of the same system showing the "computer", "auxiliary equipment rack" and "laser trimmer bench" along with major buffer interface cards used for amplifier or oscillator trimming. (See figures 1b, c and d for photographs of individual blocks.) The dotted blocks in figure 16 indicate that these blocks were designed and parts purchased (excluding the probe), but were not assembled or checked electrically at contract closure. Load-chamber and oscillator-test fixtures, however, were completed. The load-chamber test probe was replaced by a spinning dipole in lieu of the rf pickup-probe design. Prototype oscillators were tested in this chamber using a modified test approach[26]. This dipole assembly is mounted on a removable aluminum plate which can be readily replaced by the final design rf test probe.

The "auxiliary equipment rack", "amplifier electronics assembly", "rf modulator and power" and "load chamber" blocks are the designs interfacing the HP computer and quantrad laser to the UUT's. The laser "manual control box" chassis (joystick) was also modified to add "pass/fail" and "voltage out of tolerance" lights plus an override switch that allows the operator to use the laser positioning "joystick" exclusive of the computer (see figure 20).

2.4.1 Major Blocks

2.4.1.1 Hewlett-Packard Computer Equipment. - Figure 17 shows a block diagram of the major components comprising the Hewlett-Packard Computer. The letters in the lower right corners of each

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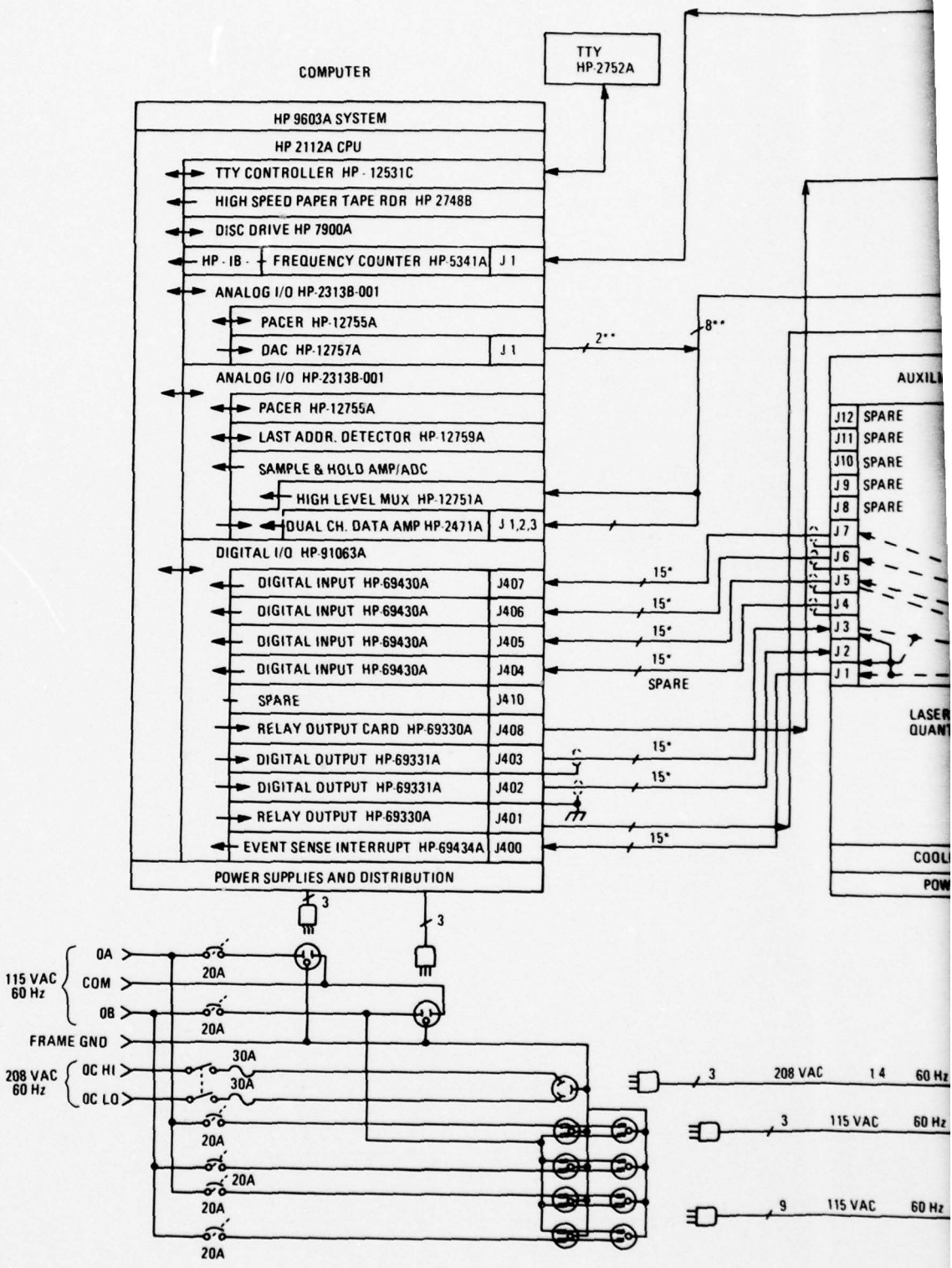
26 Actually, this approach is a standard measuring technique used with M732 oscillators.


COMPUTER
TTY
HP-2752A
HP 9603A SYSTEM
HP 2112A CPU
TTY CONTROLLER HP - 12531C
HIGH SPEED PAPER TAPE RDR HP 2748B
DISC DRIVE HP 7900A
HP - IB -
FREQUENCY COUNTER HP-5341A
J 1
ANALOG I/O HP-2313B-001
PACER HP-12755A
DAC HP-12757A
J 1
2**
8**
ANALOG I/O HP-2313B-001
PACER HP-12755A
LAST ADDR. DETECTOR HP-12759A
SAMPLE & HOLD AMP/ADC
HIGH LEVEL MUX HP-12751A
DUAL CH. DATA AMP HP-2471A
J 1,2,3
DIGITAL I/O HP-91063A
DIGITAL INPUT HP-69430A
J407
DIGITAL INPUT HP-69430A
J406
DIGITAL INPUT HP-69430A
J405
DIGITAL INPUT HP-69430A
J404
SPARE
J410
RELAY OUTPUT CARD HP-69330A
J408
DIGITAL OUTPUT HP-69331A
J403
DIGITAL OUTPUT HP-69331A
J402
RELAY OUTPUT HP-69330A
J401
EVENT SENSE INTERRUPT HP-69434A
J400
15*
SPARE
POWER SUPPLIES AND DISTRIBUTION
AUXILI
J12 SPARE
J11 SPARE
J10 SPARE
J9 SPARE
J8 SPARE
J7
J6
J5
J4
J3
J2
J1
LASER
QUANT
COOLI
POW
3
115 VAC
60 Hz
0A
COM
0B
FRAME GND
208 VAC
60 Hz
OC HI
OC LO
20A
30A
208 VAC
1 4
60 Hz
115 VAC
60 Hz
9

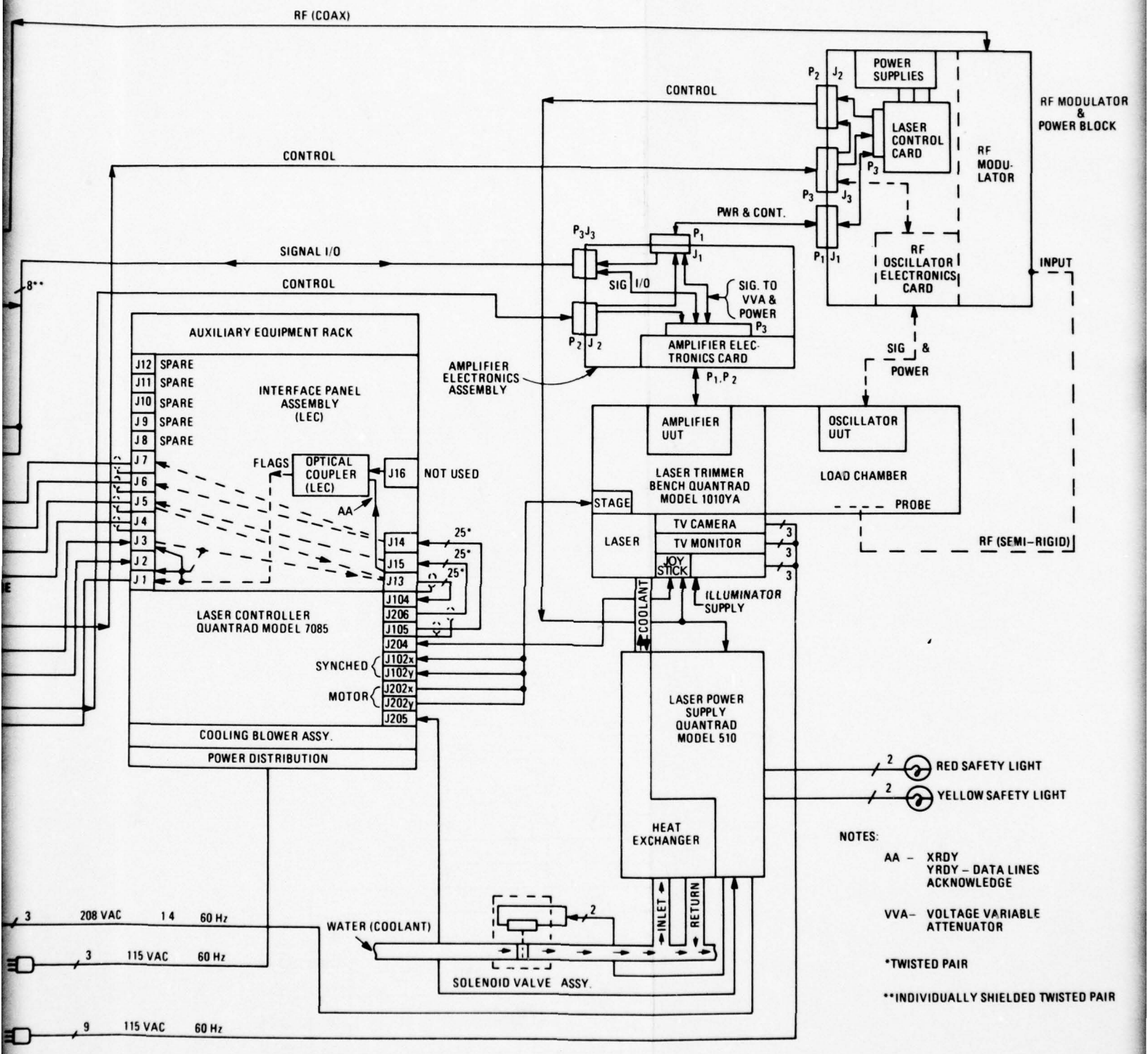


Figure 16. ECOM Test Station

2

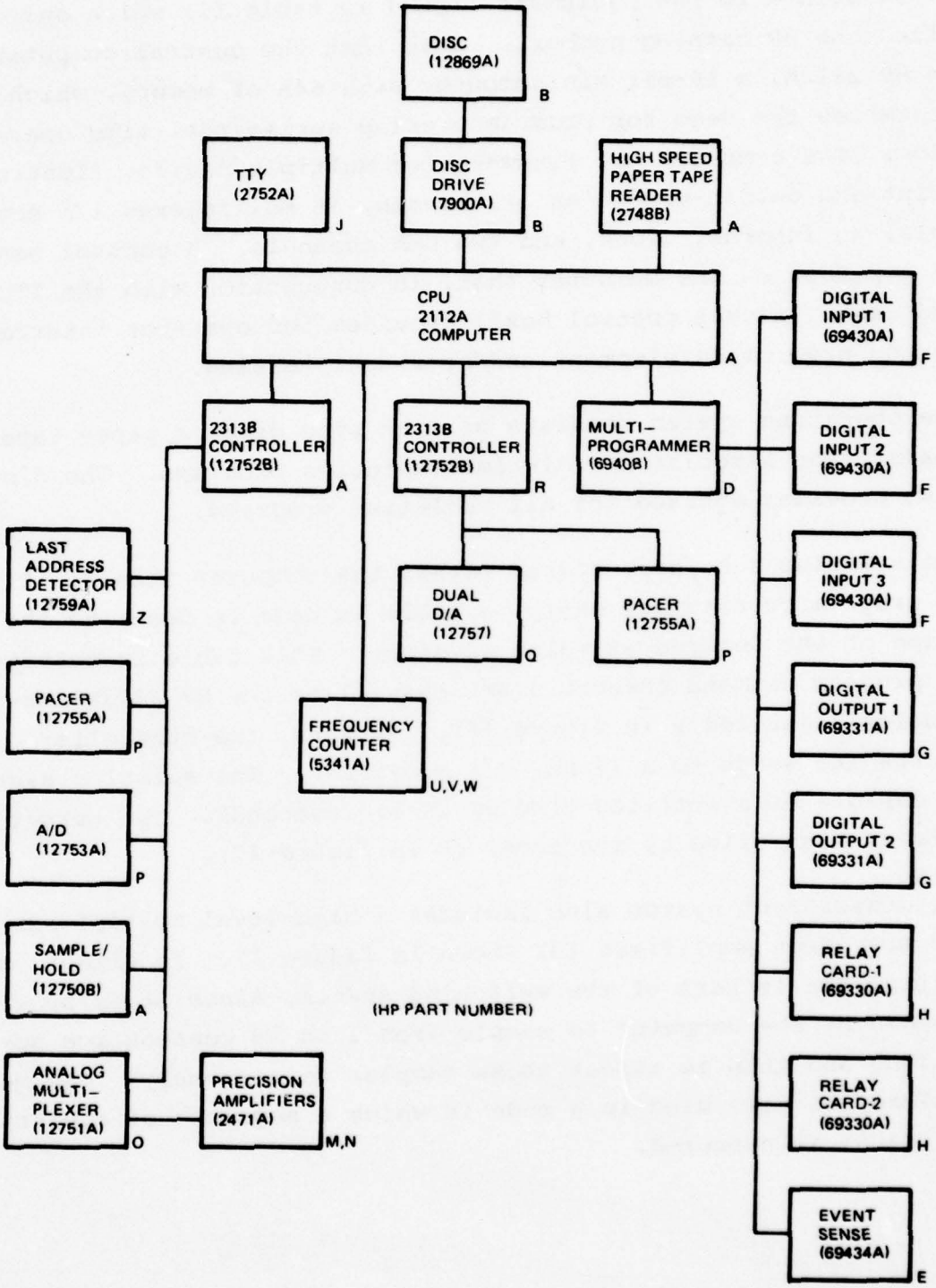


Figure 17. Computer and Computer Peripherals

block relate to the equipment listed in table III which summarizes the HP catalog numbers. Note that the central computer is an HP 2112A, a 16-bit minicomputer with 64K of memory, which minimizes the need for program overlap during real-time operation. The computer has firmware for multiply/divide, floating-point and double-precision arithmetic, 16 multiplexed i/o channels, an internal clock, and two DMA channels. A control panel is provided on the computer that, in conjunction with the TTY and laser "manual control box", provides for operator interface during program development and/or actual testing.

The operating system consists of 4.9M byte disk, a paper tape loader, and associated real-time executive programs. The disk also provides storage for all real-time programs.

The stimulus subsystem starts within the computer itself. Either by program or external entry, a table is made to describe the shape of the desired stimulus waveform. This table is outputted by program command through a DMA channel to the HP 2313B Controller (labelled R in figure 17). In turn, the controller routes the words to a 12-bit d/a converter. The stimulus system is capable of a settling time of 20 microseconds. The output rate is controlled by the pacer (P in figure 17).

The measurement system also includes a high-level multiplexer (O) and precision amplifiers (M) shown in figure 17. In effect, the multiplexer is part of the switching system, since it is programmed by the computer to sample from 1 to 16 consecutive positions and then to repeat these samples continuously. The multiplexer is also used in a mode in which a sequence of arbitrary positions is executed.

Table III. Major Hewlett-Packard Computer Components

Item	Quantity	Description
A	1	HP 9603A High-speed Measurement and Control System.
B	1	Option No. A03: RTE-III with 4.9M Byte Disc, Cabinet, Fortran IV, System Libraries.
C	1	Option No. Y13: Batch Spool Monitor.
D	1	Option No. T17: 6940A (91063A) Digital I/O Subsystem.
E	1	Option No. J17: Event Sense Interrupt.
F	3	Option No. J16: Isolated Digital Input, 12 Bits.
G	2	Option No. K04: TTL Output, 12 Bits.
H	1	Option No. K05: Relay Output Card.
I	1	Option No. P24: Replace 2108A with 2112A.
J	1	Option No. R00: Teleprinter and Local I/O, 10 cps.
K	1	Option No. 005: Additional I/O for 2313B.
L	1	Option No. 021: 10-Foot Differential Cable.
M	3	Option No. 025: 2471A Data Amplifier.
N	1	Option No. 026: Case for 2471A Cards.
O	1	Option No. 008: 16-Channel High-Level Multiplexer.
P	2	Option No. 011: Programmable Pacer (12755A).
Q	1	Option No. 013: D/A Dual 12-Bit Converter.
R	1	Option No. 558: Second 2313B-001 Integrated into 9603A.
S	1	Option No. P12: 16K Word Memory Expansion.
T	1	HP 59310B HP-IB Interface Card.
U	1	HP 5341A Frequency Counter to 4.5 GHz.
V	1	Option No. 002: Rear Panel Connectors.
W	1	Option No. 003: 1.5 GHz Frequency Range.
X	1	Option No. 011: I/O ASCII Interface.
Y	1	Option No. 908: Rack Flange Kit; HP Part No. 05326-60046.
Z	1	Last Address Detector.

The output of the analog multiplexer is fed to a sample and hold card and then to a a/d converter; from there, the DMA channel reads the words into the computer. A pacer (P) accurately times the transfer rate. The pacer rate is set by the computer.

The maximum data rate into the computer is 45,000 words per second for the specified accuracy of $\pm$0.09-percent full-scale, $\pm$1/2 LSB.

The Hewlett-Packard Multiprogrammer shown as unit D in figure 17 handles low-speed digital input/output. The output commands to the laser and the laser BITE words run through this multiplexer. The event sense interrupt is also controlled by this unit. This laser unit can be set to interrupt the computer, based on matching a bit reference word. Since there are 12 bits in the reference word, there are 2^{12} (or 4,096 independent events) that can interrupt the computer.

A relay card (Unit H) consisting of 12 single-pole, single-throw relays is also computer controlled through the multiprogrammer block. These relays, together with the analog multiplexer, form the computer-controlled interface to the laser and buffer circuitry. The frequency counter (Unit U) can read rf frequency up to 1.5GHz.

Except for the frequency counter, this system is essentially a low-frequency system. However, the frequency range can be extended to include rf and microwave test and trim by adding external buffering, rf synthesizers, and an rf spectrum analyzer. This approach is taken when testing oscillators.

Figures 18 and 19 are photographs of the HP 2313B Multiplexer a/d and d/a converters, respectively. The HP Multiprogrammer can be seen in figure 1b at the bottom right.

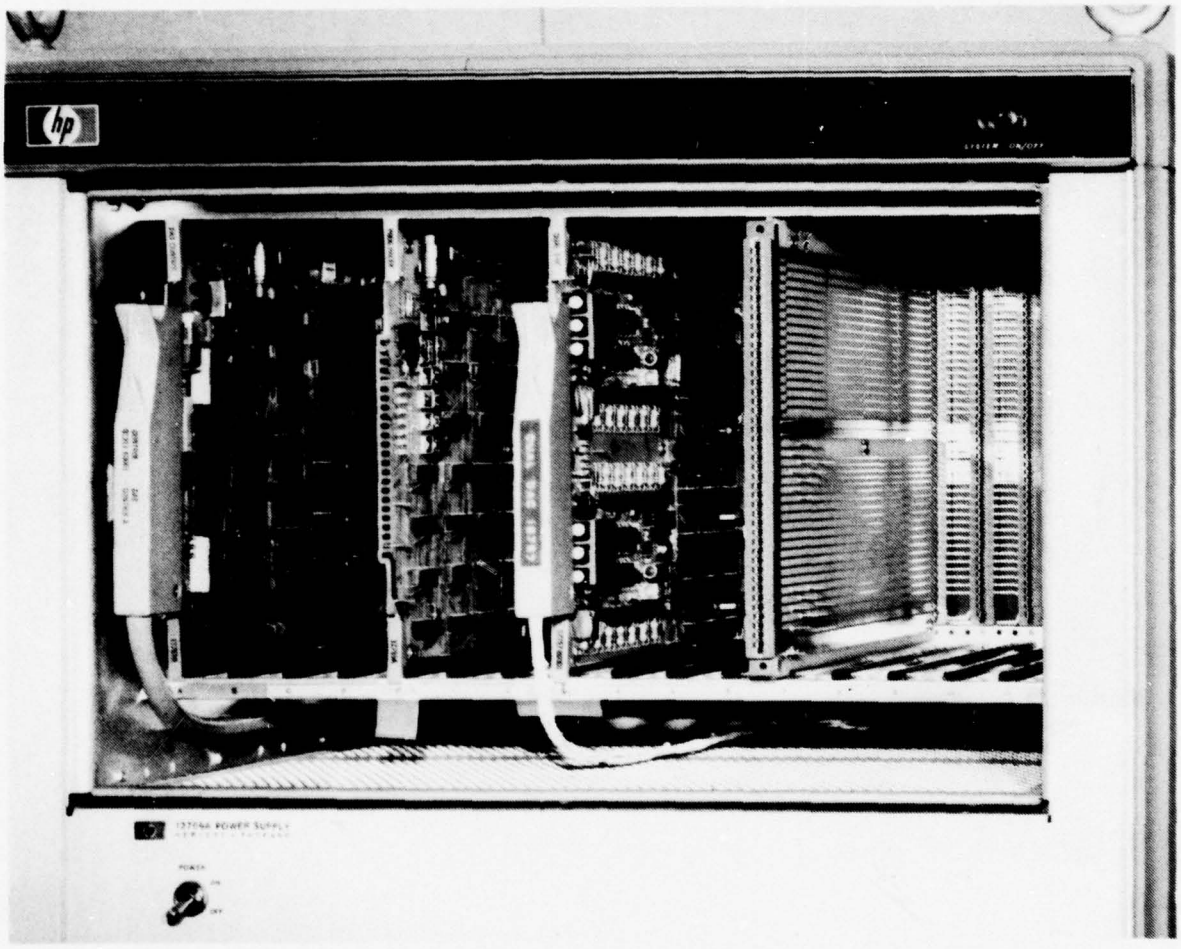


Figure 18. HP 2313B Multiplexer and A/D Converter

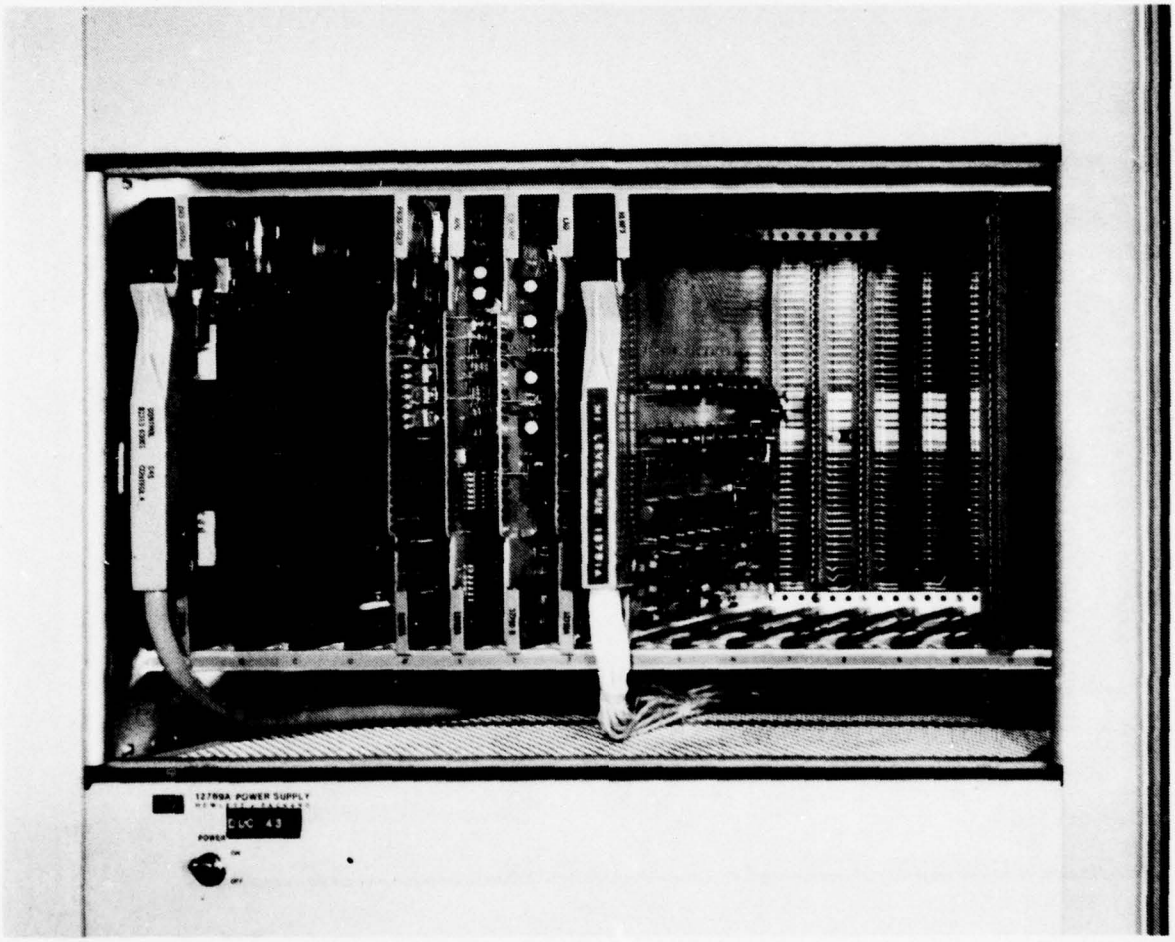


Figure 19. HP 2313B D/A Converter

2.4.1.2 Auxiliary Equipment Rack. - The auxiliary equipment rack (see figure 1d) houses the following major chassis:

- Laser Servo Drawer
- Laser Interface Drawer
- Interface Panel Assembly
- Power Distribution and Blowers

At program inception, the rf modulator was to be placed in this rack, however, the decision was subsequently made to mount the unit directly under the laser work table near the rf load chamber to minimize the distance from the load chanber rf probe to the modulator. The rack, therefore, has considerably more room than is necessary.

Both laser interface and servo drawers were placed in this rack along with an interface panel assembly which serves as a cable interface between the HP computer and the laser. This assembly also has optical isolator cards which interface three specific laser data lines to the HP computer. Seventeen additional optical isolator channels are available for use with the modulator. They are not presently being utilized.

2.4.1.3 Laser-Trimmer Bench. - The Quantrad Model 1021 Laser Trimmer consists of the following major assemblies (see figures 1b and 1d):

- YAG Laser
- Optical Subsystem
- Beam Positioner

The laser is a high-powered, continuously pumped Nd:YAG oscillator. It uses an acoustic-optic Q-switch to achieve short, high-power pulses of infrared light which are useful in material-removal applications.

The optical subsystem consists of optics which direct the laser beam (the beam positioner), provides for binocular viewing of the work area, and provides for viewing on a tv monitor. The beam positioner uses moving prisms to optically sweep the laser beam over the work area. The stage is motor driven by commands from the Hewlett-Packard computer.

Detailed descriptions of the major assemblies and modifications to the laser control box are given in the following paragraphs:

- Laser

  The laser consists of two modules: the laser power supply and the laser head (see figures 1b and 1d).

  The power-supply cabinet contains the pump-lamp power supply, the rf driver for the acousto-optic Q-switch, the water-to-water heat exchanger and laser controls.

  The laser head assembly consists of the laser-pump cavity, the optical resonators, and Q-switch. A 2.5 kW krypton-arc lamp is used to optically pump the YAG laser rod. A safety shutter insures positive and quick shutoff of laser output.

- Optical Subsystem

  The optical subsystem consists of the optics enclosure which contains the beam-expanding telescope, the trinocular head, the illuminator, the tv camera, and tv monitor. The circuit to be trimmed may be viewed through the binocular eyepiece or on the tv monitor. Laser spot-size selection is provided by adjusting the iris and spot-size knob on the control panel of the optics box.

- Beam Positioner

  A modified beam positioner, designated the Model 708S, is used in this system. It is a digitally encoded, servo-driven beam positioner, capable of receiving and storing

position commands from the computer output. It then generates the necessary velocity commands to a servo-positioning system to cause the beam to assume the programmed position. Three modes of operation can be selected, two automatic and one manual. In the automatic slew mode, the X-Y positioner, commanded by computer, slews at a rate of 5 inches/second to the position being addressed, moving simultaneously in the X and Y directions with an acceleration and deceleration program resulting in minimum positioning time consistent with a positioning accuracy of ±1/2 of the least significant bit. In the automatic trim mode, the beam positioner moves at an adjustable steady-state rate of up to 400 mils/second, the motion being confined to either axis. Acceleration and deceleration rates are consistent with minimum trim times using synchronous laser triggering to provide a uniform density of laser energy/unit length of trim cut. In the manual mode, the computer interface no longer controls the beam position or laser triggering. Control is transferred by a front panel key switch to a two-axis joystick that provides proportional velocity control in the desired directions. Laser triggering is either synchronous or asynchronous as selected from the laser front panel. The computer interface also supplies status-monitoring signals to the computer, including the two-position encoder outputs and systems data outputs from the laser and the control system.

A more detailed discussion of the Quantrad Laser is presented in the Fourth Quanterly Report[27].

- Laser Control Box Modifications

Modifications to the "laser control box" were made to allow for full operation from the laser work bench when testing

27 "Production Measurement of Fuze Components Under Dynamic Stress", 11 February 77 to 10 May 77, Contract DAAB07-76-C-0032.

UUT's once the initialization procedure was entered at the TTY.

Figure 20 is a photograph of this modified unit. The four following additions were installed and tested:

- "Pass" Light
- "Fail" Light
- "Voltage Out of Tolerance" Light
- Laser Override Switch

The first two items signal the operator when UUT passes or fails. A full TTY data printout supplements these lights.

The third item signals the operator that the UUT precision power supply (30.000 V or 27.500 V, depending upon UUT) is out of voltage tolerance[28].

The fourth item bypasses the laser-inhibit circuitry to assure laser turnoff during amplifier R_9 trimming.

Table IV summarizes the normal controls and indicators on the "laser control box".

Table IV. Laser Control Box Functions

Description	Function
Manual Light	Alert Operator That Unit Is in Manual Control.
Manual/Remote Key	Local Switch That Allows Operator to Place Laser into Manual or Computer Control.
Data Entry Button	Allows Operator to Input XY Coordinate Data into Computer After adjusting Laser Stage to R_9 (C_{21},C_{22}) Cross Hairs.

28 The computer program was set up to monitor UUT bias current shorts after B+ turn on and prior to testing.

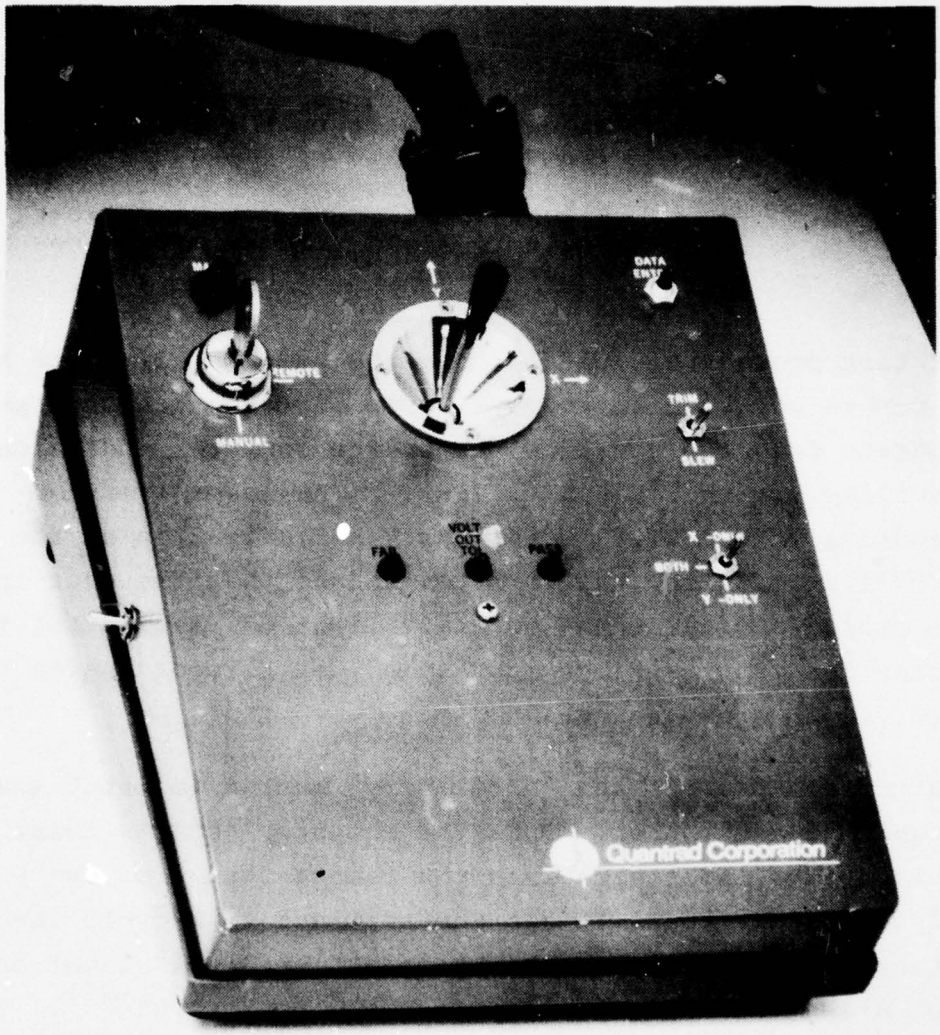


Figure 20. Modified Laser Control Box

Table IV. Laser Control Box Functions (Continued)

Description	Function
X-Only,Y-Only, Both Switch	Allows Operator to Move X, Y, or XY Coordinates of Laser Stage When in Manual Mode.
Trim Slew	Allows Operator to Laser Trim or Slew, (Manual Only).
Joystick	Allows Operator to Position Laser Stage in X and Y Coordinates When in Manual Mode.

A typical test procedure would be to place the manual/remote key into the remote position and remove it so that the test operator cannot operate from the joystick unless the computer indicates this capability via the "manual" light. (The laser-override switch should also be OFF.) After test initialization at the TTY and UUT installation, the computer senses that the door interlocks are closed and turns the "manual" light ON, indicating that the operator can use the "joystick" to adjust XY coordinates to (R_9) or (C_{21},C_{22}) cross hairs.

The operator then presses the "data entry" button to input these coordinates to the computer. Once the computer accepts these data it places the laser back into the remote condition and performs all subsequent tests. When the test and trim cycle is completed, the computer illuminates the "pass" or "fail" light and prints out all necessary data corresponding to the UUT[29]. The operator can then remove and replace the UUT and repeat the cycle.

2.4.2 Amplifier Testing

Computer access to eight UUT test points plus the fire pulse output signal is needed to test and tune ECOM production amplifier

29 A serialization program also labels R_9 or C_{21}/C_{22} for data traceability.

boards. In addition to these points, several capacitors (C_{13}, C_{14}, C_{16}, see figures 2 and 3) must be initialized to assure that quiescent conditions are maintained prior to an individual test. Bias voltage is also introduced.

All the above functions are provided via the amplifier electronics card located in the amplifier electronics assembly on the laser work bench.

2.4.2.1 Amplifier Electronics Assembly. - The amplifier electronics assembly is located directly under the optics box on the laser work table (see figure 1d). It consists of three interface connectors near the X-coordinate servomotor and an amplifier electronics card, the principle buffer between amplifier UUT's and the computer.

This card provides the interface between the amplifier board UUT's and the computer. It is a wire-wrap card containing integrated circuit operational amplifiers and associated precision resistors used as buffer amplifiers to isolate the UUT outputs from loading by the computer input circuits. It also has amplification stages to maximize S/N ratio and minimize the least significant bit error (0.005 volt) in the computer a/d converter. The amplifier electronics card is physically located near the UUT circuits to minimize capacitance loading and noise pickup. Sufficient feedback is used with the amplification stages to assure high gain stability for frequencies within its normal operating band. Dual gain and ac/dc channels are provided as required; they are relay operated and under computer control. Potentiometers are provided to trim voltage gains and null dc amplifier offset voltages.

In addition, the amplifier electronics card provides buffered signals to the laser control and rf oscillator electronic cards. Relay-controlled, low-pass filtering for the d/a computer input signal is provided to attenuate the high-frequency components due to the computer d/a output "staircase". Relay-controlled,

quick-discharge circuits for proper operation of the UUT within the required test time are also provided. Several other test and conditioning circuits are utilized. The power supply and electronics assembly provides the required voltages for the amplifier electronics card and UUT.

2.4.2.2 Amplifier Electronics Card Functions. - Tables V and VI summarize the individual test circuits and functions on this card. Reference should be made to figures 2 and 3 as a supplement to these tables.

Table V. Amplifier Electronics Card Signal-Circuit Functions

Input From	Function	Output	To	Comments
Computer d/a	Filter & Level Set	a) Amplifier UUT Input	A) V_1 Input	a) UUT Input Signal
		b) V_1 Monitor	b) Precision Amplifier	
		c) RF Modulator	c) VVA* Input	
		d) RF Modulator AC Bite	d) Signal Separate & Scale Circuit	d) AC Test Signal
V_2	Buffer, ac Gain	V_2 Monitor	Precision Amplifier	Not Used in Initial Tests
V_3	Buffer, ac or dc Gain	V_3 Monitor	Multiplexer	Designed to Check R_9/R_{11} ac or dc Gain. Not Used for Initial Testing.
V_4	Buffer, ac or dc Gain	V_4 Monitor	Multiplexer	Adjustable ac/dc Gain. Not Used for Initial Testing.
V_5	Buffer, ac Gain	a) V_5 Monitor	a) Multiplexer	a) V_5/V_1 Measurements.
		b) Trim R_9	b) Laser Control Electronics Voltage Comparator	b) For ac Gain Tuning.
V_6	Buffer, ac/dc Gain, Video Gain	V_6 Monitor	Multiplexer	Rectifier Output Signal for Measuring Rectifier Transfer Characteristics and R_{19},R_{20} Values.
V_7	Buffer, ac/dc Gain	V_7 Monitor	Multiplexer	a) DC Injection for R_{19},R_{20} Measure. b) Discharge Circuits for C_{13} and C_{14}.

*VVA - Voltage Variable Attenuator in rf Modulator.

Table V. Amplifier Electronics Card Signal-Circuit Functions (Continued)

Input From	Function	Output	To	Comments
V_8	Buffer, Video Gain	V_8 Monitor	Multiplexer	SCR Gate and Step Response Voltage Sense.
V_9	UUT Load Buffer and Video Level Adjust	a) V_9 Monitor b) V_9 Monitor	a) Multiplexer b) Isolated Digital Input Card & Event Sense Card	a) Fire Pulse Monitor b) Fire Pulse Monitor

Table VI. Amplifier Electronics Card Quick-Charge and Discharge Circuits

Relay	Function	Comments
K_9	Quick Charge, C_{16}	Used in Conjunction with K_{15} and -22 Vdc Supply.
K_{12}	Shunts R_9 for R_{11} Measurement	Not Used in Initial Testing.
K_{10}, K_{14}	Discharge C_{13}, C_{14} & Charge C_{16}	Used in Conjunction with K_9.
K_{16}, K_{17}, K_{18}	Measure R_{19}, R_{20}	In Conjunction with 0.8 Vdc Source.

Note: Relay Nomenclature (K ()) Represents Amplifier Electronics Card Relay Number.

2.4.2.3 Laser Control Electronics Card. - The laser control electronics card contains the circuits that stop the laser from cutting by comparing the UUT ac stage output voltage to a computer-generated reference voltage. The HP computer transmits a computer-determined reference signal, REF 5, from the DUAL DAC to this card which compares it with the A5 (V_5 test voltage) signal from the amplifier electronics card. When A5=REF 5 the laser STBY/LASE switch on the manual control box overrides the computer control of the laser. A laser stop "flag" is then transmitted back to the computer. This circuit is utilized during amplifier (UUT) R_9 trim.

The laser control electronics card also converts a 20 Vdc dynamic-range voltage from the computer d/a converter output to a 10 Vdc range. This circuit is the "bias offset" block in the rf modulator schematic (figure 21). It drives the VVA "linearizer" and was designed to improve the computer d/a LSB error by 2:1. The circuit converts the computer d/a output voltage range from -10.24 to +10.24 Vdc with a resolution of 0.005 Vdc to a range of 0 to

+10.24 volts with a resolution of 0.0025 Vdc. Zero to 10 volts (0 to +10V) corresponds to a VVA dynamic range of 55 dB. The circuit, therefore, allows the d/a converter to operate over its entire range and provides a 55 dB range in rf attenuation. The 0.0025-volt LSB resolution corresponds to a 0.01375-dB shift in modulator-return signal level (assuming perfect linearity) at the test oscillator[30].

2.4.3 Oscillator Testing

Figure 21 is a detailed block diagram of the signal-processing circuitry used in testing ECOM Oscillator Assemblies. Relative signal levels are shown in decibels (dB). They indicate signal levels at selected points in the circuitry with respect to a reference signal from the load-chamber probe antenna. The absolute power levels shown in parentheses are in (dBm) and represent the nominal power levels expected[31]. The design of this circuitry was completed during the program and all parts were purchased and received. The modulator, however, was not assembled or tested at contract termination.

2.4.3.1 Oscillator Sensitivity-Test Concept. - The design goal of this program was to set oscillator "sensitivity" to within ±0.5 percent of a specified nominal value. That is, all unpotted production oscillator sensitivities shall be set at a fixed voltage ±0.5 percent after trimming.

To achieve this goal, a system was devised (see figure 21) whereby maximum use is made of the resolving power and accuracy of the HP 2112A Computer a/d and d/a Converters (HP 12751A and HP 12757A, respectively). The system design is summarized as follows:

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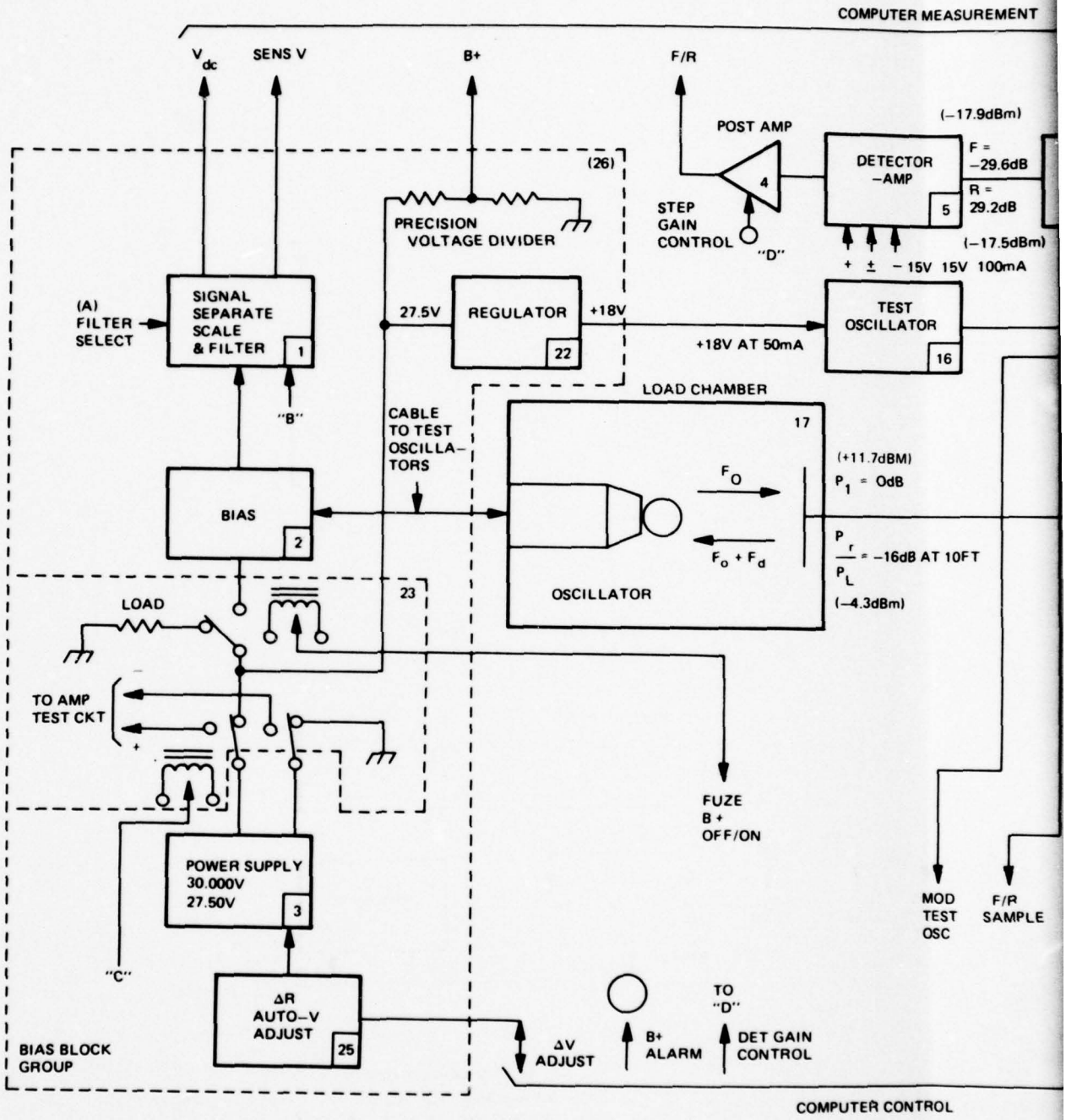
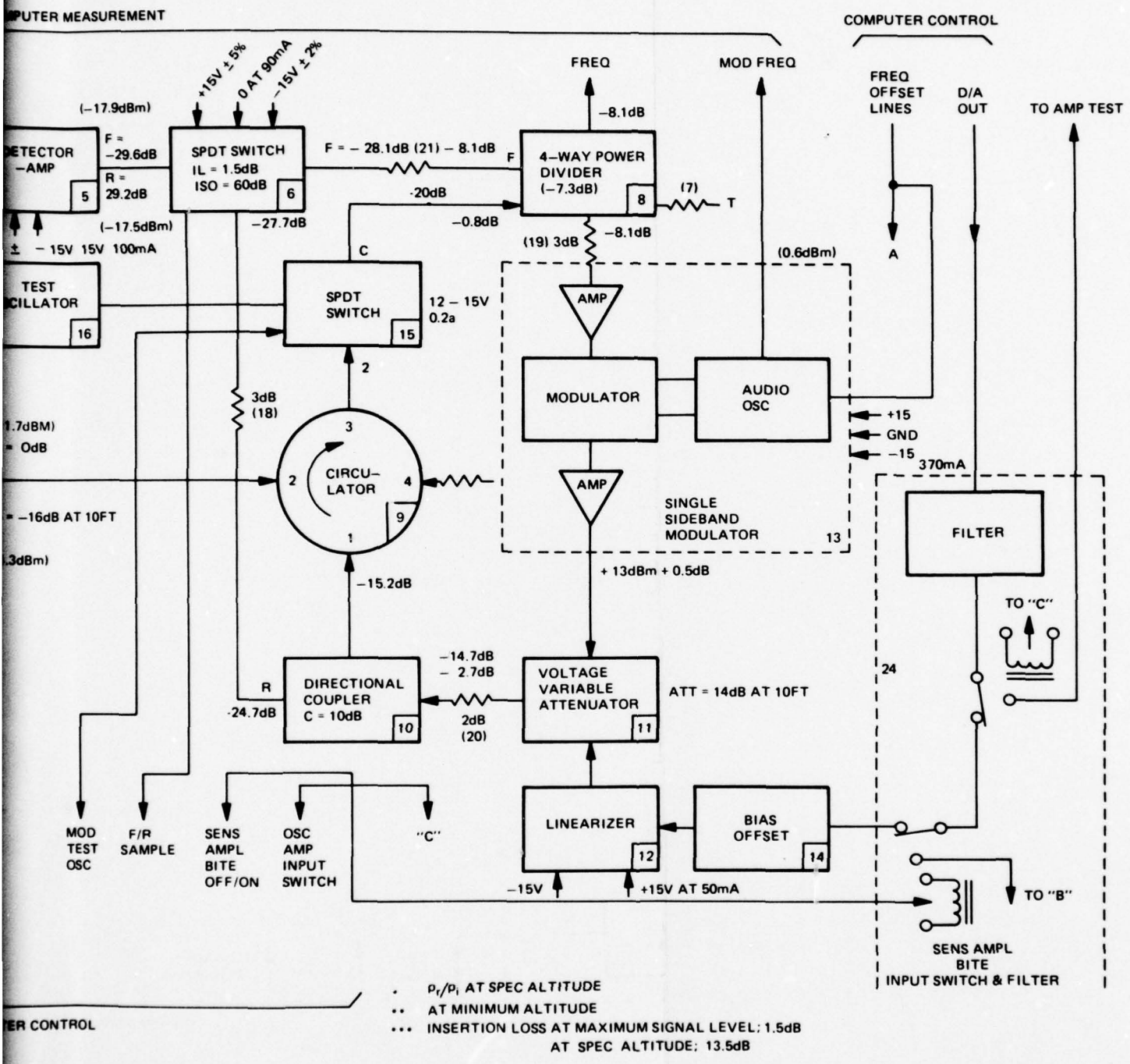
30 The shift in oscillator sensitivity represents 0.1584 percent LSB.

31 Experimental data indicates the feasibility of these values.


COMPUTER MEASUREMENT
V_{dc}
SENS V
B+
F/R
POST AMP
4
(−17.9dBm)
DETECTOR −AMP
5
F = −29.6dB
R = 29.2dB
STEP GAIN CONTROL
"D"
(−17.5dBm)
+ ± − 15V 15V 100mA
(26)
PRECISION VOLTAGE DIVIDER
(A) FILTER SELECT
SIGNAL SEPARATE SCALE & FILTER
1
27.5V
REGULATOR
22
+18V
+18V AT 50mA
TEST OSCILLATOR
16
"B"
LOAD CHAMBER
CABLE TO TEST OSCILLA-TORS
17
(+11.7dBM)
P_1 = 0dB
BIAS
2
F_O
$F_o + F_d$
$\frac{P_r}{P_L}$ = −16dB AT 10FT
(−4.3dBm)
OSCILLATOR
23
LOAD
TO AMP TEST CKT
FUZE B+ OFF/ON
MOD TEST OSC
F/R SAMPLE
POWER SUPPLY 30.000V 27.50V
3
"C"
ΔR AUTO−V ADJUST
25
TO "D"
ΔV ADJUST
B+ ALARM
DET GAIN CONTROL
BIAS BLOCK GROUP
COMPUTER CONTROL



. ρ_r/ρ_i AT SPEC ALTITUDE

.. AT MINIMUM ALTITUDE

... INSERTION LOSS AT MAXIMUM SIGNAL LEVEL; 1.5dB
AT SPEC ALTITUDE; 13.5dB

Figure 21. RF Modulator Functional Design

2

- System Calibration by Standard Oscillators

  Precalibrate the overall modulator/load chamber loop gain using several "standard" oscillator assemblies whose sensitivities were previously determined[32]. (The computer sets the loop gain while observing output sensitivity. It stops when the measured value of sensitivity equals the assigned value.) The "standards" are equi-spaced across the normal carrier frequency range for this oscillator design. The computer calculates and memorizes the ratio of reflected-to-incident power plus actual oscillator carrier frequency for each "standard" after the modulator loop gain is adjusted.

- System Test and Trim

  Individual units are trimmed after noting carrier frequency and adjusting overall modulator/load chamber loop gain to the memorized value for a given test oscillator carrier frequency[33]. Once this is accomplished, the test and trim sequence can commence.

2.4.3.2 Comments on Modulator System Approach. - Setting the ratio of reflected-to-incident power in the modulator for each test oscillator frequency eliminates the problem of insertion-loss variations of the individual rf components over frequency, temperature, and time. Loop gain setting accuracy is, therefore, dependent only on the short-term accuracy and resolution of the

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32 "Standards" are measured using an independent free-space measuring technique and sensitivity values assigned to each "standard" oscillator before modulator/load chamber calibration. Because the present primary measurement method is only accurate to about ±10 percent, all new oscillators will be set to V ±0.5 percent based on assigned values instead of on an absolute basis. The test and trim equipment should be reproducible to within ±0.5 percent as a design goal.

33 Interpolation of loop gain will be required for oscillators at frequencies between "standard" frequencies. The electrical distance around the modulator loop is minimized to reduce off-frequency ratio deviation.

a/d converter used to adjust this ratio and on potential errors in the individual detected signals in the modulator resulting from residual vswrs of rf components. Calculation error is negligible in this case.

2.4.3.3 Modulator Versatility. - The design is such that the test oscillators are stimulated by an accurately controlled burst of rf energy of constant amplitude at a frequency of $(f_o + f_d)$ [34]. Both amplitude and pulse duration are computer controlled via the voltage variable attenuator and linearizer shown in the schematic. Accurate computer monitoring of the return-signal level assures repeatable results.

The voltage variable attenuator-linearizer combination has a 55 dB dynamic range that allows the computer to provide near-continuous amplitude adjustment of return-signal levels.

Although the rf modulator provides for only three fixed-frequency (f_d) return-signal offsets, minor modifications to the existing hardware can expand modular capability to include direct computer-controlled FM.

2.4.3.4 RF Oscillator Electronics Card Functions. - The rf oscillator electronics card contains the principal signal-processing circuits associated with the rf modulator plus UUT power-supply-switching and level-adjustment circuits.

The following listing summarizes the principal functions performed by this card. Reference should be made to figure 21 for the items in this list.

a) Bias and Signal Separate and Scale Circuits (Blocks 1 and 2).

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34 f_o = carrier frequency.

f_d = single-sideband offset frequency.

b) +18.0 Vdc Regulator (Block 22).

c) The Precision Voltage Divider (p/o the Bias Block Group).

d) UUT Power Supply (PS) Off/On and PS Dummy-Load Relays.

e) The Forward/Reverse Power "Detector-Amplifier" Post Amplification Circuitry (Block 4).

f) A Current Sensor at the UUT Precision Power Supply Provides a Voltage Proportional to the Bias Current into Either UUT.

g) The "Input Switch and Filter" Circuit (Block 24) is Located on the Amplifier Electronics Card.

h) The RF SPDT Switch (Block 15) Switching Circuit.

i) The "Bias Offset" Circuit (Block 14) Is Located on the "Laser Control Electronics" Card.

2.4.4 Laser Modifications

The Model 1021 Laser Trimmer consists of the following major assemblies.

- YAG Laser
- Optical Subsystem
- Beam Positioner

The following changes were made to adapt the Model 1021 Laser Trimmer for use in the present program. Reference should be made to figures 1d, 20, 22 and 23 during the following discussion.

- The "servo driver" and "digital interface" drawers were removed from the Model 1021 cabinet and reinstalled in the "auxiliary equipment rack".
- The "laser control box" was modified to add "pass/fail" lights and a bias power supply "voltage out of tolerance" light and laser override switch as described in paragraphs 2.4.1.3 and 2.4.2.3.

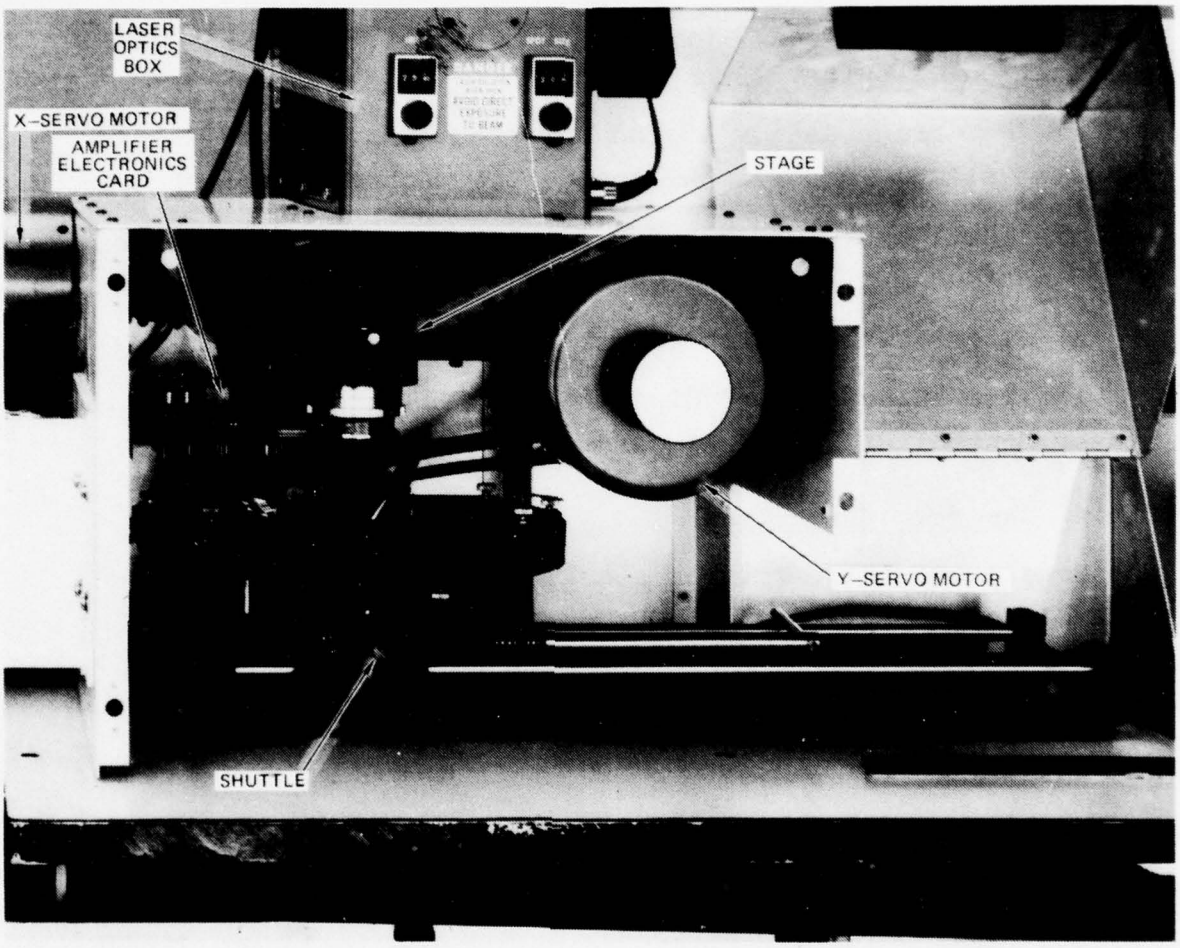

Figure 22. Shuttle and Laser Optics

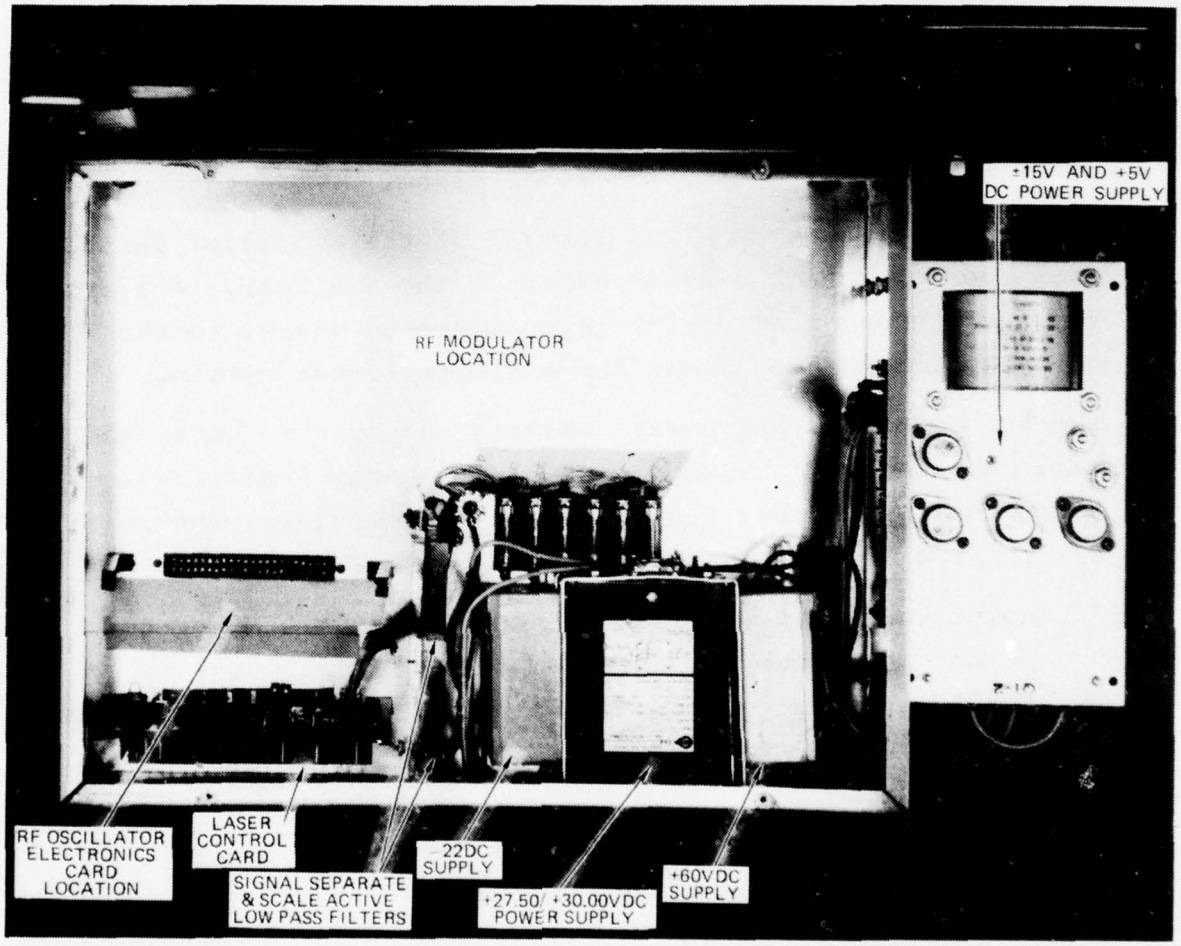

Figure 23. Modulator and Power Supply Chassis

- A removable manual-loading shuttle was mounted under the laser-beam positioner to hold amplifier UUT's during test. This shuttle is only used for amplifier test.

- An rf load-chamber assembly was added under the laser work bench to accept oscillator UUT's for testing. A hole was drilled in the laser work table to accept an auxiliary laser system which refocuses laser energy from the amplifier focal plane to the test-oscillator focal plane.

  Oscillator testing requires removal of the amplifier shuttle from the work bench, installation of the auxiliary lens system, and refocussing of the laser infrared energy to the chip-capacitor focal plane for efficient laser cutting.

- The "rf modulator and power" chassis was mounted under the laser work bench to assure minimum rf energy insertion loss from the load-chamber test probe to the modulator and to assure good rf phase stability during test.

- A bracket was added under the X-coordinate servomotor to accept interface cables to the amplifier electronics card. The amplifier electronics card is also mounted in this assembly (see figure 22).

- An access hole was drilled in the laser work bench behind the "rf modulator and power" chassis to allow for cable access to this chassis.

  Additional photographs of the loading shuttle are shown in the Fifth Quarterly Report[35].

- The visible light source on the Model 1021 Laser Trimmer was replaced by a Dolan-Jenner Model 170-D high-intensity Illuminator and fiber-optic system to enhance the visual optics observed in the tv monitor.

- The standard Model 1021 tv camera (an RCA TC-1000-C21) was replaced with a Hitachi Model HV620 for the same reason.

35 Fifth Quarterly Report, "Production Measurement of Fuze Components under Dynamic Stress", 11 May 77 to 10 August 77, Contract DAAB07-76-C-0032, figures 7 and 8.

2.5 TESTER SOFTWARE DESIGN

Programming for amplifier and oscillator testing were handled separately. Amplifier testing was given precedence since it appeared at project inception that it would be the most likely to be used because of the minor nature of the modifications to the M732 amplifier that would be necessary to adapt this unit to laser trimming. It also required measurement and calculation of several electrical properties, making the resulting test techniques potentially more useful in other applications.

Modifications to M732 oscillators was considerably more extensive (see paragraph 2.3.2), necessitating requalification of the assembly. As a result, final utilization in an actual production facility was less likely than that for the amplifier[36]. The design of an accurate test and trim system for oscillators, however, was much simpler than that for amplifiers. Once a viable system was decided upon, programming is straightforward in that only three direct measurements (sensitivity, detector voltage and rf frequency) are required to determine the necessary capacitance change to set UUT sensitivity.

2.5.1 Amplifier Test Signals and Measurements

It is not possible to use an analog M-wave stimulus signal to test and trim UUT's because of the short time requirement (1.2 seconds/unit) imposed as a program goal.

A single M-wave stimulus lasts about 1.4 seconds[37]. Because of the test amplifier's frequency response and nonlinear characteristics, at least three M-waves are needed to determine band center and band edge HOB's.

---

36 Not so for a combined oscillator/amplifier test and trim approach.

37 Assuming a start altitude of 800 feet.

A series of short signals was devised, therefore, to determine amplifier parameters without the need for an M-wave stimulus. The response to an M-wave is then calculated and the amplifier is trimmed to meet the desired mid-band HOB. The details of this operation constitute the real-time amplifier test and trim process. The analytic approach then would be extended to include the impulse response of the UUT input stage so that HOB calculations could be performed over frequency. This latter extension was not included in the initial programming.

2.5.1.1 Real-Time Test/Trim Requirements. - The real-time amplifier test and trim process contains the following requirements:

- Output a stimulus to the amplifier under test.
- Measure the amplifier response to the stimulus.
- Calculate the amplifier parameters of interest.
- Determine the required gain correction.
- Perform the resistor trim while monitoring UUT pre-amplifier output voltage.
- Recheck gain and calculate final HOB.
- Log the pertinent data on the test for future reference.

These requirements are shown in figure 24. The initialization section accepts (from the operator) the time of day and information on the test. At this time, all flags and buffers are initialized and the stimulus tables are read from the disk. At the start of test, the stimulus is outputted and the response of the amplifier to the stimulus is measured. After all amplifier parameters have been determined, a calculation to determine the required amplifier gain is performed. This calculated gain then represents a value which will cause the fuze to detonate at a specified height above the ground. The laser subsystem is then commanded to cut the trimming resistor to 95 percent of the required calculated gain while the UUT ac output is monitored. The ac gain is retested and a "shadow" cut on the resistor is made until the desired final

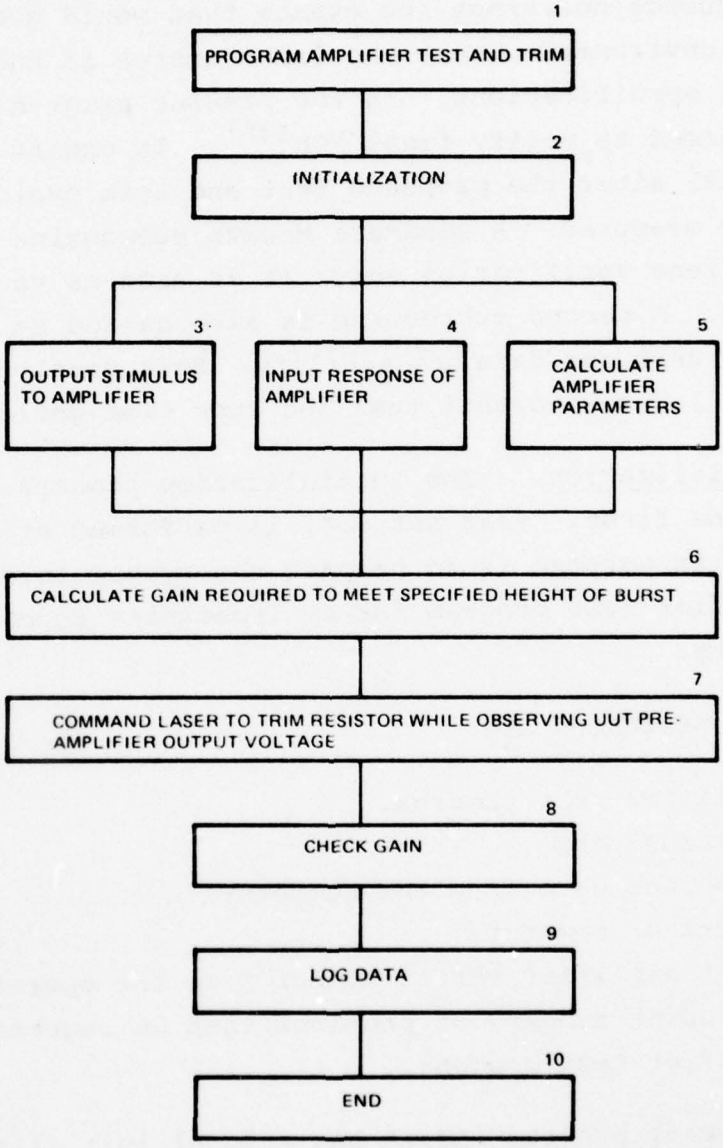

Figure 24. Functional Flowchart of the Amplifier Test and Trim Process

gain is reached. After trimming is complete, a final check verifies that the gain is correct. Data logging of the amplifier parameters and execution time of each routine completes the process.

The above sequence describes the events that would occur in a production test environment where the laser tester is known to operate within design specifications. In the present program, an additional test is performed to verify final HOB[38]. It occurs at block (8) (see figure 24) after the proposed test and trim cycle is completed and test time measured. A separate M-wave subroutine is introduced for test and tune verification only; it is used as an independent reference HOB. A second subroutine is also called at this time to serialize the unit for data traceability. Both routines are not included in the 1.2 second/unit test and tune time goals.

2.5.1.2 Initialization. - The initialization process consists of two parts. The first, "test set up", is performed at the start of operations. Its purpose is to prepare the system to continuously run the amplifier test program for an indefinite succession of amplifier units.

The functions performed are:

- Load amplifier test program.
- Load stimulus table.
- Input time and date from the operator.
- Input operator comments.
- Input last amplifier serial number from the operator.
- Load and print summary of previous test on request.
- Run amplifier test process.

The amplifier test program itself has a local initialization function. It performs the following:

38 The standard analog test method presently used to measure HOB.

- Initialize flags, buffers, etc., before each UUT test.
- Place laser into manual control. Turn on "manual" lamp on laser control box.
- Wait for the "data entry" command from the operator.
- Read initial laser start stage position.

After receipt of the "data entry" command, the amplifier test and trim process automatically energizes the UUT and continues until the unit is completely tested, and the data logged.

2.5.1.3 Input/Output Process. - The function of the input/output process is to configure the hardware for each test, provide stimuli to energize the amplifier and take sample measurements of the amplifier response. For reference, figures 2 and 3 contain block diagrams of the test amplifiers. Table VII summarizes the hardware configuration, input signals to the amplifier, measured voltages for each test and the amplifier parameters whose values must be calculated.

In order to achieve minimum execution time, it is necessary to have parallel operation of applying the stimulus, measuring the amplifier response and calculating the amplifier parameters. The measurement-control function (see figure 25) is a continuation of the initialization process. The i/o module (see figure 26) must first update the information on which i/o test is to be performed. On initialization from the control process, it will record a one. The routine to perform test 1 will configure the hardware for this test. It then initiates a read function through a DMA channel. The system returns to measurement control after initialization of the i/o process. Completion of the i/o process returns control to the i/o function. The measurement number is then updated to 2. The hardware is configured for the second amplifier measurement and an input (DMA) read is ordered. It is required that the stimulus be applied to the amplifier within several milliseconds after initialization of a read. Note that the system has the capability to have an output immediately after initiating an input.

Table VII. Test Amplifier Measurement Parameters

Item	Desired Parameter	Type	Frequency (Hz)	Time Duration	Voltage Level mVrms	Output Signal Test Points	Condition of C_{13}	Condition of C_{14}
1	AC Gain (Rectified Average)	Sinusoid	726.7	10 cycles	18	V_1, V_5	SH	SH
2	Rectifier Transfer Gains and Thresholds							
	a) +Half Cycles	Negative Parabolic	N/A	1 ms	100mV	V_5, V_6	SH	SH
	b) -Half Cycles	Positive Parabolic	N/A	1 ms	100mV	V_5, V_6	SH	SH
3	RC Integrator & Coupling Circuit Equivalent Source Impedance (R_{19} & R_{20} values)	None	(DC Input Signal at V_7)			V_6, V_7	SH	SH
4	RC Integrator and Coupling Circuit Unit Impulse Response	Sinusoid	726.7	14 ms	5	V_8	OC	OC
5	SCR Firing Potential	Sinusoid	726.7	10 cycles	100	V_8	OC	OC

Notes: 1. See figure 2 for test point location.
2. OC - Open circuited; SH - Shunted with precision low-value resistor.

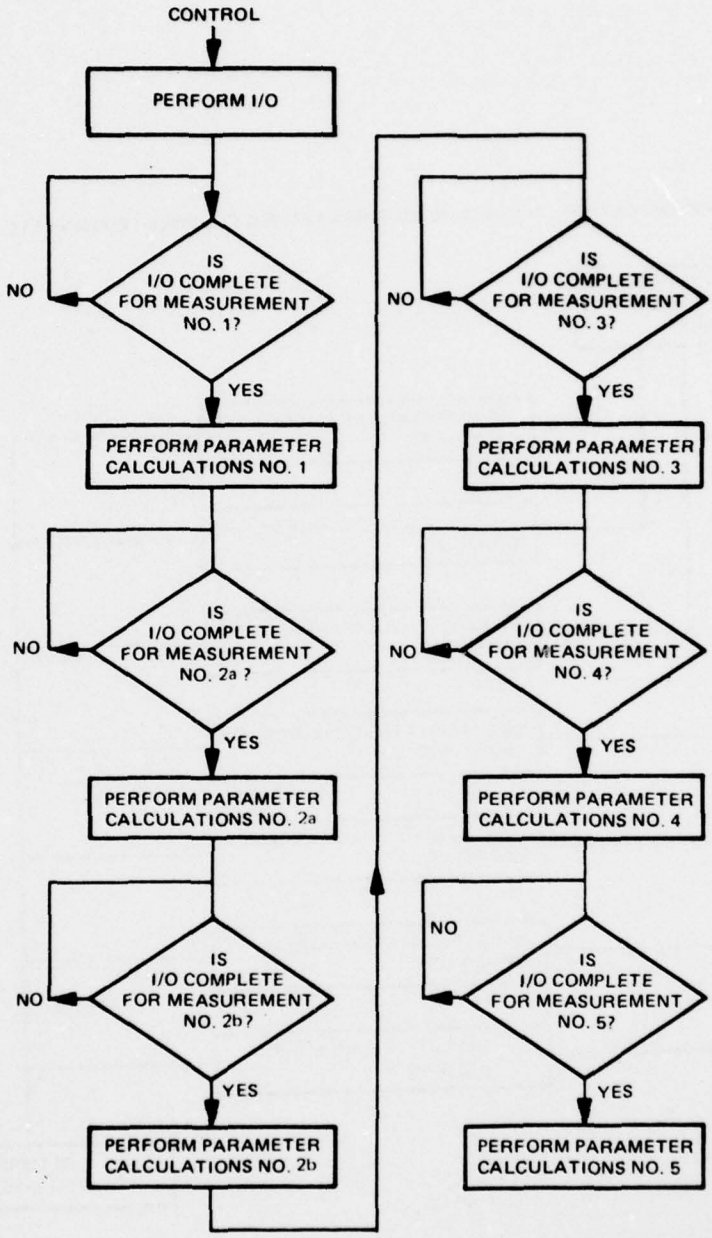

Figure 25. Measurement Control

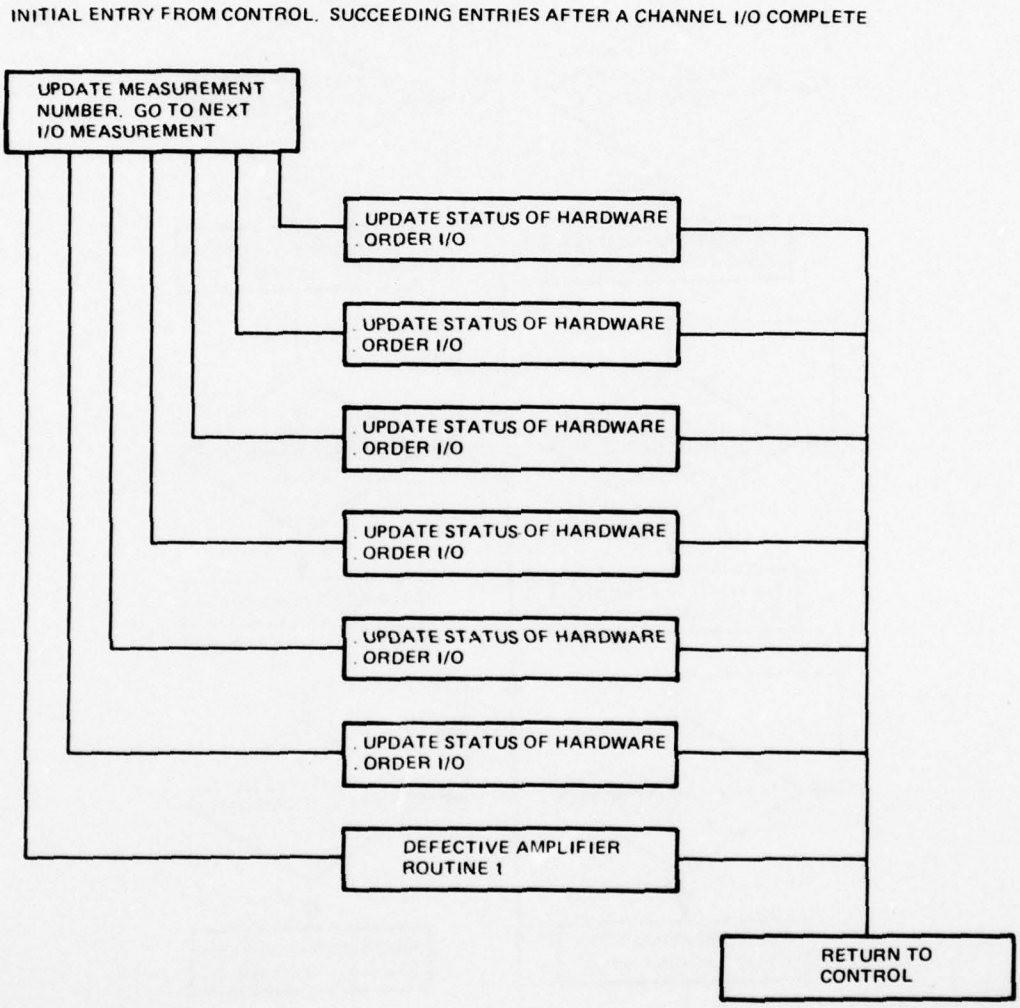

Figure 26. I/O Functional Flow

The correct timing of i/o will automatically be achieved providing the i/o is made through DMA channels. Completion of the initiating of i/o for measurement 2 returns control to the calculations that were in process at the time interrupt occurred. The i/o for the measurement is complete at this point. Calculation of the first set of parameters can then be started. These calculations may or may not be completed when an interrupt occurs at the end of the measurement 2 i/o. In this case, the interrupt causes control of the system to return to the i/o module. The measurement number is then updated to 3; the i/o is initiated for measurement 3 and control returns to complete the interrupt calculation. This process continues until all measurements are complete and all parameter calculations are carried out.

In summary, it is emphasized that the i/o process is continuous. As soon as the i/o for one measurement is complete, the i/o for the next measurement is initiated. The only limitation on parallel calculation is that the calculation must wait until all the data is present. The more sophisticated approach of using partial data to start parallel calculations is not employed for this test.

2.5.1.4 I/O Measurement/Stimulus Process. - The functional organization of the i/o measurement/stimulus process was described in the previous paragraph. Individual i/o functions are now considered. It should be stressed that the following discussion updates amplifier-test software as it existed at contract termination (table VII is part of the update). Individual tests were developed to "mesh" with the interface hardware described in paragraph 2.4.2 and UUT's[39] at least to the degree that input stimuli and subroutines were acceptable to begin UUT system testing. The addition of relay-closure commands for B+ turn-on, quick charge and discharge and buffer amplifier gain selection remained to be incorporated. This added task, however, is straightforward since all the required hardware is available.

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39 Except for updating items 2 and 3 of table VII.

Figure 27 represents a recurring sequence at the beginning of test for each UUT. The measurements themselves are now discussed in detail. The measurement process must control both the relay closures and the positions of the analog multiplexer to be able to read data. The functional flows of the measurement routines are shown in figures 28 to 33. All are similar except figure 28 which includes an initial B+ turn-on and 5-second wait to warm up the UUT[40].

- AC Gain Measurement Data

  Initially, set the pacer in analog controller 1 to 45,000 words per second, then set the pacer in analog controller 2 to 15,000 words per second. Both of these values represent the maximum capability of the a/d and the d/a converters, respectively. Next, the analog multiplexer is set to alternately read positions V_1 and V_5. To provide proper "roll over" of the analog multiplexer, the last address detector must be initialized. The actual output/input commands can then be issued. For this test, a stimulus table representing 10 complete cycles of 726.7 Hz is outputted. To allow time for the amplifier transient to die down, the initialization of the output of the stimulus is followed by a "wait" period prior to the computer input of the amplifier response. Upon completion of this command sequence, the system returns to control.

- Rectifier Transfer Function Data

  The functional flow of measurement 2a and 2b are almost identical to the previous measurement flow. Again, the pacers in controllers 1 and 2 are set to 45,000 and 15,000 words per second, respectively. They differ only in the

40 In a production situation, the units can be pre-warmed by applying B+ prior to entry to the trimming station.

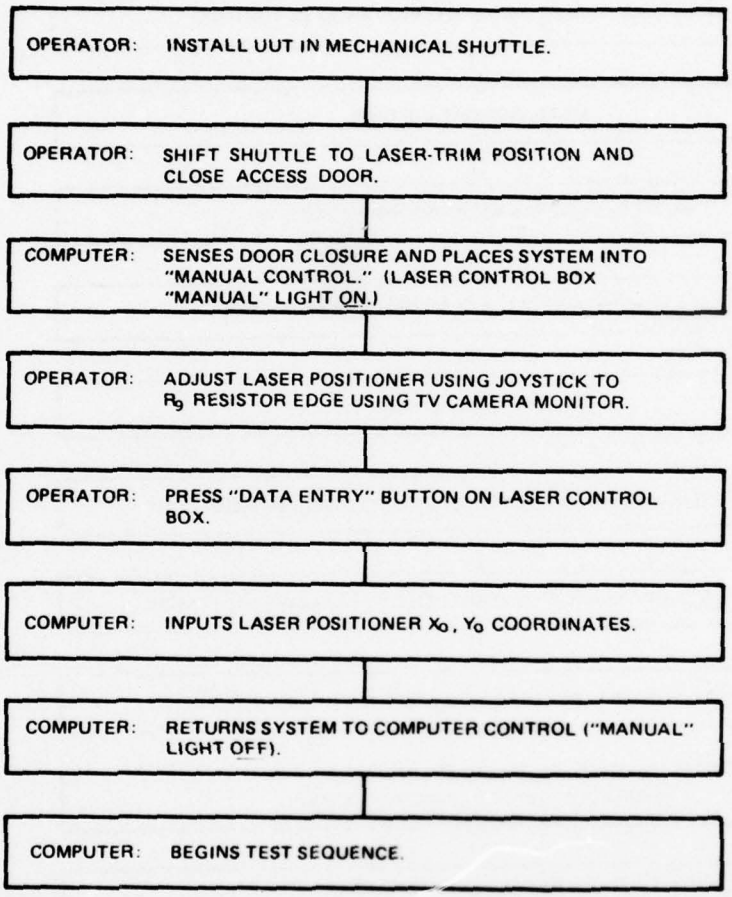

Figure 27. UUT Test Initialization Flow Graph

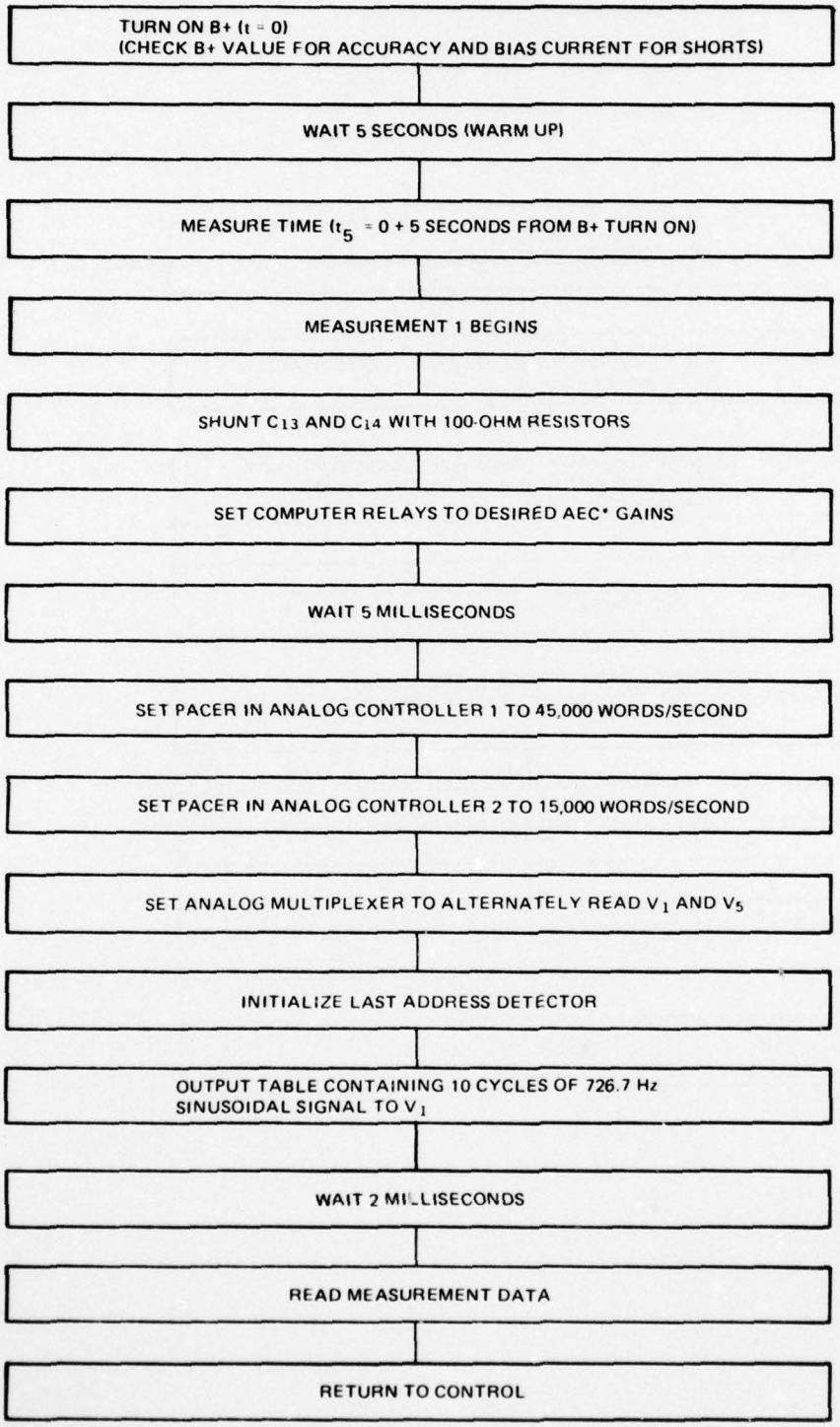

Figure 28. Functional Flow of Measurement 1 (AC Gain)

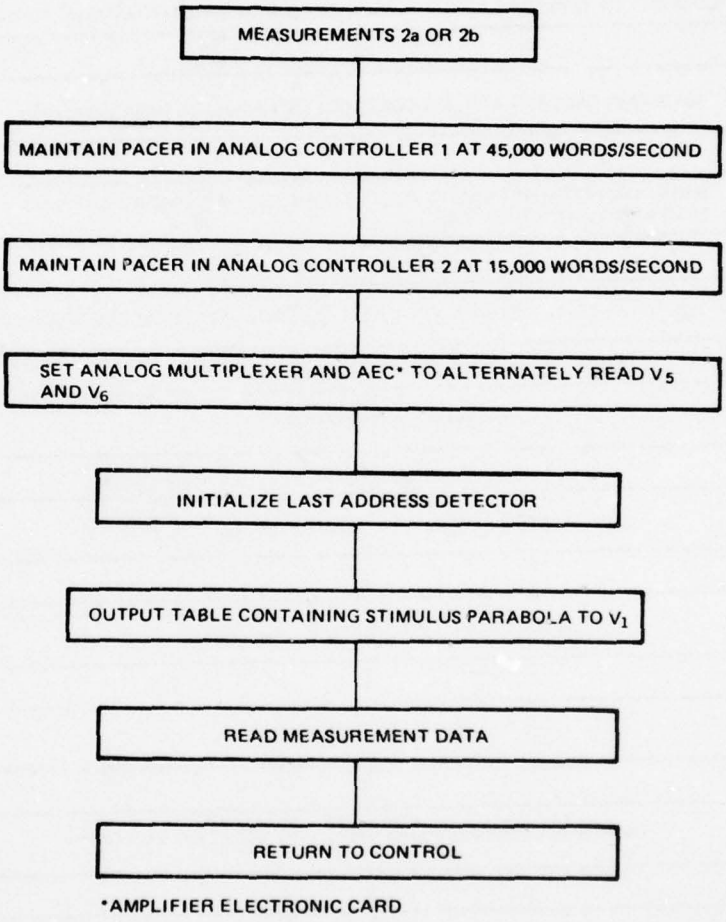

Figure 29. Functional Flow of Measurements 2a and 2b (Rectifier Transfer Characteristics)

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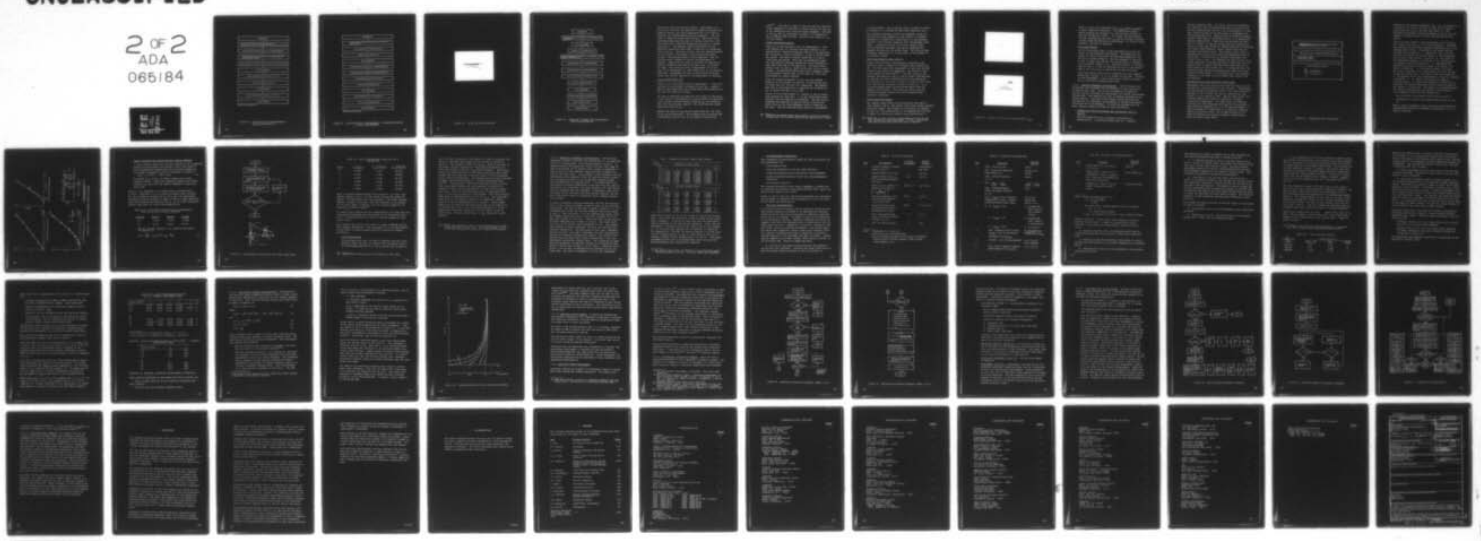

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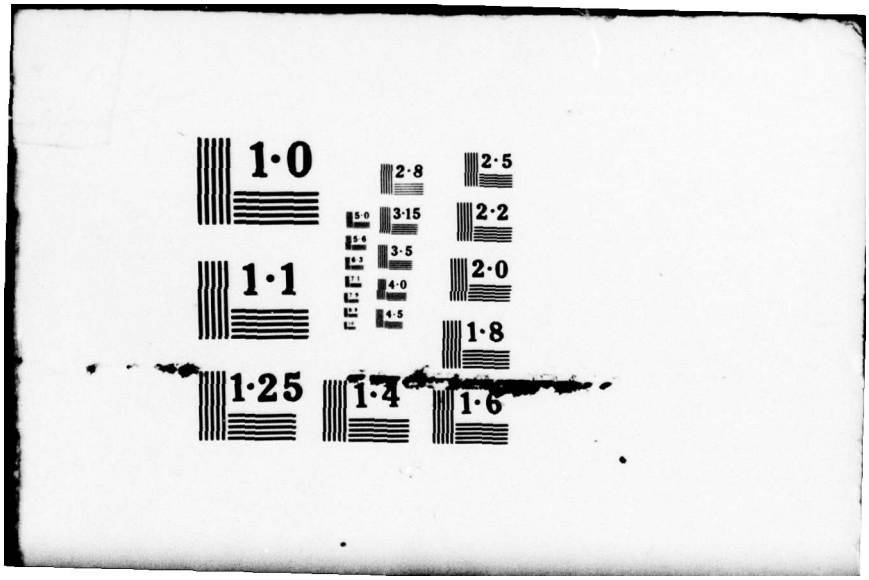
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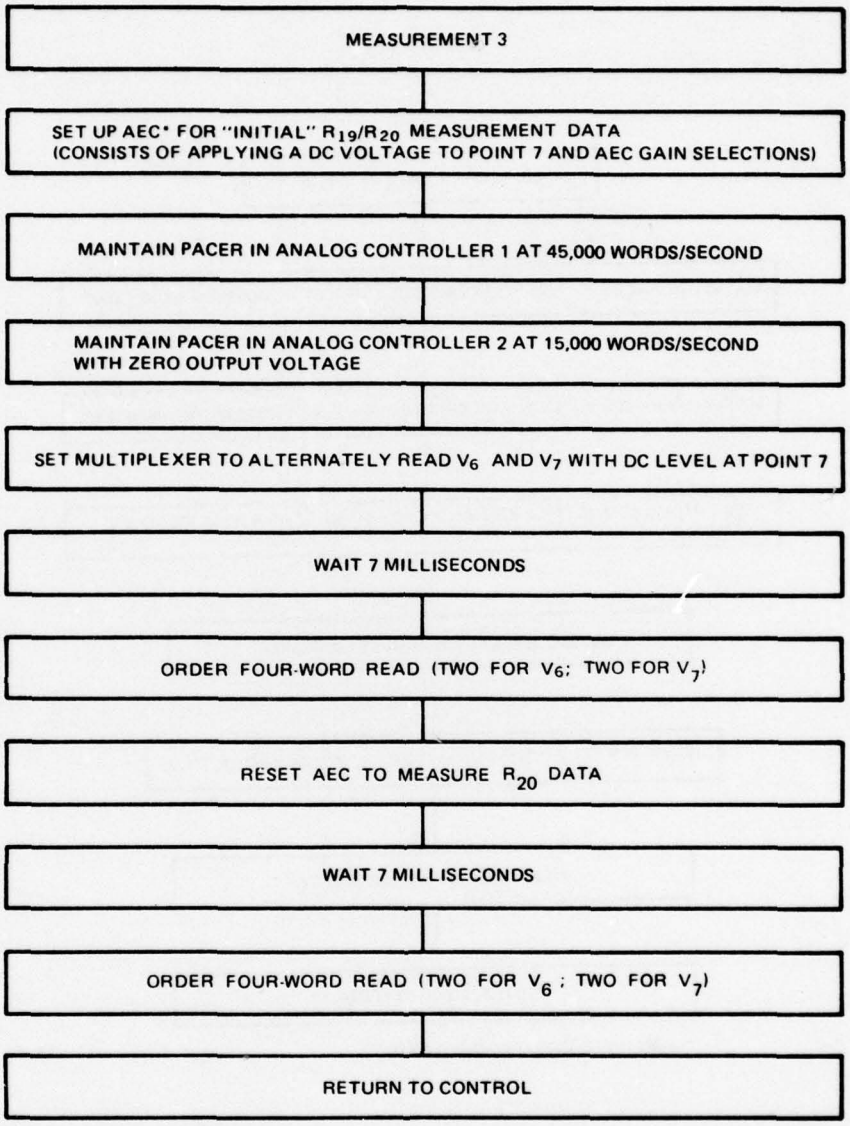

*AMPLIFIER ELECTRONICS CARD

Figure 30. Functional Flow of Measurement 3 (R_{19}/R_{20} Measurements)

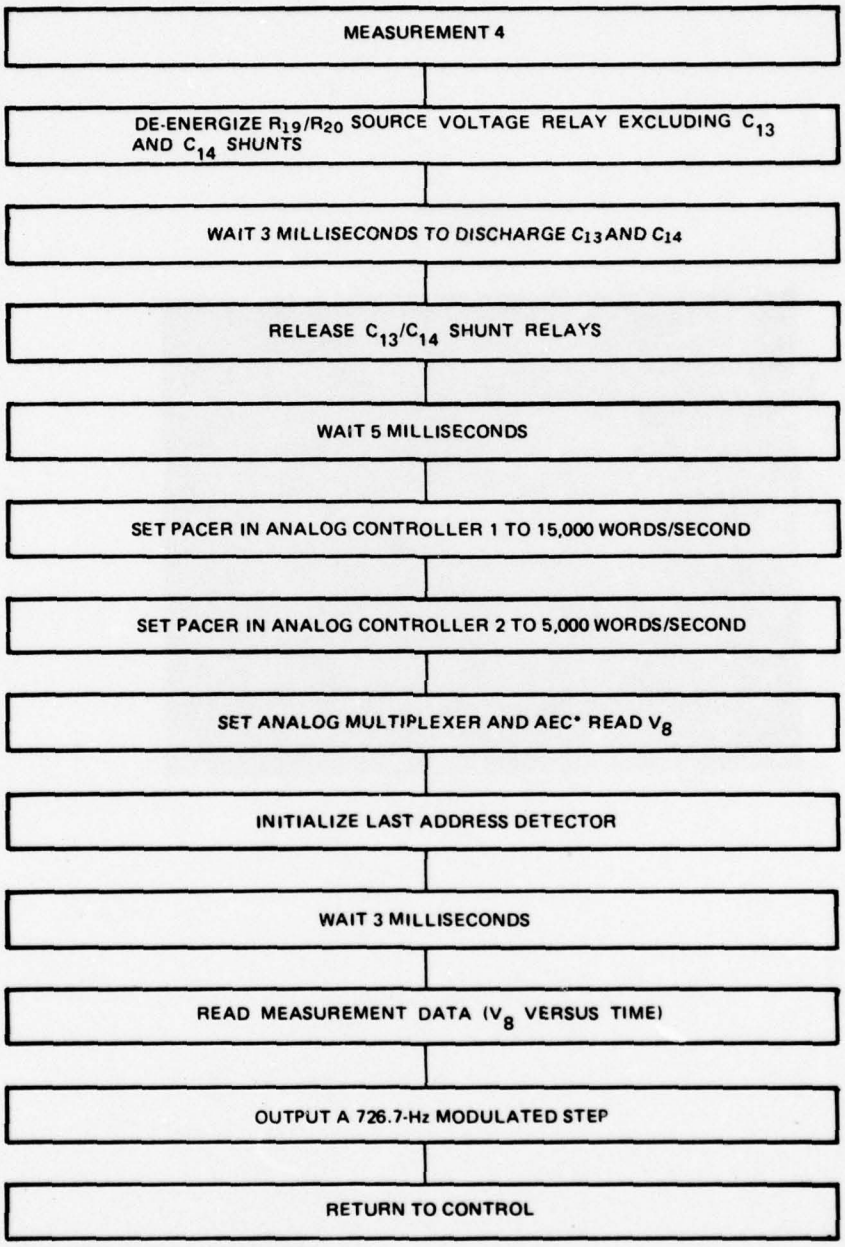

Figure 31. Functional Flow of Measurement 4 (Integrator/Coupling Circuit Step Response)

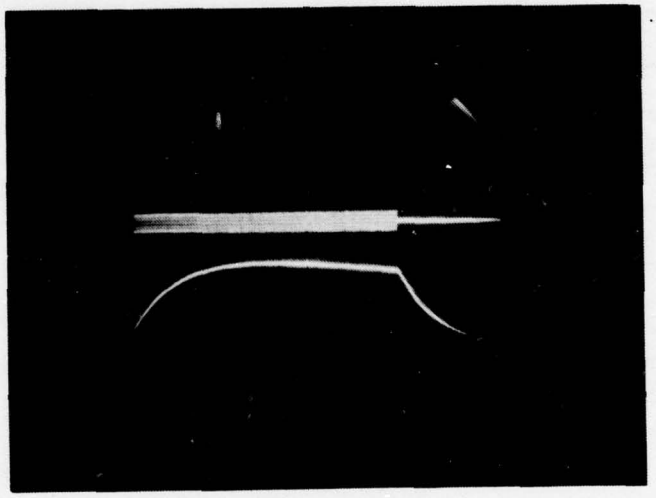

Figure 32. V_1 and V_8 Vs Time Waveform

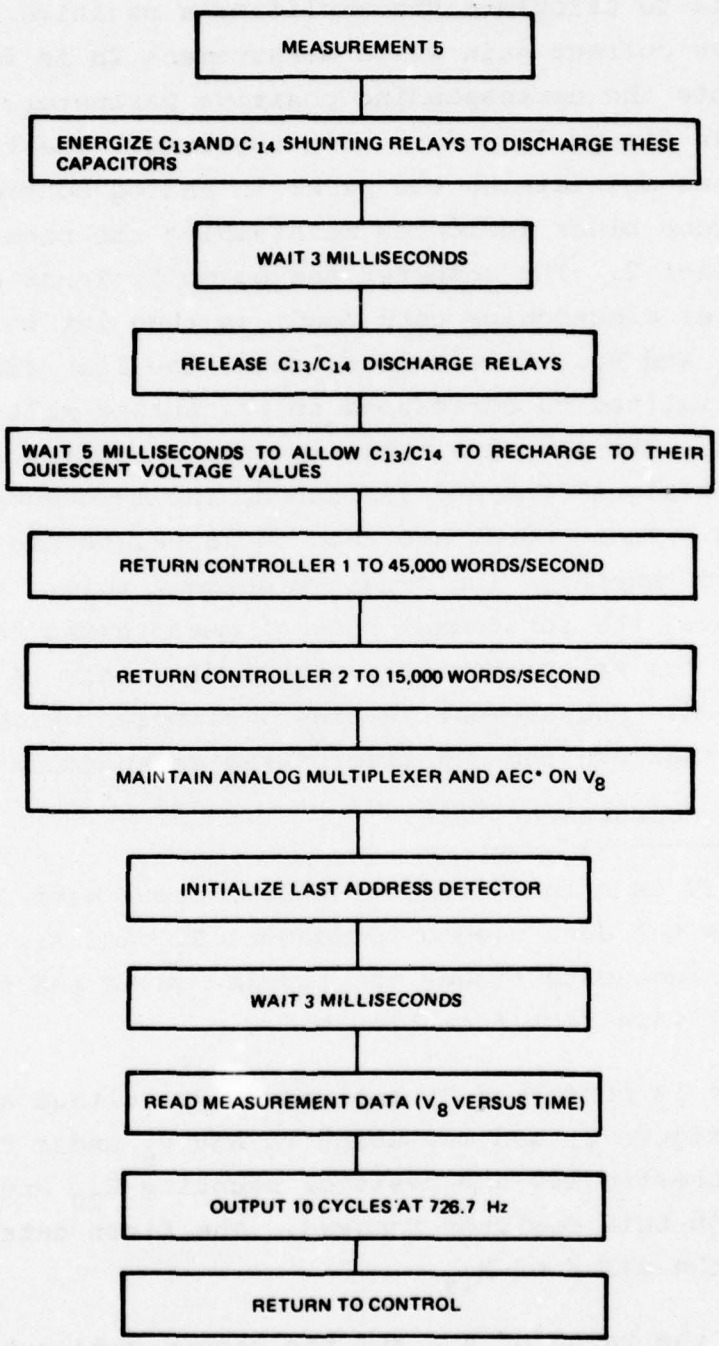

Figure 33. Functional Flowchart for Measurement 5 (SCR Firing Potential)

table which forms the stimulus signal. Measurement 2a is for data to calculate the amplifier's negative threshold and negative current gain while measurement 2b is for data to calculate the corresponding positive parameters. The flow shown in figure 29 covers both routines. The first block indicates maintaining the pacer in analog controller 1 and the second block indicates maintaining the pacer in analog controller 2. The computer analog multiplexer and the amplifier electronics card (AEC) is then set to alternately read V_5 and V_6. Once this is done, the last address detector is initialized to correspond to the analog multiplexer setting. The stimulus table is then outputted. Once the stimulus-signal command is issued, the measurement is enacted. These words are used to calculate the amplifier's negative threshold and negative current gain. As pointed out above, the functional flow of measurement 2b is the same as for measurement 2a; they differ only in the stimulus described. Measurement 2b uses a stimulus which contains values that are the negative of the measurement 2a stimulus.

- R_{19}/R_{20} Measurement Data

Figure 30 is a functional flow for measurement 3. This test provides the data needed to measure R_{19} and R_{20}. Knowing these values establishes the current gains and thresholds for the full wave rectifier blocks.

The test is performed by applying a dc voltage at test point 7 (see figure 2) and measuring V_7 and V_6 under two conditions: with a precise 100-ohm resistor shunting R_{20} and remeasurement with this resistor removed. The first data set establishes the value of R_{19}.

Knowing the value of R_{19} and the second data set, the value of R_{20} can be determined. The necessary shunt resistors and and switching circuits are on the amplifier electronics

card[41]. Note that V_1 input is zero and that the rectifier-output impedence is very high (a current source) so that R_{20} is not effected by the rectifier-output impedance. Accuracy in the R_{19} and R_{20} calculation is about $\pm$ 0.05 percent if R_{20} is shunted with 100 ohms. The wait time allows for C_{14} to fully charge.

- Output Integrator/Coupling

Figure 31 is the functional flow for measurement 4. This test obtains data to calculate the step response of the post-rectifier integrator/coupling circuit in the amplifier. Now the pacer in analog controller 1 is set to 15,000 words per second. The pacer in analog controller 2 is set to 5,000 words per second. This rate is considerably lower than the previous settings because the filter bandwidth is much lower than that of the amplifier. The analog multiplexer is set to read V_8, which is the test circuit output voltage. The amplifier-input-signal level (computer output) is low enough to assure that the scr does not "fire" and high enough for usable readings.

After the analog multiplexer is set, the last address detector is initialized, followed by a 3-millisecond wait to insure that all circuits have stabilized. The measurement then is initiated prior to applying the stimulus signal to insure that data is not lost.

Figure 32 is an oscillograph of a typical V_1 and V_8 versus time waveform for this test. V_1 is the nonfiltered output directly from the computer d/a converter. The odd stimulus frequency was selected to provide exactly 16 stairs per audio cycle so that each subsequent cycle is identical to the last. (The d/a converter pacer period is programmable

41 This test was added during the program to provide a precise current gain for rectifier positive and negative half cycles.

in finite steps.) The V_8 voltage value in figure 32 should be ignored as it includes the AEC buffer amplifier gain.

The integrator/coupling circuit and component values are such that the step response to this circuit is a double exponential in shape with a peak about 71.7 milliseconds (nominal) from stimulus inception (94.4 milliseconds worst case). A stimulus duration of 106 full cycles (about 146 milliseconds time span) was used to represent the response voltage over its usable range. The trailing edge breakpoint observed on V_8 is the result of the removal of V_1 stimulus voltage.

- SCR Firing Potential Data (Test 5)

Finding the exact SCR firing potential requires a test similar to test 4 except for a different UUT stimulus signal. The UUT input level requirement is such that the SCR actually fires under all conditions. Ten cycles at 726.7 Hz was chosen for this case[42]. The AEC circuitry and computer multiplexer is set to read V_8 versus time and data is inputted for use in determining the firing potential. The flowchart for this test is shown in figure 33 and a typical input/output waveform is shown in figure 34. V_1 in the oscillograph shows the nonfiltered output from the computer d/a converter. Note that C_{13} and C_{14} must be initialized before running this test to assure proper quiescent conditions.

- Event Sense Card Monitor

The computer event sense card also monitors test point 9 (see figures 2 and 3), the normal "fire" pulse output terminal, during all tests. The purpose of this monitor is twofold: to note if a fire pulse occurs at an inappropriate time and to check if a fire pulse actually occurs during test 5.

42 This test is very similar in requirements to that of the M732 integration time measurement. In fact, integration time can be calculated from this data if desired.

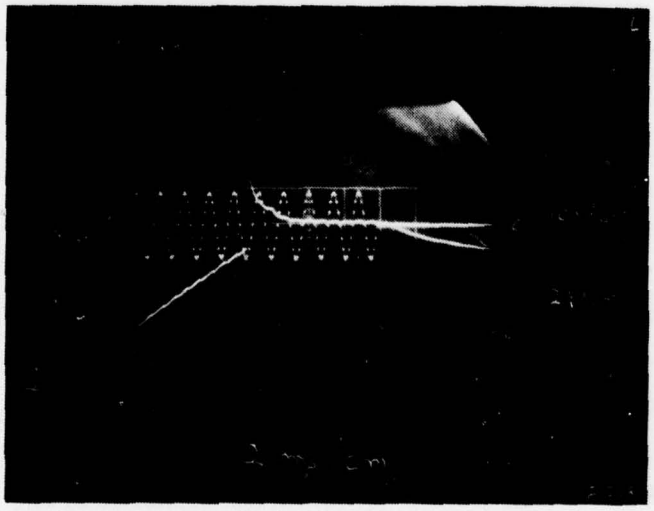

Figure 34. Typical V_1 and V_8 Vs Time Waveforms (V_{SCR})

Tests 1, 2 and 3 are conducted with C_{13}/C_{14} shunts connected to their respective capacitors. This additional loading should minimize the voltage at V_8 (the SCR gate voltage) so that the SCR does not "fire". If it does, the quick-charge circuits recharge C_{16} and reset C_{13} and C_{14} to their quiescent voltage values and the test is reinitiated. If "false" firing continues, the unit is rejected.

. Fire Pulse Monitor

The UUT fire pulse output is also monitored by the d/a converter via the high-level multiplexer. This additional d/a sensor is used to final check the test/trim sequence of the UUT with an M-wave stimulus. The test sequence is identical to test 5 except that the UUT fire pulse output is inputted to the computer instead of V_8. Data manipulation is different then for test 5 in that the differential time to the leading edge of the fire pulse is determined and HOB calculated.

Fire pulse energy could also be calculated from the computer buffer data, however, it is not needed in this case. Accuracy of this measurement ($\pm$ LSB $\pm$ pacer error) which is slightly over $\pm$ 0.012 foot at maximum read rates.

2.5.1.5 Amplifier Parameter Calculations. - The HP computer and peripherals were purchased with simultaneous i/o and calculation to minimize test time. The initial programming for amplifier testing, however, provided for simultaneous i/o without simultaneous calculations. This approach was used to expedite programming and system checkout. Once the initial system testing verified that the approach was acceptable, reprogramming to include simultaneous calculation was to be affected. It should be stressed that the basic computer hardware provides for this alternative.

. Preamplifier Rectified Average Gain Calculation (Pre- or Post-Cut

The UUT preamplifier gain calculation considered two possibilities: a rectified average gain or a discrete

fourier transform (DFT). Initially, amplifier programming was limited to the rectified average gain calculation only. The more sophisticated DFT was to be incorporated at a later time. Figure 35 sums up the steps used in programming for rectified average gain. Twenty cycles of stimulus frequency and UUT output data is alternately stored in an appropriate computer input buffer. These data plus pre-data and post-data i/o "noise" is used to provide rectified average gain. "Noise" in this case allows for possible amplifier electronics card (AEC) buffer amplifier offset voltage drift and a/d converter calibration drift. The average "noise" value is removed from V_1 and V_5 data before the appropriate gain is calculated. If both units are properly calibrated, this "noise" value is zero. The computer d/a pacer was set at an output word rate to provide precisely 16 steps per cycle of stimulus data to assure that each prefiltered cycle is an exact replica of the previous one. To accomplish this, the stimulus signal period and discrete pacer speed are inter-related and odd valued. In the present case, the stimulus frequency is 726.74419 Hz at an output pacer period of 86 microseconds.

- Thresholds and Current Generator Calculations

Measurement data from test 2a and 2b form the basis for calculating the characteristics of the rectifier. Conceptually, the a/d converter alternately looks at the input and output voltages of the rectifier (V_5 and V_6, respectively; see figure 2) over a period of time. The UUT input signal (the filtered computer d/a output) is parabolic in shape (a-positive; b-negative). UUT input filter and coupling circuitry and input amplitude and duration are such that a ramp voltage is generated at V_5 in the same time domain. A negative parabola is inputted at V_1 to provide a positive ramp at V_5 and vise versa. The V_5 ramp stimulus is of a level to exercise the rectifier transfer characteristic over its entire linear range.

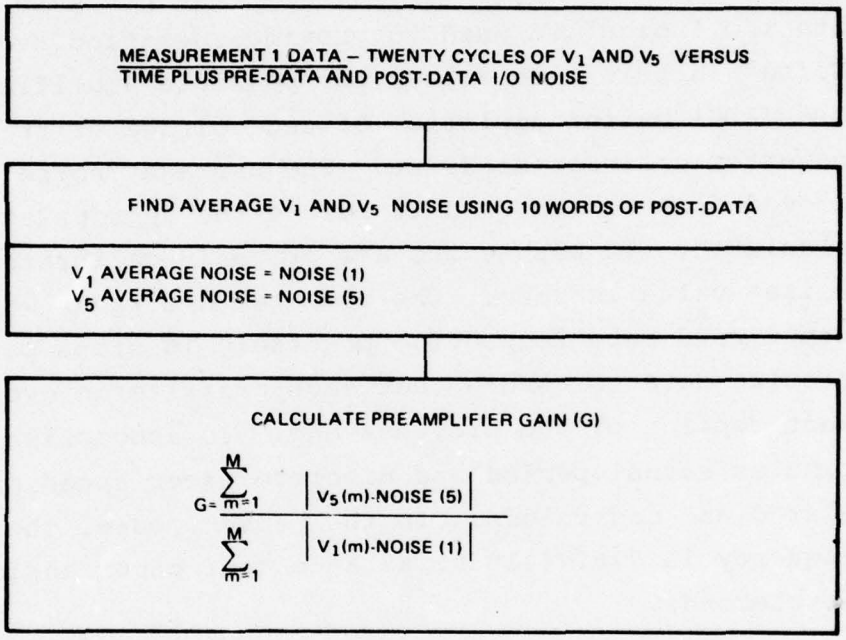

Figure 35. Preamplifier Gain Calculation

Integration and coupling capacitors (C_{14}, C_{13}) are shunted by resistors of low value (100 ohms) so that the V_6 response signal does not fire the UUT SCR (see figure 2). The high-level multiplexer alternates between V_5 and V_6 with the computer recording V_5 and V_6 versus time data during this period.

Figure 36a and b shows an idealized sketch of the raw V_5/V_6 data versus time with V_5 as a first measurement. Arbitrary time samples are noted which represent sequential data in the computer input buffer. Processing of the buffer data may be summarized as follows: 1) Modify the "raw" V_6 versus time data to provide new V_6 data points in time coincidence with V_5 using $V_6(m)=[V_6(m+1) + V_6(m-1)] /2$. The result of this processing appears in figure 36b as the circled points (O) between actual data points (x). 2) Reorganize the modified V_5/V_6 data to provide a table of V_6 versus V_5 as shown in figure 36c. 3) Piecewise linearize this curve by fitting a straight line to the linear portion of the data (figure 36c dotted line) utilizing a least mean square fit. 4) Extrapolate this linear representation to $V_6=0$ to determine a threshold, T+. 5) Repeat the process for negative half-cycle data. 6) Rescale the ordinate of figure 36c to represent the Thevenin-equivalent source voltage as shown by the equation in figure 36d. The result is a linearized transfer function approximating the rectifier characteristics. Four parameters arise from this manipulation.

- Gain for postive and negative half cycles (G+ and G-)
- Thresholds for positive and negative half cycles (T+ and T-)

Several areas of potential error occur using this simplified representation which are discussed in more detail in a subsequent paragraph.

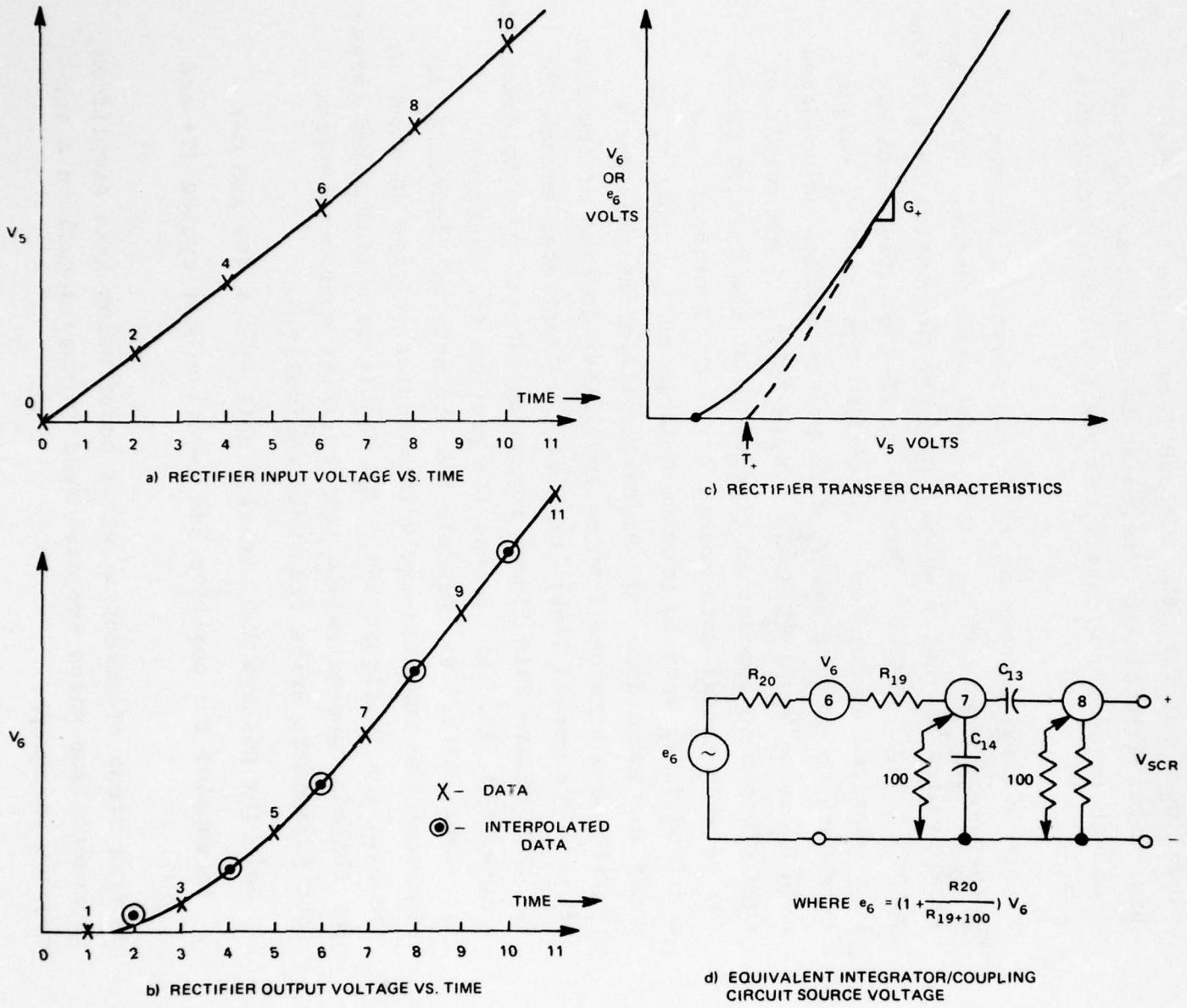

Figure 36. Rectifier Transfer Function Graphs

. Output Integrator and Coupling-Circuit Impulse Response

It can be readily shown that the step response of the integrator/coupling circuit between test points 6 and 8 (see figure 2) can be represented mathematically by the double exponential curve shown as equation (1) and in the insert in figure 37

$$e8(t) = A\ [e^{-p_1 t} - e^{-p_2 t}]\ \text{volts} \qquad (1)$$

The values of p_1 and p_2, of course, depend upon circuit component values. Table VIII summarizes nominal and extreme values of p_1 and p_2 for the range of component values presently used.

Figure 37 is a flowchart of the major steps in calculating p_1 p_2 and A. Basically, it is an iterative process where initially P_1, and A values are assumed and P_2 and a new A are calculated. Preliminary results are shown in table IX where a sample amplifier board was stimulated periodically and P_1, P_2 and A were calculated several times after an initial UUT warmup period.

Table VIII. Integrator/Coupling-Circuit Step-Response Constants p_1 and p_2 Values (1/second)

Constant	Maximum	Nominal	Minimum
p_1	4.219	3.038	2.3014
p_2	53.38	38.432	29.115

The unit impulse response is the nomalized derivative of equation (1)

$$u(t) = \frac{e_8 t}{A} = [-p_1 e^{-p_1 t} + p_2 e^{-p_2 t}] \qquad (2)$$

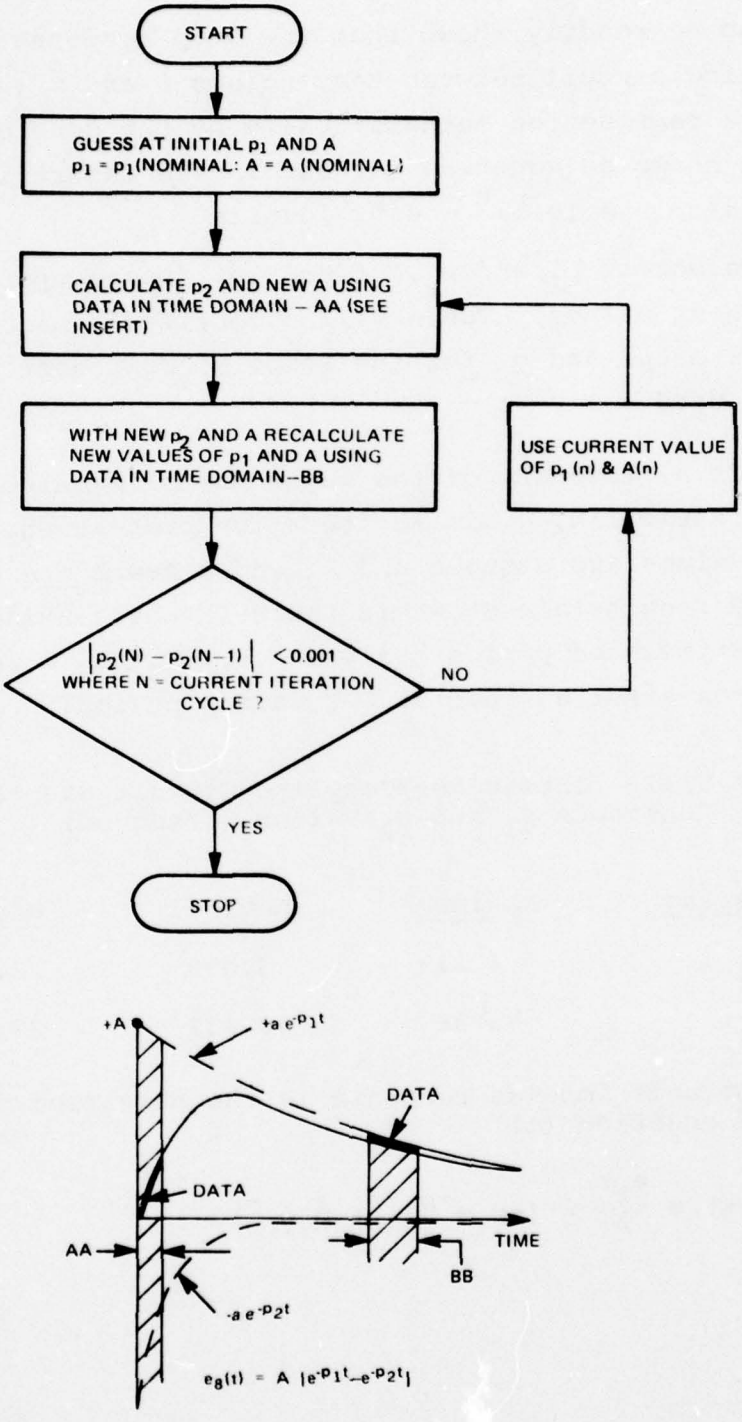

Figure 37. Step-Response Calculation Flow Graph (Simplified)

Table IX. Test 4 Step-Response Properties for a Typical UUT

Trial	A (Volts)	P_1 (1/Second)	P_2 (1/Second)
1	0.3468	2.7357	38.6216
2	0.3463	2.7359	38.6832
3	0.3461	2.7182	38.7437
4	0.3458	2.7182	38.7255
5	0.3456	2.7172	38.7255
6	0.3453	2.7090	38.7942

About 15 seconds elapsed between each iteration. At first, this appears alarming since it is many orders of magnitude above the desired 1.2-second total test time available. The times involved, however, include TTY printout, the time necessary to run through all the tests shown in table VII and two 3-second delays for recharging C_{16} between tests[43].

An overall error analysis was not accomplished at the time since the calculated HOB depended upon the results of the convolution integral of a weighted M-wave with the unit impulse response of this output filter.

This integral was derived and a table of values assembled just before contract termination. (See paragraph 2.5.1.6 for more details on the effect of M-wave weighting and the convolution integral evaluation.)

- SCR Firing Voltage

  The test data from test 5 is used to determine the SCR firing potential which can vary ±13 percent from its nominal value. An oscillograph waveform of V_1 and V_8 versus time is shown in

43 Quick-charge circuits were not available at this time.

figure 34 where 10 cycles of 726.74419 Hz is used to stimulate the UUT at an amplitude high enough to fire the SCR as quickly as possible. The program to search out $V_8=V_{scr}$ looks at the slope of the signal (dV_8/dt) starting at a data point corresponding to about 300 millivolts from t=0 (V_{scr}>400 millivolts). The program selects the lower data point as the proper value when that slope exceeds 300 millivolts and is positive within a 22.2-microsecond period (45,000 words/second). The maximum pre-fire slope attainable is about 2.88 millivolts/count at a 45,000 words/second read rate[44]. Placing about a 300 millivolts/count minimum positive slope requirement assures that the breakpoint is found to an accuracy of from 1.11 millivolts/count to 2.88 millivolts/count worst case. The 1.11 millivolt/count slope is associated with V_{scr} = 0.4 volt or an error of -0.28 percent. The 2.88 millivolts/count slope is associated with a 0.52 volt V_{scr}. The worst-case error here is -0.55 percent, which is a little high. Nominal error is 1.702 millivolts/count (-0.37 percent). These values assure that the (N+1)'st data point sits right on the peak of V_8 and the Nth data point is 22.2 microseconds before it. These numbers will reduce by a factor of 2 if the nominal center is used instead. Overall nominal error in V_{scr} should be (-0.185 percent).

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44 Worst case integration time is 4 milliseconds with an SCR firing potential of 0.52 volt. The slope becomes (0.52/4) = 0.130 V/ms; multiply this by 22.2 μs yields 2.88 mV/count.

2.5.1.6 Amplifier Programming Considerations.- The following procedure is used to calculate the required gain of the amplifier (UUT) for a desired HOB. The technique assumes linearity. It measures pre-cut UUT properties, adjusts the UUT input stage AC gain to 95 percent of the desired value, checks to determine if the new gain is within adequate limits and then increases the gain to its final value. A key element in this process is the determination of the response of the UUT rectifier output integrator and coupling circuit to the theoretical stimulus M-wave. This determination is discussed first. A straightforward gain calculation is greatly complicated by the fact that the input to this filter is a nonlinear, full wave rectifier with each section having a different gain and threshold. Furthermore, even after the output of the full wave rectifier has been derived, the output of the filter itself is calculated using a complex convolution integral.

In order to achieve a realistic execution time for this calculation, a table "look-up" scheme is used in place of the real-time calculation. The form of the table is shown in table X. It is a two-dimensional array, the vertical dimension being pole values p_1 and p_2. More correctly, it is the rescaled pole values (integer numbers) versus the ratio of rectifier threshold (T) to M-wave peak voltage at t=0, $V_5(0)$. The actual value of the entries for both dimensions are as shown in table X. This table shows only part of the overall table considered for use. The convolution integral is found separately, off-line, for each pole and threshold combination. The quantities of pole value, threshold and gain to point 5 are used to determine the pole interpolation factors and threshold interpolation factors. The values of the integral are then found using linear interpolation in the two-dimensional convolution integral table. For a given set of measured UUT properties, the SCR gate voltage is calculated and compared to the SCR gate voltage to "fire" (Vscr). From this calculation, a new ac gain is determined which provides Vscr at the proper HOB. The laser is commanded to cut R_9 (the redesigned

Table X. Normalized Convolution Integral Table (Partial)

$T/\lvert V_5(0)\rvert$	Convolution Integral Values					
P_1	0	1	2	6	7	8.0
2.0	-1.2472	-0.63136	-0.31576	-0.010581	-1.001682	0
2.5	-1.4890	-0.76827	-0.38908	-0.013200	-0.021000	0
3.0	-1.7095	-0.89807	-0.46032	-0.015807	-0.002518	0
3.5	-1.9112	-1.0213	-0.52955	-0.018403	-0.002935	0
4.0	-2.0963	-1.1384	-0.59686	-0.020989	-0.003351	0
4.5	-2.2667	-1.2499	-0.66231	-0.023564	-0.003766	0
5.0	-2.4241	-1.3562	-0.72596	-0.026128	-0.004181	0

$T/\lvert V_5(0)\rvert$	Convolution Integral Values					
P_2	0	1	2	6	7	8
29	5.2027	3.7423	2.5144	0.13771	0.023225	0
30	5.2528	3.7908	2.5572	0.14191	0.023983	0
31	5.3010	3.8374	2.5987	0.14607	0.024739	0
⋮	⋮	⋮	⋮	⋮	⋮	
40	5.6637	4.1899	2.9166	0.18212	0.031418	0
41	5.6976	4.2230	2.9469	0.18597	0.032147	0
42	5.7304	4.2550	2.9762	0.18979	0.032873	0
⋮	⋮	⋮	⋮	⋮	⋮	
52	6.0112	4.5294	3.2298	0.22642	0.039997	0
53	6.0353	4.5530	3.2518	0.22993	0.040696	0
54	6.0587	4.5760	3.2732	0.23342	0.041392	0

thick-film resistor in the ac gain stage) to provide the desired gain. Final check and calculation of HOB are made and the procedure is complete. It should be noted here that the above procedure is performed at the UUT mid-band frequency. Since only one adjustment is available (that of R_9), HOB is set at this frequency. To calculate band edge HOB's it is necessary to expand the UUT measurements to include the impulse response of the UUT input filter[45] between points (1) and (2) (see figure 2) and the interstage coupling circuit between points (3) and (5). This added programming effort was to be accomplished after the basic mid-band measurements were successfully completed.

45 The form of this filter is identical to the rectifier output integrator/coupling circuit. Only the values are different.

. Post-Measurement Calculation

The fundamental UUT measurements needed for HOB calculations and gain adjustments are:

- First Stage AC Gain
- Gains and Thresholds of the Full Wave Rectifier
- Integrator/Coupling Circuit Equivalent Source/Impedance
- Output Integrator/Coupling Circuit Unit Impulse-Response Properties
- SCR "Firing" Potential

The integrator/coupling circuit source impedance is needed only to determine the rectifier large-signal transfer gain (e_6/V_5) for positive and negative half cycles.

Tables XI and XII show the step-by-step procedure for calculation and adjustment of amplifier UUT's excluding B+ turn-on or final M-wave retest and serialization.

. HOB Error Considerations

A full-scale UUT error analysis was not initiated during the program simply because the problems to be addressed and resulting solutions had not been fully determined or completely evaluated until late in the program. An example of this is the evaluation of the convolution integral. Numerical techniques utilizing the computer (off-line) were mandated since a closed form of this integral does not exist. Computation of the full convolution integral table, using the available HP computer, took several weeks. Re-running this computation several times using different rectifier analytic representations made it impossible to provide a thorough analysis in the allowable time span and budget. Several general comments can be made, however, which relate to errors in the calculated HOB. These are summarized below.

a) A/D and d/a converters having excellent LSB resolution and accuracy were purchased. Isolation and buffer amplifiers assure the largest signal available to the a/d converter to

Table XI. UUT Pre-Cut Calculations

Item	UUT Properties	Data From Measurement*	Desired Property
1	Calculate $Gac=V_5/V_1$ (Rectified average or DFT.)**	1	Input Stage AC Gain, Gac.
2	Calculate Values of R_{19} & R_{20}.	3	R_{19}, R_{20}.
3	Assemble Rectifier V_6 vs V_5 Data for Positive and Negative Half Cycles.	2a, b	V_6 vs V_5.
4	Rescale V_6 vs V_5 Ordinate to Provide e_6 vs V_5 Where $e_6 = \left[1 + \frac{R_{20}}{R_{19} + 100}\right]$ V6.	Items 2 & 3	e_6*** vs V_5.
5	Piecewise Linearize e_6 vs V_5 Using Least Mean Square Fit to Large Signal Data.	Item 4	e_6 vs V_5.
6	Determine Rectifier Gains and Thresholds for Positive and Negative Half Cycles.	Item 5	G+, T+, G-, T-.
7	Find: Integrator/Coupling Circuit Unit Impulse Response Properties (p_1, p_2).	4	p_1, p_2.
8	Find: SCR Firing Potential.	5	Vscr

Notes: *Measurement list in table VII.

**Presently use rectified average gain.

***e_6 is the Thevenin equivalent source voltage of integrator/coupling circuit (rectifier equivalent output voltage). Output impedance is R_{20}.

Table XII. Calculations to Determine HOB

Step	Description	Data from Table XI
1	Given: Pre-cut R_9, Gac	Item 1.
2	Find: $\lvert V_5(0) \rvert$ from Theoretical M-Wave Input @ t=0*.	$\left[V_1(0)\right]$ X Gac = $\lvert V_5(0) \rvert$.
3	Given: Rectifier Thresholds (T_+, T_-).	Item 6.
4	Find: $\frac{T+}{\lvert V_5(0) \rvert}$ & $\frac{T-}{\lvert V_5(0) \rvert}$	$\frac{T+}{\lvert V_5(0) \rvert}$ & $\frac{T-}{\lvert V_5(0) \rvert}$
5	Given: Integrator/Coupling Circuit Unit Impulse Properties (p_1, p_2).	Item 7.
6	Find: $V_8(t_{HOB}$**); From Convolution Integral Table (4 Parts). Linearly Interpolate Between Primary Points.	Step 4 and 5 Results Plus Item 6, G+ & G-.
7	If: A) $V_8(t_{HOB}) > Vscr$	a) Calculate HOB, Print, Reject if Out of Specifications.
	B) $V_8(t_{HOB}) = Vscr$	b) Calculate HOB, Print, "Pass" if in Specifications.
	C) $V_8(t_{HOB}) < Vscr$	c) Go to Step 8.
8	Find: Required AC Gain to Provide $V_8(t_{HOB}) = Vscr$ (AC Gain Must Be Increased by $Vscr/V_8(t_{HOB})$.	$\frac{GAC\ (Required)}{Gac(Measured)} = \frac{Vscr}{V_8(t_{HOB})}$
9	Calculate: $V_5(0)$ Using Gac(Required).	$V_5(0) = \lvert V_1(0) \rvert$ X Gac (Required)
10	Set V_5 Voltage Comparator Reference Input Voltage to 0.95 X $\lvert V_5(0) \rvert$.	0.95 X $\lvert V_5(0) \rvert$

Table XII. Calculations to Determine HOB (Cont)

Step	Description	Data from Table XI
11	Command Laser to Cut R_9 & Stop at $0.95 \times \lvert V_5(0) \rvert$.	Laser Cut
12	Command Laser to "Shadow" Cut R_9 the Remaining 5 Percent Increase in Gain. (To Assure that Adequate Gain Resolution Is Maintained).	Laser "Shadow" Cut.
13	Remeasure Gac. Compare to Gac (Required). Calculate Final HOB & Record.	Calculate Final HOB.

Notes: *Theoretical input M-wave at V1 is,

$$V1(t) = \left[\frac{V}{(1-\frac{t}{T})}\right] SIN(W_d t)$$

where T=time from a specified maximum altitude to the ground.

Wd = 2 π fd.

fd = doppler offset frequency.

** t_{HOB} = Time necessary for the fuze to reach its desired altitude.

minimize LSB error. These buffers were designed to provide accurate, stable gains. A means of checking buffer amplifier gain in real time was incorporated to verify their stability.

b) Wherever possible, UUT gain measurements were made by viewing both input and output signals in very close time proximity.

c) Warm-up and specific measurement times after B+ turn-on are kept the same during test to provide repeatability of measurements.

d) Computational errors are kept negligible by using double precision techniques.

The following more specific comments can be made regarding the individual measurements described in tables XI and XII.

a) A rectified average AC gain is initially being used in test 1. Errors, of course, result from cable "hum" pickup and the fact that a finite time stimulus is used. The more accurate calculation would be to utilize a DFT procedure which extracts the fundamental component of the resultant output signal. This alternate was planned as system testing progressed.

b) Calculation of R19 and R20 values incur errors as a result of the shunting effect of the 100-ohm test resistor across R20. These shunt resistors, although accurate to 0.1% were to be included in the calculations. The effects of R20 on voltage and current calculations can be minimized by making the 100-ohm loading resistor even smaller and using larger buffer amplifier gains to offset the resulting low-level signal voltages. The resulting trade-off is then maximizing accuracy while maintaining a good S/N ratio.

As it stands the design provides R19 and R20 values to an accuracy of about 0.1 percent.

c) Calculations 3 and 4 are self-explanatory when considering the above.

d) Calculations 5,6 and 7 provide the bulk of the expected system error. These tests are summarized below.

e) The determination of SCR firing potential produces potential errors in several areas. The accuracy of the basic measurement is excellent in that stable buffer amplifiers are utilized to reduce LSB error to negligible proportions. The inaccuracy of the a/d converter is about 0.1 percent. Here again, once this accuracy is divided by the buffer amplifier gains, errors introduced from this source become negligible. The method of manipulating the data to determine Vscr, however, produces a finite error which varies depending upon the "integration time[46]" of the UUT.

The data processing needed to find Vscr looks at the slope of $V_8(t)$ when the UUT is stimulated with a high-level sinusoid. The pre-fire $V_8(t)$ slope varies from 50 millivolts/word to 130 millivolts/word at 45,000 words/second (2.22 microseconds between samples). If a sample happens to fall right at the peak of the SCB firing voltage (see figure 34), the voltage in memory prior to this peak is Vscr. An error in Vscr results since the pre-fire slope is finite. Table XIII summarizes expected errors for different conditions verifying accuracy in voltage measurement.

"Worst case" assumes that the (N+1) sample falls right at V_8 peak. The Nth sample is then labeled Vscr. The "least" error assumes the Nth sample falls at the required point. "Mean" is halfway between.

46 A standard M732 amplifier-board measurement is associated with the rectifier output integrator/coupling ciruit.

Table XIII. Vscr Test-Error Analysis

UUT Integration Time	Percentage Error		
	Worst Case	Mean	Least
Minimum	0.55	0.275	0
Nominal	0.37	0.185	0
Maximum	0.278	0.139	0

Doubling the sampling rate, of course, would half these values. On the whole, if it is assumed that nominal UUT's are tested, about 0.185 percent can be expected as an overall error (possibly slightly more if a/d converter and buffer amplifier accuracy are considered). The likelihood of having a "worst case", minimum "integration time" unit is small.

f) Errors introduced by finite S/N ratios at the d/a input have been minimized. The effect of noise (hum) on the a/d input cables is still unresolved.

g) The areas of greatest concern in system accuracy lie in the piecewise linearization of the rectifier transfer characteristics. The curve of e_6 versus V_5 shown in figure 36c is representative of the situation. This curve is actually only a small portion of the total e_6 vs V_5 curve. It may be significant, however, because a major portion of the time a normal M-wave occurs is in this nonlinear region. Only when the fuze nears the ground does the level of V_5 increase to the more linear portion of the curve. It is understood that the integration levels at the higher altitudes are small, however, the lack of a large voltage input is offset by the total time at these voltages.

Piecewise linearizing of the rectifier transfer characteristic may cause large errors, therefore. Using alternate analytic representations, however, should minimize the problem. Two possibilities are:

- Piecewise linearize with two or more break points to represent the e_6 vs V_5 curve more accurately.
- Represent the e_6 vs V_5 curve by a power series expansion (or other) starting at the actual threshold voltage (dot on abscissa in figure 36c).

Both approaches would probably complicate the calculation of the convolution integral table.

Other areas where linearization, or the lack of it, causes errors are:

- Linearly interpolating V_6 data to obtain data points that are time coincident with V_5 samples. (See figure 36b).
- Linearly interpolating the convolution integral table to obtain V_8 values at t_{HOB}.
- Some UUT's are not precisely linear for high-level signals.
- If the M-wave input level attains a value where the rectifier saturates. This is improbable for pre-cut R_9 levels; post-cut levels, however, are another story.

Interpolation errors between points can be minimized by increasing the data rate to expand the convolution integral table or analytically representing the convolution-integral-table data.

Table XIV and XV summarize some of the interpolation errors in the convolution integral table shown in table X.

Table XIV shows the error by interpolating p_1 in 0.5 steps (i.e., 2.0 to 3.0 for 2.5) and p_2 in unit steps (i.e., 29 to 31 for 30). In either case, the interpolated value is compared to the computer-calculated value and the percent difference is noted. Table XV shows the error by interpolating $\left[(T/|V_5(0)|\right]$ at constant p_1 or p_2.

Note that interpolation errors vary from unacceptable to negligible depending upon location in the table array. The initial table envisioned for computer memory tabulates p_1's in 0.1 steps from 2.0 to 5.0 and $\left[T/|V_5(0)|\right]$ steps of 0.1. P_2 ranges from 29 to 55 in steps of 2.0. A further differential in $\left[T/|V_5(0)|\right.$ may be needed to resolve high values of this threshold ratio.

Table array size is 31 X 81 = 2511 elements for $2.0 \leq p_1 \leq 5.0$ in steps of 0.1 and 13 X 81 = 1031 elements for $29 \leq p_2 < 55$ in steps of 2.0. In both instances $T/|V_5|$ values are in 0.1 steps. This amounts to a total of slightly over 3500 memory elements.

Table XIV. Linear Interpolation Error Of P_1 & P_2 (Percent) Using Table X Data

p_1 \ T/ $\lvert V_5(0) \rvert$	0	1	2	6	7	8
2.5	+0.72*	+0.46	+0.27	+0.045	0	0
3.5	+0.43	+0.30	+0.18	+0.028	+0.017	0
4.5	+0.29	+0.21	+0.14	+0.023	0	0
p_2						
30	-0.018	-0.025	-0.025	-0.014	-0.004	0
41	-0.010**	-0.013	-0.017	-0.008	-0.005	0
53	-0.006	-0.007	-0.009	-0.004	-0.004	0

*+0.03 percent by interpolating from p_1 = 2.4 to 2.6

**-0.04 percent by interpolating between p_2 = 39 and 45.

Table XV. Linear Interpolation Error of $\left[T/ \lvert V_5(0) \rvert\right]$ - (Percent) Using Table X Data

p_1 \ T/ $\lvert V_5(0) \rvert$	1	7
2.5	-22	-214
3.5	-95	-214
4.5	-172	-213
p_2		
30	+3.1	-196
41	+2.4	-189
53	+2.0	-182

Trade-off is, therefore, resolution versus memory availability.

Other possible approaches to save memory and retain accuracy are:

. Tailor storage space by varying resolution depending upon array location.

. Curve fit data and calculate integral values.

2.5.1.7 Convolution Integral Considerations.- The response of the rectifier output integrator/coupling circuit (filter) can be analytically determined by convolving the unit impulse response of the filter [u(t)] with the weighted M-wave input signal $V_6(t)$ as shown in equation (3).

$$V_8(t) = V_6(t) * u(t) \tag{3}$$

where

$$V_6(t) = [\text{SIN}\ [\text{COS}^{-1}(Ax)] - (Ax)\ \ \text{COS}^{-1}(Ax)]\ \frac{1}{x} \tag{4}$$

and

$$u(t) = -p_1\ e^{-p_1 t} + p_2 e^{-p_2 t} \tag{5}$$

$$A = [T/|V_5(0)|] \tag{6}$$

$$X = (1 - \frac{t}{T}) \tag{7}$$

$V_6(t)$ represents the dc term of the full wave rectifier output voltage versus time, assuming a constant sinusoidal input. The term results from finite rectifier threshold. This representation assumes the following:

- That an infinitely long sinusoid is inputted to the rectifier and that it is of constant amplitude[47].
- That the integrator capacitor (C_{14}) provides an infinitely low inpedance to all ac terms eliminating them from being transmitted to the filter output terminals. The bracketted term in equation (4) was derived by taking the fourier transform of a half-wave, rectified sinusoidal signal with a finite, rectifier threshold level. (This term becomes (1) if the rectifier threshold is zero volts.) The term

47 The normal M-wave excitation has a relatively slowly varying amplitude in the realm of interest.

$1/x = 1/(1-t/T)$ is the envelope of an idealized M-wave. The remaining quantities are defined as follows:

- t = Time (seconds)
- T = Rectifier threshold for positive (T+) or negative (T-) half cycles (volts).
- $V_5(0)$ = Magnitude of the rectifier input M-wave at t=0 (volts). T = Time for the fuze to reach the ground from a maximum altitude (seconds).
- p_1 and p_2 = Constants derived from the step-response measurements made on this filter (1/second).

Slight errors in table calculation may be introduced as a result of the finite length stimulus and the second assumption. (Note the ripple on $V_8(t)$ in the photograph in figure 34.) It was felt, however, that errors of this nature are small in comparison to the errors introduced by linearization of the rectifier-transfer function. Ultimately, this too can be accounted for.

Figure 38 shows an idealized sketch of the input signal shape ($V_6(t)$ for various ratios of $\left[A=T/|V_5(0)|\right]$. A=0 represents a rectifier with T=0 volts. Note that it is an idealized M-wave. In the case where A=1; $\left[T=|V_5(0)|\right]$, the curvature departs completely fron an M-wave. Larger values of A enhance this degradation from the original idealized driving function. It is quite evident from this, that the SCR gate voltage (and, therefore, convolution integral values) are strongly dependent upon the input signal wave shape.

The terms in the convolution integral table (table X) reflect these large variations. Note that the values for A range from 0 to 8 and that its values for A=8 are zero. This upper limit represents a threshold whose level equals the peak ac M-wave voltage at t=0 at the desired HOB. In effect, $|V_5(0)|$ equals T at the desired HOB.

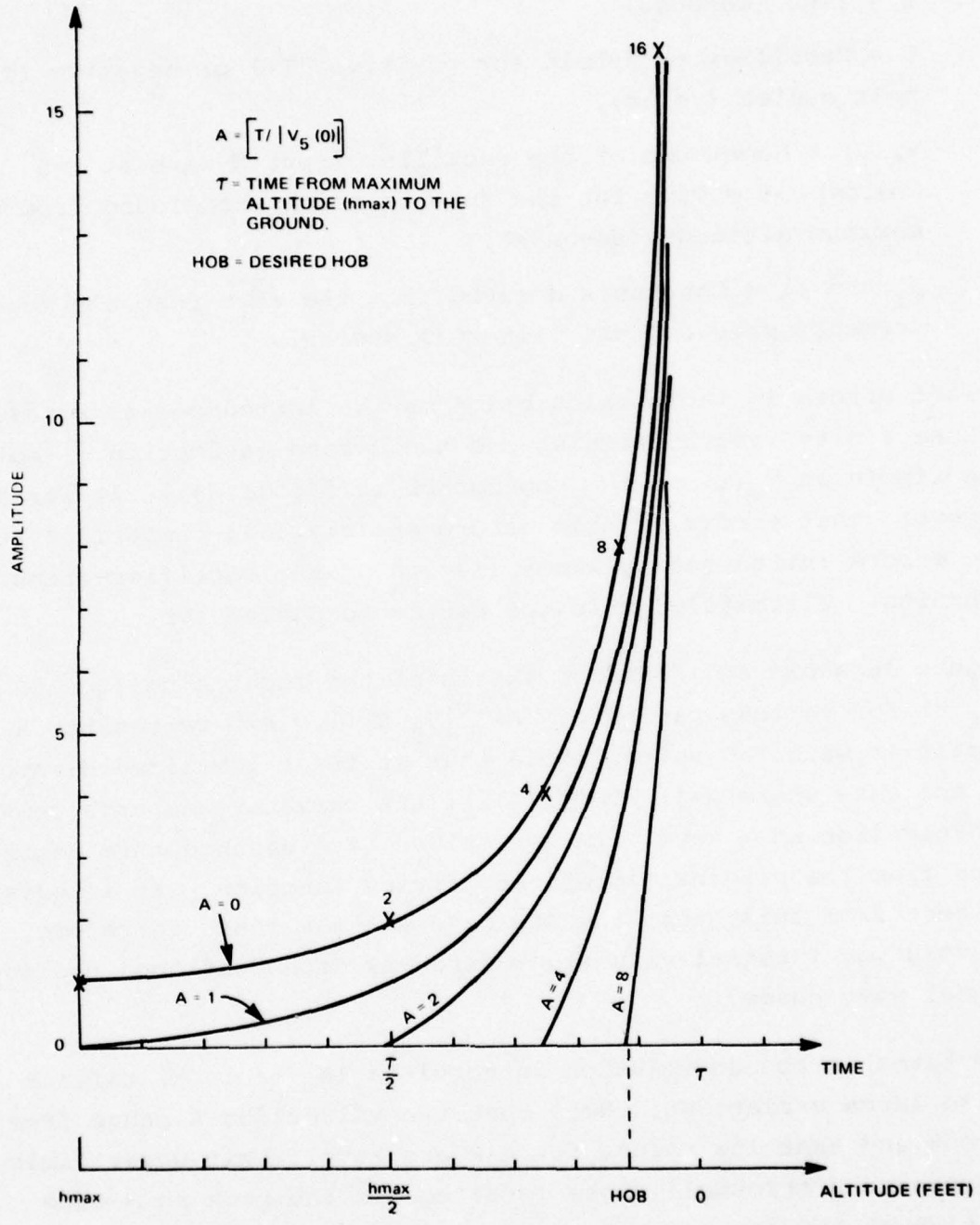

Figure 38. Integrator/Coupling Circuit Stimulus Waveforms

Measurements on sample amplifier UUT's indicate that $|V_5(0)|$ ranges near the rectifier threshold level after the UUT's have been tuned[48]. The above comments point out the need for analytically representing the rectifier transfer characteristic as accurately as possible in order to minimize HOB error. The piecewise linear approach was used as a beginning so that system testing could begin as soon as possible. The alternative e_6 versus V_5 representations described above should reduce these errors considerably.

2.5.1.8 Amplifier Tester Summary. - A system was designed and fabricated to dynamically test fundamental properties of modified M732 amplifier assemblies, calculate HOB and automatically laser trim these units to tight tolerances.

The goals of the program required that a $\pm$ 0.5 percent tolerance be placed on HOB at average test and tune rates of 3000 units/hour excluding mechanical indexing.

The engineering effort ended just prior to system testing the amplifier tester segment of the program. It was felt that the design would ultimately approach these goals.

Sufficient data and experience were accumulated to indicate that considerable improvement in accuracy and time was possible. Three thousand modified test amplifiers were constructed and functionally tested for system check out. Basic measurement and calculation techniques may be applicable to other assemblies with appropriate modifications.

2.5.2 Oscillator Tester Measurements

Oscillator testing and trimming is considerably simpler to accomplish than testing and trimming amplifiers. The results also

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48 Some may be below or above the threshold depending upon rectifier gains. Pre-cut $V_5(0)$ is definitely smaller than T.

are more accurate[49] in that a simple direct measurement is made of the desired property, sensitivity, a DFT is performed and results are recorded. The amplifier UUT's required the measurement or estimation of several properties along with a calculation of HOB based on approximations relating to the amplifier board rectifier circuitry. The main problems associated with oscillator UUT's are in the area of differential capacitance value and the ability to obtain the capacitance resolution desired to fall within the ±0.5 percent requirement. The technique incorporated[50] utilizes a set of standard oscillators to "calibrate" the rf modulator prior to operational tests. This "calibration" procedure is designed to set the rf modulator loop gain to a very precise value (LSB is 0.014 dB) just prior to test and after 5 seconds warmup. The result of this calibration phase is a table in computer memory that lists standard oscillator rf frequencies and modulator loop gains to set the standard oscillator sensitivities to their assigned values[51].

The following paragraphs present the preliminary flowcharts for oscillator testing.

The principle differential capacitance-sensitivity calculation subroutine (NLM-21) was completed and checked using production M732 fuzes. A description of this program and some of the results appear in the Fourth[50] and Sixth[52] Quarterly Reports.

2.5.2.1 RF Modulator Calibration Program.- Figure 39 shows a simplified flowchart of the rf modulator calibration program. Its purpose is to assemble a table of rf frequency (fo) versus modulator loop gain (ratio) at specified frequencies using standard

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49 The ±0.5 percent requirement is possible. Test time looks promising.

50 See the Fourth Quarterly Report, "Production Measurement of Fuze Components under Dynamic Stress", 11 February 77 to 10 May 77, Contract No. DAAB07-76-C-0032, Paragraphs 2.5 and 2.9 for more details.

51 Assigned based on free space "pole" test data.

52 Sixth Quarterly Report, "Production Measurement of Fuze Components under Dynamic Stress," 11 August 77 to 10 November 1977, Contract No. DAAB07-76-C-0032, Appendix A. NLM-21 flowchart appears as figure 42.

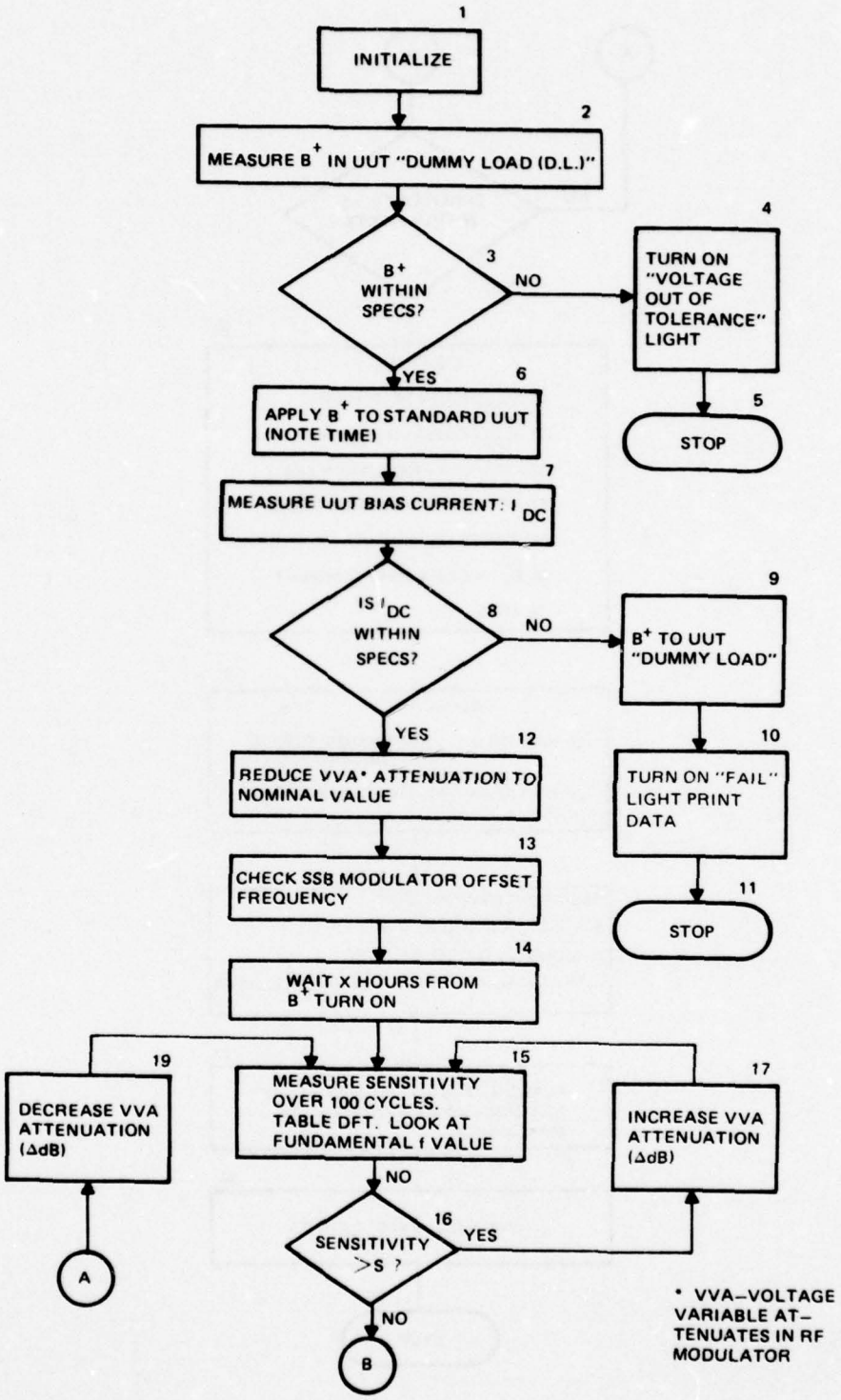

Figure 39. Modulator Calibration Flowchart (Sheet 1 of 2)

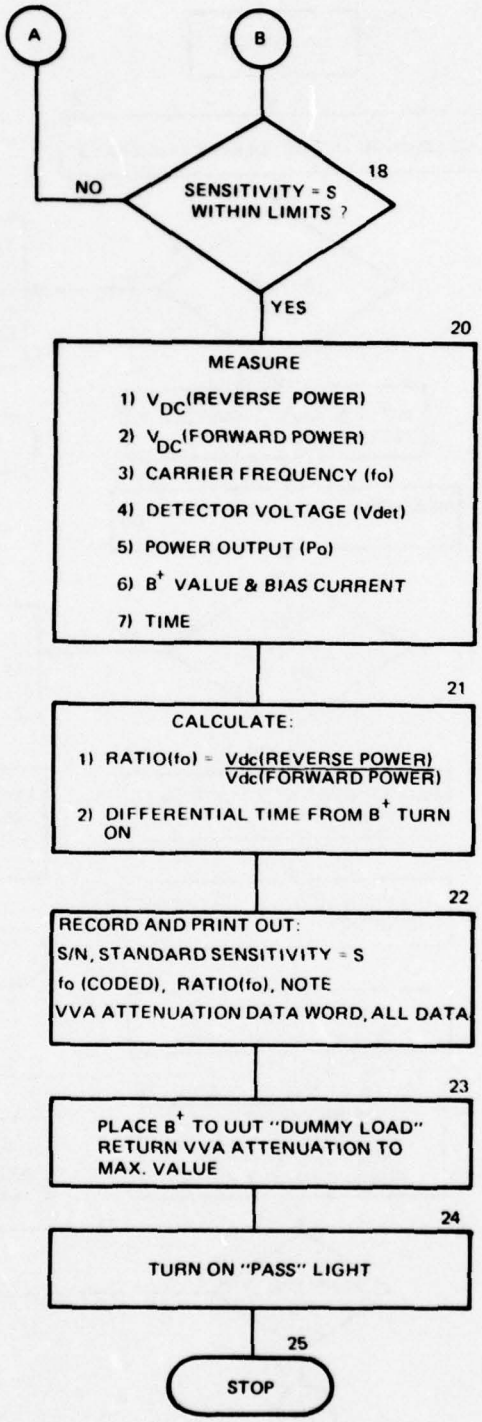

Figure 39. Modulator Calibration Flowchart (Sheet 2 of 2)

test oscillators. This data is ultimately used in the operating program to set the rf modulator loop gain at specific values depending upon UUT operating frequency. The flowchart is self-explanatory. Individual blocks are numbered in the upper right corner to simplify further explanation.

- Initialization (Block 1) - Initialization consists of the following items:

  - Set all analog buffer gains and multiplexer switches to proper values or position.
  - Initialize computer buffers and flags as required.
  - Insert via terminal the following information:

    a) "Standard" S/N
    b) Assigned sensitivity (S) from "pole" test data.
    c) Warm-up time (x)
    d) Other "pole" test data.

  "Warm-up" time depends upon the "pole" test warm-up period. Sufficient time should be allowed for the standard fuzes to stabilize electrical properties.

- SSB Offset Frequency (Block 13) - A test-signal voltage output is available at the SSB modulator through which the computer can check modulator offset frequency. The signal level is nearly 10 volts with an excellent S/N ratio that allows for an accurate measurement of this quantity.

- Sensitivity Measurement (Block 15) - The 100-cycle sample is arbitrary.

- Measurement (Block 20) - Measurements are made for all M732 production oscillator properties along with the rf modulator forward- and reverse-power measurements. These properties are not used, but are recorded as added assurance of standard oscillator operation. The data required for use in the main program is ratio(fo), fo and the VVA data word to set the attenuation close to the desired value during the operating-program calibration phase.

2.5.2.2 Oscillator Main Tuning Program. The main tuning flowchart is shown in figure 40. As in the modulator calibration flowchart (figure 39), blocks are consecutively numbered to facilitate the following descriptions.

. Initialization (Block 2) - Similar to the amplifier initialization program described in paragraph 2.5.1.2 except that oscillator parameter data is entered.

  The remaining blocks are self-explanatory with the exception of block 17.

. Test and Trim Cycles (Block 17 and Figure 42) - Measurement of sensitivity is made during this subroutine which includes DFT's after each "raw" data measurement to extract the fundamental output frequency data (true sensitivity). The reason for this approach is to minimize the effect of rf modulator spurious outputs generated in its single sideband modulator (SSBM-block 13 of figure 21). The SSBM has all spurious signals down a minimum of 25 dB below the desired upper sideband output. This value is still insufficient to eliminate the UUT detector from "seeing" these spurious signals. Additional attenuation is provided at (2fd) and higher frequencies in the "signal separate and scale" circuitry (block 1 of figure 21) to remove these residual spurious outputs. The DFT calculation provides "digital" filtering as an added precaution. The DFT or filter may have been eliminated during system testing. The cyclical test/tune sequence shown in figure 42 should have sensitivity measurements made at specific times after B+ turn-on. This is shown for the first measurement, however, it is not shown for the remaining measurements. Modifications to the program were to be incorporated to remedy this problem, however, they were not included at contract termination. The need for timing results from UUT drift after B+ turn-on. Figures 41 and 42 expand the real-time modulator

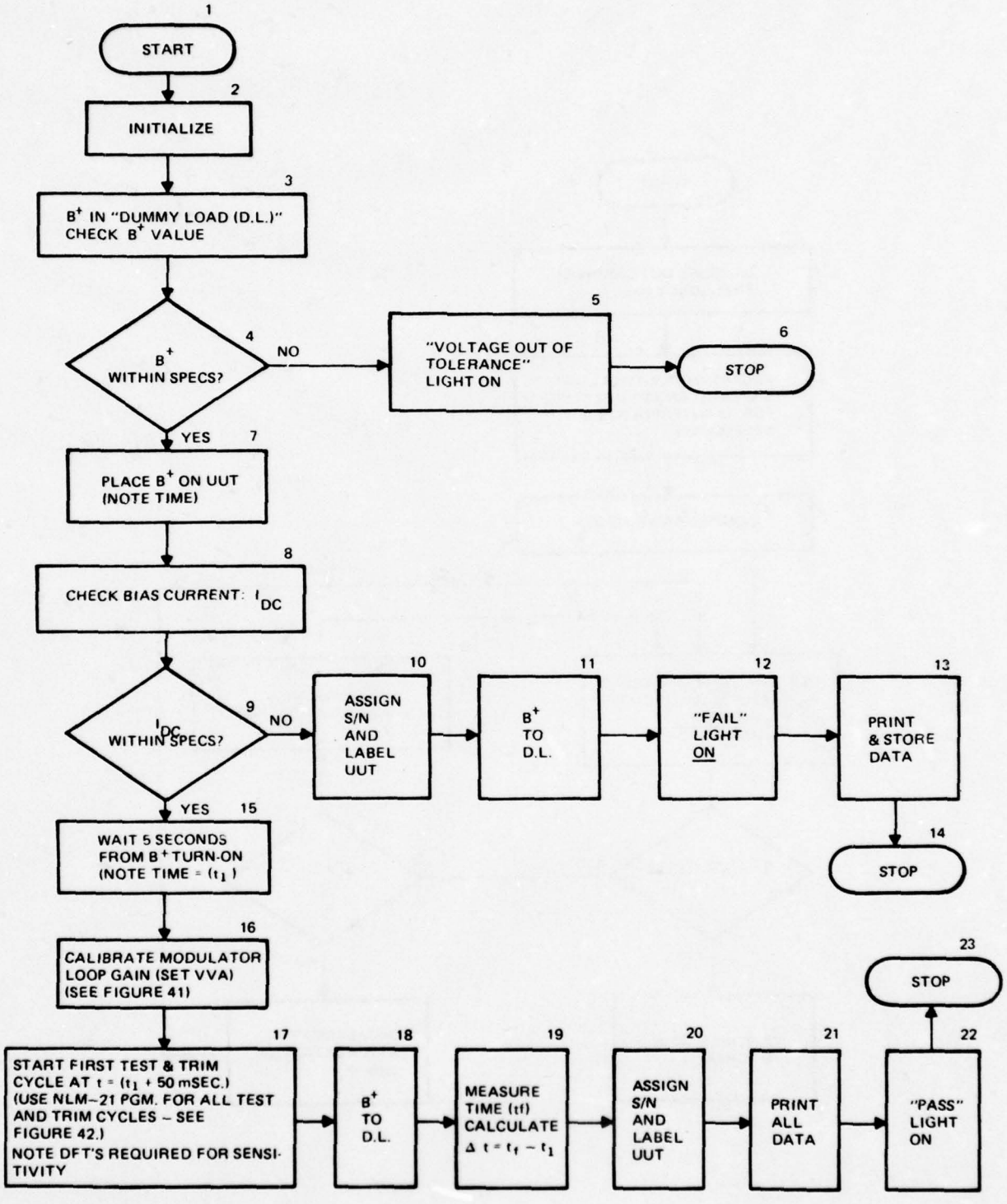

Figure 40. Main Oscillator Test/Tune Flowchart

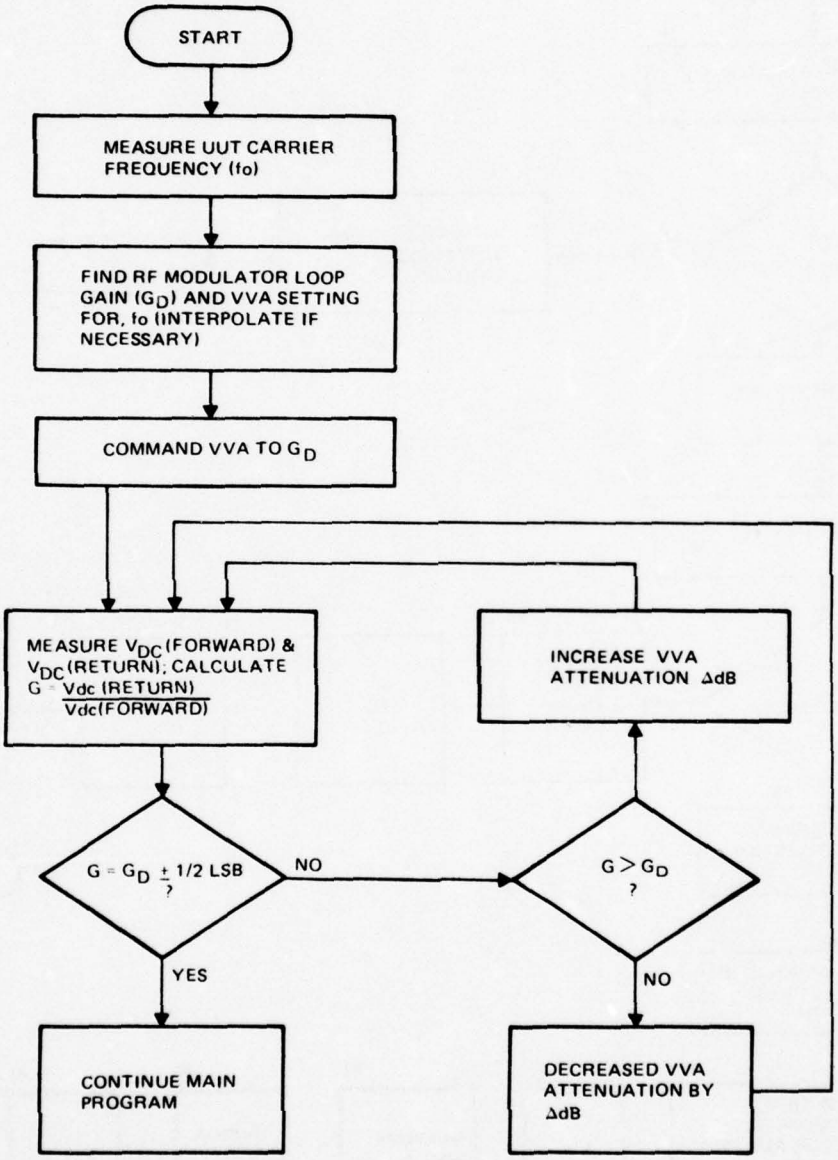

Figure 41. Real-Time Modulator Calibration Sequence

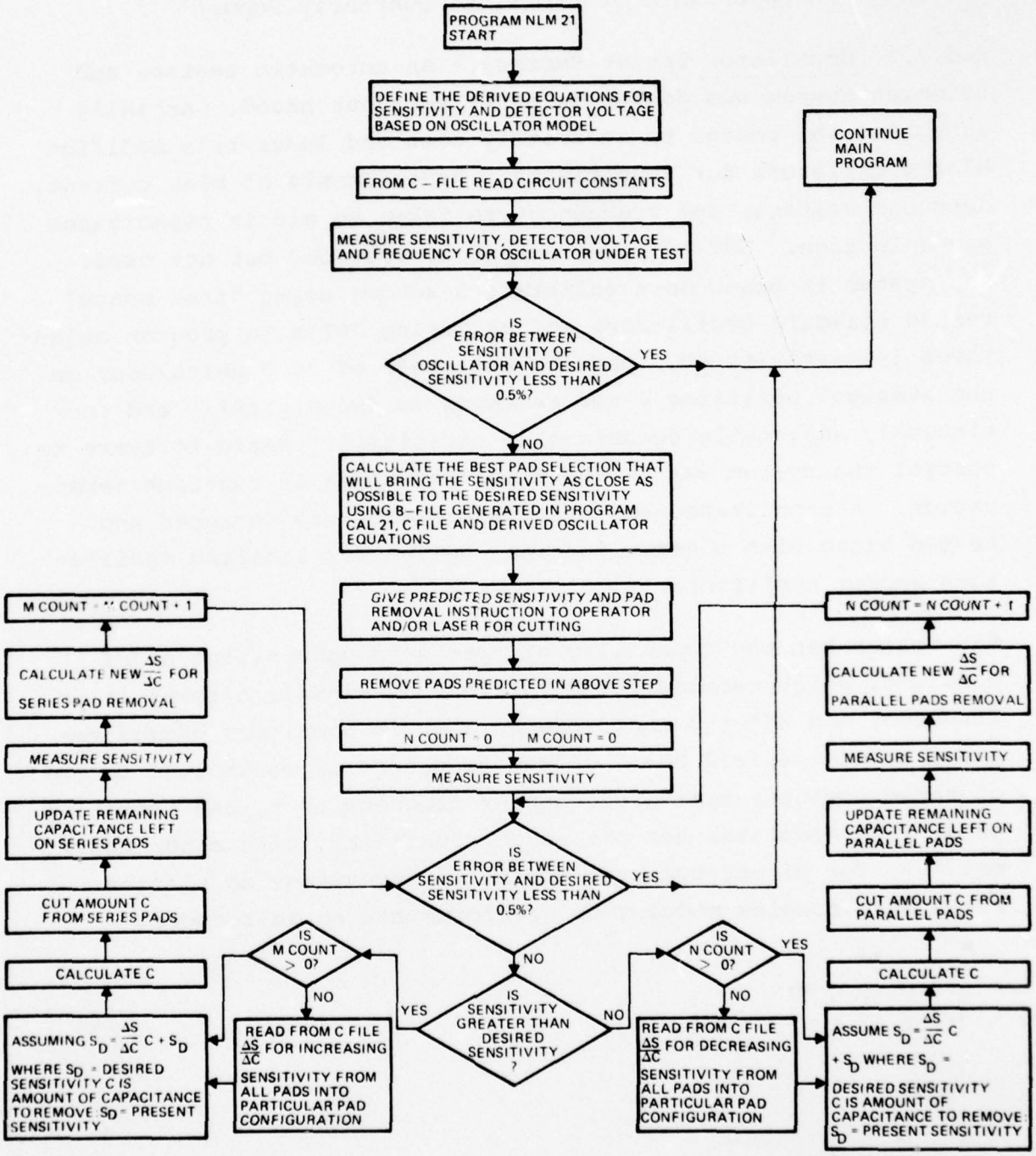

Figure 42. Flowchart for Program NLM-21

calibration sequence and NLM-21. A full description of NLM-21 is presented in Appendix A of the Sixth Quarterly Report[52].

2.5.2.3 Oscillator Tester Summary.- An automatic testing and trimming system was designed; parts were purchased, partially assembled and tested to accurately test and laser-trim modified M732 oscillators for sensitivity. Measurements of bias current, detector voltage, and frequency are taken to aid in capacitance pad selection. UUT rf power output is recorded but not used. The system is based on a calibration scheme using "free space" tested standard oscillators and adjusting UUT's to program objectives (sensitivity $\pm$0.5 percent at a rate of 3000 units/hour on the average) utilizing laser trimming of two digitally and continuously adjustable ceramic-chip capacitors. Basic software to control the system was in the flowchart stage at contract termination. A capacitance-selection subroutine was designed and tested along with a serialization routine for labeling oscillators and/or amplifiers.

The tester has the capability of precisely controlling an rf modulator which samples the UUT rf output signal, offsets it in frequency and adjusts amplitude so that it simulates ground returns at the desired HOB. Offset frequency is controlled to one of three computer-monitored doppler frequencies in the operating band. The modulator has the added capability, with minor modifications, for direct-computer-controlled frequency modulation where more complex modulation waveforms can be introduced.

3. CONCLUSIONS

The computer-controlled dynamic tester and laser-trimming system designed and fabricated during this program will ultimately be capable of testing and trimming modified M732 assemblies to tolerances approaching the design goals specified in the contract.

The idea of calculating UUT properties from fundamental measurement and impulse response data is sound (within limitations) in that the techniques employed will ultimately reduce UUT test times substantially with respect to present point-by-point response measuring techniques. This is especially true in the case of M732 amplifier assemblies.

The limitations on the approach principally fall into the area of the designer's ability to analytically and accurately represent nonlinear devices such as the full wave rectifier transfer characteristics of the M732 amplifier. The initial piecewise-linear rectifier representation used in the present system is admittedly simplistic in that accuracy will suffer substantially if used. The alternates proposed, however, promise considerable improvement.

Fundamental limitations on test and trimming time reduces to the computer's capability to rapidly perform the required calculations and the laser's capability to expeditiously cut the appropriate trimming elements. The number and complexity of the needed calculations must be minimized. The present test system minimized calculation time by relying on off-line calculation and an on-line "look-up" table (i.e., output filter convolution integral table).

Estimates of laser-cutting times for amplifier tuning vary from negligible for high-gain amplifier UUT's to as much as 1 second for low-gain UUT's with the average about 400 to 500 milliseconds.

Amplifier calculation time was about 1 second in the initial software approach. It should be pointed out, however, that the thrust of the initial program was to provide a working system with an acceptable potential accuracy.

Although some thought was given to minimizing test time, the bulk of the program effort was to design and fabricate the basic tester, modify the UTT's and provide tuning elements with sufficient resolution to meet system needs. These goals were accomplished.

Enough tester versatility was built in (both hardware and software) so that modifications could be readily introduced if needed during system testing.

Oscillator test and trimming times should be lower than that for amplifier UUT's. An estimated worst-case digital cutting time is about 500 milliseconds. Calculation times were never measured. Software complexity, however, for oscillator testing is considerably simpler than that for the amplifiers, less measurements are required and the tunable property, sensitivity, is a measured not a calculated quantity. All these reasons point to a more accurately set oscillator UUT in a shorter test and tune time.

System testing and trimming was not accomplished by contract termination, although the basic amplifier tester was within 2 weeks of beginning. Initial amplifier-trimming accuracy would probably have been 10 to 15 percent. However, the alternate rectifier representations promised considerable improvement, probably to about 1 percent. Oscillator-trimming accuracy would ultimately approach the 0.5 percent goal provided care was taken to time individual tests at precise intervals after B^+ turn-on (from a cold start).

The techniques and hardware generated during this program could readily be adapted to other UUT's in the same general frequency range. Modifications to the rf modulator hardware and/or buffer interface circuitry can expand the usefulness to other rf frequency ranges. In short, the tester is universal in that fundamental voltage and voltage-waveform measurements are made and/or generated,

UUT properties are calculated and computer-controlled accurate laser trimming of standard thick-film elements (resistance or capacitance) is performed.

Modifications to the M732 amplifier assembly were adequate for the present 3000 sample units fabricated during the program. Larger volume production quantities, however, will require a broader resistance range than that provided for the present program. The larger range "top hat" resistor was feasible for this purpose.

M732 oscillator modifications were more extensive than for the amplifier assemblies mandating a requalification if used in a production fuze. The digital capacitance designed for initially trimming test oscillators appeared adequate. Trimming speed primarily depends upon the sensitivity-capacitance prediction program.

4. RECOMMENDATIONS

The present program provided the basic tool for dynamic testing and laser trimming of selected assemblies to accurate property values. Although some limitations have been uncovered, the approach is feasible. The effort described herein should be extended to demonstrate that feasibility.

5. PERSONNEL

The following personnel worked on this program during this reporting period for the number of hours indicated:

Name	Program Function	Hours
R. Blau	Oscillator Circuit Modelling	52
R.P. Boroson	Programmer	1754
S. Conston	Digital Components and System Cabling	166
H.J. Curnan	Laser Trimmer and Fuze Microcircuits	386
R.F. DeMattos	Tester and Fuze Design (RF and Computer Interface, System Engineer (Final), Program Manager (Final)	2900
R. GiGennero	Laser Resistor Trimming Tests	377
A.J. Eisenberger	Program Manager (Initial)	778
U.Z. Escoli	Mechanical Design	884
G.L. Freed	Digital Components	314
J. Gowdy	Engineering Assistant	1239
T.R. Griffin	Fuze Microcircuits	108
P. Kaszerman	System Engineer (Initial)	1340
J.P. Michales	System Interface Hardware Design and Cabling	1070
A.H. Owens	Mechanical Design	209
R. Puszkarczuk	System Test, Programming	481
C.A. Zuroff	Programming	116
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A dynamic test and correction system was designed and partially developed which is capable of high-speed testing and laser-trimming electronic assemblies. The circuits selected for tester verification were the oscillator and amplifier assemblies of the M732 Fuze.

Program goals required that a selected critical property of each assembly be set to a ±0.5 percent tolerance at an average test and trim rate of 3000 units per hour excluding mechanical handling.

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20. Abstract (Continued)

The system was designed to measure fundamental properties of modified amplifier assemblies, calculate height of burst, and automatically laser trim a thick-film resistor to adjust this property to a precise value. Oscillator assemblies were adjusted for sensitivity by trimming one of two ceramic chip capacitors.

Height of Burst (or sensitivity) was calculated in real-time using a combination of "black box" equivalent circuit and/or circuit model representations of individual test unit stages. Pre-calculated look-up tables were introduced where complex time-consuming calculations were required.

The engineering effort ended prior to system testing the program's amplifier test segment. Tester system and hardware design and fabrication, however, was completed. Three thousand (3000) amplifiers and 75 prototype oscillators were fabricated and electrically prechecked.

Basic techniques may be applicable to other assemblies with appropriate modifications.