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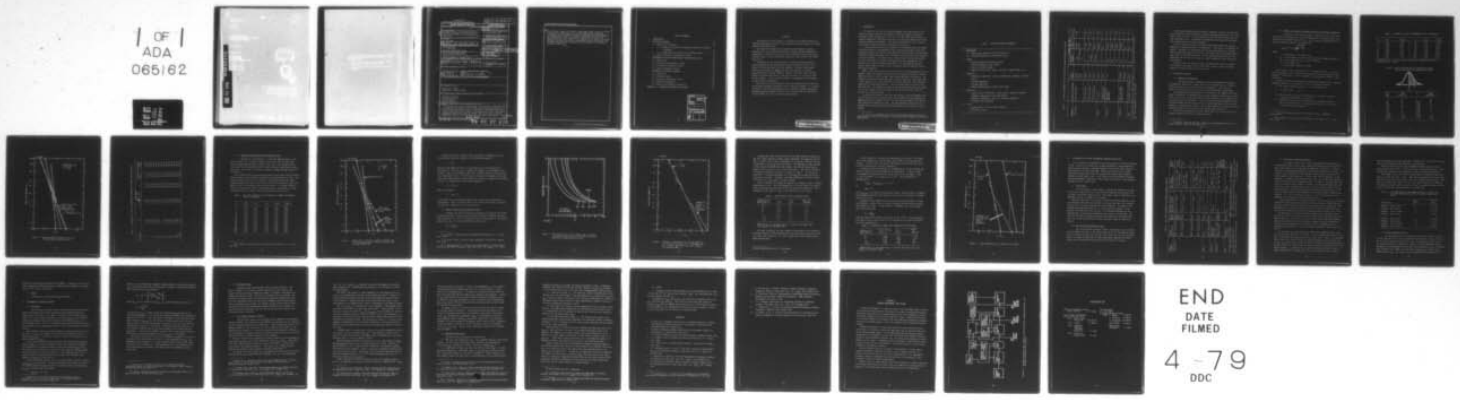

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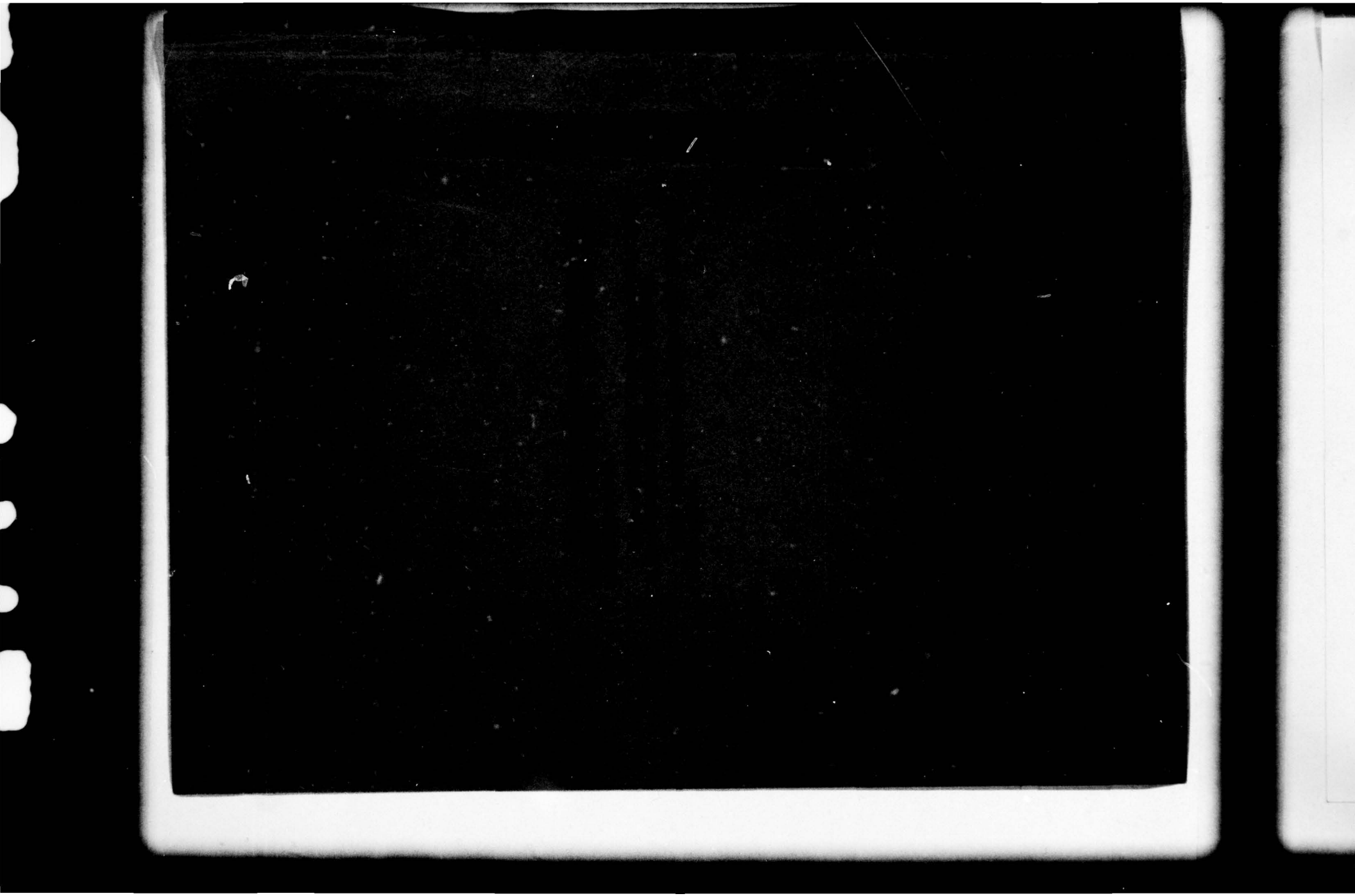

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The objective of this program phase was to provide an effective means of purchasing semiconductor devices whose neutron-induced response is within known and acceptable limits. The scope of the effort was limited to those procedures for the neutron environment for bipolar transistors, temperature-compensated reference diodes, TTL (54/74) series digital integrated circuits, 741-type operational amplifiers and junction → next page

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field effects transistors (JFET's). This final report covers the method by which the program objectives were met and provides background information for the companion document "Hardness Assurance Guidelines for Displacement Effects for Bipolar Devices" (HDL-CR-78-135-1). Specifically this final report covers background lot sample statistical methods, assesses existing CRIC experimental neutron device data, and provides the background rationale for the selection of the Hardness Assurance controls.

TABLE OF CONTENTS

Foreword

The objective of this program is to provide a cost-effective means of obtaining semiconductor devices whose response to neutron radiation is within known and acceptable limits.

The scope of this phase of the program covered hardness assurance procedures for silicon bipolar transistors, reference diodes (temperature-compensated), transistor-to-transistor logic integrated circuits (54/74 and 54L/74L series), 741-type operational amplifiers, and junction field-effect-transistors.

In addition to this interim report, a guideline document (Hardness Assurance Guidelines for Displacement Effects for Bipolar Devices, by R. Berger, IRT 8166-003, March 1978) was produced. The guideline document discusses the concept of supplier and user qualified parts, hardness assurance controls (process controls, screens, lot sample tests), and the effects of neutron radiation for each type of device covered in the scope of this program. It also contains examples of procurement specifications and part selection procedures.

This report covers the method by which the program objectives were met and provides background information for the guideline document. It assesses the amount of existing experimental data in the Harry Diamond Laboratories Component Response Information Center (CRIC) and discusses the development of the methods called for in the Guideline Document.

1. INTRODUCTION

The choice of the critical response parameters for neutron effects for hardness assurance controls was based on a worst-case bipolar transistor theoretical model developed by A. Hart et al.[1] This report also contains a computer program for calculating the worst-case transistor damage factor from terminal parameter measurements. This worst-case prediction of K_D is valid over current ranges where emitter crowding does not occur.

In the selection of devices for analysis, it was decided that the neutron radiation response of semiconductor diodes, bipolar transistors, small-scale integrated circuits and junction field effect transistors (JFET's) has been more completely characterized than some of the other more complex devices available to circuit designers. Therefore, these classes of devices were selected for an initial assessment to provide the hardness assurance methodology, test methods, and dosimetry standards applicable to all semiconductor devices. Table 1 breaks down the general device categories into more specific device functional categories.

Table 2 lists the specific devices chosen for in-depth assessment for this program. Under the category of transistors, the 2N2484, the 2N2222, and the 2N914 were chosen as the low power (small signal amplifier) NPN devices. The 2N2904 was chosen for the low power PNP transistor analysis. This device has a large sample size of about 300 units in the CRIC data bank. The 2N3264 was chosen for the high power NPN unit. This device has about 212 units in the CRIC data bank. The 2N5005 was chosen as the PNP high power unit even though it only has a sample size of 6 because of the scarcity of these types of devices in the CRIC data bank.

In the area of diodes, it was felt that the most critical parameter and type of device as far as neutron effects were concerned was the temperature-compensated silicon reference diodes. No data could be found in CRIC for the 1N935 temperature-compensated zener. The non-compensated 1N4464 data were examined but it was decided that the 1N4464 data was not of interest in this program.

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[1] *A. Hart et al, Parameter Sensitivites for Hardness Assurance; Displacement Effects for Bipolar Transistors, Final Report, Mission Research Corporation, MRC/SD-R-20.*

TABLE 1. DEVICE FUNCTIONAL CATEGORIES

1. TRANSISTORS
   - 1.1 Small-Signal Amplifiers (NPN and PNP units).
   - 1.2 Switching Transistors (NPN and PNP units).

2. DIODES
   - General Purpose and Switching Diodes
   - Silicon Reference (Zener) Diodes
   - Rectifier (Power) Diodes
   - Special Purpose Diodes (SCR's, Varactors, Tunnel Diodes, etc.)

3. LINEAR IC's
   - Operational Amplifiers (single, differential, wideband, and RF/IF units)
   - Voltage Comparators
   - Voltage Regulators
   - Modulator/Demodulators (phase-locked loops)

4. DIGIAL IC's
   - Logic Circuits (flip-flops, clocks, gates, counters, encoders/decoders, multiplexers, and time delays)
   - Memories (read/write, read only, and shift registers)
   - Interface Units (buffers)

5. JFET's
   - Linear JFET's (n- and p-channel units)
   - Switching JFET's

TABLE 2. IN-DEPTH ASSESSMENT DEVICES FOR NEUTRON HARDNESS ASSURANCE ANALYSIS

Category	Device Description	Device Number	NEUTRON TEST DATA		
			Parameter Examined	CRIC I.D. Number	Lot Size
Transistors	NPN (low power)	2N2484	K_D	700121	100
		2N2222	K_D and $V_{CE(SAT)}$	711101	12
		2N914	K_D	--	--
	PNP (low power)	2N2904	K_D	7003	312
	NPN (high power)	2N3264	$\Delta V_{CE(SAT)}$	6904	212
	PNP (high power)	2N5005	$\Delta V_{CE(SAT)}$	691117	6
Diodes	Si, Zener	1N4464	ΔV_Z	690528	326
	Temperature-compensated Zener	1N935	ΔV_Z	NA	--
Linear IC	Operational amplifier	741	ΔV_{OS}	720426	6
			ΔA_{VO}	740426	6
			ΔI_{IB}	730831	10
Digital IC	Gate, TTL, NAND, Positive logic	5N54H04	ΔV_{OL}	7404000	5
		5N54L00	I_{SK}	NA	--
JFET	N-Channel (low power)	2N4220	g_m	NA	--

I_{IB} = Input bias current, A_{VO} = Open loop voltage gain, V_{OL} = Output low logic level voltage, g_m = Transconductance, NA = Not available

Of the many different types of digital integrated circuits, the most data were found in the CRIC data bank and the most popular bipolar logic form in use today is the TTL series. Most of the data in the CRIC data bank were for the SN54 and SN54H series. The SN54L00 and SN54H04 positive logic TTL NAND gates were examined for the in-depth assessment.

Linear integrated circuits incorporate operational amplifiers, voltage comparators, voltage regulators, and modulators. Each device is different and complex. Therefore, it was decided to limit the investigation to a popular type of operational amplifier for which a reasonable amount of neutron effects data existed in the CRIC data bank. The 741 operational amplifier met this requirement and so was the only type of linear integrated circuit examined in this program.

There are very few items of neutron radiation effects data on junction field effects transistors (JFET's). There were no data listed in the CRIC computer for neutron effects on these devices.

2. STATISTICAL METHODS

2.1 Statistical Procedures

Lot sample quality conformance tests are performed with realistic environmental stresses on a random sample of devices from the lot in order to place statistical limits on the total lot (population). Since the test devices can be rejected for use the tests can be degrading or destructive.

For the applications considered in this program, a lot sample statistical plan is desired for 10 samples which will place statistical limits on the worst device in the lot at 90 percent confidence (the confidence level commonly used in quality control applications). Also, the statistical plan should allow for the establishment of a historical data base so that statistical limits can be improved as the data base expands. The variable sampling plan detailed in the guideline document[2] is the best plan for meeting these objectives.

In order to understand the variable sample plan it is first necessary to consider regression limits on a sample data line.

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[2] *R. Berger, "Hardness Assurance Guidelines for Displacement Effects for Bipolar Devices," IRT 8166-003, March 1978.*

2.1.1 Example Calculation of Regression Limits at 90 Percent Confidence

An interval can be defined around a sample data line within which 90 percent of subsequent data lines from samples of 10 representing the same underlying source variability will fall. This is done by calculating the 90 percent confidence regression interval from[3]

$$Y_{90\%} = \bar{Y} \pm t_{\alpha/2} s \sqrt{\frac{1}{N} + \frac{K_N}{N-1}}$$

where

$\bar{Y}$ is the point on the sample line,

$t_{a/2}$ is the Student "t" statistic at 90 percent confidence (Table 3),

K_N is the normalized unit variable (Table 4),

N is the sample size,

s is the sample standard deviation.

In the formula for calculating the 90 % confidence interval, it is necessary to use tables of the "Student t" distribution[4] and the K_N normalized unit variable.[3] These tables, at 90 % confidence, are reproduced in Tables 3 and 4, respectively.

The 90 % confidence regression limits around the 10 sample 2N2222 cumulative frequency regression line of Figure 2.1 can be calculated as follows

(1) The sample standard deviation, s, is calculated from

$$s = \frac{x_{93.3} - x_{6.7}}{3} = 0.20 \quad .$$

(2) The value for $t_{\alpha/2}$ at 90 % confidence ($\alpha/2 = 0.959$) is found for a sample of 10 from Table 3 to be 1.83.

(3) Knowing the values of K_N from Table 4, the confidence intervals can be calculated (Table 5) and plotted in Figure 1, the value of $\bar{Y}$ are read from the sample line.

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[3] *J. R. King, Probability Charts for Decision Making," Industrial Press (1962).*

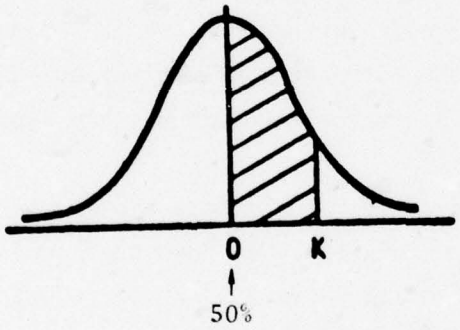
[4] *A. J. Duncan, "Quality Control and Industrial Statistics," R. D. Irwin, Inc., 1959.*

TABLE 3. "STUDENT t" AND X^2 DISTRIBUTIONS AT 90 % CONFIDENCE

N	$t_{\alpha/2}$	$X^2_{0.05}$	N	$t_{\alpha/2}$	$X^2_{0.05}$
5	2.13	0.711	14	1.77	5.89
6	2.02	1.15	15	1.76	6.57
7	1.94	1.64	20	1.72	10.1
8	1.90	2.17	25	1.71	13.8
9	1.86	2.73	30	1.70	17.7
10	1.83	3.33	41	1.68	26.5
11	1.81	3.94	61	1.67	43.2
12	1.80	4.57	101	1.66	77.9
13	1.78	5.23	344	1.65	313

Excerpted from A. J. Duncan, Quality Control and Industrial Statistics, R. D. Irvin, Inc. (1955).

TABLE 4. SELECTED PERCENTILES AND ASSOCIATED K VALUES FOR THE AREA UNDER THE STANDARD NORMAL CURVE



O-K Area	Upper Percentile	K_N	Lower Percentile
0	50	0	50
20	70	0.524	30
30	80	0.842	20
34.1	--	1.00	--
40	90	1.282	10
45	95	1.645	5
47.7	--	2.00	--
49	99	2.326	1
49.87	--	3.00	--
49.9	99.9	3.090	0.1
49.99	99.99	3.719	0.01

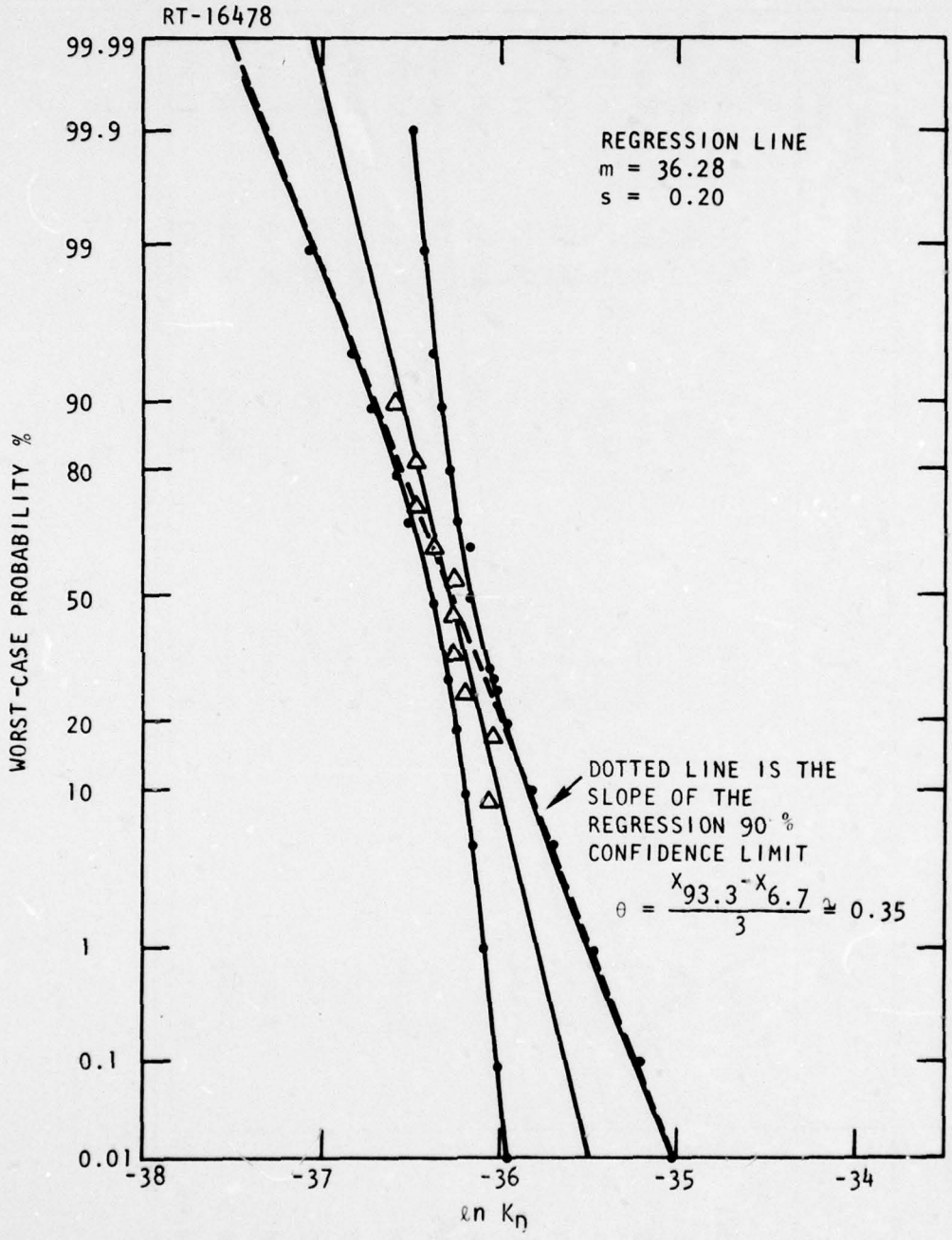


Figure 1 Regression 90% confidence limits for 10-sample 2N2222 regression line

TABLE 5. CALCULATION OF THE 90 % CONFIDENCE REGRESSION INTERVAL FOR THE 2N2222

Percentile	K_N	$t_{\alpha/2}\, s \sqrt{\frac{1}{N} + \frac{K_N^2}{N-1}}$	$\bar{Y}$	Confidence Interval Lower	Upper
0.1	3.090	0.390	-36.93	-37.32	-36.54
1	2.326	0.303	-36.77	-37.07	-36.47
5	1.645	0.229	-36.63	-36.86	-36.40
10	1.282	0.192	-36.55	-36.74	-36.36
20	0.842	0.153	-36.46	-36.61	-36.31
30	0.524	0.131	-36.40	-36.53	-36.27
50	0	0.11	-36.30	-36.41	-36.19
70	0.524	0.131	-36.20	-36.33	-36.07
80	0.842	0.153	-36.13	-36.28	-35.98
90	1.282	0.192	-36.04	-36.23	-35.85
95	1.645	0.229	-35.96	-36.19	-35.73
99	2.326	0.303	-35.83	-36.13	-35.53
99.9	3.090	0.390	-35.66	-36.05	-35.27
99.99	3.719	0.463	-35.53	-35.99	-35.07

2.1.2 Regression Versus Worst-Case Confidence Limits

The equations in Section 2.1.1 gives the sampling errors in the line of regression. In order to obtain a worst-case limit (an individual point), another quantity must be added to the error in the regression line to account for the possible deviation of the individual value from the regression value. This point is difficult to address, although Duncan[4] (page 660) discusses it.

Let us obtain these larger worst-case limits using normal theory tolerance analysis based on an estimate of the population standard deviation limit. One-sided tolerance circuit factors[4] (Table 6) are usually based on the sample standard deviation(s), which yields limits close to the regression limits and hence are not the individual limits that are desired. The normal tolerance limits (L_s) based on the sample standard deviation(s) are plotted as circles in Figure 2 for the 10-sample 2N2222 data discussed in Section 2.1.1

TABLE 6. ONE-SIDED TOLERANCE LIMIT FACTORS FOR A NORMAL DISTRIBUTION FOR 90 % CONFIDENCE

N	0.80	0.90	0.99	0.999	0.9999
5	1.86	2.74	4.67	6.11	6.90
6	1.71	2.49	4.24	5.56	6.34
7	1.61	2.33	3.97	5.20	5.99
8	1.54	2.22	3.78	4.95	5.73
9	1.48	2.13	3.64	4.77	5.55
10	1.43	2.07	3.53	4.63	5.40
15	1.30	1.87	3.21	4.21	4.97
20	1.22	1.76	3.05	4.01	4.75
30	1.14	1.66	2.88	3.79	4.51
40	1.10	1.60	2.79	3.68	4.39
50	1.07	1.56	2.73	3.60	4.31
60	1.05	1.53	2.69	3.55	4.25
100	1.00	1.47	2.60	3.43	4.12
300	0.93	1.39	2.48	3.28	3.94
500	0.91	1.36	2.44	3.23	3.89

[4] *A. J. Duncan, "Quality Control and Industrial Statistics," R. D. Irwin, Inc. 1959.*

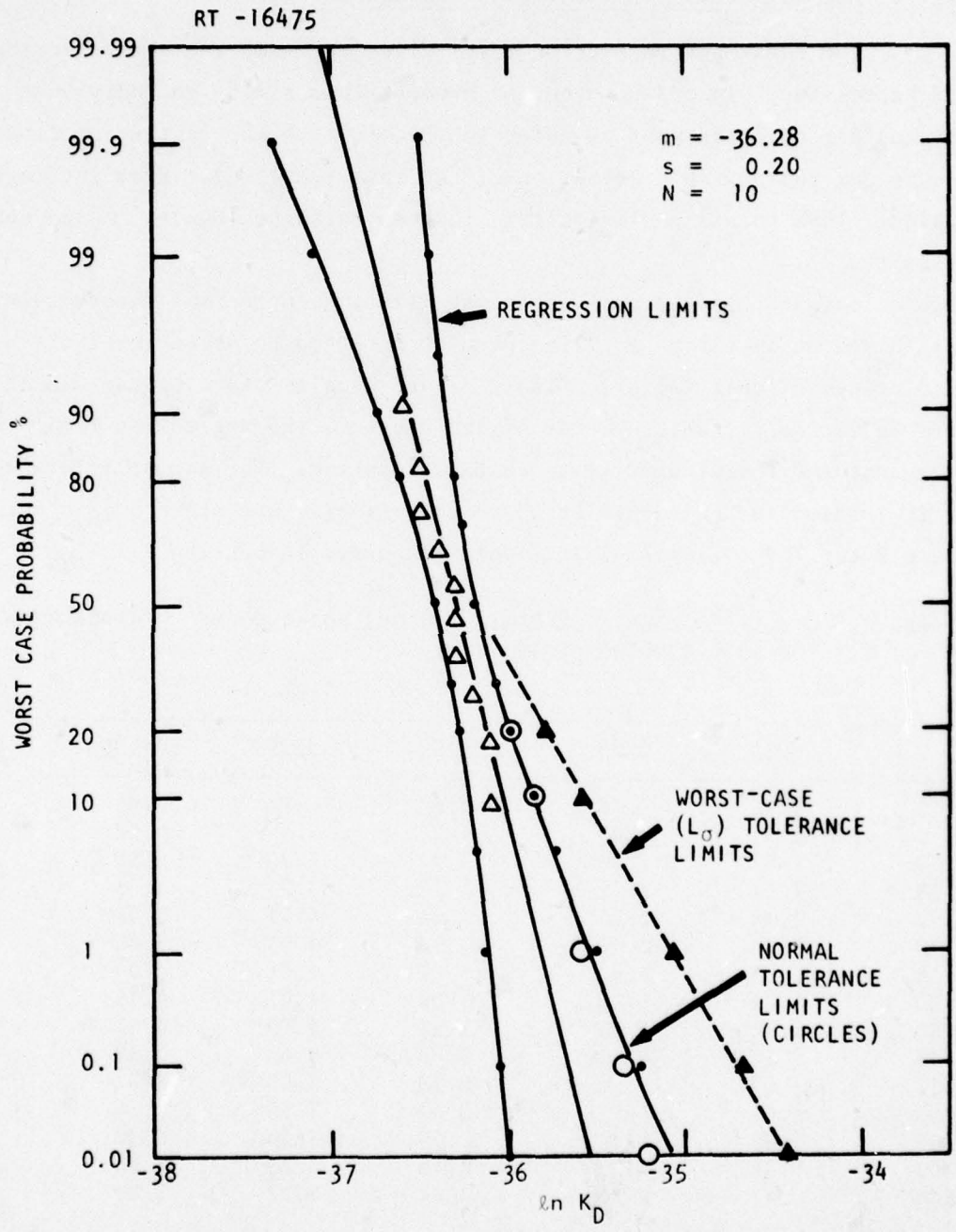


Figure 2. Comparison of regression, normal tolerance, and worst-case (individual) tolerance limits for the 10-sample 2N2222 data

Consider the use of tolerance limits now based on the population (lot) standard deviation limit estimate (σ) calculated from Duncan[4],

$$\sigma = s \frac{\sqrt{N}}{\chi} \quad ,$$

where N is the sample size and χ is the square root of the statistical χ^2 distribution.[5] This new value is roughly the tangent to the regression curve (Figure 1) and as such represents the limit (at 90 % confidence) of the values for s from samples of 10. The variation of individual value upper (worst-case) limits above this population limit estimation is given by normal theory tolerance analysis. By substitution, the tolerance equation is

$$L_\sigma = \sigma K_T + m$$

and can be reduced to

$$L_\sigma = s K_{TL} + m$$

if the values of K_{TL} are obtained from Figure 3 (which has the $\chi/\sqrt{N}$ factor incorporated). The L_σ worst-case limits calculated by this method lie outside the regression limits, as can be seen in Figure 2.

2.2 Bipolar Transistor K_D Population Limits

Messenger and Steele[6] obtained the cumulative distribution of 351 NPN assorted transistors. These data are plotted in Figure 4 along with the worst-case statistical limit at 90 % confidence calculated from Figure 3. The neutron damage factor (K_D) is calculated from the K_M factor from:

$$K_D = \frac{1}{2\pi K_M f_T} \quad .$$

---

[4] *A. J. Duncan, "Quality Control and Industrial Statistics," R. D. Irwin, Inc., (1959).*

[5] *J. M. Juran, editor, "Quality Control Handbook," Third Edition, McGraw-Hill, 1974.*

[6] *G. C. Messenger and E. L. Steele, "Statistical Modeling of Semiconductor Devices for the TREE Environment," IEEE Trans. Nucl. Sci., NS-15, 133, (1968).*

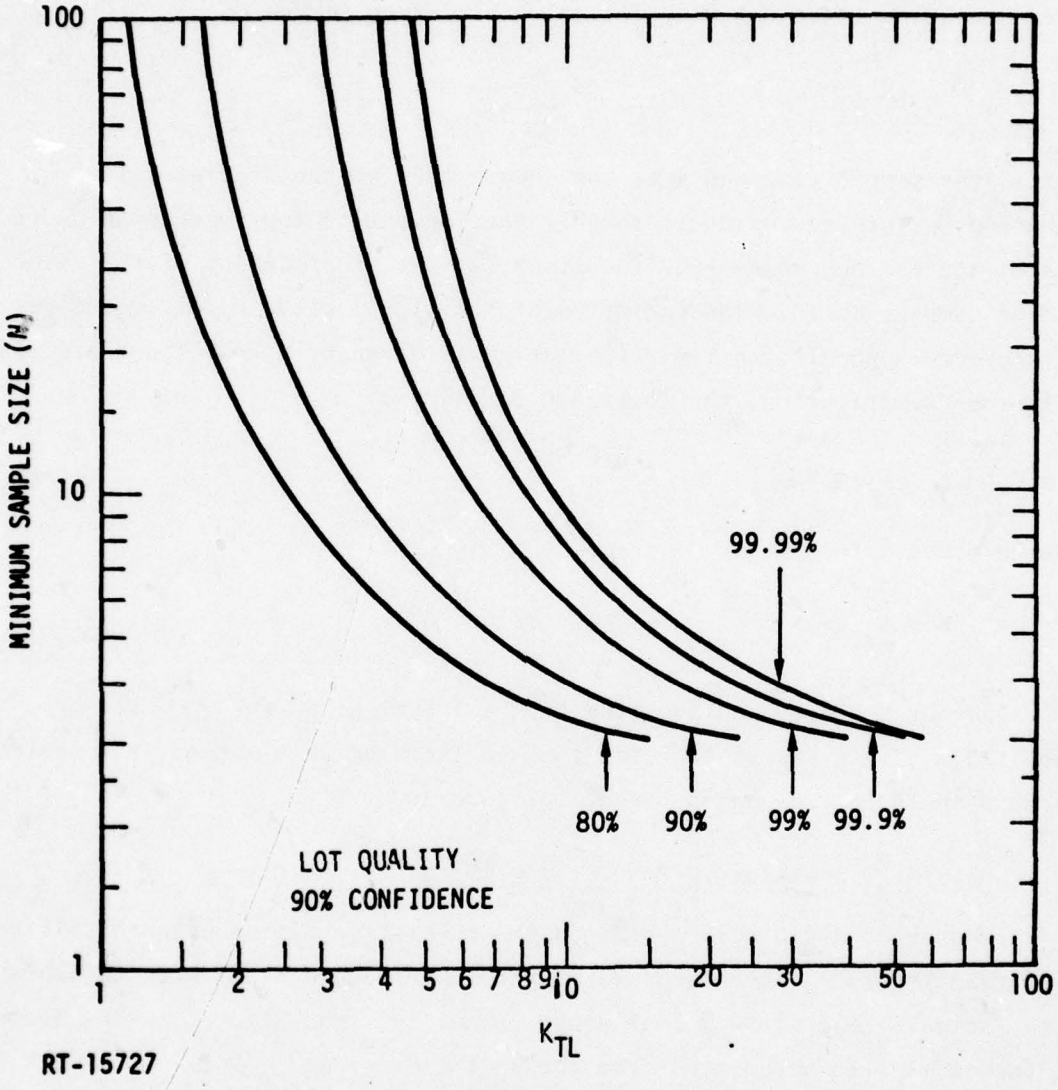


Figure 3. One-Sided Tolerance Limit Factors (K_{TL}) for normal distribution including the $X/\sqrt{N}$ factor estimate of population standard deviation limit.

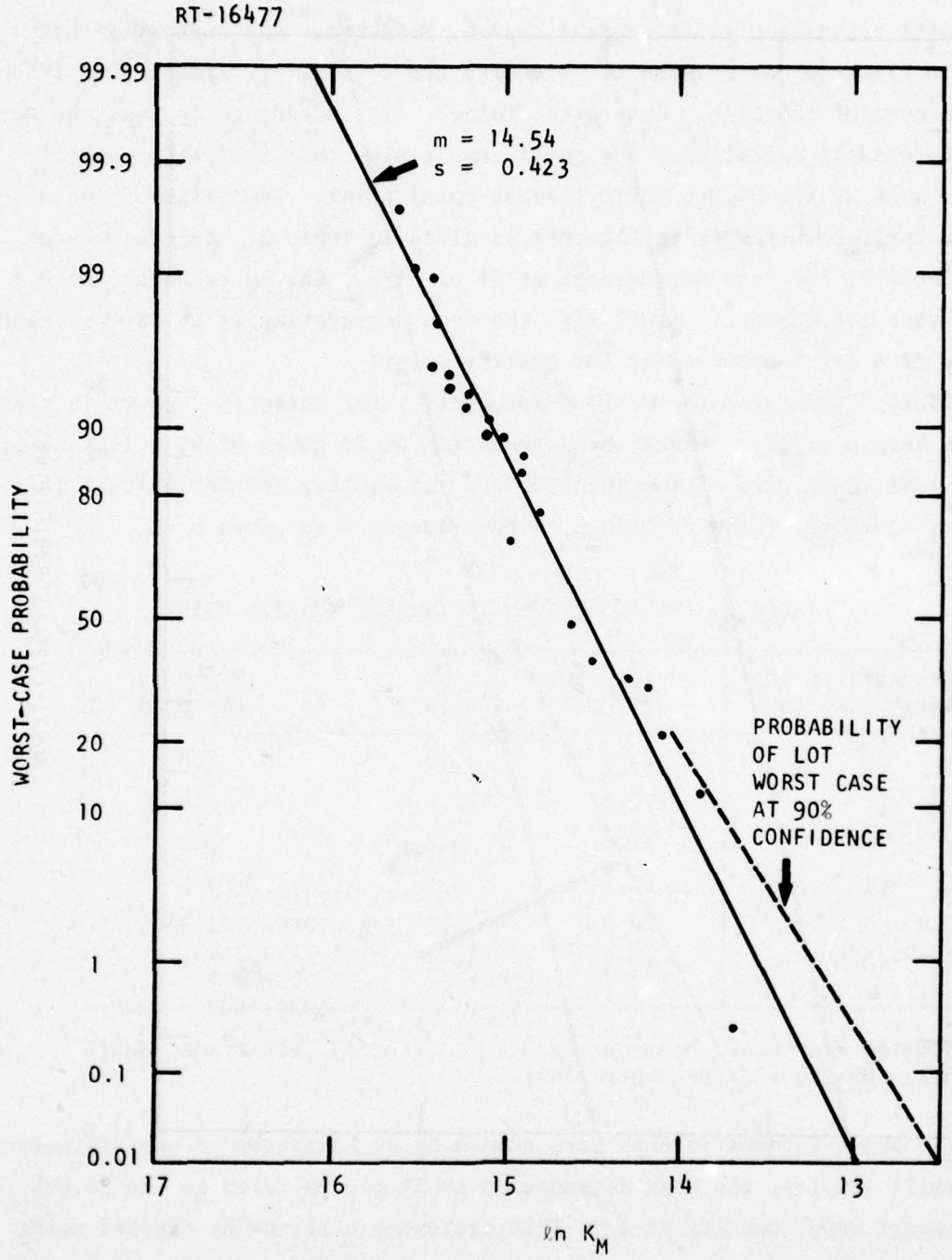


Figure 4. Cumulative distribution of ℓn K_M data from the 351 NPN transistor data of G. C. Messenger and E. L. Steele, IEEE Trans. Nucl. Sci., NS-15, 133 (December 1968).

Assuming that these statistics hold for all NPN transistors operated in the small signal amplifier current region, Messenger* has suggested that the data in Figure 4 can be used to determine the lot quality from the shifting of the mean of the $\Delta 1/h_{FE}$ data with fluence. The advantage is that the mean is more clearly established for small sample size than the higher quality points such as the 99.9 % (or 0.1 worst-case) point. The ratio of the mean to the worst-case points in Figure 4 is given in Table 7. As can be seen from Table 7, the mean degradation at 5Φ of $\Delta 1/h_{FE}$ may be taken as the 0.1 % worst-case lot quality. Similarly, the mean degradation at 2Φ may be taken as the 90 % (10 % worst-case) lot quality point.

Table 7 indicates the minimum lot quality for category 2 parts (a fluence design margin of 10). Since the degradation at 7Φ gives 99.99 % lot quality, a 10Φ test would give better than 99.99 % lot quality for NPN units. This follows since the ratio of $\Delta 1/h_{FE}$ to the fluence Φ is given by K_D.

TABLE 7. RATIO OF MEAN TO THE LOT QUALITY POINT

Probability of Worst Case (%)	$\ell n\ K_M$	K_M ($\times 10^5$)	Ratio to the Mean
50	14.5	19.8	1.0
20	14.0	12.6	1.6
10	13.8	9.8	2.0
1	13.2	5.7	3.5
0.1	12.8	3.8	5.2
0.01	12.5	2.8	7.1

Adapted from G. C. Messenger and E. L. Steele, IEEE Trans. Nucl. Sci., NS-15, 133 (December 1968).

The above information has been summed up by Messenger in one statement:* "For small samples, the mean degradation at 5Φ may be taken as the 99.9 % (or 0.1 % worst case) quality at Φ." This statement will now be checked using 2N2222 neutron data.

Private communication with G. C. Messenger.

Figure 5 shows the $\ell n\ \Delta 1/h_{FE}$ data degradation at 1Φ and 5Φ. The dotted line is the probability of the lot worst-case values at 1Φ calculated from Figure 3. As can be seen, the mean of the 5Φ data (5.28) is the same as the lot 99.9 % quality point (at 90 % confidence).

A method can now be established for determining the circuit criteria for 2N2222 lot quality at 99.9 % minimum (at 90 % confidence). Using the 2N2222 as an example, find the mean of the $\Delta 1/h_{FE}$ data at 5Φ on 10 samples. This is -5.28 in Figure 5, or a $\Delta 1/h_{FE}$ of 5.1×10^{-3}. This translates to a degraded gain of

$$1/h_{FE\phi} - 1/h_{FE0(min)} = 5.1 \times 10^{-3}$$

or

$$h_{FE\phi} = 54$$

since $h_{FE(min)}$ is 75 (from the specification sheet). Thus the 2N2222 is capable of providing minimum 99.9 % lot quality if the circuit can tolerate a degraded gain of 54 or less.

Messenger's data (Figure 4) can also be used in part selection for hardness assurance. Table 8 gives the values of K_M and the associated lot worst-case probability values. If the 2N2222 is a candidate part, its K_D values can be calculated from

$$K_D = \frac{1}{2\pi K_M f_T}$$

using the specification sheet value for f_T of 250×10^6 Hz. The resulting K_D (see Table 8) values can be used to see if the 2N2222 will meet the desired worst-case probabilities.

TABLE 8. CALCULATION OF WORST-CASE PROBABILITY FOR THE 2N2222

Probability of Worst Case (%)	Value of $\ell n\ K_M$ (Figure 4)	K_M ($\times 10^5$)	2N2222 K_D ($\times 10^{-16}$)
20	14.05	12.6	5.05
10	13.80	9.85	6.46
1	13.25	5.68	11.2
0.1	12.85	3.81	16.7
0.01	12.55	2.82	22.6

Adapted from G. C. Messenger and E. L. Steele, IEEE Trans. Nucl. Sci., NS-15, 133 (December 1968).

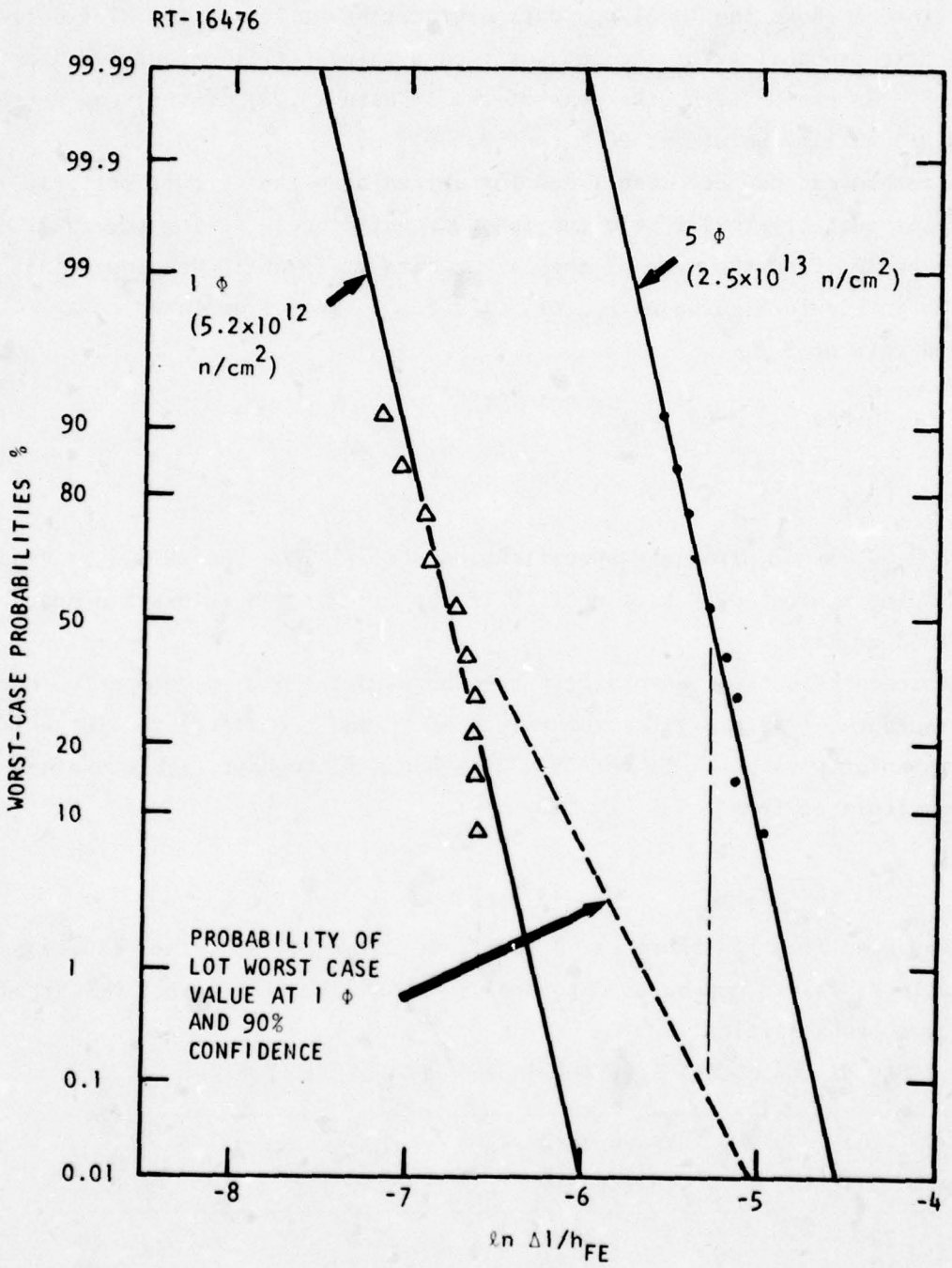


Figure 5. $\Delta 1/h_{FE}$ degradation at 1Φ and 5Φ of the 2N2222

3. ASSESSMENT OF EXISTING EXPERIMENTAL NEUTRON EFFECTS DATA

In this section, an assessment of the existing data in the CRIC data bank is made. The devices selected for in-depth assessment in this program were chosen primarily because a reasonable amount of statistical data existed for those devices in the CRIC data bank. Table 9 lists each of the in-depth assessment selected devices and the existing CRIC neutron data parameters together with the sample sizes. Also, Table 9 lists the hardness assurance screening parameters identified in this program so that gaps in the available information can be readily seen.

3.1 Transistors

For transistors, a large amount of statistical information (sample sizes greater than 100) exists in the CRIC data bank for NPN low power, PNP low power, and NPN high power devices. The largest sample of PNP power units appeared to be the six samples of the 2N5005.

The main thing which is not present in CRIC for neutron analysis is the preirradiation data which are necessary to describe the device in a physical sense so that its neutron degradation can be predicted. For example, the minimum gain bandwidth product f_T, at a given collector current, is not present in the CRIC data, and yet this is an important parameter for the determination of the neutron degradation of the gain in a transistor. Because of this lack of complete preirradiation information in the CRIC data bank, the screens identified for hardness assurance cannot be completely checked.

3.2 Silicon Voltage Reference Diodes

For silicon voltage reference diodes a large sample size was found for the 1N4464 (326 units). CRIC neutron data exists for the forward voltage (V_F), the reverse current (I_R), and the zener voltage (V_Z) in this particular device. No data was found for the 1N935 temperature compensated reference diode, which is unfortunate because this was the device of interest.

TABLE 9. CRIC DATA ASSESSMENT FOR NEUTRON HARDNESS ASSURANCE

Device Category	Device Description	Device Number	Candidate Hardness Assurance Screens	CRIC Neutron Data Parameters	Sample Size
Transistors	NPN, (low power)	2N2484, 2N2222, 2N914	h_{FEO}, f_T, $V_{CE(SAT)}$	h_{FEO}, $V_{CE(SAT)}$, I_{CBO}, K_D, V_{BE}, $V_{BE(SAT)}$	100 (2N2484)
	PNP, (low power)	2N2904	h_{FEO}, f_T, $V_{CE(SAT)}$	h_{FEO}, I_{CBO}, V_{BE}, $V_{BE(SAT)}$, $V_{CE(SAT)}$, K_D	312
	NPN, (high power)	2N3264	h_{FEO}, f_T, $V_{CE(SAT)}$	h_{FEO}, $V_{CE(SAT)}$, I_{CBO}, K_D, V_{BE}, $V_{BE(SAT)}$	212
	PNP, (high power)	2N5005	h_{FEO}, f_T, $V_{CE(SAT)}$	h_{FEO}, $V_{CE(SAT)}$, I_{CBO}, K_D	6
Diodes	Zener	1N4464	V_Z, I_R	V_F, I_R, V_Z	326
	Temp. Comp. Zener	1N935	?	None	0
Linear IC	Operational Amplifier	741	A_{VOL}, I_I	A_{VOL}, CMRR, V_{OS}, I_{OS}	~10
Digital IC	Gate, TTL, NAND, Positive Logic	SN54H04 SN54L00	I_{SK}	t_{PLH}, t_{PHL}, V_{OL}, V_{OH}	~30 (if similar units are combined)
JFET	N-channel (low power)	2N4220	g_m	None	0

I_I = Input stage bias current
A_{VOL} = Open loop voltage gain
V_{OL} = Output -low -logic -level voltage
CMRR = Common mode rejection ratio
V_{OH} = Output high-logic-level voltage
I_{OS} = Input offset current
g_m = Transconductance
I_{EE} = Power supply current
t_p = Propogation delay

3.3 TTL Digital Integrated Circuits

TTL digital logic circuits come in many different configurations, including flip flops, clocks, gates, counters, encoders, and time delay units. Most of the sample sizes in the CRIC data bank are in units of 5. However, several of the packaged configurations contain more than one type of unit. For example, in one integrated circuit package, several gates will occur with a varied number of input terminals. To get as much data as possible, it was necessary to combine these individual units of 5. In the 54H series devices, the 00, 04, 10, and 20 are compatible units. The H00 is a quad two-input gate circuit, the H04 is a hex inverter, the H10 is a triple three-input gate, and the H20 is a dual four-input gate. There is a fair amount of data on these units; however, a considerable amount of the data are fluences below 1×10^{14} n/cm^2, at which point not much degradation in any of the logic parameters has occurred. It is only for neutron levels of 1×10^{14} n/cm^2 and above that a degradation in the important logic parameters occurs.

For the degradation in the output voltage in the low state (V_{OL}) at fluences above 10^{14} n/cm^2, a sufficient statistical data base exists in the CRIC data bank for only the RSN54H and SN54H series positive logic TTL NAND gates. The SN54H04S units are the high-speed version of the TTL logic gates, with the postscript S designating the military temperature range of minus 55 to +125°C.

The RSN 54H is a high-speed radiation-hardened TTL integrated circuit. This version of TTL has a high tolerance to gamma and neutron irradiation and employs dielectric isolation, thin film resistors, small transistor geometry, shallow base diffusions, heavy gold doping, minimum collector thickness and resistivity, and aluminum interconnection systems. The RSN54H series is designated for operation over the full military temperature range, from -55° to +125°C.

The CRIC data bank contains neutron data on the propagation delay, both low to high (TPLH) and high to low (TPHL). It also contains the output voltage levels in both the high (V_{OH}) and low (V_{OL}) logic states. While the propagation delay of the TTL circuits degrades with neutron fluence it is the output sink current (I_{sk}) which is more closely related to the gain of the output transistor and hence can be tied back through the neutron sensitive transistor model to the damage constant. I_{sk} data are not generally available since that requires a special measurement. The data do not exist on the units for which neutron

data was obtained in the CRIC data bank. Therefore, the use of CRIC to obtain sink current degradation with neutrons is not possible.

Table 10 lists the devices for the RSN54H and SN54H series for which neutron data fluences above 1 x 10^{14} n/cm^2 exist in the CRIC data bank. These were the data examined to find hardness assurance correlation parameters.

Large sample sizes exist in the CRIC data bank for NAND gates which were used in an early electronic system. These gates are mostly of the older diode transistor logic (DTL) form, which is not used in modern digital design. Therefore, even though large sample sizes do exist, these data were not examined for hardness assurance analysis because it would have meant a complete circuit analysis of an older logic form which is no longer used.

TABLE 10. CRIC COMPUTER DATA FOR NEUTRON LEVELS AT 1 x 10^{14} n/cm^2 AND ABOVE FOR RSN54H and SN54H TTL POSITIVE LOGIC NAND GATES

Nomenclature		Sample Size	Fluences (n/cm^2)
RSN54H00	Quad 2 Input	12	5 x 10^{14}
RSN54H04	Hex Inverter	12	5 x 10^{14}
RSN54H10	Triple 3 Input	6	5 x 10^{14}
RSN54H20	Dual 4 Input	8	5 x 10^{14}
SN54H00S	Quad 2 Input	12	5 x 10^{14}
SN54H04S	Hex Inverter	18	5 x 10^{14}
SN54H10S	Triple 3 Input	6	5 x 10^{14}
SN54H20S	Dual 4 Input	8	5 x 10^{14}

3.4 Linear Integrated Circuits

For the purposes of this program, the most serious lack of data in the CRIC data bank is on linear integrated circuit devices. Some data exist on the 741 type of operational amplifier, hence, the selection of this device for in-depth assessment. Referring to Table 9, the CRIC data bank contains information on the degradation of the open loop voltage gain (A_{VOL}), the common mode rejection ratio (CMRR), the input offset voltage (V_{IO}) and the input offset current (I_{OS}). The types of 741's encountered are the Fairchild 741

(MA741) and the American Microsystems 741 (AMD741). Some data also exist on other operational amplifiers such as the LM101A and the LM108A over fluences from 3×10^{11} up to 1×10^{13} n/cm^2.

3.5 JFET's

No data exist in the CRIC data bank for JFET's.

4. ASSESSMENT OF CANDIDATE CONTROLS

4.1 Transistors

The transistor candidate controls were selected in the theoretical model investigations part of this program (Mission Research Corporation subcontract[1].) For details, the reader is referred to the Mission Research report. The result of the assessment was to select h_{FEO} and f_T as effective transistor-screening parameters for reducing the variability in K_D, the neutron damage factor. Also, the theoretical model identified the base width, the base doping, and configuration controls as critical parameters for process controls.

Harry Diamond Laboratories (HDL) performed a statistical analysis on 156 devices for $V_{CE(SAT)}$ for 2N5399 and other devices and found that the pre-irradiated $V_{CE(SAT)}$ is an effective screen to reduce the variability of the post-irradiation $V_{CE(SAT)}$.

The transistor theoretical model identified the emitter-base breakdown voltage (BV_{EBO}) as a possible effective screen. HDL tested this hypothesis on 40 samples of the 2N3300 and found no correlation between BV_{EBO} and K_D. The reason it was not effective is either (1) the variation in BV_{EBO} between units in a sample is not great enough, or (2) the simplifications (such as uniform instead of Gaussian doping profiles) built into the model do not characterize BV_{EBO} for actual devices.

The question arises whether or not to include hardness assurance controls on $V_{CE(SAT)}$ for transistors. The theoretical model was not able to evaluate the external terminal voltage required to operate the device in saturation. $V_{CE(SAT)}$ is given by the relationship[1]

$$V_{CE(SAT)} = \Delta V_j + V_R$$

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[1] *A. Hart et al, "Parameter Sensitivites for Hardness Assurance: Displacement Effects for Bipolar Transistors," Final Report, Mission Research Corporation/SD-R-20, December 1977.*

where ΔV_j is the difference in applied forward voltage at the two junctions and V_R is the voltage drop across the collector resistance. The theoretical Ebers-Moll expression for ΔV_j is given by[1]

$$\Delta V_j = \frac{KT}{q} \ln \left[\frac{I_{C/h_{FEI}} + I_{B/\alpha_I}}{I_B - I_{C/h_{FE}}} \right]$$

where h_{FEI} is the inverse gain (I_E/I_B), I_B is the forced base current, and

$$\alpha_I = \frac{1 + h_{FEI}}{h_{FEI}} .$$

As can be seen, ΔV_j is slowly varying with current and h_{FE} because of the logarithmic dependence. Also V_R does not change appreciably until high neutron fluences (10^{14} n/cm^2). Thus, for hardness assurance in those situations where small changes in $V_{CE(SAT)}$ are not critical, it makes sense to use a design margin (a CTF of 2 or so) large enough so that the circuit will not fail until the transistor comes out of saturation. The hardness assurance problem is then reduced to controls for K_D, the same controls for the linear amplifier application. Since this can probably be done in most of the design situations encountered, a screen and radiation test on $V_{CE(SAT)}$ is not desired.

The supplier neutron tests listed in the Guideline Document[2] are specified for those levels which produce 20 %, 50 %, and 80%-degradation of h_{FE}. The advantage of this approach is an accurate determination of K_D over the range of interest for the transistor. The disadvantage lies in the different test levels that might be selected by each supplier and the subsequent listing of the data.

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[1] *A. Hart et al, "Parameter Sensitivities for Hardness Assurance: Displacement Effects for Bipolar Transistors," Final Report, Mission Research Corporation/SD-R-20, December 1977.*

[2] *R. Berger, "Hardness Assurance Guidelines for Displacement Effects for Bipolar Devices," IRT 8166-003, March 1978.*

4.2 Reference Diodes

Reference diodes are inherently hard to neutron radiation. The small variations in V_Z caused by neutron radiation are only a part of the larger variations caused by temperature changes. Therefore, the temperature-compensated reference diode is the device of interest for this program. The selection of process controls or screens proved impossible because there were no useful experimental data, nor was there an adequate neutron effects model. The pre-irradiated zener voltage, the forward voltage, and the reverse current were analyzed for the non-temperature-compensated 1N4464 zener; however, no conclusions were reached and, since this was not the device of interest, the investigation was not pursued.

4.3 TTL Digital Integrated Circuits

The TTL family comes in the standard version (SN5400), the high-speed version (SN54H00), the Schottky version (SN5400), the low power version (SN54L00), and the low power Schottky Version (SN54LS00). A detailed physical analysis and modeling effort for TTL circuits was not in the scope of this program, so the main effort was directed to a literature search for state-of-the-art information and an assessment of possible hardness assurance controls based on the transistor theoretical worst-case model developed in this program.[1]

The most sensitive TTL parameters for neutron radiation are the propagation delay times t_{PLH} and t_{PHL} and the output logic levels V_{OL} and V_{OH}. These parameters were investigated and found not to be as effective as I_{SK} (the output sink current) for screening purposes.[7] Since I_{SK} is not in CRIC, the data analysis was limited to that reported by Johnson and Skavland.[7,8]

The output low-level voltage (V_{OL}) was examined for the TTL devices in CRIC with radiation levels around 10^{14} n/cm^2 (RSN54H00, -04, -10, -20, and SN54H00,

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[1] *A. Hart et al, "Parameter Sensitivites for Hardness Assurance: Displacement Effects for Bipolar Transistors," Final Report, Mission Research Corporation/SD-R-20, December 1977.*

[7] *A. Johnson and R. Skavland, "Terminal Measurements for Hardness Assurance in TTL Devices," IEEE Trans. Nucl. Sci., NS-22, 2303, December 1975.*

[8] *A. Johnston and R. Skavland, "Neutron Hardness Assurance Techniques for TTL Integrated Circuits," IEEE Trans. Nucl. Sci., NS-21, 393, December 1974.*

-04, -10, -20). However, V_{OL} requires an accurate measurement to determine small changes and it is non-linear with fluence so it is difficult to assess the data properly.

The output sink current is a good parameter for the radiation tests because it is proportional to the gain of the output transistor.[8] The gain can be calculated from the base current, which is determined for each device by circuit analysis. Knowing the gain of the output transistor leads to the determination of the damage factor, which is independent of the neutron fluence.

The use of I_{SK} as a screen has also been suggested. Some problems which may arise with the use of I_{SK} have been pointed out.[8] These include (1) the fact that circuit variations in V_{BE} and $V_{CE(SAT)}$ are not included, (2) resistor values are dependent on process variation, and (3) since I_{SK} is measured at a fixed base current the collector current can vary between units because of the variability of transistor gains. The variations in items (1), (2), and (3) are probably not important for a first order calculation; a statistical study of modern TTL units produced under controlled-line conditions could fully resolve this issue.

Although there is no direct way to get at the f_T of the transistors within a TTL gate, it can be estimated from t_{PHL}.[8] This estimate involves circuit analysis for each type of device and ignores other contributions to the switching speed, thus it is not an effective screen.

Another approach to hardness assurance is to use a small number of <u>breakout transistors</u> distributed in a uniform pattern over a wafer. Screens can then be applied to the f_T values of these transistors for hardness assurance. The problem with this approach is that it requires an assumption regarding the f_T variation across a wafer. Variations in f_T of discrete transistors across a wafer can approach factors of 2 or 3,[8,9] thus this approach also has its limitations which must be recognized.

Another approach for hardness assurance is the use of <u>special leads</u> to allow a V_{BE} measurement at a fixed collector current on a transistor of interest

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[8] *A. Johnston and R. Skavland, "Neutron Hardness Assurance Techniques for TTL Integrated Circuits," IEEE Trans. Nucl. Sci., <u>NS-21</u>, 393, December 1974.*

[9] *D. Millward and I. Arimura, "Hardness Assurance Through Lot Sampling Homogeneity Studies," IEEE Trans. Nucl. Sci.. <u>NS-20</u>, 354, December 1973.*

(such as the output transistor). This is a dc measurement; it can be made by the manufacturer at the wafer probe level, or it can be added as a special pinout on the packaged device. It would also be useful on devices which are much more complicated than the simple gates studied in this program. A screen on V_{BE} might be effective for neutron hardness assurance,[8] although it must be recognized that V_{BE} measurement is not as sensitive as the f_T measurement because V_{BE} varies with the logarithm of the base width while f_T varies with the square of the base width.

In summary, there is no proven screen for TTL devices which will reduce the neutron response variations. The following screens have been used by various investigators and found to be moderately successful in some applications: I_{SK}, the modified V_{OH} parameter ($V_{OH'}$), f_T measurements on special wafer breakout devices, and V_{BE} using special lead pin-out. The Guideline Document[2] was prepared under the assumption that no special leads or breakout transistors would be available, so this reduced the choice of a candidate screen to I_{SK} and $V_{OH'}$. I_{SK} was chosen based upon a review of the available open literature.

4.4 Operational Amplifiers

The most sensitive parameters to neutron are

(1) The open loop voltage gain, A_{OL}. This parameter decreases with neutron fluence. The best screen identified in the literature for reducing post-irradiation A_{VOL} variability is generally the pre-irradiated A_{VOL}.[10]

(2) Input offset voltage (V_{OS}) and input offset current (I_{OS}). For most operational amplifiers, significant changes in V_{OS} and I_{OS} do not occur until after significant changes in other device parameters.[11] Small changes in the input offset voltage and input offset current measured at low to medium neutron

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[2] *R. Berger, "Hardness Assurance Guidelines for Displacement Effects for Bipolar Devices," IRT 8166-003, March 1978.*

[8] *A. Johnston and R. Skavland, "Neutron Hardness Assurance Techniques for TTL Integrated Circuits," IEEE Trans. Nucl. Sci., NS-21, 393, December 1974.*

[10] *R. Tallon and J. Mullis, "Determination of Operational Amplifier Radiation Hardness from Electrical Parameter Measurem[illegible]," GOMAC Conference Proceedings, June 1974, p. 150.*

[11] *S. A. Johnston, "Application of Operational Amplifiers to Hardened Systems," IEEE Trans. Nucl. Sci., NS-24, 2071, December 1977.*

fluences are difficult to detect and subject therefore to error. Furthermore, Messenger* has pointed out that the low-level changes in V_{OS} and I_{OS} reported in the literature may be due to the total dose accompanying the neutron fluence.

(3) Input bias current, I_B. The input bias current increases with neutron radiation in a non-linear manner. While degradation in I_B occurs before V_{OS} and I_{OS}, it does not change significantly until high neutron fluences are encountered.* The negative power supply current has been identified as a possible screen to a limit post-irradiation variation in ΔI_B.[12]

(4) The output short circuit current degradation can be an important determination of design margin depending on the configuration of the output stage.[11] It is important for the 741 because this device uses a PNP vertical (substrate) transistor in the lower output stage.

(5) The input stage bias current, I_I. The emitter bias current of the input differential stage has been identified as an important screen for hardness assurance.[11] This is because the first stage current determines the gain requirement of the input transistors.

Various authors reviewed in the open literature have had some success with A_{VOL}, I_I, and I_{EE} as screens, but it is not known how effective they are in general. The negative power supply current I_{EE} has only been useful to one author[12] on a small sample of one device, so its value for general usage is in question. Until these screens are proven to be a cost-effective approach to hardness assurance, they should not be listed in the Guideline Document.

Process controls are also to be imposed for hardness assurance purposes. Base widths and base sheet resistivity (base doping) of the internal transistors need to be controlled for the same reason that these parameters need to be controlled in discrete units. In addition, configuration controls are important. For example, if the positive or negative supply rails pass close by the input leads in a topological asymmetrical fashion then the total dose radiation which accompanies the neutron radiation can cause increases in surface conductance which will lead to a rapid increase in leakage current.*

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*Private conversation with G. Messenger.

[11] *S. A. Johnston, "Application of Operational Amplifiers to Hardened Systems," IEEE Trans. Nucl. Sci., NS-24, 2071, December 1977.*

[12] *I. Arimura et al., "A Study of Electronics Radiation Hardened Assurance Techniques," AFWL-TR-73-134, January 1974.*

4.5 JFET's

The most sensitive JFET parameters to neutron radiation are, in order of sensitivity;[13] the source-to-drain current (I_{DSS}), the transconductance (g_m), and the pinch-off voltage (V_p).

The parameters $r_{d(on)}$ and g_m have been identified as possible screens for post-irradiation g_m and I_{DSS}. Since JFET's are very hard with respect to neutrons (I_{DSS} does not degrade significantly until 1×10^{15} n/cm^2) no supplier for radiation tests are recommended in the final Guideline Document so as not to drive up the price of an item that is inherently hard.

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[13] *R. Donovan et al., "A Survey of the Vulnerability of Contemporary Semiconductor Components to Nuclear Radiation," AFAL-TR-74-61, June 1974.*

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APPENDIX A
HARDNESS MAINTENANCE FOR SYSTEMS

Hardness Maintenance is a term that refers to the procedures applied during the system operational phase to insure that the system's operational procedures, maintenance requirements, and aging characteristics do not degrade the systems operational capability below mission completion levels. Hardness Surveillance is a term that refers to the periodic test and inspection requirements performed during the operational phase to verify the adequacy of the hardness maintenance program.

Hardness maintenance is carried out during the system operational phase (see Figure A-1): however, concepts and approaches must be generated during the design and development phases. System operational and maintenance procedures should address the hardness critical items identified in the Hardness Assurance program so that maintenance personnel will not inadvertently degrade the nuclear hardness of the system. Information should be provided so that Technical Orders will be written with these requirements in mind and written so as to be understandable to maintenance personnel.

Special markings which may be needed on the equipment to insure proper hardness maintenance procedures (stickers, special component marking, etc.) should be specified as part of the required documentation. Also, management procedures should be identified which are necessary to configuration, parts, and quality control for hardness maintenance.

Hardness critical items should be subjected to analysis in order to determine if the aging characteristics of those items will degrade the system operational capability to the point where mission completion may not be accomplished.

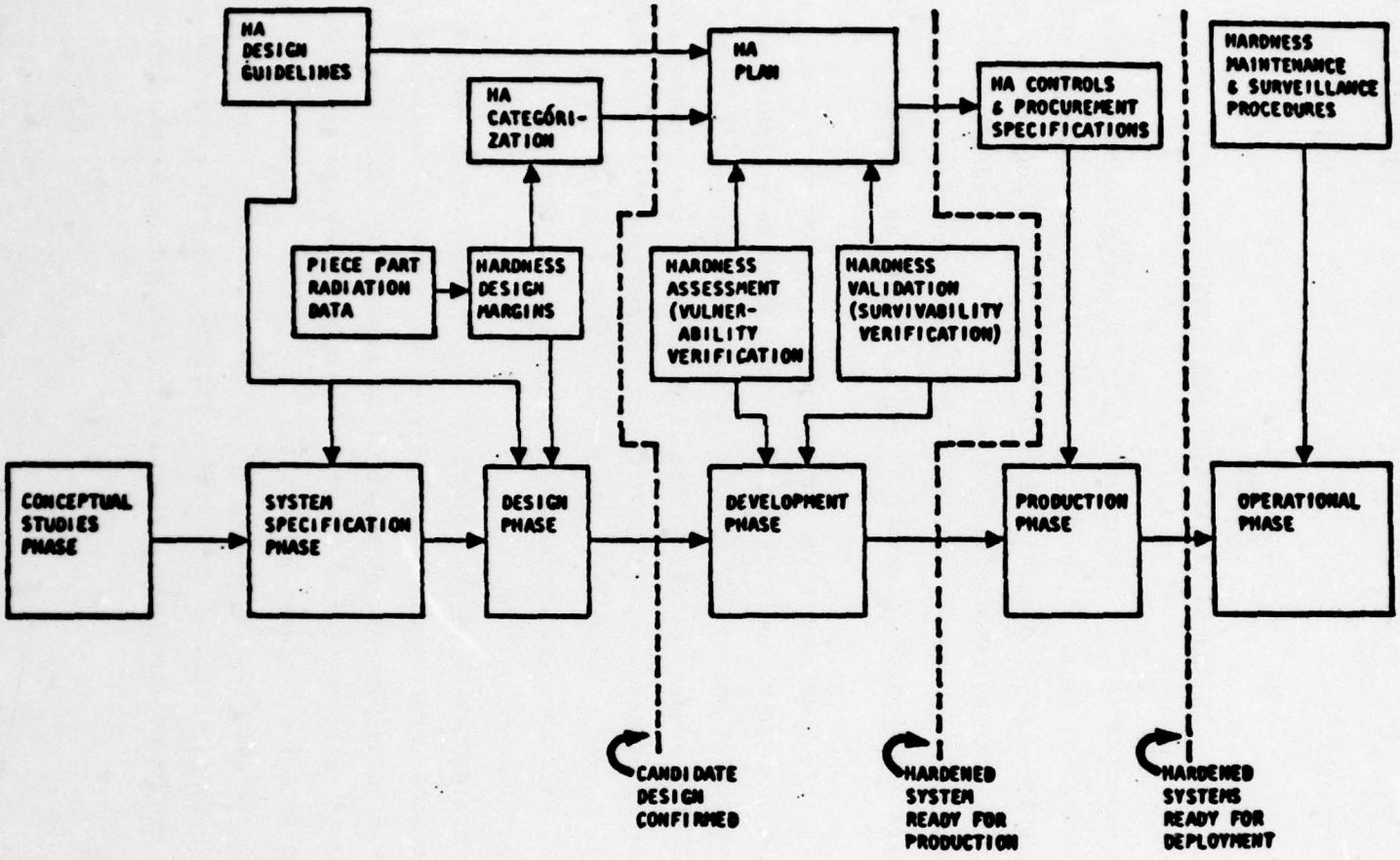

Figure A-1. Hardness Assurance (HA), Hardness Surveillance (HS), Hardness Assessment, and Hardness Validation Flow Diagram

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