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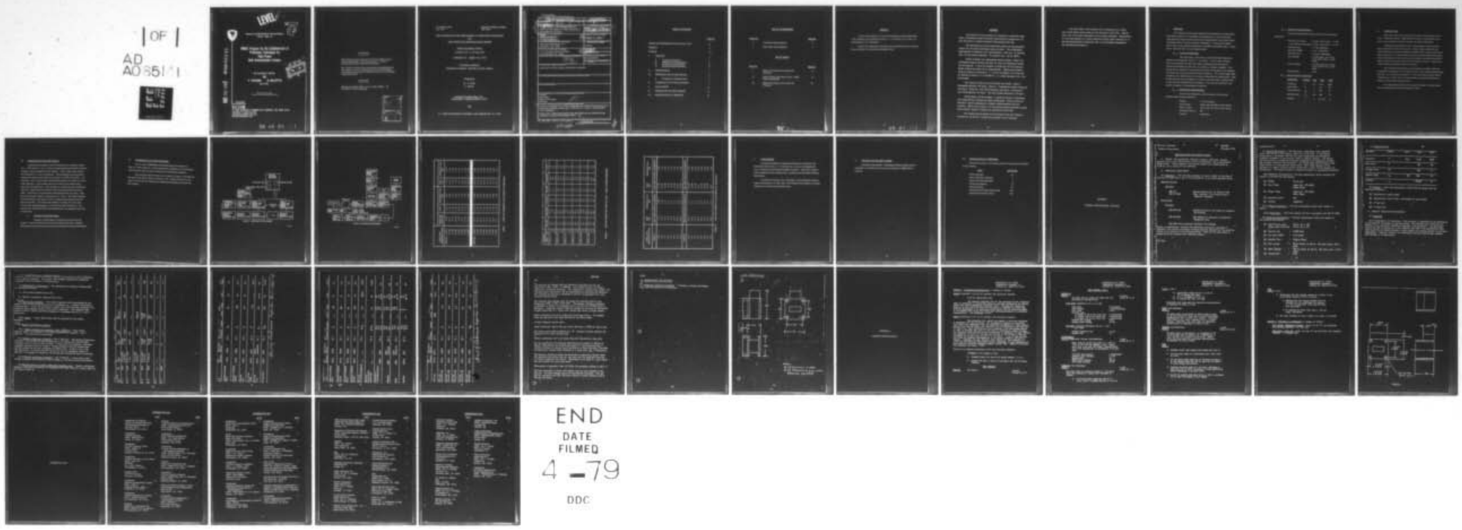

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Research and Development Technical Report
ECOM - 0039 - 8

MM&T Program for the Establishment of Production Techniques for High Power Bulk Semiconductor Limiters

8TH QUARTERLY REPORT

By

Y. ANAND R. BILOTTA

JULY 1978

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MM&T PROGRAM FOR THE ESTABLISHMENT OF PRODUCTION TECHNIQUES FOR HIGH POWER BULK SEMICONDUCTOR LIMITERS

EIGHTH QUARTERLY REPORT

23 March 1978 to 22 June 1978

CONTRACT NO. DAAB07-76-C-0039

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FOR

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

X-band bulk limiters of 3.5 mils in thickness are being fabricated using relatively low resistivity silicon, ρ = 4,000 ohm-cm, p-type, uncompensated ⟨111⟩ orientation.

Twenty (20) Confirmatory Samples were fabricated and are presently being subjected to various environmental tests.

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ABSTRACT

X-band bulk limiters of 3.5 mils in thickness are being fabricated using relatively low resistivity silicon, ρ = 4,000 ohm-cm, p-type, uncompensated ⟨111⟩ orientation.

Twenty (20) Confirmatory Samples were fabricated and are presently being subjected to various environmental tests.

PURPOSE

The objective of this program is to establish a production capability to manufacture High Power Bulk Semiconductor Limiters per U.S. Army Electronics Command Technical Requirements SCS-486.

The specification covers X-band high power bulk semiconductor limiter and low power multistage clean-up limiter. Four fundamental requirements are detailed in the specifications. They are, (1) recovery time, (2) high power capability, (3) insertion loss, and (4) VSWR.

A total of fifteen (15) engineering sample limiters, twenty (20) confirmatory sample limiters and fifty (50) pilot run production limiters will be supplied. A pilot line capable of producing 100 bulk semiconductor limiters per month will be demonstrated. Reports and documentation as required in Sections E, F, G and H of DAAB07-76-Q-0040 and as detailed in Section 3.5 of ECIPPR No. 15, dated December 1976, will be provided.

The program divides into the following four phases, Phase I - Engineering Samples (300 days), Phase II - Confirmatory Sample Production (240 days), Phase III - Pilot Line Production (180 days), and Phase IV - Final Documentation (30 days). The total program duration is 750 days.

During Phase I of this program, a number of factors in fabricating bulk semiconductor limiters are being investigated. These include iris formation, circuit configuration, material characterization and chip mounting. Efforts during Phase I will be directed toward selecting a single limiter design capable of meeting the objectives of SCS-486.

The optimum device design will be chosen at the end of Phase I. In Phases II, III and IV, a single device design will be produced.

The major effort of this program will be realization of a single bulk limiter design which meets all the objectives of SCS-486. Individually, any of the goals described can be currently obtained. Recognizably, it is the development of a single component design which achieves all of the desired performance parameters that is the formidable engineering and manufacturing endeavor.

I. OBJECTIVE

The objective of the current Manufacturing Methods and Technology Engineering program is to establish the producibility of the X-band bulk semiconductor limiter and the X-band bulk semiconductor lower power diode multistage limiter by mass production techniques. Achieving the performance goals of the program represents a formidable engineering task. These goals, from SCS-486, are summarized below.

A. Function Description

The high power, solid state, limiter described herein will operate in the frequency band 9.0 - 9.65 GHz. A multi-stage configuration is acceptable with the first stage incorporating the principle of avalanche breakdown of near-intrinsic silicon to achieve isolation. This device will be mounted in a fixed tuned resonant waveguide cavity designed to provide the necessary avalanche field conditions. The second stage shall be either a bulk effect device or a common semiconductor diode limiter. Both limiter devices will be mounted in a common structure and no external bias or drive will be necessary for its operation. The receiver protector is required to operate in unpressurized conditions.

B. Mechanical Characteristics

The bulk semiconductor limiter structure will have the following performance objectives:

Weight	:	7.0 oz maximum
Input Flange	:	mates with UG-40B/U choke flange
Output Flange	:	mates with UG-135/U cover flange
Mounting Position	:	any
Cooling	:	conduction

C. Electrical Characteristics

The bulk semiconductor limiter will have the following objectives:

Peak RF Input Power	: 30 kW, Duty Cycle = 0.001
1 μsec Pulses Continuous	: 10 kW, Duty Cycle = 0.001
Insertion Loss	: 0.7 dB (maximum)
Low Level VSWR	: 1.4:1 (maximum)
Recovery Time	: 0.8 μsec (maximum)
Flat Leakage	: 50 mW (max), for 30 kW, 0.001 Duty Cycle, 1 μsec pulse
Spike Leakage	: 750 mW (max), for 30 kW, 0.001 Duty Cycle, 1 μsec pulse
External Bias	: none

D. Absolute Rating Objectives

PARAMETER	SYMBOL	MIN	MAX	UNIT
Frequency	F	9.0	9.65	GHz
Peak Power	P	--	30	kW
Average Power	P_a	--	100	W
Ambient Temp.	T_A	-55	+85	°C
Altitude	--	--	50,000	ft

II. INTRODUCTION

This report covers the period from 23 March 1978 through 22 June 1978. During this period, semiconductor work was concentrated in the areas of semiconductor wafer processing and device fabrication.

Significant improvements in the semiconductor processing have been accomplished during this quarter. Silicon wafer resistivity and wafer thickness are being optimized to fabricate high quality bulk limiters with a good yield. A new passivation scheme (plasma nitride) and plasma etching techniques (to etch oxide and also metals) are being evaluated in order to reduce the insertion loss of bulk limiters and also to improve the power handling capability of the bulk limiters.

The Contract Specifications were amended on 28 April 1978 and is attached in Appendix II. (For reference only, the original specifications, SCS-486, can be found in Appendix I.) The Confirmatory Sample testing commenced on 15 May 1978, and bulk limiters are presently being subjected to various environmental tests.

The subsequent sections of this report describe in greater detail the work performed and results achieved to date.

III. FABRICATION AND RF TEST RESULTS

During the last quarter, four (4) relatively low resistivity wafers (ρ = 4,000 ohm-cm, ⟨111⟩, p-type uncompensated) from Wacker Chemical Company were processed for bulk limiters. These wafers were etched and polished to 3.5 mils in thickness. The phosphorous and boron diffusions were done on both sides of the wafers at 1000°C and 950°C, respectively. The 3/4 mil square checkerboard pattern was used prior to the boron diffusion. Boron nitride source was used as the dopant source during the boron diffusion. Both surfaces of a wafer were then metallized with 400 - 1000 Å layer of titanium (10%) and tungsten (90%) alloy and 2000 - 3000 Å layer of gold and then electroplated with pure gold. Both the surfaces were plated to a thickness of 3.0 mils. The active elements area were defined by etching 10 mils in diameter gold posts on the top side of the wafer. The posts were etched to a height of 3 mils using conventional photolithographic and photoresist flow techniques. The silicon mesa etching process was performed when the elements were still in wafer form.

A. Evaluation of Stamped Irises

Presently, these wafers are being wire cut into 40 mil squares. The bulk limiter chips will be mounted in low cost "stamped" gold plated copper X-band irises and will be tested for their RF performance.

IV. CALIBRATION OF RF TEST EQUIPMENT

Mr. G. Hall of ERADCOM visited Microwave Associates on May 16, 1978 to May 18, 1978 to witness the calibration of low and high power test kits and low level testing of the Confirmatory Samples.

Low and high power test set ups are shown in Figure 1 and Figure 2, and the RF test data is given in Tables I to III. These test kits will be used to RF test the bulk limiters for Confirmatory Samples and pilot line bulk limiters.

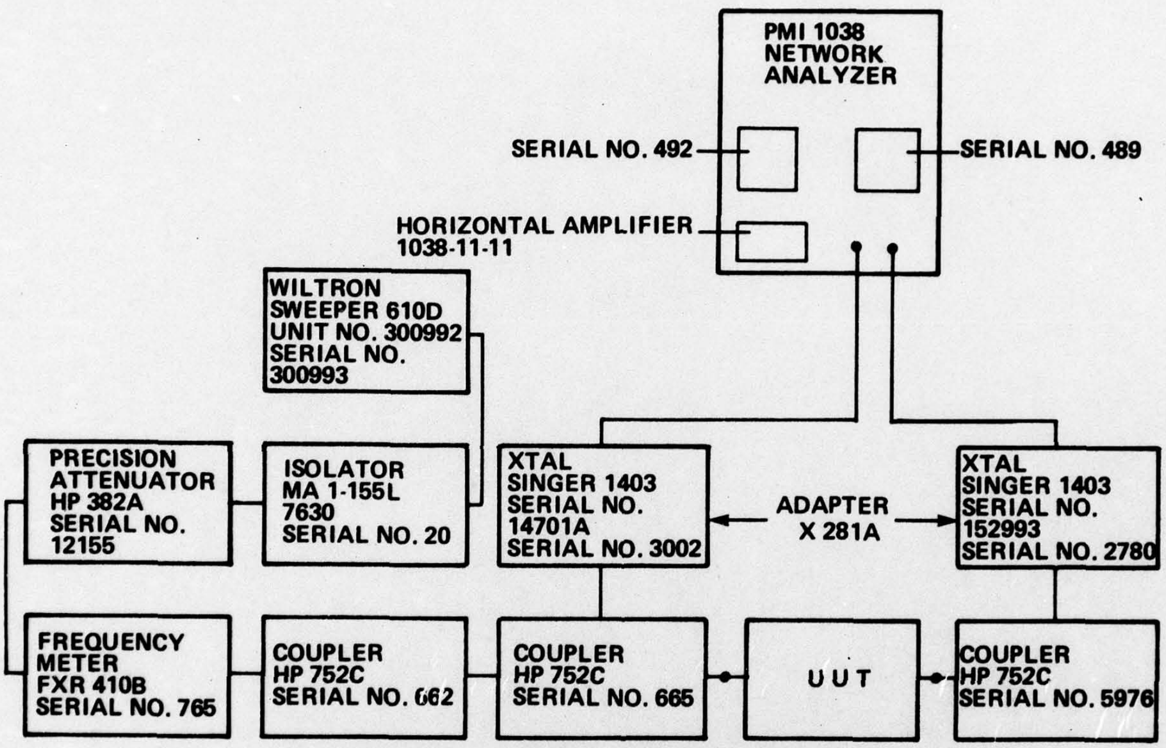

FIGURE 1. LOW POWER TEST EQUIPMENT

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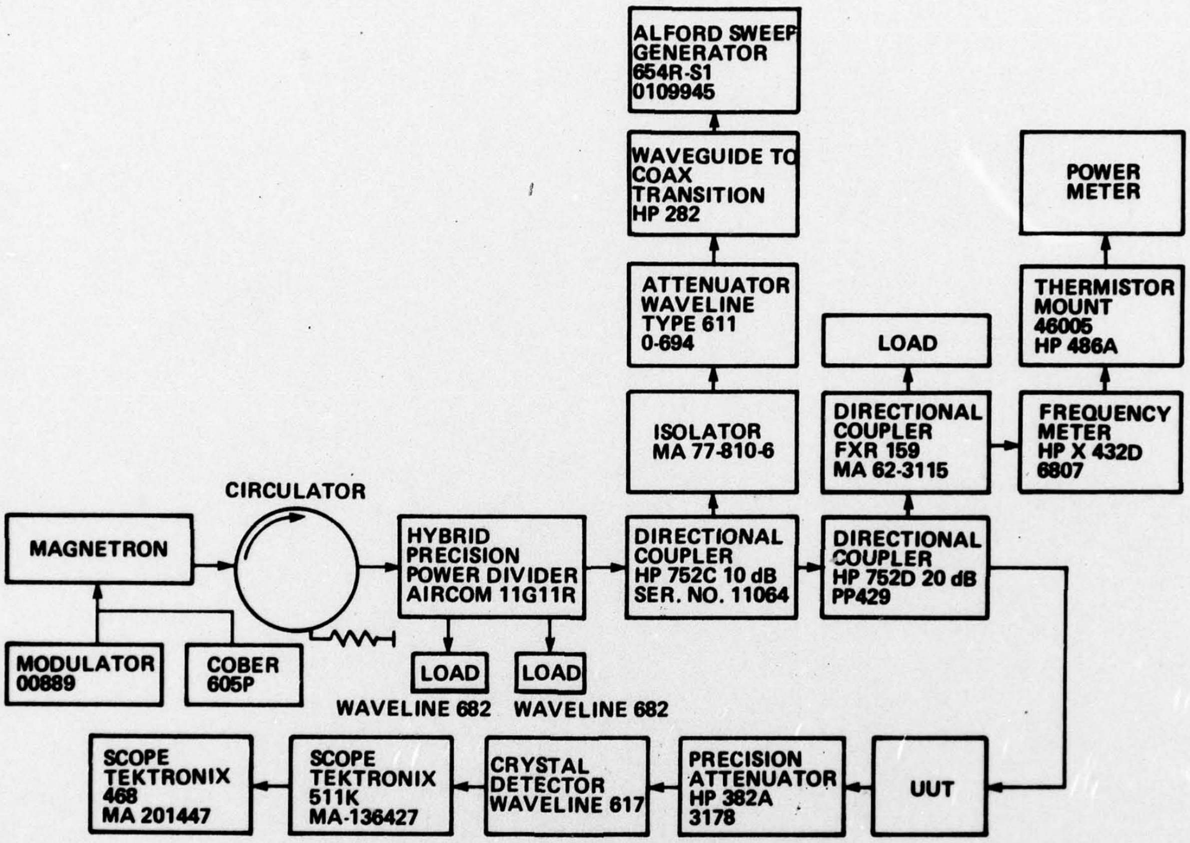


FIGURE 2. HIGH POWER TEST EQUIPMENT

D-16576

UNIT # AND FREQUENCY (GHz)	REFLECTED ATTN (dB)	VSWR	INSERTION LOSS (dB)	VSWR (dB)	INSERTION LOSS (dB)
UNIT #1: 8.900	8.50	2.20	1.60	8.2	1.60
9.000	12.0	1.67	0.95	11.2	1.10
9.100	9.75	1.95	1.10	10.6	1.00
9.200	10.70	1.83	1.00	9.2	1.10
9.300	9.50	2.00	1.10	9.7	1.10
9.400	12.0	1.67	1.00	10.4	1.10
9.500	11.70	1.70	1.00	13.5	1.00
9.600	14.10	1.50	1.00	15.6	0.90
UNIT #2: 8.900	17.7	1.31	0.85	15.6	1.00
9.000	12.6	1.60	0.85	12.8	0.90
9.100	13.6	1.70	0.90	12.0	0.90
9.200	11.7	1.70	0.90	12.0	0.90
9.300	15.3	1.42	0.80	15.6	0.90
9.400	15.0	1.22	0.90	15.6	0.90
9.500	19.9	1.22	0.90	17.5	0.90
9.600	12.7	1.59	1.00	13.5	1.10

TABLE I VSWR AND INSERTION LOSS VERSUS RF FREQUENCY

UNIT # AND FREQUENCY/POWER (GHz) / (kW)	SPIKE LEAKAGE ATTN (dB)	SPIKE LEAKAGE POWER (mW)	SPIKE WIDTH 3 dB (nsec)	FLAT LEAKAGE ATTN (dB)	FLAT LEAKAGE POWER (mW)	RECOVERY TIME (μsec)
UNIT #1: 9.375/1.0	16.6	45.71	12.0	11.6	14.45	1.50
5.0	18.7	74.13	10.0	12.1	16.22	2.10
10.0	22.2	166.0	10.0	12.3	16.98	2.50
UNIT #2: 9.375/1.0	20.5	112.2	35.0	16.0	39.81	1.80
5.0	23.0	199.5	20.0	18.2	66.07	2.40
10.0	23.2	208.9	30.0	19.5	89.13	2.80
UNIT #1: 9.00 /1.0	18.8	75.86	20.0	14.7	29.51	1.25
5.0	21.6	144.5	15.0	16.0	39.81	1.50
10.0	23.5	223.9	10.0	16.6	45.71	2.25
UNIT #2: 9.00 /1.0	21.0	125.9	20.0	16.5	44.67	1.75
5.0	24.2	263.0	16.0	17.4	54.95	2.35
10.0	25.0	316.2	16.0	18.1	64.57	2.85
UNIT #1: 9.600/1.0	17.7	58.85	30.0	13.0	19.95	1.60
5.0	19.9	97.72	20.0	15.8	38.02	2.20
10.0	21.0	125.9	11.0	16.7	46.77	2.50
UNIT #2: 9.600/1.0	23.0	199.5	50.0	18.9	77.62	1.80
5.0	24.2	263.0	10.0	22.3	169.8	2.60
10.0	24.8	302.0	10.0	22.7	186.2	3.20

TABLE II HIGH RF POWER TEST DATA OF BULK - DIODE LIMITER ASSEMBLIES

UNIT # AND FREQUENCY (GHz)	VSWR (dB)	INSERTION LOSS (dB)	VSWR (dB)	INSERTION LOSS (dB)
UNIT # 1	DATA TAKEN AFTER CALIBRATION		DATA TAKEN BEFORE CALIBRATION	
8.9	7.6	1.60	8.20	1.60
9.0	11.6	1.10	11.20	1.10
9.1	11.0	1.0	10.60	1.00
9.2	9.6	1.0	9.20	1.10
9.3	9.8	1.0	9.70	1.10
9.4	10.7	1.0	10.40	1.10
9.5	13.6	0.9	13.50	1.00
9.6	15.7	0.8	15.60	0.90
UNIT # 2	DATA TAKEN AFTER CALIBRATION		DATA TAKEN BEFORE CALIBRATION	
8.9	16.1	1.1	15.60	1.00
9.0	13.1	1.1	12.80	0.90
9.1	11.6	1.1	11.90	0.90
9.2	12.4	1.0	12.0	0.90
9.3	13.5	1.0	13.20	0.90
9.4	16.6	0.9	15.60	0.90
9.5	16.9	1.0	17.50	0.90
9.6	14.3	1.1	13.5	1.10

TABLE III VSWR AND INSERTION LOSS VERSUS RF FREQUENCY

V. CONCLUSIONS

X-band bulk limiters are being fabricated using relatively low resistivity silicon with ρ = 4,000 ohm-cm, p-type, uncompensated ⟨111⟩ orientation from Wacker Chemical Company. These bulk limiters will be tested for their insertion loss, recovery time and power handling performance.

Confirmatory Samples were fabricated, and Confirmatory Sample testing commenced on 15 May 1978, and presently bulk limiters are being subjected to various environmental tests.

VI. PROGRAM FOR THE NEXT QUARTER

During the next quarter, Confirmatory Sample testing will be completed, and twenty (20) units will be shipped to ERADCOM on schedule.

VII. IDENTIFICATION OF PERSONNEL

During this quarter, the following technical personnel contributed to this program.

TITLE	MANHOURS
Project Manager	20
Silicon Materials Manager	5
Senior Processing Engineer	5
Processing Engineer	10
Limiter Engineer	50
Engineering Assistant (Fabrication)	845
Engineering Assistant (Test)	625

APPENDIX I

ORIGINAL SPECIFICATIONS (SCS-486)

Electronic Command SCS-486

Technical Requirements 28 March 1975

High Power Bulk Semiconductor Limiter

1. SCOPE: This specification describes a passive, solid state, receiver protector using a bulk semiconductor limiter in combination with a semiconductor diode limiter. Limiter operation will provide isolation from x-Band pulses up to 30 kw over a variety of test conditions.

2. APPLICABLE DOCUMENTS

2.1 Documents. - The following documents, of issue in effect on the date of invitation for bids, form a part of this specification to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-E-1	General Specification for Electron Tube
MIL-P-11268	Parts, Materials, and Processes Used in Electronic Equipment

STANDARDS

MILITARY

MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-202	Test Methods for Electronic and Electrical Components Parts
MIL-STD-1311A	Microwave Oscillator Test Methods

(Copies of specifications, standards and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer. Both the title and number of symbol should be stipulated when requesting copies.)

FSC 5961

REQUIREMENTS:

3.1 Function Description. - The high power, solid state, limiter specified herein will operate in the frequency band 9.0 - 9.65 GHZ. A multi-stage configuration is acceptable with the first stage incorporating the principle of avalanche breakdown of near-intrinsic silicon to achieve isolation. This device will be mounted in a fixed turned resonant waveguide cavity designed to provide the necessary avalanche field conditions. The second stage shall be either a bulk effect device or a semiconductor diode limiter. Both limiter devices will be mounted in a common structure and no external bias or drive will be necessary for its operation. The receiver protector is required to operate in unpressurized conditions.

3.2 Mechanical Characteristics. - The bulk semiconductor limiter structure will conform to the following requirements:

(a)	Weight	20 oz max
(b)	Input flange	mates with UG-40B/U choke flange
(c)	Output flange	mates with UG-135/U cover flange
(d)	Mounting position	any
(e)	Cooling	conduction

3.2.1 Physical Dimensions. - The bulk semiconductor limiter shall conform to Figure 1.

3.2.2 Construction. - Parts and materials will be in accordance with MIL-P-11268.

3.3 Electrical characteristics. - The bulk semiconductor limiter will conform to the following requirements:

(a)	Peak Rf Input power, 1 μsec pulses continuous :	30 kw, Du = .001 10 kw, Du = .01
(b)	Insertion Loss :	0.7dB (max)
(c)	Low Level VSWR :	1.4:1 (max)
(d)	Recovery Time :	0.8 μsec (max)
(e)	Flat Leakage :	50 mw (max), for 30 kw, .001 duty cycle, 1 μsec pulse
(f)	Spike Leakage :	750 mw (max), for 30 kw, .001 duty cycle, 1 μsec pulse
(g)	external bias :	none

3.4 Absolute Ratings

Parameter	Symbol	Min	Max	Unit
Frequency	F	9.0	9.65	GHZ
Peak Power	P		30	kw
Average Power	Pa		100	w
Ambient Temp.	T_A	-55	+85	°C
Altitude	—		50,000	ft

3.5 Marking. - Each bulk semiconductor limiter shall be marked with the following information:

(a) Manufacturer's model number

(b) Manufacturer's serial number, individually for each limiter.

(c) rf input port.

(d) rf output port.

4. QUALITY ASSURANCE PROVISIONS

4.1 Inspection.

4.1.1 Responsibility for inspection. - The contractor is responsible for the performance of all inspection requirements as specified herein. The contractor may utilize his own facilities or any commercial laboratory acceptable to the government. The government reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements. Inspection records of the examinations and tests shall be kept complete and available to the government.

4.1.2 Test equipment and inspection facilities. - Test equipment and inspection facilities shall be of sufficient accuracy, quality, and quantity to permit performance of the required inspection. The supplier shall establish calibration of inspection equipment to the satisfaction of the government.

4.2 Classification of inspection. - The examination and testing of limiters shall be classified as follows:

a. First article inspection (see 4.3).

b. Quality conformance inspection (see 4.4.).

4.3 First article inspection. - First article inspection shall be performed by the supplier, after award of contract and prior to production at a location acceptable to the government. It shall be performed on sample units which have been produced with equipment and procedures which will be used in production. This inspection shall consist of QCI-1, QCI-2 and QCI-3 inspection in accordance with 4.4.1, 4.4.2 and 4.4.3.

4.3.1 Sample. - Twenty (20) limiters shall be submitted for first article inspection.

4.4 Quality Conformance Inspection.

4.4.1 Quality conformance inspection - Part 1 (QCI-1). - Every limiter shall be tested in all positions of the Quality Conformance Inspection - Part 1 (QCI-1). No failures shall be permitted.

4.4.2 Quality conformance inspection - Part 2 (QCI-2). - The Quality Conformance Inspection - Part 2 (QCI-2) shall be performed in accordance with MIL-STD-105, Inspection Level S1 with an AQL of 6.5%. In the event of lot rejection, tightened inspection procedures shall be invoked. Normal inspection shall be resumed when two (2) consecutive lots have conformed with QCI-2 tests. If the lot size is less than 50 limiters, the sample size shall be one (1) with an acceptance number of zero (0). For purposes of inspection, the lot size shall be one (1) month's production.

4.4.3 Quality conformance inspection - Part 3 (OCI-3). - Three limiters shall undergo continuous life testing for a min. of 2500 hrs. No failures shall be permitted.

4.5 Detailed listings of quality conformance inspection tests. - Quality conformance inspection tests shall be conducted in accordance with Table I (QCI-1), Table II (QCI-2), and Table III (QCI-3).

4.6 Test Conditions

F[illegible]meter Unit	T_A °C	Fo GHZ	Po Watts	[illegible] μ sec	P_{RR} Pulses/sec	Du	[illegible] Watts
TC 1	25±3	9.0, 9.375, 9.65±.01	30,000 ± 500	1.0±0.1	1000±25	.001	30
TC 2	25±3	9.0 – 9.65 ± .01	0.001	CW	—	—	—
TC 3	25±3	9.0, 9.375, 9.65±.01	—	1.0±0.1	1000±25	.001	—
TC 4	25±3	9.0, 9.375, 9.65±.01	10,000 ± 250	1.0±0.1	10,000 ±150	.01	100
TC 5	25±3	9.375±.01	30,000 ± 500	1.±0.1	1000 ±25	.001	30
TC 6	—	—	0	—	—	—	—
TC 7	25±3	—	0	—	—	—	—

	Mil Standard	Application Method	Test Condition	Symbol	Limits Lower	Limits Upper	Units	Notes
Maximum Leakage (flat)	1311A	4452A	TC 1	P_f		50	mw	1,3
Maximum Leakage (spike)	1311A	4452A	TC 1	P_s		750	mw	2,3
Insertion Loss	1311A	4416	TC 2	Li		0.7	db	3,4
Low Level VSWR	1311A	4473	TC 2	σ		1.4:1	—	3,4,5
Recovery Time	1311A	4471B (Method B)	TC 1	τ		0.8	μsec	3,8
Firing Power	1311A	4496	TC 3	P_{FR}		150	mw	3,6,8

Quality Conformance Inspection - Part 1 (QC 1-1)

	Mil Standard	Application Method	Test Condition	Symbol	Lower	Upper	Unit	No
Maximum Leakage (flat)	1311A	4452A	TC 1	P_f	—	100	W	1,7
Maximum Leakage (spike)	1311A	4452A	TC 1	P_s	—	400	W	2,7
Maximum Leakage (flat)	1311A	4452A	TC 4	P_f	—	50	mw	1,3
Maximum Leakage (spike)	1311A	4452A	TC 4	P_s	—	750	mw	2,3
Recovery Characteristic(phase)	—	—	TC 5	ΔR_p	—	0.5	degree	3,8,9
Recovery Characteristic (amplitude)	—	—	TC 5	ΔR_a	—	0.1	db	3,8,9
Temperature Cycling(non-oper.)	1131A	1027	TC 6	ΔL_i Δf_s $\Delta \tau$	—	0.2 100 0,2	db mw μ sec	10
Vibration	202E	204C Method A	TC 7	ΔL_i Δf_s $\Delta \tau$	—	0.2 100 0.2	db mw μ sec	10
Shock	202E	213B Method G	TC 7	ΔL_i Δf_s $\Delta \tau$	—	0.2 100 0.2	db mw μ sec	10
Humitity	1311A	1011	TC 6	ΔL_i Δf_s $\Delta \tau$	—	0 0 0	db mw μ sec	10

	Mil Standard	Application Method	Test Condition	Symbol	Lower	Upper	Unit	Notes
Life Test	1311A	4551A	TC 5	t	2500		hours	11
Life Test End-Point (1)	1311A	4452A	TC 1	P_s		1.0	watt	2,3
Life Test End-Point (2)	1311A	4416	TC 2	L_I		0.9	db	3,4
Life Test End-Point (3)	1311A	4471B	TC 1	τ		1.0	μ sec	3
Life Test End-Point (4)	1311A	4452A	TC 1	P_f		75	mw	1,3
Life Test End-Point (5)	1311A	4496	—	P_{FR}		170	mw	3,6

Quality Conformance Inspection - Part 2 (QC111-3)

:ES:

Max maximum flat leakage shall not exceed the specified limits for test frequencies 9 000, 9.375, .9.650GHZ. The incident Rf pulse will have a risetime 50 nanoseconds maximum. Test configuration reference figure 4452 - 1b. The peak power measurement will be accomplished by calibrating the deflection of a sampling oscilloscope as described in section 3.2 paragraphs 3.2.1 and 3.2.2 of Mil-Std-1311A.

The maximum spike leakage shall not exceed the specified limits for test frequencies 9.000, 9.375, 9.650 GHZ. Oscilloscope calibration technique as described in section 3.2 paragraphs 3.2.1 and 3.2.2 of Mil-Std-1311A is applicable. Amplitude variation shall be recorded by observing the distribution of spike amplitudes for 1 minute time through open shutter of scope camera.

Quality conformance test to be made using multi-stage limiter. For example using the high power bulk stage followed by the limiter diode.

A swept frequency may be used.

Match Termination used in this test circuit shall have a VSWR of 1.05 or less.

The firming power shall be defined as a dB increase of limiter insertion loss compared to the "cold" insertion loss.

Quality conformance test to be made using bulk semiconductor stage only.

For this specification the following abbreviations and symbols in addition to MIL-E-1 abbreviations and symbols shall apply; τ = time (recovery), ΔR_p = variation of phase on recovery (total deviation at a fired time), ΔR_a = variation of amplitude on recovery (total deviation at a fixed time), P_{FR} = firing power.

The maximum variation in phase and amplitude as measured by dynamic phase and amplitude test facility shall not vary more than the specified limits over a 1 minute integration time period. Measurement to be made at a point 5μsec from the cessation of 1μsec input pulse.

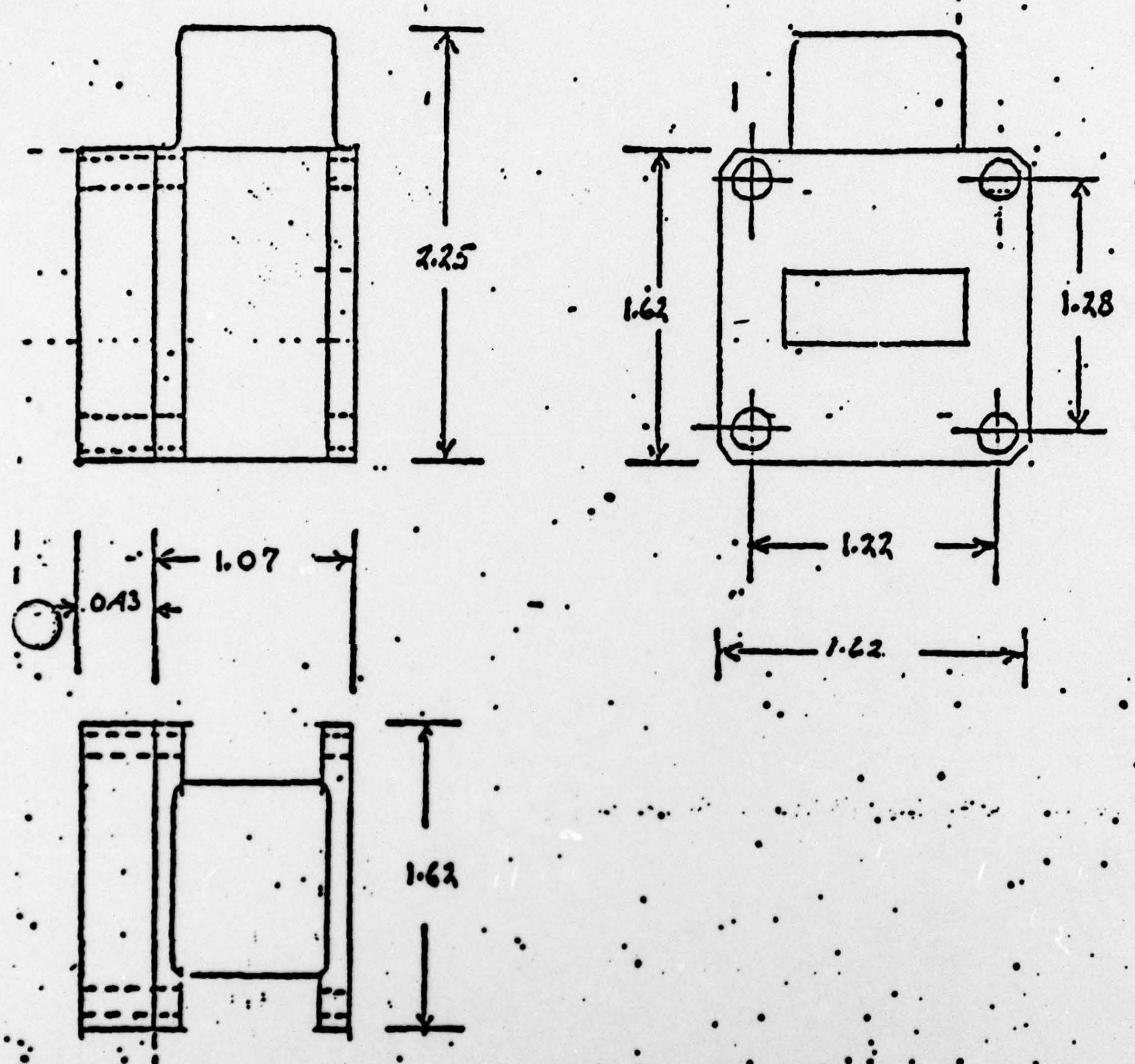
Measurement of parameters cited will follow the procedures outlined in QCI -1.

The bulk semiconductor limiter shall operate over the entire duration of the life test. The spike leakage (P_s) will be periodically monitored. Life test will be interrupted each 720 ± 20 hours intervals to permit testing of end of life test end points.

5. PREPARATION FOR DELIVERY

5.1 Packaging, Packing and Marking. - Packaging, packing and package marking shall be specified in the contract.

LINE DRAWING



NOTES:

a) all dimensions in inches

b) all tolerances ± 0.01 unless otherwise specified

APPENDIX II

MODIFIED SPECIFICATIONS

Modification No. P00001
Supplemental Agreement to
Contract No. DAAB07-76-C-0039

SECTION F, Description/Specifications is amended as follows:

Delete Subsection F.48.2 in its entirety and substitute therefor:

"Test for Operational Life:

The expected operating life for the production BL-LPL Assemblies shall be determined by calculation using the operating temperature and silicon device life-versus-temperature experience curve. The mean life expectancy shall be no less than 2500 hours and this shall be confirmed by direct high RF power measurement or by calculation using direct high RF power measurement of the burnout point along with established derating procedures for microwave semiconductors. (See paragraph F.49.6)"

Delete Subsection F.49.4 in its entirety and substitute therefor:

"The contractor will subject the samples to the tests specified in paragraph 6 of this provision. The confirmatory samples and associated test report must demonstrate that all applicable requirements of these specifications have been met before the contractor will be authorized to proceed with the pilot run. This authorization will be granted by the contracting officer. At least 15 calendar days prior to the start of confirmatory samples testing, the contractor shall furnish written notification to Commander, US Army, ERADCOM, Fort Monmouth, NJ 07703, of the time and location of the testing so that the Government may witness such testing if it so elects. A copy of this notification shall be furnished simultaneously to the project engineer addressed as follows: Commander, US Army ERADCOM, ATTN: DELSD-D-PC, Fort Monmouth, NJ 07703, and the Procuring Contracting Officer, Commander, US Army Communications and Electronics Materiel Readiness Command, CERCOM, ATTN: DRSEL-PC-C-CS-2(BAC) Fort Monmouth, New Jersey 07703."

Delete in its entirety Subsection F.49.6 and substitute therefor:

Paragraph F.49.6 change to read:

"a. Randomly number all units with serial numbers 1 to 20.

b. Subject the unit to tests in accordance with the following schedule.

TEST SCHEDULE

PHYSICAL	Per Figure 1	20 each Serial #1 to 20

TEST SCHEDULE (Cont.)

ELECTRICAL
Group A — 20 Units, Serial #1 to 20

All units will be tested and shall meet the following RF specifications.

High Power (measured at 9.3 ± 0.3 GH_z)

Peak Power	20 kilowatts
Pulse Length	0.25 microseconds
Duty Cycle	0.001
Recovery time	
to within 10 dB of low level loss	1 microsecond
to within 6 dB of low level loss	2 microsecond
to within 3 dB of low level loss	3 microsecond
Maximum Flat Leakage	50 mw
Maximum Spike Leakage	750 mw

Low Power (measured throughout the 9.0 - 9.65 GH_z range)

Maximum Insertion Loss	1.3 dB
Maximum VSWR	1.7

ENVIRONMENTAL
Group B Temperature Cycling (non-operating) — 3 each, Serial #1, 2, 3

Units shall be cycled from 25°C to + 100°C to -55°C to 25°C for one complete cycle. Thereafter they shall meet the Group A specifications above with degradations in performance of no more than:

Recovery time Increase	1 microsecond
Insertion Loss Increase	0.3 dB
Maximum VSWR	2.0
Spike Power Increase	200 mw
Flat Power Increase	25 mw

VIBRATION (non operating)
Group C — 3 each, Serial #4, 5, 6

The units shall be securely mounted to a vibration table and subjected to simple sine vibration as follows:

(a) 0.06 inch double amplitude from 20 to 26 Hz, and 2 G minimum from 26 to 2,000 Hz.

Group C (Cont.)

(b) Logarithmic sweep from 20 to 2,000 Hz for 15 minutes per sweep.
(c) or 2.5 G minimum at 50 $\pm$ 5 Hz.
(d) 15 minutes per axis, two axes.

Thereafter they shall meet the electrical specifications as explained in Group B, above.

SHOCK (non operating)
Group D

3 each
Serial #7, 8, 9

The units shall be subjected to three shocks in each of the two directions along each of the three mutually perpendicular axis (a total of 18 shocks). The shock level shall be 25 G with a duration of 11 $\pm$ 1 milliseconds. Thereafter they shall meet the electrical specifications as explained in Group B above.

HUMIDITY (non-operating)
Group E

3 each
Serial #10,11,12

The units shall be subjected to an atmosphere of 80 to 98 percent relative humidity at a temperature of -10°C to +65°C for a period of one cycle. Thereafter they shall meet the electrical specifications as explained in Group B above.

LIFE
Group F

a) Randomly select four samples from Serial #13 thru 20.

b) Set the pulse width at 1 microsecond and a duty cycle of 0.001.

c) Set the pulse power amplitude at 5KW peak and apply it to the limiter under test for at least one (1) minute to reach thermal equilibrium.

d) Increase the pulse power to 1 KW steps, remaining at each level for at least one minute to reach equilibrium before continuing to the next level.

e) Record the highest peak power level P_M that is sustained for at least one minute by each sample.

LIFE
Group F (Cont.)

f) Verify that the unit failure occured as a result of the gold-silicon eutectic (370°C) by either:

1) removing the bulk silicon element from the resonant iris and confirming the presence of a low DC resistance (less than 100 ohms) thru the sample.

2) or locating the alloy fault thru a "lap and stain" evaluation.

g) The level obtained in step e) shall be at least 5.5 KW peak.

SECTION H, Deliveries or Performance is amended as follows:

SLIN 0001AB, Confirmatory Samples, delete "23 Dec 77" and substitute the following therefor: "17 July 1978"

SLIN 0001AC, Pilot Run, delete "25 June 78" and substitute the following therefor: "19 January 1979".

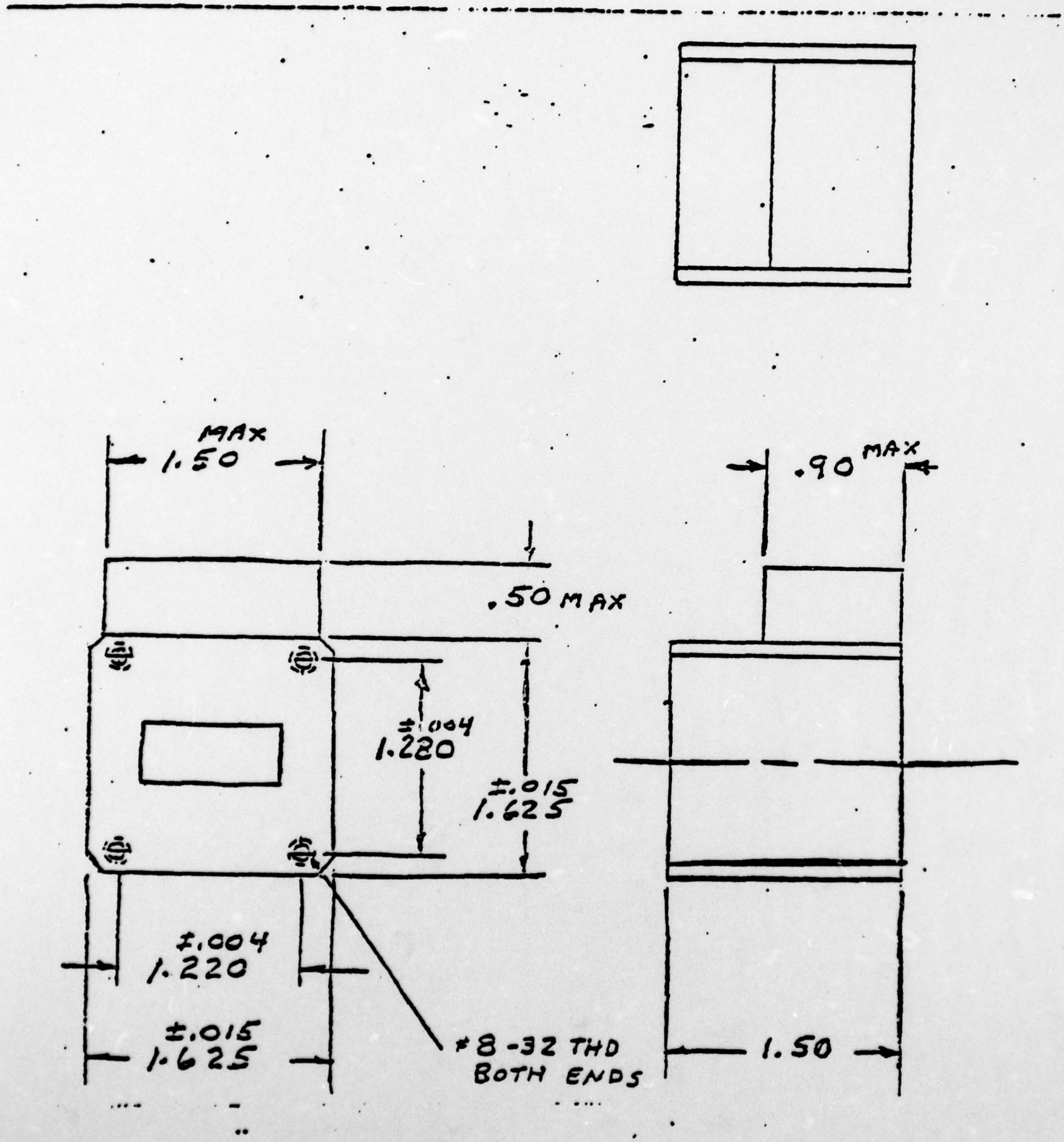

MAX
1.50
.90 MAX
.50 MAX
±.004
1.220
±.015
1.625
±.004
1.220
±.015
1.625
#8-32 THD
BOTH ENDS
1.50

FIGURE 1

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