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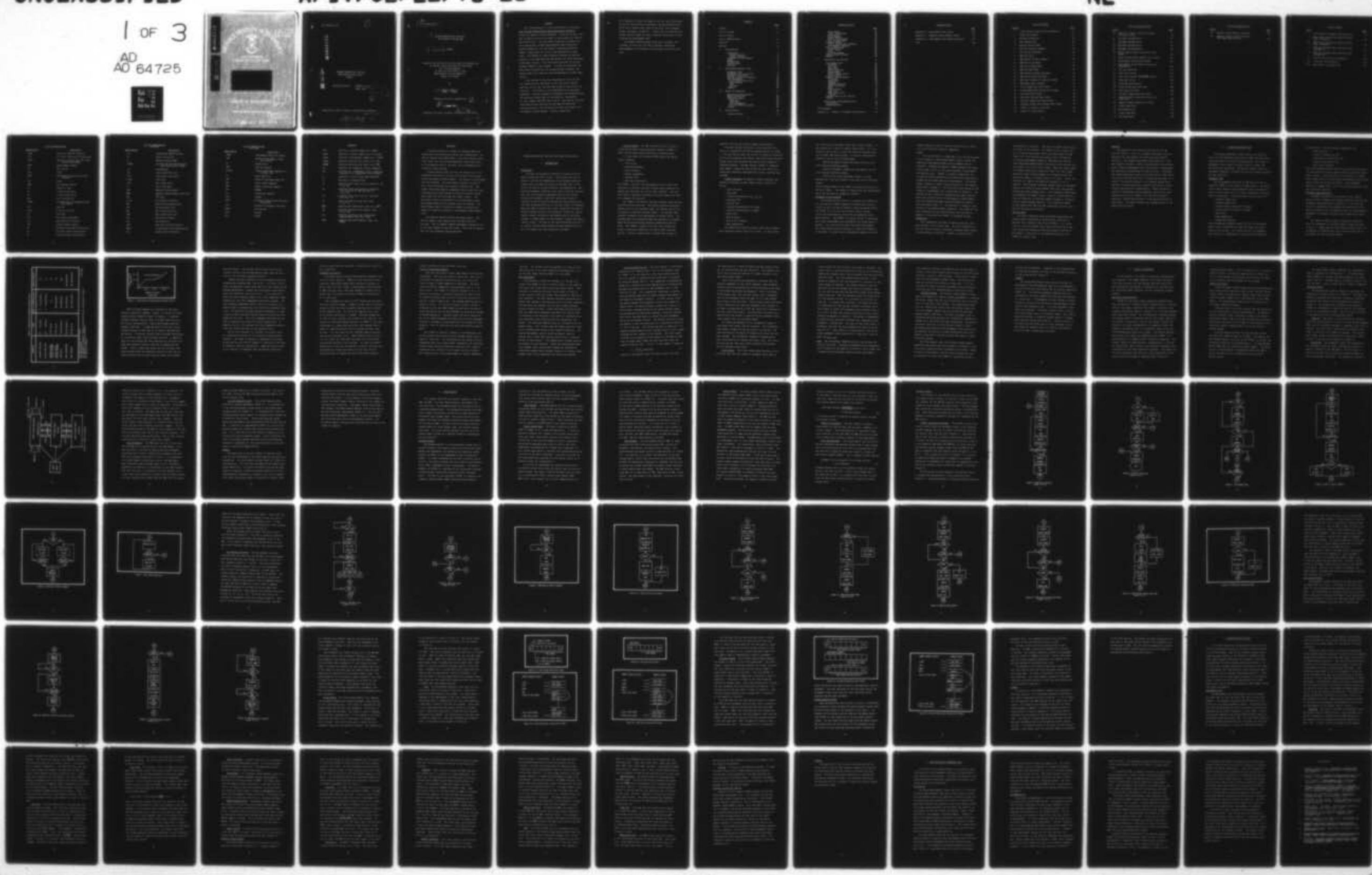

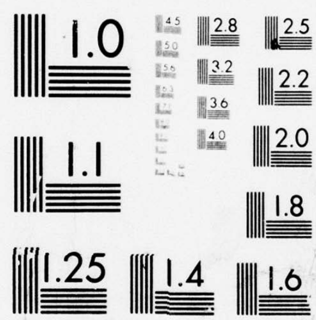

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AIRCREW MODULARIZED INFLIGHT DATA ACQUISITION SYSTEM

THESIS

AFIT/GE/EE/78-28 ROBERT E. HILL
Capt, USAF

Approved for public release; distribution unlimited.

19 Jan 79

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Director of Information

see title page

AFIT/GE/EE/78-28

AIRCREW MODULARIZED INFLIGHT DATA ACQUISITION SYSTEM

Master's THESIS

Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology
Air Training Command
in Partial Fulfillment of the
Requirements for the Degree of
Master of Science

by

Robert E. Hill
Capt USAF

Graduate Electrical Engineering

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Preface

This investigation is a continuing effort to the Aircrew Inflight Physiological Data Acquisition SYSTEM II started by Captains Jolda and Wanzek. Their effort was a concept validation while this effort is the systems and requirements definition. The next effort required to produce the third generation Inflight Physiological Data Acquisition System (IFPDAS III) for the School of Aerospace Medicine (SAM) is fabrication of a full scale demonstration model (FSD). The IFPDAS III specifications provided are general enough to allow upgrading the FSD design with newly developed integrated circuits. Only the digital portions of the man-mounted IFPDAS III are treated. In order to understand the data bases discussed and the system designs proposed, the reader needs to be familiar with microprocessor system fundamentals.

I am indebted to the Crew Technology Division of SAM for presenting this challenge to AFIT and to Dr. Mathew Kabrisky, my advisor, who provided valuable inspiration and direction. This effort is an integration of my two major sequences: Digital Information Processing and Bioengineering and provided a great deal of satisfaction. My mentors: Dr. Gary Lamont, Maj Alan Ross, and Dr. Lynn Wolaver provided those motivations necessary to overcome the obstacles. I am appreciative to the following for their assistance with the magnetic bubble memory: Charley Stewart and

Bill Manchuck of Texas Instruments, Dallas, Texas; Mike West of the Air Force Avionics Laboratory, Wright-Patterson AFB, Ohio; and Lt Dennis Kane (USN) of the Naval Post Graduate School, Monterey, California. I would like to thank Orville Wright and Dan Zanbon for their technical assistance in fabricating the development tool.

My deepest gratitude goes to my wife, Jeaneane, and children, Ty and Troy, for their patience, continuing encouragement, and tolerance of my absence during this project.

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List of Abbreviations

Abbreviation	Definition
A/DC	Analog to Digital Converter
AFIT	Air Force Institute of Technology
ASCII	American Standard Code for Information Interchange
BMM	Bubble Memory Module
CD	Coil Driver
CLR	Clear
CMOS	Complementary Metal Oxide Semiconductor
DLY	Delay
DMM	Data Manager Module
DT	Change in Time
DX	X field Diode Array
DY	Y field Diode Array
EOC	End of Conversion
EPROM	Electronically Programmable Read Only Memory
FCN	Function
FIFO	First-In-First-Out
FR	Flow Rate
FSD	Full Scale Development
G's	Acceleration of Gravity
GSS	Ground Support System
Gx	Aircraft Longitudal Acceleration
Gy	Aircraft Lateral Acceleration
Gz	Aircraft Normal Acceleration

List of Abbreviations
Continued

Abbreviation	Definition
Hex	Hexidecimal Numbering Base
Hz	Hertz (cycles/sec)
ID	Identification Number
IFPDAS	Aircrew Inflight Physiological Data Acquisition System
I/O	Input/Output
LSB	Least Significant Bit
LSBY	Least Significant Byte
LTIME	Last Time
LVAL	Last Probe Value
LZ	Last Probe Zone
MBM	Magnetic Bubble Memory
MBMC	Magnetic Bubble Memory Controller
MHz	10^6 Hertz
mm Hg	Millimeters of Mecury
MOS	Metal Oxide Semiconductor
MPU	Microprocessor Unit
MSB	Most Significant Bit
MSBY	Most Significant Byte
MUX	Multiplexer Address
N/C	No Connection
NEXT	Data Word Location Pointer
NMOS	N type Metal Oxide Semiconductor
PO_2	Oxygen Partial Pressure

List of Abbreviations
Continued

Abbreviation	Definition
PROM	Programmable Read Only Memory
RAM	Random Access Memory; read/ write memory
RL	Random Logic
ROM	Read Only Memory
R-Wave	Highest Amplitude Component of a Normal EKG
SA	Sense Amplifier
SAM	School of Aerospace Medicine
SBC	Single Board Computer
SCM	Signal Conditioner Module
STB	STROBE
TN	Termination Network
TRIG	Trigger
UART	Universal Asynchronous Receiver/ Transmitter
V/FC	Voltage to Frequency Converter
WRDCT	Word Counter
XTAL	Crystal
92K	92,204

Notation

XXXX	Signifies a decimal number (e.g. ØØ17)
XXXXB	Signifies a binary number (e.g. 01111111B)
XXXXH	Signifies a hexidecimal number (e.g. 3C9AH)
(name)	Signifies positive true logic (e.g. STB)
($\overline{\text{name}}$)	Signifies positive true logic (e.g. $\overline{\text{STB}}$)
Uxx	Signifies an integrated circuit component
UCx	Signifies non integrated circuit components mounted on an integrated circuit header
Px	Signifies a circuit card edge connector
Jx	Signifies a connector plug
Ax	Signifies the A port pins of a parallel I/O (e.g. A6)
Bx	Signifies the B port pins of a parallel I/O (e.g. B3) or DAS1128 data pin (e.g. B8)
Cx	Signifies the C port pins of a parallel I/O (e.g. C7)
Dx	Signifies positive true data lines (e.g. D7)
$\overline{\text{DBx}}$	Signifies SBC 80/20 data lines (e.g. $\overline{\text{DB7}}$)
Axx	Signifies positive true address lines (e.g. A10)
ADx	Signifies positive true, multiplexed address/data lines (e.g. ADØ)
$\overline{\text{AD}}$xx	Signifies SBC 80/20 address lines (e.g. $\overline{\text{AD15}}$)

Abstract

A baseline design of a School of Aerospace Medicine sponsored aircrew physiology monitor was accomplished. The monitor design requirements were: four hour battery operation; 2x5x9 inch size for man-mounting; record four hours of 13 parameters with 1% accuracy; and use nonmechanical, nonvolatile data storage.

A system design study verifies the feasibility of implementing the monitor using an 8-bit digital data system containing magnetic bubble memory. The design is partitioned into four modules. The Power Module contains +5 and +12 volt Lithium batteries and a module interface bus. The Signal Conditioner Module accomodates sensor amplifiers and a microprocessor based analog to digital converter system which amplifies and digitizes the sensor signals. The digitized signals are provided to a microprocessor based Data Manager Module which prepares data for storage. The Bubble Memory Module contains six memory locations each capable of supporting quarter or one megabit bubble memory chips.

The baseline design achieves the design goals. The monitor samples seven sensors every 50 msec with 0.4% accuracy. The six megabit memory accomodates storage of 1/3 of the data sampled during four hours. This rate is acceptable for the parameters being monitored.

AIRCREW MODULARIZED INFLIGHT DATA ACQUISITION SYSTEM

I. INTRODUCTION

Background

Aircrews are exposed to potentially adverse environmental conditions while flying. These conditions can be natural like the low temperatures and decreased levels of oxygen found at higher altitudes or man-made such as the artificial gravity forces resulting from maneuvering. Man-made environmental conditions also result from the life support and crew protection equipment worn by the aircrew. Adverse environmental conditions impose physiological stresses on the aircrew and decrease aircrew effectiveness. The Crew Technology Division of the USAF School of Aerospace Medicine (SAM) at Brooks AFB, Texas, recognizes the need to monitor aircrew activity, environmental conditions, physiological stress, and mission performance and to correlate changes in effectiveness to environmental changes and physiological stress. The goal of the Crew Technology Division is to improve aircrew effectiveness through optimum design of the life support and crew protection equipment.

Current System. The SAM currently has an "Aircrew Inflight Physiological Data Acquisition System" (IFPDAS I) which records seven analog functions on cassette tape:

- A time code (to correlate flight events and physiological effects)
- Pilot voice
- Electrocardiogram
- Cabin pressure
- Oxygen consumption
- Expired flow
- Vertical acceleration

The IFPDAS I consists of a man-mounted unit to record the functions on cassette tape and a ground based system to reproduce the functions on a strip chart recorder. The strip chart data is manually converted to digital signals and sent to a computer for analysis.

The IFPDAS I has several problems centered around analog recording of the functions. The analog recording technique induces noise on the recorded signal and reduces the ability to recover an accurate function signal. The cassette tape recorder interferes with performance of cockpit tasks. The cassette tape drive mechanism does not operate at a constant speed during accelerations caused by maneuvering the aircraft. The IFPDAS I system is old and lacks reliability. It has no expansion capability to record other functions such as: triaxial acceleration, inspired flow volume, or separate inspired and expired oxygen concentrations.

The Naval Weapons Laboratory, China Lake NAS, California, is developing for SAM an updated version of IFPDAS I. The Navy design added the ability to record 16 functions by first multiplexing the signals, then digitizing the multiplexed result and recording the digital data stream on a cassette recorder. The Navy design, IFPDAS II, improves upon IFPDAS I capability and reliability but retains the undesirable features associated with using a cassette tape recorder.

IFPDAS Standards. The general IFPDAS standards, projected by personnel at SAM, require that it be able to record:

- Cabin pressure
- Time code
- Triaxial acceleration (G_x, G_y, G_z)
- Inspired flow
- Expired flow
- Inspired concentration of oxygen
- Expired concentration of oxygen
- Heart rate
- Mask pressure
- Anti-G suit pressure
- Body temperature

The IFPDAS must record functions specified by probes which generate signals from 0 to 5 volts. It must record the functions by some means other than a tape recorder. It must record for 4 hours on battery power alone. It is intended to be carried in a survival vest and therefore must be no larger than 2x5x9 inches. It must be configured to operate in one of the following modes:

- Amplify parameter signals and send them to an aircraft mounted recording system.

- Digitize parameter signals and send them to an aircraft mounted recording system.

- Digitize and record parameter signals in a man-mounted unit, with and without a time code link to aircraft system.

These standards apply to an IFPDAS III design to be built in the early 1980's. The IFPDAS III design uses the technologies which are available as commercial products.

Statement of the Problem

The purpose of this effort is to design the IFPDAS III. This design uses IFPDAS standards as design goals and continues the work started by Captains Jolda and Wanzek (Ref 4). The IFPDAS III is an all solid state, digital system utilizing microprocessor controllers and magnetic bubble memory devices. The IFPDAS III example design is based upon the system requirements and supplements the system specifications. The specification detailing those technologies and system specifications necessary to fabricate IFPDAS III is provided. The specification documented together with the example design are used to specify fabrication of IFPDAS III using available comercial components.

Scope

This design effort is organized in the following manner. First, Chapter 2, System Requirements Study, defines the operating requirements based on the parameters being measured. Although the general IFPDAS standards are identified by SAM, little is said about accuracy of measurement and sampling rate. Chapter 3, Theory of Operation, describes the module operations and interactions necessary to accomplish the IFPDAS goals and requirements. The System Design, Chapter 4, details the construction of the modules identified in Chapter 3. The fabrication and testing of the IFPDAS III development tool is described in Chapter 5. The fabrication was limited to integrating the power supplies, heart rate counter and 92 kilobit magnetic bubble memory with the IFPDAS development system designed by Captains Jolda and Wanzek (Ref. 4). The testing is limited to verification of the bubble memory operation. The IFPDAS III design considerations and specifications are contained in Appendix A along with the IFPDAS III hardware designs.

Assumptions

Four assumptions are made in order to achieve a feasible design in the alloted time. The first assumption is that the function signals accurately represent their respective physiological functions. Second, no physiological probe design is required. Time does not permit custom design of probes in this effort. The IFPDAS III will accept signals, from any type probe, which are conditioned to range from 0 to 5 volts and do not exceed 10 KHz in frequency. The sensor development program at SAM specifies that all newly developed probes/signal conditioners shall produce output signals in the 0 to 5 volt range. When the signal range of interest spans only a portion of the 0 to 5 volt range, additional amplification stages can introduce offsets and expand the range of interest up to 0 to 5 volts. Third, the data does not need to be stored as frequently as it is sampled. Physiological functions change slowly and therefore need not be stored at rates greater than every few seconds except when rapid changes occur. This assumption establishes one parameter for memory sizing. Fourth, if more than four hours of operation is required, memory storage is limited to aircraft mounted memory modules. Size, power and memory sizing require that the four hour operating limit be a maximum for the man-mounted design.

Previous Work

The work by Captains Jolda and Wanzek established that digital signal conversion of physiological functions is feasible for a system of the size of IFPDAS I. It is possible to store the digital data, return the data to an analysis system and reconstruct the physiological profile of the subject. Their work is the departure point for the IFPDAS III design study.

Approach

The approach to this design study consists of two parallel efforts. First is a systems requirement study to determine the requirements for measuring physiological functions. The systems requirement study detailed in the next chapter includes a review of physiological and environmental function measurement with the accuracy of measurement and sampling rate determined for each function. Following the system requirement study is the definition of the algorithm used to decide which data is stored and how often it is stored. The parallel effort is the hardware design which consists of module definition, module specification, module design, and feasibility determination. Module definition identifies those major system components which can be used selectively to tailor IFPDAS III to the desired mode of operation. Module specification is the detailed design of each module. The module designs are implementations of the module specifications.

II. SYSTEM REQUIREMENT STUDY

The system requirements study defines the characteristics of the parameters monitored by IFPDAS and the effects these characteristics have on system design. The types of parameters, their range of values, rates of change, and accuracies are identified. The overall digital system requirements necessary to achieve the desired system accuracies are then specified.

Parameter Type

The 13 parameters specified by SAM which must be recorded by IFPDAS III are placed in three groups. The physiological group contains those parameters which are physiological in their origin or are a direct consequence of physiological occurrences. The physiological group consists of:

- Inspired oxygen flow
- Expired oxygen flow
- Inspired partial pressure of oxygen
- Expired partial pressure of oxygen
- Heart Rate
- Body temperature
- Oxygen mask pressure

The environmental parameter group consists of those parameters used to determine the phase of flight and stress loads on the aircrew. This group consists of parameters which occur as a consequence of the aircraft altitude and accelerations. The environmental parameters are:

- Cabin pressure
- Vertical acceleration (Gz)
- Longitudinal acceleration (Gx)
- Lateral acceleration (Gy)
- Anti-G suit pressure

The final parameter group consists of time correlation words. The time words are used to identify when a particular phenomenon occurred. The time words also correlate all events into a time history of the aircrews physiological and environmental conditions during the mission. Each parameter measured is tagged with a time of occurrance word which makes the correlation possible.

Parameter Characteristics

Parameter characteristics consists of the range of values, rates of change, and required sampling rates for the parameters being monitored by IFPDAS III. The characteristics for physiological parameters are specified by the medical profession but the characteristics for environmental parameters of interest to SAM are only subjectively specified.

The range of values, rates of change, and sampling rates for parameters in the physiological group are found in Table I. Oxygen mask pressure rate of change occurs as a consequence of breathing and thus correlates with the requirements for flow rate measurement.

Table I. Physiological Parameter Characteristics

PARAMETER	RANGE	RATE of CHANGE(maximum)	SAMPLING RATE(Hz)
INSPIRED FLOW RATE	0-3 liters/min	9 liters/min/sec	20
EXPIRED FLOW RATE	0-3 liters/min	9 liters/min/sec	20
INSPIRED OXYGEN PARTIAL PRESSURE	0-760 mm Hg	(1)	20
EXPIRED OXYGEN PARTIAL PRESSURE	0-760 mm Hg	NOT SPECIFIED	20
HEART RATE	30-240 beats/min	NOT SPECIFIED	8(2)
BODY TEMPERATURE	95-105 degrees F	NOT SPECIFIED	NOT SPECIFIED
MASK PRESSURE	RP$\pm$100 mm Hg	NOT SPECIFIED(3)	NOT SPECIFIED(4)

(1) Constant during single breath
(2) @ 240 beats/min
(3) Dependant on: depth of breath, airway restrictions, and regulator schedule
(4) Sampled at same rate as FLOW RATE
RP Regulator Pressure

(Ref 1&2)

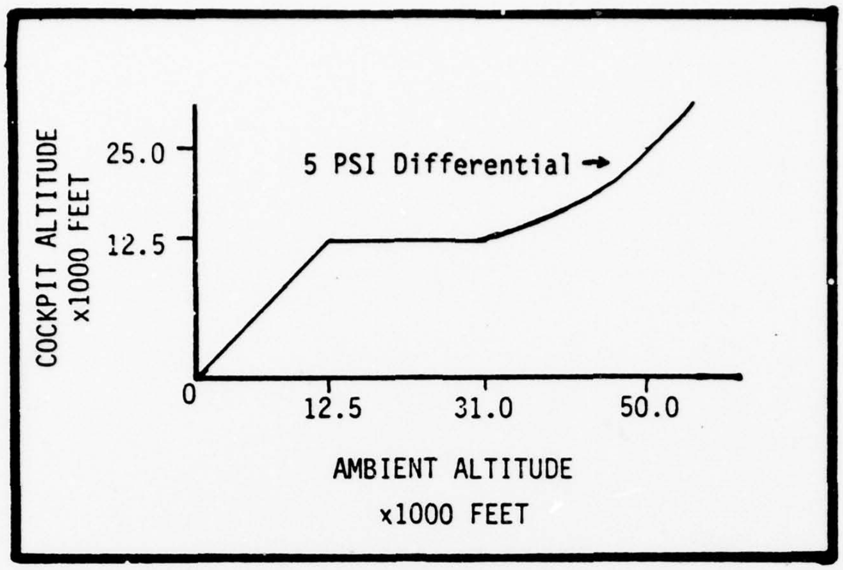

Figure 1. F-106 Cockpit Pressurization Schedule (Ref 3)

Cabin Altitude changes as a function of the cabin pressure regulator schedule. Figure 1 is typical of cabin pressurization schedules found in fighters. To monitor pressure changes from sea level to 50,000 feet with an 8-bit binary representation, limits the minimum quantized change to 200 feet. A sampling rate of 20 Hz can resolve pressure changes of 200 feet up to rates of 240,000 feet per minute. A vertical velocity rate of 48,000 feet/minute is a practical upper limit for most aircraft. A sampling rate of 4 Hz provides 200 foot resolution of aircraft altitude with vertical velocity rates up to 48,000 feet per minute. Table I shows that except for low altitude, the cabin pressure does not change as rapidly as does the aircraft altitude with vertical velocity rates up to 48,000 feet per minute. The extreme vertical velocities do not normally exist at low altitude making lower sampling rates such as 2 Hz for cabin pressure practical.

Fighter aircraft currently in use can generate vertical accelerations ranging from -3 to +9 G's. F-15 and F-16 aircraft can generate G onset rates near 4 G's per second during maximum maneuvering. Lateral and longitudinal acceleration rates are limited to less than ±2 G's. In all three axis, there are high frequency, above 4 Hz, noise components superimposed over the pilot commanded acceleration changes. The high frequency components result from air turbulance, buffeting caused by maneuvering, and internally generated vibrations. The detection of high frequency components, is undesirable as they contribute nothing toward accelerations commanded by the pilot. The pilot commanded accelerations are used to determine the state of aircraft maneuvering. A sampling rate of 8 Hz captures the pilot commanded accelerations and filters out most of the unwanted noise.

Anti-G suit pressure is a function of aircraft vertical acceleration and anti-G suit regulator pressurization schedule. The range of pressure is dependent on the type system used and the rate of change is a function of the rate of change in vertical acceleration. Sampling rate for anti-G suit pressure is dependent upon the desired resolution.

Since no specifications are given, a sampling rate equal to Gz is specified.

Parameter Accuracies

The probes used to monitor physiological parameters are not of clinical quality. IFPDAS III uses noninvasive (not surgically implanted) probes which achieve an accuracy no better than 1% of full range. Conversations with personnel at SAM indicated that, since most IFPDAS III probes are no better than 1% accurate, an overall IFPDAS III accuracy of 1% is sufficient.

Time increments as small as 10^{-6} seconds are available from most digital systems. IFPDAS III uses time to correlate events and thus the time increments required are a function of the sampling rate. For the 20 Hz sampling rate, a 50 milli-second timing pulse is needed. Absolute recognition of time in hours, minutes, and seconds is not required. As long as all monitored events external to IFPDAS III are time correlated to a known starting point, only elapsed time in number of sampling periods, 50 milli-second periods, need be used. In a four hour mission, 288,000 sampling periods, each 50 milli-seconds, occur. When keeping track of time in a 16 bit timer, the time word overflows and is duplicated every 65,536 periods or 54.6 minutes. In order to prevent ambiguities in the time correlation of events, the time tags associated with probe data words are less than 16 bits. Each probe must be sampled and data saved often enough to prevent overflow of the individual time tags.

Digital System Requirements

There are two digital system requirements which must be determined: word size and speed of execution. Word size is a function of required accuracy yet must fit within the limits of what is made commercially available. The word sizes utilized in commercial microprocessors are 4, 8, 12, and 16 bits. The IFPDAS III accuracy standard is 1%. To achieve 1% accuracy, a seven-bit word must be used, $2^7=128$. An eight-bit digital word size will provide an accuracy of one bit in 256 or about 0.4%. The maximum sampling rate required is 20 Hz. In a 50 milli-second (1/20 Hz) period a processor such as the INTEL 8080A can perform an average of 31,250 operations and the RCA CDP1802A can perform an average of 20,000 operations. Assuming eight functional operations per cycle (seven parameters monitored and one data management routine) an average of 3,000 operations are allowed for each function. This is sufficient for most data handling requirements.

The IFPDAS III design is based on a microprocessor controlled digital data acquisition and storage system using an eight bit word size. The microprocessor and support devices recommended take into account power consumption and operating voltage range, average instruction execution time, scope of instruction set, availability of support devices, development support tools, and minimum number of support components required. The systems could be expanded to 16 data bits by specifying one of the newly announced microprocessors such as the INTEL 8086, Motorola 68000, or Zilog Z8000.

Data Management

The selection of data for storage in a limited size system like IFPDAS III has a critical effect on the fidelity with which the stored data follows the actual signal. When raw data is stored and analysis occurs after all data is stored, usually after the flight, the problem of fidelity is most important. The data storage algorithms presented here address the storage of raw data and do not consider computing end functions for storage, such as total oxygen consumed during a breathing cycle. These algorithms only define methods for identifying important data which can then be used to calculate an end function or be stored in condensed form. Five algorithms which identify data for storage are discussed. The continuous method saves the information for all samples taken. This insures that the highest possible fidelity is achieved upon replay of the stored information. The running sum method, used by Jolda and Wanzek, sums all samples over a fixed time interval and the sum is saved at the end of the interval. This method saves storage space at the expense of data fidelity. Three new storage algorithms: fixed change, zone, and variable change are presented as alternative methods which achieve fidelity and storage limits between those of the continuous and running sum methods.

Continuous/Running Sum. The first method is contionuous recording of all sampled data. This is the approach taken by IFPDAS I & II and requires a very large storage medium. The first method of condensing the stored data is proposed by Jolda and Wanzek (Ref 4). The condensing is performed by computing a running sum of the sampled data or recording the maximum and minimum level for the parameter over a fixed interval of time. This condensation technique, as used by Jolda and Wanzek does much to reduce storage requirements at the expense of parameter fidelity. In their system, Jolda and Wanzek sampled the parameters at 20 Hz and summed the samples over a 10 second interval, except for triaxial G's. The G forces recorded during the 10 second interval where the maximum and minimum levels sampled. Using this method, only one or two data words are stored for each parameter during the 10 second interval. The problem with the running sum method is that the occurrance of a significant transient is lost in the sum. The running sum idea is beneficial in a breath-by-breath analysis when the data saved is total oxygen consumed and the interval is one breath. The total oxygen inspired is the sumation of the product of the partial pressure of oxygen (PO_2) times the flow rate (FR) times the sampling interval (DT). In (1) n is the number of sampling

$$V_I = \sum_{1}^{n} (PO_{2_n})(FR_n)(DT) \qquad (1)$$

periods in the breath, zero flow rate to zero flow rate.

The same equation is used to compute expired oxygen volume, V_E, by using expired PO_2 and expired FR. The algebraic sum of V_I and V_E gives the quantity of oxygen consumed in the body during that breath.

While the running sum technique is valuable when the specific parameter is not itself important, when parameter fidelity must be maintained one of the following three types of data handling methods are proposed. Each of the types; fixed change, zone, and variable change, uses a condensed form of the parameter value and adds to it a time element tag to make up the data word. Each of these three algorithms store a data word only when the parameter value changes by at least a minimum quantity from the value which occurred at the last significant event. The three data structures are identified by the method of quantifying the parameter value: fixed change, zone, and variable change.

All three new methods utilize incremental changes in time rather than actual time of occurance. The incremental time change is added to the data word as a time tag. The time tag reflects the amount of elapsed time since the last data storage. The incremental changes are summed during data reconstruction to produce the actual time. The size of the time tag and time scale factor determine the maximum interval between stored words.

Fixed Change. The fixed change method operates on the principal that only the change in parameter value need be stored along with the time that the change is detected. The actual value is reconstructed during analysis by incrementally summing the changes versus time to produce the time-correlated absolute value. The fixed change method defines a fixed amount of change and only the occurance of a positive or negative change is recorded. This method requires that the sampling rate be fast enough such that the parameter value can not vary by more than the specified change value between sampling periods. When the parameter does not change value for long periods of time, it is possible to overflow the time tag. To prevent this overflow, a no change data word is stored when the time tag has reached its maximum value. This method is useful for parameters which change slowly, 2 Hz or less, or when less accurate recording of more rapidly changing parameters is required. The method is independent of sampling rate provided a minimum rate, dependent on the parameter, is maintained. The value of the fixed change is defined by the user for each parameter and need not be the same for all. Data stability is maintained by storing the actual parameter value along with its time tag in place of every nth data word.

Zone. The zone method condenses data by scaling down the value of the probe. Accuracy of parameter value representation is traded for the benefit of storing a value rather than a change while maintaining reduced storage requirements.

This method is applied to parameters with narrow ranges of values or ones which change value rapidly but for which high accuracy in value is not necessary. A data word is stored each time the parameter changes zones. The new zone and time of occurence are stored as a data word. It is not necessary to store the actual parameter value periodically since the zone is a representation of the actual value.

Variable Change. The variable change method is used when high fidelity of rapidly changing parameters is required. The actual change from the last significant value is stored with its time tag in this method. The sampling rate used with this method must insure that the maximum change that can occur between samples does not exceed the data word change element resolution. The actual parameter value is reconstructed during analysis by incrementally summing the changes as is done with the fixed change mode. Periodically the actual value and its time tag are stored to insure accurate reconstruction of the parameter value versus time. The operator can define a minimum change which must occur before a data word is stored to reduce the number of words requiring storage.

The fixed change, zone, and variable change methods determine significant data for storage or inclusion in functions which compute desired information for storage. Based on mission requirements, the most useful methods are used as necessary to tailor the IFPDAS III operating system to satisfy the requirements. Examples of the implementation of these three methods are found in the software discussion of the System Design, Chapter 4.

Summary

The System Requirement Study results show that all physiological and environmental data can be represented by an 8-bit binary word and achieve the 1% accuracy required of IFPDAS III. The required parameter sampling rates are achievable by utilizing commercially available microprocessor controllers. The management of data storage is accomplished by selecting the appropriate data management algorithm for each parameter type. Five data management algorithms are presented: continuous (actual value), running sum, fixed change, zone, and variable change. Each type of algorithm provides a trade-off between amount of storage space required versus data fidelity. Proper selection of the type algorithm being used for each parameter tailors the IFPDAS III system to meet the fidelity requirements within the data storage space available.

III. THEORY OF OPERATION

In this chapter, the IFPDAS III operating configurations are presented. The common elements of the three configurations form the basis for the modules functional definition. The remainder of the chapter is devoted to an explanation of the individual module functions and the interaction between modules.

Operating Configurations

IFPDAS III has three primary operating configurations. The configuration 1 hardware accepts analog signals in parallel from all the probes, amplifies the signals in parallel, and transmits the analog signals in parallel to an aircraft-mounted data acquisition system. The configuration 2 hardware accepts the analog signals in parallel from all the probes, amplifies the signals in parallel to the 0-5 volt range, converts the signals to a binary representation in sequential order, and transmits the binary words in a sequential manner to an aircraft-mounted data acquisition system. The aircraft-mounted data acquisition system can communicate with IFPDAS III in configuration 2 to command special conversion sequences. The primary IFPDAS III operating mode, configuration 3, utilizes the acquisition, amplification, and conversion sequences from configuration 2 and adds additional functions. The added functions are sequential decisions as to the disposition of the current data and storage of important data in the self contained bubble memory. As in configuration 2, an aircraft-mounted system is allowed to communicate with IFPDAS III. The aircraft-mounted system either provides data to IFPDAS III or receives data from IFPDAS III for storage.

Module Definition

There are common elements among the three configurations. Each configuration requires a power source, parallel analog signal inputs, and some form of analog signal amplification. The first module common to all configurations is the Power Module. The second module common to all configurations is the Signal Conditioner Module.

Configurations 2 and 3 both require that the analog signals be converted to a binary representation. An analog to digital converter (A/DC) subsystem is added to the Signal Conditioner module (SCM) to provide the required conversions. The digital controller for the A/DC is also tasked with providing the digital communications link to the aircraft-mounted system.

The third module provides the required data service routines which identify data for storage. This module, the Data Manager Module, also acts as the IFPDAS III digital system master controller for configuration 3. The Data Manager Module (DMM) does not contain the bubble memory. The configuration 2 operating mode is enhanced by adding the DMM to screen the data prior to transmission to the aircraft-mounted system.

The Bubble Memory Module completes the complement of modules necessary for configuration 3. The Bubble Memory Module (BMM) only contains the bubble memories and memory support devices. The BMM requires the DMM for control signals and data. Figure 2 shows the four IFPDAS III MODULES.

Operating Theory

The System design section, Chapter 4, describes the hardware and software aspects of IFPDAS III. The theory of operation presented here describes the module interactive operations not obvious from the hardware descriptions in Chapter 4. The system theory presented here addresses IFPDAS III configuration 3 operation with all four modules and an aircraft-mounted system. The final topic discussed is the purpose of the aircraft-mounted system.

Power Up. When power is first applied, any hardware requiring initialization is given its initialization sequence. After the initialization sequence is complete a wait loop is entered. This wait loop is exited when an external start signal is applied to the IFPDAS III system. This external start signal serves to synchronize the start with a known time and is applied to all modules in IFPDAS III.

Conversion. The parameters signals are converted by the SCM eight successive times, averaged and placed in a specific location in the SCM memory. The time word is read from the SCM clock, scaled, and placed in memory behind the parameter value word. The conversions proceed in

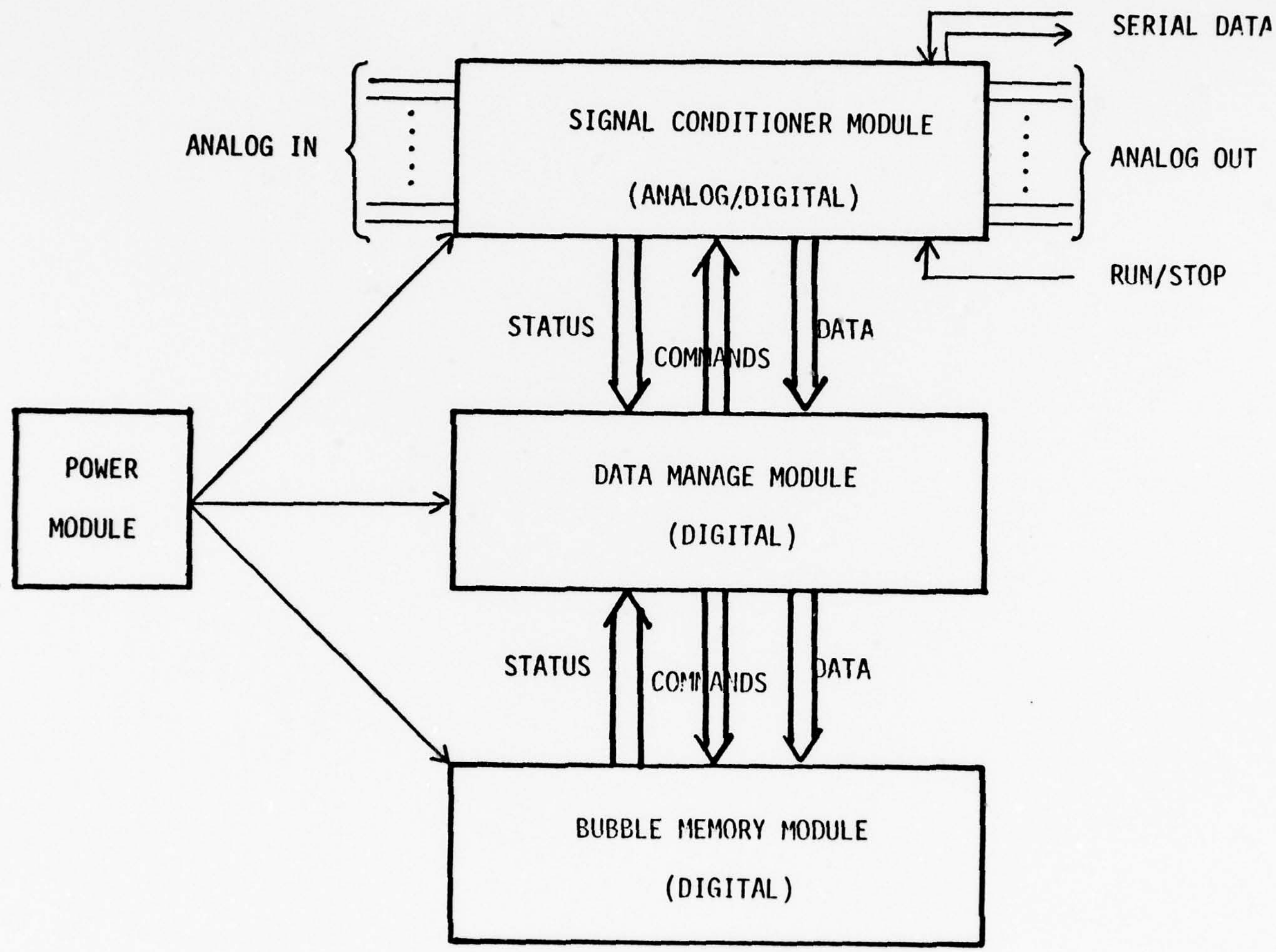

Figure 2. IFPDAS III MODULES

sequence according to a sequencer list. The sequencer list contains enough minor sequence segments to ensure that all parameters are sampled at the required rate. Parameters requiring 20 Hz conversion rates appear in each minor segment while others appear only as often as necessary. At the end of each minor segment the end of sequence flag is set and a wait loop is entered. The DMM moves the data and time from the SCM memory to the DMM memory where the DMM services the data while the SCM starts another minor segment. When the 50 millisecond timer generates an interrupt pulse, the SCM starts the next minor sequence conversion segment. The aircraft-mounted system or the DMM can issue commands to the SCM which are executed after the 50 milli-second interrupt. The aircraft-mounted system can pass data, such as time synchronization words, at the end of each minor segment.

Data Management. The DMM moves the list of data from the SCM memory to a working area of the DMM memory. From here the data is serviced by appropriate data management algorithms and is used in updating the parameter data area. When each parameter data page is filled, it is transferred to a bubble memory storage queue area of the DMM memory. When the bubble memory storage queue is full, the BMM is powered up and the data is transferred to the bubble memory. When the last word is transferred, the data manager sets a 7 msec timer that automatically powers down the memory module. The timer automatically powers down the BMM after the bubble memory storage sequence is finished (6.5 msec). The use of the timer relieves the DMM from monitoring the BMM for the end of sequence flag.

Aircraft-Mounted System. The aircraft-mounted data acquisition system complements IFPDAS III. In configuration 2, the aircraft-mounted system serves as the primary data storage system for IFPDAS III. In configuration 3, the air-crafted-mounted system serves as a secondary data storage and an additional data source. The aircraft-mounted system operating requirements and configuration must be specified by SAM. In addition to complementing IFPDAS III, the aircraft-mounted system also collects data from aircraft mounted sensors. It is possible to use the IFPDAS III modules in constructing an aircraft-mounted system. Using a container the size of a portable casette recorder, the aircraft-mounted system will accomodate all the required modules and provide space for additional memory modules.

Summary

The definition of the four IFPDAS III modules result from the task breakdowns of the three required operating configurations. The Power Module provides power all IFPDAS III configurations. The functions performed by the Signal Conditioner Module are: to collect and amplify the analog probe signals in parallel, convert the analog signals to a binary representation according to a sequence list, and to communicate either the analog signals in parallel or digital words sequentially with an aircraft-mounted system. The Data Manager Module services the digital data and decides which data must be stored. It also controls the primary memory system, the Bubble Memory Module, and acts as the IFPDAS III digital master controller. The Power, Signal Conditioner, Data Manager, and Bubble Memory Modules collectively make up the self-contained, man-mounted IFPDAS III. The aircraft-mounted system complements IFPDAS III by providing memory and collecting data from aircraft-mounted sensors. The following chapter discusses the specifications of each of the IFPDAS III modules.

IV. SYSTEM DESIGN

This chapter specifies the digital elements of the SCM, DMM, and BMM. The Power Module battery requirements are also specified. The hardware design are discussed first on a module-by-module basis. The hardware discussion concludes with a module interconnect discussion and specification of achievable data storage rates. The second section of this chapter discusses the software operating system requirements for the SCM and DMM. The third section discusses the data system format for fixed change, zone, and variable change data words. The final section presents the mission of the ground support system as it affects IFPDAS III maintenance and data analysis.

Hardware Design

The hardware design is a multiprocessor system which is custom tailored to the specific task by inserting the proper modules and components, and modifying the operating system software resident in the programmable read only memories (PROM). For power consumptation and heat disipation considerations, the design stresses the use of Metal Oxide Semiconductor (MOS) integrated circuit technologies. The digital elements of IFPDAS III interface to the analog world through a microprocessor controlled analog-to-digital converter (A/DC). The keys to the successful IFPDAS III operation are: a magnetic bubble memory (MBM) system providing compact, nonvalitile, and non mechanical data storage; and the flexibility provided by software control of data management. This design effort builds upon the work accomplished by Captains Jolda and Wanzek (Ref 4).

Power Module. The Power Module for the aircraft mounted system may differ in size and may use power from the aircraft rather than from batteries. The power module contains all power sources required by the system and the power monitoring circuits to detect a power failure. Power switching for each specific module is accomplished on the respective module.

Signal Conditioner. The Signal Conditioning Module (SCM) is common to all system configurations. It contains mounting locations for a generic set of probe sensor amplifiers and signal conditioners for each type sensor used. Flexibility in the type and number of sensors supported is maintained by packaging each specific sensor amplifier/ conditioner configuration on a common type integrated circuit carrier pack which is inserted into appropriate mounting locations on the SCM as necessary. Provisions are made for the large amplifiers necessary to send analog signals to an external system for configuration 1.

To satisfy the requirement of sending digital data to an external system and provide the digital data for more advanced systems, the Signal Conditioning Module has the space for a microprocessor (MPU), random access memory (RAM), PROM, A/DC, clock counter, and a serial communications device (UART). The SCM MPU controls the sequential conversion of each parameter signal to digital form and provides these digital values to IFPDAS III. A digital data bus exists for data and central communications internal to IFPDAS III and serial communications to an external system occurs through the UART. The data link to the external system is bidirectional allowing both data and commands to be exchanged. This module is mission tailored by adding the analog interface circuits and digital components as necessary into predefined mounting locations. It is possible to include 16 analog inputs requiring digital conversion, two discrete inputs controlling counters such as used for heart rate detection, one MPU, one PROM (2048 words), one RAM (256 words), one UART, and one timer/counter on the SCM.

Data Manager. The data manager module (DMM) is added to provide the data conditioning algorithms, perform any parameter calculations, and control data storage. This module becomes the master digital system controller of IFPDAS III. Its function is to control the operation of the data storage mdoule, direct data conversions by the SCM MPU-A/DC, perform the computations necessary to implement the data conditioning and storage algorithms and control power shut-down of other modules when not needed. The DMM contains a dedicated MPU, up to 2048 words of ROM, 1024 words of RAM, status, control, and Input/Output (I/O) registers, and data bus interface circuits.

Bubble Memory. The Bubble Memory Module (BMM) contains the magnetic bubble memory (MBM) chips, the bubble memory controller (MBMC) and associated support circuits. Six MBM chip positions are provided. Current commercial MBM products are sized at a quarter megabit. Some manufacturers have indicated that they intend to release MBM chips up to the megabit size which are size and pin compatable with the current quarter megabit chips (Ref 5). The BMM provides space for memories ranging in size from a quarter to six megabits of memory depending on the type and number of MBM chips used. The BMM stores data only on command from the data management module. The chips and suport circuits consume large quantities of power and are therefore powered down when data is not be stored. The MBM being used in the IFPDAS III Development Tool is a 92 kilobit development product from Texas Instruments. It's major-minor loop architecture (Ref 6&7) makes it slow and it consumes 11.5 watts of power. The major-minor loop archetecture requires 25.6 msec to store 36 words in the single page mode. In the multi-page mode it requires 19.26 milliseconds to store the same 36 words. The quarter megabit memory architecture, bulk replicate, provides faster data transfers, 10 milliseconds for 28 words, and lower power consumption, 5.5 watts estimated (Ref 8&9). The quarter megabit MBM is estimated to require 10.9 watt seconds to store all 1137 pages of data in the single page mode. Using these figures, one megabit of memory requires

262 watt-seconds to fill all available storage locations. If the power is derived from a 12 volt battery it must provide for a peak drain of one amp for one minute to provide the required memory drive power plus reserve.

$$(262 \text{ watt seconds}) \times \left(\frac{1 \text{ minute}}{60 \text{ seconds}}\right) \div (12 \text{ volts})$$

$$= 0.364 \text{ amp minutes} \qquad (2)$$

A 3x reserve factor is applied to prevent battery voltage drop below 12 volts.

Module Interconnect. The four IFPDAS III modules interconnect to receive power and pass data, commands, and control signals. The interconnection is provided by edge card connectors on the SCM, DMM, and BMM which are inserted into a digital bus structure integral to the Power Module.

Data Storage Rates. The system memory size and mission duration determine the maximum average rate of data storage. For a mission duration of four hours, an average data storage rate of 2.2 eight-bit words per second is allowed by each quarter megabit memory. The six megabit system supports

$$(254688 \text{ bits} \div 8 \text{ bits/word}) \div (4 \text{ hrs}) \div (3600 \text{ secs/hr})$$

$$= 2.21 \text{ words/sec} \qquad (3)$$

average storage rates up to 52 eight-bit words per second during a four hour mission. Since a data storage rate is not specified by SAM, it is assumed that this rate is sufficient and the system operating time is reduced for higher storage rates.

Software Design

The software for the SCM MPU controls data conversion and communications protocol to external systems and the DMM. The software for the DMM MPU controls data sequencing, data computing, data storage, and data control. The data management algorithms discussed previously reside in the DMM software. Data format and storage are discussed in this section. Appendix B contains example of software for implementing the DMM control.

Signal Conditioner Software. The SCM MPU controls the circuits which select the parameter signal to be converted. The MPU commands the A/DC to convert the data and receives the digital value from the A/DC (Figure 3). The processor then filters the data to remove induced noise and sends it to either the UART for transmission to an external system or to the temporary RAM where the DMM MPU can access the data. The procesor accepts command inputs from the DMM MPU and data or commands from the external system (Figures 4, 5, 6, and 7). Once a conversion cycle is starged, it is carried to completion before new data or commands are accepted. Sequencing of parameters for conversion is automatically controlled by software unless an override command is received (Figure 5).

The filtering of noise induced by the analog circuits is accomplished automatically in the conversion cycle (Figure 3): the same parameter is converted eight successive

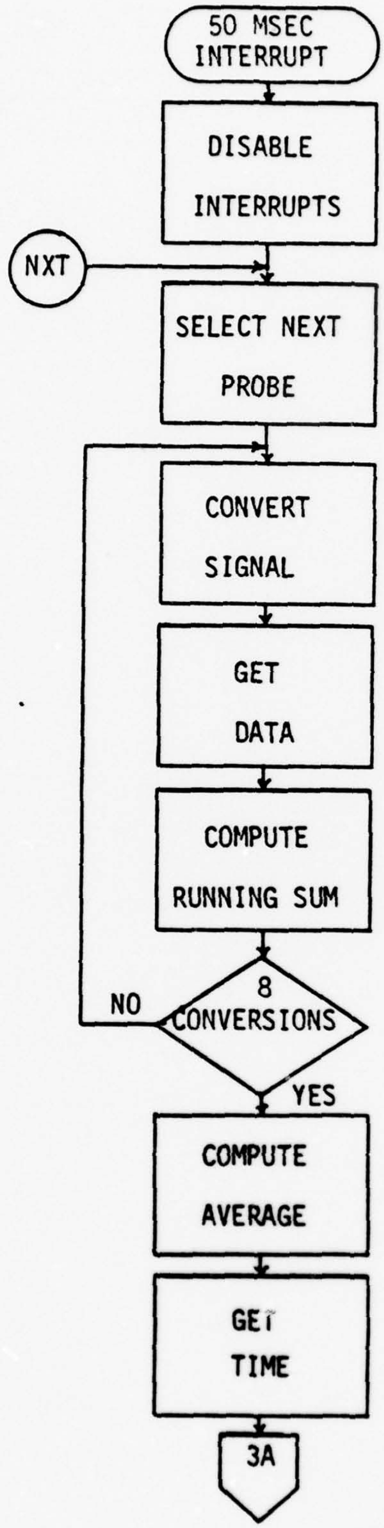

Figure 3. SCM Data Conversion
(sheet 1 of 2)

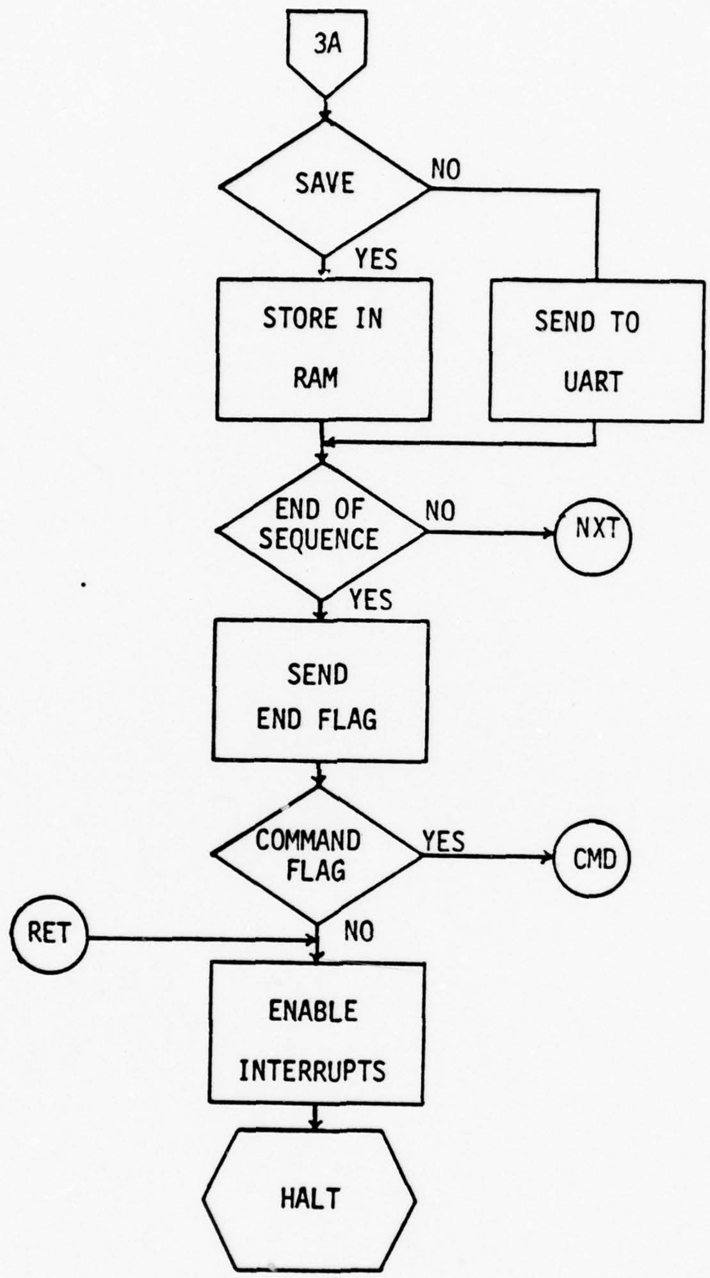

Figure 3. SCM Data Conversion (sheet 2 of 2)

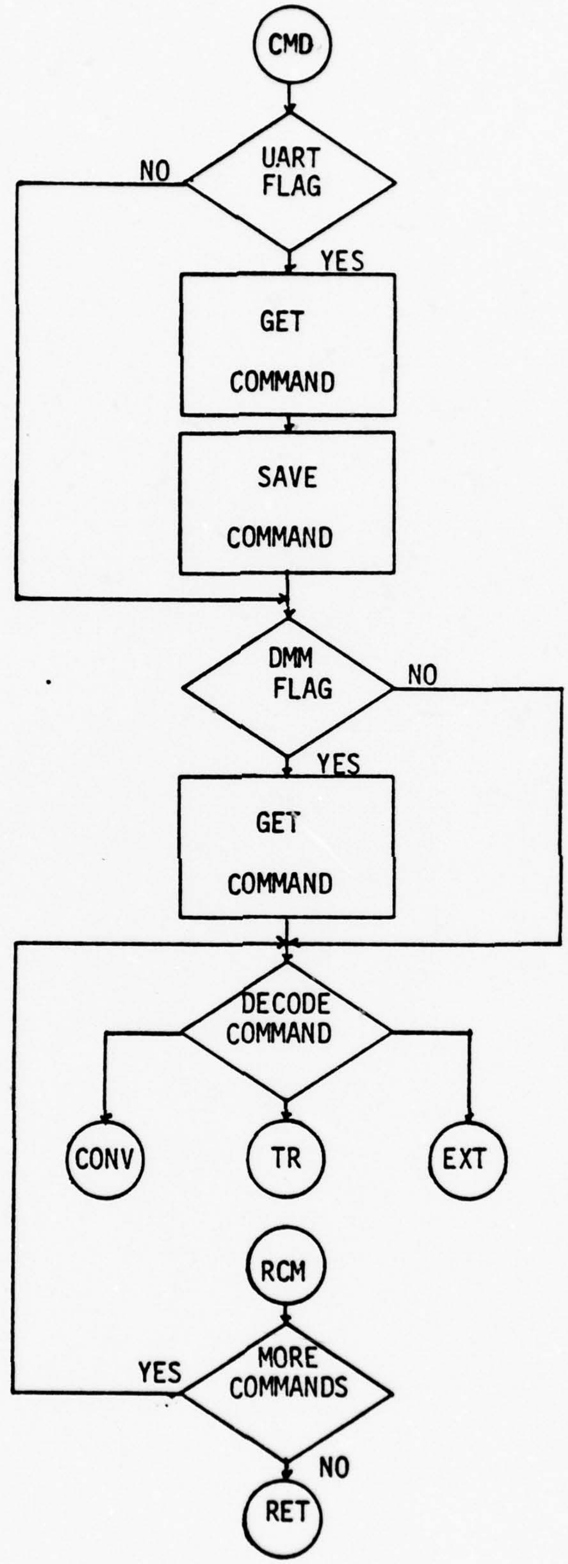

Figure 4. SCM Command Mode

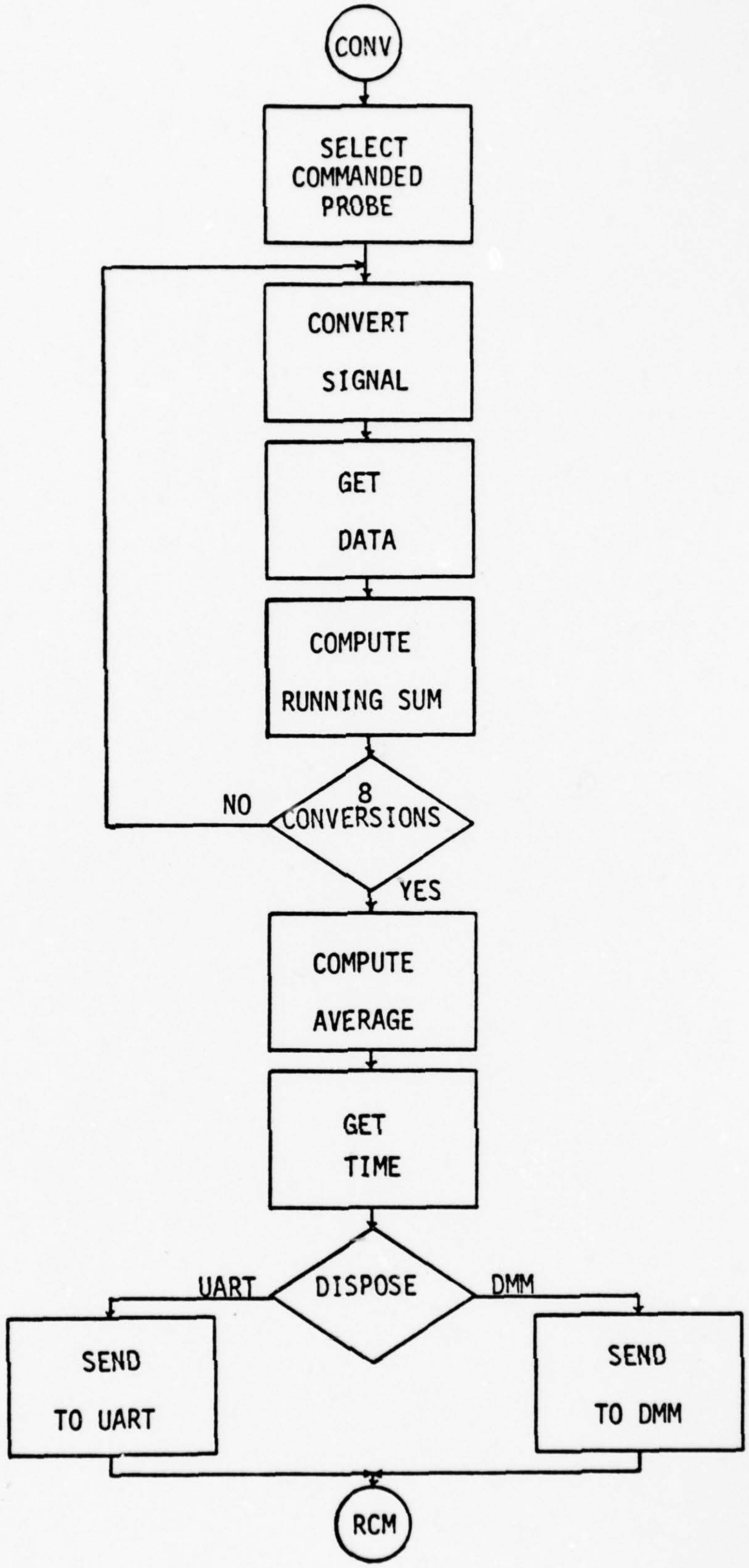

Figure 5. Special Convert Command

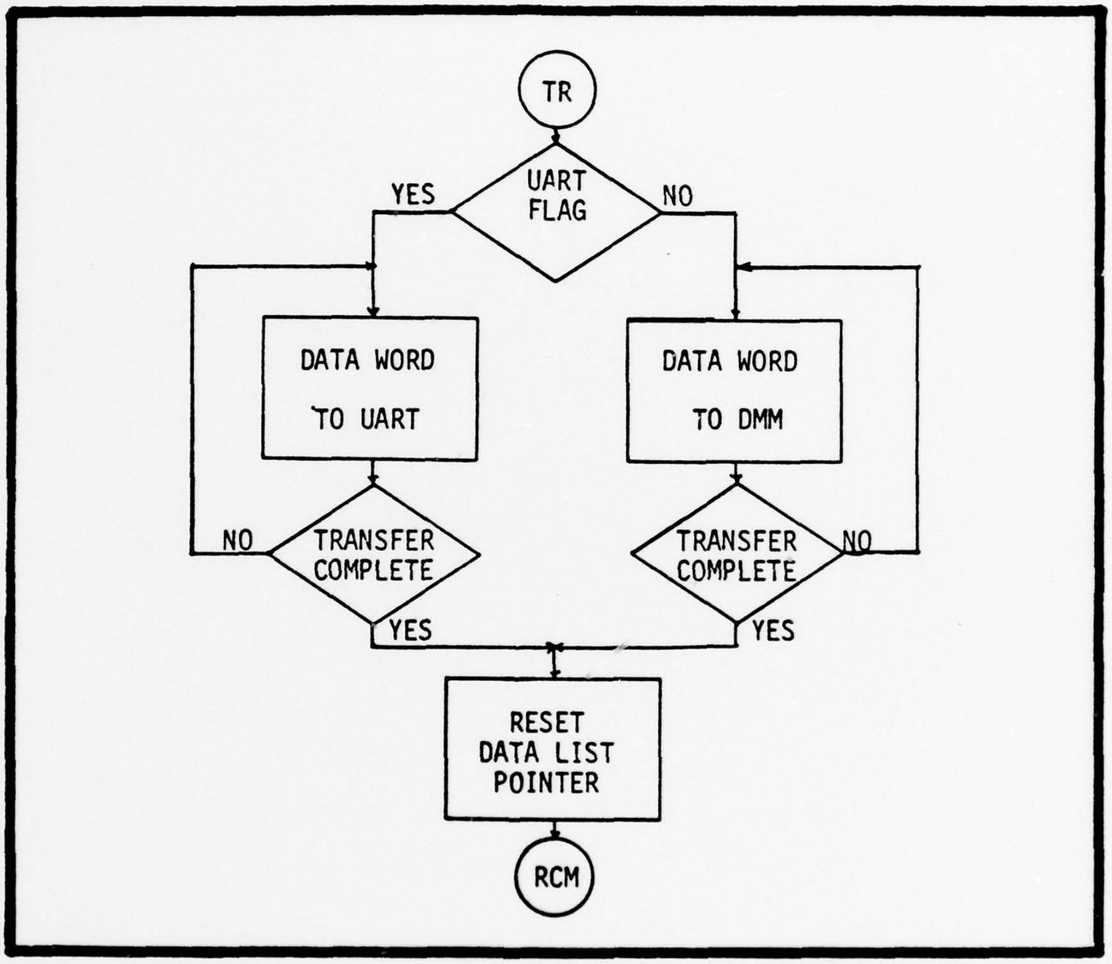

Figure 6. SCM Data Transfer Command

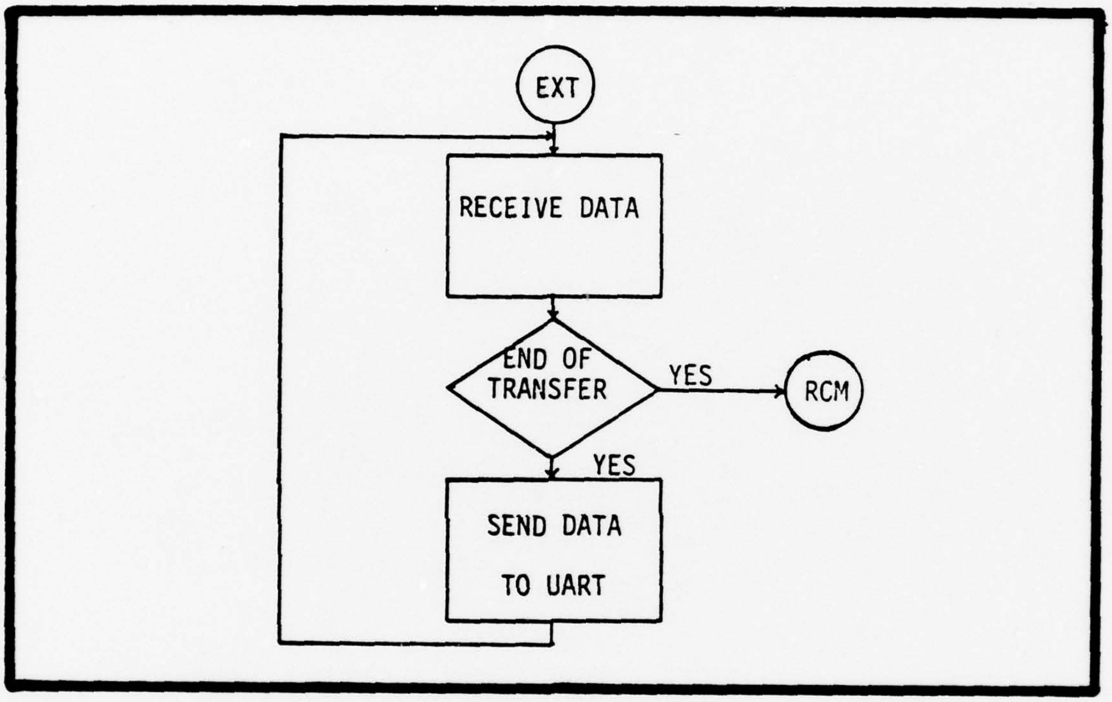

Figure 7. SCM Transmit DMM Data

times and the eight conversions are summed. After eight conversions, the computed sum is diveded by eight and the resulting average is saved as the parameter value. If the period between conversions is 100 micorseconds, the filtering technique passes those signals below 125 Hz.

After the average value is saved, the time is read from the timer (Figure 3). The time is properly scaled for the parameter and saved after the parameter value in the RAM. At the end of a sequence loop the MPU waits for a 50 msec timer interrupt before starting a new sequence (Figure 3).

Data Manager Software. The data manager transfers converted data and time from the SCM RAM to the data management module RAM while the SCM MPU is waiting to start the next sequence (Figure 6, 7, and 8). The data transferred are from a complete sequence cycle, up to 18 parameters. When an error correction is necessary, the DMM sends the single conversion command (Figure 5&9) to the SCM MPU. The SCM MPU signals the conversion is complete by setting the conversion complete flag (Figure 3) and the DMM MPU fetches the data from the SCM RAM and issues a contine command. The DMM MPU operates on the data using the proper data management algorithm. Then computes any necessary functions (Figure 10, 11, 12, 13, 14). The final data values are screened for parameters requiring storage (Figure 8). When data is to be sent to an aircraft-mounted system, the DMM

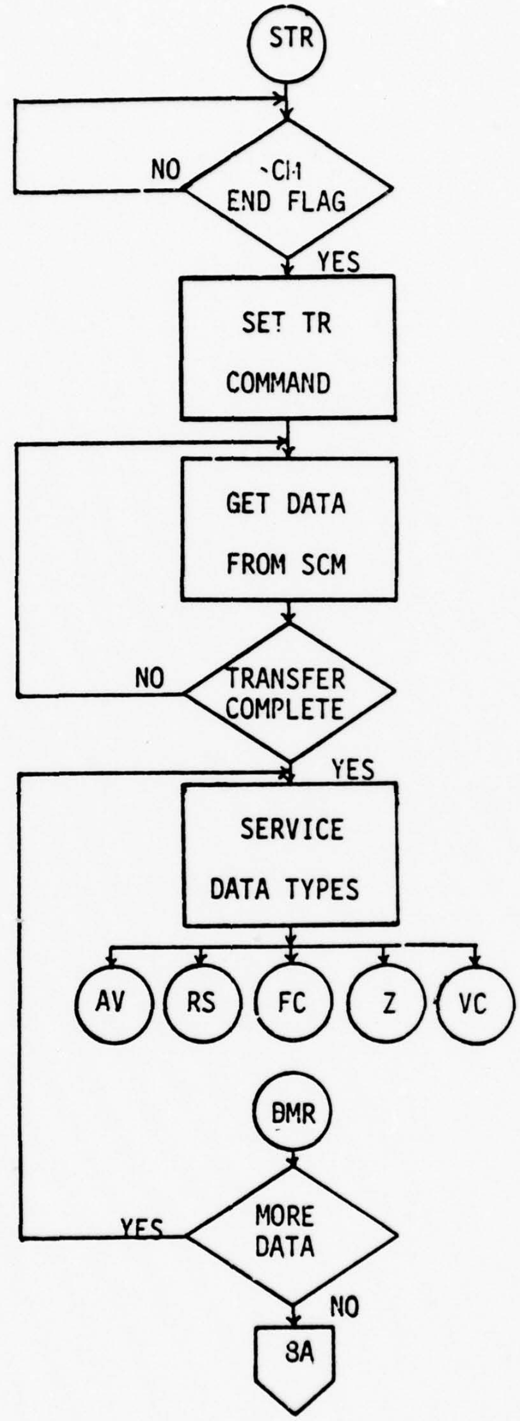

Figure 8. DMM Data Cycle
(sheet 1 of 2)

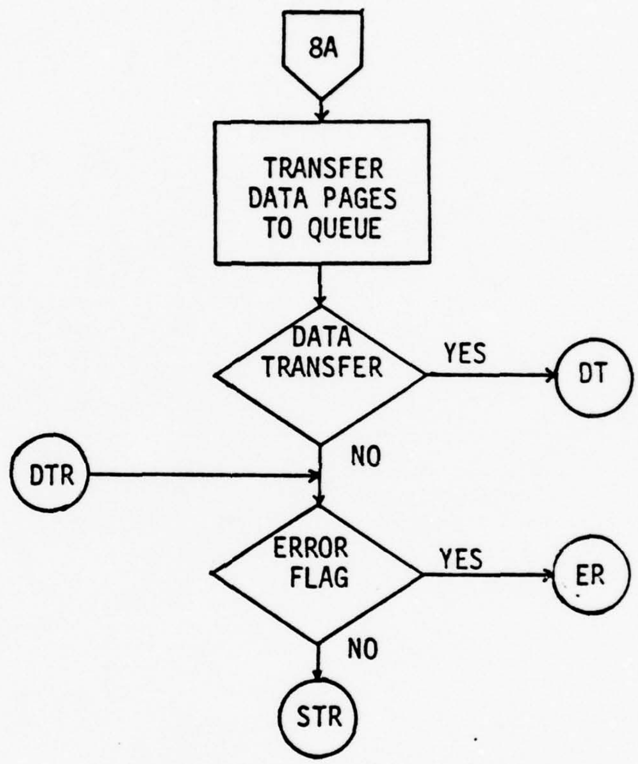

Figure 8. DMM Data Cycle
(sheet 2 Of 2)

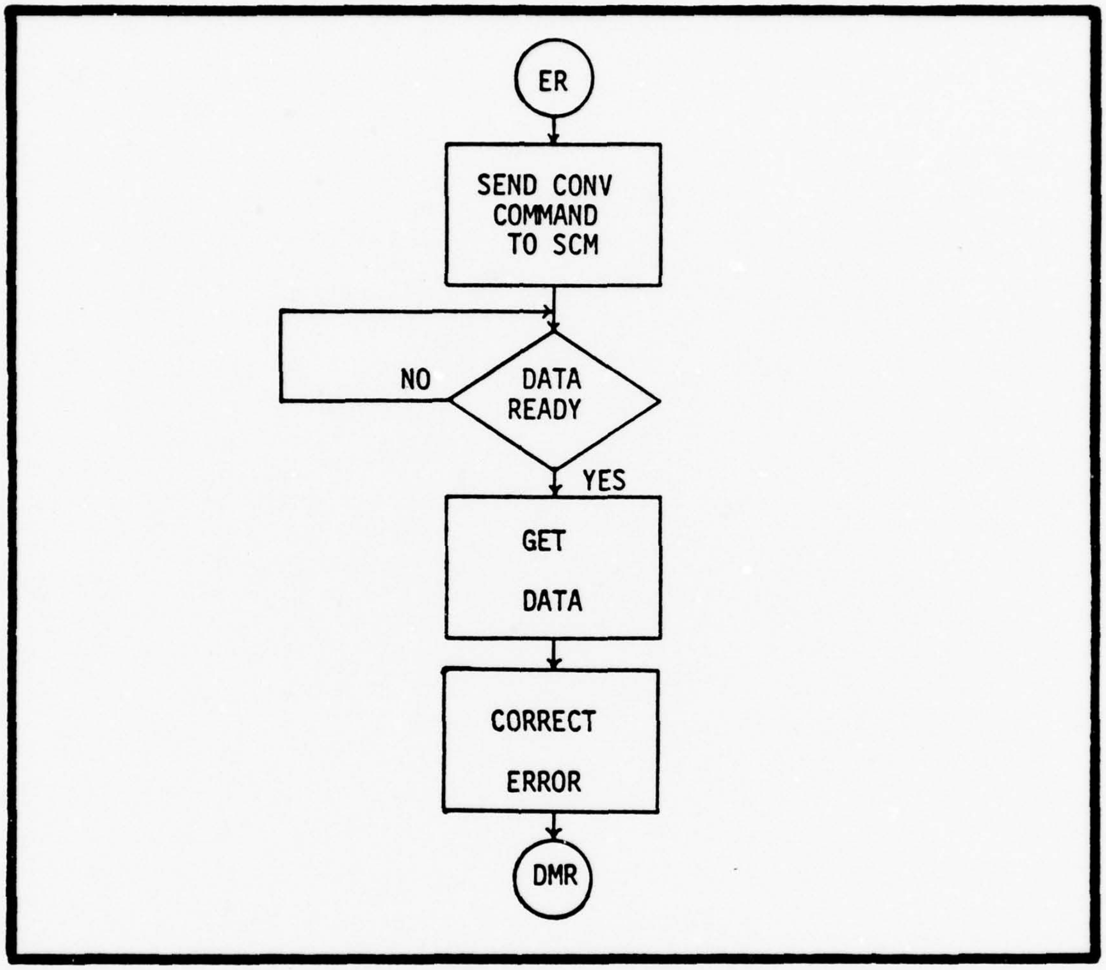

Figure 9. DMM Special Convert Command

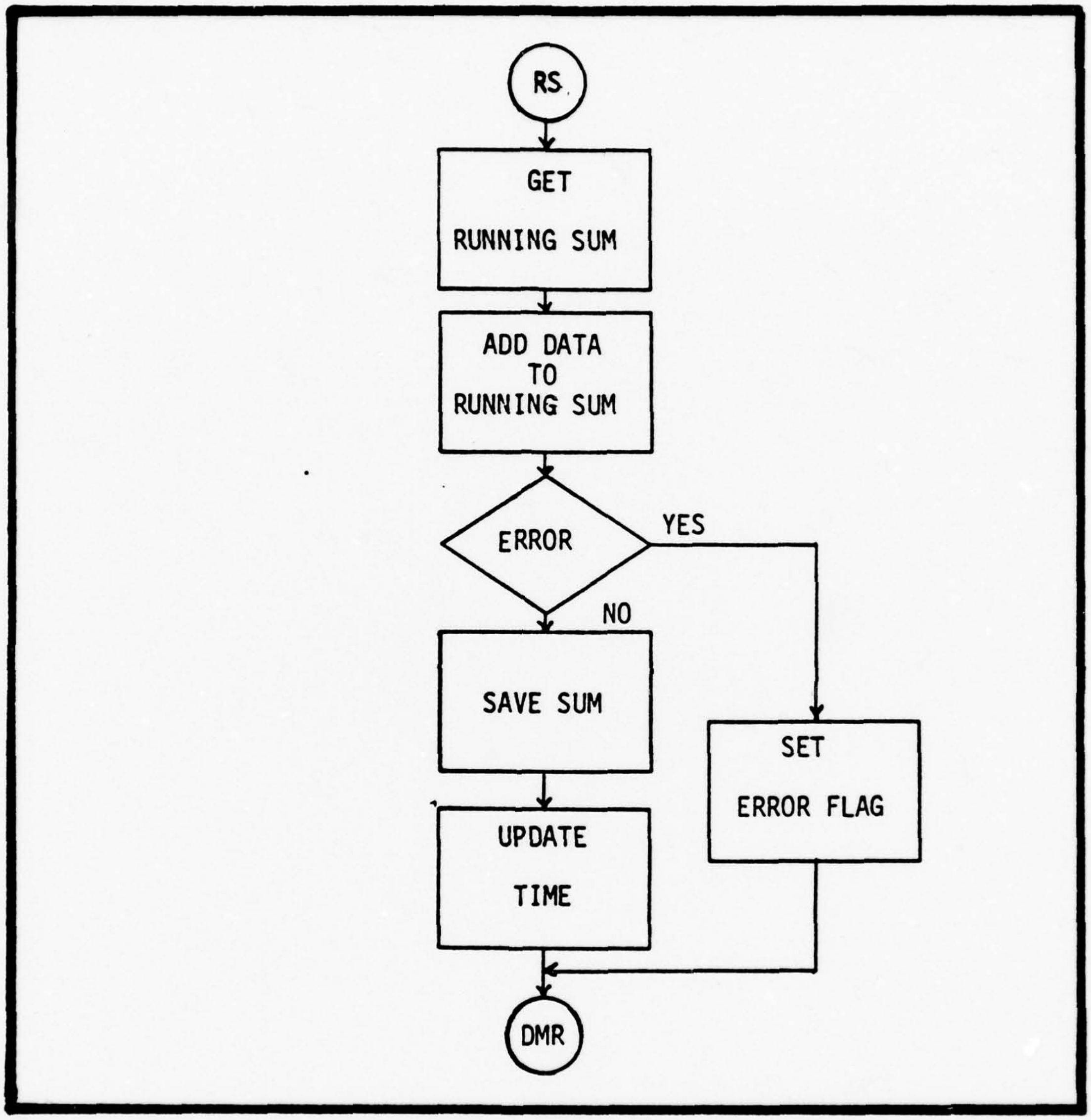

Figure 10. DMM Running Sum Mode

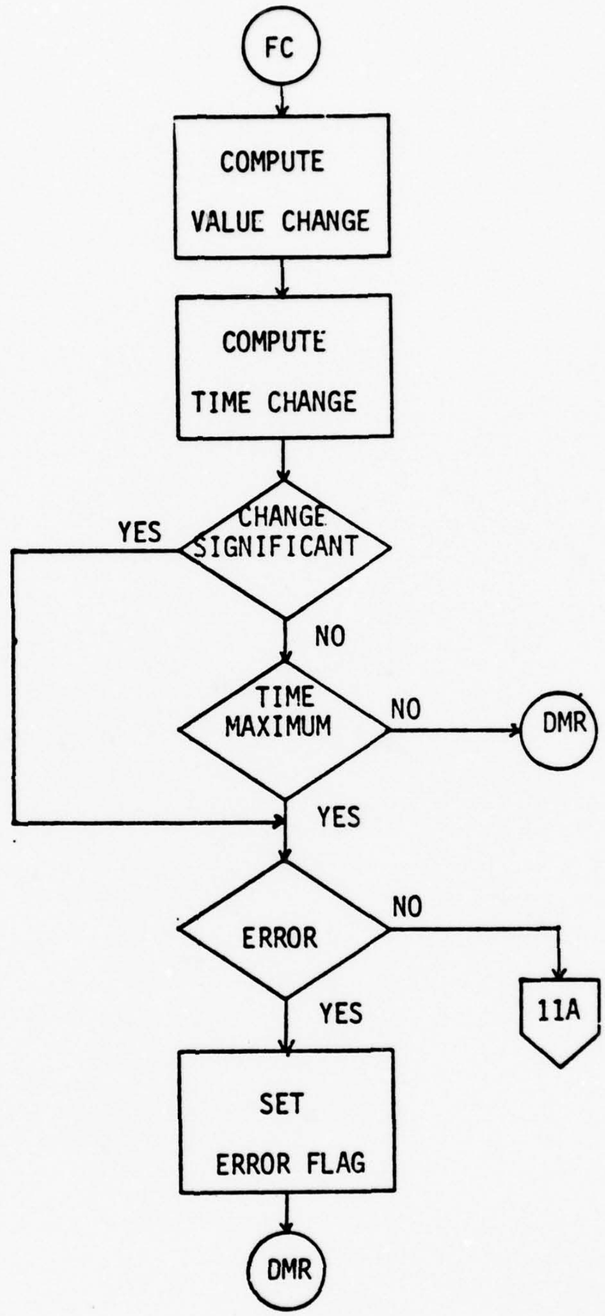

Figure 11. DMM Fixed Change Mode
(sheet 1 of 2)

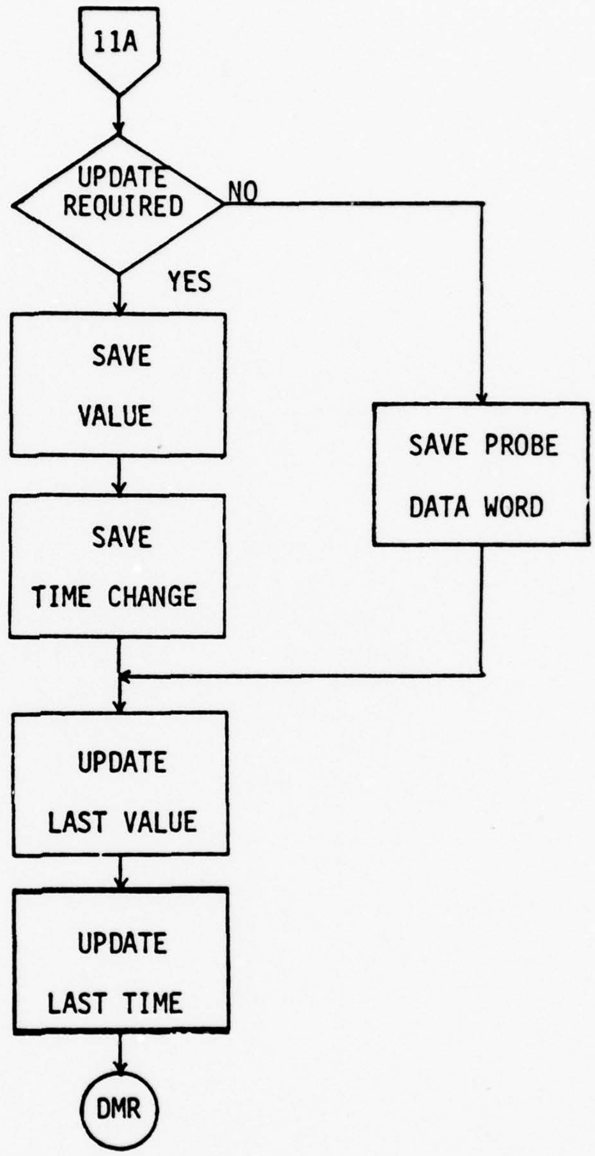

Figure 11. DMM Fixed Change Mode
(sheet 2 of 2)

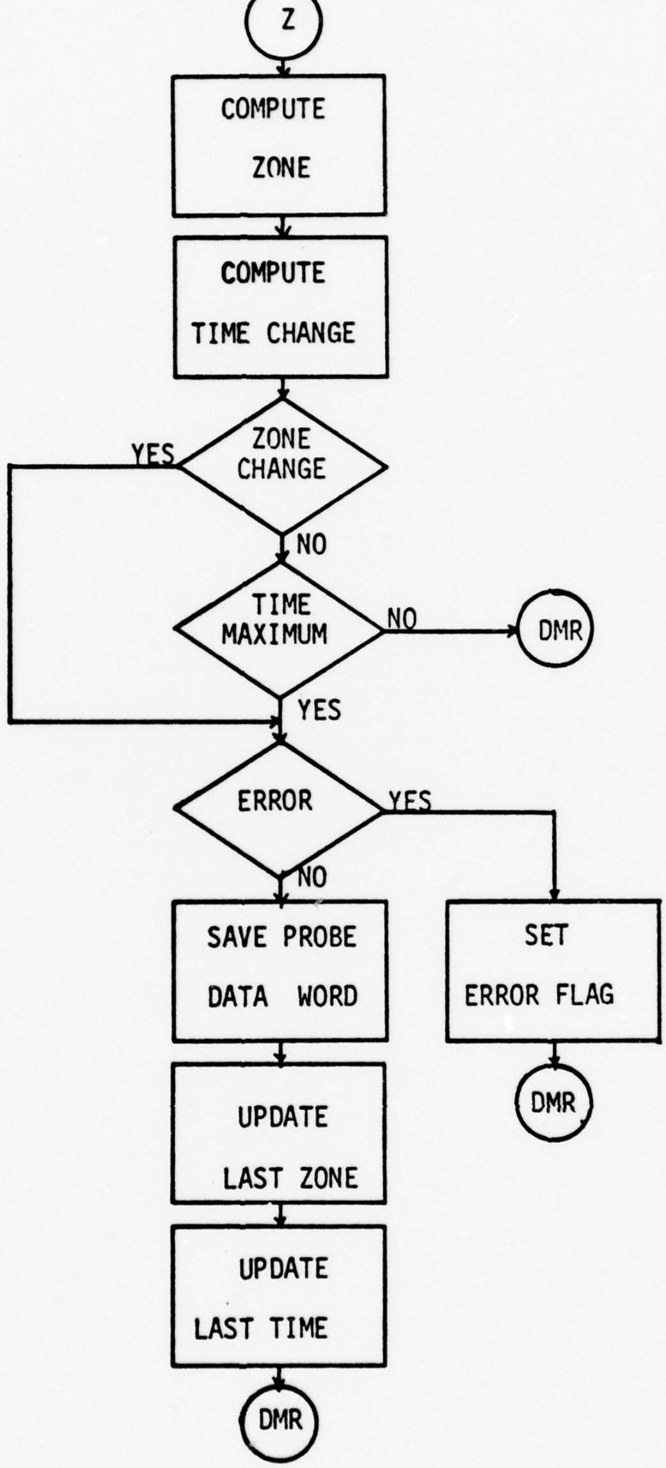

Figure 12 DMM Zone Data Method

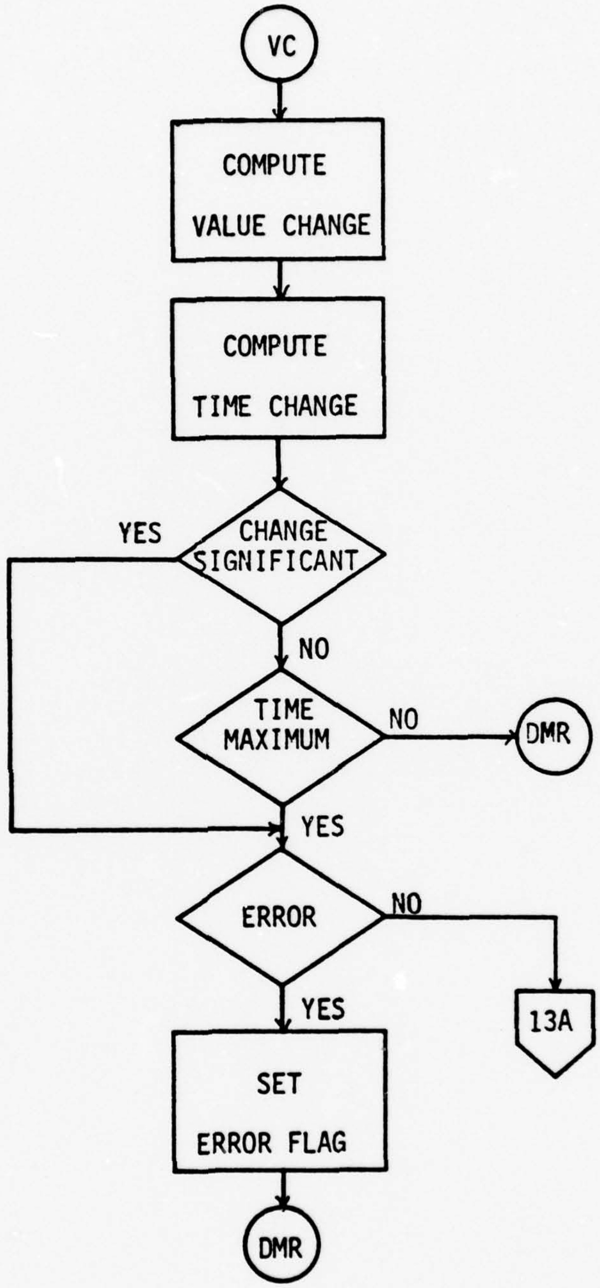

Figure 13. DMM Variable Change Data Mode
(sheet 1 of 2)

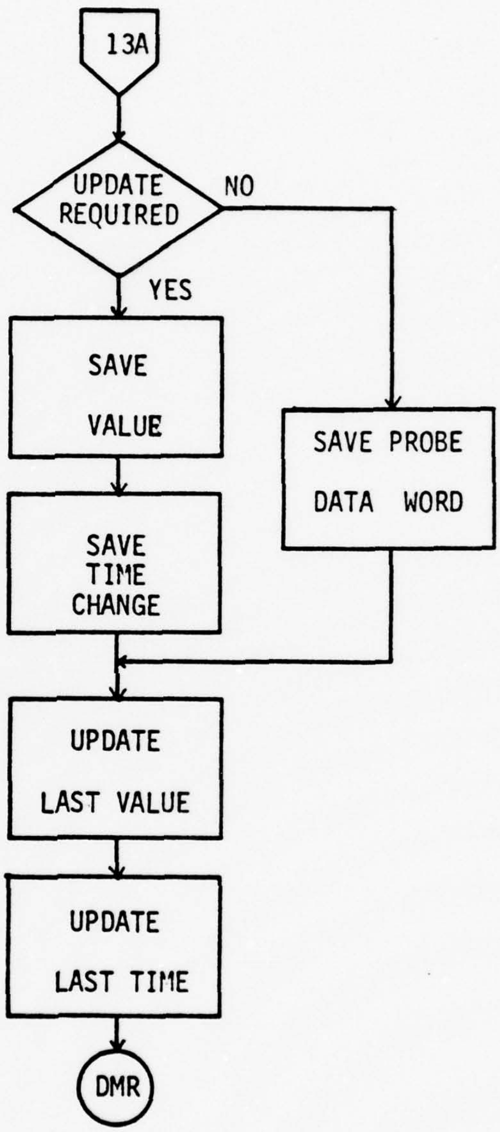

Figure 13. DMM Variable Change Data Mode
(sheet 2 of 2)

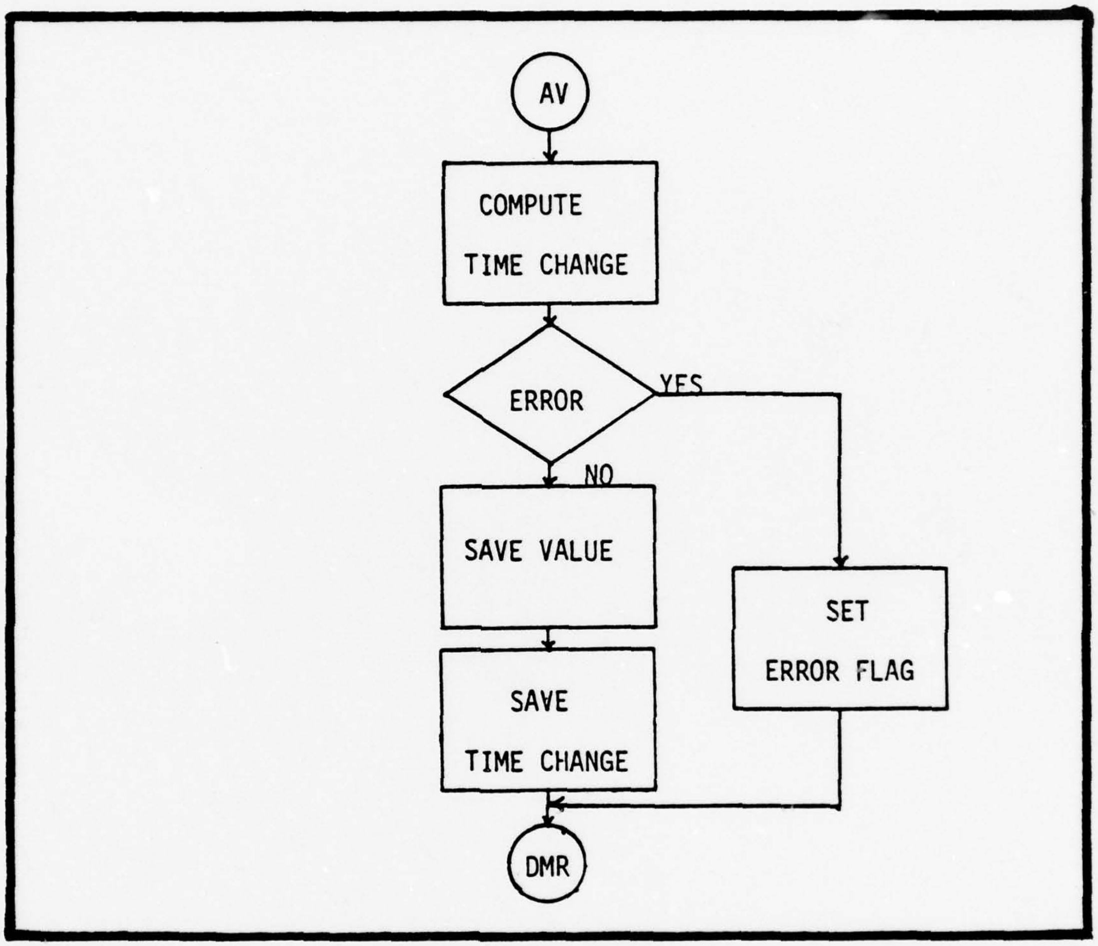

Figure 14. DMM Actual Value Data Mode

MPU generates a data list and places it into the SCM RAM. An external transfer command is issued (Figure 15) and the SCM MPU transfers the list to the external system through the UART (Figure 7). When the BMM is used, the data to be stored is temporarily saved in a data storage area, one area for each parameter. These data storage areas contain past values, counters, pointers and a page of parameter data requiring storage. As the data pages are filled, they are transferred to a bubble memory queue area of the RAM and held until transfer to the BMM can occur.

The transfer of data to the BMM (Figure 16) reouires that the module first be powered up. Next the MBMC is initialized and the first page and range of pages to be filled are loaded into the controller. The data is transferred to the memory module and the status of the transfer is monitored. When the last transfer is complete, the memory module is powered down and the data manager continues with the next cycle of data.

Data System Format

The parameter signals provided to the A/DC are scaled to range from 0 to 5 volts. The output of the A/DC is an eight bit word representing the absolute value of the parameter. Time information is available from a 16 bit counter. When a time word is fetched, both bytes of the time word are read and an eight bit word of the time scale factor appropriate to the parameter being serviced is retained and

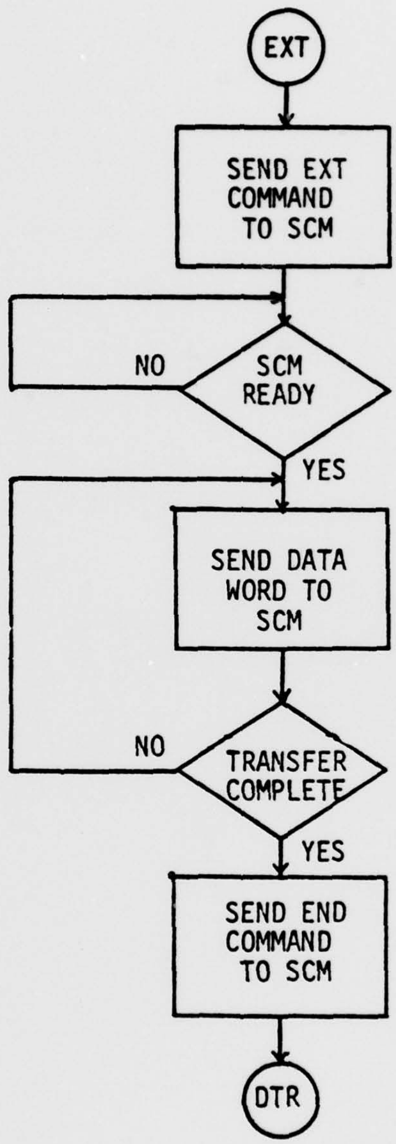

Figure 15. DMM Data Transmit to External System

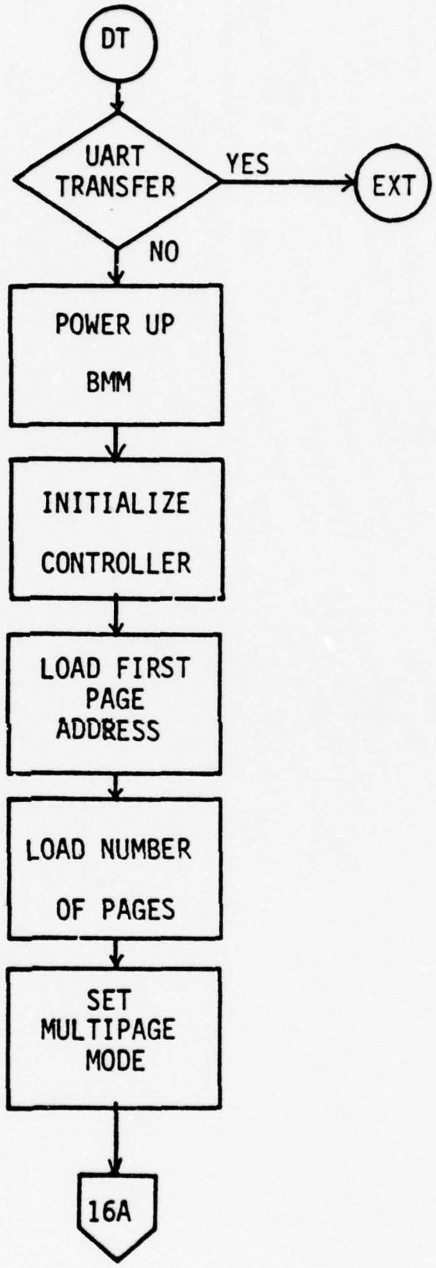

Figure 16. DMM Bubble Data Transfer
(sheet 1 of 2)

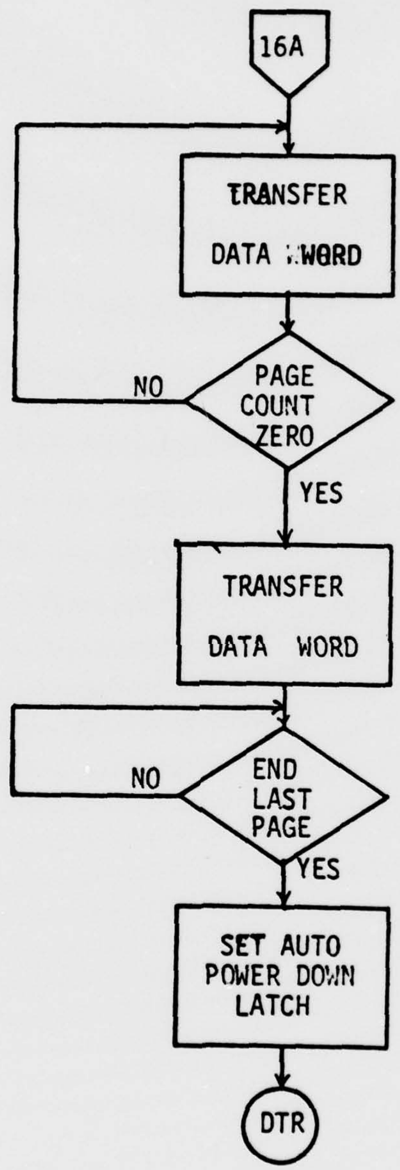

Figure 16. DMM Bubble Data Transfer
(sheet 2 of 2)

this becomes the parameter sampling time word used by the data management algorithm. When the data management algorithm computes a change in time, only the absolute value of the change is used.

Each parameter has a data storage area in the DMM RAM. These areas contain the information necessary to compute the parameter value changes or zones and the change in time. The saved data words accumulate in their respective data pages. Pointers and counters for each parameter keep track of the status of each data page and identify when the data pages must be transferred to the bubble memory queue. The bubble memories are structured in pages ranging in size from 18 words for the 92 kilobit memories to 28 words for the quarter megabit memories. The parameter data words are stored as pages, each page representing a parameter, and the first word of each page identifying which parameter that page represents.

Fixed Change. The fixed change method first computes the difference between the current parameter value and that of last significant value. This change is compared with the change value specified for that parameter. A data word is saved if they are the same. The change in time is computed and tested for a maximum value. If the change is not significant but the time is at its maximum, a no change data word is saved. Each time a data word is saved, the last parameter value and time words are updated. The construction of the data word is shown in Figure 17. Each fixed change parameter data storage area is structured as the example in Figure 18.

The time when the last data word was saved is located at LTIME. The actual parameter value at that time is located at LVAL. WRDCT is used to identify when the last data page word is saved. WRDCT also indicates when only enough data page spaces remain to update the actual probe value. NEXT points to the next available storage location in the data page. Parameter ID is a unique word which identifies this page of data as representing a specific parameter. The last two words of the data page contain the parameter actual value when the last significant change occurred and the time increment when that change occurred.

Zone. The zone method computes a data zone value by scaling the eight bit value to three bits. Eight zone values are represented by this method. The time change is computed in the same manner as the fixed change method. The current zone is compared with the last zone saved and a data word is saved if the zone has changed. A data word is also saved when the time change reaches its maximum value. Each time a data word is saved the last zone and time words are updated. The construction of the data word is shown in Figure 19. Each zone parameter data storage area is structured as the example in Figure 20.

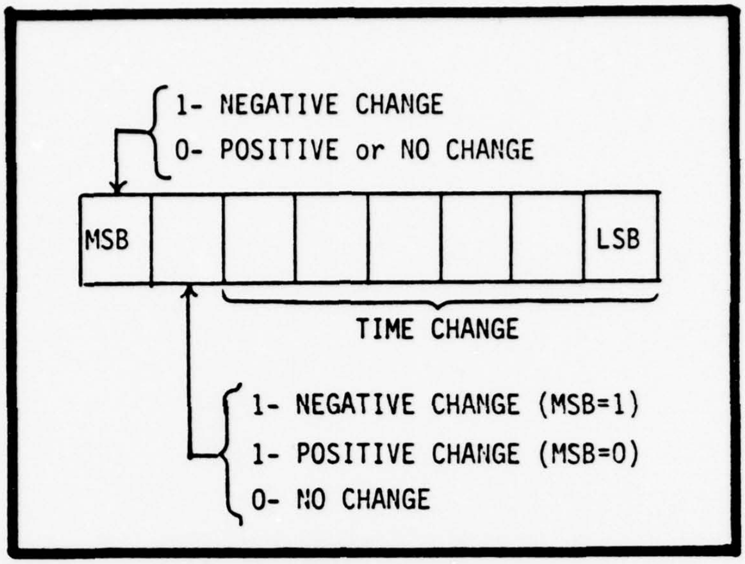

Figure 17. Fixed Change Data Word Format

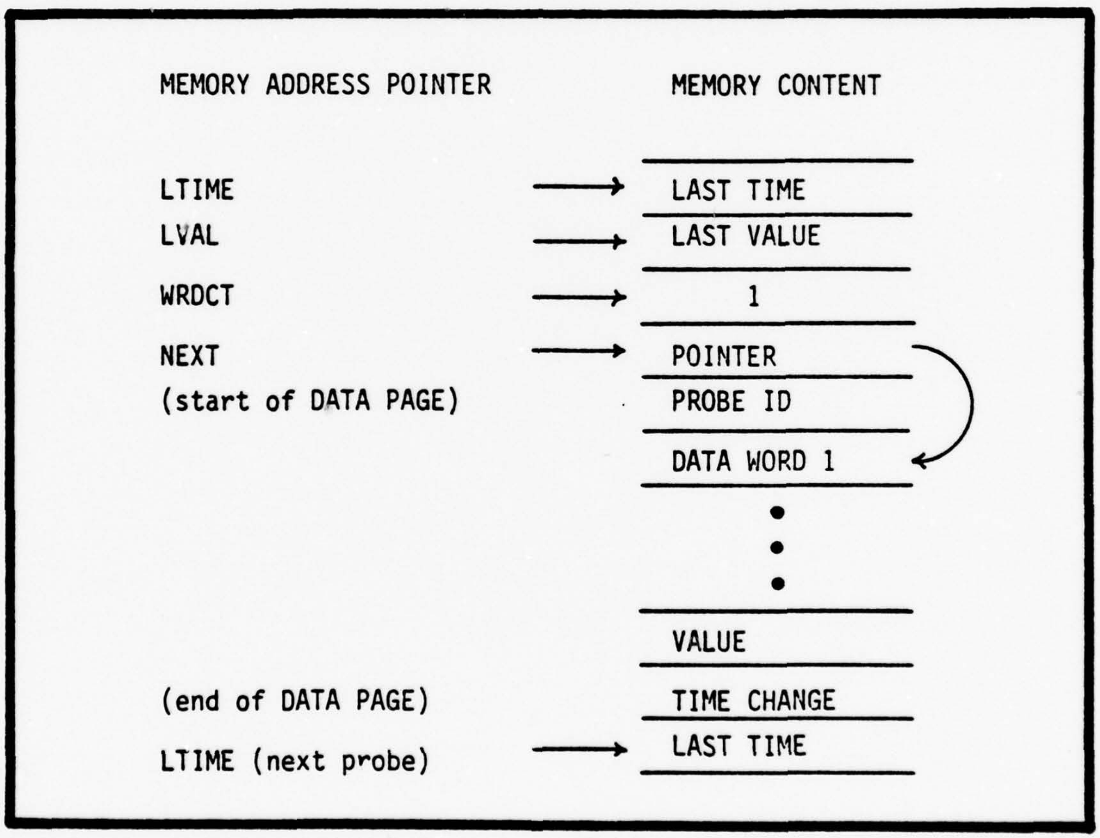

Figure 18. Fixed Change Data Storage Area Format

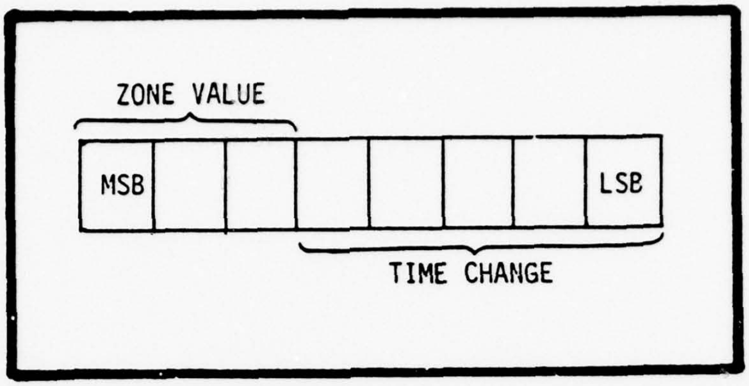

Figure 19. Zone Data Word Format

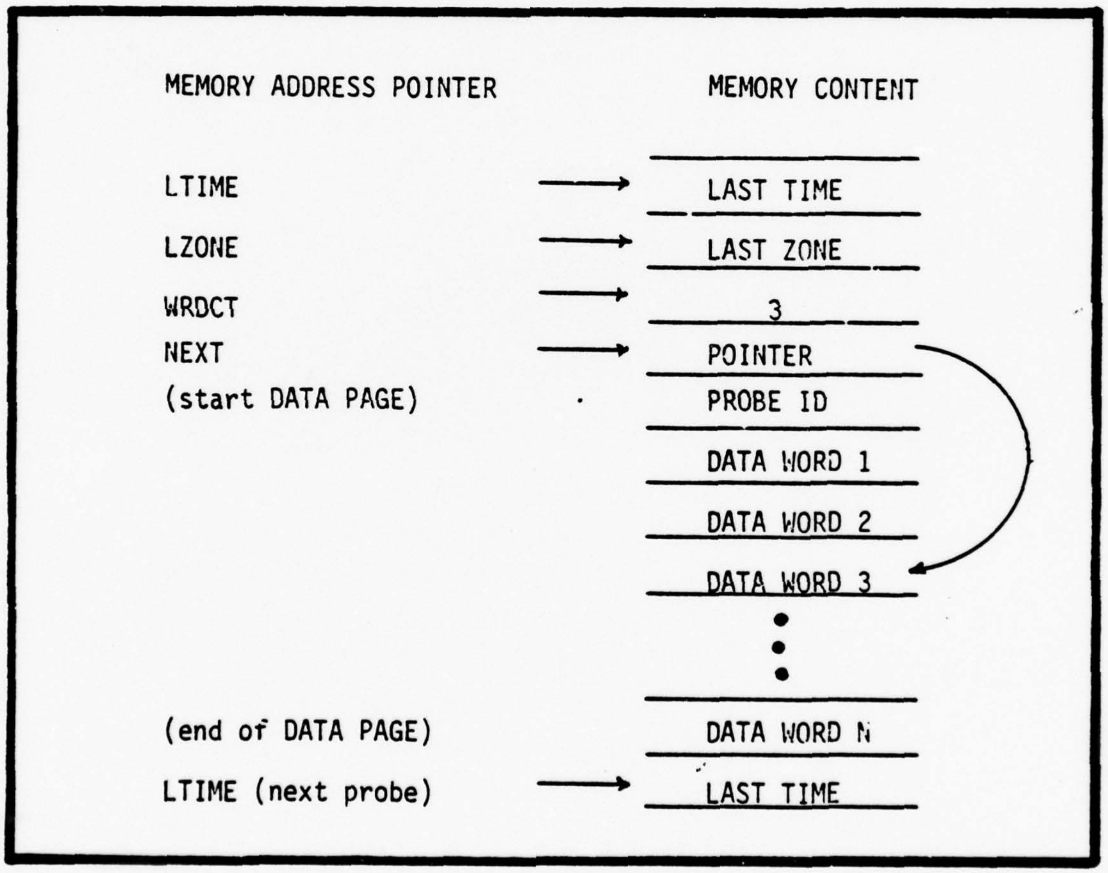

Figure 20. Zone Data Storage Area Format

The time when the last data word was saved is stored at LTIME and LZONE contains the zone value at that time. WRDCT is used to indicate when the last data page is saved. NEXT points to the next available storage location in the data page. Parameter ID is a unique word which identifies this page of data as representing a specific parameter.

Variable Change. The variable change method computes the change in time as in the fixed change mode. The value change is again the difference between the current value and the last significant value but now the actual change is saved rather than a fixed interval. The value change is tested for a significant change and a data word is saved if necessary. A data word is saved if the time change has reached its maximum value. Each time the data word is saved, the last parameter value and time words are updated. The construction of the data words is shown in Figure 21. Each variable change parameter data storage area is structured as the example in Figure 22.

The time when the last data word was saved is located at LTIME and the parameter value at that time is located at LVAL. WRDCT is used to identify when the last data page word is saved. WRDCT also indicates when only enough data page word spaces remain to save the parameter value and time change. NEXT points to the next available storage location in the data page area. NEXT increments by three on every second data word save. The parameter ID is a unique word

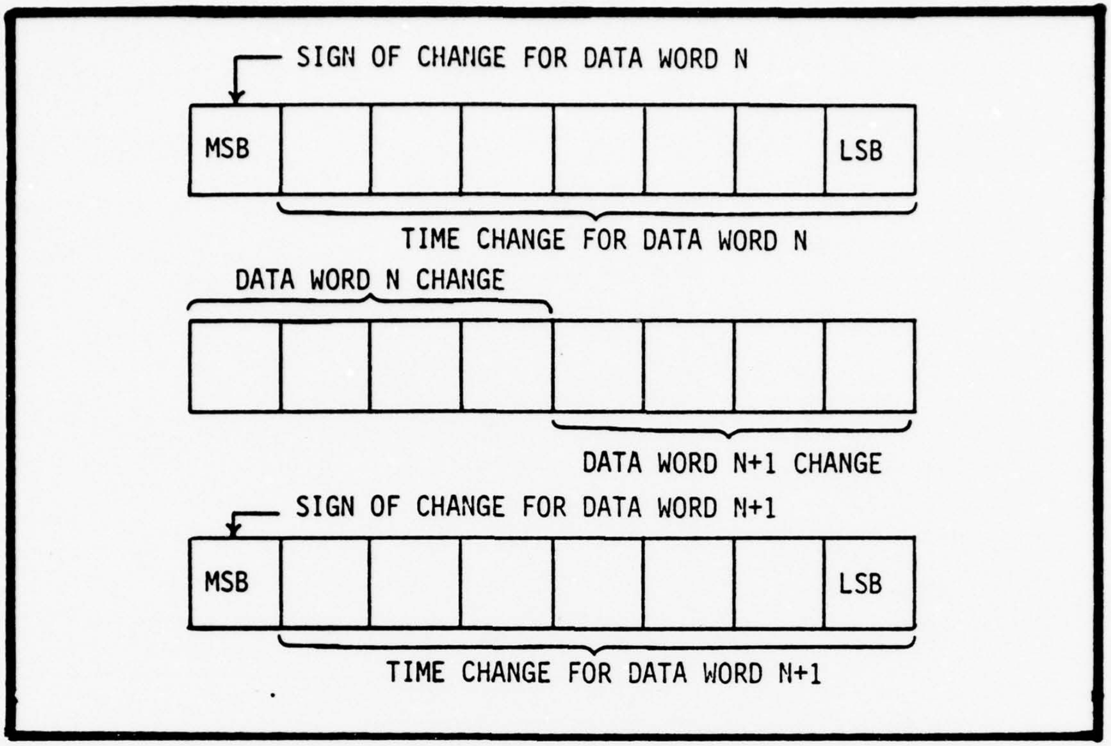

Figure 21. Variable Change Data Word Format

which identifies this page of data as representing a specific parameter. The last two words of the data page contain the parameter actual value when the last significant value occurred and the time increment.

Ground Support System

Data collected and saved during a mission is transferred to an analysis system through the ground support system (GSS). The GSS system design is not treated in this thesis. The concept of this system involves removing the memory module from IFPDAS III and connecting it to the ground support system. The GSS reads the data pages from the memory module and reconstructs the time history of the parameters using the inverse of the algorithm techniques which created the

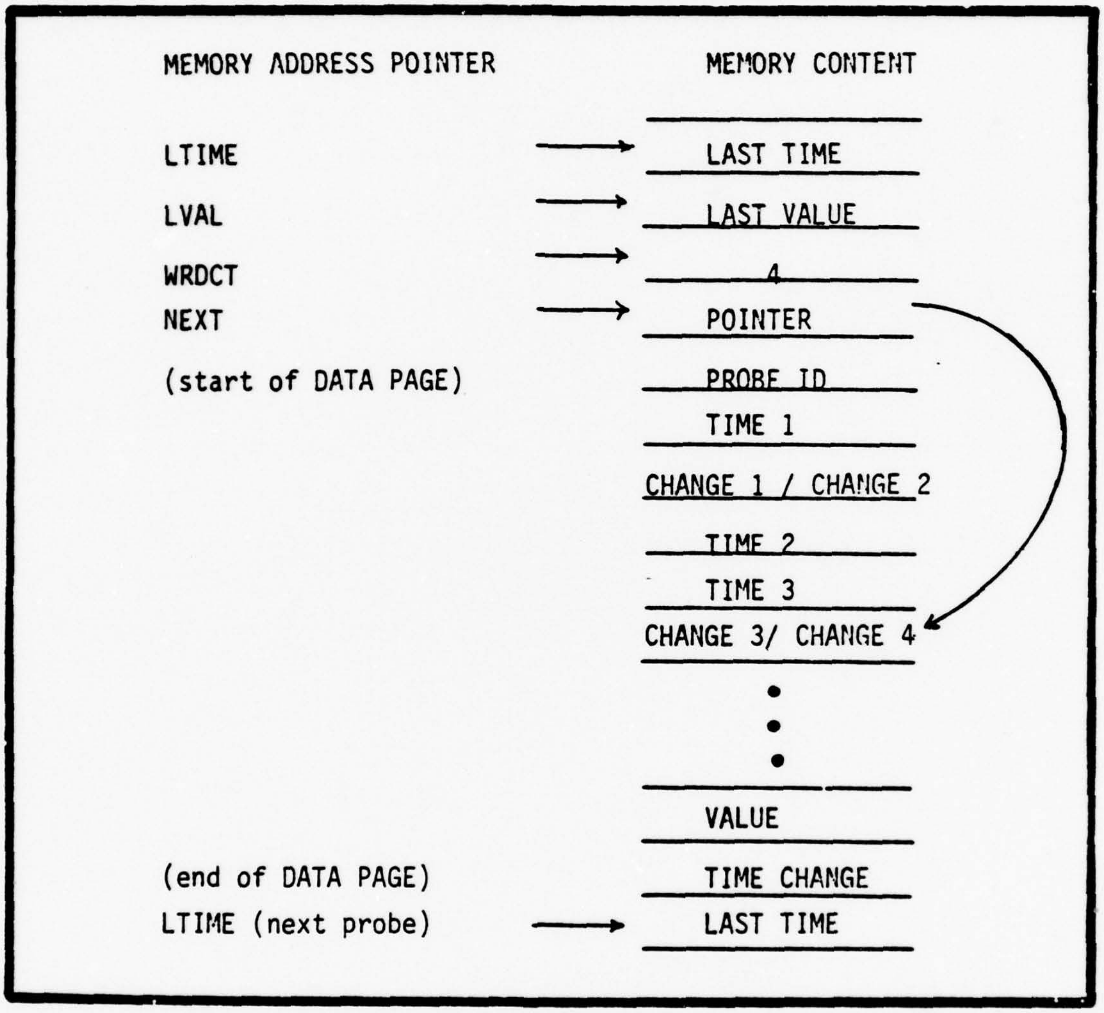

Figure 22. Variable Change Data Storage Area Format

parameter data. The parameter histories are then made available to the physiological analysis system.

The GSS is also used for maintenance and trouble shooting. The BMM is cleared and prepared for a mission by the GSS. The software operating systems are programmed into the IFPDAS III PROMSs by the GSS. Digital test words used for trouble shooting diagnastics are produced by the GSS and provided to the module under test.

Two examples of GSS software are given in Appendix B. The first routine reads data from the memory module in the multi-page mode. This data is provided to the reconstruction algorithm. The second example software is the memory clear and initialize routine to clear the entire memory and set the bubble to page zero.

<u>Summary</u>

The details of the IFPDAS III modules are presented in the first section. This discussion centered on specifying the type of components and their functions. In its six megabit configuration, the BMM provides for 52 stored words per second. This amounts to an average of one word for every three parameters sampled. A detailed hardware design and specification is found in Appendix A. The second section detailed the architecture of the SCM and DMM operating systems. The details included communications between the SCM and both the DMM and the aircraft-mounted system, through the UART. The detailed format of the three new data storage methods; fixed change, zone, and variable change is presented in the third section. The formats included a description of each type of data word and the format of the parameter data storage area in RAM. The last section presented an overview of a ground support system necessary to provide IFPDAS III maintenance and preliminary data analysis.

V FABRICATION AND TESTING

The limited fabrication accomplished during the design effort provided verification of interface concepts proposed in the final design. Some of the interface concepts fabricated are used directly in the IFPDAS III hardware design while other concepts fabricated are intended to only serve as guidelines for future design optimization efforts. All of the circuit concepts fabricated are applied to the IFPDAS III Development Tool constructed by Jolda and Wanzek (Ref 4). The specific circuit concepts fabricated consist of: interface circuits for all data sources external to the computer; control circuits for the A/DC; optimization of the heart rate counter, and an evaluation magnetic bubble memory system from Texas Instruments.

Development Tool

The development Tool constructed by Jolda and Wanzek was based upon an Intel SBC 80/20 (Ref 10&11) single board computer. The computer controlled the collection and conversion of nine analog parameter signals. An Analog Devices DAS 1128 A/DC performed the signal selection and conversions commanded by the central processor, an Intel 8080. A heart rate counter separate from the DAS 1128 provided a means of continuously monitoring heart rate. The Intel 8080 processor on the SBC 80/20 collected data for 10 seconds and then sent all the data collected to a Hazeltine 2000 Video Terminal/

Casette Recorder via a UART. The magnetic bubble memory was not available so the cassette recorder performed the function of the bubble memory for the purpose of concept validation.

During this design effort, circuits were fabricated which reduced the time required to transfer data and commands between the SBC 80/20 and the DAS 1128, heart rate counter, and bubble memory controller. The time reduction was accomplished by using address and control signals from the SBC 80/20 address, control, and data busses (Multibus). This technique accomplished in one or two computer instruction cycles transfers which took two or three cycles to perform using the I/O port interface technique implemented in Jolda and Wanzek. Using Multibus signals was easily accomplished for the required control circuits were already provided by the control circuits which interfaced the bubble memory controller to the SBC 80/20 via the Multibus. The heart rate counter optimization consisted of providing it with it's own reference oscillator, improving the accuracy and range of the count by both hardware and mathematical techniques, and improvements to the counter control circuits.

<u>Interface</u>. The control interface is reoriented to use the signals from the INTEL Multibus. Where possible, the control information is passed from the 8080 processor to the interface circuits through the Multibus address and data lines. The DAS 1128 and the magnetic bubble memory

controller (MBMC) are treated as I/O rather than memory addresses. The second four address bits, $\overline{\text{AD4}}$-$\overline{\text{AD7}}$, are decoded to provide the required unit select signals. The address map is located in Appendix D. The INTEL Multibus uses negative logic signals for address and data but the 8080 processor issues address and data as positive logic. Rather than using inverters for each address line, the software address assignments take into account the required inversion. The data lines to the magnetic bubble controller are inverted by tri-state buffers. The DAS 1128 and heart rate data lines interface through the parallel I/O ports. These I/O ports are also inverting so the output of the DAS 1128 is inverted internal to the system before it is sent to the I/O port.

<u>DAS 1128</u>. The A/DC system used is the same DAS 1128 used by Jolda and Wanzek. Only the most significant eight bits are sent to the I/O port in the 1's complement form. The control of updating the next probe MUX is accomplished through bits C6 and C7 of parallel I/O one. The next MUX address is passed to the DAS 1128 through the lower four bits of the data bus and is strobed into the DAS 1128 by issuing an OUT PROBE command. This command is decoded and activates the STROBE 2 line. The conversions are started automatically by routing DLY OUT to $\overline{\text{TRIGGER}}$. When the EOC signal is issued, it initiates a 500 nanosecond pulse at TRIGGER. The end of this pulse starts the next conversion

of the same MUX and this process continues until a new MUX address is strobed. EOC also strobes the data into port A of parallel I/O one.

Heart Rate. An oscilator circuit is added to drive the heart rate counter rather than using a signal from the SBC 80/20 timer. The oscilator generates a 262,144 Hz square wave which is divided down to 8 Hz by four sequential counters. The 8 Hz drives the Heart Rate counter rather than the 225 Hz used by Jolda and Wanzek. This allows heart rate detection below 50 beats per minute by using the counter in the following equation.

$$\text{Heart Rate} = f(60 \text{ seconds})\left(\frac{\text{count}}{255}\right) + 1.9 \qquad (4)$$

Count is the word latched into Port A of parallel I/O two. This port is inverting so a zero count appears as 255 to the computer. As the actual count increases, the count seen by the MPU decreases and is saved in this state for used in (4). The f in (4) is the frequency input to the counter (8 Hz). A computer preceived count of zero gives a minimum heart rate of 1.9 beats per minute. Each count equals 1.9 beats per minute and the maximum deductable heart rate is 482 beats per minute. The R wave detector, the counter controller and strobe generator operate as designed by Jolda and Wanzek but are rewired to improve the Heart Rate counter reset and strobe pulse pattern.

Reset/Interrupt. A manual reset switch is provided to reset the entire development system. This switch grounds the Multibus master reset line. Two debounced switches activate interrupt lines one and seven.

Acknowledge. All interface system commands except the magnetic bubble memory commands provide acknowledge by routing the unit select signal to $\overline{XACK}$. The ready signal from the magnetic bubble controller is high when the controller is ready and when the controller is not selected. The controller ready signal is gated by MBCR $\oplus$ MBCW so the ready from the magnetic bubble controller is the proper level and occurs only when the controller is selected and ready.

Memory Module Select. The magnetic bubble controller can control up to four 92 kilobit bubble memory modules. These modules must be selected before data transfer takes place. Currently three flip-flops provide the select signals by setting the select word from the data lines when the OUT MBPUR command is issued. The flip-flops are reset by OUT MBPDR. The fourth flip-flop state at Q indicates that a module is selected.

Power Control. A single flip-flop monitors data line 3 when OUT PWOFF is issued. The state of this flip-flop indicates when the operating system shut down IFPDAS III.

Magnetic Bubble Memory

The bubble memory controller and interface circuits operate as described in Appendix C. Frequent changes in logic circuit design by Texas Instruments and late arrival of parts have prevented verification of the entire memory system at this time. The only documents existing for the memory system are vague in their explanation of the signals to and from the controller and the logical sequence of commands. The following discusses the interface hardware and those operating considerations not discussed in the Texas Instruments documents (Ref 12 thru 21).

Interface. The lower four bits of the address bus go directly to the bubble memory controller (MBMC). The MBMC decoding ROMs U1&U2 are not used. The unit select signals are decoded from the second four bits of the address bus and the select and read/write signals are sent to a jumper plug in U1. The MBMC data line buffers U3 & U4 are not used, *instead a pull-up jumper* plug is provided in place of the 74LS226 buffers. The interface board provides data buffering to the Multibus through inverting buffers which are enabled by the $\overline{MBCRD}/\overline{MBCWR}$ chip select signals. To provide synchronization for the ready signal, the Multibus $\overline{CCLK}$, 9 MHz, signal is divided by three and sent to the controller through MBMC P2 pin 29. This delays the ready and causes the 8080 to enter an extra wait state but it insures stable data to and from the MBMC. Since U3 and U4 are not used, the MBMC P2 pin 20 clock signal is not used.

Addressing. The MBMC is addressed when the upper nibble of the I/O address is a 1 (Hex). The lower four address bits go directly to the controller and the software must take into consideration the level inverting by the Multibus.

Commands. When a reset is issued the MBMC registers are cleared and it is placed in a single page mode. The minor loop size and page size registers must be set and a software reset command issued before data transfers can occur. The single/multi page mode remains set until changed by a specific command or hardware reset. When testing the status bit to detect when the MBMC is finished executing the command, the Interface Application Notes (Ref 18) indicate that it takes 10 microseconds for the MBMC to set the busy bit. The recommended double test of the busy bit does not work when the MBMC is addressed by an IN or OUT command. The time required to execute an IN command takes longer than the time necessary to set the busy bit. The first loop of the idle test is replaced by a NOP time filler. The recommended busy bit test to detect the end of execution is used. The "Cold Start Initialization" is used only when a bubble module is to be used which may have been powered down before the previous transfer was completed. Under normal cases the "Cold Start Initialization" is not necessary.

Command Sequences. Each time a page is to be written the desired page number must be entered into the page select register. For single page transfers, that page is where the data is transferred. For multipage transfers the selected page marks the starting location for the transfer. For the single page mode the read/write page instructions are straightforward from the Interface Application Notes (Ref 16). For multi page transfers, the page counter register is loaded with the number of pages to be transferred. During the transfers, the MBMC interrupt line rather than byte read/written status indicates when the next byte is to be transferred (Ref 21). The page counter status is checked between transfers and when the page count zero bit is set, 18 more bytes are to be transferred before the entire operation is complete. The memory module can be powered down after the completion of the execution, no more than 12.8 milli-seconds after the last command is issued.

Module Selection. Although the MBMC can support up to four modules, only three can be used without redefining a signal pin on the MBMC interface cable. The redundancy ROM, U11, is programmed to operate with module one selected. The data line $\overline{DB\emptyset}$ activates the module one select flip-flop which drives interface pins 4 and 22.

ROMs. The function ROM, U10, is programmed with the latest version of the function generating software (Ref 19). Of the 157 minor loops in the bubble memory, only 144 are used. This allows up to 13 loops to be defective and still have a useable memory. The masking out of the bad loops is accomplished through the redundency ROM. The redundency

ROM, U11, is programmed to provide the following bad loop addresses (HEX): 0000, 004C, 0050, 0051, 0052, 0053, 0054, 0055, 0068, 0069, 006A, 006F, and 008E. Loops 0000 and 0068 are arbitrarily added to the 11 loops already defined bad by Texas Instruments to make up the required set of 13 bad loops.

Modifications. Two modifications are implemented on the MBMC board. The first modification changes the generation of $\overline{\text{STROBE}}$ and is documented in the Interface Application notes (Ref 17). This modification involved adding a 74LS109 in the U22 position and redefining the utilization of U12A, U15A, and U15C. Appendix C illustrates the completed modification. The second modification implements Modification Instructions for 92K Chevron MBM Controller Timings (Ref 19).

Page Size. The page size for the 92 kilobit memory is 18 eight-bit words. In the single page mode, an entire page of data must be written into or read from the MBMC first-in-first-out (FIFO) register to complete the transaction. Incomplete transactions can leave the bubble in an indeterminate state. During multipage transfers, the FIFO is only one word long and thus only one word is transferred at a time.

MBMC Status Bits. The MBMC status register contains 8 bits reflecting the status of the controller. Only three bits: Page Read/Written, bit zero; Controller Busy, bit five; and Page Count Zero, bit six, are usable. The remaining bits are for diagnostic testing of the MBMC or are not properly implemented.

Testing. To date only the MBMC been tested. All read and write instructions to MBMC registers work properly. Late delivery and programming of the ROMs prevented full scale testing of the memory module. Testing of the module control signals is continuing and when finished, the IFPDAS software driver testing will begin.

Software Design and Testing

Appendix B lists example IFPDAS software for the SBC 80/20 based development tool. This software collects and saves data without computing any functions. The software design testing is delayed in lieu of fabrication of the Magnetic Bubble Memory System. Once the memory system checkout is complete, the entire software package will be tested for interface operations by applying controlled analog input signals and monitoring the data sent to the bubble memory via the DTOUT subroutine. Replay of the bubble memory contents is verified against the data sent to the memory. This procedure verifies the bubble memory operation and its interface. Verification of data management algorithms is accomplished by comparing the actual data words saved against those expected from the known inputs. This software is meant to serve only as an example of algorithm implementation.

Summary

The operation of the circuits fabricated during this design effort indicate that execution speeds are increased by interfacing data sources directly to address and data busses. The heart rate counter operation is improved and provides an expanded of from 1.9 to 482 beats per minute. The value per bit is a constant 1.9 beats per minute throughout the entire range.

VI CONCLUSIONS AND RECOMMENDATIONS

The intent of this design effort is to provide a baseline design for third generation Aircrew Inflight Physiological Data Acquisition System. This baseline design and the specifications are sufficient foundations from which a prototype system can be fabricated.

Conclusions

The System Requirements Study shows that it is feasible to monitor physiological data with an 8-bit digital system. The requirements study also identifies alternate schemes for recording data which provided five levels of trade-off between data fidelity and quantity of data which may be stored. The system design describes the functional and specific design aspects of the four IFPDAS III modules: Power, Signal Conditioner, Data Manager, and Bubble Memory. Appendix A details the Module hardware architecture, design variations based upon CMOS and NMOS technologies, and presents design considerations and system specifications. This design effort did provide hardware architecture and system specifications which do constitute a system baseline.

The requirements study did not identify any parameter signal accuracy or sampling rate requirements which the hardware design cannot accomodate within the stated accuracy limit of 1%. The hardware architecture necessary to implement IFPDAS III requirements does not contain any hardware associated constraints other than memory size. The Bubble Memory Module, using six megabits of storage, accomodates data storage rates equivalent to 1/3 of all the data sampled during every 50 msec period. SAM cannot presently specify a desired data acquisition rate therefore they have no objections to this data rate for a prototype system. The final conclusion is that the baseline NMOS system is feasible and complies with system requirements and design architecture requirements.

Recommendations

The primary recommendation is that the prototype system be constructed using the NMOS design. The hardware architecture should be optimized with the latest commercial interface and memory components. An operating system must be developed and optimized for the hardware design. The two efforts must be conducted in parallel as they are closely interdependent. It is most important that the proper tools be used to assist in these developments. The most important tool is a microcomputer development system which supports the microprocessor selected for the prototype design. Examples of such development systems are the INTEL MDS-230, the Motorola Exorciser, or the Tektronix 8002/8001 Microprocessor Lab. These systems must also support a higher order language compiler and cross compiler as well as an assembly language assembler. All of these tools are necessary to develop a quality system. The development system hardware may be used as the Ground Support System once IFPDAS III becomes operational.

A candidate IFPDAS III memory system must be identified and purchased from a vender currently providing magnetic bubble memories. Such a system must have the growth potential of being able to easily substitute larger memory chips. When the memory configuration is defined then a complete power requirement study must be made with consideration given to heat dissipation as well as operating time.

The analog signal conditioners create potential problems in terms of number of power sources required and number of components in each channel. Several opportunities exist for development of custom analog interface circuits operating from a single power source and including several stages of amplification. Such custom designs are required for each type of physiological sensor used. In the case of flow rate, partial pressure of oxygen, and partial pressure of carbon dioxide detectors, SAM wishes to replace the sensors presently in use, therefore opportunities exist for development of entire sensor/amplifier systems.

Analog-to-digital conversion is the commonly accepted method for converting the analog levels to their digital counterparts. Integrated circuit manufacturers are making new versions of low signal level controlled voltage-to-frequency converters (V/FC). The emphasis on these circuits in new designs (Ref 22&23) indicates that an optimization tradeoff study of A/DC versus V/FC is necessary to identify whether V/FC should replace A/DC. Since the frequency of the V/FC output pulses correlates with the analog input signal, the digital conversion is accomplished by counting the pulses during a known interval. A digital multiplexer circuit allows several V/FCs to drive an eight bit counter and analog signal multiplexers can be used on the V/FC inputs to further expand the converter input channels. The use of V/FC may make a significant impact of the analog signal amplification required and provide faster conversion since parallel conversion channels are feasible. The V/FC concept may also reduce the actual number of circuit chips required if the amplification requirements are reduced.

The aircraft cockpit abounds with electromagnetic interference sources. Such sources make the transmission of analog and digital signals difficult. A potential answer to the problem of how to reduce the induced interference is the use of fiber optic channels to transmit the data. This technique can be investigated for both the analog and digital transmissions to the external systems. The primary considerations requiring investigation are how much power is required to support fiber optic data links and how much space do they require.

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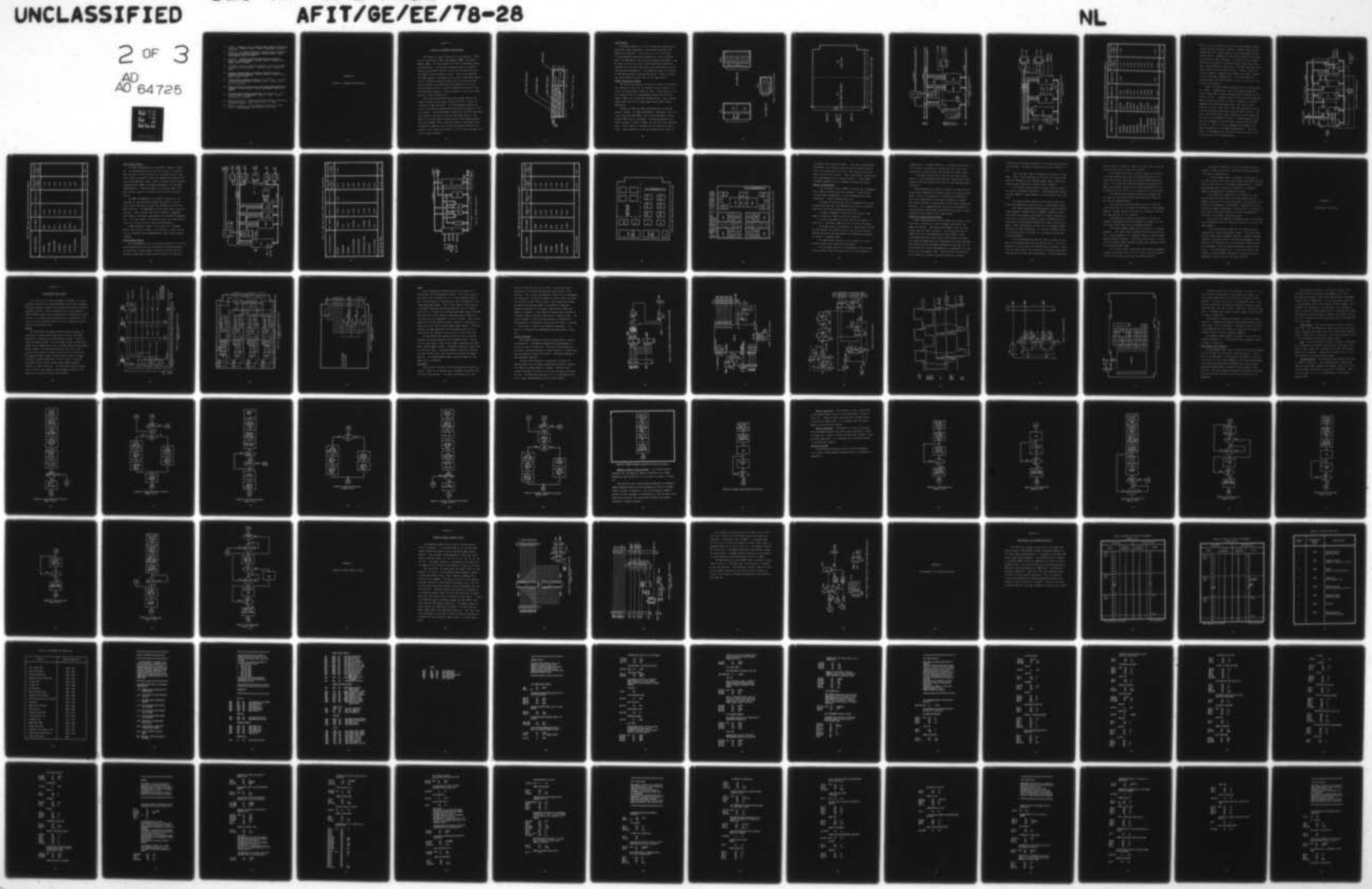

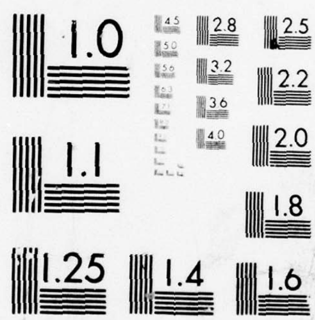

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APPENDIX A

IFPDAS III Hardware Architecture

Appendix A

IFPDAS III HARDWARE ARCHITECTURE

The IFPDAS III design consists of four modules: Power, Signal Conditioner (SCM), Data Manager (DMM), and Bubble Memory (BMM). All four modules fit into a rectangular metal ventelated box. The box has removable ends for changing modules and parallel groves in the sides to guide and hold the module circuit boards in place. The box end opposite the power module is attached to the signal conditioner module and all external connector plugs attach to this end plate. The plug types are unspecified but provide for up to 22 analog signals; serial, digital transmit and receive lines; and start/stop signals. Figure 23 shows a side view of the modules inside the metal box.

Both signal conditioner and data manager modules are single printed circuit boards measuring 5 $\frac{3}{4}$ X 5 inches including the edge connector. The bubble memory module consists of two borads connected back-to-back and spacial 0.125 inchs apart. The bubble memory controller, function generator and interface circuits are on the top board which is the same size as the signal conditioner and data manager module. The bubble memory chips, function drivers, sense amplifiers, termination networks, diode arrays and power switchers are mounted on the lower board which is 5 X 5 inches and does not have an edge connector.

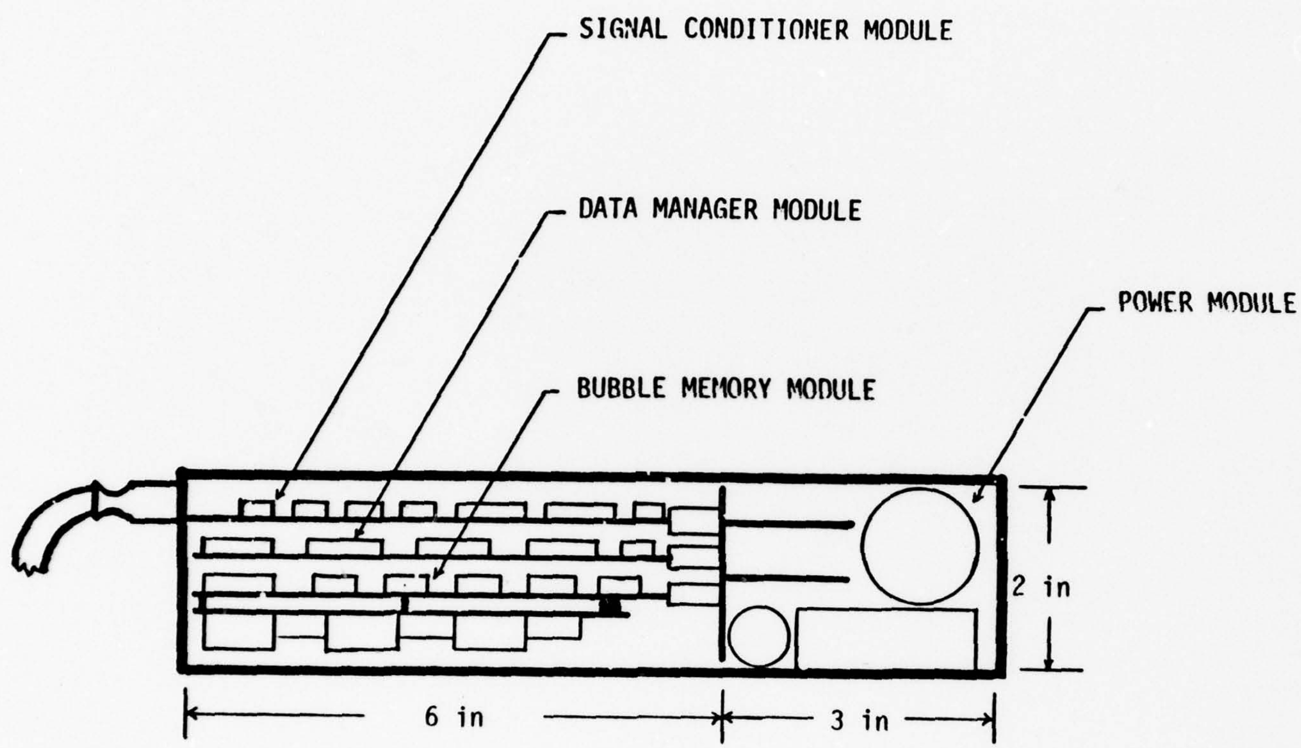


Figure 23. IFDAS III Layout, Side View

Power Module

The power module is 3 X 2 X 5 inches and contains the batteries, power regulators, interconnect backplane and edge card connectors. Two D size, 1.4 dia X 2.5 inch, lithium batteries provide an average 5.5 volts at 10 amp hours, 55 watt-hours, for the low voltage requirements. Ten AA size, 0.6 da X 2.0 inch, lithium batteries provide an average 12.5 volts at 3 amp hours, 37.5 watt-hours, for the high voltage requirements. The remaining space is devoted to voltage regulators and the back plane. Figure 24 shows the top, bottom and side views of the power module.

Signal Conditioner Module

The functional layout of the SCM is shown in Figure 25. The functional areas for the analog circuits, digital circuits and interconnect plugs are shown. The functional layout supports both the complementary Metal-Oxide Semiconductor, CMOS, and N type MOS implementations. Both designs depend upon the use of single power source CMOS analog amplifiers.

Figure 26 shows the CMOS implementation of the SCM digital system. The CMOS technology is used where such circuits exist and some NMOS circuits are used where no comparable CMOS type is available. The microprocessor unit (MPU) Q output is used to signal the end of a minor sequence loop. The EF inputs to the MPU are the interrupt service flags. Data transfers to the data manager occur when the

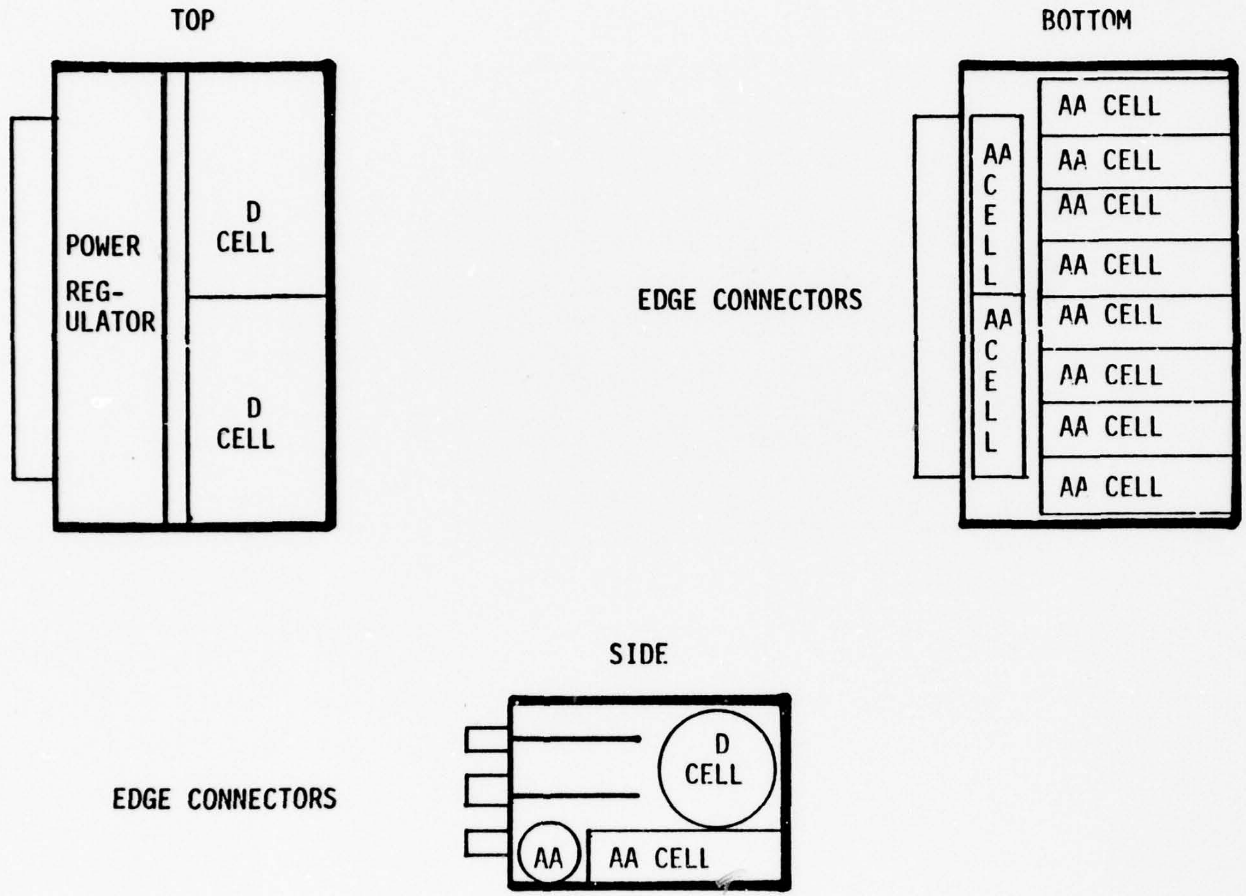


Figure 24. IFPDAS III Power Module

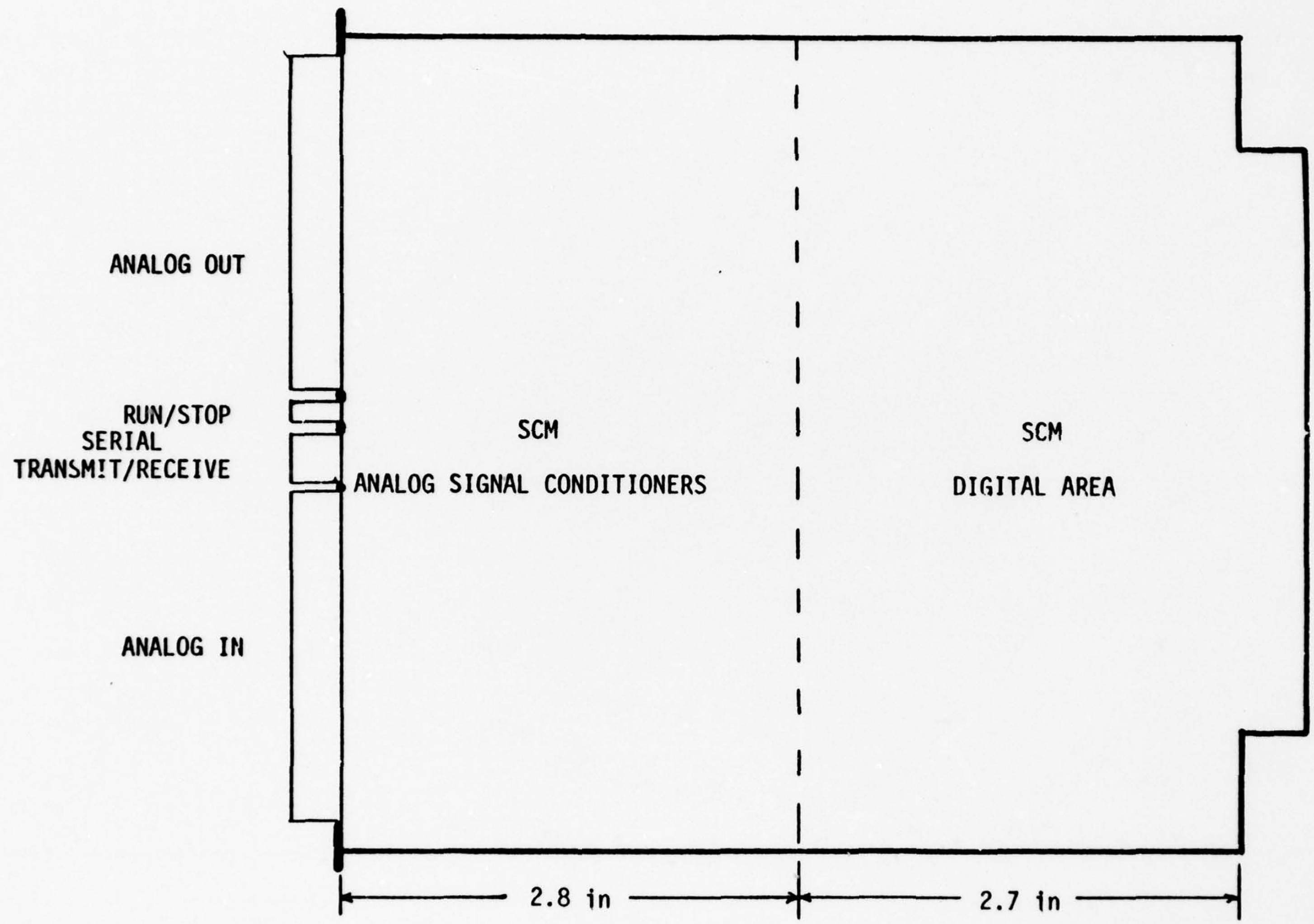


Figure 25. IFPDAS III Signal Conditioner Module Functional Layout

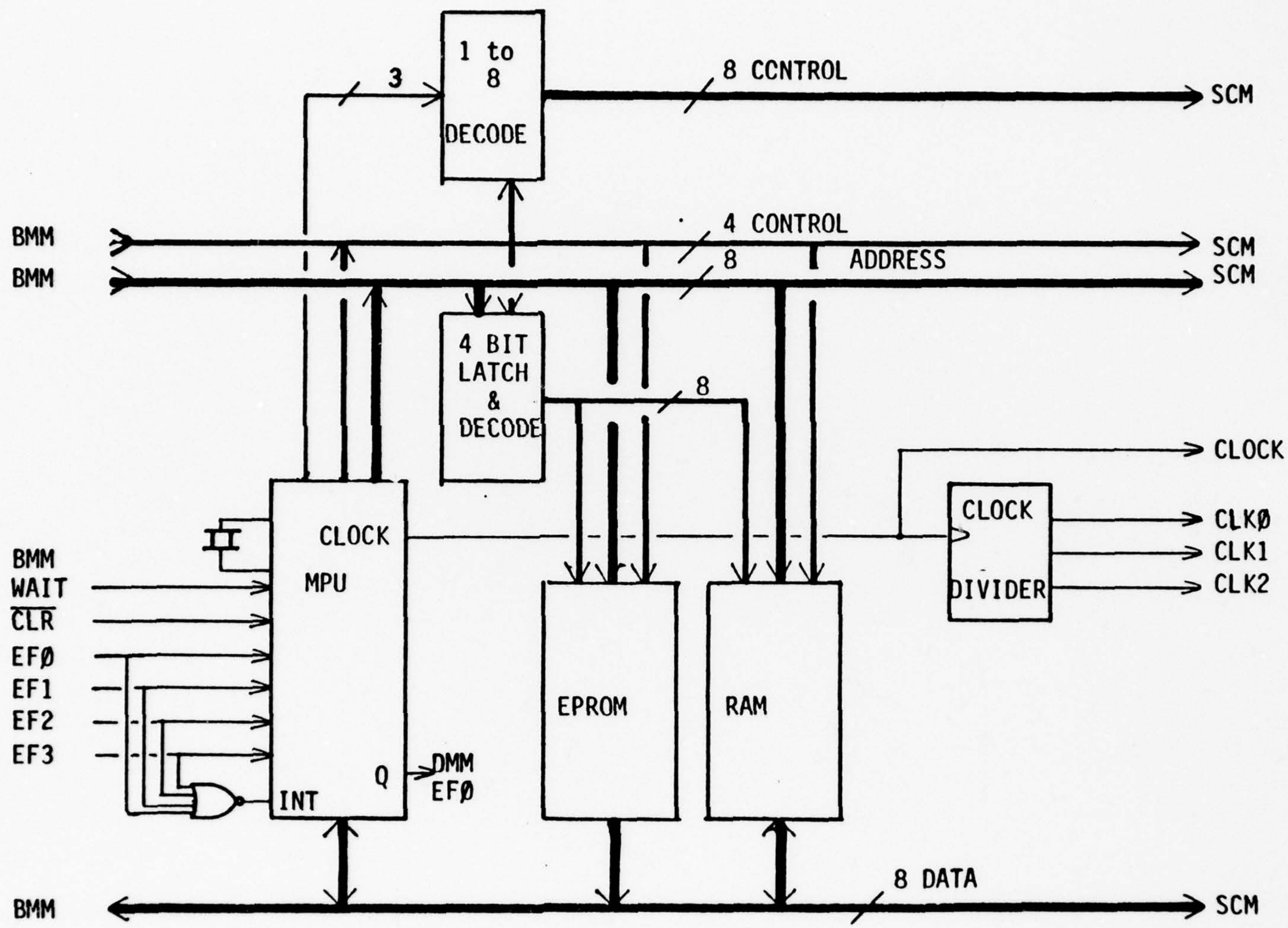


Figure 26. SCM CMOS Implementation
(sheet 1 of 2)

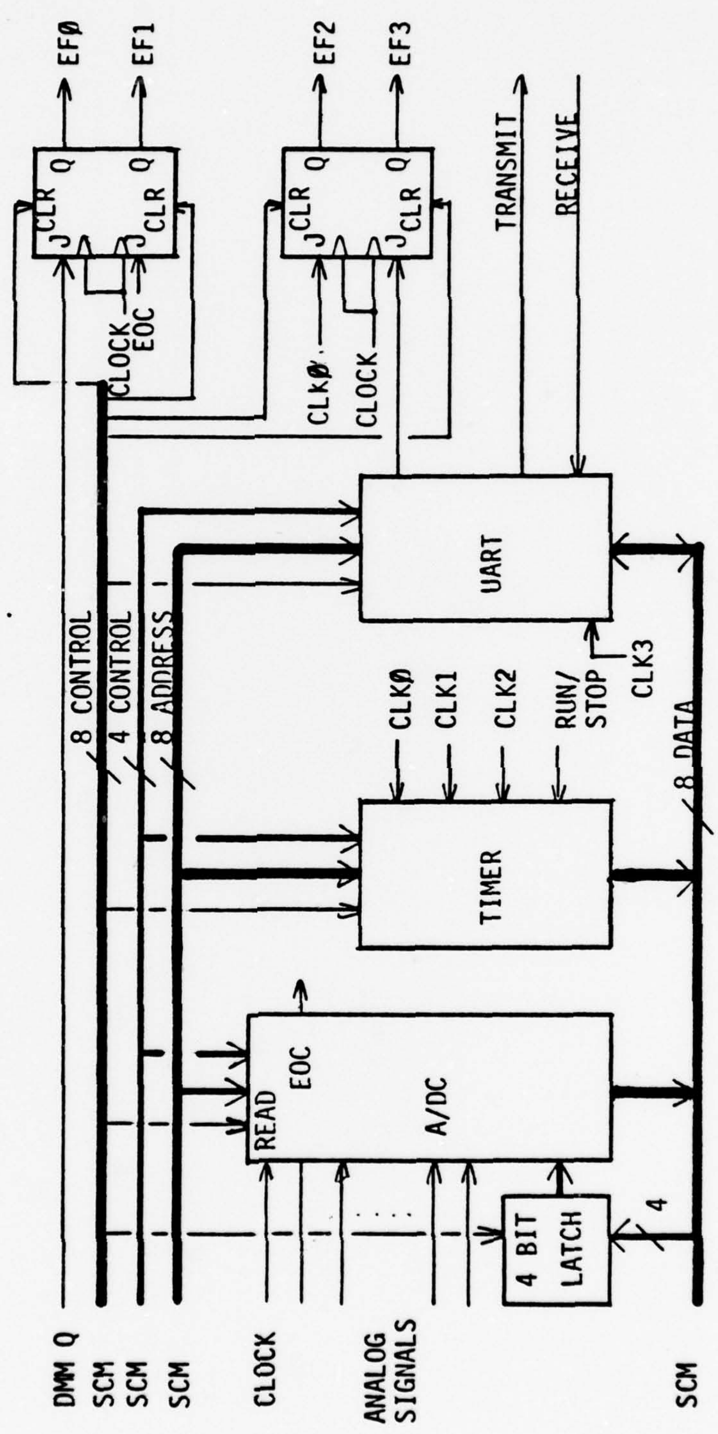


Figure 26. SCM CMOS Implementation
(sheet 2 of 2)

Table II. CMOS Signal Conditioner Module Maximum Power Consumption

ELEMENT/TECHNOLOGY	PART NUMBER	CURRENT @5V	CURRENT @12V	MISSION POWER (4hr) watt-hours 5V	MISSION POWER (4hr) watt-hours 12V
MPU/CMOS	CDP1802D	0.005	0.001	0.010	0.048
EPROM/NMOS	2758	0.105	-	2.010	-
RAM/CMOS	CDP1823SD	0.0063	-	0.126	-
UART/CMOS	CDP1854D	0.001	-	0.020	-
A/DC/CMOS	ADC0816	0.050	-	1.000	-
TIMER/NMOS	M6840	0.110	-	2.200	-
LATCH-DECODE/CMOS	CDP1858D	0.0128	-	0.256	-
LATCH/CMOS	74C175	0.0003	-	0.006	-
1 of 8 DECODE/CMOS	CDP1853D	0.0128	-	0.256	-
J-K FLIP-FLOP/CMOS	74C73	0.0006	-	0.012	-
CLOCK DIVIDER/CMOS	C4020	-	0.001	-	0.048
AND/CMOS	CD4082	0.001	-	0.002	-
TOTAL MISSION POWER				5.878	0.096

MPU is put into a pause state and the data manager assumes control of the SCM digital busses. Commands from the data manager MPU are placed directly into the SCM RAM during an SCM MPU Pause. Commands and data from the UART are fetched by servicing a UART interrupt. The timer circuit contains three 16-bit counters to provide elapsed time, heart rate, and a second discrete input count. The UART baud rate clock comes from the clock divider circuit. Table II shows the circuit elements, suggested part numbers and power consumption for the CMOS implementation. The total power is a maximum figure with some reserve since all circuits are not active simultaneously.

Figure 27 shows an NMOS implementation of the SCM digital system. Commands and, flags, are passed between the signal conditioner and data manager modules through the parallel I/O ports. Parameter data are also passed through the same I/O port, one byte at a time in response to specific commands from the data manager MPU. The timer circuit supplies the band rate clock to the UART and keeps track of the 50 millisecond time pulses from the RAM-I/O timer. The heart rate and discrete input channels are read through the I/O ports of the EPROM-I/O circuit. The MUX address, load, and start commands to the A/DC are passed through the RAM-I/O port B. Table III shows suggested part numbers and power consumption for the NMOS implementation. The total power is a maximum figure with some reserve since all circuits are not active simultaneously.

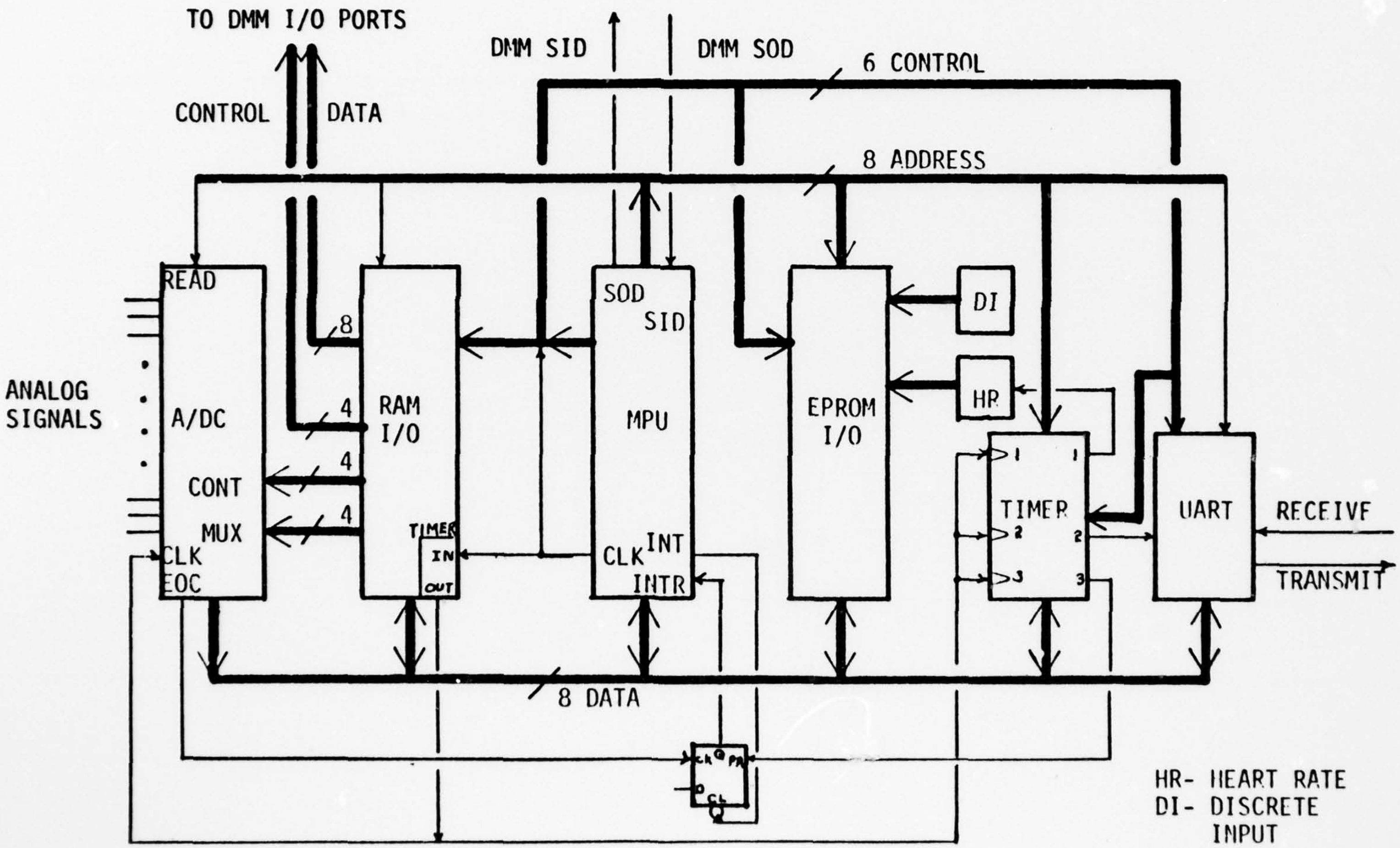


Figure 27. SCM NMOS Implementation

Table III. NMOS Signal Conditioner Module Maximum Power Consumption

ELEMENT/TECHNOLOGY	PART NUMBER	CURRENT @ 5V	CURRENT @12V	MISSION POWER (4hr) watt-hours 5V	MISSION POWER (4hr) watt-hours 12V
MPU/NMOS	8085B	0.180	-	3.600	-
RAM-I/O/NMOS	8156	0.180	-	3.600	-
EPROM-I/O/NMOS	8755	0.180	-	3.600	-
TIMER/NMOS	8253-5	0.002	-	0.010	-
UART/CMOS	IM6402	0.007	-	0.035	-
A/DC/CMOS	ADC0816	0.050	-	1.000	-
D FLIP-FLOP/CMOS	4013	0.001	-	0.020	-
TOTAL MISSION POWER				11.865	NONE

Data Manager Module

The CMOS implementation of the DMM is shown in Figure 28. The implementation uses the MPU Q output to signal an SCM interrupt and the EF inputs as interrupt service flags. Three state bus buffers isolate the DMM busses from the SCM bus and the BMM data lines. Table IV shows circuit elements, suggested part numbers and power consumption for the CMOS implementation. The total power is a maximum figure with some reserve since all circuits are not active simulataneously.

The NMOS implementation is shown in Figure 29. All transfers to the SCM occur through the parallel I/O port. Three state tranceivers connect the DMM data bus with the BMM controller. The BMM power control comes from a parallel I/O port. Table V shows the circuit elements, suggested part numbers, and power consumpution for the NMOS implementation. The total power is a maximum figure with some reserve since all circuits are not active simultaneously.

A DMM functional layout is not specified. The DMM module size, 5 $\frac{1}{2}$ X 5 inches, is sufficiently large to allow for any currently known implementation using custom support circuits.

Bubble Memory Module

The configurations of custom design support circuits for bubble memories are not yet specified by the manufacturers. The functional layout shown in Figures 30 and 31 are only estimates based upon custom support circuits for the 92k

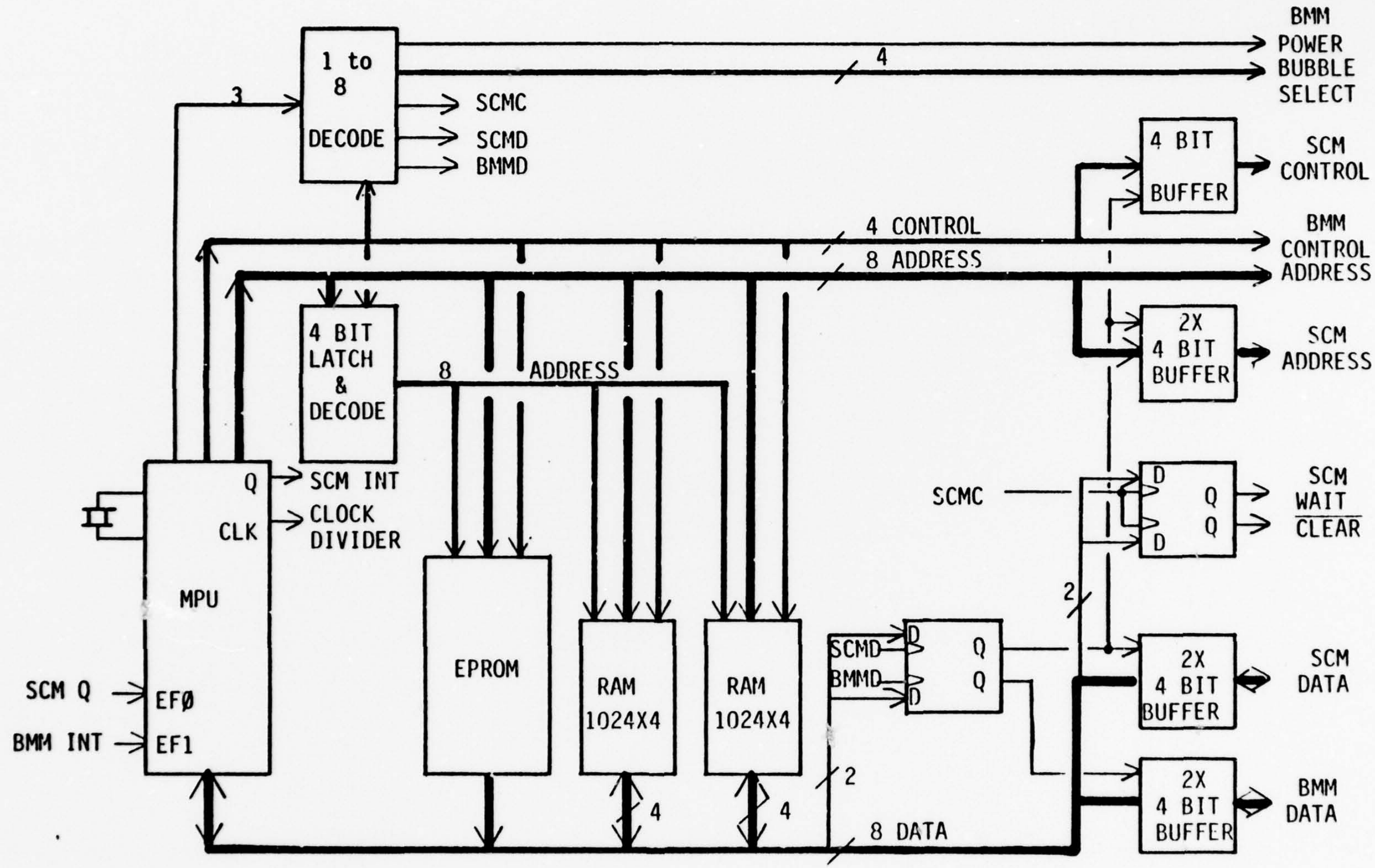


Figure 28. DMM CMOS Implementation

Table IV. CMOS Data Manager Module Maximum Power Consumption

ELEMENT/TECHNOLOGY	PART NUMBER	CURRENT @5V	CURRENT @12V	MISSION POWER (4hr) watt-hours 5V	MISSION POWER (4hr) watt-hours 12V
MPU/CMOS	CDP1802D	0.0005	0.001	0.010	0.048
EPROM/NMOS	2758	0.105	-	2.010	-
RAM/NMOS	L2114	0.140	-	2.800	-
LATCH-DECODE/CMOS	CDP1859D	0.0128	-	0.256	-
BUFFER(DATA)/NMOS	8T26	0.360	-	6.120	-
BUFFER(ADDRESS)/CMOS	CDP1856D	0.0128	-	0.256	-
DECODER/CMOS	CDP1823D	0.0128	-	0.256	-
D FLIP-FLOP/CMOS	4013	0.002	-	0.010	-
TOTAL MISSION POWER				11.706	0.048

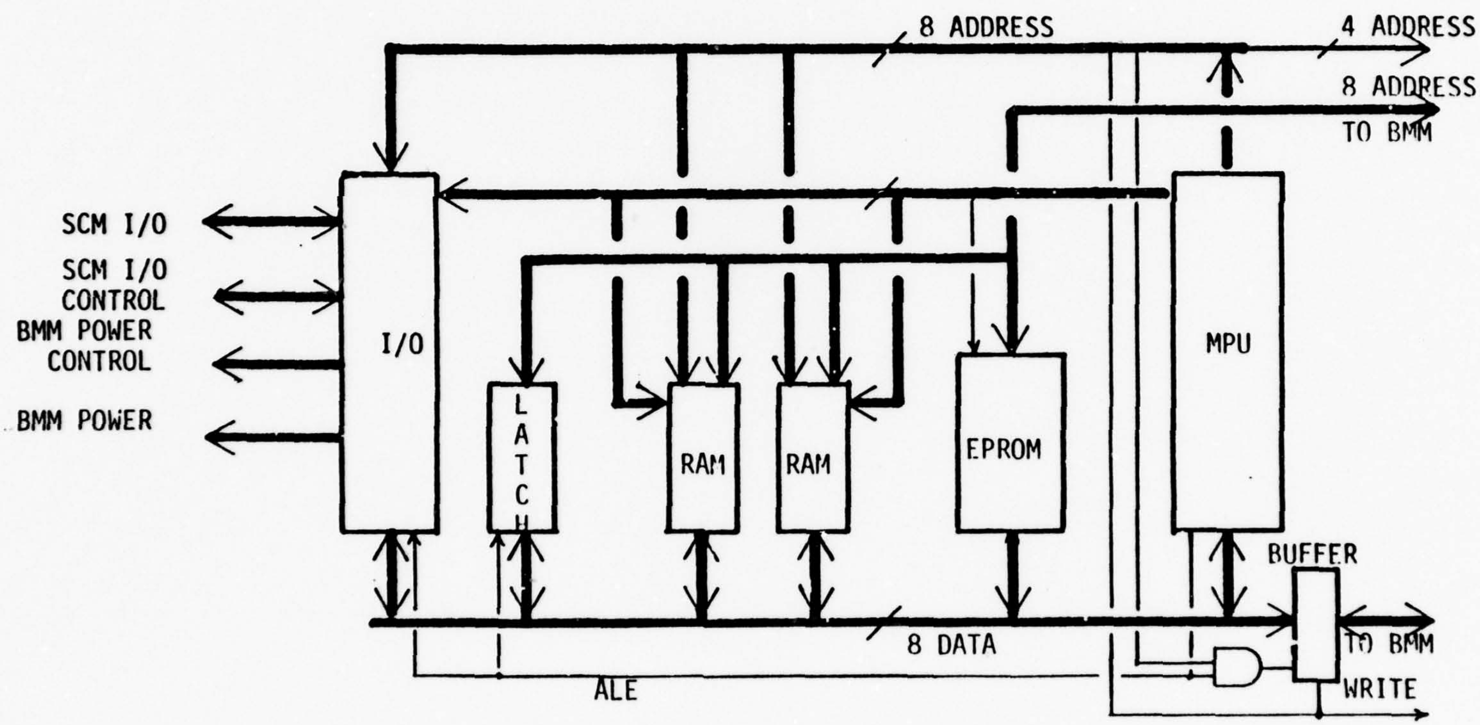


Figure 29. DMM NMOS Implementation

Table V. NMOS Data Manager Module Maximum Power Consumption

ELEMENT/TECHNOLOGY	PART NUMBER	CURRENT @5V amps	CURRENT @12V amps	MISSION POWER (4hr) watt-hours 5V	MISSION POWER (4hr) watt-hours 12V
MPU/NMOS	8085B	0.1800	-	3.600	-
EPROM/NMOS	2716	0.1100	-	2.200	-
RAM/NMOS	L2114	0.1400	-	2.800	-
I/O/NMOS	8255	0.1700	-	3.400	-
LATCH/NMOS	8212	0.0200	-	0.400	-
BUFFER/NMOS	8216	0.0200	-	0.400	-
AND/CMOS	CD4082	0.0001	-	0.002	-
TOTAL MISSION POWER				12.802	NONE

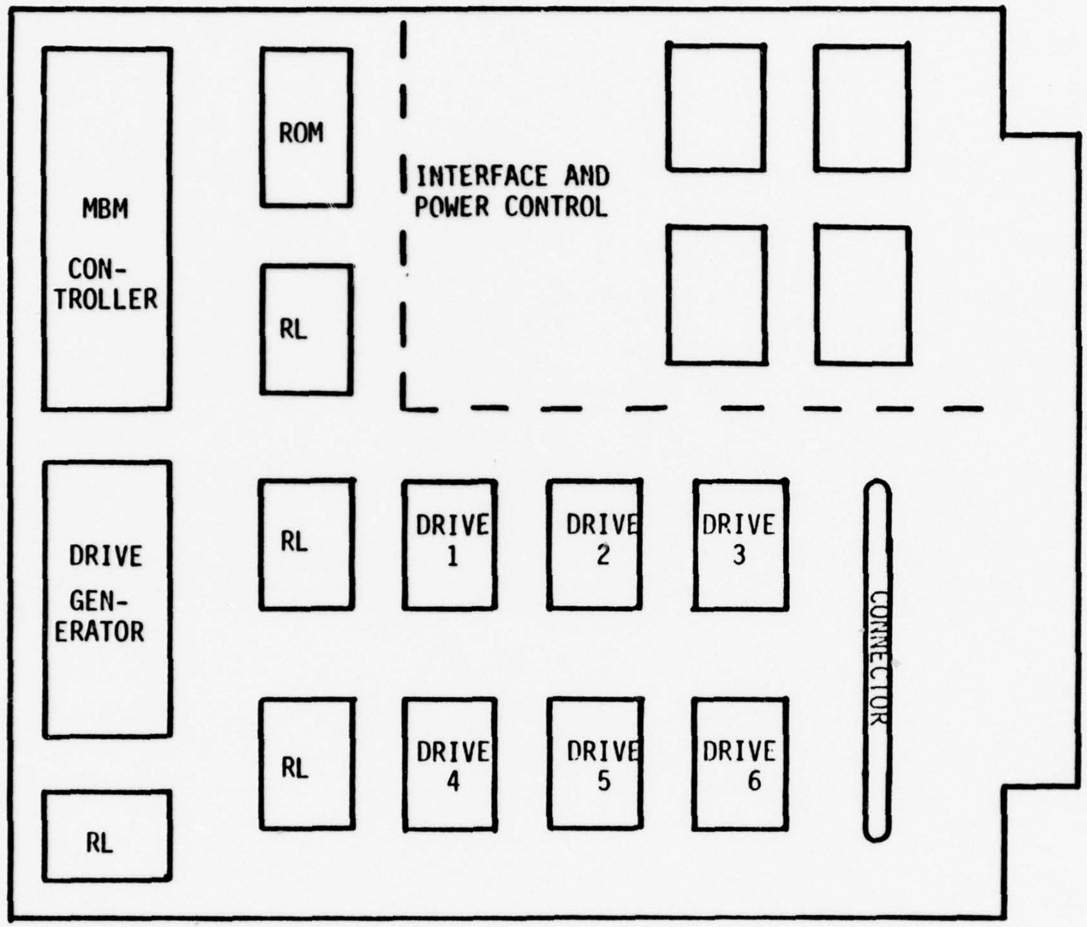


Figure 30. Bubble Memory Module Controller Level Layout

SA- DETECTOR SENSE AMPLIFIER
MBM- MAGNETIC BUBBLE MEMORY
CDX- X FIELD COIL DRIVER
CDY- Y FIELD COIL DRIVER
TN- RC TERMINATION FOR SA
DX- X FIELD DIODE NETWORK
DY- Y FIELD DIODE NETWORK

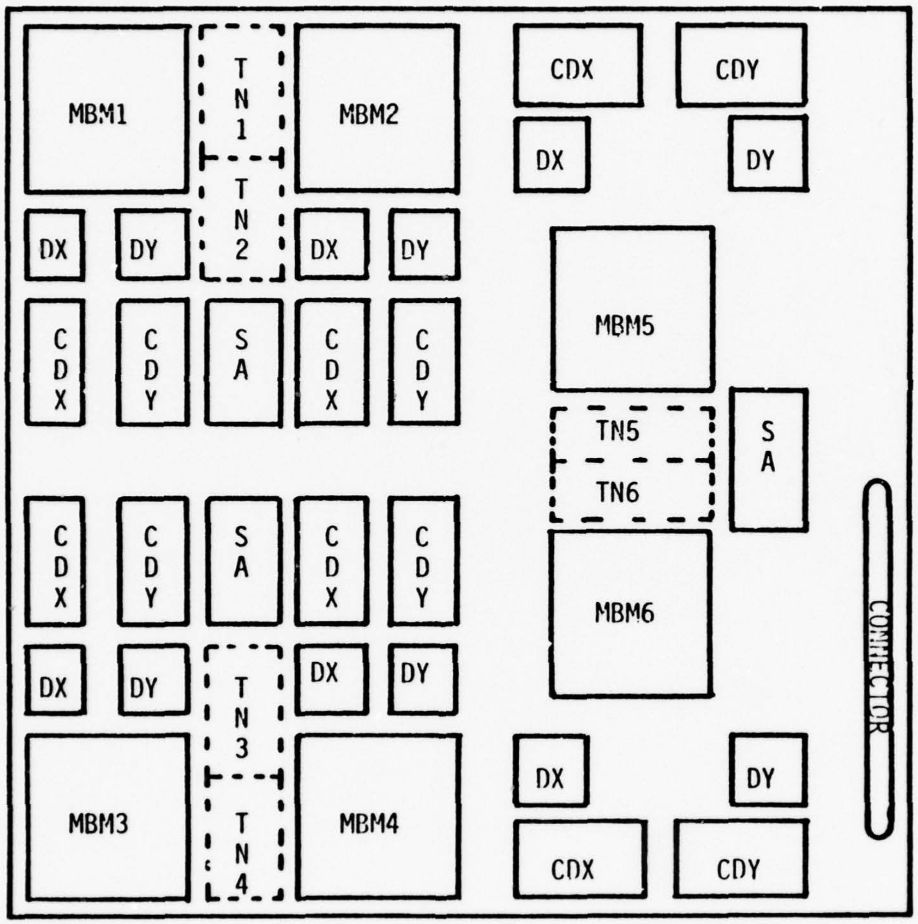


Figure 31. Bubble Memory Module Memory Level Layout

bit memory from Texas Instruments. The bubble memory power requirement is estimated, based on 92k bit memory requirements, at 12 watt hours for the 12 volt source and 5 watt hours for the 5 volt source. These requirements support peak load requirements plus a start-up reserve. These power estimates support up to six megabits of memory storage.

Design Considerations

In arriving at a final IFPDAS III design for implementation, several factors must be considered. These factors include speed of operation, size of components and power consumption. These considerations are:

- In order to convert and filter parameter data at the minimum sampling rate, the SCM MPU must be able tc perform operations while the conversions take place.

- If power consumption rates are more critical than speed of execution, CMOS circuits are required.

- If power consumption is not critical or speed of execution is important, NMOS circuits are the best choice.

- The power source requirements to support both the SCM and DMM digital and analog circuits are not significantly impacted by adding the one amp-minute requirement necessary to support a 6 megabit BMM.

- The major power consumer in the IFPDAS III is the digital system which operates continuously.

- The low power density of rechargable nickel cadimum batteries makes them unsuitable for use in the IFPDAS III package size. To power IFPDAS III, a separate container 5 X 9 X 3 inches is required to contain the 30 D size nickel cadimum cells which replace the lithium cell power supply.

- The power module size allows for only two voltage sources. The analog amplifiers must be single power source types or SCM space must be provided for the necessary power converters.

The manufacturer of digital circuits in large and very large scale integration introduce several new products each month. Even as this design is finalized and documented, four new introductions in the area of memories, counters and buffers provide for optimizations previously thought not possible. It is suggested that any use of the example design provided be optimized by using the most recent circuits available at the time of final fabrication.

IFPDAS III Design Specifications

Actual implementation of the IFPDAS III concept is possible with a variety of circuit elements available from comercial sources. The design used depends upon the technology type and vendor selected. The digital portions of IFPDAS III can be implemented with either NMOS or CMOS technologies and the actual signal interconnects and hardware required depend upon the technology and vendor selected. The operating system software concepts are the same for all technologies but actual implementation is dependant upon the details of the hardware used. The successful construction of an IFPDAS III system is possible using any suitable technology and hardware components if minimum specifications are followed. The specifications which define IFPDAS III are:

- Only two power supply voltages are feasible to implement. Space limitations make it difficult to provide more than two voltages at the required power levels without impacting space required for other circuit elements.

- The limited space devoted to power sources prohibit the use of rechargable batteries. The minimum power density for the IFPDAS III power module is six watt-hours per cubic inch.

- The analog signal amplifiers should be constructed using CMOS amplifiers requiring only a single power source.

- Only NMOS technology microprocessors have sufficient custom support elements such as, EPROMs, 1024x8 bit RAMs with three state output, and multiple latched bidirectional I/O ports in a single package to permit implementation of the digital system without awkward and large interface elements. When these memory, buffer, and I/O elements become available in CMOS technology, then the use of CMOS circuits is restricted only by the ability to produce the required system throughput.

- The microprocessors used must have an eight bit data word size and have more than ten address lines. The clock generation circuits must be provided by the processor itself, and the single fetch, non conditional instruction execution time must be less than ten microseconds. The microprocessor should require no external support circuits such as bus controllers, bus drivers, and clock drivers.

- The analog-to-digital converter should be a successive approximation type, have 16 analog channels with an input multiplexer, and eight bit latched three-state data lines. It is desirable that the converter be monolithic, CMOS, and complete conversions in 100 microseconds or less. A sample and hold circuit is not required but is desirable.

- The Random Access Memory minimum requirements are 48 words for the Signal Conditioner Module and 768 words for the Data Manager Module.

- The operating system software should be less than 1,024 words each for the Signal Conditioner and Data Manager modules. Larger operating systems are allowed if the minimum sampling rate is not affected.

- The operating systems are contained in single UV erasable Programmable Read Only Memories, EPROMS, for both the Signal Conditioner and Data Manager Modules.

- The Bubble Memory Module must provide for six memory elements. The bubble memory elements selected must provide for a system upgrade to six megabits without a bubble memory module hardware redesign. Provisions must be made to accomplish an orderly power shutdown between data storage routines to conserve battery power.

- All analog signal conditioners must provide parameter signals which range from 0-5 volts unless the input specifications of the analog-to-digital converter permit.

- The Signal Conditioner digital system must select, convert, filter, and save at least eight analog parameters in a 50 millisecond period.

- The Data Manager must be capable of operating on all data saved by the signal conditioner with enough reserve time to save the data in the Bubble Memory Module. The maximum average data storage rate allowed in a 6 megabit memory configuration is 48 words per second.

- The IFPDAS III system must be contained in a box. The box must be constructed to provide support for the modules, provisions for heat disipation, and shielding from outside electromagnetic interference. Removable end caps provide for module replacement. One end cap is connected to the signal conditioner module to provide the supporting structure for external connecting plugs.

- The signal interconnects between modules are provided by a backplane and 44 pin connectors which are a part of the power module.

- The microprocessor chosen for the design must be supported by a total development system. The system shall include Higher Order Language compilers; assembly language compilers; software drivers, monitors and debuggers; hardware incircuit emulators for the processor; Read Only Memory programmers; and a hardware development support capability. This development tool is to be used also as the IFPDAS III Ground Support Equipment and thus provide for maintenance data servicing, and data analysis.

APPENDIX B

Development Tool Design

Appendix B

DEVELOPMENT TOOL DESIGN

The tools used in the development of IFPDAS III design concepts consist of an INTEL SBC 80/20 single board computed, prototype system an Analog Devices DAS 1128 analog-to-digital converter system, a Texas Instruments 92 kilobit magnetic bubble memory system, and custom designed interface and power circuits. The basic system description is provided by the work of Jolda and Wanzek (Ref 4) and only changes or modifications are presented here.

General

The SBC 80/20 and magnetic bubble memory systems are mounted on a single chasis which also contains the power generation, regulation and distribution system. Figure 32 shows the power system. The main power switch provides the proper power sequencing for both the SBC 80/20 and the bubble memory system. The SBC 80/20 requires that the +5 volt source be the last one turned on and the first turned off. The magnetic bubble memory system requires that all power sources be stable before the +12 volt source is applied. The power switch insures proper power sequencing when rotated in either direction. The SBC 80/20 system operates with or without the magnetic bubble memory system but the memory won't operate without the SBC 80/20.

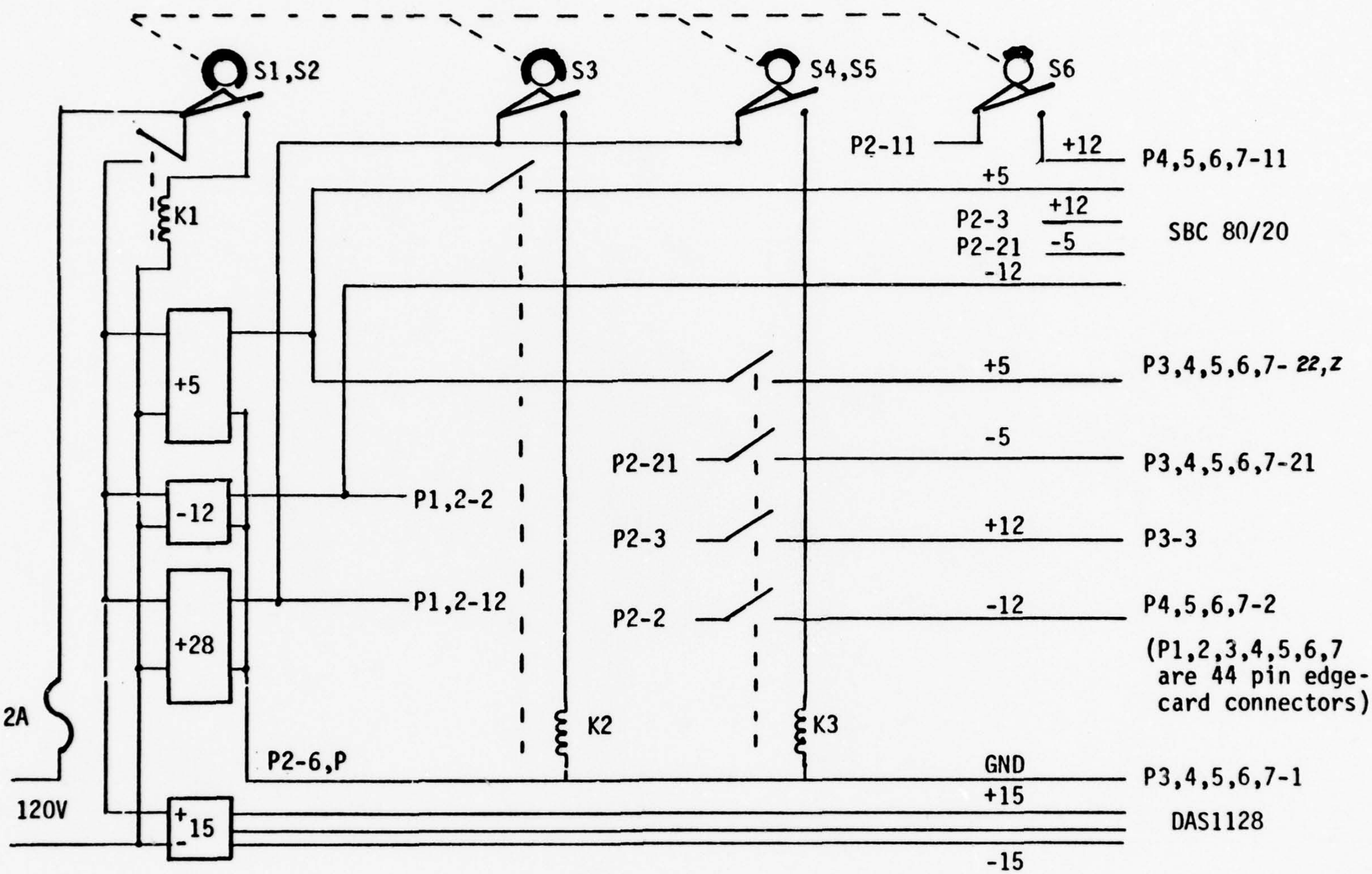
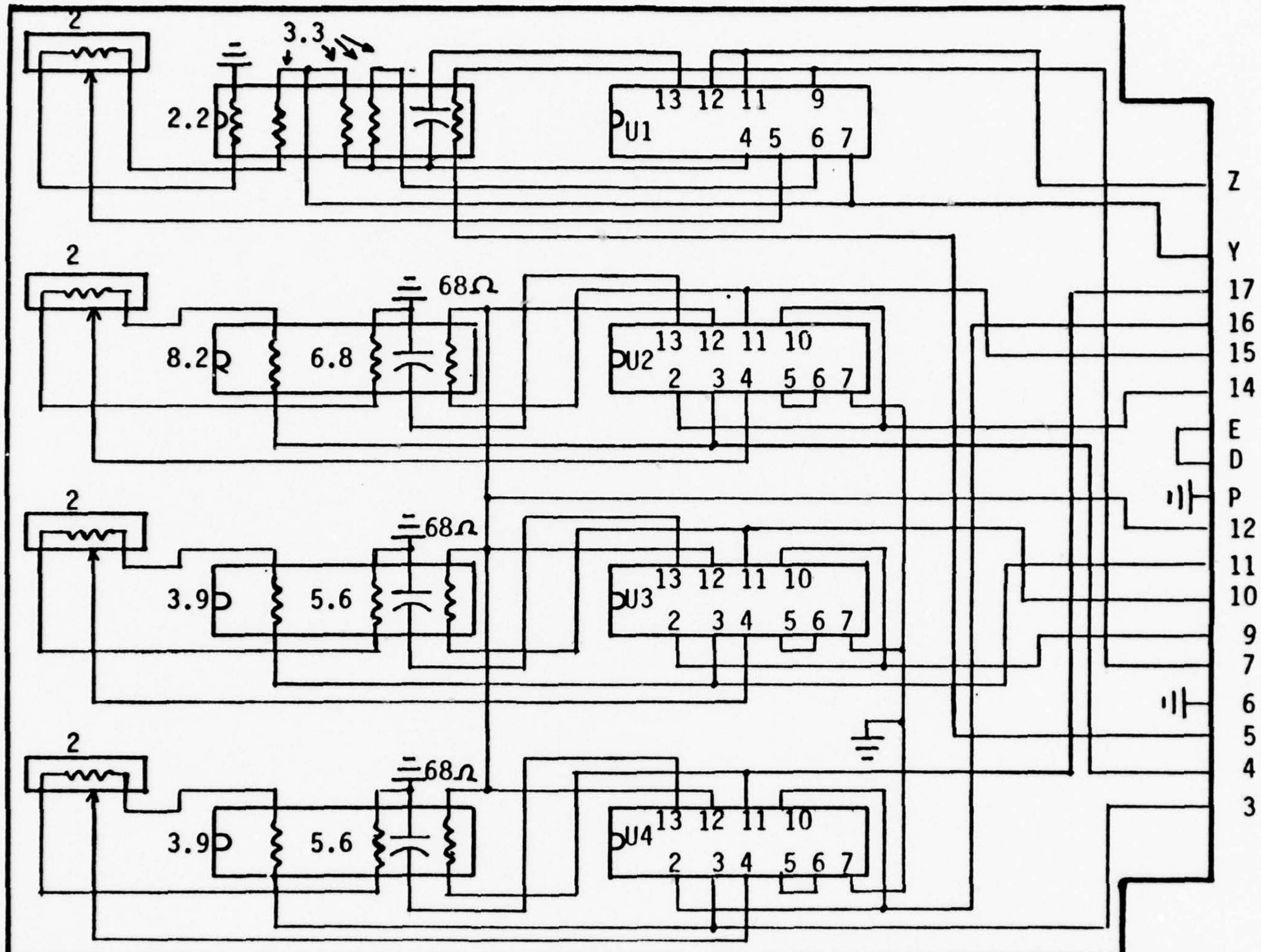


Figure 32. Development System Power System
(sheet 1 of 3)



all capacitors 0.1mfd; U1,2,3,4- 723 Regulator ; all resistors x1000 unless specified

Figure 32. Development System Power System
(sheet 2 of 3)

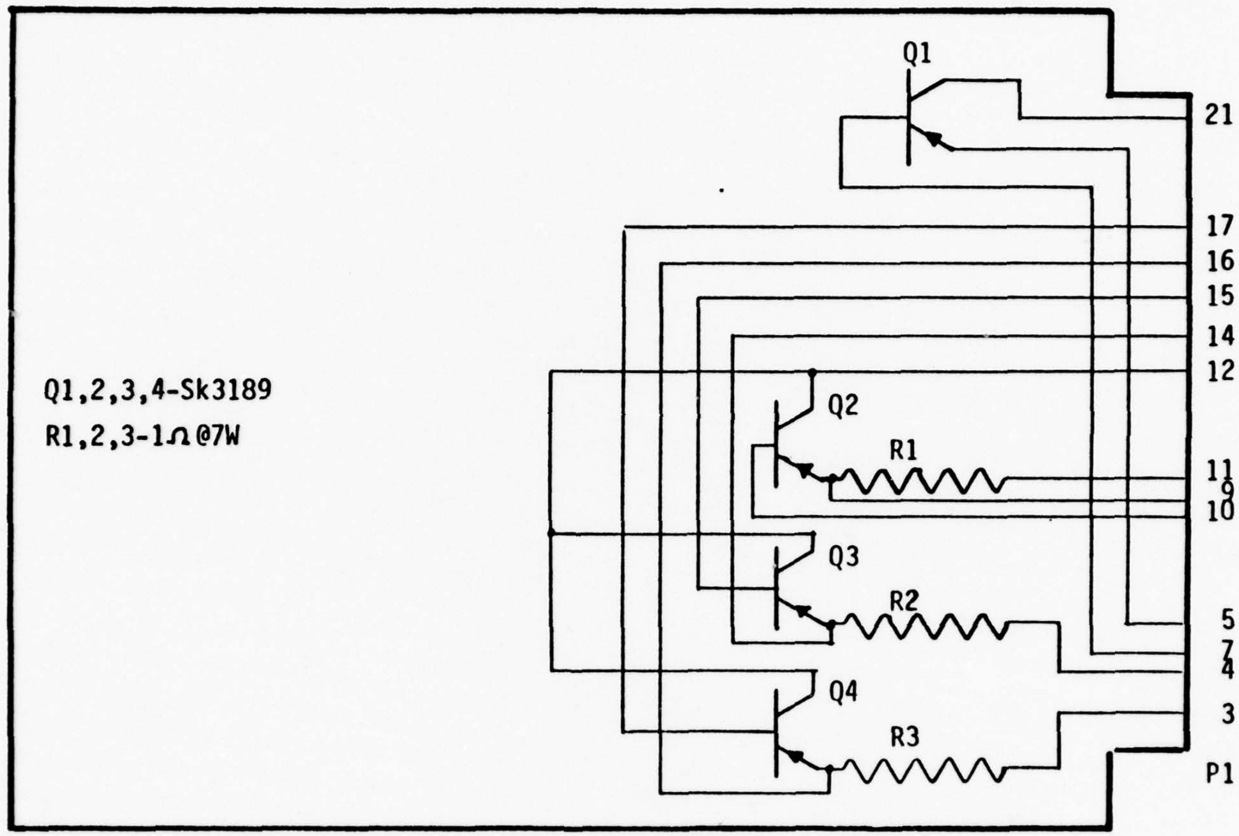


Figure 32. Development System Power System
(sheet 3 of 3)

Power

Eight independent voltage sources are required to operate the entire development system. The 5 volt source is provided by self contained 5 volt, 6 amp regulated supply. The -12 volt supply is provided by a self contained 12 volt, 1 amp regulated supply. The -5 volt supply is provided by an external regulator operating from the -12 volt supply. A 24.5 volt, 1.5 amp self contained regulated supply provides the source for three external regulators which supply +17 volts and the two independent +12 volt sources. The $\pm$15 volt power for the DAS 1128 and analog circuits is provided by a single $\pm$15 volt, 100 milliamp power supply module. The four external voltage regulators are contained on two circuit cards which are located at the top of a 44 pin card rack.

The SBC 80/20 and interface card fit into an SBC 604 Multibus card cage fastened to the common chasis. The 44 pin bus card cage is used for the power regulators and magnetic bubble memory system. The power regulators occupy the top two card slots. The bubble memory controller occupies one card slot and four card slots are provided for memory modules. The bottom memory module position does not have BDEN, pin E, connected.

SBC 80/20

The parallel I/O ports of the SBC 80/20 are rewired as shown in Table VI to provide data interface to the DAS 1128 and heart rate counter. The least significant four data bits from the DAS 1128 are not used. The analog signal address mux is provided through the lower nibble of the data bus. This allows non-sequential selection of parameters for conversion. Using the latched I/O port allows the heart rate circuit or DAS 1128 to start a new conversion without waiting to be serviced after a conversion is complete. Counter Ø provides 2 millisecond timing pulses which are summed in counter 1. The counter Ø output also provides an interrupt signal indicating the end of a sampling loop. The actual passage of 2 millisecond periods is automatically accumulated as a decreasing value from FFFF (Hex) in counter 1. This value is read by the system as necessary. Six levels of interrupt are implemented and described in Table VII.

System Interface

The system inteface circuits are described by Figures 33 through 38. 'The address decoders and acknowledge circuits are shown in Figure 33. The use of the address bus to control system activation or data transfers is faster than passing control through an I/O port. The faster method is used whenever feasible.

The DAS 1128 interface is described in Figure 34. Routing Delay Out to Trigger automatically starts a conversion when a new MUX address is loaded. The EOC signal strobes the data into the I/O port and initiates a new conversion. The DAS 1128 data word is in 1's complement form and is again complemented by the I/O port buffer.

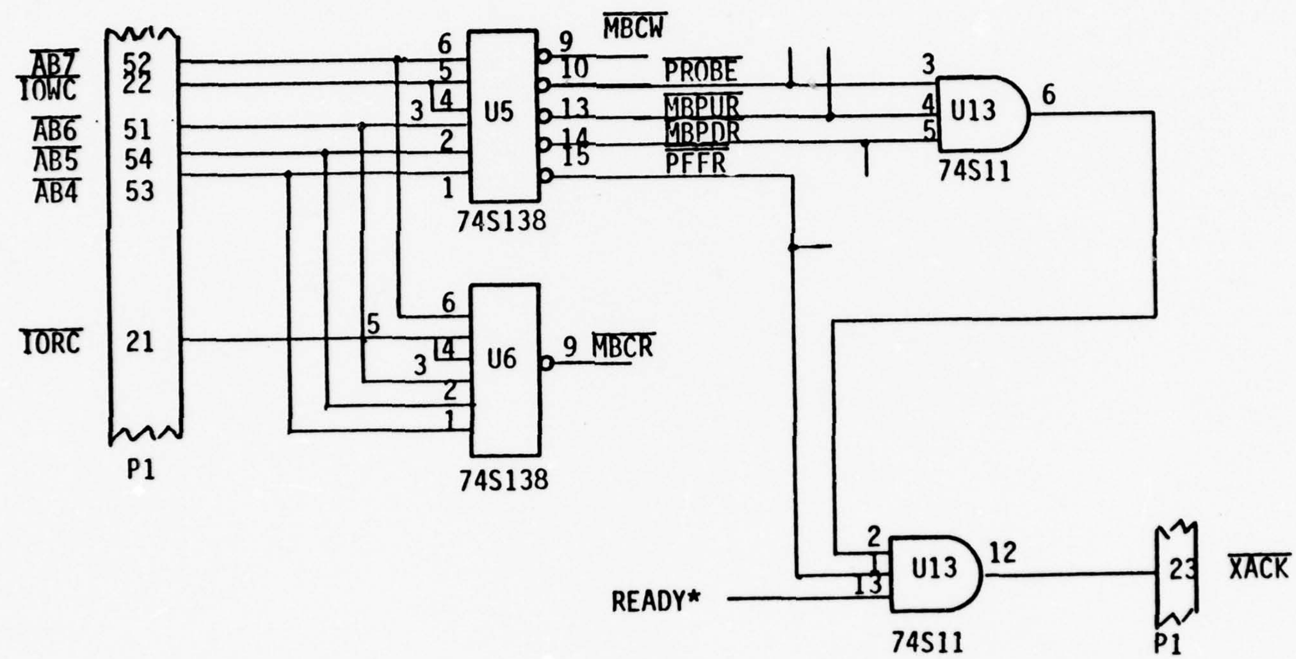


Figure 33. Development System Address Decode and Acknowledge

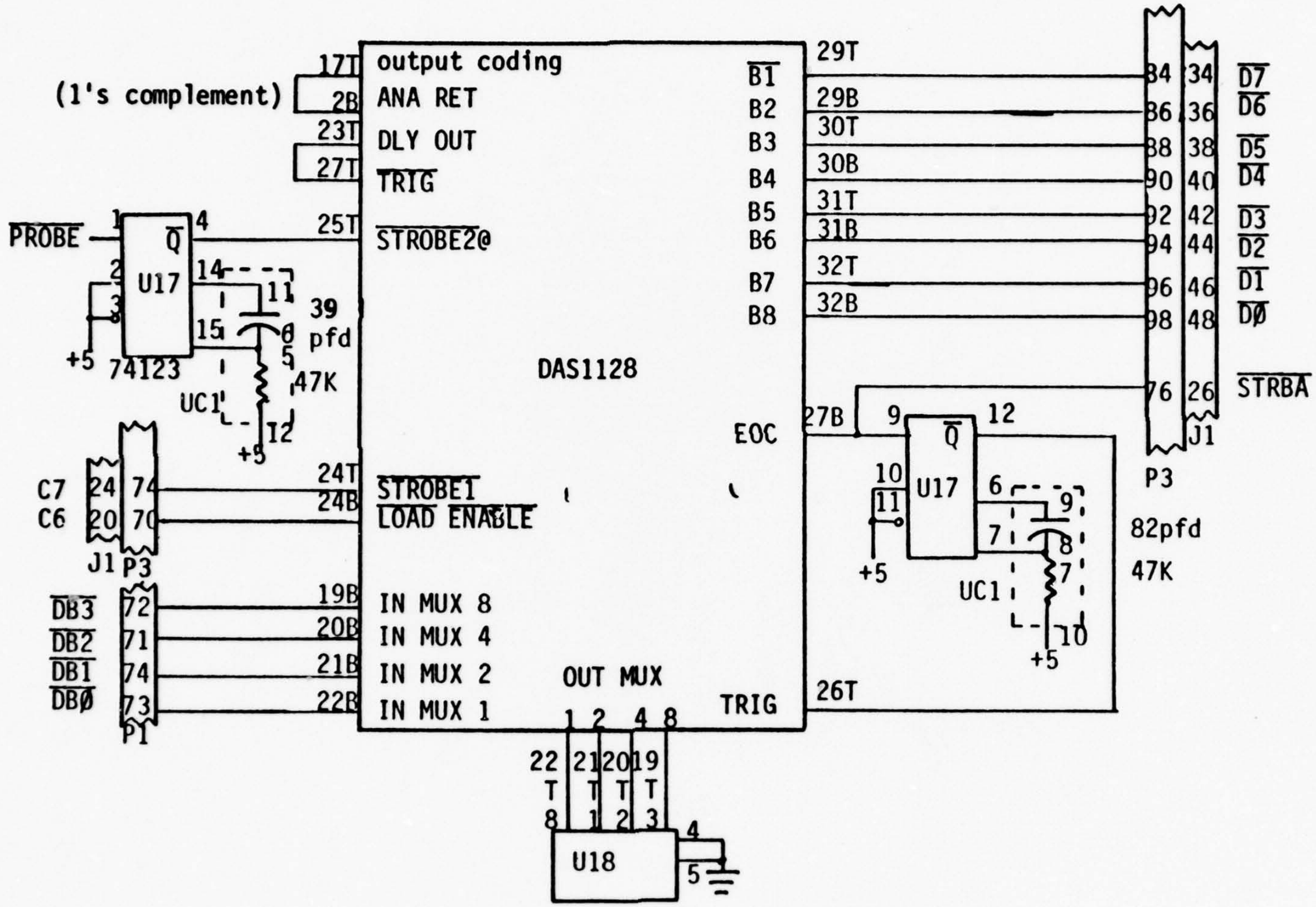


Figure 34. DAS 1128 Interface

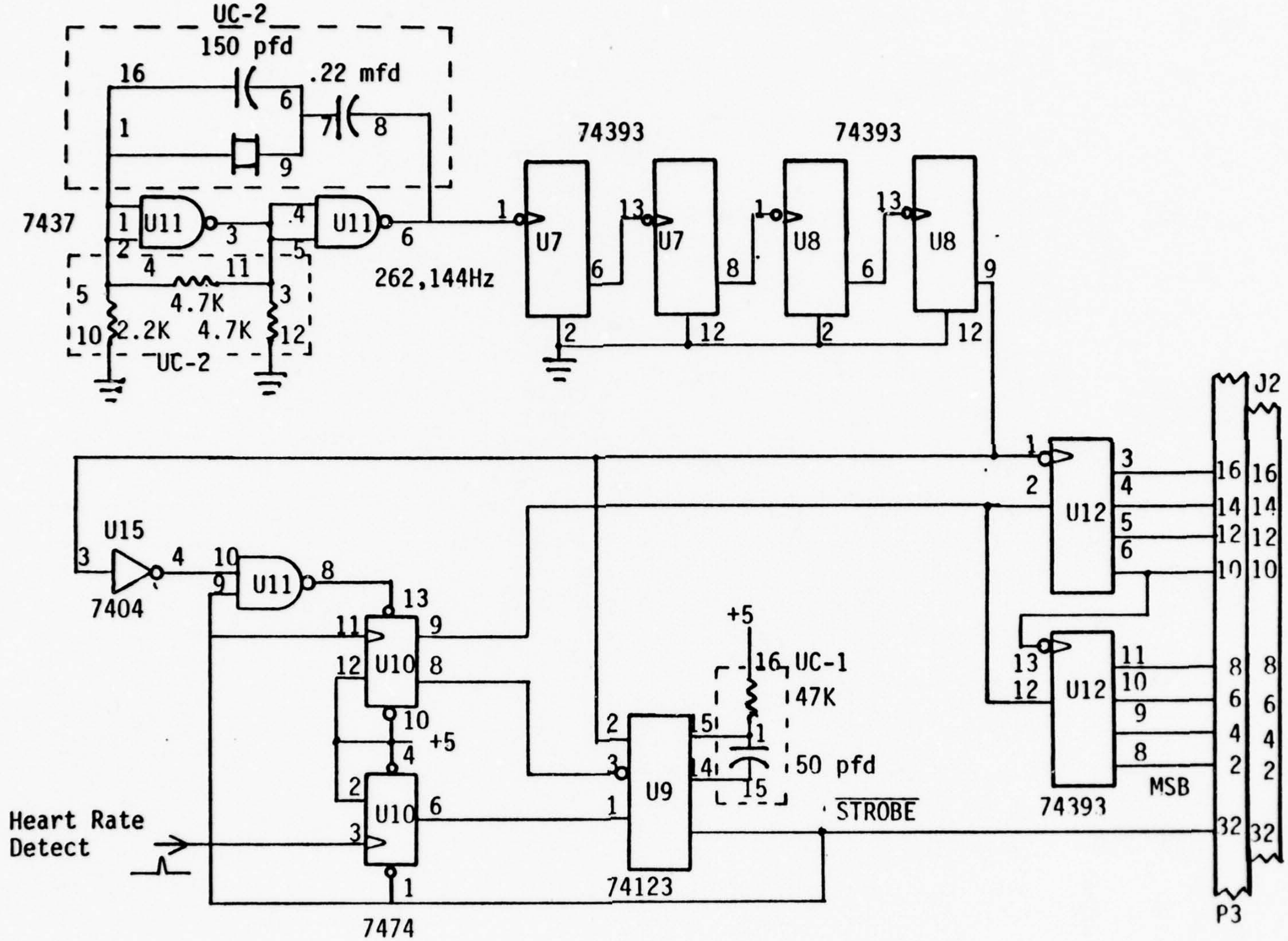


Figure 35. Heart Rate Counter

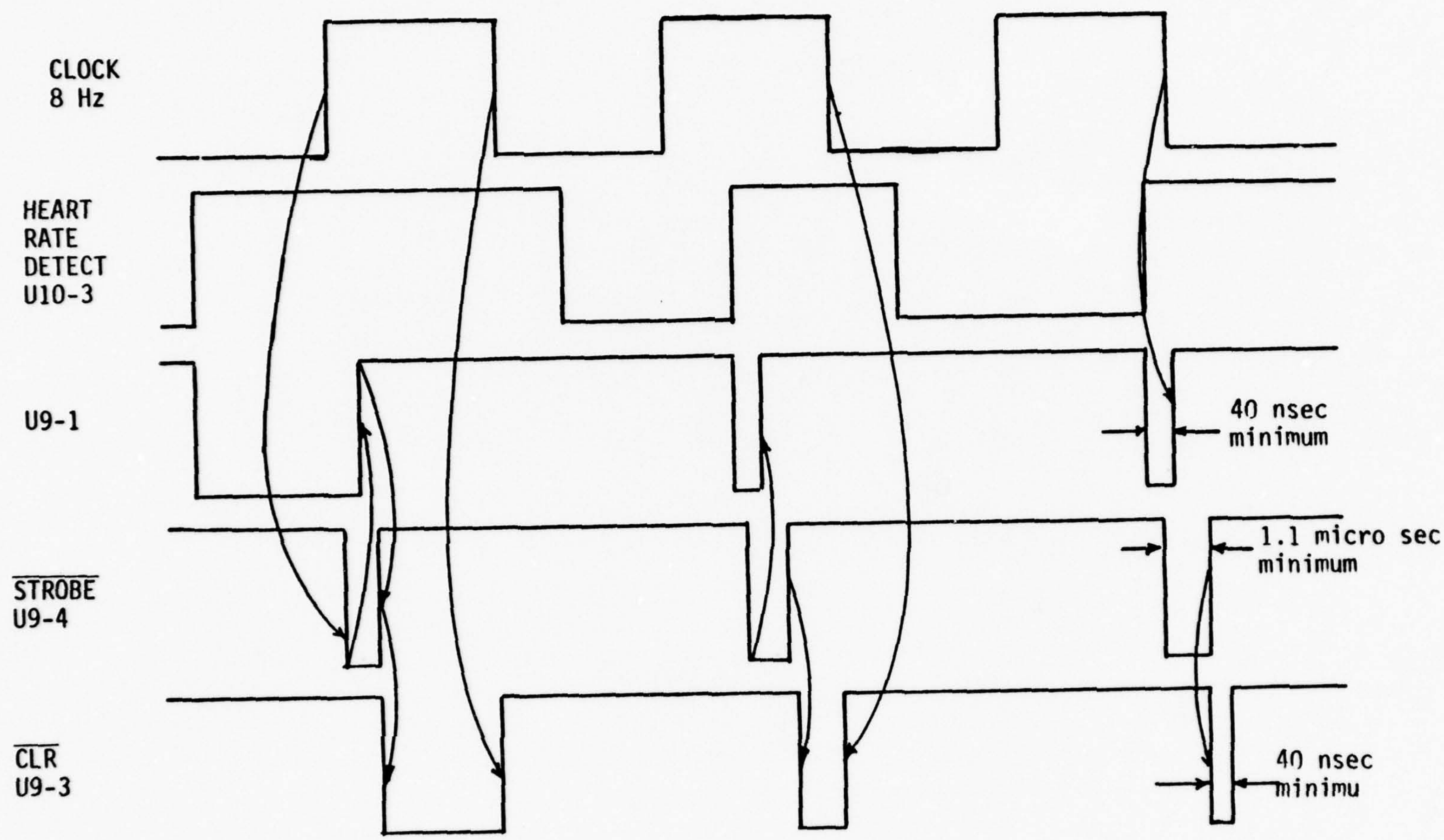


Figure 36. Heart Rate Counter $\overline{\text{CLR}}$/$\overline{\text{Strobe}}$ Timing

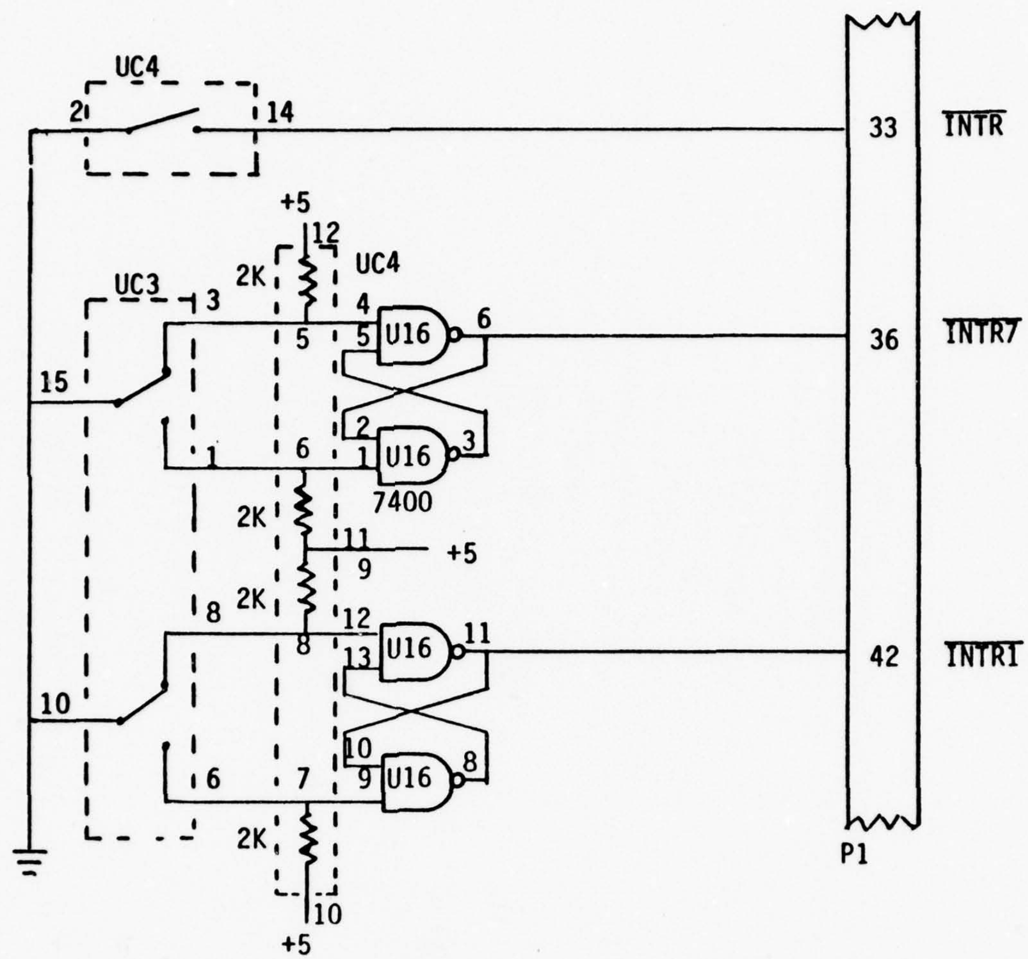


Figure 37. Interrupt Circuit

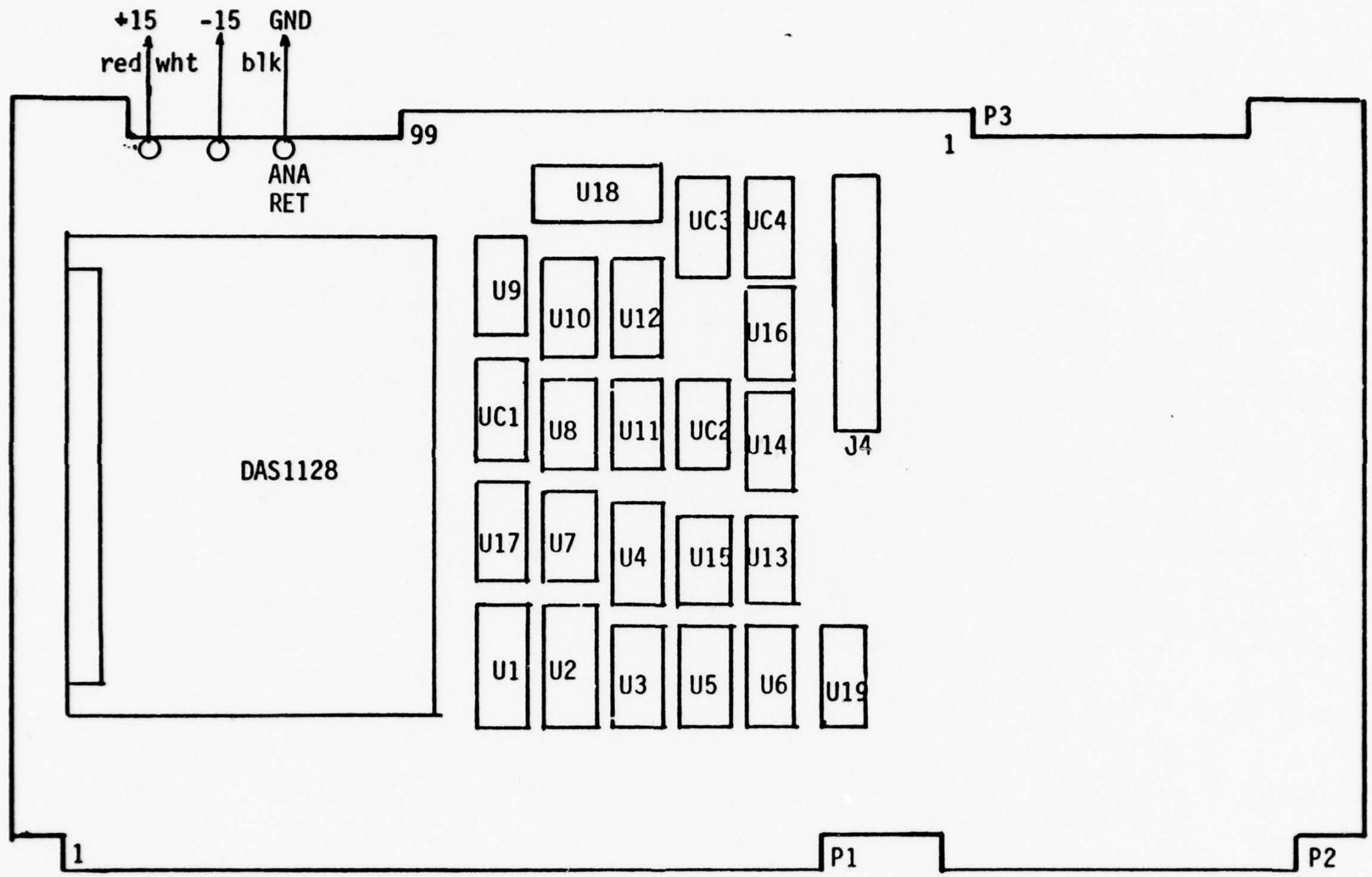


Figure 38. Interface Board Layout

The Heart rate circuit is described in Figure 35. The clock signal is generated by the crystal oscillator, U11, and reduced from 262,144 Hz to 8 Hz by the U7&U8 divider network. The heart rate count is accumulated in U12. Both U9 and U10 provide the signals necessary to stop the count, latch the data into the I/O port, clear U12, and start a new count. The heart rate counter control signal timing diagram is shown in Figure 36.

The external interrupt generation circuits are shown in Figure 37. Debounced switches are used when multiple interrupt signals are not desirable. The master reset line INTR is not debounced as this stops all operation and resets all systems to wait for initialization commands.

The magnetic bubble memory interface circuits are discussed in Appendix C. The interface board component layout is shown in Figure 38.

Development Tool Software

The development tool does not operate in the same manner as would IFPDAS III since only a single processor is available in the SBC 80/20. The software discussed in this section consist of only those elements of the total development tool operating system which implement the three new data compression techniques and magnetic bubble memory driver routines. The total operating system is designed to operate with the SBC 80/20 monitor installed to provide for user debugging.

The SCB 80/20 software is written to operate with a 16K RAM occupying the memory space CØØØ to FFFF (Hex). The operating system is moved from PROM address range Ø8ØØ to ØFFF (Hex) to CØØØ (Hex). All the data page areas are in the SBC 80/20 RAM while the other pointers; BSMSK, LSTP, and MBPCT are addressed in the 16K RAM. This approach is taken to provide a debug capability for the operating system. The operating system listing in Appendix D contains instructions for restructuring the operating system to operate without the 16K RAM.

Fixed Change. The fixed change flow chart is shown in Figure 39. This implementation receives the data and time words, computes the change, tests for significant change and stores a data byte if necessary. When the data page is full, it is transferred to the bubble memory queue.

Zone. The zone method flow chart is shown in Figure 40. This implementation receives the data and time words, computes a zone, checks for a change in the zone, and stores a data word if necessary. When the data page is full, it is transferred to the bubble memory queue.

Variable Change. The variable change method flow chart is shown in Figure 41. This implementation receives the data and time words, computes the change, tests for a significant change, and stores a data word if necessary. When the data page is full, it is transferred to the bubble memory queue.

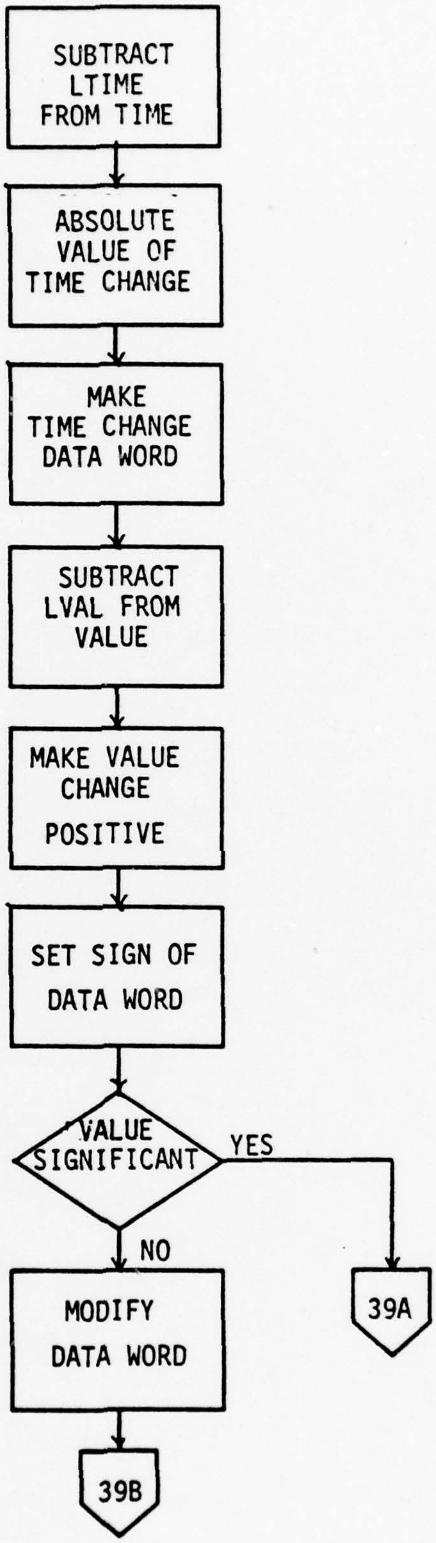


Figure 39. Fixed Change Data Flow Chart
(sheet 1 of 2)

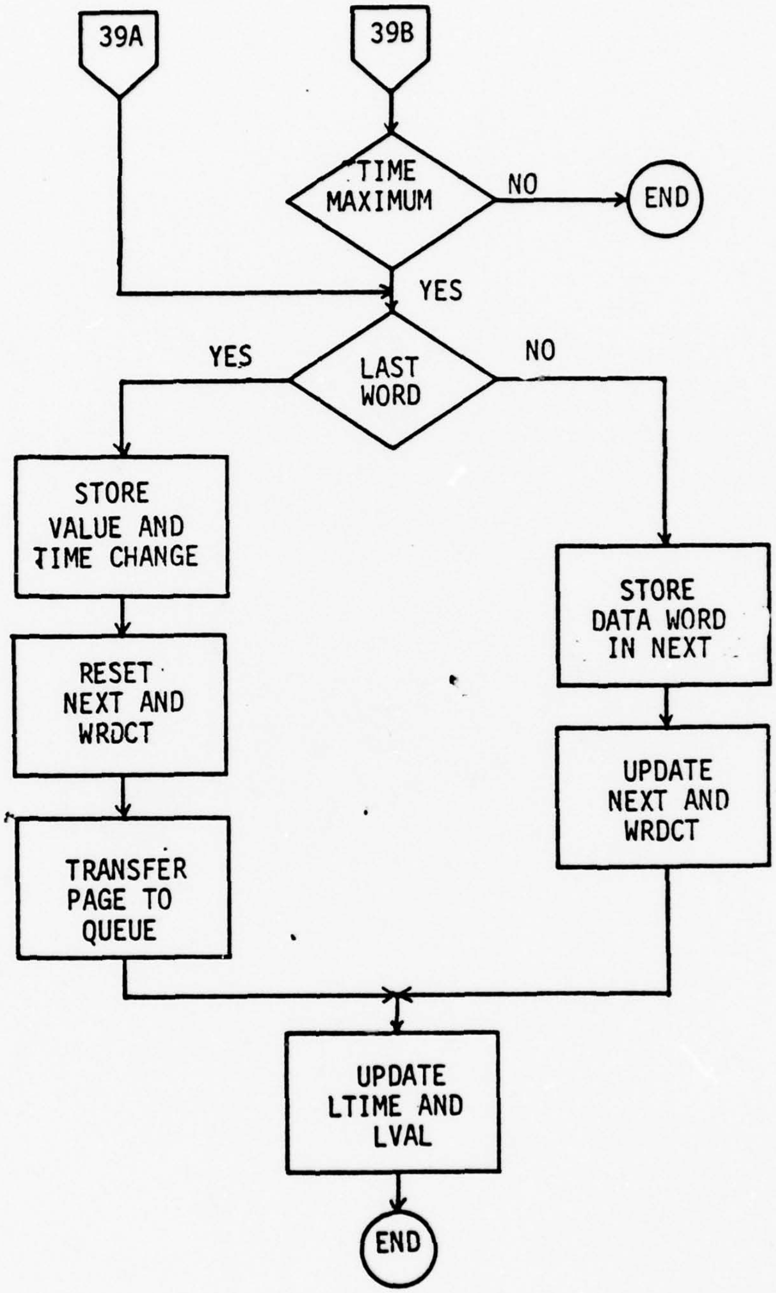


Figure 39. Fixed Change Data Flow Chart
(sheet 2 of 2)

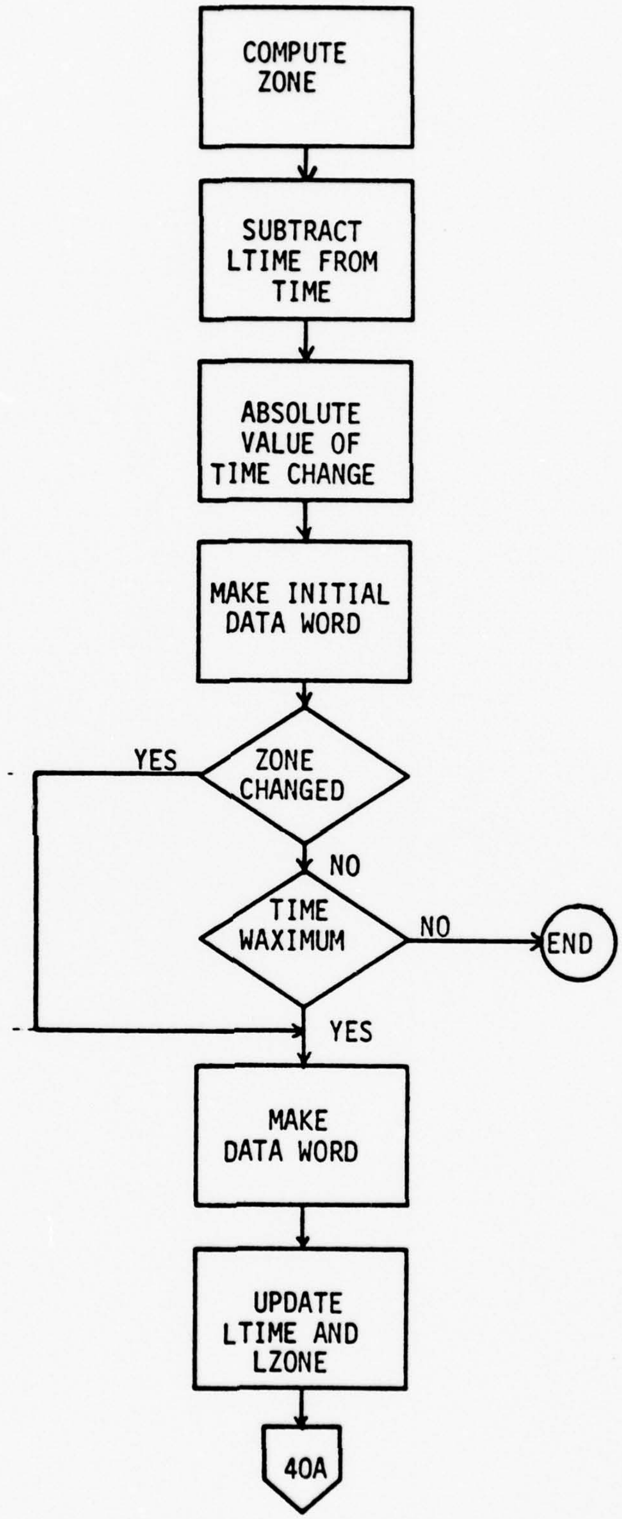


Figure 40. Zone Data Flow Chart
(sheet 1 of 2)

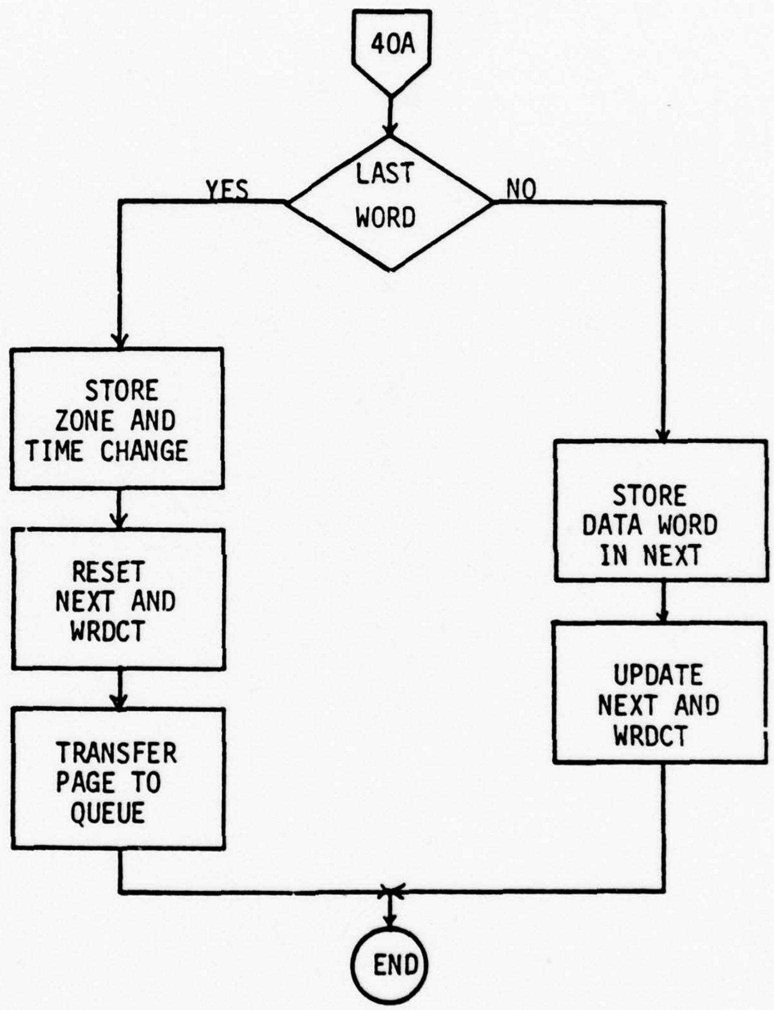


Figure 40. Zone Data Flow Chart
(sheet 2 of 2)

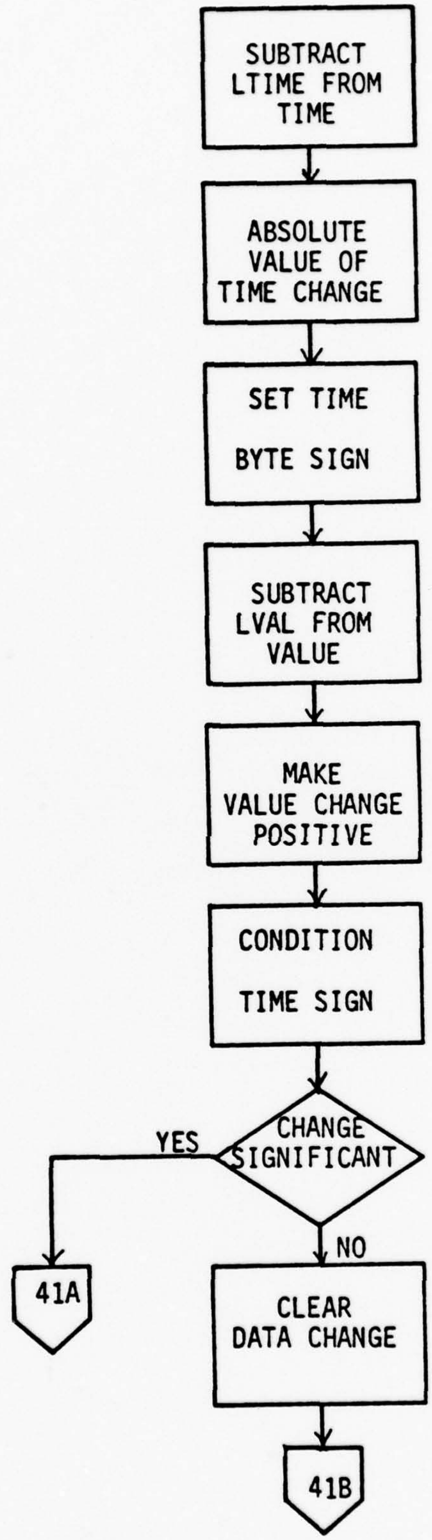


Figure 41. Variable Change Data Flow Chart
(sheet 1 of 2)

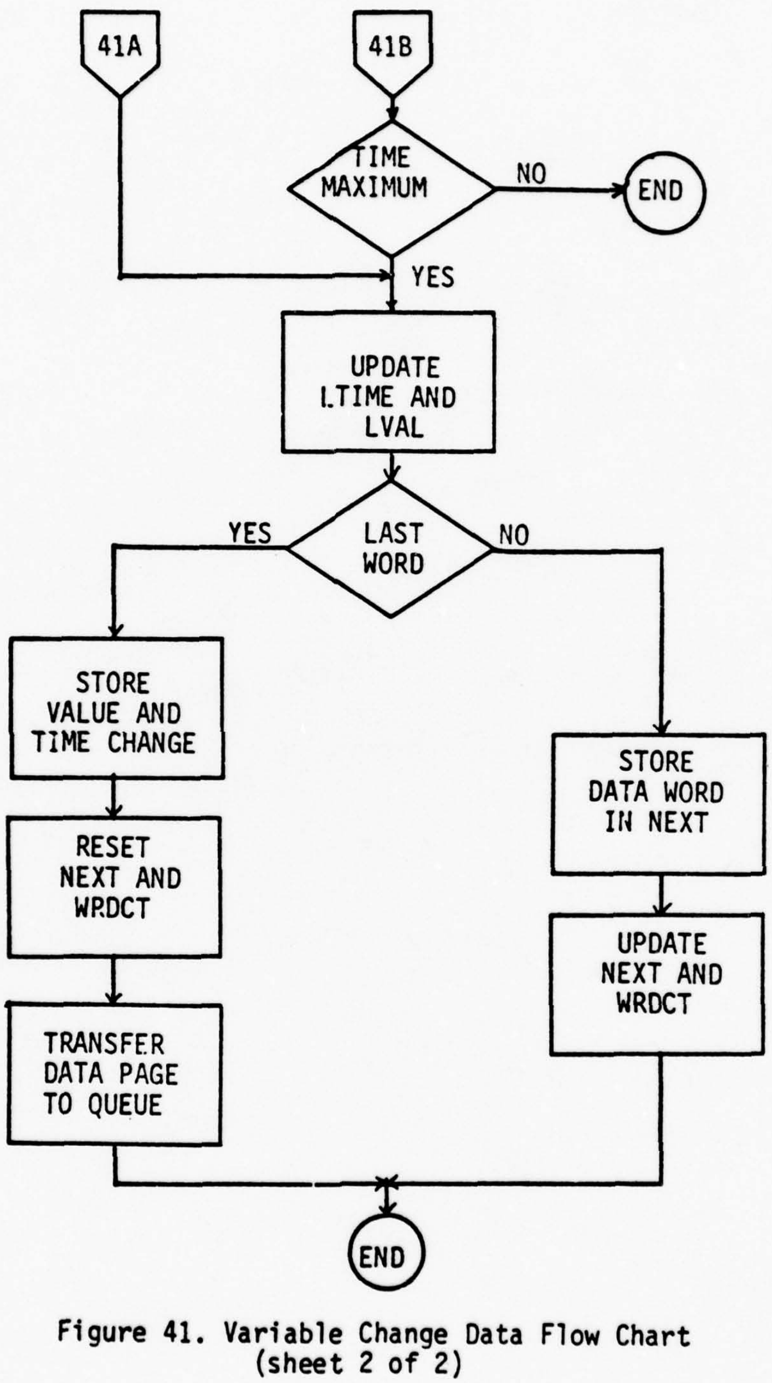


Figure 41. Variable Change Data Flow Chart
(sheet 2 of 2)

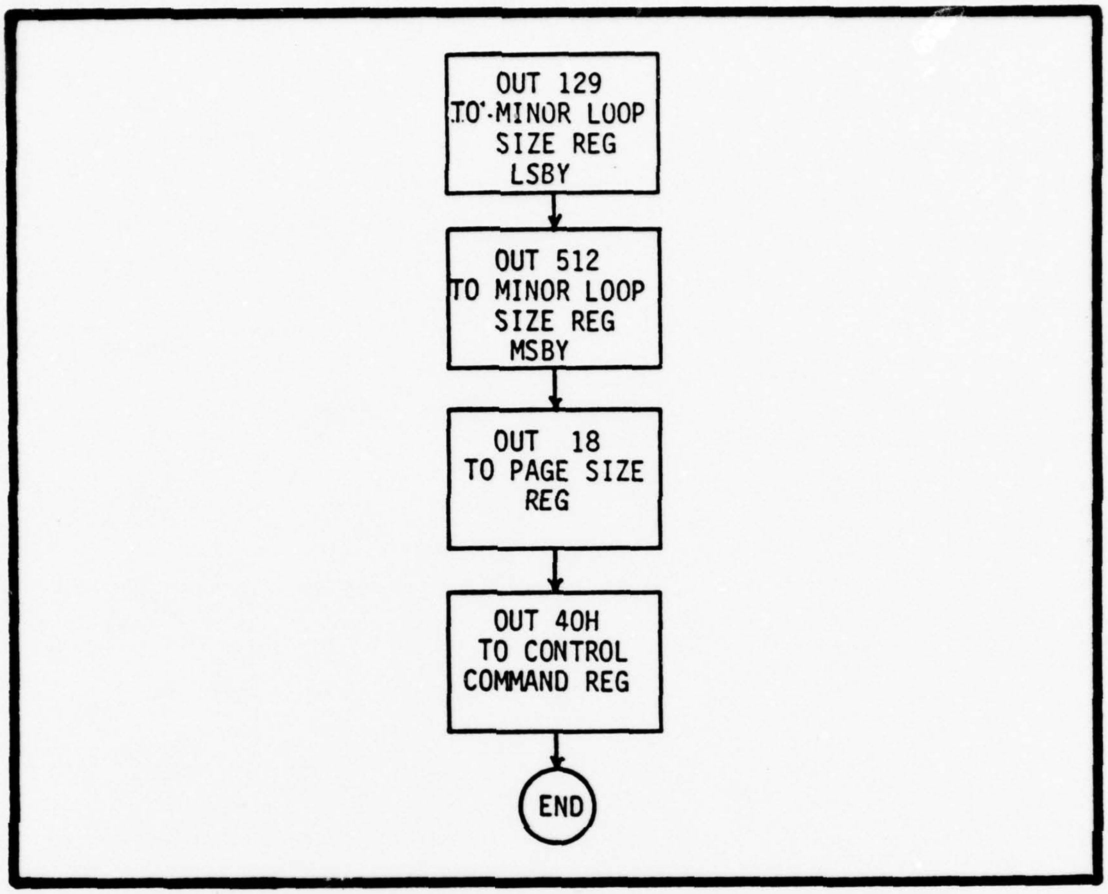


Figure 42. Magnetic Bubble Controller Initialize Flow Chart

Magnetic Bubble Initiatization. The initialization sequence for the magnetic bubble controller for an 8080 addressing the controller as an I/O port is shown in Figure 42.

The selection and initialization sequences for magnetic bubble memories which are being powered up from an unknown state is shown in Figure 43. The initialization command portion of this sequence is unnecessary if the previous shutdown occurred after the controller finished the command execution, orderly shutdown.

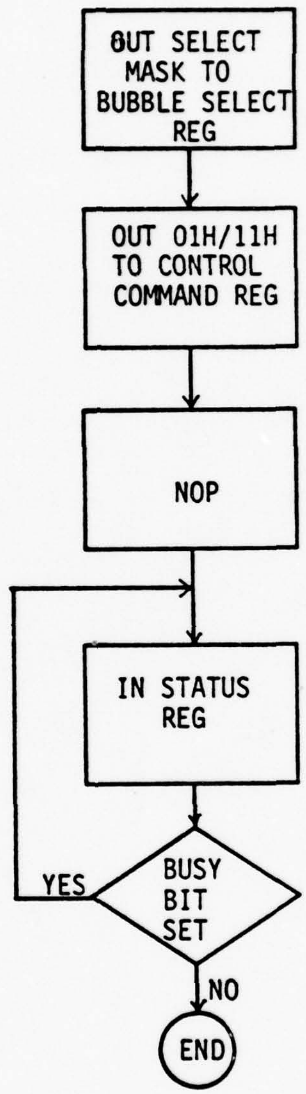


Figure 43. Magnetic Bubble Power-Up Initialize

Bubble Page Write. The sequence to save a data page in the bubble memory using a single page mode is shown in Figure 44. Figure 45 shows the same data storage routine using the multipage mode. It is assumed that the bubble module is selected and powered.

Bubble Page Read. The sequence to read a data page from the bubble memory using the single page mode is shown in Figure 46. Figure 47 shows the same data transfer in the multiple page mode. It is assumed that the bubble module is selected and powered.

Operating System

The prototype operating system for the development tool using a single magnetic bubble module is presented in Appendix D.

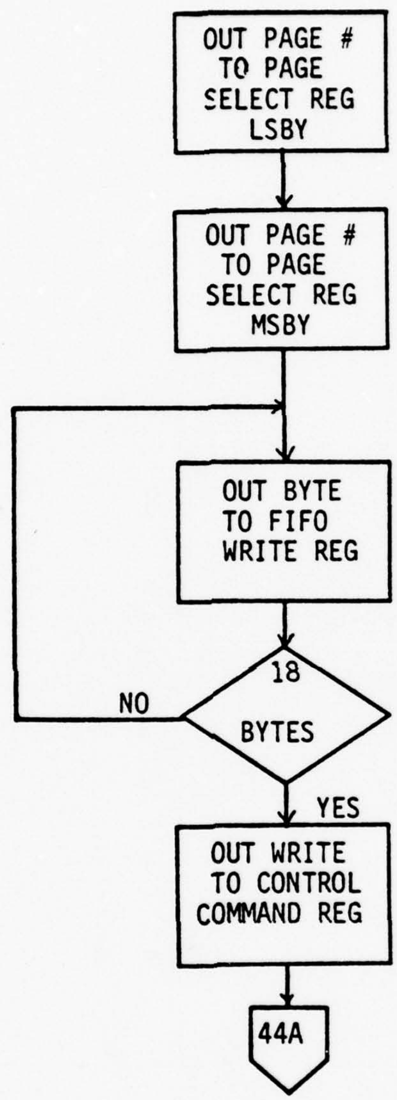


Figure 44. Single Page Write
(sheet 1 of 2)

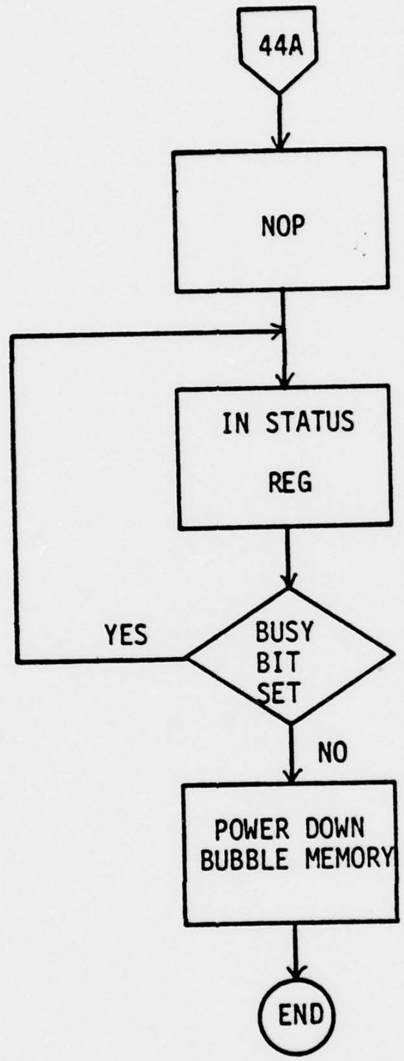


Figure 44. Single Page Write
(sheet 2 of 2)

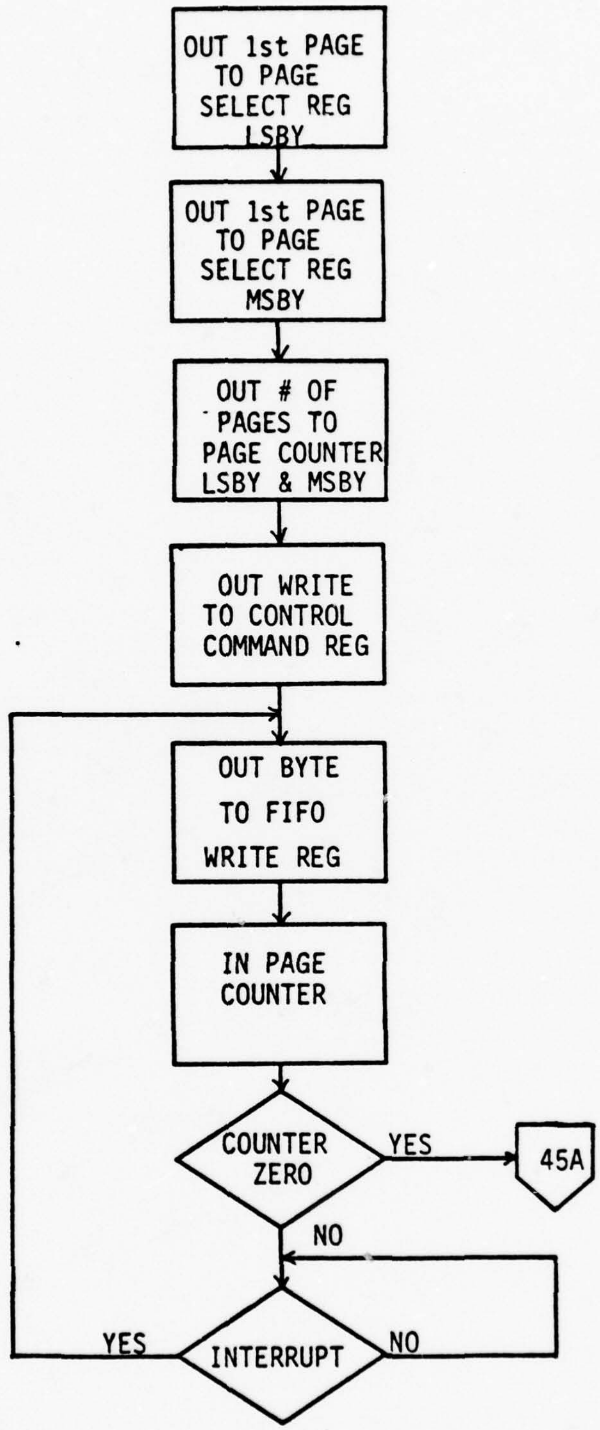


Figure 45. Multipage Write
(sheet 1 of 2)

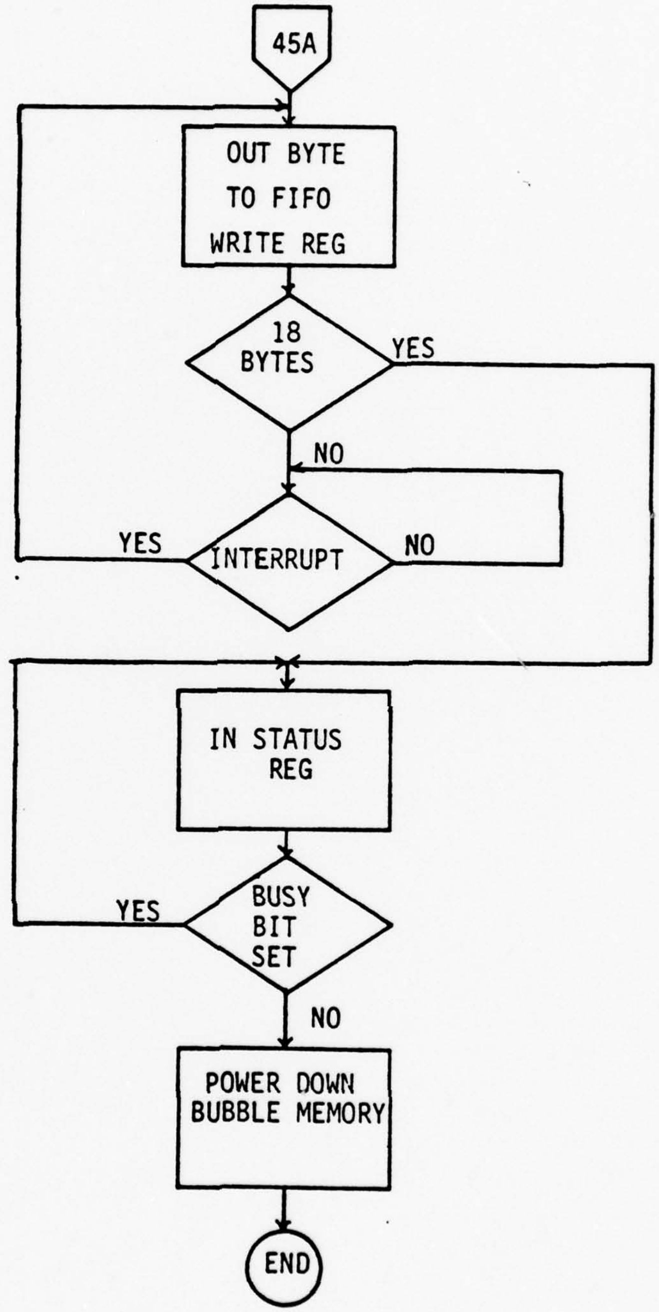


Figure 45. Multipage Write
(sheet 2 of 2)

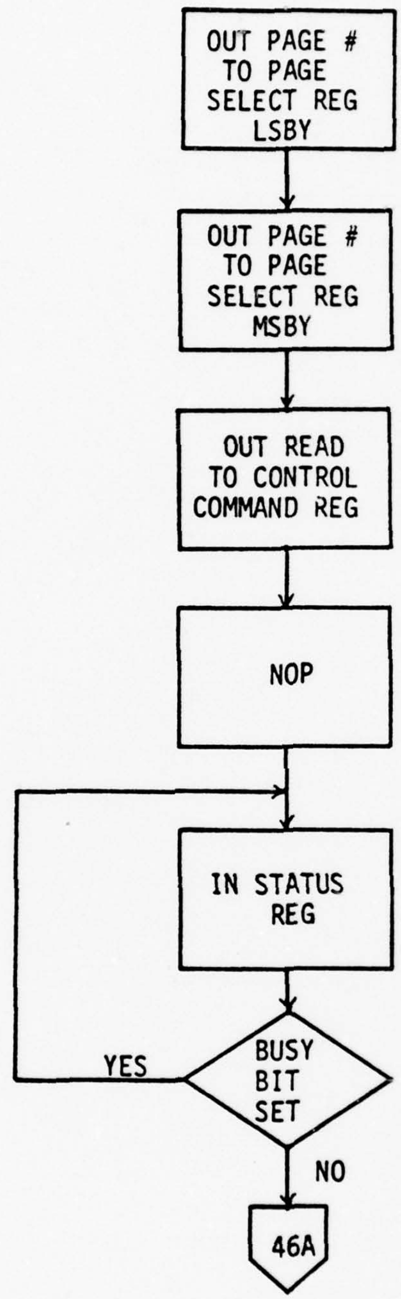


Figure 46. Single Page Read
(sheet 1 of 2)

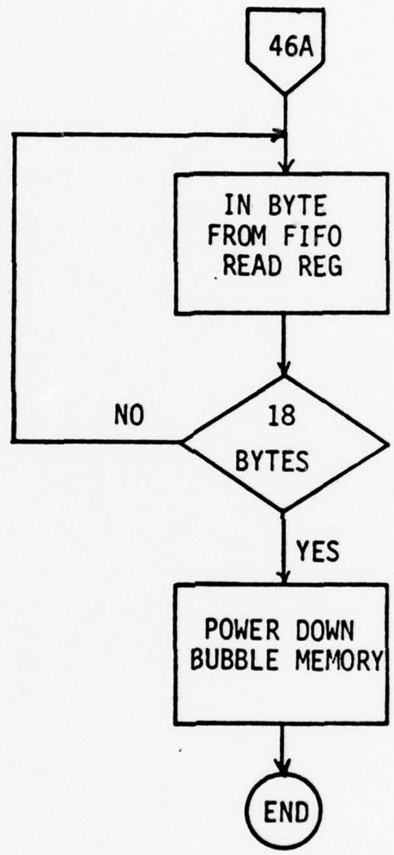


Figure 46. Single Page Read
(sheet 2 of 2)

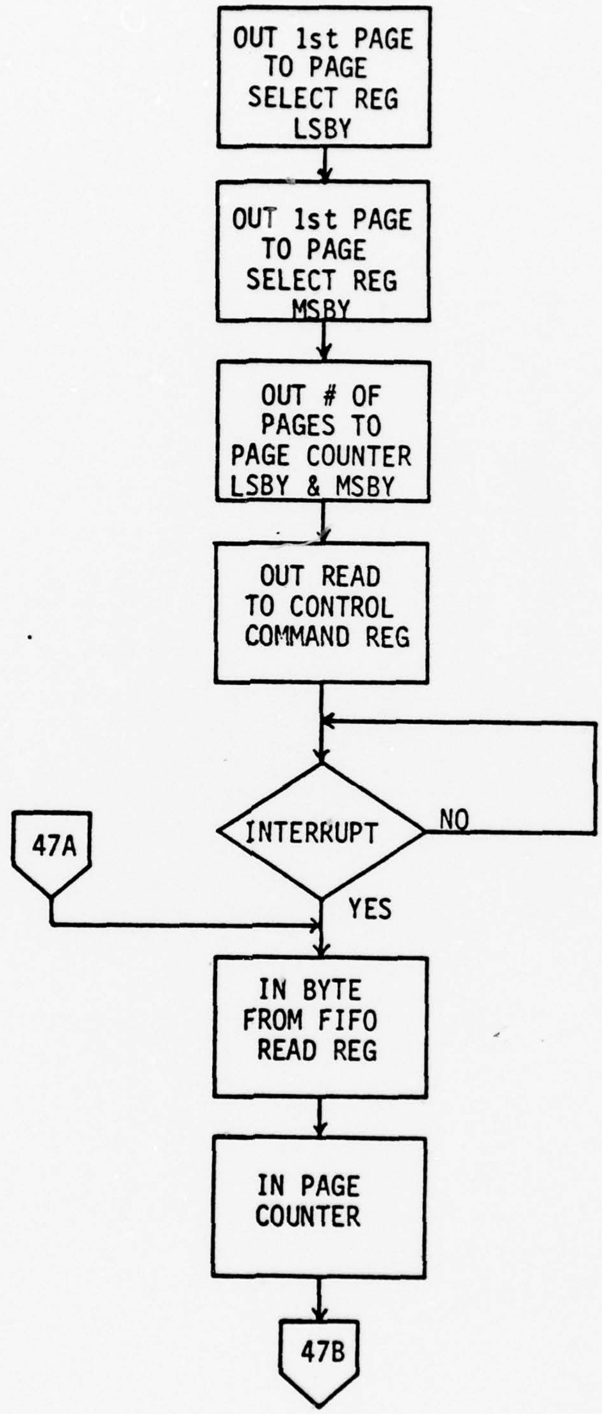


Figure 47. Multipage Read
(sheet 1 of 2)

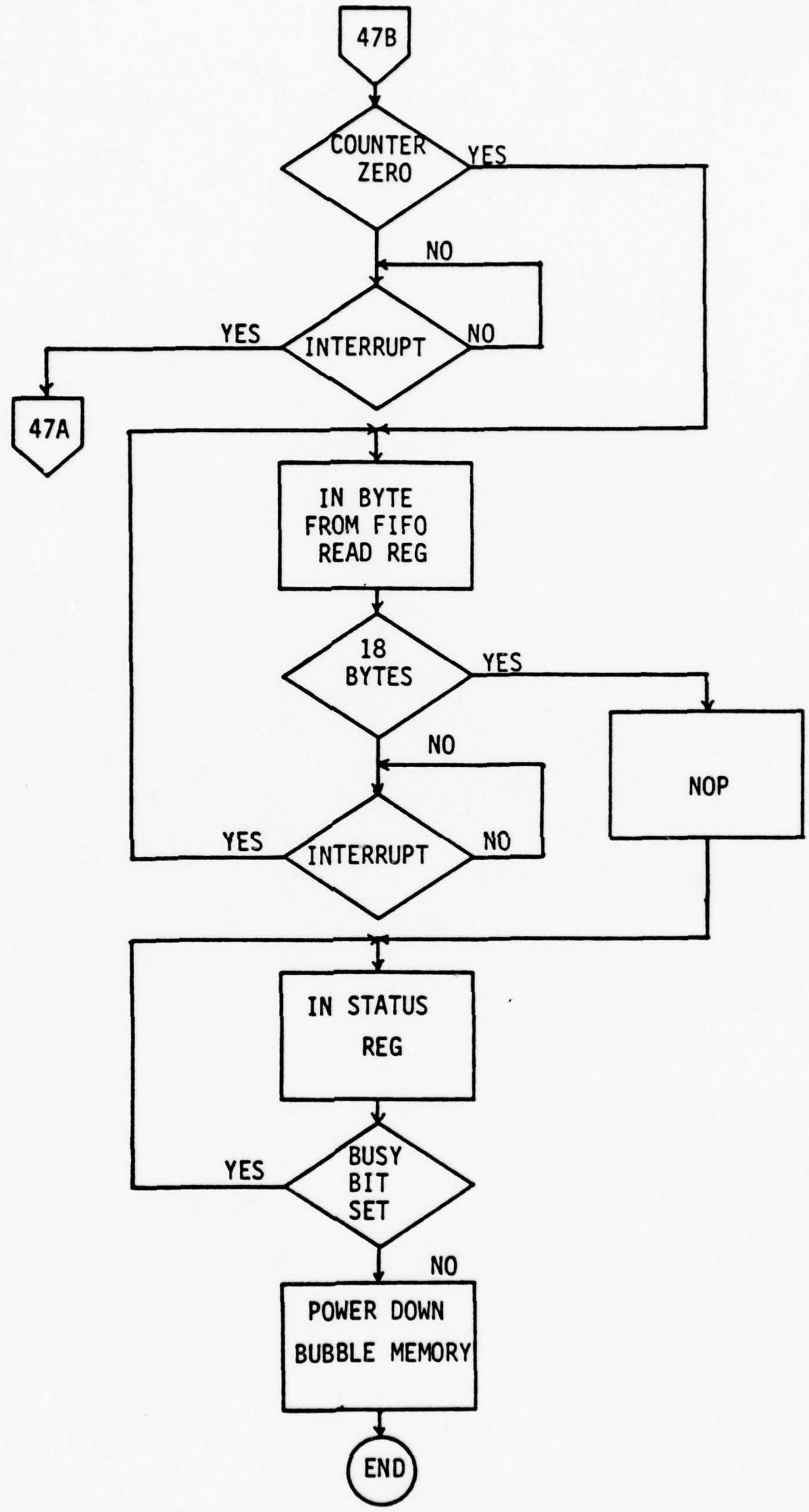


Figure 47. Multipage Read
(sheet 2 of 2)

APPENDIX C

Magnetic Bubble Memory System

Appendix C

MAGNETIC BUBBLE MEMORY SYSTEM

The magnetic bubble melory used is the BKA 0103 by Texas Instruments. This system consists of the BCA 0200 bubble controller module and one TIB 0103 bubble memory module. These systems are documented in the Texas Instruments literature (Refs. 11, 12, 13, 14, 15, 16, 17, 18, 19, and 20). The memory system is interfaced to the SBC 80/20 to appear as 15 I/0 ports from address 11 (Hex) to 1F (Hex).

The controller is enabled when the upper nibble of the address is 1 (hex). The interface board decoders, U5&U6, provide the proper select signal logically ANDed with a read or write command. The lower four bits of the address bus goes directly to the controller address pins. The controller data lines are buffered from the SBC 80/20 data bus by U1 and U2. The data buffers are enabled in response to a controller select signal and the data direction is dependent upon the state of the I/0 read or write signals. Figure 48 shows the signal interface between the SBC 80/20 interface card and the bubble controller. The memory module enable signals are supplied by U3 which is driven from the lower three bits of the SBC 80/20 data bus. The 3 MHz clock pulse provided to the bubble controller module through U19 synchronizes the controller ready signal to insure stable data.

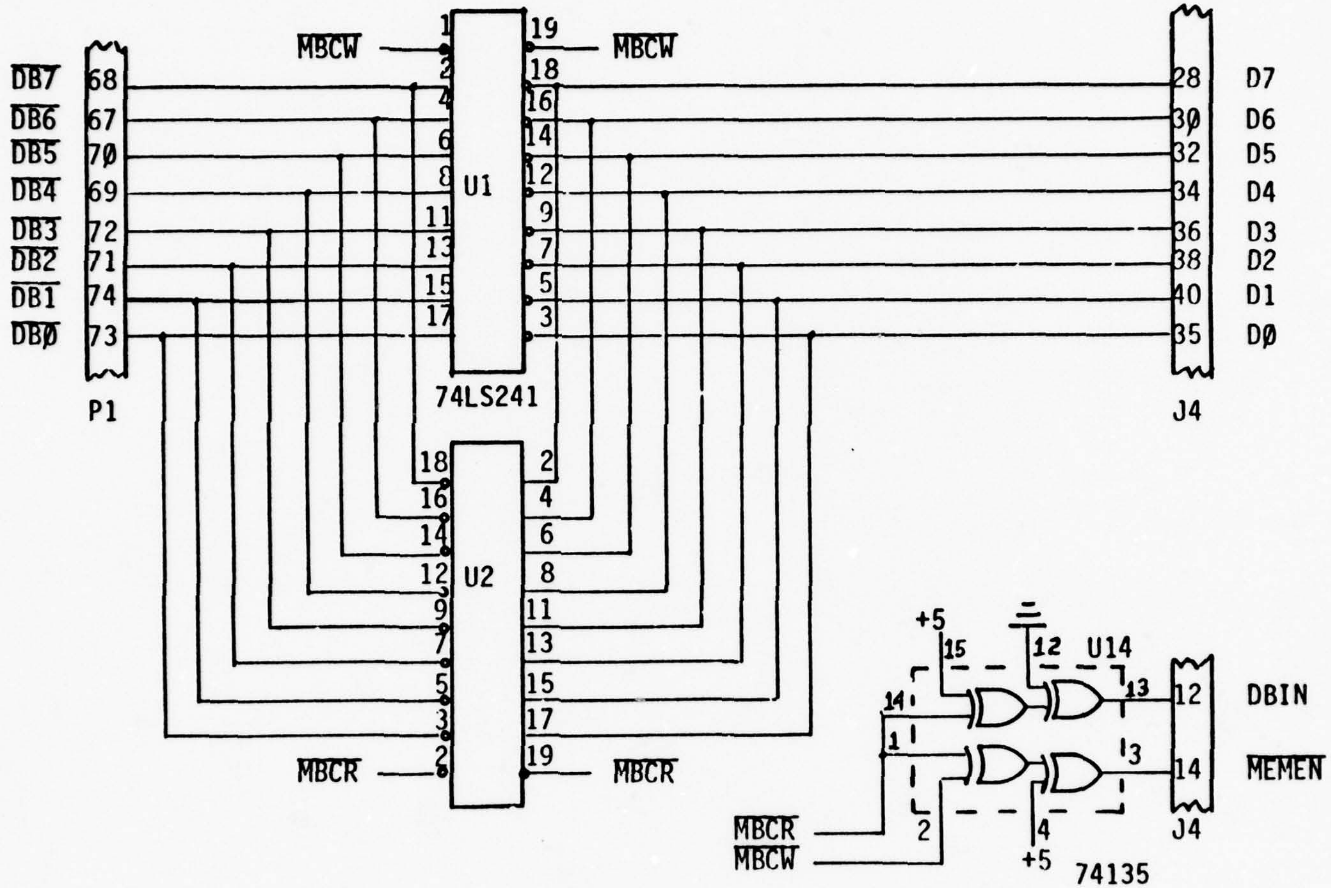


Figure 48. Magnetic Bubble Memory Interface
(sheet 1 of 2)

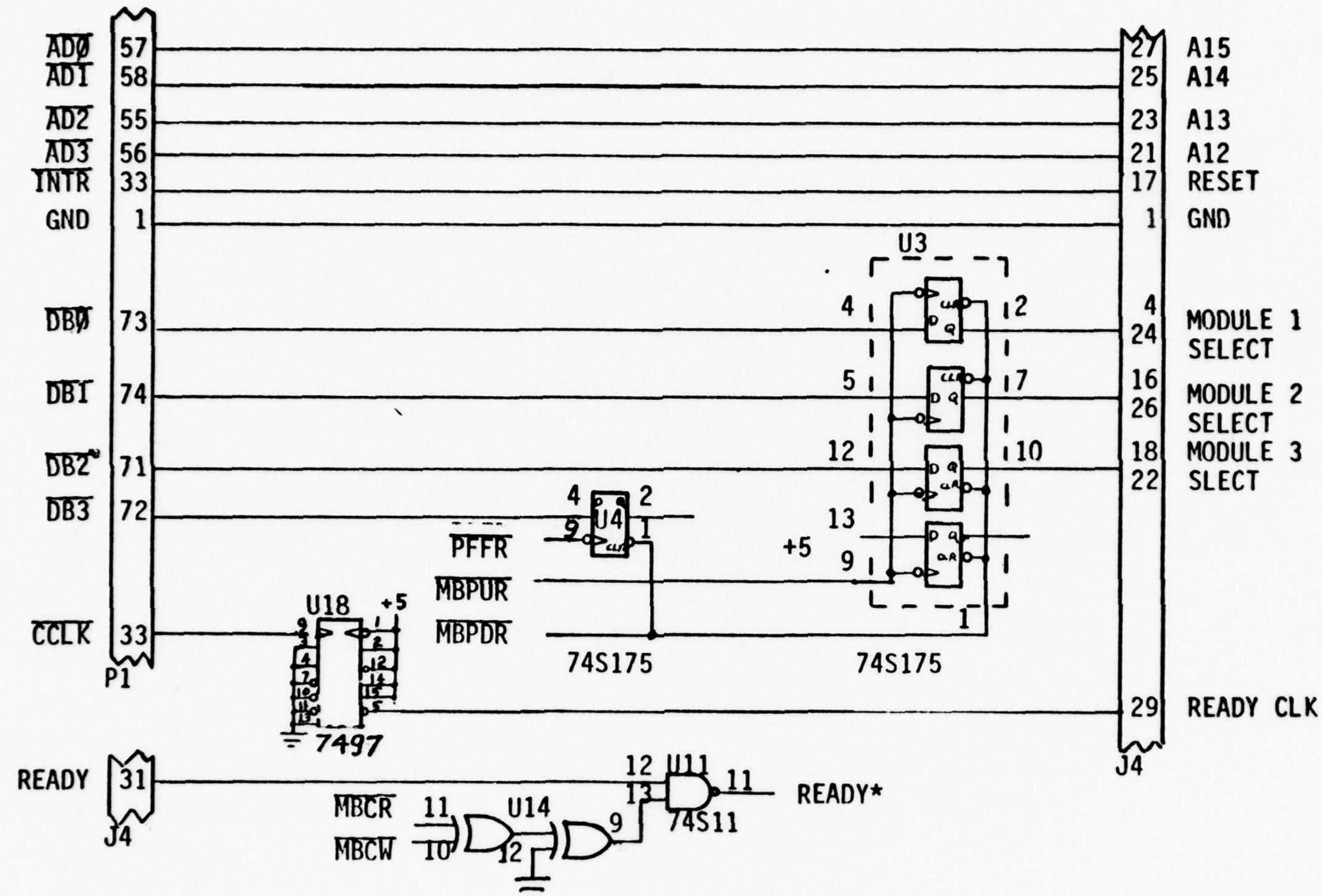


Figure 48. Magnetic Bubble Memory Interface
(sheet 2 of 2)

With address decoding provided by U5&U6 of the interface card, U1 and U2 of the bubble controller module are unnessary. The enable signal, MENEN-, is jumpered from U1-1 to U1-12 and the data direction signal state, DBIN, is jumpered from U1-4 to U1-10 and U1-11. The address decoder U2 is not used. The bubble controller data buffers, U3&U4, are also unused. A jumper plug providing pull-up resistors is substituted for the 74LS226 data latches in U3&U4.

The modification to the STROBE signal requires an additional circuit. A 74LS109, dual JK flip-flop, is located at the U22 position. The functions of U12A, U15A, and U15C are no longer required and are now utilized as shown in Figure 49 to provide the function required in the modification (Ref 19).

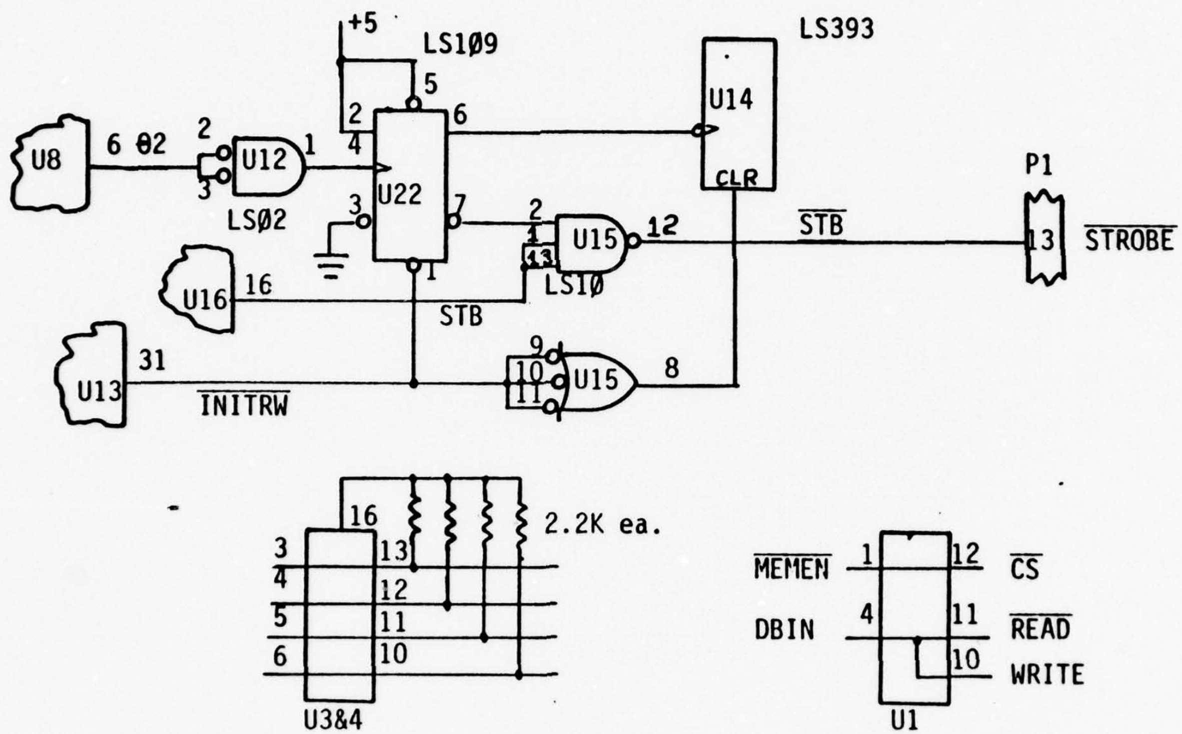


Figure 49. Magnetic Bubble Controller Board (BCA 0200) Modifications

APPENDIX D

Development Tool Operating System

Appendix D

DEVELOPMENT TOOL OPERATING SYSTEM

This operating system is compiled on a CDC 6600 computer using an INTEL MAC80 assembly language assembler for the INTEL 8080 microprocessor. It executes on an INTEL SBC 80/20 single board computer. The operating may be stored in two 8708 PROMs starting at Ø8ØØ (Hex) or read in from a cassette tape. The code executes only after being moved to RAM with a starting address of C8ØØ (Hex). The RAM must extend to D004(Hex). Table VII lists the interrupt levels and their service routine addresses. Not all interrupt lines are provided with interrupt generating sources even though a service routine is provided. Table VIII provides an address map for the major elements of the operaing system.

Table VI. Parallel I/O Port Pin Assignments
(sheet 1 of 2)

SBC 80/20		Interface Board	
Signal	J2 Pin Connection	P3 Pin Connection	Signal
Port B - Bit 7	2	2	N/C
(E9) Bit 6	4	4	N/C
Bit 5	6	6	N/C
Bit 4	8	8	N/C
Bit 3	10	10	N/C
Bit 2	12	12	N/C
Bit 1	14	14	N/C
Bit 0	16	16	N/C
Port C - Bit 5	18	18	N/C
(EA) Bit 6	20	20	N/C
Bit 1	22	22	N/C
Bit 7	24	24	N/C
$\overline{STRBA}$	26	26	$\overline{STB}$
N/C	28	28	N/C
N/C	30	30	N/C
Bit 2	32	32	N/C
Port A - Bit 7	34	34	D7 (msb)
(E8) Bit 6	36	36	D6
Bit 5	38	38	D6
Bit 4	40	40	D5
Bit 3	42	42	D3
Bit 2	44	44	D2
Bit 1	46	46	D1
Bit 0	48	48	D0 (lsb)
N/C	50	50	N/C

Odd numbered pins are GND

N/C No connection

Table VII. Parallel I/O Port Pin Assignments
(sheet 2 of 2)

SBC 80/20		Interface Board	
Signal	J1 Pin Connection	P3 Pin Connection	Signal
Port B - Bit 7	2	52	N/C
(E5) Bit 6	4	54	N/C
Bit 5	6	56	N/C
Bit 4	8	58	N/C
Bit 3	10	60	N/C
Bit 2	12	62	N/C
Bit 1	14	64	N/C
Bit 0	16	66	N/C
Port C - Bit 5	18	68	N/C
(E6) Bit 6	20	70	$\overline{\text{LOAD}}$ $\overline{\text{ENABLE}}$
Bit 1	22	72	N/C
Bit 7	24	74	$\overline{\text{STROBE}}$
$\overline{\text{STRBA}}$	26	76	$\overline{\text{EOC}}$
N/C	28	78	N/C
N/C	30	80	N/C
Bit 2	32	82	N/C
Port A - Bit 7	34	84	$\overline{\text{B1}}$ (msb)
(E4) Bit 6	36	86	B2
Bit 5	38	88	B3
Bit 4	40	90	B4
Bit 3	42	92	B5
Bit 2	44	94	B6
Bit 1	46	96	B7
Bit 0	48	98	B8 (lsb)
N/C	50	100	N/C

Odd numbered pins are GND

N/C No connection

Table VII. Interrupt Jump Table

Interrupt Level	Service Routine Address (Hex)	Cause/Response
0	CBE0	Hardware Switch/ Reset Baud Rate
1	CBE4	Hardware Switch/ IFPDAS III Hardware Initialize
2	CBE8	USART/ Return To SBC 80/20 Monitor
3	CBEC	Counter 1/ Start Sequence Loop
4	CBF0	Hardware Switch/ Data Storage Area Initialize
5	CBF4	Hardware Switch/ Bubble Data Read
6	CBF8	Not Used
7	CBFC	Hardware Switch/ Clear Bubble Contents

Table VIII. Development Tool Memory Map

Function	Address Range (Hex)
PO_2 IN Data Area	3900 - 3916
PO_2 OUT Data Area	3918 - 392E
Flow Rate Data Area	3930 - 3946
Absolute Pressure Data Area	3948 - 395E
Gx Data Area	3960 - 3976
Gy Data Area	3978 - 398E
Gz Data Area	3990 - 39A6
Heart Rate Data Area	39A8 - 39BE
Hardware Initialization	C800 - C883
Data Storage Area Initialization	C884 - C947
Sequencer	C948 - C9F3
Data Service Routines	CA00 - CB0A
Page Transfer	CB0B - CB54
Interrupt Jump Table	CBE0 - CBFF
Initialization List	CC01 - CC1B
Sequencer List	CC1C - CC57
Bubble Data Dump	CC58 - CCA5
Bubble Page Clear	CCA6 - CCEF
Sequencer List Pionter (LSTP)	D000 - D001
Bubble Memory Page Counter	D002 - D003
Bubble Select Mask	D004

```
;*************************************************

;IFPDAS III DEVELOPMENT TOOL OPERATING SYSTEM

;*************************************************

;  THIS PROGRAM CONTROLS THE OPERATION OF THE
; IFPDAS III DEVELOPMENT TOOL HARDWARE. EXECUTION
; OF THE OPERATING SYSTEM BY THE CPU RESULTS IN
; HARDWARE INITIALIZATION, DATA STORAGE AREA INIT-
; ILIZATION, CONVERSION OF PROBE DATA AND STORAGE
; OF THE DATA IN A MAGNETIC BUBBLE MEMORY. THE
; OPERATING SYSTEM SELECTS THE PROBE TO BE CONV-
; ERTED, STARTS THE CONVERSION, FETCHES THE DATA,
; PREPARES DATA FOR STORAGE AND STORES DATA IN THE
; BUBBLE MEMORY.

;*************************************************

; THE OPERATING SYSTEM CONSISTS OF THE FOFFOWING
; PROGRAM MODULES:

;  HWI - HARDWARE INITIALIZATION ROUTINE FOR THE
;        SCB 80>20 SYSTEM

;  DSI - INITIALIZATION OF THE DATA STORAGE AREA
;        IN THE RAM

;  S1  - DATA PROBE SELECTION, CONVERSION AND
;        AVERAGING

;  SR1 - TYPE 1 DATA SERVICE ROUTINE (PREPARE
;        DATA FOR STORAGE)

;  SR2 - TYPE 2 DATA SERVICE ROUTINE (PREPARE
;        DATA FOR STORAGE)

;  SR3 - TYPE 3 DATA SERVICE ROUTINE (PREPARE
;        DATA FOR STORAGE)

; PGXF - TRANSFER DATA TO THE BUBBLE MEMORY
;        AND THE CONSOLE

; MBDP - TRANSFER CONTENTS OF BUBBLE MEMORY
;        TO CONSOLE/CASETTE RECORDER

; MBCL - CLEAR THE CONTENTS OF THE BUBBLE
;        MEMORY

;DTOUT (SUBROUTINE) - SEND ASCII CHARACTERS TO
;        THE CONSOLE
```

```
;*************************************************

; NOTE: THIS OPERATING SYSTEM IS DESIGNED TO
; OPERATE WITH THE SBC 80/20 MONITOR. THE CODE
; MUST BE MOVED FROM 0800H - 0FFFH TO RAM LOCATED
; AT C800H.
; TO EXECUTE THIS CODE FROM LOCATION 0800H, THE
; FOLLOWING CHANGES MUST BE MADE:
;     ICW2  EQU  00BH
;     BSMSK EQU  3804H
;     ILISP EQU  0C01H
;     LSTP  EQU  3800H
;     MBPCT EQU  3802H
;     NPB   EQU  0C00H
;     SRAH  EQU  000AH
; SET THE FIRST ORG AT 0800H AND REASSEMBLE
; THROUGH MAC80. THE CODE THEN EXECUTES USING
; ONLY THE SBC 80/20  RAM.

;*************************************************
;*************************************************

;ASSEMBLER EQU

;*************************************************


          ;DAS 1128

00E4      DATA     EQU      0E4H ;CONVERTED DATA PORT ADDRESS
0020      IMSK     EQU      020H ;DATA READY MASK
000C      LDEN     EQU      00CH ;CLEARS BIT C6
0020      PROBE    EQU      020H ;PROBE MUX PORT
00E6      STAT1    EQU      0E6H ;DATA STATUS PORT
000E      STRB1    EQU      00EH ;CLEARS BIT C7

          ;HEART RATE

00E8      HEART    EQU      0E8H ;HEART RATE DATA PORT
00EA      STAT2    EQU      0EAH ;HEART RATE STATUS PORT

          ;INTERRUPT CONTROLLER

00DA      ICCP1    EQU      0DAH ;CONTROL PORT 1
00DB      ICCP2    EQU      0DBH ;CONTROL PORT 2
00F6      ICW1     EQU      0F6H ;CONTROL WORD 1
00CB      ICW2     EQU      0CBH ;CONTROL WORD 2
00DB      OCW1     EQU      0DBH ;MASK PORT

          ;DIAGNOSTIS LED

00D6      LED      EQU      0D6H ;LED ACTIVATION PORT
```

```
                ;MAGNETIC BUBBLE CONTROLLER

ØØ1D            MBCCR   EQU        Ø1DH ;CONTROL-COMMAND PORT
ØØ1C            MBFRR   EQU        Ø1CH ;READ FROM FIFO PORT
ØØ1B            MBFWR   EQU        Ø1BH ;WRITE TO FIFO PORT
ØØØ1            MBICW   EQU        ØØ1H ;INITIALIZE COMMAND WORD
ØØ2Ø            MBIM    EQU        Ø2ØH ;CONTROLLER IDLE MASK
ØØ17            MBLLR   EQU        Ø17H ;MINOR LOOP SIZE REG (LSBY)
ØØ16            MBLMR   EQU        Ø16H ;MINOR LOOP SIZE REG (MSBY)
ØØ1F            MBPS1   EQU        Ø1FH ;PAGE SELECT REG (LSBY)
ØØ1E            MBPS2   EQU        Ø1EH ;PAGE SELECT REG (MSBY)
ØØ13            MBPSR   EQU        Ø13H ;PAGE SIZE REGISTER
ØØØ4            MBPTB   EQU        ØØ4H ;TRANSFER FIFO PAGE TO
                                        ;BUBBLE COMMAND
ØØØ2            MBPTF   EQU        ØØ2H ;TRANSFER BUBBLE PAGE TO
                                        ;FIFO COMMAND
ØØ1A            MBSR    EQU        Ø1AH ;CONTROLLER STATUS PORT

                ;MEMORY LOCATIONS AND ADDRESSES

DØØ4            BSMSK   EQU      ØDØØ4H ;BUBBLE SELECT MASK
                                        ;STORAGE ADDRESS
CCØ1            ILSTP   EQU      ØCCØ1H ;INITIALIZATION LIST START
DØØØ            LSTP    EQU      ØDØØØH ;SEQUENCER LIST POINTER
ØØ1C            LSTPB   EQU       ØØ1CH ;SEQUENCER LIST BEGINNING
ØØ57            LSTPE   EQU       ØØ57H ;SEQUENCER LIST END
DØØ2            MBPCT   EQU      ØDØØ2H ;PAGE COUNTER STORAGE
CCØØ            NPB     EQU      ØCCØØH ;NUMBER OF DATA PROBES
ØØCA            SRAH    EQU       ØØCAH ;UPPER BYTE OF SERVICE
                                        ;ROUTINE ADDRESS

                ;PARALLEL PORTS
ØØB6            PIAM1   EQU        ØB6H ;MODE 1 COMMAND WORD
ØØE7            PPI1    EQU        ØE7H ;PIA1 COMMAND PORT
ØØEB            PPI2    EQU        ØEBH ;PIA2 COMMAND PORT

                ;REGISTERS

ØØ6Ø            MBPDR   EQU        Ø6ØH ;BUBBLE POWER DOWN REGISTER
ØØ5Ø            MBPUR   EQU        Ø5ØH ;BUBBLE SELECT AND POWER UP
ØØ7Ø            PFFR    EQU        Ø7ØH ;POWER FAIL FLAG
ØØ4Ø            PWOFF   EQU        Ø4ØH ;IFPDAS POWER OFF

                ;TIMER

ØØ3Ø            CØMD2   EQU        Ø3ØH ;COUNTER Ø MODE 2 COMMAND
ØØ7Ø            C1MD2   EQU        Ø7ØH ;COUNTER 1 MODE 2 COMMAND
ØØB6            C2MD3   EQU        ØB6H ;COUNTER 2 MODE 3 COMMAND
ØØDC            CTRØ    EQU        ØDCH ;COUNTER Ø DATA PORT
ØØDD            CTR1    EQU        ØDDH ;COUNTER 1 DATA PORT
ØØDE            CTR2    EQU        ØDEH ;COUNTER 2 DATA PORT
ØØDF            TMCP    EQU        ØDFH ;TIMER COMMAND PORT
ØØ4Ø            TWLCH   EQU        Ø4ØH ;LATCH COUNTER 1 FOR OUTPUT
```

```
              ;USART

00EC          CON      EQU       0ECH ;TRANSMIT PORT
004E          MODE     EQU       04EH ;MODE COMMAND
0001          READY    EQU       001H ;TRANSMITTER READY MASK
0037          RSTUR    EQU       037H ;RESET COMMAND
00ED          USART    EQU       0EDH ;COMMAND PORT
```

```
                ;*************************************************

                ;HARDWARE INITIALIZE

                ;THE MAGNETIC BUBBLE CONTROLLER, USART, STACK
                ;POINTER, PIA, INTERRUPT CONTROLLER, AND
                ;TIMER ARE INITIALIZED FOLLOWING AN HWI INTERRUPT
                ;(LEVEL 1). THE LAST STEPS ENABLE THE DATA
                ;STORAGE INITIALIZE, BUBBLE DATA DUMP, BUBBLE CLEAR
                ;AND MONITOR INTERRUPTS TO OCCUR.

                ;*************************************************



                ;***** MAGNETIC BUBBLE CONTROLER

C800                     ORG      0C800H
C800 F3         HWI:     DI

                ;THE MINOR LOOP COUNTERS, MBLMR & MBLLR, ARE SET TO
                ;641 BITS PER MINOR LOOP

C801 3E81                MVI      A,129
C803 D317                OUT      MBLLR
C805 3E02                MVI      A,2
C807 D316                OUT      MBLMR

                ;THE PAGE SIZE REGISTER, MBPSR, IS SET AT 18 BYTES
                ;PER PAGE

C809 3E12                MVI      A,18
C80B D313                OUT      MBPSR

                ;THE CURRENT PAGE COUNT CONTAINED AT MBPCT IS SET
                ;TO ZERO

C80D 210000              LXI      H,0
C810 2202D0              SHLD     MBPCT

                ;THE INITIALIZATION COMMAND WORD, 040 (HEX), IS
                ;SENT TO THE CONTROLLER COMMAND PORT (MBCCR)

C813 3E40                MVI      A,040H
C815 08                  DB       08H    ;NUMBER OF PROBES

C816 D31D                OUT      MBCCR
```

```
                  ;THE BUBBLE SELECT MASK IS SET TO THE FIRST MODULE

C818 3E01               MVI     A,1
C81A 3204D0             STA     BSMSK
C81D 47                 MOV     B,A

                  ;THE BUBBLE MODULE IS SELECTED AND INITIALIZED

C81E D350       HWIBC:  OUT     MBPUR

                  ;INITIALIZE THE BUBBLE
C820 3E01               MVI     A,MBICW
C822 D31D               OUT     MBCCR

                  ;THIS ROUTINE IS AN IDLE TEST OF THE MAGNETIC
                  ;BUBBLE CONTROLLER. IT TESTS THE CONTROLLER
                  ;STATUS TO DETECT WHEN THE CONTROLLER IS FINISHED
                  ;EXECUTION.

                  ;TIME FILLER

C824 00                 NOP

                  ;GET THE CONTROLLER STATUS

C825 DB1A               IN      MBSR

                  ;TEST THE IDLE BIT

C827 E620               ANI     MBIM

                  ;GET NEW STATUS IF BUSY

C829 C225C8             JNZ     $-4

                  ;POWER DOWN THE MODULE.

C82C D360               OUT     MBPDR

                  ;***** USART

                  ;THE RESET WORD, 040 (HEX), IS SENT TO THE USART
                  ;THE MODE WORD SETS THE NEW USART MODE
                  ;THE USART IS SET NOW FOR: 1 STOP BIT, NO PARITY,
                  ;8 DATA BITS, AND CLOCK=16XBAUD RATE

C82E 3E40       HWIU:   MVI     A,040H
C830 D3ED               OUT     USART
C832 3E4E               MVI     A,MODE
C834 D3ED               OUT     USART
```

```
                ;RSTUR SETS: NO HUNT MODE, NO INTERNAL RESET, RTS
                ;HIGH, RESET ERROR FLAGS, RECEIVE AND TRANSMIT
                ;ENABLED, AND DTR HIGH

C836 3E37               MVI     A,RSTUR
C838 D3ED               OUT     USART

                ;***** STACK POINTER

                ;THE STACK POINTER IS INITIALIZED AT 3FFD (HEX)

C83A 31FD3F HWISP:      LXI     SP,3FFDH

                ;***** PIA

                ;PIAM1 SETS BOTH PIAS TO MODE 1, STROBBED I-O
                ;PORTS A&B CAN BE EITHER FOR INPUT OR OUTPUT
                ;AND PORT C PROVIDES THE HANDSHAKING (STROBE)
                ;SIGNALS

C83D 3EB6   HWIP:       MVI     A,PIAM1
C83F D3E7               OUT     PPI1
C841 D3EB               OUT     PPI2

                ;BITS C6 & C7 ARE USED FOR OUTPUT. LDEN IS BIT
                ;C6 OF PIA1 IS USED TO ALLOW THE DAS MUX LOAD
                ;STRB1 IS BIT C7 OF PIA1 AND IS USED TO ALLOW
                ;STROBE2 (PROBE) TO STROBE IN THE DAS MUX

C843 3E0C               MVI     A,LDEN
C845 D3E7               OUT     PPI1
C847 3E0E               MVI     A,STRB1
C849 D3E7               OUT     PPI1

                ;***** INTERRUPT CONTROLLER

                ;THE INTERRUPT JUMP TABLE IS SET AT 0BE0 (HEX) WITH
                ;FOUR BYTES PER INTERRUPT LEVEL

C84B 3EF6   HWII:       MVI     A,ICW1
C84D D3DA               OUT     ICCP1
C84F 3ECB               MVI     A,ICW2
C851 D3DB               OUT     ICCP2

                ;***** TIMER

                ;COUNTERS CTR0 & CTR1 ARE SET UP FOR MODE 2,
                ;RATE GENERATION, OPERATION BY C0MD2 AND C1MD2

C853 3E30   HWIT:       MVI     A,C0MD2
C855 D3DF               OUT     TMCP
C857 3E70               MVI     A,C1MD2
C859 D3DF               OUT     TMCP
```

```
                ;COUNTER 0 RATE IS SET TO MODULO 2105 OR A 2 MILLI-
                ;SECOND PERIOD

C85B 3E01               MVI     A,1
C85D D3DC               OUT     CTR0
C85F 3E15               MVI     A,21
C861 D3DC               OUT     CTR0

                ;COUNTER 2 IS SET FOR MODE 3, SQUARE WAVE,
                ;OPERATION BY C2MD3. THE MODULO 56 PROVIDES THE
                ;38400 HZ NECESSARY FOR A BAUD RATE OF 1200.

C863 3EB6               MVI     A,C2MD3
C865 D3DF               OUT     TMCP
C867 3E38               MVI     A,56
C869 D3DE               OUT     CTR2
C86B AF                 XRA     A
C86C D3DE               OUT     CTR2

                ;***** INTERRUPT MASK

                ;THE INTERRUPT MASK WORD SENT TO THE MASK REGISTER
                ;ALLOWS LEVELS 2,4,5,6&7 TO INTERRUPT THE SYSTEM.
                ;THESE INTERRUPTS COME FROM THE CONSOLE(LEVEL 2),
                ;DATA STORAGE INITIALIZE(LEVEL 4),  BUBBLE DUMP
                ;(LEVEL 5), SPECIAL DATA DUMP(LEVEL 6), AND BUBBLE
                ;CLEAR(LEVEL 7)

C86E 3E0B       HWIIM:  MVI     A,00001011B
C870 D3DB               OUT     OCW1
C872 FB                 EI

                ;***** THE HARDWARE INITIALIZE IS FINISHED

                ;TO SIMULATE A HALT, THE SYSTEM IS LOOPED AROUND
                ;FLASHING THE DIAGNOSTIC LED UNTIL ONE OF THE
                ;OF THE INTERRUPTS OCCUR

C873 D3D6               OUT     LED
C875 11FFFF             LXI     D,0FFFFH
C878 1D                 DCR     E
C879 C278C8             JNZ     $-1
C87C 15                 DCR     D
C87D CA7CC8             JZ      $-1
C880 C373C8             JMP     $-13
C883 00                 NOP
```

```
;*************************************************

;DATA STORAGE INITIALIZE

;DATA STORAGE INITIALIZATION STARTS FROM A DSI
;INTERRUPT
;THE PROBE DATA AREAS ARE INITIALIZED. LTIME AND
;THE LAST 17 BYTES IN THE DATA PAGE ARE CLEARED.
; THE INITIAL VALUE FOR LVAL OR LZ IS CONVERTEDD
;COMPUTED, THEN LOADED INTO THE PROBE DATA
;AREA. WORD COUNT (WRDCT) IS TRANSFERRED FROM THE
;ILST TO THE PROBE DATA AREA AND NEXT IS SET UP
;TO POINT AT THE SECOND WORD OF THE DATA PAGE.
;THE PROBE ID IS MOVED INTO THE FIRST WORD OF THE
;DATA PAGE.
;RAM LOCATIONS FOR THE SEQUENCER LIST POINTER,
;BUBBLE SELECT MASK,AND THE PAGE COUNTER ARE
;INITIALIZED.
;THE MASTER CLOCK, COUNTER 1, IS SET TO START
;COUNTING DOWN FROM FFFF (HEX)
;CONTROL IS PASSED TO THE SEQUENCER

;*************************************************


;GET THE BEGINNING ADDRSS OF THE INITIALIZATION
;LIST IN H:L

C884 2101CC DSIP:    LXI     H,ILSTP

;GET THE PROBE MUX (ID) FROM THE INITIALIZATION
;AND START TYPE 1 INITIALIZATION

;GET PROBE DATA AREA ADDRESS

C887 23     DSIP1:   INX     H
C888 5E              MOV     E,M
C889 23              INX     H
C88A 56              MOV     D,M

;CLEAR LTIME

C88B AF              XRA     A
C88C 12              STAX    D

;CONVERT THE PROBE DATA

C88D 78              MOV     A,B
C88E D320            OUT     PROBE
```

```
                ;TEST FOR DATA READY

C890 DBE6               IN STAT1
C892 E620               ANI      IMSK
C894 CA90C8             JZ       $-4

                ;GET DATA

C897 DBE4               IN       DATA

                ;LOAD LVAL

C899 13                 INX      D
C89A 12                 STAX     D

                ;LOAD WRDCT

C89B 3E0F               MVI      A,15
C89D 13                 INX      D
C89E 12                 STAX     D

                ;SET NEXT

C89F 13                 INX      D
C8A0 3E02               MVI      A,2
C8A2 83                 ADD      E
C8A3 12                 STAX     D

                ;PLACE PROBE ID IN DATA PAGE

C8A4 13                 INX      D
C8A5 78                 MOV      A,B
C8A6 12                 STAX     D

                ;THE NEXT 17 LOCATIONS ARE CLEARED

C8A7 0E11               MVI      C,17
C8A9 AF                 XRA      A
C8AA 13                 INX      D
C8AB 12                 STAX     D
C8AC 0D                 DCR      C
C8AD C2AAC8             JNZ      $-3

                ;GET THE NEXT PROBE MUX AND TEST FOR
                ;END OF TYPE 1

C8B0 23                 INX      H
C8B1 46                 MOV      B,M
C8B2 AF                 XRA      A
C8B3 80                 ADD      B
C8B4 C287C8             JNZ      DSIP1
```

```
                ;GET PROBE MUX FROM INITIALIZATION LIST AND
                ;START TYPE 2 INITIALIZATION

C8B7 23                 INX     H
C8B8 46                 MOV     B,M

                ;GET PROBE DATA AREA ADDRESS

C8B9 23         DSIP2:  INX     H
C8BA 5E                 MOV     E,M
C8BB 23                 INX     H
C8BC 56                 MOV     D,M

                ;CLEAR LTIME

C8BD AF                 XRA     A
C8BE 12                 STAX    D

                ;CONVERT THE PROBE DATA

C8BF 78                 MOV     A,B
C8C0 D320               OUT     PROBE

                ;TEST FOR DATA READY

C8C2 DBE6               IN STAT1
C8C4 E620               ANI     IMSK
C8C6 CAC2C8             JZ      $-4

                ;GET DATA

C8C9 DBE4               IN      DATA

                ;COMPUTE ZONE

C8CB E6E0               ANI     11100000B

                ;LOAD LZONE

C8CD 13                 INX     D
C8CE 12                 STAX    D

                ;LOAD WRDCT

C8CF 3E11               MVI     A,17
C8D1 13                 INX     D
C8D2 12                 STAX    D

                ;SET NEXT

C8D3 13                 INX D
C8D4 3E02               MVI     A,2
C8D6 83                 ADD     E
C8D7 12                 STAX    D
```

```
                  ;PLACE PROBE ID IN DATA PAGE

C8D8 13                  INX      D
C8D9 78                  MOV      A,B
C8DA 12                  STAX     D

                  ;THE NEXT 17 LOCATIONS ARE CLEARED

C8DB 0E11                MVI      C,17
C8DD AF                  XRA      A
C8DE 13                  INX      D
C8DF 12                  STAX     D
C8E0 0D                  DCR      C
C8E1 C2DEC8              JNZ      $-3

                  ;GET PROBE MUX AND TEST FOR END OF TYPE 2

C8E4 23                  INX      H
C8E5 46                  MOV      B,M
C8E6 AF                  XRA      A
C8E7 80                  ADD      B
C8E8 C2B9C8              JNZ      DSIP2

                  ;GET PROBE MUX FROM INITIALIZATION LIST AND
                  ;START TYPE 3 INITIALIZATION

C8EB 23                  INX      H
C8EC 46                  MOV      B,M

                  ;GET PROBE DATA AREA ADDRESS

C8ED 23           DSIP3: INX      H
C8EE 5E                  MOV      E,M
C8EF 23                  INX      H
C8F0 56                  MOV      D,M

                  ;CLEAR LTIME

C8F1 AF                  XRA      A
C8F2 12                  STAX     D

                  ;CONVERT THE PROBE DATA

C8F3 78                  MOV      A,B
C8F4 D320                OUT      PROBE

                  ;TEST FOR DATA READY

C8F6 DBE6                IN       STAT1
C8F8 E620                ANI      IMSK
C8FA CAF6C8              JZ       $-4
```

```
                ;GET DATA

C8FD DBE4            IN        DATA

                ;LOAD WRDCT

C8FF 3EØA            MVI       A,1Ø
C9Ø1 13              INX       D
C9Ø2 12              STAX      D

                ;SET NEXT

C9Ø3 13              INX       D
C9Ø4 3EØ3            MVI       A,3
C9Ø6 83              ADD       E
C9Ø7 12              STAX      D

                ;PLACE PROBE ID IN DATA PAGE

C9Ø8 13              INX       D
C9Ø9 78              MOV       A,B
C9ØA 12              STAX      D

                ;THE NEXT 17 LOCATIONS ARE CLEARED

C9ØB ØE11            MVI       C,17
C9ØD AF              XRA       A
C9ØE 13              INX       D
C9ØF 12              STAX      D
C91Ø ØD              DCR       C
C911 C2ØEC9          JNZ       $-3

                ;GET PROBE MUX AND TEST FOR END OF TYPE 3

C914 23              INX       H
C915 46              MOV       B,M
C916 AF              XRA       A
C917 8Ø              ADD       B
C918 C2EDC8          JNZ       DSIP3

                ;GET HEART RATE PROBE DATA PAGE AREA ADDRESS

C91B 23              INX       H
C91C 5E              MOV       E,M
C91D 23              INX       H
C91E 56              MOV       D,M

                ;CLEAR LTIME

C91F AF              XRA       A
C92Ø 12              STAX      D
```

```
                ;TEST FOR HEART RATE READY

C921 DBEA               IN      STAT2
C923 E620               ANI     IMSK
C925 C221C9             JNZ     $-4

                ;GET HEART RATE

C928 DBE8               IN      HEART

                ;LOAD LVAL

C92A 13                 INX     D
C92B 12                 STAX    D

                ;LOAD WRDCT

C92C 3E0F               MVI     A,15
C92E 13                 INX     D
C92F 12                 STAX    D

                ;SET NEXT

C930 13                 INX     D
C931 3E02               MVI     A,2
C933 83                 ADD     E
C934 12                 STAX    D

                ;PLACE PROBE ID IN DATA PAGE

C935 13                 INX     D
C936 3E60               MVI     A,60H
C938 12                 STAX    D

                ;THE NEXT 17 LOCATIONS ARE CLEARED

C939 0E11               MVI     C,17
C93B AF                 XRA     A
C93C 13                 INX     D
C93D 12                 STAX    D
C93E 0D                 DCR     C
C93F C23CC9             JNZ     $-3

                ;THE DATA PAGE INITIALIZATION IS COMPLETE
                ;THE MASTER CLOCK, COUNTER 1, IS SET TO
                ;COUNT DOWN FROM FFFF (HEX)

C942 3EFF       DSIC:   MVI     A,0FFH
C944 D3DD               OUT     CTR1
C946 D3DD               OUT     CTR1

                ;CONTROL NOW PASSES TO THE SEQUENCER
```

```
;*************************************************

;SEQUENCER

;THE SEQUENCER IS THE EXECUTIVE ROUTINE WHICH
;SELECTS PROBES, CONVERTS PROBE DATA AND SELECTS
;CONVERSION ROUTINES. THE ORDER OF PROBE SELECTION
;AND SERVICE ROUTINES IS PROVIDED BY THE SEQUENCER
;LIST POINTED TO BY  LSTP+1:LSTP .
;THE SEQUENCER STARTS BY WAITING FOR COUNTER 0 TO
;ADVANCE THE TIME COUNT AND GENERATE AN INTERRUPT

;*************************************************



;THE COUNTER 0 INTERRUPT IS ENABLED AND THE SYSTEM
;HALTED UNTIL CTR0 IS TIMED OUT (INTERRUPT LEVEL 3)

C948 F3              DI
C949 3EF1            MVI      A,11110001B
C94B D3DB            OUT      OCW1
C94D FB        S1:   EI
C94E 76              HLT
C94F F3              DI

;THE CONVERSION ROUTINE IS STARTED
;THIS ROUTINE GETS THE VALUE OF THE PROBE AND THE
;TIME. IT STARTS BY MOVING THE MUX OF THE PROBE TO
;BE CONVERTED FROM THE SEQUENCER LIST AND STARTS THE
;CONVERSION.
;THE PROBE MUX IS TESTED FOR HEART RATE CONVERSION
;AND IF TRUE, THE HEART RATE IS ACQUIRED ONCE FROM
;THE HEART RATE PORT AND PLACED IN C.
;FOR OTHER PROBES, THE SIGNAL IS CONVERTED 8 TIMES
;AND THE RUNNING SUM OF THE CONVERSIONS IS AVERAGED
;AND SAVED IN C.
;WHEN THE CONVERSION IS COMPLETE, THE TIME IS
;ACQUIRED

;THE SEQUENCER LIST POINTER  LSTP  IS LOADED
;IN H:L, UPDATED AND STORED BACK IN  LSTP
;THE PROBE MUX IS MOVED FROM THE SEQUENCER LIST
;INTO A

C950 2A00D0          LHLD     LSTP
C953 7E              MOV      A,M
C954 23              INX      H
C955 2200D0          SHLD     LSTP
```

```
                ;THE PROBE MUX IS SAVED IN B AND TESTED FOR
                ;HEART RATE TYPE

C958 47                 MOV     B,A
C959 E620               ANI     00100000B
C95B C2B5C9             JNZ     CONVH

                ;THE PROBE MUX IS SENT TO THE DAS AND CONVERSION
                ;STARTED

C95E 78         CONV1:  MOV     A,B
C95F D320               OUT     PROBE

                ;D:E AND H:L ARE CLEARED FOR DOUBLE PRECISION
                ;ADDITION AND C IS SET UP FOR 8 CONVERSIONS

C961 210000             LXI     H,0000H
C964 110000             LXI     D,0000H
C967 0E08               MVI     C,8

                ;WHEN DATA IS READY MOVE IT INTO E AND ADD TO
                ;RUNNING SUM IN H:L

C969 DBE6       CONV2:  IN      STAT1
C96B E620               ANI     IMSK
C96D CA69C9             JZ      CONV2
C970 DBE4               IN      DATA
C972 5F                 MOV     E,A
C973 19                 DAD     D

                ;CONTINUE THIS PROCESS 8 TIMES

C974 0D                 DCR     C
C975 C269C9             JNZ     CONV2

                ;GET THE TIME
                ;THIS ROUTINE GETS THE TIME WORD FROM COUNTER 1
                ;FOR PROBES WHICH REQUIRE SMALL TIME INCREMENTS,
                ;THE LOWER TIME BYTE IS PLACED IN B.
                ;FOR PROBES WHICH REQUIRE LARGE TIME INCREMENTS,
                ;THE UPPER TIME BYTE IS PLACED IN B
                ;THE PROBE MUX BIT 6 INDICATES WHICH BYTE OF TIME
                ;TO USE. BIT 6 HIGH INDICATES UPPER BYTE, BIT 6 LOW
                ;INDICATES LOWER BYTE.

                ;THE COMMAND WORD TO LATCH COUNTER 1 TIME INTO THE
                ;READ PORT IS SENT TO THE TIMER COMMAND PORT.

C978 3E40               MVI     A,TWLCH
C97A D3DF               OUT     TMCP
```

```
          ;THE PROBE MUX IS TESTED FOR UPPER OR LOWER BYTE
          ;OF TIME FLAG

C97C 3E40          MVI     A,01000000B
C97E A0            ANA     B
C97F CA8BC9        JZ      TLBY

          ;PLACE THE UPPER BYTE IN B

C982 DBDD   TUBY:  IN      CTR1
C984 DBDD          IN      CTR1

          ;CORRECT FOR DOWN COUNTER

C986 2F            CMA
C987 47            MOV     B,A
C988 C38FC9        JMP     TLBY+4

          ;PLACE THE LOWER BYTE OF TIME IN B

C98B DBDD   TLBY:  IN      CTR1

          ;CORRECT FOR DOWN COUNTER

C98D 2F            CMA
C98E 47            MOV     B,A
C98F DBDD          IN      CTR1

          ;THE RUNNING SUM IN H:L IS DIVIDED BY 8, ONE
          ;BYTE AT A TIME

C991 7D     AVG:   MOV     A,L
C992 0F            RRC
C993 0F            RRC
C994 0F            RRC
C995 0F            RRC
C996 D2A8C9        JNC     AVG1
C999 F6E0          ORI     0E0H
C99B C601          ADI     1
C99D D2A8C9        JNC     AVG1
C9A0 F6E0          ORI     0E0H
C9A2 C601          ADI     1
C9A4 D2A8C9        JNC     AVG1
C9A7 24            INR     H
C9A8 E61F   AVG1:  ANI     01FH
C9AA 4F            MOV     C,A
C9AB 7C            MOV     A,H
C9AC 0F            RRC
C9AD 0F            RRC
C9AE 0F            RRC
C9AF 0F            RRC
C9B0 81            ADD     C
C9B1 4F            MOV     C,A
C9B2 C3D8C9        JMP     CONVE
```

```
                ;GET THE HEART RATE AND TIME
                ;GET THE STATUS OF THE HEART RATE DATA PORT

C9B5 DBEA   CONVH:  IN      STAT2
C9B7 E620           ANI     IMSK

                ;IF NO NEW HEART RATE IS READY (A IS ZERO),
                ;JUMP AHEAD 5 PLACES AND MOVE A INTO C

C9B9 CABEC9         JZ      $+5

                ;GET THE HEART RATE

C9BC DBE8           IN      HEART

                ;SAVE THE HEART RATE IN C

C9BE 4F             MOV     C,A

                ;GET THE TIME
                ;THIS ROUTINE GETS THE TIME WORD FROM COUNTER 1.
                ;FOR PROBES WHICH REQUIRE SMALL TIME INCREMENTS,
                ;THE LOWER TIME BYTE IS PLACED IN B.
                ;FOR PROBES WHICH REQUIRE LARGE TIME INCREMENTS,
                ;THE UPPER TIME BYTE IS PLACED IN B
                ;THE PROBE MUX BIT 6 INDICATES WHICH BYTE OF TIME
                ;TO USE. BIT 6 HIGH INDICATES UPPER BYTE, BIT 6 LOW
                ;INDICATES LOWER BYTE.

                ;THE COMMAND WORD TO LATCH COUNTER 1 TIME INTO THE
                ;READ PORT IS SENT TO THE TIMER COMMAND PORT.

C9BF 3E40           MVI     A,TWLCH
C9C1 D3DF           OUT     TMCP

                ;THE PROBE MUX IS TESTED FOR UPPER OR LOWER BYTE
                ;OF TIME FLAG

C9C3 3E40           MVI     A,01000000B
C9C5 A0             ANA     B
C9C6 CAD2C9         JZ      TLBY2

                ;PLACE THE UPPER BYTE IN B

C9C9 DBDD   TUBY2:  IN      CTR1
C9CB DBDD           IN      CTR1

                ;CORRECT FOR DOWN COUNTER

C9CD 2F             CMA
C9CE 47             MOV     B,A
C9CF C3D6C9         JMP     TLBY2+4
```

```
                ;PLACE THE LOWER BYTE OF TIME IN B

C9D2 DBDD       TLBY2:  IN      CTR1

                ;CORRECT FOR DOWN COUNTER

C9D4 2F                 CMA
C9D5 47                 MOV     B,A
C9D6 DBDD               IN      CTR1

                ;THE DATA PAGE AREA POINTER IS MOVED FROM THE
                ;SEQUENCER LIST TO D:E

C9D8 2A00D0     CONVE:  LHLD    LSTP
C9DB 5E                 MOV     E,M
C9DC 23                 INX     H
C9DD 56                 MOV     D,M
C9DE 23                 INX     H

                ;THE SEQUENCER LIST POINTER IN H:L IS COMPARED WITH
                ;THE END OF THE LIST  LSTPE . IF THE END IS REACHED
                ; LSTP  IS RESET TO  LSTPB , OTHERWISE,  LSTP  IS
                ;ADVANCED

C9DF 3A5700             LDA     LSTPE
C9E2 BD                 CMP     L
C9E3 7E                 MOV     A,M
C9E4 C2ECC9             JNZ     LSTP1
C9E7 3A1C00             LDA     LSTPB
C9EA 3D                 DCR     A
C9EB 6F                 MOV     L,A
C9EC 23         LSTP1:  INX     H
C9ED 2200D0             SHLD    LSTP

                ;THE SERVICE ROUTINE LSBY ADDRESS, IN A, IS MOVED
                ;INTO L AND THE MSBY OF THE SERVICE ROUTINE
                ;ADDRESS IS LOADED INTO H

C9F0 6F                 MOV     L,A
C9F1 26CA               MVI     H,SRAH

                ;BRANCH TO THE SELECTED SERVICE ROUTINE
C9F3 E9                 PCHL
```

```
;*************************************************

;TYPE 1 SERVICE ROUTINE

;WHEN ENTERED, B CONTAINS THE TIME, C CONTAINS THE
;PROBE CONVERTED VALUE, D:E CONTAIN THE PROBE DATA
;AREA FIRST ENTRY ADDRESS (LTIME).
;THE CHANGE IT  TIME AND VALUE ARE COMPUTED
;THE CHANGE IN VALUE (DV) AND THE CHANGE IN TIME
;(DT) ARE COMPUTED.
;DV IS COMPARED WITH A SIGNIFICANT CHANGE AND DT IS
;COMPARED WITH ITS MAXIMUM VALUE AND A DATA BYTE IS
;SAVED IN THE DATA PAGE AREA IF NECESSARY.
;AFTER 15 DATA BYTES ARE SAVED, THE NEXT DT AND THE
;PROBE VALUE ARE SAVED AS  THE LAST TWO DATA BYTES.

;*************************************************


          ;THE PROBE DATA AREA FIRST WORD ADDRESS IS
          ;PLACED IN H:L

CA00                ORG     $+0CH
CA00 EB     SR1:    XCHG

          ;DT IS COMPUTED

CA01 78             MOV     A,B
CA02 96             SUB     M
CA03 F209CA         JP      SR1PT

          ;IF NEGATIVE, DT IS MADE POSITIVE

CA06 2F             CMA
CA07 C601           ADI     1

          ;THE DV BITS OF THE DATA BYTE (BITS 6&7 OF DT) ARE
          ;CONDITIONED AND THE DATA BYTE IS SAVED IN D

CA09 F6C0   SR1PT:  ORI     11000000B
CA0B 57             MOV     D,A

          ;DV IS COMPUTED AND H:L IS INCREMENTED TO POINT
          ;TO (LVAL) IN THE PROBE DATA AREA

CA0C 79             MOV     A,C
CA0D 23             INX     H
CA0E 96             SUB     M
CA0F F219CA         JP      SR1PV
```

```
                ;IF NEGATIVE, DV IS MADE POSITIVE

CA12 2F                 CMA
CA13 C601               ADI       1
CA15 5F                 MOV       E,A
CA16 C31ECA             JMP       SR1SG

                ;THE MSB OF THE DATA BYTE IS CLEARED TO INDICATE
                ;THAT DV IS POSITIVE

CA19 5F         SR1PV:  MOV       E,A
CA1A 3E7F               MVI       A,01111111B
CA1C A2                 ANA       D
CA1D 57                 MOV       D,A

                ;DV IS COMPARED WITH THE MINIMUM SIGNIFICANT CHANGE
                ;OF 1.2% OF PROBE FULL SCALE

CA1E 3E03       SR1SG:  MVI       A,3
CA20 BB                 CMP       E
CA21 D232CA             JNC       SR1ST

                ;NO SIGNIFICANT CHANGE HAS OCCURRED, BIT6 OF THE
                ;DATA BYTE IS CLEARED AND DT IS TESTED FOR ITS
                ;MAXIMUM VALUE

CA24 3E3F               MVI       A,00111111B
CA26 A2                 ANA       D
CA27 FE3F               CPI       00111111B

                ;IF DV IS NOT SIGNIFICANT AND DT IS NOT MAXIMUM,
                ;RETURN TO THE SEQUENCER

CA29 DA4DC9             JC        S1

                ;A DATA BYTE MUST BE STORED
                ;SAVE DT

CA2C 57                 MOV       D,A

                ;UPDATE LVAL AND LTIME

CA2D 71                 MOV       M,C
CA2E 2B                 DCX       H
CA2F 70                 MOV       M,B
CA30 23                 INX       H
CA31 23                 INX       H
```

```
              ;GET THE  WORD COUNT  (WORD 3 OF THE DATA PAGE AREA
              ;AND TEST FOR LAST WORD

CA32 23       SR1ST:   INX       H
CA33 7E                MOV       A,M
CA34 3D                DCR       A
CA35 CA44CA            JZ        SR1LW

              ; THIS IS NOT THE LAST WORD
              ; UPDATE WRDCT

CA38 77       SR1S:    MOV       M,A

              ;GET  NEXT  IN H:L (SAVE THE OLD L) AND STORE THE
              ;DATA BYTE

CA39 23                INX       H
CA3A 45                MOV       B,L
CA3B 6E                MOV       L,M
CA3C 72                MOV       M,D
CA3D 23                INX       H

              ;UPDATE  NEXT

CA3E 5D                MOV       E,L
CA3F 68                MOV       L,B
CA40 71                MOV       M,C

              ;RETURN TO THE SEQUENCER

CA41 C34DC9            JMP       S1

              ; STORE THE LAST DATA WORD AND RESET (WORD COUNT)

CA44 360F     SR1LW:   MVI       M,15

              ;GET NEXT

CA46 23                INX       H
CA47 5E                MOV       E,M

              ;RESET NEXT

CA48 7B                MOV       A,E
CA49 D610              SUI       16
CA4B 77                MOV       M,A
```

```
         ;PLACE NEXT IN L (SAVE OLD L)

CA4C 45             MOV     B,L
CA4D 6B             MOV     L,E

         ;STORE DT AT  NEXT

CA4E 3E3F           MVI     A,00111111B
CA50 E602           ANI     D
CA52 77             MOV     M,A
CA53 23             INX     H

         ;STORE PROBE VALUE AT  NEXT+1

CA54 71             MOV     M,C

         ; PLACE DATA BYTE 1 ADDRESS (FIRST WORD AFTER PROBE
         ;ID) IN H:L

CA55 3EEF           MVI     A,-17
CA57 85             ADD     L
CA58 6F             MOV     L,A

         ;JUMP TO THE PAGE TRANSFER ROUTINE

CA59 C30BCB         JMP     PGXF
```

```
;*************************************************

;TYPE 2 SERVICE ROUTINE

;WHEN ENTERED, B CONTAINS THE TIME, C CONTAINS THE
;PROBE CONVERTED VALUE AND D:E CONTAIN THE PROBE DATA
;AREA FIRST ENTRY ADDRESS (LTIME)
;THE ZONE AND CHANGE IN TIME ARE COMPUTED.
;THE CURRENT ZONE IS CHECKED FOR A CHANG IN ZONE
;FROM THE LAST ZONE STORED (LZ) AND THE CHANGE IN
;TIME (DT) IS CHECKED AGAINST ITS MAXIMUM VALUE AND
;A DATA BYTE IS SAVED IN THE DATA PAGE IF NECESSARY.

;*************************************************


;THE DATA PAGE AREA FIRST WORD ADDRESS (LTIME) IS
;PLACED IN H:L.

CA5C EB         SR2:      XCHG

;THE ZONE (MODULO 32 OF C LEFT JUSTIFIED) IS
;COMPUTED

CA5D 79                   MOV       A,C
CA5E E6E0                 ANI       11100000B
CA60 5F                   MOV       E,A

;DT IS COMPUTED

CA61 78                   MOV       A,B
CA62 96                   SUB       M

;IF NEGATIVE, DT IS MADE POSITIVE

CA63 F269CA               JP        SR2PT
CA66 2F                   CMA
CA67 C601                 ADI       1

;THE ZONE BITS OF THE DATA BYTE (BITS 5,6&7 OF DT)
;ARE CLEARED AND DT SAVED IN D

CA69 E61F       SR2PT:    ANI       00011111B
CA6B 57                   MOV       D,A

;THE ZONE (IN E) IS COMPARED WITH THE LAST ZONE
;SAVED  LZ  OF THE DATA PAGE AREA  AND A DATA BYTE
;PREPARED IF THE ZONE HAS CHANGED

CA6C 7B                   MOV       A,E
CA6D 23                   INX       H
CA6E BE                   CMP       M
CA6F C279CA               JNZ       SR2DS
```

```
                ;THE ZONE DID NOT CHANGE. DT IS TESTED FOR IT'S
                ;MAXIMUM VALUE.

CA72 3E1F              MVI      A,00011111B
CA74 BA                CMP      D

                ;THE ZONE HAS NOT CHANGED AND IF DT IS NOT MAXIMUM,
                ;RETURN TO THE SEQUENCER

CA75 DA4DC9            JC       S1

                ;PRODUCE A DATA BYTE

CA78 7B                MOV      A,E
CA79 B2         SR2DS: ORA      D

                ;UPDATE  LZ  AND  LTIME
CA7A 73                MOV      M,E
CA7B 2B                DCX      H
CA7C 70                MOV      M,B
CA7D 23                INX      H

                ; NEXT  IS MOVED INTO H:L (SAVE THE OLD L)

CA7E 23                INX      H
CA7F 55                MOV      D,L
CA80 6E                MOV      L,M
CA81 6B                MOV      L,E

                ;STORE THE DATA BYTE IN THE DATA PAGE POINTED TO BY
                ;H: NEXT

CA82 77                MOV      M,A

                ;UPDATE THE  WORD COUNT  AND TEST FOR LAST WORD

CA83 6A                MOV      L,D
CA84 23                INX      H
CA85 7E                MOV      A,M
CA86 3D                DCR      A

                ;IF THAT WAS THE LAST WORD, GO TO SR2LW AND PREPAIR
                ;FOR A PAGE TRANSFER

CA87 CA91CA            JZ       SR2LW

                ;UPDATE THE  WORD COUNT

CA8A 77                MOV      M,A
```

```
             ;UPDATE  NEXT

CA8B 2B              DCX      H
CA8C 1C              INR      E
CA8D 73              MOV      M,E

             ;RETURN TO THE SEQUENCER

CA8E C34DC9          JMP      S1

             ;THE LAST WORD WAS STORED. RESET  WORD COUNT  AND
             ; NEXT

CA91 3611    SR2LW:  MVI      M,17
CA93 2B              DCX      H
CA94 7B              MOV      A,E
CA95 D610            SUI      16
CA97 77              MOV      M,A

             ;PLACE DATA BYTE 1 ADDRESS (FIRST WORD AFTER PROBE
             ;ID) IN D:E

CA98 6F              MOV      L,A

             ;JUMP TO PAGE TRANSFER ROUTINE

CA99 C30BCB          JMP      PGXF
```

```
;*************************************************

;TYPE 3 SERVICE ROUTINE

;WHEN ENTERED, B CONTAINS THE TIME, C CONTAINS THE
;PROBE CONVERTED VALUE, D:E CONTAIN THE PROBE DATA
;AREA FIRST ENTRY ADDRESS (LTIME)
;THE CHANGE IN VALUE (DV) AND THE CHANGE IN TIME
;(DT) ARE COMPUTED
;DV IS COMPARED WITH A SIGINFICANT CHANGE AND DT IS
;COMPARED WITH ITS MAXIMUM VALUE AND A DATA BYTE IS
;SAVED IN THE DATA PAGE IF NECESSARY
;AFTER 9 DATA WORDS ARE SAVED, THE NEXT DT AND THE
;PROBE VALUE ARE SAVED AS THE LAST TWO DATA BYTES.

;*************************************************


;THE DATA PAGE AREA FIRST WORD ADDRESS (LTIME) IS
;PLACED IN H:L

CA9C EB      SR3:     XCHG

                ;DT IS COMPUTED

CA9D 78               MOV     A,B
CA9E 96               SUB     M
CA9F F2A5CA           JP      SR3PT

                ;IF NEGATIVE, DT IS MADE POSITIVE

CAA2 2F               CMA
CAA3 C601             ADI     1

                ;THE DV BITS OF THE DATA BYTE (BITS 6&7 OF DT) ARE
                ;CONDITIONED AND THE DATA BYTE IS SAVED IN D

CAA5 F680    SR3PT:   ORI     10000000B
CAA7 57               MOV     D,A

                ;DV IS COMPUTED AND H:L IS INCREMENTED TO POINT TO
                ;(LVAL)

CAA8 79               MOV     A,C
CAA9 23               INX     H
CAAA 96               SUB     M
CAAB F2B5CA           JP      SR3PV

                ;IF NEGATIVE, DV IS MADE POSITIVE
```

AD-A064 725 AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OHIO SCH--ETC F/G 9/2

AIRCREW MODULARIZED INFLIGHT DATA ACQUISITION SYSTEM.(U)

DEC 78 R E HILL

UNCLASSIFIED AFIT/GE/EE/78-28 NL

3 OF 3

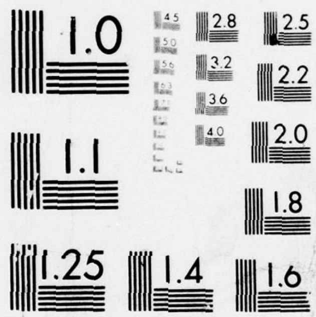
AD A064725

END

DATE FILMED

4 --79

DDC



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

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CAAE 2F              CMA
CAAF C6Ø1            ADI     1
CAB1 5F              MOV     E,A
CAB2 C3BBCA          JMP     SR3SG

          ;THE MSB OF THE TIME BYTE IS CLEARED TO INDICATE
          ;THAT DV IS POSITIVE

CAB5 5F      SR3PV:  MOV     E,A
CAB6 3E7F            MVI     A,Ø1111111B
CAB8 A2              ANA     D
CAB9 57              MOV     D,A
CABA 7B              MOV     A,E

          ;DV IS COMPARED WITH THE MINIMUM SIGNIFICANT CHANGE
          ;OF 1.2% OF PROBE FULL SCALE

CABB 3EØ3    SR3SG:  MVI     A,3
CABD BB              CMP     E
CABE D2CDCA          JNC     SR3ST

          ;NO SIGNIFICANT CHANGE HAS OCCURRED, BIT6 OF THE
          ;DATA BYTE IS CLEARED AND DT IS TESTED FOR ITS
          ;MAXIMUM VALUE

CAC1 3E7F            MVI     A,Ø1111111B
CAC3 A2              ANA     D
CAC4 FE7F            CPI     Ø1111111B

          ;IF DV IS NOT SIGNIFICANT AND DT IS NOT MAXIMUM,
          ;RETURN TO THE SEQUENCER

CAC6 DA4DC9          JC      S1

          ;A DATA BYTE MUST BE STORED
          ;UPDATE (LVAL)

CAC9 71              MOV     M,C

          ;UPDATE (LTIME)

CACA 2B              DCX     H
CACB 7Ø              MOV     M,B
CACC 23              INX     H

          ;A DATA BYTE MUST BE STORED. IF IT IS THE LAST WORD
          ;GO TO SR3LW

CACD 23      SR3ST:  INX     H
CACE 7E              MOV     A,M
CACF 3D              DCR     A
CADØ CAF7CA          JZ      SR3LW
```

```
                    ;IT IS NOT THE LAST WORD SO UPDATE THE  WORD COUNT

CAD3 77                     MOV     M,A

                    ;CHECK IF THIS IS AN EVEN DATA WORD, IF SO GO TO
                    ;SR3WE

CAD4 EAE6CA                 JPE     SR3WE

                    ;THE WORD IS ODD SO MAKE A LEFT JUSTIFIED 4 BIT DV

CAD7 3E0F                   MVI     A,00001111B
CAD9 A3                     ANA     E
CADA 07                     RLC
CADB 07                     RLC
CADC 07                     RLC
CADD 07                     RLC

                    ;STORE DV IN  NEXT

CADE 23                     INX     H
CADF 6E                     MOV     L,M
CAE0 77                     MOV     M,A

                    ;STORE DT IN  NEXT-1

CAE1 2B                     DCX     H
CAE2 72                     MOV     M,D

                    ;CONTROL IS RETURNED TO THE SEQUENCER

CAE3 C34DC9                 JMP     S1

                    ;AN EVEN DATA WORD IS TO BE MADE. MAKE DV A RIGHT
                    ;JUSTIFIED 4 BIT WORD

CAE6 3E0F           SR3WE:  MVI     A,00001111B
CAE8 A3                     ANA     E

                    ;DV IN E IS ORED WITH THE LAST DV STORED IN THE
                    ;DATA PAGE (SAVE THE OLD L)

CAE9 23                     INX     H
CAEA 45                     MOV     B,L
CAEB 6E                     MOV     L,M
CAEC B6                     ORA     M
CAED 77                     MOV     M,A

                    ;DT IS STORED IN  NEXT+1

CAEE 23                     INX     H
CAEF 72                     MOV     M,D
```

```
               ; NEXT  IS UPDATED

CAF0 23                 INX      H
CAF1 4D                 MOV      C,L
CAF2 68                 MOV      L,B
CAF3 71                 MOV      M,C

               ;CONTROL IS RETURNED TO THE SEQUENCER

CAF4 C34DC9             JMP      S1

               ;THE LAST WORD IS TO BE STORED. ACTUAL VALUE IS
               ;STORED IN PLACE OF DV. FIRST  WORD COUNT  IS RESET

CAF7 3609      SR3LW:   MVI      M,9

               ;MOVE  NEXT  IN H:L

CAF9 23                 INX      H
CAFA 45                 MOV      B,L
CAFB 6E                 MOV      L,M

               ;STORE DT AT  NEXT+2

CAFC 23                 INX      H
CAFD 23                 INX      H
CAFE 72                 MOV      M,D

               ;PROBE VALUE IS STORED IN  NEXT+3

CAFF 23                 INX      H
CB00 71                 MOV      M,C

               ; NEXT  IS RESET

CB01 7D                 MOV      A,L
CB02 68                 MOV      L,B
CB03 D60F               SUI      15
CB05 77                 MOV      M,A

               ; NEXT  IS PLACED IN L

CB06 6F                 MOV      L,A

               ;H:L IS SET TO POINT TO THE FIRST DATA BYTE AFTER
               ;PROBE ID

CB07 2B                 DCX      H

               ;JUMP TO PAGE TRANSFER ROUTINE

CB08 C30BCB             JMP      PGXF
```

```
;*************************************************

;PAGE TRANSFER ROUTINE

;PGXF SELECTS AND INITIALIZES THE BUBBLE MODULE
;DATA BYTES ARE TRANSFERRED FROM THE PROPER DATA
;PAGE TO THE        CONTROLLER AND THEN TO THE
;BUBBLE. THE PAGE COUNT (MBPCT) AND THE BUBBLE
;SELECT MASK (MBSM) ARE UPDATED
;THE AUTO POWER DOWN CIRCUIT SENDS A PULSE TO
;THE POWER DOWN REGISTER (MBPDR) 15 MSEC AFTER
;THE CONTROLLER ISSUES AN INTERRUPT. THIS
;INSURES THAT THE CONTROLLER IS FINISHED AND
;AN ORDERLY SHUTDOWN OCCURRED.

;*************************************************


            ;ENABLE AUTO POWER DOWN

CB0B AF     PGXF:   XRA     A
CB0C D370           OUT     PFFR

            ;GET THE        SELECT MASK AND SEND IT TO THE
            ;BUBBLE MODULE SELECT REGISTER  MBPUR

CB0E 3A04D0         LDA     BSMSK
CB11 D350           OUT     MBPUR

            ;GET PAGE COUNT FROM  MBPCT  AND LOAD THE MAGNETIC
            ;BUBBLE CONTROLLER PAGE SELECT REGISTERS (MBPS1 &
            ;MBPS2).

CB13 3A02D0         LDA     MBPCT
CB16 D31F           OUT     MBPS1
CB18 3A03D0         LDA     MBPCT+1
CB1B D31E           OUT     MBPS2

            ;SEND THE PROBE ID TO THE CONTROLLER FIFO

CB1D 7E             MOV     A,M
CB1E D31B           OUT     MBFWR

            ;SEND THE NEXT 17 DATA BYTES TO THE FIFO AND CLEAR
            ;EACH LOCATION AFTER THE TRANSFER

CB20 23     MORE1:  INX     H
CB21 7E             MOV     A,M
CB22 D31B           OUT     MBFWR
CB24 AF             XRA     A
CB25 77             MOV     M,A
CB26 05             DCR     B
CB27 C220CB         JNZ     MORE1
```

```
            ;TRANSFER FIFO TO BUBBLE

CB2A 3E04           MVI     A,MBPTB
CB2C D31D           OUT     MBCCR

            ;IF THIS IS NOT THE LAST PAGE IN THE BUBBLE, SELECT
            ;THE NEXT PAGE AND RETURN TO THE SEQUENCER.

CB2E 2A02D0 PGXF3:  LHLD    MBPCT
CB31 23             INX     H
CB32 2202D0         SHLD    MBPCT
CB35 3E02           MVI     A,2
CB37 BC             CMP     H
CB38 C24DC9         JNZ     S1
CB3B 3E82           MVI     A,130
CB3D BD             CMP     L
CB3E C24DC9         JNZ     S1

            ;THE LAST PAGE WAS USED.
            ;SHUT DOWN THE POWER TO IFPDAS

CB41 3EFF           MVI     A,0FFH
CB43 D340           OUT     PWOFF

            ;SIMULATE IFPDAS HALTED

CB45 D3D6           OUT     LED
CB47 2107FF         LXI     H,0FF07H
CB4A 2D             DCR     L
CB4B C24ACB         JNZ     $-1
CB4E 25             DCR     H
CB4F C24ECB         JNZ     $-1
CB52 C345CB         JMP     $-13
```

```
            ;*************************************************
            ;INTERRUPT JUMP TABLE
            ;*************************************************

CBE0                    ORG     $+8BH

            ;RESET MONITOR BAUD RATE

CBE0 C3DA03             JMP     03DAH
CBE3 00                 NOP

            ;START IFFDAS

CBE4 C300C8             JMP     HWI
CBE7 00                 NOP

            ;RETURN TO MONITOR

CBE8 CF                 RST     1
CBE9 0000               DW      0
CBEB 00                 DB      0

            ;COUNTER 0 INTERRUPT

CBEC C34DC9             JMP     S1
CBEF 00                 NOP

            ;DATA STORAGE INITIALIZE

CBF0 C384C8             JMP     DSIP
CBF3 00                 NOP

            ;BUBBLE DATA DUMP

CBF4 C358CC             JMP     MBDP
CBF7 00                 NOP

            ;NOT USED

CBF8 CF                 RST     1
CBF9 0000               DW      0
CBFB 00                 DB      0

            ;BUBBLE CLEAR

CBFC C3A6CC             JMP     MBCL
CBFF 00                 NOP

            ;END OF INTERRUPT TABLE
```

```
;***********************************************
;INITIALIZATION LIST
;***********************************************

CCØØ Ø8          DB      Ø8H    ;NUMBER OF PROBES

        ;START OF TYPE 1 PROBE INITIALIZATION

CCØ1 44          DB      44H    ;ABSOLUTE PRESSURE MUX
CCØ2 4839        DW      3948H  ;DATA PAGE AREA ADDR
CCØ4 ØØ          DB      ØØH    ;END OF TYPE 1

        ;START OF TYPE 2 PROBE INITIALIZATION

CCØ5 45          DB      45H    ;GX MUX
CCØ6 6Ø39        DW      396ØH  ;DATA PAGE AREA ADDR
CCØ8 46          DB      46H    ;GY MUX
CCØ9 7839        DW      3978H  ;DATA PAGE AREA ADDR
CCØB 47          DB      47H    ;GZ MUX
CCØC 9Ø39        DW      399ØH  ;DATA PAGE AREA ADDR
CCØE ØØ          DB      ØØH    ;END OF TYPE 2

        ;START OF TYPE 3 INITIALIZATION

CCØF Ø1          DB      Ø1H    ;PSR O2 IN MUX
CC1Ø ØØ39        DW      39ØØH  ;DATA PAGE AREA ADDR
CC12 Ø2          DB      Ø2H    ;PSR O2 OUT MUX
CC13 1839        DW      3918H  ;DATA PAGE AREA ADDR
CC15 Ø3          DB      Ø3H    ;FLOW RATE MUX
CC16 3Ø39        DW      393ØH  ;DATA PAGE AREA ADDR
CC18 ØØ          DB      ØØH    ;END OF TYPE 3

        ;HEART RATE INITIALIZATION

CC19 A839        DW      39A8H  ;DATA PAGE AREA ADDR
CC1B ØØ          DB      ØØH    ;INITIALIZATION LIST END


;***********************************************
;SEQUENCER LIST
;***********************************************

CC1C Ø1          DB      Ø1H    ;PSR O2 IN MUX
CC1D ØØ39        DW      39ØØH  ;DATA PAGE AREA ADDR
```

```
CC1F 02          DB     02H    ;PSR O2 OUT MUX
CC20 1839        DW     3918H  ;DATA PAGE AREA ADDR
CC22 03          DB     03H    ;FLOW RATE MUX
CC23 3039        DW     3930H  ;DATA PAGE AREA ADDR
CC25 60          DB     60H    ;HEART RATE MUX
CC26 A839        DW     39A8H  ;DATA PAGE AREA ADDR

           ;END OF MINOR SEQUENCE LOOP 1

CC28 01          DB     01H    ;PSR O2 IN MUX
CC29 0039        DW     3900H  ;DATA PAGE AREA ADDR
CC2B 02          DB     02H    ;PSR O2 OUT MUX
CC2C 1839        DW     3918H  ;DATA PAGE AREA ADDR
CC2E 03          DB     03H    ;FLOW RATE MUX
CC2F 3039        DW     3930H  ;DATA PAGE AREA ADDR
CC31 44          DB     44H    ;ABSOLUTE PSR MUX
CC32 4839        DW     3948H  ;DATA PAGE AREA ADDR

           ;END OF MINOR SEQUENCE LOOP 2

CC34 01          DB     01H    ;PSR O2 IN MUX
CC35 0039        DW     3900H  ;DATA PAGE AREA ADDR
CC37 02          DB     02H    ;PSR O2 OUT MUX
CC38 1839        DW     3918H  ;DATA PAGE AREA ADDR
CC3A 03          DB     03H    ;FLOW RATE MUX
CC3B 3039        DW     3930H  ;DATA PAGE AREA ADDR
CC3D 45          DB     45H    ;GX MUX
CC3E 6039        DW     3960H  ;DATA PAGE AREA ADDR

           ;END OF MINOR SEQUENCE LOOP 3

CC40 01          DB     01H    ;PSR O2 IN MUX
CC41 0039        DW     3900H  ;DATA PAGE AREA ADDR
CC43 02          DB     02H    ;PSR O2 OUT MUX
CC44 1839        DW     3918H  ;DATA PAGE AREA ADDR
CC46 03          DB     03H    ;FLOW RATE MUX
CC47 3039        DW     3930H  ;DATA PAGE AREA ADDR
CC49 46          DB     46H    ;GY MUX
CC4A 7839        DW     3978H  ;DATA PAGE AREA ADDR

           ;END OF MINOR SEQUENCE LOOP 4

CC4C 01          DB     01H    ;PSR O2 IN MUX
CC4D 0039        DW     3900H  ;DATA PAGE AREA ADDR
CC4F 02          DB     02H    ;PSR O2 OUT MUX
CC50 1839        DW     3918H  ;DATA PAGE AREA ADDR
CC52 03          DB     03H    ;FLOW RATE MUX
CC53 3039        DW     3930H  ;DATA PAGE AREA ADDR
CC55 47          DB     47H    ;GZ MUX
CC56 9039        DW     3990H  ;DATA PAGE AREA ADDR
```

```
;**************************************************

;BUBBLE DATA DUMP

;THIS ROUTINE IS ENTERED FROM THE MBDP (LEVEL 5)
;INTERRUPT AND TRANSFERS ALL 641 BUBBLE PAGES TO
;A HAZELTINE 2000 TERMINAL AND CASETTE RECORDER.
;EACH PAGE CONTAINS 18 DATA BYTES
;IF THE FIRST BYTE OF THE PAGE (PROBE ID) IS ZERO,
;IT IS ASSUMED THAT NO MORE BUBBLE PAGES CONTAIN
;DATA.

;**************************************************



;INITIALIZE THE BUBBLE SELECT MASK  BSMSK

CC58 3E01    MBDP:    MVI     A,1
CC5A D350    MBDP9:   OUT     MBPUR
CC5C 3204D0           STA     BSMSK

;SELECT PAGE ZERO AND SINGLE PAGE TRANSFER MODE

CC5F AF               XRA     A
CC60 D31F             OUT     MBPS1
CC62 D31E             OUT     MBPS2
CC64 3202D0           STA     MBPCT
CC67 3203D0           STA     MBPCT+1

;TRANSFER A PAGE FROM THE BUBBLE

CC6A 3E02    MBDP7:   MVI     A,MBPTF
CC6C D31D             OUT     MBCCR

;LOOP UNTIL THE CONTROLLER IS FINISHED THE PAGE
;TRANSFER.

CC6E         MBDP4:

;THIS ROUTINE TESTS THE MAGNETIC BUBBLE CONTROLLER
;STATUS TO DETECT WHEN THE CONTROLLER IS FINISHED
;EXECUTION.

;TIME FILLER

CC6E 00               NOP

;GET THE CONTROLLER STATUS

CC6F DB1A             IN      MBSR
```

```
                ;TEST THE IDLE BIT

CC71 E620           ANI     MBIM

                ;GET NEW STATUS IF BUSY

CC73 C26FCC         JNZ     $-4

                ;SET UP FOR 18 DATA BYTE TRANSFERS TO THE CONSOLE

CC76 1611           MVI     D,17

                ;GET THE FIRST DATA BYTE AND SEND IT TO THE CONSOLE
                ;IF IT IS NOT ZERO. IF IT IS ZERO, GO TO MBDPE

CC78 DB1C           IN      MBFRR
CC7A A7             ANA     A
CC7B CAA1CC         JZ      MBDPE
CC7E CDF0CC         CALL    DTOUT

                ;GET 17 MORE DATA BYTES AND TRANSFER THEM TO THE
                ;CONSOLE.

CC81 DB1C   MBDP6:  IN      MBFRR
CC83 CDF0CC         CALL    DTOUT
CC86 15             DCR     D
CC87 C281CC         JNZ     MBDP6

                ;IF MORE PAGES REMAIN IN THE BUBBLE, SELECT THE
                ;NEXT PAGE AND CONTINUE THE TRANSFER. IF NO MORE
                ;PAGES REMAIN, STOP AND POWER DOWN THE BUBBLE
CC8A 3A02D0         LDA     MBPCT
CC8D FE81           CPI     129
CC8F 5F             MOV     E,A
CC90 C2A1CC         JNZ     MBDPE
CC93 3A03D0         LDA     MBPCT+1
CC96 FE02           CPI     2
CC98 CAA1CC         JZ      MBDPE
CC9B 3A04D0         LDA     BSMSK
CC9E C35ACC         JMP     MBDP9
CCA1 D360   MBDPE:  OUT     MBPDR

                ;RETURN TO THE MONITOR

CCA3 C33C00         JMP     03CH
```

```
;************************************************

;BUBBLE PAGES CLEAR

;THIS ROUTINE IS ENTERED FROM THE MBCL INTERRUPT
;(LEVEL 7) AND SETS ALL BUBBLE BYTES TO ZERO.
;WHEN FINISHED, CONTROL IS RETURNED TO THE
;MONITOR

;************************************************



;THE FIRST BUBBLE MODULE IS SELECTED AND THE
;MASK IS SAVED IN BSMSK

CCA6 3E01   MBCL:   MVI     A,1
CCA8 D350           OUT     MBPUR
CCAA 3204D0 MBCLA:  STA     BSMSK

;SELECT PAGE ZERO AND CLEAR THE PAGE COUNTER

CCAD AF             XRA     A
CCAE D31F           OUT     MBPS1
CCB0 D31E           OUT     MBPS2
CCB2 3202D0         STA     MBPCT
CCB5 3203D0         STA     MBPCT+1

;SEND 18 ZERO WORDS TO THE CONTROLLER FIFO

CCB8 0612   MBCL8:  MVI     B,18
CCBA D31B           OUT     MBFWR
CCBC 05             DCR     B
CCBD C2BACC         JNZ     $-3

;TRANSFER THE FIFO TO THE BUBBLE

CCC0 3E04           MVI     A,MBPTB
CCC2 D31D           OUT     MBCCR

;LOOP UNTIL THE CONTROLLER IS FINISHED THE TRANSFER
;THIS ROUTINE TESTS THE MAGNETIC BUBBLE CONTROLLER
;STATUS TO DETECT WHEN THE CONTROLLER IS FINISHED
;EXECUTION.

;TIME FILLER

CCC4 00             NOP

;GET THE CONTROLLER STATUS

CCC5 DB1A           IN      MBSR
```

```
                ;TEST THE IDLE BIT

CCC7 E620               ANI     MBIM

                ;GET NEW STATUS IF BUSY

CCC9 C2C5CC             JNZ     $-4

                ;IF MORE PAGES REMAIN GO TO MBCL6. IF NOT, GO TO
                ;MBCL7

CCCC 3A02D0             LDA     MBPCT
CCCF FE81               CPI     129
CCD1 5F                 MOV     E,A
CCD2 C2DDCC             JNZ     MBCL6
CCD5 3A03D0             LDA     MBPCT+1
CCD8 FE02               CPI     2
CCDA CAEBCC             JZ      MBCL7

                ;SELECT THE NEXT PAGE AND CONTINUE THE CLEAR
                ;ROUTINE.

CCDD 3A03D0     MBCL6:  LDA     MBPCT+1
CCE0 57                 MOV     D,A
CCE1 13                 INX     D
CCE2 7B                 MOV     A,E
CCE3 D31F               OUT     MBPS1
CCE5 7A                 MOV     A,D
CCE6 D31E               OUT     MBPS2
CCE8 C3B8CC             JMP     MBCL8

                ;NO MORE BUBBLES REMAIN SO POWER DOWN THE BUBBLE
CCEB D360       MBCL7:  OUT     MBPDR

                ;RETURN TO THE MONITOR

CCED C33C00             JMP     03CH
```

```
                ;*************************************************

                ;SUBROUTINE DTOUT

                ;THIS SUBROUTINE MAKES TWO ASCII CHARACTERS OF
                ;A DATA BYTE AND SENDS THEM TO THE HAZELTINE
                ;2000 CONSOLE AND CASETTE RECORDER.
                ;IT IS CALLED BY BUBBLE DATA DUMP AND SPECIAL
                ;DATA PAGE DUMP

                ;*************************************************


                ;B IS SAVED ON THE STACK THEN SET TO COUNT
                ;TWO CONVERSIONS

CCF0 C5         DTOUT:  PUSH    B
CCF1 0602               MVI     B,2

                ;THE DATA BYTE IS SAVED ON THE STACK

CCF3 F5                 PUSH    PSW

                ;THE UPPER NIBBLE IS RIGHT JUSTIFIED

CCF4 0F                 RRC
CCF5 0F                 RRC
CCF6 0F                 RRC
CCF7 0F                 RRC

                ;THE UPPER NIBBLE IS CLEARED

CCF8 E60F               ANI     00FH

                ;INSURE THAT CHARACTERS A-F CAUSE A CARRY

CCFA C690               ADI     090H

                ;DECIMAL ADJUST THE ACCMULATOR

CCFC 27                 DAA

                ;ADD THE CARRY AND ADJUST THE UPPER NIBBLE

CCFD CE40               ACI     040H

                ;DECIMAL ADJUST THE ACCUMULATOR

CCFF 27                 DAA
```

```
                  ;MOVE THE ASCII CHARACTER INTO C

CD00 4F                 MOV       C,A

                  ;SEND THE CHARACTER TO THE CONSOLE WHEN THE USART
                  ;IS READY.

CD01 DBED               IN        USART
CD03 E601               ANI       READY
CD05 C201CD             JNZ       $-4
CD08 79                 MOV       A,C
CD09 D3EC               OUT       CON

                  ;GET THE DATA BYTE FROM THE STACK

CD0B F1                 POP       PSW

                  ;REPEAT THE PROCESS FOR THE SECOND NIBBLE

CD0C 05                 DCR       B
CD0D C2F8CC             JNZ       DTOUT+8

                  ;RESTORE B AND RETURN

CD10 C1                 POP       B
CD11 C9                 RET

                        END
```

VITA

Robert Edwin Hill was born on 2 February 1944 in Eugene, Oregon. He graduated from high school in Kimberly, Idaho in 1962. He attended The University of Washington, Seattle, Washington and received the degree of Bachelor of Science in Electrical Engineering and was commissioned from the Reserve Officers Training Corps program in June 1967. He immediately entered Undergraduate Pilot Training at Vance AFB, Oklahoma and received his wings in June 1968. He then served as an F-106 pilot in the 5th Fighter Interceptor Squadron, Minot, North Dakota. He flew in Viet Nam as an O2-A Forward Air Controller, instructor pilot and flight examiner with the 19th and 21st Tactical Air Support Squadrons from June 1971 to June 1972. He returned to flying the F-106 at Tyndall AFB, Florida with the 475th Test Squadron as an operational test pilot. In July 1975 he joined the Air Force Avionics Laboratory as a program manager for air-to-air gun fire control system development until entering the School of Engineering, Air Force Institute of Technology, in June 1977. He is a member of Eta Kappa Nu and Tau Beta Pi.

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A baseline design of a School of Aerospace Medicine sponsored aircrew physiology monitor was accomplished. The monitor design requirements were: four hour battery operation; 2x5x9 inch size for man-mounting; record four hours of 13 parameters with 1% accuracy; and use nonmechanical, nonvolatile data storage.

A system design study verifies the feasibility of implementing the monitor using an 8-bit digital data system containing magnetic bubble memory. The design is partitioned into four modules. The Power Module contains +5 and +12

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Block 20 - Cont'd

volt Lithium batteries and a module interface bus. The Signal Conditioner Module accomodates sensor amplifiers and a microprocessor based analog to digital converter system which amplifies and digitizes the sensor signals. The digitized signals are provided to a microprocessor based Data Manager Module which prepares data for storage. The Bubble Memory Module contains six memory locations each capable of supporting quarter or one megabit bubble memory chips.

The baseline design achieves the design goals. The monitor samples seven sensors every 50 msec with 0.4% accuracy. The six megabit memory accomodates storage of 1/3 of the data sampled during four hours. This rate is acceptable for the parameters being monitored.