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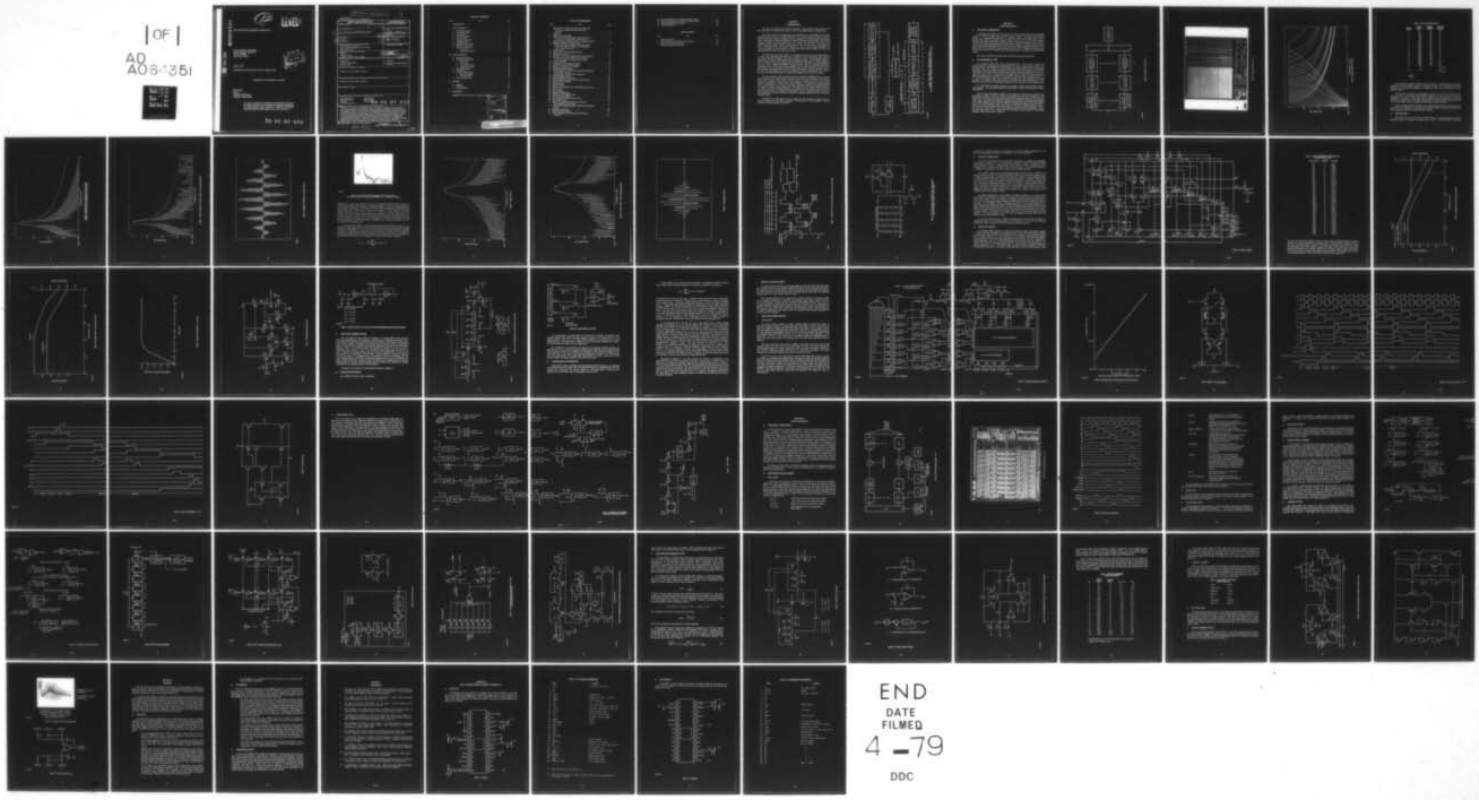

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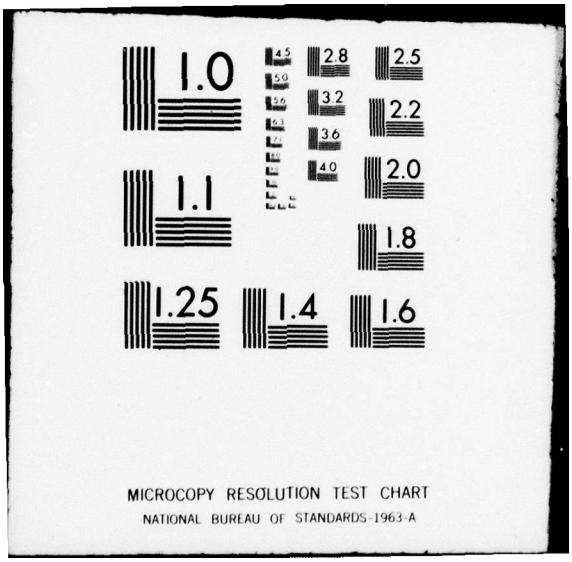
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LEVEL II

CCDs FOR SPEECH BANDWIDTH REDUCTION

Texas Instruments Incorporated
Central Research Laboratories
P.O. Box 225936
Dallas, Texas 75222

January 1979

Final Report for Period 18 April 1977–31 January 1979

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The need for security in voice communication is met by converting voice to digital form so that sophisticated digital encryption is possible. It is desirable that the digital voice signal be compatible with conventional 3-kHz analog voice transmission bands; hence, the vocoder that converts analog voice signals to digital form must employ some form of bandwidth compression to yield data rates down to 2.4 kilobits/second. Linear prediction techniques are commonly used to implement vocoders in essentially all-digital systems, but with current technology such systems are expensive, fairly large, and consume large amounts of power. This report concerns the application of CCD technology to the vocoder problem using a second, much older approach, the channel vocoder. The objective is to demonstrate the potential of analog CCD technology to achieve a low-cost, low-power vocoder system. Two custom-designed CCD/NMOS integrated circuits are the key to this approach, and the design of these circuits is detailed in this report.

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SECTION I
INTRODUCTION

The high cost of secure voice systems is presently a major problem for all branches of the DoD. This high cost severely limits the use of secure voice systems in spite of the great need.

This report concerns the initial phase of the development of a potentially low-cost, highly integrated vocoder based on the Belgard algorithm. This 2.4-kbps system is based on a channel bank approach that is highly compatible with the capabilities of monolithic filters implemented with a combination of charge-coupled devices (CCDs) and switched-capacitor filters. Two custom integrated circuits are being developed for this vocoder and they will be combined with commercial microcomputer circuits to implement the total vocoder system. This program has been a cooperative effort with Lincoln Laboratory, and the system design, simulation, and construction tasks have been performed by Lincoln. This report will concentrate only on the two analog integrated circuits to be used in the vocoder.

The function of this vocoder system is to reduce the data rate of speech transmission to 2.4 kbps while maintaining high quality and intelligibility in the reconstructed speech signal at the receiver. The block diagram of the system is shown in Figure 1. This integrated system is a channel vocoder based on the Belgard system and algorithm developed in the United Kingdom.[1] The two portions of the system enclosed in the dashed lines in the figure are being implemented with two custom designed CCD/NMOS integrated circuits, while the remaining functions are implemented with a few simple analog components and five TMS 9940 microcomputer circuits. One of these two special circuits is used for speech analysis and the other for synthesis. Three of the TMS 9940 microcomputers are used to implement a modified Gold-Rabiner pitch tracker.[2] The other two TMS 9940s control the analyzer and synthesizer and interface the modem.

The basic operation of the channel vocoder is to determine periodically (every 20 ms) the spectral envelope of the speech using a filter bank. The nature of the excitation of the speaker's voice (either a periodic pulse train for voiced sounds or a random noise source for unvoiced sounds) is determined by a pitch tracker. These parameters are encoded into a compact digital code and transmitted to the receiver which then synthesizes a signal having approximately the same spectral envelope. The synthesizer uses a filter bank excited by either a periodic pulse train or random noise where the gain parameters of the filter bank, the selection of the excitation, and the pulse period are controlled by the information from the transmitted signal. The vocoder takes advantage of the fact that phase information is relatively unimportant in man's perception of speech sounds.

In Section II of this report, the voice analysis IC will be described. Several of the key circuit techniques used will also be discussed. In Section III, the voice synthesis IC will be described. A summary appears in Section IV.

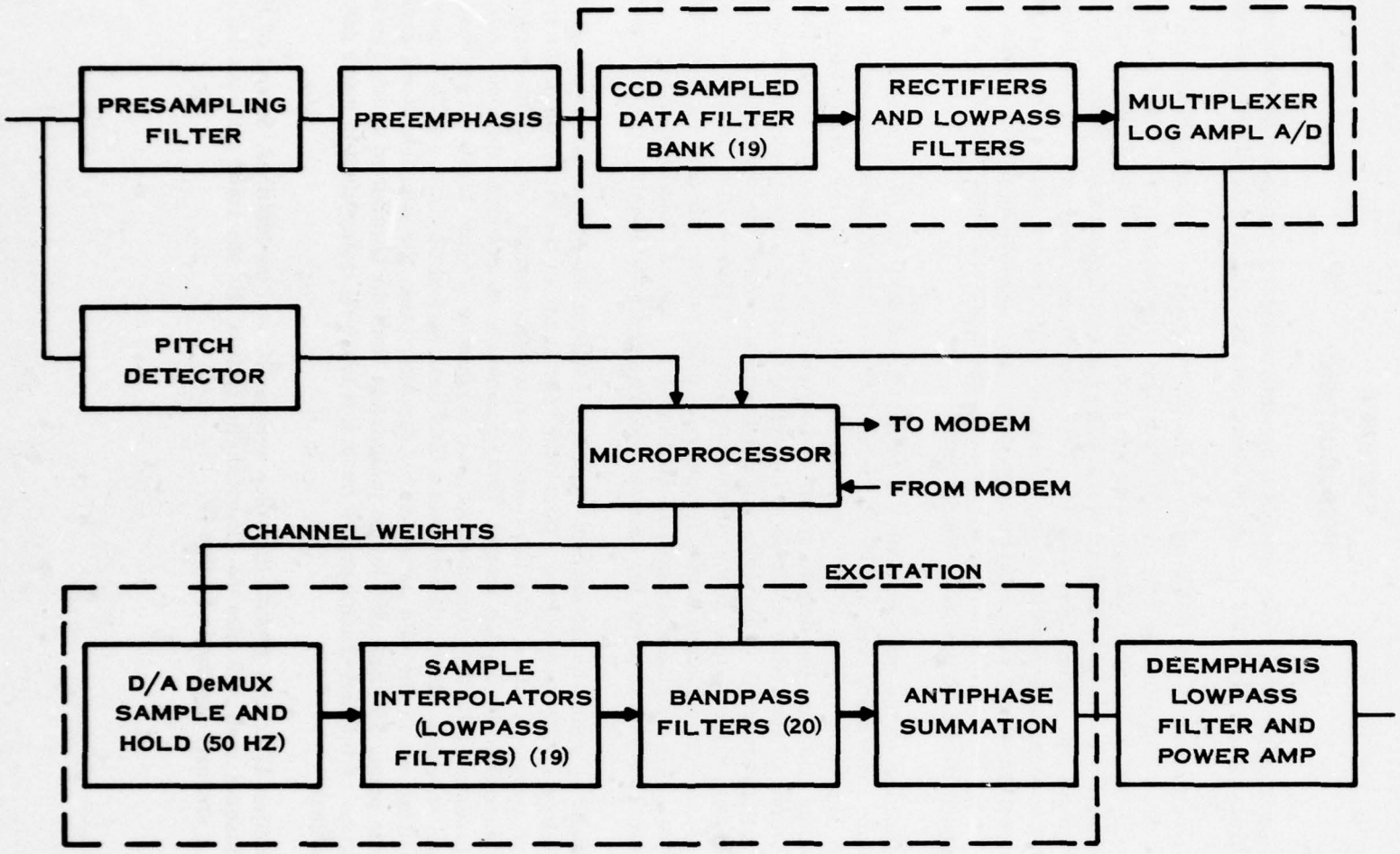

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Figure 1. Block Diagram of a Belgard Channel Vocoder
(The dashed lines enclose the analysis and synthesis ICs being developed.)

SECTION II
VOICE ANALYSIS IC

A. FUNCTIONAL DESCRIPTION

A simplified block diagram of the analyzer IC is shown in Figure 2(A), and a photograph of the IC is shown in Figure 2(B). The chip contains a bank of 19 channels. Each channel consists of a bandpass filter followed by a half-wave rectifier and low-pass filter. The 19 bandpass filters span the frequency spectrum from 180 Hz to 4.1 kHz. The ideal frequency response of the analyzer filter bank is plotted in Figure 3. Each channel output is thus a measure of the energy in the corresponding spectral range. The 19 channels are sampled once every 20 ms and then sequentially multiplexed into an A/D converter having a logarithmic response. A 5-bit digital code with 1.5-dB steps is thus generated for each of the 19 segments of the spectrum. The chip also contains the necessary clocks and timing circuitry to interface the microprocessor system.

This section describes in detail the major functional blocks of the analyzer IC.

B. CCD BANDPASS FILTERS

Early analysis indicated that CCD transversal filters[3,4,5] would provide a silicon area efficient approach to fabricating the Belgard filter bank. Table 1 shows both the analyzer and synthesizer filter center frequencies and bandwidth. The original Belgard system used recursive Butterworth filters (two complex pole pairs) that cannot be exactly matched with CCD transversal filters. As described below, the Butterworth characteristics are matched from the center of each band down to about −20 dB. Outside this region, the CCD filters will fall off much more rapidly than Butterworth characteristics, but stopband attenuation will be limited to about −50 to −60 dB. Discussions with Lincoln Laboratory indicate that these characteristics will be acceptable. The sharper filtering may perhaps be desirable and Lincoln simulations of 50-dB stopband levels prove that no performance degradation can be detected with this stopband level.

The CCD FIR filter weighting coefficients are designed using the Parks, McClellan, Rabiner design program[6] with appropriate subroutine modifications to model the Butterworth response characteristics.

Typical of the low-frequency channels are the frequency characteristics of channel 6 that are plotted in Figure 4. Both the Butterworth (smooth curve) and the 100-stage CCD FIR characteristics are shown. The FIR response matches the Butterworth within 0.4 dB in the band center, and in the stopband the ripple is weighted by the reciprocal of the Butterworth response in the design program to yield a sidelobe response somewhat below the Butterworth throughout most of the audio frequency band. The effects of weighting coefficient roundoff (which is required by the photomask fabrication equipment) can be seen by comparing Figures 4 and 5. The roundoff to the nearest of the 500 available increments results in nonuniform sidelobe structures with peaks in the −60-dB range for this filter as seen in Figure 5. The impulse response of filter 6 can be seen in Figure 6.

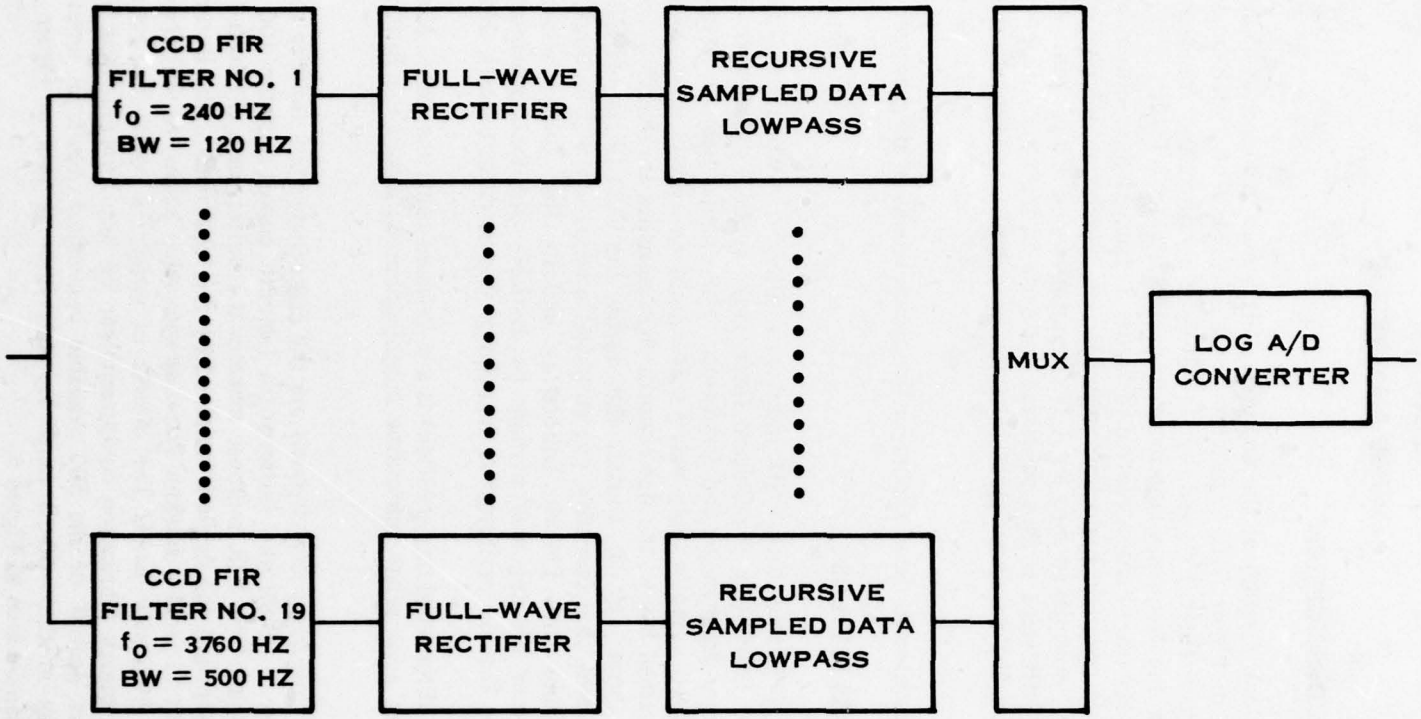

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Figure 2. Analyzer IC (Sheet 1 of 2)

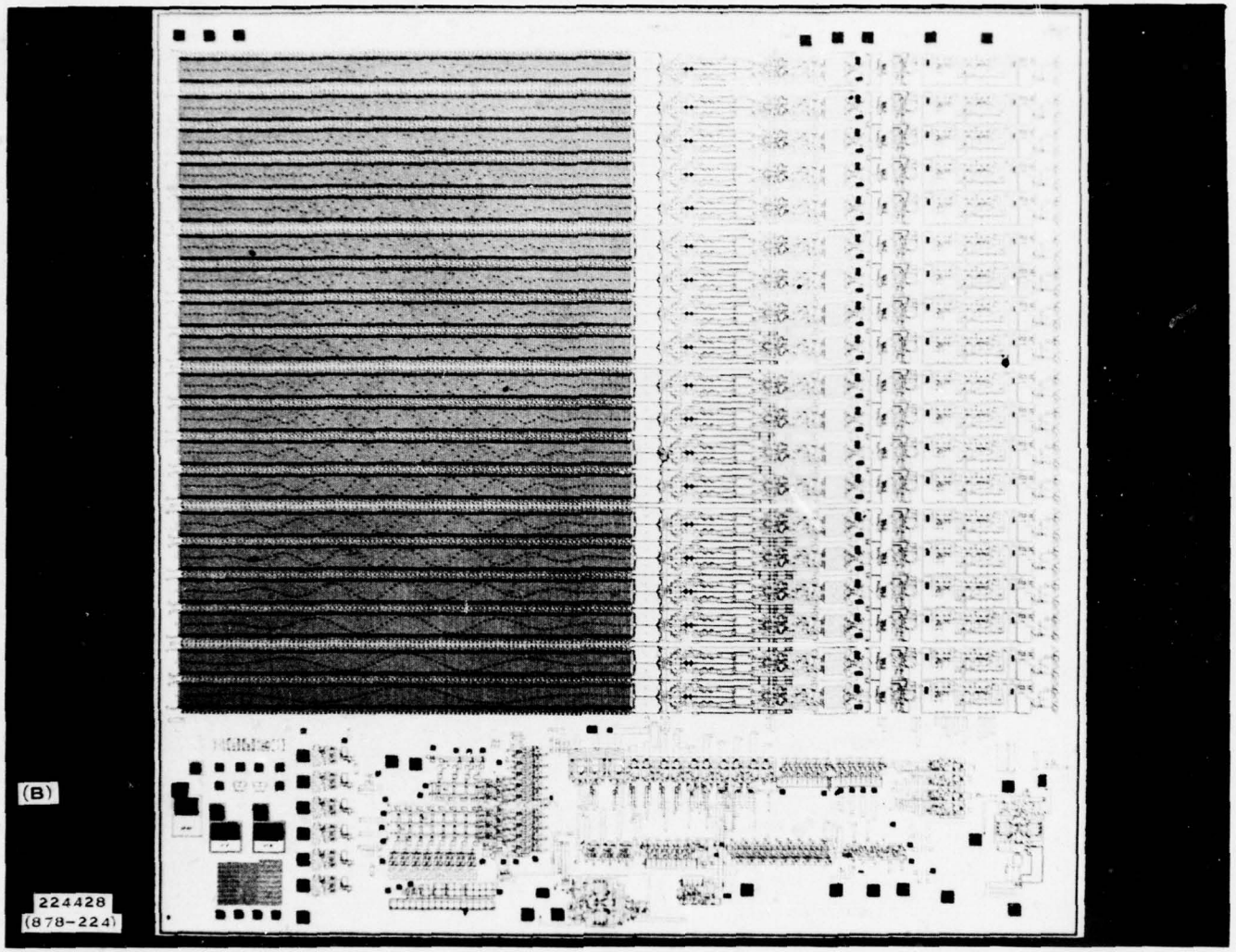

Figure 2. Analyzer IC (Sheet 2 of 2)

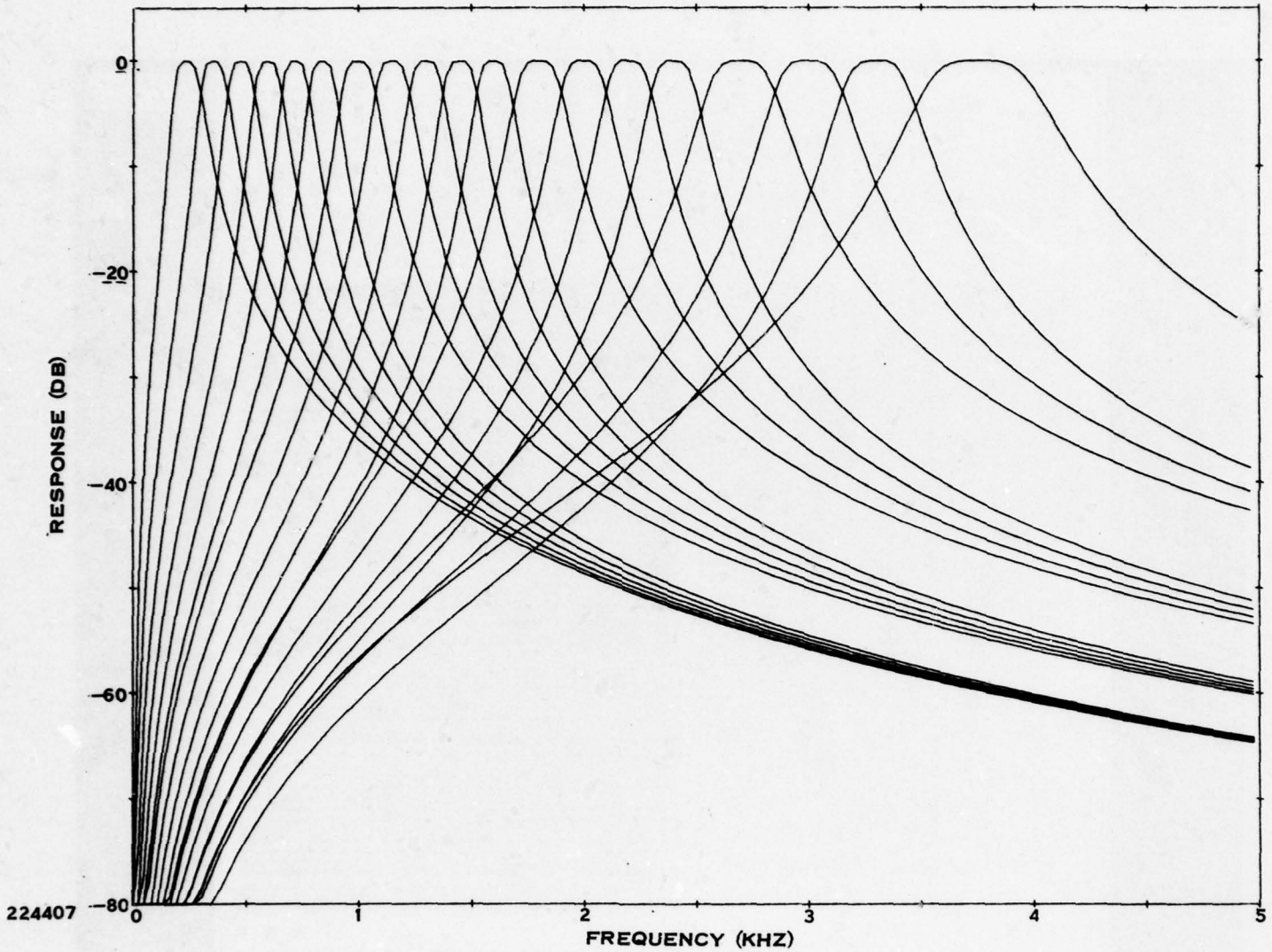

Figure 3. Belgard Analyzer Filter Bank

TABLE 1. BELGARD FILTER BANKS

Channel Number	Center Frequency (Hz)	Analyzer Bandwidth (Hz)	Synthesizer Bandwidth (Hz)
1	240	130	45
2	360	130	45
3	480	130	45
4	600	130	45
5	720	130	45
6	840	130	45
7	1000	165	45
8	1150	165	45
9	1300	165	45
10	1450	165	45
11	1600	165	45
12	1800	220	65
13	2000	220	65
14	2200	220	65
15	2400	220	65
16	2700	330	65
17	3000	330	65
18	3700	330	65
19	3760	500	[1] 65, $f_o = 3600$
19a	3750		[2] 500, $f_o = 3750$

[1] Voiced
[2] Unvoiced

The experimental response of filter 6 is shown in Figure 7. If performance is in qualitative agreement with the calculated response, the passband is very close to expectations, and the stopbands are well below the response of a Butterworth filter, and should provide more than adequate rejection.

The frequency response of the high-frequency channels (17) is shown in Figures 8 and 9. As in channel 6, the roundoff limits sidelobe response, this time to about −50 dB. The bandwidth of this filter is wider than filter 6, resulting in less processing gain and greater sensitivity to roundoff error. The impulse response plot in Figure 10 reveals a larger proportion of very small weights, which is consistent with the greater roundoff sensitivity.

These two filters represent extremes in the design bandwidth with all the others lying in between. We have plotted all of the other cases and have confirmed that the other cases do not have unexpected problems in roundoff sensitivity and gain.

C. CCD TOPOLOGY

The CCD structure for the split electrode filters is a four-electrode-per-cell, double-polysilicon device. To simplify the output sense circuitry, a clocking scheme is used that

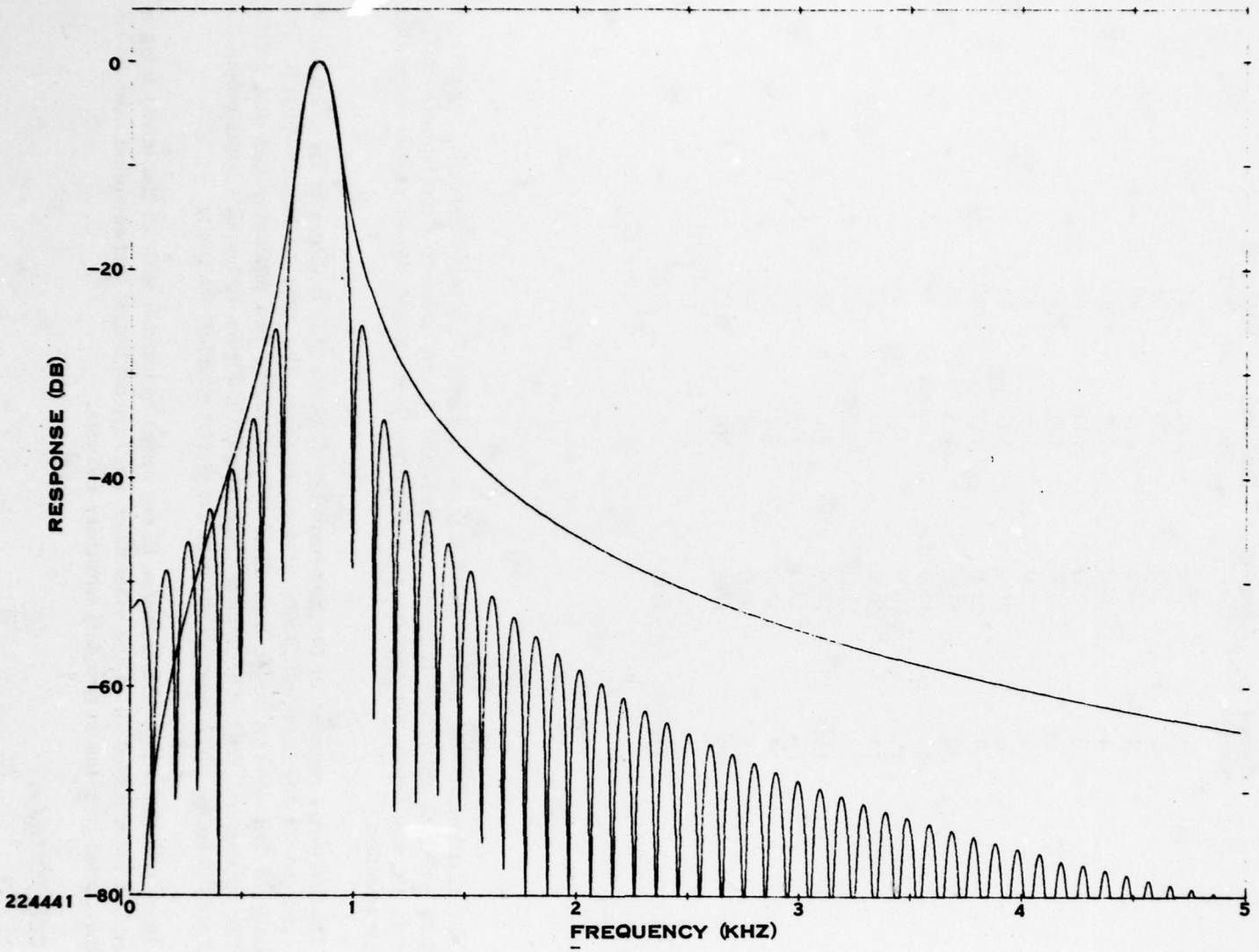

Figure 4. Analyzer Filter 6 [The Butterworth characteristic (smooth curve) and the FIR characteristic are both shown.]

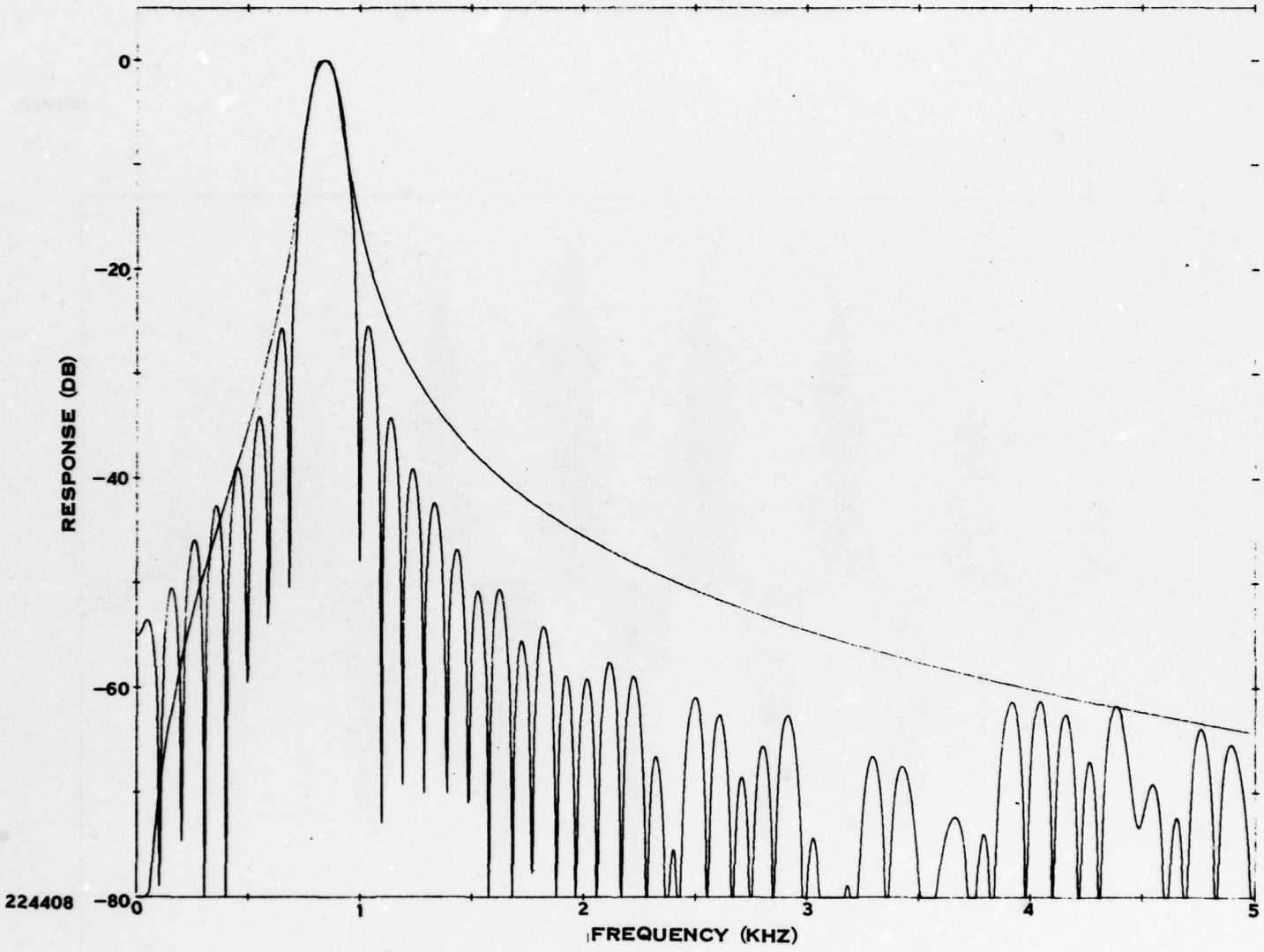

Figure 5. Analyzer Channel 6 Showing the Effects of Tapweight Roundoff

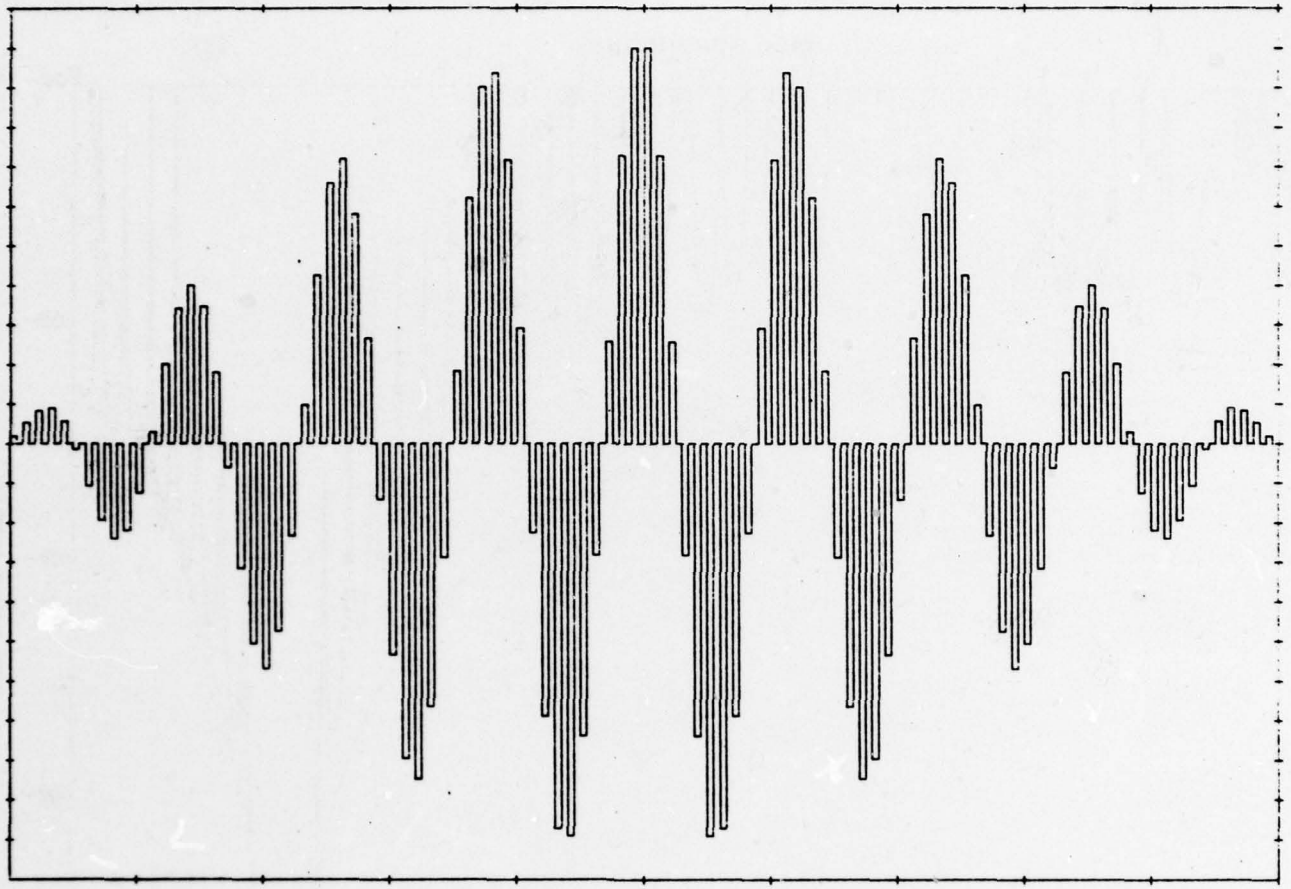

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Figure 6. Weighting Coefficients for Analyzer Filter 6

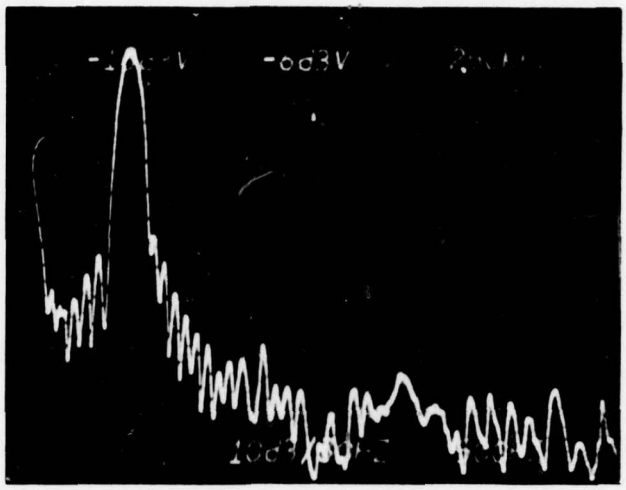

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Figure 7. Experimental Frequency Response of CCD Analyzer Filter 6 (The center frequency is 840 Hz and the bandwidth at the −3-dB points is 130 Hz.)

maintains two of the four electrodes per cell at dc potentitals and that pulses the other two electrodes. The charge transfer process is illustrated in Figure 11. Here the surface potential is drawn (positive downward) to illustrate the potential wells for signal electron charge packets at various times in the clock cycle. At time t_1, the charges are shared under the ϕ_1 and ϕ_2 electrodes and the ϕ_1 and ϕ_2 clocks are ON (15 V). At time t_2, the ϕ_1 clock is in the OFF (0-volt) state and the charge packets have moved forward to the wells under the ON ϕ_2 electrodes. At time t_3, the ϕ_2 clock is OFF and the charge packets have been pushed over the barrier created by the 2-Vdc bias on the third electrode of each CCD cell and are stored under the sense electrodes. The sense electrodes are maintained at a constant dc potential (7.5 V) by the output circuit described below.

The output sense circuit is a charge integrating amplifier as illustrated in Figure 12. The difference in charge sensed by the two parts of each split electrode is proportional to the signal charge and to the difference in the area of the two pieces of the electrode. Thus, the weighting coefficient is obtained by controlling the positions of the split in the electrode. The products of the weighted charge packets are summed by simply tying the electrodes to the two summing bus lines that form the two inputs to the integrator. The output signal voltage is therefore

$$V_{out}\ (n) = \frac{C_{IN}}{C_f} \sum_{k=1}^{N} h_K \cdot V_{IN}\ (n - K)$$

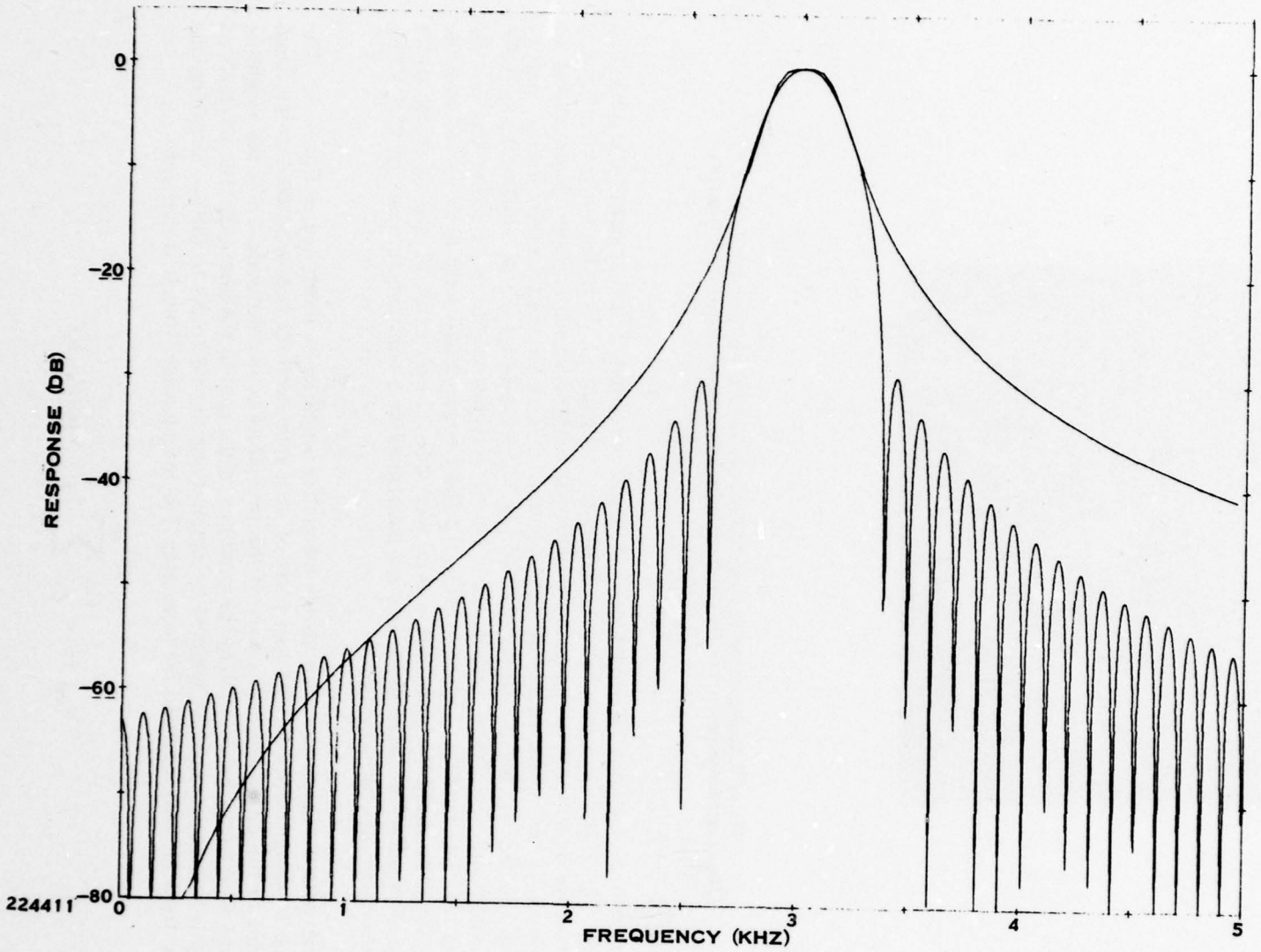

Figure 8. Analyzer Filter 17

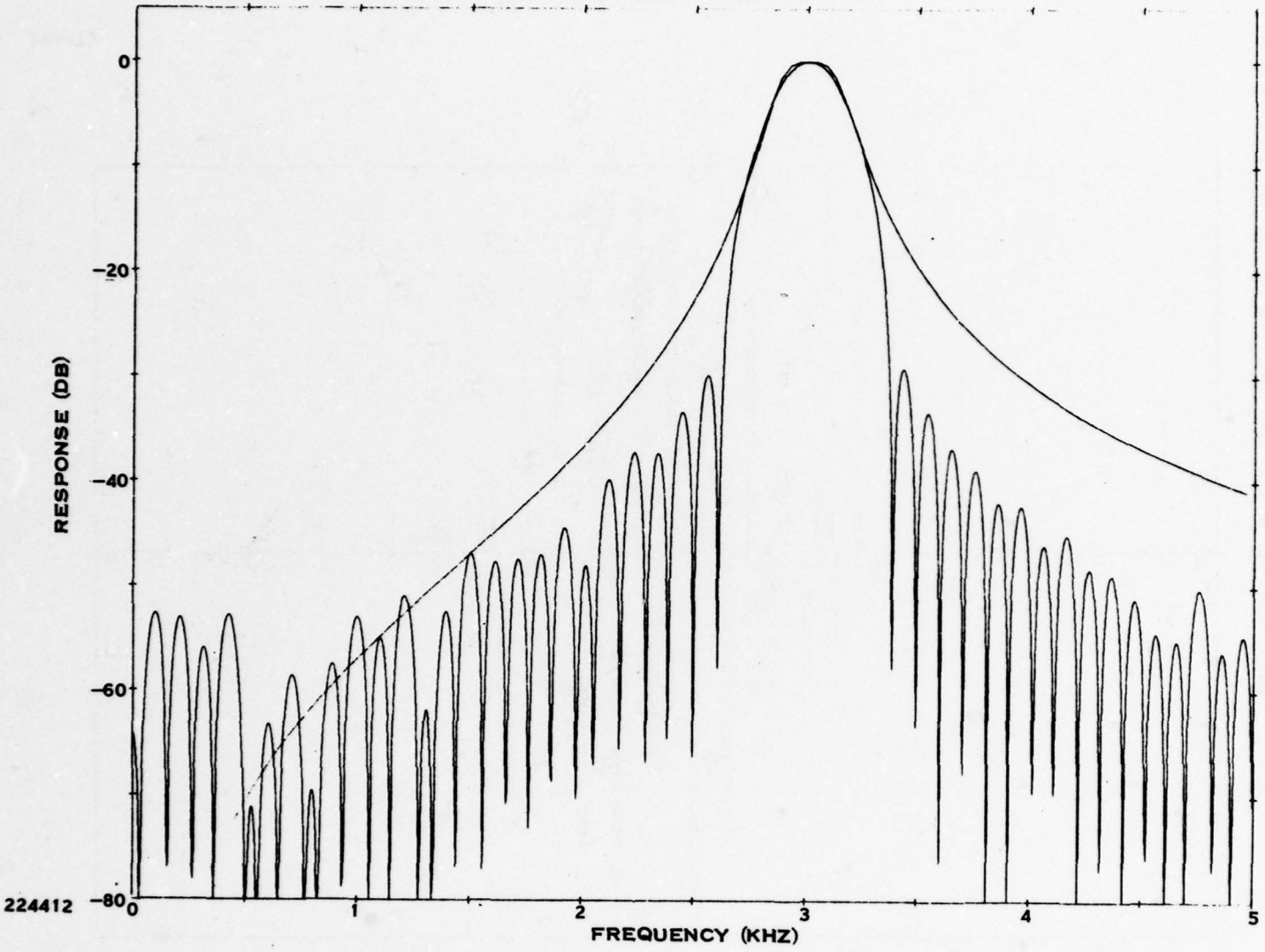

Figure 9. Analyzer Filter 17 With Tapweight Roundoff

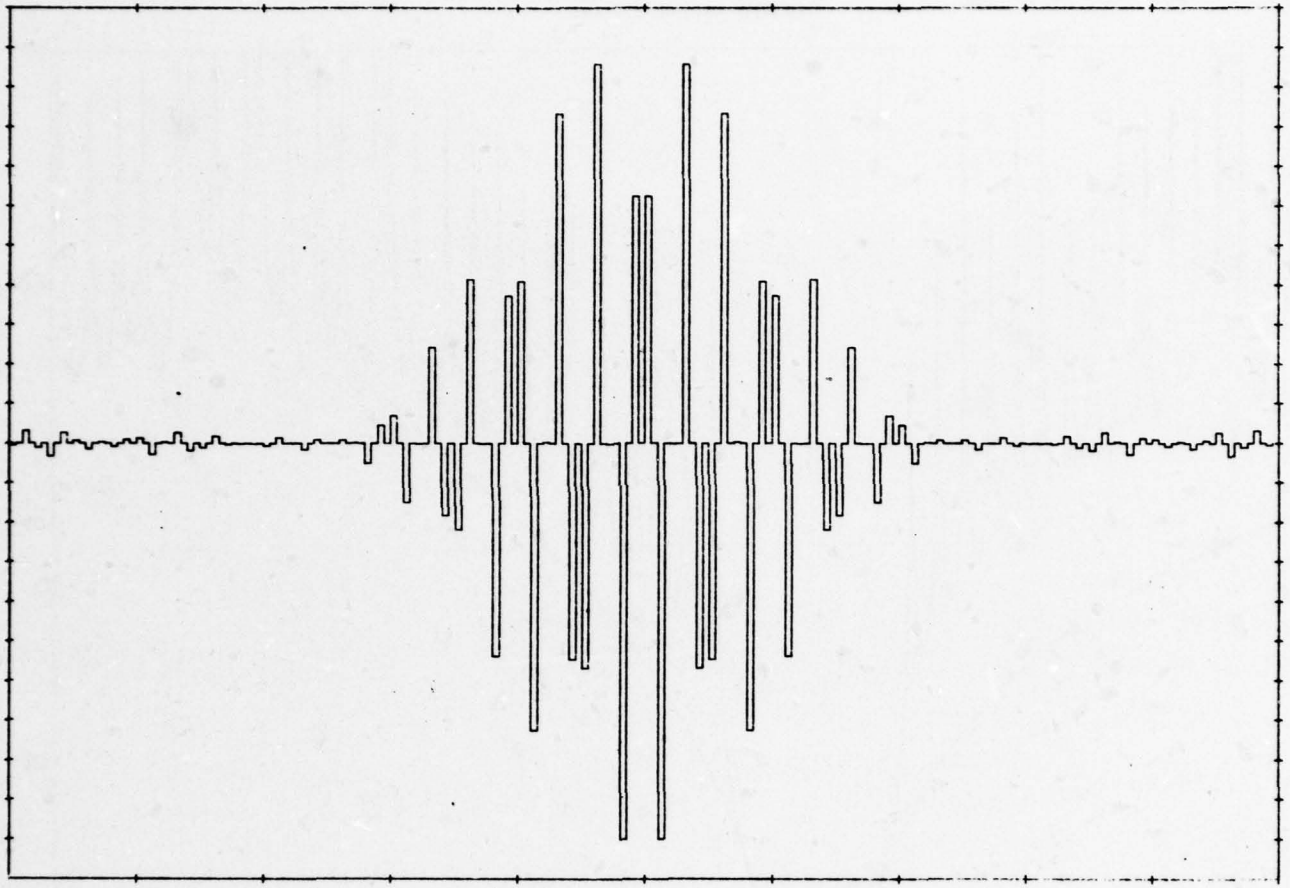

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Figure 10. Tapweights of Filter 17

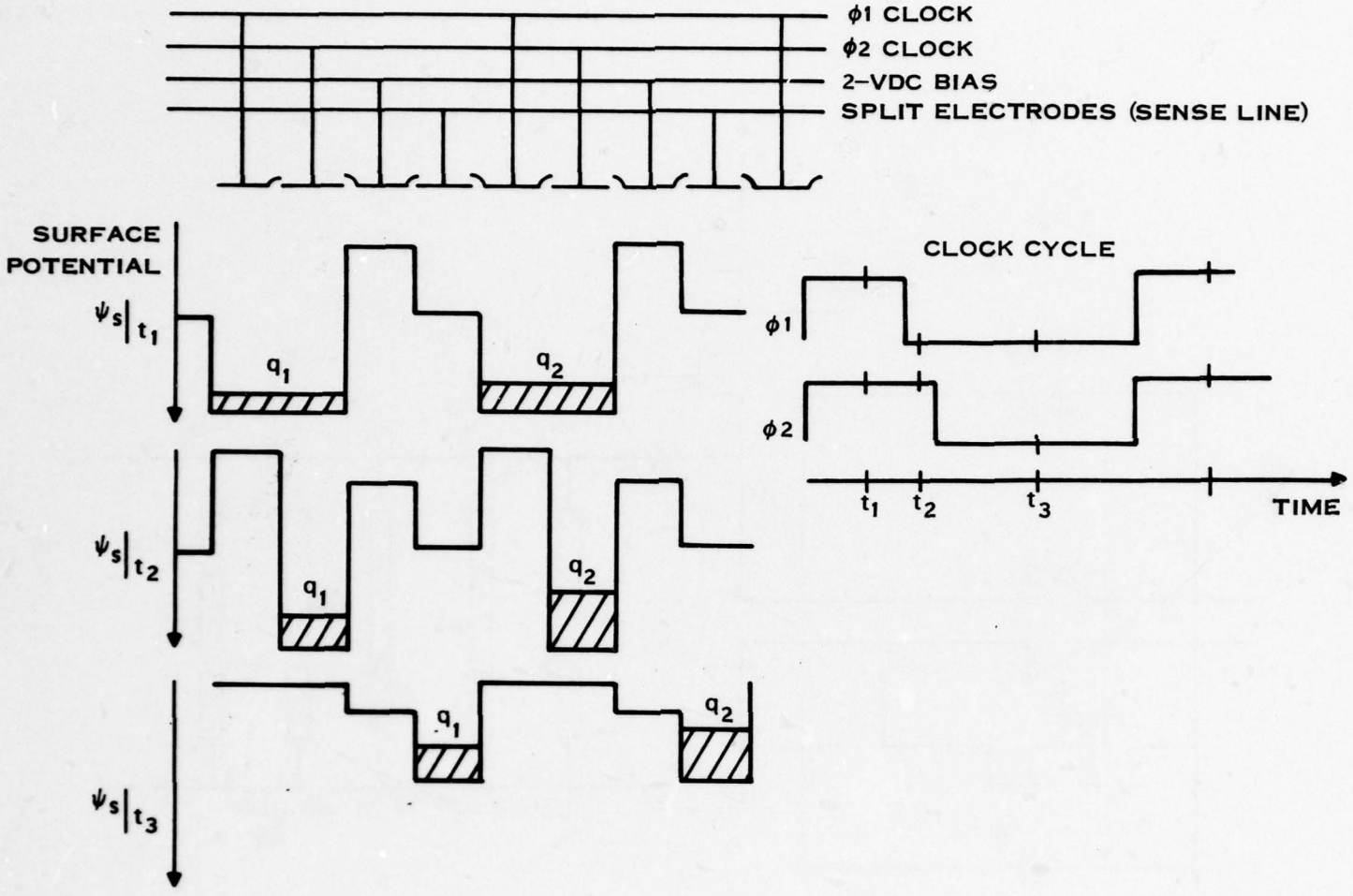

Figure 11. Schematic of CCD Change Transfer Process and Clock Timing

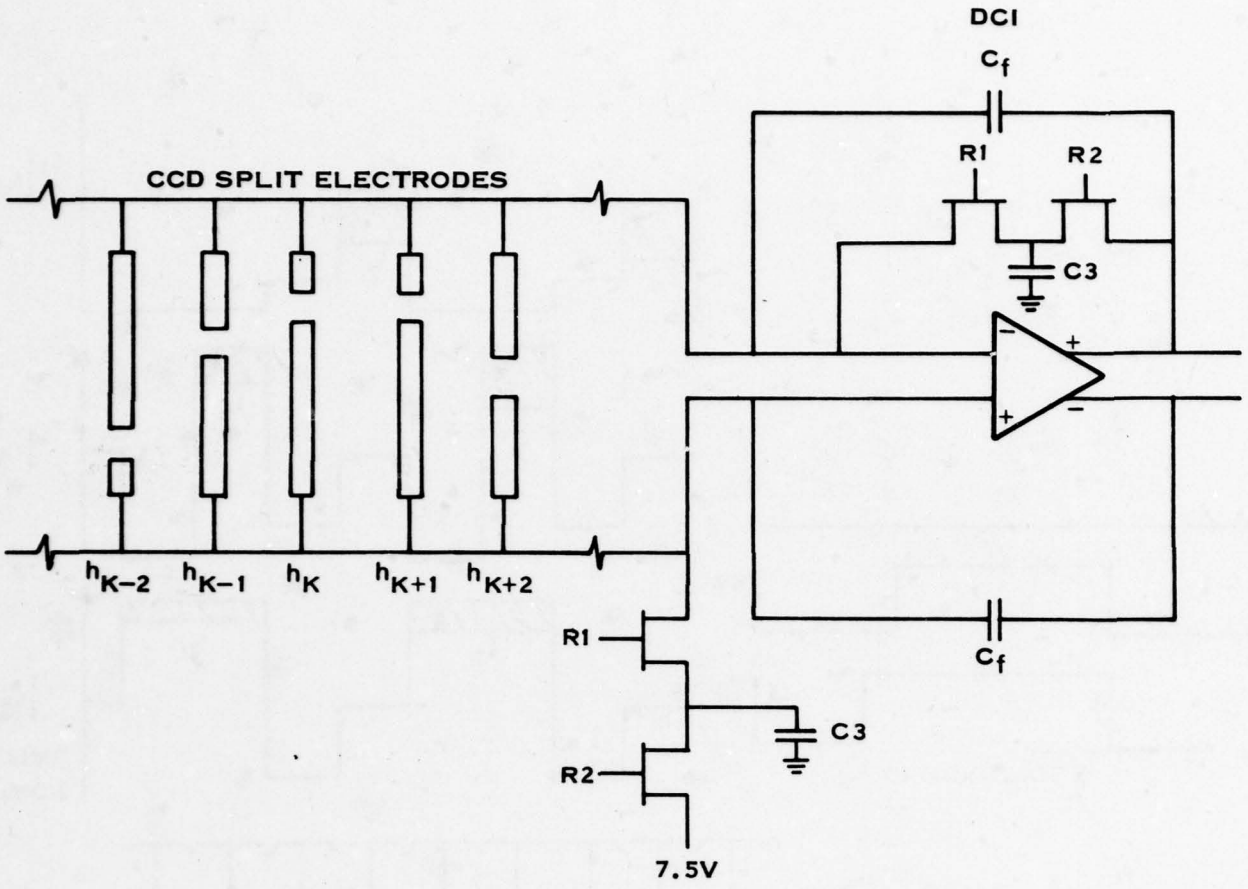

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Figure 12. CCD Output Circuit (The differential current integrator circuit, DCI, integrator provides an output voltage.)

in which C_{in} is the input capacitance of the CCD, h_K is the filter weighting coefficient, C_f is the gain determining feedback capacitor of the integrator, and n is the time index.

D. CCD FILTER AMPLIFIER

The CCD bandpass filters use the split electrode technique to implement the tapweights. This technique requires the use of an amplifier to sense the charge on the split clock lines differentially and provide a voltage output. This amplifier is called a differential current integrator (DCI). A schematic of the DCI used is shown in Figure 13. The amplifier functions as an integrator, integrating the CCD output signal onto the feedback capacitors.

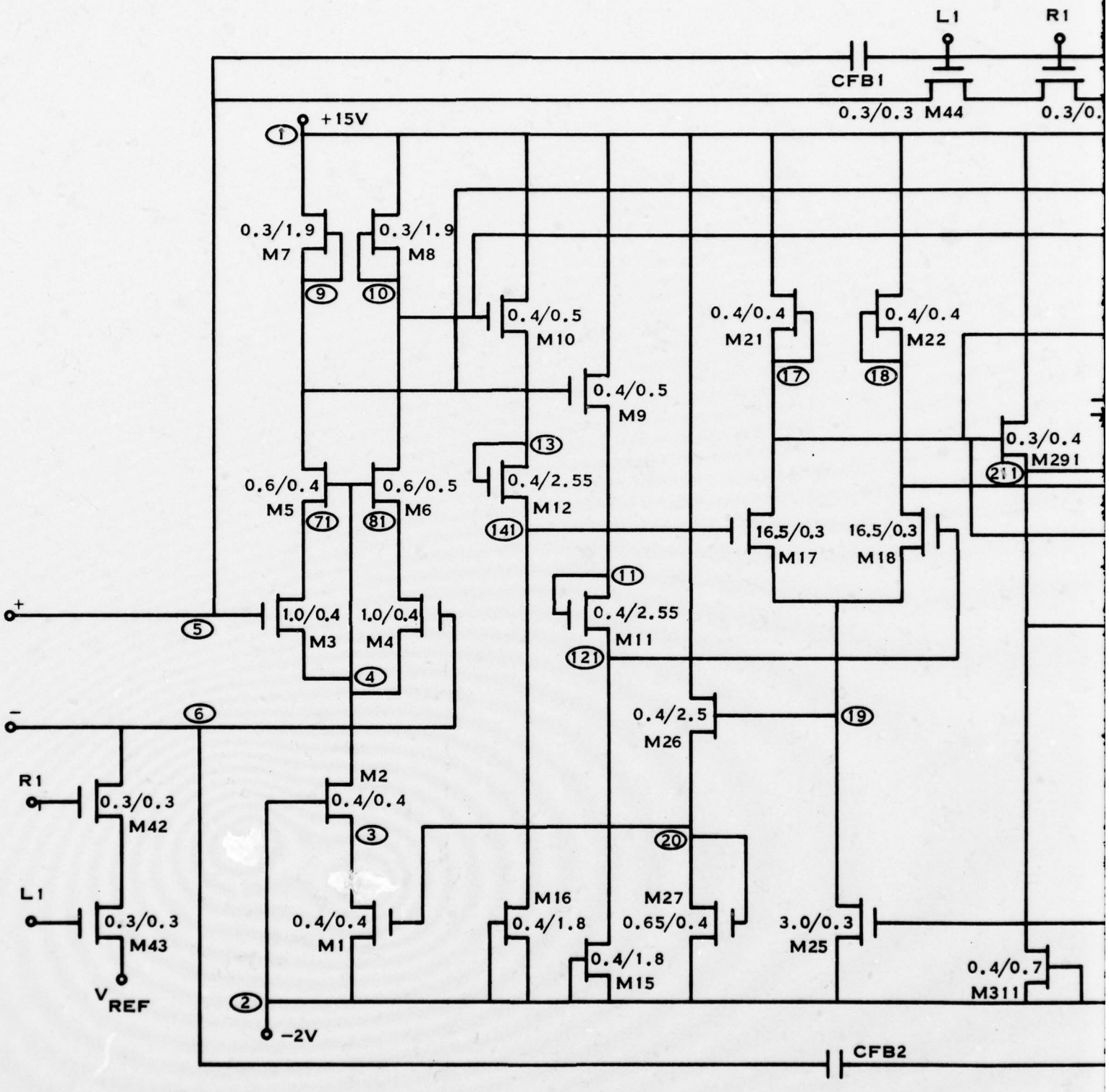
The amplifier consists of two differential gain stages. The first stage is formed by the active devices M3 and M4 with cascode devices M5 and M6 and load devices M7 and M8. A pair of voltage translating buffers is provided by M9, M10, M11, and M12. A second differential stage is formed with M17, M18, M21, and M22 with differential outputs obtained on nodes 17 and 18. The internal compensation capacitors (4.0 pF) are buffered by source followers M281 and M291, and the gain controlling feedback capacitors are buffered by followers M28 and M29. In order to suppress common mode responses, the output common mode voltage on node 24 is sensed. This signal is buffered and fed back to control the current source of the output differential stage. This negative feedback loop minimizes the common mode response of the amplifier. Device sizes are given in Table 2.

The design characteristics of the amplifier are plotted in Figures 14, 15, and 16. Open loop frequency characteristics are in Figure 14, which shows magnitude and phase characteristics. The dc gain is about 65 dB. The amplifiers are typically used with a closed loop voltage gain of about 5, so the closed loop frequency response was checked for that gain. The results are plotted in Figure 15. The amplifier has only a 63-degree phase shift at the unit gain frequency of 1.5 MHz. This high phase margin was designed to avoid overshooting in the transient response, which might interfere with the performance of the rectifier circuit that follows the DCI. The transient response is plotted in Figure 16, which shows a very smooth transient corresponding to about a 2-μs time constant. The amplifier is well settled within the 12.5-μs interval between the charge transfer to the sense electrodes of the CCD and the sampling clock edge which allows the rectifier circuit to sample the DCI output.

In the chip, each filter has a different processing gain. Each DCI gain is adjusted by changing the value of the feedback capacitors C_f for each filter so that the filter bank has uniform gain. That is, the gains of all filters are equal at their band centers.

E. RECTIFIER CIRCUITS

The bandpass filtered signals are rectified by the halfwave rectifier circuit shown in Figure 17. This circuit takes advantage of the sampled-data nature of the CCD output signal to establish a reference level with low offset. The rectifying action is obtained by using the MOS transistor M_{52} to charge capacitor C_2 to the cutoff point of the transistor. The differential amplifier formed by M_{46}-M_{51} and the associated depletion load current sources is used as a comparator to achieve sharper M_{47}, M_{50}, M_{55} cutoff characteristics. Once each cycle the reset clocks R_1, R_2 and R_3 are turned on. This connects the input to a fixed reference and also discharges the output capacitors C_1 and C_2. The turnoff edges of the reset clocks are staggered in time with the result that offsets due to the turnoff of the reset clocks are stored on the capacitors. After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R1
CFB1
0.3/0.3 M44
0.3/0.
+15V
1
0.3/1.9 M7
0.3/1.9 M8
9
10
0.4/0.5 M10
0.4/0.5 M9
0.4/0.4 M21
0.4/0.4 M22
17
18
0.3/0.4 M291
211
13
0.6/0.4 M5
0.6/0.5 M6
0.4/2.55 M12
71
81
141
16.5/0.3 M17
16.5/0.3 M18
11
0.4/2.55 M11
121
+
5
1.0/0.4 M3
1.0/0.4 M4
4
−
6
0.4/2.5 M26
19
R1
0.3/0.3 M42
M2 0.4/0.4
3
20
L1
0.3/0.3 M43
0.4/0.4 M1
M16 0.4/1.8
M27 0.65/0.4
3.0/0.3 M25
0.4/1.8 M15
0.4/0.7 M311
V REF
2
−2V
CFB2

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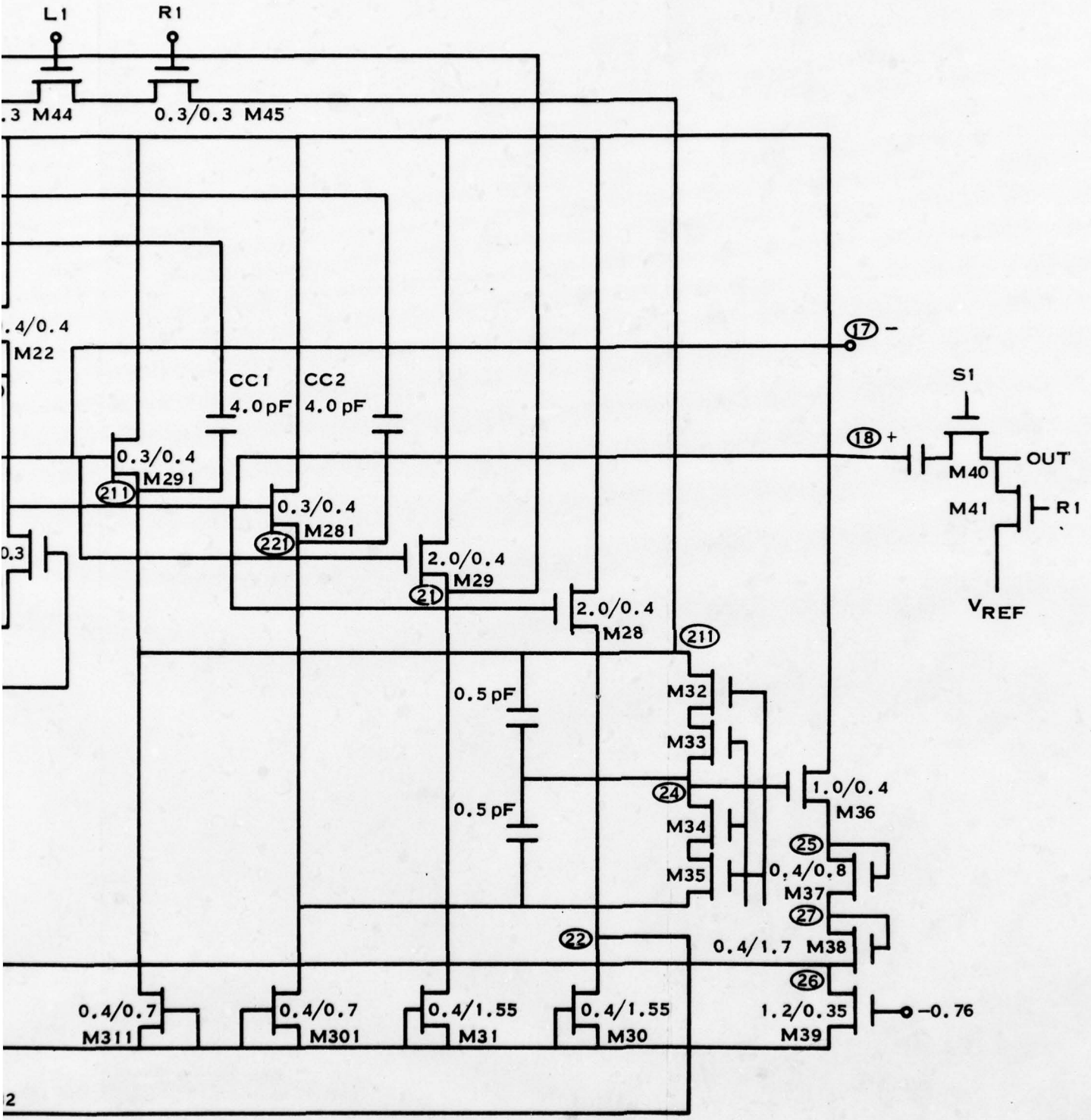

Figure 13. CCD Filter Amplifier

TABLE 2. DEVICE DIMENSIONS IN DIFFERENTIAL CURRENT INTEGRATOR

Device Number	Depl/Enh	W/L (mils)
M1	E	0.4/0.4
M2	D	0.4/0.4
M3	E	1.0/0.4
M4	E	1.0/0.4
M5	D	0.6/0.4
M6	D	0.6/0.4
M7	D	0.3/1.9
M8	D	0.3/1.9
M9	E	0.4/0.5
M10	E	0.4/0.5
M11	E	0.4/2.55
M12	E	0.4/2.55
M15	D	0.4/1.8
M16	D	0.4/1.8
M17	E	16.5/0.3
M18	E	16.5/0.3
M21	D	0.4/0.4
M22	D	0.4/0.4
M25	E	3.0/0.3
M26	D	0.4/2.5
M27	E	0.65/0.4
M281	D	0.3/0.4
M291	D	0.3/0.4
M301	D	0.4/0.7
M311	D	0.4/0.7
M28	E	2.0/0.4
M29	E	2.0/0.4
M30	D	0.4/1.55
M31	D	0.4/1.55
M32	E	0.3/0.3
M33	E	0.3/0.3
M34	E	0.3/0.3
M35	E	0.3/0.3
M36	E	1.0/0.4
M37	E	0.4/0.8
M38	E	0.4/0.7
M39	E	1.2/0.35
M40	E	0.3/0.3
M41	E	0.3/0.3

the reset cycle, the sample pulse S_1 is turned on and the input is applied through the coupling capacitor C_{IN}. The stray capacitance on the gate of M_{46} and the alternate switching of M_{40} and M_{41} forms a switched capacitor resistor.[7,8] This resistor and capacitor C_{IN} effectively ac couple the input signal. If the input voltage is positive with respect to the reference level, the output node will be pulled up by M_{52} through capacitor C_2. If the input sample is negative with respect to V_{ref}, M_{52} remains cutoff and the output remains unchanged. Experimenting shows that the circuit has approximately 10-mV offset, which is adequate for this application.

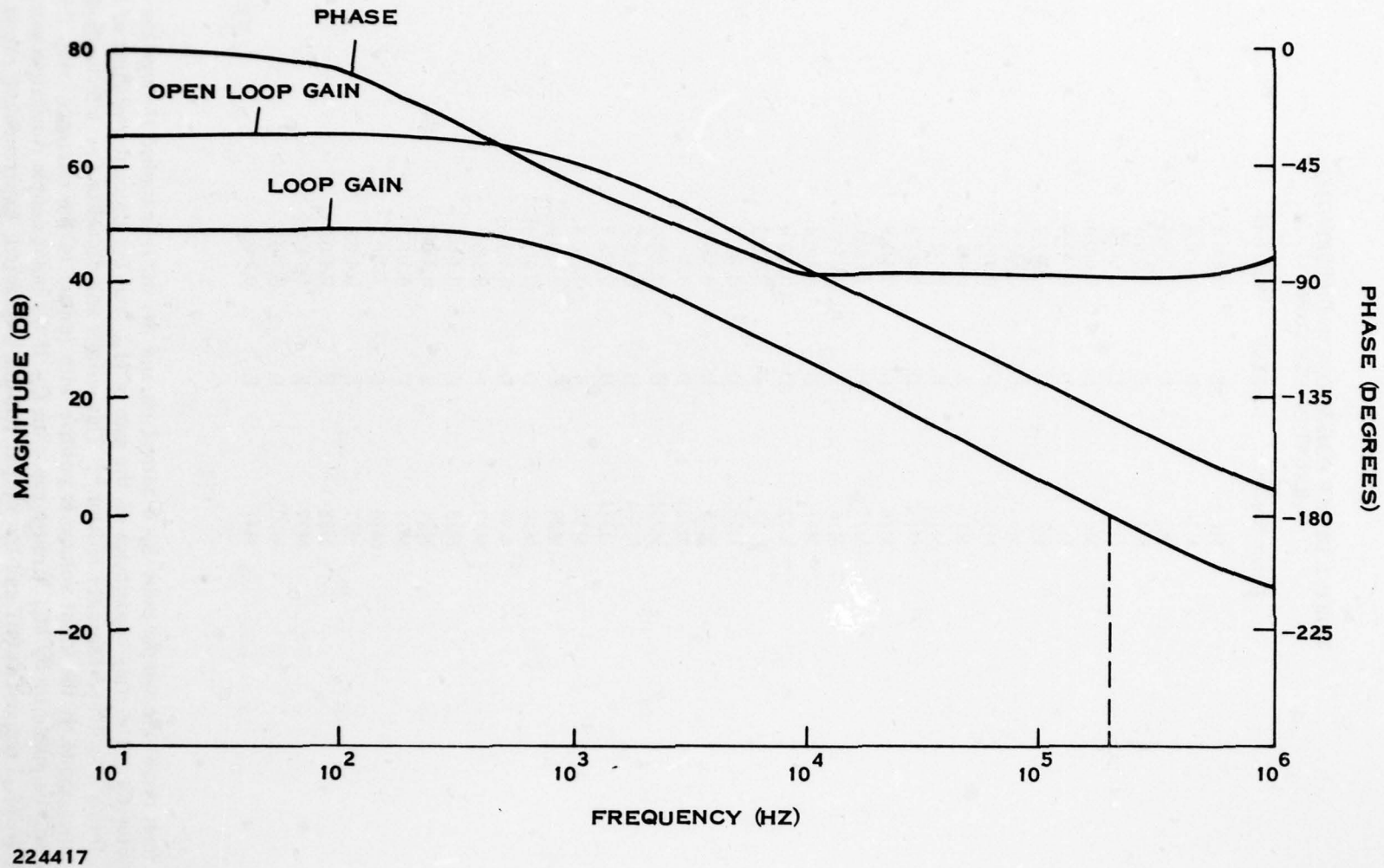

Figure 14. Amplifier Open Loop Frequency Response

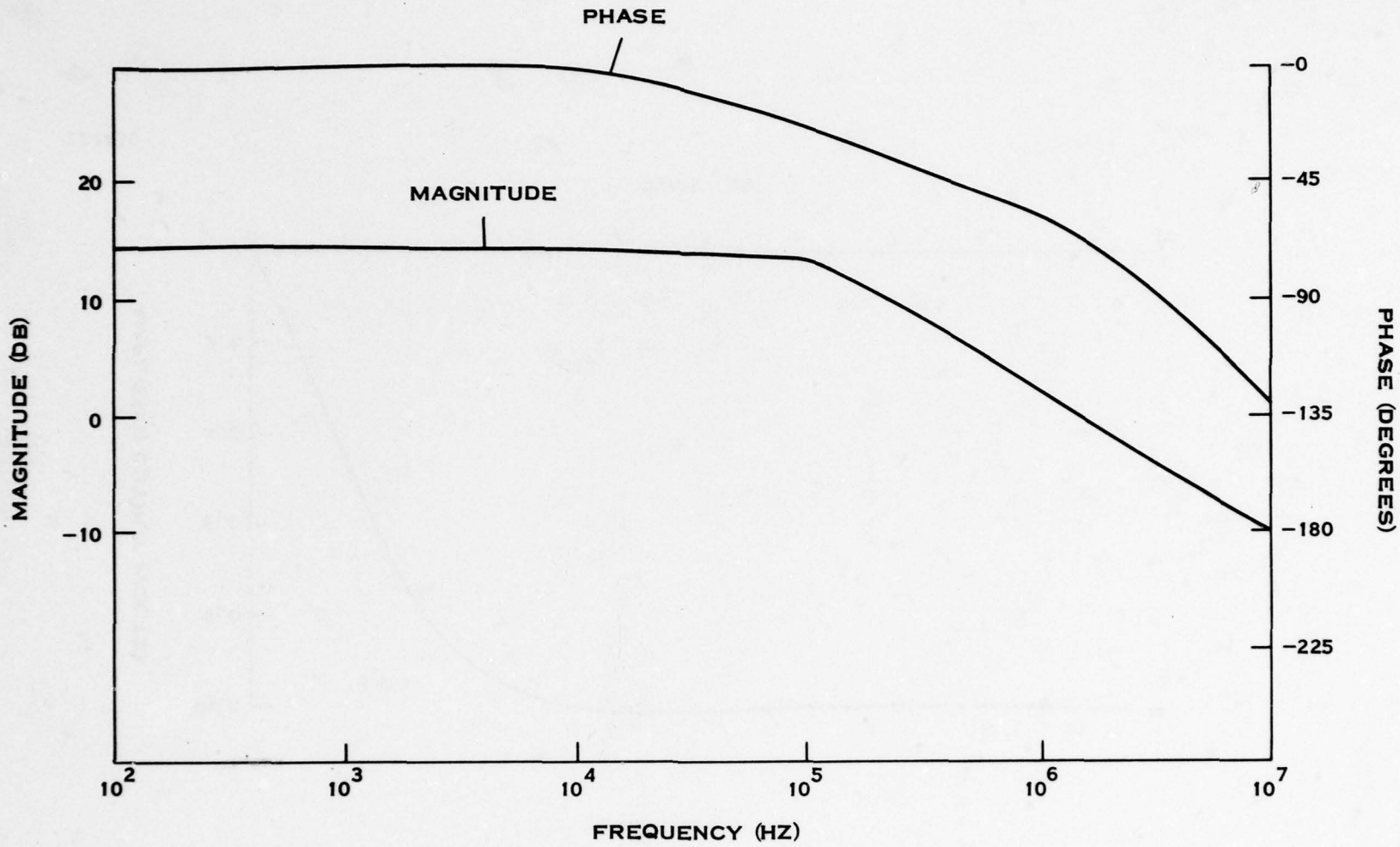

Figure 15. Amplifier Closed Loop Frequency Response

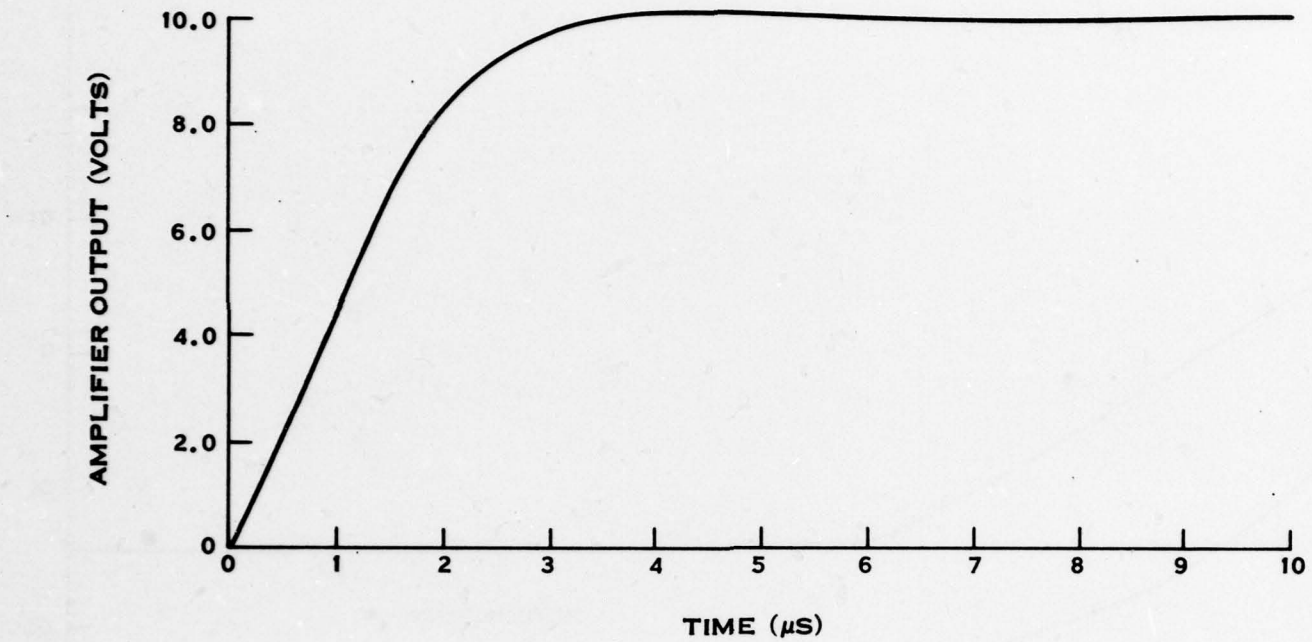

Figure 16. Closed Loop Transient V_{IN} = 2.0 Volts

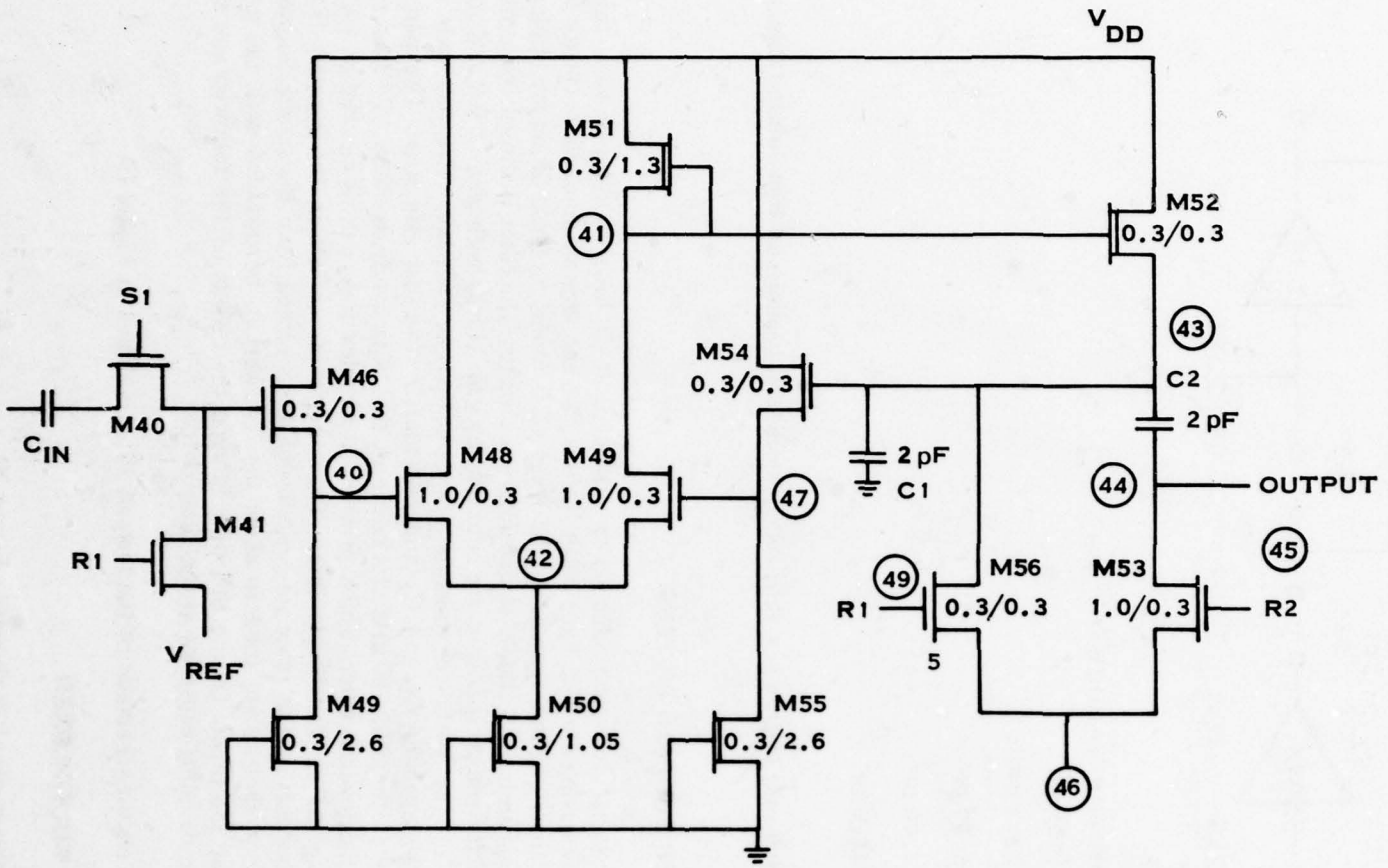

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Figure 17. MOS Halfwave Rectifier Circuit

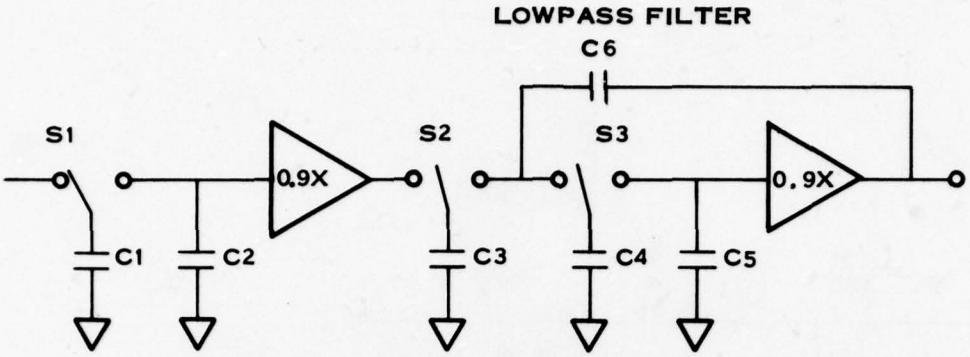


Figure 18. Schematic Diagram of a Three-Pole Lowpass Filter Implemented With Switched Capacitors

F. ANALYZER LOWPASS FILTERS

After the signal for each channel is rectified, it is lowpass filtered with three-pole Butterworth filters having a 35-Hz bandwidth. In this case the area advantage was clearly in favor of the switched capacitor filter approach rather than CCD filters, so these filters are implemented with switches, capacitors, and simple source follower circuits. The filter is shown conceptually in Figure 18, where the source followers are indicated by gain blocks with gain of 0.9 and the MOS transistors used in the switched resistors are indicated as switches. The real axis pole is implemented with capacitor C_1 and C_2 and buffered by the first gain stage. This part of the filter is operated at the same 10-kHz clock rate as the CCD bandpass filters. To save area the second stage of the lowpass filter, which provides a complex pole pair, is clocked at 1 kHz and uses the first stage as an antialiasing filter. To eliminate dc offsets in the lowpass filter, the energy storage elements of the filter are periodically disconnected from the source followers and other switches (not shown) are used to allow the followers to be cascaded with the reference voltage applied at the input. During this time interval the offsets of the followers are sampled and stored on the coupling capacitor at the filter output.

A detailed circuit schematic of the lowpass filter is shown in Figure 19.

G. ANALOG MULTIPLEXER

The multiplexer circuit is shown in Figure 20.

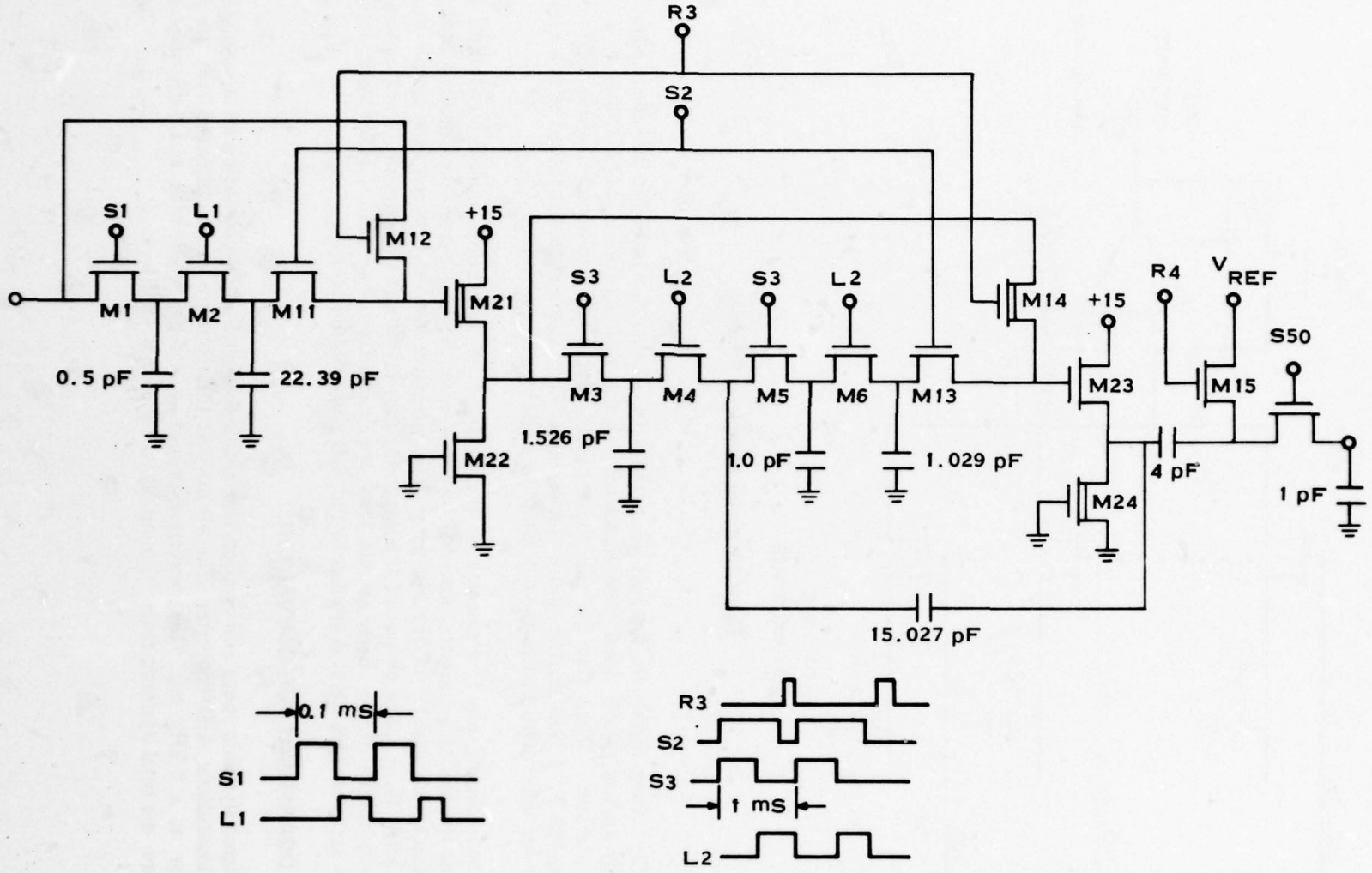


Figure 19. Circuit Schematic of the Three-Pole Lowpass Filter

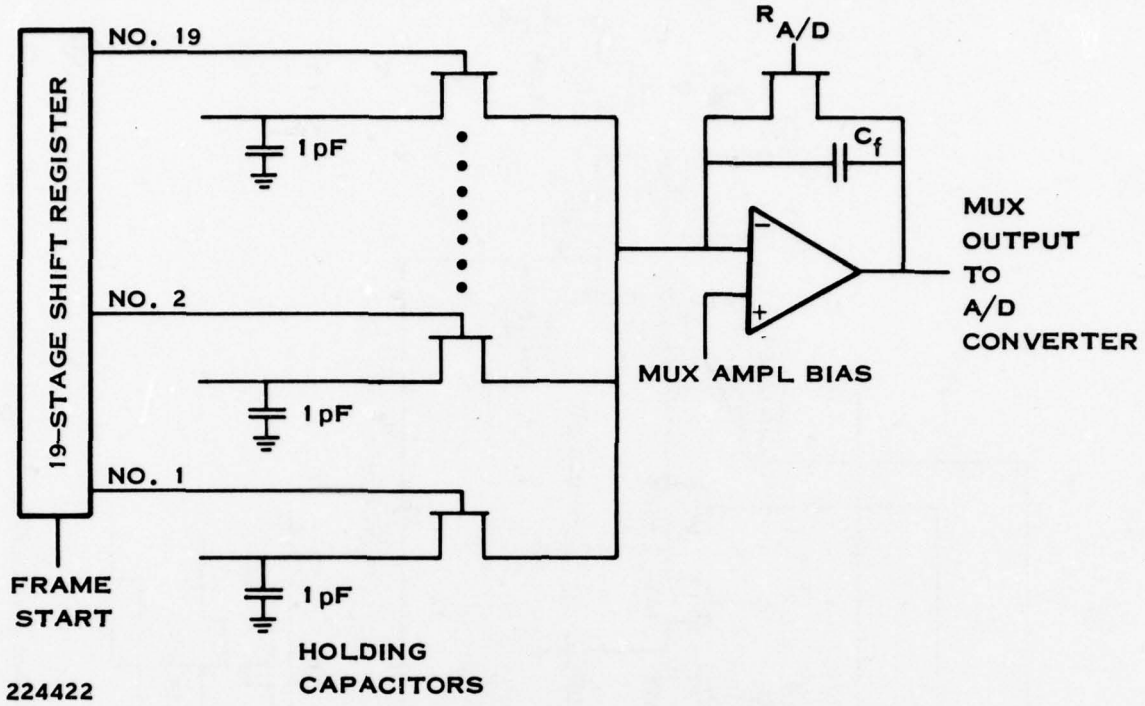


Figure 20. Analog Multiplexer Schematic

The analog signals are sampled when the clock labeled S_{50} in Figure 20 is enabled by the externally applied strobe signal. This signal couples the output of each lowpass filter to a 1 pF holding capacitor. Then one by one these holding capacitors are switched onto the output summing bus by a shift register that is clocked at a 1-kHz rate and that is loaded with a single 1 by the same logic that initiates the S_{50} sampling pulse.

The summing bus is connected to the input of an operational amplifier integrator that maintains the bus at a constant potential by transferring the charge from each holding capacitor to the feedback capacitor of the integrator. The integrator is reset between each sample by the pulse labeled $R_{A/D}$. The output of the integrator thus provides a sequence of 19 analog samples once each speech frame. Each sample lasts approximately 1-ms with a 30-μs reset interval between samples. This signal is applied to the A/D converter input.

H. LOGARITHMIC A/D CONVERTER

Signal dynamic range compression and analog-to-digital (A/D) conversion are accomplished in the logarithmic A/D converter. The 19 lowpass filter outputs are multiplexed into the A/D converter at a 1-kHz rate. The converter output is a 5-bit word with a 1.5-dB step size. Therefore, the total dynamic range of input signal covered is 48 dB.

A block diagram of the converter is shown in Figure 21. Logarithmic response is obtained with an array of eight polysilicon capacitors (C_0 through C_7) weighted so that the sum

$$C_{sum} = \sum_{n=i}^{7} C_n \text{ for } i = 0 \text{ through } 7$$

is incremented in 6-dB steps and with a polysilicon resistive divider (R_0-R_3), which makes available four reference voltages (V_0 through V_3) and a reset voltage V_{reset} spaced 1.5 dB apart to the capacitor array. A successive approximation technique is used to determine the digital word. A 10-stage shift register (SR10) clocked by 10-kHz pulses Q1 and S1 A/D continuously circulates a single 1 bit to provide sequencing for the A/D converter. When $SR10_0$ is high, the converter goes through a reset cycle. At this time the latches containing the digital output (Q_1-Q_5) are reset to 0 and the bottom plates of the capacitors C_0 through C_7 are clamped to V_{reset}, while the signal amplifier and the high-gain comparator A2 are reset. A signal from one of the 19 lowpass filter outputs is then applied to C_{sig} by the A1 amplifier. The signal is inverted by A1 and appears on node n_c attenuated in half by the capacitor array. The comparator saturates in the high state if the signal is greater than approximately 4 mV.

To determine the first 3 bits (Q_1, Q_2, Q_3) of the digital output, $LATCH_1$ through $LATCH_3$ are sequentially set to 1 by the shift register. When $LATCH_1$ is set, the CAPACITOR DECODE circuit causes the bottom plates of capacitors C_3 through C_7 to be switched from V_{reset} to V_{switch} ($V_{switch} = V_0$ at this time). This causes the voltage on node n_c to increase by an amount proportional to $C_3 + C_4 + C_5 + C_6 + C_7$ and to V_0 (25.5 dB). If this voltage increase is greater than the decrease that was caused by the signal, then the comparator A2 will change state and, at the end of this cycle, the Q_1 output of $LATCH_1$ will be reset to 0. If the voltage increase is not enough to cause the comparator to change state, then the Q_1 output of $LATCH_1$ will remain set to 1. Bits Q_2 and Q_3 are determined in the same fashion, after which the capacitors that bring the voltage on node n_c to within 6 dB below the comparator switching threshold remain clamped to V_{switch}. The other capacitors are clamped to V_{reset}. Next, $LATCH_4$ is set, causing the voltage V_{switch} to increase by 3 dB from V_0 to V_2. This causes the voltage on node n_c to increase by 3 dB. If the comparator changes state, then the Q_4 output of $LATCH_4$ is reset to 0; otherwise, it remains 1 Q_5 is determined in the same way. The digital word is now completely determined and the shift register ($SR10_8$) causes the MOS to TTL converters to sample the word. $SR10_0$ provides a data-ready signal to the microprocessor which then has 800 μs to read the word before any change will be made.

Experimental evaluation of the A/D converter has included a measurement of the switching point of the A/D for all possible 5-bit codes. A typical curve is plotted in Figure 22. These data were obtained by injecting a signal from an external pulse generator on the input of the A/D. This procedure ensures that only the A/D characteristics are being measured rather than a complete channel of the analyzer. The curve shows good 1.5-dB steps throughout most of the range; however, the step size grows at the lower end of the scale. The reason for this deviation may be a small offset in the comparator that is not completely compensated. This departure from ideal behavior is being investigated although it is possible that the small elevation may not be audibly perceptible.

I. MOS/TTL OUTPUT BUFFERS

The analyzer A/D converter has six output signals, five data lines, and a data-ready signal. Each of these is buffered by an identical amplifier to provide TTL level outputs with a fanout of two standard loads. A computer model of the circuit indicates that each amplifier will dissipate 0.67 mW and that the rise and fall times under maximum load are 80 to 90 ns. Each amplifier consumes 0.65×10^{-5} cm^2 (36 mil^2) of surface area.

The schematic diagram of one of these drivers is shown in Figure 23. The circuit consists of two depletion load inverters, a flip-flop, and a push-pull output stage. Transistor pairs M1, M3, M2 and M4 form the two inverters. The inverted input signal appears on node A and the true signal reappears on node B where the levels now are 0 V and V_{DD} (15 V). These signals are applied to the load transistors (M5 and M6) of a flip-flop, and the outputs of the flip-flop drive the push-pull output stage (M9 and M10). Because the flip-flop and the push-pull stages are composed of enhancement mode devices, there is no quiescent current required, resulting in the low on-chip power dissipation.

J. ANALYZER TIMING CIRCUITS

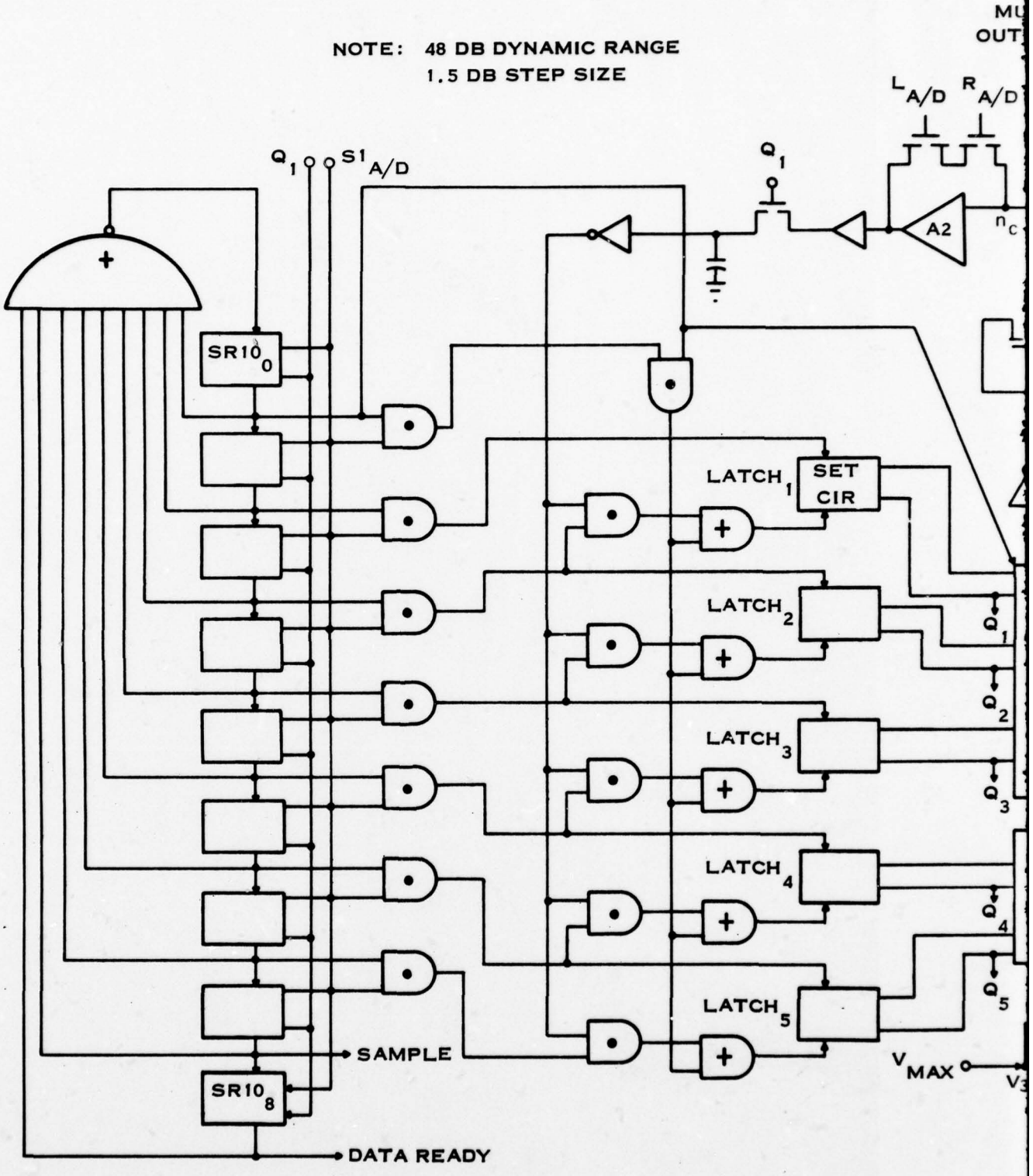
1. Clock Circuits

The speech analyzer requires a complex clocking scheme to perform the variety of functions previously described. A 40-kHz square-wave clock signal is input to the chip and all other clock signals are derived from this master clock. The diagram shown in Figure 24 shows the clock signals used. The 40-kHz master clock (MC) is first sent to a generator that produces two nonoverlapping 40-kHz signals (A and B). The A and B clocks operate a shift register divider that generates four-phase, 10-kHz clocks (Q_1, Q_2, Q_3, and Q_4) and a 1-kHz signal (ϕ_{10}). These signals (MC, A, B, Q_1, Q_2, Q_3, Q_4 and ϕ_{10}) are combined to generate positive-going edges to trigger the clock driver circuits that generate all of the other clock waveforms shown in Figure 24.

The basic clock driver circuit shown in Figure 25 was built in two sizes, one for large capacitive loads (>720 pF) and one for small loads (<10 pF). This circuit requires two nonoverlapping signals at its inputs labeled PU and PD for pullup and pulldown, respectively. This circuit is completely dynamic and draws no dc power, yet it provides a low output impedance that minimizes interactions between the various clock circuits.

Figure 26 (A), (B), and (C) show how the various timing signals MC, A, B, Q_1, Q_2, Q_3, Q_4 and ϕ_{10} are combined to the inputs of the clock drivers to provide the pullup and pulldown signals for the drivers. The blocks labeled GEN1L and GEN1S are the large and small versions of the driver circuit shown in Figure 25. One example of the logic is the ϕ_1 clock driver for the CCD clock. This driver is shown in the upper left corner of Figure 26(B). The pullup signal to the driver is obtained by gating the A′ clock (delay A) using the Q_1 signal on the gate of a series MOSFET. The pulldown command is obtained by simply using the B clock. Note that in all cases the logic ensures that the pullup (PU) and pulldown (PD) signals are never on simultaneously.

NOTE: 48 DB DYNAMIC RANGE
1.5 DB STEP SIZE



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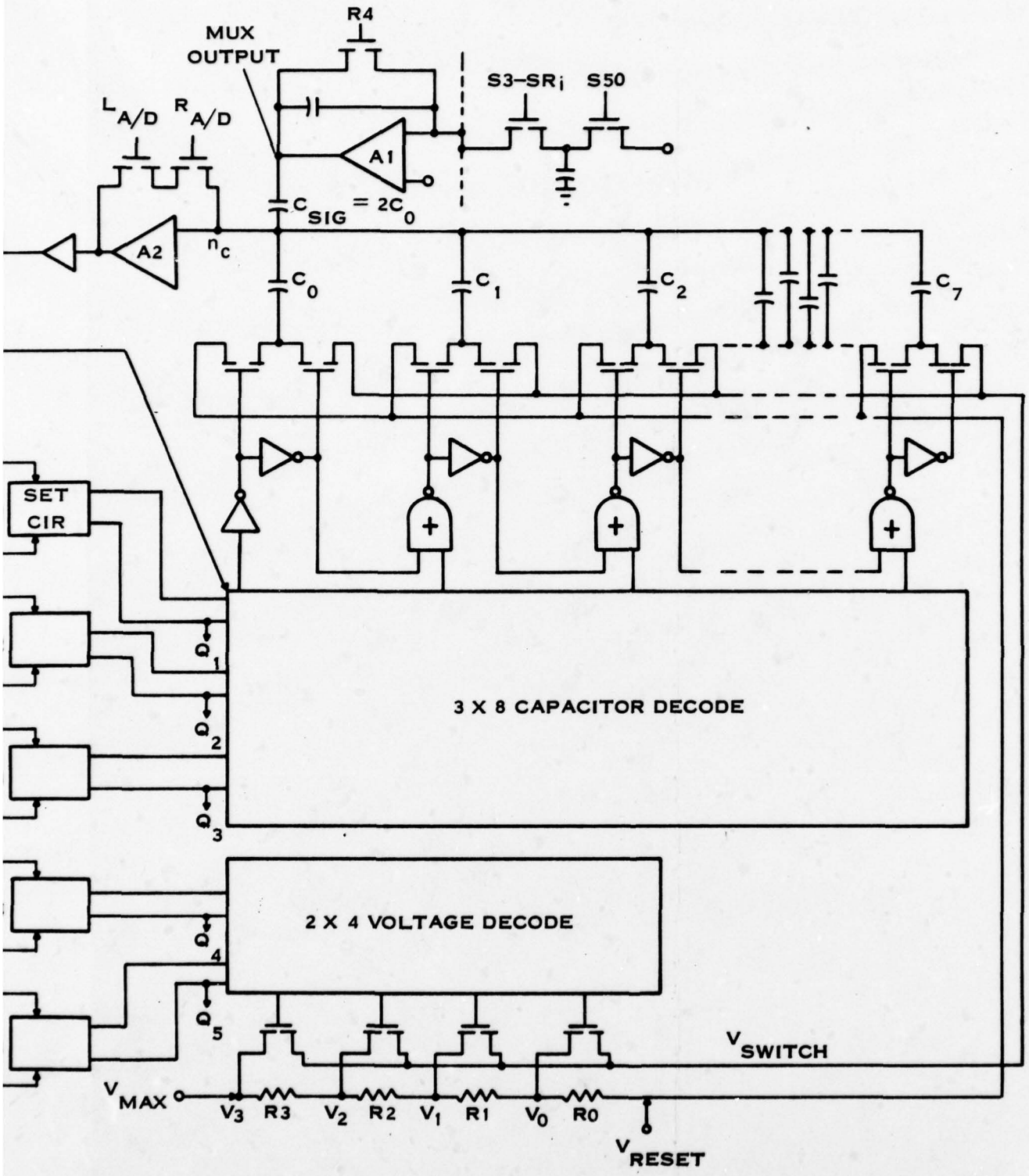

Figure 21. Fine-Bit Logarithmic A/D Converter

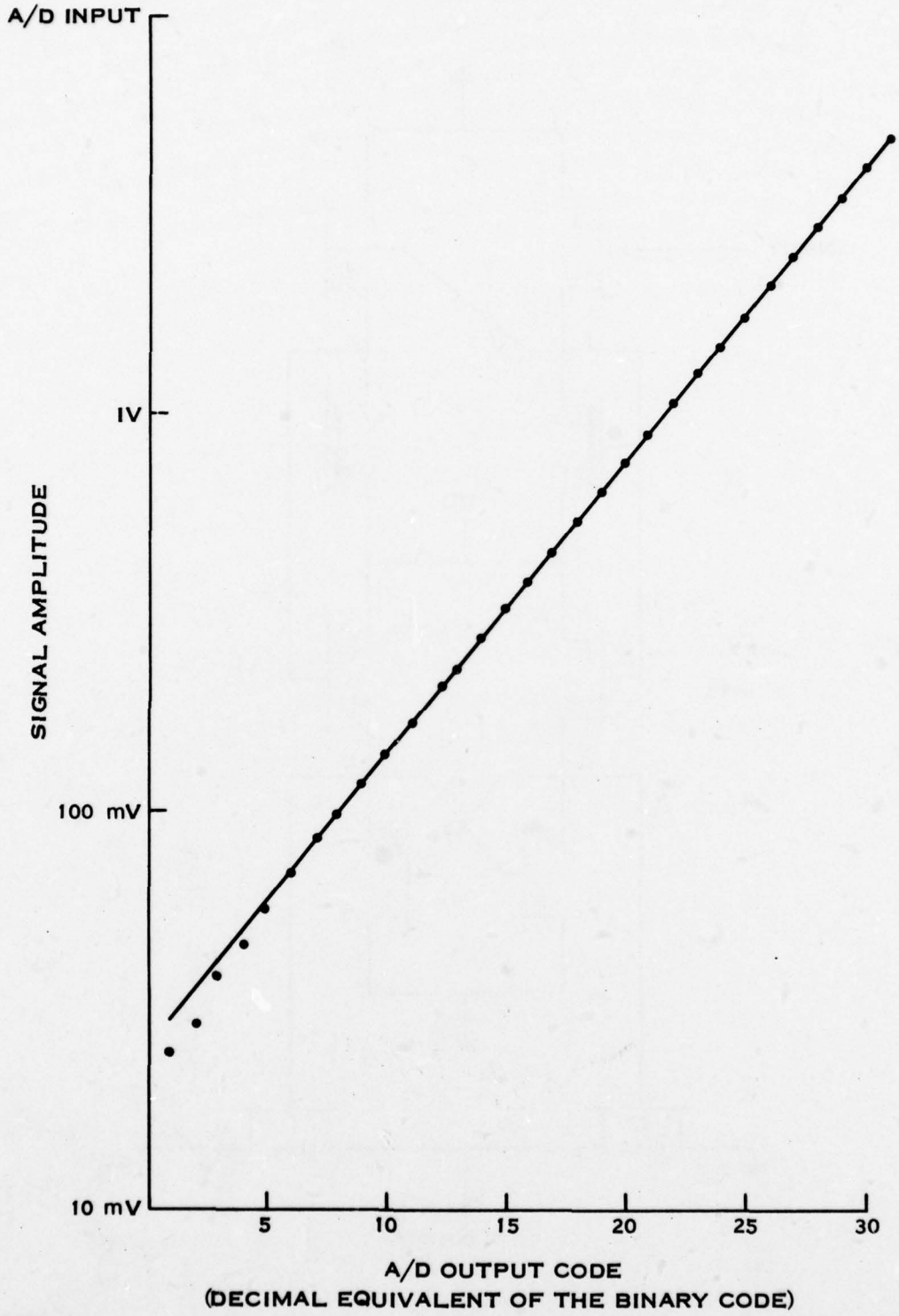

Figure 22. Transition Points in the Output Code of the A/D Converter

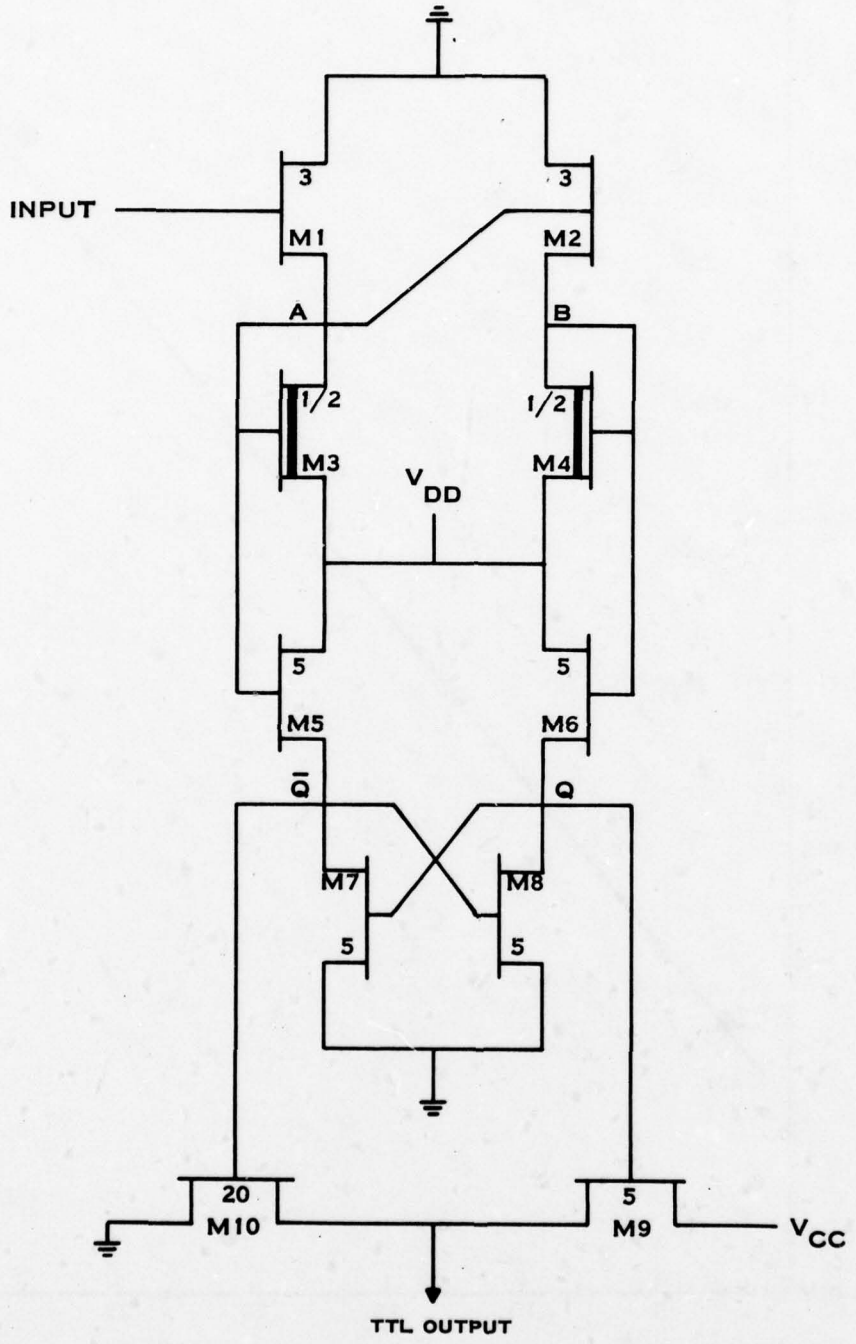

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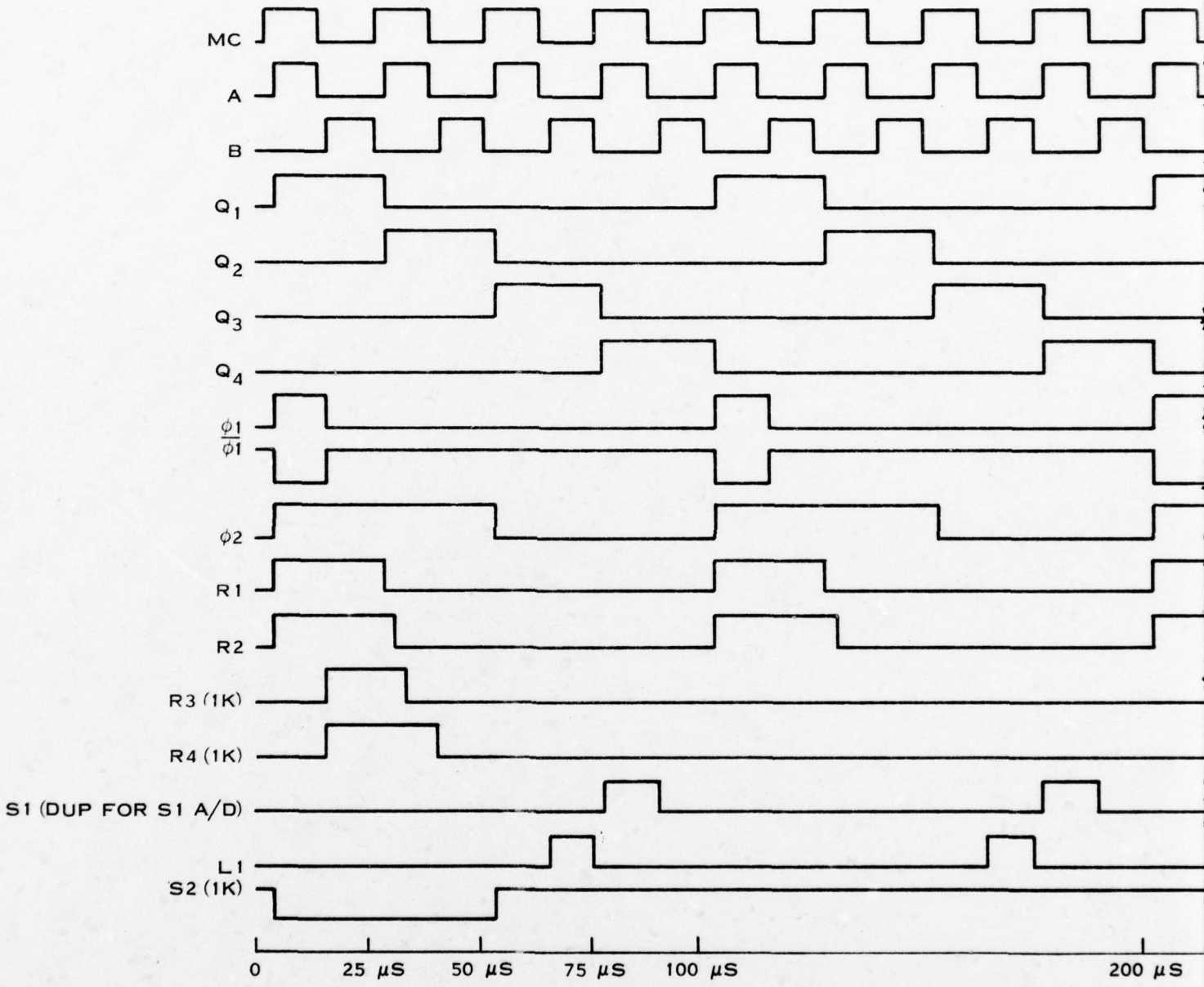
Figure 23. MOS to TTL Output Buffers


MC
A
B
Q1
Q2
Q3
Q4
φ1
φ1
φ2
R1
R2
R3 (1K)
R4 (1K)
S1 (DUP FOR S1 A/D)
L1
S2 (1K)
0
25 μS
50 μS
75 μS
100 μS
200 μS

224444

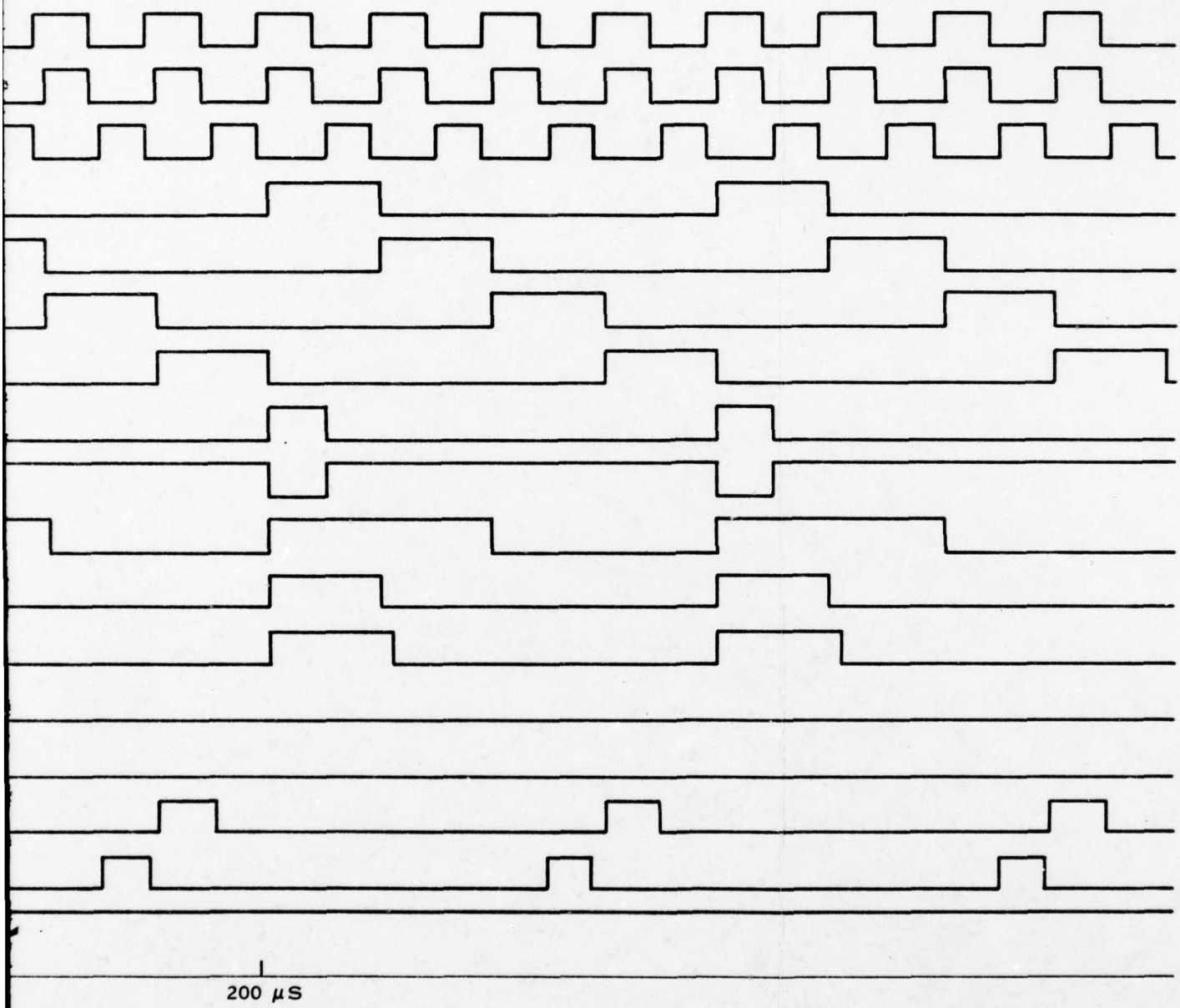
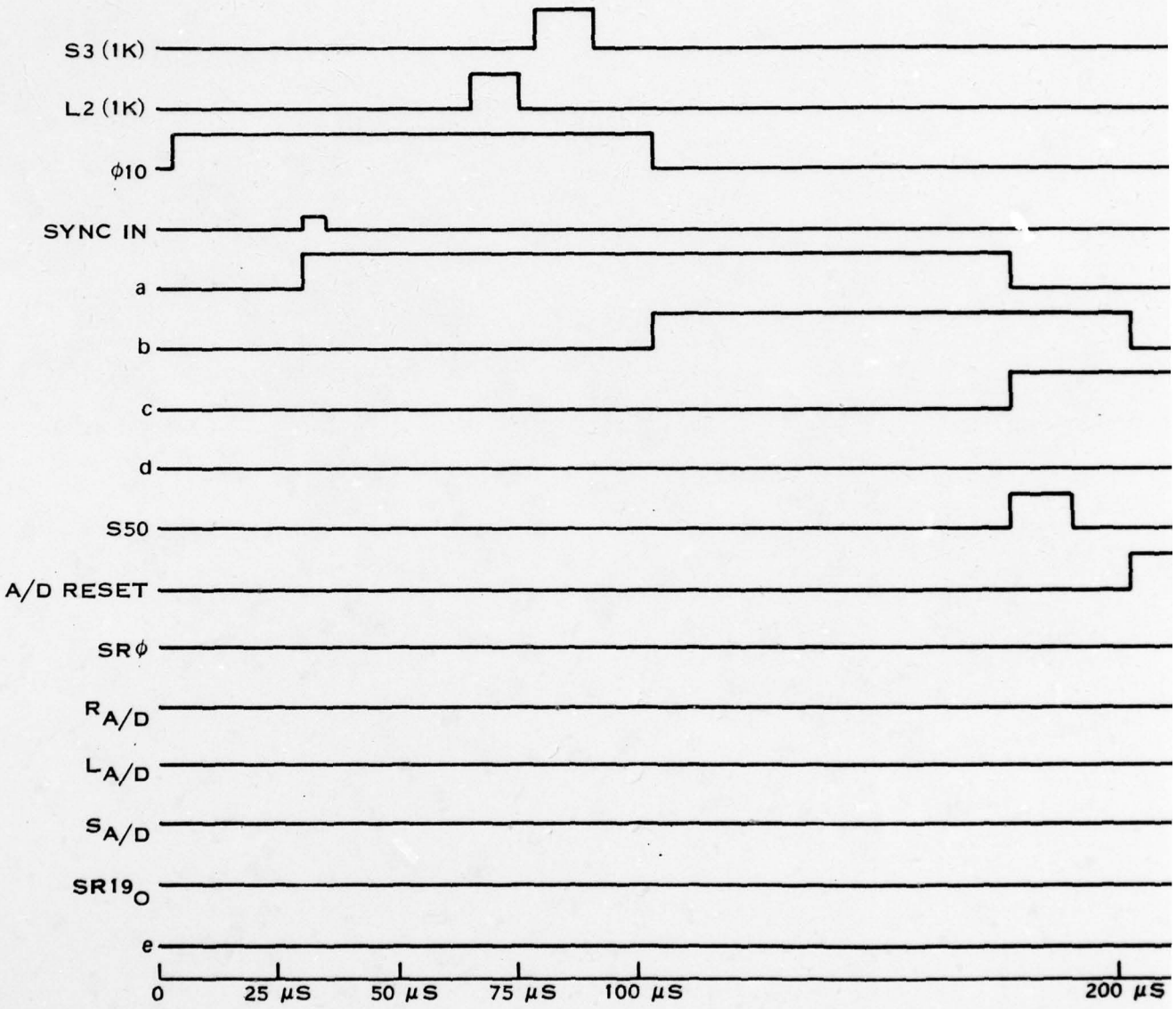


Figure 24. Analyzer Timing (Sheet 1 of 2)


S3 (1K)
L2 (1K)
ϕ10
SYNC IN
a
b
c
d
S50
A/D RESET
SRϕ
R A/D
L A/D
S A/D
SR19 O
e
0
25 μS
50 μS
75 μS
100 μS
200 μS

224445

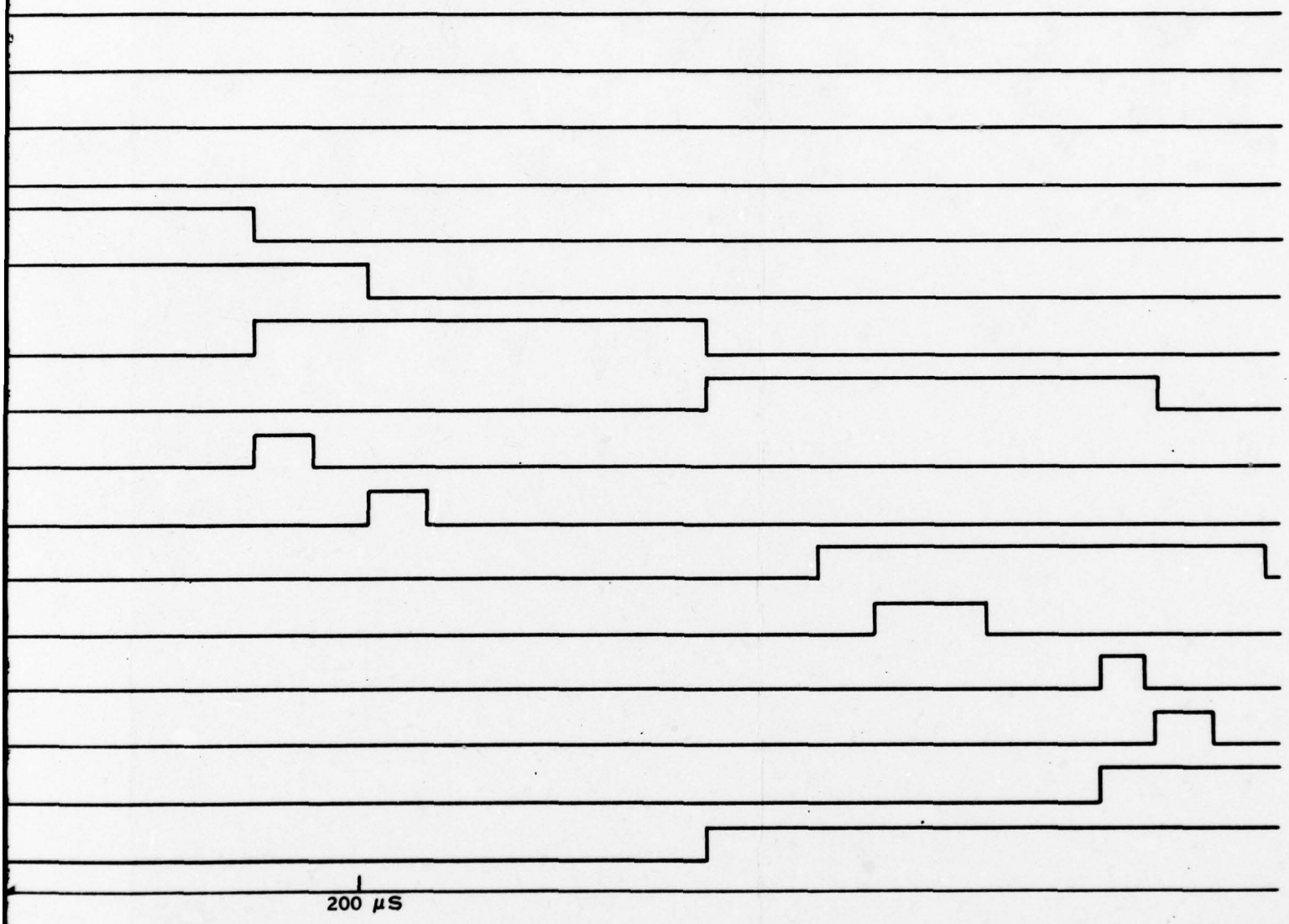


Figure 24. Analyzer Timing (Sheet 2 of 2)

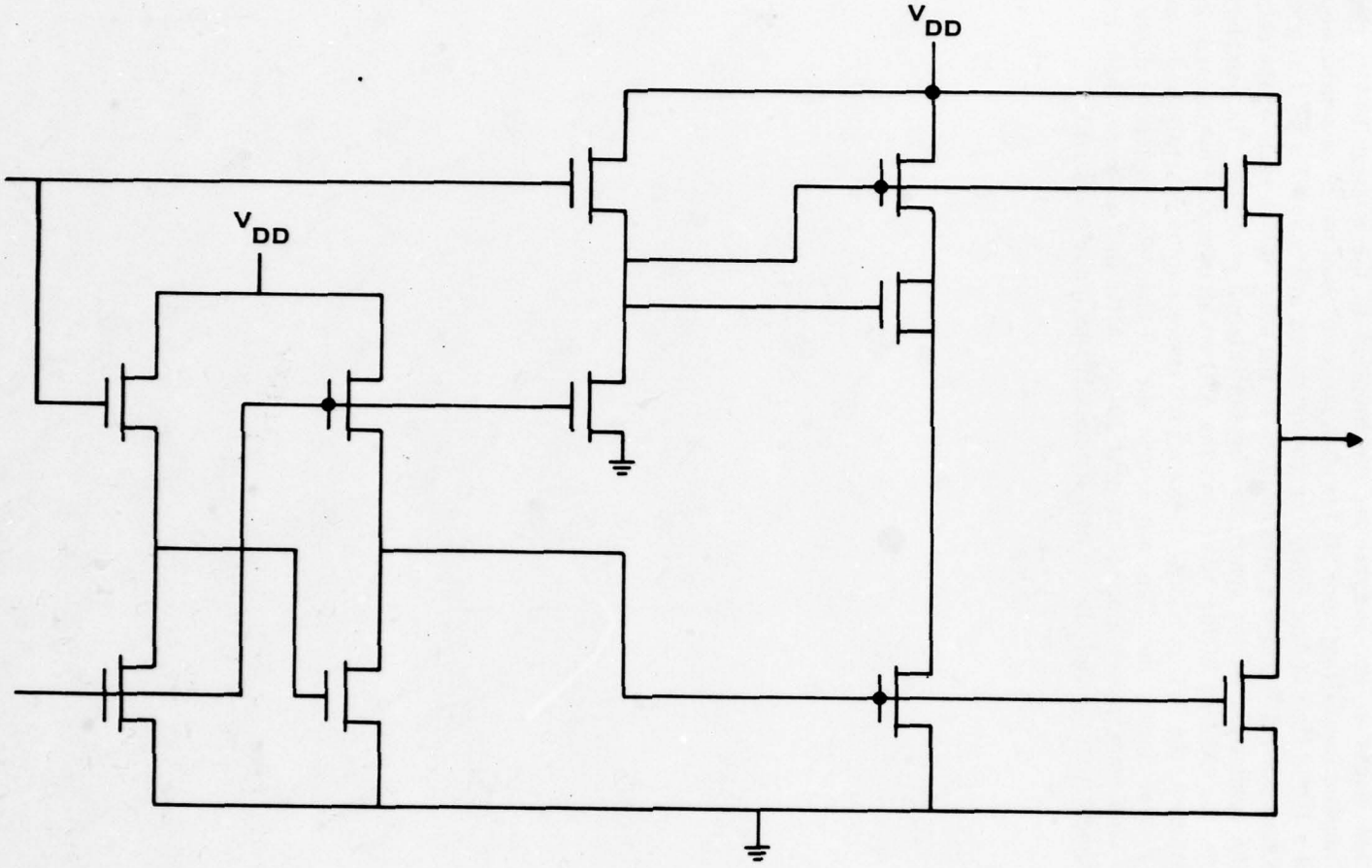


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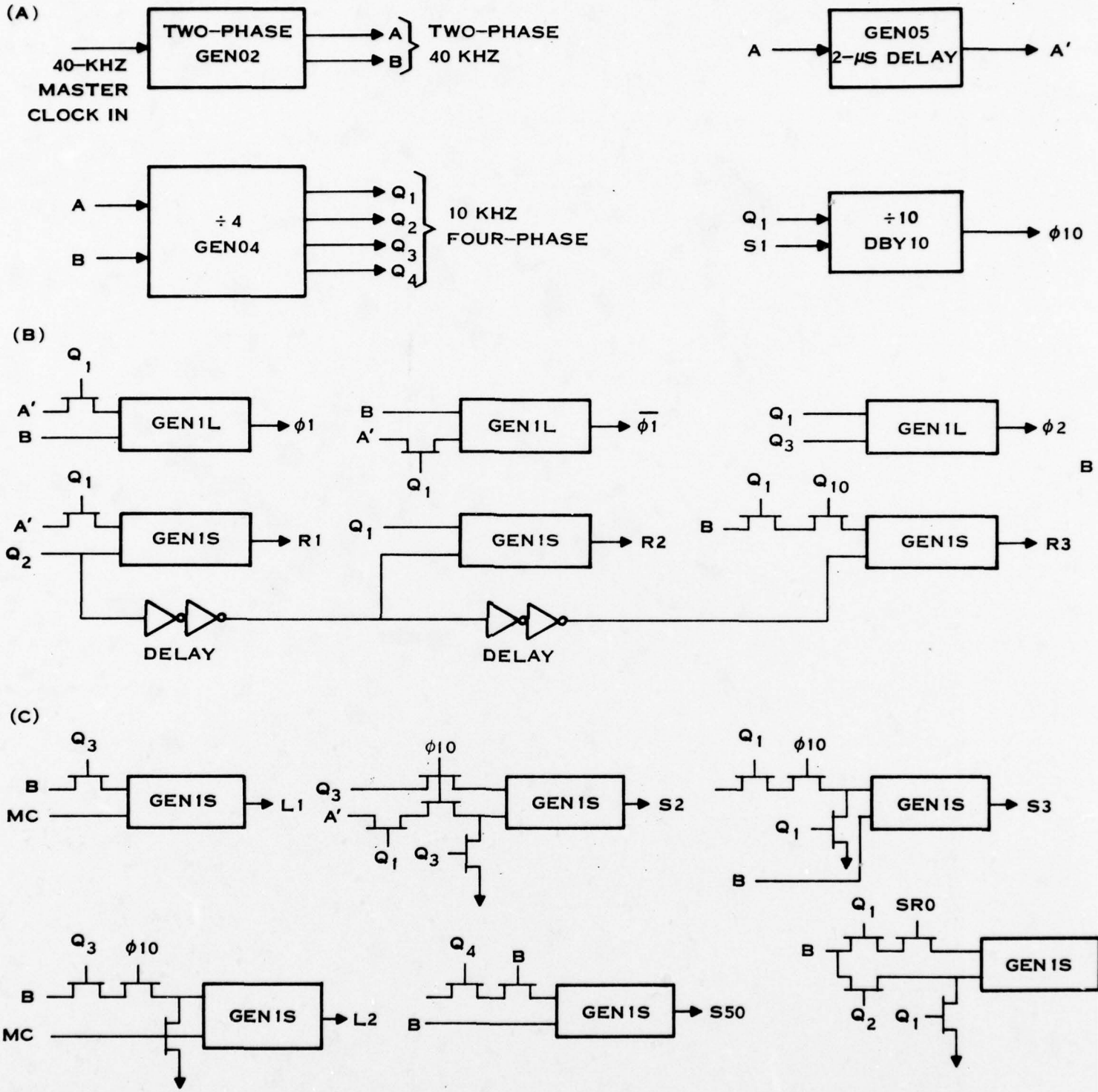
Figure 25. Clock Drive Circuit

2. Synchronization Circuit

All of the clocks in the analyzer are synchronized to the internal 10-kHz signal Q_1. However, the microprocessor that controls the analyzer is not required to be synchronous and it may command a frame start at any time. The circuit shown in Figure 27 is used to generate an internal frame start pulse S50 which is synchronized to the next 10-kHz cycle of the chip, which occurs after the application of the sync pulse by the external processor. The sampling of the channel outputs, the clocking of the MUX, and the A/D are all initialized by the sync input. As previously mentioned, the A/D provides a "data ready" strobe output signal for each conversion. On receiving a sync input, the chip will sample the 19 channels, provide 19 digital output words, and 19 data ready pulses, during the next 19 ms. After this sequence, there will be no more output signals from the chip until a new frame start sync pulse is received.


(A)
40-KHZ MASTER CLOCK IN
TWO-PHASE GEN02
A
B
TWO-PHASE 40 KHZ
A
GEN05 2-μS DELAY
A'
A
B
÷4 GEN04
Q1
Q2
Q3
Q4
10 KHZ FOUR-PHASE
Q1
S1
÷10 DBY10
φ10
(B)
Q1
A'
B
GEN1L
φ1
B
A'
Q1
GEN1L
φ1
Q1
Q3
GEN1L
φ2
B
Q1
A'
Q2
GEN1S
R1
Q1
GEN1S
R2
Q1
Q10
B
GEN1S
R3
DELAY
DELAY
(C)
Q3
B
MC
GEN1S
L1
φ10
Q3
A'
Q1
Q3
GEN1S
S2
Q1
φ10
Q1
B
GEN1S
S3
Q3
φ10
B
MC
GEN1S
L2
Q4
B
B
GEN1S
S50
Q1
SR0
B
Q2
Q1
GEN1S
224427

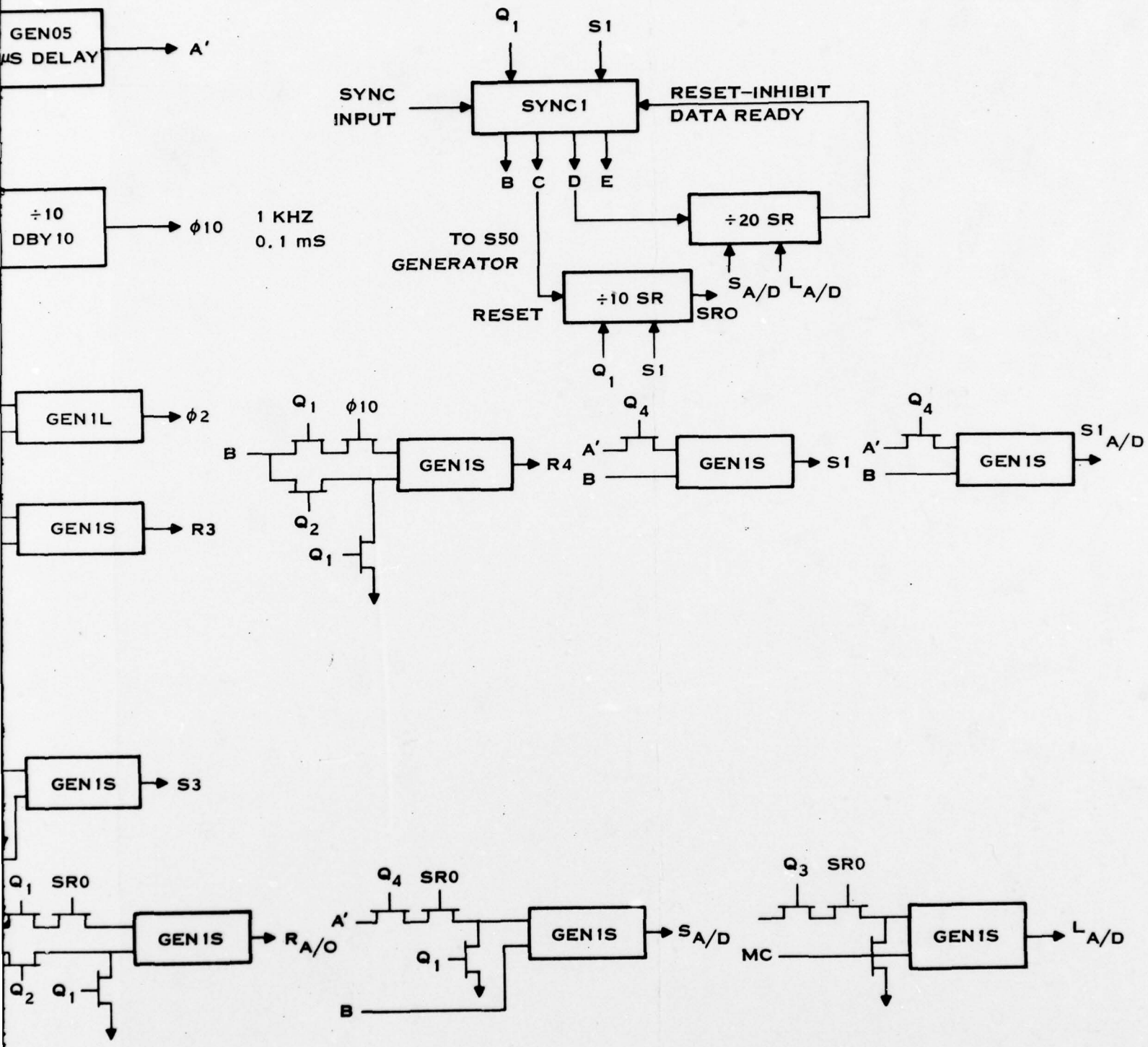


Figure 26. Derivation of Clock Signals From the 40 KHz Masters Clock n_c

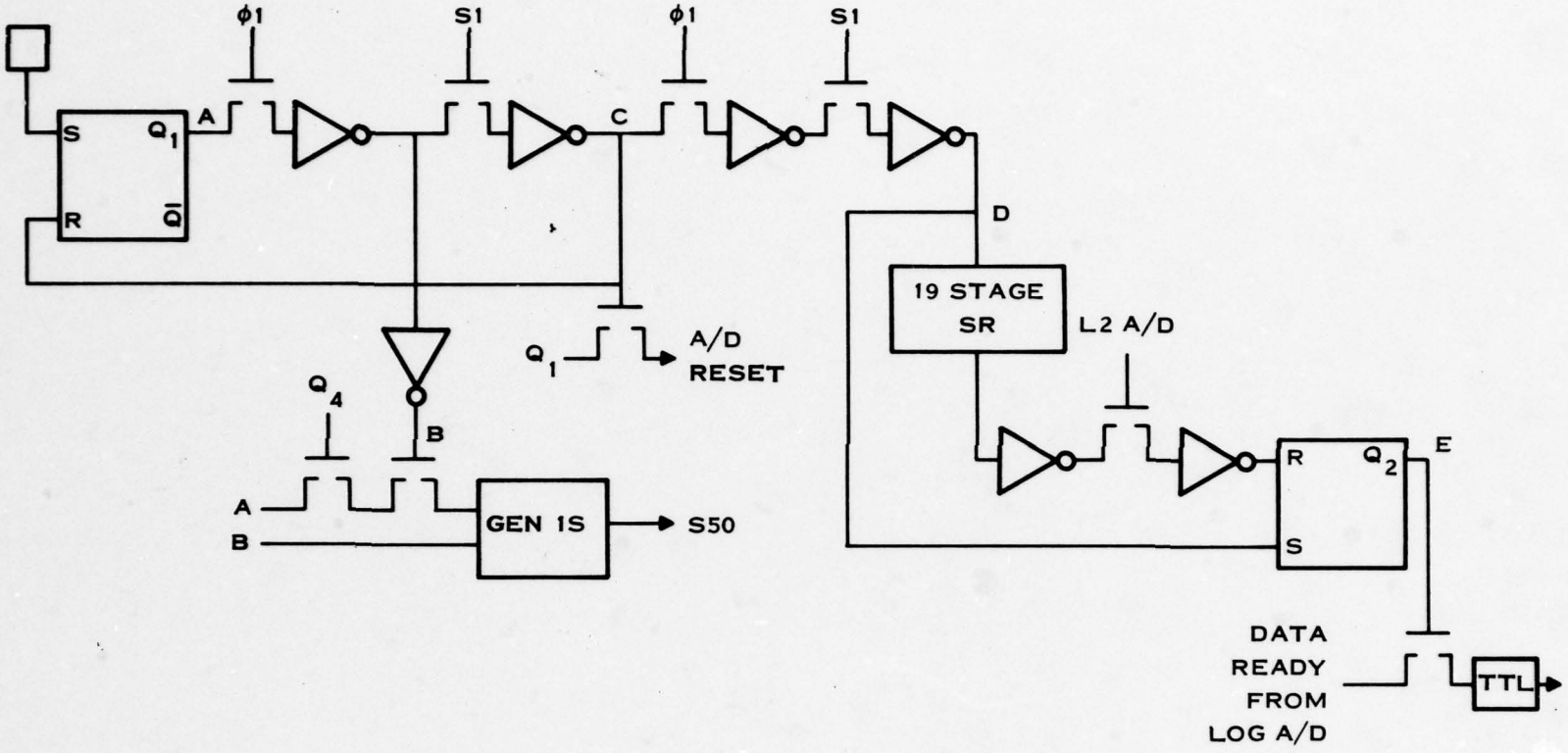


Figure 27. Sync Circuitry

SECTION III
VOICE SYNTHESIS IC

A. FUNCTIONAL DESCRIPTION

A block diagram of the speech synthesizer IC is shown in Figure 28(A). The input to this chip is a sequence of 20 eight-bit digital words at a rate of one per ms. One of these words controls the selection of voiced or unvoiced V/U excitation on the chip which is either a pseudorandom sequence or a pulse generator whose period is controlled by the data in the excitation word. This excitation word is recognized by nonzero bits in the three MSB positions and it also serves the function of speech frame synchronization. The remaining 19 words of input data all have zeros in the three MSB positions and the five LSB lines are directed to an anti-logarithmic D/A converter. The output of the D/A is demultiplexed to 19 sample-and-hold circuits, one for each of the synthesis channel. Each synthesis channel consists of a three-pole lowpass filter, a modulator, and a bandpass filter. The lowpass filter provides interpolation between the speech frames, and its output is used to modulate the amplitude of the excitation pulses which are applied to the bandpass filter of the corresponding channel. The outputs of the 19 channels are then summed together with every other channel having the opposite polarity in the sum. The reason for the antiphase summation is to avoid large output pulses that could result from coherent responses of all of the channels and would require a larger dynamic range in the output amplifier. As noted earlier, the relative phase of the different parts of the speech spectrum is not too important in speech perception.

The logic and clock circuits are described in Subsection III.B. The analog signal channel is described in Subsection III.C. and the lowpass and bandpass filters are described in Subsections III.D and III.E, respectively.

B. SYNTHESIZER SYSTEM TIMING

1. Clock System

As was done in the analyzer, all timing on the synthesizer bar is derived from the 40-kHz master clock input, the strobe input, and the state of the data inputs. The timing is shown in Figure 29. Nonoverlapping 40-kHz clocks ϕ_{41} and ϕ_{42}, the four 10-kHz clocks Q_{10} through Q_{13}, and the two 1-kHz clocks, Q_0 and Q_1 are derived from the master clock alone and are logically combined to form the pullup and pulldown pulses for the chip's clock driver circuits. These drivers use no static power and are designed to drive bus line and gate capacitance of 3 to 10 pF with approximately 100- to 200-ns rise and fall times. The function of each timing waveform is described below.

ϕ_{11}, ϕ_{12}	10-kHz clocks used in the lowpass filters (LPFs)
ϕ_1, ϕ_2	1-kHz clocks used in the lowpass filters (LPFs)
ϕ_{41S}, ϕ_{42S}	40-kHz clocks for the bandpass filters (BPFs)
ϕ_{41L}, ϕ_{42L}	Delayed 40-kHz clocks for the bandpass filters (BPFs)

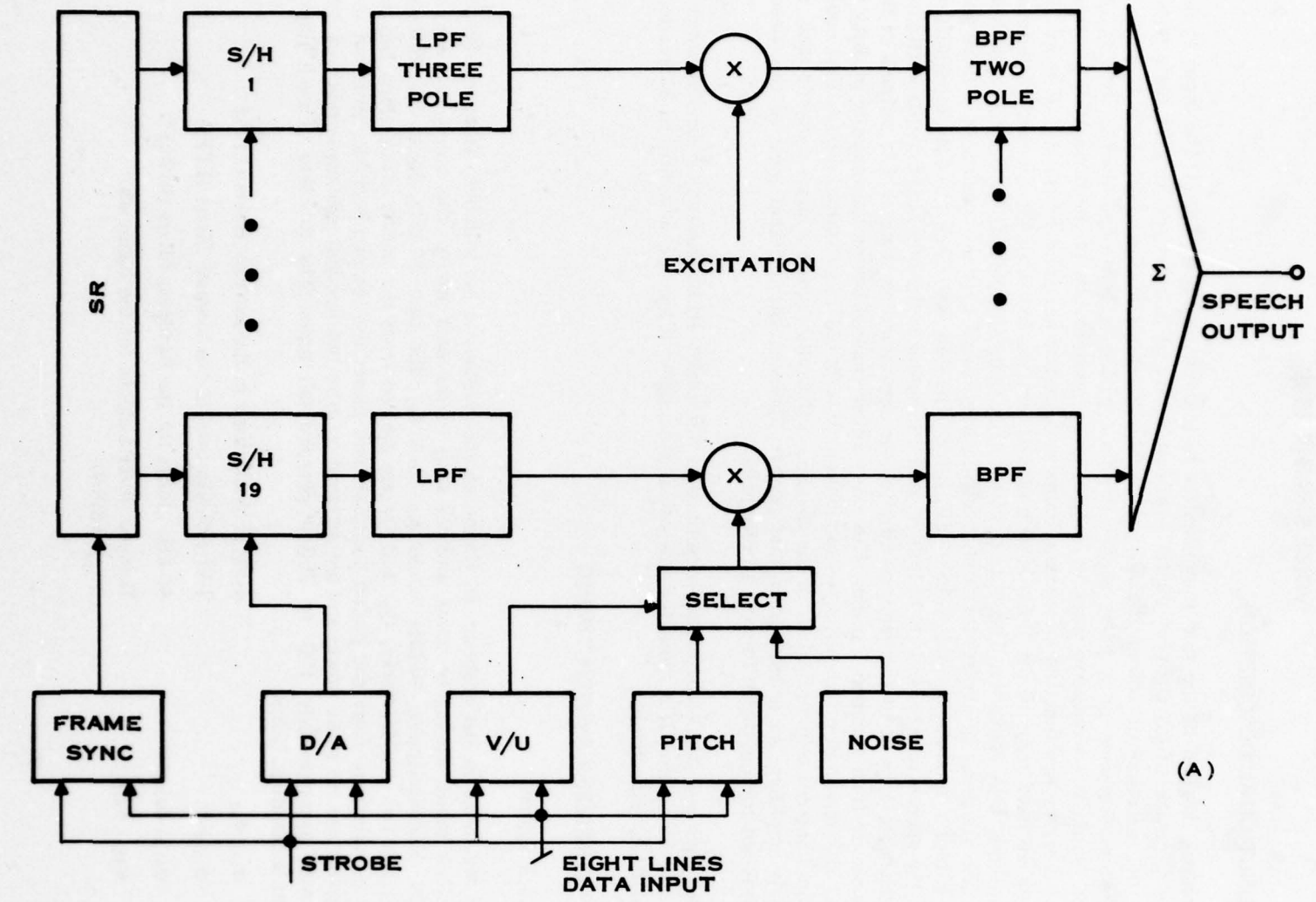


Figure 28. Speech Synthesizer (Sheet 1 of 2)

(B)

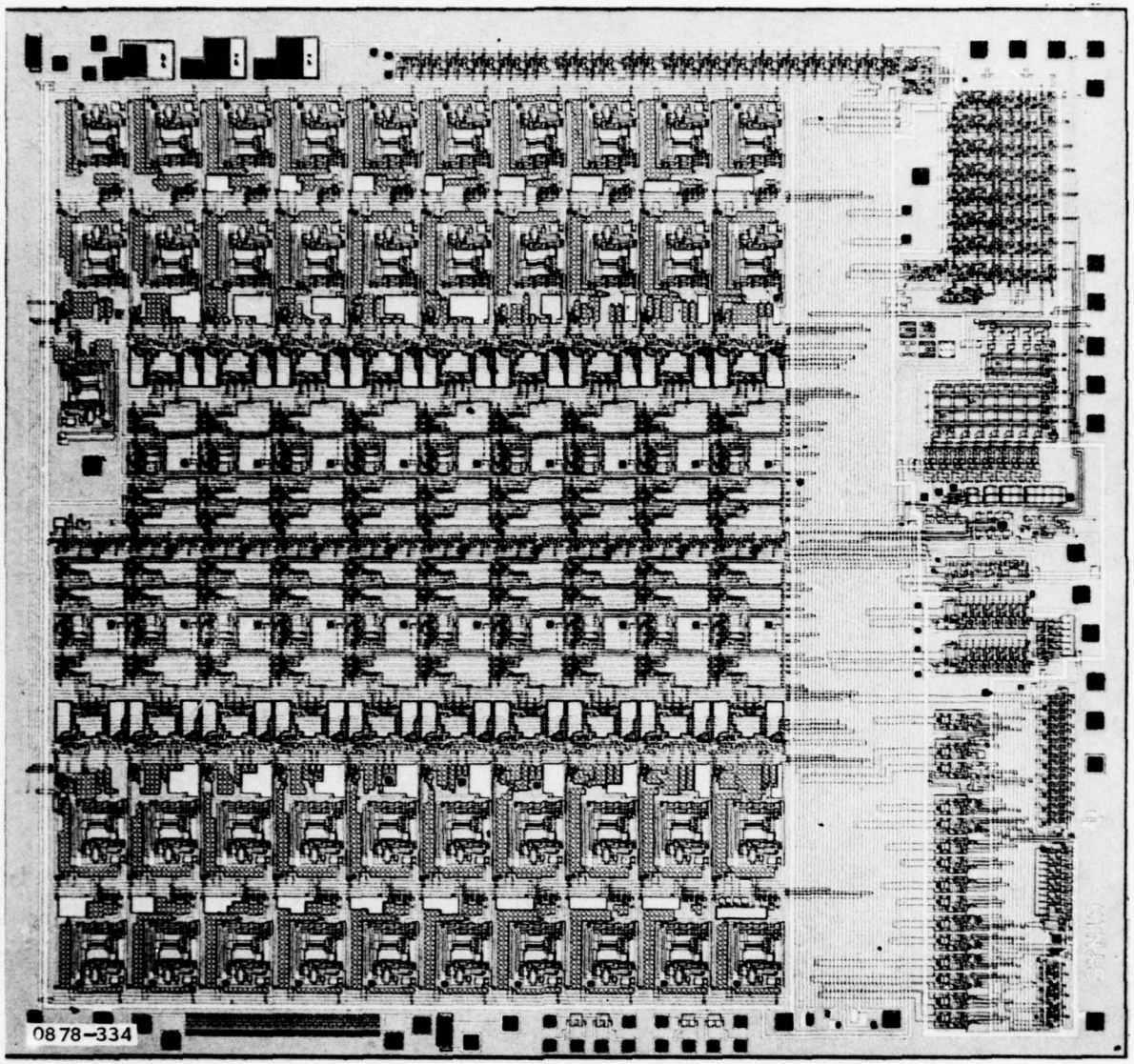


Figure 28. Speech Synthesizer (Sheet 2 of 2)

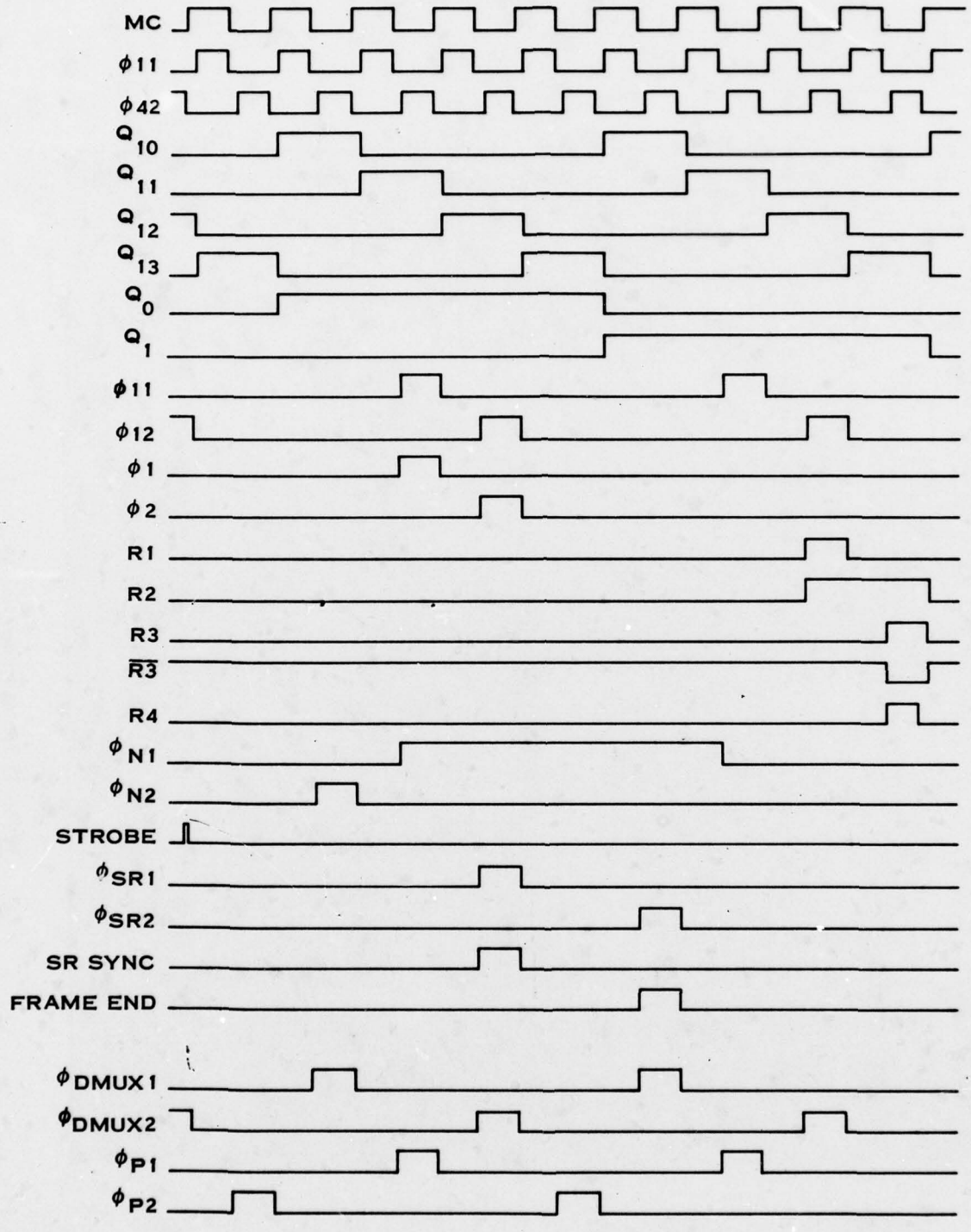


Figure 29. Synthesizer Timing Diagram

ϕ_{N1}, ϕ_{N2}	1-kHz clocks used by the noise generator. The 100-μs pulse ϕ_{N1} gates the noise generator outputs.
ϕ_{P1}, ϕ_{P2}	10-kHz clocks used by the pitch generator. The 100-μs pitch generator output pulse (P and $\overline{P}$) is triggered with the leading edge of ϕ_{P1}.
ϕ_{DMUX1}, ϕ_{DMUX2}	10-kHz clocks used in the sync generator to synchronize the demultiplexer to the strobe input.
ϕ_{SR1}, ϕ_{SR2}	≈1-kHz pulses that clock the demultiplexer shift register when the strobe input is pulsed. ϕ_{SR2} is gated by the SR outputs to generate the 50-Hz $S1_i$ sample pulses on the first sample-and-hold buffer.
Frame End	(Also S2 or $S1_{20}$) ϕ_{SR2} is gated by the 20th SR stage to generate S2. This is the sample pulse for the second sample-and-hold buffer. It also loads the new pitch word into the pitch counter.
SR Sync	This pulse resets the demultiplexer shift register with ϕ_{SR1} when it is determined that a pitch word is being input. This condition is satisfied when one or more of the three most significant data inputs are 1. Although this may not occur for each pitch word input, once the chip has been synchronized, it should remain in sync.
RD/A	Sets the D/A output to zero when the data inputs are all zero.
R1, *R2*, $\overline{R3}$, *R3*, *R4*	These clocks are used to eliminate any offsets in the analog chain and are described in Subsection III.C.

The logic diagrams for these clocks are shown in Figure 30. The same clock driver GEN1S that was used for the analyzer chip was used on the synthesizer.

2. Pitch Counter

An 8-bit counter is used to generate the pitch excitation. The counter is loaded when a frame-end pulse occurs as described above. The logic of the counter is shown in Figure 31, and the circuit schematic is shown in Figure 32.

3. Noise Generator Logic

The noise generator circuit employs a 16-stage shift register with exclusive-OR feedback to generate a pseudorandom sequence of length $2_{16} - 1$ bits. The shift register is clocked at a 1-kHz rate. The logic diagram is indicated in Figure 33. The output of the last stage of the shift

register is used to control the polarity of a 100-μs pulse used to excite the filter bank of the synthesizer. A 1 output causes a positive noise pulse and a 0 output causes a negative noise pulse.

4. Voiced/Unvoiced Select

The presence of all 1s on the input data bus is used to indicate an unvoiced speech frame. The circuit of Figure 34 is used to detect this condition. The output of the input data inverters is strobed by the frame-end signal into a NOR gate. If any of the input lines is not a 1, the pitch counter output is gated out and the noise generator output is inhibited. Otherwise, the pitch is inhibited and the noise is enabled.

C. ANALOG SIGNAL CHANNEL

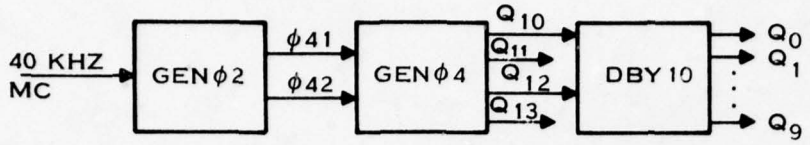
A block diagram of one channel of the synthesizer is shown in Figure 35. Because the sample-and-hold circuits and lowpass filters have unpredictable offsets, the channels are designed so that the offset for each individual channel is sampled, stored, and subtracted from the signal patch. This assures zero output from a channel when it has a zero-input level. The scheme is similar to that used in analyzer 1C. In the synthesizer circuit, offset is stored in three capacitors in the modulator circuit. The modulator is designed to output pitch or noise excitation pulses that are proportional in amplitude to the lowpass filtered input to the channel.

Five reset pulses are used to establish dc levels on high impedence nodes and to eliminate voltage offsets generated by the source followers in the sample-and-hold buffers and the lowpass filter. R2 clamps the D/A converter to the zero output state for the reset cycle. R1 then establishes the high impedence D/A output at V_{ref}. Next, $\overline{R3}$ (normally high) turns off and R3 (normally low) turns on, nondestructively bypassing all memory capacitors in the sample-and-hold buffers and the lowpass filter. At the same time, R4 turns on and off storing the combined offsets of the four previous source followers on each of the three capacitors in the excitation modulator. Finally, R3 returns low and $\overline{R3}$ high, restoring the memory elements to the circuit and R2 turns off allowing the data to appear on the D/A output. In order to prevent a reset from occurring when a pitch pulse occurs, the inputs to the R3, $\overline{R3}$, and R4 generators are logically ANDed with the complemented pitch pulse $\overline{P}$. Because of the timing of the noise generator clock (ϕ_{N1} and ϕ_{N2}), a reset cycle cannot occur during a noise pulse.

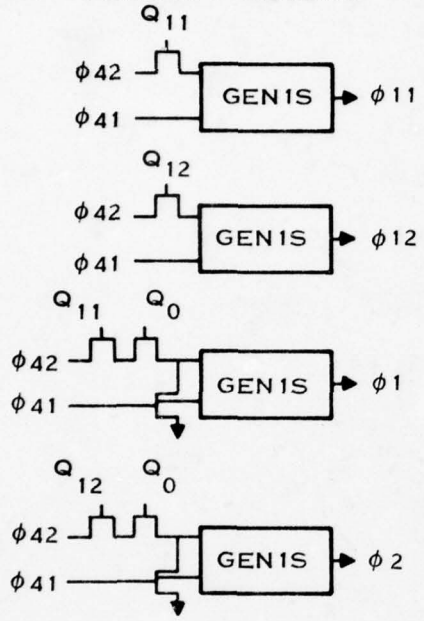
The modulator coupling capacitors are all left with their output side at a 7.5-volt reference level and their input side at the offset voltage of the previous stages at the end of the reset cycle. When either the pitch generator P or noise N+ is subsequently turned on, the appropriate capacitor is reconnected to the output of the lowpass filter and a pulse appears at the buffer output that is proportional to the lowpass filter output voltage at that particular time. The capacitor for negative noise pulse is connected with the opposite polarity of $\overline{N}-$ and N– so that negative pulses are produced when the N– signal is turned on.

D. LOWPASS FILTERS

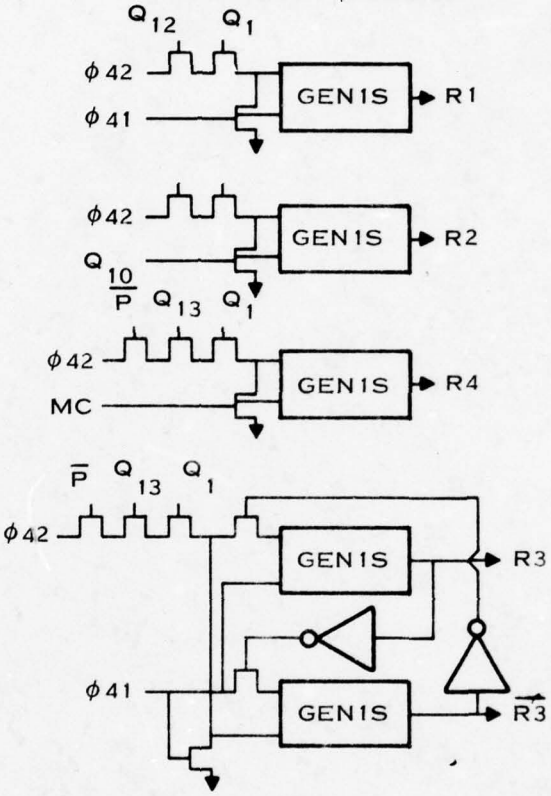
The lowpass filters have a design very similar to the analyzer lowpass filters. In the synthesizer, the three-pole Butterworth response with a 35-Hz bandwidth is used to interpolate from the 50-Hz sample rate of the sample-and-hold input up to the 40-kHz sample rate of the bandpass filters. Therefore, a 1-kHz sample rate is used in the first stage and a 10-kHz sample

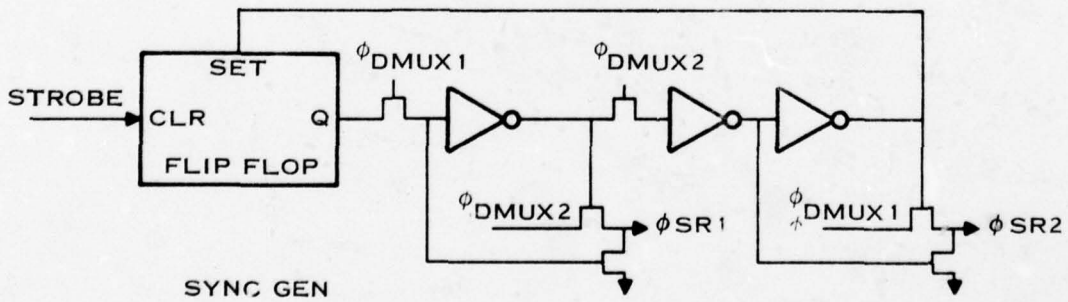


FOUR LPF CLOCKS



FIVE RESET CLOCKS





SYNC GEN

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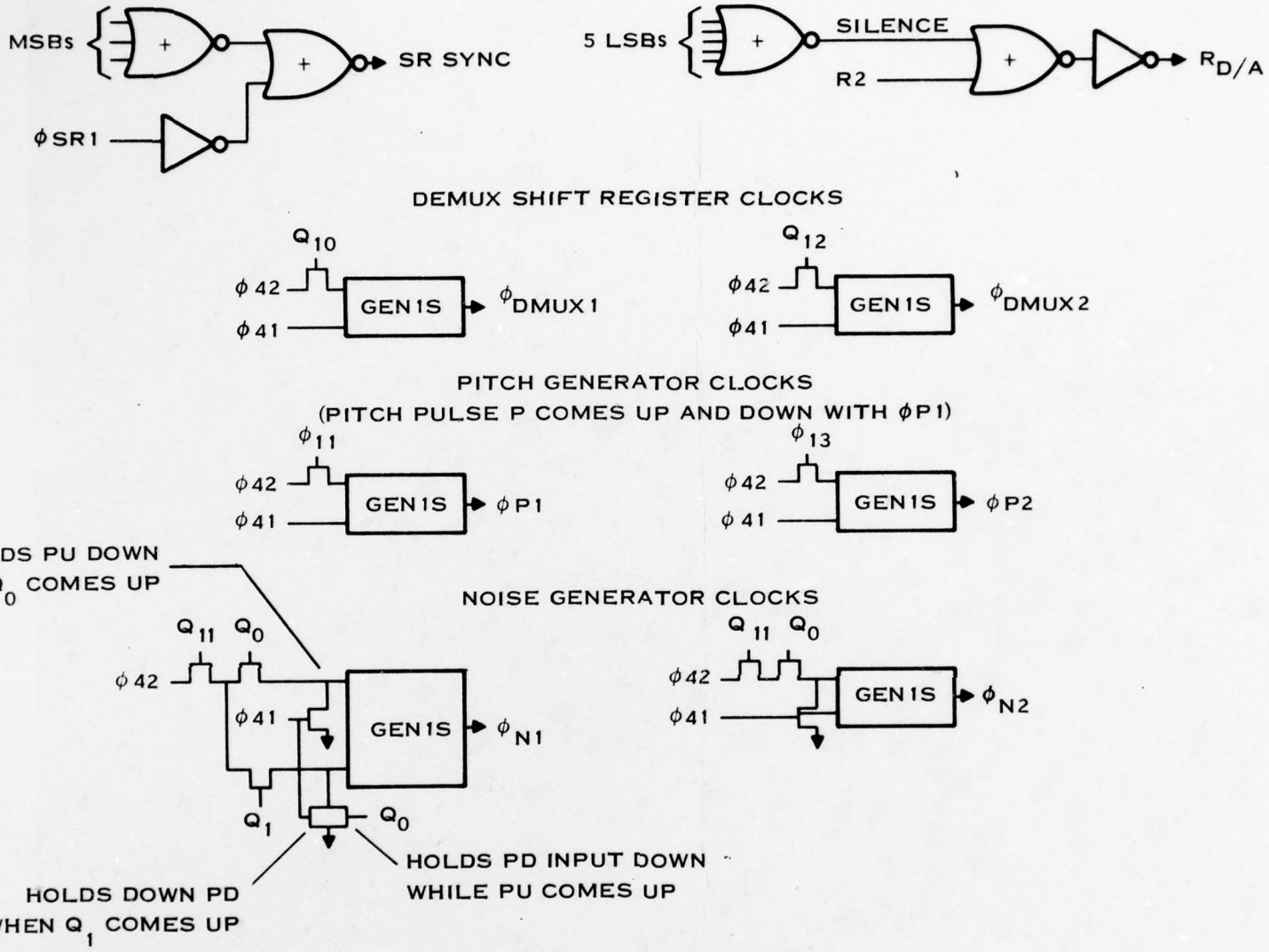


Figure 30. Synthesizer Clock Generation Logic

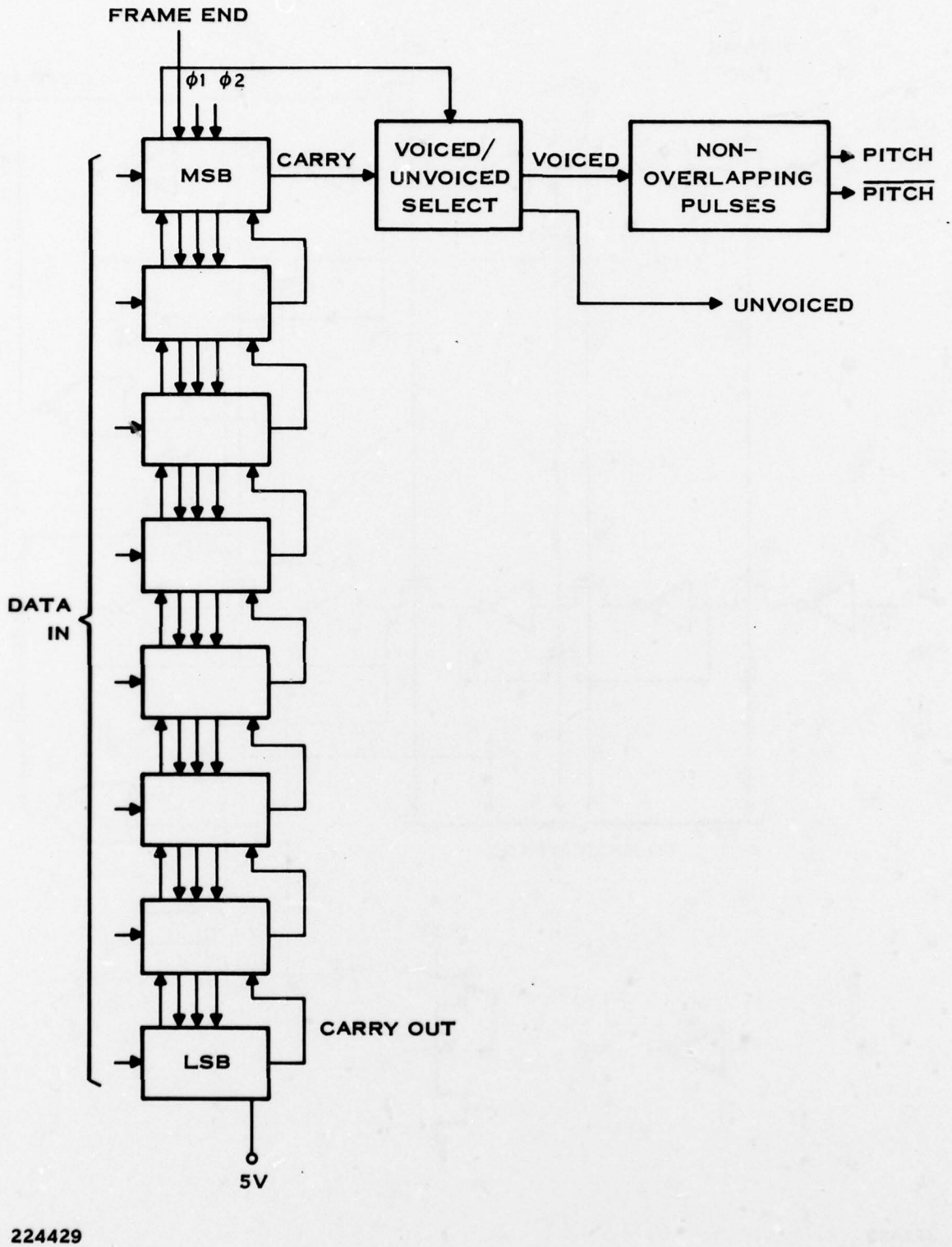


Figure 31. Pitch Counter Logic Diagram

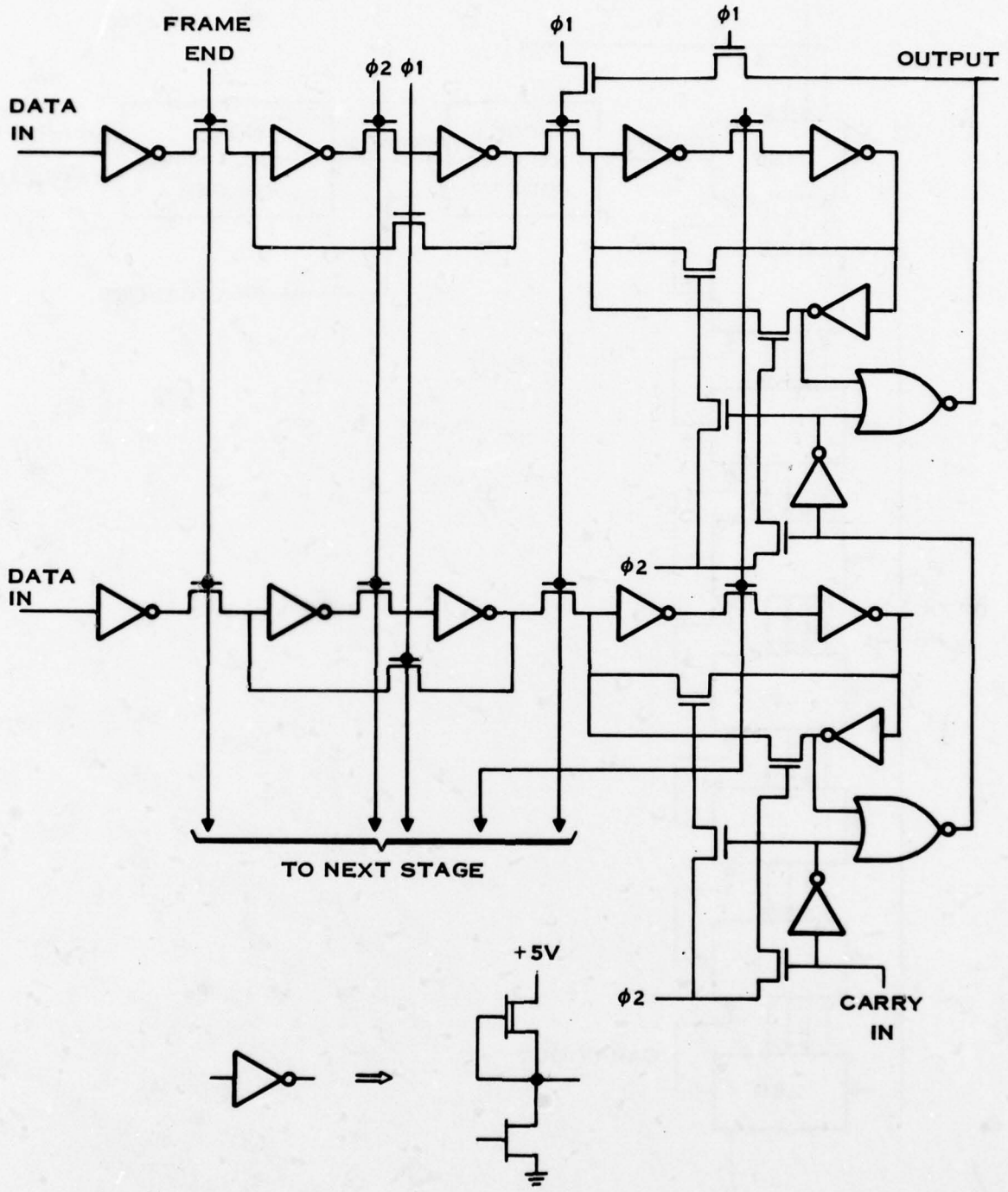
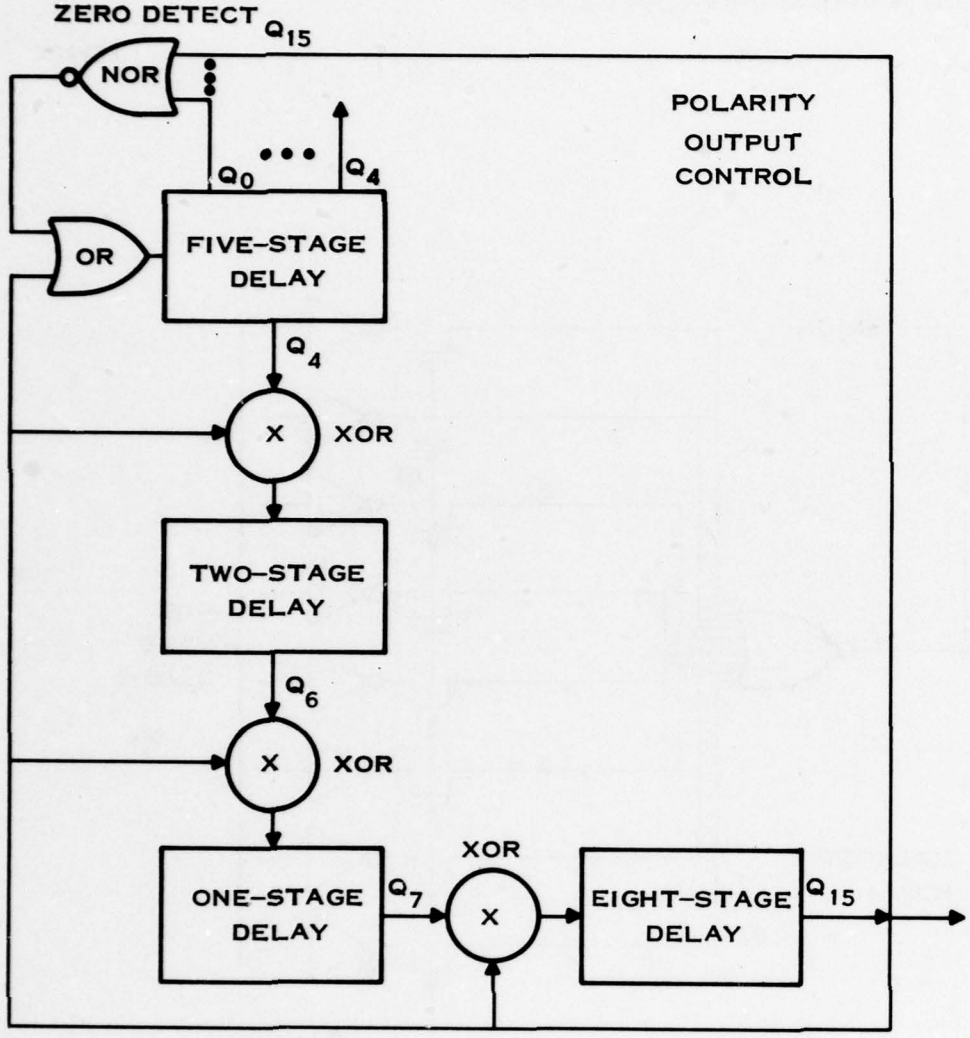
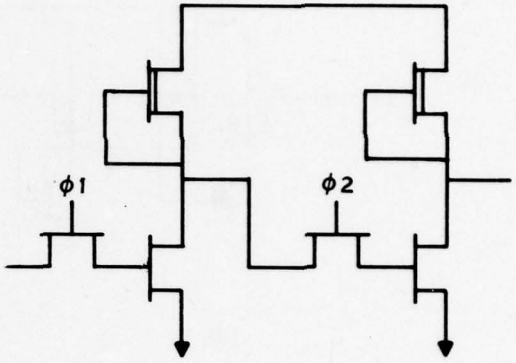


Figure 32. Last Two Stages of the Pitch Counter Circuit





ONE DELAY STAGE

Figure 33. Noise Generator Logic

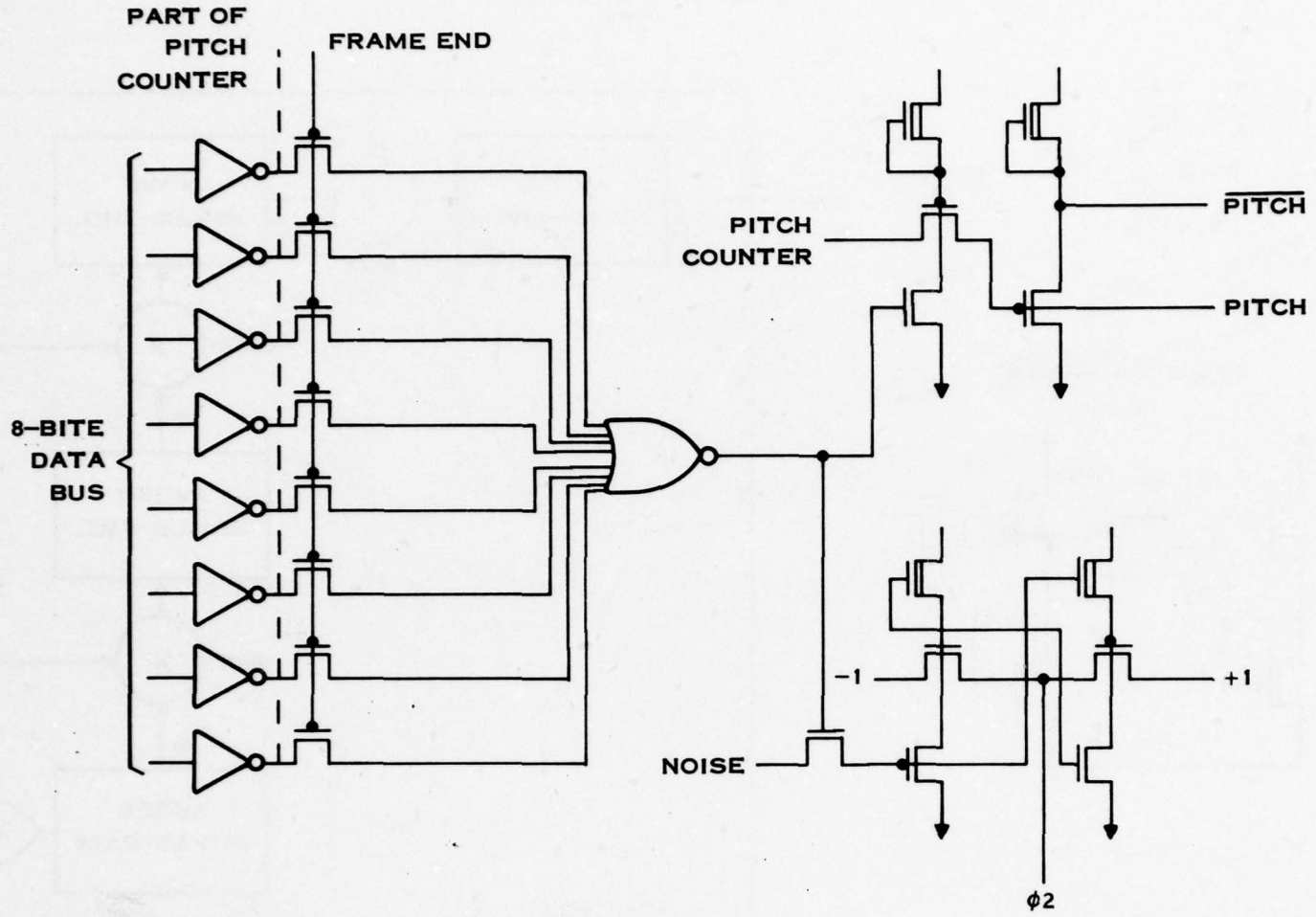


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Figure 34. Logic Used to Detect Unvoiced Frames and Generate Nonoverlapping Excitation Pulses

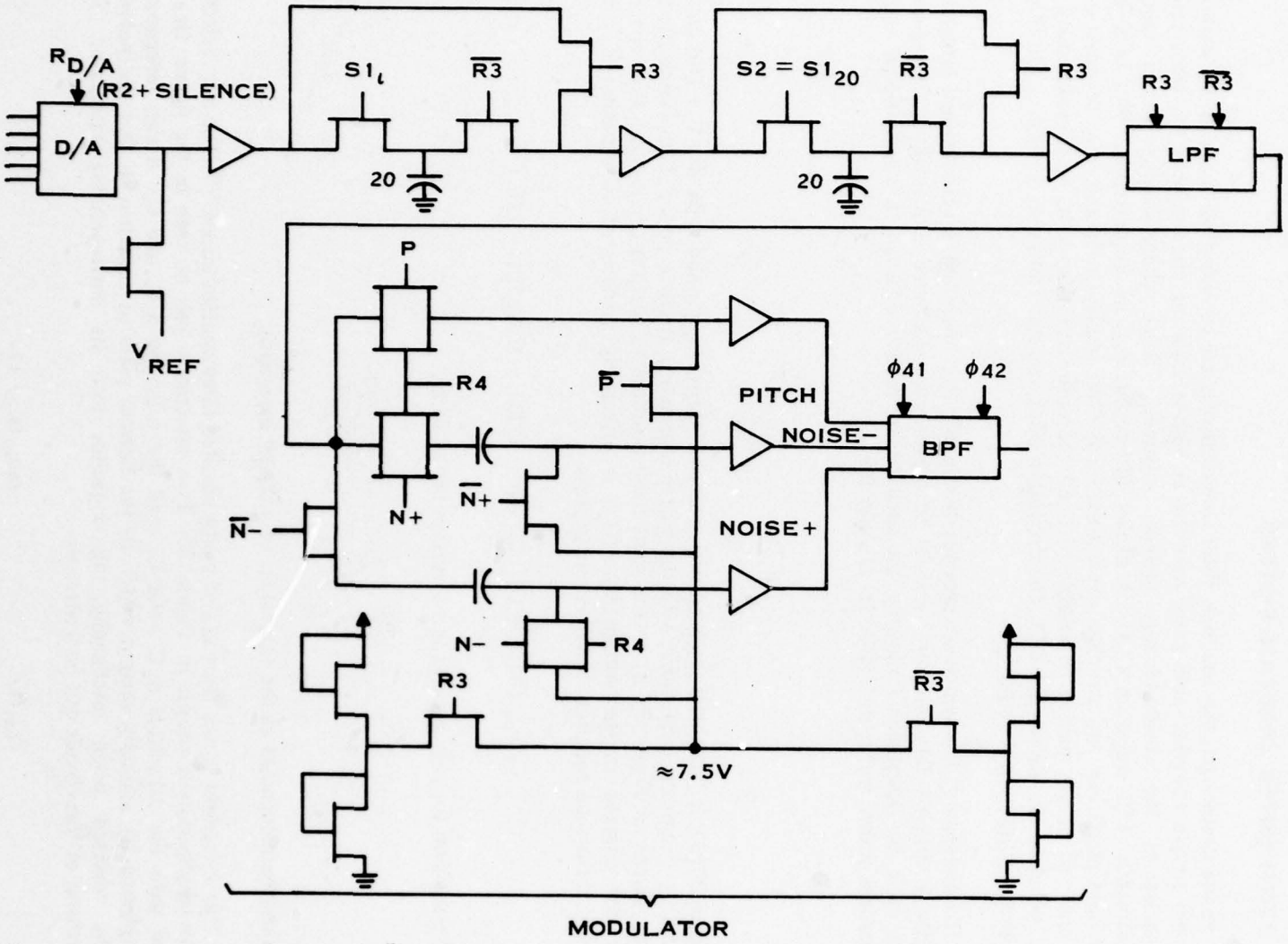

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Figure 35. Analog Signal Channel Showing Offset Correction and Modulation Scheme

rate is used in the second stage. The capacitor ratios are different than those in the analyzer filters because of the different sample rates. The circuit diagram is shown in Figure 36.

E. SYNTHESIZER BANDPASS FILTERS

In the synthesizer, the bandpass filter characteristics are simpler than those in the analyzer. They are simple complex pole pairs resulting in high-Q resonant circuits with the same center frequencies as the corresponding analyzer channels. These characteristics would require approximately 150 stages in CCD transversal filters, but can be implemented with only two operational amplifiers and switched capacitors. Each filter implemented this way occupies only 0.48 mm^2 of silicon making it possible to build the entire synthesizer IC in approximately 32 mm^2, including all clocks, the D/A, the excitation pitch counter and noise generator, the filters, and the summing output amplifier.

To understand the switched capacitor bandpass filter operation, a conventional integrator, and then a sampled data integrator and its Z-transform are examined, and finally a second-order section will be described. Following the analysis of reference seven, a conventional analog integrator is shown in Figure 37(A). Its transfer function is

$$H(\omega) = -\frac{1}{j\omega R_1 C_2} \tag{1}$$

In Figure 37(B), R_1 has been replaced with a double throw switch and capacitor C_1. This circuit operates in a sampled data mode with the switch alternating at clock period T_c between the left position shown in Figure 37(B) to the right hand position. In the nth clock cycle, the capacitor C_1 is first charged to the voltage v_{in} (nT_c) is effectively transferred to capacitor C_2. The following difference equation describes the process.

$$C_2\, v_{out}[nT_c] = C_2\, v_{out}\,[(n-1)T_c] - C_1 v_{in}[(n-1)T_c] \tag{2}$$

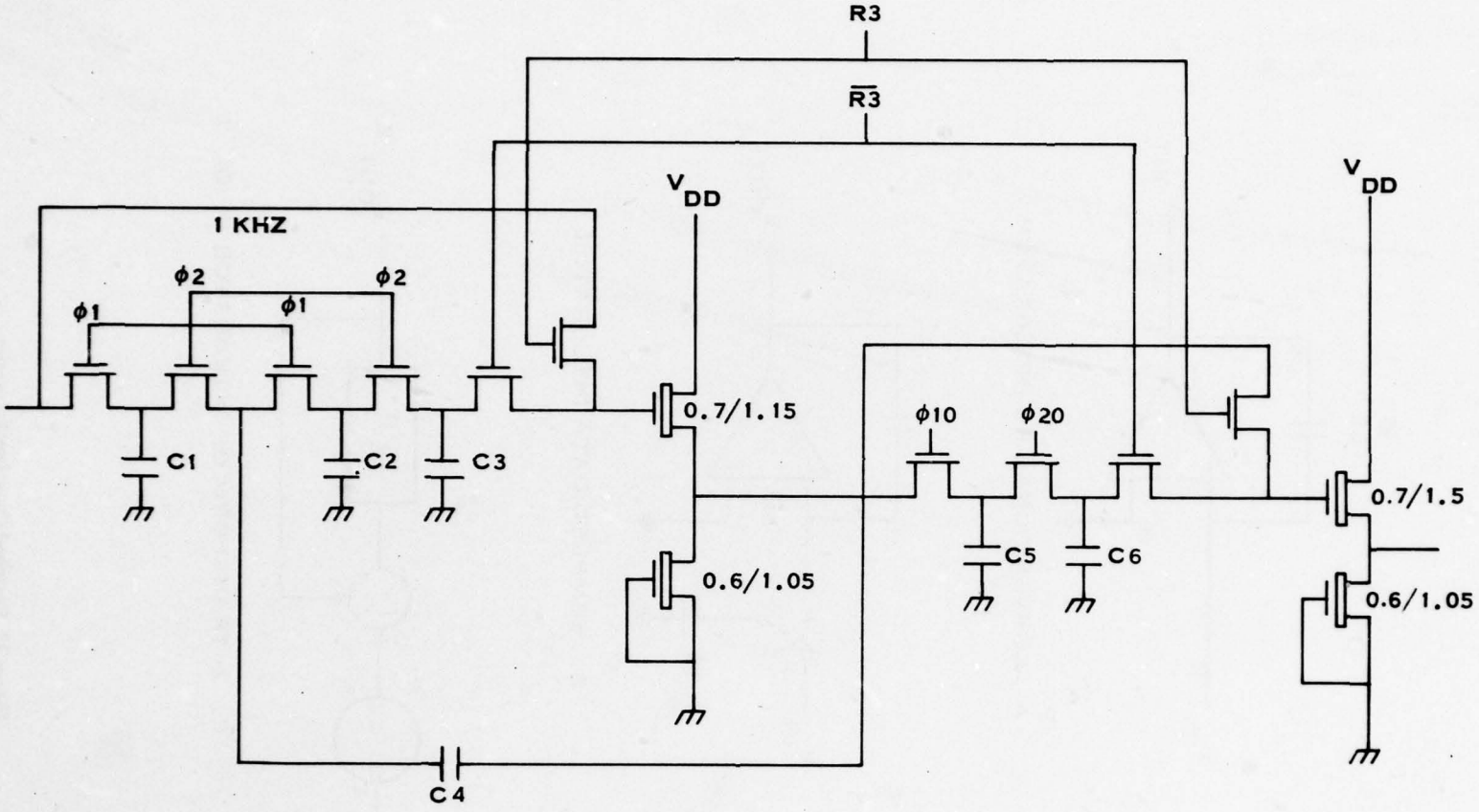
The Z-transform for this circuit can be written in the form

$$H(z) = -\frac{(C_1/C_2)\, z^{-1}}{1 - z^{-1}} \tag{3}$$

which can be recognized as the equivalent of a digital integrator.

This integrator forms the basis of many possible filter configurations.[7,10] The one selected for this application is shown in Figure 38. Two integrators can be seen in the figure. One is formed with the capacitors $\alpha_L C_L$ and C_L and the other by $\alpha_c C_c$ and C_c. A sign inversion is accomplished by adding a second switch to the bottom plate of capacitor so that the polarity can be reversed when discharging this capacitor into its corresponding integrator. The Z-transform of this circuit can be written as

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{-\alpha_i \alpha_c\,(z-1)}{z^2 - (2 - \alpha_c\alpha_T - \alpha_c\alpha_L)z + (1 - \alpha_c\alpha_T)} \tag{4}$$



C1 = 1.45 pF

C2 = 1.0 pF

C3 = 1.026 pF

C4 = 13.93 pF

C5 = 0.5 pF

C6 = 22.48 pF

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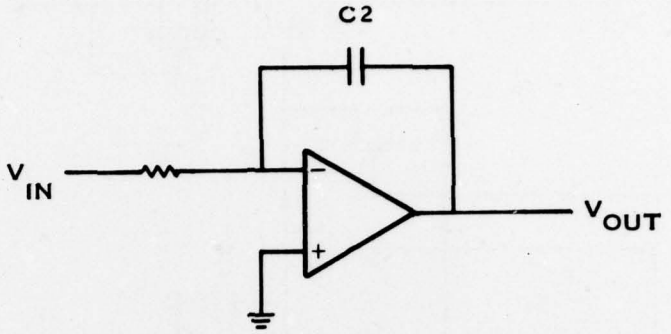
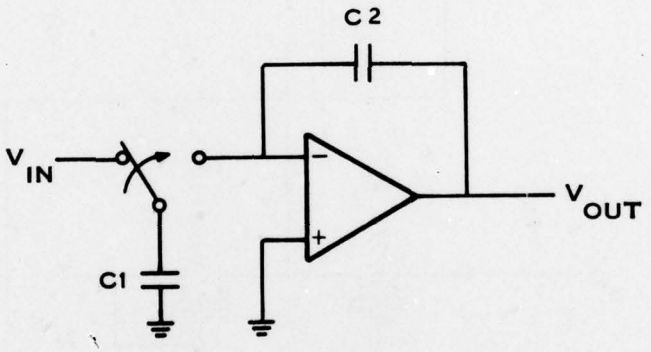
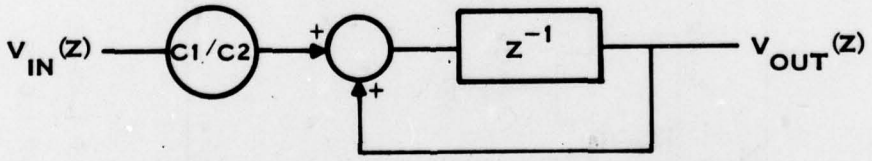
Figure 36. Synthesizer Lowpass Filter



A. CONVENTIONAL RC INTEGRATOR



B. SAMPLED DATA INTEGRATOR



C. Z-TRANSFORM OF INTEGRATOR IN (B)

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Figure 37. Switched Capacitor Integrator

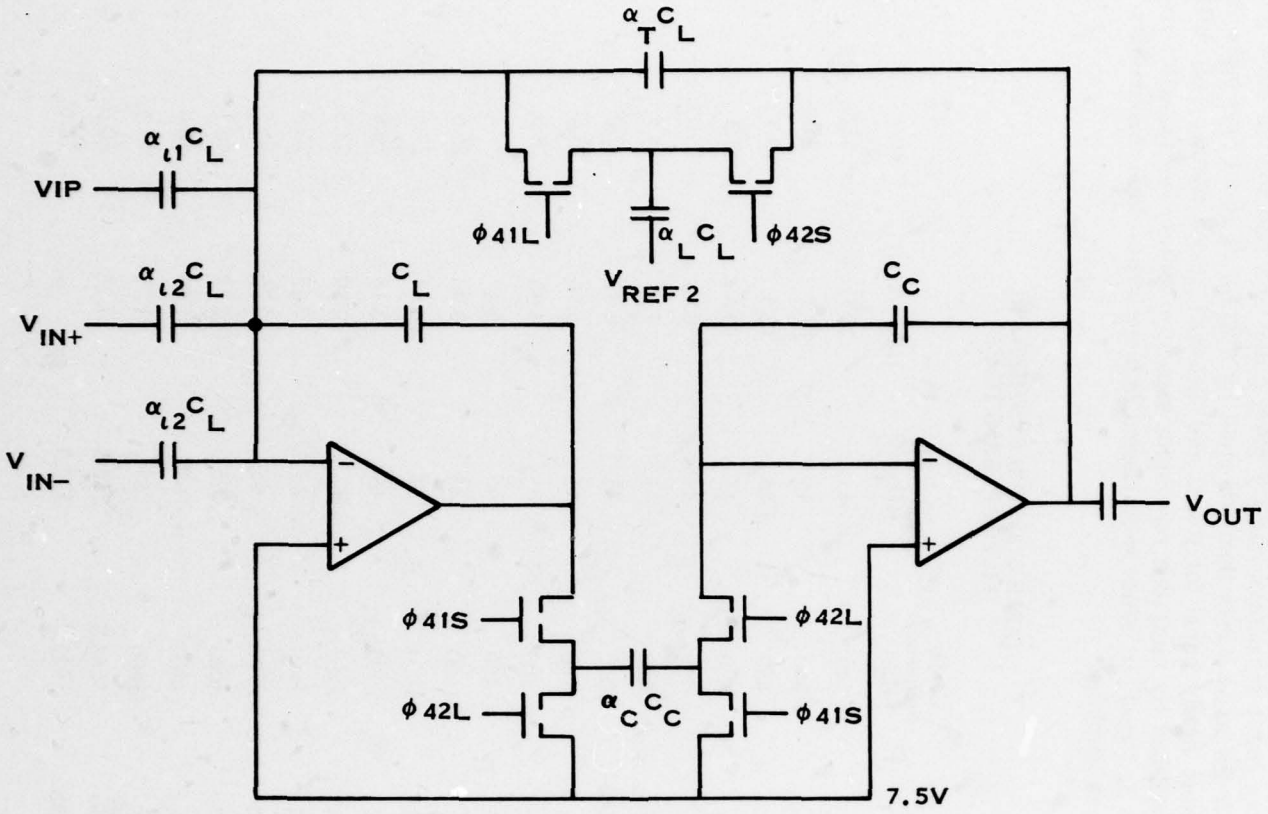

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Figure 38. Twopole Bandpass Filter Using Two Switched Capacitor Integrators

The Z-transform shows that the frequency response is independent of the absolute values of either C_c or C_L, but depends only on the capacitor ratios a_c, a_L, and a_T. MOS fabrication techniques allow the control of such capacitor ratios to a precision on the order of 0.1 percent, which is adequate for many filtering problems including the one described here.

There are three input capacitors, one for pitch pulses and two for the noise pulses. The channel gain is lower for noise pulses than for pitch by a factor of about 3 to make the energy in the excitation more nearly equal for voiced and unvoiced speech frames. This difference in gain is easily accomplished by using different input capacitor values. The capacitor ratio values are shown in Table 3. Capacitor values were chosen in these ratios while maintaining less than 10-pF loading on each amplifier.

TABLE 3. SPEECH SYNTHESIZER FILTER PARAMETERS

No.	Center Frequency (Hz)	Bandwidth (Hz)	$1/\alpha_L = 1/\alpha_C$	$1/\alpha_T$
1	240	45	26.5	5.33
2	360	45	17.7	8.00
3	480	45	13.3	10.7
4	600	45	10.6	13.3
5	720	45	8.84	16.0
6	840	45	7.58	18.7
7	1000	45	6.37	22.2
8	1150	45	5.54	25.6
9	1300	45	4.90	28.9
10	1450	45	4.39	32.2
11	1600	45	3.98	35.6
12	1800	65	3.54	27.6
13	2000	65	3.18	30.8
14	2200	65	2.89	33.8
15	2400	65	2.65	36.9
16	2700	65	2.36	41.5
17	3000	65	2.12	46.1
18	3300	65	1.93	50.8
19	3600	65	1.77	55.4
19a	3568.8	336.8	1.78	10.6
19b	3922.8	370.3	1.62	10.6

For pitch input, $\alpha_{i1} = \alpha_T \times 3.0$; for noise input, $\alpha_{i2} = \alpha_{i1/3.0}$ except on channels 1 and 2 where $\alpha_{i2} = \alpha_{i1/8}$.

For unvoiced speech frames, the 19th channel is switched to a cascade of two second-order sections as shown in Figure 39. For voiced frames, the pitch pulses are applied to the second-stage input, which has the characteristics shown under filter 19 in Table 3. When the unvoiced (UV) line goes high, the second-stage filter ratios (a_T and a_L) are switched to the characteristics labeled 19a in Table 3. In this case, the noise input is applied to the first stage filter 19b.

1. Operational Amplifier

The key to successful switched capacitor filters is an NMOS operational amplifier with low power and small silicon area. Recently, various NMOS amplifier designs have been reported[11,12] and the design of the amplifier used in the bandpass filter has incorporated ideas from the previous designs. However, this amplifier was optimized for small silicon area and low power. The amplifier circuit topology is shown in Figure 40. The principle specifications are listed in Table 4. There are 41 of these amplifiers on the speech synthesizer IC.

TABLE 4. OPERATIONAL AMPLIFIER CHARACTERISTICS

Power	4.3 mW
Gain open loop	1800
Bandwidth	1.6 MHz
Slew rate	2.2 V/μs
Load	10 pF
Phase margin	56 degrees
Silicon area	0.09 mm^2

2. Filter Performance

Typical performance measurements of the synthesizer bandpass filters are illustrated by the response characteristics shown in Figure 41. These measurements are made by injecting an input signal directly to the filter input using a probe and a small probe pad designed into the circuit for measurement purposes. In normal operation, these filter input points are not directly accessible. Although a large number of chips have not been statistically characterized, the center frequencies are typically within 20 Hz and bandwidths within 1 to 2 Hz of the design goals listed in Table 3.

F. OUTPUT SUMMING CIRCUIT

The same operational amplifier circuit that was used for the bandpass filters was used as the output summing amplifier. To avoid large spikes in the output, all the even-numbered filters were summed with a positive sign and the odd-numbered filters were summed with a negative sign. The output summing circuit is shown in Figure 42.

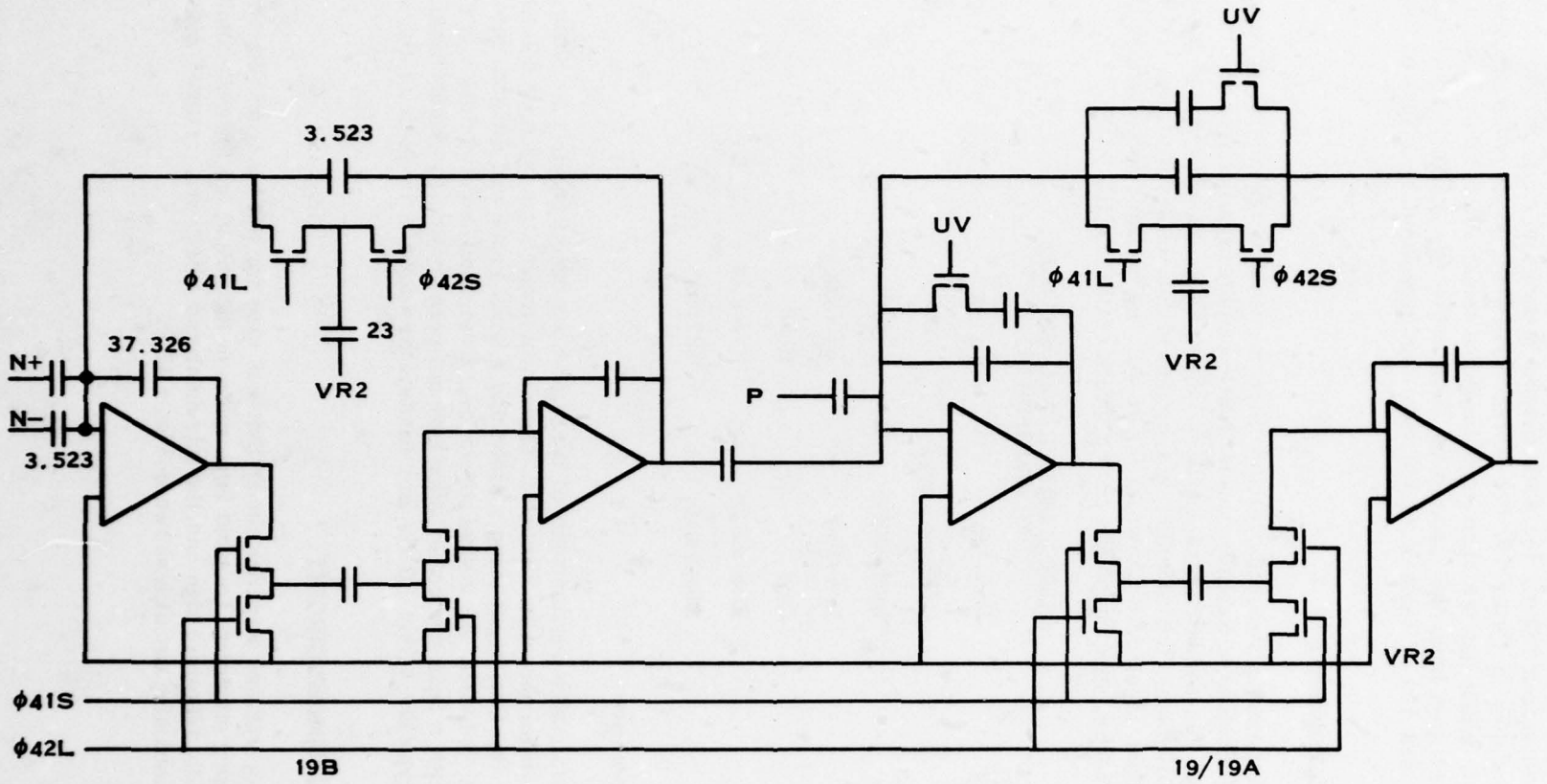


Figure 39. Second Order Bandpass for the Highest Frequency Channel

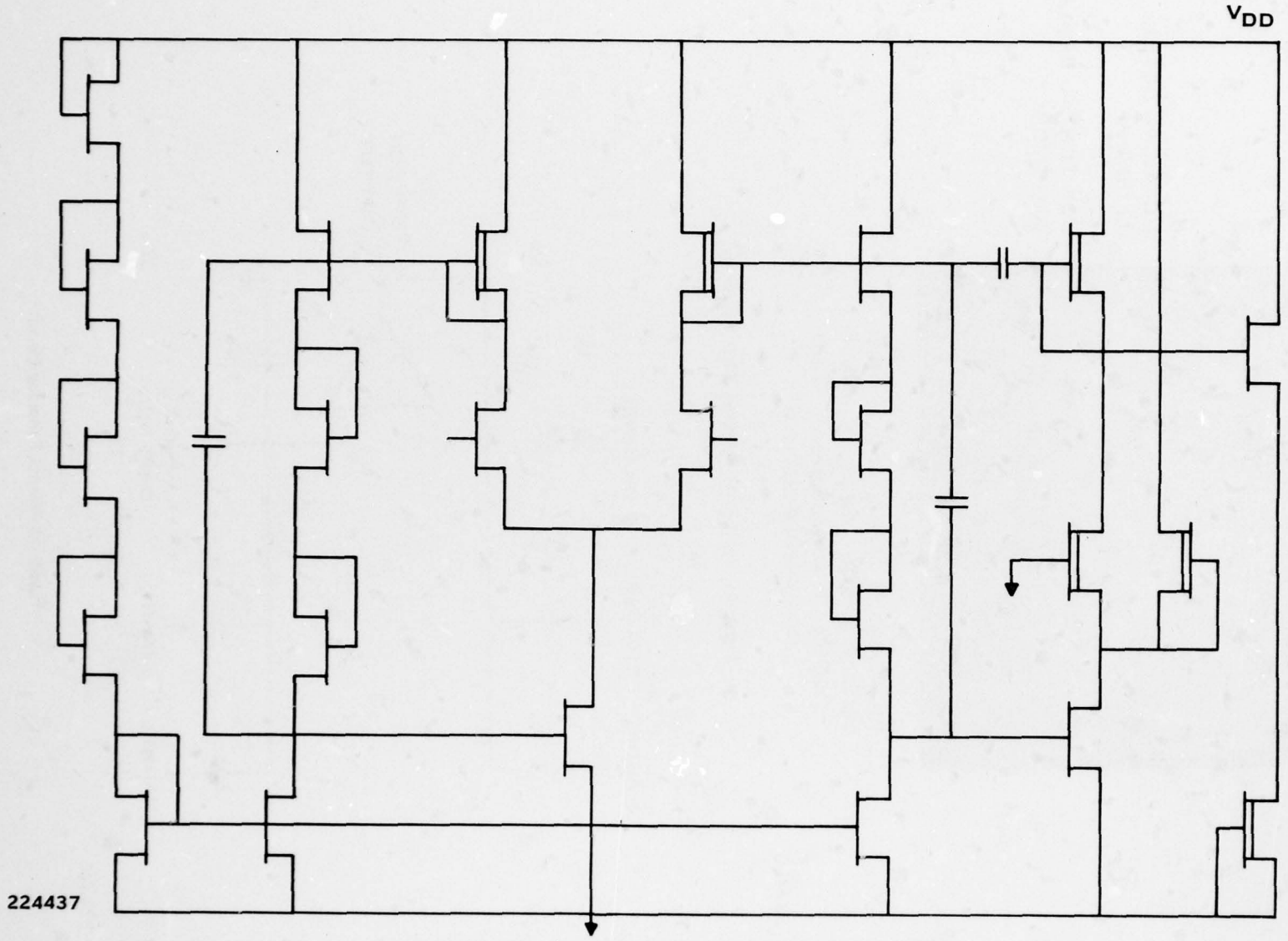
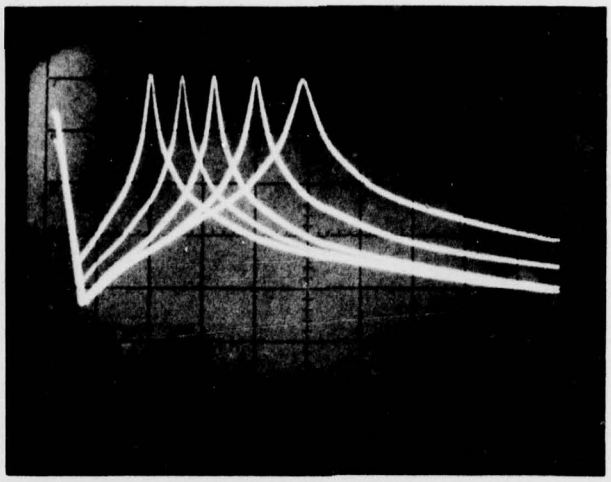


Figure 40. Operational Amplifier Used in the Switched Capacitor Filters



VERTICAL SCALE:
10 DB/DIV

HORIZONTAL SCALE:
500 HZ/DIV

FILTERS 7, 9, 11, 13, AND 15 WITH
CENTER FREQUENCIES OF 1000 HZ,
1300 HZ, 1600 HZ, 2000 HZ, AND
2400 HZ RESPECTIVELY

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Figure 41. Synthesizer Bandpass Filter Responses

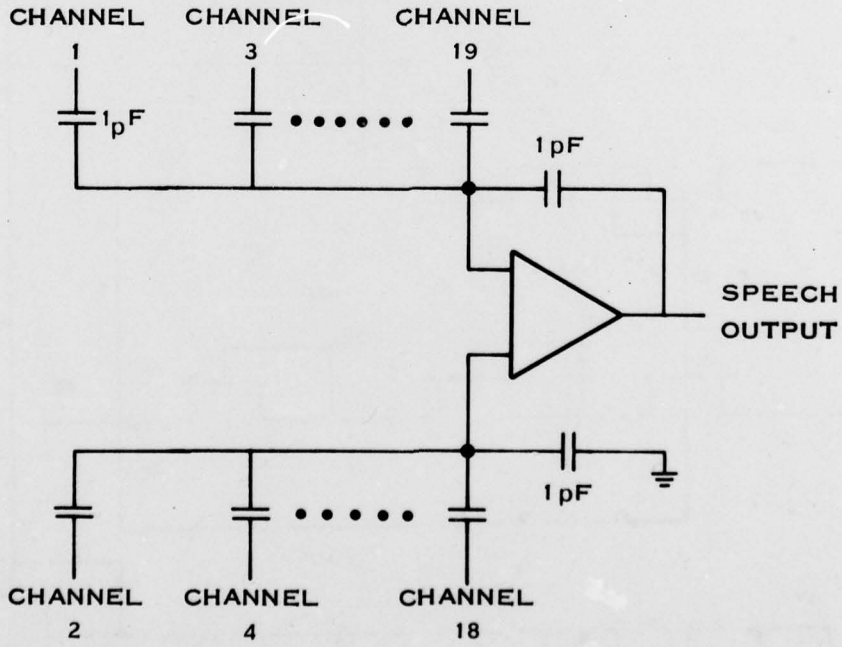

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Figure 42. Output Summing Circuit

SECTION IV
SUMMARY

This report has covered a description of the design of the two integrated circuits for the channel recoder. This report also has included some experimental evaluation data from individual functional elements within the ICs. This section summarizes the overall status of the chip development program and review the remaining problem areas.

In the first design iterations of each chip, successful demonstration proved that all of the circuit functions were operational, although there were minor layout errors in both the analyzer and synthesizer which have prevented testing of the complete function of the circuits as a single unit. These integrated circuits are both quite large and very complex and they employ circuit techniques not previously demonstrated in LSI form. Thus, it was not unexpected that another design iteration might be needed to achieve fully functional devices. The designs appear to be successful, because in the evaluations performed to date, there have been no major problems uncovered. The following subsections detail the status of each chip.

A. ANALYZER

The analyzer has had two design iterations. In the first pass effort, there was a parasitic capacitance in the CCD output amplifiers that caused them to fail. This was a photomask coding error that made the analog multiplexer circuit inoperative. A second pass was made and now functional chips are being tested both at the individual circuit level at Texas Instruments and with speech signals at Lincoln Laboratory. The problems identified so far are minor in that relatively straightforward corrections can be made to remedy them. The problems are listed below:

The analog multiplexer has an offset in the output corresponding to the lowest frequency channel. The cause is a capacitive coupling of a sync pulse that can be eliminated with a minor change in the bar layout.

The maximum signal level at the input that does not distort the signal is 2 volts peak to peak rather than 4 volts peak to peak as expected. We are investigating the cause of this limit even though there is still adequate dynamic range with its presence.

When the sync pulse from the controller is applied asynchronously to the analyzer's internal clocks, it causes a periodic offset pulse in the analog multiplexer output. This offset is a beating phenomenon between the internal clocks and the external sync rate. It has been experimentally verified that when the external sync causes the sampling of the analog outputs to occur in one particular 100-μs interval (of the possible 10 different positions) this offset occurs. It is caused by a coupling between the clock labeled S1 in Figure 24 and the sampling clock S50. A simple change in the logic can be made to eliminate this interaction.

We are using a -7-volt substrate voltage to keep parasitic field oxide transistors turned off. The MOS process is designed so that a -5-volt substrate voltage should be sufficient. The possibility of a processing error that might explain this discrepancy is being investigated. This is only a minor problem since the change in substrate supply voltage has very little effect on the active circuits.

The investigation of the analyzer IC is not completed, but at this time no other problems have been identified.

B. SYNTHESIZER

All of the individual components of the synthesizer appear to be operational. However, due to some of the problems listed below, the chip cannot be tested as a complete unit generating speech waveforms. Using probes to inject corrective signals at key points, we have demonstrated that we can generate pitch and noise pulses and control the amplitude of each of the synthesizer channels. The known problem areas are listed below:

The pitch counter circuit has a layout error. The circuit diagram of Figure 32 shows that the Frame End pulse is used to load new data into the latches at the counter input. If the Frame End pulse occurs after ϕ_1 and before ϕ_2, the circuit should perform as desired. However, due to an oversight, the Frame End pulse occurs after ϕ_2 and before ϕ_1 and the result is that the latch automatically overwrites the new data with its previous state. This problem can be corrected in probe testing by injecting an artificial FE pulse from off chip, but no bonding pad is available to avoid operating with probes. A very simple logic circuit change will allow the problem to be corrected.

The noise generator circuit has a floating mode that can allow it to malfunction. This problem requires the addition of one transistor to ensure desired operation. A minor layout correction will be necessary.

The switches in the D/A converter used to connect the bottom capacitor plates alternately between ground potential and the reference voltage of the converter are not capable of switching to the full voltage intended. The reference voltage was intended to be 10 volts, but the present limit is approximately 3.5 volts. The effect is to attenuate the output voltage range to 35 percent of the design goal. The problem can be solved by a minor layout correction. The D/A logic was supposed to operate on the 15-volt supply, but because of a layout error, it was connected to the 5-volt supply.

The switch that changes the Q of the 19a filter is inoperative because of a minor layout error. Thus, the filter remains always in the low Q (unvoiced) mode. A simple layout correction will remedy this problem.

C. RECOMMENDATIONS

In view of the relatively minor problems remaining to be corrected before the ICs can be tested with real speech signals, it appears that a successful vocoder demonstration is probable. More analysis should be done to make certain that all problems have been identified, so that the next pass at the chips will provide this successful vocoder demonstation. At this time, it appears that approximately 1 month of probing and analysis work should suffice to define all necessary connections. Approximately 1 more month will be required to implement these design corrections. After that, 2 or 3 months are required to fabricate new ICs. Allowing time for testing, about 6 months total are needed before the vocoder chips can be demonstrated in the system that has been designed and breadboarded at Lincoln Laboratory.

SECTION V
REFERENCES

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APPENDIX A

PINOUT DESCRIPTION OF CHANNEL VOCODER ICs.

A. ANALYZER

A description of the pin functions on the analyzer IC is shown in Figure A-1 and Table A-1. In this preliminary description, several adjustable voltages are shown. In all cases but the trimmer cable labeled MUX AMP BIAS, a fixed voltage will suffice in the final design of the chips. These voltage adjustments are presently included to help analyze circuit performance and optimize the final design.

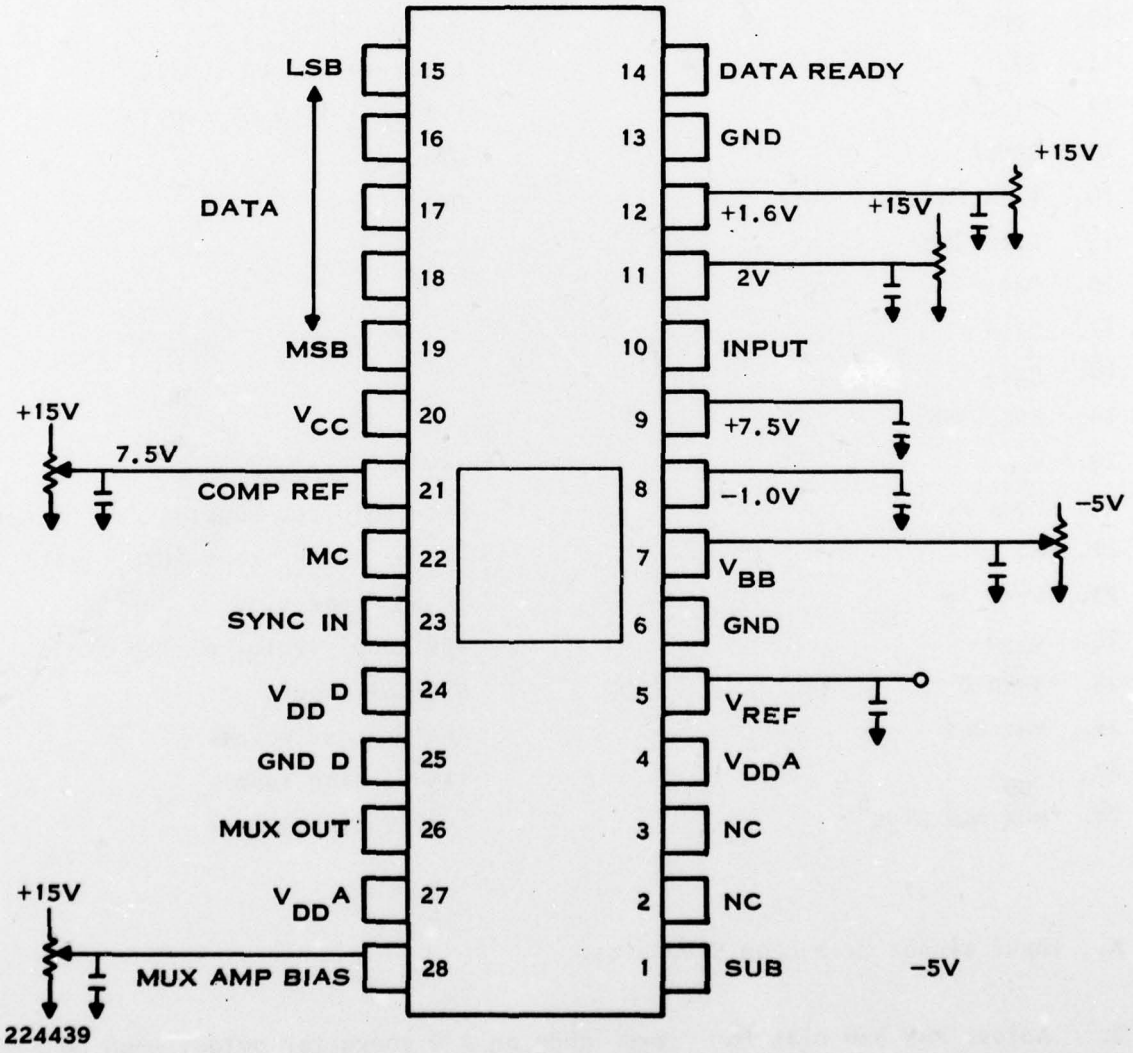

Figure A-1. Analyzer

TABLE A-1. ANALYZER PIN DESCRIPTION

	Name	Comment
1.	Sub	Substrate -5V supply
2.	NC	
3.	NC	
4.	V_{DD}[A]	Analog +15V
5.	V_{ref}	Generated on chip - Add .1μF
6.	GRNDA	Analog ground
7.	V_{BB}	Ext. - 2V supply
8.	-4,2	Internally generated - Add .1μF
9.	+7.5V	Internally generated - Add .1μF
10.	Input[A]	Analog speech input
11.	+2V	External +2V DC supply
12.	+1.6	External 1.6V DC supply
13.	GRNDA	Ground
14.	Data Ready	Output
15.	Data 2SB	
16.	Data	
17.	Data	
18.	Data	
19.	Data MSB	
20.	V_{CC}	+5V DC supply
21.	Comp Ref	External 7.5V supply
22.	MC	40 KHz clock input (DTL level)
23.	Sync In	50 Hz frame sync
24.	V_{DD} D	15V supply (digital logic)
25.	GRND D	Digital ground
26.	MUX OUT	Analog test point
27.	V_{DD}[A]	+15V analog supply
28.	MUX Amp Bias[B]	~7.5V bias adjust

A. Input signal 2V p-p on 5.0V bias.

B. Adjust Mux Amp bias for "zero" code on A/D converter output when no AC signal is input.

B. SYNTHESIZER

A description of the synthesizer pin functions is provided in Figure A-2 and Table A-2, as is the case for the analyzer. In the final form only one trimmer will be used. All other variable voltages will be fixed.

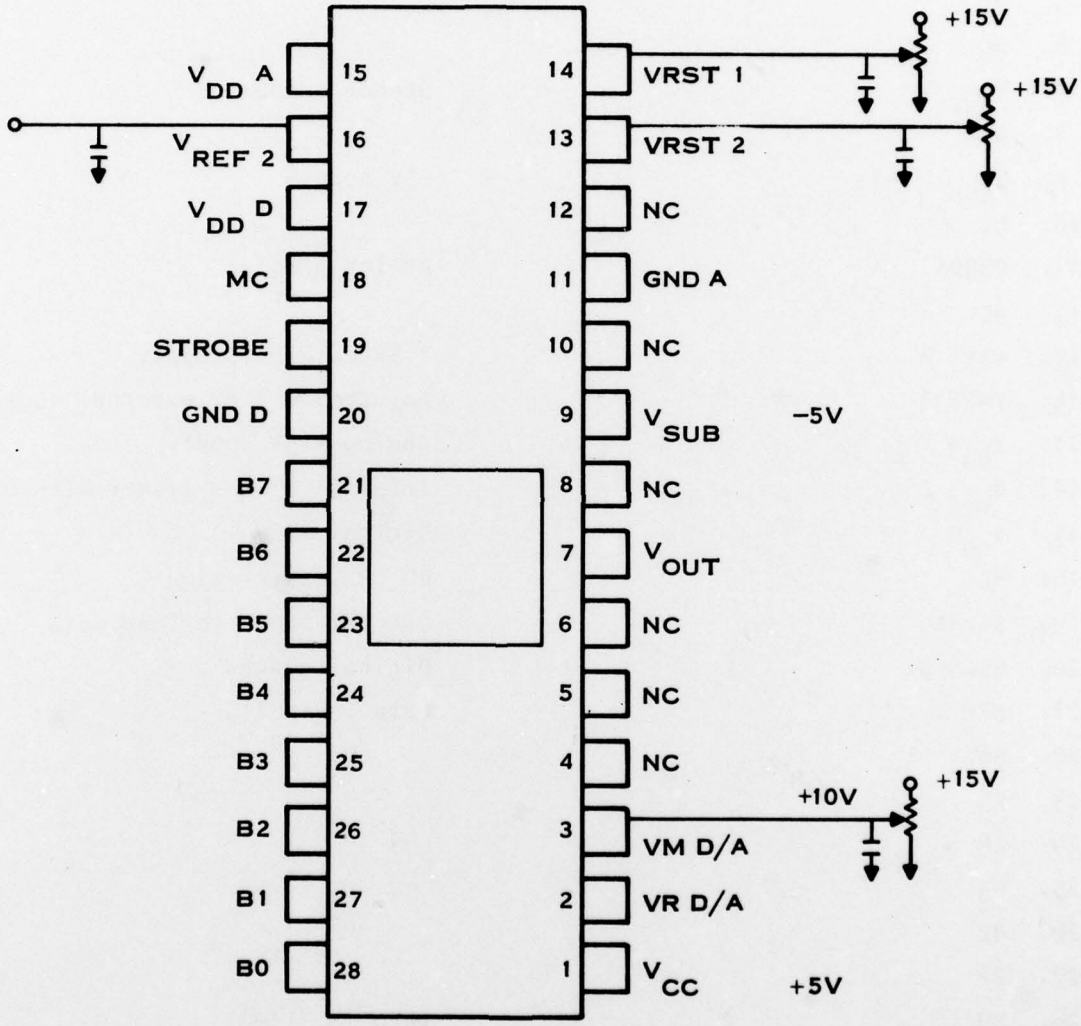

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Figure A-2. Synthesizer

TABLE A-2. SYNTHESIZER PIN DESCRIPTION

	Name	Comment
1.	V_{CC}	+5V logic supply
2.	VR D/A	Ground
3.	VM D/A	+10V D/A reference
4.	NC	
5.	NC	
6.	NC	
7.	V_{OUT}	Speech output
8.	NC	
9.	V_{SUB}	-5V supply
10.	NC	
11.	GRNDA	Analog ground
12.	NC	
13.	VRST 2	7.5V external supply
14.	VRST 1	Adjustable 7.5V external supply
15.	$V_{DD}{}^{A}$	Analog +15V supply
16.	V_{ref} 2	Internal bias - filter with 0.1μF
17.	$V_{DD}{}^{D}$	Digital +15V
18.	MC	40 kHz master clock
19.	Strobe	Digital input to load data
20.	GRND D	Digital ground
21.	B7	Data in (MSB)
22.	B6	"
23.	B5	"
24.	B4	"
25.	B3	"
26.	B2	"
27.	B1	"
28.	B0	Data In (LSB)